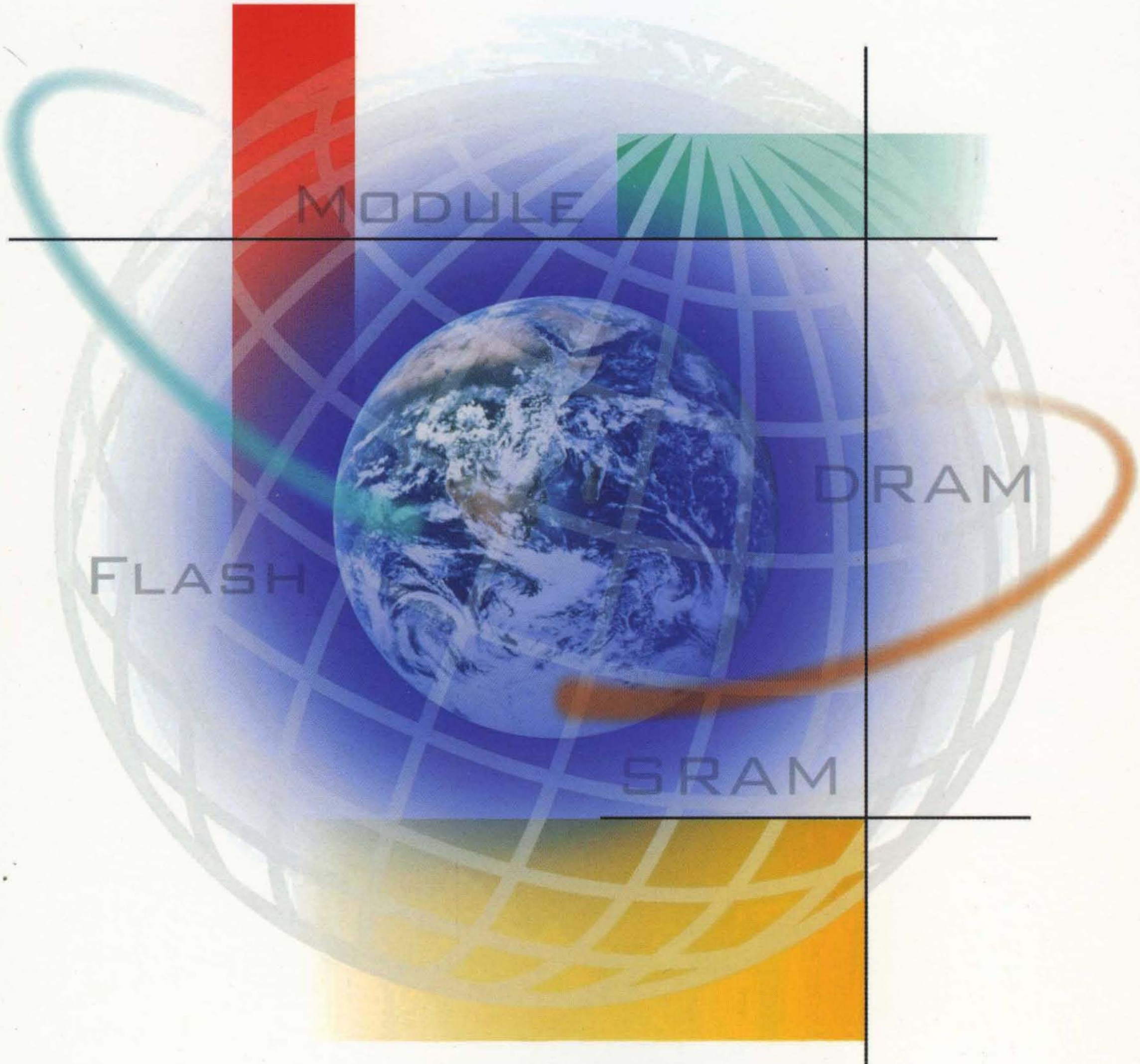
1999 DATA BOOK



A World Memory Leader

MICRON®

MICRON
TECHNOLOGY, INC.

MEMORY DATA BOOK

8000 S. Federal Way
P.O. Box 6
Boise, Idaho 83707-0006
Telephone: 208-368-3900
Fax: 208-368-4617
E-mail: prodmktg@micron.com
Internet: www.micron.com/mti
Customer Comment Line:
U.S.A. 800-932-4992
Fax 01-208-368-5018

Printed in the U.S.A.

PREFACE PAGE

DDR/SLDRAM/RDRAM PAGE

SDRAM PAGE

2KR .... 2,048 Refresh
8KR .... 8,192 Refresh
4KR .... 4,096 Refresh
S .... Optional Self Refresh on 16Mb SDRAMs (all other SDRAMs have Self Refresh)

*The 8 Meg x 8 DDR SDRAM data sheet is found in the DDR/SLDRAM/RDRAM section.

SGRAM PAGE

DDR .... Double Data Rate
SDR .... Single Data Rate

**The 512K x 32 DDR SGRAM data sheet is found in the DDR/SLDRAM/RDRAM section.

†The 2 Meg x 32 SDRAM data sheet is found in the SDRAM section.

EDO DRAM

EDO	Extended Data-Out
4KR	4,096 Refresh
S	Self Refresh
DC	Dual CAS
8KR	8,192 Refresh

FPM DRAM

FPM	FAST PAGE MODE
4KR	4,096 Refresh
S	Self Refresh
DC	Dual CAS
8KR	8,192 Refresh

SDRAM DIMM/SODIMM

SDRAM DIMM/SODIMM (continued)

SGRAM SODIMM

DRAM DIMM/SODIMM

N .... Nonbuffered   S .... Self Refresh

ZBT SRAM*

*All ZBT SRAMs have 3.3V supply voltage.
**The placeholder in the part number is replaced with an "L" for 3.3V I/O parts and a "V" for 2.5V I/O parts.

ZBT SRAM* (continued) PAGE

*All ZBT SRAMs have 3.3V supply voltage.
**The placeholder in the part number is replaced with an "L" for 3.3V I/O parts and a "V" for 2.5V I/O parts.

SYNCBURST SRAM† PAGE

SCD .... Single-Cycle Deselect DCD .... Double-Cycle Deselect

†All SyncBurst SRAMs have 3.3V supply voltage.
**The placeholder in the part number is replaced with an "L" for 3.3V I/O parts and a "V" for 2.5V I/O parts.

SYNCBURST SRAM† (continued)

SCD	Single-Cycle Deselect	DCD	Double-Cycle Deselect

†All SyncBurst SRAMs have 3.3V supply voltage.
**The placeholder in the part number is replaced with an "L" for 3.3V I/O parts and a "V" for 2.5V I/O parts.

BOOT BLOCK FLASH MEMORY

BB	Boot Block	AUTO	Automated W/E Algorithm
ET	Extended Temperature	V	Low Voltage
SVT	SmartVoltage Technology		

EVEN-SECTORED FLASH MEMORY

AUTO	Automated W/E Algorithm	SE	Even Sectored
DPD	Deep Power-Down		

FLASH CARDS

GENERAL TECHNICAL NOTES PAGE

DRAM TECHNICAL NOTES PAGE

SRAM TECHNICAL NOTES PAGE

SRAM TECHNICAL NOTES (continued) PAGE

FLASH TECHNICAL NOTES PAGE

PRODUCT RELIABILITY PAGE

PACKAGE INFORMATION PAGE

SALES AND SERVICE INFORMATION PAGE

IMPORTANT NOTICE

Micron Technology, Inc. (Micron), reserves the right to change products or specifications without notice. Customers are advised to obtain the latest versions of product specifications, which should be considered in evaluating a product's appropriateness for a particular use. There is no assurance that Micron's semiconductor products are appropriate for any application by a customer.

MICRON MAKES NO WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OTHER THAN COMPLIANCE WITH MICRON'S SPECIFICATION SHEET FOR THE PRODUCT AT THE TIME OF DELIVERY. IN NO EVENT SHALL MICRON BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES AS A RESULT OF THE PERFORMANCE, OR FAILURE TO PERFORM, OF ANY MICRON PRODUCT.

ANY CLAIM AGAINST MICRON MUST BE MADE WITHIN 90 DAYS FROM THE DATE OF SHIPMENT BY MICRON AND MICRON HAS NO LIABILITY THEREAFTER. Micron's liability is limited to replacement of defective product, or either Customer or Micron may elect refund of amounts paid in lieu of replacement. The warranty covers only defects arising under normal use and not malfunctions resulting from misuse, abuse, modification or repairs by anyone other than Micron.

MICRON'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS OR FOR USE IN OTHER CRITICAL APPLICATIONS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF MICRON. Life support devices or systems are those which are intended to support or sustain life and whose failure to perform can be reasonably expected to result in a significant injury or death to the user. Critical components are those whose failure to perform can be reasonably expected to cause failure of a life support device or system or affect its safety or effectiveness. Critical applications are those applications that may involve potential risk of death, personal injury, or severe property or environmental damage.

MICRON DOES NOT WARRANT PRODUCT TO BE FREE OF CLAIMS OF PATENT, COPYRIGHT, TRADEMARK, OR ANY OTHER INTELLECTUAL PROPERTY INFRINGEMENT BY ANY THIRD PARTY AND DISCLAIMS ANY SUCH WARRANTY OR INDEMNIFICATION AGAINST SUCH INFRINGEMENT.

Micron's terms and conditions of sale may be changed at any time without notice. Warranties may vary based on product type. Current warranty information will be included in Micron's confirmation statements.

Dear Customer:

Micron Technology, Inc., is dedicated to the design, manufacture and marketing of high-quality, highly reliable memory components. Our corporate mission is:

"To be the most efficient and innovative global provider of semiconductor memory solutions."

At Micron, we are investing time, talent and resources to bring you the finest DRAMs, SRAMs, Flash and other specialty memory products. We have developed a unique intelligent burn-in system, AMBYX™, which evaluates and reports the quality level of each and every component we produce.

We are dedicated to continuous improvement of all our products and services. This means continual reduction of electrical and mechanical defect levels. It also means the addition of new services such as bonded inventory, on-line forecasting and electronic data interchange programs. And when you have a design or application question, you can get the answers you need from our World Wide Web site (www.micron.com/mti) or by contacting one of Micron's Applications Engineers.

We're proud of our products, our progress and our performance. And we're pleased that you're choosing Micron as your memory supplier.

The Micron Team

ADVANTAGES

Micron Technology, Inc. (Micron), brings quality, productivity and innovation together to provide advantages for our customers. Our products feature some of the industry's fastest speeds. And we establish delivery standards based on customer expectations, including JIT programs, made possible by ever-increasing product reliability.

MEMORY PRODUCTS

Micron is working to provide customers with the widest range of memory products available anywhere. Our product line includes PC100, PC133 and double data rate (DDR) synchronous DRAM, as well as higher speed graphics RAM and higher density synchronous SRAM products. Micron's flash memory line offers boot block flash, sectored erase flash and flash cards. For the future, Micron plans production of both RDRAM® and SLDRAM packet-based architectures.

DIE SALES

In addition to our durable packaging, Micron is one of the leaders in the industry in bare die. Demand for die is increasing for use in highly specialized applications. Micron's bare die products are available in 8-inch wafers and Gel-Pak.

INTERNET ACCESS

One visit to Micron's Web site will confirm that customer satisfaction continues to be a priority. We have dedicated significant resources to our Internet site in an effort to make complete product and service information readily available to our customers. Current data sheets are on line and ready for immediate access. Detailed information on our DRAM, RDRAM, DDR SDRAM, SDRAM, SLDRAM, SGRAM, SRAM, Module, Die and Flash offerings are provided to help our customers in selecting, ordering and obtaining the appropriate Micron device for their designs.

From our Web site, you can quickly look up Micron part numbers, identify local sales representatives and distributors, obtain product availability information or receive technical assistance from one of our Applications Engineers.

From products and service, to technology, to company news and employment—all of the information you need is at your fingertips.

Use the Internet to reach any Micron contact as well. All you need is the individual's "username" and you have the address: username@micron.com. It's that simple. Visit the Micron Web site or contact us by e-mail.

QUALITY

Quality is the most important thing we provide to our customers with each Micron shipment. That's because we believe that quality must be internalized consistently at each level of our company. We provide every Micron team member with the training and motivation needed to make Micron's quality philosophy a reality.

One way we have measurably improved both productivity and product quality is through our own quality improvement program formed by individuals throughout the company. Micron quality teams get together to address a wide range of issues within their areas. We consistently and regularly perform a company-wide self-assessment based on the Malcolm Baldrige National Quality Award criteria. We've also implemented statistical process controls to evaluate every facet of the memory design, fabrication, assembly and shipping process. And our AMBYX intelligent burn-in and test system* gives Micron a unique edge in product reliability.

These quality programs have resulted in Micron becoming one of the first U.S. semiconductor manufacturers to receive ISO 9001 certification. ISO 9001 is the most comprehensive level of certification in the internationally recognized ISO family of specifications. The certification confirms that Micron's systems for accepting orders, reviewing customers' specifications, manufacturing and testing products, and delivering those products to our customers are quality controlled and produce consistent results.

*For more information on AMBYX, see Section 5.

ABOUT THIS BOOK

CONTENT

Micron's 1999 *Memory Data Book* provides abbreviated data sheets on Micron's line of DRAMs, SRAMs and Flash Memory. For the most up-to-date, full-length data sheets, please visit our Web site at www.micron.com/mti or call he Micron Literature Room at 208-368-3900.

SECTION ORGANIZATION

Micron's 1999 *Memory Data Book* contains a detailed Table of Contents with a sequential index of products, as well as product selection guides at the beginning of each section. The *Data Book* is organized into seven sections:

- Section 1: DRAM selection guide and DRAM component and module data sheets.
- Section 2: SRAM selection guide and SRAM data sheets.
- Section 3: Flash Memory selection guide and Flash data sheets.
- Section 4: DRAM, SRAM and Flash technical notes.
- Section 5: Summary of Micron's unique quality and reliability programs and testing operation, including our AMBYX intelligent burn-in and test system.*
- Section 6: Package information for DRAM, SRAM and Flash memory components and for DRAM modules.
- Section 7: Customer service notes and sales information, including part numbering guides and a list of sales representatives and distributors worldwide.

DATA SHEET SEQUENCE

Data sheets in this book are ordered first by width and second by depth. For example, the ZBT SRAM section begins with the 128K x 18, followed by all other x18 configurations in order of ascending depth.

DATA SHEET DESIGNATIONS

As detailed in the table below, each Micron product data sheet is classified as either Advance, Preliminary (indicated on the top of each data sheet) or Final (final data sheets have no marking).

SURVEY

We have included a removable, postage-paid survey form in the front of this book. Your time in completing and returning this survey will enhance our efforts to continually improve our product literature.

For more information on Micron product literature, or to order additional copies of this publication, contact:

Micron Semiconductor Products, Inc.
8000 S. Federal Way
P.O. Box 6
Boise, ID 83707-0006
Phone: 208-368-3900
Fax: 208-368-4617
E-mail: prodmktg@micron.com
Customer Comment Line: 800-932-4992
Customer Comment Fax: 01-208-368-5018

DATA SHEET DESIGNATIONS

DATA SHEET MARKING	DEFINITION
Advance	This data sheet contains initial descriptions of products still under development.
Preliminary	This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.
No Marking	This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

NOTE: Micron uses acronyms to refer to certain industry-standard-setting bodies. These are defined below:
EIA/JEDEC—Electronics Industry Association/Joint Electron Device Engineering Council
PCMCIA—Personal Computer Memory Card International Association

Micron's *Quality/Reliability Handbook* is available by calling 208-368-3900.

DDR/SLDRAM/RDRAM PRODUCT SELECTION GUIDE

Product	Memory Configuration	Part Number	Voltage	Clock[1] (MHz)	Data Rate	Package/No. of Pins			Page
						FBGA	TSOP	TQFP	
DDR SDRAM	16 Meg x 4	MT46V16M4	2.5V	100, 133	2x	–	66	–	1-3
DDR SDRAM	32 Meg x 4	MT46V32M4	2.5V	100, 133	2x	–	66	–	1-7
DDR SDRAM	64 Meg x 4	MT46V64M4	2.5V	100, 133	2x	–	66	–	1-9
DDR SDRAM	8 Meg x 8	MT46V8M8	2.5V	100, 133	2x	–	66	–	1-3
DDR SDRAM	16 Meg x 8	MT46V16M8	2.5V	100, 133	2x	–	66	–	1-7
DDR SDRAM	32 Meg x 8	MT46V32M8	2.5V	100, 133	2x	–	66	–	1-9
DDR SDRAM	4 Meg x 16	MT46V4M16	2.5V	100, 133	2x	–	66	–	1-3
DDR SDRAM	8 Meg x 16	MT46V8M16	2.5V	100, 133	2x	–	66	–	1-7
DDR SDRAM	16 Meg x 16	MT46V16M16	2.5V	100, 133	2x	–	66	–	1-9
RDRAM	8 Meg x 18	MT6V8M18	2.5V	300, 400	2x	54	–	–	1-13
SLDRAM	8 Meg x 18	MT49V8M18C	2.5V	400	2x	TBD	–	–	1-11
DDR SGRAM	512K x 32	MT45V512K32	2.5V	150, 167	2x	–	–	100	1-1
DDR SDRAM	2 Meg x 32	MT46V2M32	2.5V	150, 167	2x	–	–	100	1-5

NOTE: 1. DDR SDRAM (x4, x8, x16) clock rate at CAS latency of 2.
DDR SGRAM (x32) clock rate at CAS latency of 3.
DDR SDRAM (x32) clock rate at CAS latency of 3.

DOUBLE DATA RATE SGRAM

MT45V512K32 – 128K x 32 x 4 banks

For the latest data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional, intermittent data strobe (DQS) transmitted/received with data and used in capturing data at the receiver
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CLK and CLK#)
- DLL to align DQ and DQS transitions with CLK transitions (JEDEC mode only)
- Commands entered on each positive CLK edge; data referenced to both edges of DQS
- Four internal banks for concurrent operation: 128K x 32 x 4 banks, with 9 row- and 8 column-address bits per bank
- Burst lengths: 2, 4, 8 or full page
- Auto precharge option for each burst access
- 16-column BLOCK WRITE
- BYTE WRITE operation (masking via DM0-3)
- Auto Refresh and Self Refresh Modes
- 16ms, 2,048-cycle auto refresh (7.8µs/cycle)
- 2.5V (SSTL_2 compatible) I/O
- +2.5V ±0.2V V_{DD}, +2.5V ±0.2V $V_{DD}Q$
- Same footprint as 2 Meg x 32 DDR SDRAM

OPTIONS

OPTIONS	MARKING
Timing - JEDEC Mode Cycle Time (Clock Frequency)	
6ns (≤ 167 MHz) @ CL = 3	-6
6.5ns (≤ 150 MHz) @ CL = 3	-65
Plastic Package	
100-pin TQFP (0.65mm lead pitch)	LG
100-pin TQFP, Reverse Bend	RG

- Part Number Example: MT45V512K32LG-6

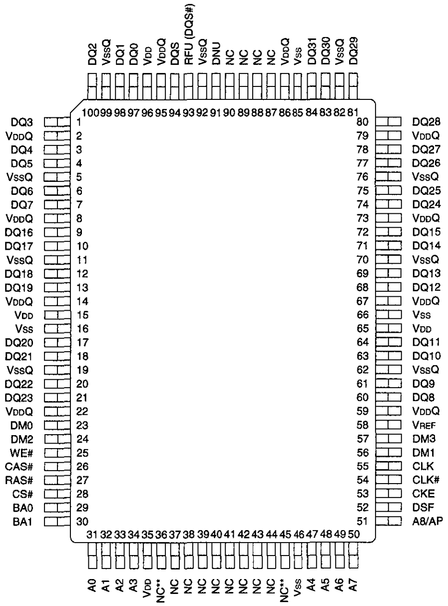
KEY TIMING PARAMETERS (JEDEC Mode)

SPEED GRADE	CLOCK FREQUENCY (1/^{t}CK)		ACCESS TIME	DQ-DQS SKEW
	CL = 2*	CL = 3*		
-6	111 MHz	167 MHz	±0.1 ^{t}CK	±0.075 ^{t}CK
-65	100 MHz	150 MHz	±0.1 ^{t}CK	±0.075 ^{t}CK

*CL = CAS (READ) latency

PIN ASSIGNMENT (Top View) 100-Pin TQFP† (Normal Bend Shown)

(D-1)



	512K x 32
Configuration	128K x 32 x 4 banks
Refresh Count	2K
Row Addressing	512 (A0-A8)
Bank Addressing	4 (BA0, BA1)
Column Addressing	256 (A0-A7)

**Reserved for 2 Meg x 32 DDR addressing
†JEDEC standard MS-026 BHA (LQFP)

16Mb DDR SGRAM PART NUMBERS

PART NUMBER	ARCHITECTURE
MT45V512K32LG	512K x 32
MT45V512K32RG	512K x 32

NOTE

This device provides dual-mode operation: JEDEC mode and non-JEDEC mode. The recommended mode of operation for higher performance and/or more robust timing is the JEDEC mode. Accordingly, this document focuses primarily on the JEDEC mode of operation. The non-JEDEC mode differences are noted as exceptions in the text, and the non-JEDEC mode timing diagrams are included in Appendix I in the full-length version of this data sheet.

The device defaults to the non-JEDEC mode upon power-up to accommodate controllers designed for that mode of operation only. The device enters the JEDEC mode of operation when the DLL is enabled, via a LOAD MODE REGISTER command to the extended mode register. Once in the JEDEC mode, the device remains in that mode until powered down.

Note that the DLL may be disabled after entering JEDEC mode, but this mode of operation is provided for test and debug purposes only. Specifications unique to this mode of operation are not guaranteed.

GENERAL DESCRIPTION

The 16Mb DDR SGRAM is a high-speed CMOS, dynamic random-access memory containing 16,777,216 bits. It is internally configured as a quad-bank DRAM, with each 4,194,304-bit bank organized as 512 rows by 256 columns by 32 bits.

The 16Mb DDR SGRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$ prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 16Mb DDR SGRAM consists of a single 64-bit, one-clock-cycle data transfer at the internal DRAM core and two corresponding 32-bit, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transferred externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SGRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The 16Mb DDR SGRAM operates from a differential clock: CLK and CLK# (the crossing of CLK going HIGH and CLK# going LOW will be referred to as the positive edge of CLK). Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CLK.

Read and write accesses to the DDR SGRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ, WRITE or BLOCK WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A8 select the row). The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SGRAM provides for programmable READ or WRITE burst lengths of 2, 4 or 8 locations, or the full page. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

As with standard SGRAMs, the pipelined, multibank architecture of DDR SGRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

DDR SGRAMs differ from DDR SDRAMs in configuration and by providing 16-column BLOCK WRITE and full-page burst capability. The quad-bank pipelined architecture combined with the additional graphics functions results in a device particularly well suited to high-performance graphics applications or other high-bandwidth applications.

The 16Mb DDR SGRAM is designed to operate in 2.5V, low-power memory systems. An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

DOUBLE DATA RATE SDRAM

MT46V16M4 - 4 Meg x 4 x 4 banks
MT46V8M8 - 2 Meg x 8 x 4 banks
MT46V4M16 - 1 Meg x 16 x 4 banks

For the latest data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

EATURES

- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional, intermittent data strobe (DQS) transmitted/received with data and used in capturing data at the receiver
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CLK and CLK#)
- DLL to align DQ and DQS transitions with CLK transitions
- Commands entered on each positive CLK edge; data referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4 or 8
- Auto precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- 64ms, 4,096-cycle refresh
- 2.5V (SSTL_2 compatible) I/O
- +2.5V ±0.2V VDD, +2.5V ±0.2V VDDQ

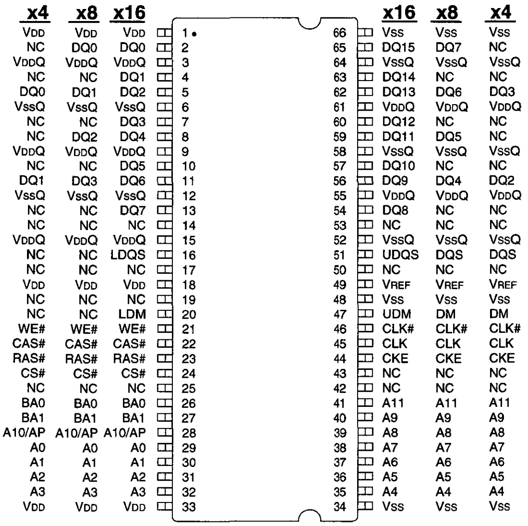
PTIONS — MARKING

Configuration	
16 Meg x 4 (4 Meg x 4 x 4 banks)	16M4
8 Meg x 8 (2 Meg x 8 x 4 banks)	8M8
4 Meg x 16 (1 Meg x 16 x 4 banks)	4M16
Plastic Package	
66-pin TSOP (400 mil width, 0.65mm pin pitch)	TG
Timing - Cycle Time	
7.5ns @ CL = 2	-75
10ns @ CL = 2	-10

Part Number Example: MT46V8M8TG-75

PIN ASSIGNMENT (Top View)

66-Pin TSOP
(C-6)



x4	x8	x16	Pin	Pin	x16	x8	x4
VDD	VDD	VDD	1	66	Vss	Vss	Vss
NC	DQ0	DQ0	2	65	DQ15	DQ7	NC
VDDQ	VDDQ	VDDQ	3	64	VssQ	VssQ	VssQ
NC	NC	DQ1	4	63	DQ14	NC	NC
DQ0	DQ1	DQ2	5	62	DQ13	DQ6	DQ3
VssQ	VssQ	VssQ	6	61	VDDQ	VDDQ	VDDQ
NC	NC	DQ3	7	60	DQ12	NC	NC
NC	DQ2	DQ4	8	59	DQ11	DQ5	NC
VDDQ	VDDQ	VDDQ	9	58	VssQ	VssQ	VssQ
NC	NC	DQ5	10	57	DQ10	NC	NC
DQ1	DQ3	DQ6	11	56	DQ9	DQ4	DQ2
VssQ	VssQ	VssQ	12	55	VDDQ	VDDQ	VDDQ
NC	NC	DQ7	13	54	DQ8	NC	NC
NC	NC	NC	14	53	NC	NC	NC
VDDQ	VDDQ	VDDQ	15	52	VssQ	VssQ	VssQ
NC	NC	LDQS	16	51	UDQS	DQS	DQS
NC	NC	NC	17	50	NC	NC	NC
VDD	VDD	VDD	18	49	VREF	VREF	VREF
NC	NC	NC	19	48	Vss	Vss	Vss
NC	NC	LDM	20	47	UDM	DM	DM
WE#	WE#	WE#	21	46	CLK#	CLK#	CLK#
CAS#	CAS#	CAS#	22	45	CLK	CLK	CLK
RAS#	RAS#	RAS#	23	44	CKE	CKE	CKE
CS#	CS#	CS#	24	43	NC	NC	NC
NC	NC	NC	25	42	NC	NC	NC
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
VDD	VDD	VDD	33	34	Vss	Vss	Vss

	16 Meg x 4	8 Meg x 8	4 Meg x 16
Configuration	4 Meg x 4 x 4 banks	2 Meg x 8 x 4 banks	1 Meg x 16 x 4 banks
Refresh Count	4K	4K	4K
Row Addressing	4K (A0-A11)	4K (A0-A11)	4K (A0-A11)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	1K (A0-A9)	512 (A0-A8)	256 (A0-A7)

EY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY (1/^{t}CK)	
	CL = 2*	CL = 2.5*
-75	133 MHz	150 MHz
-10	100 MHz	133 MHz

L = CAS (READ) latency

64Mb DDR SDRAM PART NUMBERS

PART NUMBER	ARCHITECTURE
MT46V16M4TG	16 Meg x 4
MT46V8M8TG	8 Meg x 8
MT46V4M16TG	4 Meg x 16

GENERAL DESCRIPTION

The 64Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864 bits. It is internally configured as a quad-bank DRAM.

The 64Mb DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n* prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 64Mb DDR SDRAM effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The 64Mb DDR SDRAM operates from a differential clock: CLK and CLK# (the crossing of CLK going HIGH and CLK# going LOW will be referred to as the positive edge of CLK). Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CLK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

DOUBLE DATA RATE SDRAM

MT46V2M32 - 512K x 32 x 4 banks

For the latest data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional, intermittent data strobe (DQS) transmitted/received with data, to be used in capturing data at the receiver
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CLK and CLK#)
- DLL to align DQ and DQS transitions with CLK transitions
- Commands entered on each positive CLK edge; data referenced to both edges of DQS
- Four internal banks for concurrent operation: 512K x 32 x 4 banks, with 11 row- and 8 column-address bits per bank
- BYTE WRITE operation (masking via DM0-3)
- Burst lengths: 2, 4, 8 or full page
- Auto precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- 32ms, 2,048-cycle refresh
- 2.5V (SSTL_2 compatible) I/O
- +2.5V ±0.2V VDD, +2.5V ±0.2V VDDQ

OPTIONS MARKING

OPTIONS	MARKING
Configuration	
2 Meg x 32 (512K x 32 x 4 banks)	2M32
Plastic Package	
100-pin TQFP (0.65mm lead pitch)	LG
100-pin TQFP, Reverse Bend	RG**
Timing - Cycle Time	
6ns (≤ 167 MHz) @ CL = 3	-6
6.5ns (≤ 150 MHz) @ CL = 3	-65

Part Number Example: MT46V2M32LG-6

KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY ($1/{}^tCK$)	
	CL = 2*	CL = 3*
-6	111 MHz	167 MHz
-65	100 MHz	150 MHz

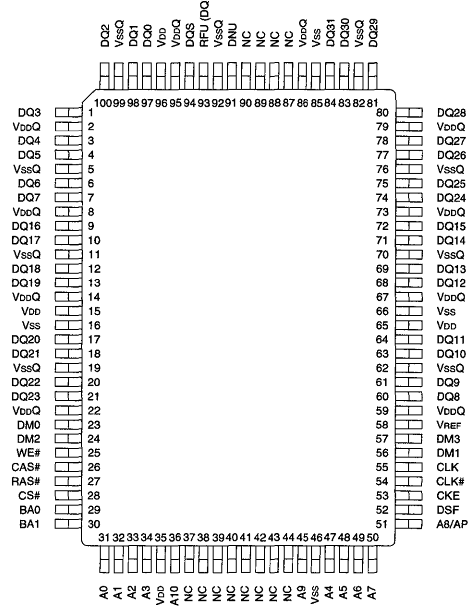
CL = CAS (READ) latency

Contact factory for offering

PIN ASSIGNMENT (Top View)

100-Pin TQFP†
(Normal Bend Shown)

(D-1)



	2 Meg x 32
Configuration	512K x 32 x 4 banks
Refresh Count	2K
Row Addressing	2K (A0-A10)
Bank Addressing	4 (BA0, BA1)
Column Addressing	256 (A0-A7)

†JEDEC standard MS-026 BHA (LQFP)

64Mb (x32) DDR SDRAM PART NUMBER

PART NUMBER	ARCHITECTURE
MT46V2M32LG	2 Meg x 32

GENERAL DESCRIPTION

The 64Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864 bits. It is internally configured as a quad-bank DRAM.

The 64Mb DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n* prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 64Mb DDR SDRAM effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The 64Mb DDR SDRAM operates from a differential clock: CLK and CLK# (the crossing of CLK going HIGH and CLK# going LOW will be referred to as the postive edge of CLK). Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CLK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, 8 or full page. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

DOUBLE DATA RATE SDRAM

MT46V32M4 - 8 Meg x 4 x 4 banks
MT46V16M8 - 4 Meg x 8 x 4 banks
MT46V8M16 - 2 Meg x 16 x 4 banks

For the latest data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

EATURES

- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional, intermittent data strobe (DQS) transmitted/received with data and used in capturing data at the receiver
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CLK and CLK#)
- DLL to align DQ and DQS transitions with CLK transitions
- Commands entered on each positive CLK edge; data referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4 or 8
- Auto precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- 64ms, 4,096-cycle refresh
- 2.5V (SSTL_2 compatible) I/O
- +2.5V ±0.2V V_{DD}, +2.5V ±0.2V $V_{DD}Q$

PTIONS MARKING

Configuration	
32 Meg x 4 (8 Meg x 4 x 4 banks)	32M4
16 Meg x 8 (4 Meg x 8 x 4 banks)	16M8
8 Meg x 16 (2 Meg x 16 x 4 banks)	8M16
Plastic Package	
66-pin TSOP (400 mil width, 0.65mm pin pitch)	TG
Timing - Cycle Time	
7.5ns @ CL = 2	-75
10ns @ CL = 2	-10

Part Number Example: MT46V16M8TG-75

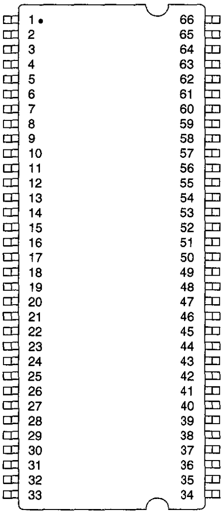
EY TIMING PARAMETERS

SPEED RADE	CLOCK FREQUENCY (1/t_{CK})	
	CL = 2*	CL = 2.5*
-75	133 MHz	150 MHz
-10	100 MHz	133 MHz

= CAS (READ) latency

PIN ASSIGNMENT (Top View)

66-Pin TSOP
(C-6)



x4	x8	x16			x16	x8	x4
V_{DD}	V_{DD}	V_{DD}	1	66	V_{SS}	V_{SS}	V_{SS}
NC	DQ0	DQ0	2	65	DQ15	DQ7	NC
$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$	3	64	$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$
NC	NC	DQ1	4	63	DQ14	NC	NC
DQ0	DQ1	DQ2	5	62	DQ13	DQ6	DQ3
$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$	6	61	$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$
NC	NC	DQ3	7	60	DQ12	NC	NC
NC	DQ2	DQ4	8	59	DQ11	DQ5	NC
$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$	9	58	$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$
NC	NC	DQ5	10	57	DQ10	NC	NC
DQ1	DQ3	DQ6	11	56	DQ9	DQ4	DQ2
$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$	12	55	$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$
NC	NC	DQ7	13	54	DQ8	NC	NC
NC	NC	NC	14	53	NC	NC	NC
$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$	15	52	$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$
NC	NC	LDQS	16	51	UDQS	DQS	DQS
NC	NC	NC	17	50	NC	NC	NC
V_{DD}	V_{DD}	V_{DD}	18	49	V_{REF}	V_{REF}	V_{REF}
NC**	NC**	NC**	19	48	V_{SS}	V_{SS}	V_{SS}
NC	NC	LDM	20	47	UDM	DM	DM
WE#	WE#	WE#	21	46	CLK#	CLK#	CLK#
CAS#	CAS#	CAS#	22	45	CLK	CLK	CLK
RAS#	RAS#	RAS#	23	44	CKE	CKE	CKE
CS#	CS#	CS#	24	43	NC	NC	NC
NC	NC	NC	25	42	NC	NC	NC
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
V_{DD}	V_{DD}	V_{DD}	33	34	V_{SS}	V_{SS}	V_{SS}

**The definition of a QFC# signal for this pin is pending.

	32 Meg x 4	16 Meg x 8	8 Meg x 16
Configuration	8 Meg x 4 x 4 banks	4 Meg x 8 x 4 banks	2 Meg x 16 x 4 banks
Refresh Count	4K	4K	4K
Row Addressing	4K (A0-A11)	4K (A0-A11)	4K (A0-A11)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	2K (A0-A9, A11)	1K (A0-A9)	512 (A0-A8)

128Mb DDR SDRAM PART NUMBERS

PART NUMBER	ARCHITECTURE
MT46V32M4TG	32 Meg x 4
MT46V16M8TG	16 Meg x 8
MT46V8M16TG	8 Meg x 16

GENERAL DESCRIPTION

The 128Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,217,728 bits. It is internally configured as a quad-bank DRAM.

The 128Mb DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n* prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 128Mb DDR SDRAM effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The 128Mb DDR SDRAM operates from a differential clock: CLK and CLK# (the crossing of CLK going HIGH and CLK# going LOW will be referred to as the positive edge of CLK). Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CLK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burs access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2 Class II compatible.

DOUBLE DATA RATE SDRAM

MT46V64M4 - 16 Meg x 4 x 4 banks
MT46V32M8 - 8 Meg x 8 x 4 banks
MT46V16M16 - 4 Meg x 16 x 4 banks

For the latest data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional, intermittent data strobe (DQS) transmitted/received with data, to be used in capturing data at the receiver
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CLK and CLK#)
- DLL to align DQ and DQS transitions with CLK transitions
- Commands entered on each positive CLK edge; data referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4 or 8
- Auto precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- 64ms, 4,096-cycle refresh
- 2.5V (SSTL_2 compatible) I/O
- +2.5V ±0.2V VDD, +2.5V ±0.2V VDDQ

OPTIONS — MARKING

OPTIONS	MARKING
Configuration	
64 Meg x 4 (16 Meg x 4 x 4 banks)	64M4
32 Meg x 8 (8 Meg x 8 x 4 banks)	32M8
16 Meg x 16 (4 Meg x 16 x 4 banks)	16M16
Plastic Package	
66-pin TSOP (400 mil width, 0.65mm pin pitch)	TG
Timing - Cycle Time	
7.5ns @ CL = 2	-75
10ns @ CL = 2	-10

Part Number Example: MT46V32M8TG-75

KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY (1/^{t}CK)	
	CL = 2*	CL = 2.5*
-75	133 MHz	150 MHz
-10	100 MHz	133 MHz

L = CAS (READ) latency

PIN ASSIGNMENT (Top View)

66-Pin TSOP

(C-6)

x4	x8	x16	Pin	Pin	x16	x8	x4
VDD	VDD	VDD	1	66	VSS	VSS	VSS
NC	DQ0	DQ0	2	65	DQ15	DQ7	NC
VDDQ	VDDQ	VDDQ	3	64	VSSQ	VSSQ	VSSQ
NC	NC	DQ1	4	63	DQ14	NC	NC
DQ0	DQ1	DQ2	5	62	DQ13	DQ6	DQ3
VSSQ	VSSQ	VSSQ	6	61	VDDQ	VDDQ	VDDQ
NC	NC	DQ3	7	60	DQ12	NC	NC
NC	DQ2	DQ4	8	59	DQ11	DQ5	NC
VDDQ	VDDQ	VDDQ	9	58	VSSQ	VSSQ	VSSQ
NC	NC	DQ5	10	57	DQ10	NC	NC
DQ1	DQ3	DQ6	11	56	DQ9	DQ4	DQ2
VSSQ	VSSQ	VSSQ	12	55	VDDQ	VDDQ	VDDQ
NC	NC	DQ7	13	54	DQ8	NC	NC
NC	NC	NC	14	53	NC	NC	NC
VDDQ	VDDQ	VDDQ	15	52	VSSQ	VSSQ	VSSQ
NC	NC	LDQS	16	51	UDQS	DQS	DQS
NC	NC	NC	17	50	NC	NC	NC
VDD	VDD	VDD	18	49	VREF	VREF	VREF
NC**	NC**	NC**	19	48	VSS	VSS	VSS
NC	NC	LDM	20	47	UDM	DM	DM
WE#	WE#	WE#	21	46	CLK#	CLK#	CLK#
CAS#	CAS#	CAS#	22	45	CLK	CLK	CLK
RAS#	RAS#	RAS#	23	44	CKE	CKE	CKE
CS#	CS#	CS#	24	43	NC	NC	NC
NC	NC	NC	25	42	A12	A12	A12
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
VDD	VDD	VDD	33	34	VSS	VSS	VSS

**The definition of a QFC# signal for this pin is pending.

	64 Meg x 4	32 Meg x 8	16 Meg x 16
Configuration	16 Meg x 4 x 4 banks	8 Meg x 8 x 4 banks	4 Meg x 16 x 4 banks
Refresh Count	4K	4K	4K
Row Addressing	4K (A0-A11)	4K (A0-A11)	4K (A0-A11)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	4K (A0-A9, A11-A12)	2K (A0-A9, A11)	1K (A0-A9)

256Mb DDR SDRAM PART NUMBERS

PART NUMBER	ARCHITECTURE
MT46V64M4TG	64 Meg x 4
MT46V32M8TG	32 Meg x 8
MT46V16M16TG	16 Meg x 16

GENERAL DESCRIPTION

The 256Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM.

The 256Mb DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n* prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The 256Mb DDR SDRAM operates from a differential clock: CLK and CLK# (the crossing of CLK going HIGH and CLK# going LOW will be referred to as the positive edge of CLK). Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CLK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

800 Mb/s/pin SLDRAM

MT49V8M18C - 4 Meg x 18 x 2 banks

For the latest data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

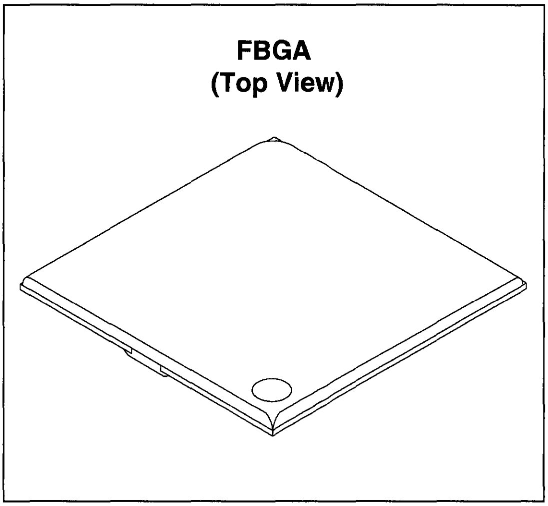
FEATURES

- Very high speed 400 MHz clock rate with 800 MHz data rate
- 1.6 GB/s peak I/O bandwidth for very high bandwidth over narrow system memory bus
- Pipelined (concurrent) operation for up to four transactions
- Two-bank, 16-segment buffer architecture for hiding row access and precharge time
- Data burst lengths of 4 or 8
- Command packet length of 4
- Packet-oriented protocol for pin compatibility across multiple densities
- Auto Refresh and Self Refresh Modes
- Command clock for commands and addresses; bidirectional data clocks for read and write data
- Dual data clocks for smooth handoff from one data source to another
- Programmable offset between data and data clocks
- Programmable READ delays, adjustable in coarse increments equal to one data bit time, and fine increments which are a fraction of a bit time; allow for specific temporal placement of data at the memory controller data pins
- Programmable WRITE delays, adjustable in coarse increments equal to one data bit time; allow for optimally adjusted write data temporal placement by the memory controller
- 64ms, 8,192-cycle refresh
- SLIO Interface Technology
  Drivers: calibrated V_{OH} and V_{OL} levels
  Receivers: narrow setup and hold windows
- Single +2.5V ±0.2V power supply

OPTIONS

OPTIONS	MARKING
• Timing 400 MHz data rate	-4Z
• Package FBGA	F

- Part Number Example: MT49V8M18CF-4Z



FBGA (Top View)

GENERAL DESCRIPTION

The 144Mb SLDRAM is a synchronous, very high-speed, packet-oriented, pipelined dynamic random-access memory ontaining 150,994,944 bits. The 144Mb SLDRAM is internally configured as two banks of 1 Meg x 72; each of the 1 Meg x 72 banks is organized as 8,192 rows by 128 columns by 72 bits. Each row is further divided into four segments, which are 32 columns by 72 bits each.

The banks are accessed indirectly through the use of intermediate storage buffers (segment buffers). Data is transferred between a segment buffer and a bank via PREFETCH and RESTORE operations (for a PREFETCH, data moves from the bank to the segment buffer; for a RESTORE, data moves in the opposite direction). The size of the data word for these internal transfers is equal to one segment (32 x 72 bits). Data is transferred between a segment buffer and the I/O interface via READ and WRITE operations. A READ or WRITE burst of four involves the data of one column in the selected segment buffer. For a burst of eight, two columns are accessed. The 72 bits per column access are transferred over the I/O interface in a burst of four 18-bit words.

All transactions begin with a request packet. PREFETCH, RESTORE, READ and WRITE request packets contain the specific command and address information required. A row must be opened (activated) prior to a PREFETCH or RESTORE, and a row must be closed (precharged) prior to opening another row in the same bank. Request packets for combinations of commands are supported (e.g. ROW OPEN and PREFETCH, PREFETCH and READ, WRITE and RESTORE, etc.). PREFETCH and RESTORE requests

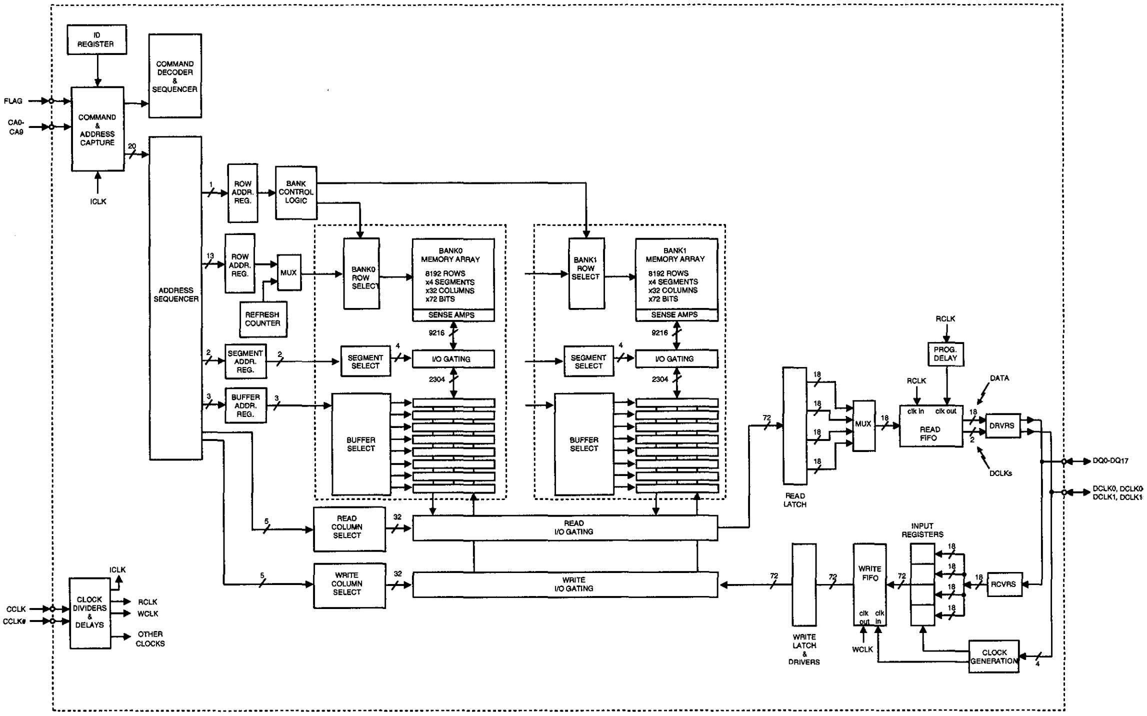
GENERAL DESCRIPTION (continued)

indicate whether to leave the row open after the access or to perform a self-timed precharge at the completion of the access (auto precharge).

The buffered architecture of 144Mb SLDRAM results in enhanced system performance in the form of lower average latency per access, more efficient bus utilization and reduced power consumption, while at the same time achieving an 800 Mb/s/pin (or 1.6 GB/s) data rate. This performance is provided in a cost-effective manner due to the reduction in the number of internal banks and related redundant logic, and the decoupling of I/O interface frequency from core frequency.

The 144Mb SLDRAM is designed to operate in 2.5V memory systems. An auto refresh mode is provided along with two power-saving modes: standby and shutdown. Self refresh is provided in the shutdown mode. The 144Mb SLDRAM includes SLIO, an adaptive, very high-speed, interface technology.

FUNCTIONAL BLOCK DIAGRAM



DIRECT RAMBUS™ DRAM

MT6V8M18 - 256K x 18 x 32 banks

For the latest data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

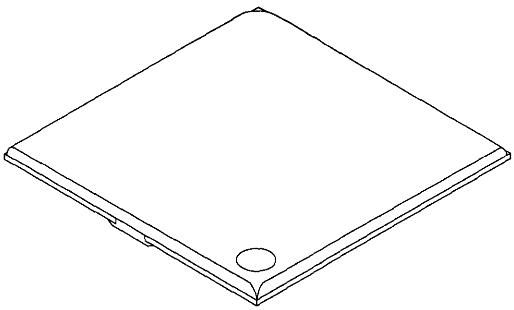
- High-speed 300 MHz and 400 MHz clocks with 2x data rates
- 1.6 GB/s peak I/O bandwidth
- Rambus signaling level (RSL) using differential 300 MHz and 400 MHz transmit and receive clocks
- Packet-oriented Rambus protocol transmitted in 8-bit-long packets
- Separate control (8 bit) and data (18 bit) buses for increased data bandwidth capability
- Control bus with separate row (3 bit) and column (5 bit) buses for easier command scheduling
- Programmable output delay timing for round-trip delay of 1 to 5 cycles
- Support for up to four simultaneous transactions (within bank restrictions)
- Write buffer to reduce READ latency
- Three precharge mechanisms for controller flexibility
- Programmable power states for flexibility in power consumption versus data access time
- Power-down self-refresh and active refresh
- Organization: 1KB pages and 32 banks, x18 organization
- Chip-scale package (CSP) FBGA
- 32ms, 16,384 cycle refresh
- 2.5V power supply with 1.8V CMOS supply for I/Os

PTIONS	MARKING
Configuration	
8 Meg x 18	8M18
Package	
FBGA	F
Timing (Cycle Time)	
300 MHz Clock Rate, Access Time = 53ns	-3A
300 MHz Clock Rate, Access Time = 45ns	-3C
400 MHz Clock Rate, Access Time = 50ns	-4B
400 MHz Clock Rate, Access Time = 45ns	-4C
400 MHz Clock Rate, Access Time = 40ns	-4D

ENERAL DESCRIPTION

The MT6V8M18 Direct RDRAM® is a general-purpose, gh-performance, packet-oriented dynamic randomess memory containing 150,994,944 bits. The MT6V8M18 nternally configured as 32 banks of 32K x 144; each of the K x 144 banks is organized as 512 rows by 64 columns by 144 bits. The 144 bits are serially multiplexed onto the RDRAM's I/O pins as eight 18-bit words.

54-Bump FBGA (Top View)



PART NUMBERS

PART NUMBER	ORGANIZATION[1]	CLK FREQ. (MHz)	ACCESS TIME (ns)
MT6V8M18F-3A	256K x 18 x 32s	300	53
MT6V8M18F-3C[2]	256K x 18 x 32s	300	45
MT6V8M18F-4B	256K x 18 x 32s	400	50
MT6V8M18F-4C[2]	256K x 18 x 32s	400	45
MT6V8M18F-4D[2]	256K x 18 x 32s	400	40

NOTE: 1. The "32s" designation indicates that this RDRAM core is composed of 32 banks which use a "split" bank architecture.
2. These speed grades may not be available on initial product and are provided for future design-in support. Please contact the factory for availability.

The MT6V8M18 uses Rambus signaling level (RSL) technology to achieve 300 MHz or 400 MHz clock speeds using differential clocks. Control and I/O data is transferred on both rising and falling edges of the clock. This allows data transfers at 1.25ns per two bytes (10ns per 16 bytes) during peak operation.

All DRAM commands are communicated to the MT6V8M18 through a 3-bit row or 5-bit column bus in

GENERAL DESCRIPTION (continued)

packets which are 8 bits in length. These packets are then decoded on the RDRAM into the operation and address requiring access.

Initialization and mode configuration for the MT6V8M18 are accessed through slow speed CMOS Serial I/O interface.

The architecture of Direct RDRAMs allows high sustained bandwidth memory transactions for multiple, simultaneous, semi-random addresses. The Direct RDRAM's thirty-two banks can support up to four simultaneous transactions (within bank restrictions).

System-oriented features include power management, byte masking and x18 organization. The two data bits in the x18 organization are general and can be used for additional storage and bandwidth, or for error correction.

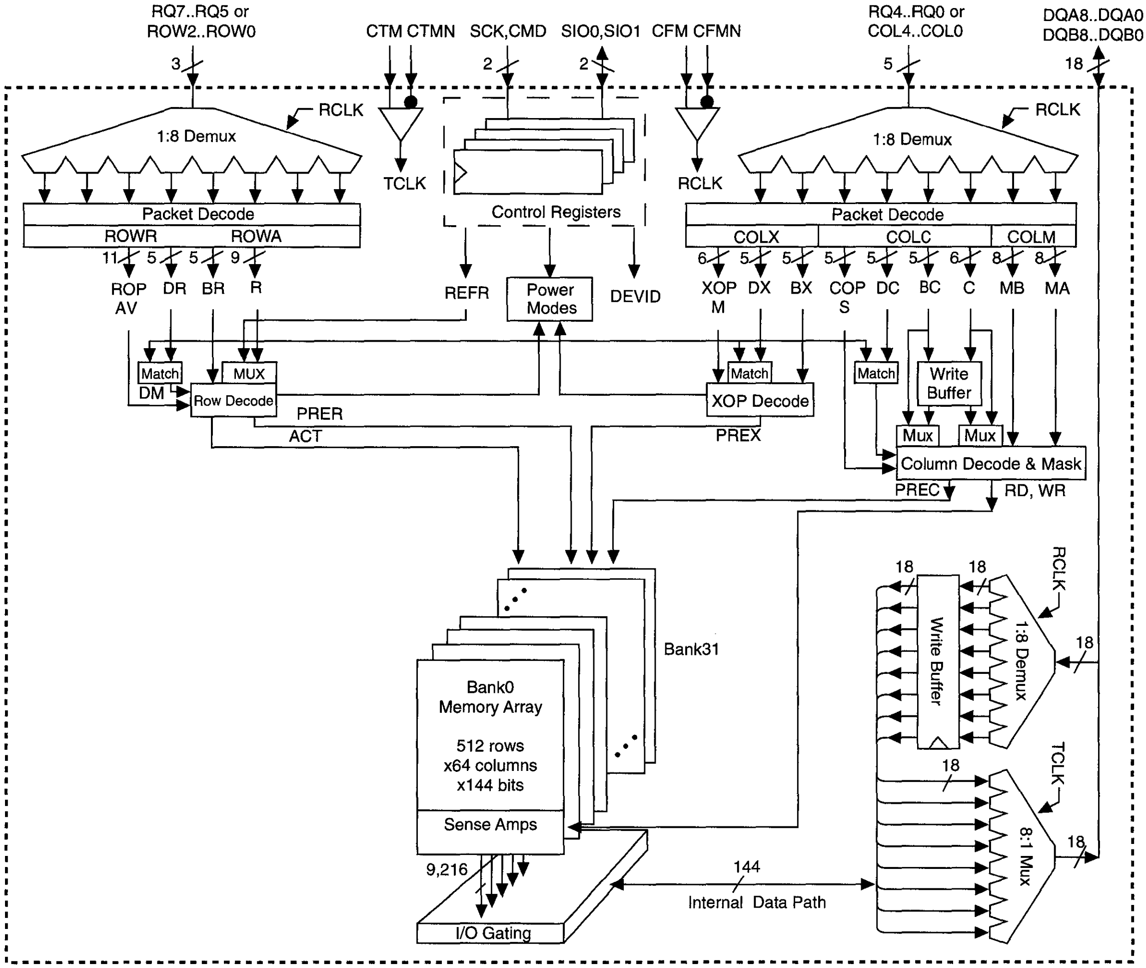
DEVICE PINOUT

The bump layout table below shows the pin assignments of the center-bonded RDRAM package from the top side of the package (the view looking down on the package as it is mounted on the circuit board). The MT6V8M18 is available in an FBGA chip-scale package.

FBGA BUMP LAYOUT
(Top View)

10	DQA7	DQA4	CFM	CFMN	RQ5	RQ3	DQB0	DQB4	DQB7
9	GND	V_{DD}	GND	GNDa	V_{DD}	GND	V_{DD}	V_{DD}	GND
8	CMD	DQA5	DQA2	V_{DD}a	RQ6	RQ2	DQB1	DQB5	SIO1
7									
6									
5									
4									
3	SCK	DQA6	DQA1	V_{REF}	RQ7	RQ1	DQB2	DQB6	SIO0
2	V_{CMOS}	GND	V_{DD}	GND	GND	V_{DD}	GND	GND	V_{CMOS}
1	DQA8	DQA3	DQA0	CTMN	CTM	RQ4	RQ0	DQB3	DQB8
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**J**

FUNCTIONAL BLOCK DIAGRAM



DRAM 1

SDRAM PRODUCT SELECTION GUIDE

Memory Configuration	Options	Part Number	Maximum Clock Frequency (MHz)	Package/No. of Pins	Page
				TSOP	
16 Meg x 4	4KR	MT48LC16M4A2	133, 125	54	1-17
32 Meg x 4	4KR	MT48LC32M4A2	133, 125	54	1-25
64 Meg x 4	8KR	MT48LC64M4A2	143, 133, 125	54/66**	1-33
8 Meg x 8	4KR	MT48LC8M8A2	133, 125	54	1-17
8 Meg x 8*	4KR, 2.5V I/O	MT46V8M8	150, 133, 100	66	1-3
16 Meg x 8	4KR	MT48LC16M8A2	133, 125	54	1-25
32 Meg x 8	8KR	MT48LC32M8A2	143, 133, 125	54/66**	1-33
1 Meg x 16	2KR, 4KR, S	MT48LC1M16A1 S	166, 143, 125	50	1-41
4 Meg x 16	4KR	MT48LC4M16A2	133, 125	54	1-17
8 Meg x 16	4KR	MT48LC8M16A2	133, 125	54	1-25
16 Meg x 16	8KR	MT48LC16M16A2	143, 133, 125	54/66**	1-33
2 Meg x 32	4KR	MT48LC2M32B2	166, 143, 125	86	1-45

2KR = 2,048 Refresh; 4KR = 4,096 Refresh; 8KR = 8,192 Refresh; S = Optional Self Refresh on 16Mb SDRAMs (all other SDRAMs have Self Refresh)

*The 8 Meg x 8 DDR SDRAM data sheet is found in the DDR/SLDRAM/RDRAM section.
**The 66-pin TSOP package is under consideration.

SYNCHRONOUS DRAM

MT48LC16M4A2 -4 Meg x 4 x 4 banks
MT48LC8M8A2 - 2 Meg x 8 x 4 banks
MT48LC4M16A2 -1 Meg x 16 x 4 banks

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- PC100-compliant, includes CONCURRENT AUTO PRECHARGE; PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Modes: standard and low power
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

OPTIONS

OPTIONS	MARKING
• Configurations	
16 Meg x 4 (4 Meg x 4 x 4 banks)	16M4
8 Meg x 8 (2 Meg x 8 x 4 banks)	8M8
4 Meg x 16 (1 Meg x 16 x 4 banks)	4M16
• WRITE Recovery (^{t}WR)	
^{t}WR = 1 CLK (No longer supported.)	A1
^{t}WR = 2 CLK	A2
• Plastic Package - OCPL*	
54-pin TSOP (400 mil)	TG
• Timing (Cycle Time)	
7.5ns (133 MHz)	-75
8ns (125 MHz)	-8E
10ns (100 MHz)	-10
• Self Refresh	
Standard	None
Low Power	L†

- Part Number Example: MT48LC8M8A2TG-8E

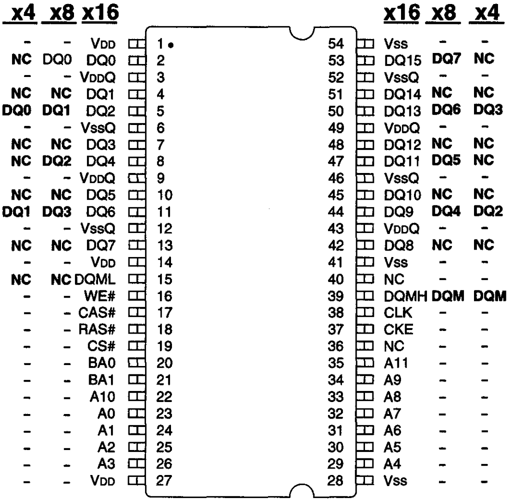
KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2**	CL = 3**		
-75	133 MHz	–	5.4ns	1.8ns	0.8ns
-8E	125 MHz	–	6ns	2ns	1ns
-10	100 MHz	–	7ns	3ns	1ns
-8E	100 MHz	6ns	–	2ns	1ns
-10	66 MHz	9ns	–	3ns	1ns

Off-center parting line
*CL = CAS (READ) latency
Contact factory for availability

PIN ASSIGNMENT (Top View)

54-Pin TSOP
(C-5)



x4	x8	x16	Pin	Pin	x16	x8	x4
-	-	VDD	1	54	Vss	-	-
NC	DQ0	DQ0	2	53	DQ15	DQ7	NC
-	-	VDDQ	3	52	VssQ	-	-
NC	NC	DQ1	4	51	DQ14	NC	NC
DQ0	DQ1	DQ2	5	50	DQ13	DQ6	DQ3
-	-	VssQ	6	49	VDDQ	-	-
NC	NC	DQ3	7	48	DQ12	NC	NC
NC	DQ2	DQ4	8	47	DQ11	DQ5	NC
-	-	VDDQ	9	46	VssQ	-	-
NC	NC	DQ5	10	45	DQ10	NC	NC
DQ1	DQ3	DQ6	11	44	DQ9	DQ4	DQ2
-	-	VssQ	12	43	VDDQ	-	-
NC	NC	DQ7	13	42	DQ8	NC	NC
-	-	VDD	14	41	Vss	-	-
NC	NC	DQML	15	40	NC	-	-
-	-	WE#	16	39	DQMH	DQM	DQM
-	-	CAS#	17	38	CLK	-	-
-	-	RAS#	18	37	CKE	-	-
-	-	CS#	19	36	NC	-	-
-	-	BA0	20	35	A11	-	-
-	-	BA1	21	34	A9	-	-
-	-	A10	22	33	A8	-	-
-	-	A0	23	32	A7	-	-
-	-	A1	24	31	A6	-	-
-	-	A2	25	30	A5	-	-
-	-	A3	26	29	A4	-	-
-	-	VDD	27	28	Vss	-	-

Note: The # symbol indicates signal is active LOW. A dash (–) indicates x8 and x4 pin function is same as x16 pin function.

	16 Meg x 4	8 Meg x 8	4 Meg x 16
Configuration	4 Meg x 4 x 4 banks	2 Meg x 8 x 4 banks	1 Meg x 16 x 4 banks
Refresh Count	4K	4K	4K
Row Addressing	4K (A0-A11)	4K (A0-A11)	4K (A0-A11)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	1K (A0-A9)	512 (A0-A8)	256 (A0-A7)

64Mb SDRAM PART NUMBERS

PART NUMBER	ARCHITECTURE
MT48LC16M4A2TG	16 Meg x 4
MT48LC8M8A2TG	8 Meg x 8
MT48LC4M16A2TG	4 Meg x 16

GENERAL DESCRIPTION

The 64Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 16,777,216-bit banks is organized as 4,096 rows by 1,024 columns by 4 bits. Each of the x8's 16,777,216-bit banks is organized as 4,096 rows by 512 columns by 8 bits. Each of the x16's 16,777,216-bit banks is organized as 4,096 rows by 256 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 64Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

The 64Mb SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.

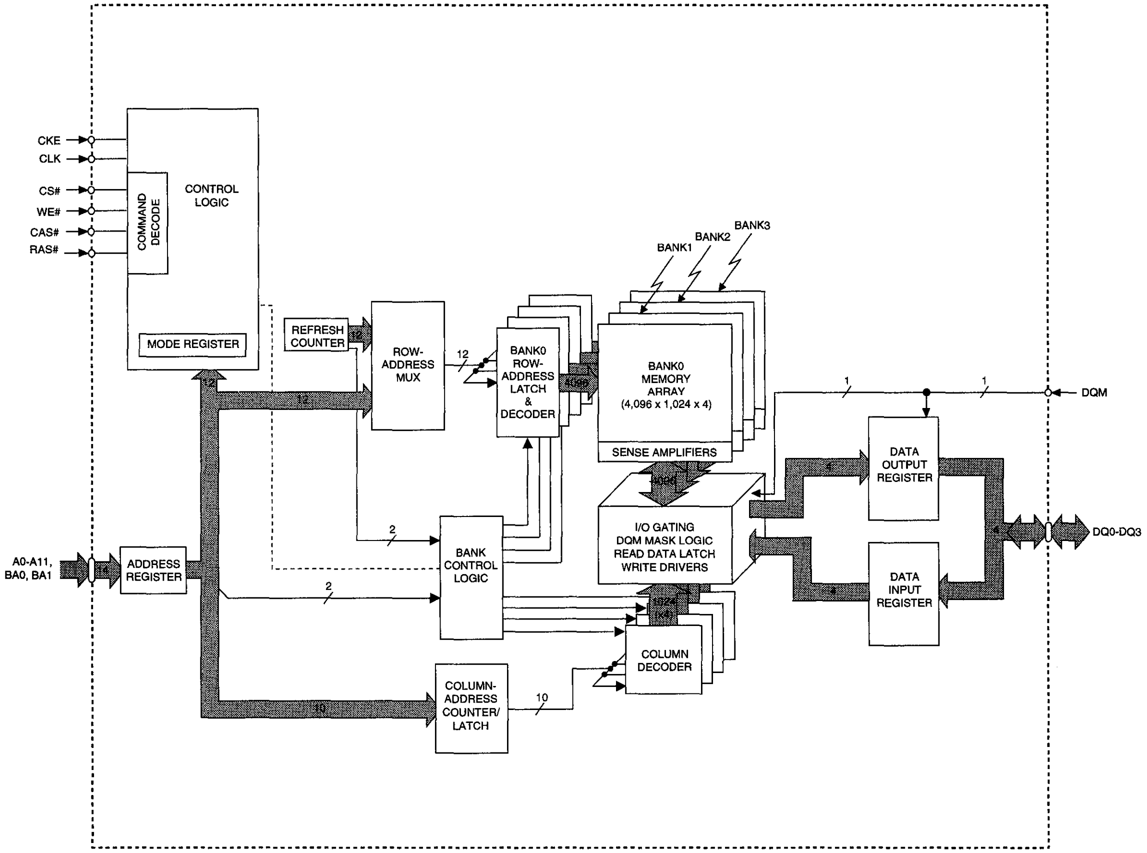
TABLE OF CONTENTS (for full data sheet)

Timing Waveforms

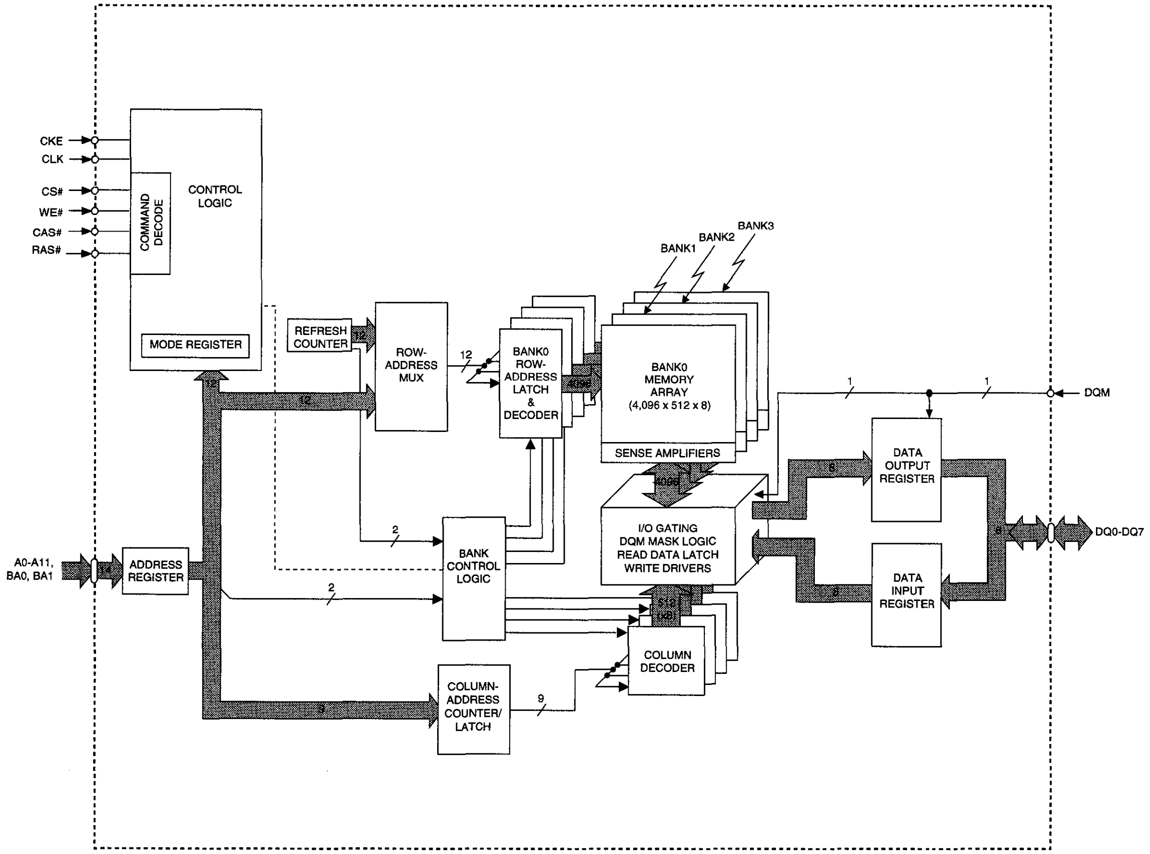
  Reads

  Writes

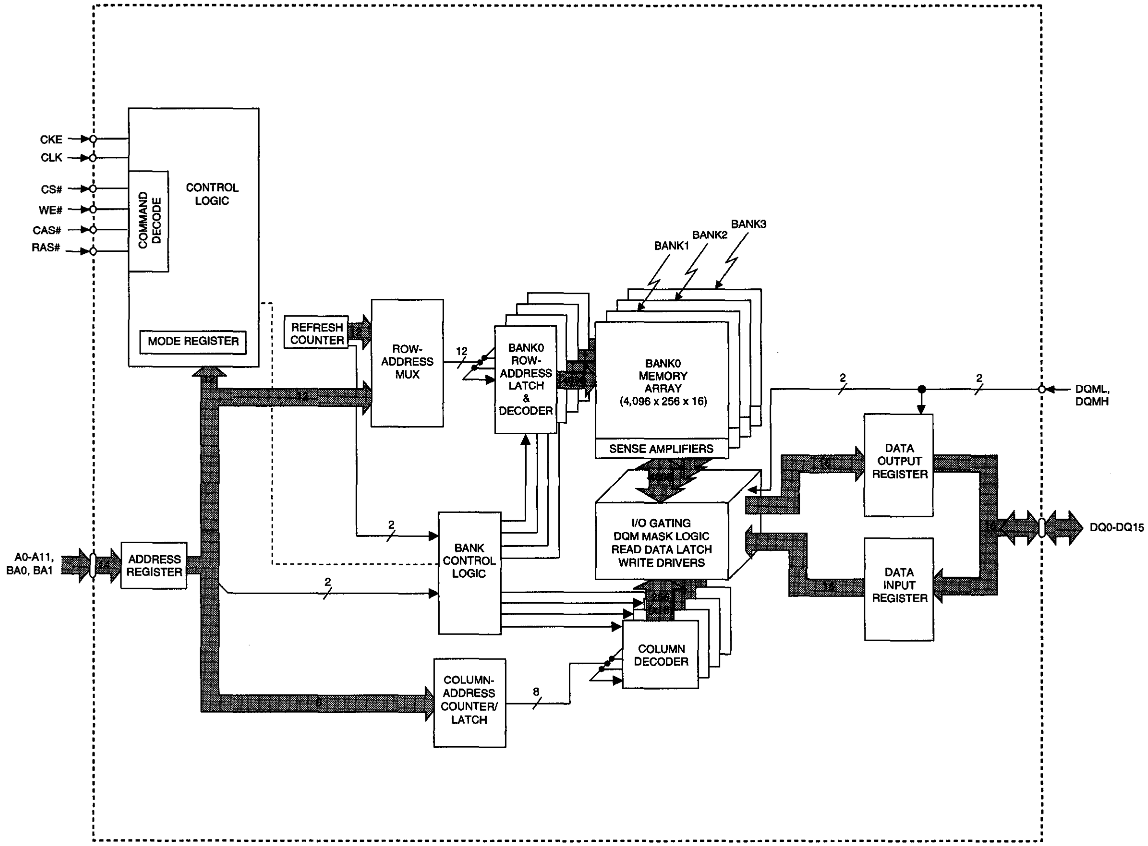
FUNCTIONAL BLOCK DIAGRAM
16 Meg x 4 SDRAM



FUNCTIONAL BLOCK DIAGRAM
8 Meg x 8 SDRAM



FUNCTIONAL BLOCK DIAGRAM
4 Meg x 16 SDRAM



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
38	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
37	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
19	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
16, 17, 18	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
39	x4, x8: DQM	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. On the x4 and x8, DQML (Pin 15) is a NC and DQMH is DQM. On the x16, DQML corresponds to DQ0-DQ7 and DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.
15, 39	x16: DQML, DQMH		
20, 21	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
23-26, 29-34, 22, 35	A0-A11	Input	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column-address A0-A9 [x4]; A0-A8 [x8]; A0-A7 [x16]; with A10 defining AUTO PRECHARGE) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 4, 5, 7, 8, 10, 11, 13, 42, 44, 45, 47, 48, 50, 51, 53	DQ0-DQ15	x16: I/O	Data Input/Output: Data bus for x16 (4, 7, 10, 13, 42, 45, 48, 51 are NCs for x8; and 2, 4, 7, 8, 10, 13, 42, 45, 47, 48, 51, 53 are NCs for x4).
2, 5, 8, 11, 44, 47, 50, 53	DQ0-DQ7	x8: I/O	Data Input/Output: Data bus for x8 (2, 8, 47, 53 are NCs for x4).
5, 11, 44, 50	DQ0-DQ3	x4: I/O	Data Input/Output: Data bus for x4.
36, 40	NC	–	No Connect: These pins should be left unconnected.
3, 9, 43, 49	$V_{DD}Q$	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
6, 12, 46, 52	$V_{SS}Q$	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 14, 27	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
28, 41, 54	V_{SS}	Supply	Ground.

SYNCHRONOUS DRAM

MT48LC32M4A2 - 8 Meg x 4 x 4 banks
MT48LC16M8A2 - 4 Meg x 8 x 4 banks
MT48LC8M16A2 - 2 Meg x 16 x 4 banks

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

EATURES

- PC100-compliant, includes CONCURRENT AUTO PRECHARGE; PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

PTIONS MARKING

Configurations	
32 Meg x 4 (8 Meg x 4 x 4 banks)	32M4
16 Meg x 8 (4 Meg x 8 x 4 banks)	16M8
8 Meg x 16 (2 Meg x 16 x 4 banks)	8M16
WRITE Recovery (ᵗWR)	
ᵗWR = 1 CLK (No longer supported.)	A1
ᵗWR = 2 CLK	A2
Plastic Package - OCPL*	
54-pin TSOP (400 mil)	TG
Timing (Cycle Time)	
7.5ns (133 MHz)	-75
8ns (125 MHz)	-8E
8ns (125 MHz)	-8C

Part Number Example: MT48LC16M8A2TG-8E

EY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2**	CL = 3**		
-75	133 MHz	–	5.4ns	1.8ns	0.8ns
-8E	125 MHz	–	6ns	2ns	1ns
-8C	125 MHz	–	6ns	2ns	1ns
-8E	100 MHz	6ns	–	2ns	1ns
-8C	83 MHz	9ns	–	2ns	1ns

ff-center parting line
CL = CAS (READ) latency

PIN ASSIGNMENT (Top View)

54-Pin TSOP
(C-5)

x4	x8	x16	Pin	Pin	x16	x8	x4
-	-	VDD	1•	54	VSS	-	-
NC	DQ0	DQ0	2	53	DQ15	DQ7	NC
-	-	VDDQ	3	52	VSSQ	-	-
NC	NC	DQ1	4	51	DQ14	NC	NC
DQ0	DQ1	DQ2	5	50	DQ13	DQ6	DQ3
-	-	VSSQ	6	49	VDDQ	-	-
NC	NC	DQ3	7	48	DQ12	NC	NC
NC	DQ2	DQ4	8	47	DQ11	DQ5	NC
-	-	VDDQ	9	46	VSSQ	-	-
NC	NC	DQ5	10	45	DQ10	NC	NC
DQ1	DQ3	DQ6	11	44	DQ9	DQ4	DQ2
-	-	VSSQ	12	43	VDDQ	-	-
NC	NC	DQ7	13	42	DQ8	NC	NC
-	-	VDD	14	41	VSS	-	-
NC	NC	DQML	15	40	NC	-	-
-	-	WE#	16	39	DQMH	DQM	DQM
-	-	CAS#	17	38	CLK	-	-
-	-	RAS#	18	37	CKE	-	-
-	-	CS#	19	36	NC	-	-
-	-	BA0	20	35	A11	-	-
-	-	BA1	21	34	A9	-	-
-	-	A10	22	33	A8	-	-
-	-	A0	23	32	A7	-	-
-	-	A1	24	31	A6	-	-
-	-	A2	25	30	A5	-	-
-	-	A3	26	29	A4	-	-
-	-	VDD	27	28	VSS	-	-

Note: The # symbol indicates signal is active LOW. A dash (–) indicates x8 and x4 pin function is same as x16 pin function.

	32 Meg x 4	16 Meg x 8	8 Meg x 16
Configuration	8 Meg x 4 x 4 banks	4 Meg x 8 x 4 banks	2 Meg x 16 x 4 banks
Refresh Count	4K	4K	4K
Row Addressing	4K (A0-A11)	4K (A0-A11)	4K (A0-A11)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	2K (A0-A9, A11)	1K (A0-A9)	512 (A0-A8)

128Mb SDRAM PART NUMBERS

PART NUMBER	ARCHITECTURE
MT48LC32M4A2TG	32 Meg x 4, ᵗWR = 2 CLK
MT48LC16M8A2TG	16 Meg x 8, ᵗWR = 2 CLK
MT48LC8M16A2TG	8 Meg x 16, ᵗWR = 2 CLK

GENERAL DESCRIPTION

The 128Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,217,728 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 33,554,432-bit banks is organized as 4,096 rows by 2,048 columns by 4 bits. Each of the x8's 33,554,432-bit banks is organized as 4,096 rows by 1,024 columns by 8 bits. Each of the x16's 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence

The 128Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

The 128Mb SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.

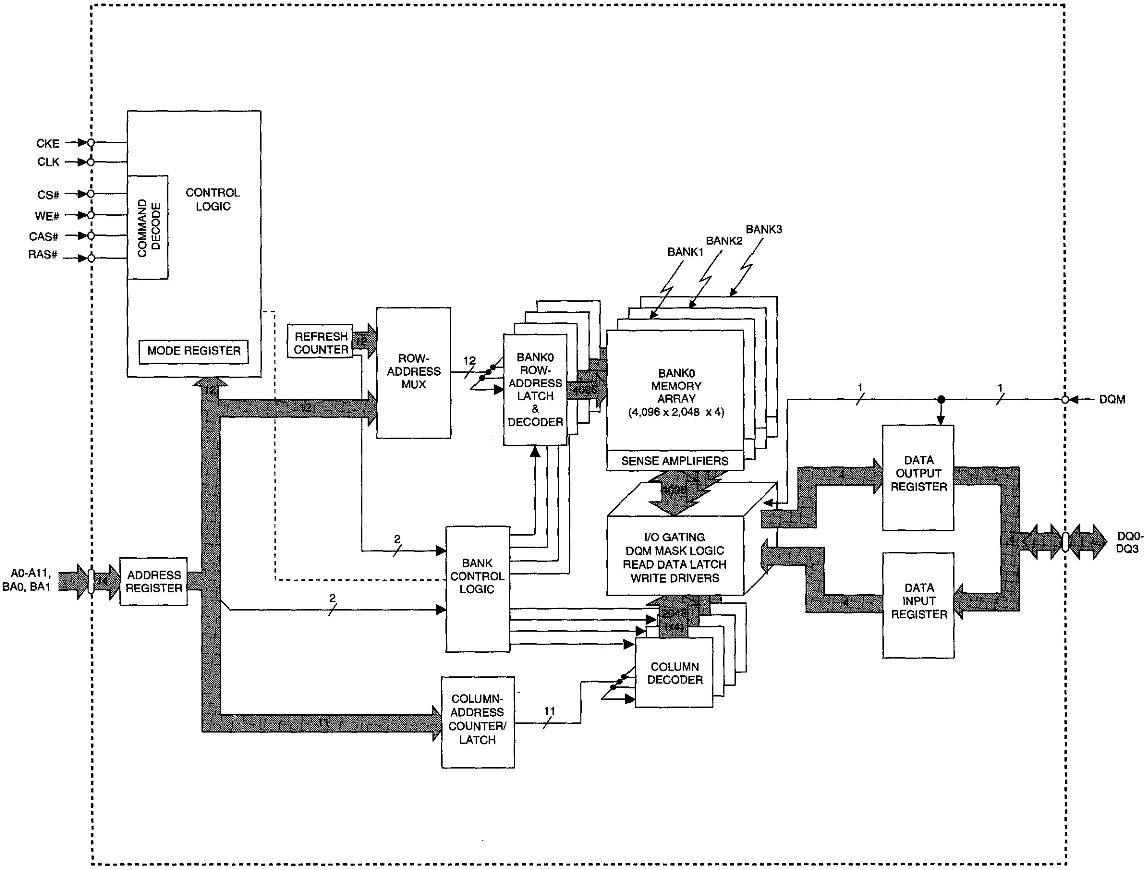
TABLE OF CONTENTS (for full data sheet)

Timing Waveforms

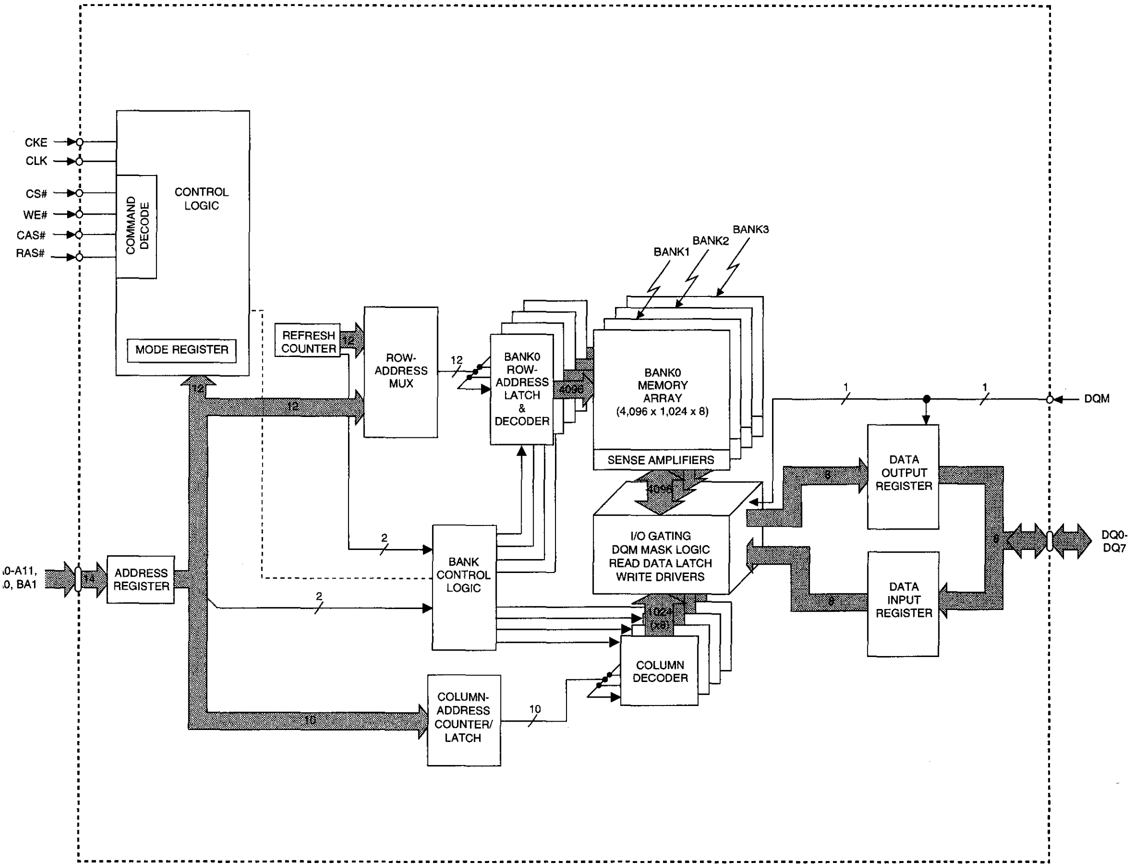
- Reads

- Writes

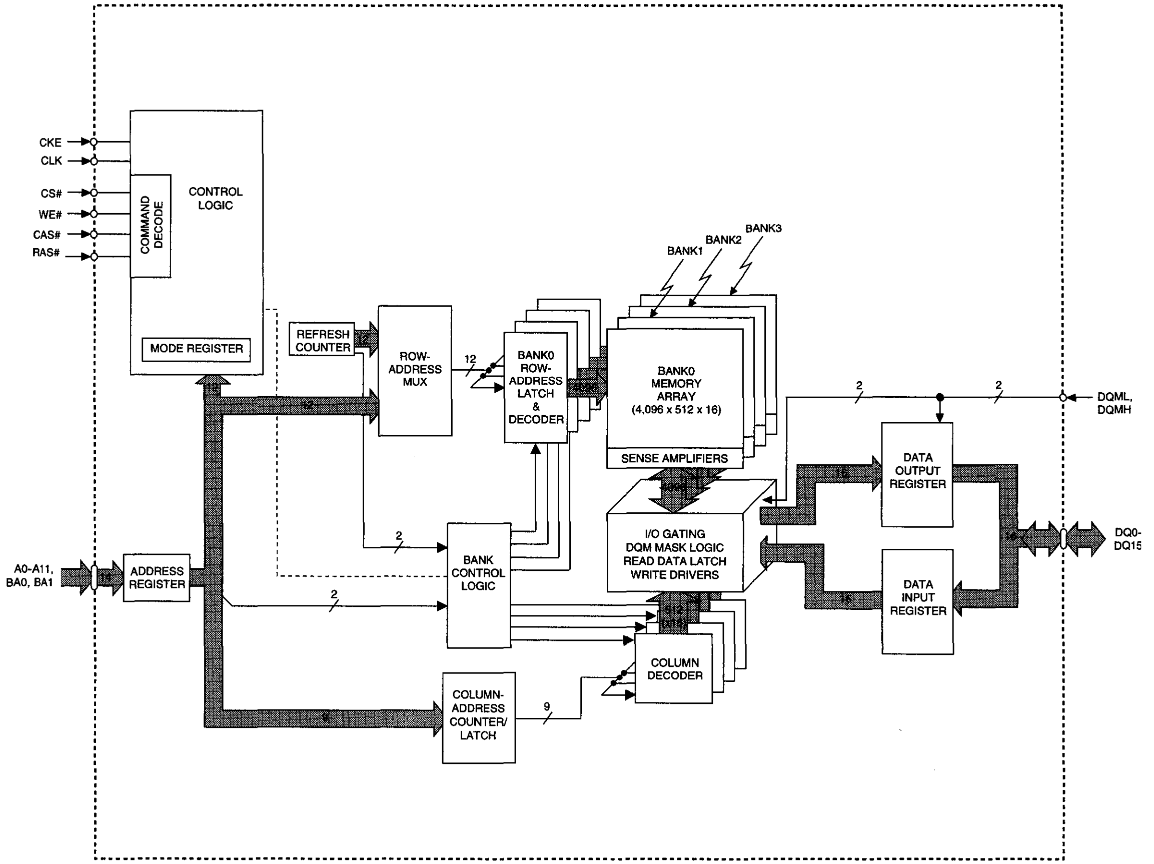
FUNCTIONAL BLOCK DIAGRAM
32 Meg x 4 SDRAM



FUNCTIONAL BLOCK DIAGRAM
16 Meg x 8 SDRAM



FUNCTIONAL BLOCK DIAGRAM
8 Meg x 16 SDRAM



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
38	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
37	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
19	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
16, 17, 18	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
39	x4, x8: DQM	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. On the x4 and x8, DQML (Pin 15) is a NC and DQMH is DQM. On the x16, DQML corresponds to DQ0-DQ7 and DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.
15, 39	x16: DQML, DQMH		
20, 21	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
23-26, 29-34, 22, 35	A0-A11	Input	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column-address A0-A9, A11 [x4]; A0-A9 [x8]; A0-A8 [x16]; with A10 defining AUTO PRECHARGE) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 4, 5, 7, 8, 10, 11, 13, 42, 44, 45, 47, 48, 50, 51, 53	DQ0-DQ15	x16: I/O	Data Input/Output: Data bus for x16 (4, 7, 10, 13, 42, 45, 48, 51 are NCs for x8; and 2, 4, 7, 8, 10, 13, 42, 45, 47, 48, 51, 53 are NCs for x4).
2, 5, 8, 11, 44, 47, 50, 53	DQ0-DQ7	x8: I/O	Data Input/Output: Data bus for x8 (2, 8, 47, 53 are NCs for x4).
5, 11, 44, 50	DQ0-DQ3	x4: I/O	Data Input/Output: Data bus for x4.
36, 40	NC	–	No Connect: These pins should be left unconnected.
3, 9, 43, 49	VDDQ	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
6, 12, 46, 52	VSSQ	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 14, 27	VDD	Supply	Power Supply: +3.3V ±0.3V.
28, 41, 54	VSS	Supply	Ground.

SYNCHRONOUS DRAM

MT48LC64M4A2 - 16 Meg x 4 x 4 banks
MT48LC32M8A2 - 8 Meg x 8 x 4 banks
MT48LC16M16A2 - 4 Meg x 16 x 4 banks

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

EATURES

PC100-compliant, includes CONCURRENT AUTO PRECHARGE; PC133-compliant
Fully synchronous; all signals registered on positive edge of system clock
Internal pipelined operation; column address can be changed every clock cycle
Internal banks for hiding row access/precharge
Programmable burst lengths: 1, 2, 4, 8 or full page
Auto Precharge and Auto Refresh Modes
Self Refresh Mode
64ms, 8,192-cycle refresh
LVTTL-compatible inputs and outputs
Single +3.3V ±0.3V power supply

PTIONS

	MARKING
Configurations	
64 Meg x 4 (16 Meg x 4 x 4 banks)	64M4
32 Meg x 8 (8 Meg x 8 x 4 banks)	32M8
16 Meg x 16 (4 Meg x 16 x 4 banks)	16M16
WRITE Recovery (ᵗWR)	
ᵗWR = 1 CLK (No longer supported.)	A1
ᵗWR = 2 CLK	A2
Plastic Packages - OCPL*	
54-pin TSOP (400 mil)	TG
66-pin TSOP (400 mil) (Under evaluation.)	
60-bump FBGA (8mm x 16mm) (Under evaluation.)	
Timing (Cycle Time)	
7ns (143 MHz)	-7
7.5ns (133 MHz)	-75
8ns (125 MHz)	-8E

Part Number Example: MT48LC16M16A2TG-8E

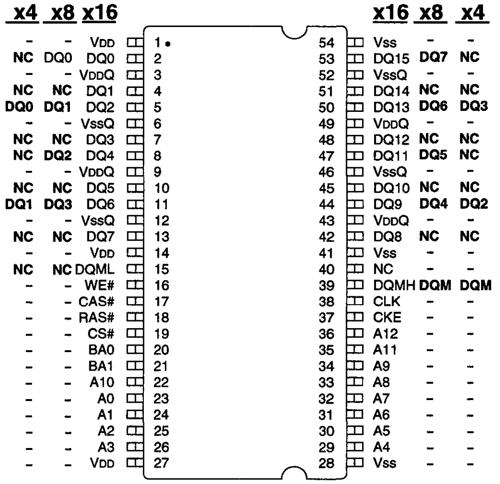
EY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2**	CL = 3**		
-7	143 MHz	–	5.4ns	1.8ns	0.8ns
-75	133 MHz	–	5.4ns	1.8ns	0.8ns
-7	133 MHz	5.5ns	–	1.8ns	0.8ns
-8E	125 MHz	–	6ns	2ns	1ns
-8E	100 MHz	6ns	–	2ns	1ns

ff-center parting line
CL = CAS (READ) latency

PIN ASSIGNMENT (Top View)

54-Pin TSOP
(C-5)



Note: The # symbol indicates signal is active LOW. A dash (–) indicates x8 and x4 pin function is same as x16 pin function.

	64 Meg x 4	32 Meg x 8	16 Meg x 16
Configuration	16 Meg x 4 x 4 banks	8 Meg x 8 x 4 banks	4 Meg x 16 x 4 banks
Refresh Count	8K	8K	8K
Row Addressing	8K (A0-A12)	8K (A0-A12)	8K (A0-A12)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	2K (A0-A9, A11)	1K (A0-A9)	512 (A0-A8)

256Mb SDRAM PART NUMBERS

PART NUMBER	ARCHITECTURE
MT48LC64M4A2TG	64 Meg x 4
MT48LC32M8A2TG	32 Meg x 8
MT48LC16M16A2TG	16 Meg x 16

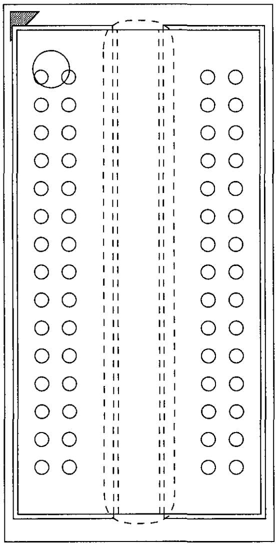
PIN ASSIGNMENT (Top View)

66-Pin TSOP

(C-6)

x4	x8	x16	Pin	Pin	x16	x8	x4
-	-	VDD	1 •	66	Vss	-	-
NC	DQ0	DQ0	2	65	DQ15	**DQ7**	**NC**
-	-	VDDQ	3	64	VssQ	-	-
NC	**NC**	DQ1	4	63	DQ14	**NC**	**NC**
DQ0	**DQ1**	DQ2	5	62	DQ13	**DQ6**	**DQ3**
-	-	VssQ	6	61	VDDQ	-	-
NC	**NC**	DQ3	7	60	DQ12	**NC**	**NC**
NC	**DQ2**	DQ4	8	59	DQ11	**DQ5**	**NC**
-	-	VDDQ	9	58	VssQ	-	-
NC	**NC**	DQ5	10	57	DQ10	**NC**	**NC**
DQ1	**DQ3**	DQ6	11	56	DQ9	**DQ4**	**DQ2**
-	-	VssQ	12	55	VDDQ	-	-
NC	**NC**	DQ7	13	54	DQ8	**NC**	**NC**
-	-	NC	14	53	NC	-	-
-	-	VDDQ	15	52	VssQ	-	-
-	-	NC	16	51	NC	-	-
-	-	NC	17	50	NC	-	-
-	-	VDD	18	49	VREF	-	-
-	-	NC	19	48	Vss	-	-
NC	**NC**	DQML	20	47	DQMH	**DQM**	**DQM**
-	-	WE#	21	46	NC	-	-
-	-	CAS#	22	45	CLK	-	-
-	-	RAS#	23	44	CKE	-	-
-	-	CS#	24	43	NC	-	-
-	-	NC	25	42	A12	-	-
-	-	BA0	26	41	A11	-	-
-	-	BA1	27	40	A9	-	-
-	-	A10	28	39	A8	-	-
-	-	A0	29	38	A7	-	-
-	-	A1	30	37	A6	-	-
-	-	A2	31	36	A5	-	-
-	-	A3	32	35	A4	-	-
-	-	VDD	33	34	Vss	-	-

60-Bump FBGA



x16		x8		x4		x4		x8		x16	
1	2	1	2	1	2	7	8	7	8	7	8
DQ15	Vss	DQ7	Vss	NC	Vss	VDD	NC	VDD	DQ0	VDD	DQ0
DQ14	VssQ	NC	VssQ	NC	VssQ	VDDQ	NC	VDDQ	NC	VDDQ	DQ1
VDDQ	DQ13	VDDQ	DQ6	VDDQ	DQ3	DQ0	VssQ	DQ1	VssQ	DQ2	VssQ
DQ11	DQ12	DQ5	NC	NC	NC	NC	NC	NC	DQ2	DQ3	DQ4
DQ10	VssQ	NC	VssQ	NC	VssQ	VDDQ	NC	VDDQ	NC	VDDQ	DQ5
VDDQ	DQ9	VDDQ	DQ4	VDDQ	DQ2	DQ1	VssQ	DQ3	VssQ	DQ6	VssQ
NC	DQ8	NC	NC	NC	NC	NC	NC	NC	NC	DQ7	NC
NC	Vss	NC	Vss	NC	Vss	VDD	NC	VDD	NC	VDD	DQML
VREF	DQMH	VREF	DQM	VREF	DQM	WE#	CAS#	WE#	CAS#	WE#	CAS#
NC	CLK	NC	CLK	NC	CLK	RAS#	NC	RAS#	NC	RAS#	NC
A12	CKE	A12	CKE	A12	CKE	NC	CS#	NC	CS#	NC	CS#
A11	A9	A11	A9	A11	A9	BA1	BA0	BA1	BA0	BA1	BA0
A8	A7	A8	A7	A8	A7	A0	A10	A0	A10	A0	A10
A6	A5	A6	A5	A6	A5	A2	A1	A2	A1	A2	A1
A4	Vss	A4	Vss	A4	Vss	VDD	A3	VDD	A3	VDD	A3

ENERAL DESCRIPTION

The 256Mb SDRAM is a high-speed CMOS, dynamic andom-access memory containing 268,435,456 bits. It is ternally configured as a quad-bank DRAM with a synhronous interface (all signals are registered on the positive dge of the clock signal, CLK). Each of the x4's 67,108,864-it banks is organized as 8,192 rows by 2,048 columns by bits. Each of the x8's 67,108,864-bit banks is organized as ,192 rows by 1,024 columns by 8 bits. Each of the x16's 7,108,864-bit banks is organized as 8,192 rows by 512 olumns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; ccesses start at a selected location and continue for a rogrammed number of locations in a programmed seuence. Accesses begin with the registration of an ACTIVE ommand, which is then followed by a READ or WRITE ommand. The address bits registered coincident with the CTIVE command are used to select the bank and row to be ccessed (BA0, BA1 select the bank; A0-A12 select the row). he address bits registered coincident with the READ or RITE command are used to select the starting column ocation for the burst access.

The SDRAM provides for programmable READ or RITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 256Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

The 256Mb SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.

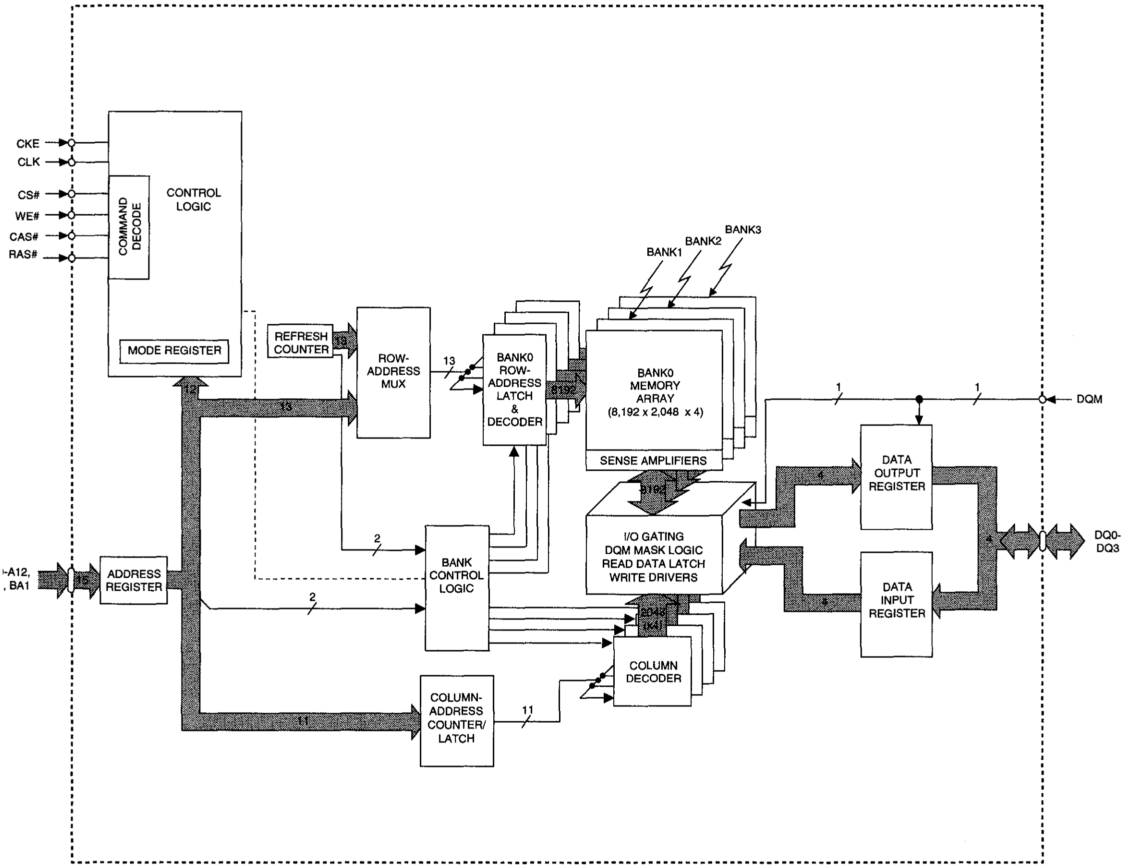
TABLE OF CONTENTS (for full data sheet)

Timing Waveforms

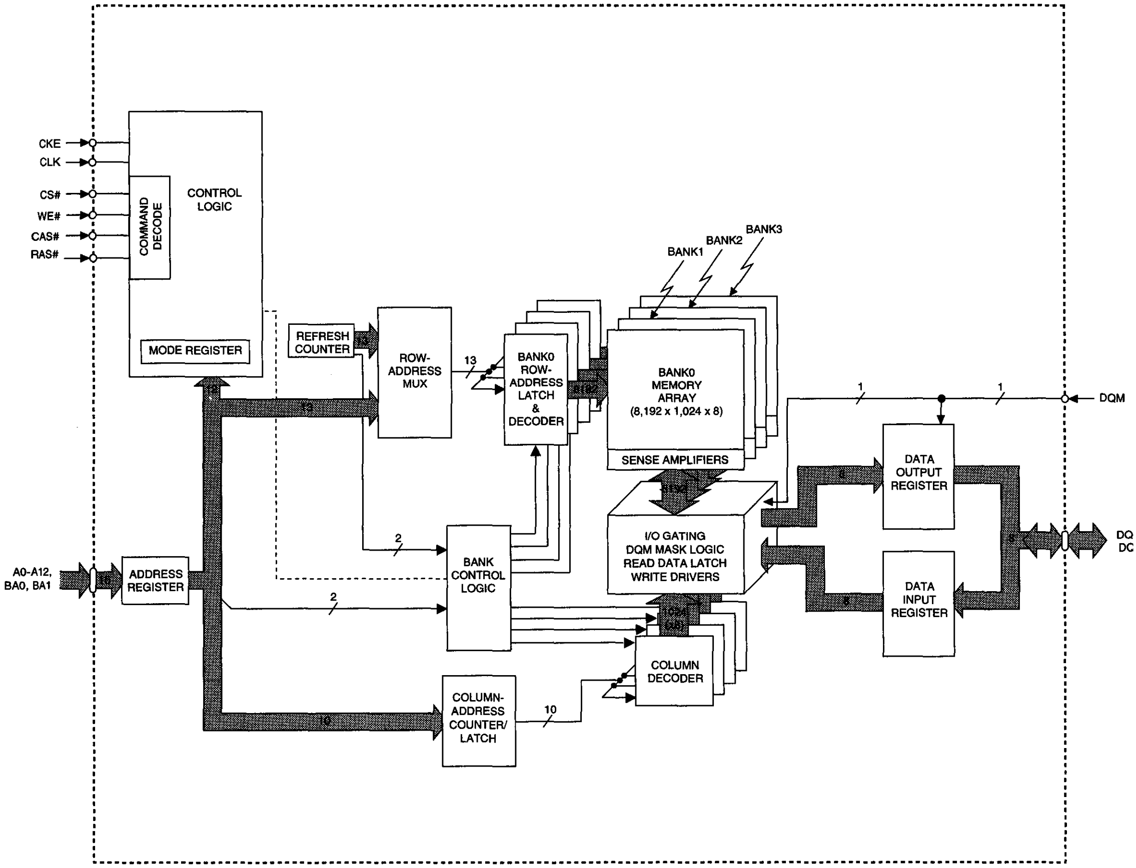
  Reads

  Writes

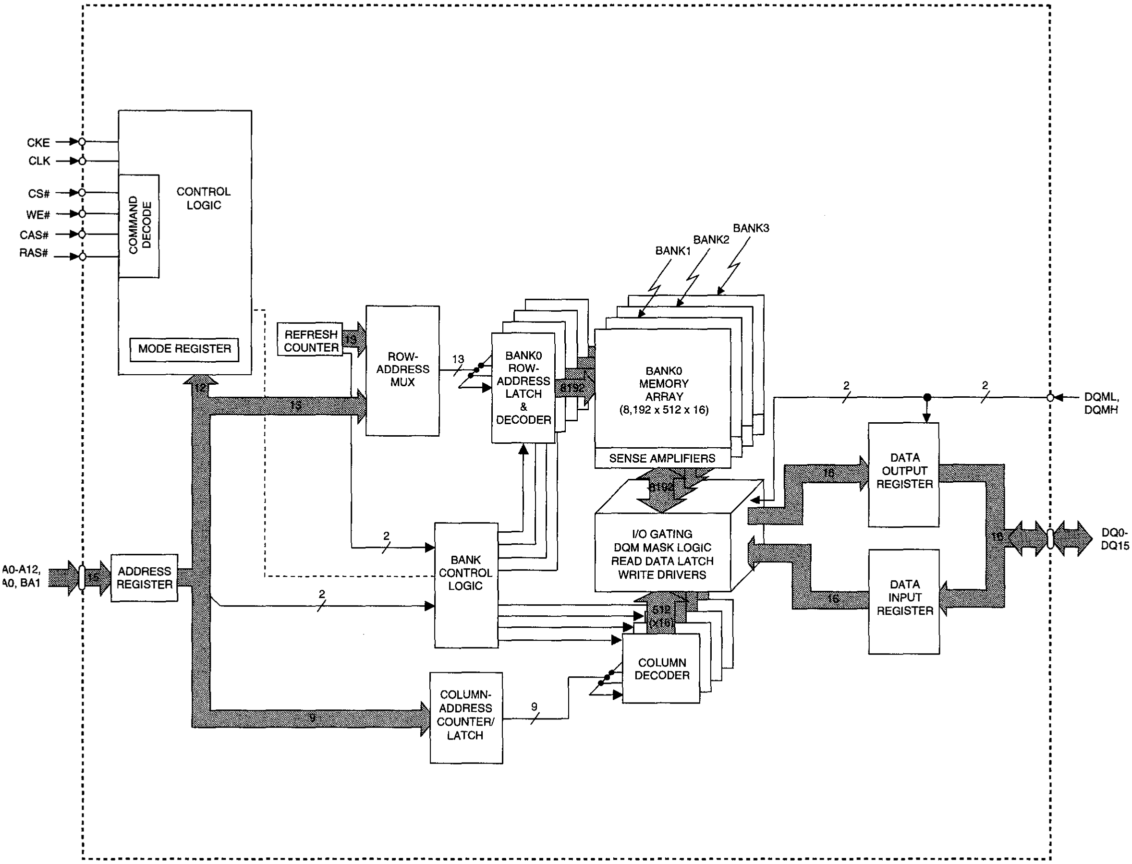
FUNCTIONAL BLOCK DIAGRAM
64 Meg x 4 SDRAM



FUNCTIONAL BLOCK DIAGRAM
32 Meg x 8 SDRAM



FUNCTIONAL BLOCK DIAGRAM
16 Meg x 16 SDRAM



Micron Technology, Inc., reserves the right to change products or specifications without notice.

PIN DESCRIPTIONS

54-PIN TSOP	SYMBOL	TYPE	DESCRIPTION
38	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
37	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
19	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
18, 17, 16	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
39	x4, x8: DQM	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. On the x4 and x8, DQML (Pin 15) is a NC and DQMH is DQM. On the x16, DQML corresponds to DQ0-DQ7 and DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.
15, 39	x16: DQML, DQMH		
20, 21	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
23-26, 29-34, 22, 35, 36	A0-A12	Input	Address Inputs: A0-A12 are sampled during the ACTIVE command (row-address A0-A12) and READ/WRITE command (column-address A0-A9, A11 [x4]; A0-A9 [x8]; A0-A8 [x16]; with A10 defining AUTO PRECHARGE) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by A10 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 4, 5, 7, 8, 10, 11, 13, 42, 44, 45, 47, 48, 50, 51, 53	DQ0-DQ15	x16: I/O	Data Input/Output: Data bus for x16 (4, 7, 10, 13, 42, 45, 48, 51 are NCs for x8; and 2, 4, 7, 8, 10, 13, 42, 45, 47, 48, 51, 53 are NCs for x4).
2, 5, 8, 11, 44, 47, 50, 53	DQ0-DQ7	x8: I/O	Data Input/Output: Data bus for x8 (2, 8, 47, 53 are NCs for x4).
5, 11, 44, 50	DQ0-DQ3	x4: I/O	Data Input/Output: Data bus for x4.
40	NC	–	No Connect: This pin should be left unconnected.
3, 9, 43, 49	VDDQ	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
6, 12, 46, 52	VSSQ	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 14, 27	VDD	Supply	Power Supply: +3.3V ±0.3V.
28, 41, 54	VSS	Supply	Ground.

SYNCHRONOUS DRAM

MT48LC1M16A1 S - 512K x 16 x 2 banks

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- PC100-compliant; includes CONCURRENT AUTO PRECHARGE
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
  1 Meg x 16 - 512K x 16 x 2 banks architecture with 11 row, 8 column addresses per bank
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge Mode
- Self Refresh and Adaptable Auto Refresh Modes
  - 32ms, 2,048-cycle refresh or
  - 64ms, 2,048-cycle refresh or
  - 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

OPTIONS MARKING

OPTIONS	MARKING
• Configuration	
1 Meg x 16 (512K x 16 x 2 banks)	1M16A1
• Plastic Package - OCPL*	
50-pin TSOP (400 mil)	TG
• Timing (Cycle Time)	
6ns (166 MHz)	-6
7ns (143 MHz)	-7
8ns (125 MHz)	-8A
• Refresh	
2K or 4K with Self Refresh Mode at 64ms	S

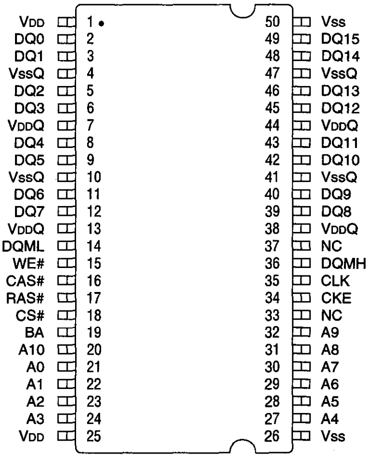
- Part Number Example: MT48LC1M16A1TG-7S

KEY TIMING PARAMETERS

SPEED	CLOCK	ACCESS TIME CL = 3**	ᵗAA	SETUP	HOLD
-6	166 MHz	5.5ns	17.5ns	2ns	1ns
-7	143 MHz	5.5ns	19.5ns	2ns	1ns
-8A	125 MHz	6ns	20ns	2ns	1ns

Off-center parting line
CL = CAS (READ) latency

PIN ASSIGNMENT (Top View)
50-Pin TSOP
(C-4)



Note: The # symbol indicates signal is active LOW.

	1 Meg x 16
Configuration	512K x 16 x 2 banks
Refresh Count	2K or 4K
Row Addressing	2K (A0-A10)
Bank Addressing	2 (BA)
Column Addressing	256 (A0-A7)

16Mb (x16) SDRAM PART NUMBER

PART NUMBER	ARCHITECTURE
MT48LC1M16A1TG S	1 Meg x 16

GENERAL DESCRIPTION

The 16Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 16,777,216 bits. It is internally configured as a dual 512K x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 512K x 16-bit banks is organized as 2,048 rows by 256 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed

GENERAL DESCRIPTION (continued)

sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 1 Meg x 16 SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

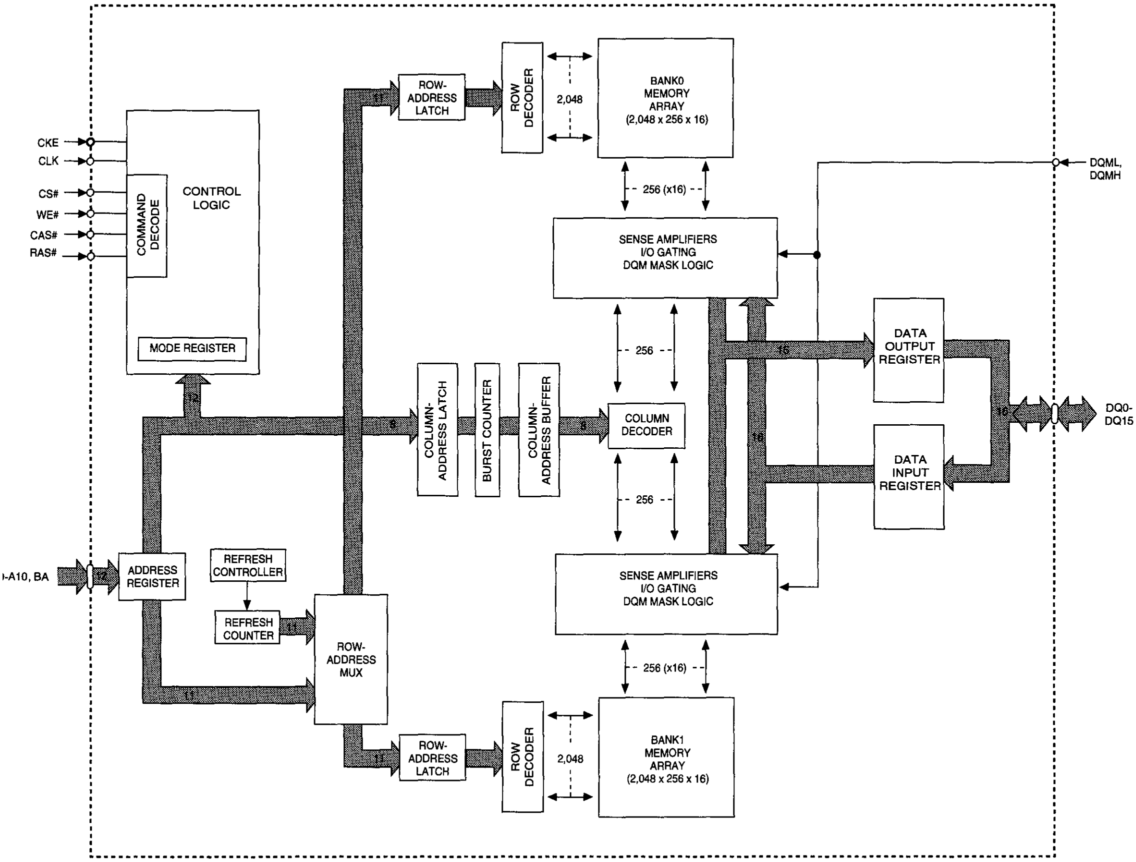
The 1 Meg x 16 SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

TABLE OF CONTENTS (for full data sheet)

Timing Waveforms

FUNCTIONAL BLOCK DIAGRAM
1 Meg x 16 SDRAM



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
35	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
34	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), ACTIVE POWER-DOWN (row ACTIVE in either bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
18	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
15, 16, 17	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
14, 36	DQML, DQMH	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. DQML corresponds to DQ0-DQ7; DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.
19	BA	Input	Bank Address Inputs: BA defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the twelfth bit of the Mode Register.
21-24, 27-32, 20	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7, with A10 defining AUTO PRECHARGE) to select one location out of the 512K available in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49	DQ0-DQ15	Input/ Output	Data I/O: Data bus.
33, 37	NC	–	No Connect: These pins should be left unconnected.
7, 13, 38, 44	$V_{DD}Q$	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
4, 10, 41, 47	$V_{SS}Q$	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 25	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
26, 50	V_{SS}	Supply	Ground.

SYNCHRONOUS DRAM

MT48LC2M32B2 - 512K x 32 x 4 banks

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- PC100-compliant; includes CONCURRENT AUTO PRECHARGE
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh (15.6µs/row)
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

OPTIONS	MARKING
• Configuration	
2 Meg x 32 (512K x 32 x 4 banks)	2M32B2
• Plastic Package - OCPL*	
86-pin TSOP (400 mil)	TG
• Timing (Cycle Time)	
6ns (166 MHz)	-6
7ns (143 MHz)	-7
8ns (125 MHz)	-8E

- Part Number Example: MT48LC2M32B2TG-8E

KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME CL = 3**	SETUP TIME	HOLD TIME
-6	166 MHz	5ns	2ns	1ns
-7	143 MHz	5.5ns	2ns	1ns
-8E	125 MHz	6ns	2ns	1ns

*Off-center parting line
**CL = CAS (READ) latency

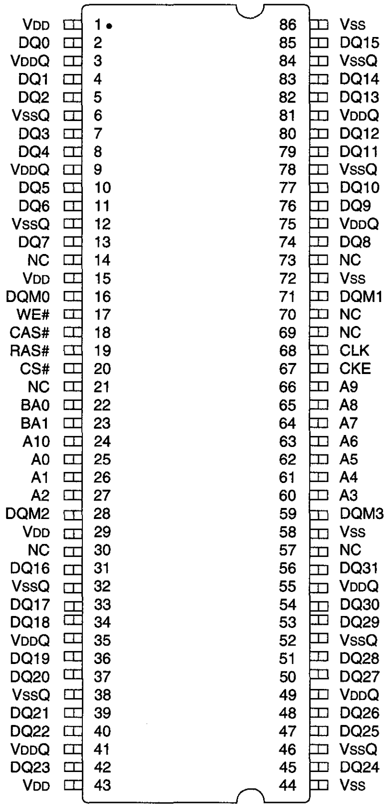
64Mb (x32) SDRAM PART NUMBER

PART NUMBER	ARCHITECTURE
MT48LC2M32B2TG	2 Meg x 32

PIN ASSIGNMENT (Top View)

86-Pin TSOP

(C-7)



Note: The # symbol indicates signal is active LOW.

	2 Meg x 32
Configuration	512K x 32 x 4 banks
Refresh Count	4K
Row Addressing	2K (A0-A10)
Bank Addressing	4 (BA0, BA1)
Column Addressing	256 (A0-A7)

GENERAL DESCRIPTION

The 64Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864-bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 16,777,216-bit banks is organized as 2,048 rows by 256 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 64Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

The 64Mb SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.

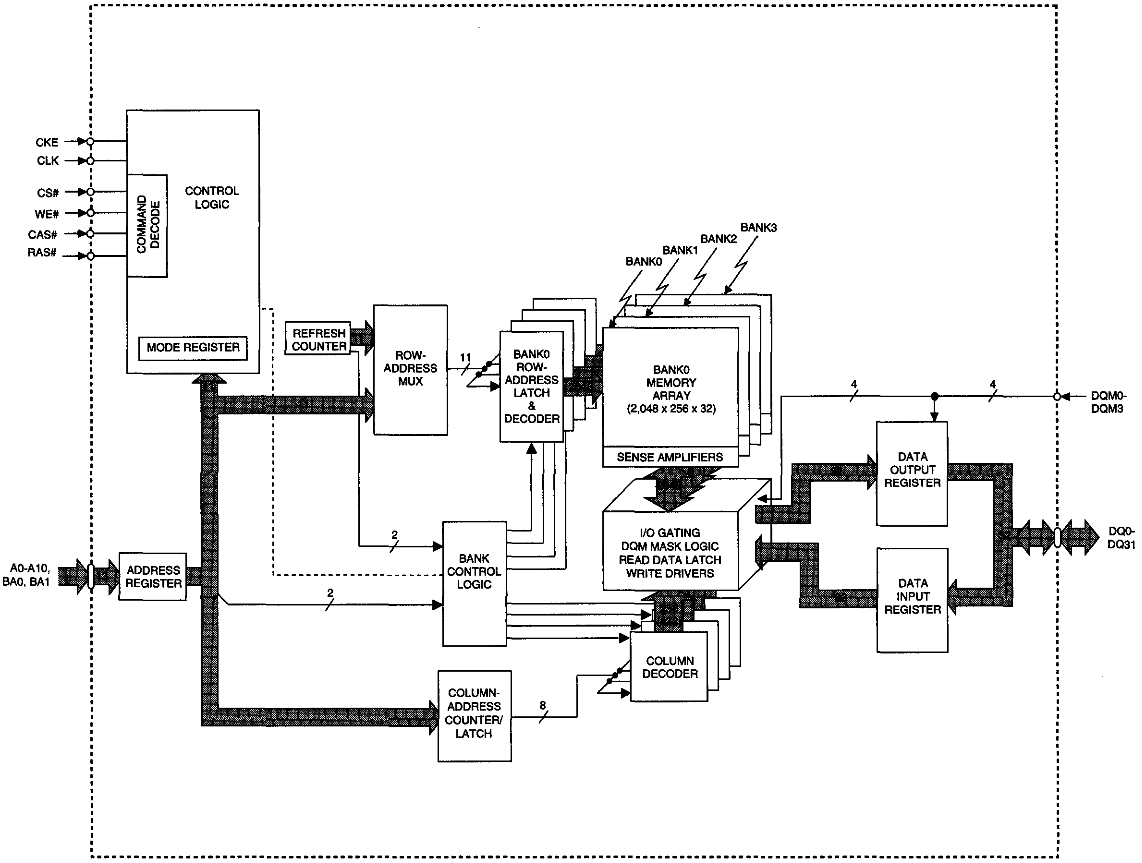
TABLE OF CONTENTS (for full data sheet)

Timing Waveforms

Reads

Writes

FUNCTIONAL BLOCK DIAGRAM
2 Meg x 32 SDRAM



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
68	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
67	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
20	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
19, 18, 17	RAS#, CAS# WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
16, 71, 28, 59	DQM0-DQM3	Input	Input/Output Mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) during a READ cycle. DQM0 corresponds to DQ0-DQ7, DQM1 corresponds to DQ8-DQ15, DQM2 corresponds to DQ16-DQ23 and DQM3 corresponds to DQ24-DQ31. DQM0-DQM3 are considered same state when referenced as DQM.
22, 23	BA0, BA1	Input	Bank Address Input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
25-27, 60-66, 24	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7 with A10 defining AUTO PRECHARGE) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 4, 5, 7, 8, 10, 11, 13, 74, 76, 77, 79, 80, 82, 83, 85, 31, 33, 34, 36, 37, 39, 40, 42, 45, 47, 48, 50, 51, 53, 54, 56	DQ0-DQ31	Input/ Output	Data I/Os: Data bus.
14, 21, 30, 57, 69, 70, 73	NC	–	No Connect: These pins should be left unconnected. Pin 70 is reserved for SSTL reference voltage supply.
3, 9, 35, 41, 49, 55, 75, 81	$V_{DD}Q$	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
6, 12, 32, 38, 46, 52, 78, 84	$V_{SS}Q$	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 15, 29, 43	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
44, 58, 72, 86	V_{SS}	Supply	Ground.

DRAM 1

SGRAM PRODUCT SELECTION GUIDE

Memory Configuration	Part Number	Voltage	Data Rate	Data Rate Per Pin (MHz)	Maximum Clock Frequency (MHz)	Number of Pins		Page
						TQFP	TSOP	
256K x 32	MT41LC256K32D4	3.3V	SDR	100	100	100	–	1-51
512K x 32*	MT45V512K32	2.5V	DDR	333, 300	167, 150	100	–	1-1
2 Meg x 32**	MT48LC2M32B2	3.3V	SDR	143, 133, 125	166, 143, 125	–	86	1-45

DDR = Double Data Rate, SDR = Single Data Rate
*The 512K x 32 DDR SGRAM data sheet is found in the DDR/SLDRAM/RDRAM section.
**The 2 Meg x 32 SDRAM data sheet is found in the SDRAM section.

SYNCHRONOUS GRAPHICS RAM

MT41LC256K32D4 – 128K x 32 x 2 banks

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Dual internal banks for hiding row access/precharge; dual 128K x 32 architecture
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Block Write and Write-Per-Bit Modes
- Independent byte operation via DQM0-DQM3
- Auto Precharge and Auto Refresh Modes
- 17ms, 1,024-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

OPTIONS

OPTIONS	MARKING
• Timing 10ns cycle (≤ 100 MHz clock rate)	-10
• Plastic Package 100-pin TQFP (0.65mm lead pitch)	LG

- Part Number Example: MT41LC256K32D4LG-10

KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-10	100 MHz	9ns	3ns	1ns

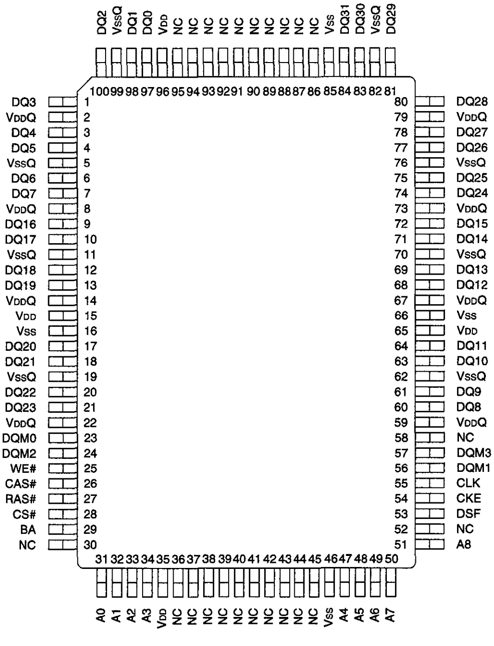
GENERAL DESCRIPTION

The MT41LC256K32D4 SGRAM is a high-speed CMOS, dynamic random-access memory containing 8,388,608 bits. It is internally configured as a dual 128K x 32 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 128K x 32-bit banks is organized as 512 rows by 256 columns by 32 bits. Read and write accesses to the SGRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed (BA selects the bank, A0-A8 select the row). Then, the address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

PIN ASSIGNMENT (Top View)

100-Pin TQFP*

(D-1)



*JEDEC standard MS-026 BHA (LQFP)

The SGRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The MT41LC256K32D4 uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank

GENERAL DESCRIPTION (continued)

will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

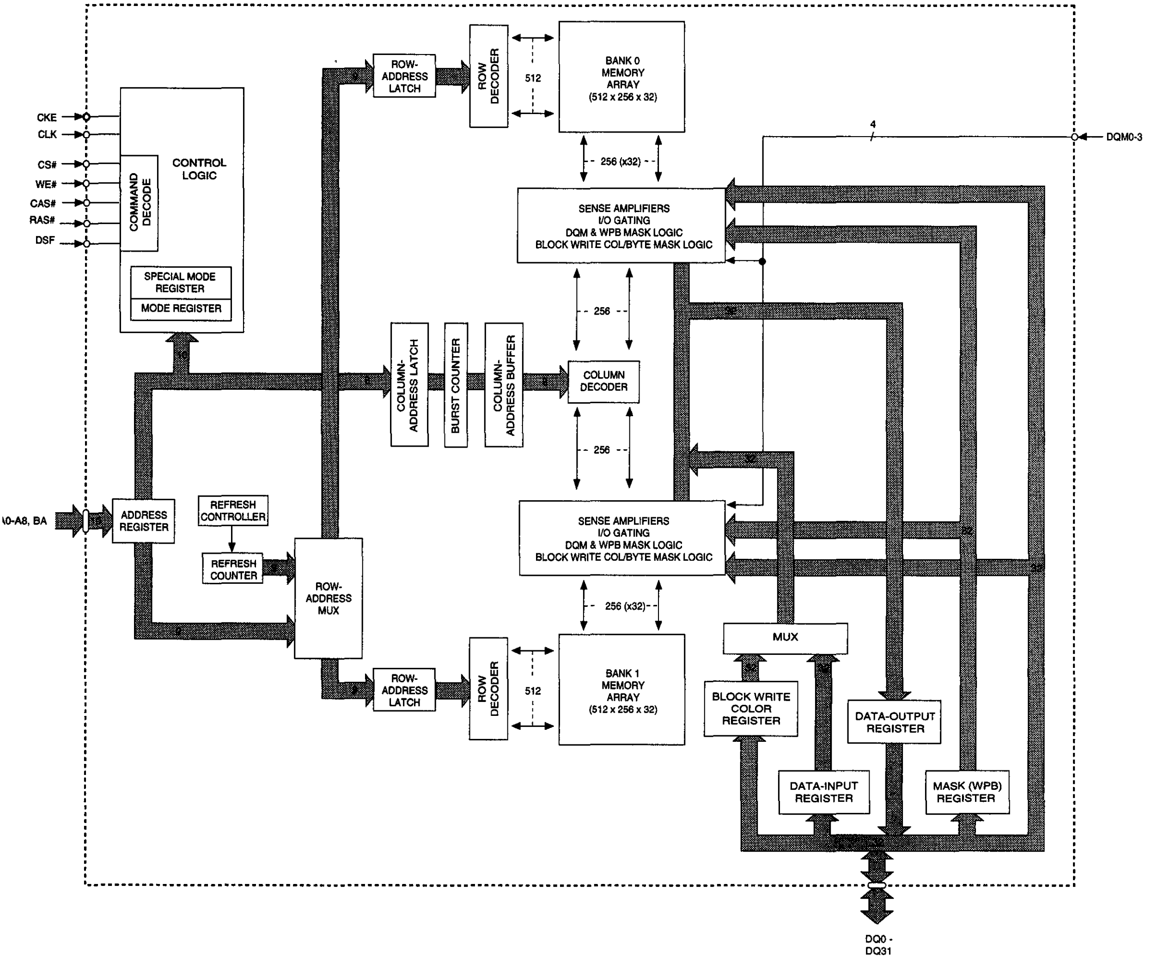
Synchronous graphics RAMs (SGRAMs) differ from synchronous DRAMs (SDRAMs) by providing an eight-column BLOCK WRITE function and a MASKED WRITE (or WRITE-PER-BIT) function to accommodate high-performance graphics applications. The BLOCK WRITE and MASKED WRITE functions may be combined with individual byte enables (DQ mask or DQM pins).

The CMOS dynamic memory structure of the MT41LC256K32D4 is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

The two-bank synchronous DRAM and x32 configuration provided by the SGRAM are well suited for applications requiring high memory bandwidth, and when combined with special graphics functions, result in a device particularly well suited to high-performance graphics applications.

SGRAMs offer substantial advances in dynamic memory operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation; the ability to interleave between internal banks to hide precharge time; the capability to randomly change column addresses on each clock cycle during a burst access; and special functions such as MASKED WRITEs and BLOCK WRITEs.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
55	CLK	Input	Clock: CLK is driven by the system clock. All SGRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
54	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. After both banks are precharged, deactivating the clock provides power-down mode and self refresh mode. CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
28	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
27, 26, 53, 25	RAS#, CAS#, DSF, WE#	Input	Command Inputs: RAS#, CAS#, DSF and WE# define the command being entered.
23, 56, 24, 57	DQM0-DQM3	Input	Input/Output Masks: DQM0-DQM3 are byte-specific, nonpersistent I/O buffer controls. The I/O buffers are placed in a High-Z state when DQM is sampled HIGH. Input data is masked when DQM is sampled HIGH during a WRITE cycle. Output data is masked (two-clock latency) when DQM is sampled HIGH during a READ cycle. DQM0 masks DQ0-DQ7, DQM1 masks DQ8-DQ15, DQM2 masks DQ16-DQ23, and DQM3 masks DQ24-DQ31.
29	BA	Input	Bank Address: BA defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the tenth bit of the Mode and Special Mode Registers.
31-34, 47-51	A0-A8	Input	Address Inputs: A0-A8 are sampled during the ACTIVE command (row-address A0-A8) and READ/WRITE command (column-address A0-A7, with A8 defining AUTO PRECHARGE) to select one location out of the 131,072 available in the respective bank. A8 is sampled during a PRECHARGE command to determine if both banks are to be precharged (A8 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER or LOAD SPECIAL MODE REGISTER command.
97, 98, 100, 1, 3, 4, 6, 7, 60, 61, 63, 64, 68, 69, 71, 72, 9, 10, 12, 13, 17, 18, 20, 21, 74, 75, 77, 78, 80, 81, 83, 84	DQ0-DQ31	Input/ Output	Data I/Os: Data bus. The I/Os are byte-maskable during READs and WRITEs.The DQs also serve as column/byte mask inputs during BLOCK WRITEs.
30, 36-45, 52, 58, 86-95	NC	–	No Connect: These pins should be left unconnected.
2, 8, 14, 22, 59, 67, 73, 79	$V_{DD}Q$	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
5, 11, 19, 62, 70, 76, 82, 99	$V_{SS}Q$	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
15, 35, 65, 96	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
16, 46, 66, 85	V_{SS}	Supply	Ground.

DRAM 1

EDO DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Address Pins		Package/No. of Pins		Page
				Row	Column	SOJ	TSOP	
3.3V EDO DRAMs								
16 Meg x 4	EDO, 8KR	MT4LC16M4G3	50, 60	13	11	32	32	1-55
16 Meg x 4	EDO, 8KR, S	MT4LC16M4G3 S	50, 60	13	11	32	32	1-55
16 Meg x 4	EDO, 4KR	MT4LC16M4H9	50, 60	12	12	32	32	1-55
16 Meg x 4	EDO, 4KR, S	MT4LC16M4H9 S	50, 60	12	12	32	32	1-55
8 Meg x 8	EDO, 8KR	MT4LC8M8P4	50, 60	13	10	32	32	1-59
8 Meg x 8	EDO, 8KR, S	MT4LC8M8P4 S	50, 60	13	10	32	32	1-59
8 Meg x 8	EDO, 4KR	MT4LC8M8C2	50, 60	12	11	32	32	1-59
8 Meg x 8	EDO, 4KR, S	MT4LC8M8C2 S	50, 60	12	11	32	32	1-59
4 Meg x 16	EDO, DC, 4KR	MT4LC4M16R6	50, 60	12	10	–	50	1-63
4 Meg x 16	EDO, DC, 4KR, S	MT4LC4M16R6 S	50, 60	12	10	–	50	1-63

EDO = Extended Data-Out; DC = Dual CAS; 4KR = 4,096 Refresh; 8KR = 8,192 Refresh; S = Self Refresh

DRAM

MT4LC16M4G3, MT4LC16M4H9

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x4 pinout, timing, functions and packages
- 12 row, 12 column addresses (H9) or 13 row, 11 column addresses (G3)
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- Extended Data-Out (EDO) PAGE MODE access
- Optional self refresh (S) for low-power data retention
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) REFRESH distributed across 64ms

OPTIONS

OPTIONS	MARKING
• Refresh Addressing	
4,096 (4K) rows	H9
8,192 (8K) rows	G3
• Plastic Packages	
32-pin SOJ (400 mil)	DJ
32-pin TSOP (400 mil)	TG
• Timing	
50ns access	-5
60ns access	-6
• Refresh Rates	
Standard Refresh	None
Self Refresh (128ms period)	S*

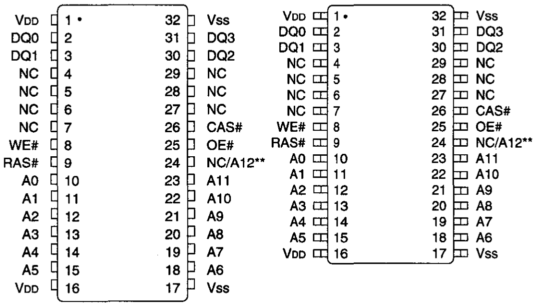
NOTE: 1. The 16 Meg x 4 EDO DRAM base number differentiates the offerings in one place - MT4LC16M4H9. The fifth field distinguishes the address offerings: H9 designates 4K addresses and G3 designates 8K addresses.
2. The "#" symbol indicates signal is active LOW.

Contact factory for availability

KEY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

PIN ASSIGNMENT (Top View)



32-Pin SOJ (A-1)

32-Pin TSOP (C-1)

** NC on H9 version, A12 on G3 version

16 MEG x 4 EDO DRAM PART NUMBERS

PART NUMBER	REFRESH ADDRESSING	PACKAGE	REFRESH
MT4LC16M4H9DJ-x	4K	SOJ	Standard
MT4LC16M4H9DJ-x S	4K	SOJ	Self
MT4LC16M4H9TG-x	4K	TSOP	Standard
MT4LC16M4H9TG-x S	4K	TSOP	Self
MT4LC16M4G3DJ-x	8K	SOJ	Standard
MT4LC16M4G3DJ-x S	8K	SOJ	Self
MT4LC16M4G3TG-x	8K	TSOP	Standard
MT4LC16M4G3TG-x S	8K	TSOP	Self

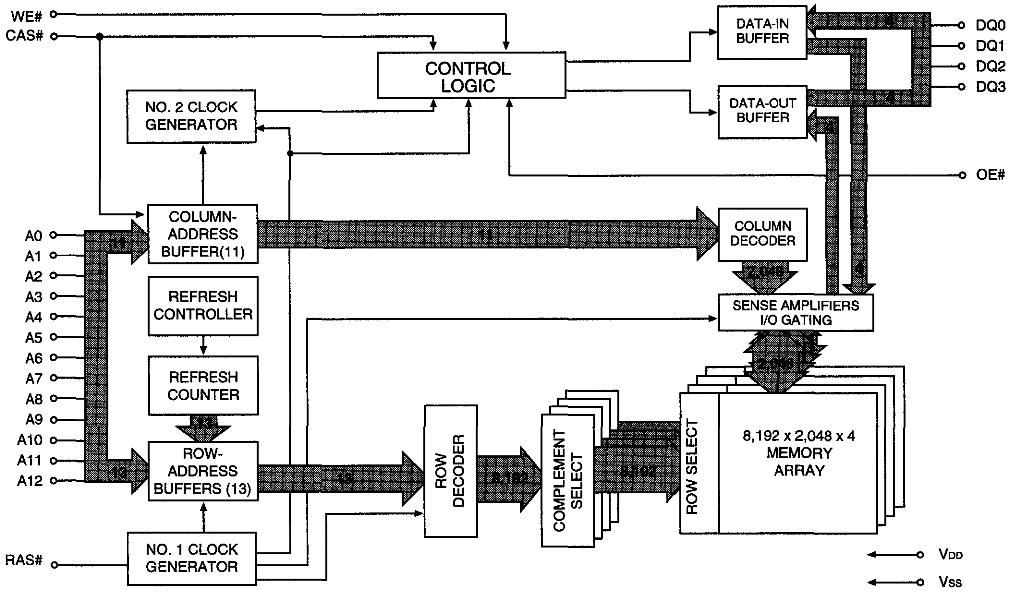
x = speed

GENERAL DESCRIPTION

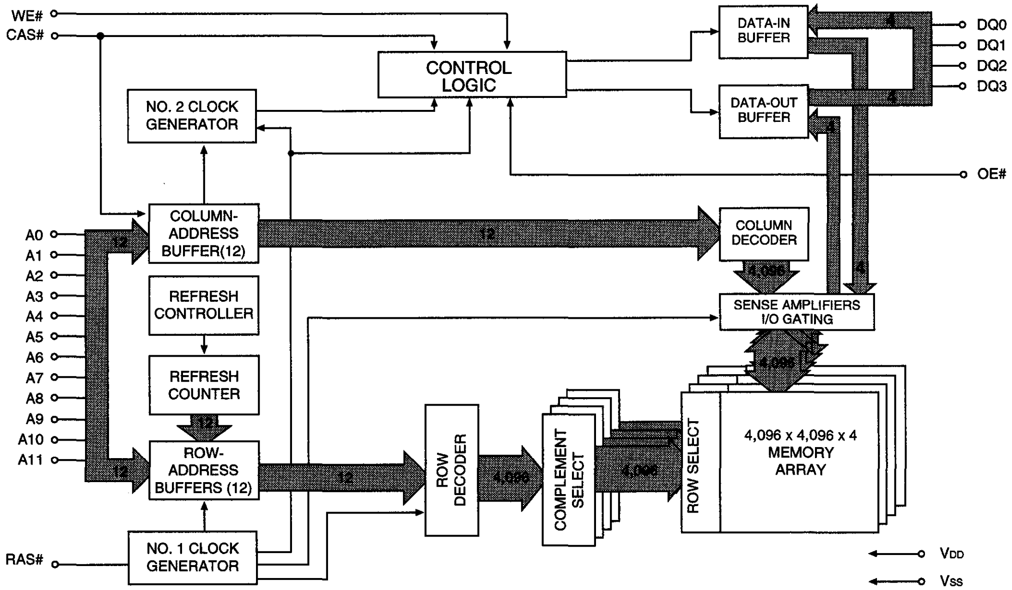
The 16 Meg x 4 DRAM is a high-speed CMOS, dynamic random-access memory device containing 67,108,864 bits and designed to operate from 3V to 3.6V. The MT4LC16M4H9 and MT4LC16M4G3 are functionally organized as 16,777,216 locations containing 4 bits each. The 16,777,216 memory locations are arranged in 4,096 rows by 4,096 columns on the H9 version and 8,192 rows by 2,048 columns on the G3 version. During READ or WRITE cycles, each location is uniquely addressed via the address bits. First, the row address is latched by the RAS# signal, then the column address is latched by CAS#. The device provides EDO-PAGE-MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

The 16 Meg x 4 DRAM must be refreshed periodically in order to retain stored data.

FUNCTIONAL BLOCK DIAGRAM
MT4LC16M4G3 (13 row addresses)



FUNCTIONAL BLOCK DIAGRAM
MT4LC16M4H9 (12 row addresses)



)RAM ACCESS

Each location in the DRAM is uniquely addressable, as ıentioned in the General Description. The data for each ›cation is accessed via the four I/O pins (DQ0-DQ3). A ›gic HIGH on WE# dictates read mode, while a logic LOW n WE# dictates write mode. During a WRITE cycle, data-ı (D) is latched by the falling edge of WE# or CAS#, 'hichever occurs last. An EARLY WRITE occurs when /E# is taken LOW prior to CAS# falling. A LATE WRITE or EAD-MODIFY-WRITE occurs when WE# falls after CAS# ı taken LOW. During EARLY WRITE cycles, the data utputs (Q) will remain High-Z, regardless of the state of 'E#. During LATE WRITE or READ-MODIFY-WRITE ycles, OE# must be taken HIGH to disable the data outputs rior to applying input data. If a LATE WRITE or READ-IODIFY-WRITE is attempted while keeping OE# LOW, no /RITE will occur, and the data outputs will drive read data 'om the accessed location.

;DO PAGE MODE

DRAM READ cycles have traditionally turned the out-ut buffers off (High-Z) with the rising edge of CAS#. If AS# went HIGH and OE# was LOW (active), the output uffers would be disabled. The 16 Meg x 4 DRAM offers an ccelerated page mode cycle by eliminating output disable 'om CAS# HIGH. This option is called EDO and it allows AS# precharge time (^{t}CP) to occur without the output data oing invalid (see READ and EDO-PAGE-MODE READ 'aveforms).

EDO operates like any DRAM READ or FAST-PAGE-IODE READ, except data is held valid after CAS# goes IGH, as long as RAS# and OE# are held LOW and WE# is eld HIGH. OE# can be brought LOW or HIGH while CAS# ıd RAS# are LOW, and the DQs will transition between alid data and High-Z. Using OE#, there are two methods › disable the outputs and keep them disabled during the AS# HIGH time. The first method is to have OE# HIGH 'hen CAS# transitions HIGH and keep OE# HIGH for)EHC thereafter. This will disable the DQs, and they will emain disabled (regardless of the state of OE# after that oint) until CAS# falls again. The second method is to have 'E# LOW when CAS# transitions HIGH and then bring 'E# HIGH for a minimum of ^{t}OEP anytime during the AS# HIGH period. This will disable the DQs, and they 'ill remain disabled (regardless of the state of OE# after ıat point) until CAS# falls again. (Please refer to Figure 1.) 'uring other cycles, the outputs are disabled at ^{t}OFF time ter RAS# and CAS# are HIGH or at ^{t}WHZ after WE# ansitions LOW. The ^{t}OFF time is referenced from the sing edge of RAS# or CAS#, whichever occurs last. WE# ın also perform the function of disabling the output driv-s under certain conditions, as shown in Figure 2.

EDO-PAGE-MODE operations are always initiated with a row address strobed in by the RAS# signal, followed by a column address strobed in by CAS#, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling CAS# while holding RAS# LOW and entering new column addresses with each CAS# cycle. Returning RAS# HIGH terminates the EDO-PAGE-MODE operation.

DRAM REFRESH

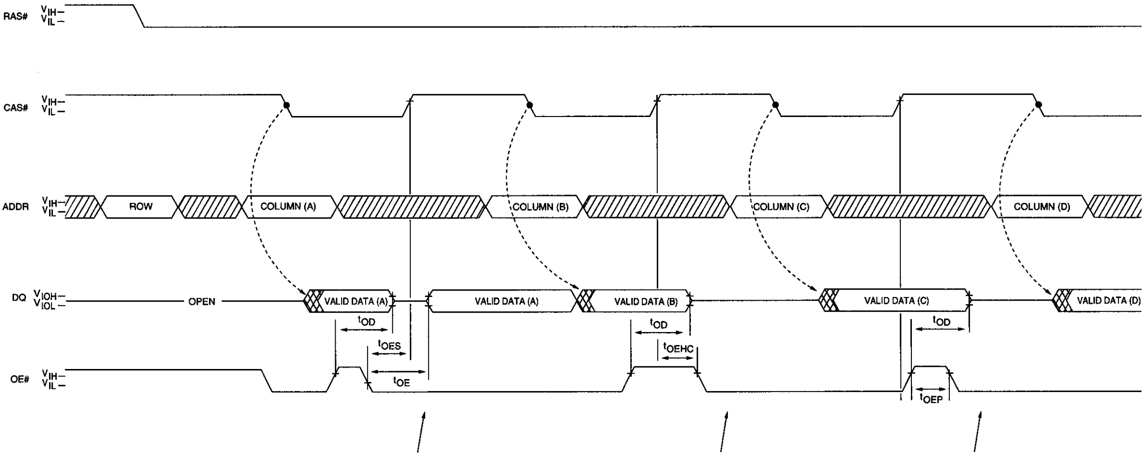
The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all 8,192 rows (G3) or all 4,096 rows (H9) in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC16M4G3 internally refreshes two rows for every CBR cycle, whereas the MT4LC16M4H9 refreshes one row for every CBR cycle. So with either device, executing 4,096 CBR cycles covers all rows. The CBR refresh will invoke the internal refresh counter for automatic RAS# addressing. Alternatively, RAS#-ONLY REFRESH capability is inherently provided. However, with this method, some compatibility issues may become apparent. For example, both G3 and H9 versions require 4,096 CBR REFRESH cycles, yet each requires a different number of RAS#-ONLY REFRESH cycles (G3 = 8,192 and H9 = 4,096). JEDEC strongly recommends the use of CBR REFRESH for this device.

An optional self refresh mode is also available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^{t}RASS. The "S" option allows for an extended refresh period of 128ms, or 31.25µs per row for a 4K refresh and 15.625µs per row for an 8K refresh, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

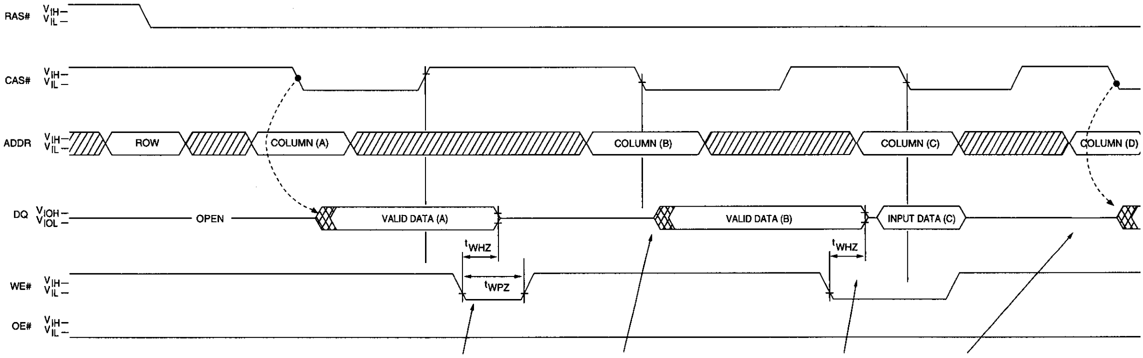


The DQs go back to Low-Z if ^{t}OES is met.

The DQs remain High-Z until the next CAS# cycle if ^{t}OEHC is met.

The DQs remain High-Z until the next CAS# cycle if ^{t}OEP is met.

Figure 1
OE# CONTROL OF DQs



The DQs go to High-Z if WE# falls and, if ^{t}WPZ is met, will remain High-Z until CAS# goes LOW with WE# HIGH (i.e., until a READ cycle is initiated).

WE# may be used to disable the DQs to prepare for input data in an EARLY WRITE cycle. The DQs will remain High-Z until CAS# goes LOW with WE# HIGH (i.e., until a READ cycle is initiated).

▨ DON'T CAR

▩ UNDEFINE

Figure 2
WE# CONTROL OF DQs

MICRON
TECHNOLOGY, INC.

8 MEG x 8 EDO DRAM

DRAM

MT4LC8M8P4, MT4LC8M8C2

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x8 pinout, timing, functions and packages
- 12 row, 11 column addresses (C2) or 13 row, 10 column addresses (P4)
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- Extended Data-Out (EDO) PAGE MODE access
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) REFRESH distributed across 64ms
- Optional self refresh (S) for low-power data retention

OPTIONS

OPTIONS	MARKING
• Refresh Addressing	
4,096 (4K) rows	C2
8,192 (8K) rows	P4
• Plastic Packages	
32-pin SOJ (400 mil)	DJ
32-pin TSOP (400 mil)	TG
• Timing	
50ns access	-5
60ns access	-6
• Refresh Rates	
Standard Refresh	None
Self Refresh	S*

NOTE: 1. The 8 Meg x 8 EDO DRAM base number differentiates the offerings in one place - MT4LC8M8C2. The fifth field distinguishes the address offerings: C2 designates 4K addresses and P4 designates 8K addresses.
2. The "#" symbol indicates signal is active LOW.

*Contact factory for availability

KEY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

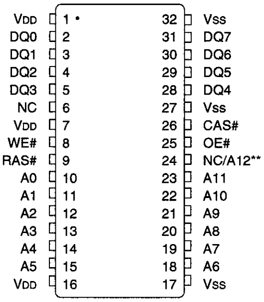
GENERAL DESCRIPTION

The 8 Meg x 8 DRAM is a high-speed CMOS, dynamic random-access memory devices containing 67,108,864 bits and designed to operate from 3V to 3.6V. The MT4LC8M8C2 and MT4LC8M8P4 are functionally organized as 8,388,608 locations containing eight bits each. The 8,388,608 memory locations are arranged in 4,096 rows by 2,048 columns on the C2 version and 8,192 rows by 1,024 columns on the P4 version. During READ or WRITE cycles, each location is uniquely addressed via the address bits. First, the row address is latched by the RAS# signal, then the column address is latched by CAS#. Both devices provide EDO-PAGE-MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

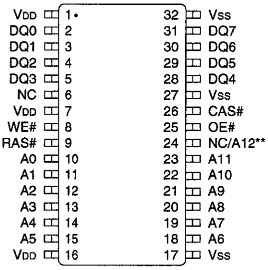
The 8 Meg x 8 DRAM must be refreshed periodically in order to retain stored data.

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(A-1)



32-Pin TSOP
(C-1)



**NC on C2 version and A12 on P4 version

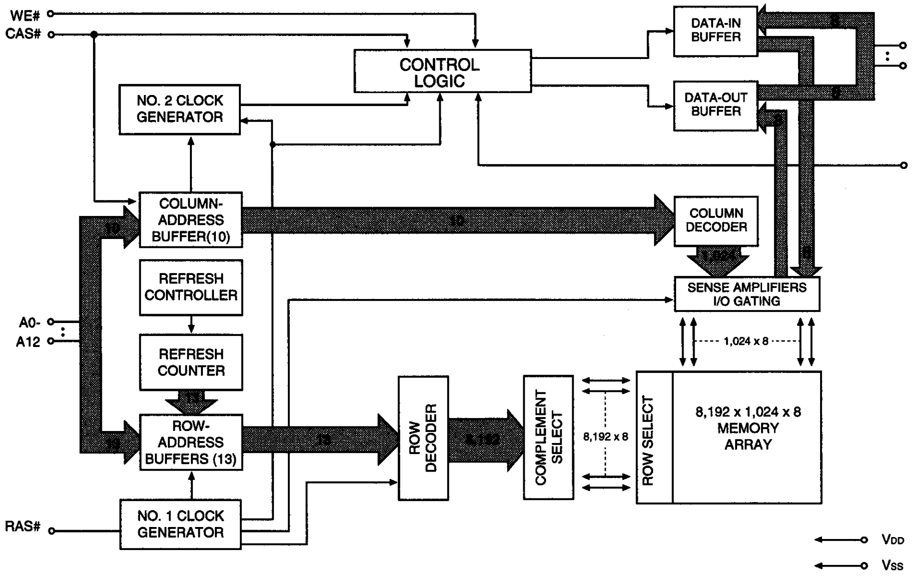
8 MEG x 8 EDO DRAM PART NUMBERS

PART NUMBER	REFRESH ADDRESSING	PACKAGE	REFRESH
MT4LC8M8C2DJ-x	4K	SOJ	Standard
MT4LC8M8C2DJ-x S	4K	SOJ	Self
MT4LC8M8C2TG-x	4K	TSOP	Standard
MT4LC8M8C2TG-x S	4K	TSOP	Self
MT4LC8M8P4DJ-x	8K	SOJ	Standard
MT4LC8M8P4DJ-x S	8K	SOJ	Self
MT4LC8M8P4TG-x	8K	TSOP	Standard
MT4LC8M8P4TG-x S	8K	TSOP	Self

x = speed

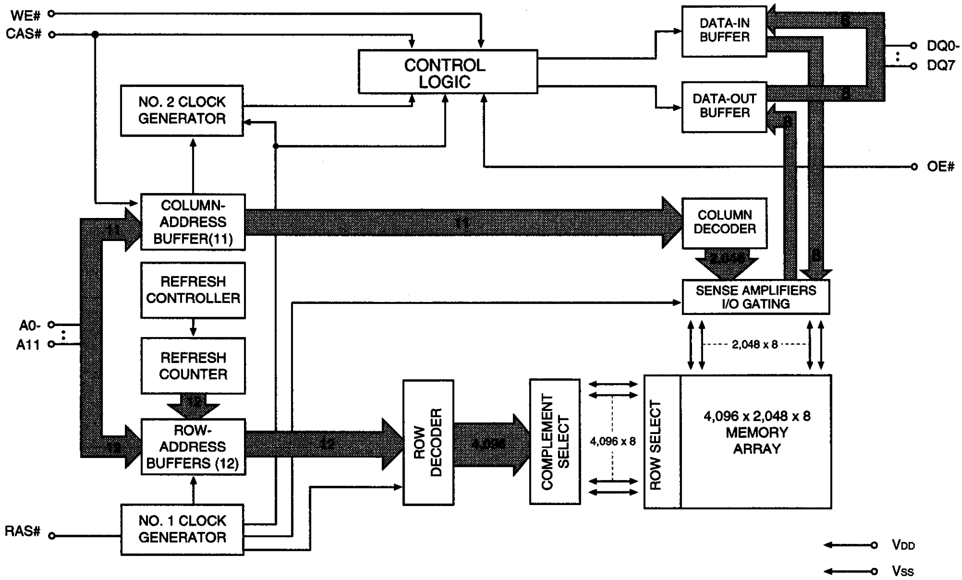
FUNCTIONAL BLOCK DIAGRAM

MT4LC8M8P4 (13 row addresses)



FUNCTIONAL BLOCK DIAGRAM

MT4LC8M8C2 (12 row addresses)



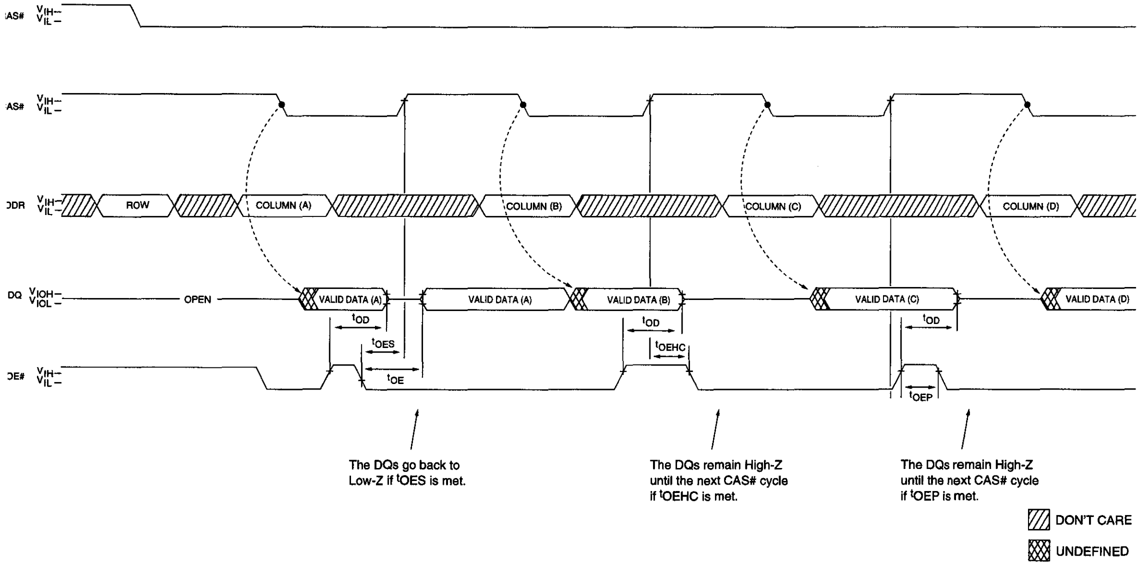
DRAM ACCESS

Each location in the DRAM is uniquely addressable, as mentioned in the General Description. The data for each ocation is accessed via the eight I/O pins (DQ0-DQ7). A ogic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-n (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# s taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z, regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE ycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data outputs will drive read data from the accessed location.

EDO PAGE MODE

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. If CAS# went HIGH and OE# was LOW (active), the output uffers would be disabled. The 8 Meg x 8 DRAM offers an ccelerated page mode cycle by eliminating output disable from CAS# HIGH. This option is called EDO, and it allows CAS# precharge time (^{t}CP) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms in the noted appendix).

EDO operates like any DRAM READ or FAST-PAGE-MODE READ, except data is held valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW and WE# is held HIGH. OE# can be brought LOW or HIGH while CAS# and RAS# are LOW, and the DQs will transition between valid data and High-Z. Using OE#, there are two methods to disable the outputs and keep them disabled during the CAS# HIGH time. The first method is to have OE# HIGH when CAS# transitions HIGH and keep OE# HIGH for ^{t}OEHC thereafter. This will disable the DQs, and they will remain disabled (regardless of the state of OE# after that point) until CAS# falls again. The second method is to have OE# LOW when CAS# transitions HIGH and then bring OE# HIGH for a minimum of ^{t}OEP anytime during the CAS# HIGH period. This will disable the DQs, and they will remain disabled (regardless of the state of OE# after that point) until CAS# falls again (see Figure 1). During other cycles, the outputs are disabled at ^{t}OFF time after RAS# and CAS# are HIGH or at ^{t}WHZ after WE# transitions LOW. The ^{t}OFF time is referenced from the rising edge of



The DQs go back to Low-Z if ^{t}OES is met.

The DQs remain High-Z until the next CAS# cycle if ^{t}OEHC is met.

The DQs remain High-Z until the next CAS# cycle if ^{t}OEP is met.

▨ DON'T CARE

▩ UNDEFINED

Figure 1
OE# CONTROL OF DQs

EDO PAGE MODE (continued)

RAS# or CAS#, whichever occurs last. WE# can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 2.

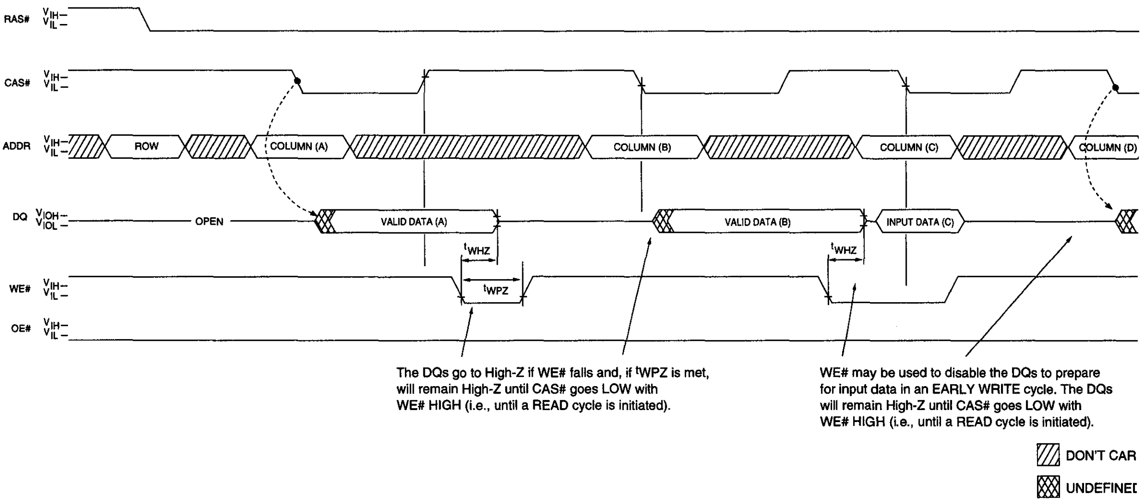
EDO-PAGE-MODE operations are always initiated with a row address strobed in by the RAS# signal, followed by a column address strobed in by CAS#, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling CAS# while holding RAS# LOW and entering new column addresses with each CAS# cycle. Returning RAS# HIGH terminates the EDO-PAGE-MODE operation.

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all 8,192 rows (P4) or all 4,096 rows (C2) in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC8M8P4 internally refreshes two rows for every CBR cycle, whereas the MT4LC8M8C2 refreshes one row for every CBR cycle. So with either device, executing 4,096 CBR cycles covers all rows. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing. Alternatively, RAS#-ONLY REFRESH capability is inherently provided. However, with this method, some compatibility issues may become apparent. For example, both C2 and P4 versions require 4,096 CBR REFRESH cycles, yet each requires a different number of RAS#-ONLY REFRESH cycles (C2 = 4,096 and P4 = 8,192). JEDEC strongly recommends the use of CBR REFRESH for this device.

An optional self refresh mode is also available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^{t}RASS. The "S" option allows for an extended period of 128ms, or 31.25µs per row for a 4K refresh and 15.625µs per row for an 8K refresh, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh.



The DQs go to High-Z if WE# falls and, if ^{t}WPZ is met, will remain High-Z until CAS# goes LOW with WE# HIGH (i.e., until a READ cycle is initiated).

WE# may be used to disable the DQs to prepare for input data in an EARLY WRITE cycle. The DQs will remain High-Z until CAS# goes LOW with WE# HIGH (i.e., until a READ cycle is initiated).

Figure 2
WE# CONTROL OF DQs

DRAM

MT4LC4M16R6

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

EATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x16 pinout, timing, functions and package
- 12 row, 10 column addresses
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- Extended Data-Out (EDO) PAGE MODE access
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) REFRESH distributed across 64ms
- Optional self refresh (S) for low-power data retention

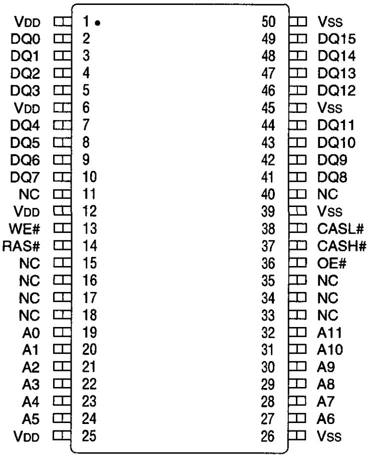
OPTIONS	MARKING
Plastic Package	
50-pin TSOP (400 mil)	TG
Timing	
50ns access	-5
60ns access	-6
Refresh Rates	
Standard Refresh	None
Self Refresh	S*

OTE: 1. The "#" symbol indicates signal is active LOW.

ontact factory for availability

PIN ASSIGNMENT (Top View)

50-Pin TSOP
(C-4)



EY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

MEG x 16 EDO DRAM PART NUMBERS

PART NUMBER	REFRESH ADDRESSING	PACKAGE	REFRESH
MT4LC4M16R6TG-x	4K	400-TSOP	Standard
MT4LC4M16R6TG-x S	4K	400-TSOP	Self

= speed

ENERAL DESCRIPTION

The MT4LC4M16R6 is a high-speed CMOS, dynamic ndom-access memory device containing 67,108,864 ts and designed to operate from 3V to 3.6V. The T4LC4M16R6 is functionally organized as 4,194,304 locaons containing 16 bits each. The 4,194,304 memory locations are arranged in 4,096 rows by 1,024 columns. During READ or WRITE cycles, each location is uniquely addressed via the address bits: 12 row address bits (A0-A11) and 10 column address bits (A0-A9). In addition, both byte and word accesses are supported via the two CAS# pins (CASL# and CASH#).

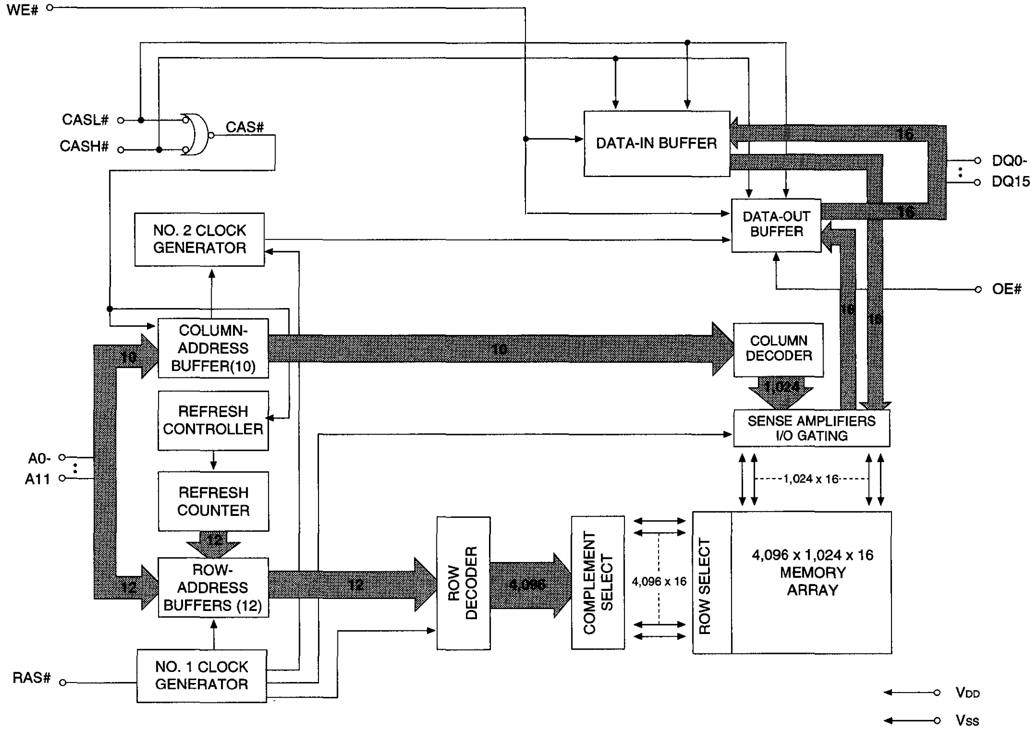
The CAS# functionality and timing related to address and control functions (e.g., latching column addresses or selecting CBR REFRESH) is such that the internal CAS# signal is determined by the first external CAS# signal (CASL# or CASH#) to transition LOW and the last to transition back HIGH. The CAS# functionality and timing related to driving or latching data is such that each CAS# signal independently controls the associated eight DQ pins.

The row address is latched by the RAS# signal, then the column address is latched by CAS#. This device provides EDO-PAGE-MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

The 4 Meg x 16 DRAM must be refreshed periodically in order to retain stored data.

FUNCTIONAL BLOCK DIAGRAM

MT4LC4M16R6 (12 row addresses)



DRAM ACCESS

Each location in the DRAM is uniquely addressable, as mentioned in the General Description. Use of both CAS# signals results in a word access via the 16 I/O pins (DQ0-DQ15). Using only one of the two signals results in a BYTE access cycle. CASL# transitioning LOW selects an access cycle for the lower byte (DQ0-DQ7), and CASH# transitioning LOW selects an access cycle for the upper byte (DQ8-DQ15). General byte and word access timing is shown in Figures 1 and 2.

A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS# (CASL# or CASH#), whichever occurs last. An EARLY WRITE occurs when WE is taken LOW prior to either CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE falls after CAS# (CASL# or CASH#) is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z, regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applyin input data. If a LATE WRITE or READ-MODIFY-WRITE attempted while keeping OE# LOW, no WRITE will occu and the data outputs will drive read data from the accesse location.

Additionally, both bytes must always be of the sar mode of operation if both bytes are active. A CAS# precharg must be satisfied prior to changing modes of operatio between the upper and lower bytes. For example, an EARL WRITE on one byte and a LATE WRITE on the other by are not allowed during the same cycle. However, an EARL WRITE on one byte and a LATE WRITE on the other byt after a CAS# precharge has been satisfied, are permissibl

EDO PAGE MODE

DRAM READ cycles have traditionally turned the ou put buffers off (High-Z) with the rising edge of CAS#. CAS# went HIGH and OE# was LOW (active), the outpu

DO PAGE MODE (continued)

uffers would be disabled. The MT4LC4M16R6 offers an ccelerated page mode cycle by eliminating output disable om CAS# HIGH. This option is called EDO, and it allows AS# precharge time (^{t}CP) to occur without the output data oing invalid (see READ and EDO-PAGE-MODE READ aveforms).

EDO operates like any DRAM READ or FAST-PAGE-ODE READ, except data is held valid after CAS# goes IGH, as long as RAS# and OE# are held LOW and WE# held HIGH. OE# can be brought LOW or HIGH while AS# and RAS# are LOW, and the DQs will transition tween valid data and High-Z. Using OE#, there are two ethods to disable the outputs and keep them disabled ıring the CAS# HIGH time. The first method is to have E# HIGH when CAS# transitions HIGH and keep OE# IGH for ^{t}OEHC thereafter. This will disable the DQs, and ey will remain disabled (regardless of the state of OE# ter that point) until CAS# falls again. The second method to have OE# LOW when CAS# transitions HIGH and then bring OE# HIGH for a minimum of ^{t}OEP anytime during the CAS# HIGH period. This will disable the DQs, and they will remain disabled (regardless of the state of OE# after that point) until CAS# falls again (see Figure 3). During other cycles, the outputs are disabled at ^{t}OFF time after RAS# and CAS# are HIGH or at ^{t}WHZ after WE# transitions LOW. The ^{t}OFF time is referenced from the rising edge of RAS# or CAS#, whichever occurs last. WE# can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 4.

EDO-PAGE-MODE operations are always initiated with a row address strobed in by the RAS# signal, followed by a column address strobed in by CAS#, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling CAS# while holding RAS# LOW and entering new column addresses with each CAS# cycle. Returning RAS# HIGH terminates the EDO-PAGE-MODE operation.

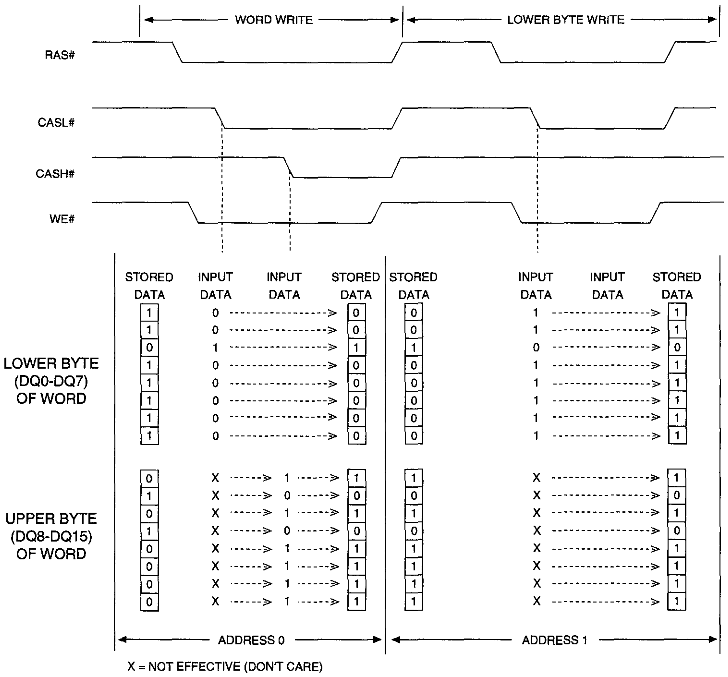


Figure 1
WORD AND BYTE WRITE EXAMPLE

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all rows in the 4 Meg x 16 DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The CBR REFRESH will invoke the internal refresh counter for automatic RAS# addressing. Alternatively, RAS#-ONLY REFRESH capability is inherently provided. However, with this method, some compatibility issues may become apparent. JEDEC strongly recommends the use of CBR REFRESH for this device.

An optional self refresh mode is also available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for th specified ᵗRASS. The "S" option allows the user the choic of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms or 31.25µs per row, when using a distributed CBR REFRESH. This refresh rate can be applied during norma operation, as well as during a standby or battery backu mode.

The self refresh mode is terminated by driving RAS HIGH for a minimum time of ᵗRPS. This delay allows for th completion of any internal refresh cycles that may be i process at the time of the RAS# LOW-to-HIGH transition. I the DRAM controller uses a distributed refresh sequence, burst refresh is not required upon exiting self refresh.

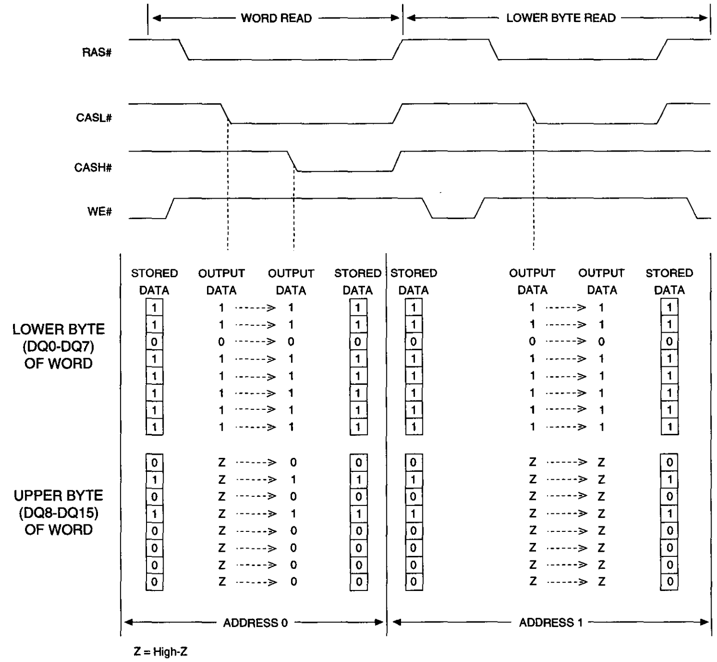
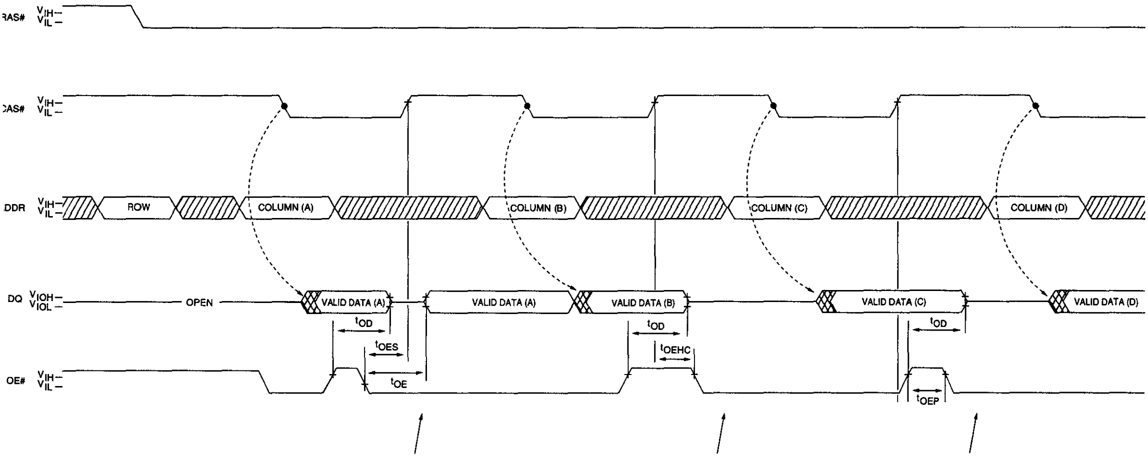


Figure 2
WORD AND BYTE READ EXAMPLE

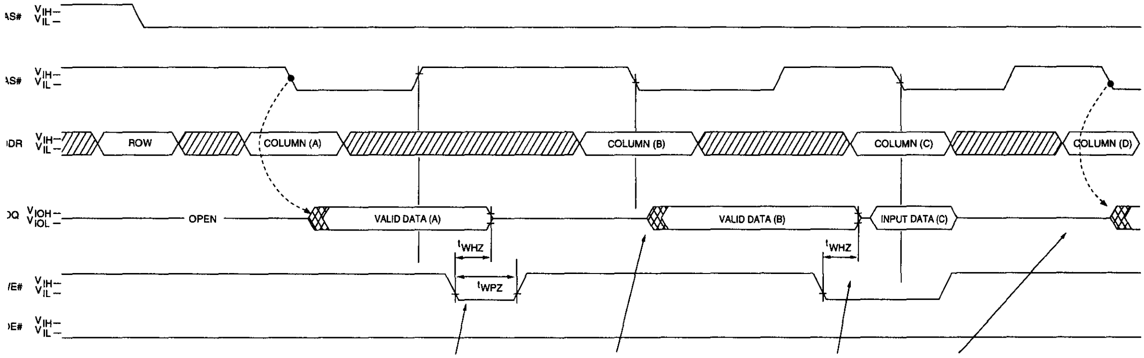


The DQs go back to Low-Z if tOES is met.

The DQs remain High-Z until the next CAS# cycle if tOEHC is met.

The DQs remain High-Z until the next CAS# cycle if tOEP is met.

Figure 3
OE# CONTROL OF DQs



The DQs go to High-Z if WE# falls and, if tWPZ is met, will remain High-Z until CAS# goes LOW with WE# HIGH (i.e., until a READ cycle is initiated).

WE# may be used to disable the DQs to prepare for input data in an EARLY WRITE cycle. The DQs will remain High-Z until CAS# goes LOW with WE# HIGH (i.e., until a READ cycle is initiated).

▨ DON'T CARE

▩ UNDEFINED

Figure 4
WE# CONTROL OF DQs

DRAM 1

FPM DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Address Pins		Package/No. of Pins		Page
				Row	Column	SOJ	TSOP	
3.3V FPM DRAMs								
16 Meg x 4	FPM, 8KR	MT4LC16M4A7	50, 60	13	11	32	32	1-69
16 Meg x 4	FPM, 8KR, S	MT4LC16M4A7 S	50, 60	13	11	32	32	1-69
16 Meg x 4	FPM, 4KR	MT4LC16M4T8	50, 60	12	12	32	32	1-69
16 Meg x 4	FPM, 4KR, S	MT4LC16M4T8 S	50, 60	12	12	32	32	1-69
8 Meg x 8	FPM, 8KR	MT4LC8M8E1	50, 60	13	10	32	32	1-73
8 Meg x 8	FPM, 8KR, S	MT4LC8M8E1 S	50, 60	13	10	32	32	1-73
8 Meg x 8	FPM, 4KR	MT4LC8M8B6	50, 60	12	11	32	32	1-73
8 Meg x 8	FPM, 4KR, S	MT4LC8M8B6 S	50, 60	12	11	32	32	1-73
4 Meg x 16	FPM, DC, 4KR	MT4LC4M16F5	50, 60	12	10	–	50	1-77
4 Meg x 16	FPM, DC, 4KR, S	MT4LC4M16F5 S	50, 60	12	10	–	50	1-77

FPM = FAST PAGE MODE; DC = Dual CAS; 4KR = 4,096 Refresh; 8KR = 8,192 Refresh; S = Self Refresh

DRAM

MT4LC16M4A7, MT4LC16M4T8

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

EATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x4 pinout, timing, functions and packages
- 13 row, 11 column addresses (A7)
- 12 row, 12 column addresses (T8)
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- FAST-PAGE-MODE (FPM) access
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) REFRESH distributed across 64ms
- Optional self refresh (S) for low-power data retention

PTIONS	MARKING
Refresh Addressing	
4,096 (4K) rows	T8
8,192 (8K) rows	A7
Plastic Packages	
32-pin SOJ (400 mil)	DJ
32-pin TSOP (400 mil)	TG
Timing	
50ns access	-5
60ns access	-6
Refresh Rates	
Standard Refresh	None
Self Refresh (128ms period)	S*

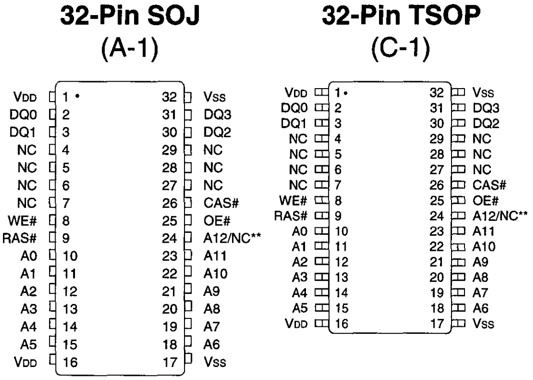
OTE: 1. The 16 Meg x 4 FPM DRAM base number differentiates the offerings in one place - MT4LC16M4A7. The fifth field distinguishes various options: A7 designates an 8K refresh and T8 designates a 4K refresh for FPM DRAMs.
2. The # symbol indicates signal is active LOW.

ontact factory for availability

EY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC
-5	90ns	50ns	30ns	25ns	13ns
-6	110ns	60ns	35ns	30ns	15ns

PIN ASSIGNMENT (Top View)



**A12 on A7 version and NC on T8 version

16 MEG x 4 FPM DRAM PART NUMBERS

PART NUMBER	REFRESH ADDRESSING	PACKAGE	REFRESH
MT4LC16M4A7DJ-x	8K	SOJ	Standard
MT4LC16M4A7DJ-x S	8K	SOJ	Self
MT4LC16M4A7TG-x	8K	TSOP	Standard
MT4LC16M4A7TG-x S	8K	TSOP	Self
MT4LC16M4T8DJ-x	4K	SOJ	Standard
MT4LC16M4T8DJ-x S	4K	SOJ	Self
MT4LC16M4T8TG-x	4K	TSOP	Standard
MT4LC16M4T8TG-x S	4K	TSOP	Self

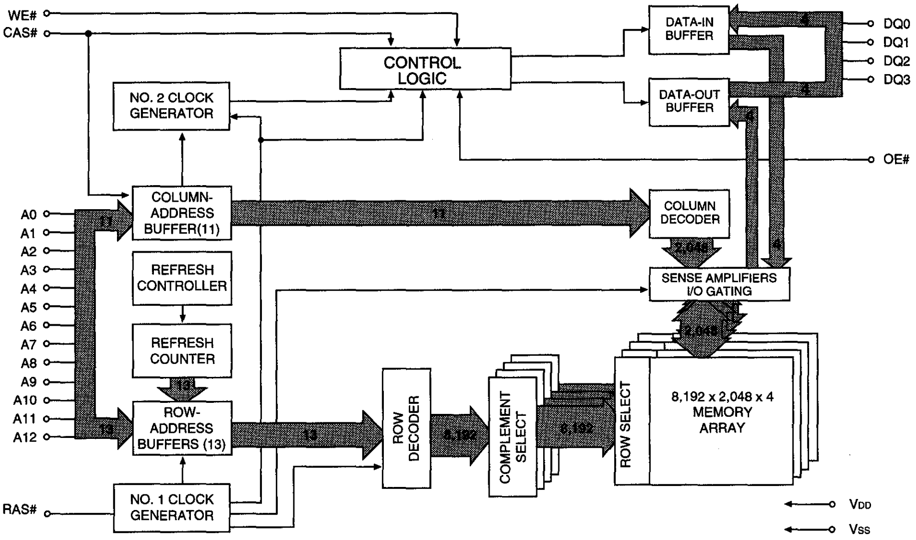
x = speed

ENERAL DESCRIPTION

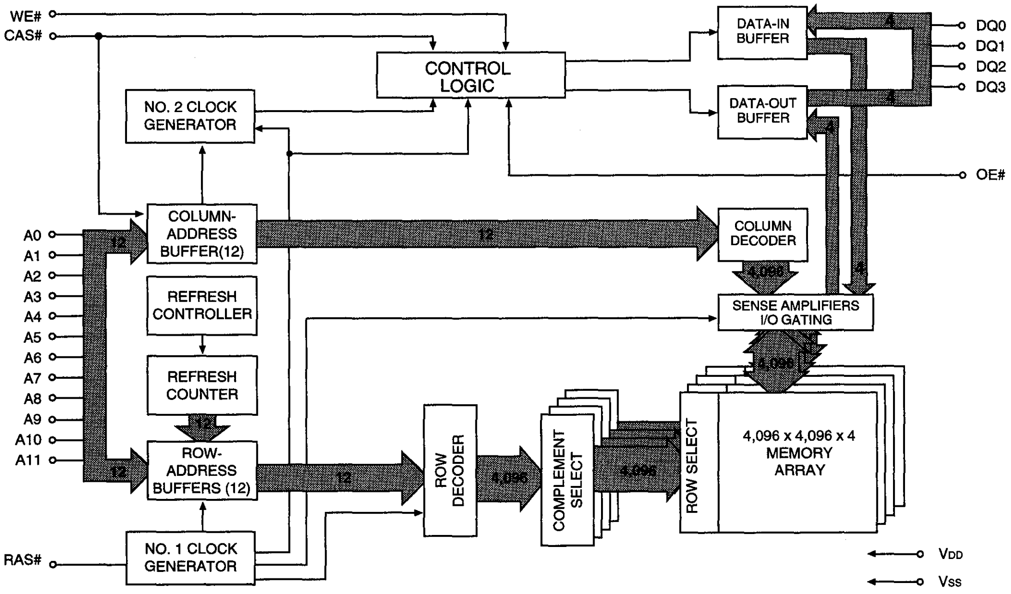
The MT4LC16M4A7 and MT4LC16M4T8 are high-speed MOS, dynamic random-access memory devices contain- g 67,108,864 bits organized in a x4 configuration. The T4LC16M4A7 and MT4LC16M4T8 are functionally orga- zed as 16,777,216 locations containing four bits each. The ,777,216 memory locations are arranged in 8,192 rows by 2,048 columns for the MT4LC16M4A7 or 4,096 rows by 4,096 columns for the MT4LC16M4T8. During READ or WRITE cycles, each location is uniquely addressed via the address bits. First, the row address is latched by the RAS# signal, then the column address by CAS#. Both devices provide FAST-PAGE-MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

The MT4LC16M4A7 and MT4LC16M4T8 must be refreshed periodically in order to retain stored data.

FUNCTIONAL BLOCK DIAGRAM
MT4LC16M4A7 (13 row addresses)



FUNCTIONAL BLOCK DIAGRAM
MT4LC16M4T8 (12 row addresses)



FAST PAGE MODE ACCESS

Each location in the DRAM is uniquely addressable as mentioned in the General Description. The data for each location is accessed via the four I/O pins (DQ0-DQ3). The WE# signal must be activated to execute a WRITE operation; otherwise, a READ operation will be performed. The OE# signal must be activated to enable the DQ output drivers for a read access and can be deactivated to disable output data if necessary.

FAST-PAGE-MODE operations are always initiated with a row address strobed in by the RAS# signal, followed by a column address strobed in by CAS#, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling CAS# while holding RAS# LOW and entering new column addresses with each CAS# cycle. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all 8,192 rows (A7) or all 4,096 rows (T8) in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC16M4A7 internally refreshes two rows for every CBR cycle, whereas the MT4LC16M4T8 refreshes one row for every CBR cycle. So with either device, executing 4,096 CBR cycles covers all rows. The CBR refresh will invoke the internal refresh counter for automatic RAS# addressing. Alternatively, RAS#-ONLY REFRESH capability is inherently provided. However, with this method only one row is refreshed at a time; so for the MT4LC16M4A7, 8,192 RAS#-ONLY REFRESH cycles must be executed every 64ms to cover all rows. Some compatibility issues may become apparent. JEDEC strongly recommends the use of CBR REFRESH for this device.

An optional self refresh mode is also available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^tRASS. The "S" option allows for an extended refresh period of 128ms, or 31.25µs per row for a 4K refresh and 15.625µs per row for an 8K refresh, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^tRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes RAS#-ONLY or burst refresh sequence, all rows must be refreshed within the average internal refresh rate prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

DRAM

MT4LC8M8E1, MT4LC8M8B6

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x8 pinout, timing, functions and packages
- 13 row, 10 column addresses (E1) or 12 row, 11 column addresses (B6)
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- FAST PAGE MODE (FPM) access
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) REFRESH distributed across 64ms
- Optional self refresh (S) for low-power data retention

OPTIONS	MARKING
• Refresh Addressing	
4,096 (4K) rows	B6
8,192 (8K) rows	E1
• Plastic Packages	
32-pin SOJ (400 mil)	DJ
32-pin TSOP (400 mil)	TG
• Timing	
50ns access	-5
60ns access	-6
• Refresh Rates	
Standard Refresh (32ms period)	None
Self Refresh (128ms period)	S*

NOTE: 1. The 8 Meg x 8 FPM DRAM base number differentiates the offerings in one place - MT4LC8M8E1. The fifth field distinguishes various options: E1 designates an 8K refresh and B6 designates a 4K refresh for FPM DRAMs.
2. The # symbol indicates signal is active LOW.

Contact factory for availability

KEY TIMING PARAMETERS

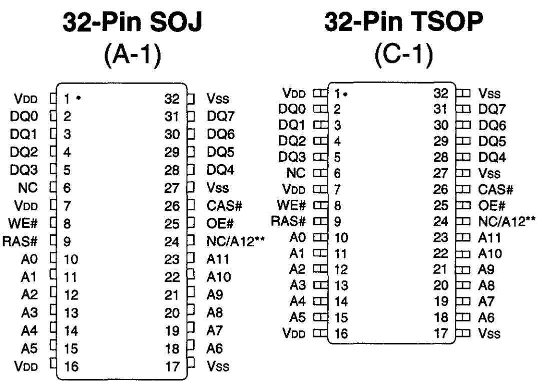
SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC
-5	90ns	50ns	30ns	25ns	13ns
-6	110ns	60ns	35ns	30ns	15ns

GENERAL DESCRIPTION

The MT4LC8M8E1 and MT4LC8M8B6 are high-speed CMOS, dynamic random-access memory devices contain- ıg 67,108,864 bits organized in a x8 configuration. The MT4LC8M8E1 and MT4LC8M8B6 are functionally orga- ized as 8,388,608 locations containing eight bits each. The ,388,608 memory locations are arranged in 8,192 rows by 1,024 columns for the MT4LC8M8E1 or 4,096 rows by 2,048 columns for the MT4LC8M8B6. During READ or WRITE cycles, each location is uniquely addressed via the address bits. First, the row address is latched by the RAS# signal, then the column address by CAS#. Both devices provide FAST-PAGE-MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

The MT4LC8M8E1 and MT4LC8M8B6 must be refreshed periodically in order to retain stored data.

PIN ASSIGNMENT (Top View)



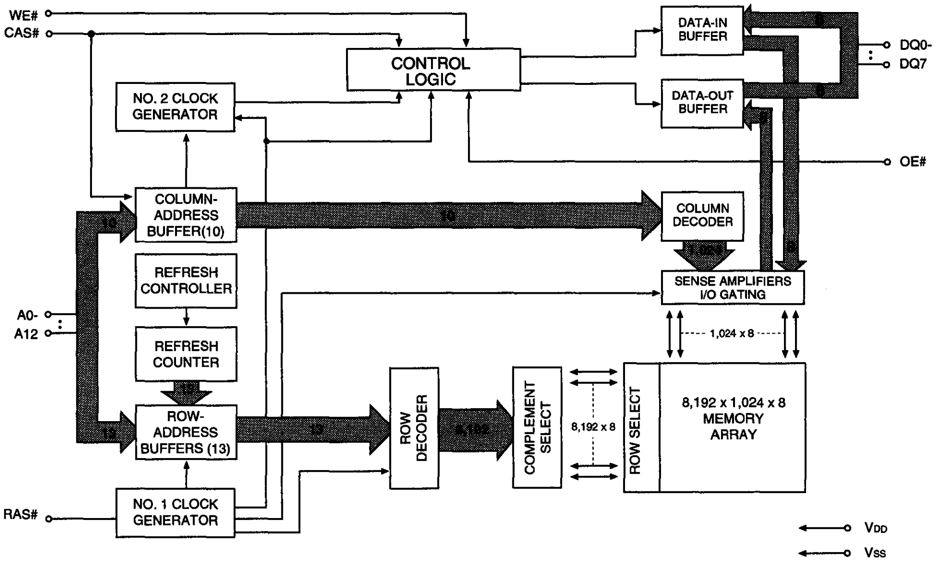
**A12 on E1 version, NC on B6 version

8 MEG x 8 FPM DRAM PART NUMBERS

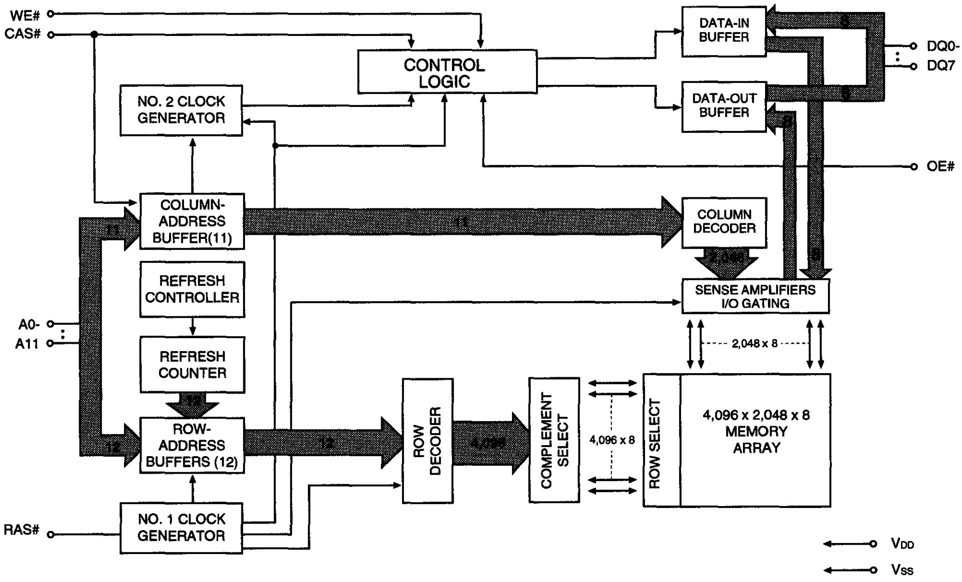
PART NUMBER	REFRESH ADDRESSING	PACKAGE	REFRESH
MT4LC8M8E1DJ-x	8K	SOJ	Standard
MT4LC8M8E1DJ-x S	8K	SOJ	Self
MT4LC8M8E1TG-x	8K	TSOP	Standard
MT4LC8M8E1TG-x S	8K	TSOP	Self
MT4LC8M8B6DJ-x	4K	SOJ	Standard
MT4LC8M8B6DJ-x S	4K	SOJ	Self
MT4LC8M8B6TG-x	4K	TSOP	Standard
MT4LC8M8B6TG-x S	4K	TSOP	Self

x = speed

FUNCTIONAL BLOCK DIAGRAM
MT4LC8M8E1 (13 row addresses)



FUNCTIONAL BLOCK DIAGRAM
MT4LC8M8B6 (12 row addresses)



FAST PAGE MODE ACCESS

Each location in the DRAM is uniquely addressable as mentioned in the General Description. The data for each location is accessed via the eight I/O pins (DQ0-DQ7). The WE# signal must be activated to execute a WRITE operation; otherwise, a READ operation will be performed. The OE# signal must be activated to enable the DQ output drivers for a read access and can be deactivated to disable output data if necessary.

FAST-PAGE-MODE operations are always initiated with a row address strobed in by the RAS# signal, followed by a column address strobed in by CAS#, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling CAS# while holding RAS# LOW and entering new column addresses with each CAS# cycle. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all 8,192 rows (E1) or all 4,096 rows (B6) in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC8M8E1 internally refreshes two rows for every CBR cycle, whereas the MT4LC8M8B6 refreshes one row for every CBR cycle. So with either device, executing 4,096 CBR cycles covers all rows. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing. Alternatively, RAS#-ONLY REFRESH capability is inherently provided. However, with this method only one row is refreshed at a time; so for the MT4LC8M8E1, 8,192 RAS#-ONLY REFRESH cycles must be executed every 64ms to cover all rows. Some compatibility issues may become apparent. JEDEC strongly recommends the use of CBR REFRESH for this device.

An optional self refresh mode is also available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^tRASS. The "S" option allows for an extended refresh period of 128ms, or 31.25µs per row for a 4K refresh and 15.625µs per row for an 8K refresh when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^tRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes RAS#-ONLY or burst refresh sequence, all rows must be refreshed within the average internal refresh rate prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

DRAM

MT4LC4M16F5

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x16 pinout, timing, functions and packages
- 12 row, 10 column addresses
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- FAST PAGE MODE (FPM) access
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) REFRESH distributed across 64ms
- Optional self refresh (S) for low-power data retention

OPTIONS MARKING

OPTIONS	MARKING
• Plastic Package	
50-pin TSOP (400 mil)	TG
• Timing	
50ns access	-5
60ns access	-6
• Refresh Rates	
Standard Refresh (16ms period)	None
Self Refresh (128ms period)	S*

- Part Number Example: MT4LC4M16F5TG-5

OTE: 1. The # symbol indicates signal is active LOW.

Contact factory for availability

EY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC
-5	90ns	50ns	30ns	25ns	13ns
-6	110ns	60ns	35ns	30ns	15ns

ENERAL DESCRIPTION

The MT4LC4M16F5 is a high-speed CMOS, dynamic andom-access memory device containing 67,108,864 bits rganized in a x16 configuration. The MT4LC4M16F5 is unctionally organized as 4,194,304 locations containing 16 its each. The 4,194,304 memory locations are arranged in ,096 rows by 1,024 columns. During READ or WRITE ycles, each location is uniquely addressed via the address its: 12 row-address bits (A0-A11) and 10 column-address its (A0-A9). In addition, both byte and word accesses are upported via the two CAS# pins (CASL# and CASH#).

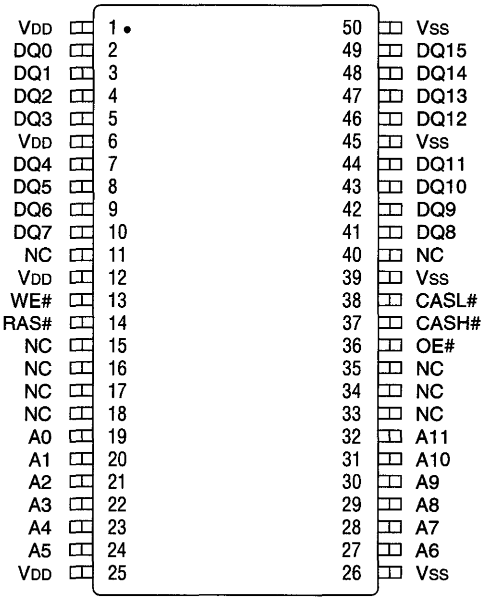
The CAS# functionality and timing related to address and control functions (e.g., latching column addresses or selecting CBR REFRESH) are such that the internal CAS# signal is determined by the first external CAS# signal (CASL# or CASH#) to transition LOW and the last to transition back HIGH. The CAS# functionality and timing related to driving or latching data are such that each CAS# signal independently controls the associated eight DQ pins.

The row address is latched by the RAS# signal, then the column address by CAS#. The device provides FAST-PAGE-MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

The MT4LC4M16F5 must be refreshed periodically in order to retain stored data.

PIN ASSIGNMENT (Top View)

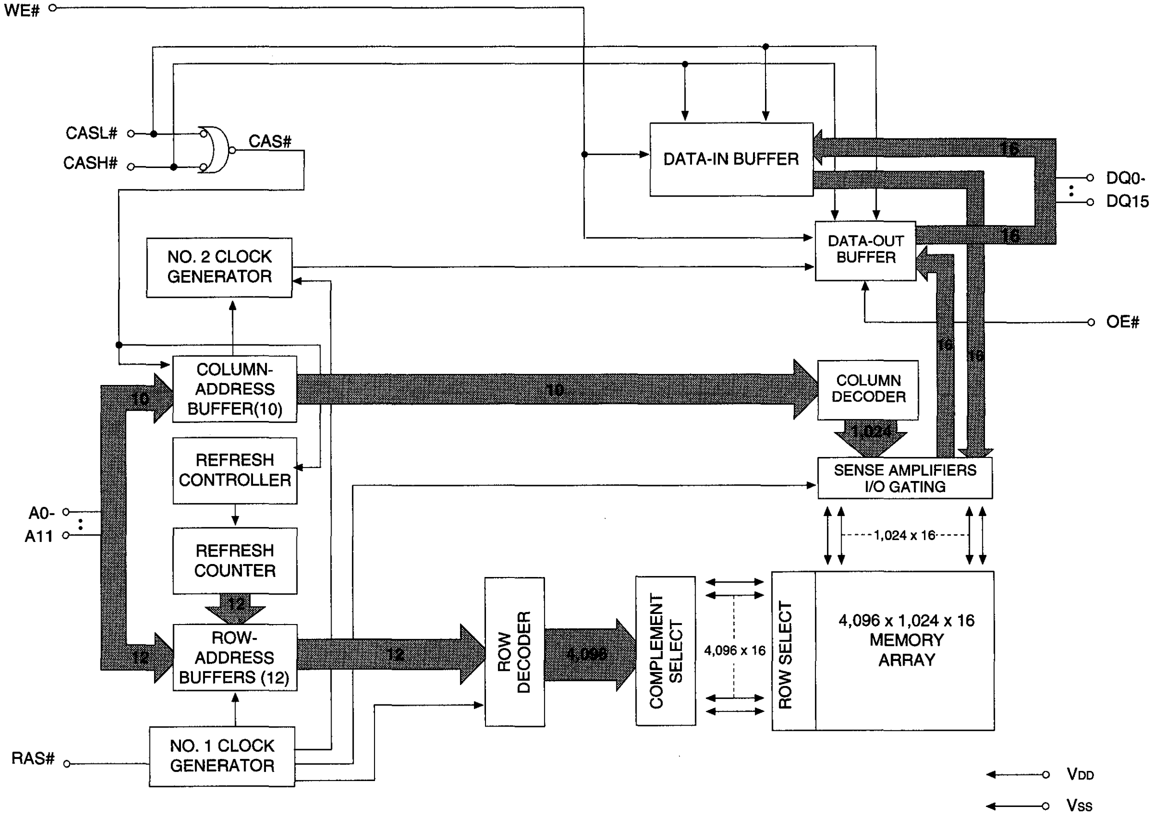
50-Pin TSOP
(C-4)



Signal	Pin	Pin	Signal
VDD	1	50	Vss
DQ0	2	49	DQ15
DQ1	3	48	DQ14
DQ2	4	47	DQ13
DQ3	5	46	DQ12
VDD	6	45	Vss
DQ4	7	44	DQ11
DQ5	8	43	DQ10
DQ6	9	42	DQ9
DQ7	10	41	DQ8
NC	11	40	NC
VDD	12	39	Vss
WE#	13	38	CASL#
RAS#	14	37	CASH#
NC	15	36	OE#
NC	16	35	NC
NC	17	34	NC
NC	18	33	NC
A0	19	32	A11
A1	20	31	A10
A2	21	30	A9
A3	22	29	A8
A4	23	28	A7
A5	24	27	A6
VDD	25	26	Vss

FUNCTIONAL BLOCK DIAGRAM

MT4LC4M16F5 (12 row addresses)



FAST PAGE MODE ACCESS

Each location in the DRAM is uniquely addressable, as mentioned in the General Description. Use of both CAS# signals results in a word access via the 16 I/O pins (DQ0-DQ15). Use of only one of the two results in a BYTE access cycle. CASL# transitioning LOW selects an access cycle for the lower byte (DQ0-DQ7) and CASH# transitioning LOW selects an access cycle for the upper byte (DQ8-DQ15). General byte and word access timing is shown in Figures 1 and 2.

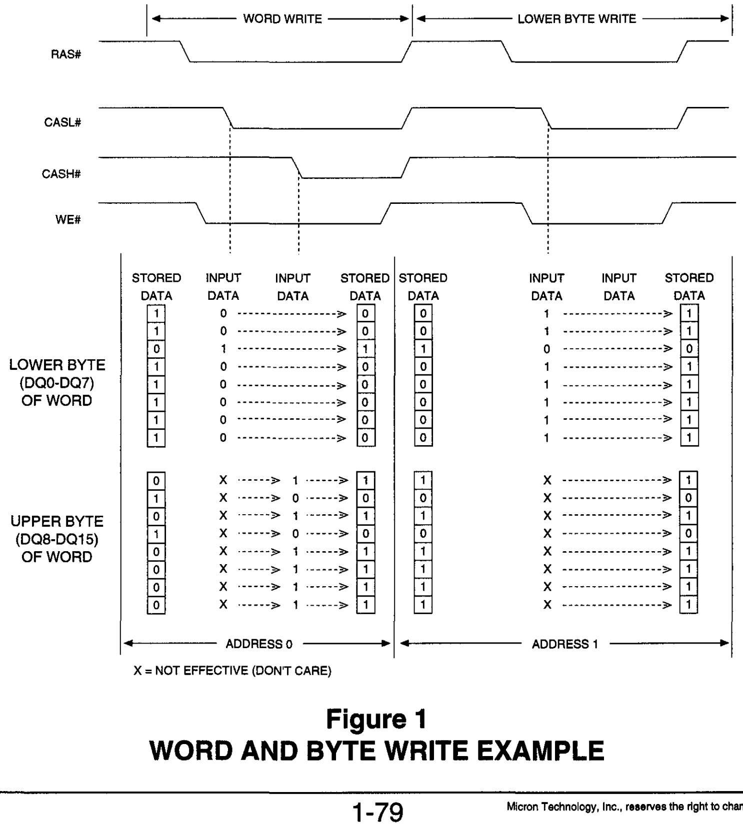
Additionally, both bytes must always be of the same mode of operation if both bytes are active. A CAS# precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY WRITE on one byte and a LATE WRITE on the other byte are not allowed during the same cycle. However, an EARLY WRITE on one byte and a LATE WRITE on the other byte, after a CAS# precharge has been satisfied, are permissible.

The WE# signal must be activated to execute a WRITE operation; otherwise a READ operation will be performed. The OE# signal must be activated to enable the DQ output drivers for a read access and can be deactivated to disable output data if necessary.

FAST-PAGE-MODE operations are always initiated with a row address strobed in by the RAS# signal, followed by a column address strobed in by CAS#, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling CAS# while holding RAS# LOW and entering new column addresses with each CAS# cycle. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all rows in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC4M16F5



X = NOT EFFECTIVE (DON'T CARE)

Figure 1
WORD AND BYTE WRITE EXAMPLE

DRAM REFRESH (continued)

internally refreshes one row for every CBR cycle, so executing 4,096 CBR cycles covers all rows. The CBR REFRESH will invoke the internal refresh counter for automatic RAS# addressing. Alternatively, RAS#-ONLY REFRESH capability is inherently provided. However, with this method some compatibility issues may become apparent. JEDEC strongly recommends the use of CBR REFRESH for this device.

An optional self refresh mode is available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^tRASS. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms, or 125µs per row, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^tRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

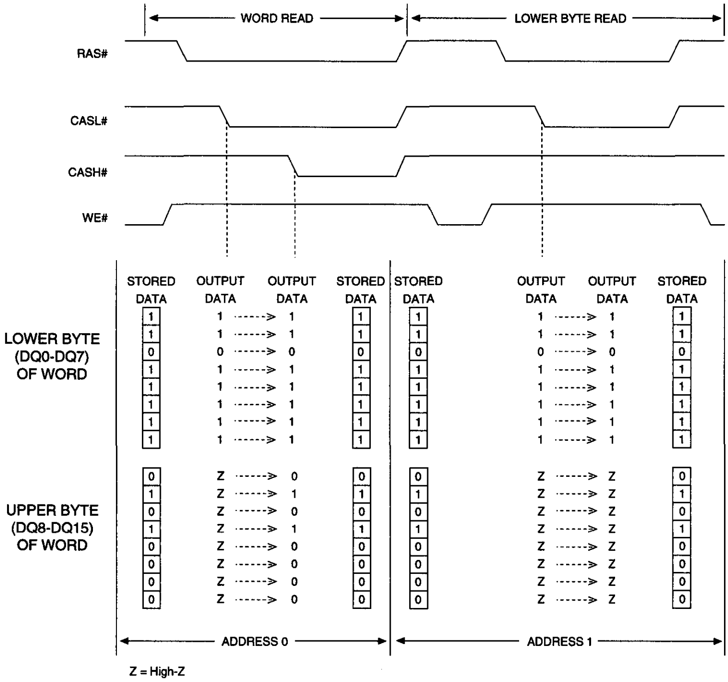


Figure 2
WORD AND BYTE READ EXAMPLE

RAM 1

SDRAM DIMM/SODIMM PRODUCT SELECTION GUIDE

Memory Configuration		Part Number	Clock Frequency (MHz)	Package and Number of Pins		Page
				SODIMM	DIMM	
Small-Outline DIMMs (SODIMMs)						
4 Meg x 64	3.3V	MT4LSDT464H	66	144	–	1-101
4 Meg x 64	3.3V	MT4LSDT464H	100	144	–	1-105
8 Meg x 64	3.3V	MT8LSDT864H	66	144	–	1-101
8 Meg x 64	3.3V	MT8LSDT864H	100	144	–	1-105
16 Meg x 64	3.3V	MT8LSDT1664H	66	144	–	1-113
DIMMs						
1 Meg x 32	3.3V	MT2LSDT132U	100	–	100	1-81
2 Meg x 32	3.3V	MT4LSDT232UD	100	–	100	1-81
4 Meg x 32	3.3V	MT2LSDT432U	100	–	100	1-85
8 Meg x 32	3.3V	MT4LSDT832UD	100	–	100	1-85
16 Meg x 32	3.3V	MT4LSDT1632UD	100	–	100	1-89
16 Meg x 32	3.3V	MT8LSDT1632U	100	–	100	1-93
32 Meg x 32	3.3V	MT8LSDT3232U	100	–	100	1-93
4 Meg x 64	3.3V	MT4LSDT464A	100, 66	–	168	1-97
8 Meg x 64	3.3V	MT8LSDT864A	100, 66	–	168	1-109
16 Meg x 64	3.3V	MT16LSDT1664A	100, 66	–	168	1-109
32 Meg x 64	3.3V	MT16LSDT3264A	100	–	168	1-117
4 Meg x 72	3.3V	MT5LSDT472A	100, 66	–	168	1-121
8 Meg x 72	3.3V	MT9LSDT872	100	–	168	1-125
8 Meg x 72	3.3V	MT9LSDT872A	100, 66	–	168	1-129
16 Meg x 72	3.3V	MT18LSDT1672A	100, 66	–	168	1-129
16 Meg x 72	3.3V	MT18LSDT1672	100	–	168	1-133
32 Meg x 72	3.3V	MT18LSDT3272	100	–	168	1-137
32 Meg x 72	3.3V	MT36LSDT3272	100	–	168	1-141
32 Meg x 72	3.3V	MT18LSDT3272A	100	–	168	1-145
64 Meg x 72	3.3V	MT36LSDT6472	100	–	168	1-149

SYNCHRONOUS DRAM MODULE

MT2LSDT132U, MT4LSDT232UD

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

EATURES

- JEDEC pinout in a 100-pin, dual in-line memory module (DIMM)
- 4MB (1 Meg x 32) and 8MB (2 Meg x 32)
- Utilizes 100 MHz SDRAM components
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)

PTIONS	MARKING
Package	
100-pin DIMM (gold)	G
Timing	
10ns cycle (≤100 MHz clock rate)	-10

EY SDRAM COMPONENT TIMING ARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2*	CL = 3*		
-10	100 MHz	–	7.5ns	3ns	1ns
-10	66 MHz	9ns	–	3ns	1ns

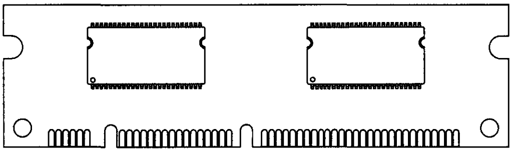
L = CAS (READ) latency

ART NUMBERS

ART NUMBER	CONFIGURATION	DEVICE PACKAGE
MT2LSDT132UG-10_	1 Meg x 32	TSOP
MT4LSDT232UDG-10_	2 Meg x 32	TSOP

OTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT2LSDT132UG-10C1.

PIN ASSIGNMENT (Front View)
100-Pin DIMM
(H-3; 4MB)
(H-4; 8MB)



PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK
1	Vss	26	Vss	51	Vss	76	Vss
2	DQ0	27	CKE0	52	DQ8	77	NC/CKE1*
3	DQ1	28	WE#	53	DQ9	78	DNU
4	DQ2	29	S0#	54	DQ10	79	NC/S1#*
5	DQ3	30	S2#	55	DQ11	80	NC/S3#*
6	VDD	31	VDD	56	VDD	81	VDD
7	DQ4	32	NC	57	DQ12	82	NC
8	DQ5	33	NC	58	DQ13	83	NC
9	DQ6	34	NC	59	DQ14	84	NC
10	DQ7	35	NC	60	DQ15	85	NC
11	DQMB0#	36	Vss	61	DQMB1#	86	Vss
12	Vss	37	DQMB2#	62	Vss	87	DQMB3#
13	A0	38	DQ16	63	A1	88	DQ24
14	A2	39	DQ17	64	A3	89	DQ25
15	A4	40	DQ18	65	A5	90	DQ26
16	A6	41	DQ19	66	A7	91	DQ27
17	A8	42	VDD	67	A9	92	VDD
18	A10	43	DQ20	68	BA0	93	DQ28
19	NC	44	DQ21	69	NC	94	DQ29
20	NC	45	DQ22	70	NC	95	DQ30
21	VDD	46	DQ23	71	VDD	96	DQ31
22	DNU	47	Vss	72	RAS#	97	Vss
23	RFU	48	SDA	73	CAS#	98	SA0
24	RFU	49	SCL	74	RFU	99	SA1
25	CK0	50	VDD	75	NC/CK1*	100	SA2

*8MB version only

GENERAL DESCRIPTION

The MT2LSDT132U and MT4LSDT232UD are high-speed CMOS, dynamic random-access, 4MB and 8MB memories organized in a x32 configuration. These modules use SDRAMs that are internally configured as dual memory arrays with a synchronous interface (all signals are registered on the positive edge of the clock signal CK0).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed

GENERAL DESCRIPTION (continued)

sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 selects the bank; A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The modules provide for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

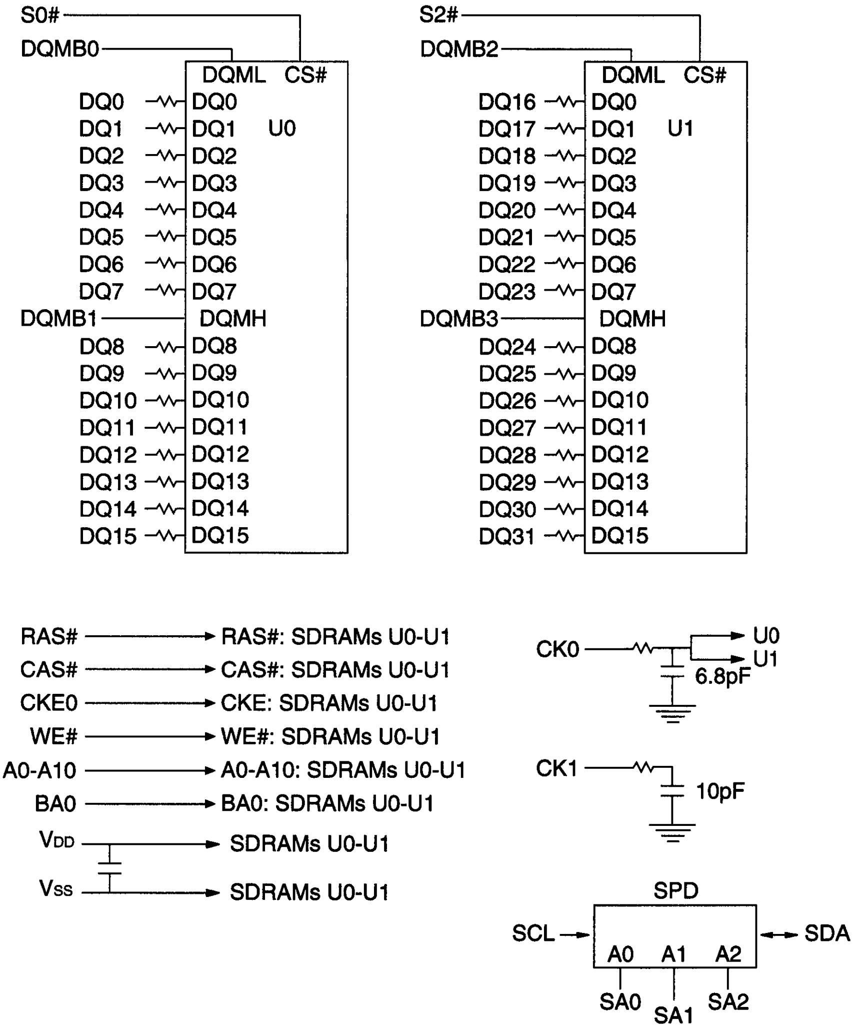
The modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 16Mb: x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

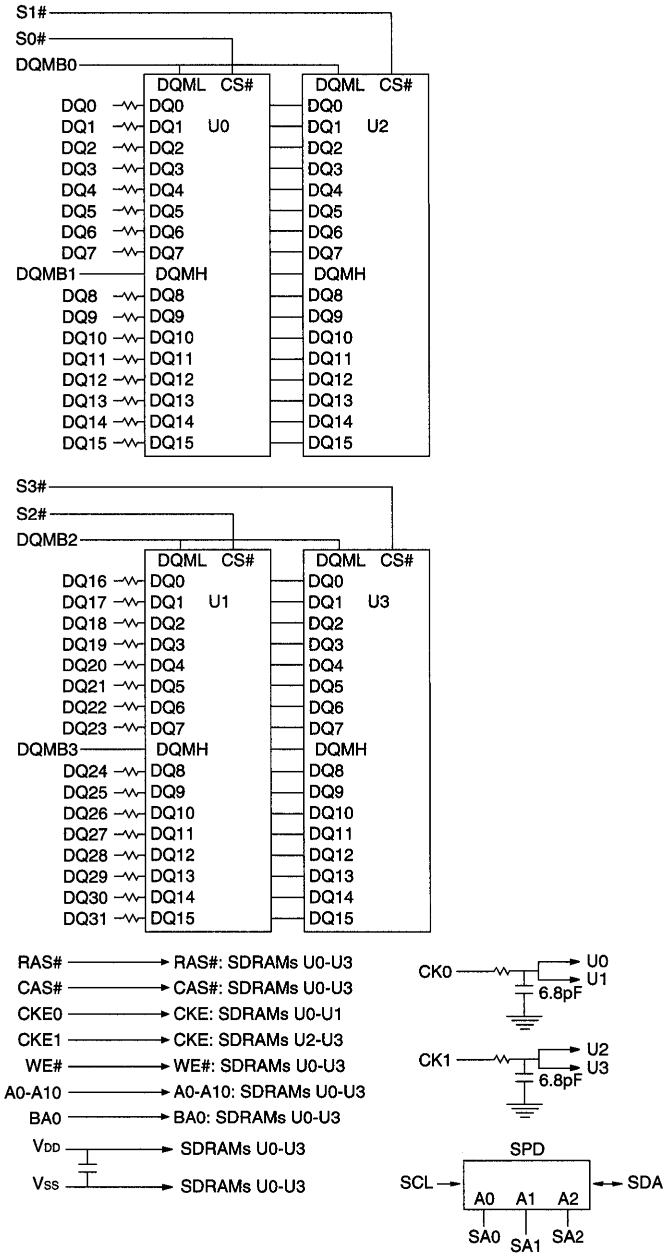
These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The firs 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT2LSDT132U (4MB)



NOTE: All resistor values are 10 ohms. U0-U1 = MT48LC1M16A1TG SDRAMs

FUNCTIONAL BLOCK DIAGRAM
MT4LSDT232UD (8MB)



NOTE: All resistor values are 10 ohms. U0-U3 = MT48LC1M16A1TG SDRAMs

SYNCHRONOUS RAM MODULE

MT2LSDT432U, MT4LSDT832UD

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/ datasheet.html

EATURES

- JEDEC pinout in a 100-pin, dual in-line memory module (DIMM)
- 16MB (4 Meg x 32) and 32MB (8 Meg x 32)
- Utilizes 100 MHz SDRAM components
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)

PTIONS — MARKING

Package	
100-pin DIMM (gold)	G
Timing	
10ns cycle (≤100 MHz clock rate)	-10

EY SDRAM COMPONENT TIMING ARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2*	CL = 3*		
-10	100 MHz	9ns	7ns	3ns	1ns

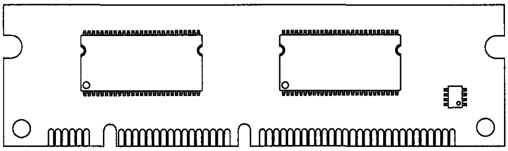
L = CAS (READ) latency

ART NUMBERS

ART NUMBER	CONFIGURATION	DEVICE PACKAGE
MT2LSDT432UG-10_	4 Meg x 32	TSOP
MT4LSDT832UDG-10_	8 Meg x 32	TSOP

OTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT2LSDT432UG-10D1.

PIN ASSIGNMENT (Front View)
100-Pin DIMM
(H-6; 16MB)
(H-5; 32MB)



PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK
1	Vss	26	Vss	51	Vss	76	Vss
2	DQ0	27	CKE0	52	DQ8	77	NC/CKE1**
3	DQ1	28	WE#	53	DQ9	78	DNU
4	DQ2	29	S0#	54	DQ10	79	NC/S1#**
5	DQ3	30	S2#	55	DQ11	80	NC/S3#**
6	VDD	31	VDD	56	VDD	81	VDD
7	DQ4	32	NC	57	DQ12	82	NC
8	DQ5	33	NC	58	DQ13	83	NC
9	DQ6	34	NC	59	DQ14	84	NC
10	DQ7	35	NC	60	DQ15	85	NC
11	DQMB0#	36	Vss	61	DQMB1#	86	Vss
12	Vss	37	DQMB2#	62	Vss	87	DQMB3#
13	A0	38	DQ16	63	A1	88	DQ24
14	A2	39	DQ17	64	A3	89	DQ25
15	A4	40	DQ18	65	A5	90	DQ26
16	A6	41	DQ19	66	A7	91	DQ27
17	A8	42	VDD	67	A9	92	VDD
18	A10	43	DQ20	68	BA0	93	DQ28
19	BA1	44	DQ21	69	A11	94	DQ29
20	NC (A12)	45	DQ22	70	NC (A13)	95	DQ30
21	VDD	46	DQ23	71	VDD	96	DQ31
22	DNU	47	Vss	72	RAS#	97	Vss
23	RFU	48	SDA	73	CAS#	98	SA0
24	RFU	49	SCL	74	RFU	99	SA1
25	CK0	50	VDD	75	NC/CK1**	100	SA2

**32MB version only

NOTE: Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

ENERAL DESCRIPTION

The MT2LSDT432U and MT4LSDT832UD are high-speed MOS, dynamic random-access, 16MB and 32MB solid-tate memories organized in a x32 configuration. These modules are configured as dual banks with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0 and CK1).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an AC-

GENERAL DESCRIPTION (continued)

TIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 selects the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The modules provide for a programmable READ or WRITE burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

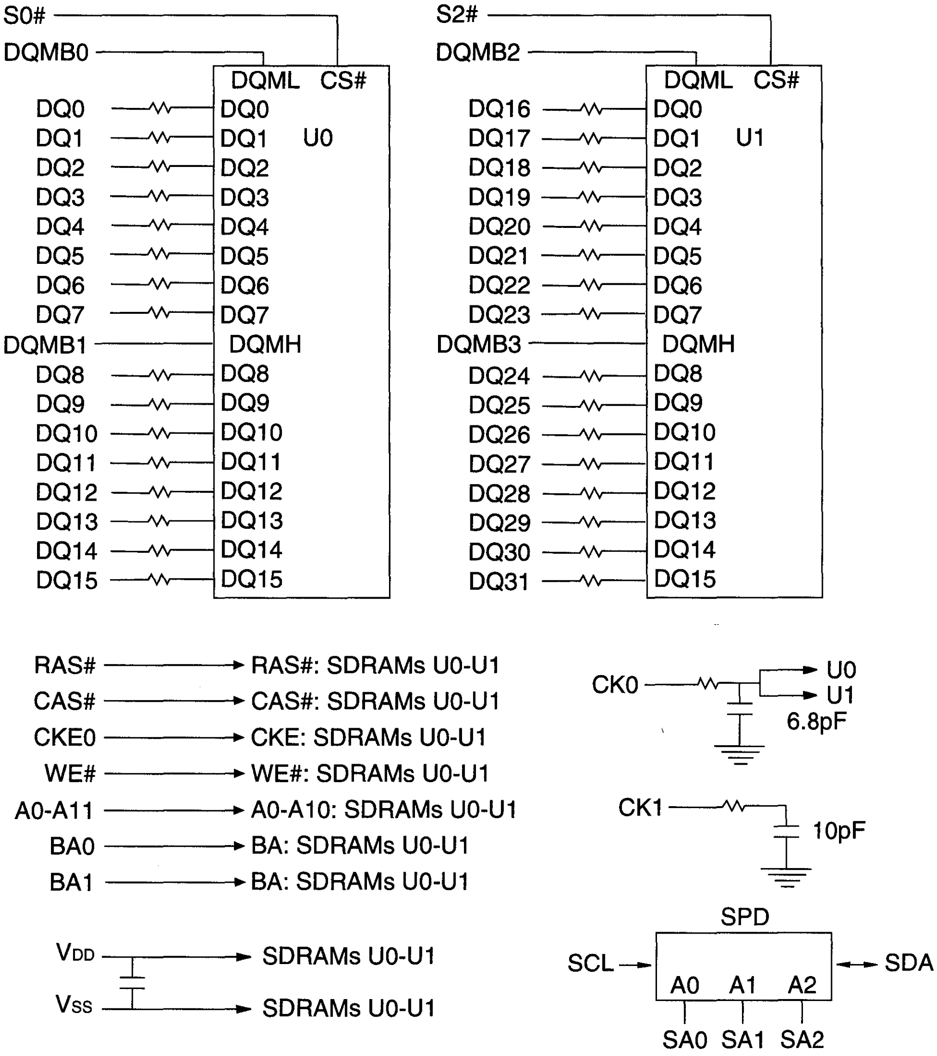
The modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64 Meg: x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

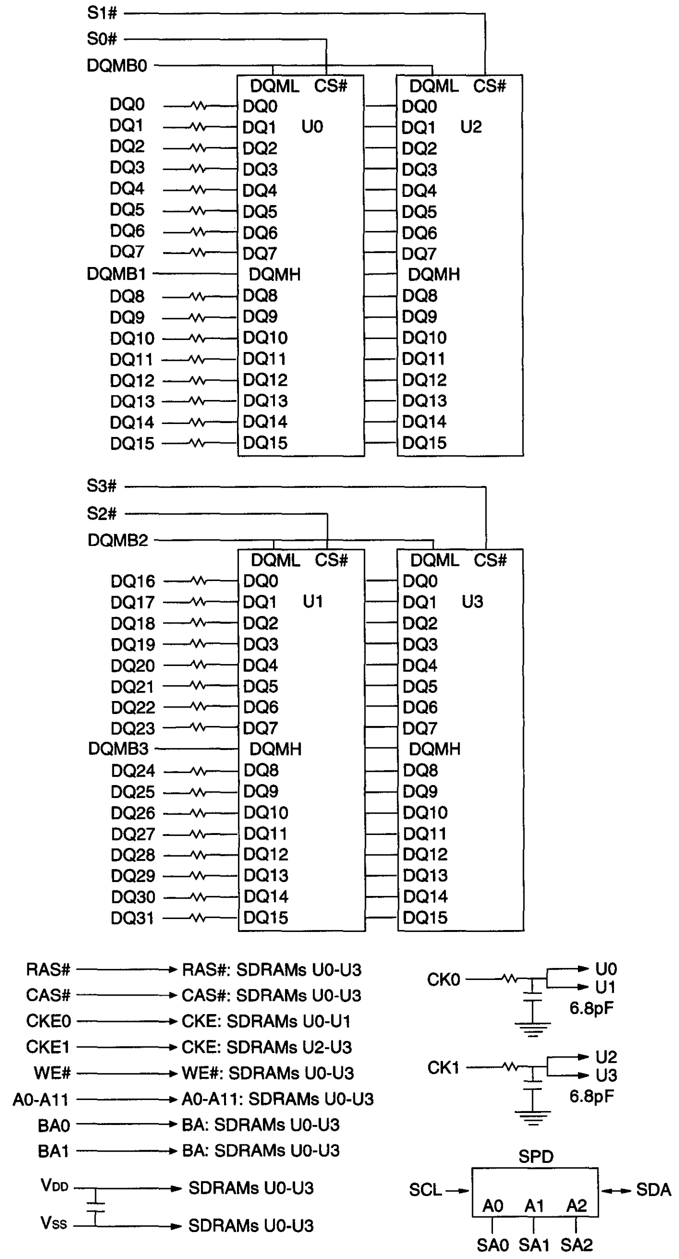
FUNCTIONAL BLOCK DIAGRAM
MT2LSDT432U (16MB)



NOTE: All resistor values are 10 ohms.

U0-U1 = MT48LC4M16A2TG SDRAMs

FUNCTIONAL BLOCK DIAGRAM
MT4LSDT832UD (32MB)



NOTE: All resistor values are 10 ohms.

U0-U3 = MT48LC4M16A2TG SDRAMs

ADVANCE

MICRON TECHNOLOGY, INC.

16 MEG x 32
SDRAM DIMM

SYNCHRONOUS DRAM MODULE

MT4LSDT1632UD

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC pinout in a 100-pin, dual in-line memory module (DIMM)
- 64MB (16 Meg x 32)
- Utilizes 100 MHz SDRAM components
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)

OPTIONS	MARKING
• Package	
100-pin DIMM (gold)	G
• Timing	
10ns cycle (≤100 MHz clock rate)	-10

KEY SDRAM COMPONENT TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2*	CL = 3*		
-10	100 MHz	9ns	7ns	3ns	1ns

*CL = CAS (READ) latency

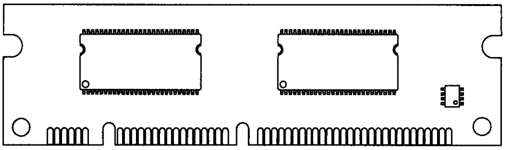
PART NUMBER

PART NUMBER	CONFIGURATION	DEVICE PACKAGE
MT4LSDT1632UDG-10_	16 Meg x 32	TSOP

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT4LSDT1632UDG-10D1.

PIN ASSIGNMENT (Front View)

100-Pin DIMM
(H-5)



PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK
1	Vss	26	Vss	51	Vss	76	Vss
2	DQ0	27	CKE0	52	DQ8	77	CKE1
3	DQ1	28	WE#	53	DQ9	78	DNU
4	DQ2	29	S0#	54	DQ10	79	S1#
5	DQ3	30	S2#	55	DQ11	80	S3#
6	VDD	31	VDD	56	VDD	81	VDD
7	DQ4	32	NC	57	DQ12	82	NC
8	DQ5	33	NC	58	DQ13	83	NC
9	DQ6	34	NC	59	DQ14	84	NC
10	DQ7	35	NC	60	DQ15	85	NC
11	DQMB0	36	Vss	61	DQMB1	86	Vss
12	Vss	37	DQMB2	62	Vss	87	DQMB3
13	A0	38	DQ16	63	A1	88	DQ24
14	A2	39	DQ17	64	A3	89	DQ25
15	A4	40	DQ18	65	A5	90	DQ26
16	A6	41	DQ19	66	A7	91	DQ27
17	A8	42	VDD	67	A9	92	VDD
18	A10	43	DQ20	68	BA0	93	DQ28
19	BA1	44	DQ21	69	A11	94	DQ29
20	NC	45	DQ22	70	NC	95	DQ30
21	VDD	46	DQ23	71	VDD	96	DQ31
22	DNU	47	Vss	72	RAS#	97	Vss
23	RFU	48	SDA	73	CAS#	98	SA0
24	RFU	49	SCL	74	RFU	99	SA1
25	CK0	50	VDD	75	CK1	100	SA2

GENERAL DESCRIPTION

The MT4LSDT1632UD is a high-speed CMOS, dynamic random-access, 64MB solid-state memory organized in a x32 configuration. This module is configured as dual banks with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0 and CK1).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an AC-

GENERAL DESCRIPTION (continued)

TIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The module provides for a programmable READ or WRITE burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the precharge cycles and provide seamless, high-speed, random-access operation.

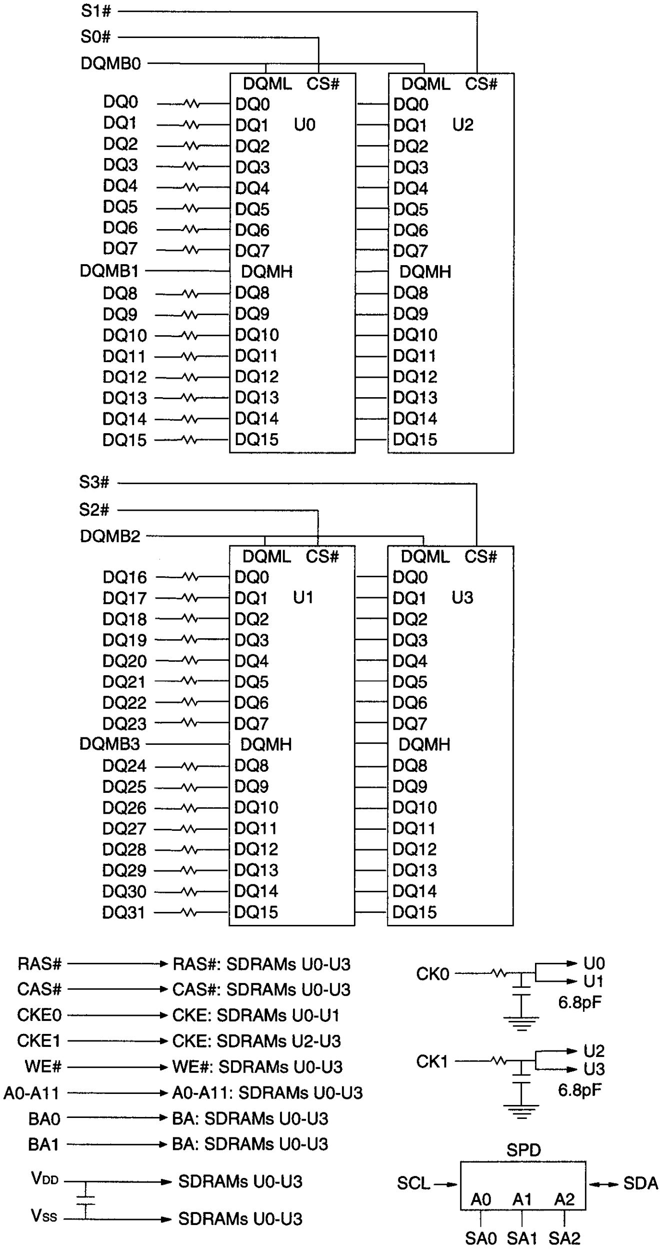
The module is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 128Mb: x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT4LSDT1632UD (64MB)



NOTE: All resistor values are 10 ohms.

U0-U3 = MT48LC8M16A2TG SDRAMs

SYNCHRONOUS DRAM MODULE

MT8LSDT1632U, MT8LSDT3232U

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

EATURES

- JEDEC pinout in a 100-pin, dual in-line memory module (DIMM)
- 64MB (16 Meg x 32), 128MB (32 Meg x 32)
- Utilizes 125 MHz SDRAM components
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)

PTIONS	MARKING
Package	
100-pin DIMM (gold)	G
Timing	
10ns cycle (≤100 MHz clock rate)	-10

EY SDRAM COMPONENT TIMING ARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2*	CL = 3*		
-10	100 MHz	9ns	7ns	3ns	1ns

L = CAS (READ) latency

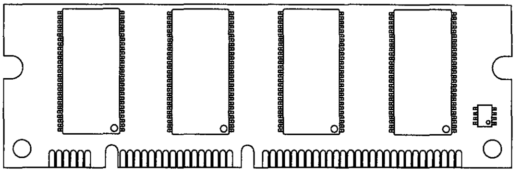
ART NUMBERS

ART NUMBER	CONFIGURATION	DEVICE PACKAGE
T8LSDT1632UG-10__	16 Meg x 32	TSOP
T8LSDT3232UG-10__	32 Meg x 32	TSOP

OTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8LSDT3232UG-10D1.

PIN ASSIGNMENT (Front View)

100-Pin DIMM
(H-7)



PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK
1	VSS	26	VSS	51	VSS	76	VSS
2	DQ0	27	CKE0	52	DQ8	77	CKE1
3	DQ1	28	WE#	53	DQ9	78	DNU
4	DQ2	29	S0#	54	DQ10	79	S1#
5	DQ3	30	S2#	55	DQ11	80	S3#
6	VDD	31	VDD	56	VDD	81	VDD
7	DQ4	32	NC	57	DQ12	82	NC
8	DQ5	33	NC	58	DQ13	83	NC
9	DQ6	34	NC	59	DQ14	84	NC
10	DQ7	35	NC	60	DQ15	85	NC
11	DQMB0	36	VSS	61	DQMB1	86	VSS
12	VSS	37	DQMB2	62	VSS	87	DQMB3
13	A0	38	DQ16	63	A1	88	DQ24
14	A2	39	DQ17	64	A3	89	DQ25
15	A4	40	DQ18	65	A5	90	DQ26
16	A6	41	DQ19	66	A7	91	DQ27
17	A8	42	VDD	67	A9	92	VDD
18	A10	43	DQ20	68	BA0	93	DQ28
19	BA1	44	DQ21	69	A11	94	DQ29
20	NC	45	DQ22	70	NC	95	DQ30
21	VDD	46	DQ23	71	VDD	96	DQ31
22	DNU	47	VSS	72	RAS#	97	VSS
23	RFU	48	SDA	73	CAS#	98	SA0
24	RFU	49	SCL	74	RFU	99	SA1
25	CK0	50	VDD	75	CK1	100	SA2

GENERAL DESCRIPTION

The MT8LSDT1632U and MT8LSDT3232U are high-speed CMOS, dynamic random-access, 64MB and 128MB solid-state memories organized in a x32 configuration. These modules use internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0 and CK1).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed

GENERAL DESCRIPTION (continued)

sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The modules provide for a programmable READ or WRITE burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the precharge cycles and provide seamless, high-speed, random-access operation.

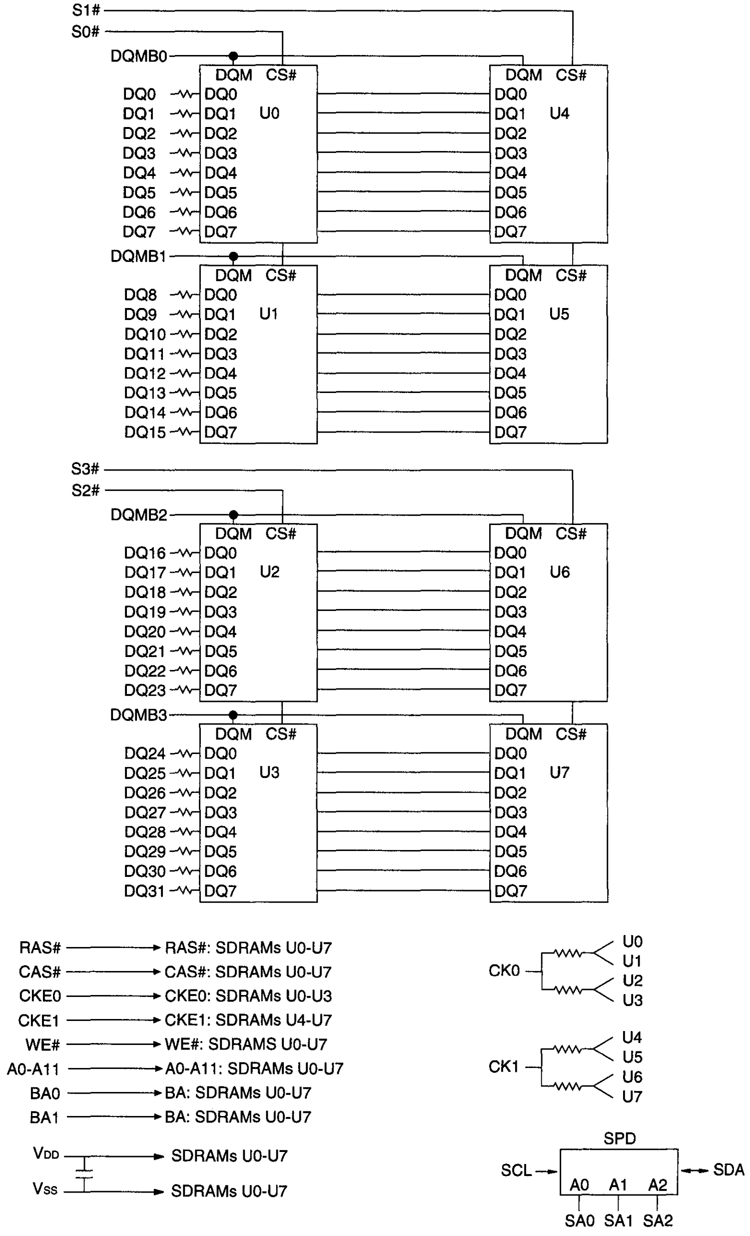
The modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb: x4, x8, x16 SDRAM data sheet or the 128Mb: x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD) The SPD function is implemented using a 2,048-bit EEPROM This nonvolatile storage device contains 256 bytes. The firs 128 bytes can be programmed by Micron to identify the module type and various DRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals together with SA(2:0), which provide eight unique DIMM/ EEPROM addresses.

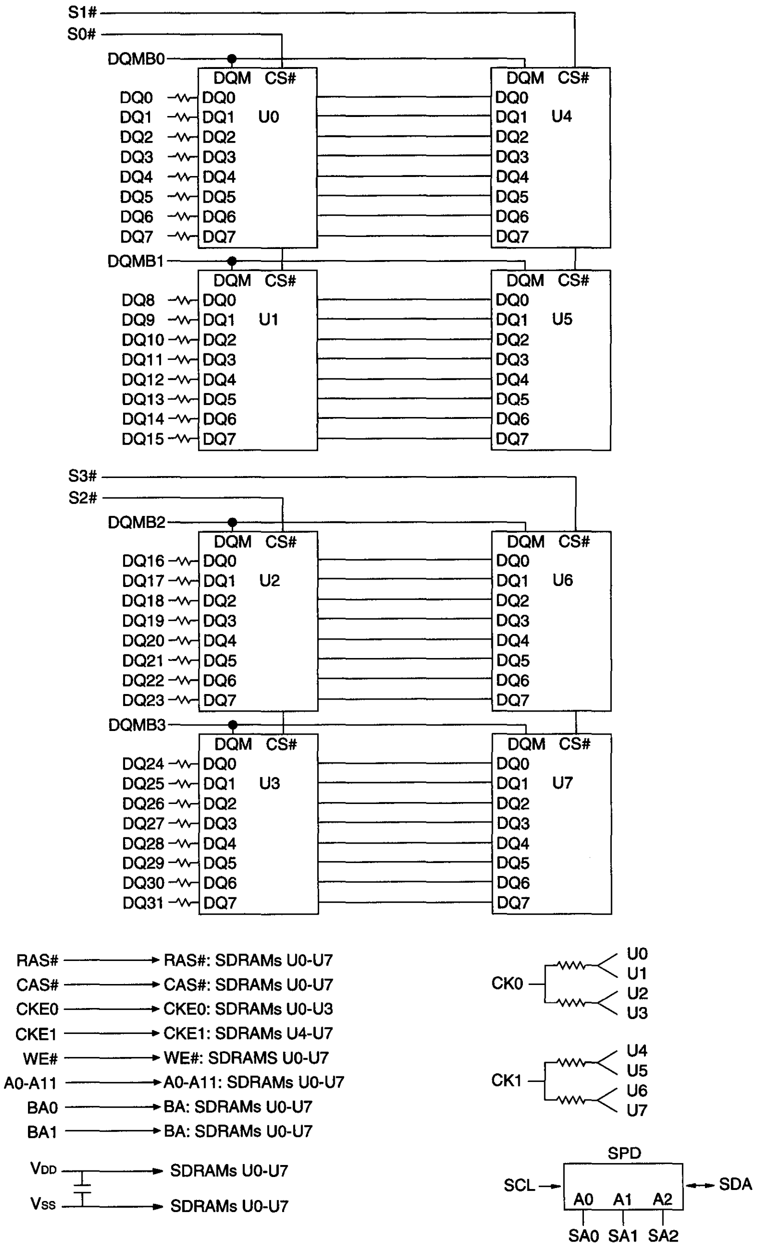
FUNCTIONAL BLOCK DIAGRAM
MT8LSDT1632U (64MB)



NOTE: All resistor values are 10 ohms.

U0-U7 = MT48LC8M8A2TG SDRAMs

FUNCTIONAL BLOCK DIAGRAM
MT8LSDT3232U (128MB)



NOTE: All resistor values are 10 ohms.

U0-U7 = MT48LC16M8A2TG SDRAMs

SYNCHRONOUS DRAM MODULE

MT4LSDT464A

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- PC100-compliant; includes CONCURRENT AUTO PRECHARGE
- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- Utilizes 100 MHz and 125 MHz SDRAM components
- Nonbuffered
- 32MB (4 Meg x 64)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (^{t}WR) version; one-clock ^{t}WR not supported

OPTIONS MARKING

OPTIONS	MARKING
Package	
168-pin DIMM (gold)	G
Frequency/CAS Latency	
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10C
66 MHz/CL = 2 (10ns, 100 MHz SDRAMs)	-662

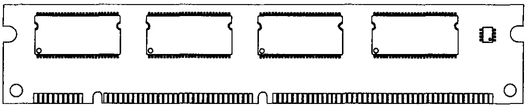
KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIMES	HOLD TIMES
-10E	-8E	2	6ns	2ns	1ns
-10C	-8C	3	6ns	2ns	1ns
-662	-10	2	9ns	3ns	1ns

NOTE: Pin symbols in parentheses are not used on this module but may be used for other modules in this product family. They are for reference only.

PIN ASSIGNMENT (Front View)

168-Pin DIMM
(H-8)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	NC (S3#)
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	DNU	90	VDD	132	NC (A13)
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	NC (CKE1)	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	Vss	110	VDD	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	NC (S1#)	156	DQ59
31	DNU	73	VDD	115	RAS#	157	VDD
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	NC/WP*	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CK1	167	SA2
42	CK0	84	VDD	126	NC (A12)	168	VDD

*-10C/-10E versions only

Micron Technology, Inc., reserves the right to change products or specifications without notice.

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT4LSDT464AG-10E__	4 Meg x 64	100 MHz
MT4LSDT464AG-10C__	4 Meg x 64	100 MHz
MT4LSDT464AG-662__	4 Meg x 64	66 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT4LSDT464AG-10EB2.

GENERAL DESCRIPTION

The MT4LSDT464A is a high-speed CMOS, dynamic random-access, 32MB memory organized in a x64 configuration. This module uses internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK3).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The module provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

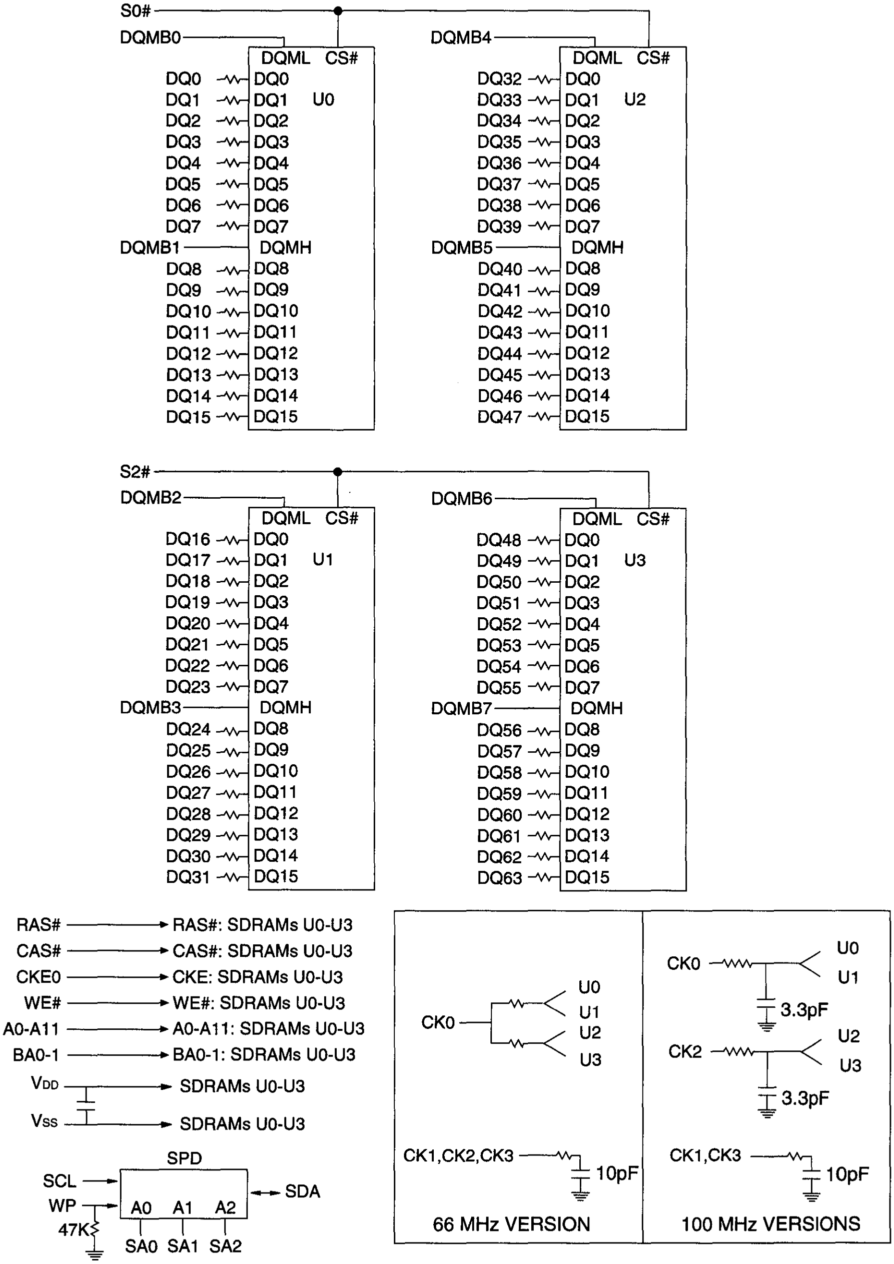
The module is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb: x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT4LSDT464A (32MB)



NOTE: All resistor values are 10 ohms.

U0-U3 = MT48LC4M16A2TG SDRAMs

SMALL-OUTLINE SDRAM MODULE

MT4LSDT464H, MT8LSDT864H

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/ datasheet.html

FEATURES

- JEDEC-standard 144-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 100 MHz SDRAM components
- Nonbuffered
- 32MB (4 Meg x 64) and 64MB (8 Meg x 64)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (^{t}WR) version; one-clock ^{t}WR not supported

OPTIONS	MARKING
• Package	
144-pin SODIMM (gold)	G
• Frequency/CAS Latency	
66 MHz/CL = 2 (10ns, 100 MHz SDRAMs)	-662
• Module Height	
1.150" (32MB)	-662_1
1.000" (32MB)	-662_2
1.050" (64MB)	-662_3

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	CLOCK FREQUENCY	SPEED GRADE	ACCESS TIME	SETUP TIME	HOLD TIME
-662	100 MHz	-10	9ns	3ns	1ns

PART NUMBERS

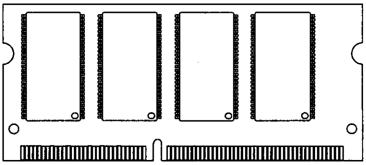
PART NUMBER	CONFIGURATION	VERSION
MT4LSDT464HG-662__	4 Meg x 64	66 MHz, CL = 2
MT8LSDT864HG-662__	8 Meg x 64	66 MHz, CL = 2

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8LSDT864HG-662C1.

PIN ASSIGNMENT (Front View)

144-Pin Small-Outline DIMM

(I-3; 32MB, 1.00")
(I-8; 32MB, 1.15")
(I-5; 64MB)



PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	Vss	2	Vss	73	DNU	74	CK1
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	VDD	46	VDD	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	NC	58	NC	129	VDD	130	VDD
59	NC	60	NC	131	DQ28	132	DQ60
61	CK0	62	CKE0	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	RAS#	66	CAS#	137	DQ31	138	DQ63
67	WE#	68	RFU (CKE1)	139	Vss	140	Vss
69	S0#	70	RFU (A12)	141	SDA	142	SCL
71	RFU (S1#)	72	RFU (A13)	143	VDD	144	VDD

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

GENERAL DESCRIPTION

The MT4LSDT464H and MT8LSDT864H are high-speed CMOS, dynamic random-access, 32MB and 64MB memories organized in a x64 configuration. These modules use SDRAMs that are internally configured as quad-bank DRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK1).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

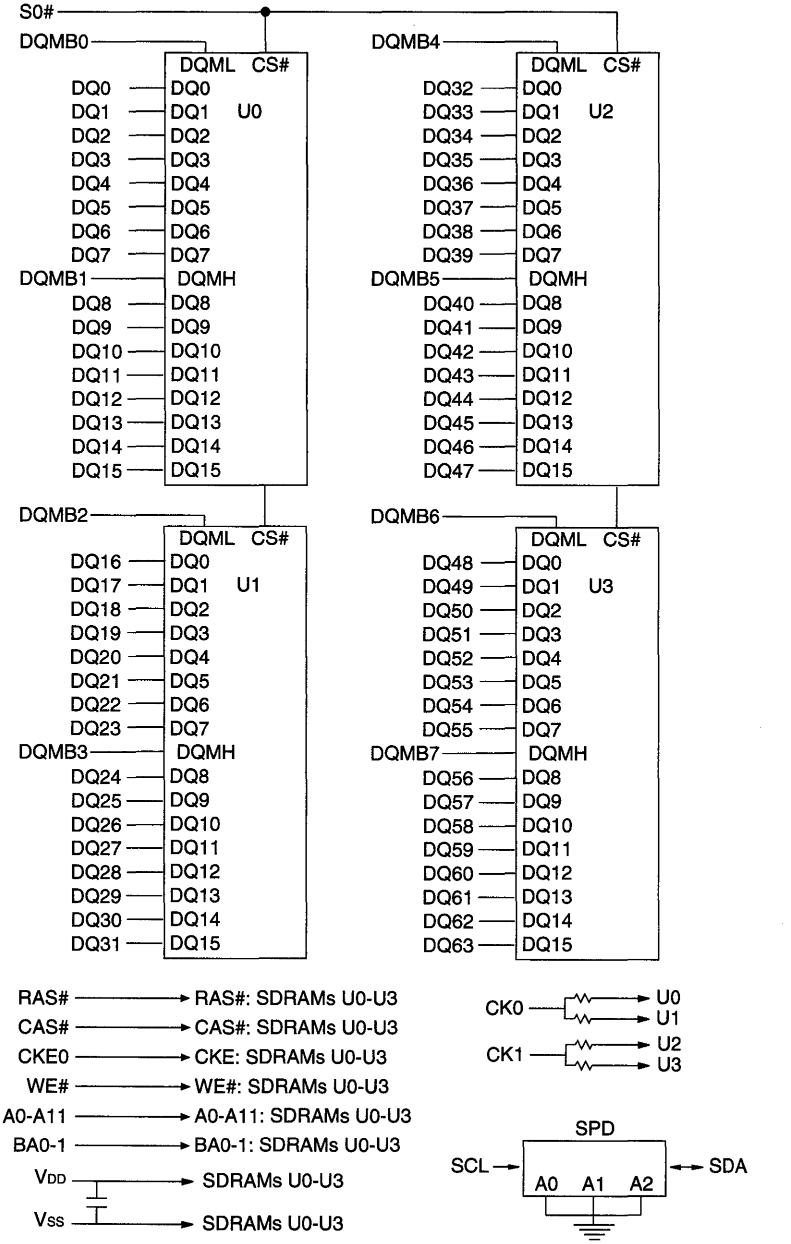
The modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs, outputs and clocks are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb: x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals.

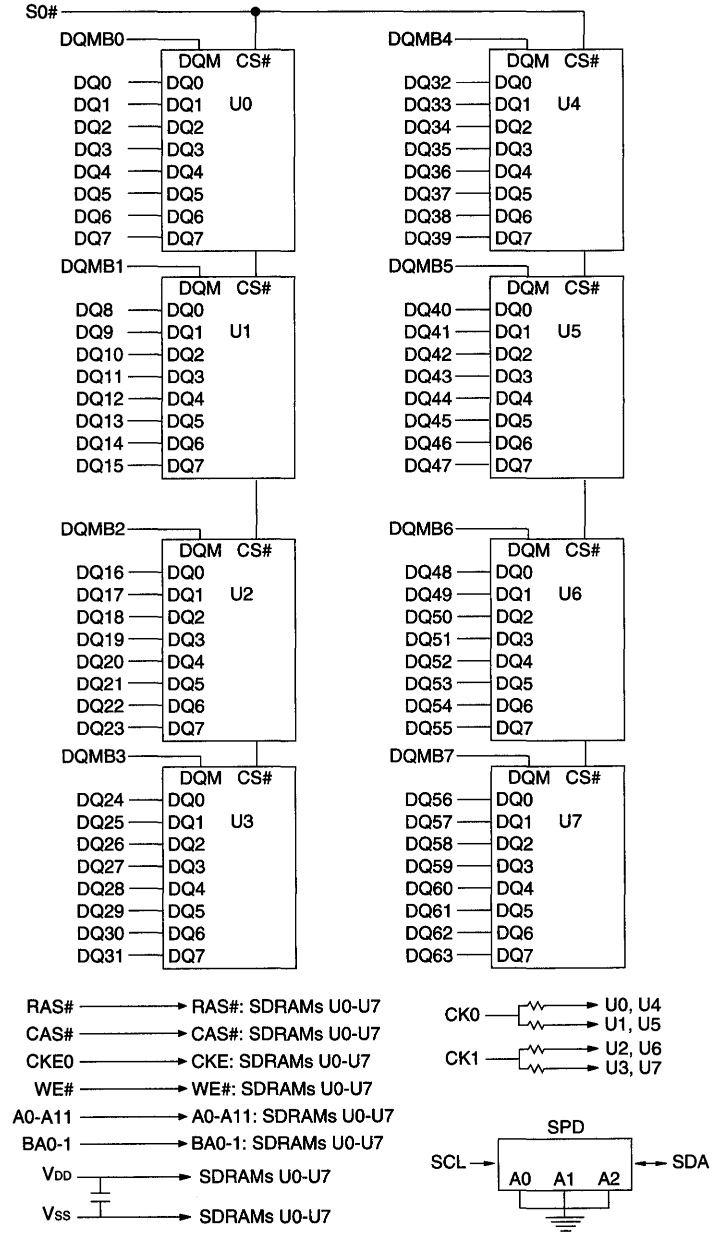
FUNCTIONAL BLOCK DIAGRAM
MT4LSDT464H (32MB)



NOTE: All resistor values are 10 ohms.

U0-U3 = MT48LC4M16A2TG SDRAMs

FUNCTIONAL BLOCK DIAGRAM
MT8LSDT864H (64MB)



NOTE: All resistor values are 10 ohms.

U0-U7 = MT48LC8M8A2TG SDRAMs

SMALL-OUTLINE SDRAM MODULE

MT4LSDT464H, MT8LSDT864H

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- PC100 rev 1.0, 144-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 125 MHz SDRAM components
- Module height = 1.00" (32MB), 1.250" (64MB)
- 32MB (4 Meg x 64), 64MB (8 Meg x 64)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (^{t}WR) version; one-clock ^{t}WR not supported

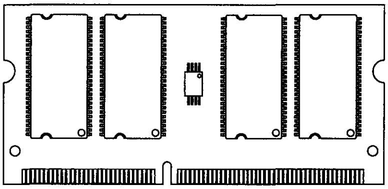
OPTIONS	MARKING
• Package 144-pin SODIMM (gold)	 G
• Frequency/CAS Latency	
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10C

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-10E	-8E	2	6ns	2ns	1ns
-10C	-8C	3	6ns	2ns	1ns

PIN ASSIGNMENT (Front View)
144-Pin Small-Outline DIMM

(I-4; 32MB)
(I-9; 64MB)



PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	Vss	2	Vss	73	DNU	74	CK1
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	VDD	46	VDD	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	NC	58	NC	129	VDD	130	VDD
59	NC	60	NC	131	DQ28	132	DQ60
61	CK0	62	CKE0	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	RAS#	66	CAS#	137	DQ31	138	DQ63
67	WE#	68	CKE1	139	Vss	140	Vss
69	S0#	70	RFU (A12)	141	SDA	142	SCL
71	S1#	72	RFU (A13)	143	VDD	144	VDD

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

Micron Technology, Inc., reserves the right to change products or specifications without notice.

PART NUMBERS

PART NUMBER	CONFIGURATION	VERSION
MT4LSDT464HG-10E__	4 Meg x 64	100 MHz, CL = 2
MT4LSDT464HG-10C__	4 Meg x 64	100 MHz, CL = 3
MT8LSDT864HG-10E__	8 Meg x 64	100 MHz, CL = 2
MT8LSDT864HG-10C__	8 Meg x 64	100 MHz, CL = 3

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8LSDT864HG-10CB4.

GENERAL DESCRIPTION

The MT4LSDT464H and MT8LSDT864H are high-speed CMOS, dynamic random-access, 32MB and 64MB memories organized in a x64 configuration. These modules use SDRAMs that are internally configured as quad-bank DRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK1).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

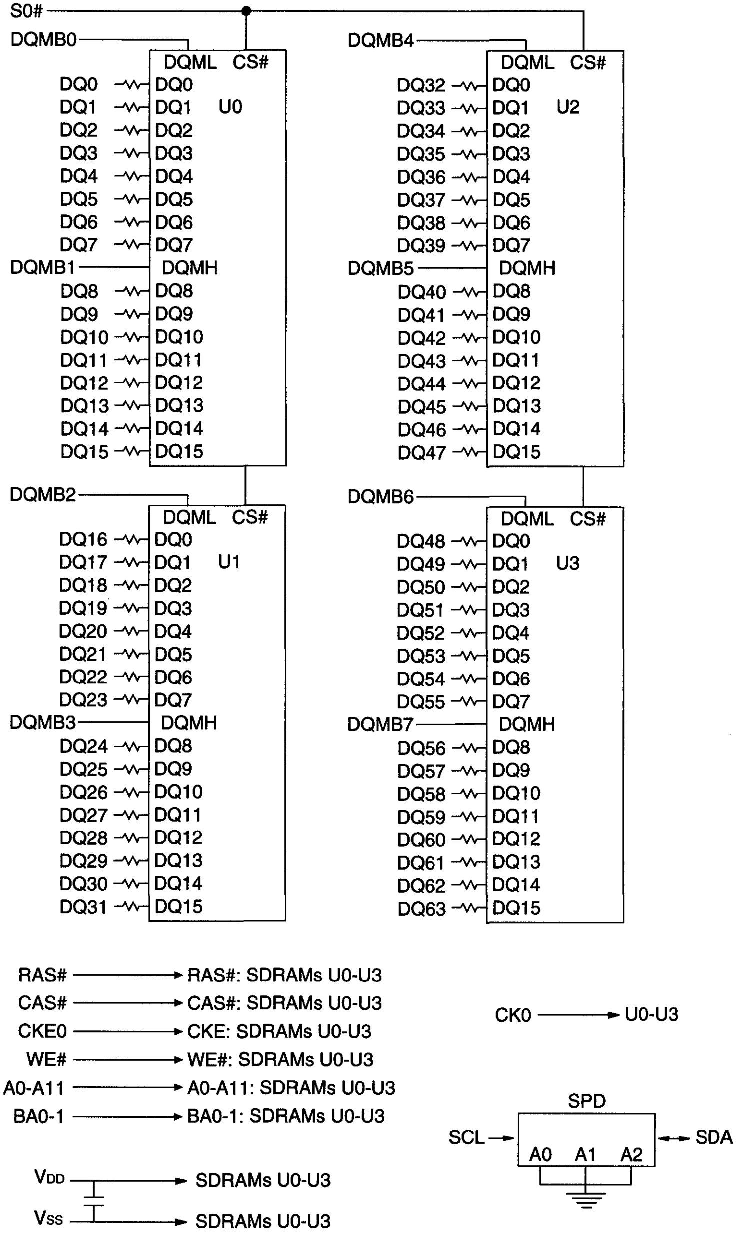
The modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs, outputs and clocks are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb: x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals.

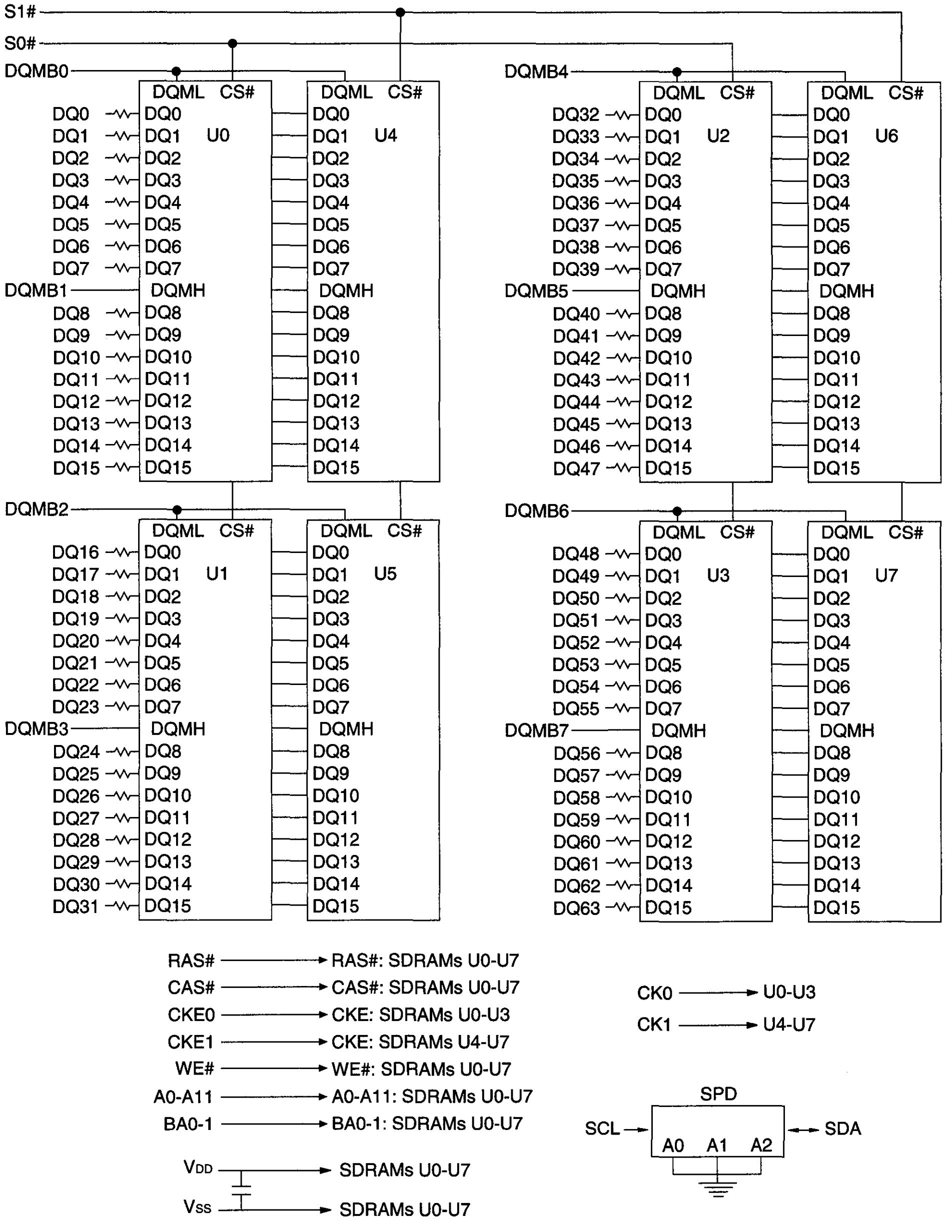
FUNCTIONAL BLOCK DIAGRAM
MT4LSDT464H (32MB)



NOTE: All resistor values are 10 ohms.

U0-U3 = MT48LC4M16A2TG SDRAMs

FUNCTIONAL BLOCK DIAGRAM
MT8LSDT864H (64MB)



NOTE: All resistor values are 10 ohms.

U0-U7 = MT48LC4M16A2TG SDRAMs

SYNCHRONOUS DRAM MODULE

MT8LSDT864A, MT16LSDT1664A

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- PC100-compliant; includes CONCURRENT AUTO PRECHARGE
- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- Utilizes 100 MHz and 125 MHz SDRAM components
- Nonbuffered
- 64MB (8 Meg x 64) and 128MB (16 Meg x 64)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (^{t}WR) version; one-clock ^{t}WR not supported

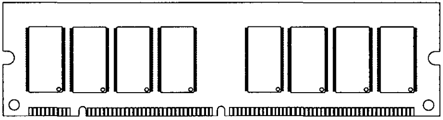
OPTIONS

OPTIONS	MARKING
• Package	
168-pin DIMM (gold)	G
• Frequency/CAS Latency	
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10C
66 MHz/CL = 2 (10ns, 100 MHz SDRAMs)	-662

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-10E	-8E	2	6ns	2ns	1ns
-10C	-8C	3	6ns	2ns	1ns
-662	-10	2	9ns	3ns	1ns

PIN ASSIGNMENT (Front View)
168-Pin DIMM
(H-18; 64MB, 66 MHz), (H-21; 64MB, 100 MHz), (H-22; 128MB)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#*
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	DNU	90	VDD	132	RFU
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	CKE1*	105	NC	147	NC
22	NC	64	VSS	106	NC	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	VSS	110	VDD	152	VSS
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#*	156	DQ59
31	DNU	73	VDD	115	RAS#	157	VDD
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	NC/WP**	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CK1	167	SA2
42	CK0	84	VDD	126	RFU	168	VDD

*128MB version only **-10C/-10E versions only

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT8LSDT864AG-662__	8 Meg x 64	66 MHz
MT8LSDT864AG-10C__	8 Meg x 64	100 MHz
MT8LSDT864AG-10E__	8 Meg x 64	100 MHz
MT16LSDT1664AG-662__	16 Meg x 64	66 MHz
MT16LSDT1664AG-10C__	16 Meg x 64	100 MHz
MT16LSDT1664AG-10E__	16 Meg x 64	100 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8LSDT864AG-10EB4.

GENERAL DESCRIPTION

The MT8LSDT864A and MT16LSDT1664A are high-speed CMOS, dynamic random-access, 64MB and 128MB memories organized in a x64 configuration. These modules use internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK3).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The modules provide for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

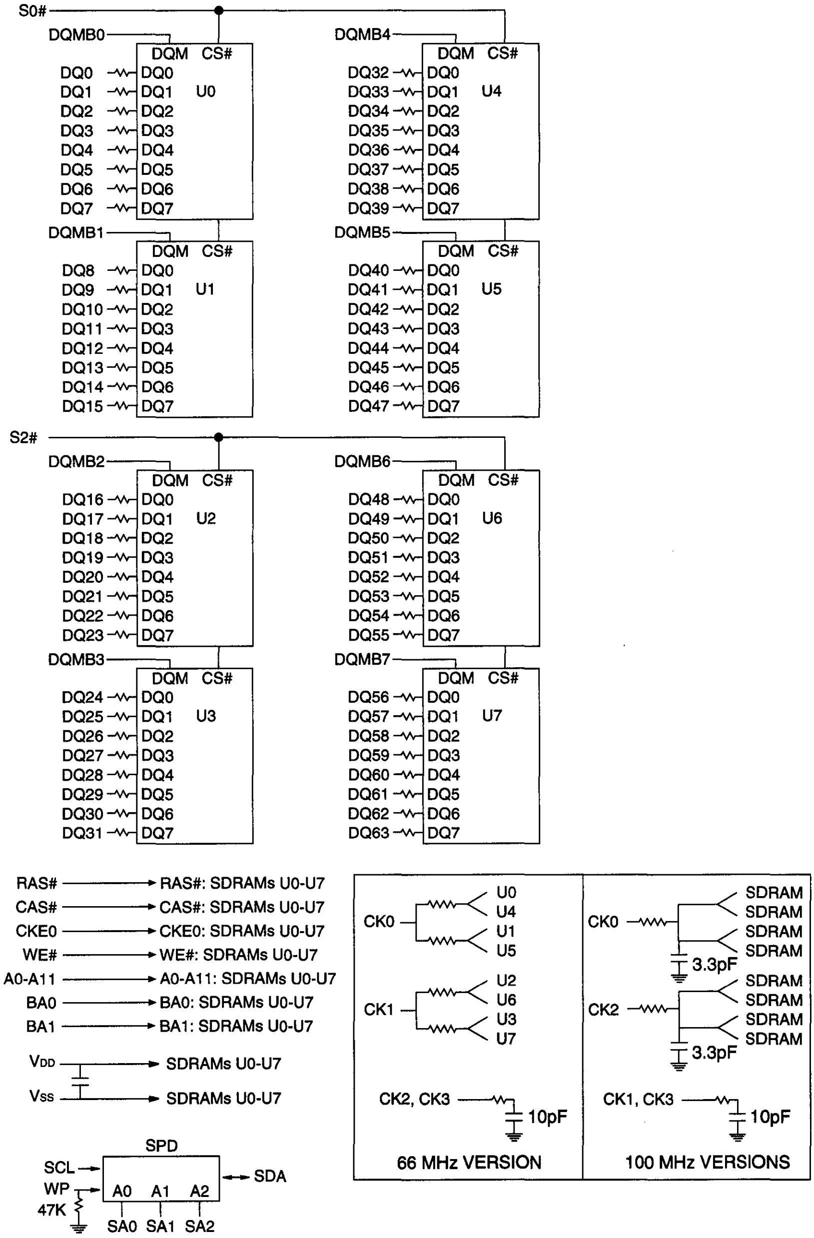
The modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb: x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

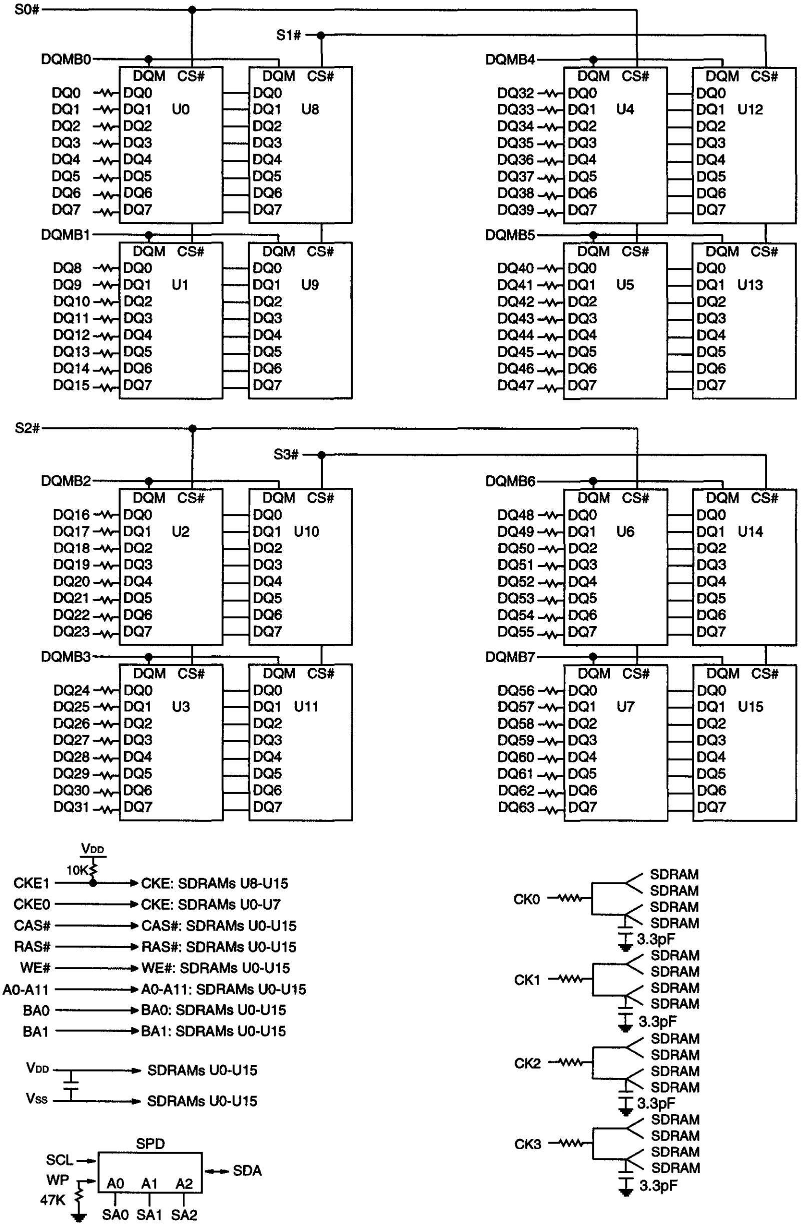
FUNCTIONAL BLOCK DIAGRAM
MT8LSDT864A (64MB)



NOTE: All resistor values are 10 ohms.

U0-U7 = MT48LC8M8A2GT SDRAMs

FUNCTIONAL BLOCK DIAGRAM
MT16LSDT1664A (128MB)



NOTE: All resistor values are 10 ohms unless otherwise specified.

U0-U15 = MT48LC8M8A2TG SDRAMs

ADVANCE

MICRON TECHNOLOGY, INC.

16 MEG x 64
SDRAM SODIMM

MALL-OUTLINE DRAM MODULE

MT8LSDT1664H

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

EATURES

- JEDEC-standard 144-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 100 MHz SDRAM components
- Nonbuffered
- 128MB (16 Meg x 64)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (^{t}WR) version; one-clock ^{t}WR not supported

PTIONS	MARKING
Package	
144-pin SODIMM (gold)	G
Frequency/CAS Latency	
66 MHz/CL = 2 (10ns, 100 MHz SDRAMs)	-662

EY SDRAM COMPONENT IMING PARAMETERS

MODULE MARKING	CLOCK FREQUENCY	SPEED GRADE	ACCESS TIME	SETUP TIME	HOLD TIME
-662	100 MHz	-10	9ns	3ns	1ns

ART NUMBER

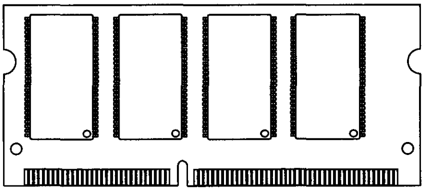
PART NUMBER	CONFIGURATION	VERSION
MT8LSDT1664HG-662__	16 Meg x 64	66 MHz, CL = 2

OTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8LSDT1664HG-662<u>D1</u>.

PIN ASSIGNMENT (Front View)

144-Pin Small-Outline DIMM

(I-5)



PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	Vss	2	Vss	73	DNU	74	CK1
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	VDD	46	VDD	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	NC	58	NC	129	VDD	130	VDD
59	NC	60	NC	131	DQ28	132	DQ60
61	CK0	62	CKE0	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	RAS#	66	CAS#	137	DQ31	138	DQ63
67	WE#	68	RFU (CKE1)	139	Vss	140	Vss
69	S0#	70	RFU (A12)	141	SDA	142	SCL
71	RFU (S1#)	72	RFU (A13)	143	VDD	144	VDD

NOTE: Symbols in parentheses are not used on this module but may be used for other modules in this product family. They are for reference only.

GENERAL DESCRIPTION

The MT8LSDT1664H is a high-speed CMOS, dynamic random-access, 128MB memory organized in a x64 configuration. This module uses SDRAMs that are internally configured as quad-bank DRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK1).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

This module provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed random-access operation.

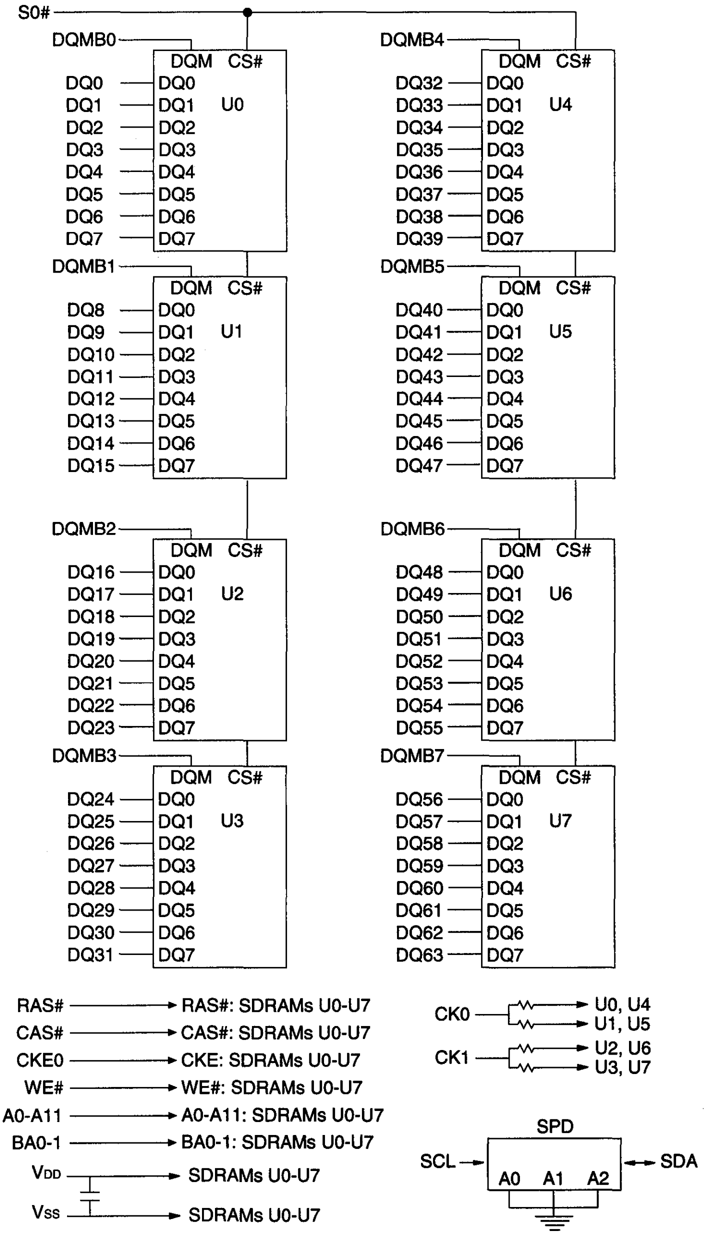
The module is designed to operate in 3.3V, low-powe memory systems. An auto refresh mode is provided, alon with a power-saving, power-down mode. All inputs, outputs and clocks are LVTTL-compatible.

SDRAM modules offer substantial advances i DRAM operating performance, including the ability t synchronously burst data at a high data rate with automati column-address generation, the ability to interleave between internal banks in order to hide precharge time, an the capability to randomly change column addresses o each clock cycle during a burst access. For more informatio regarding SDRAM operation, refer to the 128Mb: x4, x8, x1 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD) The SPD function is implemented using a 2,048-bit EEPROM This nonvolatile storage device contains 256 bytes. The firs 128 bytes can be programmed by Micron to identify th module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage ar available for use by the customer. System READ/WRIT operations between the master (system logic) and the slav EEPROM device (DIMM) occur via a standard IIC bu using the DIMM's SCL (clock) and SDA (data) signals.

FUNCTIONAL BLOCK DIAGRAM
MT8LSDT1664H (128MB)



NOTE: All resistor values are 10 ohms.

U0-U7 = MT48LC16M8A2TG SDRAMs

ADVANCE

MICRON TECHNOLOGY, INC.

32 MEG x 64
SDRAM DIMM

SYNCHRONOUS DRAM MODULE

MT16LSDT3264A

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- PC100-compliant; includes CONCURRENT AUTO PRECHARGE
- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- Utilizes 125 MHz SDRAM components
- Nonbuffered
- 256MB (32 Meg x 64)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (^{t}WR) version; one-clock ^{t}WR not supported

OPTIONS — MARKING

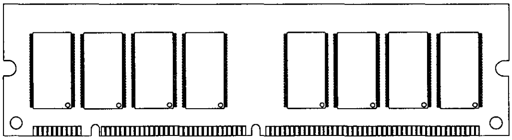
OPTIONS	MARKING
Package	
168-pin DIMM (gold)	G
Frequency/CAS Latency	
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10C
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10B

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-10E	-8E	2	6ns	2ns	1ns
10B/-10C	-8B/-8C	3	6ns	2ns	1ns

PIN ASSIGNMENT (Front View)

168-Pin DIMM
(H-22)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	DNU	90	VDD	132	RFU
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	CKE1	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	Vss	110	VDD	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#	156	DQ59
31	DNU	73	VDD	115	RAS#	157	VDD
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CK1	167	SA2
42	CK0	84	VDD	126	RFU	168	VDD

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT16LSDT3264AG-10E_	32 Meg x 64	100 MHz
MT16LSDT3264AG-10C_	32 Meg x 64	100 MHz
MT16LSDT3264AG-10B_	32 Meg x 64	100 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT16LSDT3264AG-10CD1.

GENERAL DESCRIPTION

The MT16LSDT3264A is a high-speed CMOS, dynamic random-access, 256MB memory organized in a x64 configuration. This module uses internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK3).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The module provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The module uses an internal pipelined architecture t achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it als allows the column address to be changed on every cloc cycle to achieve a high-speed, fully random acces Precharging one bank while accessing one of the other thre banks will hide the precharge cycles and provide seamles high-speed, random-access operation.

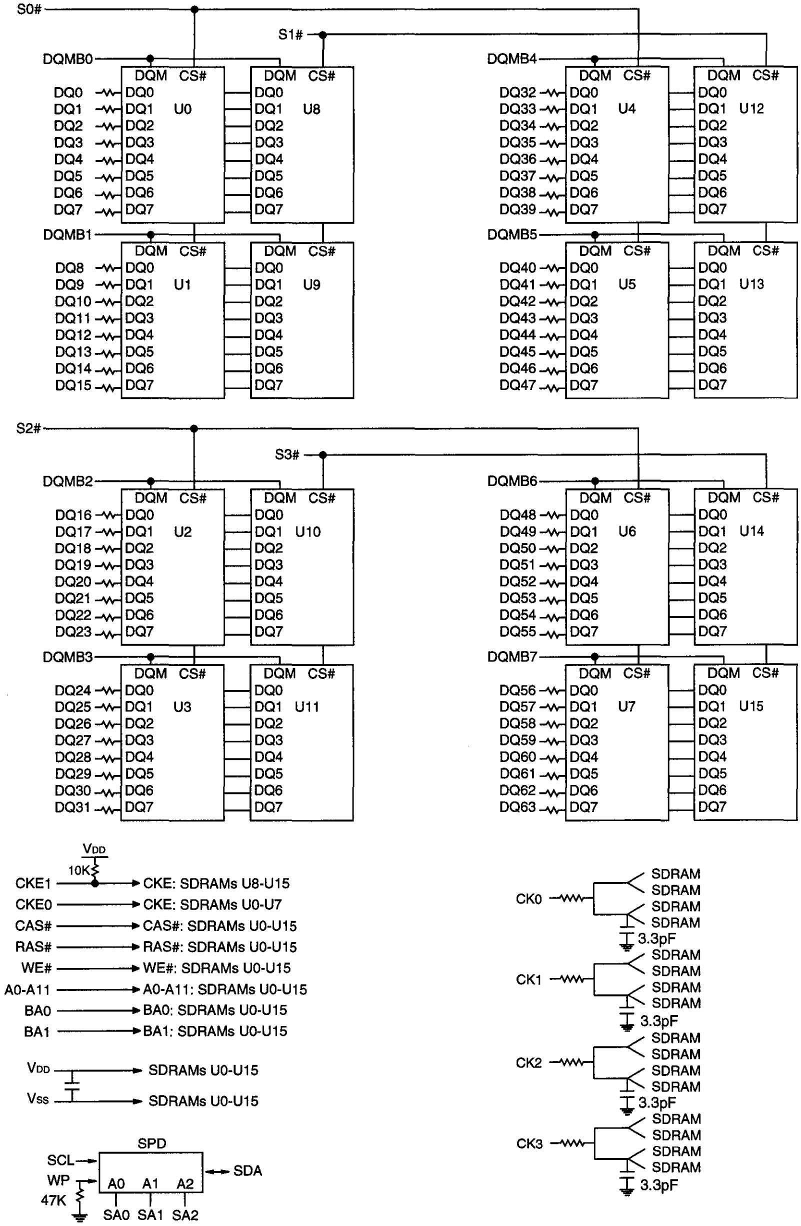
The module is designed to operate in 3.3V, low-powe memory systems. An auto refresh mode is provided, alon with a power-saving, power-down mode. All inputs an outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automati column-address generation, the ability to interleave between internal banks in order to hide precharge time and th capability to randomly change column addresses on eac clock cycle during a burst access. For more informatio regarding SDRAM operation, refer to the 128Mb: x4, x8, x1 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD) The SPD function is implemented using a 2,048-bit EEPROM This nonvolatile storage device contains 256 bytes. The firs 128 bytes can be programmed by Micron to identify th module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage ar available for use by the customer. System READ/WRIT operations between the master (system logic) and the slav EEPROM device (DIMM) occur via a standard IIC bu using the DIMM's SCL (clock) and SDA (data) signals together with SA(2:0), which provide eight unique DIMM/ EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT16LSDT3264A (256MB)



NOTE: All resistor values are 10 ohms unless otherwise specified.

U0-U15 = MT48LC16M8A2TG SDRAMs

Micron Technology, Inc., reserves the right to change products or specifications without notice.

MICRON
TECHNOLOGY, INC.

4 MEG x 72
SDRAM DIMM

SYNCHRONOUS DRAM MODULE

MT5LSDT472A

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

EATURES

PC100-compliant; includes CONCURRENT AUTO PRECHARGE
JEDEC-standard 168-pin, dual in-line memory module (DIMM)
Utilizes 100 MHz and 125 MHz SDRAM components
Nonbuffered
32MB (4 Meg x 72)
Single +3.3V ±0.3V power supply
Fully synchronous; all signals registered on positive edge of system clock
Internal pipelined operation; column address can be changed every clock cycle
Internal SDRAM banks for hiding row access/precharge
Programmable burst lengths: 1, 2, 4, 8 or full page
Auto Precharge and Auto Refresh Modes
Self Refresh Mode
64ms, 4,096-cycle refresh
LVTTL-compatible inputs and outputs
Serial presence-detect (SPD)
Two-clock WRITE recovery (ᵗWR) version; one-clock ᵗWR not supported

PTIONS

	MARKING
Package	
168-pin DIMM (gold)	G
Frequency/CAS Latency	
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10C
66 MHz/CL = 2 (10ns, 100 MHz SDRAMs)	-662

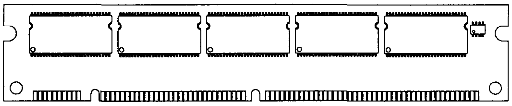
EY SDRAM COMPONENT IMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-10E	-8E	2	6ns	2ns	1ns
-10C	-8C	3	6ns	2ns	1ns
-662	-10	2	9ns	3ns	1ns

OTE: Pin symbols in parentheses are not used on this module but may be used for other modules in this product family. They are for reference only.

PIN ASSIGNMENT (Front View)

168-Pin DIMM
(H-9)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	NC (S3#)
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	DNU	90	VDD	132	NC (A13)
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC (CKE1)	105	CB4	147	NC
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	Vss	110	VDD	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	NC (S1#)	156	DQ59
31	DNU	73	VDD	115	RAS#	157	VDD
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	NC (CK3)
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	NC/WP*	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	NC (CK1)	167	SA2
42	CK0	84	VDD	126	NC (A12)	168	VDD

*-10C/-10E versions only

Micron Technology, Inc., reserves the right to change products or specifications without notice.

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT5LSDT472AG-10E__	4 Meg x 72	100 MHz
MT5LSDT472AG-10C__	4 Meg x 72	100 MHz
MT5LSDT472AG-662__	4 Meg x 72	66 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT5LSDT472AG-10CB1.

GENERAL DESCRIPTION

The MT5LSDT472A is a high-speed CMOS, dynamic random-access, 32MB memory organized in a x72 configuration. This module uses internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0, CK2).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The module provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

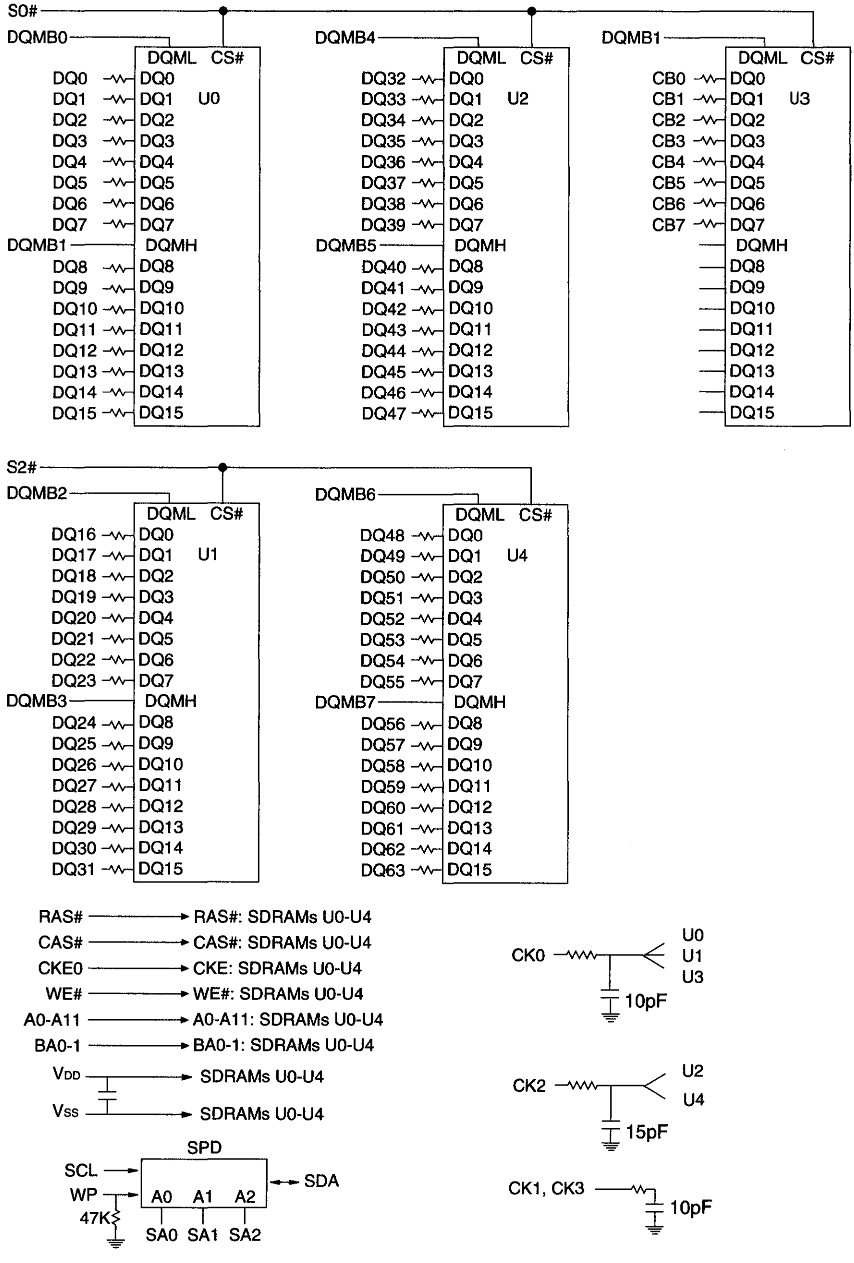
The module is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb: x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD) The SPD function is implemented using a 2,048-bit EEPROM This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT5LSDT472A (32MB)



NOTE: All resistor values are 10 ohms.

U0-U4 = MT48LC4M16A2TG SDRAMs

SYNCHRONOUS DRAM MODULE

MT9LSDT872

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

EATURES

- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- PC100-compliant
- Registered inputs with one clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- Utilizes 125 MHz SDRAM components
- ECC-optimized pinout
- 64MB (8 Meg x 72)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (^{t}WR) version; one-clock ^{t}WR not supported

PTIONS

PTIONS	MARKING
Package	
168-pin DIMM (gold)	G
Frequency/CAS Latency*	
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10C

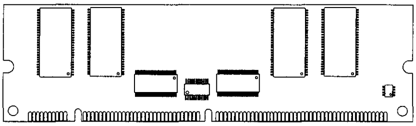
evice latency only; extra clock cycle required due to input register.

EY SDRAM COMPONENT IMING PARAMETERS

MODULE MARKING	SPEED GRADE	ACCESS TIME	SETUP TIME	HOLD TIME
-10E	-8E	6ns	2ns	1ns
-10C	-8C	6ns	2ns	1ns

PIN ASSIGNMENT (Front View) 168-Pin DIMM

(H-25)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	RFU (S3#)
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vdd	48	DNU	90	Vdd	132	RFU (A13)
7	DQ4	49	Vdd	91	DQ36	133	Vdd
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vdd	101	DQ45	143	Vdd
18	Vdd	60	DQ20	102	Vdd	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	RFU (CKE1)	105	CB4	147	REGE
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vdd	68	Vss	110	Vdd	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	RFU (S1#)	156	DQ59
31	DNU	73	Vdd	115	RAS#	157	Vdd
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	Vdd	82	SDA	124	Vdd	166	SA1
41	Vdd	83	SCL	125	NC	167	SA2
42	CK0	84	Vdd	126	RFU (A12)	168	Vdd

NOTE: Symbols in parentheses are not used on this module but may be used for other modules in this product family. They are for reference only.

Micron Technology, Inc., reserves the right to change products or specifications without notice.

PRELIMINARY

MICRON TECHNOLOGY, INC.

8 MEG x 72
REGISTERED SDRAM DIMM

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT9LSDT872G-10E__	8 Meg x 72	100 MHz
MT9LSDT872G-10C__	8 Meg x 72	100 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9LSDT872G-10EB1

GENERAL DESCRIPTION

The MT9LSDT872 is a high-speed CMOS, dynamic random-access, 64MB memory organized in a x72 configuration. This module uses internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of clock signal CK0).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The module provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The module is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb: x4, x8 x16 SDRAM data sheet.

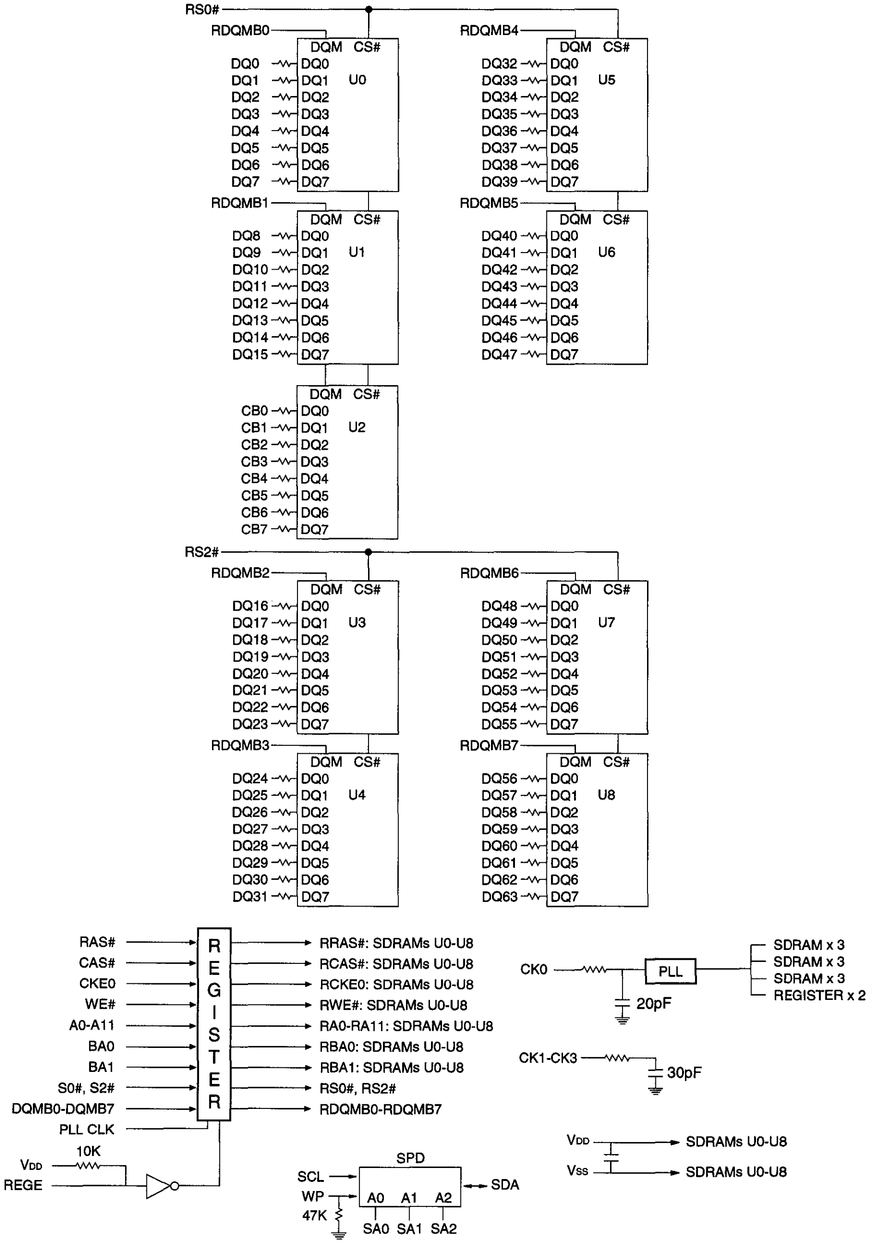
PLL AND REGISTER OPERATION

The module can be operated in either registered mode (REGE pin HIGH), where the control/address input signals are latched in the register on one rising clock edge and sen to the SDRAM devices on the following rising clock edge (data access is delayed by one clock), or in buffered mode (REGE pin LOW) where the input signals pass through the register/buffer to the SDRAM devices on the same clock. A phase-lock loop (PLL) on the module is used to redrive the clock signals to the SDRAM devices to minimize system clock loading (CK0 is connected to the PLL, and CK1, CK2 and CK3 are terminated).

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD) The SPD function is implemented using a 2,048-bit EEPROM This nonvolatile storage device contains 256 bytes. The firs 128 bytes can be programmed by Micron to identify th module type and various SDRAM organizations and tim ing parameters. The remaining 128 bytes of storage ar available for use by the customer. System READ/WRITE operations between the master (system logic) and the slav EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, togethe with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT9LSDT872 (64MB)



NOTE: All resistor values are 10 ohms unless otherwise specified.

U0-U8 = MT48LC8M8A2TG SDRAMs

SYNCHRONOUS DRAM MODULE

MT9LSDT872A, MT18LSDT1672A

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- PC100-compliant; includes CONCURRENT AUTO PRECHARGE
- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- Nonbuffered
- ECC-optimized pinout
- 64MB (8 Meg x 72) and 128MB (16 Meg x 72)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (^{t}WR) version; one-clock ^{t}WR not supported

OPTIONS | MARKING

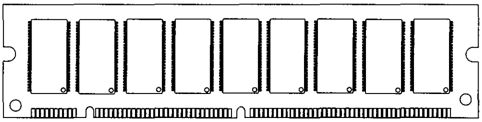
OPTIONS	MARKING
• Package	
168-pin DIMM (gold)	G
• Frequency/CAS Latency	
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10C
66 MHz/CL = 2 (10ns, 100 MHz SDRAMs)	-662

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-10E	-8E	2	6ns	2ns	1ns
-10C	-8C	3	6ns	2ns	1ns
-662	-10	2	9ns	3ns	1ns

PIN ASSIGNMENT (Front View)
168-Pin DIMM

(H-19; 64MB, 66 MHz), (H-23; 64MB, 100 MHz), (H-24; 128MB)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#*
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{DD}	48	DNU	90	V_{DD}	132	RFU
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1*	105	CB4	147	NC
22	CB1	64	V_{SS}	106	CB5	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#*	156	DQ59
31	DNU	73	V_{DD}	115	RAS#	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	NC/WP**	123	A11	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	CK1	167	SA2
42	CK0	84	V_{DD}	126	RFU	168	V_{DD}

*128MB version only **-10C/-10E versions only

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT9LSDT872AG-662__	8 Meg x 72	66 MHz
MT9LSDT872AG-10C__	8 Meg x 72	100 MHz
MT9LSDT872AG-10E__	8 Meg x 72	100 MHz
MT18LSDT1672AG-662__	16 Meg x 72	66 MHz
MT18LSDT1672AG-10C__	16 Meg x 72	100 MHz
MT18LSDT1672AG-10E__	16 Meg x 72	100 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9LSDT872AG-10EB4.

GENERAL DESCRIPTION

The MT9LSDT872A and MT18LSDT1672A are high-speed CMOS, dynamic random-access, 64MB and 128MB memories organized in a x72 configuration. These modules use internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK3).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The modules provide for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

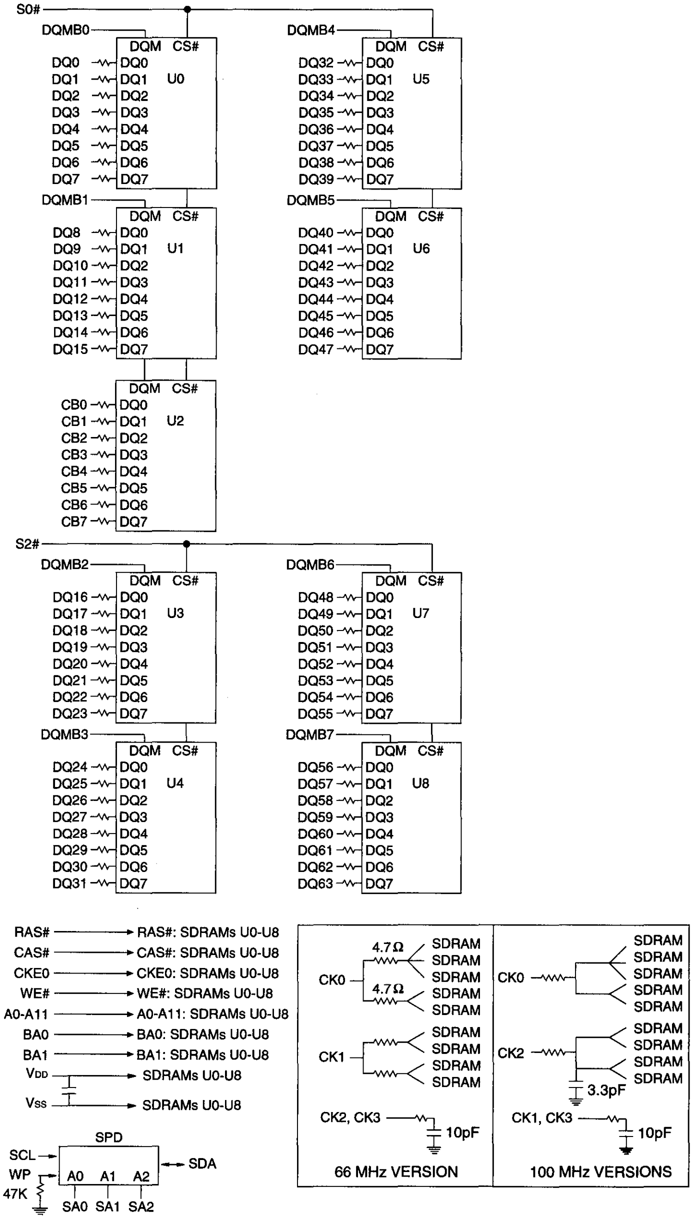
The modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb: x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

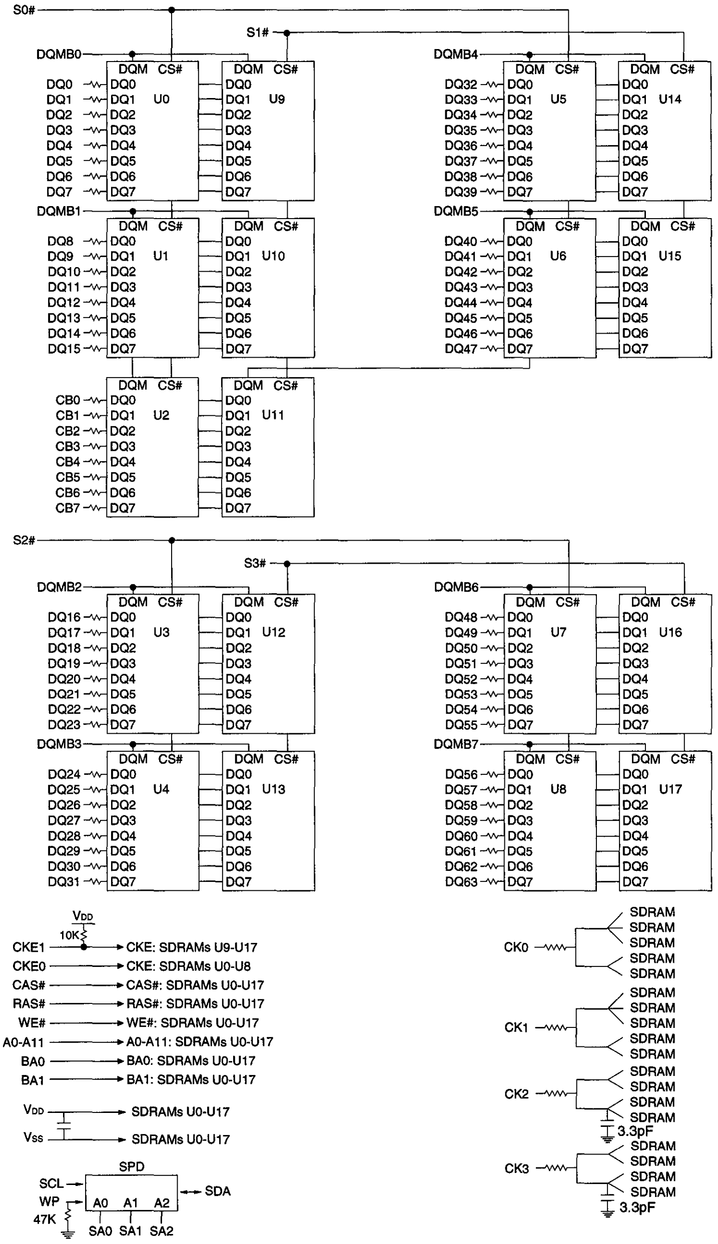
FUNCTIONAL BLOCK DIAGRAM
MT9LSDT872A (64MB)



NOTE: All resistor values are 10 ohms unless otherwise specified.

U0-U8 = MT48LC8M8A2TG SDRAMs

FUNCTIONAL BLOCK DIAGRAM
MT18LSDT1672A (128MB)



NOTE: All resistor values are 10 ohms unless otherwise specified.

U0-U17 = MT48LC8M8A2TG SDRAMs

SYNCHRONOUS DRAM MODULE

MT18LSDT1672

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- PC100-compliant
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- Utilizes 100 MHz and 125 MHz SDRAM components
- ECC-optimized pinout
- 128MB (16 Meg x 72)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of PLL clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (^{t}WR) version; one-clock ^{t}WR not supported

OPTIONS

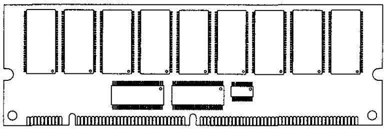
OPTIONS	MARKING
• Package	
168-pin DIMM (gold)	G
• Frequency/CAS Latency*	
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10C

*Device latency only; extra clock cycle required due to input register.

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	ACCESS TIME	SETUP TIME	HOLD TIME
-10E	-8E	6ns	2ns	1ns
-10C	-8C	6ns	2ns	1ns

PIN ASSIGNMENT (Front View)
168-Pin DIMM
(H-26)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	RFU (S3#)
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	DNU	90	VDD	132	RFU (A13)
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	RFU (CKE1)	105	CB4	147	REGE
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	VSS	110	VDD	152	VSS
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	RFU (S1#)	156	DQ59
31	DNU	73	VDD	115	RAS#	157	VDD
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CK1	167	SA2
42	CK0	84	VDD	126	RFU (A12)	168	VDD

NOTE: Symbols in parentheses are not used on this module but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT18LSDT1672G-10E__	16 Meg x 72	100 MHz
MT18LSDT1672G-10C__	16 Meg x 72	100 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18LSDT1672G-10EB1

GENERAL DESCRIPTION

The MT18LSDT1672 is a high-speed CMOS, dynamic random-access, 128MB memory organized in a x72 configuration. This module uses internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of clock signal CK0).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The module provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The module is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb: x4, x8, x16 SDRAM data sheet.

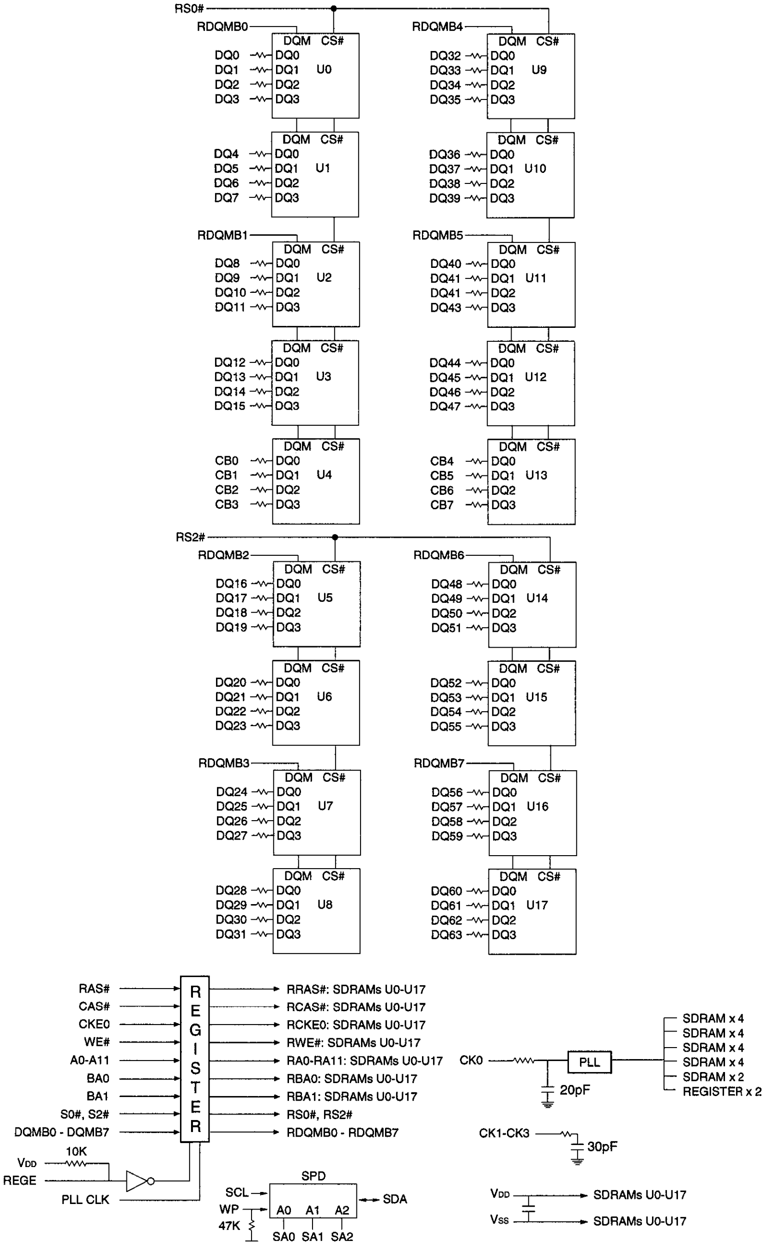
PLL AND REGISTER OPERATION

The module can be operated in either registered mode (REGE pin HIGH), where the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock), or in buffered mode (REGE pin LOW) where the input signals pass through the register/buffer to the SDRAM devices on the same clock. A phase-lock loop (PLL) on the module is used to redrive the clock signals to the SDRAM devices to minimize system clock loading (CK0 is connected to the PLL, and CK1, CK2 and CK3 are terminated).

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT18LSDT1672 (128MB)



NOTE: All resistor values are 10 ohms unless otherwise specified.

U0-U17 = MT48LC16M4A2TG SDRAMs

SYNCHRONOUS DRAM MODULE

MT18LSDT3272

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- PC100-compliant
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- Utilizes 125 MHz SDRAM components
- ECC-optimized pinout
- 256MB (32 Meg x 72)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of PLL clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (ᵗWR) version; one-clock ᵗWR not supported

OPTIONS

OPTIONS	MARKING
• Package	
168-pin DIMM (gold)	G
• Frequency/CAS Latency*	
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10C
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10B

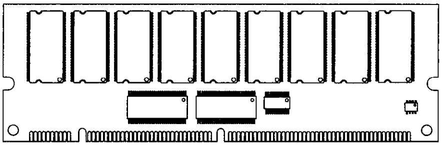
Device latency only; extra clock cycle required due to input register.

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-10E	-8E	2	6ns	2ns	1ns
-10B/-10C	-8B/-8C	3	6ns	2ns	1ns

PIN ASSIGNMENT (Front View) 168-Pin DIMM

(H-26)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	NC (S3#)
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	DNU	90	VDD	132	NC (A13)
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC (CKE1)	105	CB4	147	REGE
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	Vss	110	VDD	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	NC (S1#)	156	DQ59
31	DNU	73	VDD	115	RAS#	157	VDD
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CK1	167	SA2
42	CK0	84	VDD	126	NC (A12)	168	VDD

NOTE: Symbols in parentheses are not used on this module but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT18LSDT3272G-10E__	32 Meg x 72	100 MHz
MT18LSDT3272G-10C__	32 Meg x 72	100 MHz
MT18LSDT3272G-10B__	32 Meg x 72	100 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18LSDT3272G-10CD1

GENERAL DESCRIPTION

The MT18LSDT3272 is a high-speed CMOS, dynamic random-access, 256MB memory organized in a x72 configuration. This module uses internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of clock signal CK0).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The module provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The module is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 128Mb: x4, x8, x16 SDRAM data sheet.

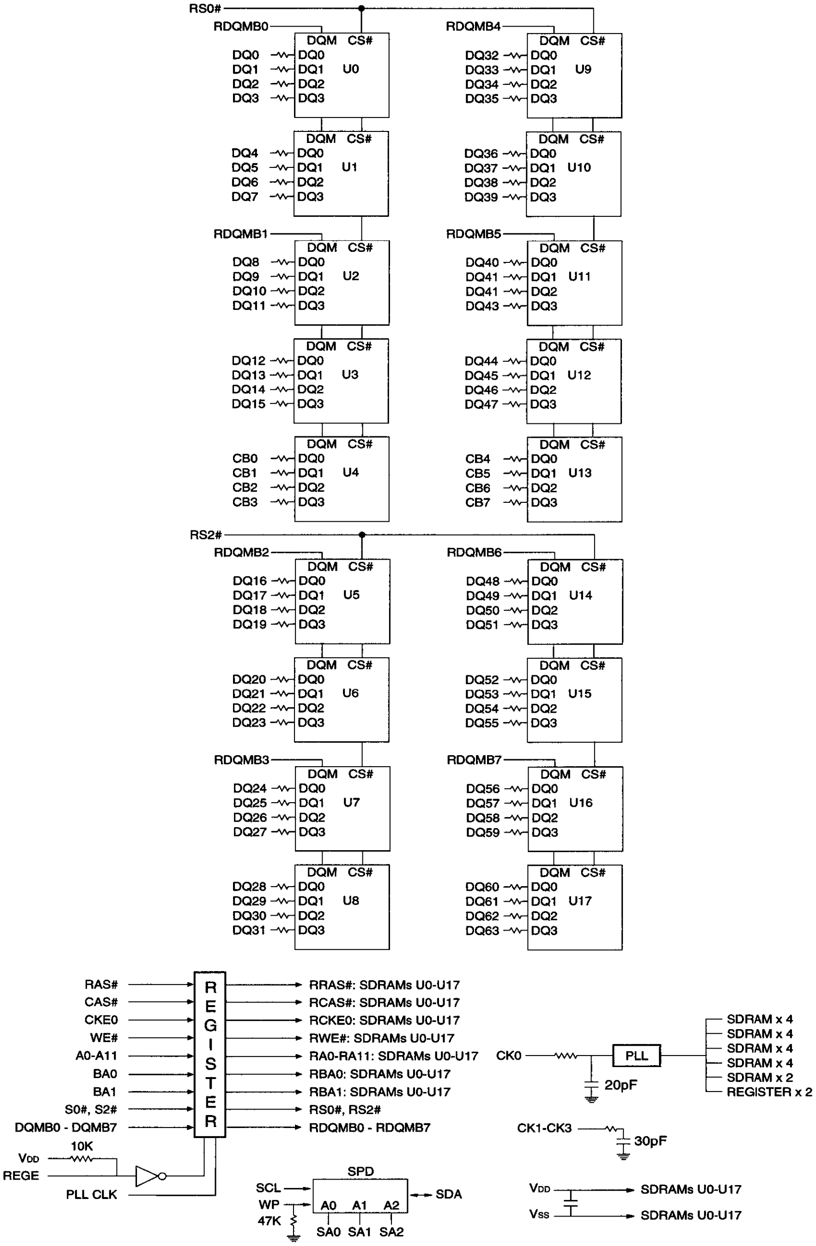
PLL AND REGISTER OPERATION

The module can be operated in either registered mode (REGE pin HIGH), where the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock), or in buffered mode (REGE pin LOW) where the input signals pass through the register/buffer to the SDRAM devices on the same clock. A phase-lock loop (PLL) on the module is used to redrive the clock signals to the SDRAM devices to minimize system clock loading (CK0 is connected to the PLL, and CK1, CK2 and CK3 are terminated).

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT18LSDT3272 (256MB)



NOTE: All resistor values are 10 ohms unless otherwise specified.

U0-U17 = MT48LC32M4A2TG SDRAMs

SYNCHRONOUS DRAM MODULE

MT36LSDT3272

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- PC100-compliant
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- Utilizes 125 MHz SDRAM components
- ECC-optimized pinout
- 256MB (32 Meg x 72)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of PLL clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (^{t}WR) version; one-clock ^{t}WR not supported

OPTIONS — MARKING

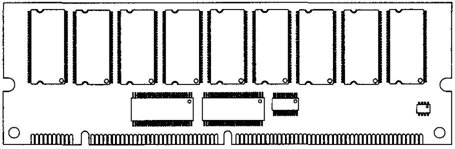
OPTIONS	MARKING
• Package	
168-pin DIMM (gold)	G
• Frequency/CAS Latency*	
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10C

*Device latency only; extra clock cycle required due to input register.

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	ACCESS TIME	SETUP TIME	HOLD TIME
-10E	-8E	6ns	2ns	1ns
-10C	-8C	6ns	2ns	1ns

PIN ASSIGNMENT (Front View)
168-Pin DIMM
(H-27)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	DNU	90	VDD	132	NC (A13)
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC (CKE1)	105	CB4	147	REGE
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	Vss	110	VDD	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#	156	DQ59
31	DNU	73	VDD	115	RAS#	157	VDD
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CK1	167	SA2
42	CK0	84	VDD	126	NC (A12)	168	VDD

NOTE: Symbols in parentheses are not used on this module but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT36LSDT3272G-10E__	32 Meg x 72	100 MHz
MT36LSDT3272G-10C__	32 Meg x 72	100 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT36LSDT3272G-10EB1

GENERAL DESCRIPTION

The MT36LSDT3272 is a high-speed CMOS, dynamic random-access, 256MB memory organized in a x72 configuration. This module uses internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of clock signal CK0).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The module provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The module is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb: x4, x8, x16 SDRAM data sheet.

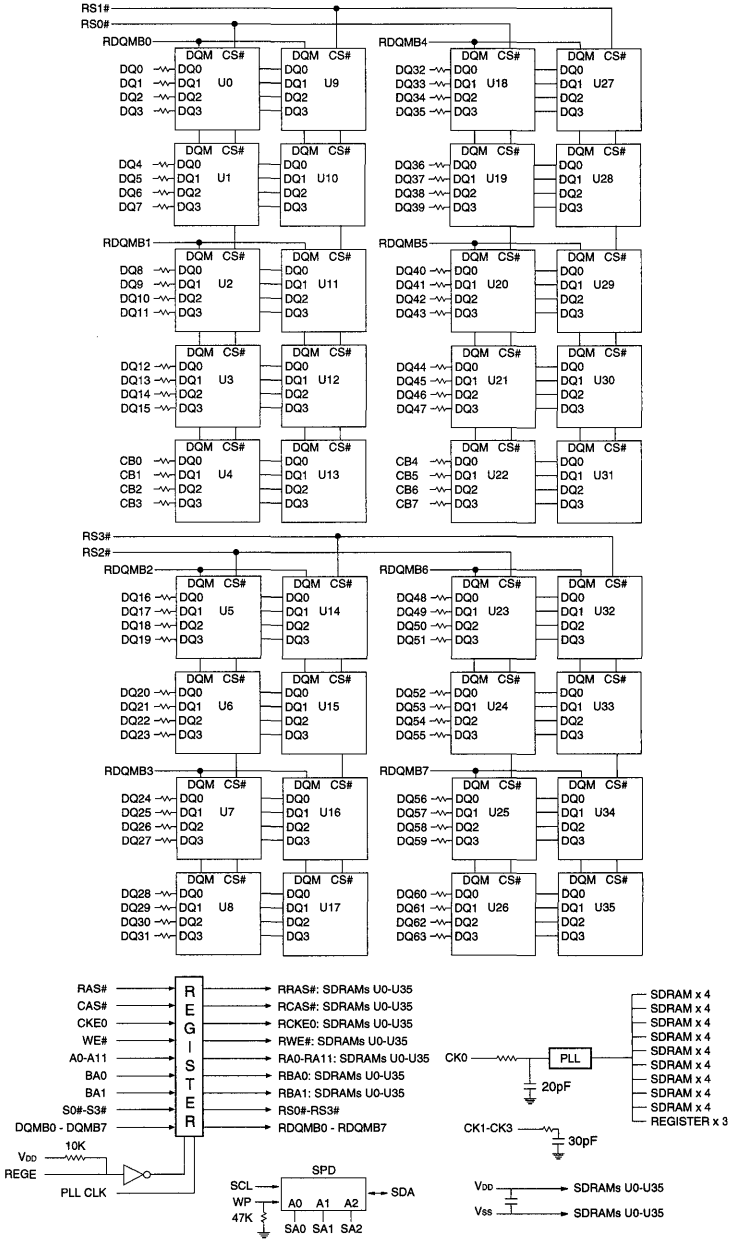
PLL AND REGISTER OPERATION

The module can be operated in either registered mode (REGE pin HIGH), where the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock), or in buffered mode (REGE pin LOW) where the input signals pass through the register/buffer to the SDRAM devices on the same clock. A phase-lock loop (PLL) on the module is used to redrive the clock signals to the SDRAM devices to minimize system clock loading (CK0 is connected to the PLL, and CK1, CK2 and CK3 are terminated).

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT36LSDT3272 (256MB)



NOTE: All resistor values are 10 ohms unless otherwise specified.

U0-U35 = MT48LC16M4A2TG SDRAMs

Micron Technology, Inc., reserves the right to change products or specifications without notice.

SYNCHRONOUS DRAM MODULE

MT18LSDT3272A

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- PC100-compliant; includes CONCURRENT AUTO PRECHARGE
- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- Utilizes 125 MHz SDRAM components
- Nonbuffered
- ECC-optimized pinout
- 256MB (32 Meg x 72)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (^{t}WR) version; one-clock ^{t}WR not supported

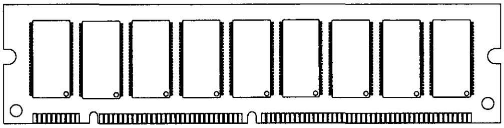
OPTIONS

OPTIONS	MARKING
• Package	
168-pin DIMM (gold)	G
• Frequency/CAS Latency	
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10C
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10B

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-10E	-8E	2	6ns	2ns	1ns
-10B/-10C	-8B/-8C	3	6ns	2ns	1ns

PIN ASSIGNMENT (Front View)
168-Pin DIMM
(H-24)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	DNU	90	VDD	132	RFU
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	Vss	110	VDD	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#	156	DQ59
31	DNU	73	VDD	115	RAS#	157	VDD
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CK1	167	SA2
42	CK0	84	VDD	126	RFU	168	VDD

Micron Technology, Inc., reserves the right to change products or specifications without notice.

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT18LSDT3272AG-10E_	32 Meg x 72	100 MHz
MT18LSDT3272AG-10C_	32 Meg x 72	100 MHz
MT18LSDT3272AG-10B_	32 Meg x 72	100 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18LSDT3272AG-10CD1.

GENERAL DESCRIPTION

The MT18LSDT3272A is a high-speed CMOS, dynamic random-access, 256MB memory organized in a x72 configuration. This module uses internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK3).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The module provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The module uses an internal pipelined architecture tc achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it alsc allows the column address to be changed on every clocl cycle to achieve a high-speed, fully random access Precharging one bank while accessing one of the other threε banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

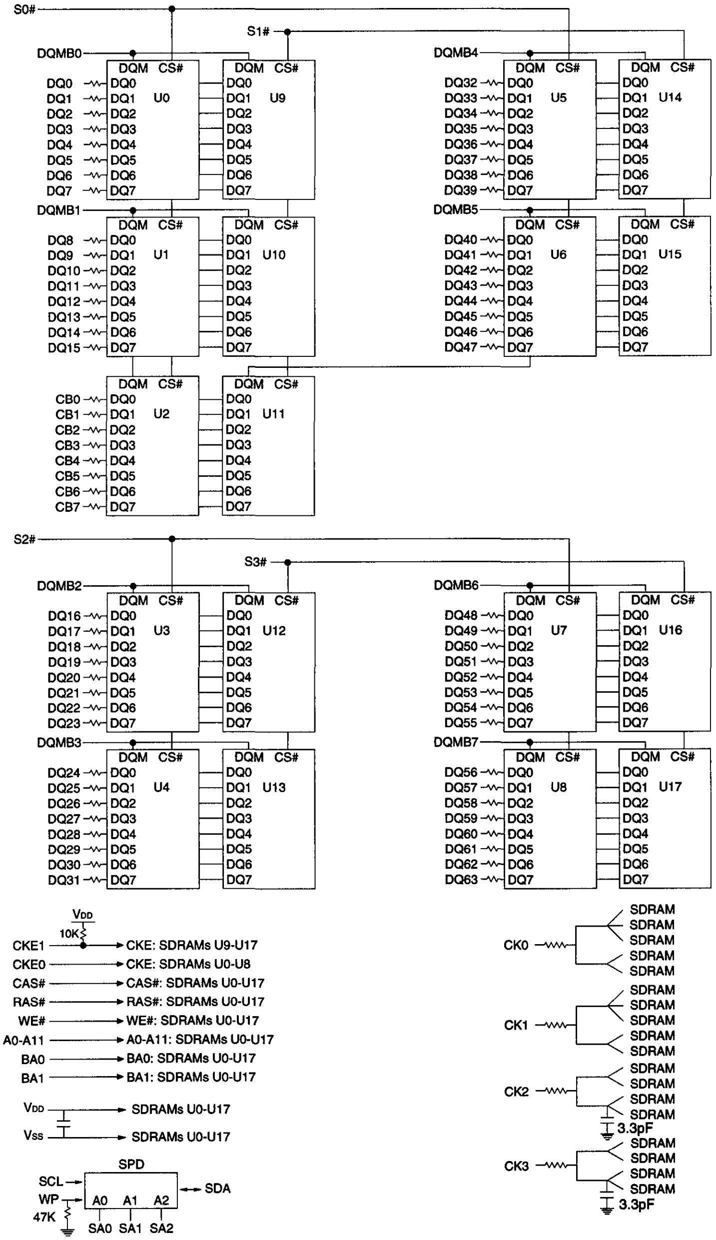
The module is designed to operate in 3.3V, low-powe memory systems. An auto refresh mode is provided, alon with a power-saving, power-down mode. All inputs an outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automati column-address generation, the ability to interleave between internal banks in order to hide precharge time and th capability to randomly change column addresses on eacl clock cycle during a burst access. For more informatio regarding SDRAM operation, refer to the 128Mb: x4, x8, x1 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD) The SPD function is implemented using a 2,048-bit EEPROM This nonvolatile storage device contains 256 bytes. The firs 128 bytes can be programmed by Micron to identify th module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage ar available for use by the customer. System READ/WRIT operations between the master (system logic) and the slav EEPROM device (DIMM) occur via a standard IIC bu using the DIMM's SCL (clock) and SDA (data) signals together with SA(2:0), which provide eight unique DIMM/ EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT18LSDT3272A (256MB)



NOTE: All resistor values are 10 ohms unless otherwise specified.

U0-U17 = MT48LC16M8A2TG SDRAMs

SYNCHRONOUS DRAM MODULE

MT36LSDT6472

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/ datasheet.html

FEATURES

- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- PC100-compliant
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- Utilizes 125 MHz SDRAM components
- ECC-optimized pinout
- 512MB (64 Meg x 72)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of PLL clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/ precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Two-clock WRITE recovery (^{t}WR) version; one-clock ^{t}WR not supported

OPTIONS MARKING

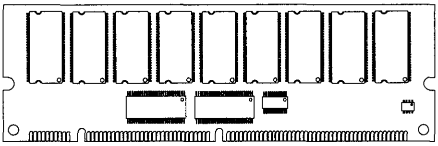
OPTIONS	MARKING
• Package	
168-pin DIMM (gold)	G
• Frequency/CAS Latency*	
100 MHz/CL = 2 (8ns, 125 MHz SDRAMs)	-10E
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10C
100 MHz/CL = 3 (8ns, 125 MHz SDRAMs)	-10B

*Device latency only; extra clock cycle required due to input register.

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-10E	-8E	2	6ns	2ns	1ns
-10B/-10C	-8B/-8C	3	6ns	2ns	1ns

PIN ASSIGNMENT (Front View)
168-Pin DIMM
(H-27)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{DD}	48	DNU	90	V_{DD}	132	NC (A13)
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC (CKE1)	105	CB4	147	REGE
22	CB1	64	V_{SS}	106	CB5	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#	156	DQ59
31	DNU	73	V_{DD}	115	RAS#	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	CK1	167	SA2
42	CK0	84	V_{DD}	126	NC (A12)	168	V_{DD}

NOTE: Symbols in parentheses are not used on this module but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT36LSDT6472G-10E__	64 Meg x 72	100 MHz
MT36LSDT6472G-10C__	64 Meg x 72	100 MHz
MT36LSDT6472G-10B__	64 Meg x 72	100 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT36LSDT6472G-10CD1

GENERAL DESCRIPTION

The MT36LSDT6472 is a high-speed CMOS, dynamic random-access, 512MB memory organized in a x72 configuration. This module uses internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of clock signal CK0).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The module provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the $2n$ rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The module is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 128Mb: x4, x8, x16 SDRAM data sheet.

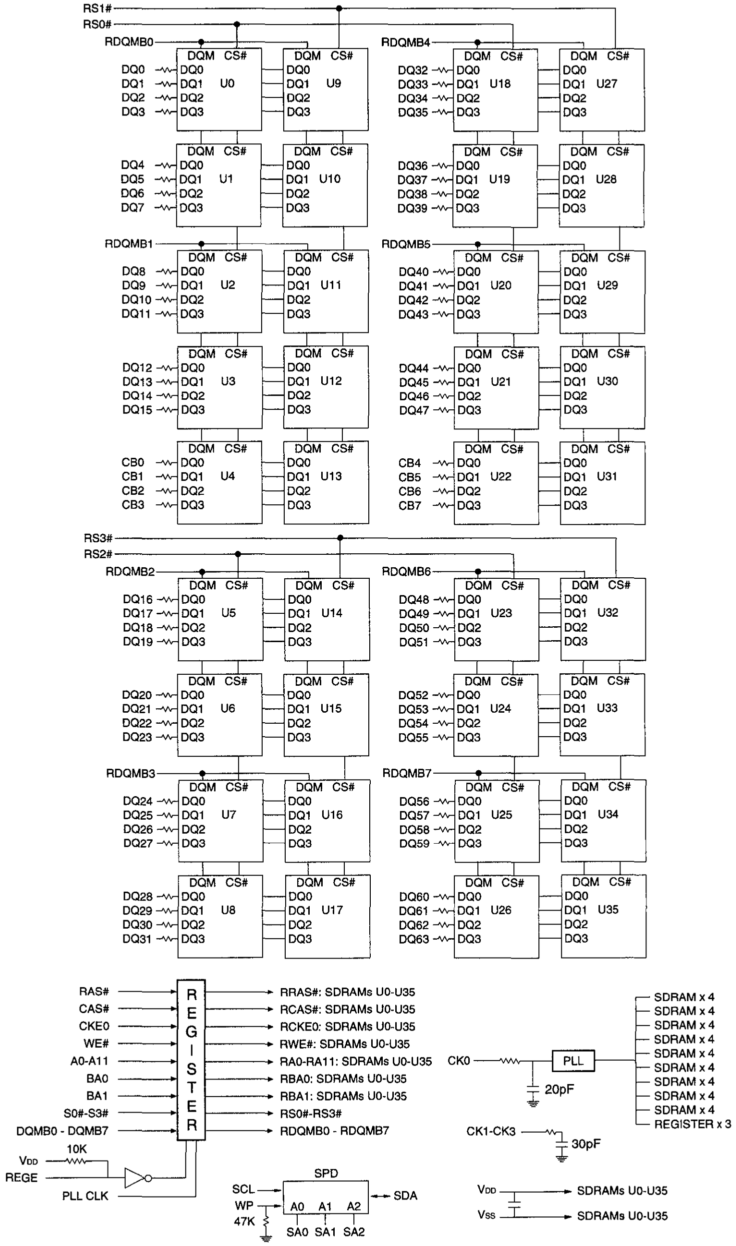
PLL AND REGISTER OPERATION

The module can be operated in either registered mode (REGE pin HIGH), where the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock), or in buffered mode (REGE pin LOW) where the input signals pass through the register/buffer to the SDRAM devices on the same clock. A phase-lock loop (PLL) on the module is used to redrive the clock signals to the SDRAM devices to minimize system clock loading (CK0 is connected to the PLL, and CK1, CK2 and CK3 are terminated).

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT36LSDT6472 (512MB)



NOTE: All resistor values are 10 ohms unless otherwise specified.

U0-U35 = MT48LC32M4A2TG SDRAMs

Micron Technology, Inc., reserves the right to change products or specifications without notice.

DRAM 1

SGRAM SODIMM PRODUCT SELECTION GUIDE

Memory Configuration	Voltage	Part Number	Clock Frequency (MHz)	Access Time (ns)	Package/No. of Pins	Page
					SODIMM	
256K x 64	3.3V	MT2LG25664H	125, 100, 83	6, 6.5, 9	144	1-153
256K x 64	3.3V	MT2LG25664KH	125, 100, 83	6, 6.5, 9	144	1-153
512K x 64	3.3V	MT4LG51264H	125, 100, 83	6, 6.5, 9	144	1-153
512K x 64	3.3V	MT4LG51264KH	125, 100, 83	6, 6.5, 9	144	1-153

SYNCHRONOUS GRAPHICS RAM SODIMM

MT2LG25664(K)H, MT4LG51264(K)H

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

JEDEC pinout in a 144-pin, small-outline, dual in-line memory module (SODIMM)
2MB (256K x 64) and 4MB (512K x 64)
Fully synchronous; all signals registered on positive edge of system clock
Single +3.3V ±0.3V power supply
LVTTL-compatible inputs and outputs
Internal pipelined operation; column address can be changed every clock cycle
Programmable burst lengths: 1, 2, 4, 8 or full page
Block Write and Write-Per-Bit Modes
Independent byte operation via DQM0-DQM7
Auto Precharge and Auto Refresh Modes
17ms, 1,024-cycle refresh
Optional serial presence-detect (SPD)

OPTIONS	MARKING
Frequency	
125 MHz	-25
100 MHz	-10
83 MHz	-83
SPD	
With SPD	None
Without SPD	K
Package	
144-pin SODIMM (gold)	G

SGRAM COMPONENT KEY TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	ACCESS TIME	SETUP TIME	HOLD TIME
-25	7ns	6ns	2ns	1ns
-10	8ns	6.5ns	2.5ns	1ns
-83	10ns	9ns	3ns	1ns

PART NUMBERS

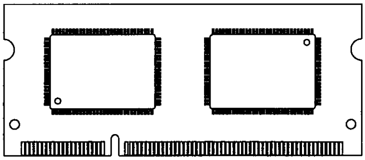
PART NUMBER	CONFIGURATION	OPTIONS
MT2LG25664HG-xx	256K x 64	SPD
MT2LG25664KHG-xx	256K x 64	
MT4LG51264HG-xx	512K x 64	SPD
MT4LG51264KHG-xx	512K x 64	

xx = frequency

PIN ASSIGNMENT (Front View)

144-Pin Small-Outline DIMM

(I-7; 2MB)
(I-6; 4MB)



PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	VSS	2	VSS	73	NC/CLK1*	74	CLK0
3	DQ63	4	DQ62	75	VDD	76	VDD
5	DQ61	6	DQ60	77	RSVD	78	RSVD
7	DQ59	8	DQ58	79	NC (A11)	80	NC (A10)
9	DQ57	10	DQ56	81	BA0 (A9)	82	A8
11	VDD	12	VDD	83	A7	84	A6
13	DQ55	14	DQ54	85	VSS	86	VSS
15	DQ53	16	DQ52	87	A5	88	A4
17	DQ51	18	DQ50	89	A3	90	A2
19	DQ49	20	DQ48	91	A1	92	A0
21	VSS	22	VSS	93	VDD	94	VDD
23	DQMB7	24	DQMB6	95	DQ31	96	DQ30
25	DQMB5	26	DQMB4	97	DQ29	98	DQ28
27	VDD	28	VDD	99	DQ27	100	DQ26
29	DQ47	30	DQ46	101	DQ25	102	DQ24
31	DQ45	32	DQ44	103	VSS	104	VSS
33	DQ43	34	DQ42	105	DQ23	106	DQ22
35	DQ41	36	DQ40	107	DQ21	108	DQ20
37	VSS	38	VSS	109	DQ19	110	DQ18
39	DQ39	40	DQ38	111	DQ17	112	DQ16
41	DQ37	42	DQ36	113	VDD	114	VDD
43	DQ35	44	DQ34	115	DQMB3	116	DQMB2
45	DQ33	46	DQ32	117	DQMB1	118	DQMB0
47	VDD	48	VDD	119	VSS	120	VSS
49	RSVD	50	RSVD	121	DQ15	122	DQ14
51	RSVD	52	RSVD	123	DQ13	124	DQ12
53	RSVD	54	RSVD	125	DQ11	126	DQ10
55	VSS	56	VSS	127	DQ9	128	DQ8
57	DSF	58	RFU	129	VDD	130	VDD
59	RFU	60	RFU	131	DQ7	132	DQ6
61	RFU	62	SA0/NC**	133	DQ5	134	DQ4
63	VDD	64	VDD	135	DQ3	136	DQ2
65	NC/CS1#*	66	CS0#	137	DQ1	138	DQ0
67	RAS#	68	CAS#	139	VSS	140	VSS
69	WE#	70	CKE	141	SDA/NC**	142	SCL/NC**
71	VSS	72	VSS	143	VDD	144	VDD

* 4MB version only
** K version only

NOTE: Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

GENERAL DESCRIPTION

The MT2LG25664(K)H and MT4LG51264(K)H SGRAM modules are high-speed CMOS, dynamic random-access 2MB and 4MB memories organized in a small-outline, x64 configuration.

Read and write accesses to the modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A8 select the row). Then the address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

Synchronous graphics RAMs (SGRAMs) differ from synchronous DRAMs (SDRAMs) by providing an eight-column BLOCK WRITE function and a MASKED WRITE (or WRITE-PER-BIT) function to accommodate high-performance graphics applications. The BLOCK WRITE and MASKED WRITE functions may be combined with individual byte enables (DQ mask or DQM pins).

The CMOS dynamic memory structure of thes modules is designed to operate in 3.3V, low-power memor systems. An auto refresh mode is provided, along with power-saving, power-down mode. All inputs and output are LVTTL-compatible. (Refer to the MT41LC256K32D SGRAM data sheet for additional information on SGRA functionality.)

RESISTOR STRAPPING DETECTION

Three resistor straps are used to indicate the modul frequency and timing. Table 1 shows the settings. A logi LOW (i.e., 0) indicates that the strapping resistor is tied t ground (Vss). A logic HIGH (i.e., 1) indicates that th strapping resistor is tied to VDD.

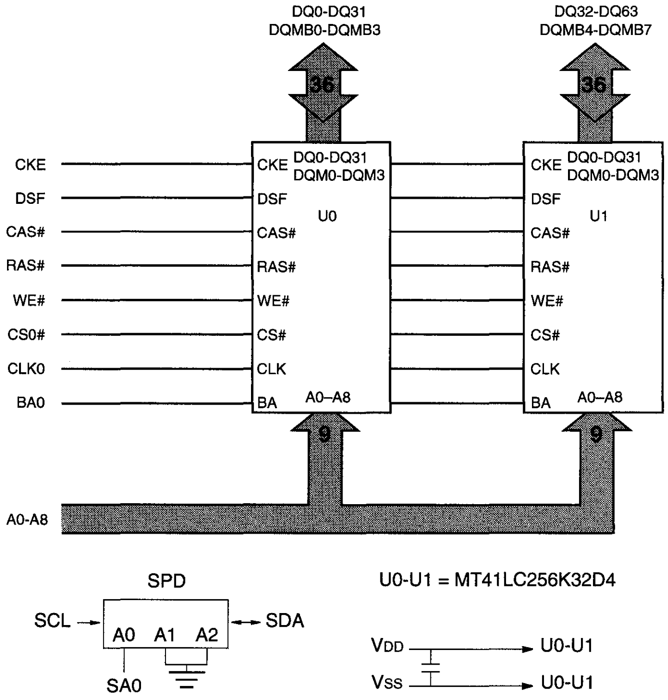
Table 1

MODULE FREQUENCY	DQ31	DQ30	DQ29
125 MHz	0	1	1
100 MHz	0	1	0
83 MHz	0	0	1

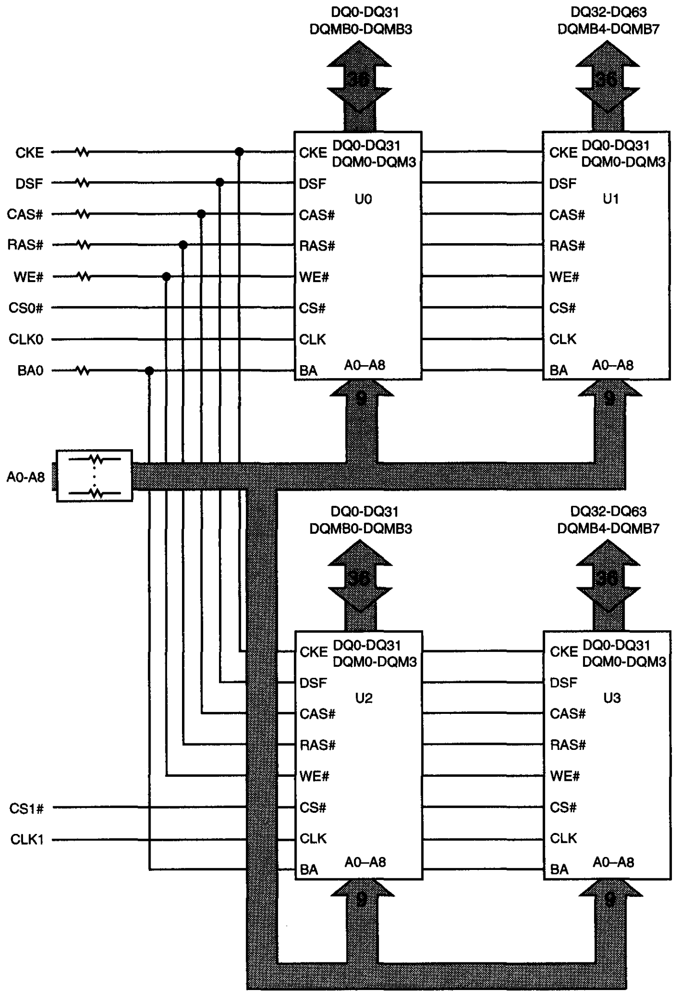
SERIAL PRESENCE-DETECT OPERATION

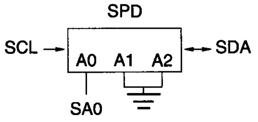
These modules can also incorporate serial presence detect (SPD). The SPD function is implemented using 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed b Micron to identify the module type and various DRA organizations and timing parameters. The remaining 12 bytes of storage are available for use by the custome System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur vi a standard IIC bus using the DIMM's SCL (clock) and SD (data) signals, together with SA(0), which provide tw unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT2LG25664(K)H (2MB)

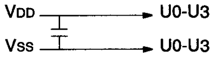


FUNCTIONAL BLOCK DIAGRAM
MT4LG51264(K)H (4MB)





U0-U3 = MT41LC256K32D4



NOTE: All resistor values are 10 ohms unless otherwise specified.

DRAM 1

DRAM DIMM/SODIMM PRODUCT SELECTION GUIDE

Memory Configuration	Part Number	Access Cycle	Access Time (ns)	Address Pins		Number of Pins		Page
				Row	Column	DIMM	SODIMM	
3.3V SODIMMs								
4 Meg x 64	MT4LDT464H	FPM	50, 60	12	10	–	144	1-165
4 Meg x 64	MT4LDT464H S	FPM, S	50, 60	12	10	–	144	1-165
4 Meg x 64	MT4LDT464H X	EDO	50, 60	12	10	–	144	1-165
4 Meg x 64	MT4LDT464H XS	EDO, S	50, 60	12	10	–	144	1-165
8 Meg x 64	MT8LDT864H	FPM	50, 60	12	11	–	144	1-165
8 Meg x 64	MT8LDT864H S	FPM, S	50, 60	12	11	–	144	1-165
8 Meg x 64	MT8LDT864H X	EDO	50, 60	12	11	–	144	1-165
8 Meg x 64	MT8LDT864H XS	EDO, S	50, 60	12	11	–	144	1-165
3.3V DIMMs								
4 Meg x 32	MT2LDT432U	FPM	50, 60	12	10	100	–	1-157
4 Meg x 32	MT2LDT432U X	EDO	50, 60	12	10	100	–	1-157
8 Meg x 32	MT4LDT832U	FPM	50, 60	12	10	100	–	1-157
8 Meg x 32	MT4LDT832U X	EDO	50, 60	12	10	100	–	1-157
4 Meg x 64	MT4LDT464A	FPM, N	50, 60	12	10	168	–	1-161
4 Meg x 64	MT4LDT464A X	EDO, N	50, 60	12	10	168	–	1-161
8 Meg x 64	MT8LDT864A	FPM, N	50, 60	12	10	168	–	1-161
8 Meg x 64	MT8LDT864A X	EDO, N	50, 60	12	10	168	–	1-161
8 Meg x 64	MT8LD864A X	EDO, N	50, 60	12	11	168	–	1-169
16 Meg x 64	MT16LD1664A X	EDO, N	50, 60	12	12	168	–	1-169
32 Meg x 64	MT32LD3264A X	EDO, N	50, 60	12	12	168	–	1-169
8 Meg x 72	MT9LD(T)872 X	EDO	50, 60	12	11	168	–	1-175
8 Meg x 72	MT9LD872A X	EDO, N	50, 60	12	11	168	–	1-181
16 Meg x 72	MT18LD(T)1672 X	EDO	50, 60	12	10	168	–	1-175
16 Meg x 72	MT18LD1672A X	EDO, N	50, 60	12	12	168	–	1-181
32 Meg x 72	MT36LD(T)3272 X	EDO	50, 60	12	12	168	–	1-175
32 Meg x 72	MT36LD3272A X	EDO, N	50, 60	12	12	168	–	1-181

FPM = FAST PAGE MODE; EDO = Extended Data-Out; N = Nonbuffered; S = Self Refresh

DRAM MODULE

MT2LDT432U (X), MT4LDT832U (X)

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/ datasheet.html

FEATURES

- JEDEC pinout in a 100-pin, dual in-line memory module (DIMM)
- 16MB (4 Meg x 32) and 32MB (8 Meg x 32)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are TTL-compatible
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) refresh distributed across 64ms
- FAST-PAGE-MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- Serial presence-detect (SPD)

OPTIONS

OPTIONS	MARKING
• Package	
100-pin DIMM (gold)	G
• Timing	
50ns access	-5
60ns access	-6
• Access Cycles	
FAST PAGE MODE	None
EDO PAGE MODE	X

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

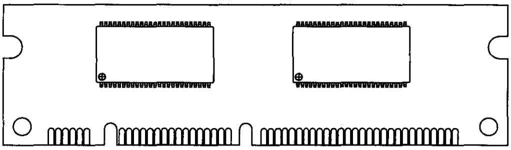
FPM Operating Mode

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}RP
-5	90ns	50ns	30ns	25ns	13ns	30ns
-6	110ns	60ns	35ns	30ns	15ns	40ns

PIN ASSIGNMENT (Front View)

100-Pin DIMM

(H-1; 16MB)
(H-2; 32MB)



PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK
1	Vss	26	Vss	51	Vss	76	Vss
2	DQ0	27	DNU	52	DQ8	77	DNU
3	DQ1	28	WE#	53	DQ9	78	OE#
4	DQ2	29	RAS0#	54	DQ10	79	RAS1#
5	DQ3	30	RAS2#	55	DQ11	80	RAS3#
6	Vdd	31	Vdd	56	Vdd	81	Vdd
7	DQ4	32	NC	57	DQ12	82	NC
8	DQ5	33	NC	58	DQ13	83	NC
9	DQ6	34	NC	59	DQ14	84	NC
10	DQ7	35	NC	60	DQ15	85	NC
11	CAS0#	36	Vss	61	CAS1#	86	Vss
12	Vss	37	CAS2#	62	Vss	87	CAS3#
13	A0	38	DQ16	63	A1	88	DQ24
14	A2	39	DQ17	64	A3	89	DQ25
15	A4	40	DQ18	65	A5	90	DQ26
16	A6	41	DQ19	66	A7	91	DQ27
17	A8	42	Vdd	67	A9	92	Vdd
18	A10	43	DQ20	68	A11	93	DQ28
19	NC (A12)	44	DQ21	69	NC (A13)	94	DQ29
20	NC	45	DQ22	70	NC	95	DQ30
21	Vdd	46	DQ23	71	Vdd	96	DQ31
22	DNU	47	Vss	72	DNU	97	Vss
23	RFU	48	SDA	73	DNU	98	SA0
24	RFU	49	SCL	74	RFU	99	SA1
25	DNU	50	Vdd	75	DNU	100	SA2

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	SPEED
MT2LDT432UG-5 X	4 Meg x 32	50ns
MT2LDT432UG-6 X	4 Meg x 32	60ns
MT4LDT832UG-5 X	8 Meg x 32	50ns
MT4LDT832UG-6 X	8 Meg x 32	60ns

FPM Operating Mode

PART NUMBER	CONFIGURATION	SPEED
MT2LDT432UG-5	4 Meg x 32	50ns
MT2LDT432UG-6	4 Meg x 32	60ns
MT4LDT832UG-5	8 Meg x 32	50ns
MT4LDT832UG-6	8 Meg x 32	60ns

GENERAL DESCRIPTION

The MT2LDT432U (X) and MT4LDT832U (X) are randomly accessed 16MB and 32MB memories organized in a x32 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each location is uniquely addressed via the address bits. The row address is latched by the RAS# signal, then the column address is latched by the CAS# signal.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z, regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data outputs will drive read data from the accessed location.

FAST PAGE MODE

FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" option, is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW and WE# is held HIGH. (Refer to the 4 Meg x 16 [MT4LC4M16R6] DRAM data sheet for additional information on EDO functionality.)

REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

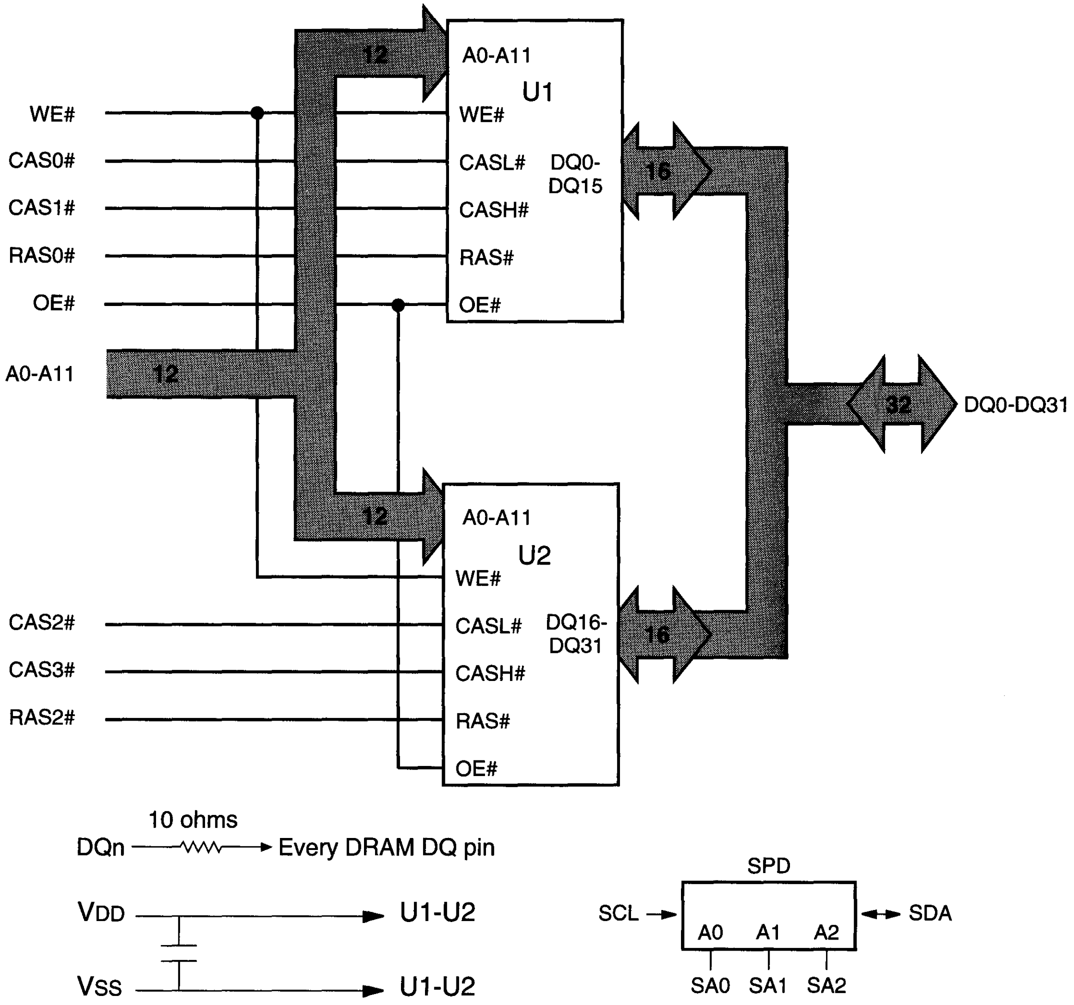
STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time.

SERIAL PRESENCE-DETECT OPERATION

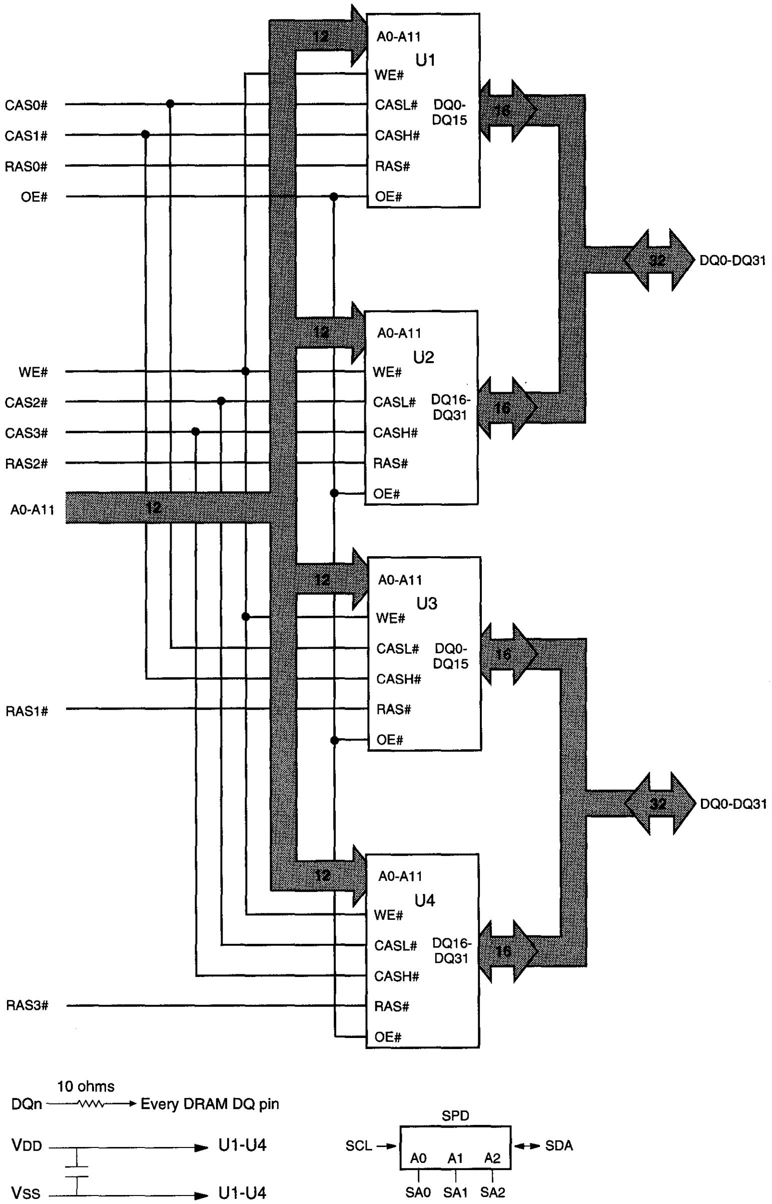
This module family incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT2LDT432U (X) (16MB)



U1-U2 = MT4LC4M16F5 FAST PAGE MODE
U1-U2 = MT4LC4M16R6 EDO PAGE MODE

FUNCTIONAL BLOCK DIAGRAM
MT4LDT832U (X) (32MB)



U1-U4 = MT4LC4M16F5 FAST PAGE MODE
U1-U4 = MT4LC4M16R6 EDO PAGE MODE

MICRON
TECHNOLOGY, INC.

4, 8 MEG x 64
NONBUFFERED DRAM DIMMs

DRAM MODULE

MT4LDT464A (X), MT8LDT864A (X)

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC-standard ECC pinout in a 168-pin, dual in-line memory module (DIMM)
- 32MB (4 Meg x 64) and 64MB (8 Meg x 64)
- Nonbuffered
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are LVTTL-compatible
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) refresh distributed across 64ms
- FAST-PAGE-MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- Serial presence-detect (SPD)

OPTIONS / MARKING

OPTIONS	MARKING
• Package	
168-pin DIMM (gold)	G
• Timing	
50ns access	-5
60ns access	-6
• Access Cycle	
FAST PAGE MODE	None
EDO PAGE MODE	X

KEY TIMING PARAMETERS

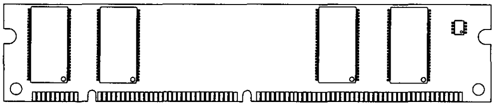
EDO Operating Mode

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

FPM Operating Mode

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}RP
-5	90ns	50ns	30ns	25ns	13ns	30ns
-6	110ns	60ns	35ns	30ns	15ns	40ns

PIN ASSIGNMENT (Front View)
168-Pin DIMM
(H-10; 32MB), (H-11; 64MB)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2#	86	DQ32	128	RFU
3	DQ1	45	RAS2#	87	DQ33	129	RAS3#
4	DQ2	46	CAS2#	88	DQ34	130	CAS6#
5	DQ3	47	CAS3#	89	DQ35	131	CAS7#
6	VDD	48	WE2#	90	VDD	132	RFU
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	RFU	104	DQ47	146	RFU
21	NC	63	NC	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	Vss	110	VDD	152	Vss
27	WE0#	69	DQ24	111	RFU	153	DQ56
28	CAS0#	70	DQ25	112	CAS4#	154	DQ57
29	CAS1#	71	DQ26	113	CAS5#	155	DQ58
30	RAS0#	72	DQ27	114	RAS1#	156	DQ59
31	OE0#	73	VDD	115	RFU	157	VDD
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	NC (A12)	81	NC	123	NC (A13)	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	RFU	167	SA2
42	RFU	84	VDD	126	RFU	168	VDD

NOTE: Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	SPEED
MT4LDT464AG-5 X	4 Meg x 64	50ns
MT4LDT464AG-6 X	4 Meg x 64	60ns
MT8LDT864AG-5 X	8 Meg x 64	50ns
MT8LDT864AG-6 X	8 Meg x 64	60ns

FPM Operating Mode

PART NUMBER	CONFIGURATION	SPEED
MT4LDT464AG-5	4 Meg x 64	50ns
MT4LDT464AG-6	4 Meg x 64	60ns
MT8LDT864AG-5	8 Meg x 64	50ns
MT8LDT864AG-6	8 Meg x 64	60ns

GENERAL DESCRIPTION

The MT4LDT464A (X) and MT8LDT864A (X) are randomly accessed 32MB and 64MB memories organized in a x64 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 12 bits (A0-A11) at RAS# time and 10 bits (A0-A9) at CAS# time.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data-outputs will drive read data from the accessed location.

EDO PAGE MODE

EDO PAGE MODE is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also tristate the outputs. Independent of OE# control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last. (Refer to the 4 Meg x 16 [MT4LC4M16R6] DRAM data sheet for additional information on EDO functionality.)

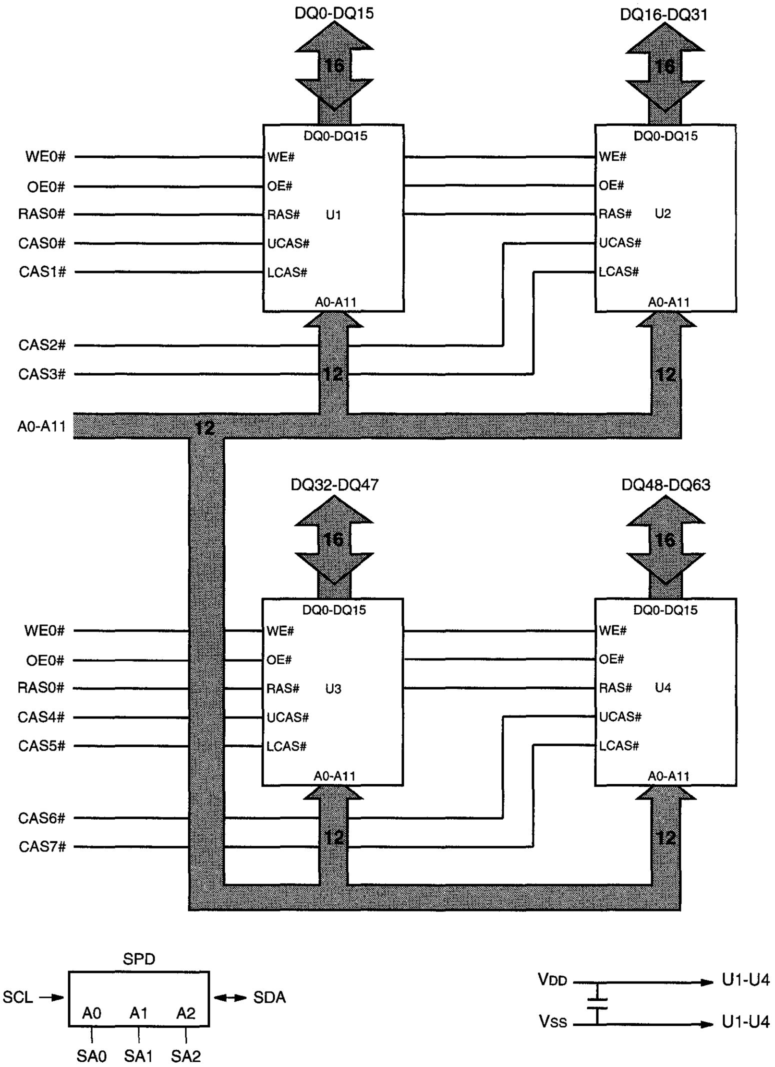
REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses (A0-A11) are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

SERIAL PRESENCE-DETECT OPERATION

This module family incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

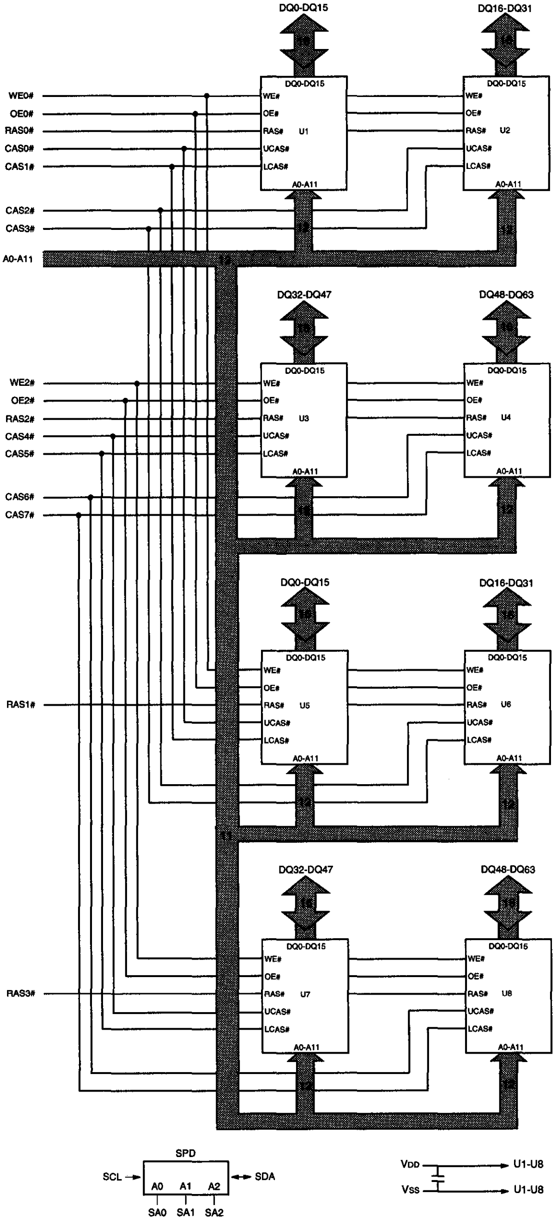
FUNCTIONAL BLOCK DIAGRAM
MT4LDT464A (X) (32MB)



U1-U4 = MT4LC4M16F5 FAST PAGE MODE

U1-U4 = MT4LC4M16R6 EDO PAGE MODE

FUNCTIONAL BLOCK DIAGRAM
MT8LDT864A (X) (64MB)



U1-U8 = MT4LC4M16F5 FAST PAGE MODE U1-U8 = MT4LC4M16R6 EDO PAGE MODE

MICRON
TECHNOLOGY, INC.

4, 8 MEG x 64
DRAM SODIMMs

SMALL-OUTLINE DRAM MODULE

MT4LDT464H (X)(S), MT8LDT864H (X)(S)

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC pinout in a 144-pin, small-outline, dual in-line memory module (SODIMM)
- 32MB (4 Meg x 64) and 64MB (8 Meg x 64)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are TTL-compatible
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) refresh distributed across 64ms
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- Optional Self Refresh Mode (S)
- Serial presence-detect (SPD)

OPTIONS	MARKING
• Package	
144-pin SODIMM (gold)	G
• Timing	
50ns access	-5
60ns access	-6
• Access Cycles	
FAST PAGE MODE	None
EDO PAGE MODE	X
• Refresh Rates	
Standard Refresh	None
Self Refresh (128ms period)	S*

*Contact factory for availability

KEY TIMING PARAMETERS

FPM Operating Mode

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}RP
-5	90ns	50ns	30ns	25ns	13ns	30ns
-6	110ns	60ns	35ns	30ns	15ns	40ns

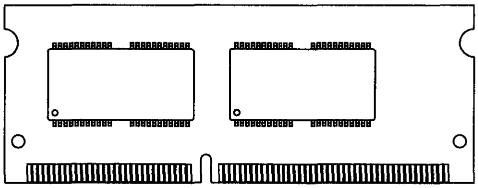
EDO Operating Mode

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

PIN ASSIGNMENT (Front View)

144-Pin Small-Outline DIMM

(I-1; 32MB)
(I-2; 64MB)



PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	Vss	2	Vss	73	OE#	74	RFU
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	RSVD	78	RSVD
7	DQ2	8	DQ34	79	RSVD	80	RSVD
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	CAS0#	24	CAS4#	95	DQ21	96	DQ53
25	CAS1#	26	CAS5#	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	A11
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	NC (A12)
39	DQ9	40	DQ41	111	A10	112	NC (A13)
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	CAS2#	116	CAS6#
45	VDD	46	VDD	117	CAS3#	118	CAS7#
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	RSVD	58	RSVD	129	VDD	130	VDD
59	RSVD	60	RSVD	131	DQ28	132	DQ60
61	RFU	62	RFU	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	RFU	66	RFU	137	DQ31	138	DQ63
67	WE#	68	RFU	139	Vss	140	Vss
69	RAS0#	70	NC	141	SDA	142	SCL
71	NC	72	NC	143	VDD	144	VDD

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

FPM Operating Mode

PART NUMBER	CONFIGURATION	REFRESH
MT4LDT464HG-x	4 Meg x 64	Standard
MT4LDT464HG-x S	4 Meg x 64	Self
MT8LDT864HG-x	8 Meg x 64	Standard
MT8LDT864HG-x S	8 Meg x 64	Self

x = speed

EDO Operating Mode

PART NUMBER	CONFIGURATION	REFRESH
MT4LDT464HG-x X	4 Meg x 64	Standard
MT4LDT464HG-x XS	4 Meg x 64	Self
MT8LDT864HG-x X	8 Meg x 64	Standard
MT8LDT864HG-x XS	8 Meg x 64	Self

x = speed

GENERAL DESCRIPTION

The MT4LDT464H (X)(S) and MT8LDT864H (X)(S) are randomly accessed 32MB and 64MB memories organized in a small-outline, x64 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each location is uniquely addressed via the address bits. The row address is latched by the RAS# signal, then the column address is latched by the CAS# signal.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z, regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data outputs will drive read data from the access location.

FAST PAGE MODE

FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" option, is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW and WE# is held HIGH. (Refer to the 8 Meg x 8 EDO DRAM data sheet for additional information on EDO functionality.)

REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

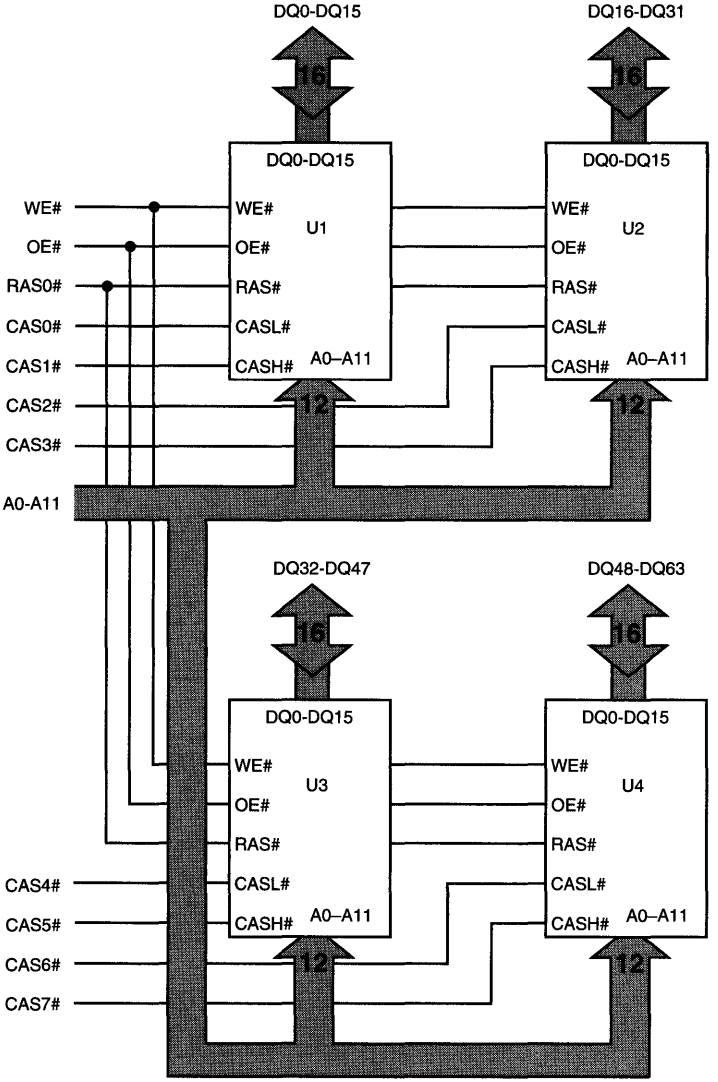
An optional self refresh mode is also available on the "S" version. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms, or 125µs per row when using distributed CBR REFESH. The optional self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^{t}RASS.

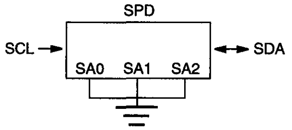
The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst refresh sequence, all 1,240 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time.

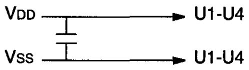
FUNCTIONAL BLOCK DIAGRAM
MT4LDT464H (X) (32MB)



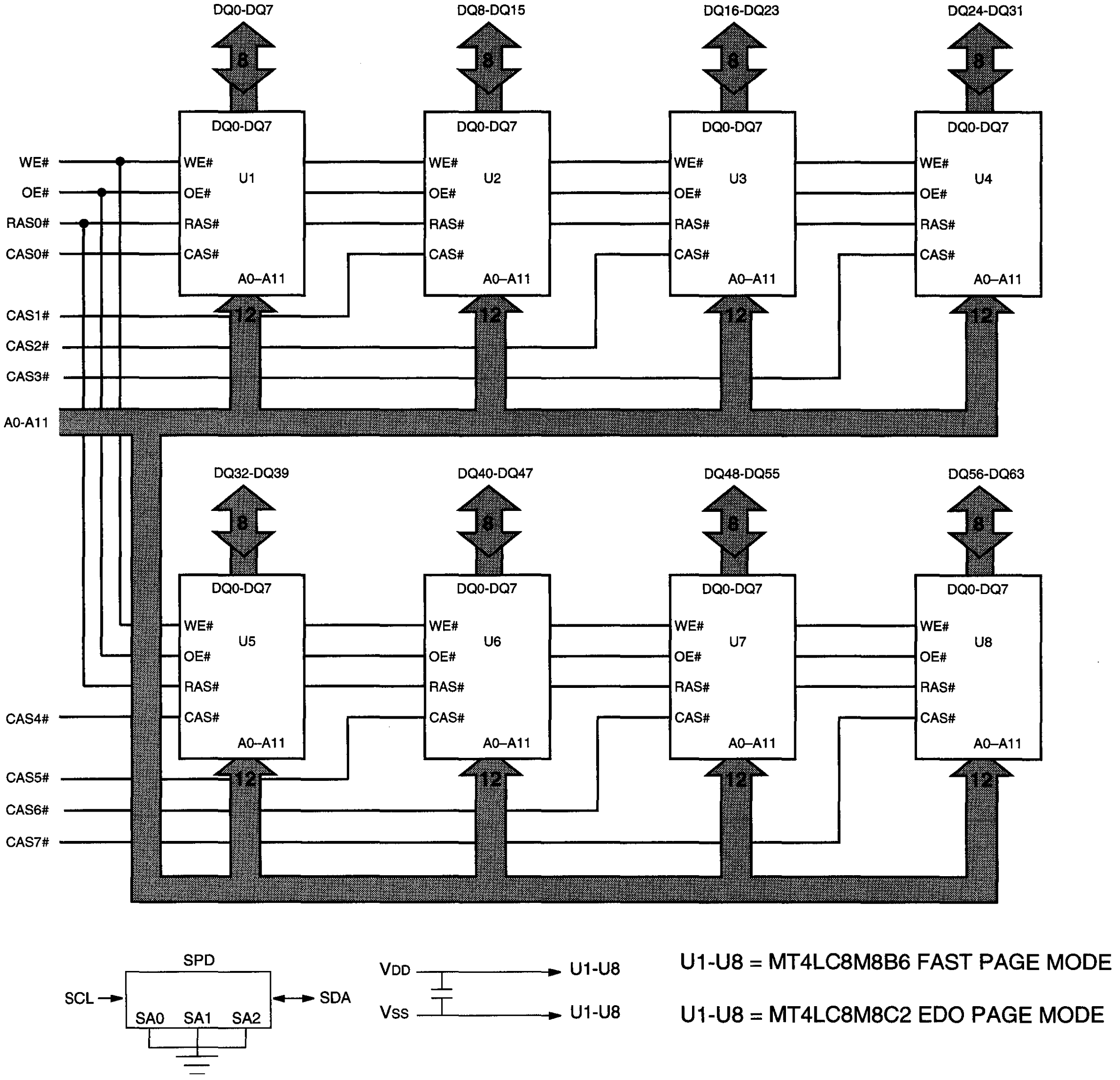


U1-U4 = MT4LC4M16R6 EDO PAGE MODE

U1-U4 = MT4LC4M16F5 FAST PAGE MODE



FUNCTIONAL BLOCK DIAGRAM
MT8LDT864H (X) (64MB)



U1-U8 = MT4LC8M8B6 FAST PAGE MODE

U1-U8 = MT4LC8M8C2 EDO PAGE MODE

DRAM MODULE

MT8LD864A X, MT16LD1664A X, MT32LD3264A X

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Eight-CAS# ECC pinout in a 168-pin, dual in-line memory module (DIMM)
- 64MB (8 Meg x 64), 128MB (16 Meg x 64) and 256MB (32 Meg x 64)
- Nonbuffered
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are LVTTL-compatible
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) refresh distributed across 64ms
- Extended Data-Out (EDO) PAGE MODE access cycle
- Serial presence-detect (SPD)

OPTIONS

OPTIONS	MARKING
• Package	
168-pin DIMM (gold)	G
• Timing	
50ns access	-5
60ns access	-6
• Access Cycle	
EDO PAGE MODE	X

KEY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

PART NUMBERS

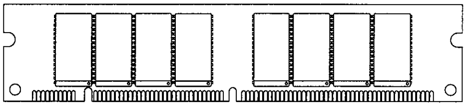
PART NUMBER	CONFIGURATION	SPEED
MT8LD864AG-5 X	8 Meg x 64	50ns
MT8LD864AG-6 X	8 Meg x 64	60ns
MT16LD1664AG-5 X	16 Meg x 64	50ns
MT16LD1664AG-6 X	16 Meg x 64	60ns
MT32LD3264AG-5 X*	32 Meg x 64	50ns
MT32LD3264AG-6 X*	32 Meg x 64	60ns

*Contact factory for availability

NOTE: Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PIN ASSIGNMENT (Front View) 168-Pin DIMM

(H-14; 64MB)
(H-17; 128MB)
(H-30; 256MB)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2#	86	DQ32	128	RFU
3	DQ1	45	RAS2#	87	DQ33	129	NC/RAS3#**
4	DQ2	46	CAS2#	88	DQ34	130	CAS6#
5	DQ3	47	CAS3#	89	DQ35	131	CAS7#
6	VDD	48	WE2#	90	VDD	132	RFU
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	RFU	104	DQ47	146	RFU
21	NC	63	NC	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	Vss	110	VDD	152	Vss
27	WE0#	69	DQ24	111	RFU	153	DQ56
28	CAS0#	70	DQ25	112	CAS4#	154	DQ57
29	CAS1#	71	DQ26	113	CAS5#	155	DQ58
30	RAS0#	72	DQ27	114	NC/RAS1#**	156	DQ59
31	OE0#	73	VDD	115	RFU	157	VDD
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	NC (A12)	81	NC	123	NC (A13)	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	RFU	167	SA2
42	RFU	84	VDD	126	RFU	168	VDD

** 256MB version only

GENERAL DESCRIPTION

The Micron® MT8LD864A X, MT16LD1664A X and MT32LD3264A X are randomly accessed 64MB, 128MB and 256MB memories organized in a x64 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 22/23 address bits, which are entered 12 bits (A0-A11) at RAS# time and 11/12 bits (A0-A11) at CAS# time.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data-outputs will drive read data from the accessed location.

EDO PAGE MODE

EDO PAGE MODE is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also tristate the outputs. Independent of OE# control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last. (Refer to the 16 Meg x 4 [MT4LC16M4H9] DRAM data sheet for additional information on EDO functionality.)

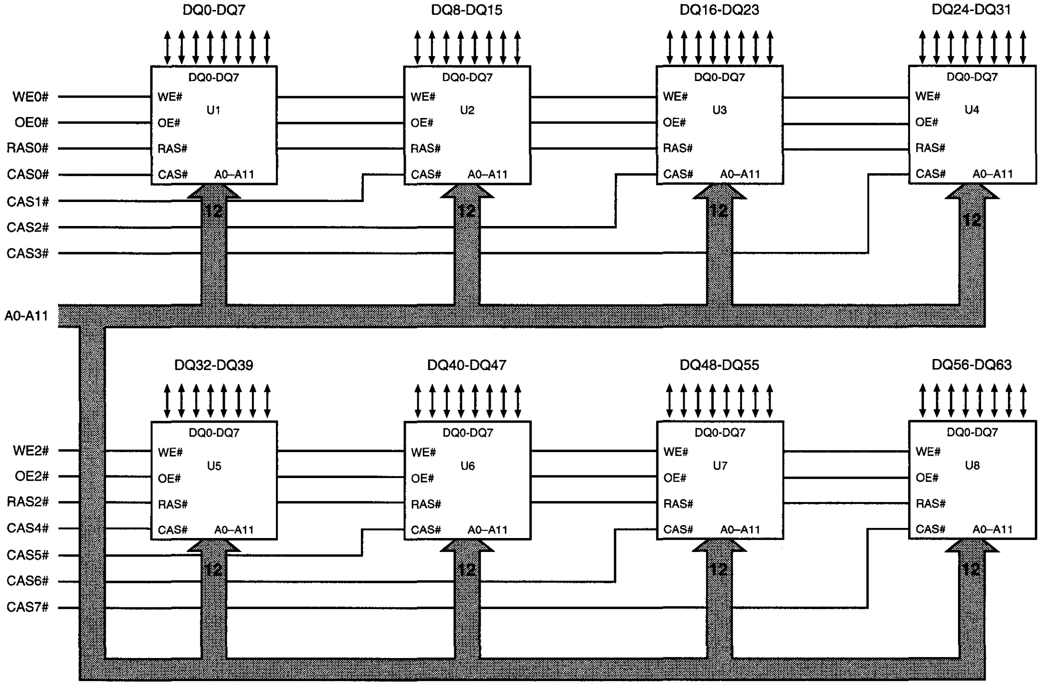
REFRESH

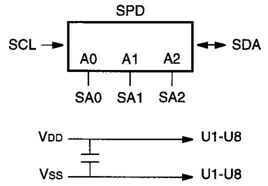
Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses (A0-A10/A11) are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

SERIAL PRESENCE-DETECT OPERATION

This module family incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide 8 unique DIMM/EEPROM addresses.

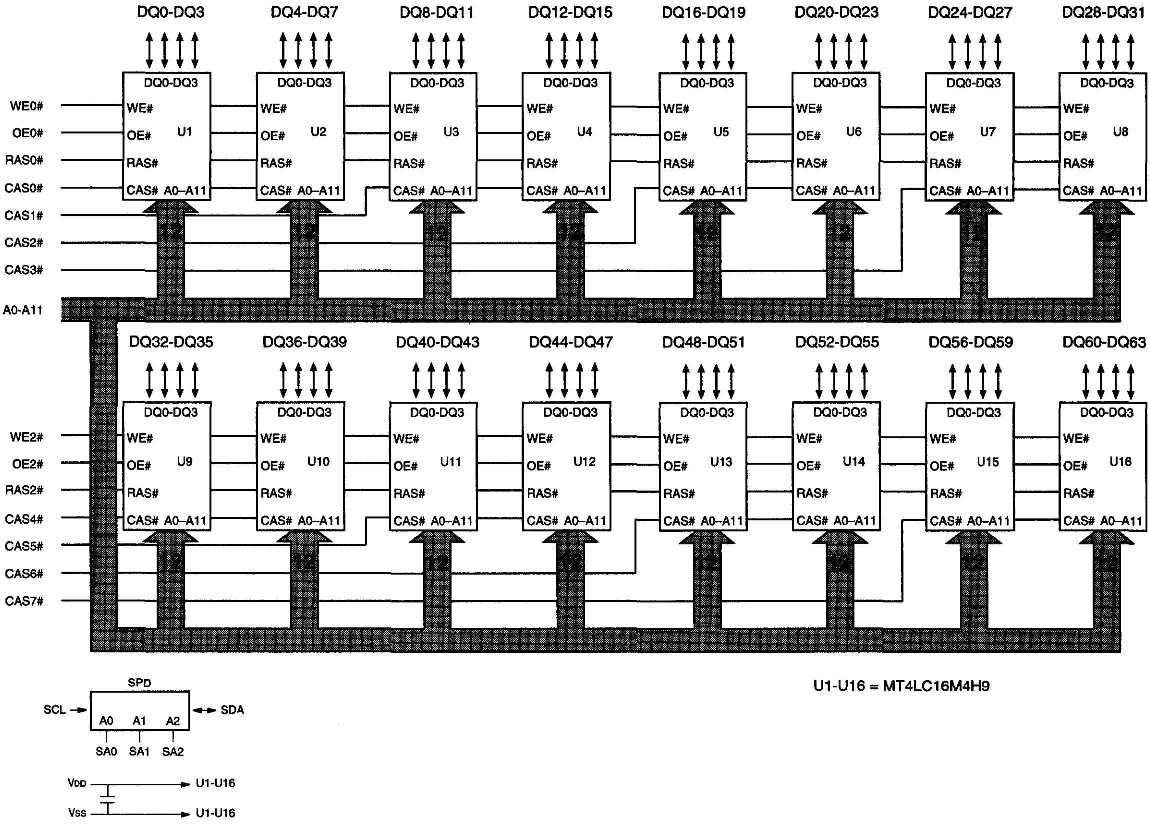
FUNCTIONAL BLOCK DIAGRAM
MT8LD864A X (64MB)





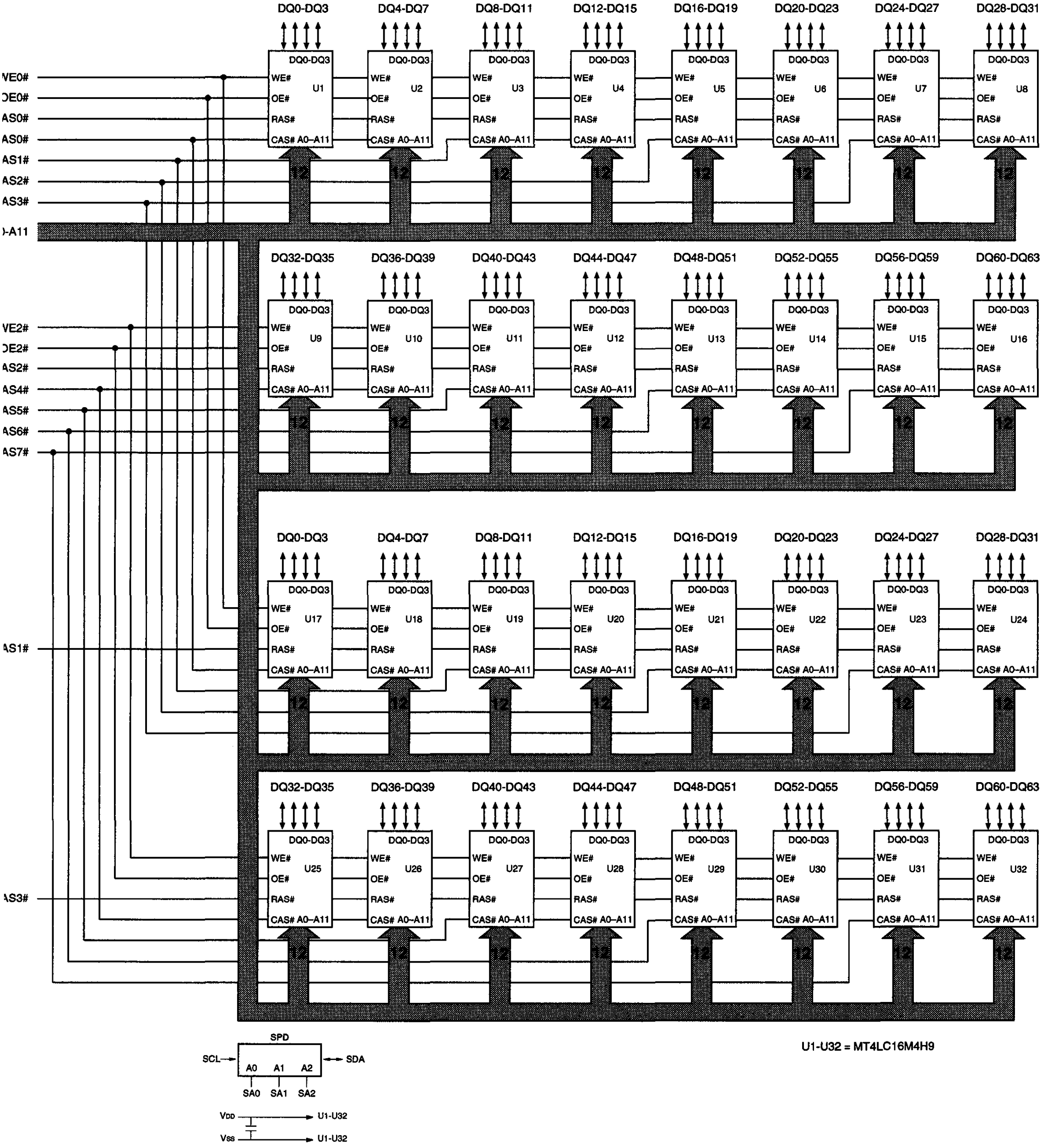
U1-U8 = MT4LC8M8C2

FUNCTIONAL BLOCK DIAGRAM
MT16LD1664A X (128MB)



U1-U16 = MT4LC16M4H9

FUNCTIONAL BLOCK DIAGRAM
MT32LD3264A X (256MB)



U1-U32 = MT4LC16M4H9

DRAM MODULE

MT9LD(T)872 X, MT18LD(T)1672 X, MT36LD(T)3272 X

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC-standard ECC pinout in a 168-pin, dual in-line memory module (DIMM)
- 64MB (8 Meg x 72), 128MB (16 Meg x 72) and 256MB (32 Meg x 72)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are LVTTL-compatible
- All inputs are buffered except RAS#
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) refresh distributed across 64ms
- Extended Data-Out (EDO) PAGE MODE access cycle

OPTIONS

OPTIONS	MARKING
• Components	
SOJ	D
TSOP	DT
• Package	
168-pin DIMM (gold)	G
• Timing	
50ns access	-5
60ns access	-6
• Access Cycle	
EDO PAGE MODE	X

KEY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-5	84ns	50ns	20ns	30ns	18ns	8ns
-6	104ns	60ns	25ns	35ns	20ns	10ns

PART NUMBERS

PART NUMBER	CONFIGURATION	SPEED
MT9LD872G-5 X	8 Meg x 72 ECC	50ns
MT9LDT872G-5 X	8 Meg x 72 ECC	50ns
MT9LD872G-6 X	8 Meg x 72 ECC	60ns
MT9LDT872G-6 X	8 Meg x 72 ECC	60ns
MT18LD1672G-5 X	16 Meg x 72 ECC	50ns
MT18LDT1672G-5 X	16 Meg x 72 ECC	50ns
MT18LD1672G-6 X	16 Meg x 72 ECC	60ns
MT18LDT1672G-6 X	16 Meg x 72 ECC	60ns
MT36LD3272G-5 X	32 Meg x 72 ECC	50ns
MT36LDT3272G-5 X	32 Meg x 72 ECC	50ns
MT36LD3272G-6 X	32 Meg x 72 ECC	60ns
MT36LDT3272G-6 X	32 Meg x 72 ECC	60ns

PIN ASSIGNMENT (Front View)

168-Pin DIMM

(H-16; 64MB, SOJ), (H-20; 64MB, TSOP),
(H-13; 128MB, SOJ), (H-31; 128MB, TSOP),
(H-29; 256MB, SOJ), (H-32; 256MB, TSOP)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2#	86	DQ36	128	RFU
3	DQ1	45	RAS2#	87	DQ37	129	NC/RAS3#*
4	DQ2	46	CAS4#	88	DQ38	130	NC/CAS5#*
5	DQ3	47	RFU	89	DQ39	131	RFU
6	Vdd	48	WE2#	90	Vdd	132	PDE#
7	DQ4	49	Vdd	91	DQ40	133	Vdd
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	Vdd	101	DQ49	143	Vdd
18	Vdd	60	DQ24	102	Vdd	144	DQ60
19	DQ14	61	RFU	103	DQ50	145	RFU
20	DQ15	62	RFU	104	DQ51	146	RFU
21	DQ16	63	RFU	105	DQ52	147	RFU
22	DQ17	64	RFU	106	DQ53	148	RFU
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vdd	68	Vss	110	Vdd	152	Vss
27	WE0#	69	DQ28	111	RFU	153	DQ64
28	CAS0#	70	DQ29	112	NC/CAS1#*	154	DQ65
29	RFU	71	DQ30	113	RFU	155	DQ66
30	RAS0#	72	DQ31	114	NC/RAS1#*	156	DQ67
31	OE0#	73	Vdd	115	RFU	157	Vdd
32	Vss	74	DQ32	116	Vss	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC (A12)	81	PD5	123	NC (A13)	165	PD6
40	Vdd	82	PD7	124	Vdd	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vdd	126	B0	168	Vdd

*256MB version only

NOTE: Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

GENERAL DESCRIPTION

The Micron® MT9LD(T)872 X, MT18LD(T)1672 X and MT36LD(T)3272 X are randomly accessed 64MB, 128MB and 256MB memories organized in a x72 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the address bits. First, the row address is latched by the RAS# signal, then the column address by CAS#. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ35, while B0 is common to the DRAMs used for DQ36-DQ71.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. EARLY WRITE occurs when WE# goes LOW prior to CAS# going LOW, and the output pins remain open (High-Z) until the next CAS# cycle.

EDO PAGE MODE

EDO PAGE MODE is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

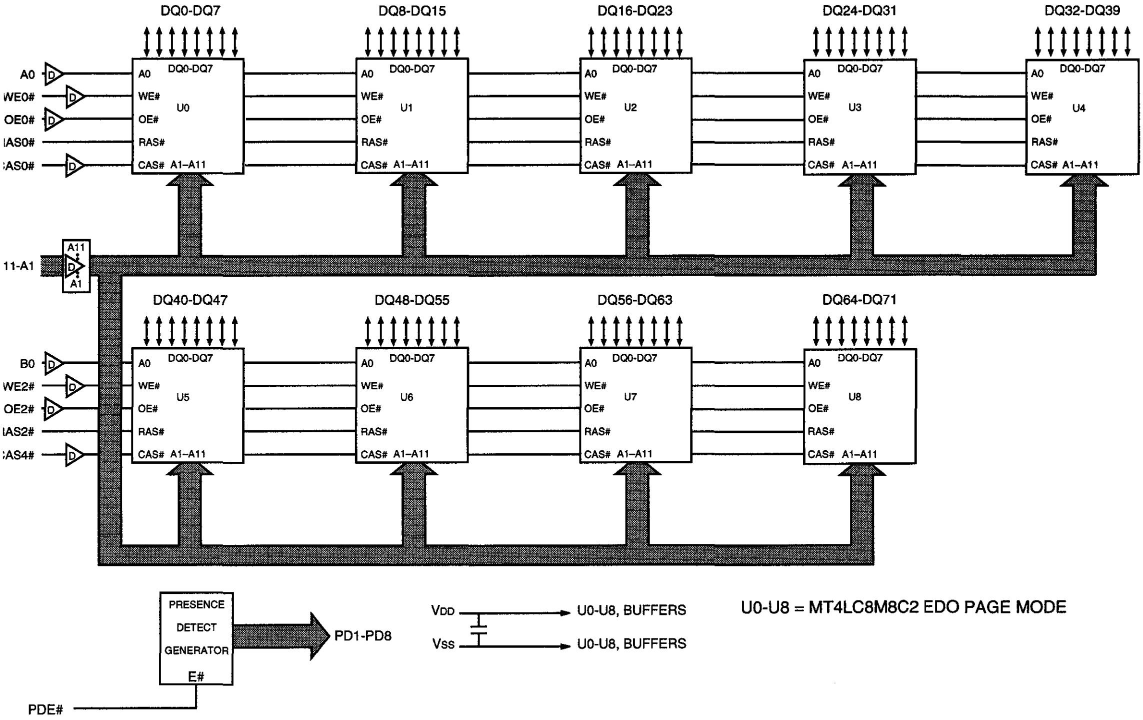
FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also tristate the outputs. Independent of OE# control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last. (Refer to the MT4LC16M4H9 DRAM data sheet for additional information on EDO functionality.)

REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all 4,096 combinations of RAS# addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

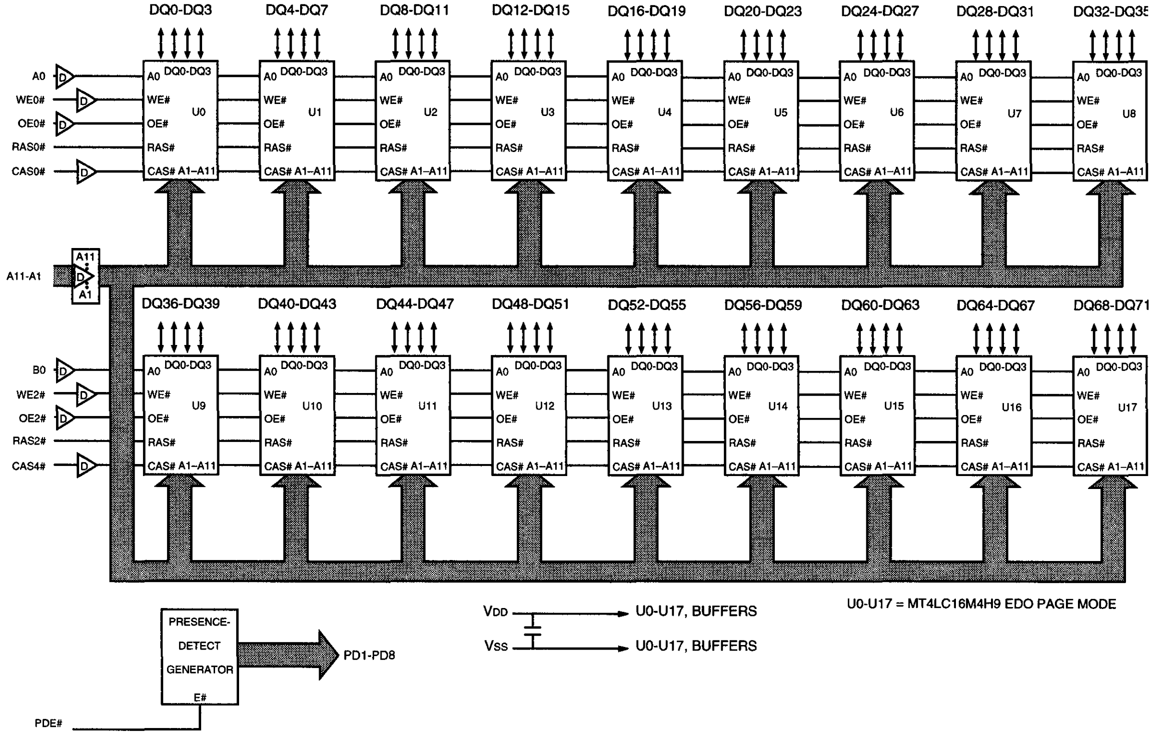
FUNCTIONAL BLOCK DIAGRAM
MT9LD(T)872 X (64MB)



U0-U8 = MT4LC8M8C2 EDO PAGE MODE

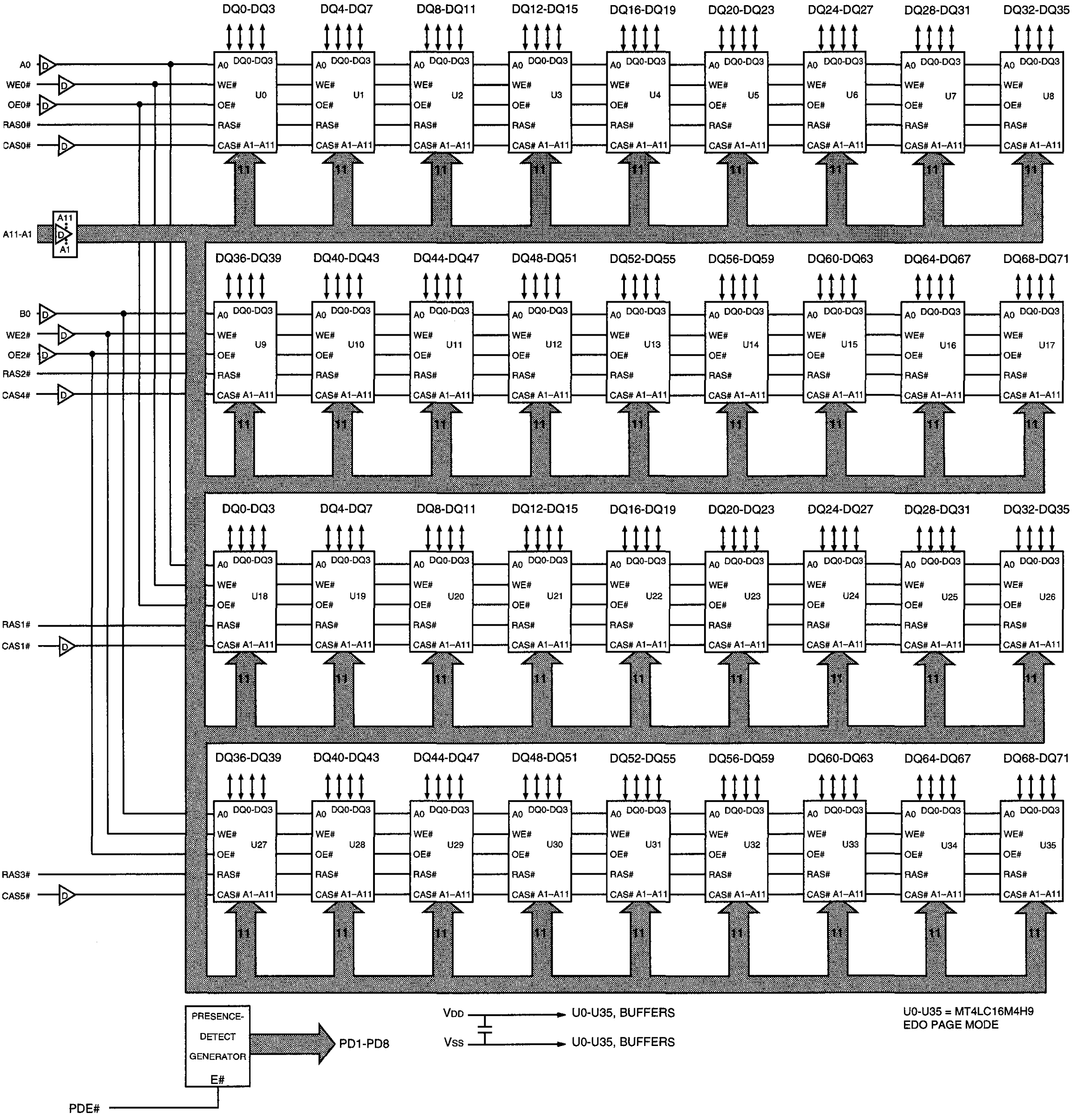
OTE: 1. All inputs with the exception of RAS# are redriven.
2. D = line buffers.

FUNCTIONAL BLOCK DIAGRAM
MT18LD(T)1672 X (128MB)



NOTE: 1. All inputs with the exception of RAS# are redriven.
2. D = line buffers.

FUNCTIONAL BLOCK DIAGRAM
MT36LD(T)3272 X (256MB)



NOTE: 1. All inputs with the exception of RAS# are redriven.
2. D = line buffers.

MICRON TECHNOLOGY INC.

8, 16, 32 MEG x 72
NONBUFFERED DRAM DIMMs

DRAM MODULE

MT9LD872A X, MT18LD1672A X, MT36LD3272A X

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

EATURES

- Eight-CAS# ECC pinout in a 168-pin, dual in-line memory module (DIMM)
- 64MB (8 Meg x 72), 128MB (16 Meg x 72) and 256MB (32 Meg x 72)
- Nonbuffered
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are LVTTL-compatible
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) refresh distributed across 64ms
- Extended Data-Out (EDO) PAGE MODE access cycle
- Serial presence-detect (SPD)

PTIONS MARKING

Package	
168-pin DIMM (gold)	G
Timing	
50ns access	-5
60ns access	-6
Access Cycle	
EDO PAGE MODE	X

EY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

ART NUMBERS

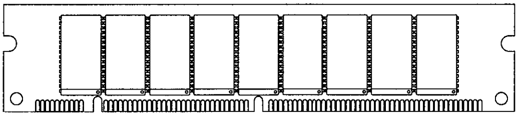
PART NUMBER	CONFIGURATION	SPEED
MT9LD872AG-5 X	8 Meg x 72 ECC	50ns
MT9LD872AG-6 X	8 Meg x 72 ECC	60ns
MT18LD1672AG-5 X	16 Meg x 72 ECC	50ns
MT18LD1672AG-6 X	16 Meg x 72 ECC	60ns
MT36LD3272AG-5 X*	32 Meg x 72 ECC	50ns
MT36LD3272AG-6 X*	32 Meg x 72 ECC	60ns

ontact factory for availability

OTE: Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PIN ASSIGNMENT (Front View)
168-Pin DIMM

(H-12; 64MB), (H-15; 128MB), (H-28; 256MB)



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2#	86	DQ32	128	RFU
3	DQ1	45	RAS2#	87	DQ33	129	NC/RAS3#**
4	DQ2	46	CAS2#	88	DQ34	130	CAS6#
5	DQ3	47	CAS3#	89	DQ35	131	CAS7#
6	VDD	48	WE2#	90	VDD	132	RFU
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	RFU	104	DQ47	146	RFU
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	Vss	110	VDD	152	Vss
27	WE0#	69	DQ24	111	RFU	153	DQ56
28	CAS0#	70	DQ25	112	CAS4#	154	DQ57
29	CAS1#	71	DQ26	113	CAS5#	155	DQ58
30	RAS0#	72	DQ27	114	NC/RAS1#**	156	DQ59
31	OE0#	73	VDD	115	RFU	157	VDD
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	NC (A12)	81	NC	123	NC (A13)	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	RFU	167	SA2
42	RFU	84	VDD	126	RFU	168	VDD

**256MB version only

GENERAL DESCRIPTION

The Micron® MT9LD872A X, MT18LD1672A X and MT36LD3272A X are randomly accessed 64MB, 128MB and 256MB memories organized in a x72 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 22/23 address bits, which are entered 12 bits (A0-A11) at RAS# time and 11/12 bits (A0-A11) at CAS# time.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data-outputs will drive read data from the accessed location.

EDO PAGE MODE

EDO PAGE MODE is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also tristate the outputs. Independent of OE# control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last. (Refer to the 16 Meg x 4 [MT4LC16M4H9 DRAM data sheet for additional information on EDO functionality.)

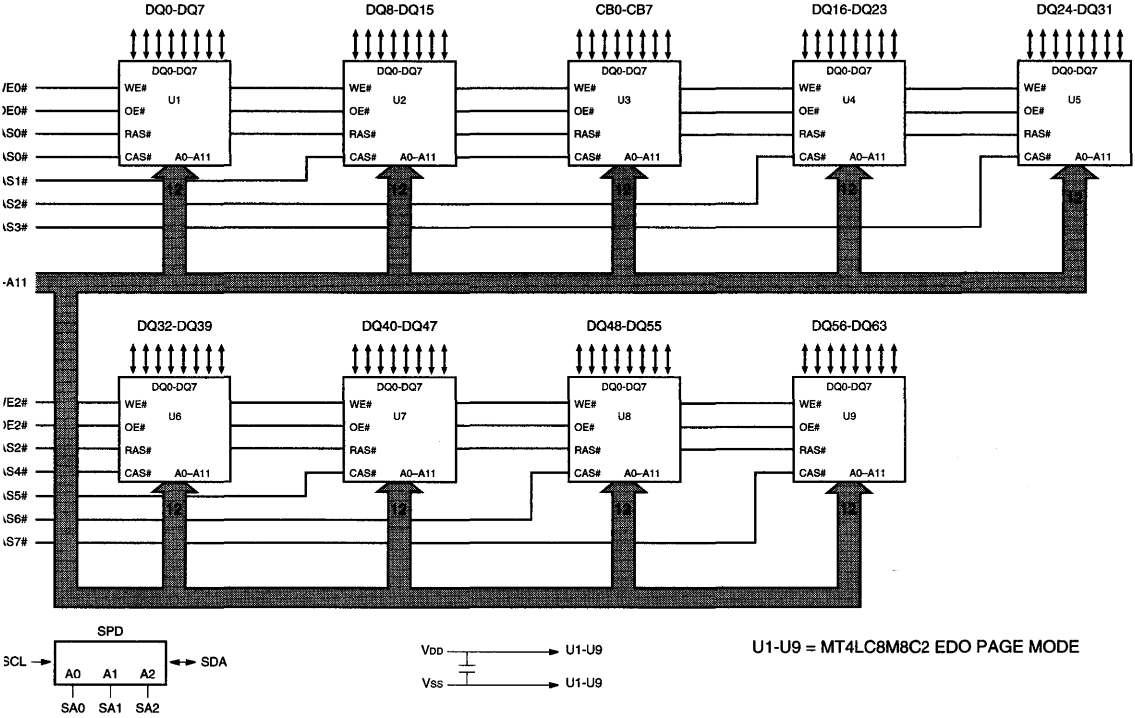
REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses (A0-A10/A11) are executed at least every ^{t}REF regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

SERIAL PRESENCE-DETECT OPERATION

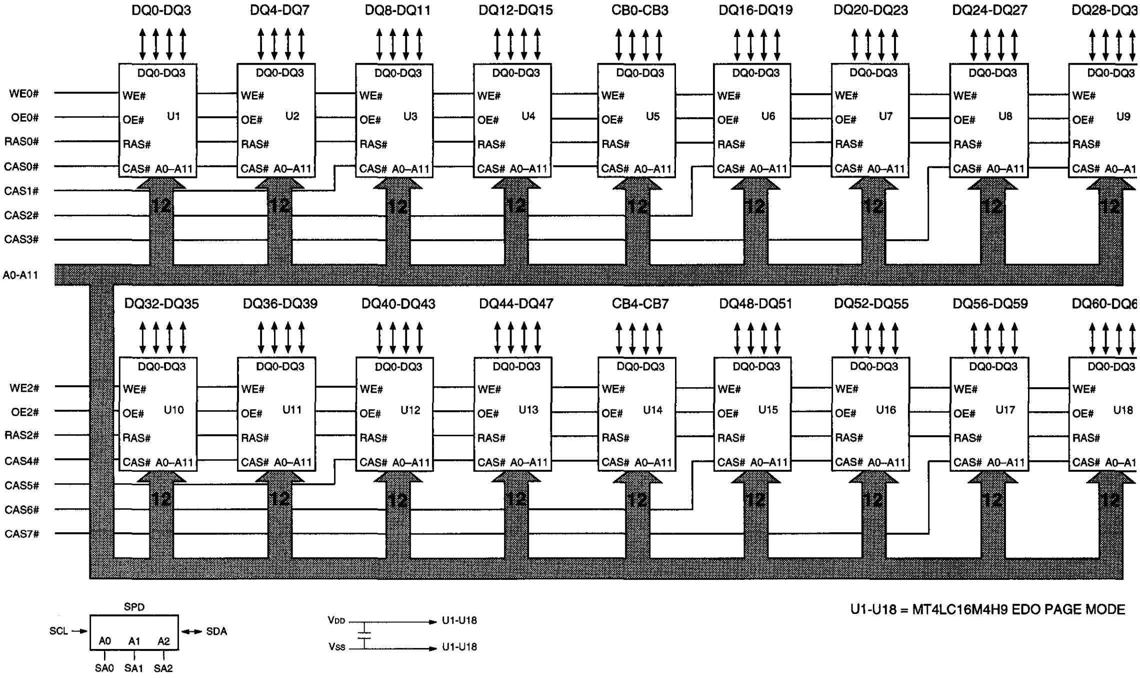
This module family incorporates serial presence-detec (SPD). The SPD function is implemented using a 2,048-bi EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals together with SA(2:0), which provide 8 unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
MT9LD872A X (64MB)



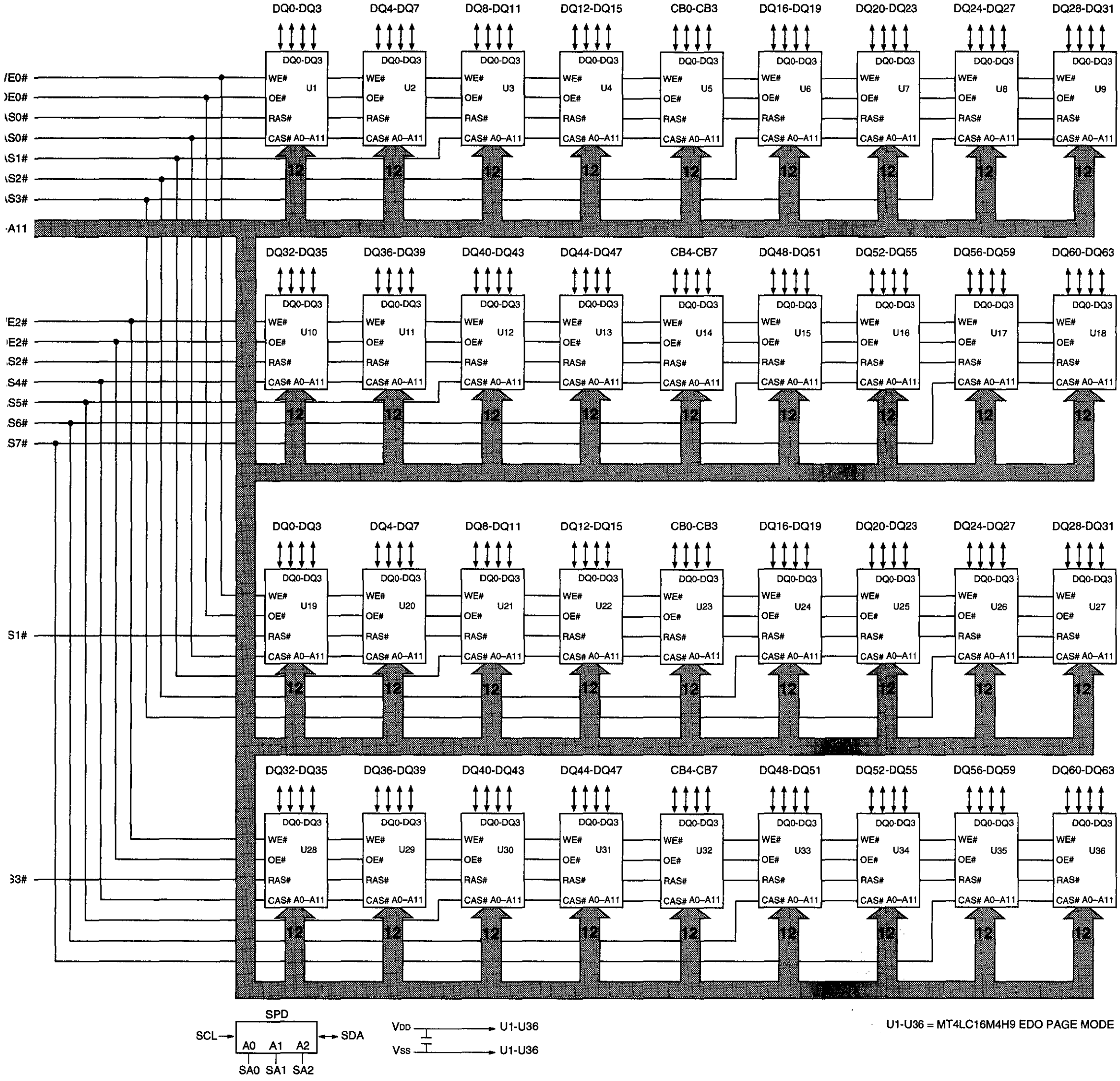
U1-U9 = MT4LC8M8C2 EDO PAGE MODE

FUNCTIONAL BLOCK DIAGRAM
MT18LD1672A X (128MB)



U1-U18 = MT4LC16M4H9 EDO PAGE MODE

FUNCTIONAL BLOCK DIAGRAM
MT36LD3272A X (256MB)



U1-U36 = MT4LC16M4H9 EDO PAGE MODE

ZBT SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Supply Voltage	I/O Voltage	Control Functions	Part Number	Cycle Time (ns)	No. of Pins/ Package	Page
128K x 18	3.3V	3.3V	Flow-Through ZBT	MT55L128L18F	10, 11, 12	100/TQFP	2-1
128K x 18	3.3V	3.3V	Pipelined ZBT	MT55L128L18P	7, 7.5, 8.5, 10	100/TQFP	2-7
256K x 18	3.3V	3.3V	Flow-Through ZBT	MT55L256L18F	10, 11, 12	100/TQFP	2-13
256K x 18	3.3V	3.3V	Pipelined ZBT	MT55L256L18P	6, 7.5, 10	100/TQFP	2-19
256K x 18	3.3V	3.3V/2.5V	SMART ZBT (Pipelined)	MT56L256_18P*	ADVANCE	ADVANCE	2-37
512K x 18	3.3V	3.3V/2.5V	Flow-Through ZBT	MT55L512_18F	10, 11, 12	100/TQFP	2-25
512K x 18	3.3V	3.3V/2.5V	Pipelined ZBT	MT55L512_18P	6, 7.5, 10	100/TQFP	2-31
512K x 18	3.3V	3.3V/2.5V	SMART ZBT (Pipelined)	MT56L512_18P	ADVANCE	ADVANCE	2-37
64K x 32	3.3V	3.3V	Flow-Through ZBT	MT55L64L32F	10, 11, 12	100/TQFP	2-1
64K x 32	3.3V	3.3V	Pipelined ZBT	MT55L64L32P	7, 7.5, 8.5, 10	100/TQFP	2-7
128K x 32	3.3V	3.3V	Flow-Through ZBT	MT55L128L32F	10, 11, 12	100/TQFP	2-13
128K x 32	3.3V	3.3V	Pipelined ZBT	MT55L128L32P	6, 7.5, 10	100/TQFP	2-19
128K x 32	3.3V	3.3V/2.5V	SMART ZBT (Pipelined)	MT56L128_32P	ADVANCE	ADVANCE	2-37
256K x 32	3.3V	3.3V/2.5V	Flow-Through ZBT	MT55L256_32F	10, 11, 12	100/TQFP	2-25
256K x 32	3.3V	3.3V/2.5V	Pipelined ZBT	MT55L256_32P	6, 7.5, 10	100/TQFP	2-31
256K x 32	3.3V	3.3V/2.5V	SMART ZBT (Pipelined)	MT56L256_32P	ADVANCE	ADVANCE	2-37
64K x 36	3.3V	3.3V	Flow-Through ZBT	MT55L64L36F	10, 11, 12	100/TQFP	2-1
64K x 36	3.3V	3.3V	Pipelined ZBT	MT55L64L36P	7, 7.5, 8.5, 10	100/TQFP	2-7
128K x 36	3.3V	3.3V	Flow-Through ZBT	MT55L128L36F	10, 11, 12	100/TQFP	2-13
128K x 36	3.3V	3.3V	Pipelined ZBT	MT55L128L36P	6, 7.5, 10	100/TQFP	2-19
128K x 36	3.3V	3.3V/2.5V	SMART ZBT (Pipelined)	MT56L128_36P	ADVANCE	ADVANCE	2-37
256K x 36	3.3V	3.3V/2.5V	Flow-Through ZBT	MT55L256_36F	10, 11, 12	100/TQFP	2-25
256K x 36	3.3V	3.3V/2.5V	Pipelined ZBT	MT55L256_36P	6, 7.5, 10	100/TQFP	2-31
256K x 36	3.3V	3.3V/2.5V	SMART ZBT (Pipelined)	MT56L256_36P	ADVANCE	ADVANCE	2-37

*The placeholder in the part number is replaced with an “L” for 3.3V I/O parts and a “V” for 2.5V I/O parts.

ADVANCE

MICRON TECHNOLOGY, INC.

2Mb: 128K x 18, 64K x 32/36
3.3V I/O, FLOW-THROUGH ZBT SRAM

2Mb ZBT™ SRAM

MT55L128L18F, MT55L64L32F, MT55L64L36F

3.3V VDD, 3.3V I/O

FEATURES

- High frequency and 100 percent bus utilization
- Fast cycle times: 10ns, 11ns and 12ns
- Single +3.3V ±5% power supply
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs eliminate the need to control OE#
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or Interleaved Burst Modes
- Burst feature (optional)
- Pin/function compatibility with 4Mb, 8Mb and 16Mb ZBT SRAM family
- Automatic power-down

OPTIONS	MARKING
Timing (Access/Cycle/MHz)	
7.5ns/10ns/100 MHz	-10
8.5ns/11ns/90 MHz	-11
9ns/12ns/83 MHz	-12
Configurations	
128K x 18	MT55L128L18F
64K x 32	MT55L64L32F
64K x 36	MT55L64L36F
Package	
100-pin TQFP	T
Options	
Standard version	None
Low-power version	P

Part Number Example: MT55L128L18FT-10

GENERAL DESCRIPTION

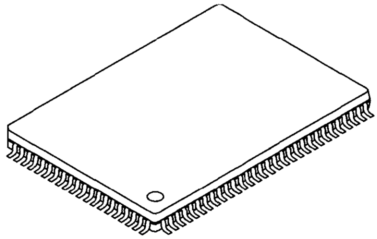
The Micron® Zero Bus Turnaround™ (ZBT™) SRAM family mploys high-speed, low-power CMOS designs using an dvanced CMOS process.

The MT55L128L18F and MT55L64L32/36F SRAMs ntegrate a 128K x 18, 64K x 32, or 64K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles when transitioning from READ to WRITE, or vice versa. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc# and BWd#) and read/write (R/W#).

Asynchronous inputs include the output enable (OE#, which may be tied LOW for control signal minimization), clock (CLK) and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW or left unconnected if burst is unused. The flow-through data-out (Q) is enabled by OE#. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

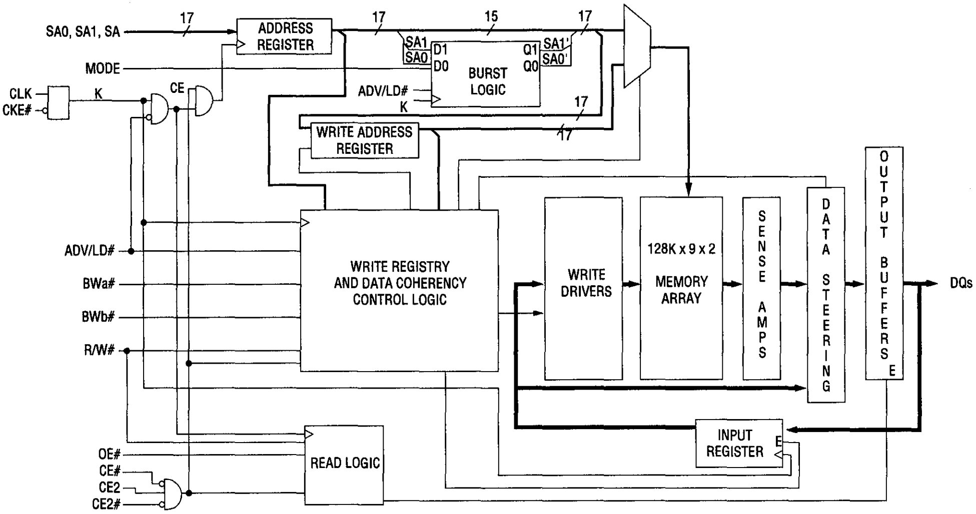
All READ, WRITE and DESELECT cycles are initiated by the ADV/LD# input. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV/LD#). Use of burst mode is optional. It is allowable to give an address for each individual READ and WRITE cycle. BURST cycles wrap around after the fourth access from a base address.

100-Pin TQFP*
(D-1)

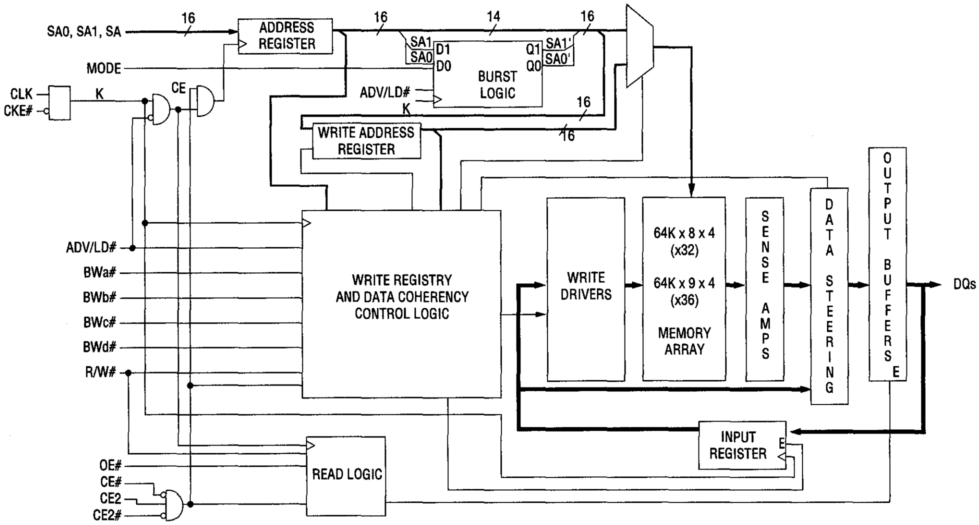


*JEDEC-standard MS-026 BHA (LQFP).

FUNCTIONAL BLOCK DIAGRAM
128K x 18



FUNCTIONAL BLOCK DIAGRAM
64K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

GENERAL DESCRIPTION (continued)

To allow for continuous, 100 percent use of the data bus, the flow-through ZBT SRAM uses a LATE WRITE cycle. For example, if a WRITE cycle begins in clock cycle one, the address is present on rising edge one. BYTE WRITEs need to be asserted on the same cycle as the address. The write data associated with the address is required one cycle later, or on the rising edge of clock cycle two.

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During a BYTE WRITE cycle, BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; and BWd# controls DQd pins. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD# is LOW. Parity/ECC bits are only available on the x18 and x36 versions.

Micron's 2Mb ZBT SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are LVTTL-compatible. The device is ideally suited for systems requiring high bandwidth and zero bus turnaround delays.

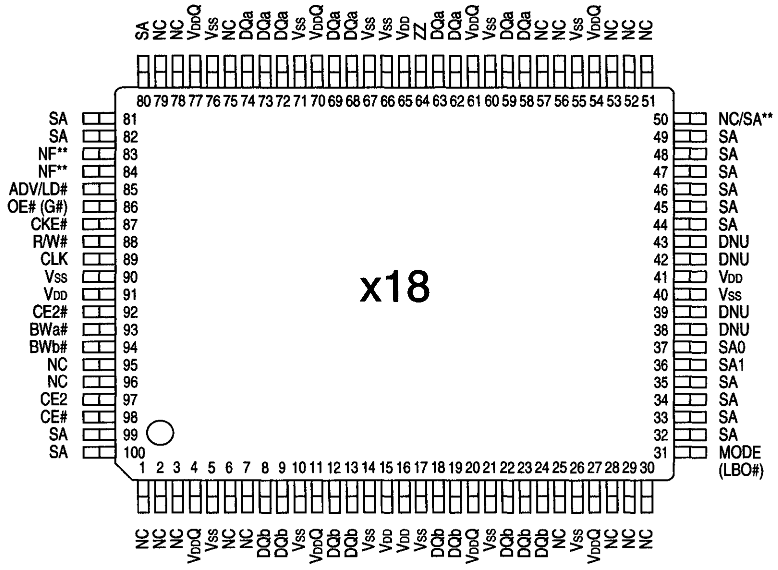
Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

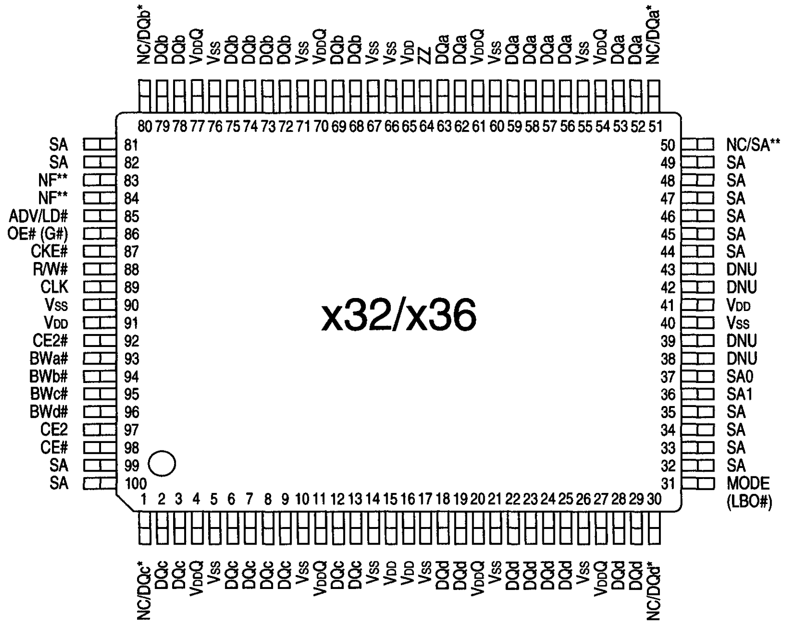
PIN ASSIGNMENT TABLE

PIN #	x18	x32	x36
1	NC	NC	DQc
2	NC	DQc	DQc
3	NC	DQc	DQc
4	VDDQ		
5	VSS		
6	NC	DQc	DQc
7	NC	DQc	DQc
8	DQb	DQc	DQc
9	DQb	DQc	DQc
10	VSS		
11	VDDQ		
12	DQb	DQc	DQc
13	DQb	DQc	DQc
14	VSS		
15	VDD		
16	VDD		
17	VSS		
18	DQb	DQd	DQd
19	DQb	DQd	DQd
20	VDDQ		
21	VSS		
22	DQb	DQd	DQd
23	DQb	DQd	DQd
24	DQb	DQd	DQd
25	NC	DQd	DQd
26	VSS		
27	VDDQ		
28	NC	DQd	DQd
29	NC	DQd	DQd
30	NC	NC	DQd
31	MODE (LBO#)		
32	SA		
33	SA		
34	SA		
35	SA		
36	SA1		
37	SA0		
38	DNU		
39	DNU		
40	VSS		
41	VDD		
42	DNU		
43	DNU		
44	SA		
45	SA		
46	SA		
47	SA		
48	SA		
49	SA		
50	NC/SA*		
51	NC	NC	DQa
52	NC	DQa	DQa
53	NC	DQa	DQa
54	VDDQ		
55	VSS		
56	NC	DQa	DQa
57	NC	DQa	DQa
58	DQa		
59	DQa		
60	VSS		
61	VDDQ		
62	DQa		
63	DQa		
64	ZZ		
65	VDD		
66	VSS		
67	VSS		
68	DQa	DQb	DQb
69	DQa	DQb	DQb
70	VDDQ		
71	VSS		
72	DQa	DQb	DQb
73	DQa	DQb	DQb
74	DQa	DQb	DQb
75	NC	DQb	DQb
76	VSS		
77	VDDQ		
78	NC	DQb	DQb
79	NC	DQb	DQb
80	SA	NC	DQb
81	SA		
82	SA		
83	NF*		
84	NF*		
85	ADV/LD#		
86	OE# (G#)		
87	CKE#		
88	R/W#		
89	CLK		
90	VSS		
91	VDD		
92	CE2#		
93	BWa#		
94	BWb#		
95	NC	BWc#	BWc#
96	NC	BWd#	BWd#
97	CE2		
98	CE#		
99	SA		
100	SA		

* Pins 50, 83 and 84 are reserved for address expansion.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





* NC for x32 version, DQx for x36 version.

** Pins 50, 83 and 84 are reserved for address expansion.

PIN DESCRIPTIONS

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 44-49, 80-82, 99, 100	37 36 32-35, 44-49, 81, 82, 99, 100	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Pins 50, 83 and 84 are reserved as address bits for the higher-density 4Mb, 8Mb and 16Mb ZBT SRAMs, respectively. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
93 94 – –	93 94 95 96	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW).
92	92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
86	86	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
85	85	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
87	87	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE# is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.

PIN DESCRIPTIONS (continued)

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
88	88	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
38, 39, 42, 43	38, 39, 42, 43	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to minimize thermal impedance.
(a) 58, 59, 62, 63, 68, 69, 72-74 (b) 8, 9, 12, 13, 18, 19, 22-24	(a) 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
N/A	51 80 1 30	NC/DQa NC/DQb NC/DQc NC/DQd	NC/ I/O	No Connect/Data Bits: On the x32 version, these pins are no connect (NC) and can be left floating or connected to GND to minimize thermal impedance. On the x36 version, these bits are DQs.
31	31	MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
1-3, 6, 7, 25, 28-30, 51-53, 56, 57, 75, 78, 79, 95, 96	N/A	NC	NC	No Connect: These pins can be left floating or connected to GND to minimize thermal impedance.
50	50	NC/SA	NC	No Connect: NC pin 50 is reserved as an address bit for the higher-density 4Mb ZBT SRAM. This pin can be left floating or connected to GND to minimize thermal impedance.
83, 84	83, 84	NF	–	No Function: These pins are internally connected to the die and will have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals. Pins 83 and 84 are reserved as address bits for the 8Mb and 16Mb ZBT SRAMs.
15, 16, 41, 65, 91	15, 16, 41, 65, 91	VDD	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	VDDQ	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90	5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90	Vss	Supply	Ground: GND.

2Mb
ZBT™ SRAM

MT55L128L18P, MT55L64L32P, MT55L64L36P

3.3V VDD, 3.3V I/O

FEATURES

- High frequency and 100 percent bus utilization
- Fast cycle times: 7ns, 7.5ns, 8.5ns and 10ns
- Single +3.3V ±5% power supply
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs eliminate the need to control OE#
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or Interleaved Burst Modes
- Burst feature (optional)
- Pin/function compatibility with 4Mb, 8Mb and 16Mb ZBT SRAM family
- Automatic power-down

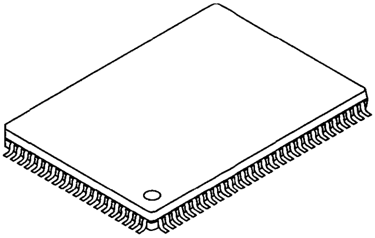
OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
4ns/7ns/143 MHz	-7
4.2ns/7.5ns/133 MHz	-7.5
4.5ns/8.5ns/117 MHz	-8.5
5ns/10ns/100 MHz	-10
• Configurations	
128K x 18	MT55L128L18P
64K x 32	MT55L64L32P
64K x 36	MT55L64L36P
• Package	
100-pin TQFP	T
• Options	
Standard version	None
Low-power version	P

- Part Number Example: MT55L128L18PT-7.5

GENERAL DESCRIPTION

The Micron® Zero Bus Turnaround™ (ZBT™) SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

100-Pin TQFP*
(D-1)



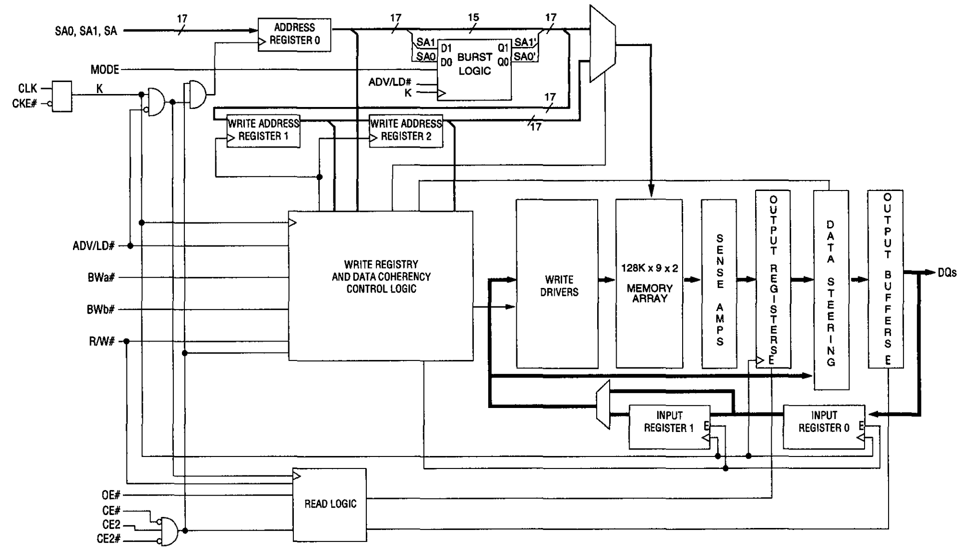
*JEDEC-standard MS-026 BHA (LQFP).

The MT55L128L18P and MT55L64L32/36P SRAMs integrate a 128K x 18, 64K x 32, or 64K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles when transitioning from READ to WRITE, or vice versa. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc# and BWd#) and read/write (R/W#).

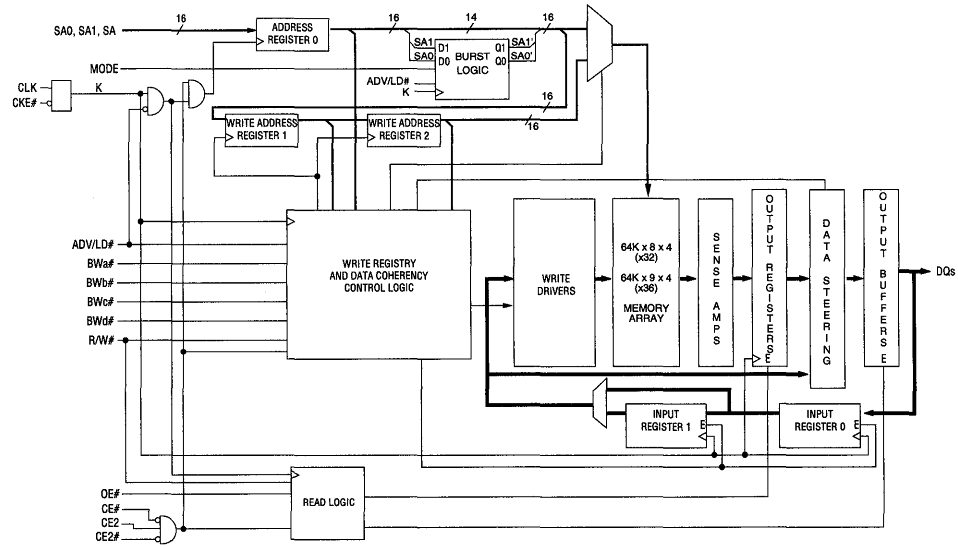
Asynchronous inputs include the output enable (OE#, which may be tied LOW for control signal minimization), clock (CLK) and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW or left unconnected if burst is unused. The data-out (Q), enabled by OE#, is registered by the rising edge of CLK. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

All READ, WRITE and DESELECT cycles are initiated by the ADV/LD# input. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV/LD#). Use of burst mode is optional. It is allowable

FUNCTIONAL BLOCK DIAGRAM
128K x 18



FUNCTIONAL BLOCK DIAGRAM
64K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

GENERAL DESCRIPTION (continued)

to give an address for each individual READ and WRITE cycle. BURST cycles wrap around after the fourth access from a base address.

To allow for continuous, 100 percent use of the data bus, the pipelined ZBT SRAM uses a LATE LATE WRITE cycle. For example, if a WRITE cycle begins in clock cycle one, the address is present on rising edge one. BYTE WRITEs need to be asserted on the same cycle as the address. The data associated with the address is required two cycles later, or on the rising edge of clock cycle three.

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During a BYTE WRITE cycle, BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; and BWd# controls DQd pins. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD# is LOW. Parity/ECC bits are only available on the x18 and x36 versions.

Micron's 2Mb ZBT SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are LVTTL-compatible. The device is ideally suited for systems requiring high bandwidth and zero bus turnaround delays.

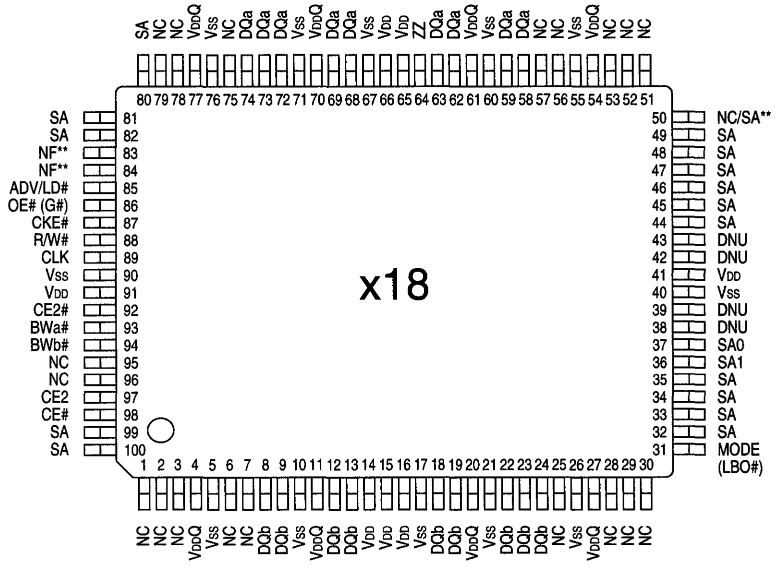
Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

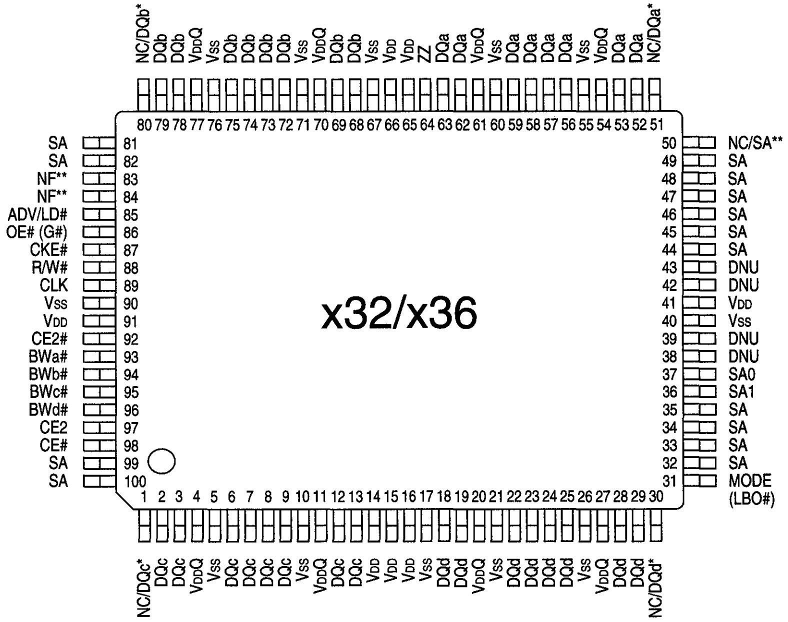
PIN ASSIGNMENT TABLE

PIN #	x18	x32	x36
1	NC	NC	DQc
2	NC	DQc	DQc
3	NC	DQc	DQc
4	VDDQ		
5	VSS		
6	NC	DQc	DQc
7	NC	DQc	DQc
8	DQb	DQc	DQc
9	DQb	DQc	DQc
10	VSS		
11	VDDQ		
12	DQb	DQc	DQc
13	DQb	DQc	DQc
14	VDD		
15	VDD		
16	VDD		
17	VSS		
18	DQb	DQd	DQd
19	DQb	DQd	DQd
20	VDDQ		
21	VSS		
22	DQb	DQd	DQd
23	DQb	DQd	DQd
24	DQb	DQd	DQd
25	NC	DQd	DQd
26	VSS		
27	VDDQ		
28	NC	DQd	DQd
29	NC	DQd	DQd
30	NC	NC	DQd
31	MODE (LBO#)		
32	SA		
33	SA		
34	SA		
35	SA		
36	SA1		
37	SA0		
38	DNU		
39	DNU		
40	VSS		
41	VDD		
42	DNU		
43	DNU		
44	SA		
45	SA		
46	SA		
47	SA		
48	SA		
49	SA		
50	NC/SA*		
51	NC	NC	DQa
52	NC	DQa	DQa
53	NC	DQa	DQa
54	VDDQ		
55	VSS		
56	NC	DQa	DQa
57	NC	DQa	DQa
58	DQa		
59	DQa		
60	VSS		
61	VDDQ		
62	DQa		
63	DQa		
64	ZZ		
65	VDD		
66	VDD		
67	VSS		
68	DQa	DQb	DQb
69	DQa	DQb	DQb
70	VDDQ		
71	VSS		
72	DQa	DQb	DQb
73	DQa	DQb	DQb
74	DQa	DQb	DQb
75	NC	DQb	DQb
76	VSS		
77	VDDQ		
78	NC	DQb	DQb
79	NC	DQb	DQb
80	SA	NC	DQb
81	SA		
82	SA		
83	NF*		
84	NF*		
85	ADV/LD#		
86	OE# (G#)		
87	CKE#		
88	R/W#		
89	CLK		
90	VSS		
91	VDD		
92	CE2#		
93	BWa#		
94	BWb#		
95	NC	BWc#	BWc#
96	NC	BWd#	BWd#
97	CE2		
98	CE#		
99	SA		
100	SA		

* Pins 50, 83 and 84 are reserved for address expansion.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





* NC for x32 version, DQx for x36 version.

** Pins 50, 83 and 84 are reserved for address expansion.

PIN DESCRIPTIONS

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 44-49, 80-82, 99, 100	37 36 32-35, 44-49, 81, 82, 99, 100	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Pins 50, 83 and 84 are reserved as address bits for the higher-density 4Mb, 8Mb and 16Mb ZBT SRAMs, respectively. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
93 94 – –	93 94 95 96	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BWs are associated with addresses and apply to subsequent data. BYTE WRITEs need to be asserted on the same cycle as the address. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW).
92	92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
86	86	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
85	85	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
87	87	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE# is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.

PIN DESCRIPTIONS (continued)

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
88	88	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
38, 39, 42, 43	38, 39, 42, 43	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to minimize thermal impedance.
(a) 58, 59, 62, 63, 68, 69, 72-74 (b) 8, 9, 12, 13, 18, 19, 22-24	(a) 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
N/A	51 80 1 30	NC/DQa NC/DQb NC/DQc NC/DQd	NC/ I/O	No Connect/Data Bits: On the x32 version, these pins are no connect (NC) and can be left floating or connected to GND to minimize thermal impedance. On the x36 version, these bits are DQs.
1-3, 6, 7, 25, 28-30, 51-53, 56, 57, 75, 78, 79, 95, 96	N/A	NC	NC	No Connect: These pins can be left floating or connected to GND to minimize thermal impedance.
31	31	MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
50	50	NC/SA	NC	No Connect: NC pin 50 is reserved as an address bit for the higher-density 4Mb ZBT SRAM. This pin can be left floating or connected to GND to minimize thermal impedance.
83, 84	83, 84	NF	–	No Function: These pins are internally connected to the die and will have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals. Pins 83 and 84 are reserved as address bits for the 8Mb and 16Mb ZBT SRAMs.
14-16, 41, 65, 66, 91	14-16, 41, 65, 66, 91	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground: GND.

ADVANCE

MICRON TECHNOLOGY, INC.

4Mb: 256K x 18, 128K x 32/36
3.3V I/O, FLOW-THROUGH ZBT SRAM

4Mb
ZBT™ SRAM

MT55L256L18F, MT55L128L32F, MT55L128L36F

3.3V VDD, 3.3V I/O

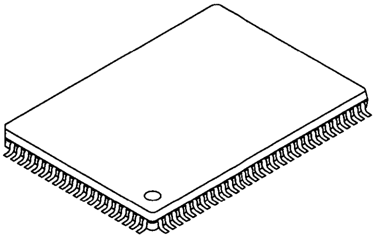
EATURES

- High frequency and 100 percent bus utilization
- Fast cycle times: 10ns, 11ns and 12ns
- Single +3.3V ±5% power supply
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs eliminate the need to control OE#
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or Interleaved Burst Modes
- Burst feature (optional)
- Pin/function compatibility with 2Mb, 8Mb and 16Mb ZBT SRAM family
- Automatic power-down

PTIONS	MARKING
Timing (Access/Cycle/MHz)	
7.5ns/10ns/100 MHz	-10
8.5ns/11ns/90 MHz	-11
9ns/12ns/83 MHz	-12
Configurations	
256K x 18	MT55L256L18F
128K x 32	MT55L128L32F
128K x 36	MT55L128L36F
Package	
100-pin TQFP	T
Options	
Standard version	None
Low-power version	P

Part Number Example: MT55L256L18FT-11

100-Pin TQFP*
(D-1)



*JEDEC-standard MS-026 BHA (LQFP).

ENERAL DESCRIPTION

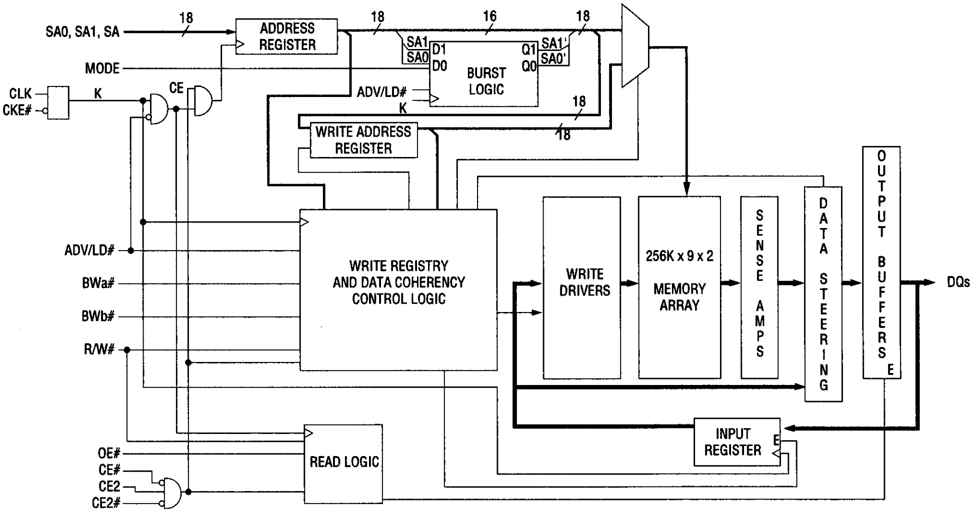
The Micron® Zero Bus Turnaround™ (ZBT™) SRAM family mploys high-speed, low-power CMOS designs using an dvanced CMOS process.

The MT55L256L18F and MT55L128L32/36F SRAMs ntegrate a 256K x 18, 128K x 32, or 128K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles when transitioning from READ to WRITE, or vice versa. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc# and BWd#) and read/write (R/W#).

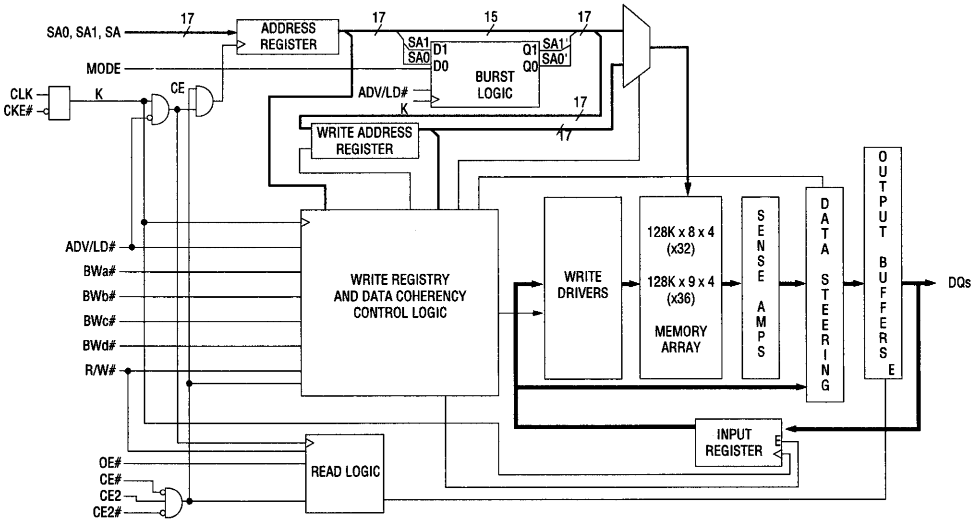
Asynchronous inputs include the output enable (OE#, which may be tied LOW for control signal minimization), clock (CLK) and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW or left unconnected if burst is unused. The flow-through data-out (Q) is enabled by OE#. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

All READ, WRITE and DESELECT cycles are initiated by the ADV/LD# input. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV/LD#). Use of burst mode is optional. It is allowable to give an address for each individual READ and WRITE cycle. BURST cycles wrap around after the fourth access from a base address.

FUNCTIONAL BLOCK DIAGRAM
256K x 18



FUNCTIONAL BLOCK DIAGRAM
128K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

ENERAL DESCRIPTION (continued)

To allow for continuous, 100 percent use of the data bus, e flow-through ZBT SRAM uses a LATE WRITE cycle. For xample, if a WRITE cycle begins in clock cycle one, the ddress is present on rising edge one. BYTE WRITEs need be asserted on the same cycle as the address. The write ata associated with the address is required one cycle later, r on the rising edge of clock cycle two.

Address and write control are registered on-chip to simlify WRITE cycles. This allows self-timed WRITE cycles. dividual byte enables allow individual bytes to be writn. During a BYTE WRITE cycle, BWa# controls DQa pins; Wb# controls DQb pins; BWc# controls DQc pins; and BWd# controls DQd pins. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD# is LOW. Parity/ECC bits are only available on the x18 and x36 versions.

Micron's 4Mb ZBT SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are LVTTL-compatible. The device is ideally suited for systems requiring high bandwidth and zero bus turnaround delays.

Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

IN ASSIGNMENT TABLE

IN #	x18	x32	x36
1	NC	NC	DQc
2	NC	DQc	DQc
3	NC	DQc	DQc
4	VDDQ		
5	VSS		
6	NC	DQc	DQc
7	NC	DQc	DQc
8	DQb	DQc	DQc
9	DQb	DQc	DQc
10	VSS		
11	VDDQ		
12	DQb	DQc	DQc
13	DQb	DQc	DQc
14	VSS		
15	VDD		
16	VDD		
17	VSS		
18	DQb	DQd	DQd
19	DQb	DQd	DQd
20	VDDQ		
21	VSS		
22	DQb	DQd	DQd
23	DQb	DQd	DQd
24	DQb	DQd	DQd
25	NC	DQd	DQd

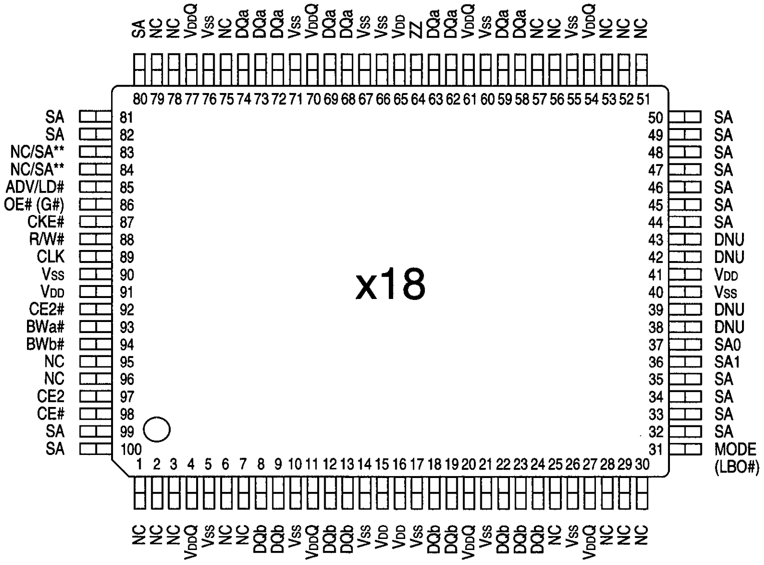
PIN #	x18	x32	x36
26	VSS		
27	VDDQ		
28	NC	DQd	DQd
29	NC	DQd	DQd
30	NC	NC	DQd
31	MODE (LBO#)		
32	SA		
33	SA		
34	SA		
35	SA		
36	SA1		
37	SA0		
38	DNU		
39	DNU		
40	VSS		
41	VDD		
42	DNU		
43	DNU		
44	SA		
45	SA		
46	SA		
47	SA		
48	SA		
49	SA		
50	SA		

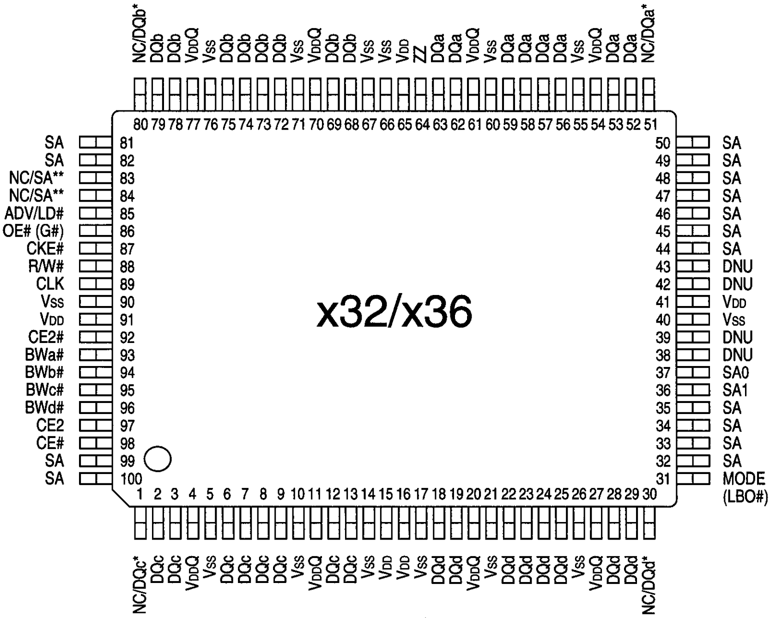
PIN #	x18	x32	x36
51	NC	NC	DQa
52	NC	DQa	DQa
53	NC	DQa	DQa
54	VDDQ		
55	VSS		
56	NC	DQa	DQa
57	NC	DQa	DQa
58	DQa		
59	DQa		
60	VSS		
61	VDDQ		
62	DQa		
63	DQa		
64	ZZ		
65	VDD		
66	VSS		
67	VSS		
68	DQa	DQb	DQb
69	DQa	DQb	DQb
70	VDDQ		
71	VSS		
72	DQa	DQb	DQb
73	DQa	DQb	DQb
74	DQa	DQb	DQb
75	NC	DQb	DQb

PIN #	x18	x32	x36
76	VSS		
77	VDDQ		
78	NC	DQb	DQb
79	NC	DQb	DQb
80	SA	NC	DQb
81	SA		
82	SA		
83	NC/SA*		
84	NC/SA*		
85	ADV/LD#		
86	OE# (G#)		
87	CKE#		
88	R/W#		
89	CLK		
90	VSS		
91	VDD		
92	CE2#		
93	BWa#		
94	BWb#		
95	NC	BWc#	BWc#
96	NC	BWd#	BWd#
97	CE2		
98	CE#		
99	SA		
100	SA		

Pins 83 and 84 are reserved for address expansion.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





* NC for x32 version, DQx for x36 version.
** Pins 83 and 84 are reserved for address expansion.

IN DESCRIPTIONS

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 44-50, 80-82, 99, 100	37 36 32-35, 44-50, 81, 82, 99, 100	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Pins 83 and 84 are reserved as address bits for the higher-density 8Mb and 16Mb ZBT SRAMs, respectively. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
93 94 – –	93 94 95 96	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW).
92	92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
86	86	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
85	85	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
87	87	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.

PIN DESCRIPTIONS (continued)

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
88	88	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
38, 39, 42, 43	38, 39, 42, 43	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to minimize thermal impedance.
(a) 58, 59, 62, 63, 68, 69, 72-74 (b) 8, 9, 12, 13, 18, 19, 22-24	(a) 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge CLK.
N/A	51 80 1 30	NC/DQa NC/DQb NC/DQc NC/DQd	NC/ I/O	No Connect/Data Bits: On the x32 version, these pins are no connect (NC) and can be left floating or connected to GND to minimize thermal impedance. On the x36 version, these bits are DQs.
31	31	MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
1-3, 6, 7, 25, 28-30, 51-53, 56, 57, 75, 78, 79, 95, 96	N/A	NC	NC	No Connect: These pins can be left floating or connected to GND to minimize thermal impedance.
83, 84	83, 84	NC/SA	NC	No Connect: NC pins 83 and 84 are reserved as address bits for the 8Mb and 16Mb ZBT SRAMs, respectively. These pins can be left floating or connected to GND to minimize thermal impedance.
15, 16, 41, 65, 91	15, 16, 41, 65, 91	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90	5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90	V_{SS}	Supply	Ground: GND.

4Mb ZBT™ SRAM

MT55L256L18P, MT55L128L32P, MT55L128L36P

3.3V VDD, 3.3V I/O

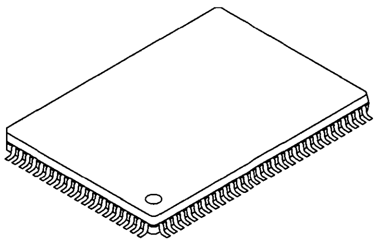
FEATURES

- High frequency and 100 percent bus utilization
- Fast cycle times: 6ns, 7.5ns and 10ns
- Single +3.3V ±5% power supply
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs eliminate the need to control OE#
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or Interleaved Burst Modes
- Burst feature (optional)
- Pin/function compatibility with 2Mb, 8Mb and 16Mb ZBT SRAM family
- Automatic power-down

OPTIONS	MARKING
Timing (Access/Cycle/MHz)	
4ns/6ns/166 MHz	-6
4.2ns/7.5ns/133 MHz	-7.5
5ns/10ns/100 MHz	-10
Configurations	
256K x 18	MT55L256L18P
128K x 32	MT55L128L32P
128K x 36	MT55L128L36P
Package	
100-pin TQFP	T
Options	
Standard version	None
Low-power version	P

Part Number Example: MT55L256L18PT-7.5

100-Pin TQFP*
(D-1)



*JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

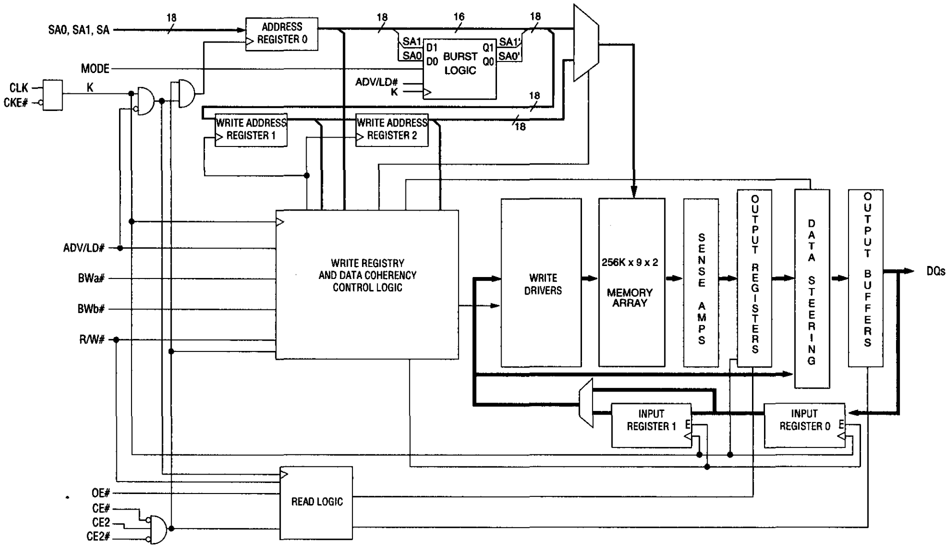
The Micron® Zero Bus Turnaround™ (ZBT™) SRAM family mploys high-speed, low-power CMOS designs using an dvanced CMOS process.

The MT55L256L18P and MT55L128L32/36P SRAMs integrate a 256K x 18, 128K x 32, or 128K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles when transitioning from READ to WRITE, or vice versa. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc# and BWd#) and read/write (R/W#).

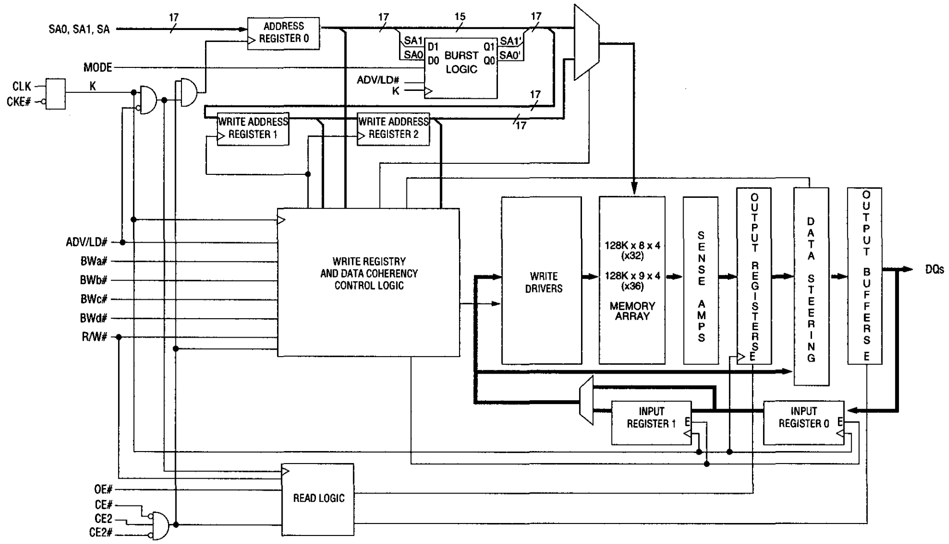
Asynchronous inputs include the output enable (OE#, which may be tied LOW for control signal minimization), clock (CLK) and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW or left unconnected if burst is unused. The data-out (Q), enabled by OE#, is registered by the rising edge of CLK. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

All READ, WRITE and DESELECT cycles are initiated by the ADV/LD# input. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV/LD#). Use of burst mode is optional. It is allowable to give an address for each individual READ and WRITE cycle. BURST cycles wrap around after the fourth access from a base address.

FUNCTIONAL BLOCK DIAGRAM
256K x 18



FUNCTIONAL BLOCK DIAGRAM
128K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

ENERAL DESCRIPTION (continued)

To allow for continuous, 100 percent use of the data bus, he pipelined ZBT SRAM uses a LATE LATE WRITE cycle. or example, if a WRITE cycle begins in clock cycle one, the ddress is present on rising edge one. BYTE WRITEs need o be asserted on the same cycle as the address. The data ssociated with the address is required two cycles later, or n the rising edge of clock cycle three.

Address and write control are registered on-chip to implify WRITE cycles. This allows self-timed WRITE cycles. ndividual byte enables allow individual bytes to be written. uring a BYTE WRITE cycle, BWa# controls DQa pins; Wb# controls DQb pins; BWc# controls DQc pins; and BWd# controls DQd pins. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD# is LOW. Parity/ECC bits are only available on the x18 and x36 versions.

Micron's 4Mb ZBT SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are LVTTL-compatible. The device is ideally suited for systems requiring high bandwidth and zero bus turnaround delays.

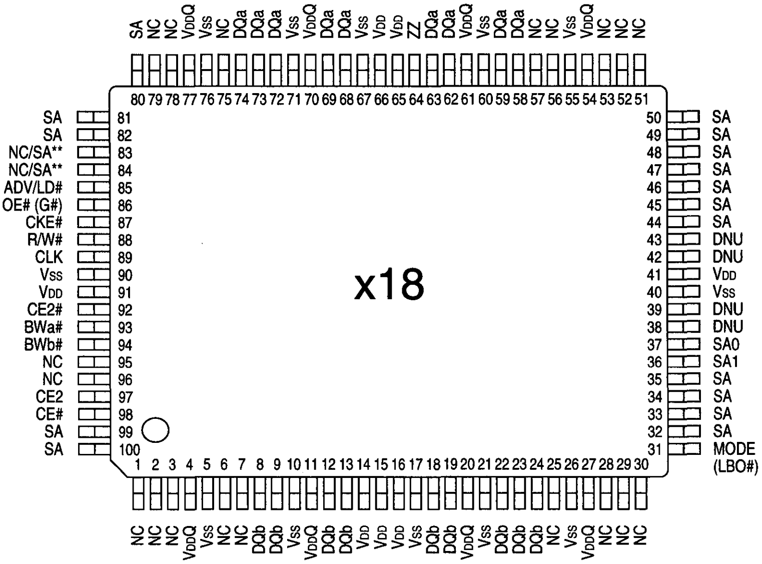
Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

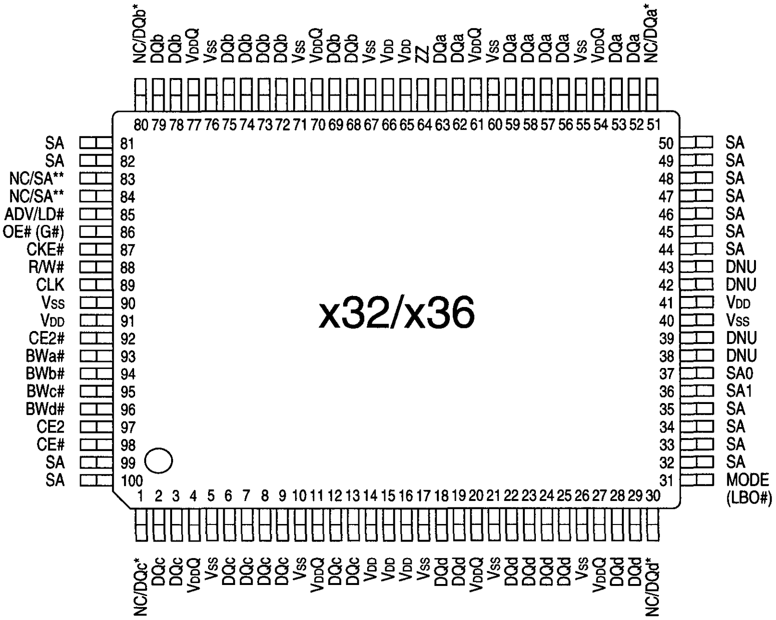
IN ASSIGNMENT TABLE

PIN #	x18	x32	x36
1	NC	NC	DQc
2	NC	DQc	DQc
3	NC	DQc	DQc
4	VDDQ		
5	VSS		
6	NC	DQc	DQc
7	NC	DQc	DQc
8	DQb	DQc	DQc
9	DQb	DQc	DQc
10	VSS		
11	VDDQ		
12	DQb	DQc	DQc
13	DQb	DQc	DQc
14	VDD		
15	VDD		
16	VDD		
17	VSS		
18	DQb	DQd	DQd
19	DQb	DQd	DQd
20	VDDQ		
21	VSS		
22	DQb	DQd	DQd
23	DQb	DQd	DQd
24	DQb	DQd	DQd
25	NC	DQd	DQd
26	VSS		
27	VDDQ		
28	NC	DQd	DQd
29	NC	DQd	DQd
30	NC	NC	DQd
31	MODE (LBO#)		
32	SA		
33	SA		
34	SA		
35	SA		
36	SA1		
37	SA0		
38	DNU		
39	DNU		
40	VSS		
41	VDD		
42	DNU		
43	DNU		
44	SA		
45	SA		
46	SA		
47	SA		
48	SA		
49	SA		
50	SA		
51	NC	NC	DQa
52	NC	DQa	DQa
53	NC	DQa	DQa
54	VDDQ		
55	VSS		
56	NC	DQa	DQa
57	NC	DQa	DQa
58	DQa		
59	DQa		
60	VSS		
61	VDDQ		
62	DQa		
63	DQa		
64	ZZ		
65	VDD		
66	VDD		
67	VSS		
68	DQa	DQb	DQb
69	DQa	DQb	DQb
70	VDDQ		
71	VSS		
72	DQa	DQb	DQb
73	DQa	DQb	DQb
74	DQa	DQb	DQb
75	NC	DQb	DQb
76	VSS		
77	VDDQ		
78	NC	DQb	DQb
79	NC	DQb	DQb
80	SA	NC	DQb
81	SA		
82	SA		
83	NC/SA*		
84	NC/SA*		
85	ADV/LD#		
86	OE# (G#)		
87	CKE#		
88	R/W#		
89	CLK		
90	VSS		
91	VDD		
92	CE2#		
93	BWa#		
94	BWb#		
95	NC	BWc#	BWc#
96	NC	BWd#	BWd#
97	CE2		
98	CE#		
99	SA		
100	SA		

* Pins 83 and 84 are reserved for address expansion.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





* NC for x32 version, DQx for x36 version.

** Pins 83 and 84 are reserved for address expansion.

IN DESCRIPTIONS

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 44-50, 80-82, 99, 100	37 36 32-35, 44-50, 81, 82, 99, 100	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Pins 83 and 84 are reserved as address bits for higher-density 8Mb and 16Mb ZBT SRAMs, respectively. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
93 94 – –	93 94 95 96	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWs are associated with addresses and apply to subsequent data. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW).
92	92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
86	86	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
85	85	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
87	87	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE# is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.

PIN DESCRIPTIONS (continued)

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
88	88	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
38, 39, 42, 43	38, 39, 42, 43	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to minimize thermal impedance.
(a) 58, 59, 62, 63, 68, 69, 72-74 (b) 8, 9, 12, 13, 18, 19, 22-24	(a) 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
N/A	51 80 1 30	NC/DQa NC/DQb NC/DQc NC/DQd	NC/ I/O	No Connect/Data Bits: On the x32 version, these pins are no connect (NC) and can be left floating or connected to GND to minimize thermal impedance. On the x36 version, these bits are DQs.
31	31	MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
1-3, 6, 7, 25, 28-30, 51-53, 56, 57, 75, 78, 79, 95, 96	N/A	NC	NC	No Connect: These pins can be left floating or connected to GND to minimize thermal impedance.
83, 84	83, 84	NC/SA	NC	No Connect: Pins 83 and 84 are reserved as address bits for higher-density 8Mb and 16Mb ZBT SRAMs, respectively. These pins can be left floating or connected to GND to minimize thermal impedance.
14-16, 41, 65, 66, 91	14-16, 41, 65, 66, 91	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground: GND.

8Mb
ZBT™ SRAM

MT55L512L18F, MT55L256L32F,
MT55L256L36F; MT55L512V18F,
MT55L256V32F, MT55L256V36F

3.3V VDD, 3.3V or 2.5V I/O, Selectable Burst Mode

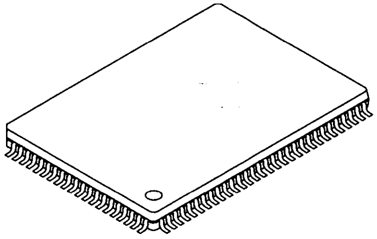
FEATURES

- High frequency and 100 percent bus utilization
- Fast cycle times: 10ns, 11ns and 12ns
- Single +3.3V ±5% power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer supply (VDDQ)
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs eliminate the need to control OE#
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or Interleaved Burst Modes
- Burst feature (optional)
- Pin/function compatibility with 2Mb, 4Mb and 16Mb ZBT SRAM family
- Automatic power-down

OPTIONS	MARKING
Timing (Access/Cycle/MHz)	
7.5ns/10ns/100 MHz	-10
8.5ns/11ns/90 MHz	-11
9ns/12ns/83 MHz	-12
Configurations	
3.3V I/O	
512K x 18	MT55L512L18F
256K x 32	MT55L256L32F
256K x 36	MT55L256L36F
2.5V I/O	
512K x 18	MT55L512V18F
256K x 32	MT55L256V32F
256K x 36	MT55L256V36F
Package	
100-pin TQFP	T
Options	
Standard version	None
Low-power version	P

Part Number Example: MT55L256L32FT-11

100-Pin TQFP*
(D-1)



*JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

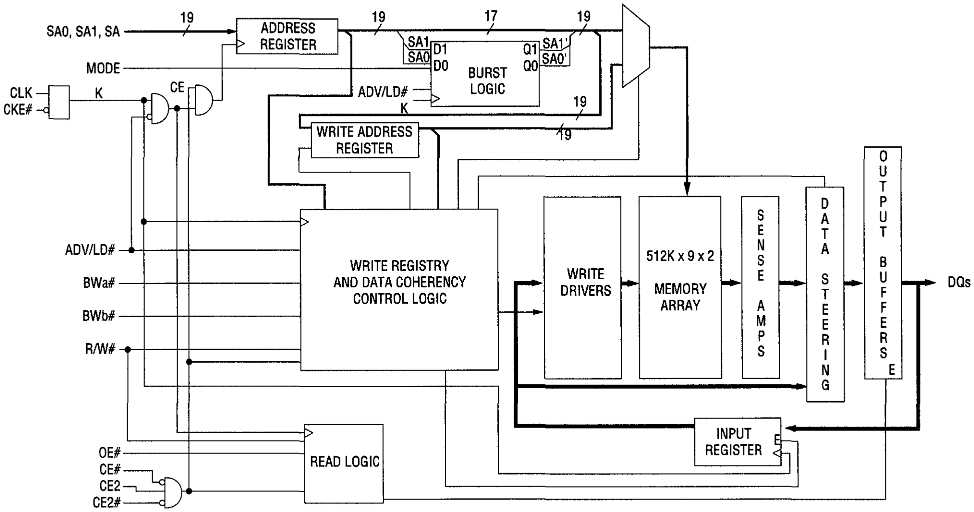
The Micron® Zero Bus Turnaround™ (ZBT™) SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

Micron's 8Mb ZBT SRAMs integrate a 512K x 18, 256K x 32 or 256K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles when transitioning from READ to WRITE, or vice versa. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc# and BWd#) and read/write (R/W#).

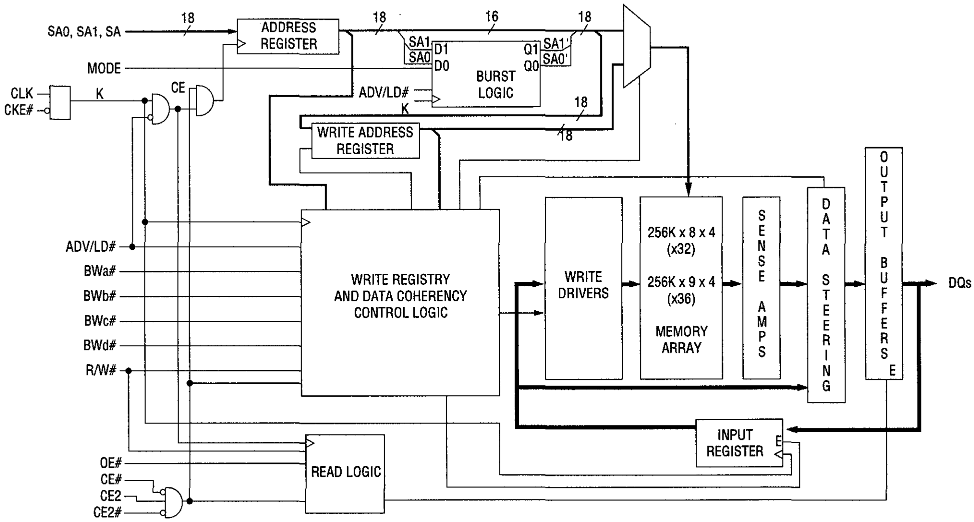
Asynchronous inputs include the output enable (OE#, which may be tied LOW for control signal minimization), clock (CLK) and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW or left unconnected if burst is unused. The flow-through data-out (Q) is enabled by OE#. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

All READ, WRITE and DESELECT cycles are initiated by the ADV/LD# input. Subsequent burst addresses can be

FUNCTIONAL BLOCK DIAGRAM
512K x 18



FUNCTIONAL BLOCK DIAGRAM
256K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

ENERAL DESCRIPTION (continued)

ternally generated as controlled by the burst advance pin ADV/LD#). Use of burst mode is optional. It is allowable give an address for each individual READ and WRITE ycle. BURST cycles wrap around after the fourth access om a base address.

To allow for continuous, 100 percent use of the data bus, e flow-through ZBT SRAM uses a LATE WRITE cycle. For xample, if a WRITE cycle begins in clock cycle one, the ddress is present on rising edge one. BYTE WRITEs need be asserted on the same cycle as the address. The write ata associated with the address is required one cycle later, r on the rising edge of clock cycle two.

Address and write control are registered on-chip to simlify WRITE cycles. This allows self-timed WRITE cycles. ndividual byte enables allow individual bytes to be written. During a BYTE WRITE cycle, BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; and BWd# controls DQd pins. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD# is LOW. Parity/ECC bits are only available on the x18 and x36 versions.

Micron's 8Mb ZBT SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are LVTTL-compatible. Users can choose either a 3.3V or 2.5V I/O version. The device is ideally suited for systems requiring high bandwidth and zero bus turnaround delays.

Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

IN ASSIGNMENT TABLE

IN #	x18	x32	x36
1	NC	NC	DQc
2	NC	DQc	DQc
3	NC	DQc	DQc
4	VDDQ		
5	Vss		
6	NC	DQc	DQc
7	NC	DQc	DQc
8	DQb	DQc	DQc
9	DQb	DQc	DQc
10	Vss		
11	VDDQ		
12	DQb	DQc	DQc
13	DQb	DQc	DQc
14	Vss		
15	VDD		
16	VDD		
17	Vss		
18	DQb	DQd	DQd
19	DQb	DQd	DQd
20	VDDQ		
21	Vss		
22	DQb	DQd	DQd
23	DQb	DQd	DQd
24	DQb	DQd	DQd
25	NC	DQd	DQd

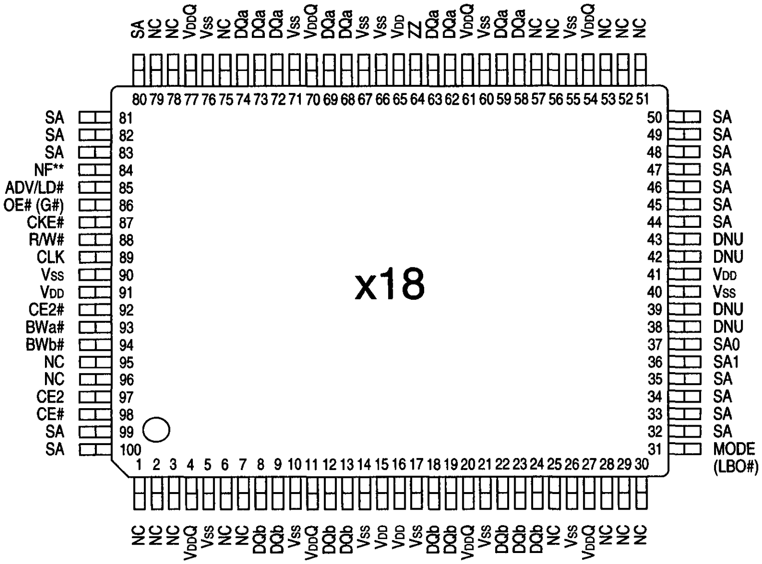
PIN #	x18	x32	x36
26	Vss		
27	VDDQ		
28	NC	DQd	DQd
29	NC	DQd	DQd
30	NC	NC	DQd
31	MODE (LBO#)		
32	SA		
33	SA		
34	SA		
35	SA		
36	SA1		
37	SA0		
38	DNU		
39	DNU		
40	Vss		
41	VDD		
42	DNU		
43	DNU		
44	SA		
45	SA		
46	SA		
47	SA		
48	SA		
49	SA		
50	SA		

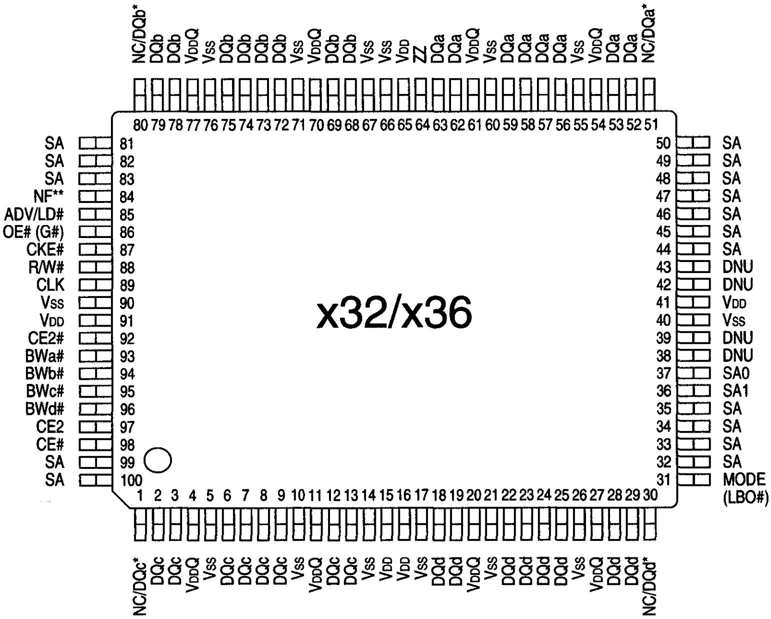
PIN #	x18	x32	x36
51	NC	NC	DQa
52	NC	DQa	DQa
53	NC	DQa	DQa
54	VDDQ		
55	Vss		
56	NC	DQa	DQa
57	NC	DQa	DQa
58	DQa		
59	DQa		
60	Vss		
61	VDDQ		
62	DQa		
63	DQa		
64	ZZ		
65	VDD		
66	Vss		
67	Vss		
68	DQa	DQb	DQb
69	DQa	DQb	DQb
70	VDDQ		
71	Vss		
72	DQa	DQb	DQb
73	DQa	DQb	DQb
74	DQa	DQb	DQb
75	NC	DQb	DQb

PIN #	x18	x32	x36
76	Vss		
77	VDDQ		
78	NC	DQb	DQb
79	NC	DQb	DQb
80	SA	NC	DQb
81	SA		
82	SA		
83	SA		
84	NF*		
85	ADV/LD#		
86	OE# (G#)		
87	CKE#		
88	R/W#		
89	CLK		
90	Vss		
91	VDD		
92	CE2#		
93	BWa#		
94	BWb#		
95	NC	BWc#	BWc#
96	NC	BWd#	BWd#
97	CE2		
98	CE#		
99	SA		
100	SA		

Pin 84 is reserved for address expansion.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





* NC for x32 version, DQx for x36 version.
** Pin 84 is reserved for address expansion.

PIN DESCRIPTIONS

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 44-50, 80-83, 99, 100	37 36 32-35, 44-50, 81-83, 99, 100	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Pin 84 is reserved as an address bit for the higher-density 16Mb ZBT SRAM. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
93 94 – –	93 94 95 96	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW).
92	92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
86	86	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
85	85	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
87	87	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.

PIN DESCRIPTIONS (continued)

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
88	88	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
38, 39, 42, 43	38, 39, 42, 43	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to minimize thermal impedance.
(a) 58, 59, 62, 63, 68, 69, 72-74 (b) 8, 9, 12, 13, 18, 19, 22-24	(a) 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge CLK.
N/A	51 80 1 30	NC/DQa NC/DQb NC/DQc NC/DQd	NC/ I/O	No Connect/Data Bits: On the x32 version, these pins are no connect (NC) and can be left floating or connected to GND to minimize thermal impedance. On the x36 version, these bits are DQs.
31	31	MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
1-3, 6, 7, 25, 28-30, 51-53, 56, 57, 75, 78, 79, 95, 96	N/A	NC	NC	No Connect: These pins can be left floating or connected to GND to minimize thermal impedance.
84	84	NF	–	No Function: This pin is internally connected to the die and will have the capacitance of an input pin. It is allowable to leave this pin unconnected or driven by signals. Pin 84 is reserved as an address pin for the 16Mb ZBT SRAM.
15, 16, 41, 65, 91	15, 16, 41, 65, 91	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90	5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90	V_{SS}	Supply	Ground: GND.

8Mb
ZBT™ SRAM

MT55L512L18P, MT55L256L32P,
MT55L256L36P; MT55L512V18P,
MT55L256V32P, MT55L256V36P

3.3V VDD, 3.3V or 2.5V I/O, Selectable Burst Mode

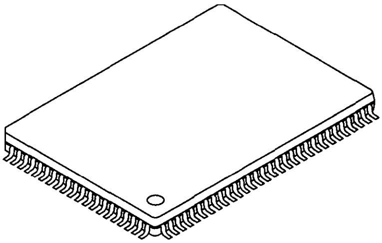
FEATURES

- High frequency and 100 percent bus utilization
- Fast cycle times: 6ns, 7.5ns and 10ns
- Single +3.3V ±5% power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer supply (VDDQ)
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs eliminate the need to control OE#
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or Interleaved Burst Modes
- Burst feature (optional)
- Pin/function compatibility with 2Mb, 4Mb and 16Mb ZBT SRAM family
- Automatic power-down

OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
3.5ns/6ns/166 MHz	-6
4.2ns/7.5ns/133 MHz	-7.5
5ns/10ns/100 MHz	-10
• Configurations	
3.3V I/O	
512K x 18	MT55L512L18P
256K x 32	MT55L256L32P
256K x 36	MT55L256L36P
2.5V I/O	
512K x 18	MT55L512V18P
256K x 32	MT55L256V32P
256K x 36	MT55L256V36P
• Package	
100-pin TQFP	T
• Options	
Standard version	None
Low-power version	P

- Part Number Example: MT55L256L32PT-7.5

100-Pin TQFP*
(D-1)



*JEDEC-standard MS-026 BHA (LQFP).

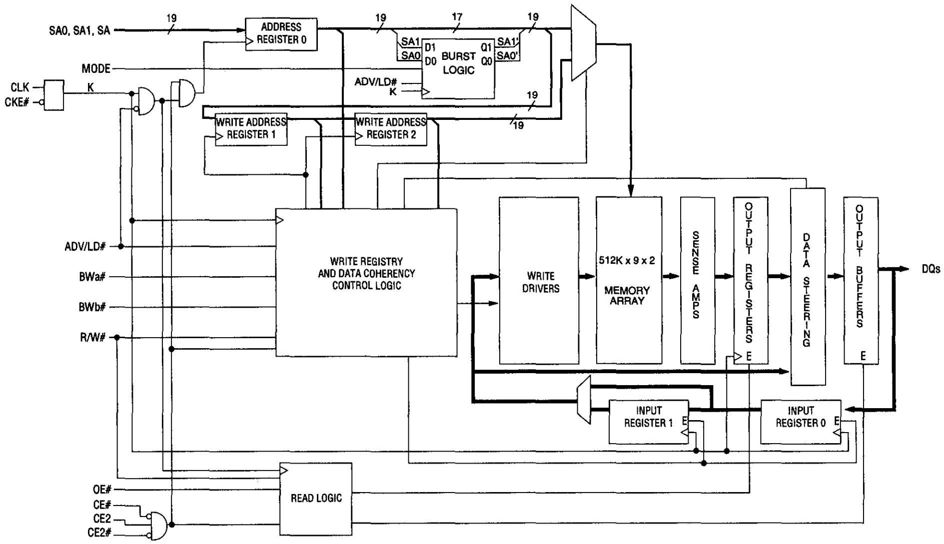
GENERAL DESCRIPTION

The Micron® Zero Bus Turnaround™ (ZBT™) SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

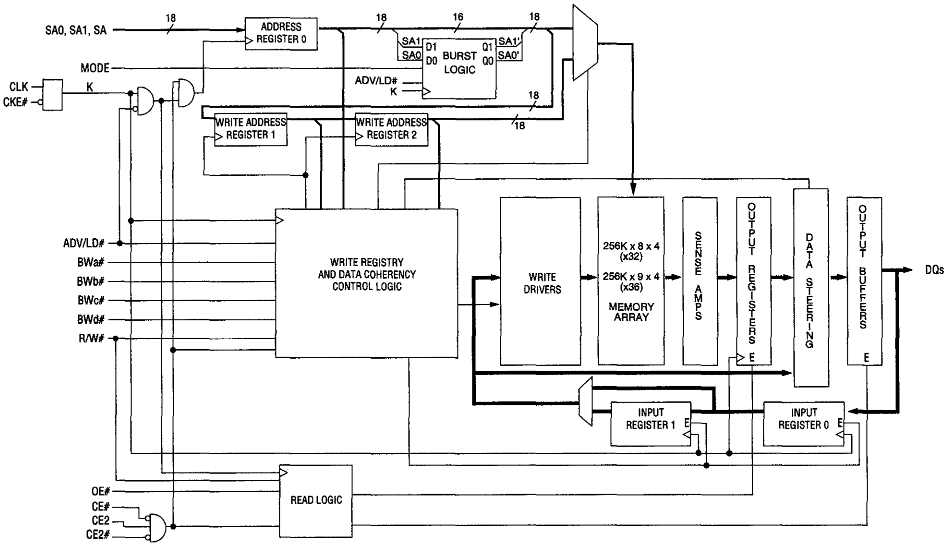
Micron's 8Mb ZBT SRAMs integrate a 512K x 18, 256K x 32 or 256K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles when transitioning from READ to WRITE, or vice versa. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc# and BWd#) and read/write (R/W#).

Asynchronous inputs include the output enable (OE#, which may be tied LOW for control signal minimization), clock (CLK) and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW or left unconnected if burst is unused. The data-out (Q), enabled by OE#, is registered by the rising edge of CLK. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

FUNCTIONAL BLOCK DIAGRAM
512K x 18



FUNCTIONAL BLOCK DIAGRAM
256K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

GENERAL DESCRIPTION (continued)

All READ, WRITE and DESELECT cycles are initiated by the ADV/LD# input. Subsequent burst addresses can be nternally generated as controlled by the burst advance pin (ADV/LD#). Use of burst mode is optional. It is allowable to give an address for each individual READ and WRITE cycle. BURST cycles wrap around after the fourth access from a base address.

To allow for continuous, 100 percent use of the data bus, the pipelined ZBT SRAM uses a LATE LATE WRITE cycle. For example, if a WRITE cycle begins in clock cycle one, the address is present on rising edge one. BYTE WRITEs need o be asserted on the same cycle as the address. The data associated with the address is required two cycles later, or on the rising edge of clock cycle three.

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During a BYTE WRITE cycle, BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; and BWd# controls DQd pins. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD# is LOW. Parity/ECC bits are only available on the x18 and x36 versions.

Micron's 8Mb ZBT SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are LVTTL-compatible. Users can choose either a 2.5V or 3.3V I/O version. The device is ideally suited for systems requiring high bandwidth and zero bus turnaround delays.

Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

PIN ASSIGNMENT TABLE

PIN #	x18	x32	x36
1	NC	NC	DQc
2	NC	DQc	DQc
3	NC	DQc	DQc
4	VDDQ		
5	VSS		
6	NC	DQc	DQc
7	NC	DQc	DQc
8	DQb	DQc	DQc
9	DQb	DQc	DQc
10	VSS		
11	VDDQ		
12	DQb	DQc	DQc
13	DQb	DQc	DQc
14	VDD		
15	VDD		
16	VDD		
17	VSS		
18	DQb	DQd	DQd
19	DQb	DQd	DQd
20	VDDQ		
21	VSS		
22	DQb	DQd	DQd
23	DQb	DQd	DQd
24	DQb	DQd	DQd
25	NC	DQd	DQd

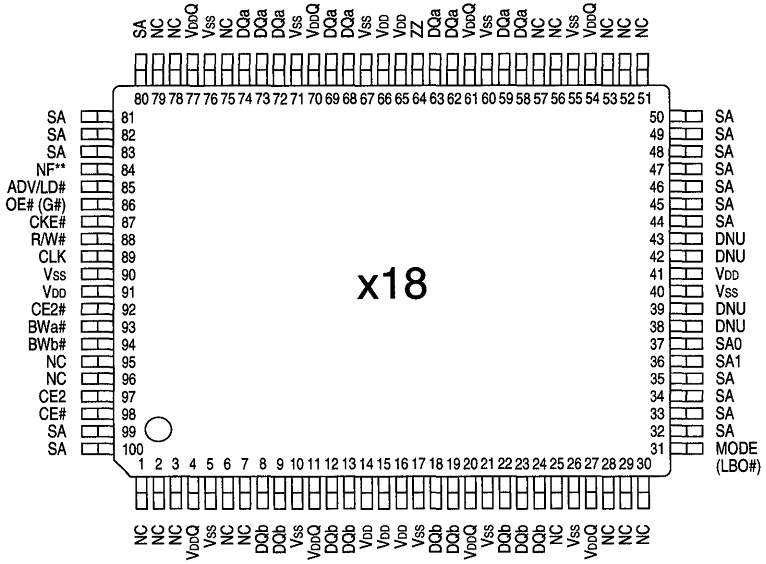
PIN #	x18	x32	x36
26	VSS		
27	VDDQ		
28	NC	DQd	DQd
29	NC	DQd	DQd
30	NC	NC	DQd
31	MODE (LBO#)		
32	SA		
33	SA		
34	SA		
35	SA		
36	SA1		
37	SA0		
38	DNU		
39	DNU		
40	VSS		
41	VDD		
42	DNU		
43	DNU		
44	SA		
45	SA		
46	SA		
47	SA		
48	SA		
49	SA		
50	SA		

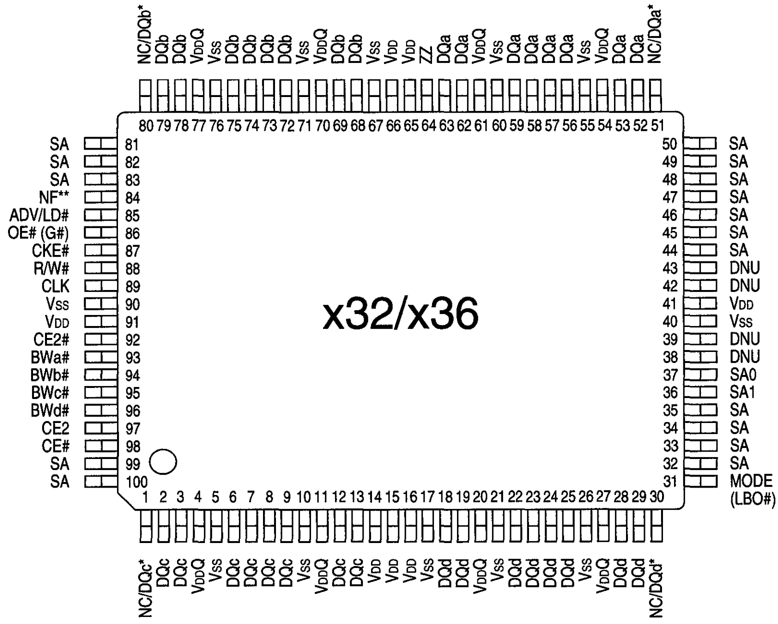
PIN #	x18	x32	x36
51	NC	NC	DQa
52	NC	DQa	DQa
53	NC	DQa	DQa
54	VDDQ		
55	VSS		
56	NC	DQa	DQa
57	NC	DQa	DQa
58	DQa		
59	DQa		
60	VSS		
61	VDDQ		
62	DQa		
63	DQa		
64	ZZ		
65	VDD		
66	VDD		
67	VSS		
68	DQa	DQb	DQb
69	DQa	DQb	DQb
70	VDDQ		
71	VSS		
72	DQa	DQb	DQb
73	DQa	DQb	DQb
74	DQa	DQb	DQb
75	NC	DQb	DQb

PIN #	x18	x32	x36
76	VSS		
77	VDDQ		
78	NC	DQb	DQb
79	NC	DQb	DQb
80	SA	NC	DQb
81	SA		
82	SA		
83	SA		
84	NF*		
85	ADV/LD#		
86	OE# (G#)		
87	CKE#		
88	R/W#		
89	CLK		
90	VSS		
91	VDD		
92	CE2#		
93	BWa#		
94	BWb#		
95	NC	BWc#	BWc#
96	NC	BWd#	BWd#
97	CE2		
98	CE#		
99	SA		
100	SA		

Pin 84 is reserved for address expansion.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





* NC for x32 version, DQx for x36 version.

** Pin 84 is reserved for address expansion.

PIN DESCRIPTIONS

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 44-50, 80-83, 99, 100	37 36 32-35, 44-50, 81-83, 99, 100	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Pin is reserved as an address bit for higher-density 16Mb ZBT SRAMs. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
93 94 – –	93 94 95 96	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWs are associated with addresses and apply to subsequent data. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW).
92	92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
86	86	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
85	85	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
87	87	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE# is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.

PIN DESCRIPTIONS (continued)

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
88	88	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
38, 39, 42, 43	38, 39, 42, 43	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to minimize thermal impedance.
(a) 58, 59, 62, 63, 68, 69, 72-74 (b) 8, 9, 12, 13, 18, 19, 22-24	(a) 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
N/A	51 80 1 30	NC/DQa NC/DQb NC/DQc NC/DQd	NC/ I/O	No Connect/Data Bits: On the x32 version, these pins are no connect (NC) and can be left floating or connected to GND to minimize thermal impedance. On the x36 version, these bits are DQs.
31	31	MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
1-3, 6, 7, 25, 28-30, 51-53, 56, 57, 75, 78, 79, 95, 96	N/A	NC	NC	No Connect: These pins can be left floating or connected to GND to minimize thermal impedance.
84	84	NF	–	No Function: This pin is internally connected to the die and will have the capacitance of an input pin. It is allowable to leave this pin unconnected or driven by signals. Pin 84 is reserved as an address pin for the 16Mb ZBT SRAM.
14-16, 41, 65, 66, 91	14-16, 41, 65, 66, 91	VDD	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	VDDQ	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	VSS	Supply	Ground: GND.

4Mb and 8Mb SMART ZBT™ SRAM

MT56L256_18P, MT56L128_32P,
MT56L128_36P; MT56L512_18P,
MT56L256_32P, MT56L256_36P

3.3V VDD, 3.3V or 2.5V I/O

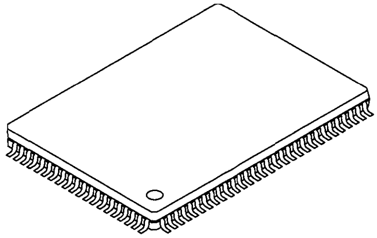
FEATURES

- High frequency and 100 percent bus utilization
- Fast cycle times: 5ns, 6ns, 7.5ns and 10ns
- Single +3.3V ±5% power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer supply (VDDQ)
- SMART ZBT output control for minimized bus contention across a broad set of applications
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs eliminate the need to control OE#
- Common data inputs and data outputs
- Pin/function compatibility with 16Mb SMART ZBT SRAM family
- Automatic power-down

OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
3.7ns/5ns/200 MHz	-5
4ns/6ns/166 MHz	-6
4.5ns/7.5ns/133 MHz	-7.5
5.5ns/10ns/100 MHz	-10
• Configurations	
4Mb	
256K x 18	MT56L256_18P
128K x 32	MT56L128_32P
128K x 36	MT56L128_36P
8Mb	
512K x 18	MT56L512_18P
256K x 32	MT56L256_32P
256K x 36	MT56L256_36P
• Package	
100-pin TQFP	T
• Options	
Low-power version	P

- Part Number Example: MT56L256L18PT-6

100-Pin TQFP*
(D-1)



*JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

The Micron® SMART Zero Bus Turnaround™ (SMART ZBT™) SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

Micron's 4Mb and 8Mb SMART ZBT SRAMs integrate a 256K x 18, 128K x 32, or 128K x 36 and a 512K x 18, 256K x 32, or 256K x 36 SRAM core, respectively, with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles when transitioning from READ to WRITE, or vice versa. New SMART ZBT technology provides enhanced output delay to allow the bus to clear before the outputs drive, thereby reducing the magnitude or occurrence of bus contention.

All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enables (CE#), (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc# and BWd#) and read/write (R/W#).

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW or left unconnected if burst is unused. The flow-through data-out (Q) is enabled by OE#. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

All READ, WRITE and DESELECT cycles are initiated by the ADV/LD# input. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV/LD#).

SMART ZBT and SMART Zero Bus Turnaround are trademarks of Integrated Device Technology, Inc., and the architecture is supported by Micron Technology, Inc.
Micron is a registered trademark of Micron Technology, Inc.

SYNCBURST™ SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Supply Voltage	I/O Voltage	Mode	Part Number	Access Time (ns)	Cycle Time (ns)	Package/No. of Pins			Page
							TQFP	BGA	DIE*	
64K x 18	3.3V	3.3V	Flow-Through	MT58LC64K18B4	7.5, 8.5, 9, 10	8.8, 10, 10.5, 15	100	–	C1/C2	2-39
64K x 18	3.3V	3.3V	Pipelined, SCD	MT58LC64K18D9	3.8, 4.2, 5, 6	6.6, 7.5, 10, 11	100	–	C1/C2	2-43
64K x 18	3.3V	3.3V	Pipelined, DCD	MT58LC64K18C6	3.8, 4.2, 4.5, 5, 6	6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-47
128K x 18	3.3V	3.3V	Flow-Through	MT58LC128K18B4	7.5, 8.5, 9, 10	8.8, 10, 10.5, 15	100	–	C1/C2	2-51
128K x 18	3.3V	2.5V	Flow-Through	MT58LC128K18E1	7.5, 8.5, 9, 10	8.8, 10, 10.5, 15	100	–	C1/C2	2-51
128K x 18	3.3V	3.3V	Pipelined, SCD	MT58LC128K18D9	3.5, 3.8, 4.2, 4.5, 5, 6	5, 6, 6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-55
128K x 18	3.3V	2.5V	Pipelined, SCD	MT58LC128K18G1	3.5, 3.8, 4.2, 4.5, 5, 6	5, 6, 6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-55
128K x 18	3.3V	3.3V	Pipelined, DCD	MT58LC128K18C6	3.5, 3.8, 4.2, 4.5, 5, 6	5, 6, 6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-59
128K x 18	3.3V	2.5V	Pipelined, DCD	MT58LC128K18F1	3.5, 3.8, 4.2, 4.5, 5, 6	5, 6, 6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-59
256K x 18	3.3V	3.3V/2.5V	Flow-Through	MT58L256_18F**	6.8, 7.5, 8.5, 10	8, 8.8, 10, 15	100	119		2-63
256K x 18	3.3V	3.3V/2.5V	Pipelined, SCD	MT58L256_18P	2.9, 3.1, 3.5, 4, 5	4.4, 5, 6, 7.5, 10	100	119		2-67
256K x 18	3.3V	3.3V	Pipelined, DCD	MT58L256L18D	3.5, 4.2, 5	6, 7.5, 10	100	119		2-71
512K x 18	3.3V	3.3V/2.5V	Flow-Through	MT58L512_18F	6.8, 7.5, 8.5, 10	8, 8.8, 10, 15	100	119		2-75
512K x 18	3.3V	3.3V/2.5V	Pipelined, SCD	MT58L512_18P	2.9, 3.1, 3.5, 4, 5	4.4, 5, 6, 6.6, 7.5, 10	100	119		2-81
512K x 18	3.3V	3.3V	Pipelined, DCD	MT58L512L18D	3.5, 4, 5	6, 7.5, 10	100	119		2-87
32K x 32	3.3V	3.3V	Flow-Through	MT58LC32K32B4	7.5, 8.5, 9, 10	8.8, 10, 10.5, 15	100	–	C1/C2	2-39
32K x 32	3.3V	3.3V	Pipelined, SCD	MT58LC32K32D9	3.8, 4.2, 5, 6	6.6, 7.5, 10, 11	100	–	C1/C2	2-43
32K x 32	3.3V	3.3V	Pipelined, DCD	MT58LC32K32C6	3.8, 4.2, 4.5, 5, 6	6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-47
64K x 32	3.3V	3.3V	Flow-Through	MT58LC64K32B4	7.5, 8.5, 9, 10	8.8, 10, 10.5, 15	100	–	C1/C2	2-51
64K x 32	3.3V	2.5V	Flow-Through	MT58LC64K32E1	7.5, 8.5, 9, 10	8.8, 10, 10.5, 15	100	–	C1/C2	2-51
64K x 32	3.3V	3.3V	Pipelined, SCD	MT58LC64K32D9	3.5, 3.8, 4.2, 4.5, 5, 6	5, 6, 6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-55
64K x 32	3.3V	2.5V	Pipelined, SCD	MT58LC64K32G1	3.5, 3.8, 4.2, 4.5, 5, 6	5, 6, 6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-55
64K x 32	3.3V	3.3V	Pipelined, DCD	MT58LC64K32C6	3.5, 3.8, 4.2, 4.5, 5, 6	5, 6, 6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-59
64K x 32	3.3V	2.5V	Pipelined, DCD	MT58LC64K32F1	3.5, 3.8, 4.2, 4.5, 5, 6	5, 6, 6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-59
128K x 32	3.3V	3.3V/2.5V	Flow-Through	MT58L128_32F	6.8, 7.5, 8.5, 10	8, 8.8, 10, 15	100	119		2-63
128K x 32	3.3V	3.3V/2.5V	Pipelined, SCD	MT58L128_32P	2.9, 3.1, 3.5, 4, 5	4.4, 5, 6, 7.5, 10	100	119		2-67
128K x 32	3.3V	3.3V	Pipelined, DCD	MT58L128L32D	3.5, 4.2, 5	6, 7.5, 10	100	119		2-71
256K x 32	3.3V	3.3V/2.5V	Flow-Through	MT58L256_32F	6.8, 7.5, 8.5, 10	8, 8.8, 10, 15	100	119		2-75
256K x 32	3.3V	3.3V/2.5V	Pipelined, SCD	MT58L256_32P	2.9, 3.1, 3.5, 4, 5	4.4, 5, 6, 6.6, 7.5, 10	100	119		2-81
256K x 32	3.3V	3.3V	Pipelined, DCD	MT58L256L32D	3.5, 4, 5	6, 7.5, 10	100	119		2-87
32K x 36	3.3V	3.3V	Flow-Through	MT58LC32K36B4	7.5, 8.5, 9, 10	8.8, 10, 10.5, 15	100	–	C1/C2	2-39
32K x 36	3.3V	3.3V	Pipelined, SCD	MT58LC32K36D9	3.8, 4.2, 5, 6	6.6, 7.5, 10, 11	100	–	C1/C2	2-43
32K x 36	3.3V	3.3V	Pipelined, DCD	MT58LC32K36C6	3.8, 4.2, 4.5, 5, 6	6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-47
64K x 36	3.3V	3.3V	Flow-Through	MT58LC64K36B4	7.5, 8.5, 9, 10	8.8, 10, 10.5, 15	100	–	C1/C2	2-51
64K x 36	3.3V	2.5V	Flow-Through	MT58LC64K36E1	7.5, 8.5, 9, 10	8.8, 10, 10.5, 15	100	–	C1/C2	2-51
64K x 36	3.3V	3.3V	Pipelined, SCD	MT58LC64K36D9	3.5, 3.8, 4.2, 4.5, 5, 6	5, 6, 6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-55
64K x 36	3.3V	2.5V	Pipelined, SCD	MT58LC64K36G1	3.5, 3.8, 4.2, 4.5, 5, 6	5, 6, 6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-55
64K x 36	3.3V	3.3V	Pipelined, DCD	MT58LC64K36C6	3.5, 3.8, 4.2, 4.5, 5, 6	5, 6, 6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-59
64K x 36	3.3V	2.5V	Pipelined, DCD	MT58LC64K36F1	3.5, 3.8, 4.2, 4.5, 5, 6	5, 6, 6.6, 7.5, 8.5, 10, 11	100	–	C1/C2	2-59
128K x 36	3.3V	3.3V/2.5V	Flow-Through	MT58L128_36F	6.8, 7.5, 8.5, 10	8, 8.8, 10, 15	100	119		2-63
128K x 36	3.3V	3.3V/2.5V	Pipelined, SCD	MT58L128_36P	2.9, 3.1, 3.5, 4, 5	4.4, 5, 6, 7.5, 10	100	119		2-67
128K x 36	3.3V	3.3V	Pipelined, DCD	MT58L128L36D	3.5, 4.2, 5	6, 7.5, 10	100	119		2-71
256K x 36	3.3V	3.3V/2.5V	Flow-Through	MT58L256_36F	6.8, 7.5, 8.5, 10	8, 8.8, 10, 15	100	119		2-75
256K x 36	3.3V	3.3V/2.5V	Pipelined, SCD	MT58L256_36P	2.9, 3.1, 3.5, 4, 5	4.4, 5, 6, 6.6, 7.5, 10	100	119		2-81
256K x 36	3.3V	3.3V	Pipelined, DCD	MT58L256L36D	3.5, 4, 5	6, 7.5, 10	100	119		2-87

SCD = Single-cycle deselect, DCD = Double-cycle deselect
*Contact factory for availability of C3- to C7-level die products.
**The placeholder in the part number is replaced with an "L" for 3.3V I/O parts and a "V" for 2.5V I/O parts.

1Mb SYNCBURST™ SRAM

MT58LC64K18B4, MT58LC32K32B4,
MT58LC32K36B4

3.3V VDD, 3.3V I/O, Flow-Through

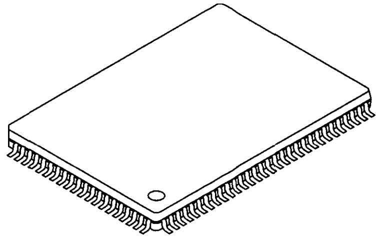
FEATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (VDD)
- Separate +3.3V +0.3V/-0.165V isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- x18, x32 and x36 versions available

OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
7.5ns/8.8ns/113 MHz	-7.5
8.5ns/10ns/100 MHz	-8.5
9ns/10.5ns/95 MHz	-9
10ns/15ns/66 MHz	-10
• Configurations	
64K x 18	MT58LC64K18B4
32K x 32	MT58LC32K32B4
32K x 36	MT58LC32K36B4
• Package	
100-pin TQFP	LG

- Part Number Example: MT58LC32K36B4LG-8.5

100-Pin TQFP*
(D-1)



*JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

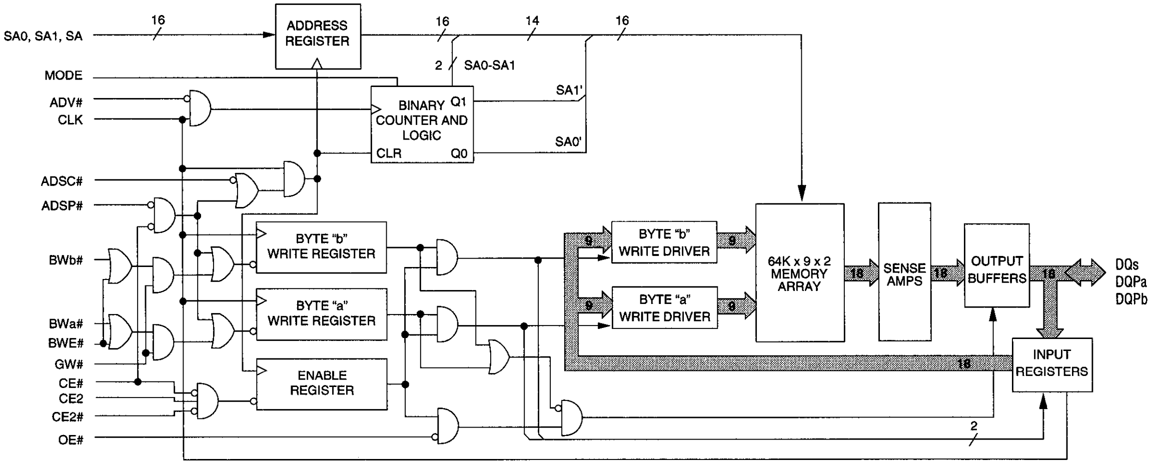
The MT58LC64K18B4 and MT58LC32K32/36B4 1Mb SRAMs integrate a 64K x 18, 32K x 32, or 32K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

Asynchronous inputs include the output enable (OE#), snooze enable (ZZ) and clock (CLK). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

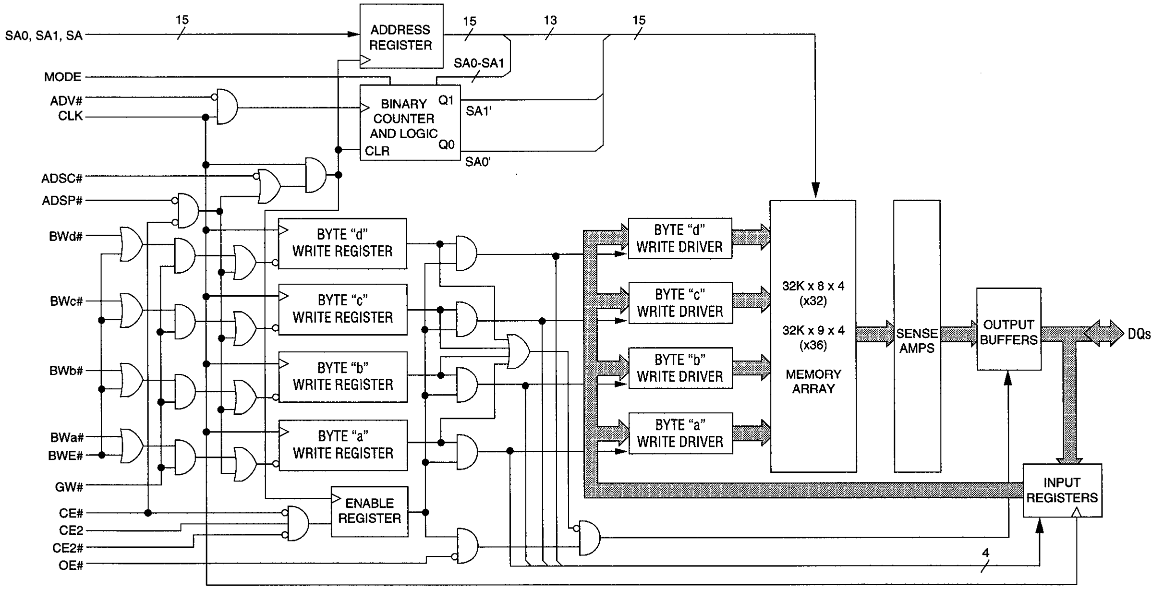
Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

FUNCTIONAL BLOCK DIAGRAM
64K x 18



FUNCTIONAL BLOCK DIAGRAM
32K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

GENERAL DESCRIPTION (continued)

Micron's 1Mb SyncBurst SRAMs operate from a +3.3V power supply, and all inputs and outputs are TTL-compatible. The device is ideally suited for 486, Pentium®, 680X0 and PowerPC™ systems and systems that benefit from a very wide data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

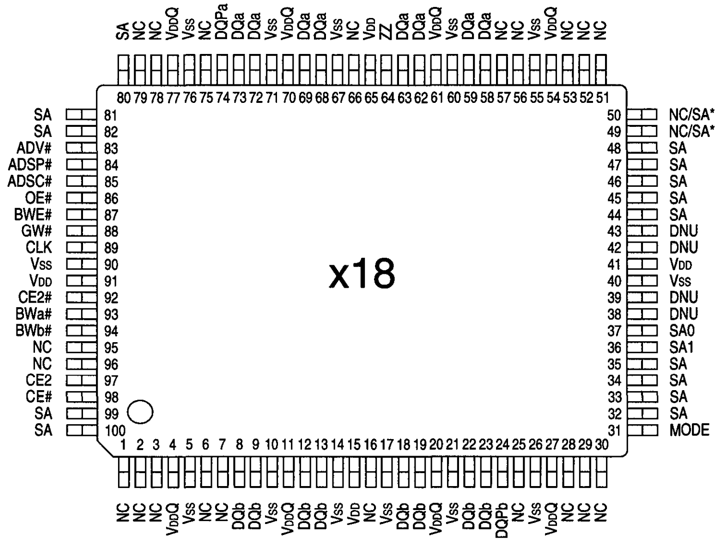
TQFP PIN ASSIGNMENT TABLE

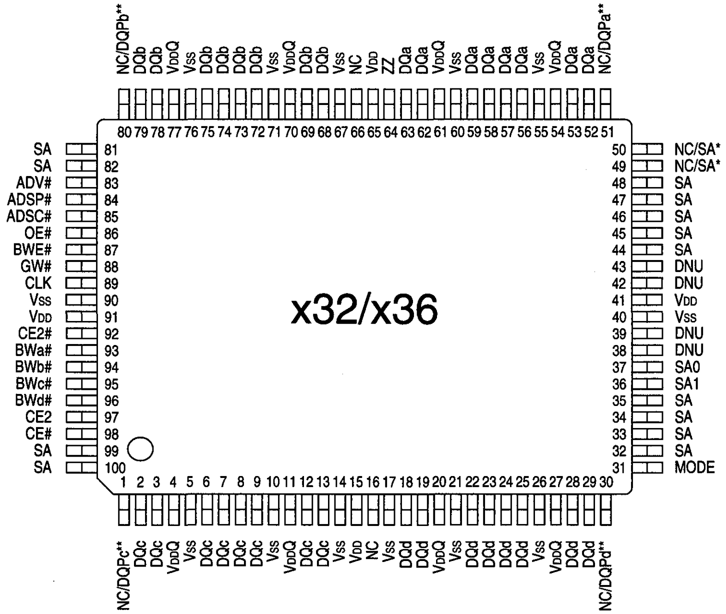
PIN #	x18	x32/x36
1	NC	NC/DQPc**
2	NC	DQc
3	NC	DQc
4	VDDQ	
5	Vss	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	Vss	
11	VDDQ	
12	DQb	DQc
13	DQb	DQc
14	Vss	
15	VDD	
16	NC	
17	Vss	
18	DQb	DQd
19	DQb	DQd
20	VDDQ	
21	Vss	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd
26	Vss	
27	VDDQ	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd**
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	Vss	
41	VDD	
42	DNU	
43	DNU	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	NC/SA*	
50	NC/SA*	
51	NC	NC/DQPa**
52	NC	DQa
53	NC	DQa
54	VDDQ	
55	Vss	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	Vss	
61	VDDQ	
62	DQa	
63	DQa	
64	ZZ	
65	VDD	
66	NC	
67	Vss	
68	DQa	DQb
69	DQa	DQb
70	VDDQ	
71	Vss	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb
76	Vss	
77	VDDQ	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb**
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	Vss	
91	VDD	
92	CE2#	
93	BWa#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

* Pins 49 and 50 are reserved for address expansion.

** No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





* Pins 49 and 50 are reserved for address expansion.

** No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

1Mb SYNCBURST™ SRAM

MT58LC64K18D9, MT58LC32K32D9, MT58LC32K36D9

3.3V VDD, 3.3V I/O, Pipelined, Single-Cycle Deselect

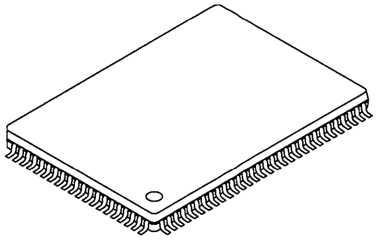
FEATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (VDD)
- Separate +3.3V +0.3V/-0.165V isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Single-cycle deselect (Pentium® BSRAM-compatible)
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP for high density, high speed
- Low capacitive bus loading
- x18, x32 and x36 options available

OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
3.8ns/6.6ns/150 MHz	-6.6
4.2ns/7.5ns/133 MHz	-7.5
5ns/10ns/100 MHz	-10
6ns/11ns/90 MHz	-11
• Configurations	
64K x 18	MT58LC64K18D9
32K x 32	MT58LC32K32D9
32K x 36	MT58LC32K36D9
• Package	
100-pin TQFP	LG

- Part Number Example: MT58LC64K18D9LG-11

100-Pin TQFP*
(D-1)



*JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

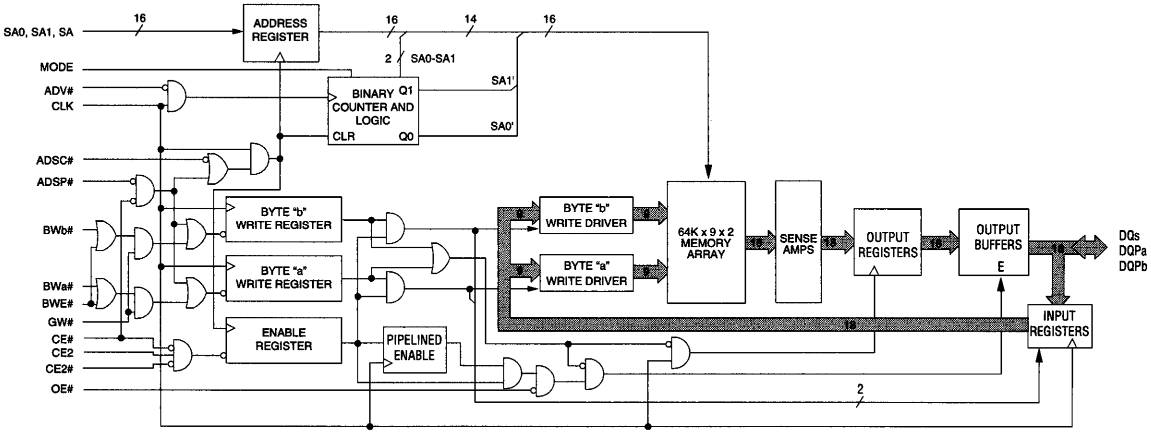
The MT58LC64K18D9 and MT58LC32K32/36D9 1Mb SRAMs integrate a 64K x 18, 32K x 32, or 32K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

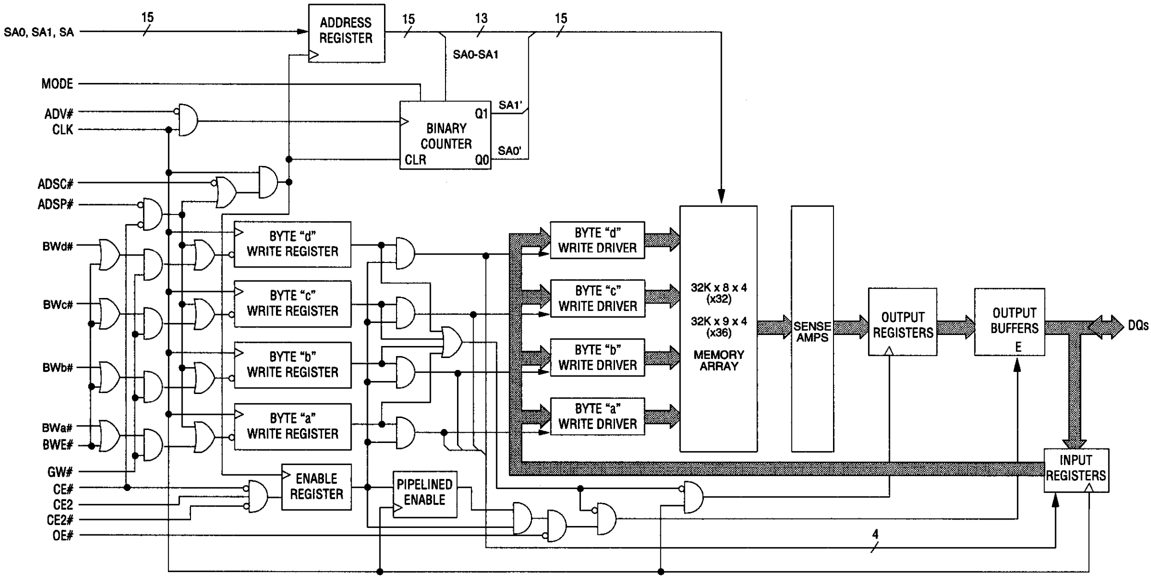
Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. GW# LOW causes all bytes to be written. Parity pins are only available on the x18 and x36 versions.

FUNCTIONAL BLOCK DIAGRAM
64K x 18



FUNCTIONAL BLOCK DIAGRAM
32K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

ENERAL DESCRIPTION (continued)

This device incorporates a single-cycle deselect feature uring READ cycles. If the device is immediately deselected fter a READ cycle, the output bus goes to a High-Z state KQHZ nanoseconds after the rising edge of clock.

Micron's 1Mb SyncBurst SRAMs operate from a +3.3V ower supply, and all inputs and outputs are TTL-ompatible. The device is ideally suited for Pentium and PowerPC™ pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

QFP PIN ASSIGNMENT TABLE

PIN #	x18	x32/x36
1	NC	NC/DQPc**
2	NC	DQc
3	NC	DQc
4	VDDQ	
5	Vss	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	Vss	
11	VDDQ	
12	DQb	DQc
13	DQb	DQc
14	VDD	
15	VDD	
16	NC	
17	Vss	
18	DQb	DQd
19	DQb	DQd
20	VDDQ	
21	Vss	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd

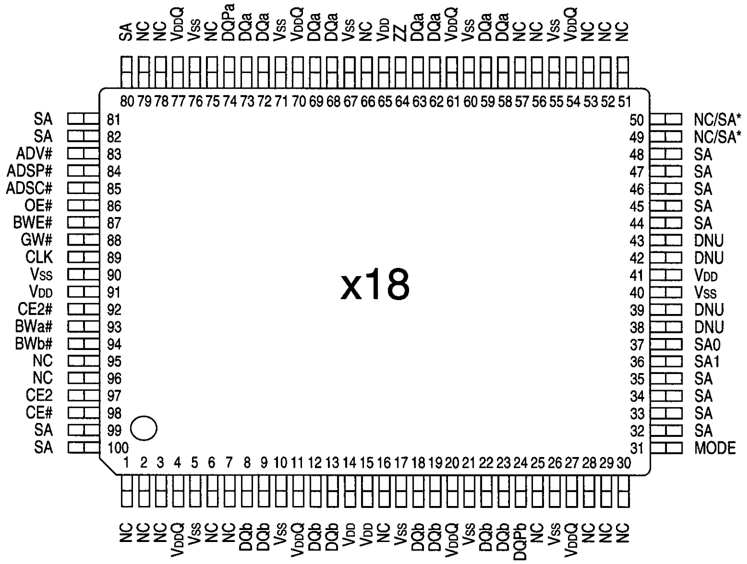
PIN #	x18	x32/x36
26	Vss	
27	VDDQ	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd**
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	Vss	
41	VDD	
42	DNU	
43	DNU	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	NC/SA*	
50	NC/SA*	

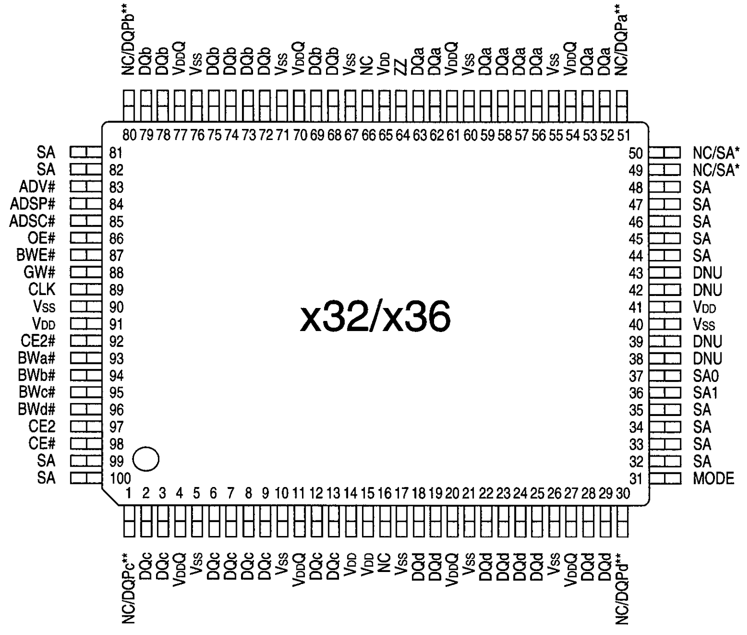
PIN #	x18	x32/x36
51	NC	NC/DQPa**
52	NC	DQa
53	NC	DQa
54	VDDQ	
55	Vss	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	Vss	
61	VDDQ	
62	DQa	
63	DQa	
64	ZZ	
65	VDD	
66	NC	
67	Vss	
68	DQa	DQb
69	DQa	DQb
70	VDDQ	
71	Vss	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb

PIN #	x18	x32/x36
76	Vss	
77	VDDQ	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb**
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	Vss	
91	VDD	
92	CE2#	
93	BWa#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

Pins 49 and 50 are reserved for address expansion.
* No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





* Pins 49 and 50 are reserved for address expansion.

** No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

1Mb SYNCBURST™ SRAM

MT58LC64K18C6, MT58LC32K32C6, MT58LC32K36C6

3.3V VDD, 3.3V I/O, Pipelined, Double-Cycle Deselect

FEATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (VDD)
- Separate +3.3V +0.3V/-0.165V isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- x18, x32 and x36 options available

OPTIONS

OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
3.8ns/6.6ns/150 MHz	-6.6
4.2ns/7.5ns/133 MHz	-7.5
4.5ns/8.5ns/117 MHz	-8.5
5ns/10ns/100 MHz	-10
6ns/11ns/90 MHz	-11
• Configurations	
64K x 18	MT58LC64K18C6
32K x 32	MT58LC32K32C6
32K x 36	MT58LC32K36C6
• Package	
100-pin TQFP	LG

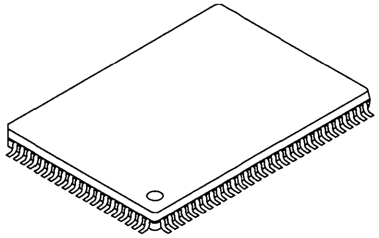
- Part Number Example: MT58LC64K18C6LG-7.5

GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

The MT58LC64K18C6 and MT58LC32K32/36C6 1Mb SRAMs integrate a 64K x 18, 32K x 32, or 32K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

100-Pin TQFP*
(D-1)



*JEDEC-standard MS-026 BHA (LQFP).

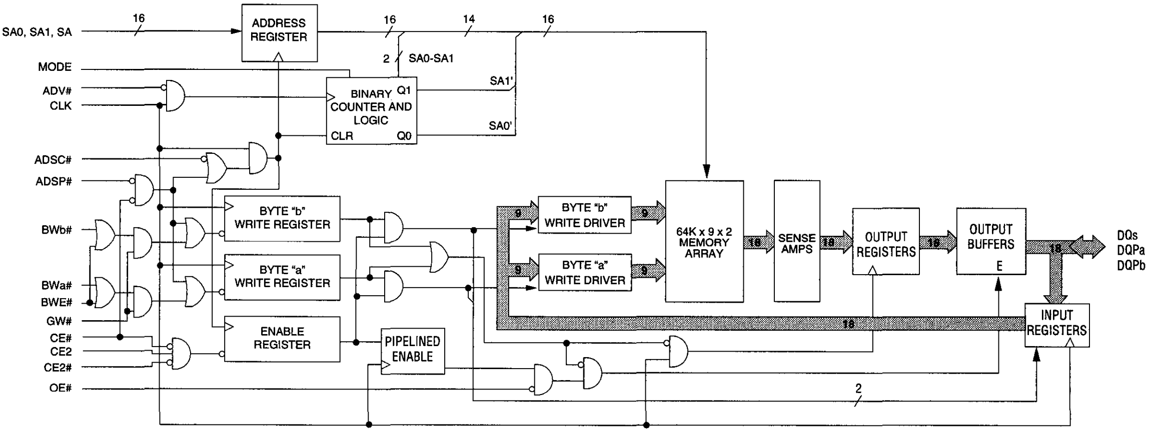
Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

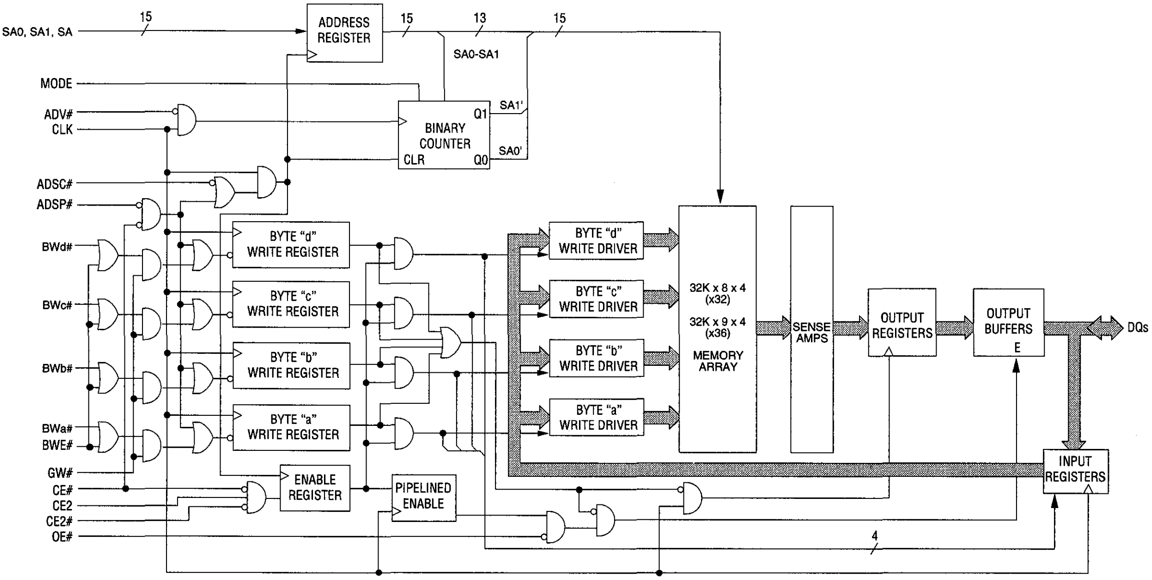
Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. GW# LOW causes all bytes to be written. Parity pins are only available on the x18 and x36 versions.

The device incorporates an additional pipelined enable register which delays turning off the output buffer an

FUNCTIONAL BLOCK DIAGRAM
64K x 18



FUNCTIONAL BLOCK DIAGRAM
32K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

;ENERAL DESCRIPTION (continued)

ɔdditional cycle when a deselect is executed. This feature llows depth expansion without penalizing system erformance.

Micron's 1Mb SyncBurst SRAMs operate from a +3.3V ower supply, and all inputs and outputs are TTL-ɔmpatible. The device is ideally suited for Pentium® and PowerPC™ pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

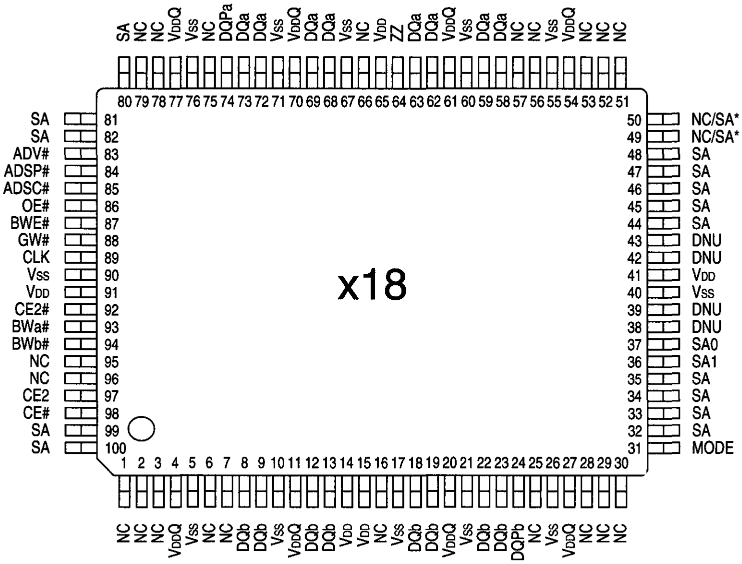
Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

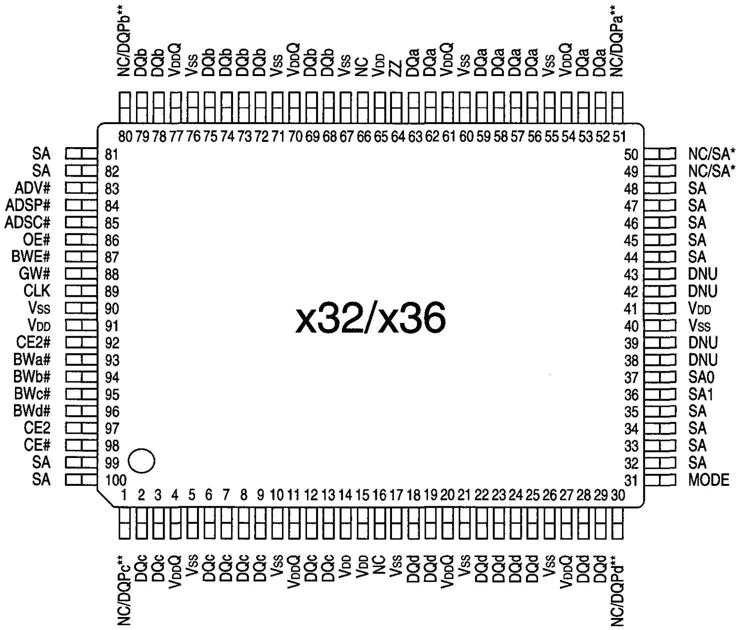
'QFP PIN ASSIGNMENT TABLE

PIN #	x18	x32/x36
1	NC	NC/DQPc**
2	NC	DQc
3	NC	DQc
4	VDDQ	
5	VSS	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	VSS	
11	VDDQ	
12	DQb	DQc
13	DQb	DQc
14	VDD	
15	VDD	
16	NC	
17	VSS	
18	DQb	DQd
19	DQb	DQd
20	VDDQ	
21	VSS	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd
26	VSS	
27	VDDQ	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd**
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	VSS	
41	VDD	
42	DNU	
43	DNU	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	NC/SA*	
50	NC/SA*	
51	NC	NC/DQPa**
52	NC	DQa
53	NC	DQa
54	VDDQ	
55	VSS	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	VSS	
61	VDDQ	
62	DQa	
63	DQa	
64	ZZ	
65	VDD	
66	NC	
67	VSS	
68	DQa	DQb
69	DQa	DQb
70	VDDQ	
71	VSS	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb
76	VSS	
77	VDDQ	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb**
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	VSS	
91	VDD	
92	CE2#	
93	BWa#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

Pins 49 and 50 are reserved for address expansion.
No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





* Pins 49 and 50 are reserved for address expansion.

** No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

2Mb SYNCBURST™ SRAM

MT58LC128K18B4, MT58LC64K32B4,
MT58LC64K36B4; MT58LC128K18E1,
MT58LC64K32E1, MT58LC64K36E1

3.3V VDD, 3.3V or 2.5V I/O, Flow-Through

FEATURES

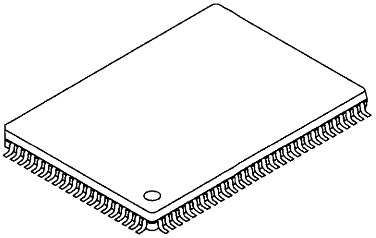
- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- x18, x32 and x36 versions available

OPTIONS

OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
7.5ns/8.8ns/113 MHz	-7.5
8.5ns/10ns/100 MHz	-8.5
9ns/10.5ns/95 MHz	-9
10ns/15ns/66 MHz	-10
• Configurations	
3.3V I/O	
128K x 18	MT58LC128K18B4
64K x 32	MT58LC64K32B4
64K x 36	MT58LC64K36B4
2.5V I/O	
128K x 18	MT58LC128K18E1
64K x 32	MT58LC64K32E1
64K x 36	MT58LC64K36E1
• Package	
100-pin TQFP	LG

- Part Number Example: MT58LC64K36B4LG-8.5

100-Pin TQFP*
(D-1)



*JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

Micron's 2Mb SyncBurst SRAMs integrate a 128K x 18, 64K x 32, or 64K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

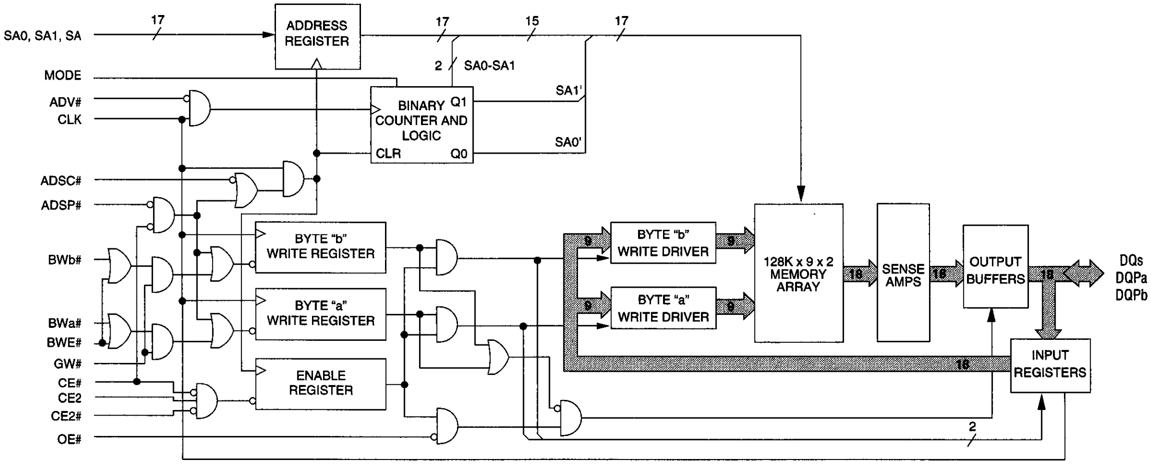
Asynchronous inputs include the output enable (OE#), snooze enable (ZZ) and clock (CLK). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

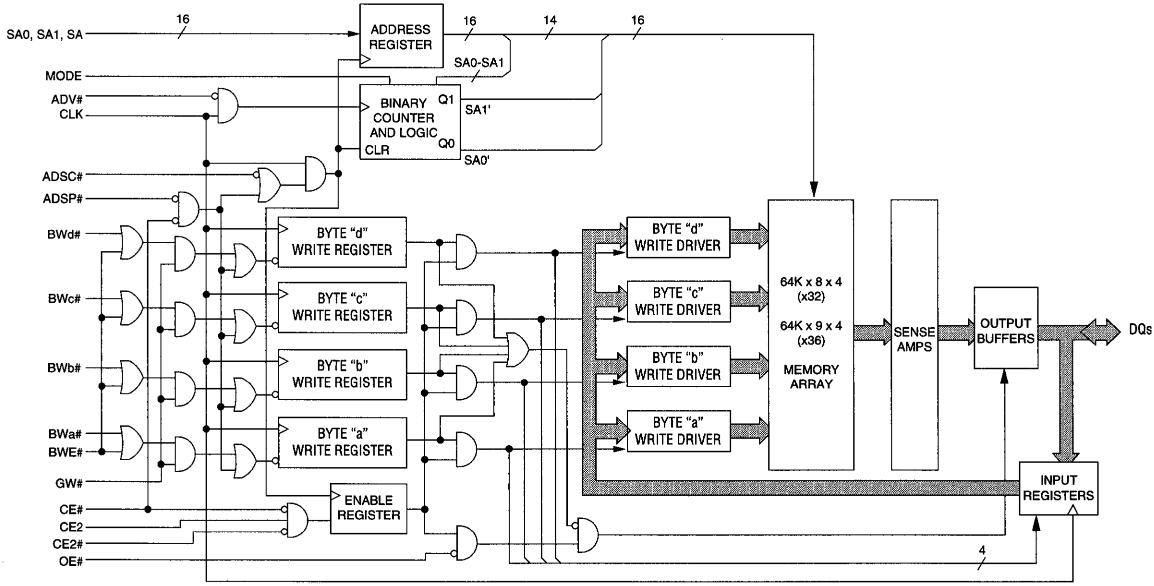
Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. During WRITE cycles on the x32 and x36 devices, BWa#

Micron Technology, Inc., reserves the right to change products or specifications without notice.

FUNCTIONAL BLOCK DIAGRAM
128K x 18



FUNCTIONAL BLOCK DIAGRAM
64K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

ENERAL DESCRIPTION (continued)

ontrols DQa pins and DQPa; BWb# controls DQb pins and QPb; BWc# controls DQc pins and DQPc; BWd# controls Qd pins and DQPd. GW# LOW causes all bytes to be ritten. Parity bits are only available on the x18 and x36 ersions.

Micron's 2Mb SyncBurst SRAMs operate from a +3.3V DD power supply, and all inputs and outputs are TTL-ompatible. Users can choose either a 3.3V or 2.5V I/O version. The device is ideally suited for 486, Pentium®, 680X0 and PowerPC™ systems and systems that benefit from a very wide data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

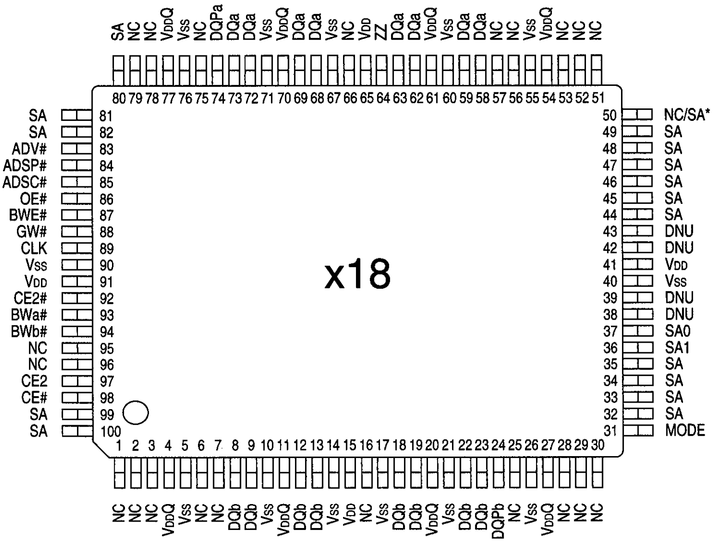
QFP PIN ASSIGNMENT TABLE

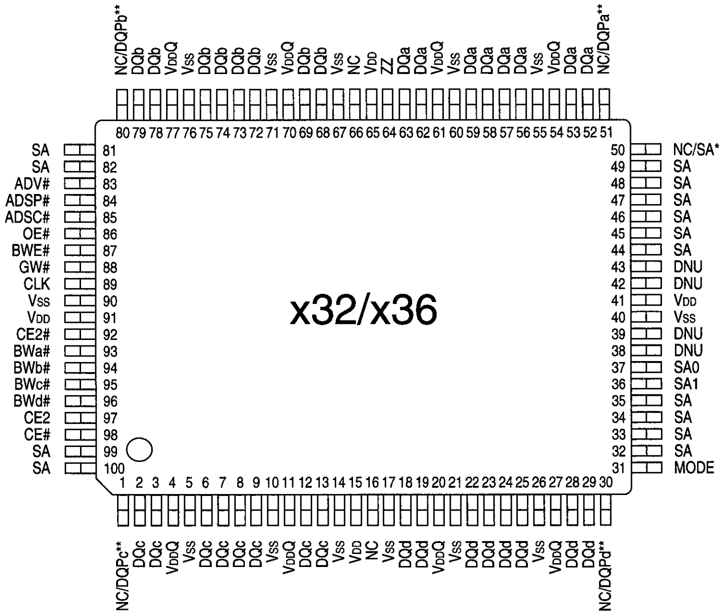
IN #	x18	x32/x36
1	NC	NC/DQPc**
2	NC	DQc
3	NC	DQc
4	VDDQ	
5	Vss	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	Vss	
11	VDDQ	
12	DQb	DQc
13	DQb	DQc
14	Vss	
15	VDD	
16	NC	
17	Vss	
18	DQb	DQd
19	DQb	DQd
20	VDDQ	
21	Vss	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd
26	Vss	
27	VDDQ	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd**
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	Vss	
41	VDD	
42	DNU	
43	DNU	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	SA	
50	NC/SA*	
51	NC	NC/DQPa**
52	NC	DQa
53	NC	DQa
54	VDDQ	
55	Vss	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	Vss	
61	VDDQ	
62	DQa	
63	DQa	
64	ZZ	
65	VDD	
66	NC	
67	Vss	
68	DQa	DQb
69	DQa	DQb
70	VDDQ	
71	Vss	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb
76	Vss	
77	VDDQ	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb**
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	Vss	
91	VDD	
92	CE2#	
93	BWa#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

Pin 50 is reserved for address expansion.

No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





* Pin 50 is reserved for address expansion.

** No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

MICRON
TECHNOLOGY, INC.

**2Mb: 128K x 18, 64K x 32/36
PIPELINED, SCD SYNCBURST SRAM**

2Mb SYNCBURST™ SRAM

MT58LC128K18D9, MT58LC64K32D9, MT58LC64K36D9; MT58LC128K18G1, MT58LC64K32G1, MT58LC64K36G1

3.3V VDD, 3.3V or 2.5V I/O, Pipelined, Single-Cycle Deselect

EATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Single-cycle deselect (Pentium® BSRAM-compatible)
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP for high density, high speed
- Low capacitive bus loading
- x18, x32 and x36 options available

PTIONS / MARKING

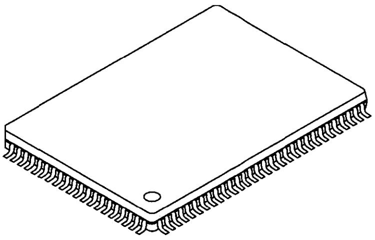
PTIONS	MARKING
Timing (Access/Cycle/MHz)	
3.5ns/5ns/200 MHz	-5
3.5ns/6ns/166 MHz	-6
3.8ns/6.6ns/150 MHz	-6.6
4.2ns/7.5ns/133 MHz	-7.5
4.5ns/8.5ns/117 MHz	-8.5
5ns/10ns/100 MHz	-10
6ns/11ns/90 MHz	-11*

*-11 is only available with 3.3V I/O

Configurations	
3.3V I/O	
128K x 18	MT58LC128K18D9
64K x 32	MT58LC64K32D9
64K x 36	MT58LC64K36D9
2.5V I/O	
128K x 18	MT58LC128K18G1
64K x 32	MT58LC64K32G1
64K x 36	MT58LC64K36G1
Package	
100-pin TQFP	LG

Part Number Example: MT58LC128K18D9LG-11

100-Pin TQFP**
(D-1)



**JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

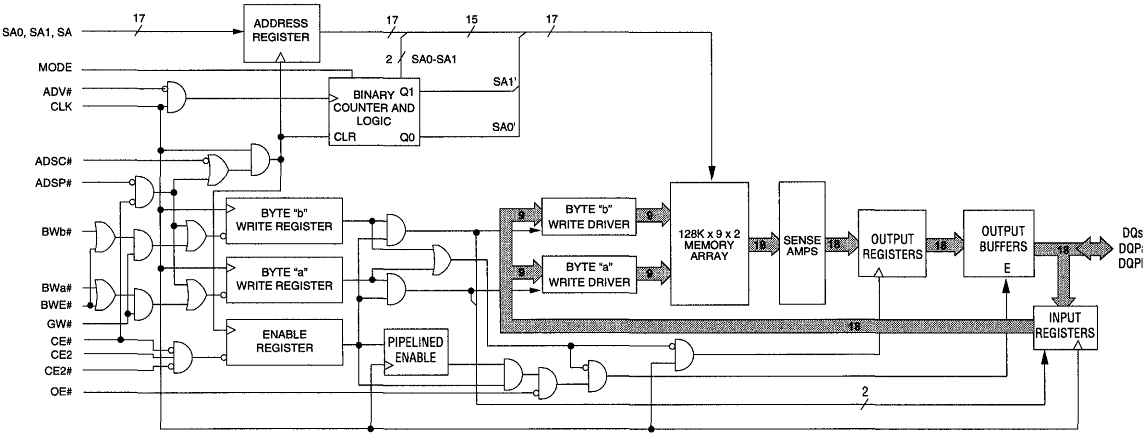
Micron's 2Mb SyncBurst SRAMs integrate a 128K x 18, 64K x 32, or 64K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

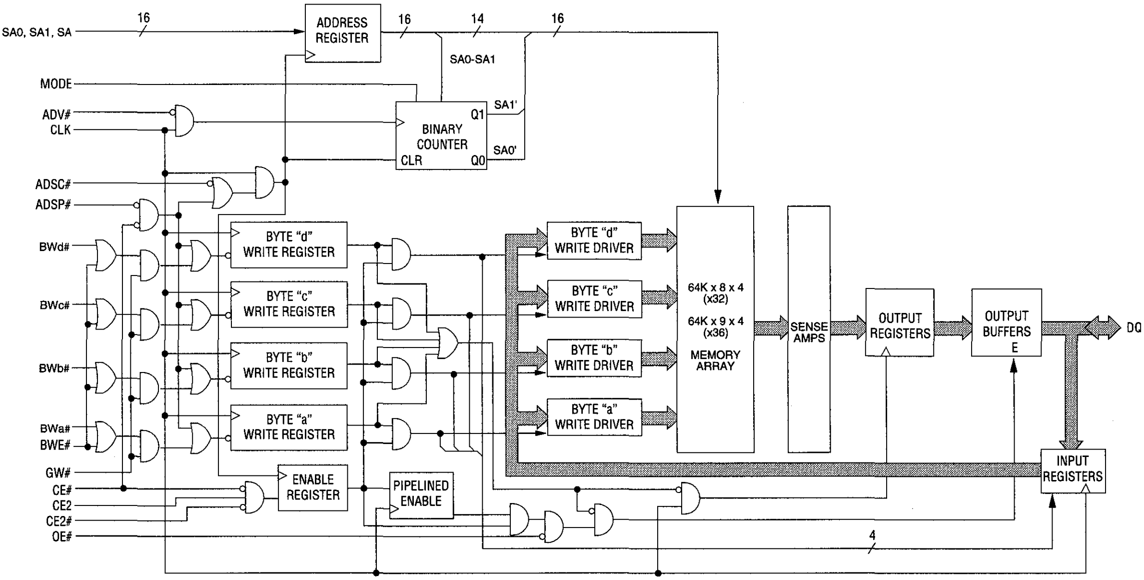
Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written.

FUNCTIONAL BLOCK DIAGRAM
128K x 18



FUNCTIONAL BLOCK DIAGRAM
64K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

ENERAL DESCRIPTION (continued)

uring WRITE cycles on the x18 device, BWa# controls Qa pins and DQPa; BWb# controls DQb pins and DQPb. uring WRITE cycles on the x32 and x36 devices, BWa# ontrols DQa pins and DQPa; BWb# controls DQb pins and QPb; BWc# controls DQc pins and DQPc; BWd# controls Qd pins and DQPd. GW# LOW causes all bytes to be ritten. Parity pins are only available on the x18 and x36 ersions.

This device incorporates a single-cycle deselect feature uring READ cycles. If the device is immediately deselected ter a READ cycle, the output bus goes to a High-Z state QHZ nanoseconds after the rising edge of clock.

Micron's 2Mb SyncBurst SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are TTL-compatible. Users can choose either a 3.3V or 2.5V I/O version. The device is ideally suited for Pentium and PowerPC™ pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

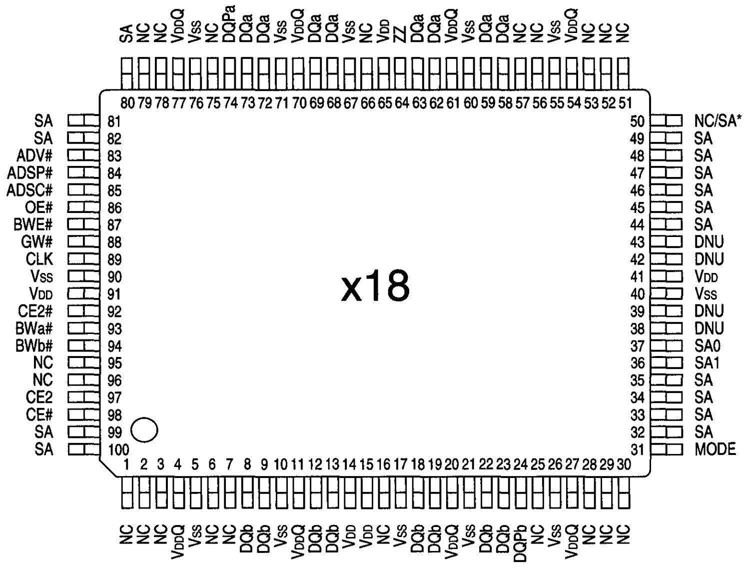
Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

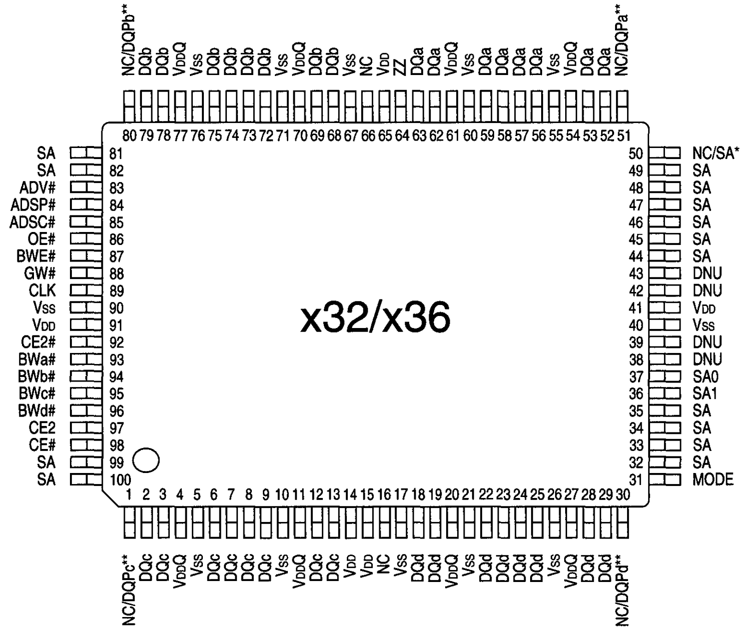
QFP PIN ASSIGNMENT TABLE

IN #	x18	x32/x36	PIN #	x18	x32/x36	PIN #	x18	x32/x36	PIN #	x18	x32/x36
1	NC	NC/DQPc**	26	Vss		51	NC	NC/DQPa**	76	Vss	
2	NC	DQc	27	VDDQ		52	NC	DQa	77	VDDQ	
3	NC	DQc	28	NC	DQd	53	NC	DQa	78	NC	DQb
4	VDDQ		29	NC	DQd	54	VDDQ		79	NC	DQb
5	Vss		30	NC	NC/DQPd**	55	Vss		80	SA	NC/DQPb**
6	NC	DQc	31	MODE		56	NC	DQa	81	SA	
7	NC	DQc	32	SA		57	NC	DQa	82	SA	
8	DQb	DQc	33	SA		58	DQa		83	ADV#	
9	DQb	DQc	34	SA		59	DQa		84	ADSP#	
10	Vss		35	SA		60	Vss		85	ADSC#	
11	VDDQ		36	SA1		61	VDDQ		86	OE#	
12	DQb	DQc	37	SA0		62	DQa		87	BWE#	
13	DQb	DQc	38	DNU		63	DQa		88	GW#	
14	VDD		39	DNU		64	ZZ		89	CLK	
15	VDD		40	Vss		65	VDD		90	Vss	
16	NC		41	VDD		66	NC		91	VDD	
17	Vss		42	DNU		67	Vss		92	CE2#	
18	DQb	DQd	43	DNU		68	DQa	DQb	93	BWa#	
19	DQb	DQd	44	SA		69	DQa	DQb	94	BWb#	
20	VDDQ		45	SA		70	VDDQ		95	NC	BWc#
21	Vss		46	SA		71	Vss		96	NC	BWd#
22	DQb	DQd	47	SA		72	DQa	DQb	97	CE2	
23	DQb	DQd	48	SA		73	DQa	DQb	98	CE#	
24	DQPb	DQd	49	SA		74	DQPa	DQb	99	SA	
25	NC	DQd	50	NC/SA*		75	NC	DQb	100	SA	

Pin 50 is reserved for address expansion.
No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





* Pin 50 is reserved for address expansion.

** No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

2Mb SYNCBURST™ SRAM

MT58LC128K18C6, MT58LC64K32C6, MT58LC64K36C6; MT58LC128K18F1, MT58LC64K32F1, MT58LC64K36F1

3.3V VDD, 3.3V or 2.5V I/O, Pipelined, Double-Cycle Deselect

FEATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- x18, x32 and x36 options available

OPTIONS

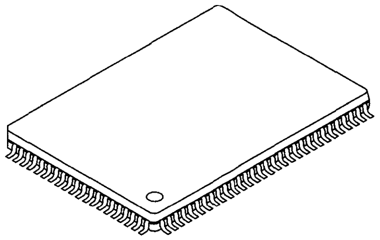
OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
3.5ns/5ns/200 MHz	-5
3.5ns/6ns/166 MHz	-6
3.8ns/6.6ns/150 MHz	-6.6
4.2ns/7.5ns/133 MHz	-7.5
4.5ns/8.5ns/117 MHz	-8.5
5ns/10ns/100 MHz	-10
6ns/11ns/90 MHz	-11*

*-11 is only available with 3.3V I/O

OPTIONS	MARKING
• Configurations	
3.3V I/O	
128K x 18	MT58LC128K18C6
64K x 32	MT58LC64K32C6
64K x 36	MT58LC64K36C6
2.5V I/O	
128K x 18	MT58LC128K18F1
64K x 32	MT58LC64K32F1
64K x 36	MT58LC64K36F1
• Package	
100-pin TQFP	LG

Part Number Example: MT58LC128K18C6LG-7.5

100-Pin TQFP**
(D-1)



**JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

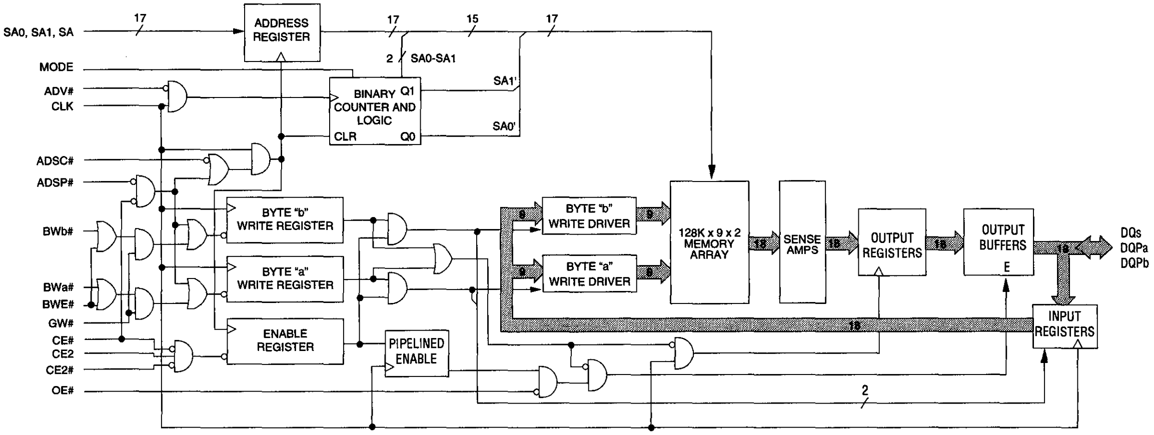
Micron's 2Mb SyncBurst SRAMs integrate a 128K x 18, 64K x 32, or 64K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

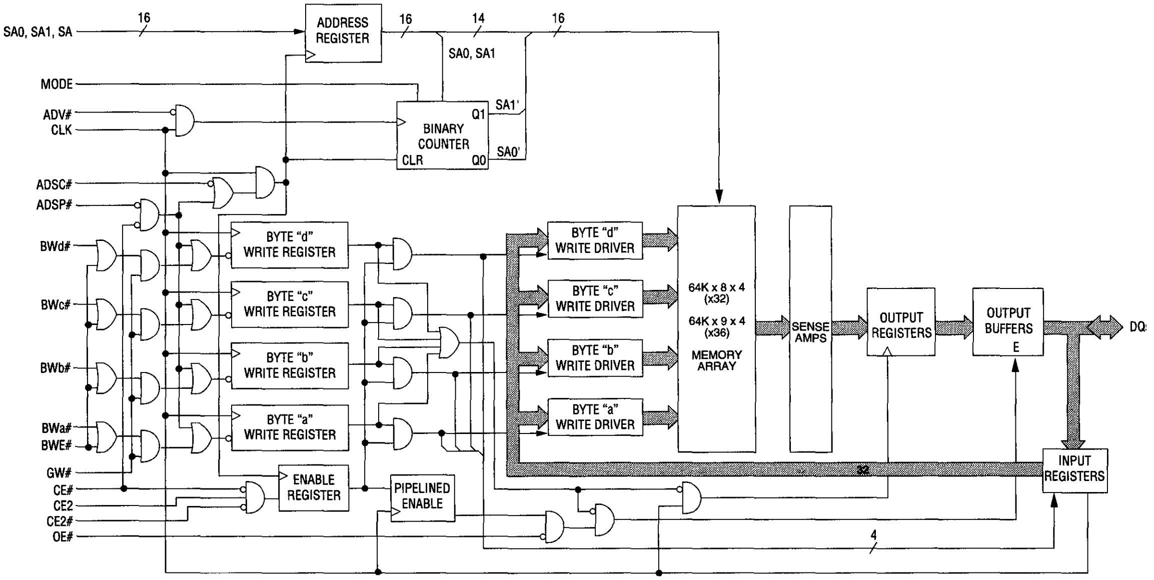
Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written.

FUNCTIONAL BLOCK DIAGRAM
128K x 18



FUNCTIONAL BLOCK DIAGRAM
64K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

GENERAL DESCRIPTION (continued)

During WRITE cycles on the x18 device, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. GW# LOW causes all bytes to be written. Parity pins are only available on the x18 and x36 versions.

The device incorporates an additional pipelined enable register which delays turning off the output buffer an additional cycle when a deselect is executed. This feature allows depth expansion without penalizing system performance.

Micron's 2Mb SyncBurst SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are TTL-compatible. Users can choose either a 3.3V or 2.5V I/O version. The device is ideally suited for Pentium® and PowerPC™ pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

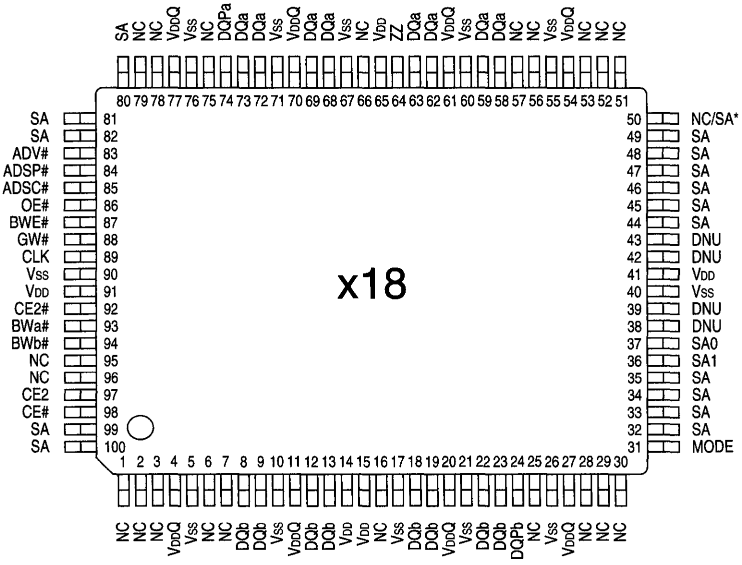
Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

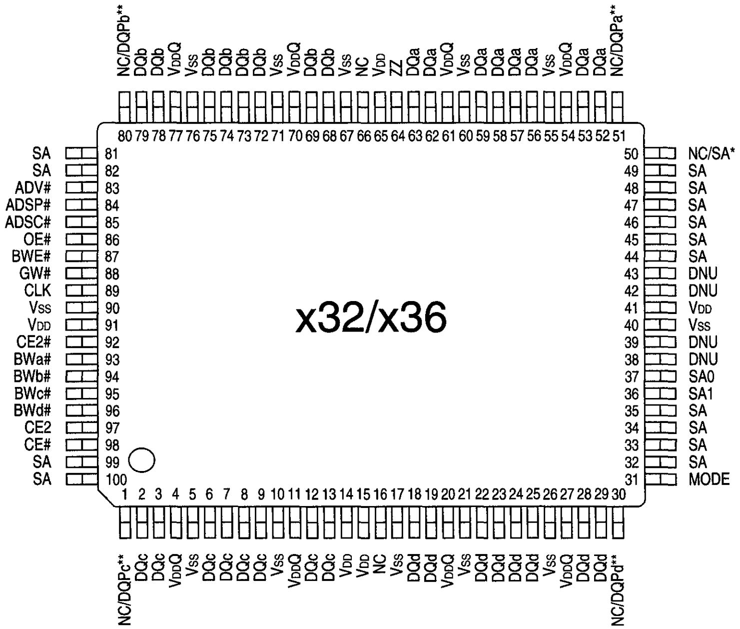
TQFP PIN ASSIGNMENT TABLE

PIN #	x18	x32/x36
1	NC	NC/DQPc**
2	NC	DQc
3	NC	DQc
4	VDDQ	
5	Vss	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	Vss	
11	VDDQ	
12	DQb	DQc
13	DQb	DQc
14	VDD	
15	VDD	
16	NC	
17	Vss	
18	DQb	DQd
19	DQb	DQd
20	VDDQ	
21	Vss	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd
26	Vss	
27	VDDQ	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd**
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	Vss	
41	VDD	
42	DNU	
43	DNU	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	SA	
50	NC/SA*	
51	NC	NC/DQPa**
52	NC	DQa
53	NC	DQa
54	VDDQ	
55	Vss	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	Vss	
61	VDDQ	
62	DQa	
63	DQa	
64	ZZ	
65	VDD	
66	NC	
67	Vss	
68	DQa	DQb
69	DQa	DQb
70	VDDQ	
71	Vss	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb
76	Vss	
77	VDDQ	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb**
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	Vss	
91	VDD	
92	CE2#	
93	BWa#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

* Pin 50 is reserved for address expansion.
** No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





* Pin 50 is reserved for address expansion.

** No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

ADVANCE

MICRON TECHNOLOGY, INC.

4Mb: 256K x 18, 128K x 32/36
FLOW-THROUGH SYNCBURST SRAM

4Mb SYNCBURST™ SRAM

MT58L256L18F, MT58L128L32F,
MT58L128L36F; MT58L256V18F,
MT58L128V32F, MT58L128V36F

3.3V VDD, 3.3V or 2.5V I/O, Flow-Through

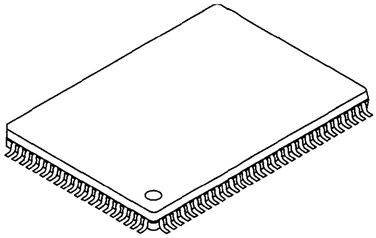
FEATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- 119-bump BGA package
- Low capacitive bus loading
- x18, x32 and x36 versions available

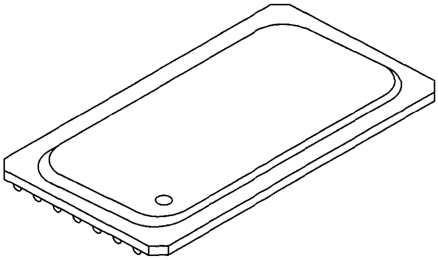
OPTIONS	MARKING
Timing (Access/Cycle/MHz)	
7.5ns/8ns/113 MHz	-7.5
8.5ns/10ns/100 MHz	-8.5
10ns/15ns/66 MHz	-10
Configurations	
3.3V I/O	
256K x 18	MT58L256L18F
128K x 32	MT58L128L32F
128K x 36	MT58L128L36F
2.5V I/O	
256K x 18	MT58L256V18F
128K x 32	MT58L128V32F
128K x 36	MT58L128V36F
Package	
100-pin TQFP	T
119-bump, 14mm x 22mm BGA	B

Part Number Example: MT58L256L18FT-8.5

100-Pin TQFP**
(D-1)



119-Bump BGA
(F-1)



**JEDEC-standard MS-026 BHA (LQFP).

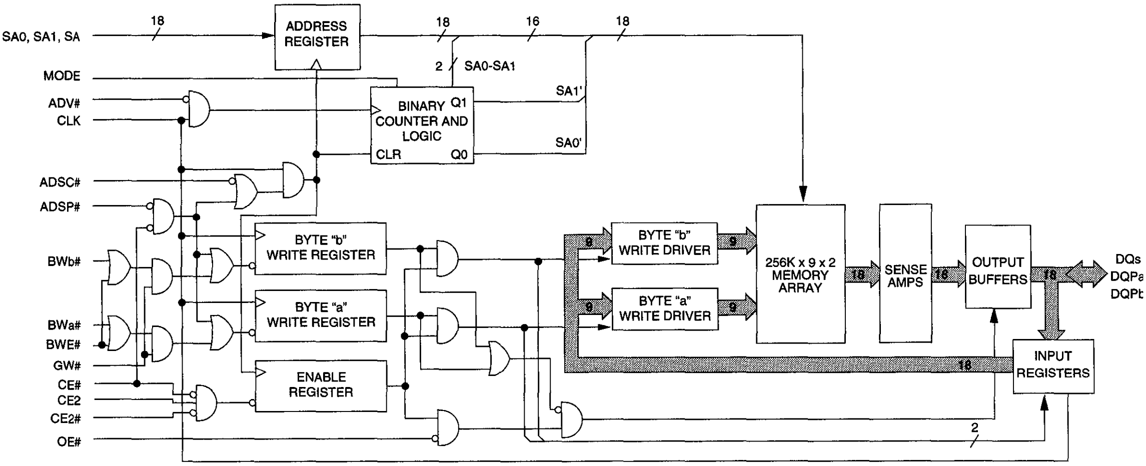
GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-eed, low-power CMOS designs that are fabricated using advanced CMOS process.

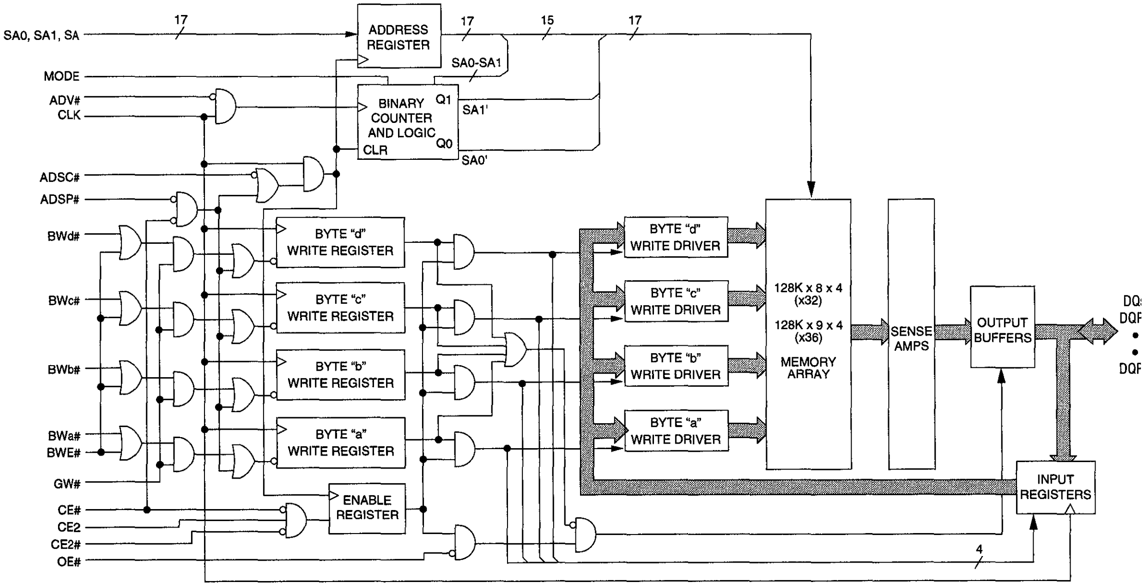
Micron's 4Mb SyncBurst SRAMs integrate a 256K x 18, 8K x 32, or 128K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2#, CE2), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is

FUNCTIONAL BLOCK DIAGRAM
256K x 18



FUNCTIONAL BLOCK DIAGRAM
128K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

GENERAL DESCRIPTION (continued)

also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

Micron's 4Mb SyncBurst SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are TTL-compatible. Users can choose either a 2.5V or 3.3V I/O version. The device is ideally suited for 486, Pentium®, 680x0 and PowerPC™ systems and those systems that benefit from a wide synchronous data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

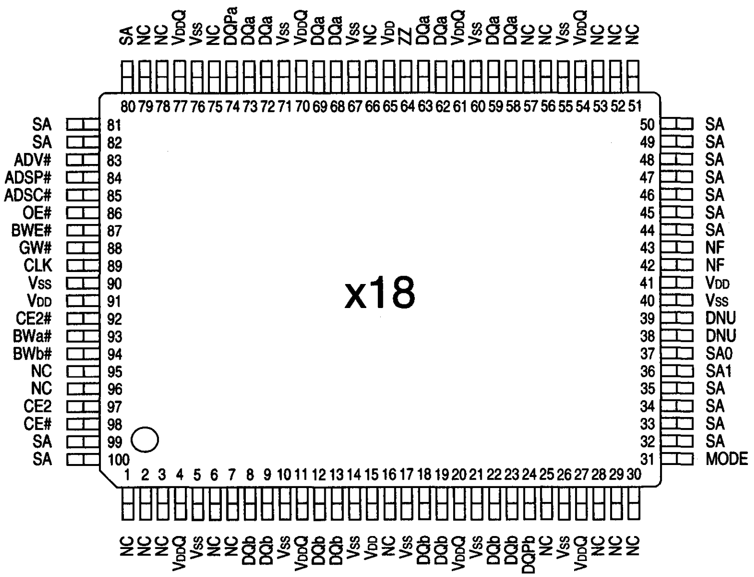
Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

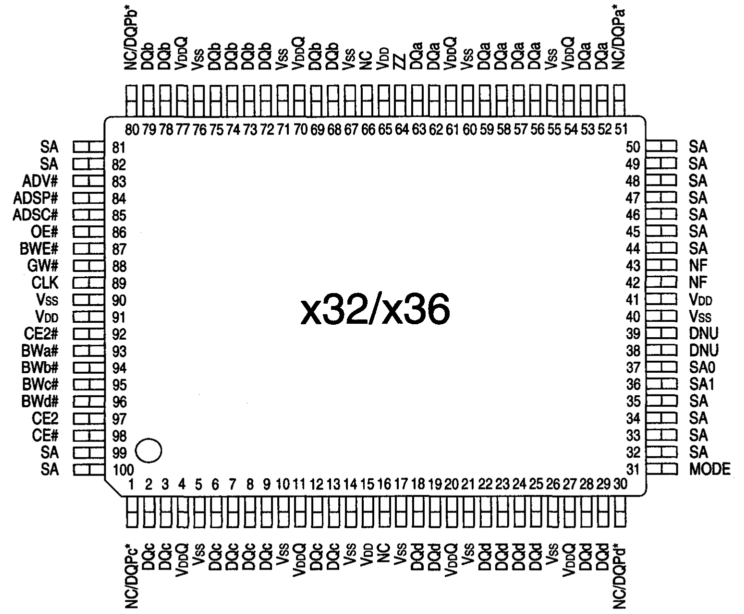
TQFP PIN ASSIGNMENT TABLE

PIN #	x18	x32/x36
1	NC	NC/DQPc*
2	NC	DQc
3	NC	DQc
4	VDDQ	
5	VSS	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	VSS	
11	VDDQ	
12	DQb	DQc
13	DQb	DQc
14	VSS	
15	VDD	
16	NC	
17	VSS	
18	DQb	DQd
19	DQb	DQd
20	VDDQ	
21	VSS	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd
26	VSS	
27	VDDQ	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd*
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	VSS	
41	VDD	
42	NF	
43	NF	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	SA	
50	SA	
51	NC	NC/DQPa*
52	NC	DQa
53	NC	DQa
54	VDDQ	
55	VSS	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	VSS	
61	VDDQ	
62	DQa	
63	DQa	
64	ZZ	
65	VDD	
66	NC	
67	VSS	
68	DQa	DQb
69	DQa	DQb
70	VDDQ	
71	VSS	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb
76	VSS	
77	VDDQ	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb*
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	VSS	
91	VDD	
92	CE2#	
93	BWa#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

4Mb SYNCBURST™ SRAM

MT58L256L18P, MT58L128L32P,
MT58L128L36P; MT58L256V18P,
MT58L128V32P, MT58L128V36P

3.3V VDD, 3.3V or 2.5V I/O, Pipelined, Single-Cycle Deselect

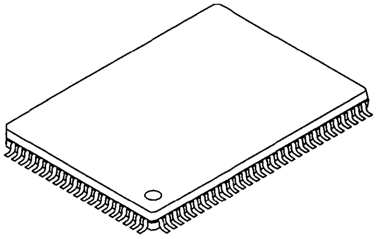
FEATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Single-cycle deselect (Pentium® BSRAM-compatible)
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- 119-bump BGA package
- Low capacitive bus loading
- x18, x32 and x36 versions available

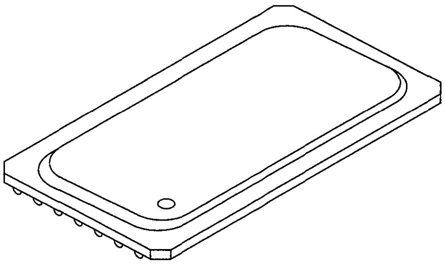
OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
2.9ns/4.4ns/227 MHz	-4.4
3.1ns/5ns/200 MHz	-5
3.5ns/6ns/166 MHz	-6
4ns/7.5ns/133 MHz	-7.5
5ns/10ns/100 MHz	-10
• Configurations	
3.3V I/O	
256K x 18	MT58L256L18P
128K x 32	MT58L128L32P
128K x 36	MT58L128L36P
2.5V I/O	
256K x 18	MT58L256V18P
128K x 32	MT58L128V32P
128K x 36	MT58L128V36P
• Packages	
100-pin TQFP	T
119-bump, 14mm x 22mm BGA	B

- Part Number Example: MT58L256L18PT-6

100-Pin TQFP*
(D-1)



119-Bump BGA
(F-1)



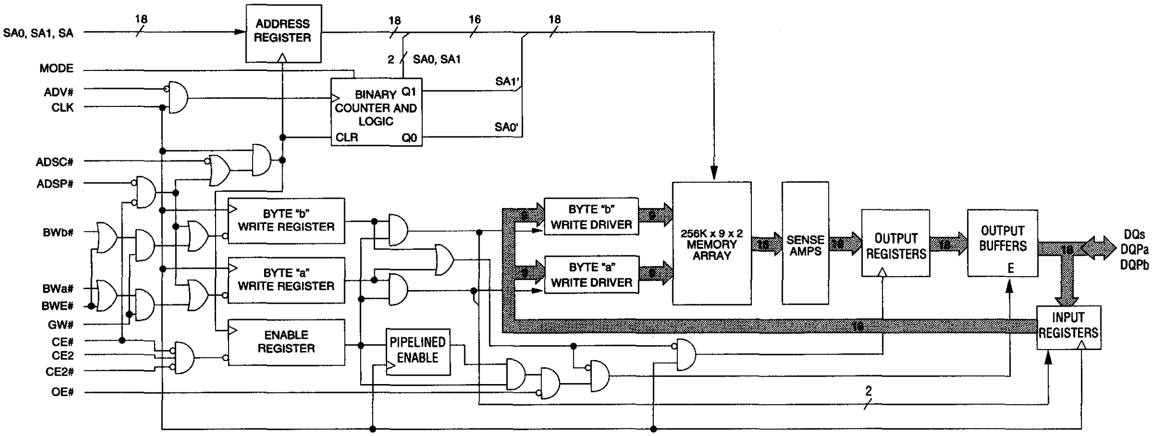
*JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

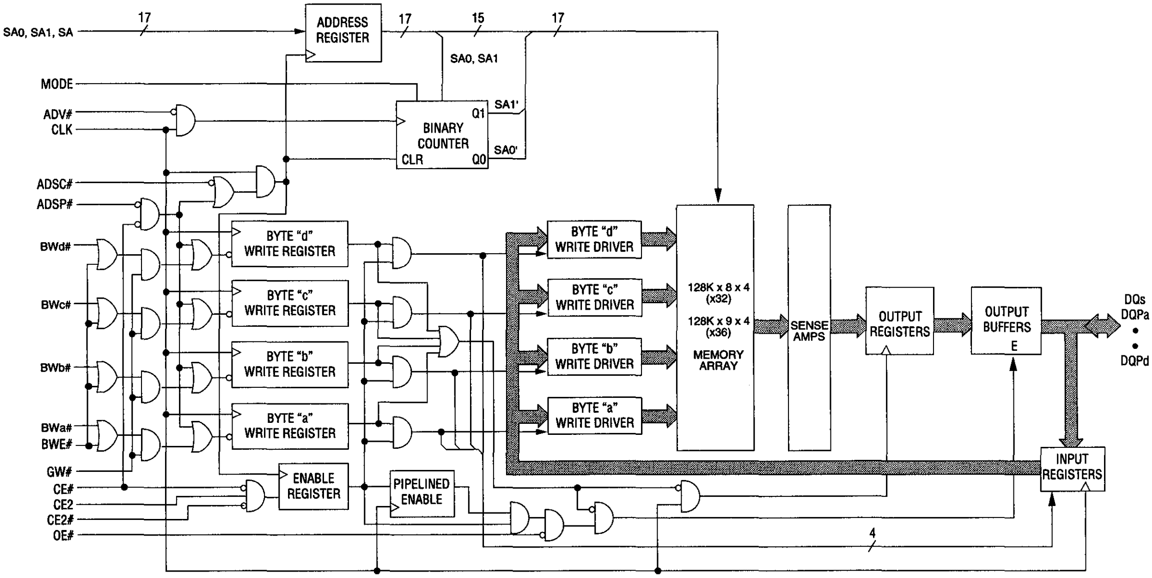
The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

Micron's 4Mb SyncBurst SRAMs integrate a 256K x 18, 128K x 32, or 128K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs

FUNCTIONAL BLOCK DIAGRAM
256K x 18



FUNCTIONAL BLOCK DIAGRAM
128K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

GENERAL DESCRIPTION (continued)

(ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb; BWc# controls DQc's and DQPc; BWd# controls DQd's and DQPd. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

This device incorporates a single-cycle deselect feature during READ cycles. If the device is immediately deselected after a READ cycle, the output bus goes to a High-Z state ^{t}KQHZ nanoseconds after the rising edge of clock.

Micron's 4Mb SyncBurst SRAMs operate from a +3.3V V_{DD} power supply, and all inputs and outputs are TTL-compatible. Users can choose either a 3.3V or 2.5V I/O version. The device is ideally suited for Pentium and PowerPC™ pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

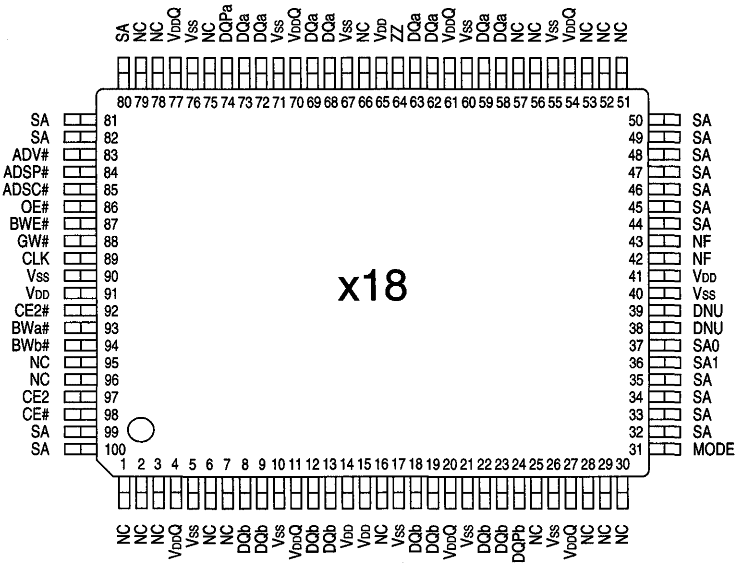
Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

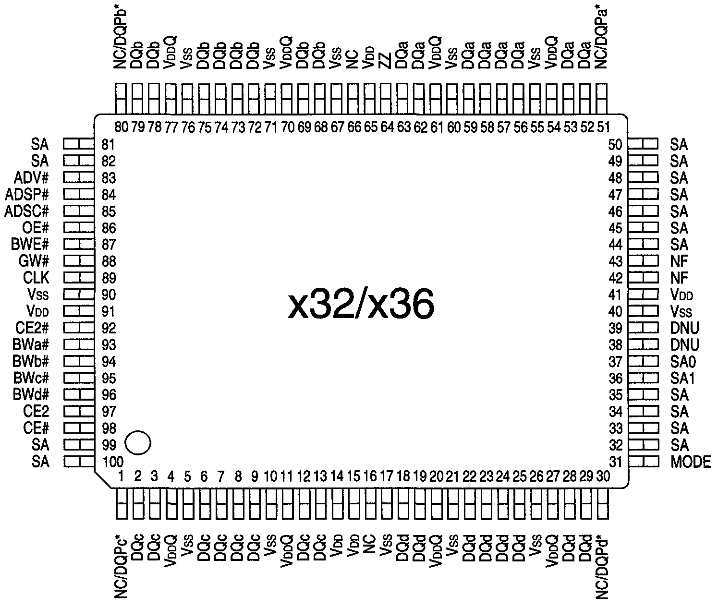
TQFP PIN ASSIGNMENT TABLE

PIN #	x18	x32/x36
1	NC	NC/DQPc*
2	NC	DQc
3	NC	DQc
4	$V_{DD}Q$	
5	V_{SS}	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	V_{SS}	
11	$V_{DD}Q$	
12	DQb	DQc
13	DQb	DQc
14	V_{DD}	
15	V_{DD}	
16	NC	
17	V_{SS}	
18	DQb	DQd
19	DQb	DQd
20	$V_{DD}Q$	
21	V_{SS}	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd
26	V_{SS}	
27	$V_{DD}Q$	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd*
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	V_{SS}	
41	V_{DD}	
42	NF	
43	NF	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	SA	
50	SA	
51	NC	NC/DQPa*
52	NC	DQa
53	NC	DQa
54	$V_{DD}Q$	
55	V_{SS}	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	V_{SS}	
61	$V_{DD}Q$	
62	DQa	
63	DQa	
64	ZZ	
65	V_{DD}	
66	NC	
67	V_{SS}	
68	DQa	DQb
69	DQa	DQb
70	$V_{DD}Q$	
71	V_{SS}	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb
76	V_{SS}	
77	$V_{DD}Q$	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb*
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	V_{SS}	
91	V_{DD}	
92	CE2#	
93	BWa#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

ADVANCE

MICRON TECHNOLOGY, INC.

4Mb: 256K x 18, 128K x 32/36
3.3V I/O PIPELINED, DCD SYNCBURST SRAM

4Mb SYNCBURST™ SRAM

MT58L256L18D, MT58L128L32D, MT58L128L36D

3.3V VDD, 3.3V I/O, Pipelined, Double-Cycle Deselect

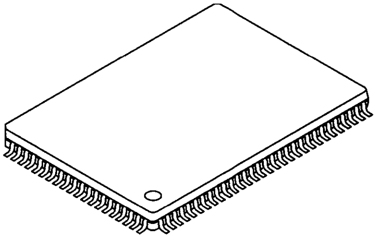
FEATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (VDD)
- Separate +3.3V isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- 119-bump BGA package
- Low capacitive bus loading
- x18, x32 and x36 versions available

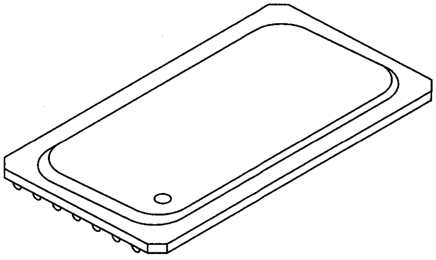
OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
3.5ns/6ns/166 MHz	-6
4.2ns/7.5ns/133 MHz	-7.5
5ns/10ns/100 MHz	-10
• Configurations	
256K x 18	MT58L256L18D
128K x 32	MT58L128L32D
128K x 36	MT58L128L36D
• Packages	
100-pin TQFP	T
119-bump, 14mm x 22mm BGA	B

- Part Number Example: MT58L256L18DT-6

100-Pin TQFP*
(D-1)



119-Bump BGA
(F-1)



*JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

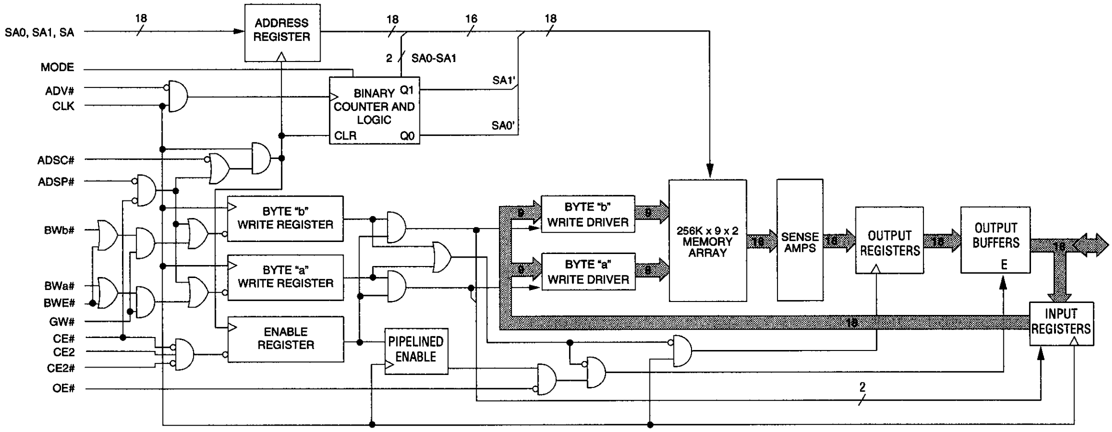
The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

Micron's 4Mb SyncBurst SRAMs integrate a 256K x 18, 128K x 32, or 128K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

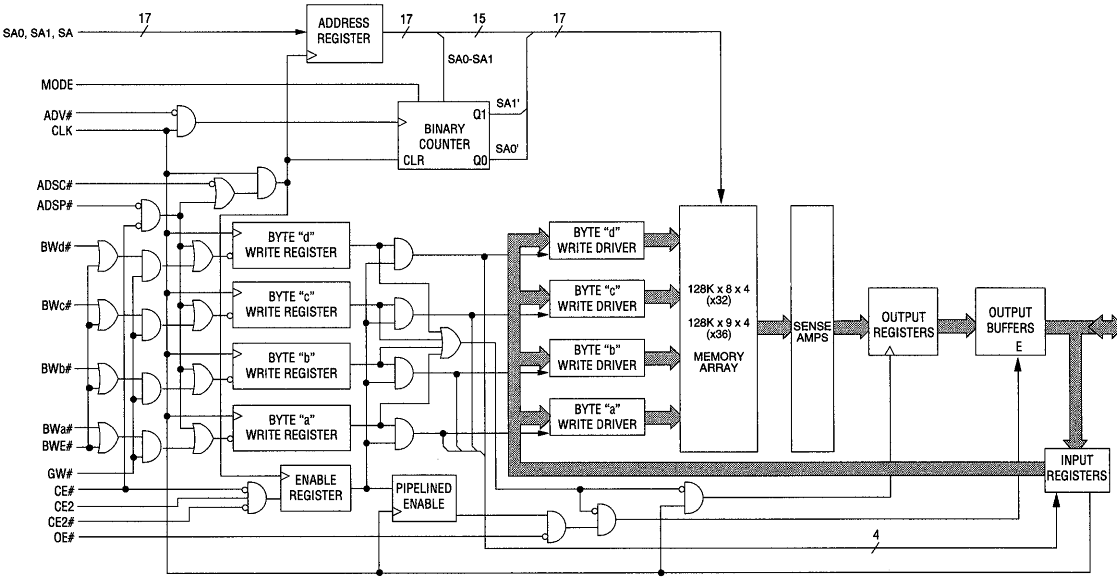
Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV#).

FUNCTIONAL BLOCK DIAGRAM
256K x 18



FUNCTIONAL BLOCK DIAGRAM
128K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

GENERAL DESCRIPTION (continued)

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb; BWc# controls DQc's and DQPc; BWd# controls DQd's and DQPd. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

This device incorporates an additional pipelined enable register which delays turning off the output buffer an additional cycle when a deselect is executed. This feature allows depth expansion without penalizing system performance.

Micron's 4Mb SyncBurst SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are TTL-compatible. The device is ideally suited for Pentium® and PowerPC™ pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

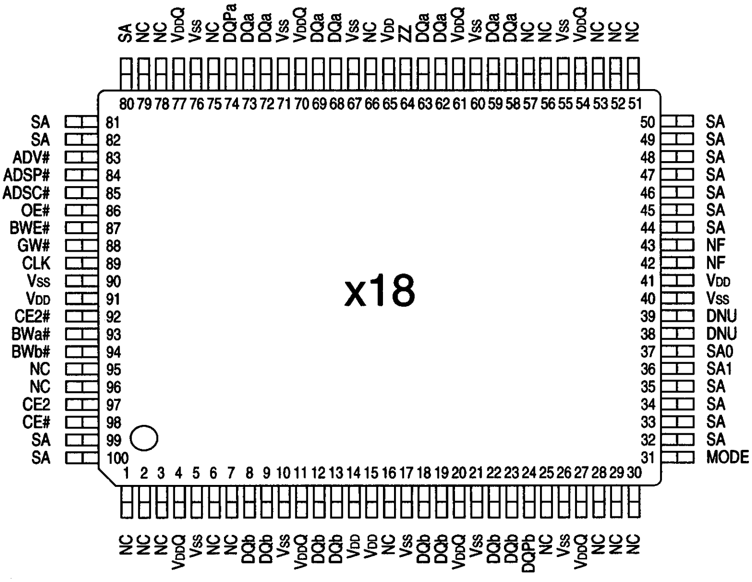
Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

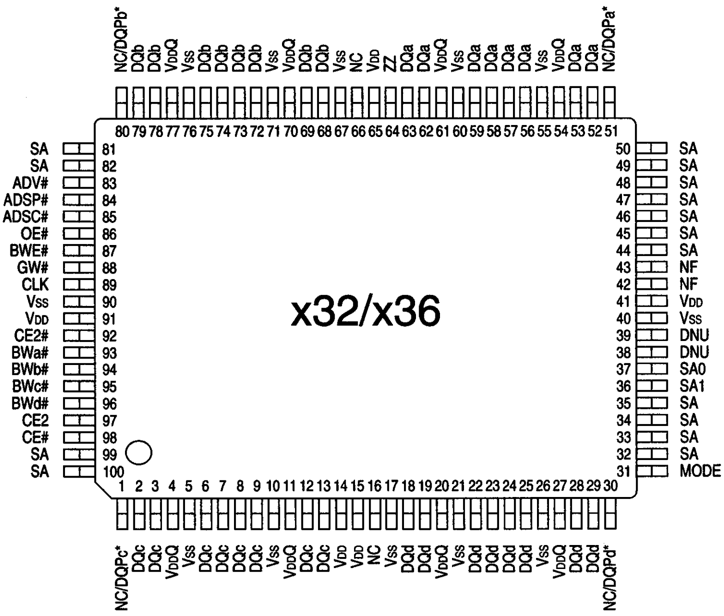
TQFP PIN ASSIGNMENT TABLE

PIN #	x18	x32/x36
1	NC	NC/DQPc*
2	NC	DQc
3	NC	DQc
4	VDDQ	
5	VSS	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	VSS	
11	VDDQ	
12	DQb	DQc
13	DQb	DQc
14	VDD	
15	VDD	
16	NC	
17	VSS	
18	DQb	DQd
19	DQb	DQd
20	VDDQ	
21	VSS	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd
26	VSS	
27	VDDQ	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd*
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	VSS	
41	VDD	
42	NF	
43	NF	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	SA	
50	SA	
51	NC	NC/DQPa*
52	NC	DQa
53	NC	DQa
54	VDDQ	
55	VSS	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	VSS	
61	VDDQ	
62	DQa	
63	DQa	
64	ZZ	
65	VDD	
66	NC	
67	VSS	
68	DQa	DQb
69	DQa	DQb
70	VDDQ	
71	VSS	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb
76	VSS	
77	VDDQ	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb*
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	VSS	
91	VDD	
92	CE2#	
93	BWa#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(D-1)





*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

Micron Technology, Inc., reserves the right to change products or specifications without notice.

8Mb SYNCBURST™ SRAM

MT58L512L18F, MT58L256L32F,
MT58L256L36F; MT58L512V18F,
MT58L256V32F, MT58L256V36F

3.3V VDD, 3.3V or 2.5V I/O, Flow-Through

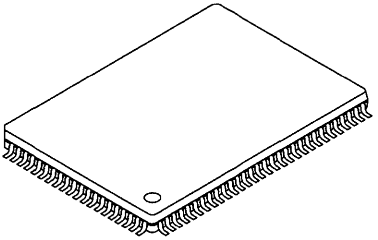
FEATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- 119-bump BGA package
- Low capacitive bus loading
- x18, x32 and x36 versions available

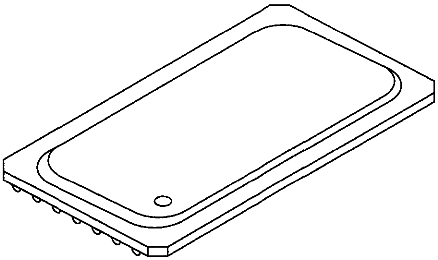
OPTIONS	MARKING
Timing (Access/Cycle/MHz)	
6.8ns/8ns/125 MHz	-6.8
7.5ns/8.8ns/113 MHz	-7.5
8.5ns/10ns/100 MHz	-8.5
10ns/15ns/66 MHz	-10
Configurations	
3.3V I/O	
512K x 18	MT58L512L18F
256K x 32	MT58L256L32F
256K x 36	MT58L256L36F
2.5V I/O	
512K x 18	MT58L512V18F
256K x 32	MT58L256V32F
256K x 36	MT58L256V36F
Packages	
100-pin TQFP (2-chip enable)	T
100-pin TQFP (3-chip enable)	S
119-bump, 14mm x 22mm BGA	B

- Part Number Example: MT58L256V36FT-10

100-Pin TQFP*
(D-1)



119-Bump BGA
(F-1)



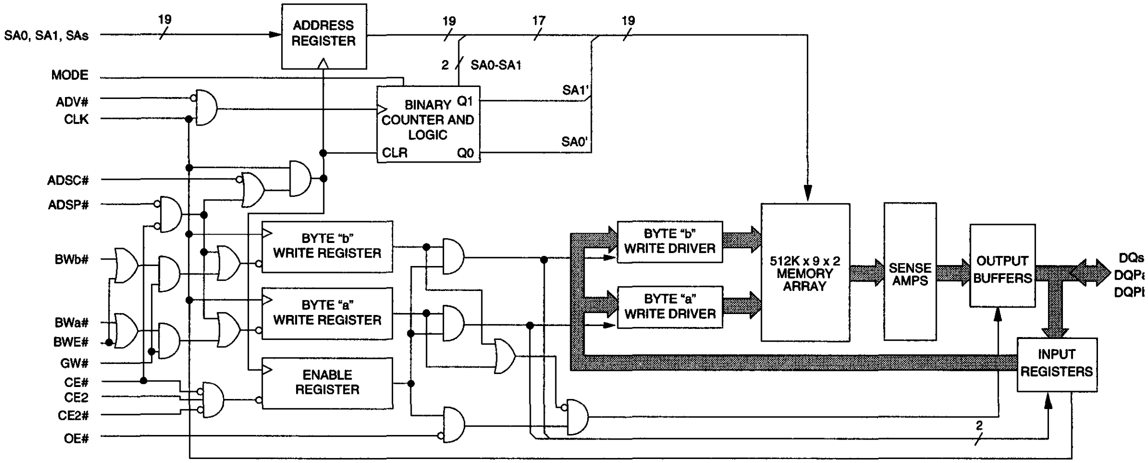
*JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

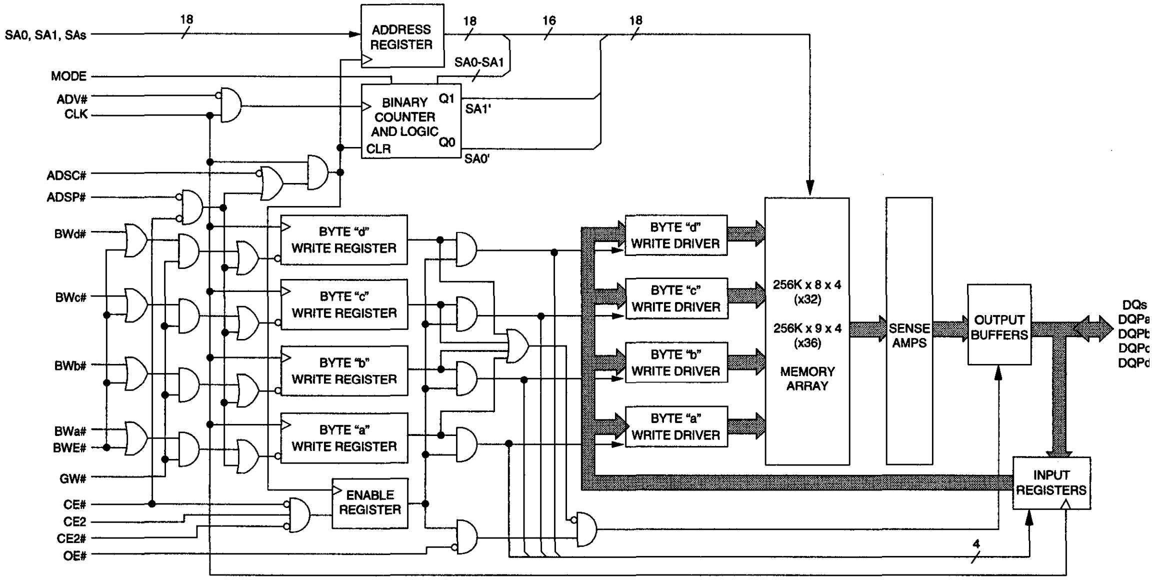
The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

Micron's 8Mb SyncBurst SRAMs integrate a 512K x 18, 256K x 32, or 256K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2#, CE2), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#). Note that CE2# is not available on the T Version.

FUNCTIONAL BLOCK DIAGRAM
512K x 18



FUNCTIONAL BLOCK DIAGRAM
256K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

ENERAL DESCRIPTION (continued)

Asynchronous inputs include the output enable (OE#), lock (CLK) and snooze enable (ZZ). There is also a burst node input (MODE) that selects between interleaved and inear burst modes. The data-out (Q), enabled by OE#, is lso asynchronous. WRITE cycles can be from one to two ytes wide (x18) or from one to four bytes wide (x32/x36), s controlled by the write control inputs.

Burst operation can be initiated with either address status rocessor (ADSP#) or address status controller (ADSC#) nputs. Subsequent burst addresses can be internally enerated as controlled by the burst advance input (ADV#).

Address and write control are registered on-chip to implify WRITE cycles. This allows self-timed WRITE cycles. ndividual byte enables allow individual bytes to be vritten. During WRITE cycles on the x18 device, BWa# ontrols DQa's and DQPa; BWb# controls DQb's and DQPb. uring WRITE cycles on the x32 and x36 devices, BWa# ontrols DQa's and DQPa; BWb# controls DQb's and DQPb; Wc# controls DQc's and DQPc; BWd# controls DQd's and DQPd. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

Micron's 8Mb SyncBurst SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are TTL-compatible. Users can choose either a 3.3V or 2.5V I/O version. The device is ideally suited for 486, Pentium®, 680x0 and PowerPC™ systems and those systems that benefit from a wide synchronous data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

TQFP Pinouts

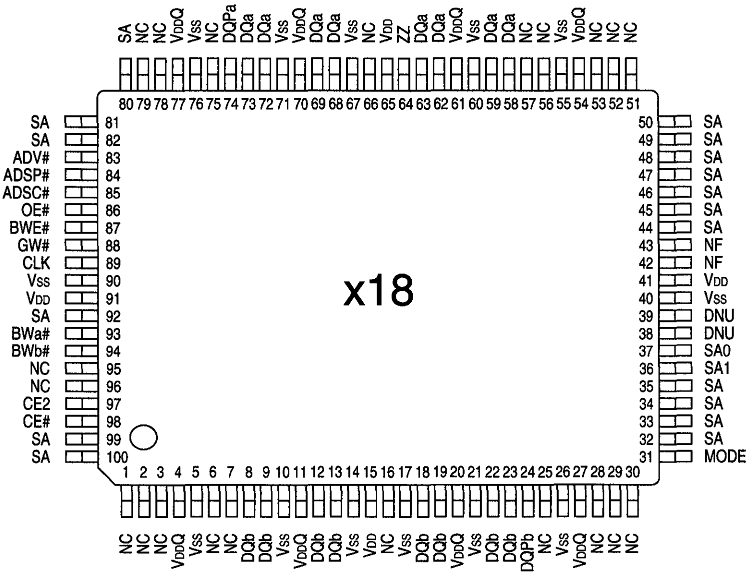
At the time of the writing of this data sheet, there are two pinouts in the industry. Micron will support both pinouts for this part.

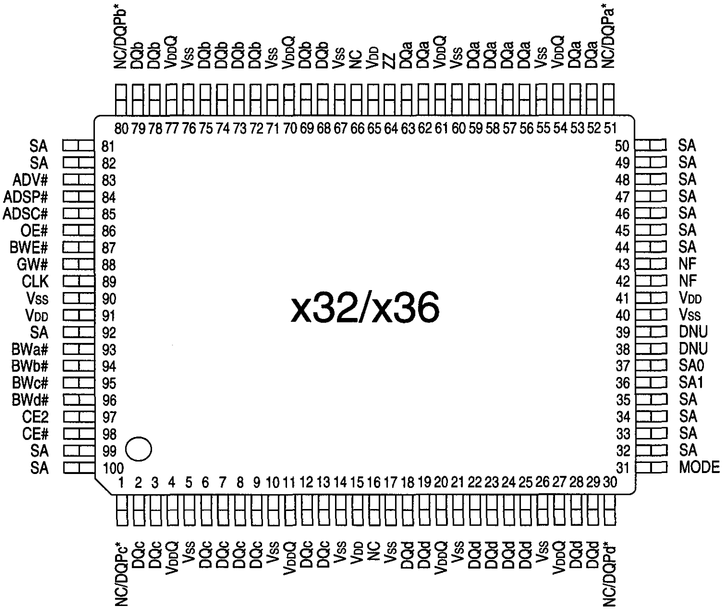
QFP PIN ASSIGNMENT TABLE

PIN #	x18	x32/x36
1	NC	NC/DQPc*
2	NC	DQc
3	NC	DQc
4	VDDQ	
5	Vss	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	Vss	
11	VDDQ	
12	DQb	DQc
13	DQb	DQc
14	Vss	
15	VDD	
16	NC	
17	Vss	
18	DQb	DQd
19	DQb	DQd
20	VDDQ	
21	Vss	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd
26	Vss	
27	VDDQ	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd*
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	Vss	
41	VDD	
42	NF	
43	NF (T Version) SA (S Version)	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	SA	
50	SA	
51	NC	NC/DQPa*
52	NC	DQa
53	NC	DQa
54	VDDQ	
55	Vss	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	Vss	
61	VDDQ	
62	DQa	
63	DQa	
64	ZZ	
65	VDD	
66	NC	
67	Vss	
68	DQa	DQb
69	DQa	DQb
70	VDDQ	
71	Vss	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb
76	Vss	
77	VDDQ	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb*
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	Vss	
91	VDD	
92	SA (T Version) CE2# (S Version)	
93	BWa#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP, 2-Chip Enable,
T Version
(D-1)

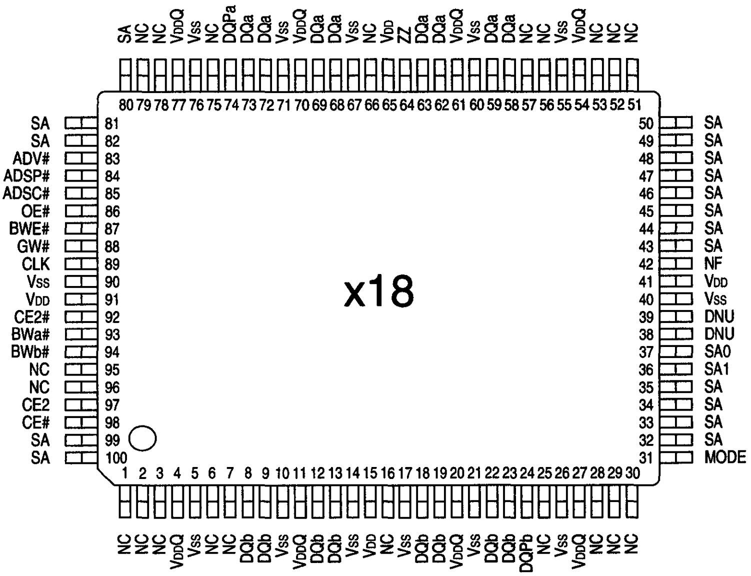


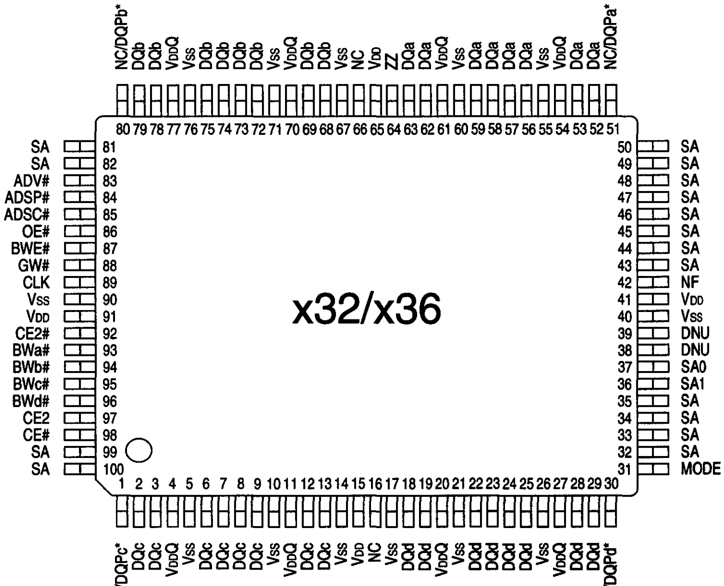


*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP, 3-Chip Enable,
S Version

(D-1)





*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

8Mb SYNCBURST™ SRAM

MT58L512L18P, MT58L256L32P,
MT58L256L36P; MT58L512V18P,
MT58L256V32P, MT58L256V36P

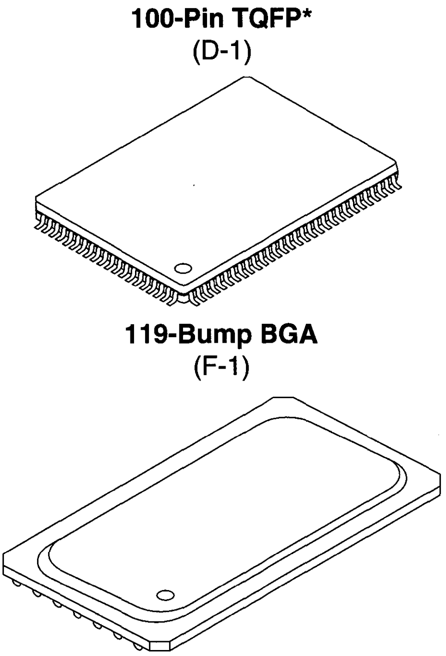
3.3V VDD, 3.3V or 2.5V I/O, Pipelined, Single-Cycle Deselect

FEATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Single-cycle deselect (Pentium® BSRAM-compatible)
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- 119-bump BGA package
- Low capacitive bus loading
- x18, x32 and x36 versions available

OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
2.9ns/4.4ns/227 MHz	-4.4
3.1ns/5ns/200 MHz	-5
3.5ns/6ns/166 MHz	-6
4ns/7.5ns/133 MHz	-7.5
5ns/10ns/100 MHz	-10
• Configurations	
3.3V I/O	
512K x 18	MT58L512L18P
256K x 32	MT58L256L32P
256K x 36	MT58L256L36P
2.5V I/O	
512K x 18	MT58L512V18P
256K x 32	MT58L256V32P
256K x 36	MT58L256V36P
• Packages	
100-pin TQFP (2-chip enable)	T
100-pin TQFP (3-chip enable)	S
119-bump, 14mm x 22mm BGA	B

- Part Number Example: MT58L512L18PT-6



100-Pin TQFP*
(D-1)

119-Bump BGA
(F-1)

*JEDEC-standard MS-026 BHA (LQFP).

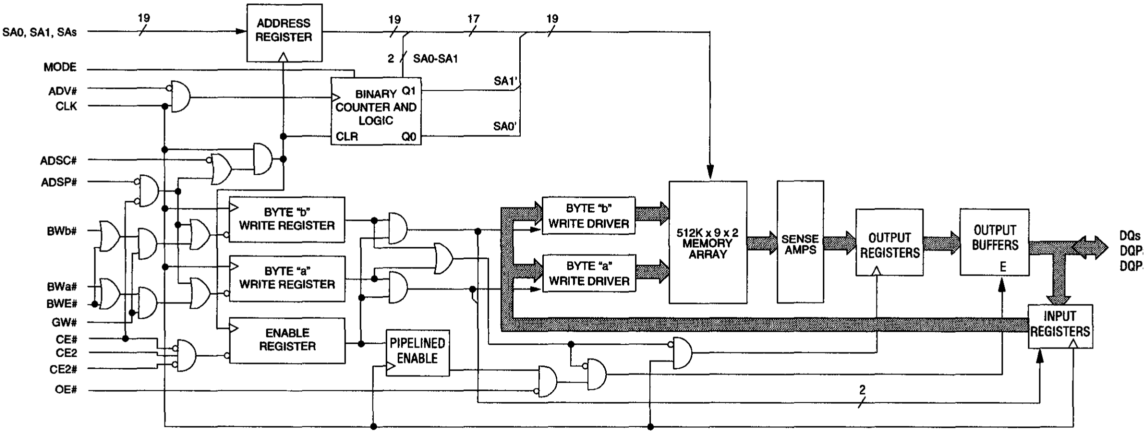
GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

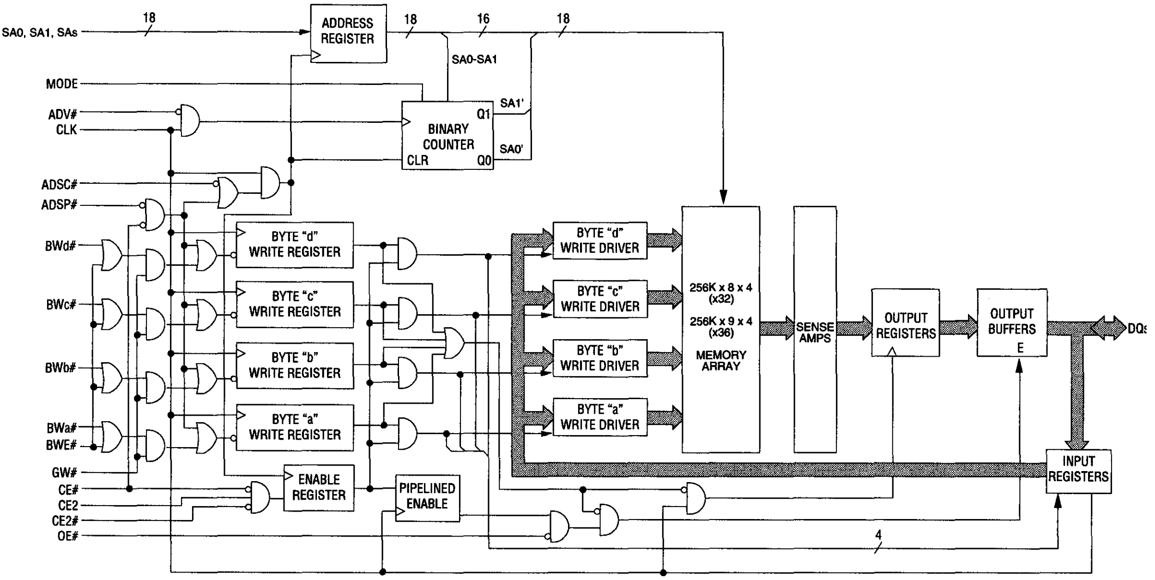
Micron's 8Mb SyncBurst SRAMs integrate a 512K x 18, 256K x 32, or 256K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#). Note that CE2# is not available on the T Version.

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst

FUNCTIONAL BLOCK DIAGRAM
512K x 18



FUNCTIONAL BLOCK DIAGRAM
256K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

GENERAL DESCRIPTION (continued)

mode input (MODE) that selects between interleaved and inear burst modes. The data-out (Q), enabled by OE#, is lso asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), s controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) nputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV#).

Address and write control are registered on-chip to implify WRITE cycles. This allows self-timed WRITE cycles. ndividual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb; BWc# controls DQc's and DQPc; BWd# controls DQd's and DQPd. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

This device incorporates a single-cycle deselect feature during READ cycles. If the device is immediately deselected after a READ cycle, the output bus goes to a High-Z state ^{t}KQHZ nanoseconds after the rising edge of clock.

Micron's 8Mb SyncBurst SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are TTL-compatible. Users can choose either a 3.3V or 2.5V I/O version. The device is ideally suited for Pentium and PowerPC™ pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

TQFP Pinouts

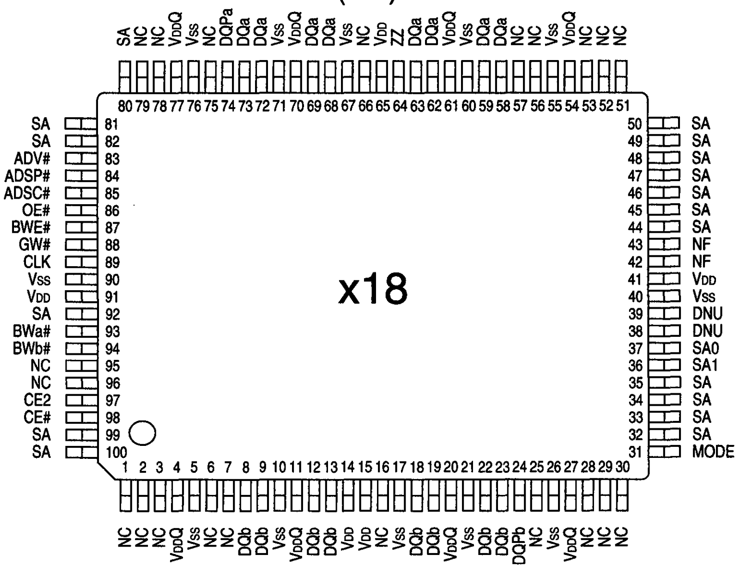
At the time of the writing of this data sheet, there are two pinouts in the industry. Micron will support both pinouts for this part.

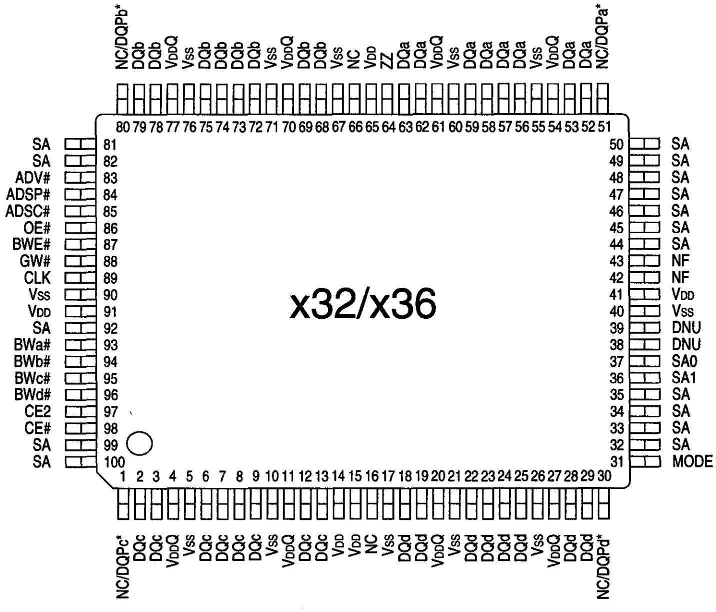
TQFP PIN ASSIGNMENT TABLE

PIN #	x18	x32/x36
1	NC	NC/DQPc*
2	NC	DQc
3	NC	DQc
4	VDDQ	
5	Vss	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	Vss	
11	VDDQ	
12	DQb	DQc
13	DQb	DQc
14	VDD	
15	VDD	
16	NC	
17	Vss	
18	DQb	DQd
19	DQb	DQd
20	VDDQ	
21	Vss	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd
26	Vss	
27	VDDQ	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd*
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	Vss	
41	VDD	
42	NF	
43	NF (T Version) SA (S Version)	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	SA	
50	SA	
51	NC	NC/DQPa*
52	NC	DQa
53	NC	DQa
54	VDDQ	
55	Vss	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	Vss	
61	VDDQ	
62	DQa	
63	DQa	
64	ZZ	
65	VDD	
66	NC	
67	Vss	
68	DQa	DQb
69	DQa	DQb
70	VDDQ	
71	Vss	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb
76	Vss	
77	VDDQ	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb*
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	Vss	
91	VDD	
92	SA (T Version) CE2# (S Version)	
93	BWa#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

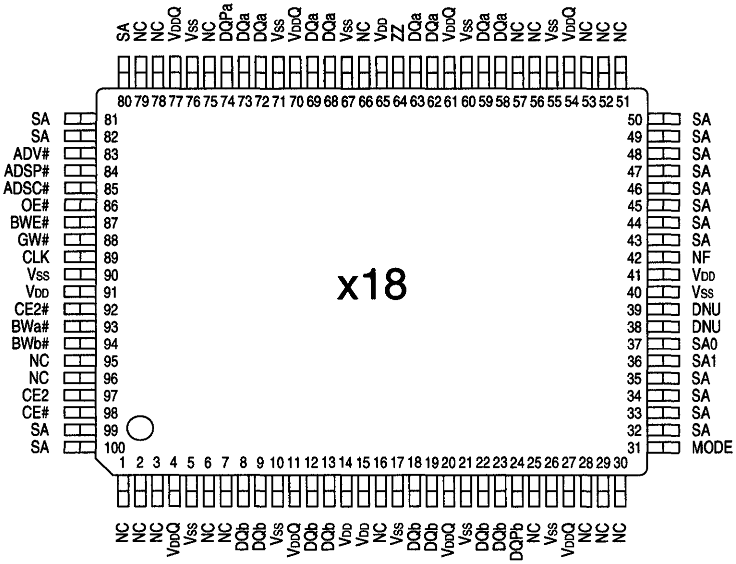
PIN ASSIGNMENT (Top View)
100-Pin TQFP, 2-Chip Enable, T Version
(D-1)

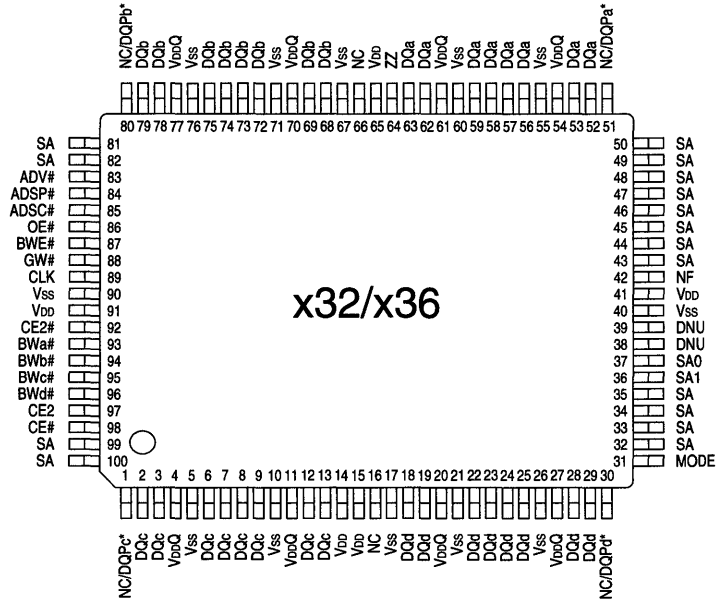




*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP, 3-Chip Enable,
S Version
(D-1)





*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

3Mb SYNCBURST™ SRAM

MT58L512L18D, MT58L256L32D, MT58L256L36D

3.3V VDD, 3.3V I/O, Pipelined, Double-Cycle Deselect

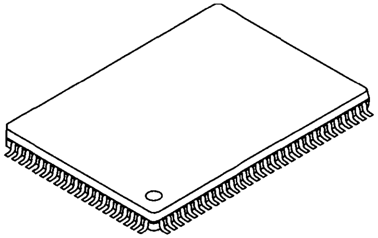
'EATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (VDD)
- Separate +3.3V isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- 119-bump BGA package
- Low capacitive bus loading
- x18, x32 and x36 versions available

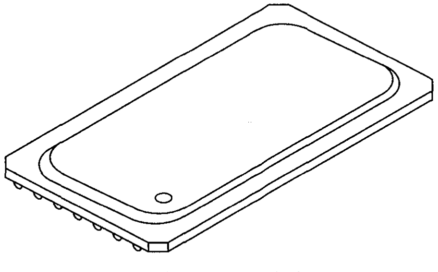
)PTIONS	MARKING
Timing (Access/Cycle/MHz)	
3.5ns/6ns/166 MHz	-6
4ns/7.5ns/133 MHz	-7.5
5ns/10ns/100 MHz	-10
Configurations	
512K x 18	MT58L512L18D
256K x 32	MT58L256L32D
256K x 36	MT58L256L36D
Packages	
100-pin TQFP (2-chip enable)	T
100-pin TQFP (3-chip enable)	S
119-bump, 14mm x 22mm BGA	B

- Part Number Example: MT58L512L18DT-7.5

100-Pin TQFP*
(D-1)



119-Bump BGA
(F-1)



*JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-peed, low-power CMOS designs that are fabricated using in advanced CMOS process.

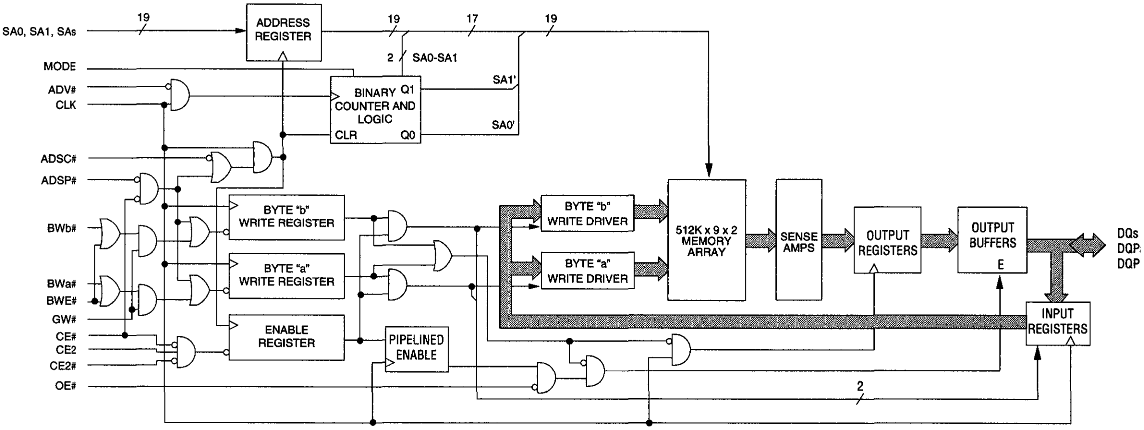
Micron's 8Mb SyncBurst SRAMs integrate a 512K x 18, 56K x 32, or 256K x 36 SRAM core with advanced ynchronous peripheral circuitry and a 2-bit burst counter. ll synchronous inputs pass through registers controlled y a positive-edge-triggered single-clock input (CLK). The ynchronous inputs include all addresses, all data inputs, ctive LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#). Note that CE2# is not available on the T Version.

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

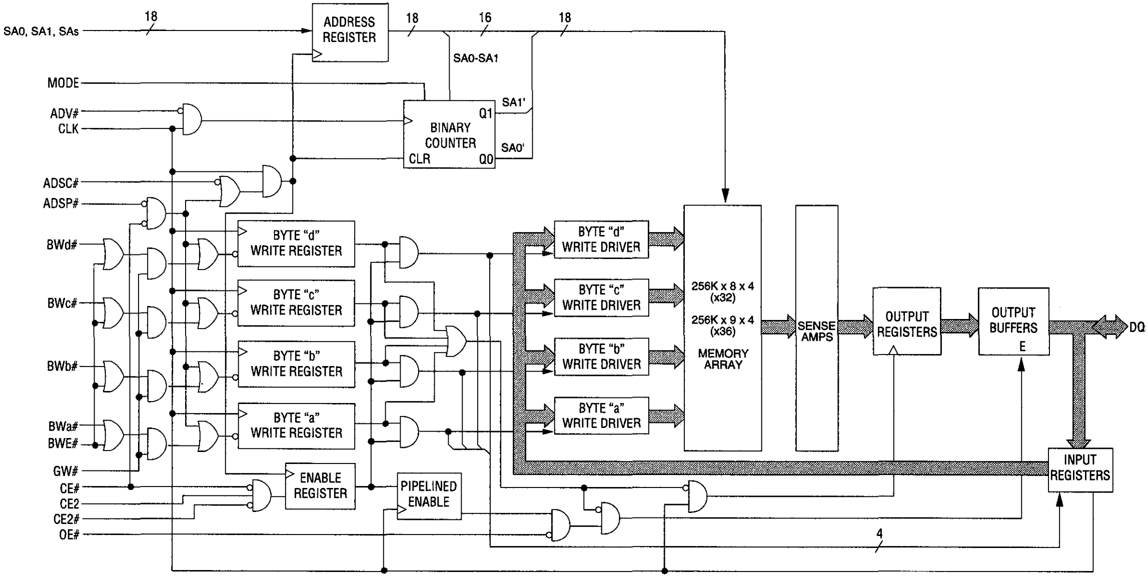
Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written.

FUNCTIONAL BLOCK DIAGRAM
512K x 18



FUNCTIONAL BLOCK DIAGRAM
256K x 32/36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

ENERAL DESCRIPTION (continued)

uring WRITE cycles on the x18 device, BWa# controls Qa's and DQPa; BWb# controls DQb's and DQPb. During RITE cycles on the x32 and x36 devices, BWa# controls Qa's and DQPa; BWb# controls DQb's and DQPb; BWc# ontrols DQc's and DQPc; BWd# controls DQd's and DQPd. W# LOW causes all bytes to be written. Parity bits are only vailable on the x18 and x36 versions.

This device incorporates an additional pipelined enable egister which delays turning off the output buffer an dditional cycle when a deselect is executed. This feature llows depth expansion without penalizing system erformance.

Micron's 8Mb SyncBurst SRAMs operate from a +3.3V DD power supply, and all inputs and outputs are TTL-compatible. The device is ideally suited for Pentium® and PowerPC™ pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

Please refer to the Micron Web site (www.micron.com/mti/msp/html/sramprod.html) for the latest full-length data sheet.

TQFP Pinouts

At the time of the writing of this data sheet, there are two pinouts in the industry. Micron will support both pinouts for this part.

QFP PIN ASSIGNMENT TABLE

IN #	x18	x32/x36
1	NC	NC/DQPc*
2	NC	DQc
3	NC	DQc
4	V$_{DD}$Q	
5	V$_{SS}$	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	V$_{SS}$	
11	V$_{DD}$Q	
12	DQb	DQc
13	DQb	DQc
14	V$_{DD}$	
15	V$_{DD}$	
16	NC	
17	V$_{SS}$	
18	DQb	DQd
19	DQb	DQd
20	V$_{DD}$Q	
21	V$_{SS}$	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd

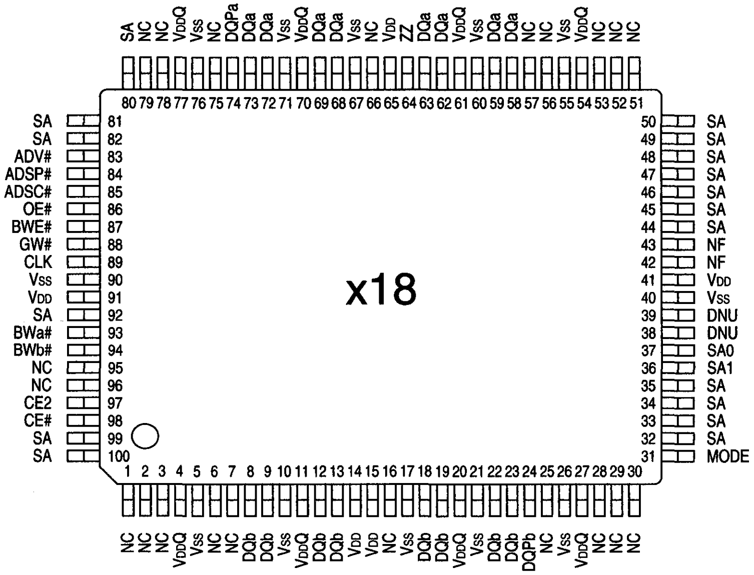
PIN #	x18	x32/x36
26	V$_{SS}$	
27	V$_{DD}$Q	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd*
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	V$_{SS}$	
41	V$_{DD}$	
42	NF	
43	NF (T Version) SA (S Version)	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	SA	
50	SA	

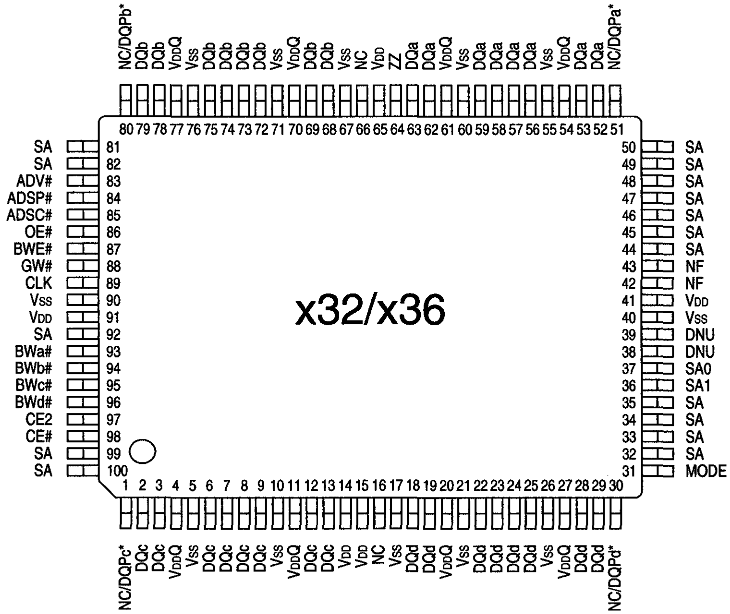
PIN #	x18	x32/x36
51	NC	NC/DQPa*
52	NC	DQa
53	NC	DQa
54	V$_{DD}$Q	
55	V$_{SS}$	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	V$_{SS}$	
61	V$_{DD}$Q	
62	DQa	
63	DQa	
64	ZZ	
65	V$_{DD}$	
66	NC	
67	V$_{SS}$	
68	DQa	DQb
69	DQa	DQb
70	V$_{DD}$Q	
71	V$_{SS}$	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb

PIN #	x18	x32/x36
76	V$_{SS}$	
77	V$_{DD}$Q	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb*
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	V$_{SS}$	
91	V$_{DD}$	
92	SA (T Version) CE2# (S Version)	
93	BWa#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

o Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View)
100-Pin TQFP, 2-Chip Enable,
T Version
(D-1)

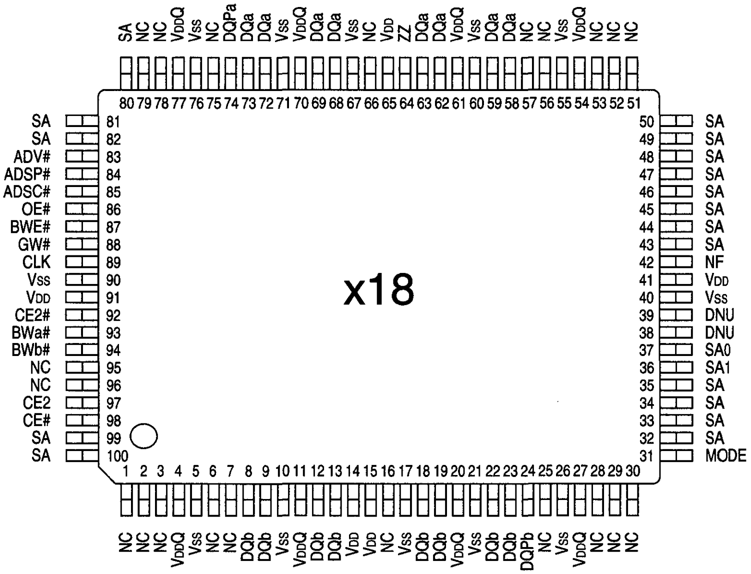


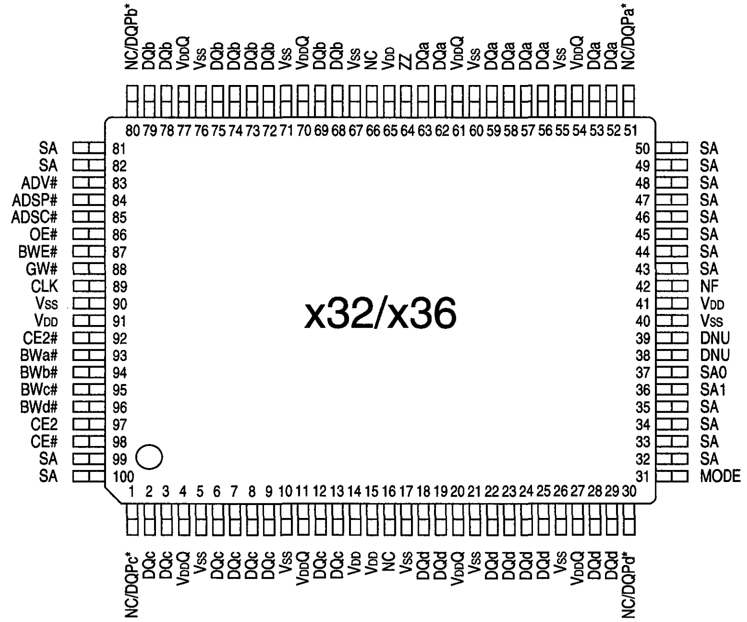


*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

PIN ASSIGNMENT (Top View) 100-Pin TQFP, 3-Chip Enable, S Version

(D-1)





*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

FLASH MEMORY 3

BOOT BLOCK FLASH MEMORY PRODUCT SELECTION GUIDE

Memory Configuration	Features/ Options	Part Number	Voltage*	Maximum Current Draw		Package/# of Pins			Page
				Standby	Active	FBGA	SOP	TSOP	
256K x 8	BB, AUTO	MT28F002B1[1]	SVT	130µA	60mA	–	–	40	3-1
128K x 16/ 256K x 8	BB, AUTO	MT28F200B1[1]	SVT	130µA	60mA	–	44	48	3-5
256K x 8	BB, AUTO	MT28F002C1[2]	12V	130µA	60mA	–	–	40	3-9
512K x 8	BB, AUTO	MT28F004B1[1]	SVT	130µA	60mA	–	–	40	3-11
256K x 16/ 512K x 8	BB, AUTO	MT28F400B1[1]	SVT	130µA	60mA	–	44	48	3-15
1 Meg x 8	BB, AUTO	MT28F008B1[1]	SVT	130µA	60mA	–	–	40	3-19
512K x 16/ 1 Meg x 8	BB, AUTO	MT28F800B1[1]	SVT	130µA	60mA	–	44	48	3-23
256K x 16	BB, AUTO	MT28F400B5 ET[3]	Smart 5	150µA	65mA	–	44	48	3-27
512K x 16	BB, AUTO	MT28F800B5 ET[3]	Smart 5	150µA	65mA	–	44	48	3-27
256K x 16	BB, AUTO	MT28F400B1 VET[1]		110µA	30mA	–	–	48	3-29
512K x 16	BB, AUTO	MT28F800B1 VET[1]		110µA	30mA	–	–	48	3-29
512K x 8	BB, AUTO	MT28F004B1 VET[1]		110µA	30mA	–	–	40	3-29
1 Meg x 8	BB, AUTO	MT28F008B1 VET[1]		110µA	30mA	–	–	40	3-29
1 Meg x 8	BB, AUTO	MT28F008B3	3V Only	100µA	30mA	–	–	40	3-31
512K x 16/ 1 Meg x 8	BB, AUTO	MT28F800B3	3V Only	100µA	30mA	48	44	48	3-31
1 Meg x 8	BB, AUTO	MT28F008B5[4]	5V Only	120µA	35mA	–	–	40	3-39
512K x 16/ 1 Meg x 8	BB, AUTO	MT28F800B5[4]	5V Only	120µA	35mA	–	44	48	3-39

BB = Boot Block, AUTO = Automated W/E Algorithm, ET = Extended Temperature, V = Low Voltage,
SVT = SmartVoltage Technology

Micron is currently migrating its flash process technology from 0.42µm to compatible 0.3µm devices. This migration should be complete by mid 1999 and may result in changes of existing part numbers. Please check our Web site for the latest data sheet updates.

*Operating and WRITE/ERASE Voltages

Voltage Technology	Operating	W/E
12V	5V	12V
SVT	3.3V or 5V	5V or 12V
Smart 3**	3.0V to 3.6V	3.0V to 3.6V or 12V
Smart 5	5V	5V or 12V

**Smart 3 devices are also available with a 2.7V operating voltage option.

NOTE:

1. Part numbers with a B1 (SmartVoltage) designation will be replaced with a B3 (Smart 3) or B5 (Smart 5) designation.
2. Part numbers with a C1 (BIOS-Optimized SmartVoltage) designation will be replaced with a C5 (BIOS-Optimized Smart 5) designation.
3. Part numbers with a B5 (Smart 5) designation will be maintained and migrate to 0.3µm die.
4. These part types have migrated to 0.3µm devices.

FLASH MEMORY

MT28F002B1

SMARTVOLTAGE

FEATURES

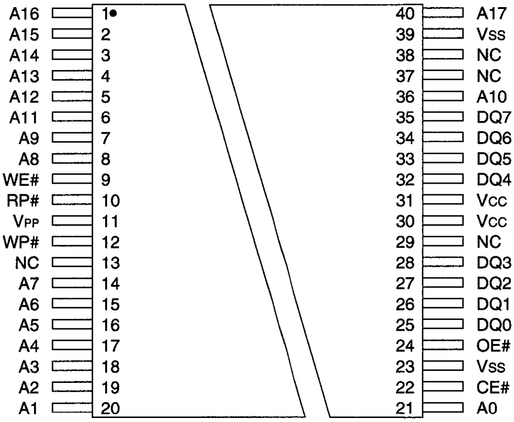
- Five erase blocks:
  - 16KB boot block (protected)
  - Two 8KB parameter blocks
  - Two main memory blocks
- SmartVoltage Technology (SVT):
  - 3.3V ±0.3V or 5V ±10% VCC
  - 5V ±10% or 12V ±5% VPP
- Address access times:
  - 60ns, 80ns at 5V VCC
  - 90ns, 110ns at 3.3V VCC
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence

OPTIONS	MARKING
• Timing (5V VCC/3.3V VCC)	
60ns/90ns access	-6
80ns/110ns access	-8
• Boot Block Starting Address	
Top (3FFFFH)	T
Bottom (00000H)	B
• Package	
Plastic 40-pin TSOP Type 1 (10mm x 20mm)	VG

- Part Number Example: MT28F002B1VG-8 T

PIN ASSIGNMENT (Top View)

40-Pin TSOP Type I
(C-2)



GENERAL DESCRIPTION

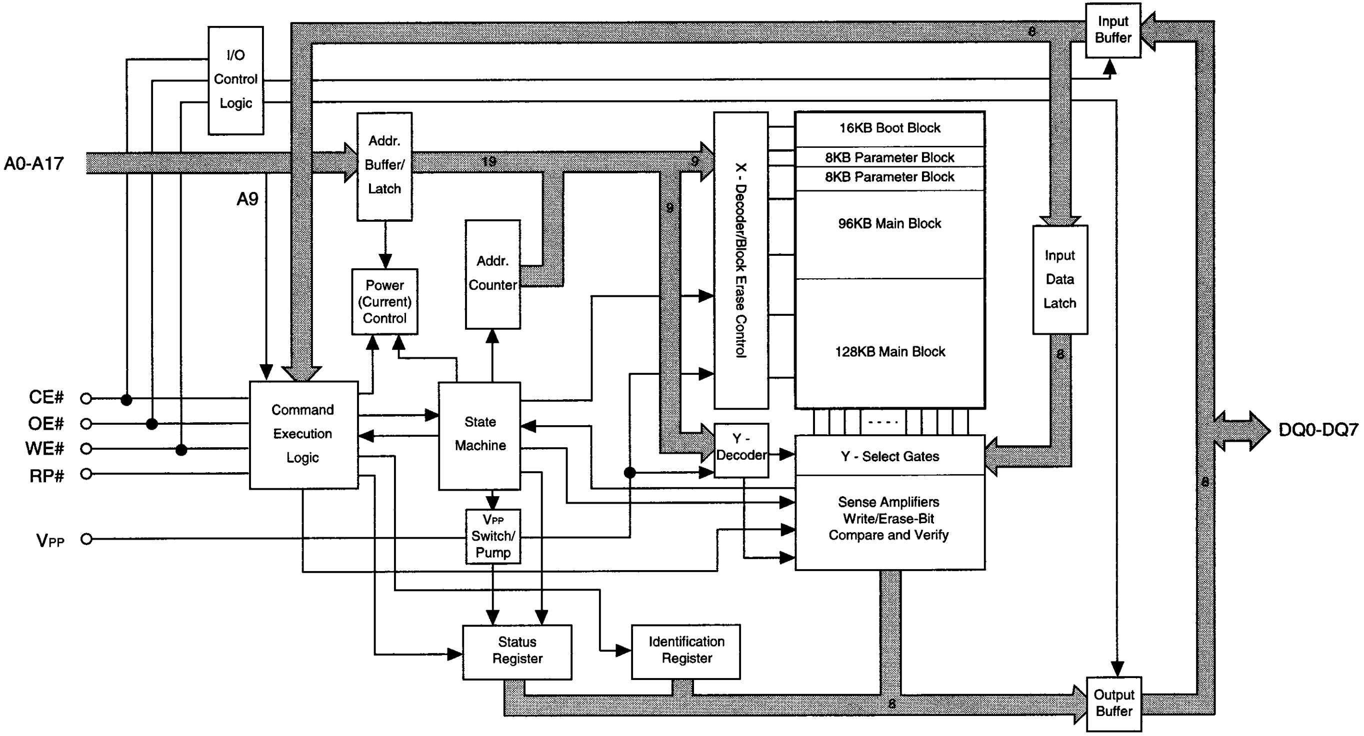
The MT28F002B1 is a nonvolatile, electrically block-erasable (flash), programmable read-only memory containing 2,097,152 bits organized as 262,144 words by 8 bits. SmartVoltage Technology (SVT) provides industry-standard, multi- or single-voltage, dual-supply operation. Writing or erasing the device is done with either a 5V or 12V VPP voltage, while all operations are performed with a 3.3V or 5V VCC. It is fabricated with Micron's advanced CMOS floating-gate process.

The MT28F002B1 is organized into five separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28F002B1 features a hardware-protected boot block. Writing or erasing the boot block requires either applying a super-voltage to the RP# pin or driving WP# HIGH in addition to executing the normal WRITE or ERASE sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density and are written and erased with no additional security measures.

The byte address is issued to read the memory array with CE# and OE# LOW and WE# HIGH. Valid data is output until the next address is issued, or CE# or OE# goes HIGH.

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest full-length data sheet.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
9	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# = LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
22	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
12	WP#	Input	Write Protect: Unlocks the boot block when HIGH if $V_{PP} = V_{PPH1}$ (5V) or V_{PPH2} (12V) and RP# = V_{IH} during a WRITE or ERASE. Does not affect WRITE or ERASE operation on other blocks.
10	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# unlocks the boot block and overrides the condition of WP# when at V_{HH} (12V), and must be held at V_{IH} during all other modes of operation.
24	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
21, 20, 19, 18, 17, 16, 15, 14, 8, 7, 36, 6, 5, 4, 3, 2, 1, 40	A0-A17	Input	Address Inputs: Select a unique byte out of the 262,144 available.
25, 26, 27, 28, 32, 33, 34, 35	DQ0-DQ7	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE. These pins are used to input commands to the CEL.
13, 29, 37, 38	NC	–	No Connect: These pins may be driven or left unconnected.
11	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the WRITE or ERASE, V_{PP} must be at V_{PPH1} (5V) or V_{PPH2} (12V). V_{PP} = "Don't Care" during all other operations.
30, 31	V_{CC}	Supply	Power Supply: +5V ±10% or +3.3V ±0.3V.
23, 39	V_{SS}	Supply	Ground.

TRUTH TABLE[1]

FUNCTION	**RP#**	**CE#**	**OE#**	**WE#**	**WP#**	**A0**	**A9**	**V_{PP}**	**DQ0-DQ7**
Standby	H	H	X	X	X	X	X	X	High-Z
RESET	L	X	X	X	X	X	X	X	High-Z
READ									
READ	H	L	L	H	X	X	X	X	Data-Out
Output Disable	H	L	H	H	X	X	X	X	High-Z
WRITE/ERASE (EXCEPT BOOT BLOCK)[2]									
ERASE SETUP	H	L	H	L	X	X	X	X	20H
ERASE CONFIRM[3]	H	L	H	L	X	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H
WRITE[4]	H	L	H	L	X	X	X	V_{PPH}	Data-In
READ ARRAY[5]	H	L	H	L	X	X	X	X	FFH
WRITE/ERASE (BOOT BLOCK)[2, 7]									
ERASE SETUP	H	L	H	L	X	X	X	X	20H
ERASE CONFIRM[3]	V_{HH}	L	H	L	X	X	X	V_{PPH}	D0H
ERASE CONFIRM[3, 6]	H	L	H	L	H	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H
WRITE[4]	V_{HH}	L	H	L	X	X	X	V_{PPH}	Data-In
WRITE[4, 6]	H	L	H	L	H	X	X	V_{PPH}	Data-In
READ ARRAY[5]	H	L	H	L	X	X	X	X	FFH
DEVICE IDENTIFICATION[8, 9]									
Manufacturer Compatibility	H	L	L	H	X	L	V_{ID}	X	89H
Device (top boot)	H	L	L	H	X	H	V_{ID}	X	7CH
Device (bottom boot)	H	L	L	H	X	H	V_{ID}	X	7DH

NOTE:
1. L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}.
2. V_{PPH} = V_{PPH1} = 5V or V_{PPH2} = 12V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. The READ ARRAY command must be issued before reading the array after writing or erasing.
6. When WP# = V_{IH}, RP# may be at V_{IH} or V_{HH}.
7. V_{HH} = 12V.
8. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE command.
9. A1-A8, A10-A17 = V_{IL}.

FLASH MEMORY

MT28F200B1

SMARTVOLTAGE

FEATURES

- Five erase blocks:
  - 16KB/8K-word boot block (protected)
  - Two 8KB/4K-word parameter blocks
  - Two main memory blocks
- SmartVoltage Technology (SVT):
  - 3.3V ±0.3V or 5V ±10% Vcc
  - 5V ±10% or 12V ±5% VPP
- Address access times:
  - 60ns, 80ns at 5V Vcc
  - 90ns, 110ns at 3.3V Vcc
- Selectable organizations:
  - 131,072 x 16 or
  - 262,144 x 8
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence
- Byte- or word-wide READ and WRITE
- TSOP and SOP packaging options

OPTIONS	MARKING
• Timing (5V Vcc/3.3V Vcc)	
60ns/90ns access	-6
80ns/110ns access	-8
• Boot Block Starting Address	
Top (1FFFFH)	T
Bottom (00000H)	B
• Packages	
Plastic SOP (600 mil)	SG
Plastic 48-pin TSOP Type 1 (12mm x 20mm)	WG

- Part Number Example: MT28F200B1SG-8 T

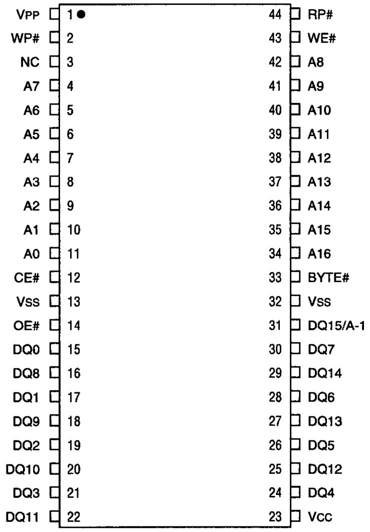
GENERAL DESCRIPTION

The MT28F200B1 is a nonvolatile, electrically block-erasable (flash), programmable read-only memory containing 2,097,152 bits organized as 131,072 words by 16 bits or 262,144 words by 8 bits. SmartVoltage Technology (SVT) provides industry-standard, multi- or single-voltage, dual-supply operation. Writing or erasing the device is done with either a 5V or 12V VPP voltage, while all operations are performed with a 3.3V or 5V Vcc. It is fabricated with Micron's advanced CMOS floating-gate process.

PIN ASSIGNMENT (Top View)

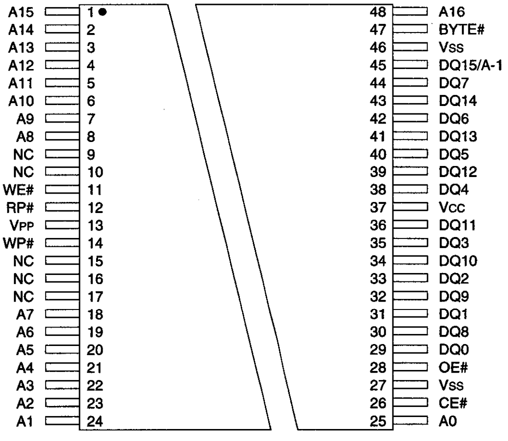
44-Pin SOP

(B-1)



48-Pin TSOP Type I

(C-3)



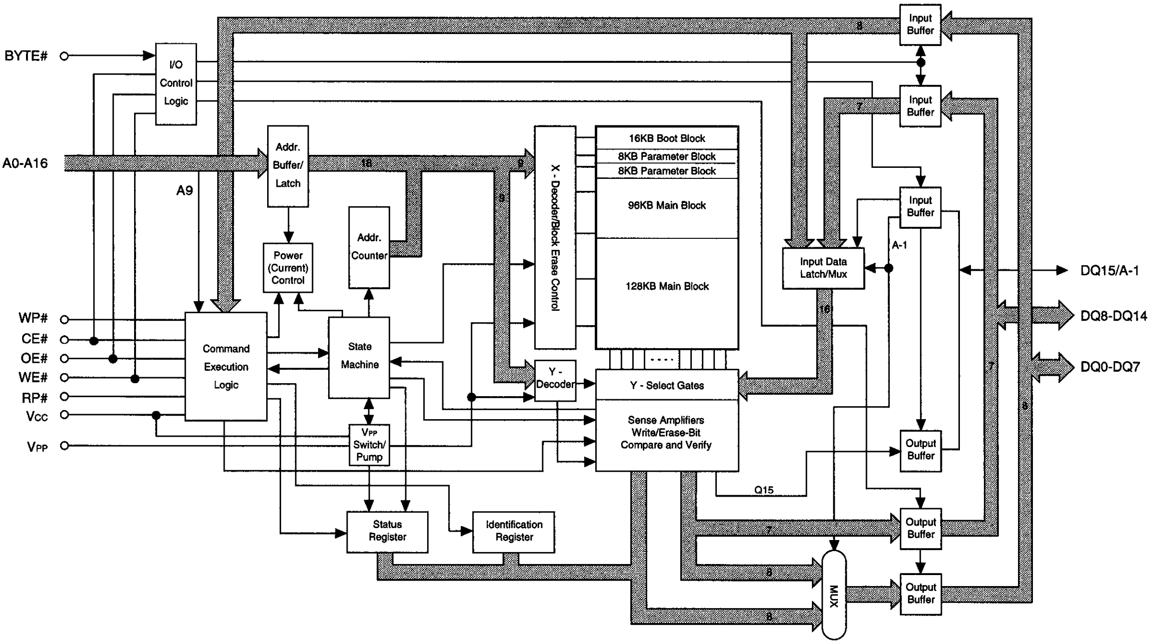
GENERAL DESCRIPTION (continued)

The MT28F200B1 is organized into five separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28F200B1 features a hardware-protected boot block. Writing or erasing the boot block requires either applying a super-voltage to the RP# pin or driving WP# HIGH in addition to executing the normal WRITE or ERASE sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density and are written and erased with no additional security measures.

The byte or word address is issued to read the memory array with CE# and OE# LOW and WE# HIGH. Valid data is output until the next address is issued. The BYTE# pin is used to switch the data path between 8 bits wide and 16 bits wide. When BYTE# is LOW, the dual-use pin DQ15/A-1 becomes the lowest order address bit (A-1). When BYTE# is HIGH, the DQ15/A-1 pin becomes the most significant data bit (DQ15).

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest full-length data sheet.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
43	11	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
2	14	WP#	Input	Write Protect: Unlocks the boot block when HIGH if $V_{PP} = V_{PPH1}$ (5V) or V_{PPH2} (12V) and RP# = V_{IH} during a WRITE or ERASE. Does not affect WRITE or ERASE operation on other blocks.
12	26	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
44	12	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# unlocks the boot block and overrides the condition of WP# when at V_{HH} (12V), and must be held at V_{IH} during all other modes of operation.
14	28	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
33	47	BYTE#	Input	Byte Enable: If BYTE# = HIGH, the upper byte is active through DQ8-DQ15. If BYTE# = LOW, DQ8-DQ14 are High-Z, and all data is accessed through DQ0-DQ7. DQ15/A-1 becomes the least significant address input.
11, 10, 9, 8, 7, 6, 5, 4, 42, 41, 40, 39, 38, 37, 36, 35, 34	25, 24, 23, 22, 21, 20, 19, 18, 8, 7, 6, 5, 4, 3, 2, 1, 48	A0-A16	Input	Address Inputs: Select a unique, 16-bit word out of the 131,072 available. The DQ15/A-1 input becomes the lowest order address when BYTE# = LOW to allow for a selection of an 8-bit byte from the 262,144 available.
31	45	DQ15/A-1	Input/ Output	Data I/O: MSB of data when BYTE# = HIGH. Address Input: LSB of address input when BYTE# = LOW during READ or WRITE operation.
15, 17, 19, 21, 24, 26, 28, 30	29, 31, 33, 35, 38, 40, 42, 44	DQ0-DQ7	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE. These pins are used to input commands to the CEL.
16, 18, 20, 22, 25, 27, 29	30, 32, 34, 36, 39, 41, 43	DQ8-DQ14	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE when BYTE# = HIGH. These pins are High-Z when BYTE# is LOW.
3	9, 10, 15, 16, 17	NC	–	No Connect: These pins may be driven or left unconnected.
1	13	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the WRITE or ERASE, V_{PP} must be at V_{PPH1} (5V) or V_{PPH2} (12V). V_{PP} = "Don't Care" during all other operations.
23	37	V_{CC}	Supply	Power Supply: +5V ±10% or +3.3V ±0.3V.
13, 32	27, 46	V_{SS}	Supply	Ground.

TRUTH TABLE[1]

FUNCTION	RP#	CE#	OE#	WE#	WP#	BYTE#	A0	A9	V_{PP}	DQ0-DQ7	DQ8-DQ14	DQ15/A-1
Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
RESET	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
READ												
READ (word mode)	H	L	L	H	X	H	X	X	X	Data-Out	Data-Out	Data-Out
READ (byte mode)	H	L	L	H	X	L	X	X	X	Data-Out	High-Z	A-1
Output Disable	H	L	H	H	X	X	X	X	X	High-Z	High-Z	High-Z
WRITE/ERASE (EXCEPT BOOT BLOCK)[2]												
ERASE SETUP	H	L	H	L	X	X	X	X	X	20H	X	X
ERASE CONFIRM[3]	H	L	H	L	X	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	X	10H/40H	X	X
WRITE (word mode)[4]	H	L	H	L	X	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (byte mode)[4]	H	L	H	L	X	L	X	X	V_{PPH}	Data-In	X	A-1
READ ARRAY[5]	H	L	H	L	X	X	X	X	X	FFH	X	X
WRITE/ERASE (BOOT BLOCK)[2, 7]												
ERASE SETUP	H	L	H	L	X	X	X	X	X	20H	X	X
ERASE CONFIRM[3]	V_{HH}	L	H	L	X	X	X	X	V_{PPH}	D0H	X	X
ERASE CONFIRM[3, 6]	H	L	H	L	H	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	X	10H/40H	X	X
WRITE (word mode)[4]	V_{HH}	L	H	L	X	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (word mode)[4, 6]	H	L	H	L	H	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (byte mode)[4]	V_{HH}	L	H	L	X	L	X	X	V_{PPH}	Data-In	X	A-1
WRITE (byte mode)[4, 6]	H	L	H	L	H	L	X	X	V_{PPH}	Data-In	X	A-1
READ ARRAY[5]	H	L	H	L	X	X	X	X	X	FFH	X	X
DEVICE IDENTIFICATION[8, 9]												
Manufacturer compatibility (word mode)[10]	H	L	L	H	X	H	L	V_{ID}	X	89H	00H	–
Manufacturer compatibility (byte mode)	H	L	L	H	X	L	L	V_{ID}	X	89H	High-Z	X
Device (word mode, top boot)[10]	H	L	L	H	X	H	H	V_{ID}	X	74H	22H	–
Device (byte mode, top boot)	H	L	L	H	X	L	H	V_{ID}	X	74H	High-Z	X
Device (word mode, bottom boot)[10]	H	L	L	H	X	H	H	V_{ID}	X	75H	22H	–
Device (byte mode, bottom boot)	H	L	L	H	X	L	H	V_{ID}	X	75H	High-Z	X

NOTE:

1. L = V_{IL} (LOW), H = V_{IH} (HIGH), X = V_{IL} or V_{IH} ("Don't Care").
2. V_{PPH} = V_{PPH1} = 5V or V_{PPH2} = 12V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. The READ ARRAY command must be issued before reading the array after writing or erasing.
6. When WP# = V_{IH}, RP# may be at V_{IH} or V_{HH}.
7. V_{HH} = 12V.
8. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE command.
9. A1-A8, A10-A16 = V_{IL}.
10. Value reflects DQ8-DQ15.

FLASH MEMORY

MT28F002C1

FEATURES

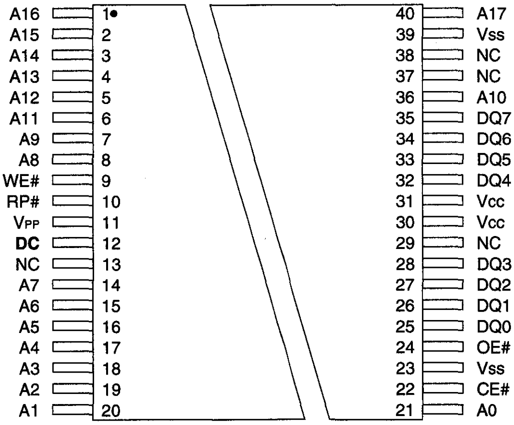
- Five erase blocks:
  - 16KB/8K-word boot block (protected)
  - Two 8KB/4K-word parameter blocks
  - Two main memory blocks (96KB and 128KB)
- Top boot block organization
- Address access time: 80ns
- Industry-standard pinouts
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence
- TSOP packaging

OPTIONS	MARKING
• Timing 80ns access	-8
• Boot Block Starting Address Top	T
• Package Plastic 40-pin TSOP Type 1 (10mm x 20mm)	VG

- Part Number Example: MT28F002C1VG-8 T

PIN ASSIGNMENT (Top View)

40-Pin TSOP Type I
(C-2)



GENERAL DESCRIPTION

The MT28F002C1 (x8) is nonvolatile, electrically block-erasable (flash), programmable read-only memory containing 2,097,152 bits. It is fabricated with Micron's advanced CMOS floating-gate process. Device operation and features of the MT28F002C1 are identical to the SmartVoltage MT28F002B1, except the BIOS-optimized device is specified to operate at 5V Vcc and 12V VPP, and it is available in a top boot configuration only. In addition, the WP# pin is a "Don't Care." For further information on device operation or features, refer to the MT28F002B1 data sheet.

System designers can easily accommodate multiple types of boot block flash by connecting the DC pin ("Don't Care") to Vss. By doing this, a Micron SmartVoltage device or the BIOS-optimized device can be used in the same socket without any further hardware or software changes.

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest full-length data sheet.

PIN DESCRIPTIONS

TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
9	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
12	DC	Input	Don't Care: This pin can be left floating, can be tied to a control pin or can be tied to Vss or Vcc (±10µA input leakage). It should be tied to Vss to allow for compatibility with SmartVoltage 2Mb boot block flash.
22	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
10	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# unlocks the boot block and overrides the condition of WP# when at VHH (12V), and must be held at VIH during all other modes of operation.
24	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
21, 20, 19, 18, 17, 16, 15, 14, 8, 7, 36, 6, 5, 4, 3, 2, 1, 40	Addr	Input	Address Inputs: Select a unique location within the array.
25, 26, 27, 28, 32, 33, 34, 35	DQ0-DQ7	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE. These pins are used to input commands to the CEL.
3, 29, 37, 38	NC	–	No Connect: These pins may be driven or left unconnected.
11	VPP	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the WRITE or ERASE, VPP must be at VPPH (12V). VPP is "Don't Care" during all other operations.
30, 31	Vcc	Supply	Power Supply: +5V ±10%.
23, 39	Vss	Supply	Ground.

FLASH MEMORY

MT28F004B1

SMARTVOLTAGE

FEATURES

- Seven erase blocks:
  - 16KB boot block (protected)
  - Two 8KB parameter blocks
  - Four main memory blocks
- SmartVoltage Technology (SVT):
  - 3.3V ±0.3V or 5V ±10% Vcc
  - 5V ±10% or 12V ±5% VPP
- Address access times:
  - 60ns, 80ns at 5V Vcc
  - 90ns, 110ns at 3.3V Vcc
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence

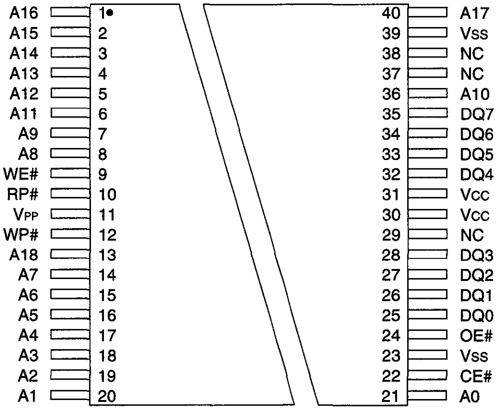
OPTIONS

OPTIONS	MARKING
• Timing (5V Vcc/3.3V Vcc)	
60ns/90ns access	-6
80ns/110ns access	-8
• Boot Block Starting Address	
Top (7FFFFH)	T
Bottom (00000H)	B
• Package	
Plastic 40-pin TSOP Type 1 (10mm x 20mm)	VG

- Part Number Example: MT28F004B1VG-8 T

PIN ASSIGNMENT (Top View)

40-Pin TSOP Type I
(C-2)



GENERAL DESCRIPTION

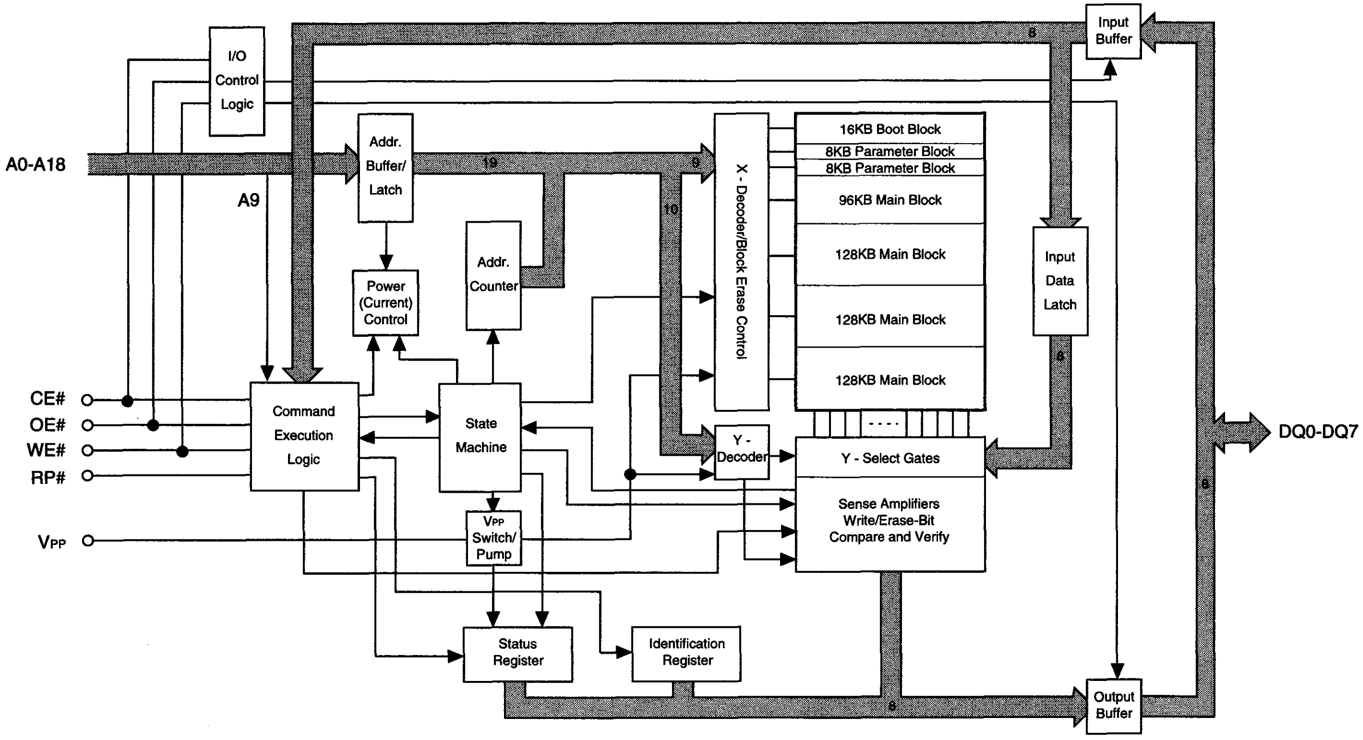
The MT28F004B1 is a nonvolatile, electrically block-erasable (flash), programmable read-only memory containing 4,194,304 bits organized as 524,288 words by 8 bits. SmartVoltage Technology (SVT) provides industry-standard, multi- or single-voltage, dual-supply operation. Writing or erasing the device is done with either a 5V or 12V VPP voltage, while all operations are performed with a 3.3V or 5V Vcc. It is fabricated with Micron's advanced CMOS floating-gate process.

The MT28F004B1 is organized into seven separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28F004B1 features a hardware-protected boot block. Writing or erasing the boot block requires either applying a super-voltage to the RP# pin or driving WP# HIGH in addition to executing the normal WRITE or ERASE sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density and are written and erased with no additional security measures.

The byte address is issued to read the memory array with CE# and OE# LOW and WE# HIGH. Valid data is output until the next address is issued, or CE# or OE# goes HIGH.

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest full-length data sheet.

FUNCTIONAL BLOCK DIAGRAM



IN DESCRIPTIONS

TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
9	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# = LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
22	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
12	WP#	Input	Write Protect: Unlocks the boot block when HIGH if $V_{PP} = V_{PPH1}$ (5V) or V_{PPH2} (12V) and RP# = V_{IH} during a WRITE or ERASE. Does not affect WRITE or ERASE operation on other blocks.
10	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# unlocks the boot block and overrides the condition of WP# when at V_{HH} (12V), and must be held at V_{IH} during all other modes of operation.
24	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
21, 20, 19, 18, 17, 16, 15, 14, 3, 7, 36, 6, 5, 4, 3, 2, 1, 40, 13	A0-A18	Input	Address Inputs: Select a unique byte out of the 524,288 available.
25, 26, 27, 28, 32, 33, 34, 35	DQ0-DQ7	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE. These pins are used to input commands to the CEL.
29, 37, 38	NC	–	No Connect: These pins may be driven or left unconnected.
11	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the WRITE or ERASE, V_{PP} must be at V_{PPH1} (5V) or V_{PPH2} (12V). V_{PP} = "Don't Care" during all other operations.
30, 31	V_{CC}	Supply	Power Supply: +5V ±10% or +3.3V ±0.3V.
23, 39	V_{SS}	Supply	Ground.

TRUTH TABLE[1]

FUNCTION	RP#	CE#	OE#	WE#	WP#	A0	A9	V_{PP}	DQ0-DQ7
Standby	H	H	X	X	X	X	X	X	High-Z
RESET	L	X	X	X	X	X	X	X	High-Z
READ									
READ	H	L	L	H	X	X	X	X	Data-Out
Output Disable	H	L	H	H	X	X	X	X	High-Z
WRITE/ERASE (EXCEPT BOOT BLOCK)[2]									
ERASE SETUP	H	L	H	L	X	X	X	X	20H
ERASE CONFIRM[3]	H	L	H	L	X	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H
WRITE[4]	H	L	H	L	X	X	X	V_{PPH}	Data-In
READ ARRAY[5]	H	L	H	L	X	X	X	X	FFH
WRITE/ERASE (BOOT BLOCK)[2, 7]									
ERASE SETUP	H	L	H	L	X	X	X	X	20H
ERASE CONFIRM[3]	V_{HH}	L	H	L	X	X	X	V_{PPH}	D0H
ERASE CONFIRM[3, 6]	H	L	H	L	H	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H
WRITE[4]	V_{HH}	L	H	L	X	X	X	V_{PPH}	Data-In
WRITE[4, 6]	H	L	H	L	H	X	X	V_{PPH}	Data-In
READ ARRAY[5]	H	L	H	L	X	X	X	X	FFH
DEVICE IDENTIFICATION[8, 9]									
Manufacturer Compatibility	H	L	L	H	X	L	V_{ID}	X	89H
Device (top boot)	H	L	L	H	X	H	V_{ID}	X	78H
Device (bottom boot)	H	L	L	H	X	H	V_{ID}	X	79H

NOTE:
1. L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}.
2. V_{PPH} = V_{PPH1} = 5V or V_{PPH2} = 12V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. The READ ARRAY command must be issued before reading the array after writing or erasing.
6. When WP# = V_{IH}, RP# may be at V_{IH} or V_{HH}.
7. V_{HH} = 12V.
8. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE command.
9. A1-A8, A10-A18 = V_{IL}.

FLASH MEMORY

MT28F400B1

SMARTVOLTAGE

EATURES

- Seven erase blocks:
  - 16KB/8K-word boot block (protected)
  - Two 8KB/4K-word parameter blocks
  - Four main memory blocks
- SmartVoltage Technology (SVT):
  - 3.3V ±0.3V or 5V ±10% Vcc
  - 5V ±10% or 12V ±5% VPP
- Address access times:
  - 60ns, 80ns at 5V Vcc
  - 90ns, 110ns at 3.3V Vcc
- Selectable organizations:
  - 262,144 x 16 or
  - 524,288 x 8
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence
- Byte- or word-wide READ and WRITE
- TSOP and SOP packaging options

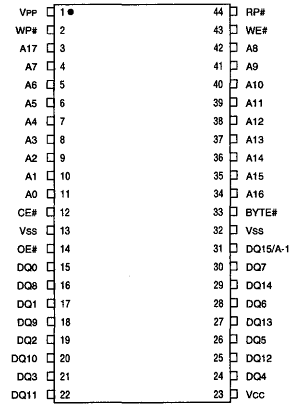
PTIONS

PTIONS	MARKING
Timing (5V Vcc/3.3V Vcc)	
60ns/90ns access	-6
80ns/110ns access	-8
Boot Block Starting Address	
Top (3FFFFH)	T
Bottom (00000H)	B
Packages	
Plastic SOP (600 mil)	SG
Plastic 48-pin TSOP Type 1 (12mm x 20mm)	WG

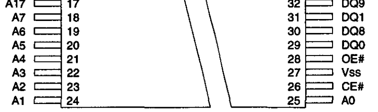
- Part Number Example: MT28F400B1SG-8 T

PIN ASSIGNMENT (Top View)

44-Pin SOP
(B-1)



48-Pin TSOP Type I
(C-3)



ENERAL DESCRIPTION

The MT28F400B1 is a nonvolatile, electrically block-rasable (flash), programmable read-only memory con-aining 4,194,304 bits organized as 262,144 words by 16 bits r 524,288 words by 8 bits. SmartVoltage Technology (SVT) rovides industry-standard, multi- or single-voltage, dual-upply operation. Writing or erasing the device is done vith either a 5V or 12V VPP voltage, while all operations are erformed with a 3.3V or 5V Vcc. It is fabricated with Micron's advanced CMOS floating-gate process.

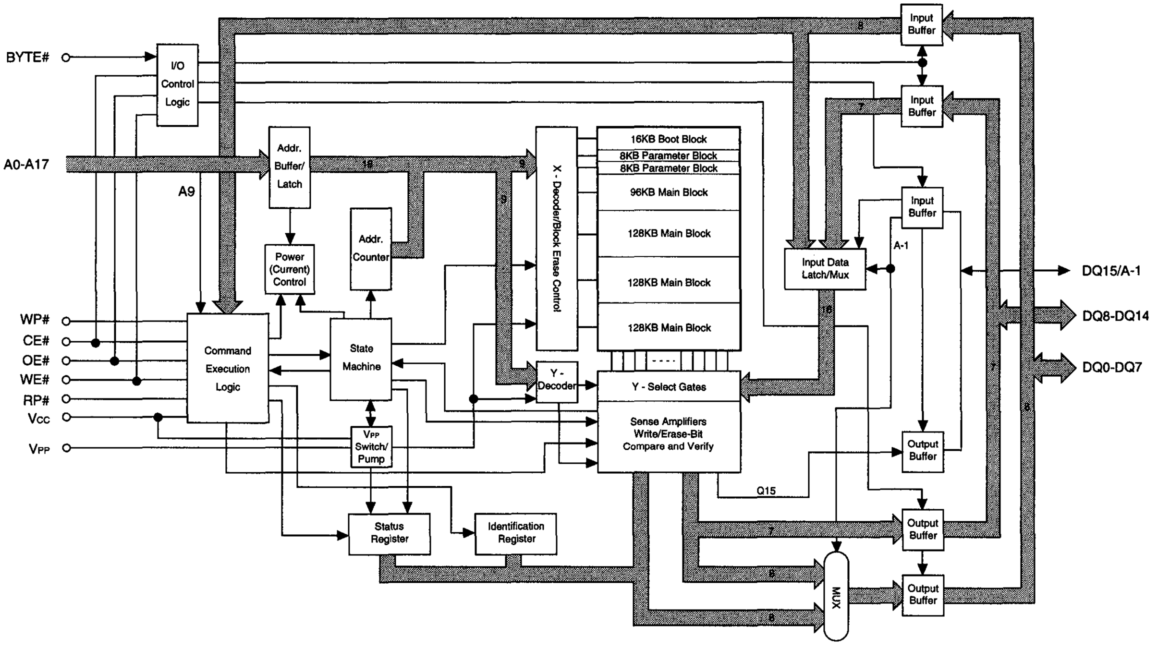
The MT28F400B1 is organized into seven separately rasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28F400B1 features a hardware-protected boot block. Writing or erasing the boot block requires either applying a super-voltage to the RP# pin or driving WP# HIGH in addition to executing the normal WRITE or ERASE sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density and are written and erased with no additional security measures.

GENERAL DESCRIPTION (continued)

The byte or word address is issued to read the memory array with CE# and OE# LOW and WE# HIGH. Valid data is output until the next address is issued. The BYTE# pin is used to switch the data path between 8 bits wide and 16 bits wide. When BYTE# is LOW, the dual-use pin DQ15/A-1 becomes the lowest order address bit (A-1). When BYTE# is HIGH, the DQ15/A-1 pin becomes the most significant data bit (DQ15).

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest full-length data sheet.

FUNCTIONAL BLOCK DIAGRAM



IN DESCRIPTIONS

SOP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
43	11	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
2	14	WP#	Input	Write Protect: Unlocks the boot block when HIGH if $V_{PP} = V_{PPH1}$ (5V) or V_{PPH2} (12V) and RP# = V_{IH} during a WRITE or ERASE. Does not affect WRITE or ERASE operation on other blocks.
12	26	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
44	12	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# unlocks the boot block and overrides the condition of WP# when at V_{HH} (12V), and must be held at V_{IH} during all other modes of operation.
14	28	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
33	47	BYTE#	Input	Byte Enable: If BYTE# = HIGH, the upper byte is active through DQ8-DQ15. If BYTE# = LOW, DQ8-DQ14 are High-Z, and all data is accessed through DQ0-DQ7. DQ15/A-1 becomes the least significant address input.
11, 10, 9, 8, 7, 6, 5, 4, 42, 41, 40, 39, 38, 37, 36, 35, 34, 3	25, 24, 23, 22, 21, 20, 19, 18, 8, 7, 6, 5, 4, 3, 2, 1, 48, 17	A0-A17	Input	Address Inputs: Select a unique, 16-bit word out of the 262,144 available. The DQ15/A-1 input becomes the lowest order address when BYTE# = LOW to allow for a selection of an 8-bit byte from the 524,288 available.
31	45	DQ15/A-1	Input/ Output	Data I/O: MSB of data when BYTE# = HIGH. Address Input: LSB of address input when BYTE# = LOW during READ or WRITE operation.
15, 17, 19, 21, 24, 26, 28, 30	29, 31, 33, 35, 38, 40, 42, 44	DQ0-DQ7	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE. These pins are used to input commands to the CEL.
16, 18, 20, 22, 25, 27, 29	30, 32, 34, 36, 39, 41, 43	DQ8-DQ14	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE when BYTE# = HIGH. These pins are High-Z when BYTE# is LOW.
–	9, 10, 15, 16	NC	–	No Connect: These pins may be driven or left unconnected.
1	13	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the WRITE or ERASE, V_{PP} must be at V_{PPH1} (5V) or V_{PPH2} (12V). V_{PP} = "Don't Care" during all other operations.
23	37	V_{CC}	Supply	Power Supply: +5V ±10% or +3.3V ±0.3V.
13, 32	27, 46	V_{SS}	Supply	Ground.

TRUTH TABLE[1]

FUNCTION	RP#	CE#	OE#	WE#	WP#	BYTE#	A0	A9	V_{PP}	DQ0-DQ7	DQ8-DQ14	DQ15/A-1
Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
RESET	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
READ												
READ (word mode)	H	L	L	H	X	H	X	X	X	Data-Out	Data-Out	Data-Ou
READ (byte mode)	H	L	L	H	X	L	X	X	X	Data-Out	High-Z	A-1
Output Disable	H	L	H	H	X	X	X	X	X	High-Z	High-Z	High-Z
WRITE/ERASE (EXCEPT BOOT BLOCK)[2]												
ERASE SETUP	H	L	H	L	X	X	X	X	X	20H	X	X
ERASE CONFIRM[3]	H	L	H	L	X	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	X	10H/40H	X	X
WRITE (word mode)[4]	H	L	H	L	X	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (byte mode)[4]	H	L	H	L	X	L	X	X	V_{PPH}	Data-In	X	A-1
READ ARRAY[5]	H	L	H	L	X	X	X	X	X	FFH	X	X
WRITE/ERASE (BOOT BLOCK)[2, 7]												
ERASE SETUP	H	L	H	L	X	X	X	X	X	20H	X	X
ERASE CONFIRM[3]	V_{HH}	L	H	L	X	X	X	X	V_{PPH}	D0H	X	X
ERASE CONFIRM[3, 6]	H	L	H	L	H	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	X	10H/40H	X	X
WRITE (word mode)[4]	V_{HH}	L	H	L	X	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (word mode)[4, 6]	H	L	H	L	H	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (byte mode)[4]	V_{HH}	L	H	L	X	L	X	X	V_{PPH}	Data-In	X	A-1
WRITE (byte mode)[4, 6]	H	L	H	L	H	L	X	X	V_{PPH}	Data-In	X	A-1
READ ARRAY[5]	H	L	H	L	X	X	X	X	X	FFH	X	X
DEVICE IDENTIFICATION[8, 9]												
Manufacturer Compatibility (word mode)[10]	H	L	L	H	X	H	L	V_{ID}	X	89H	00H	–
Manufacturer Compatibility (byte mode)	H	L	L	H	X	L	L	V_{ID}	X	89H	High-Z	X
Device (word mode, top boot)[10]	H	L	L	H	X	H	H	V_{ID}	X	70H	44H	–
Device (byte mode, top boot)	H	L	L	H	X	L	H	V_{ID}	X	70H	High-Z	X
Device (word mode, bottom boot)[10]	H	L	L	H	X	H	H	V_{ID}	X	71H	44H	–
Device (byte mode, bottom boot)	H	L	L	H	X	L	H	V_{ID}	X	71H	High-Z	X

NOTE:

1. L = V_{IL} (LOW), H = V_{IH} (HIGH), X = V_{IL} or V_{IH} ("Don't Care").
2. V_{PPH} = V_{PPH1} = 5V or V_{PPH2} = 12V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. The READ ARRAY command must be issued before reading the array after writing or erasing.
6. When WP# = V_{IH}, RP# may be at V_{IH} or V_{HH}.
7. V_{HH} = 12V.
8. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE command.
9. A1-A8, A10-A17 = V_{IL}.
10. Value reflects DQ8-DQ15.

FLASH MEMORY

MT28F008B1

SMARTVOLTAGE

FEATURES

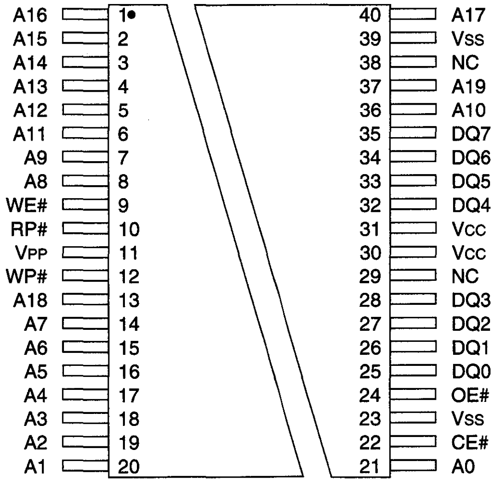
- Eleven erase blocks:
  16KB boot block (protected)
  Two 8KB parameter blocks
  Eight main memory blocks
- SmartVoltage Technology (SVT):
  3.3V ±0.3V or 5V ±10% V_{CC}
  5V ±10% or 12V ±5% V_{PP}
- Address access times:
  80ns at 5V V_{CC}
  110ns at 3.3V V_{CC}
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence

OPTIONS	MARKING
• Timing (5V Vcc/3.3V Vcc)	
80ns/110ns access	-8
• Boot Block Starting Address	
Top (FFFFFH)	T
Bottom (00000H)	B
• Package	
Plastic 40-pin TSOP Type 1 (10mm x 20mm)	VG

- Part Number Example: MT28F008B1VG-8 T

PIN ASSIGNMENT (Top View)

40-Pin TSOP Type I
(C-2)



GENERAL DESCRIPTION

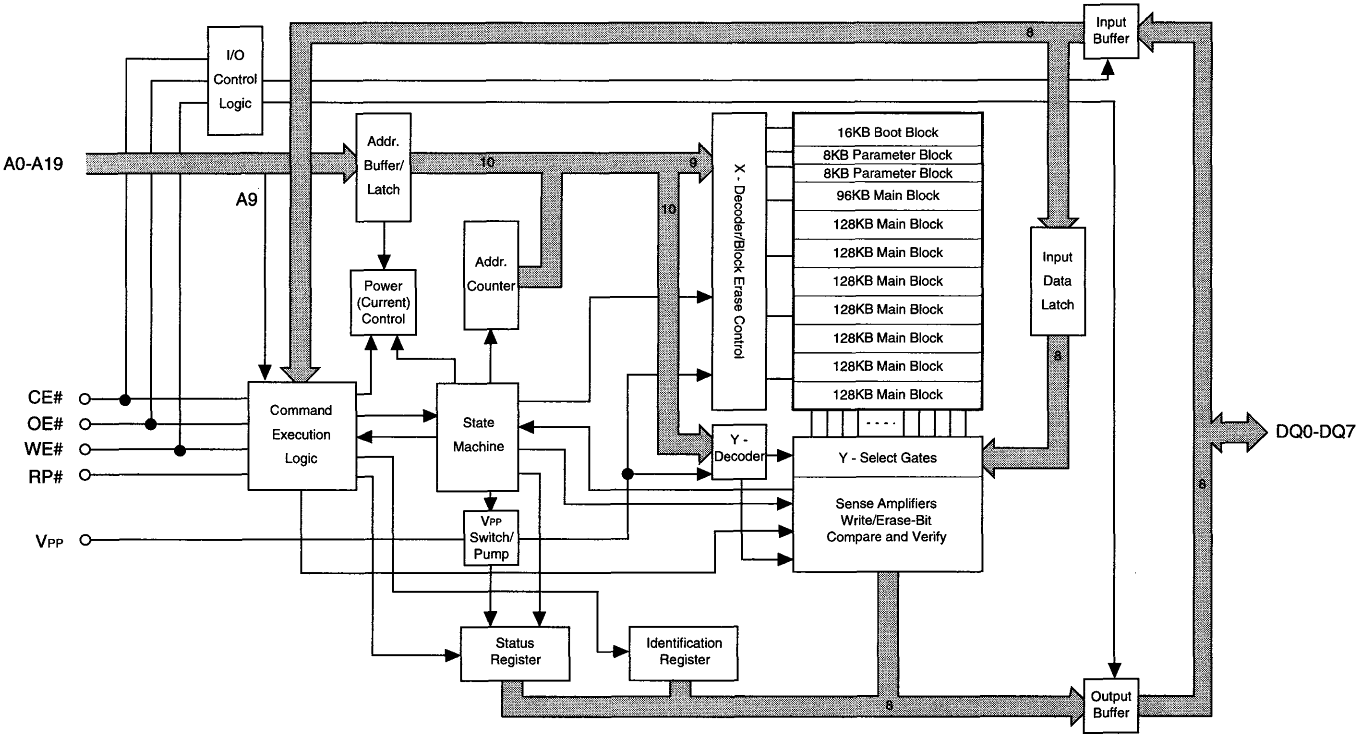
The MT28F008B1 is a nonvolatile, electrically block-erasable (flash), programmable read-only memory containing 8,388,608 bits organized as 1,048,576 words by 8 bits. SmartVoltage Technology (SVT) provides industry-standard, multi- or single-voltage, dual-supply operation. Writing or erasing the device is done with either a 5V or 12V V_{PP} voltage, while all operations are performed with a 3.3V or 5V V_{CC}. It is fabricated with Micron's advanced CMOS floating-gate process.

The MT28F008B1 is organized into eleven separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28F008B1 features a hardware-protected boot block. Writing or erasing the boot block requires either applying a super-voltage to the RP# pin or driving WP# HIGH in addition to executing the normal WRITE or ERASE sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density and are written and erased with no additional security measures.

The byte address is issued to read the memory array with CE# and OE# LOW and WE# HIGH. Valid data is output until the next address is issued, or CE# or OE# goes HIGH.

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest full-length data sheet.

FUNCTIONAL BLOCK DIAGRAM



'IN DESCRIPTIONS

TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
9	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# = LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
22	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
12	WP#	Input	Write Protect: Unlocks the boot block when HIGH if $V_{PP} = V_{PPH1}$ (5V) or V_{PPH2} (12V) and RP# = V_{IH} during a WRITE or ERASE. Does not affect WRITE or ERASE operation on other blocks.
10	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# unlocks the boot block and overrides the condition of WP# when at V_{HH} (12V), and must be held at V_{IH} during all other modes of operation.
24	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
21, 20, 19, 18, 17, 16, 15, 14, 8, 7, 36, 6, 5, 4, 3, 2, 1, 40, 13, 37	A0-A19	Input	Address Inputs: Select a unique byte out of the 1,048,576 available.
25, 26, 27, 28, 32, 33, 34, 35	DQ0-DQ7	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE. These pins are used to input commands to the CEL.
29, 38	NC	–	No Connect: These pins may be driven or left unconnected.
11	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the WRITE or ERASE, V_{PP} must be at V_{PPH1} (5V) or V_{PPH2} (12V). V_{PP} = "Don't Care" during all other operations.
30, 31	V_{CC}	Supply	Power Supply: +5V ±10% or +3.3V ±0.3V.
23, 39	V_{SS}	Supply	Ground.

TRUTH TABLE[1]

FUNCTION	RP#	CE#	OE#	WE#	WP#	A0	A9	V_{PP}	DQ0-DQ7
Standby	H	H	X	X	X	X	X	X	High-Z
RESET	L	X	X	X	X	X	X	X	High-Z
READ									
READ	H	L	L	H	X	X	X	X	Data-Out
Output Disable	H	L	H	H	X	X	X	X	High-Z
WRITE/ERASE (EXCEPT BOOT BLOCK)[2]									
ERASE SETUP	H	L	H	L	X	X	X	X	20H
ERASE CONFIRM[3]	H	L	H	L	X	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H
WRITE[4]	H	L	H	L	X	X	X	V_{PPH}	Data-In
READ ARRAY[5]	H	L	H	L	X	X	X	X	FFH
WRITE/ERASE (BOOT BLOCK)[2, 7]									
ERASE SETUP	H	L	H	L	X	X	X	X	20H
ERASE CONFIRM[3]	V_{HH}	L	H	L	X	X	X	V_{PPH}	D0H
ERASE CONFIRM[3, 6]	H	L	H	L	H	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H
WRITE[4]	V_{HH}	L	H	L	X	X	X	V_{PPH}	Data-In
WRITE[4, 6]	H	L	H	L	H	X	X	V_{PPH}	Data-In
READ ARRAY[5]	H	L	H	L	X	X	X	X	FFH
DEVICE IDENTIFICATION[8, 9]									
Manufacturer Compatibility	H	L	L	H	X	L	V_{ID}	X	89H
Device (top boot)	H	L	L	H	X	H	V_{ID}	X	98H
Device (bottom boot)	H	L	L	H	X	H	V_{ID}	X	99H

NOTE:
1. L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}.
2. V_{PPH} = V_{PPH1} = 5V or V_{PPH2} = 12V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. The READ ARRAY command must be issued before reading the array after writing or erasing.
6. When WP# = V_{IH}, RP# may be at V_{IH} or V_{HH}.
7. V_{HH} = 12V.
8. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE command.
9. A1-A8, A10-A19 = V_{IL}.

FLASH MEMORY

MT28F800B1

SMARTVOLTAGE

EATURES

- Eleven erase blocks:
  - 16KB/8K-word boot block (protected)
  - Two 8KB/4K-word parameter blocks
  - Eight main memory blocks
- SmartVoltage Technology (SVT):
  - 3.3V ±0.3V or 5V ±10% Vcc
  - 5V ±10% or 12V ±5% Vpp
- Address access times:
  - 80ns at 5V Vcc
  - 110ns at 3.3V Vcc
- Selectable organizations:
  - 524,288 x 16 or
  - 1,048,576 x 8
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence
- Byte- or word-wide READ and WRITE
- TSOP and SOP packaging options

PTIONS

PTIONS	MARKING
Timing (5V Vcc/3.3V Vcc)	
80ns/110ns access	-8
Boot Block Starting Address	
Top (7FFFFH)	T
Bottom (00000H)	B
Packages	
Plastic SOP (600 mil)	SG
Plastic 48-pin TSOP Type 1 (12mm x 20mm)	WG

Part Number Example: MT28F800B1SG-8 T

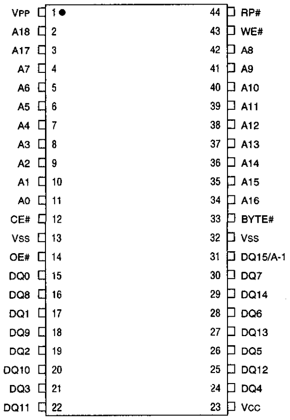
ENERAL DESCRIPTION

The MT28F800B1 is a nonvolatile, electrically block-rasable (flash), programmable read-only memory con-ining 8,388,608 bits organized as 524,288 words by 16 its or 1,048,576 words by 8 bits. SmartVoltage Technology VT) provides industry-standard, multi- or single-oltage, dual-supply operation. Writing or erasing the evice is done with either a 5V or 12V Vpp voltage, while ll operations are performed with a 3.3V or 5V Vcc. It is bricated with Micron's advanced CMOS floating-gate rocess.

PIN ASSIGNMENT (Top View)

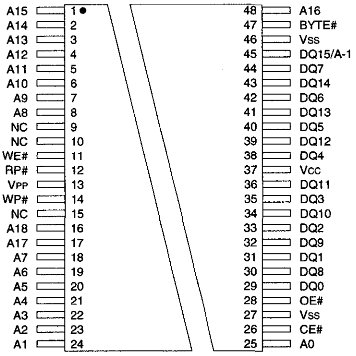
44-Pin SOP

(B-1)



48-Pin TSOP Type I

(C-3)



The MT28F800B1 is organized into eleven separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28F800B1 features a hardware-protected boot block. Writing or erasing the boot block requires either applying a super-voltage to the RP# pin or driving WP# HIGH in addition to executing the normal WRITE or ERASE sequences. This block may be used to store code implemented in low-level system

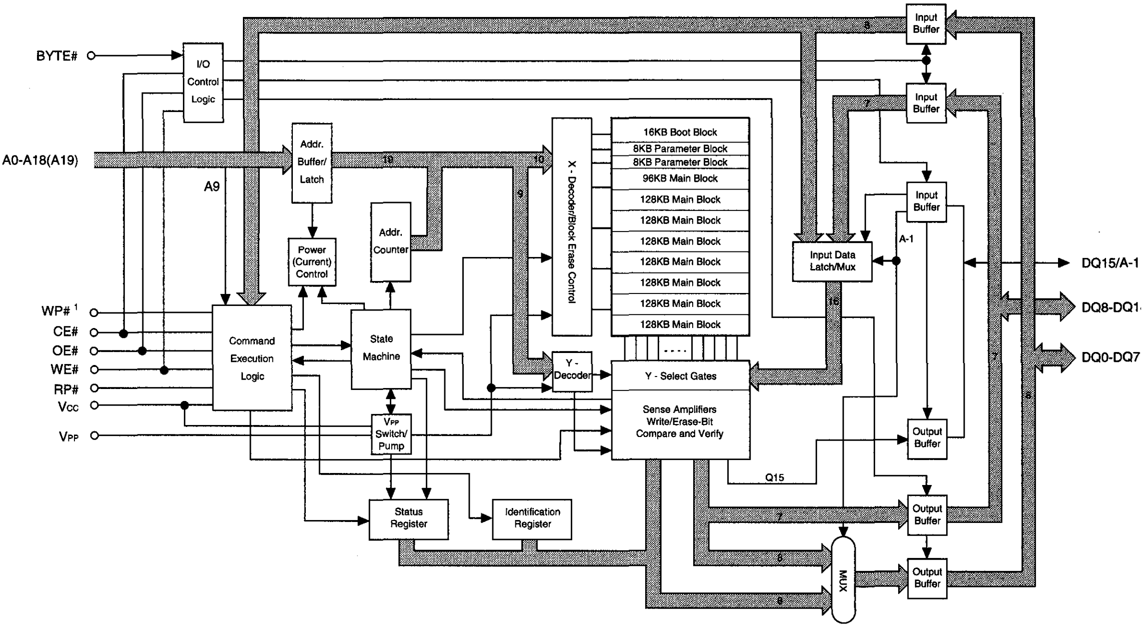
GENERAL DESCRIPTION (continued)

recovery. The remaining blocks vary in density and are written and erased with no additional security measures.

The byte or word address is issued to read the memory array with CE# and OE# LOW and WE# HIGH. Valid data is output until the next address is issued. The BYTE# pin is used to switch the data path between 8 bits wide and 16 bits wide. When BYTE# is LOW, the dual-use pin DQ15/A-1 becomes the lowest order address bit (A-1). When BYTE# i HIGH, the DQ15/A-1 pin becomes the most significan data bit (DQ15).

Please refer to Micron's Web site (www.micron.com flash/htmls/datasheets.html) for the latest full-length dat sheet.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. On MT28F800B1 WG only.

IN DESCRIPTIONS

SOP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
43	11	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
–	14	WP#	Input	Write Protect: Unlocks the boot block when HIGH if $V_{PP} = V_{PPH1}$ (5V) or V_{PPH2} (12V) and RP# = V_{IH} during a WRITE or ERASE. Does not affect WRITE or ERASE operation on other blocks.
12	26	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
44	12	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# unlocks the boot block and overrides the condition of WP# when at V_{HH} (12V), and must be held at V_{IH} during all other modes of operation.
14	28	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
33	47	BYTE#	Input	Byte Enable: If BYTE# = HIGH, the upper byte is active through DQ8-DQ15. If BYTE# = LOW, DQ8-DQ14 are High-Z, and all data is accessed through DQ0-DQ7. DQ15/A-1 becomes the least significant address input.
11, 10, 9, 8, 7, 6, 5, 4, 42, 41, 40, 39, 38, 37, 36, 35, 34, 3, 2	25, 24, 23, 22, 21, 20, 19, 18, 8, 7, 6, 5, 4, 3, 2, 1, 48, 17, 16	A0-A18	Input	Address Inputs: Select a unique 16-bit word out of the 524,288 available. The DQ15/A-1 input becomes the lowest order address when BYTE# = LOW to allow for a selection of an 8-bit byte from the 1,048,576 available.
31	45	DQ15/ A-1	Input/ Output	Data I/O: MSB of data when BYTE# = HIGH. Address Input: LSB of address input when BYTE# = LOW during READ or WRITE operation.
15, 17, 19, 21, 24, 26, 28, 30	29, 31, 33, 35, 38, 40, 42, 44	DQ0-DQ7	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE. These pins are used to input commands to the CEL.
16, 18, 20, 22, 25, 27, 29	30, 32, 34, 36, 39, 41, 43	DQ8-DQ14	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE when BYTE# = HIGH. These pins are High-Z when BYTE# is LOW.
–	9, 10, 15	NC	–	No Connect: These pins may be driven or left unconnected.
1	13	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the WRITE or ERASE, V_{PP} must be at V_{PPH1} (5V) or V_{PPH2} (12V). V_{PP} = "Don't Care" during all other operations.
23	37	V_{CC}	Supply	Power Supply: +5V ±10% or +3.3V ±0.3V.
13, 32	27, 46	V_{SS}	Supply	Ground.

TRUTH TABLE[1]

FUNCTION	RP#	CE#	OE#	WE#	WP#	BYTE#	A0	A9	V_{PP}	DQ0-DQ7	DQ8-DQ14	DQ15/A-1
Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
RESET	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
READ												
READ (word mode)	H	L	L	H	X	H	X	X	X	Data-Out	Data-Out	Data-Ou
READ (byte mode)	H	L	L	H	X	L	X	X	X	Data-Out	High-Z	A-1
Output Disable	H	L	H	H	X	X	X	X	X	High-Z	High-Z	High-Z
WRITE/ERASE (EXCEPT BOOT BLOCK)[2]												
ERASE SETUP	H	L	H	L	X	X	X	X	X	20H	X	X
ERASE CONFIRM[3]	H	L	H	L	X	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	X	10H/40H	X	X
WRITE (word mode)[4]	H	L	H	L	X	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (byte mode)[4]	H	L	H	L	X	L	X	X	V_{PPH}	Data-In	X	A-1
READ ARRAY[5]	H	L	H	L	X	X	X	X	X	FFH	X	X
WRITE/ERASE (BOOT BLOCK)[2, 7]												
ERASE SETUP	H	L	H	L	X	X	X	X	X	20H	X	X
ERASE CONFIRM[3]	V_{HH}	L	H	L	X	X	X	X	V_{PPH}	D0H	X	X
ERASE CONFIRM[3, 6]	H	L	H	L	H	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	X	10H/40H	X	X
WRITE (word mode)[4]	V_{HH}	L	H	L	X	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (word mode)[4, 6]	H	L	H	L	H	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (byte mode)[4]	V_{HH}	L	H	L	X	L	X	X	V_{PPH}	Data-In	X	A-1
WRITE (byte mode)[4, 6]	H	L	H	L	H	L	X	X	V_{PPH}	Data-In	X	A-1
READ ARRAY[5]	H	L	H	L	X	X	X	X	X	FFH	X	X
DEVICE IDENTIFICATION[8, 9]												
Manufacturer Compatibility (word mode)[10]	H	L	L	H	X	H	L	V_{ID}	X	89H	00H	–
Manufacturer Compatibility (byte mode)	H	L	L	H	X	L	L	V_{ID}	X	89H	High-Z	X
Device (word mode, top boot)[10]	H	L	L	H	X	H	H	V_{ID}	X	9CH	88H	–
Device (byte mode, top boot)	H	L	L	H	X	L	H	V_{ID}	X	9CH	High-Z	X
Device (word mode, bottom boot)[10]	H	L	L	H	X	H	H	V_{ID}	X	9DH	88H	–
Device (byte mode, bottom boot)	H	L	L	H	X	L	H	V_{ID}	X	9DH	High-Z	X

NOTE:

1. L = V_{IL} (LOW), H = V_{IH} (HIGH), X = V_{IL} or V_{IH} ("Don't Care").
2. $V_{PPH} = V_{PPH1} = 5V$ or $V_{PPH2} = 12V$.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. The READ ARRAY command must be issued befor reading the array after writing or erasing.
6. When WP# = V_{IH}, RP# may be at V_{IH} or V_{HH}.
7. $V_{HH} = 12V$.
8. $V_{ID} = 12V$; may also be read by issuing the IDENTIFY DEVICE command.
9. A1-A8, A10-A18 = V_{IL}.
10. Value reflects DQ8-DQ15.

MICRON
TECHNOLOGY, INC.

256K, 512K x 16
BOOT BLOCK FLASH MEMORY

FLASH MEMORY

MT28F400B5 ET, MT28F800B5 ET

Smart 5, Extended Temperature

FEATURES

- Extended temperature range operation: -40°C to +85°C
- Boot block architecture:
  - 16KB/4K-word boot block (protected)
  - Two 8KB/4K-word parameter blocks
  - Multiple 128KB/64K-word main blocks
- Smart 5 Voltage Technology:
  - 5V ±10% VCC
  - 5V ±10% or 12V ±5% VPP
- Address access time:
  - 80ns
- Available densities:
  - 4Mb, 8Mb
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence
- TSOP and SOP packaging options

OPTIONS

OPTIONS	MARKING
Timing	
80ns access	-8
Boot Block Starting Address	
Top	T
Bottom	B
Operating Temperature Range	
Extended (-40°C to +85°C)	ET
Packages	
Plastic SOP (600 mil)	SG
Plastic 48-pin TSOP Type 1 (12mm x 20mm)	WG

- Part Number Example: MT28F400B5WG-8 TET

GENERAL DESCRIPTION

The Micron® Smart 5 extended temperature flash memory amily consists of 4Mb and 8Mb, x16, boot block flash memories. They are fabricated with Micron's advanced CMOS floating-gate process. Device operation and features of the MT28F400B5 ET and MT28F800B5 ET are identical to he SmartVoltage commercial temperature MT28F400B1 and MT28F800B1 respectively, except that extended temperature range operation (-40°C to +85°C) is supported for all operations. For further information on device operation or features, refer to the MT28F400B1 or MT28F800B1 data heets.

PIN ASSIGNMENT (Top View)

44-Pin SOP
(B-1)

8Mb	4Mb	Pin	Pin	4Mb	8Mb
VPP	VPP	1	44	RP#	RP#
A18	WP#	2	43	WE#	WE#
A17	A17	3	42	A8	A8
A7	A7	4	41	A9	A9
A6	A6	5	40	A10	A10
A5	A5	6	39	A11	A11
A4	A4	7	38	A12	A12
A3	A3	8	37	A13	A13
A2	A2	9	36	A14	A14
A1	A1	10	35	A15	A15
A0	A0	11	34	A16	A16
CE#	CE#	12	33	BYTE#	BYTE#
Vss	Vss	13	32	Vss	Vss
OE#	OE#	14	31	DQ15/A-1	DQ15/A-1
DQ0	DQ0	15	30	DQ7	DQ7
DQ8	DQ8	16	29	DQ14	DQ14
DQ1	DQ1	17	28	DQ6	DQ6
DQ9	DQ9	18	27	DQ13	DQ13
DQ2	DQ2	19	26	DQ5	DQ5
DQ10	DQ10	20	25	DQ12	DQ12
DQ3	DQ3	21	24	DQ4	DQ4
DQ11	DQ11	22	23	Vcc	Vcc

48-Pin TSOP Type I
(C-3)

8Mb	4Mb	Pin	Pin	4Mb	8Mb
A15	A15	1	48	A16	A16
A14	A14	2	47	BYTE#	BYTE#
A13	A13	3	46	Vss	Vss
A12	A12	4	45	DQ15/A-1	DQ15/A-1
A11	A11	5	44	DQ7	DQ7
A10	A10	6	43	DQ14	DQ14
A9	A9	7	42	DQ6	DQ6
A8	A8	8	41	DQ13	DQ13
NC	NC	9	40	DQ5	DQ5
NC	NC	10	39	DQ12	DQ12
WE#	WE#	11	38	DQ4	DQ4
RP#	RP#	12	37	Vcc	Vcc
VPP	VPP	13	36	DQ11	DQ11
WP#	WP#	14	35	DQ3	DQ3
NC	NC	15	34	DQ10	DQ10
A18	NC	16	33	DQ2	DQ2
A17	A17	17	32	DQ9	DQ9
A7	A7	18	31	DQ1	DQ1
A6	A6	19	30	DQ8	DQ8
A5	A5	20	29	DQ0	DQ0
A4	A4	21	28	OE#	OE#
A3	A3	22	27	Vss	Vss
A2	A2	23	26	CE#	CE#
A1	A1	24	25	A0	A0

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest full-length data sheet.

FLASH MEMORY

MT28F400B1 VET, MT28F800B1 VET, MT28F004B1 VET, MT28F008B1 VET

Low Voltage, Extended Temperature

FEATURES

- Extended temperature range operation:
  -40°C to +85°C
- Boot block architecture:
  16KB/4K-word boot block (protected)
  Two 8KB/4K-word parameter blocks
  Multiple 128KB/64K-word main blocks
- Low-voltage operation:
  3.0V to 3.6V V_{CC}
  5V ±10% or 12V ±5% V_{PP}
- Address access time:
  100ns at 3.3V ±0.3V
- Available densities:
  4Mb, 8Mb
- Industry-standard pinouts
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence
- TSOP and FBGA* packaging options

OPTIONS	MARKING
• Timing	
100ns access	-10
• Boot Block Starting Address	
Top	T
Bottom	B
• Voltage	
3.0V to 3.6 V_{CC}	V
• Operating Temperature Range	
Extended (-40°C to +85°C)	ET
• Packages	
Plastic 40-pin TSOP Type 1 (10mm x 20mm)	VG
Plastic 48-pin TSOP Type 1 (12mm x 20mm)	WG
48-bump FBGA (8 x 6 ball grid)	FB*

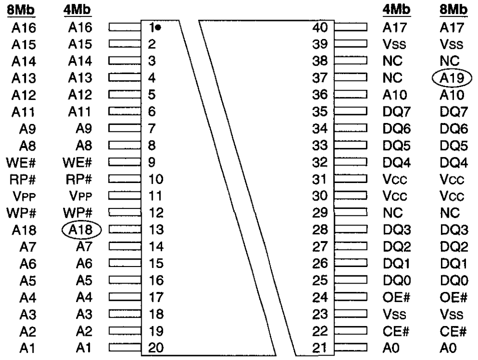
- Part Number Example: MT28F400B1WG-10 TVET

* MT28F800B1 VET only. Contact factory for availability.

PIN ASSIGNMENT (Top View)

40-Pin TSOP Type I

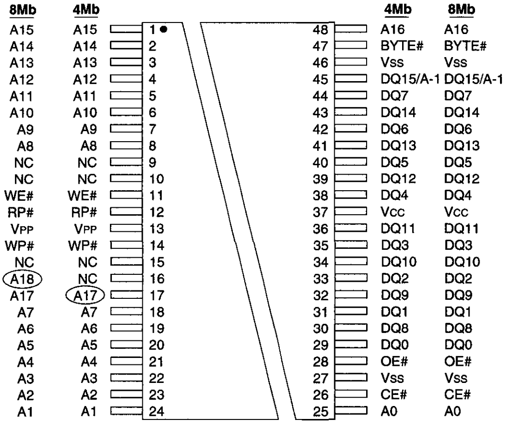
(C-2)



8Mb	4Mb	Pin	Pin	4Mb	8Mb
A16	A16	1	40	A17	A17
A15	A15	2	39	Vss	Vss
A14	A14	3	38	NC	NC
A13	A13	4	37	NC	A19
A12	A12	5	36	A10	A10
A11	A11	6	35	DQ7	DQ7
A9	A9	7	34	DQ6	DQ6
A8	A8	8	33	DQ5	DQ5
WE#	WE#	9	32	DQ4	DQ4
RP#	RP#	10	31	Vcc	Vcc
VPP	VPP	11	30	Vcc	Vcc
WP#	WP#	12	29	NC	NC
A18	A18	13	28	DQ3	DQ3
A7	A7	14	27	DQ2	DQ2
A6	A6	15	26	DQ1	DQ1
A5	A5	16	25	DQ0	DQ0
A4	A4	17	24	OE#	OE#
A3	A3	18	23	Vss	Vss
A2	A2	19	22	CE#	CE#
A1	A1	20	21	A0	A0

48-Pin TSOP Type I

(C-3)



8Mb	4Mb	Pin	Pin	4Mb	8Mb
A15	A15	1	48	A16	A16
A14	A14	2	47	BYTE#	BYTE#
A13	A13	3	46	Vss	Vss
A12	A12	4	45	DQ15/A-1	DQ15/A-1
A11	A11	5	44	DQ7	DQ7
A10	A10	6	43	DQ14	DQ14
A9	A9	7	42	DQ6	DQ6
A8	A8	8	41	DQ13	DQ13
NC	NC	9	40	DQ5	DQ5
NC	NC	10	39	DQ12	DQ12
WE#	WE#	11	38	DQ4	DQ4
RP#	RP#	12	37	Vcc	Vcc
VPP	VPP	13	36	DQ11	DQ11
WP#	WP#	14	35	DQ3	DQ3
NC	NC	15	34	DQ10	DQ10
A18	NC	16	33	DQ2	DQ2
A17	A17	17	32	DQ9	DQ9
A7	A7	18	31	DQ1	DQ1
A6	A6	19	30	DQ8	DQ8
A5	A5	20	29	DQ0	DQ0
A4	A4	21	28	OE#	OE#
A3	A3	22	27	Vss	Vss
A2	A2	23	26	CE#	CE#
A1	A1	24	25	A0	A0

GENERAL DESCRIPTION

The Micron® low voltage, extended temperature flash memory family consists of 4Mb and 8Mb boot block flash memories. They are fabricated with Micron's advanced CMOS floating-gate process. Device operation and features are identical to the commercial temperature equivalent except that extended temperature range operation (-40°C to +85°C) is supported for all operations. For further information on device operation or features, refer to the equivalent commercial temperature device data sheets.

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest full-length data sheet.

PRELIMINARY

MICRON TECHNOLOGY, INC.

8Mb SMART 3 BOOT BLOCK FLASH MEMORY

FLASH MEMORY

MT28F800B3
MT28F008B3

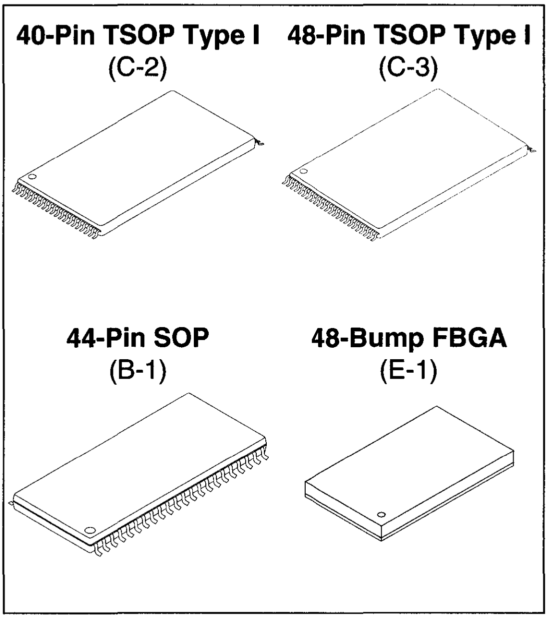
3V Only, Dual Supply (Smart 3)

FEATURES

- Boot block architecture:
  - 16KB/8K-word boot block (protected)
  - Two 8KB/4K-word parameter blocks
  - Eight main memory blocks
- 3V-only, dual-supply operation:
  - 3.0V to 3.6V VCC (100ns Commercial and Extended Temperatures)
  - 2.7V to 3.6V VCC (120ns Extended Temperature)
  - 3V (VPP ≥ VCC) or 5V VPP (100ns Commercial and Extended Temperatures)
  - 2.7V (VPP ≥ VCC) or 5V VPP (120ns Extended Temperature)
- 12V VPP tolerant
- Address access times:
  - 100ns at 3.0V to 3.6V VCC
  - 100ns at 3.0V to 3.6V VCC (-40°C to +85°C)
  - 120ns at 2.7Vto 3.6V VCC (-40°C to +85°C)
- Industry-standard pinouts
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence
- TSOP, SOP and FBGA packaging options
- Byte- or word-wide READ and WRITE (MT28F800B3):
  - 1 Meg x 8/512K x 16

OPTIONS	MARKING
Timing	
100ns (3.3V VCC)	-10
100ns (3.3V VCC)	-10 ET
120ns (2.7V to 3.6V VCC)	-12 VET
Configurations	
1 Meg x 8	MT28F008B3
512K x 16/1 Meg x 8	MT28F800B3
Boot Block Starting Address	
Top	T
Bottom	B
Operating Temperature Range	
Extended (-40°C to +85°C)	ET
Commercial (0°C to +70°C)	None
Packages	
Plastic 40-pin TSOP Type 1 (10mm x 20mm)	VG
Plastic 48-pin TSOP Type 1 (12mm x 20mm)	WG
Plastic SOP (600 mil)	SG
48-bump FBGA (6 x 8 ball grid; 0.8mm pitch)	FB

Part Marking Example: MT28F800B3WG-10 BET



GENERAL DESCRIPTION

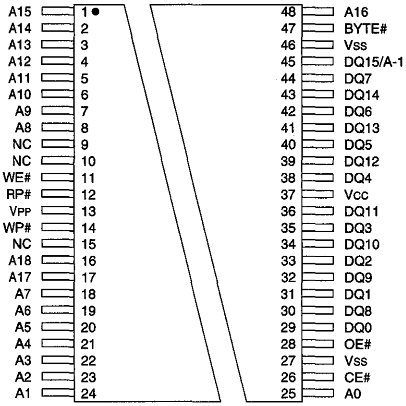
The MT28F008B3 (x8) and MT28F800B3 (x16/x8) are low voltage, nonvolatile, electrically block-erasable (flash), programmable read-only memories containing 8,388,608 bits organized as 524,288 words by 16 bits or 1,048,576 words by 8 bits. Depending on speed and temperature options, writing or erasing the device can be done with a VPP voltage ranging from 2.7V to 5V, and all other operations can be done with a VCC range from 2.7V to 3.6V. These devices are fabricated with Micron's advanced CMOS floating-gate process.

The MT28F008B3 and MT28F800B3 are organized into separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the devices feature a hardware-protected boot block. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density and are written and erased with no additional security measures.

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest full-length data sheet.

PIN ASSIGNMENT (Top View)

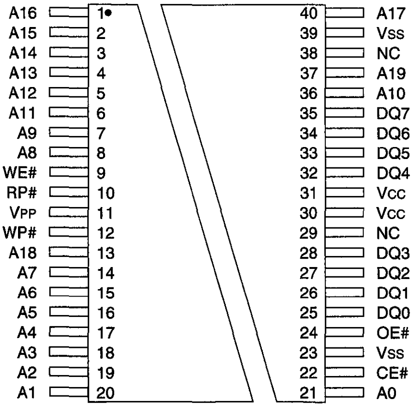
48-Pin TSOP Type I (C-3)



Signal	Pin	Pin	Signal
A15	1	48	A16
A14	2	47	BYTE#
A13	3	46	Vss
A12	4	45	DQ15/A-1
A11	5	44	DQ7
A10	6	43	DQ14
A9	7	42	DQ6
A8	8	41	DQ13
NC	9	40	DQ5
NC	10	39	DQ12
WE#	11	38	DQ4
RP#	12	37	Vcc
VPP	13	36	DQ11
WP#	14	35	DQ3
NC	15	34	DQ10
A18	16	33	DQ2
A17	17	32	DQ9
A7	18	31	DQ1
A6	19	30	DQ8
A5	20	29	DQ0
A4	21	28	OE#
A3	22	27	Vss
A2	23	26	CE#
A1	24	25	A0

ORDER NUMBER AND PART MARKING
MT28F800B3WG-10 B
MT28F800B3WG-10 T
MT28F800B3WG-10 BET
MT28F800B3WG-10 TET
MT28F800B3WG-12 BVET
MT28F800B3WG-12 TVET

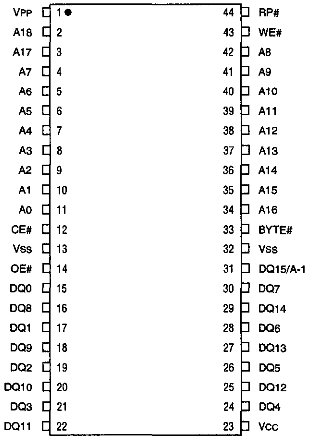
40-Pin TSOP Type I (C-2)



Signal	Pin	Pin	Signal
A16	1	40	A17
A15	2	39	Vss
A14	3	38	NC
A13	4	37	A19
A12	5	36	A10
A11	6	35	DQ7
A9	7	34	DQ6
A8	8	33	DQ5
WE#	9	32	DQ4
RP#	10	31	Vcc
VPP	11	30	Vcc
WP#	12	29	NC
A18	13	28	DQ3
A7	14	27	DQ2
A6	15	26	DQ1
A5	16	25	DQ0
A4	17	24	OE#
A3	18	23	Vss
A2	19	22	CE#
A1	20	21	A0

ORDER NUMBER AND PART MARKING
MT28F008B3VG-10 B
MT28F008B3VG-10 T
MT28F008B3VG-10 BET
MT28F008B3VG-10 TET
MT28F008B3VG-12 BVET
MT28F008B3VG-12 TVET

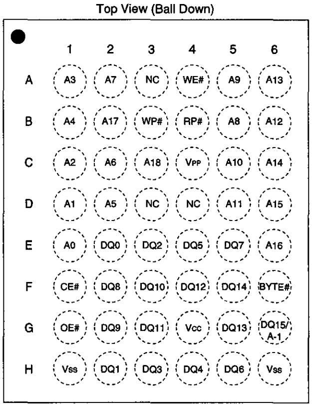
44-Pin SOP (B-1)



Signal	Pin	Pin	Signal
VPP	1	44	RP#
A18	2	43	WE#
A17	3	42	A8
A7	4	41	A9
A6	5	40	A10
A5	6	39	A11
A4	7	38	A12
A3	8	37	A13
A2	9	36	A14
A1	10	35	A15
A0	11	34	A16
CE#	12	33	BYTE#
Vss	13	32	Vss
OE#	14	31	DQ15/A-1
DQ0	15	30	DQ7
DQ8	16	29	DQ14
DQ1	17	28	DQ6
DQ9	18	27	DQ13
DQ2	19	26	DQ5
DQ10	20	25	DQ12
DQ3	21	24	DQ4
DQ11	22	23	Vcc

ORDER NUMBER AND PART MARKING
MT28F800B3SG-10 B
MT28F800B3SG-10 T
MT28F800B3SG-10 BET
MT28F800B3SG-10 TET
MT28F800B3SG-12 BVET
MT28F800B3SG-12 TVET

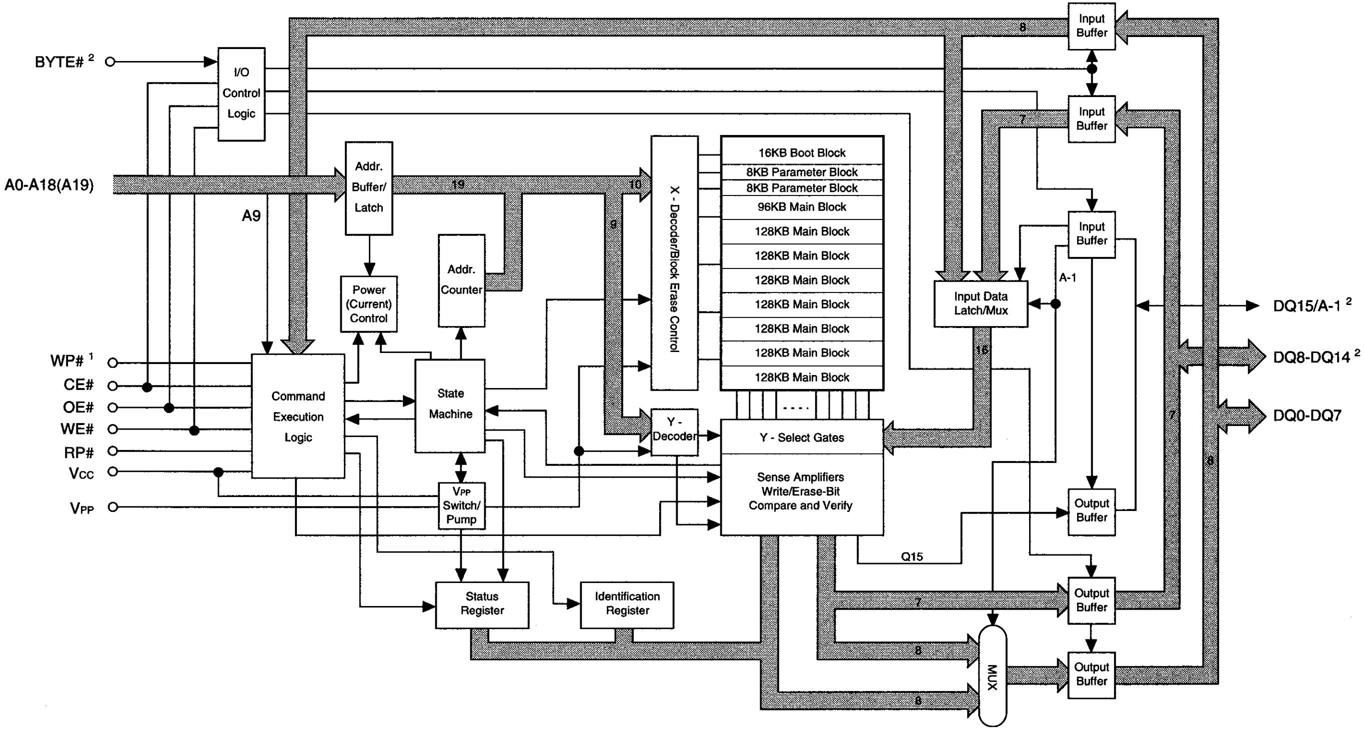
48-Bump FBGA (E-1)



	1	2	3	4	5	6
A	A3	A7	NC	WE#	A9	A13
B	A4	A17	WP#	RP#	A8	A12
C	A2	A6	A18	VPP	A10	A14
D	A1	A5	NC	NC	A11	A15
E	A0	DQ0	DQ2	DQ5	DQ7	A16
F	CE#	DQ8	DQ10	DQ12	DQ14	BYTE#
G	OE#	DQ9	DQ11	Vcc	DQ13	DQ15/A-1
H	Vss	DQ1	DQ3	DQ4	DQ6	Vss

ORDER NUMBER	PART MARKING
MT28F800B3FB-10 T	FBCDD
MT28F800B3FB-10 B	FCCDD
MT28F800B3FB-10 TET	FFCDD
MT28F800B3FB-10 BET	FGCDD
MT28F800B3FB-12 TVET	FHCDF
MT28F800B3FB-12 BVET	FJCDF

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. Does not apply to MT28F800B3SG.
2. Does not apply to MT28F008B3.

PIN DESCRIPTIONS

TSOP (48) PIN NUMBERS	TSOP (40) PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
11	9	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
14	12	WP#	Input	Write Protect: Unlocks the boot block when HIGH if $V_{PP} = V_{PPH1}$ (3V) or V_{PPH2} (5V) and RP# = V_{IH} during a WRITE or ERASE. Does not affect WRITE or ERASE operation on other blocks.
26	22	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
12	10	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# unlocks the boot block and overrides the condition of WP# when at V_{HH} (12V), and must be held at V_{IH} during all other modes of operation.
28	24	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
47	–	BYTE#	Input	Byte Enable: If BYTE# = HIGH, the upper byte is active through DQ8-DQ15. If BYTE# = LOW, DQ8-DQ14 are High-Z, and all data is accessed through DQ0-DQ7. DQ15/A-1 becomes the least significant address input.
25, 24, 23, 22, 21, 20, 19, 18, 8, 7, 6, 5, 4, 3, 2, 1, 48, 17, 16	21, 20, 19, 18, 17, 16, 15, 14, 8, 7, 36, 6, 5, 4, 3, 2, 1, 40, 13, 37	A0-A18/ (A19)	Input	Address Inputs: Select a unique 16-bit word or 8-bit byte. The DQ15/A-1 input becomes the lowest order address when BYTE# = LOW (MT28F800B3) to allow for a selection of an 8-bit byte from the 1,048,576 available.
45	–	DQ15/ A-1	Input/ Output	Data I/O: MSB of data when BYTE# = HIGH. Address Input: LSB of address input when BYTE# = LOW during READ or WRITE operation.
29, 31, 33, 35, 38, 40, 42, 44	25, 26, 27, 28, 32, 33, 34, 35	DQ0- DQ7	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE. These pins are used to input commands to the CEL.
30, 32, 34, 36, 39, 41, 43	–	DQ8- DQ14	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE when BYTE# = HIGH. These pins are High-Z when BYTE# is LOW.
9, 10, 15	29, 38	NC	–	No Connect: These pins may be driven or left unconnected.
13	11	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the WRITE or ERASE, V_{PP} must be at V_{PPH1} (3V), V_{PPH2} (5V) or V_{PPH3} (12V)[1]. V_{PP} = "Don't Care" during all other operations.
37	30, 31	V_{CC}	Supply	Power Supply: +3.3V ±0.3V or 2.7V-3.6V (VET version).
27, 46	23, 39	V_{SS}	Supply	Ground.

NOTE: 1. 12V V_{PP} may be used for a maximum of 100 WRITE/ERASE cycles and may be connected for a maximum of 100 hours.

PIN DESCRIPTIONS (continued)

SOP PIN NUMBERS	FBGA BUMP NUMBERS	SYMBOL	TYPE	DESCRIPTION
43	A4	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
–	B3	WP#	Input	Write Protect: Unlocks the boot block when HIGH if V_{PP} = V_{PPH1} (3V) or V_{PPH2} (5V) and RP# = V_{IH} during a WRITE or ERASE. Does not affect WRITE or ERASE operation on other blocks.
12	F1	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
44	B4	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# unlocks the boot block and overrides the condition of WP# when at V_{HH} (12V), and must be held at V_{IH} during all other modes of operation.
14	G1	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
33	F6	BYTE#	Input	Byte Enable: If BYTE# = HIGH, the upper byte is active through DQ8-DQ15. If BYTE# = LOW, DQ8-DQ14 are High-Z, and all data is accessed through DQ0-DQ7. DQ15/A-1 becomes the least significant address input.
11, 10, 9, 8, 7, 6, 5, 4, 42, 41, 40, 39, 38, 37, 36, 35, 34, 3, 2	E1, D1, C1, A1, B1, D2, C2, A2, B5, A5, C5, D5, B6, A6, C6, D6, E6, B2, C3	A0-A18/ (A19)	Input	Address Inputs: Select a unique 16-bit word or 8-bit byte. The DQ15/A-1 input becomes the lowest order address when BYTE# = LOW (MT28F800B3) to allow for a selection of an 8-bit byte from the 1,048,576 available.
31	G6	DQ15/ A-1	Input/ Output	Data I/O: MSB of data when BYTE# = HIGH. Address Input: LSB of address input when BYTE# = LOW during READ or WRITE operation.
15, 17, 19, 21, 24, 26, 28, 30	E2, H2, E3, H3, H4, E4, H5, E5	DQ0-DQ7	Input/ Output	Data I/Os: Data output during any READ operation or data input during a WRITE. These pins are used to input commands to the CEL.
16, 18, 20, 22, 25, 27, 29	F2, G2, F3, G3, F4, G5, F5	DQ8-DQ14	Input/ Output	Data I/Os: Data output during any READ operation or data input during a WRITE when BYTE# = HIGH. These pins are High-Z when BYTE# is LOW.
–	A3, D3, D4	NC	–	No Connect: These bumps may be driven or left unconnected.

PIN DESCRIPTIONS (continued)

SOP PIN NUMBERS	FBGA BUMP NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	C4	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the WRITE or ERASE, V_{PP} must be at V_{PPH1} (3V), V_{PPH2} (5V) or V_{PPH3} (12V)[1]. V_{PP} = "Don't Care" during all other operations.
23	G4	V_{CC}	Supply	Power Supply: +3.3V ±0.3V or 2.7V-3.6V (VET version).
13, 32	H1, H6	V_{SS}	Supply	Ground.

NOTE: 1. 12V V_{PP} may be used for a maximum of 100 WRITE/ERASE cycles and may be connected for a maximum of 100 hours.

TRUTH TABLE (MT28F800B3)[1]

FUNCTION	RP#	CE#	OE#	WE#	WP#	BYTE#	A0	A9	V_{PP}	DQ0-DQ7	DQ8-DQ14	DQ15/A-1
Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
RESET	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
READ												
READ (word mode)	H	L	L	H	X	H	X	X	X	Data-Out	Data-Out	Data-Out
READ (byte mode)	H	L	L	H	X	L	X	X	X	Data-Out	High-Z	A-1
Output Disable	H	L	H	H	X	X	X	X	X	High-Z	High-Z	High-Z
WRITE/ERASE (EXCEPT BOOT BLOCK)[2]												
ERASE SETUP	H	L	H	L	X	X	X	X	X	20H	X	X
ERASE CONFIRM[3]	H	L	H	L	X	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	X	10H/40H	X	X
WRITE (word mode)[4]	H	L	H	L	X	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (byte mode)[4]	H	L	H	L	X	L	X	X	V_{PPH}	Data-In	X	A-1
READ ARRAY[5]	H	L	H	L	X	X	X	X	X	FFH	X	X
WRITE/ERASE (BOOT BLOCK)[2, 7]												
ERASE SETUP	H	L	H	L	X	X	X	X	X	20H	X	X
ERASE CONFIRM[3]	V_{HH}	L	H	L	X	X	X	X	V_{PPH}	D0H	X	X
ERASE CONFIRM[3, 6]	H	L	H	L	H	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	X	10H/40H	X	X
WRITE (word mode)[4]	V_{HH}	L	H	L	X	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (word mode)[4, 6]	H	L	H	L	H	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (byte mode)[4]	V_{HH}	L	H	L	X	L	X	X	V_{PPH}	Data-In	X	A-1
WRITE (byte mode)[4, 6]	H	L	H	L	H	L	X	X	V_{PPH}	Data-In	X	A-1
READ ARRAY[5]	H	L	H	L	X	X	X	X	X	FFH	X	X
DEVICE IDENTIFICATION[8, 9]												
Manufacturer Compatibility (word mode)[10]	H	L	L	H	X	H	L	V_{ID}	X	89H	00H	–
Manufacturer Compatibility (byte mode)	H	L	L	H	X	L	L	V_{ID}	X	89H	High-Z	X
Device (word mode, top boot)[10]	H	L	L	H	X	H	H	V_{ID}	X	9CH	88H	–
Device (byte mode, top boot)	H	L	L	H	X	L	H	V_{ID}	X	9CH	High-Z	X
Device (word mode, bottom boot)[10]	H	L	L	H	X	H	H	V_{ID}	X	9DH	88H	–
Device (byte mode, bottom boot)	H	L	L	H	X	L	H	V_{ID}	X	9DH	High-Z	X

NOTE:

1. L = V_{IL} (LOW), H = V_{IH} (HIGH), X = V_{IL} or V_{IH} ("Don't Care").
2. V_{PPH} = V_{PPH1} = 3V or V_{PPH2} = 5V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. The READ ARRAY command must be issued before reading the array after writing or erasing.
6. When WP# = V_{IH}, RP# may be at V_{IH} or V_{HH}.
7. V_{HH} = 12V.
8. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE command.
9. A1-A8, A10-A18 = V_{IL}.
10. Value reflects DQ8-DQ15.

TRUTH TABLE (MT28F008B3)[1]

FUNCTION	RP#	CE#	OE#	WE#	WP#	A0	A9	V_{PP}	DQ0-DQ7
Standby	H	H	X	X	X	X	X	X	High-Z
RESET	L	X	X	X	X	X	X	X	High-Z
READ									
READ	H	L	L	H	X	X	X	X	Data-Out
Output Disable	H	L	H	H	X	X	X	X	High-Z
WRITE/ERASE (EXCEPT BOOT BLOCK)[2]									
ERASE SETUP	H	L	H	L	X	X	X	X	20H
ERASE CONFIRM[3]	H	L	H	L	X	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H
WRITE[4]	H	L	H	L	X	X	X	V_{PPH}	Data-In
READ ARRAY[5]	H	L	H	L	X	X	X	X	FFH
WRITE/ERASE (BOOT BLOCK)[2, 7]									
ERASE SETUP	H	L	H	L	X	X	X	X	20H
ERASE CONFIRM[3]	V_{HH}	L	H	L	X	X	X	V_{PPH}	D0H
ERASE CONFIRM[3, 6]	H	L	H	L	H	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H
WRITE[4]	V_{HH}	L	H	L	X	X	X	V_{PPH}	Data-In
WRITE[4, 6]	H	L	H	L	H	X	X	V_{PPH}	Data-In
READ ARRAY[5]	H	L	H	L	X	X	X	X	FFH
DEVICE IDENTIFICATION[8, 9]									
Manufacturer Compatibility	H	L	L	H	X	L	V_{ID}	X	89H
Device (top boot)	H	L	L	H	X	H	V_{ID}	X	98H
Device (bottom boot)	H	L	L	H	X	H	V_{ID}	X	99H

NOTE:
1. L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}.
2. V_{PPH} = V_{PPH1} = 3V or V_{PPH2} = 5V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. The READ ARRAY command must be issued before reading the array after writing or erasing.
6. When WP# = V_{IH}, RP# may be at V_{IH} or V_{HH}.
7. V_{HH} = 12V.
8. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE command.
9. A1-A8, A10-A19 = V_{IL}.

FLASH MEMORY

MT28F800B5
MT28F008B5

5V Only, Dual Supply (Smart 5)

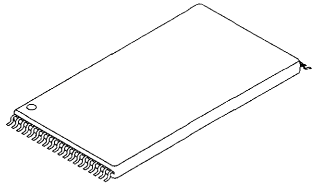
FEATURES

- Boot block architecture:
  16KB/8K-word boot block (protected)
  Two 8KB/4K-word parameter blocks
  Eight main memory blocks
- 5V-only, dual-supply operation:
  5V ±10% V_{CC}
  5V ±10% V_{PP} (12V V_{PP} tolerant)
- Address access time:
  80ns
- Industry-standard pinouts
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence
- TSOP and SOP packaging options
- Byte- or word-wide READ and WRITE (MT28F800B5):
  1 Meg x 8/512K x 16

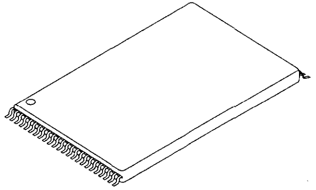
OPTIONS	MARKING
• Timing	
80ns	-8
• Configurations	
1 Meg x 8	MT28F008B5
512K x 16/1 Meg x 8	MT28F800B5
• Boot Block Starting Address	
Top	T
Bottom	B
• Operating Temperature Range	
Extended (-40°C to +85°C)	ET
Commercial (0°C to +70°C)	None
• Packages	
Plastic 40-pin TSOP Type 1 (10mm x 20mm)	VG
Plastic 48-pin TSOP Type 1 (12mm x 20mm)	WG
Plastic SOP (600 mil)	SG

- Part Marking Example: MT28F800B5WG-8 BET

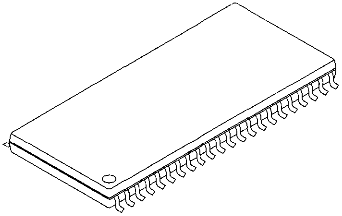
40-Pin TSOP Type I
(C-2)



48-Pin TSOP Type I
(C-3)



44-Pin SOP
(B-1)



GENERAL DESCRIPTION

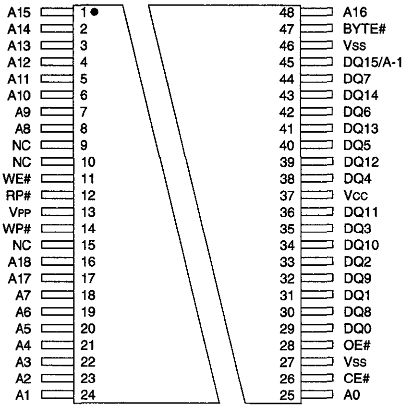
The MT28F008B5 (x8) and MT28F800B5 (x16/x8) are nonvolatile, electrically block-erasable (flash), programmable read-only memories containing 8,388,608 bits organized as 524,288 words by 16 bits or 1,048,576 words by 8 bits. Writing or erasing the device is done with a 5V V_{PP} voltage (12V-tolerant), while all operations are performed with a 5V V_{CC} ($V_{PP} \geq V_{CC}$). 12V V_{PP} may be used for a mximum of 100 WRITE/ERASE cycles and may be connected for a maximum of 100 hours. These devices are fabricated with Micron's advanced CMOS floating-gate process.

The MT28F008B5 and MT28F800B5 are organized into separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the device features a hardware-protected boot block. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density and are written and erased with no additional security measures.

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest full-length data sheet.

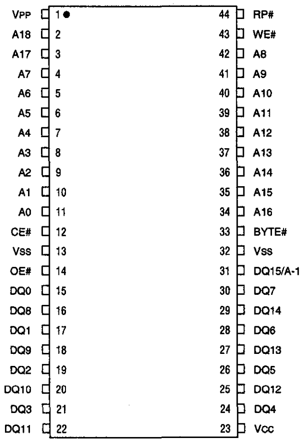
PIN ASSIGNMENT (Top View)

48-Pin TSOP Type I (C-3)



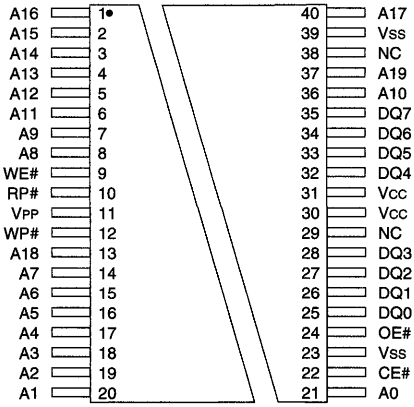
ORDER NUMBER AND PART MARKING
MT28F800B5WG-8 B
MT28F800B5WG-8 T
MT28F800B5WG-8 BET
MT28F800B5WG-8 TET

44-Pin SOP (B-1)



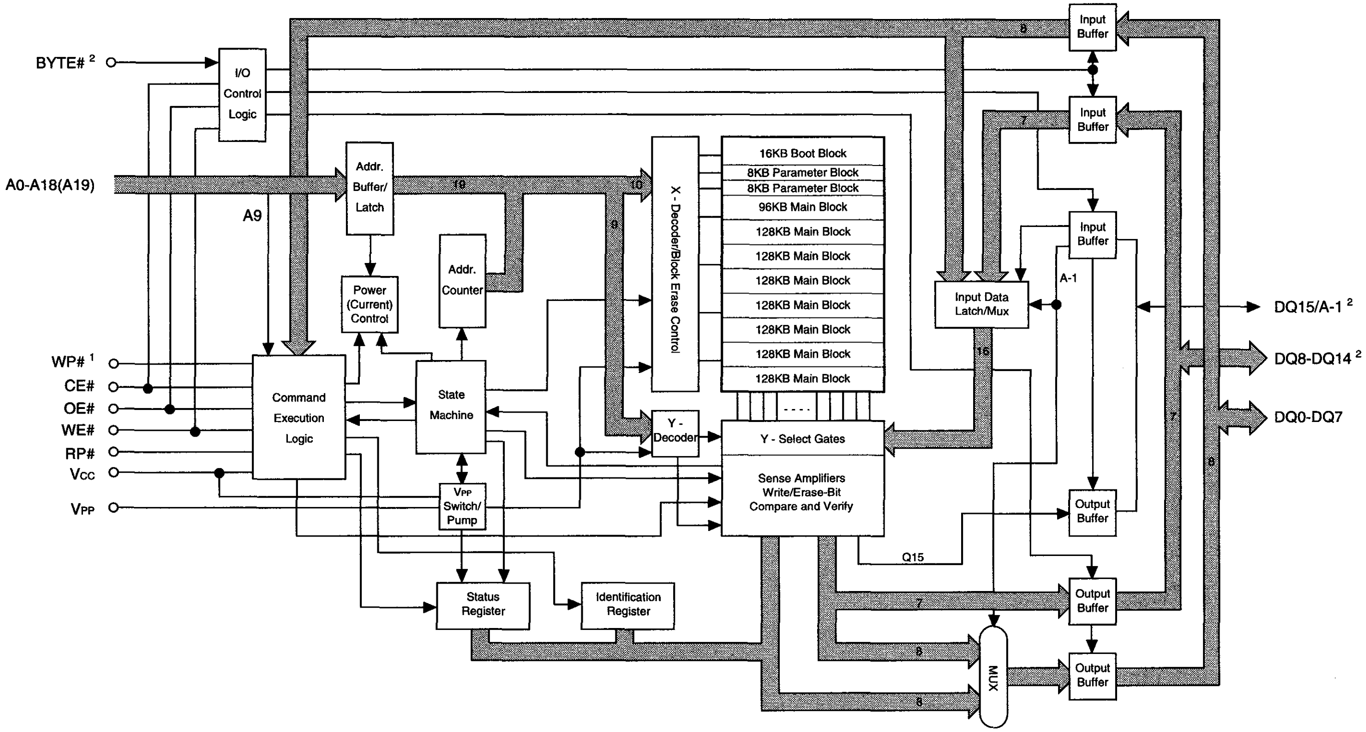
ORDER NUMBER AND PART MARKING
MT28F800B5SG-8 B
MT28F800B5SG-8 T
MT28F800B5SG-8 BET
MT28F800B5SG-8 TET

40-Pin TSOP Type I (C-2)



ORDER NUMBER AND PART MARKING
MT28F008B5VG-8 B
MT28F008B5VG-8 T
MT28F008B5VG-8 BET
MT28F008B5VG-8 TET

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. Does not apply to MT28F800B5SG.
2. Does not apply to MT28F008B5.

PIN DESCRIPTIONS

TSOP (48) PIN NUMBERS	TSOP (40) PIN NUMBERS	SOP (44) PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
11	9	43	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
14	12	–	WP#	Input	Write Protect: Unlocks the boot block when HIGH if V_{PP} = V_{PPH1} (5V) or V_{PPH2} (12V) and RP# = V_{IH} during a WRITE or ERASE. Does not affect WRITE or ERASE operation on other blocks.
26	22	12	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
12	10	44	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# unlocks the boot block and overrides the condition of WP# when at V_{HH} (12V)[1], and must be held at V_{IH} during all other modes of operation.
28	24	14	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
47	–	33	BYTE#	Input	Byte Enable: If BYTE# = HIGH, the upper byte is active through DQ8-DQ15. If BYTE# = LOW, DQ8-DQ14 are High-Z, and all data is accessed through DQ0-DQ7. DQ15/A-1 becomes the least significant address input.
25, 24, 23, 22, 21, 20, 19, 18, 8, 7, 6, 5, 4, 3, 2, 1, 48, 17, 16	21, 20, 19, 18, 17, 16, 15, 14, 8, 7, 36, 6, 5, 4, 3, 2, 1, 40, 13, 37	11, 10, 9, 8, 7, 6, 5, 4, 42, 41, 40, 39, 38, 37, 36, 35, 34, 3, 2	A0-A18/ (A19)	Input	Address Inputs: Select a unique 16-bit word or 8-bit byte. The DQ15/A-1 input becomes the lowest order address when BYTE# = LOW (MT28F800B5) to allow for a selection of an 8-bit byte from the 1,048,576 available.
45	–	31	DQ15/ A-1	Input/ Output	Data I/O: MSB of data when BYTE# = HIGH. Address Input: LSB of address input when BYTE# = LOW during READ or WRITE operation.
29, 31, 33, 35, 38, 40, 42, 44	25, 26, 27, 28, 32, 33, 34, 35	15, 17, 19, 21, 24, 26, 28, 30	DQ0-DQ7	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE. These pins are used to input commands to the CEL.
30, 32, 34, 36, 39, 41, 43	–	16, 18, 20, 22, 25, 27, 29	DQ8-DQ14	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE when BYTE# = HIGH. These pins are High-Z when BYTE# is LOW.

NOTE: 1. 12V V_{PP} may be used for a maximum of 100 WRITE/ERASE cycles and may be connected for a maximum of 100 hours.

IN DESCRIPTIONS (continued)

TSOP (48) PIN NUMBERS	TSOP (40) PIN NUMBERS	SOP (44) PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
9, 10, 15	29, 38	–	NC	–	No Connect: These pins may be driven or left unconnected.
13	11	1	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the WRITE or ERASE, V_{PP} must be at V_{PPH1} (5V) or V_{PPH2} (12V)[1]. V_{PP} = “Don’t Care” during all other operations.
37	30, 31	23	V_{CC}	Supply	Power Supply: +5V ±10%.
27, 46	23, 39	13, 32	V_{SS}	Supply	Ground.

OTE: 1. 12V V_{PP} may be used for a maximum of 100 WRITE/ERASE cycles and may be connected for a maximum of 100 hours.

TRUTH TABLE (MT28F800B5)[1]

FUNCTION	RP#	CE#	OE#	WE#	WP#	BYTE#	A0	A9	V_{PP}	DQ0-DQ7	DQ8-DQ14	DQ15/A-1
Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
RESET	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
READ												
READ (word mode)	H	L	L	H	X	H	X	X	X	Data-Out	Data-Out	Data-Ou
READ (byte mode)	H	L	L	H	X	L	X	X	X	Data-Out	High-Z	A-1
Output Disable	H	L	H	H	X	X	X	X	X	High-Z	High-Z	High-Z
WRITE/ERASE (EXCEPT BOOT BLOCK)[2]												
ERASE SETUP	H	L	H	L	X	X	X	X	X	20H	X	X
ERASE CONFIRM[3]	H	L	H	L	X	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	X	10H/40H	X	X
WRITE (word mode)[4]	H	L	H	L	X	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (byte mode)[4]	H	L	H	L	X	L	X	X	V_{PPH}	Data-In	X	A-1
READ ARRAY[5]	H	L	H	L	X	X	X	X	X	FFH	X	X
WRITE/ERASE (BOOT BLOCK)[2, 7]												
ERASE SETUP	H	L	H	L	X	X	X	X	X	20H	X	X
ERASE CONFIRM[3]	V_{HH}	L	H	L	X	X	X	X	V_{PPH}	D0H	X	X
ERASE CONFIRM[3, 6]	H	L	H	L	H	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	X	10H/40H	X	X
WRITE (word mode)[4]	V_{HH}	L	H	L	X	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (word mode)[4, 6]	H	L	H	L	H	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (byte mode)[4]	V_{HH}	L	H	L	X	L	X	X	V_{PPH}	Data-In	X	A-1
WRITE (byte mode)[4, 6]	H	L	H	L	H	L	X	X	V_{PPH}	Data-In	X	A-1
READ ARRAY[5]	H	L	H	L	X	X	X	X	X	FFH	X	X
DEVICE IDENTIFICATION[8, 9]												
Manufacturer Compatibility (word mode)[10]	H	L	L	H	X	H	L	V_{ID}	X	89H	00H	–
Manufacturer Compatibility (byte mode)	H	L	L	H	X	L	L	V_{ID}	X	89H	High-Z	X
Device (word mode, top boot)[10]	H	L	L	H	X	H	H	V_{ID}	X	9CH	88H	–
Device (byte mode, top boot)	H	L	L	H	X	L	H	V_{ID}	X	9CH	High-Z	X
Device (word mode, bottom boot)[10]	H	L	L	H	X	H	H	V_{ID}	X	9DH	88H	–
Device (byte mode, bottom boot)	H	L	L	H	X	L	H	V_{ID}	X	9DH	High-Z	X

NOTE:
1. L = V_{IL} (LOW), H = V_{IH} (HIGH), X = V_{IL} or V_{IH} ("Don't Care").
2. $V_{PPH} = V_{PPH1} = 5V$ or $V_{PPH2} = 12V$.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. The READ ARRAY command must be issued before reading the array after writing or erasing.
6. When WP# = V_{IH}, RP# may be at V_{IH} or V_{HH}.
7. $V_{HH} = 12V$.
8. $V_{ID} = 12V$; may also be read by issuing the IDENTIFY DEVICE command.
9. A1-A8, A10-A18 = V_{IL}.
10. Value reflects DQ8-DQ15.

'RUTH TABLE (MT28F008B5)[1]

FUNCTION	RP#	CE#	OE#	WE#	WP#	A0	A9	V_{PP}	DQ0-DQ7
Standby	H	H	X	X	X	X	X	X	High-Z
RESET	L	X	X	X	X	X	X	X	High-Z
READ									
READ	H	L	L	H	X	X	X	X	Data-Out
Output Disable	H	L	H	H	X	X	X	X	High-Z
WRITE/ERASE (EXCEPT BOOT BLOCK)[2]									
ERASE SETUP	H	L	H	L	X	X	X	X	20H
ERASE CONFIRM[3]	H	L	H	L	X	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H
WRITE[4]	H	L	H	L	X	X	X	V_{PPH}	Data-In
READ ARRAY[5]	H	L	H	L	X	X	X	X	FFH
WRITE/ERASE (BOOT BLOCK)[2, 7]									
ERASE SETUP	H	L	H	L	X	X	X	X	20H
ERASE CONFIRM[3]	V_{HH}	L	H	L	X	X	X	V_{PPH}	D0H
ERASE CONFIRM[3, 6]	H	L	H	L	H	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H
WRITE[4]	V_{HH}	L	H	L	X	X	X	V_{PPH}	Data-In
WRITE[4, 6]	H	L	H	L	H	X	X	V_{PPH}	Data-In
READ ARRAY[5]	H	L	H	L	X	X	X	X	FFH
DEVICE IDENTIFICATION[8, 9]									
Manufacturer Compatibility	H	L	L	H	X	L	V_{ID}	X	89H
Device (top boot)	H	L	L	H	X	H	V_{ID}	X	98H
Device (bottom boot)	H	L	L	H	X	H	V_{ID}	X	99H

IOTE:
1. L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}.
2. $V_{PPH} = V_{PPH1} = 5V$ or $V_{PPH2} = 12V$.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. The READ ARRAY command must be issued before reading the array after writing or erasing.
6. When WP# = V_{IH}, RP# may be at V_{IH} or V_{HH}.
7. $V_{HH} = 12V$.
8. $V_{ID} = 12V$; may also be read by issuing the IDENTIFY DEVICE command.
9. A1-A8, A10-A19 = V_{IL}.

EVEN-SECTORED FLASH MEMORY PRODUCT SELECTION GUIDE

Memory Configuration	Features/ Options	Part Number	Voltage	Maximum Current Draw		Package/# of Pins		Page
				Standby	Active	SOP	TSOP	
2 Meg x 8	SE, AUTO, DPD	MT28F016S5	5V Only	100µA	50mA	–	40	3-47

AUTO = Automated W/E Algorithm, SE = Even Sectored, DPD = Deep Power-Down

ADVANCE

MICRON TECHNOLOGY, INC.

2 MEG x 8
EVEN-SECTORED FLASH MEMORY

FLASH MEMORY

MT28F016S5

5V Only, Dual Supply (Smart 5)

FEATURES

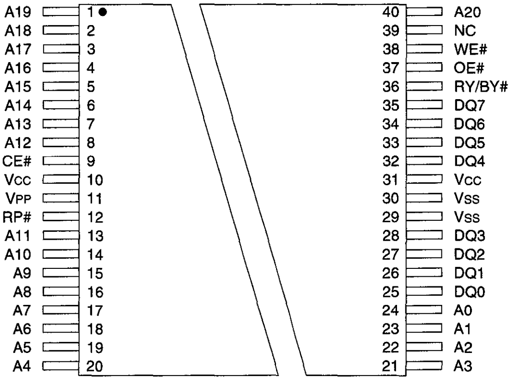
- Thirty-two 64KB erase blocks
- Deep Power-Down Mode:
  10µA MAX
- Smart 5 voltage:
  5V ±10% Vcc
  5V ±10% VPP (12V VPP tolerant)
- Address access times:
  90ns, 120ns at 5V Vcc
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence

OPTIONS	MARKING
• Timing (5V Vcc)	
90ns access	-9
120ns access	-12
• Package	
Plastic 40-pin TSOP Type 1 (10mm x 20mm)	VG

- Part Number Example: MT28F016S5VG-9

PIN ASSIGNMENT (Top View)

40-Pin TSOP Type I
(C-2)



GENERAL DESCRIPTION

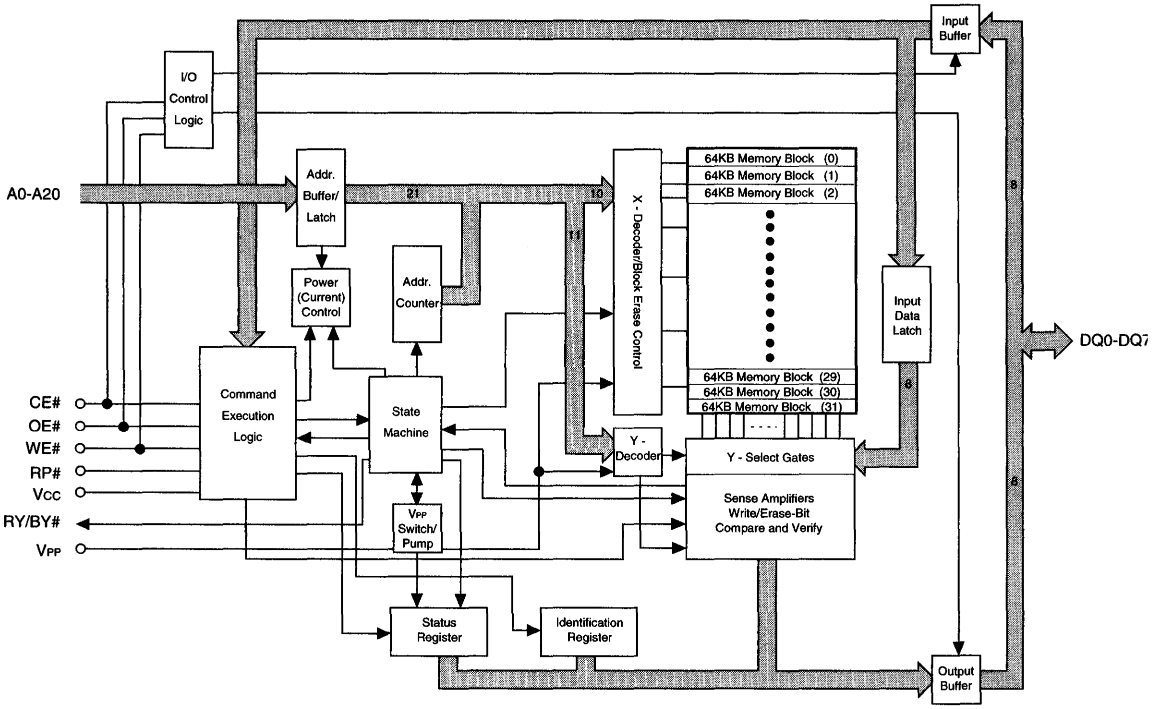
The MT28F016S5 is a nonvolatile, electrically block-erasable (flash), programmable, read-only memory containing 16,777,216 bits. Writing or erasing the device is done with 5V VPP voltage, which is 12V VPP tolerant, while all operations are performed with 5V Vcc (VPP ≥ Vcc). It is fabricated with Micron's advanced CMOS floating-gate process.

The MT28F016S5 is organized into 32 separately erasable blocks. ERASEs may be interrupted to allow other operations with the ERASE SUSPEND command. After the ERASE SUSPEND command is issued, READ operations may be executed.

Operations are executed with commands from an industry-standard command set. In addition to status register polling, the MT28F016S5 provides a READY/BUSY# (RY/BY#) output to indicate WRITE and ERASE completion.

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest full-length data sheet.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
38	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
9	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
12	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# must be held at V_{IH} during all other modes of operation.
37	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 8, 7, 6, 5, 4, 3, 2, 1, 40	A0-A20	Input	Address Inputs: Select a unique, 8-bit byte out of the 2,097,152 available.
36	RY/BY#	Output	Ready/Busy: Indicates the status of internal state machine. When RY/BY# = V_{OL}, the ISM is busy processing a command. If RY/BY# = V_{OH}, the ISM is ready to accept a new command. During deep power-down, device configuration read or erase suspend, RY/BY# = V_{OH}. Output is always active.
25, 26, 27, 28, 32, 33, 34, 35	DQ0-DQ7	Input/ Output	Data I/O: Data output pins during any READ operation or data input pins during a WRITE. Used to input commands to the CEL.
39	NC	–	No Connect: This pin may be driven or left unconnected.
11	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the operation, V_{PP} must be at V_{PPH} (5V) ($V_{PP} \geq V_{CC}$). V_{PP} = "Don't Care" during all other operations.
10, 31	V_{CC}	Supply	Power Supply: +5V ±10%.
29, 30	V_{SS}	Supply	Ground.

TRUTH TABLE[1]

FUNCTION	RP#	CE#	OE#	WE#	Address	V_{PP}	DQ0-DQ7	RY/BY#
Standby	H	H	X	X	X	X	High-Z	V_{OH}
Deep Power-Down/Reset	L	X	X	X	X	X	High-Z	V_{OH}
READ								
READ	H	L	L	H	X	X	Data-Out	V_{OH}
Output Disable	H	L	H	H	X	X	High-Z	V_{OH}
WRITE/ERASE [2, 3]								
ERASE SETUP	H	L	H	L	X	X	20H	V_{OH}
ERASE CONFIRM [4]	H	L	H	L	BA	V_{PPH}	D0H	$V_{OH} \rightarrow V_{OL}$
WRITE SETUP	H	L	H	L	X	X	10H/40H	V_{OH}
WRITE [5]	H	L	H	L	WA	V_{PPH}	Data-In	$V_{OH} \rightarrow V_{OL}$
READ ARRAY [6]	H	L	H	L	X	X	FFH	V_{OH}
DEVICE CONFIGURATION								
Manufacturer Compatibility	H	L	L	H	000000H	X	89H	V_{OH}
Device ID	H	L	L	H	000001H	X	A0H	V_{OH}

NOTE:
1. L = V_{IL} (LOW), H = V_{IH} (HIGH), X = V_{IL} or V_{IH} ("Don't Care").
2. V_{PPH} = 5V.
3. BA = Block Address; WA = Write Address.
4. Operation must be preceded by ERASE SETUP command.
5. Operation must be preceded by WRITE SETUP command.
6. The READ ARRAY command must be issued before reading the array after writing or erasing.

FLASH CARD PRODUCT SELECTION GUIDE

Card Density	Operating Voltage	Form Factor	Interface	Page
4MB	3.3V or 5V	CompactFlash Card	16-bit PC Card ATA and/or ATA (IDE) Compatible	3-51
8MB	3.3V or 5V	CompactFlash Card	16-bit PC Card ATA and/or ATA (IDE) Compatible	3-51
10MB	3.3V or 5V	CompactFlash Card	16-bit PC Card ATA and/or ATA (IDE) Compatible	3-51
15MB	3.3V or 5V	CompactFlash Card	16-bit PC Card ATA and/or ATA (IDE) Compatible	3-51

COMPACTFLASH™

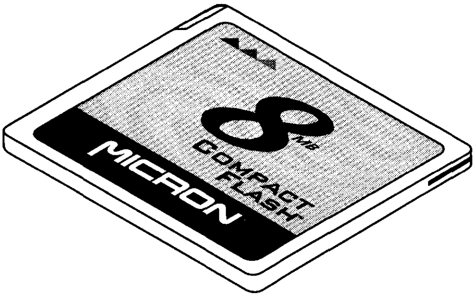
MTCF004A, MTCF008A, MTCF010A, MTCF015A

COMPACTFLASH ATA/ATA (IDE)

EATURES

- Implements highly integrated memory controller:
  - Fully compatible with CompactFlash™ specification
  - ATA (IDE) compatible
  - 16-bit PC Card ATA standard with optional adapter
  - Also PCMCIA 2.1 compatible with optional adapter
- Smallest ATA-compatible form factor: (36.4mm x 42.8mm x 3.3mm)
- Uses standard ATA software drivers; no additional software drivers required
- High reliability:
  - No moving parts
  - Noiseless
  - 10,000 card insertions/removals
  - 500,000 hours MTBF
  - High shock and vibration tolerance
- Powerful Reed-Solomon error detection and correction
- Optimized power consumption:
  - Selectable based on performance and power requirements
  - Automatic sleep mode with fast wake-up
- Supports standard power-management commands:
  - POWER-DOWN command
  - SLEEP command
- High performance:
  - 6 MB/s burst rate
  - Multiple mode supported for fast data transfers (two sectors/block)
- Available densities:
  - 4MB, 8MB, 10MB, 15MB
- 3.3V or 5V supply voltage (no 12V required)

COMPACTFLASH CARD
(G-1)



GENERAL DESCRIPTION

The Micron® CompactFlash Card is a small form factor, 0-pin connector, solid-state disk card with densities nging from 4MB to 15MB. Maximum compatibility across arious platforms is ensured since the CompactFlash Card nplements an industry-standard PCMCIA ATA- and IDE-ompatible electrical interface. Additionally, the card is echanically and electrically compliant with the ompactFlash Association (CFA) CompactFlash specifica-on. Micron's 40 megabit flash memory is implemented on e card, which is specifically designed for high-erformance, low-cost, mass-storage applications.

Micron's CompactFlash Card can be used in any applica-on designed for the CompactFlash specification. Though it maintains compatibility with the electrical interface of a standard PCMCIA card, CompactFlash has a 66 percent smaller form factor that makes it an ideal choice for space-constrained, portable applications. With a 50-pin to 68-pin PCMCIA adapter, the CompactFlash Card can be used in any Type II or Type III PCMCIA slot. With no moving parts, silent operation and durable enclosure, the Micron CompactFlash Card provides a superior memory solution for any application requiring rugged, compact, low-power (battery-powered) and reliable mass storage.

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest data sheet revision.

SPECIFICATION SUMMARY

PERFORMANCE

(0°C ≤ T_A ≤ +60°C; Vcc = 3.3V ±0.3V or 5V ±10%)

PARAMETER	TYP	UNITS	NOTES
Initial access	1	ms	
Initial WRITE to buffer	400	ns	
Sustained rate (READ)	1	MB/s	1
Sustained rate (WRITE)	400	KB/s	2
Burst rate	6	MB/s	3
Data path	x8 or x16	Bits	
Buffer/burst size	512	Bytes	4
Power-up time	2	ms	

CURRENT DRAIN

(0°C ≤ T_A ≤ +60°C; Vcc = 3.3V ±0.3V or 5V ±10%)

PARAMETER	MAX	UNITS	NOTES
READ current	75	mA	5
WRITE current	100	mA	5
Sleep mode current	<0.5	mA	

NOTE:
1. Parameter depends on software overhead.
2. Faster transfer rates are possible based on parameter selection.
3. Parameter is specified for a READ or WRITE.
4. Buffer/burst size is 1,024 bytes in multiple mode.
5. Typical current draw is selectable based on power and performance requirements.

PECIFICATION SUMMARY (continued)

ELIABILITY

°C ≤ T_A ≤ +60°C; Vcc = 3.3V ±0.3V or 5V ±10%)

PARAMETER	TYP	UNITS	NOTES
WRITE/ERASE cycle endurance	400,000	Per Sector	
MTBF	>500,000	Hours	
Start/stop cycles	NA	–	

NVIRONMENTAL CONDITIONS

PARAMETER	MIN	MAX	UNITS	NOTES
Temperature (operating)	0	+60	°C	
Temperature (nonoperating)	-20	+85	°C	
Shock (operating)	–	1,000	G	1
Shock (nonoperating)	–	1,000	G	1
Vibration (operating)	–	15	G	2
Vibration (nonoperating)	–	15	G	2
Humidity (operating)	8%	95%	–	3
Humidity (nonoperating)	8%	95%	–	3
Humidity (maximum wet bulb)	–	+30	°C	
Altitude (operating)	-200	+80,000	Feet	
Noise	–	0	db	

OTE:

1. Parameter is specified for any axis or direction. A ruggedized version of the CompactFlash Card is expected in the future.
2. Measured peak to peak.
3. Noncondensing.

TECHNICAL NOTES 4

GENERAL TECHNICAL NOTE SELECTION GUIDE

Technical Note	Title	Page
TN-00-01	Moisture Absorption in Plastic Packages	4-1
TN-00-03	Using Gel-Pak Trays with Micron Die	4-3
TN-00-04	The Performance Potential of Die-Based Products	4-5
TN-00-05	Die Yield Issues	4-13
TN-00-06	Bypass Capacitor Selection for High-Speed Designs	4-15
TN-00-07	IBIS Behavioral Models	4-21
TN-00-08	Using Vendor-Supplied Thermal Impedance	4-25
TN-00-09	Accelerate Design Cycles With Micron Simulation Models	4-27
TN-00-10	Micron Meets the Need for Simulation Models	4-33

For the latest technical information on Micron products, read our quarterly technical newsletter *Design Line*.
Call 208-368-3900 to be added to our mailing list or visit our Web site (www.micron.com/mti/msp/html/dlindex.html).

TECHNICAL NOTE

MOISTURE ABSORPTION IN PLASTIC PACKAGES

This article was originally published in 1992.

INTRODUCTION

All plastic integrated-circuit packages have a tendency to absorb moisture. During surface-mount assembly, this moisture can vaporize when subjected to the heat associated with solder reflow operations. Vaporization creates internal stresses that can cause the plastic molding compound to crack. Cracks in the package may cause broken bond wires or allow contamination to penetrate to the die and potentially reduce the reliability of the semiconductor device. The cracking process associated with surface-mountable devices is commonly referred to as the "popcorn effect."

Cracks in the plastic pose several reliability concerns. The moisture path to the die is shortened, allowing ion migration or corrosion to occur more readily. Minor cracks which might not be harmful initially could propagate with time, resulting in a longer-term functional failure.

Since plastic packages absorb moisture, care must be taken to prevent exposure to high humidity conditions for any long period prior to surface-mounting the devices on the printed circuit board. If exposed to excessive moisture, the devices should be baked to remove moisture prior to solder reflow operations.

This technical note describes the shipping procedures that ensure Micron's customers will receive memory devices that do not exhibit the popcorn effect. It also discusses Micron's recommendations for baking the devices if they are exposed to excessive moisture.

ABSORPTION CHARACTERISTICS

Micron's extensive testing empirically characterizes the moisture absorption characteristics of plastic packages. As the plastic takes on moisture, the weight of the device increases. Micron employs a standard procedure for weighing the device before and after it is exposed to moisture. We calculate the percentage of weight gain to determine the relative efficiency of different packaging techniques used for shipping devices.

MICRON PROCEDURES/DEVICE STORAGE

Micron has reduced the chance of having popcorn failures with surface-mount packages by shipping all surface-mount devices in sealed bags containing a desiccant. Devices stored in these bags show no measurable weight gain when subjected to a high-humidity environment for extended periods.

To prevent device failure due to the popcorn effect, store plastic surface-mount packages carefully before PCB assembly. Any concerns about the moisture absorption can be eliminated by storing the devices in Micron's shipping bags. We designed these containers to prevent the passage of water vapor for long periods of time.

MOISTURE SENSITIVITY LEVEL

JEDEC Test Method A112-A provides a means of testing and classifying devices for a certain level of moisture sensitivity. The six moisture sensitivity levels according to this JEDEC standard are described in Table 1, along with the associated floor life and soak requirements. Micron now characterizes its devices to A112-A levels, and the results are available upon request.

DEVICE BAKING

If devices have been removed from their shipping containers and exposed to high levels of moisture, Micron recommends a device bake-out procedure before surface mounting. For tape-and-reeled devices, this bake-out may be accomplished by placing the parts in a tray and baking them in an oven for 160 hours at 40°C. Any moisture is driven out of the devices during the exposure to the heat.

Loose components or components in trays may be baked at a temperature greater than 90°C but less than 100°C for 24 hours. It is important not to exceed the boiling point of water to prevent the popcorn effect during baking.

SUMMARY

1. All plastic packages absorb moisture when exposed to high levels of humidity for long time intervals.
2. Micron ships all surface-mount packages in containers to minimize absorption of moisture.
3. If devices have been removed from their shipping containers and exposed to excessive moisture, they should be baked before being surface-mounted.

REFERENCES

Bhattacharyya, B. K., et al., "Moisture Absorption and Mechanical Performance of Surface Mountable Plastic Packages," in Proceedings of the 38th Electronics Components Conference, 1988.

Kitano, M., et al., "Analysis of Package Cracking During Reflow Soldering Process," in 26th Annual Proceeding, Reliability Physics, 1988.

Lin, R., et al., "Moisture Induced Package Cracking in Plastic Encapsulated Surface Mounted Components During Solder Reflow Process," in 26th Annual Proceeding, Reliability Physics, 1988.

Table 1
MOISTURE SENSITIVITY LEVELS

<table>
<tr><th rowspan="2">LEVEL</th><th colspan="2">FLOOR LIFE</th><th colspan="4">SOAK REQUIREMENTS</th></tr>
<tr><th>CONDITIONS</th><th>TIME</th><th colspan="3">TIME (HOURS)</th><th>CONDITIONS</th></tr>
<tr><td>1</td><td>≤30°C/90% RH</td><td>Unlimited</td><td colspan="3">168</td><td>85°C/85% RH</td></tr>
<tr><td>2</td><td>≤30°C/60% RH</td><td>1 Year</td><td colspan="3">168</td><td>85°C/60% RH</td></tr>
<tr><td colspan="3"></td><td>MET[1]</td><td>FLOOR LIFE[1]</td><td>SOAK TIME[1]</td><td></td></tr>
<tr><td>3</td><td>≤30°C/60% RH</td><td>168 Hours</td><td>24</td><td>168</td><td>192</td><td>30°C/60% RH</td></tr>
<tr><td>4</td><td>≤30°C/60% RH</td><td>72 Hours</td><td>24</td><td>72</td><td>96</td><td>30°C/60% RH</td></tr>
<tr><td>5</td><td>≤30°C/60% RH</td><td>24/48 Hours</td><td>24</td><td>24/48</td><td>48/72</td><td>30°C/60% RH</td></tr>
<tr><td>6</td><td>≤30°C/60% RH</td><td>6 Hours</td><td>0</td><td>6</td><td>0</td><td>30°C/60% RH</td></tr>
</table>

NOTE: 1. Soak Time (total soak time for evaluation) = MET + Floor Life where:
MET = Semiconductor manufacturer's exposure time default value between bake and bag, plus the maximum time allowed out of the bag at the distributor's facility. The actual times *may* be used rather than the default times, but they *must* be used if they exceed the default times.
Floor Life = Package after it is removed from dry pack bag (level 6 after completion of bake).

2. There are two possible floor lives and soak times in level 5. The correct floor life will be determined by the manufacturer and will be noted on the dry pack bag label per JEP113, "Symbol and Labels for Moisture Sensitive Devices."

TECHNICAL NOTE

USING GEL-PAK TRAYS WITH MICRON DIE

INTRODUCTION

To provide a robust packaging environment when shipping die products, Micron uses Gel-Pak trays. This technical note describes the Gel-Pak tray, the advantages it has over other forms of packaging, and how customers can store and use die from this package.

GEL-PAK

Gel-Pak was chosen because of its advantages over other methods of packaging. Although die can be stored in traditional waffle-packs or chip trays, these packages cannot be used for shipping die. In these packages, the die may easily move within the storage cavity during shipment. This movement can be abrasive to the die and can cause chipping or breakage.

Gel-Pak minimizes these problems. Figure 1 shows a side view of a Gel-Pak containing die. Right below the die is a gel membrane that uses surface tension to rigidly hold the die in place. Because the die cannot move, the chances of damage are greatly reduced. In addition, the topside of the die which contains the device circuitry is not in contact with any surface that could damage the die.

Micron uses conductive Gel-Paks. The plastic used in the construction of the tray and cover is electrically conducting and protects the die from harmful static electricity. We still recommend that ESD precautions be taken whenever handling or moving the Gel-Pak tray.

STORAGE REQUIREMENTS

Micron die are packaged for shipping within a cleanroom environment and packaged in a vacuum-sealed bag to minimize exposure to humidity. Upon receipt, the customer should transfer the Gel-Pak tray to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% ±10% relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times during inspection and assembly.

USING GEL-PAKS

Figure 2 shows a Gel-Pak being used when die are being removed during an assembly process. Underneath the gel membrane is a release pattern formed of fabric mesh or molded pattern which defines a series of voids underneath the die. When a vacuum is applied to the tray, the gel membrane is deformed and the amount of surface area in contact with the die is greatly reduced. A holding fixture should be provided for positive positioning of the tray so that a leak-free vacuum can be delivered to the underside of the tray. Empirical tests show that the surface tension force is reduced by over two orders of magnitude, allowing the die to be easily removed.

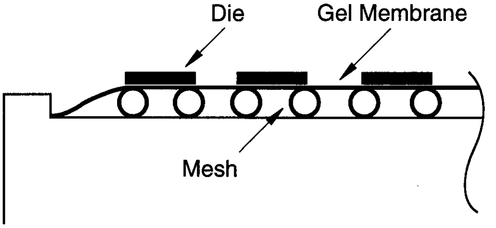


Figure 1
CROSS-SECTIONAL VIEW OF A GEL-PAK

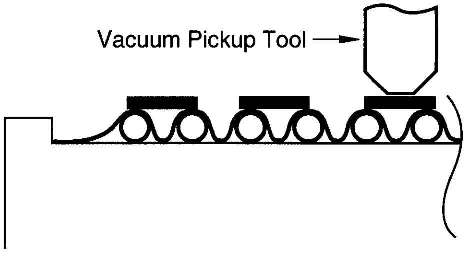


Figure 2
VACUUM APPLIED TO GEL-PAK

Once the vacuum is applied to the container, it is recommended that a vacuum pickup tool be used to remove and place the die. This will minimize the risk of breakage or chipping. Replaceable rubber tips for pickup tools may provide for a more positive device removal from vacuum release trays. The maximum tip size compatible with the device should be used.

With some pick-and-place machines, the vacuum is activated by the contact pressure of the pickup tool on the die. This may result in the die being pushed slightly into the gel, which in turn reduces the ease with which the die can be picked from the gel. Some equipment manufacturers have indicated that their pick-and-place machines can be easily modified to activate the vacuum automatically with very low contact pressure, or the operator may manually activate the vacuum with essentially no contact pressure.

Vacuum Work Stations are available from Gel-Pak and provide an easy way to apply the vacuum to the Gel-Pak. Micron uses 2- and 4-inch Gel-Paks. The 4-inch Vacuum Work Station can be used with both types.

Figure 3 shows a typical orientation of die in a Gel-Pak. All die are placed in the Gel-Pak with identical orientation. Refer to individual die data sheets for the exact orientation for a particular die and part number.

CONCLUSION

By using the methods outlined above, customers will be able to use Micron die shipped in Gel-Paks. Following these guidelines will ensure ease of use and minimum breakage.

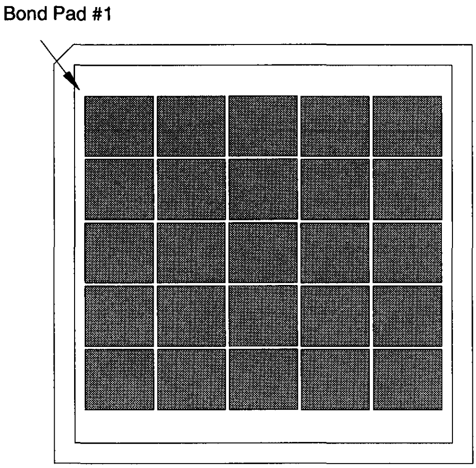


Figure 3
ORIENTATION OF DIE IN GEL-PAK

TECHNICAL NOTE

THE PERFORMANCE POTENTIAL OF DIE-BASED PRODUCTS

This article was originally published in 1995.

INTRODUCTION

High-performance systems are approaching clock speeds where interconnect delays represent a significant fraction of cycle time. Multichip modules (MCMs), flip-chip and stacked technologies are increasingly being used to minimize these delays as well as reduce board area and volume. This technical note describes how and why bare die products can be used in these new packaging technologies, how to simulate the performance of these devices and the various levels of die available from Micron.

WHY USE DIE INSTEAD OF PACKAGED PARTS?

There are multiple reasons to consider using bare die instead of more traditional packages such as BGA, TQFP or SOJ. Bare die are primarily used to maximize performance and minimize board area and volume. Many applications such as desktop computers, workstations, servers, mainframes, networks (ATM) and others are considering the use of these new technologies.

Interconnect delay can represent a large percentage of the cycle time of a circuit. Figure 1 shows interconnect delay as a percentage of cycle time. A constant 2ns chip-to-chip delay was chosen. As systems migrate to 100 MHz bus frequencies (and greater), the interconnect delay can dominate the cycle time. Excessive interconnect delay could mean the addition of costly wait states or reduced bus frequencies with correspondingly lower system performance.

Bare die are most frequently used in nontraditional packages such as flip-chip and MCMs. These packages can reduce signal trace length capacitance and associated inductance on signal lines over traditional packages such as TQFP, SOJ and BGA. This reduction is due both to reduced package capacitance and reduced trace lengths leading to higher performance, especially for busses operating at high frequencies. For example, consider a 100 MHz system that requires 10ns cycle parts. If the access time required is 5ns, extra capacitance can cause significant delays. Just an extra

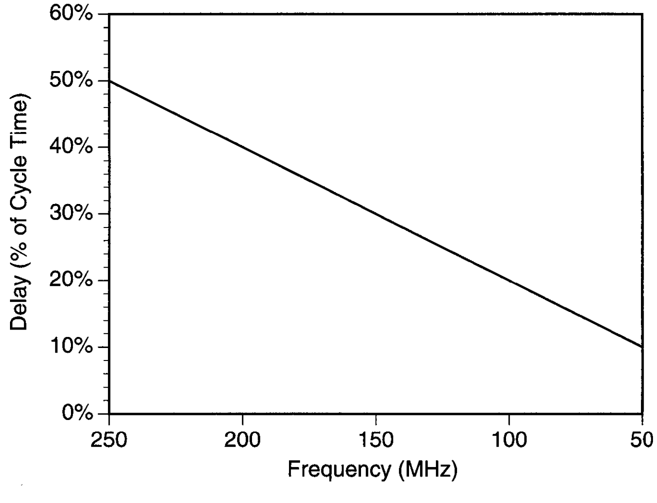


Figure 1
INTERCONNECT DELAY AS A PERCENTAGE OF CYCLE TIME

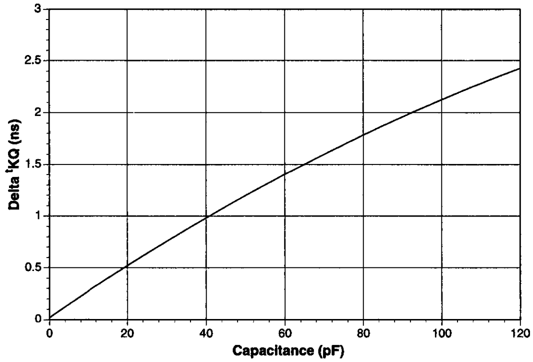


Figure 2
IMPACT OF BUS CAPACITANCE vs. ACCESS TIME

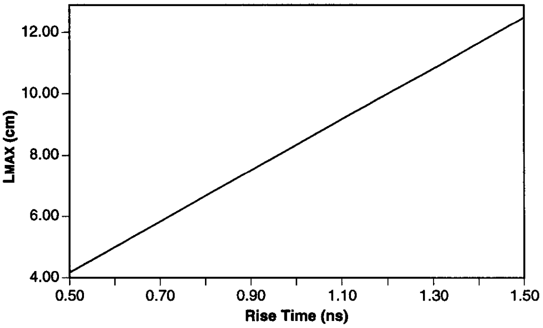


Figure 3
MAXIMUM TRACE LENGTH ALLOWABLE WITHOUT TERMINATION

1ns of delay impacts access time by 20 percent. Figure 2 is a curve showing access time for a synchronous 1Mb 3.3V SRAM (Micron part number MT58LC32K36D8) versus external capacitive load. As you can see, even minor increases in capacitance can cause a significant change in access time at these high frequencies.

An added advantage of shorter trace lengths is a reduced requirement for termination of signal lines. Figure 3 shows the maximum trace length allowable for unterminated lines for a microstrip line on a board using a polyimide dielectric and Equation 1. If line lengths are less than LMAX, the circuit may be treated as an RC time constant. Notice that as rise and fall times approach 1ns and faster, LMAX becomes very small (< 8cm). As rise and fall times decrease, LMAX also decreases, meaning that there will be an increasing need to terminate lines unless the trace length is decreased.

A most compelling argument for using bare die in MCMs can be made for high frequency operation such as in cache memories. Pentium® and PowerPC™ processors already use bus frequencies of 66 MHz and are expected to increase to 75, 100 and beyond. These systems require careful layout and design to attain zero-wait-state performance. For an analysis, see "Processors, Cache SRAMs and Die" at the end of this article.

$$L_{MAX} = \frac{t_r}{2T_d}$$

L_{MAX} = Maximum trace length where circuit can be treated as an RC time constant
t_r = Rise time/fall time
T_d = Signal speed (ns per cm)

Equation 1

There is always the need to decrease the size of memory packages, especially for applications such as portable computers and hand-held equipment. Bare die can be used in packaging technologies such as chip-on-board and MCMs to reduce the board area required. Die stacking can be used to reduce both board area and total volume required for a memory implementation.

Packaged parts such as TQFP or BGA take up fixed board areas regardless of die size. For example, consider a 32K x 36 synchronous SRAM in a 100-pin TQFP package. As the die size is reduced from generation to generation, no reduction in board area is possible because the same package dimensions are used. Table 1 shows the area of the die and package, and the ratio of the two. Packaging techniques such as flip-chip can take advantage of die shrink area reductions. Micron notifies die customers well in advance of impending die shrinks.

HOW ARE DIE TIMING AND PERFORMANCE TESTED AND DETERMINED?

Customers purchase bare die for use in MCMs or stacked packages where multiple die are required for each package. Although the yield for individual die is usually very high, the overall yield decreases as the die count increases. Figure 4 shows how the module yield varies versus die yield and die count. This yield does not include packaging yield loss.

Earlier MCM technologies have had to consider rework and replacement because fully tested and burned-in die were unavailable. After the MCM was burned in and

Table 1
1Mb SYNCBURST™ DIE/PACKAGE BOARD AREA COMPARISON

1Mb SYNCBURST SRAM GENERATION	TQFP AREA (cm^2)	DIE AREA (cm^2)	TQFP/DIE AREA RATIO
Generation 1	3.59	0.90	3.98
Generation 2	3.59	0.53	6.77
Generation 3	3.59	0.32	11.21

ested, infant mortalities would occur, making rework necssary. This additional step was the main contributor to the igh cost of the module. Few applications, other than nilitary or satellites, can justify the high cost of these nodules. For most users, rework must be eliminated to educe costs. This can only happen if the reliability of each lie is increased or redundancy is used (which also increases osts).

To alleviate the problems associated with using bare die r wafers, Micron offers four different levels of testing. hese levels are described in detail below and customers nay choose the version best suited to their needs based pon price and performance.

STANDARD PROBE (C1)

Standard probe, or C1 level, is the first version of die product offered by Micron. A wafer probe test is performed on the die with guardband added to ensure the die will perform over the commercial temperature range (0°C to 70°C). This is the same probe test used for packaged die and consists of various functional and parametric tests of each die. Test patterns, timing, voltage margins, limits and test sequences are determined for each product individually based upon product yields and reliability data.

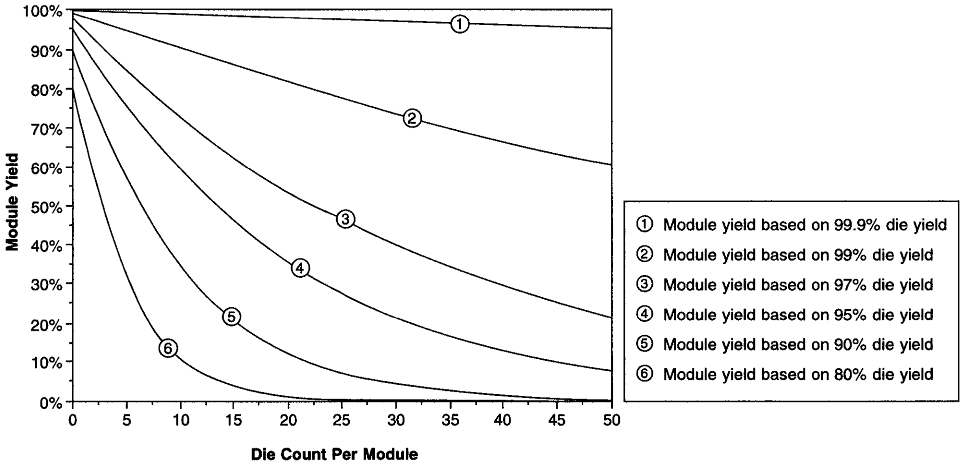


Figure 4
MODULE YIELD vs. DIE COUNT AND DIE YIELD

C1-level products may be optimal for customers having different types of die in a module where some of these die require burn-in after assembly of the package. As an example, consider a module which has both Micron die and other vendors' die. If the Micron die were burned in and the others were not, a module burn-in cycle would be necessary. This means that Micron devices that are already past the infant mortality stage would receive an additional high temperature cycle that would stress the part and potentially reduce the operating lifetime of the part. It would be better to use nonburned-in die in this application and burn in the whole module at the same time.

This C1 level may also be of interest to users who buy wafers and will do additional processing steps. Burn-in of the die should be done after all post-processing steps such as bumping or metallization are completed.

SPEED PROBE (C2)

Speed probe, or C2 level, begins with the same wafer probe test used in C1-level die. The difference is that the testing of the die is done with a hot chuck speed probe to assure the speed performance of the die for the fastest speed grades. Critical parameters such as access times and pulse widths are temperature dependent and this probe gives both functionality and a speed map of the wafer at temperature. A die map is provided with each wafer showing each die position and the speed probed for that die. For die, customers can choose a specific speed grade or speed-graded die (multiple speed grades). The C2 level will be of interest to customers that require faster speed grades.

PROBE$^{\text{Plus}™}$ (C3)

PROBEPlus, or C3-level, die incorporate all the testing done in the C1 and C2 levels with the inclusion of a dynamic burn-in step. The purpose of the burn-in step is to operate the parts until they have passed the infant mortality failure stage.

One of the main benefits of the die manufacturer performing burn-in is to ensure that the optimal burn-in time is not exceeded. If burn-in is done at the MCM level and several different die types are used, some die may be burned-in past their infant mortality phase and into the useful lifetime of the part. Micron uses a dynamic burn-in cycle which allows us to optimize the process so that infant mortalities are eliminated, but not so much that the device is overstressed.

Micron PROBEPlus die can be used in boards with other components that are not burned-in. These PROBEPlus die can undergo another burn-in phase. Although this subjects the part to the stress of an additional burn-in, the useful operating life is so long that the effect is usually minimal. Although the nonburned-in parts may still have infant mortalities, the yield loss at the module level will be minimized by using Micron burned-in die. Overall, the module yield will be higher by choosing Micron PROBEPlus (burned-in) die versus nonburned-in die.

PROBEPlus may be the most attractive level to users since it allows infant mortalities to be isolated and removed before the die are used. Users wanting to skip an MCM burn-in phase will want this level. Packaging technologies that do not allow rework will also require parts that are burned in.

KNOWN GOOD DIE (C7)

The highest level of testing that Micron offers is known good die or KGDPlus®. The KGDPlus process provides the customer with fully warranted die with equal quality and reliability to packaged parts. Micron's KGDPlus process allows Micron to fully test and burn-in die product after it is initially tested to the C1 level. This level of testing checks all timing and current parameters and ensures that they meet the specification.

This guarantee of timing and power does not mean that the die will meet all the timing on the data sheet for every possible packaging technology. It means that the die will meet the data sheet parameters for the packages that we offer it in. For example, a KGD die version of Micron's MT58LC32K36B3S27B SyncBurst SRAM will be guaranteed to meet the data sheet parameters if packaged in a TQFP package with identical leadframe and bondwire capacitance, inductance and resistance.

WAFER vs. DIE

Micron does offer products in either die-level or wafer-level form. Some users prefer wafer-level products since their manufacturing process may require additional processing which adds metal layers or bump pads for flip-chip. Die-level products are available at all levels, but wafer-level is only available in the C1 and C2 levels because the C3 and C7 manufacturing processes are designed for individual die only.

THE THERMAL MODEL

Die users need to be concerned with power dissipation and how to model it since the thermal impedances of their package will vary. In general, systems are concerned with power dissipation due to using high-powered parts, limited airflow or large numbers of components. Data sheets for packaged memories typically specify an absolute maximum rating for power dissipation over a temperature range. For instance, most 5V SRAMs are rated at one watt over a temperature range of 0°C to +70°C.

More recently, SRAMs use a maximum junction temperature instead of power dissipation. For instance, Micron's

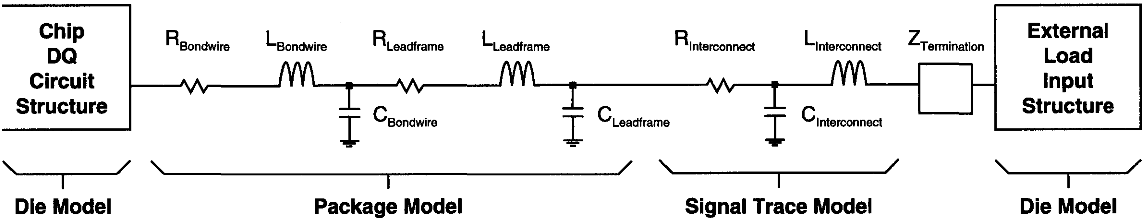


Figure 5
THE INTERCONNECT MODEL

SyncBurst SRAM family specifies an absolute maximum unction temperature of +150°C and provides thermal resisances for the package (θ_{JA} and θ_{JC}). The user can then calculate the power dissipation of the part and the associated junction temperature. This method is described in Micron Technical Note TN-05-14, "SRAM Thermal Design Considerations."

Die users must treat the package differently than either of he methods above. Users must still ensure that the maxinum allowable junction temperature is not exceeded, and hey must determine their own thermal impedance numbers (unlike with packaged parts). This can be done by using one of a variety of software tools.

THE PACKAGE MODEL

Packaged parts are guaranteed to meet data sheet timing and power dissipation specifications. It is difficult, if not mpossible, to generate a die specification that will meet iming and power dissipation for all the various packaging echnologies (flip-chip, stacking, MCM, etc.). Because of his, it is essential that users modeling their package are able o simulate the performance of their product.

As an example of a package model, let's use the SOJ package. Figure 5 shows a model for simulating a single DQ signal in the system. The chip DQ circuit structure is die-specific and will require a SPICE model or IBIS model. These models are discussed in the next section.

The package model varies widely for different package ypes and even among different pins in a single package. A 32-pin SOJ leadframe is shown in Figure 6. The pins near the ends of the chip have more capacitance and inductance as compared to those in the center due to the length of the eadframe. Inductance may vary from 5nH for the shortest eads to 10nH for the longest. Typically, most high-frequency parts have the highest speed I/O near the center of the package to minimize the lead length and associated parasitics.

Different types of I/O on a package may require different simulations. For example, inputs must be treated differently than outputs. Clock lines may be among the most highly loaded lines and require exact simulation due to heavy capacitive loading. VDD and GND lines should also be treated with special deference.

Component manufacturers typically characterize the capacitance of their parts in package form. This means that the capacitance of the leadframe and possibly the bondwire (in flip-chip) must be subtracted from the total pin capacitance before using it in a model. Capacitance due to the plastic package is typically less than 1pF.

SIMULATION MODELS

One of the main reasons to use MCMs or hybrid packaging is to improve performance. As mentioned previously, this is possible because line length and parasitics are reduced. However, high-speed lines may have to be simulated to quantify delay times and assure that system timing can be met. This is done using simulation models such as SPICE.

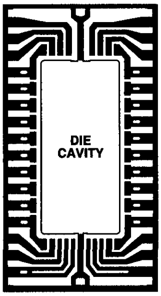


Figure 6
A PACKAGE LEADFRAME

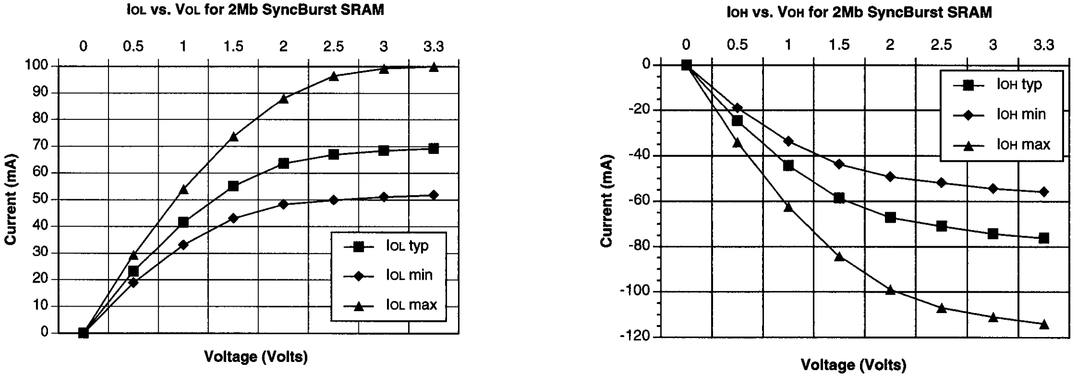
Figure 5 shows how to model the interconnect of a signal line. The user must construct a SPICE model for the interconnect and acquire a model for the SRAM I/O and all other I/Os on the same signal trace. This can be difficult because many vendors release SPICE models only under a nondisclosure agreement and consider the models proprietary.

Because of the difficulties in generating SPICE models, an alternative model called IBIS (I/O Buffer Information Specification) has been developed. The idea behind this model is that it can be developed using nonproprietary information about the design or process technology. It is generated using V/I curves, timing characteristics and package information. An example of information required for an IBIS file is shown in Figure 7. A text file is generated from this information for the simulator.

For more information on simulation models see Technical Note TN-00-09, "Accelerate Design Cycles with Micron Simulation Models" or visit Micron's Web site at www.micron.com/mti/msp/models/index.html.

PURCHASING DIE PRODUCTS

Micron distributes die products through Chip Supply, Inc. For more information on Micron die products, visit their Web site at www.chipsupply.com.


IOL vs. VOL for 2Mb SyncBurst SRAM

IOH vs. VOH for 2Mb SyncBurst SRAM

VOL	IOL TYP	IOL MIN	IOL MAX
0.00	0.00	0.00	0.00
0.50	23.10	18.80	29.30
1.00	41.50	33.10	54.00
1.50	55.10	43.00	73.70
2.00	63.60	48.30	88.10
2.50	66.90	49.90	96.50
3.00	68.40	51.10	99.30
3.30	69.20	51.80	100.00

VOH	IOH TYP	IOH MIN	IOH MAX
0.0	0.00	0.00	0.00
0.5	-24.70	-19.00	-34.10
1.0	-44.40	-33.70	-62.50
1.5	-58.70	-43.80	-84.30
2.0	-67.20	-49.30	-99.00
2.5	-71.00	-51.90	-107.00
3.0	-74.30	-54.40	-111.00
3.3	-76.20	-55.80	-114.00

BEYOND THE RAIL INFO			
DIODE TO GND		DIODE TO VDD	
V	I (mA)	V	I (mA)
-1.3	-1.42E-02	n/a	n/a
-1.2	-1.11E-02	n/a	n/a
-1.1	-8.22E-03	n/a	n/a
-1	-5.71E-03	n/a	n/a
-0.9	-3.58E-03	n/a	n/a
-0.8	-1.91E-03	n/a	n/a
-0.7	-7.61E-04	n/a	n/a
-0.6	-1.90E-04	n/a	n/a
-0.5	-1.71E-05	n/a	n/a
-0.4	-4.67E-07	n/a	n/a
-0.3	-1.22E-08	n/a	n/a
-0.2	0	n/a	n/a
6.6	0	n/a	n/a

PACKAGING CHARACTERISTICS			
	MIN	MAX	UNIT
R_Pkg	50.0	70.0	mOhm
L_Pkg	5.0	7.0	nH
C_Pkg	0.2	1.0	pF
C_Cmp	3.0	7.0	pF

Figure 7
AN IBIS MODEL FOR A 2Mb 3.3V PIPELINED SYNCBURST SRAM

CONCLUSION

This article has stressed the reasons why die applications are becoming more widespread and the different ways that Micron can support these die users. Micron offers four different levels of die support ranging from C1 (standard probe) to C7 (known good die). Users will choose a level based upon a price-performance trade-off. Support is also available in helping users model their various applications by providing information such as IBIS models.

APPLICATION EXAMPLE: PROCESSORS, CACHE SRAMs AND DIE

One of the optimal applications for die is with SRAM cache memory and microprocessors. Processors such as PowerPC and Pentium already operate at frequencies 66 MHz and higher. In the near future, bus frequencies may ncrease to over 100 MHz. These types of applications are optimal for MCMs because they minimize loading, capacitance and trace length, which is critical at these high frequencies.

Consider a 100 MHz system using two Micron SyncBurst SRAMs as secondary cache. Let's compare an implementation using a TQFP package versus an MCM. Assume that the processor uses a 72-bit wide bus and requires two pipelined 64K x 36 SRAMs for a 64K x 72 implementation. At 100 MHz, assume that the SRAMs are capable of a 5ns access time (^{t}KQ or clock to output valid). Figure 8 shows the system which consists of the processor, cache controller and SRAMs.

Table 2 shows some of the differences between the two implementations. The reduction in capacitance is due both to the reduction in the trace length and the elimination of the package leadframe. The reduction in the board area of the SRAMs alone would be 85 percent.

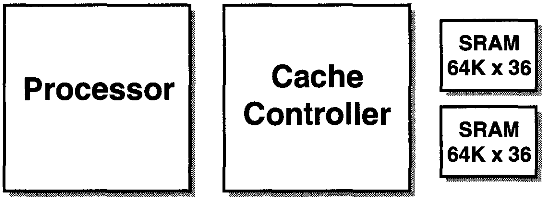


Figure 8
PROCESSOR, CACHE CONTROLLER AND CACHE SRAMs

A result of the decreased trace length and capacitive loading is a ^{t}KQ reduction of 0.35ns. Although this may seem like a small amount, it is a reduction of almost 10 percent in the access time. This amount is very significant in high-performance systems. A performance difference of a few percentage points in high-end systems such as servers or mainframes can be critical in maintaining a competitive edge.

Optimization of the cache interface will become more important as the difference in processor clock frequency and cache bus frequency increases. For example, consider a system using a 100 MHz clock in the processor and a 50 MHz clock frequency on the bus. Every time the processor has to go off-chip for data from the cache, it takes two 50 MHz clock cycles to get the first piece of data (zero-wait-state operation). However, this equates to four processor cycles in which the processor is just waiting for data. An extreme case of this is the Digital Alpha 21164 microprocessor which can run up to 500 MHz. If the same cache memory were used, the processor would be waiting 20 clock cycles for data.

Table 2
DIFFERENCES BETWEEN PACKAGED PARTS (TQFP) AND THE USE OF DIE (MCM)

PARAMETER	TQFP	MCM
Maximum Trace Length (cm)	12.5	5
External Capacitive Load (pF)	30	22
Board Area (of SRAMs) (cm^2)	3.5	0.5
Clock to Output Valid Reduction (Δ^{t}KQ) (ns)	n/a	0.35

TECHNICAL NOTE

DIE YIELD ISSUES

NTRODUCTION

Uses of bare die vary widely and include flip-chip, ultichip modules (MCMs), hybrid modules and 3D or acked technologies. Different applications may see vary- g yields at packaging, burn-in and test. This article dis- usses some of the yield issues that users may confront hen using die products.

UALITY LEVELS OF DIE

Micron offers a choice of four quality levels of die. Each ersion has different yields in the customer's test and burn- flow, and the die user should choose the appropriate vel based upon a price-performance-yield trade-off. A rief description of each level is given below:

tandard Probe or C1: This is the lowest-cost die product vailable from Micron. Wafers are probed to check func- onality and limited parametric tests.

peed Probe or C2: This version uses more extensive wafer robe tests. The parts are also speed graded to guarantee Q for SRAMs and ^{t}RAC, ^{t}CAC and ^{t}AA for DRAMs.

ROBE^{Plus}™ or C3: This level incorporates all the testing one with C1 and C2, as well as an intelligent burn-in of the ie using Micron's AMBYX® test system.

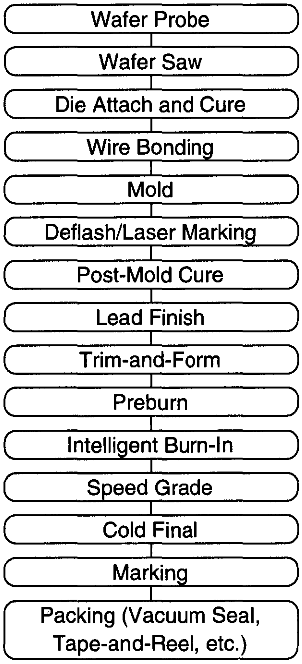
GD^{Plus}® (Known Good Die) or C7: This version ensures uality and reliability equal to standard packaged product. omplete AC and DC testing of the die is done, as well as urn-in, so that the device is warranted to meet data sheet pecifications.

IE vs. PACKAGE

Users of packaged parts, such as TQFP or BGA, have very igh manufacturing yields. Since these parts have been ubjected to a series of tests and burn-in to eliminate infant ortalities and failures, the user sees an extremely low FIT ate (typically < 20 FITs). Usually, the only manufacturing tep is an infrared reflow step, which mates the part to the oard. The manufacturer of packaged parts will see yield oss at various steps in the manufacturing process. This loss s never seen by the user, who receives the highest quality arts. Die users, however, are taking on some of the test and creening steps previously performed by the die manufacturer. Consequently, users will now encounter yield issues that were previously hidden when they purchased packaged parts.

The Fabrication Flowchart for a 1Mb SRAM (TQFP package) shows some of the steps that occur after the fabrication of a die, including packaging and test. Yield loss can occur at any of these steps. Die users must realize that yield loss will occur and will vary from lot to lot. The rest of this note discusses some yield issues that may occur with bare die.

FABRICATION FLOWCHART FOR A 1Mb SYNCHRONOUS SRAM



PROCESSING WAFERS

Some users purchase die in wafer form so further processing steps can be performed. These additional steps include adding metal layers, passivation or bumping pads for flip chip, among others. These extra steps can add new failure modes, causing higher yield loss in packaging, test or burn-in. The addition of extra processing may void any applicable die warranty.

Street widths (or spacing between adjacent die) are typically 5 to 6 mils but will migrate to 4 mils over time. Users sawing wafers should plan for 4-mil street widths for compatibility with current and future spacing. Care must be taken when aligning the wafer to ensure that active die area is not sawed because saw widths may be up to 3 mils wide.

BURN-IN

Users that purchase C1- or C2-level die will probably want to perform a burn-in step after assembly. This step is necessary to ensure that infant mortalities (inherent manufacturing defects caused by contamination and/or process variability) are eliminated before the product is shipped to the end customer.

Because of the variability in infant mortalities, yield during burn-in will vary from lot to lot and wafer to wafer. A dynamic burn-in that cycles the inputs and control signals under bias is recommended. For details on the way Micron performs burn-in using our AMBYX intelligent burn-in and test system, refer to Micron's *Quality and Reliability Handbook.*

C3- and C7-level die will not require burn-in because they have already received Micron's AMBYX-based burn-in and infant mortalities have been removed. Users that have die from multiple vendors may have some die in their system which are not burned-in. Subjecting Micron die to a double burn-in is permitted and should have a minimal effect on the useful lifetime of the product.

TEST

A post-packaging test will usually be performed to check for timing and functionality to ensure that no defects have occurred during packaging. Test yield can vary due to a number of factors, including the level of die purchasec packaging, assembly, packaging technology used, test prc gram or tester.

C2-, C3- and C7-level die come with a guarantee of one c more timing parameters. These parameters are only guai anteed if customers use the same packaging and leadfram that Micron uses in production parts. For instance, if a use purchased a 32K x 36 SRAM die and packaged it in a TQF package or another package with similar capacitance, ir ductance, resistance and trace length, then the timing spec fications will be guaranteed. Any packaging method thε increases capacitance, inductance, or resistance on an signal or power line may require a derating factor to param eters such as access time, cycle time, setups and hold: Micron Applications Engineers are available to determin an appropriate derating factor.

VISUAL INSPECTION

Some users perform a visual inspection of die usin MIL-STD-883D. This requires a high-power visual inspec tion of die (75X to 150X) for Class B components. Becaus memories make use of redundant elements, a visual inspec tion may detect a defect which has been bypassed by redundant row or column. This can cause users to rejec good die. Micron inspects die to a 10X magnification an will not accept returns of die with physical defects detecte at higher magnifications.

PURCHASING DIE PRODUCTS

Micron distributes die products through Chip Suppl Inc. For more information on Micron die products, visi their Web site at www.chipsupply.com.

CONCLUSION

This technical note discussed some of the major issue affecting die yield for users of bare die. Die users mus now contend with issues that were previously faced onl by the semiconductor manufacturers, and they need to b aware that die yield will vary because of these issues Contact Micron Applications Engineering at 208-368-395 to resolve die-related issues.

TECHNICAL NOTE

BYPASS CAPACITOR SELECTION FOR HIGH-SPEED DESIGNS

This article was originally published in 1996.

INTRODUCTION

In order to guarantee better performance from high-speed digital integrated circuits (ICs), manufacturers are ightening power supply noise margins. With lower power supply noise margins, the designer needs to pay closer attention to local bypass capacitor selection.

As bus speeds increase and switching times decrease, proper selection of local bypass capacitors for high-speed digital ICs is becoming increasingly complex. With wider parts becoming prevalent in cache subsystems, the amount of current required from the bypass capacitor to decouple noise from the current transients switching across the power bus is increasing. At the same time that the current transients become larger, the need to choose smaller capacitance values is becoming more important. Smaller capacitance values offer lower series inductance.

The role of the bypass capacitor is to decouple the power supply bus from the IC. Figure 1 shows the equivalent circuit of a decoupling loop. The objective is to eliminate the effects of the power bus inductance and resistance (R1, Rg2, L2, Lg2 in Figure 1) so that transient currents flowing across the power bus do not cause excessive noise at the power and ground pins of the IC. Therefore, the bypass capacitor should have low effective series resistance (ESR) and series inductance while having a large enough capacitance value to supply current to the IC during switching.

Several factors need to be considered when selecting local bypass capacitors. These factors include selecting the proper capacitor value, dielectric material, geometry and the location of the capacitor in relation to the IC. Careful observance of fundamental principles will determine how well the capacitor can suppress switching noise.

Selecting the correct bypass capacitor in a high-speed design has economic and design reliability consequences. You may be tempted to place any large value capacitor across the power pins for bypass. But choosing a value that exceeds the necessary value can result in higher series inductance, increased expense and inferior electrical or nominal value stability characteristics.

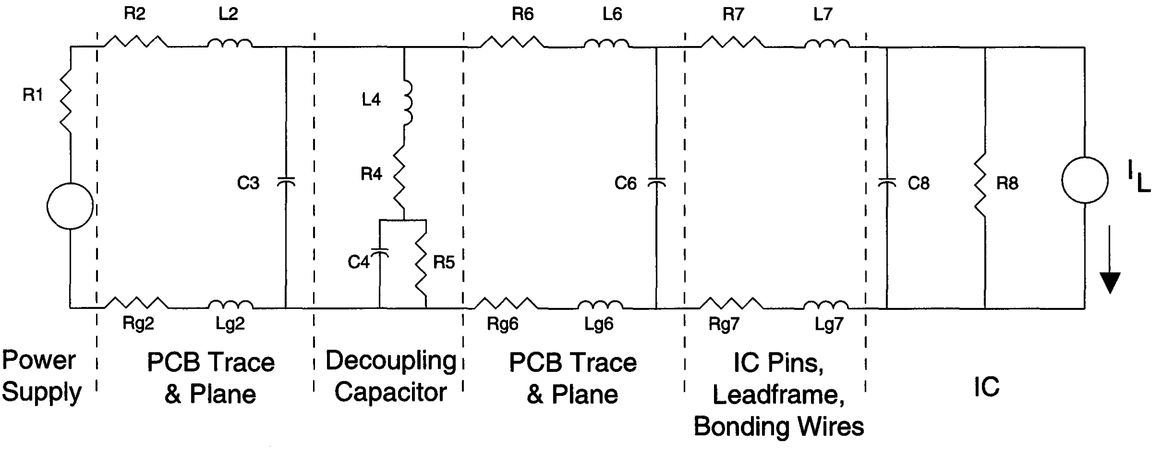


Figure 1
BYPASS DECOUPLING LOOP

SELECTING A CAPACITOR VALUE

There are two methods for selecting a bypass capacitor. One method uses a simple calculation that relies upon the load being driven by the outputs from the IC. The second method uses the maximum allowed reactance of the bypass circuit to determine the number and size of the bypass elements. Using the first method, you can get an approximation of the ideal value without having to determine the impedance characteristics of other components in the system. The second method considers the impedance routing back to the power supply.

The importance of adequate bypass is especially apparent if you consider the speed and width of newer cache designs. If you are designing with Micron's SyncBurst™ SRAMs, you can have as many as 36 outputs firing simultaneously for each IC. If each output is driving a large load, the current surge can be very high.

For example, if you are driving a 30pF load from 0V to 3V with 2ns edges, the transient current will be:

$$I = C\frac{dV}{dt}$$

$$I = \frac{30pF(3V)}{2ns}$$

$$I = 45mA$$

Therefore, the current demanded by the SRAM switching all 36 outputs is 36 x 45mA = 1.62A in 2ns.

The SyncBurst SRAM has a V_{DD} tolerance of 3.3V +0.3V/ -0.165V. If you consider some droop from the power bus and a switching time of 2ns, and allow a maximum voltage dip (ΔV) on the SRAM of -0.05V, the choice of bypass capacitor becomes:

$$C = \frac{I\,dt}{dV}$$

$$C = 64nF$$

Choosing a value of 70nF will allow for variations due to temperature and aging. Better yet, choose two 34nF and place them in parallel to help reduce ESR. If you were to select a large capacitor, such as a 0.47µF, you could be adding unnecessary inductance that can cause glitching on the supply lines and violate the IC power supply noise specification.

For example, using the relationship V = L × di/dt, if a series inductance as small as 1.5nH is present, then under the conditions described above glitching could be as high as 1.4V. When considering the entire bypass loop, however, actual glitching will probably be much less because of parallel inductances and capacitances.

In looking at simulation and empirical data, glitching on the bypass capacitor can be quite significant depending on the number of outputs switching and the impedance of the PCB and power bus. Simulation results for Micron's 32K x 36 SyncBurst SRAM have shown that under worst-case conditions (all outputs driving LOW to HIGH, 66 MHz bus), as little as 1nH bypass series inductance can cause noise on the supply that violates the low side of 3.3V +0.3V/ -0.165V supply specification. Changing the size of bypass capacitance has little effect on changing the peaking of this noise since the series inductance of the bypass capacitor dominates the effective impedance across the capacitor under high current with very fast switching times.

Considering the effects of series inductance, the method for calculating a bypass capacitor based on charge sharing presented in the previous example may not provide the needed low impedance path necessary to bypass a high-speed, wide I/O device such as the SyncBurst SRAM. You may need to use a method of calculation based on the reactance of the bypass capacitor in relation to the reactance of the bypass loop.

Reference 1 offers a method for calculation based on the allowed reactance of the local bypass capacitor. The result of this calculation is a capacitor array that is intended to be distributed around the PCB. It is very important to note that this design method assumes solid power and ground planes.

In this example, it is assumed that you are using solid power and ground planes and you are bypassing the entire board. The choice for board level bypass capacitors is made much the same way as the following example illustrates for choosing a local bypass capacitor. When determining the board-level bypass, you must determine the power bus inductance and bypass the board from the supply noise that can occur from large current spikes switching across the power bus inductance.

The following example assumes you have already selected a board level bypass. Suppose you wanted to determine the local bypass capacitor for a SyncBurst SRAM. You need to determine the maximum reactance the circuit can tolerate and stay within the 3.3V +0.3V/-0.165V supply margin. If you are allowing a total change in voltage across the supply pins of 0.05V and the current is changing by around 1.62A, then the maximum reactance at the supply pins becomes:

$$X_{MAX} = \frac{DV}{DI}$$

$$X_{MAX} = 31m\Omega$$

The highest frequency for which the board-level bypass capacitor is effective for bypassing supply noise is determined by its series inductance. The board-level bypass is used to bypass supply noises at frequencies higher than the frequencies not bypassed by the power supply (F_{BYPASS}). Yet he board-level bypass is usually too large to bypass frequencies higher than F_{BYPASS}. If you use an electrolytic for board-level bypass, a typical series inductance is 5nH.

$$F_{BYPASS} = \frac{X_{MAX}}{2pL_{SERIES}} = 982\text{ kHz}$$

There is another frequency (Ref. 1) called the knee frequency. It can be shown that most energy in digital pulses concentrates below the knee frequency and that the behavior of a circuit at the knee frequency determines its processing of a step edge. Therefore, behavior of the circuit at frequencies above the knee frequency hardly affects digital performance. The knee frequency for any digital signal is related to the rise and fall time of its digital edges, but not its clock rate. The knee frequency is given as:

$$F_{KNEE} = \frac{0.5}{T_r} = 250\text{ MHz for } T_r = 2\text{ns}$$

Next, calculate how much inductance you can tolerate in the circuit.

$$L_{TOT} = \frac{X_{MAX}}{2pF_{KNEE}} = \frac{X_{MAX} \times T_r}{p}$$

$$L_{TOT} = 19.7\text{pH}$$

The data sheet for a common surface mount chip capacitor shows a series inductance of around 1.5nH. Use this number to find the number of capacitors needed in the array to sufficiently reduce inductance.

$$N = \frac{L_{SERIES}}{L_{TOT}}$$

For this example, N = 76.

The total array bypass must have an impedance less than X_{MAX} down to the frequency F_{BYPASS}. This is true since the board-level bypass capacitor bypasses frequencies below F_{BYPASS}. The array bypass values are determined as follows:

$$C_{ARRAY} = \frac{1}{2pF_{BYPASS}X_{MAX}}$$

$$C_{ARRAY} = 5.23\mu\text{F}$$

$$C_{ELEMENT} = \frac{C_{ARRAY}}{N}$$

$$C_{ELEMENT} = 69\text{nF}$$

From this calculation, in order to minimize the effects of series inductance in the bypass capacitors, you must distribute 76 64nF capacitors around the board. This bypass will only take care of one SyncBurst SRAM switching into 30pf loads used in this example. Any other high-speed circuits that could be switching at the same time as the SRAM would require additional bypass.

From this analysis, it may seem that 76 capacitors distributed around a PCB is a bit unreasonable. There are alternatives to the standard EIA-sized capacitors available that can significantly reduce series inductance and help eliminate the need to add such a large number of parallel capacitors. Some of these alternatives are mentioned below.

DIELECTRIC AND GEOMETRY

Just as important as selecting the correct capacitance value is selecting the correct dielectric material and device geometry. Some materials have better dielectric properties but sacrifice temperature and aging characteristics. Multilayer ceramic (MLC) capacitors are available in a variety of sizes and dielectric materials.

The capacitance value you select can not only determine the size of the component but also the dielectric material. Depending upon your design goal, selection of the dielectric is not a trivial matter.

For example, suppose you decide to just place 0.47µF bypass capacitors throughout your design. Not only are you adding unnecessary series impedance, but you may end up selecting a capacitor that uses Z5U formulation instead of X7R for a dielectric. The Z5U formulation provides a high dielectric constant compared to X7R and other common ceramic formulations. Yet Z5U has inferior temperature and aging stability compared to X7R. Figure 2 shows examples of typical temperature characteristic curves taken from manufacturers' data sheets. These curves show a comparison between the temperature dependence of capacitance for Z5U and X7R. If you calculated a 64nF capacitor, you could choose an X7R dielectric and get better capacitance stability over temperature while at the same time reducing overall series inductance.

Remember that selecting a large capacitance value in a high-speed design can result in high inductance and defeat the purpose of the bypass capacitor. Reducing series inductance is the primary concern for high-speed design. There are other methods applied by capacitor manufacturers that can, in conjunction with careful component selection, reduce overall series inductance.

The length-width aspect ratio of the capacitor has an effect on inductance. The EIA standard sizes for MLC capacitors are specified by a four digit number. For example, a 0805 is a chip capacitor with a length of .08 inches and a width of .05 inches. This size ratio results in an inductance of about 2nH. At extremely high frequencies, this much capacitance can cause severe glitching. Reversing this size ratio can result in much lower inductance. AVX Corporation (Myrtle Beach, SC) has developed reverse

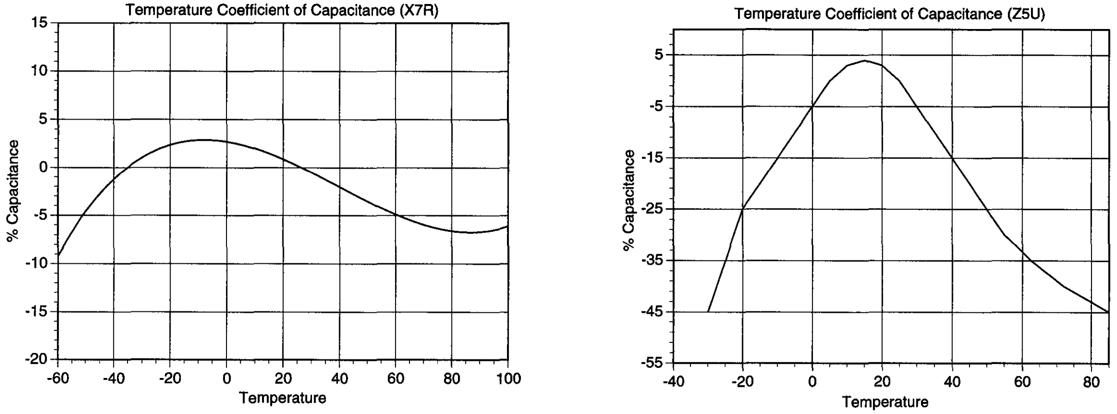


Figure 2
TEMPERATURE DEPENDENCE OF CAPACITANCE

aspect ratio capacitors. Reversing the aspect ratio so that the width is greater than the length has the effect of lowering the series inductance. AVX has also developed a line of capacitors known as Low Inductance Capacitor Arrays (LICA). The LICA product family allows you to connect to more than one of the same value capacitor within the same package. Each capacitor is designed to reduce inductance through internal design structures (perpendicular current paths) and interconnect methods (C4 "flip-chip" technology).

In addition to reducing series inductance, it is often advantageous to reduce effective series resistance (ESR). The dissipation factor given in manufacturer data sheets indicates the relative ESR for a component. However, low ESR can cause unexpected problems in designs where long power bus leads are present, such as a design where several high-speed ICs are connected to the power bus in parallel.

Figure 3 shows an example of a long LC resonator with the power bus acting as a low-loss inductor between each bypass capacitor (Ref. 2). If repetitive pulses are applied to the power bus in this circuit, ringing can build in amplitude, resulting in a very noisy power bus. To solve this problem, electrolytic capacitors, which have inherently high ESR, can be placed across the bus to help dampen the ringing.

PLACEMENT OF CAPACITOR

The placement of the capacitor in relation to the IC can have as much to do with determining its effectiveness as selecting the correct value. The rule of thumb is to place the capacitor as close as possible to the IC. This will minimize inductance caused by long lead lengths (in designs without solid power and ground planes) and minimize transit delays from the capacitor to the IC. Capacitors that fit under the IC can result in the shortest lead lengths.

However, some packages, such as Micron's 100-pin TQFP, cannot accommodate capacitors mounted under the package. To help solve this problem, you can mount capacitors across the power bus very near the memory devices. Figure 4 suggests a configuration that will reduce bus inductance for two 100-pin TQFP devices.

Figure 4 shows parallel combinations of capacitors to help minimize the inductance of each element. The figure illustrates one possible configuration. Of course, all designs must be evaluated individually. This configuration will help bypass all of the several power and grounds found on this package as long as the bypass capacitors are very near the ICs and there are solid power and ground planes.

CONCLUSION

The solution for providing power supply decoupling for high-speed circuits, such as Micron's SyncBurst SRAM, relies upon the characteristics of the bypass elements. Items to keep in mind when selecting a bypass solution are as follows:

1. The inductance of the bypass capacitor is more a determining factor for the effectiveness of the bypass than the capacitance value. Therefore, select bypass capacitors based on series inductance values.

Distribute bypass elements throughout the PCB, yet concentrate bypass elements close to the ICs demanding large current transients—even if you have solid power and ground planes. Keep the bypass capacitors as close as possible to the ICs.

Use the impedance method presented above to determine the total inductance your design can tolerate and carefully select low inductance capacitors to bypass ICs demanding high current transients.

REFERENCES

Johnson, Howard, and Martin, Graham, "High-Speed Digital Design: A Hand Book of Black Magic," Englewood Cliffs, NJ: Prentice Hall, ISBN 0-13-395724-1.

Pease, Robert, "Troubleshooting Analog Circuits," Stoneham, MA: Butterworth-Heinemann, ISBN 0-7506-9184-0.

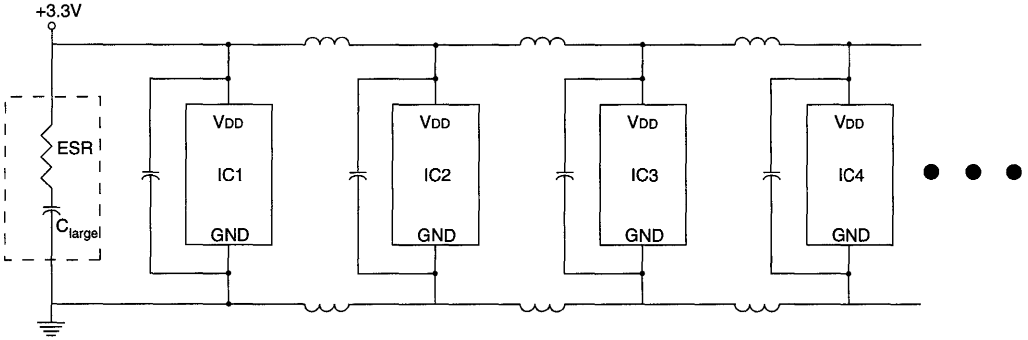


Figure 3
POWER BUS LC RESONATOR

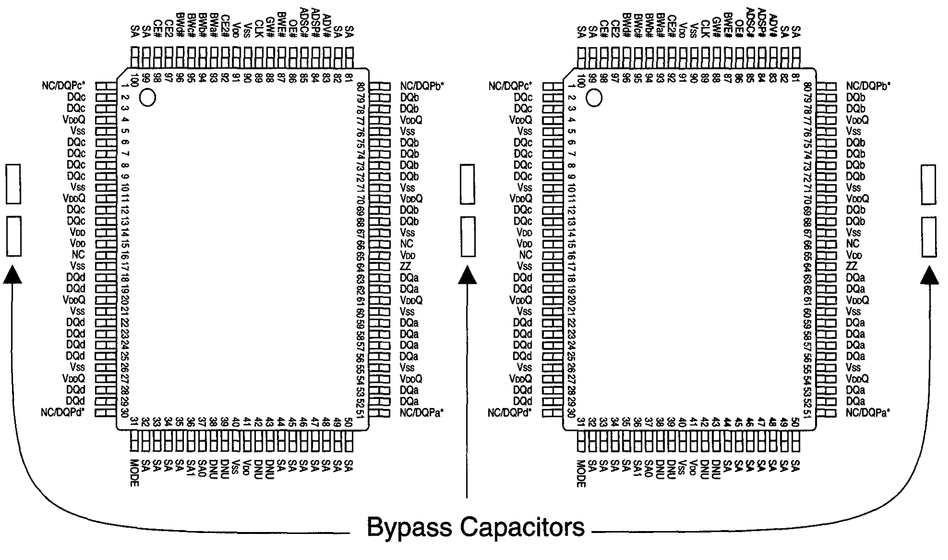


Figure 4
BYPASSING TWO HIGH-SPEED, 100-PIN TQFP PACKAGES

TECHNICAL NOTE

IBIS BEHAVIORAL MODELS

This article was originally published in 1996.

NTRODUCTION

A new standard for formatting analog models of digital ntegrated circuit I/O characteristics is beginning to merge and promises to provide fast, accurate simulations or transmission line and signal integrity analysis. This tandard is rapidly being adopted by semiconductor manufacturers and electronic design automation vendors to assist system designers in efforts to increase bus speeds with greater confidence.

The I/O-buffer information specification (IBIS) was developed at Intel® as a way of supporting designs for the entium® system. The IBIS specification provides a standard parsed file format of current/voltage (I/V) characteristics, device package parasitics and ESD protection device haracteristics for several types of I/O structures. Some of hese structures include ECL, open source, open drain and ristate.

SPICE vs. IBIS

IBIS models obtained from manufacturers have definite advantages over SPICE models. Most IBIS behavioral data s taken from actual devices. Thus, if the IBIS data is properly taken, the resulting model data has a direct correlation o the actual device. Another advantage is that IBIS models end to simulate much faster than SPICE models. Some sources quote as much as a 25-fold increase in the performance of IBIS over SPICE.

Why would you need IBIS-formatted models if SPICE nodels are available? The answer to this question is quite simple. Semiconductor manufacturers are reluctant to provide SPICE models of I/O structures to the public because he models often communicate confidential process and circuit design information or the manufacturer only has nodels for in-house silicon-simulation tools. When SPICE models are made available to the public, the models are often "sanitized" so that any proprietary information is masked. This can result in a model that does not accurately convey the analog behavior of the device. Whether or not the SPICE model is accurate depends on the nature of the proprietary information removed from the model and the extent to which the model made available to the public is maintained to reflect the latest process and design of the device.

STRUCTURE OF AN IBIS MODEL

The current version of IBIS is composed of five basic elements as shown in Figure 1 (Ref. 1) below. Element 1 is the pull-down structure, element 2 is the pull-up structure, element 3 contains the protection devices, element 4 is the intrinsic skew time for a rising or falling signal, and element 5 is the package parasitics. Within an IBIS file, each pin can have a different model to reflect differences in input or output structure.

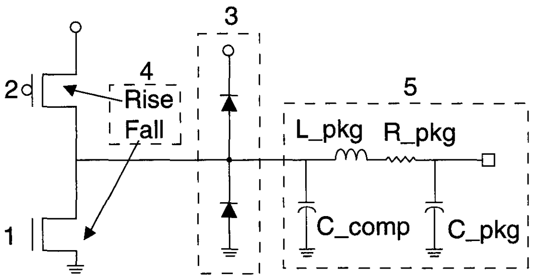


Figure 1
ELEMENTS OF AN IBIS MODEL

The following are examples of what the elements of an IBIS model look like when formatted for the IBIS file parser. Element 1 is the pull-down information that describes the I/V characteristics during pull-down. You can see that there is data for minimum and maximum current for given voltages. (These are temperature- and process-dependent specifications.)

[Pull-down]

| Voltage	I(typ)	I(min)	I(max)
|			
-5	-177.7m	-165.8m	-189.6m
-4	-149.5m	-138.8m	-160.1m
-3	-117.5m	-108.5m	-126.5m
-2	-81.4m	-74.5m	-88.3m
data omitted			
10	139.4m	128.6m	150.2m

You may notice that the data is taken for -VDD to 2VDD. The main reason the voltage sweep is done over such a wide range is that this allows a behavioral model for signal reflections caused by improper termination. Sweeping over this voltage range also allows modeling of the device for overshoot and undershoot situations when the protection diodes are forward biased. The current from the protection diodes is not included in this data. When the data is captured, the current from the protection diode is subtracted from the overall current before the current data is entered in the table. Diode current is later added by the simulator from model data when appropriate.

Element 2 contains data for the pull-up state of the buffer when the output drives high. This data is entered into the table using the formula VTABLE = VDD - VOUTPUT since the current through the pull-up device is dependent on the voltage between the output and VDD.

```
[Pull-up]
|
| Voltage     I(typ)      I(min)     I(max)
|
   -5         -223.0m     -204.0m    -242.0m
   -4         -197.4m     -190.7m    -204.0m
   -3         -161.8m     -156.6m    -167.0m
   -2         -125.3m     -118.6m    -132.0m
   data omitted.....
   10           0.0         0.0        0.0
```

The minimum and maximum values are determined by the minimum and maximum operating temperatures, supply voltages and process variations. With the minimum and maximum values for data points, a worst-case and best-case model can be assembled. By combining the highest current values with the fastest ramp time and minimum package characteristics, a fast model can be derived. A slow model can be derived by combining the lowest current with the slowest ramp time and maximum package characteristics.

Notice the keyword surrounded by square brackets before each element of the model. This keyword indicates the nature of the data that follows so that the simulator can either use the data from the parsed ASCII file directly or translate the data into a format used by the simulation software.

Element 3 contains data describing the ground and power clamp diodes.

```
[GND_clamp]
|
| Voltage        I(typ)       I(min)      I(max)
|
   -5            -188.3m      NA          NA
   -4            -144.9m      NA          NA
   -3            -109.3m      NA          NA
   -2             -58.9m      NA          NA
   data omitted.....
   10               0.1u      NA          NA
|
[POWER_clamp]
|
| Voltage          I(typ)       I(min)        I(max)
|
   -5               18.4m       NA            NA
   -4               11.6m       NA            NA
   -3                3.5m       NA            NA
   -2                0.8m       NA            NA
   data omitted.....
   10                0.1u       NA            NA
```

The power and ground clamp diodes are modeled in parallel with the driver information in the first two elements to ensure that the diode characteristics are present even when the output buffer is in tristate. Data for the diodes is taken with the output tristated (if possible) and is done using the same methods described above for the pull-up and pull-down structures.

Element 4 contains the ramp time for the pull-up and pull-down devices. This information is indicated by the keyword [Ramp] and is provided to ensure proper AC operation of the model.

```
[Ramp]
|              typ         min          max
dV/dt_f     1.98/58p   1.87/60.5p   2.09/56.9p
dV/dt_r     1.55/158p  1.46/160p    1.64/177p
```

The min and max columns represent the minimum and maximum slew rates for the buffers. These values are very small since they represent the intrinsic values of the transistors with all package parasitics and external loads removed.

Element 5 adds the component and package parasitics. C_comp is the capacitance of the die itself, excluding the package capacitance. The package characteristic resistance, inductance and capacitance are added by R_pkg, L_pkg, and C_pkg, respectively.

```
[Package]
|
|              typ        min         max
R_pkg        52mohm     51mohm      53mohm
L_pkg        6.425nH    3.33nH      9.52nH
C_pkg        0.875pF    0.4pF       1.35pF
•
data omitted.....
•
|              typ        min         max
C_comp       2.33p      2.17p       3.14p
```

Many of the capabilities of the IBIS model to simulate "real world" situations are actually dependent on the capabilities of the simulation software. The latest version of the IBIS format (Version 3.0) contains more keyword areas that provide necessary data to model such things as ground bounce, simultaneous switching output events, gradual turn on (slew rate controlled) outputs, etc. IBIS models cannot be used to measure propagation delays or provide timing information. The main purpose of IBIS data is to simulate transmission lines and analyze signal integrity issues.

IBIS OPEN FORUM

Analog simulator vendors, computer manufacturers and IC vendors have formed a group known as the IBIS Open Forum. This group is an open, voluntary association of companies that has worked to develop the IBIS standard in its present form. At the time of this writing, the group has managed to become part of the Electronics Industries Association and is working to get IBIS accepted as an EIA standard. This group has also assembled documentation (cookbook) outlining suggested methods for data extraction. Using the methods outlined in the "IBIS Cookbook," a model with the five elements shown in Figure 1 can be assembled.

There is a program available from the IBIS forum called the IBIS Golden Parser that checks an IBIS-compatible model for proper syntax. An IBIS model that follows the proper syntax can be used either directly by a simulator or translated into a format that can be used by a simulator. This program is available on several platforms and is offered at no charge by the IBIS forum. The source code is available for a nominal fee.

Not only can the data be extracted from empirical data, but a program developed at North Carolina State University translates SPICE to IBIS. The program works with Berkeley SPICE 2 and 3, PSPICE and HSPICE. This translator produces IBIS-formatted output from actual simulation results. The program is available in the public domain for semiconductor manufacturers and end users to use to generate IBIS models from SPICE models.

FUTURE VERSIONS OF IBIS

The process of proposing changes to the IBIS format is through a buffer issue resolution document (BIRD). Through this process, a majority vote of the forum ratifies proposed changes.

The latest IBIS version as of this writing is version 3.0. All versions (future and present) are backwards compatible with previous versions. Version 3.0 has been ratified as an EIA standard.

The IBIS committee is constantly working to improve the quality and quantity of information provided in IBIS standard files. New versions of the standard file format are constantly under review.

SOFTWARE VENDOR SUPPORT OF IBIS

As of this writing, there are 33 companies and organizations that have either participated in creating the IBIS specification or are creating/distributing/using IBIS models. As more models are made available and the IBIS format becomes more widely known, the number of software vendors supporting IBIS will increase.

MICRON SUPPORT OF IBIS

Micron has already produced IBIS models for several DRAM and SRAM devices; IBIS models for Flash devices are available upon request. Future support of IBIS will continue as long as we continue to receive customer requests for this type of assistance.

MORE INFORMATION

More information about IBIS and the IBIS Open Forum is available through the Internet. To subscribe to the IBIS Forum reflector, send your e-mail address to ibis-request@vhdl.org. The domain is 198.31.14.3. For more information, visit their Web site at www.eia.org/eia/ibis/ibis.html.

Information is also available through anonymous ftp at vhdl.org or by calling the VHDL International BBS (414) 335-0110. You will find documentation, IBIS Cookbook, recent press releases, Golden Parser, etc., residing in the pub/ibis directory.

REFERENCES

Duehren, D., W. Hobbs, A. Muranyi, and R. Rosenbaum. 1995. "I/O-buffer Modeling Spec Simplifies Simulation for High-speed Systems," *EDN*. March 16, 1995: 65-70.

TECHNICAL NOTE

USING VENDOR-SUPPLIED THERMAL IMPEDANCE

This article was originally published in 1997.

NTRODUCTION

The recent migration to 3.3V technology has dramatically helped to reduce power. Yet it still remains essential to perform an accurate thermal analysis of low-power memory omponents to ensure that the device is not overheating, hereby reducing its long-term reliability. This is especially rue as operating frequencies increase and bus widths widen. In this paper, we will discuss how Micron determines thermal impedance and how to best use these values.

THERMAL IMPEDANCE

To evaluate the thermal performance of a circuit, the total power dissipation of the device (including I/O) must be calculated. In doing so, there are several questions the designer must ask. Will this power level damage the device or cause long-term reliability problems? Is a heat sink or forced airflow necessary? Thermal impedance is used along with power dissipation to answer these questions. Calculating total power dissipation is covered in Micron Technical Note TN-05-14, "SRAM Thermal Design Considerations.")

A simplistic way of evaluating thermal performance is to ensure that the maximum power dissipation is not exceeded. Some previous generations of SRAMs have specified a maximum power dissipation of one watt. If the power dissipation was significantly under one watt, it was assumed that the device would operate with no thermal problems. If the power dissipation was approaching or exceeding one watt, then a more detailed thermal analysis was necessary to determine if some type of cooling was required (airflow over the device, heat sink, etc.).

Using maximum power dissipation is not the preferred method of thermal analysis. A number of other variables can significantly affect the thermal properties of a design. These include the package (molding compound, leadframe), circuit board (materials used, thickness and number of metal layers), the proximity to a fan or other devices, etc.

A better method of thermal analysis is to determine the unction temperature of a device based upon power dissipation and thermal impedance. The lifetime of a component is directly related to the operating temperature. For nstance, Intel® has stated that every 10°C rise above the operating (temperature) range of Pentium® parts results in a halving of the MTBF (Ref. 1). Micron has specified an absolute maximum junction temperature of +150°C but recommends a significantly lower temperature to maximize device lifetime.

To calculate the junction temperature, the thermal impedance of the device must be known. Although the junction temperature cannot be directly measured, the case temperature and ambient temperature can. Therefore, either a junction-to-case thermal impedance (θ_{jc}) or junction-to-ambient (θ_{ja}) is needed to calculate the true junction temperature. Junction temperature is calculated using one of the two equations below:

$T_j = T_c + P\theta_{jc}$ (if case temperature is known)
$T_j = T_a + P\theta_{ja}$ (if ambient temperature is known)

T_j is the junction temperature, T_c is the case temperature, T_a is the ambient temperature and P is the power dissipated by the device.

HOW IS THERMAL IMPEDANCE DETERMINED?

Thermal impedance for Micron devices is detailed in the *Reliability Monitor*, published for each component family. (Contact the Micron Literature Room at 208-368-3945 to request a copy.) One way of measuring thermal impedances is by placing a package into an IC socket with a thermocouple glued to the topside of the package to measure case temperature. The contact area with the thermocouple is minimized so that it will not act as an additional heat sink. The measurements are taken with the IC package inserted into the same socket assembly but suspended inside a one-cubic-foot closed container which provides a still-air environment. The junction temperature is measured by characterizing the IC's input pin to substrate voltages at various temperatures.

The problem with the above method is that the numbers given are worst-case values for thermal impedance and may give a significantly higher junction temperature than would actually occur in a system (Ref. 2). In a real-world system, the socket is soldered onto a circuit board and the leadframe conducts heat away from the die into the metal of the power planes and traces of the circuit board. Variations in the number and thickness of the signal and power layers of a board can also influence actual thermal resistance. One study has concluded that this can change the θ_{ja} of a package by 25 to 50 percent and that θ_{jc} is significantly affected by the entire system in which the package is mounted (Ref. 3). Placement of a heat sink on a device or forcing air over the device will also provide an easier path for heat conduction and thereby affect the actual thermal impedance of the system. Although the above method may be inaccurate for determining real-world junction temperatures, it is valid in comparing the thermal resistance among different IC vendors. It is also useful in making a preliminary estimate to see if heating problems will occur in a system.

Using still-air suspended thermal impedance values may force a designer to cool a device when it may not be necessary. Thermal data was taken from Micron devices that were soldered onto a printed circuit board, measuring 4.25 x 1.125 inches, with four layers. The device used in these calculations was a 2Mb SyncBurst™ SRAM in a 100-pin TQFP package. In a still-air suspended environment, θ_{ja} was 40°C/W and θ_{jc} was 4°C/W. In a circuit board, θ_{ja} was 25°C/W and θ_{jc} was less than 2°C/W. As you can see, the PCB board provides a significant difference in the thermal impedance of the device.

The measurement of thermal impedance may vary from vendor to vendor so it may be difficult to compare thermal numbers. For an exact comparison, a similar method should be adopted. Currently, the JEDEC standardization committee is evaluating several different approaches with the goal of developing a standard method of measuring thermal impedance. This evaluation method will probably consist of a circuit board with a set number of layers (both power planes and signal layers), specified area and thickness. A device can then be soldered to this board and tested both in still air and forced air to determine a thermal impedance that will more accurately reflect real-world conditions.

WHAT IS A DESIGNER TO DO?

Most designs require the components to be second-sourced. Just as the comparison of timing and power dissipation among vendors is important to the design process, so is the need to make thermal comparisons. The still air and suspended technique described above is a method to compare different vendors' parts and should reveal gross disparities in thermal performance between vendors. However, the preferred method will be to use the JEDEC-standard approach (once approved) and compare thermal impedances determined from parts mounted on standardized boards. Users will benefit from this comparative approach as vendors are moving toward taking thermal data from circuit boards. Micron will be providing thermal data for all new devices using this superior method.

Vendor-supplied thermal measurements taken with circuit boards will certainly provide more accurate numbers for users, but how will those numbers compare to an actua application? This is a fundamental question facing users. If the size of the board and the number of layers are similar then it may be valid to use the vendor-supplied θ_{ja} and θ_{jc} and compute the junction temperatures. Even if the board is somewhat different, using the thermal numbers may still be valid if the computed junction temperature is very low

There are cases where vendor-supplied thermal impedance values may not be accurate enough for use in thermal calculations, such as when the circuit board is very different than the vendor's. It can also occur when the junction temperature is higher than desired and the user is trying to make a choice as to what type of fan/airflow to include in a system. Purchasers of bare die for use in multichip modules (MCMs) or flip-chip applications will not be able to use any vendor-supplied data. These users may have to use a finite element analysis tool in order to simulate the thermal properties of their chip and board.

It would also be helpful to users if thermal impedance could be calculated for various airflows. Forced airflow is common in many designs and having vendor-supplied data for a package with various airflows is becoming essential.

CONCLUSION

Thermal impedance values provided from chip manufacturers are useful in performing thermal analysis of systems. Thermal resistances calculated under still-air and suspended environments will give worst-case junction temperatures, and these may vary significantly from real-world conditions that occur once the device is soldered onto a multilayer circuit board. Similarly, forced airflow will reduce the thermal resistance of the device. Micron Applications Engineers are available to assist customers with questions regarding thermal analysis of circuit boards.

REFERENCES

Intel's "Pentium™ Processors and Related Products." Mt. Prospect, IL: Intel Corp., 1995, pp. 2-645.

J. A. Andrews, "Package Thermal Resistance Model: Dependency on Equipment Design," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Vol. 11, No. 4, December 1988, pp. 528-537.

D. Billings and R. P. Stout, "Effect on Observed Package Thermal Performance of System Board Metal Content," in *Proceedings of the 1995 IEEE 11th Annual Semiconductor Thermal Measurement and Management Symposium*, San Jose, CA, 1995.

TECHNICAL NOTE

ACCELERATE DESIGN CYCLES WITH MICRON SIMULATION MODELS

his article was originally published in 1997.

NTRODUCTION

Design engineers face many difficulties when approach- g the design of a high-frequency memory bus interface. wo of these problems require assistance from the silicon endor: signal integrity and logic circuit design. Signal tegrity has become an issue due to the high bus speeds sed with the latest processors. Close attention must be aid to high frequency design rules for layout and imped- nce matching. The second issue, the increasing complexity f memory devices, has developed because logic that was nce relegated to the memory controller is now migrating ward the memory device. This requires, in some in- ances, obtaining logic models from the semiconductor anufacturer to validate the logic designs for interfacing to e memory device.

Micron has recognized these difficulties and has begun fforts to supply the tools necessary to verify new designs rior to layout. Published data sheets alone are no longer nough to complete a design. The trend is moving toward lectronic data books where the "data sheet" is not just a rinted specification but also includes an input/output /O) behavioral model and, in some cases, a logic behav- ral model. Making these tools readily available will help reamline the design process, giving customers faster de- gn turnaround, as well as a high degree of confidence in ecifying Micron parts.

ECIDING WHICH MODELS TO PROVIDE

Micron currently provides signal integrity analysis tools r all of its products as part of an internal qualification rocess. The parameters used for the analog I/O models are btained from laboratory measurements performed by the roduct engineering department. These parameters are en formatted into an Input/Output Buffer Information pecification (IBIS) file. For more information about IBIS- rmatted files, see Micron Technical Note TN-00-07.

Because so many resources are required to generate a lly functional logic model for a complex device, the ecision to provide one is not made lightly. Factors which ust be considered include customer demand for the model, e complexity of the device compared to preceding related evices, the length of time the product has been on the arket prior to our entry, and the level of support provided y Electronic Design Automation (EDA) tools vendors or ird-party model developers.

SUPPORT AND DISTRIBUTION OF MODELS

All of Micron's IBIS models are updated as new die revisions are qualified or as bugs are discovered. IBIS models are available on Micron's Web site (www.micron.com/mti/msp/models/index.html); technical support is available by calling 208-368-3900.

ANALOG MODELS FOR SIGNAL INTEGRITY ANALYSIS

VALIDATION OF IBIS MODELS

Micron's IBIS models are entered into a verification loop before they are released. This process validates proper operation of the IBIS model compared to internal SPICE models and waveforms captured from memory testers. Figure 1 shows the test flow for validating IBIS models.

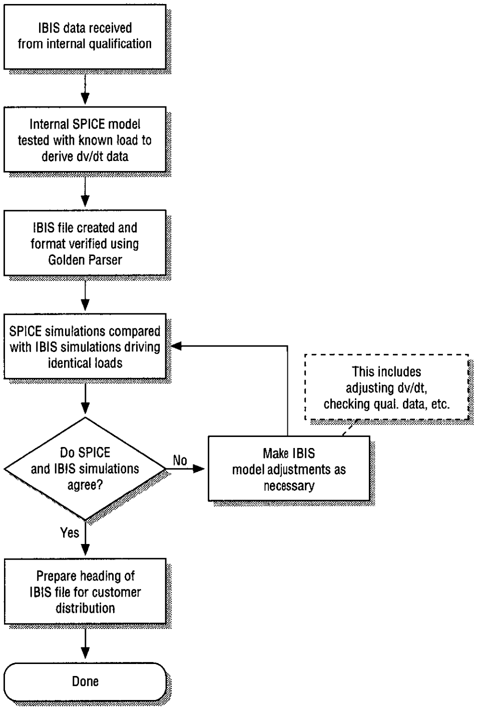


Figure 1
IBIS MODEL VALIDATION FLOW

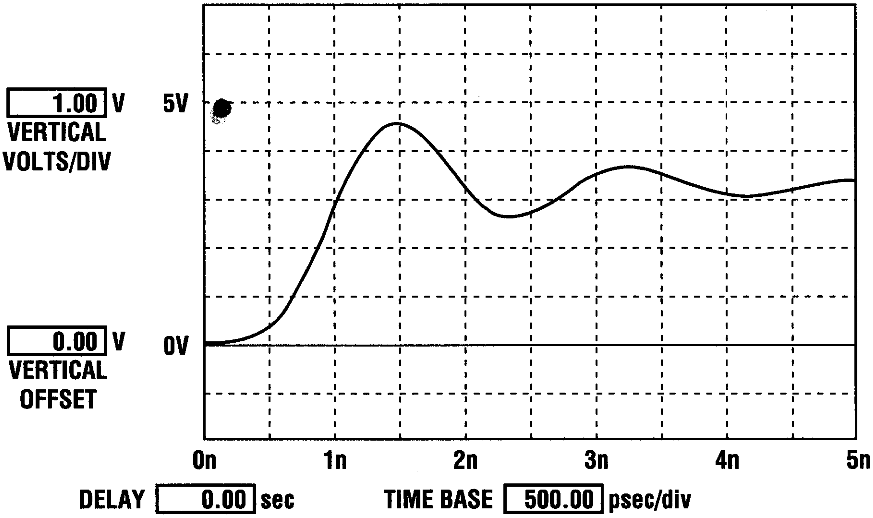
The IBIS model validation process begins with validating the model against Micron's internal SPICE model for the same I/O buffer. The SPICE models are verified during the design process and serve as a solid reference point for testing the IBIS model. Tester waveforms are also used to check the IBIS model by driving the IBIS model into a model of the tester load and comparing the output with the actual tester waveform. The load used when checking the IBIS model against the SPICE model is varied to exercise the IBIS model over a sufficient range. This gives a better indication of how the IBIS model reacts to overshoot or undershoot for inputs and how accurately it behaves when driving transmission lines and high loads.

If there are discrepancies between the IBIS model behavior and the SPICE results, the model is checked for entry errors and other obvious errors that the Golden Parser is not designed to trap. If no entry errors are found, each discrepancy is evaluated to determine which part of the IBIS model caused the inconsistency with the SPICE simulation. For instance, if the IBIS model had much higher overshoot or undershoot than the SPICE model for a given load, then the dv/dt for the IBIS model would be adjusted and the model again simulated. Adjusting the die capacitance parameter or any of the packaging parasitic is not as feasible as adjusting the dv/dt parameter since device parasitic is accurately measured as part of the device qualification process. This process is repeated until the IBI simulation matches the SPICE results.

Figures 2a and 2b illustrate the correlation between a IBIS simulation and SPICE simulation for a Micro MT4LC4M4DJ (4 Meg x 4 DRAM). The correlation betwee the SPICE simulation and IBIS simulation shows that fo many situations, IBIS models prove adequate for critica path analysis.

I/O MODELS SPEED BOARD DESIGN

With ever increasing clock speeds, the need to perfor signal integrity analysis early in the design phase is becoming tantamount to the importance of circuit logic design. I has been common practice to perform signal integrity analysis after layout is completed. However, under conditions o intense competition and short product cycle times, findin a bug after the layout is completed can cause a product t miss its window of opportunity. To avoid this proble many EDA tools are now providing a vehicle to perfor signal integrity analysis in conjunction with layout an routing. By performing signal integrity analysis durin routing, or even prior to layout, a post-layout debug cycl can be avoided. This blurs the demarcation between computer system design and CAD layout. The logic designe



DATE: 4/25/1996 at 13:56
LINESIM PRO VER 3.21
FILE: D24CDIMM.TLN

Figure 2a
IBIS RESULTS

must start taking a more active role in determining the consequences of proper layout by communicating design choices to the layout engineer early in the design process. But in order for this scenario to play out, accurate I/O models must be available.

In the past, bus speeds were slow enough that routing was netlist-driven, and vendor-supplied I/O models were not necessary to complete a design. Today, however, semiconductor manufacturers are increasingly required to assume a more active role in the design and layout process.

PRINTED CIRCUIT BOARD (PCB) LAYOUT AUTOMATION WITH IBIS AND RAIL

With bus speeds increasing and routing becoming more rules-driven as opposed to netlist-driven, accurate I/O models for integrated circuits have become a requirement. To help automate rules-driven routing, a standard method for communicating design guidelines among semiconductor vendors, PCB layout software vendors and hardware design teams is being developed. If the I/O model can be combined with a description of signaling and layout constraints and be used directly in an EDA tool that integrates layout with simulation, then the time taken for design layout can be greatly reduced.

A new file format intended for the integration of I/O models with descriptions of design constraints is being developed by an industry consortium which includes silicon vendors, EDA tools vendors and interested designers. The format for presenting the design constraints is described by a standard file format complementary to IBIS called Rule Augmented Interconnect Layout (RAIL).

RAIL allows a silicon vendor to describe recommended operating conditions for which its component is designed. The RAIL file dictates electrical constraints such as flight times, skews, undershoots, etc. The RAIL layout constraints are simulated and judged using IBIS-formatted models. IBIS files are then used to provide the necessary information to model the performance of net drivers and receivers. RAIL files then specify the design constraints necessary to evaluate the acceptability of the measured performance for a given design.

In order to develop the design constraints for final layout detailed by RAIL files, contributions by both the silicon vendor and the hardware designer are necessary. Figure 3 outlines the process to obtain and use the final RAIL file and how to use it with the EDA tool. The silicon vendor develops a RAIL file that contains constraints derived for a standard application. That file is further modified to fit the

Figure 2b
SPICE RESULTS

constraints derived by the design engineer. Then, using the RAIL file, along with any IBIS files, the design is either hand- or auto-routed and design constraints are verified throughout the routing process. This allows an overlap of routing and signal integrity analysis instead of the common method of post-route design verification.

The RAIL file is used in hand-route or auto-route software with integrated simulation capability. In either case, the software dictates the correct layout based on the design constraints outlined in the RAIL file. Like IBIS, the RAIL files are human readable and machine parsable, and they follow a common format. The RAIL format is still in the developmental stages even though there is very active EDA vendor support. Micron will continue to evaluate the use of RAIL as the standard emerges.

Currently, IBIS files are being used with pre- and post-layout software tools. By identifying problem areas before prototype builds, design iterations can be avoided. Micron currently uses Hyperlynx LineSim Pro to verify IBIS files. A tool similar to LineSim Pro would be one method for semiconductor vendors to determine constraints for RAIL-formatted files.

Almost all major EDA tools vendors are supplying tools that are IBIS-capable, and the IBIS committee is continuing to work on increasing the breadth of operating conditions covered by IBIS-formatted models. While skeptics still question the validity of using behavioral models in lieu of transistor-level models, in the majority of situations, behavioral models are adequate—as has been proven by the many successful designs that have been verified using IBIS models.

REMAINING MODELING DIFFICULTIES

Beyond the typical difficulties associated with acceptance, the various packaging of semiconductor devices also presents a problem. This issue becomes more obvious when memory modules are viewed as another packaging technology. Having only a behavioral model of the component does not provide good behavioral accuracy when the component is packaged as a module.

To address this problem, the IBIS committee is now considering two extended package formats that will enable accurate modeling of components packaged as modules. The first format under consideration models the module dimensionally. The file is comprised of dimensional and layer information about traces on the PCB. Adding this information, together with the packaging and I/V characteristics of the integrated circuits, can enable a properly designed EDA tool to extract electrical characteristics of the added package parasitic. This allows the module traces to be modeled as transmission lines rather than being lumped as parasitic. The dimensional data can be presented similarly to the stack-up information available from any layout tool. Most EDA tools are already designed to accept data in this kind of format.

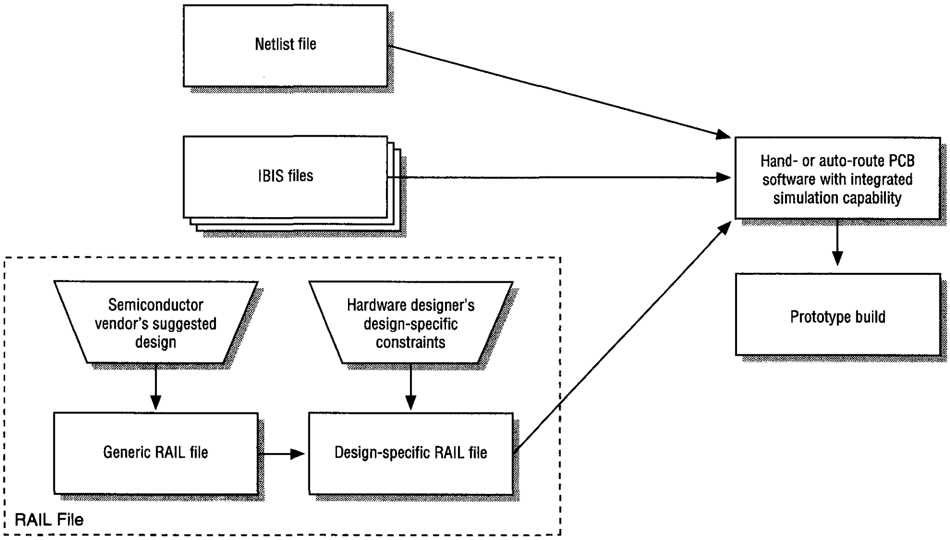


Figure 3
AUTOMATED RULES-CONSTRAINED DESIGN USING RAIL AND IBIS FILES

The second method for extending the package model llows the addition of components attached to boards, onnectors and cables. This method involves describing the onnections electrically by creating matrices that describe nutual inductances and capacitances. Included in this decription are the values of inductances and capacitances per mit length of the connection. The coefficients of such lescriptions can be extracted from field solvers or meaured on the bench. This package extension can more ccurately model IC interconnects as well as interconnects nternal to the IC. For example, a bond wire can be modeled s sections of resistor-inductor-capacitor (R-L-C). Another rea addressed by the electrical description is the package arasitics, which can be associated three-dimensionally for levices such as multichip modules. This enables field solvrs to model cross-talk for device interconnects.

Without a standard format for modeling memory modles, the burden of providing accurate electrical models rom the motherboard, through the connector, to the comonent on the module, rests with the design engineer. An xample of one such model is shown in Figure 4. Figure 4 is model of an I/O for Micron's SyncBurst™ SRAM "cache n a stick" (COASt) module.

To model the Burndy CELP connector, electrical characerization was obtained from the socket manufacturer. Aicron's IBIS model for the SyncBurst SRAM was used, along with signal trace characteristics taken from dimensional data for the COASt module. The IBIS model for the Pentium® output driver was obtained from public sources on the Internet, and the signal trace from the Pentium to the module socket was estimated for a worst-case length.

In the simulations, the IBIS models for the components were varied over fast, slow and typical conditions to obtain results over a wide range of operating temperatures and process variations. All of this can be contained and modeled using an IBIS representation. The model was developed and simulated using Hyperlynx LineSim Pro, which allows quick and easy verification of how varying terminations and trace lengths can affect design performance prior to layout.

Until a standard format is available for representing module parasitics, parasitic resistances and capacitances added by the PC board will be represented as lumped values within the IBIS-formatted component model. Further testing is needed to determine the accuracy of this format vs. providing dimensional information about lead traces on the module, so customers can develop a model such as that shown in Figure 4. The results of additional testing will determine the type of modeling information that will be provided to assist customers in modeling Micron's modules.

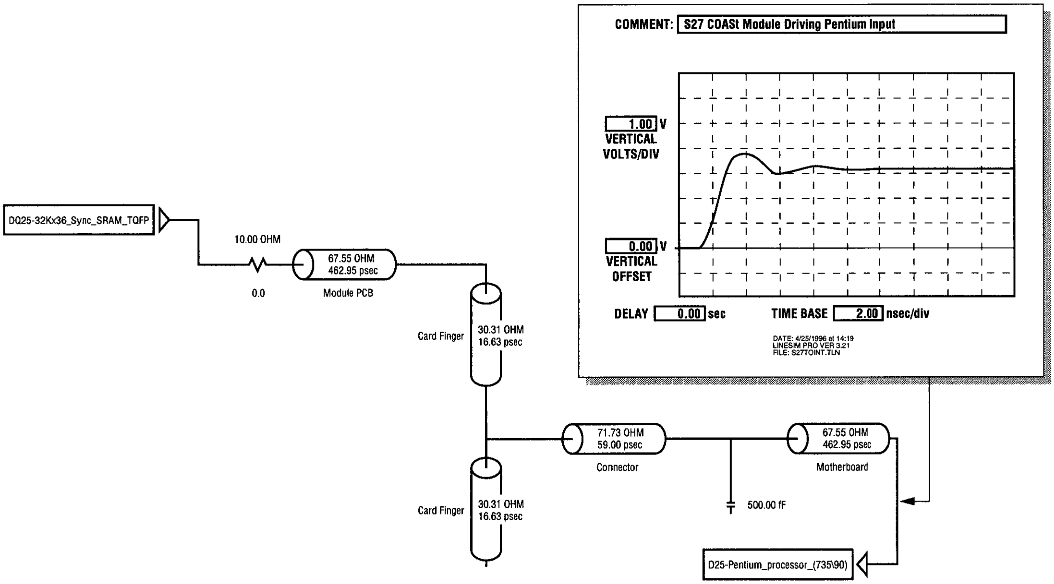


Figure 4
MICRON'S SYNCBURST SRAM "CACHE ON A STICK" (COASt) MODULE

LOGIC MODELS FOR CIRCUIT DESIGN VERIFICATION

VALIDATION OF VHDL/VERILOG MODELS

Logic models provided by Micron are written in the two most popular logic synthesis languages: Verilog and VHDL. The decision to provide both Verilog and VHDL models follows from the worldwide use of both languages by Micron customers and the fact that both are IEEE standard languages. Today, many EDA tools used for logic simulation and synthesis provide co-simulation capability. With co-simulation tools available from most major EDA vendors, someday logic models will be provided in only one language.

The verification process for Micron's logic models extends to the operation described in the data sheet specifications. Micron manufactures devices that follow specifications established by the JEDEC standards committee; therefore, all product data sheets describe only the industry-wide accepted operating modes of the device. Operating modes that are particular to Micron's design are not described in the data sheets. Similarly, and as a service to customers who may use competitors' designs, Micron's logic models are not written to emulate any operating modes outside data sheet specifications.

After the preliminary code describing the design behavior is written, test vectors are developed that test the timing checks and logic of the logic model. The test bench is written to test for race conditions, invalid logic implementation and proper operation of the output logic. When minimum and maximum times are given for a timing parameter, the model is written so that unknown states are placed on the bus for times between the minimum time the bus may not be available and the time a known state will be on the bus. This way, a circuit is verified to the worst-case conditions available from the device.

The test bench is also written to provide input variables through a text file. The test bench then applies the inputs to the behavioral model, and the output is verified against data sheet specifications. Conditions of operation are varied so all possible combinations of state transitions can be simulated to verify proper operation, and all example conditions presented in the data sheet are tested and verified. Then, all timing violation checks are tested and verified to the timing parameters given in the data sheet.

USING LOGIC BEHAVIORAL MODELS PROVIDED BY MICRON

Traditional design verification techniques require a set of test vectors that represent all possible input combinations developed by the design engineer. These test vectors are then applied in design simulations, and the output from the simulations is compared to the design specifications. This is the method Micron uses to verify logic behavioral model designs. However, when a complex design such as an ASIC is developed using languages such as VHDL or Verilog, these techniques become prone to errors because they rely on interpretations between simulation output and expected output. In addition, any functionality missed by the test vectors will be missed by the simulation.

There are now formal design validation tools being developed that compare two levels of a design description to verify correct logic at the gate level. These tools can validate a behavioral description of a design against a register transfer level (RTL) description before synthesis is completed. The logic models provided by Micron assist in developing an accurate behavioral model. Without a behavioral model of the memory device, validation of the design behavioral model interfacing to the memory device becomes an exercise in validating the design behavior against memory device data sheet specifications. Without the memory device behavioral model, design errors can be made at the behavioral level, thus propagating design errors to the RTL level. This is why a behavioral logic model of the memory device can be crucial to a successful design.

Using a behavioral logic model to verify a design depends on the experience the hardware designer has had with a particular type of device and the complexity of the device. Often, logic interfaces to memory devices can be designed without the aid of a behavioral model because data sheet specifications provide enough information to complete the design. However, as memory devices perform more complex functions, it becomes extremely difficult, and even impossible, to verify a design prior to hardware implementation without the aid of a behavioral logic model. Because behavioral logic models are required to complete simulation verification of a design, Micron has developed behavioral logic models for Extended Data-Out (EDO) and Synchronous DRAMs, Synchronous Graphics RAMs (SGRAMs), SyncBurst SRAMs and Zero Bus Turnaround™ (ZBT™) SRAMs to help expedite controller designs. Future model development will depend on device complexity and customer demand.

SUMMARY

Micron has assumed an active role in helping customers complete new designs faster and with a greater degree of confidence. Increasing bus frequencies demand that analog I/O models be available to complete signal integrity analysis of a design. As more complex functions are incorporated into the memory device, behavioral logic models become a requirement to complete simulations for circuit verification. Having recognized this, Micron will continue improving customer service by providing software model support.

TECHNICAL NOTE

MICRON MEETS THE NEED FOR SIMULATION MODELS

his article was originally published in 1998.

ENERAL DESCRIPTION

As memory devices become more and more complex, the lemands for simulation models continue to increase. Comanies are turning to IBIS, SPICE, Verilog and VHDL simuation models to accelerate design cycles through accurate imulation and to reduce costs through verification of deign, prior to prototype.

IBIS and SPICE are analog simulation models for signal ntegrity analysis. IBIS data is obtained from circuit simulaion or laboratory measurement performed by product ngineering departments using a curve tracer or oscillocope. This data is then formatted in tabulate voltage versus urrent (V/I) characteristics, timing characteristics, packge information and I/O structures. Finally, the IBIS file is hecked, simulated and verified against a SPICE simulation r actual device for the same I/O buffer. Any model created sing IBIS format is compatible with most industry-wide simulation platforms. For more information about IBIS-formatted files, see Micron Technical Note TN-00-07.

SPICE data is obtained from circuit simulation. With SPICE models, circuit blocks may be represented as behavioral models and simulated in a functional form. This allows designers to test and verify circuit theory during the design process, thus saving time and money in the development of the transistor and component levels of the actual device. SPICE models also serve as a solid reference point for testing IBIS models.

Verilog and VHDL are logic simulation models used in circuit design verification. To best serve our customers, all of Micron's logic simulation models are written in both Verilog and VHDL. Micron's models are derived from our published data sheets and specifications. We test our models using test vectors that represent possible input combinations developed by the design engineer and then compare the outputs from the model simulations to the data sheets and specifications to make sure they are correct. Once the

Table 1
MICRON'S SIMULATION MODELS

	DENSITY	IBIS	SPICE	VERILOG	VHDL
DRAM	16Mb	✓		✓	✓
	64Mb	✓		✓	✓
SGRAM	8Mb			✓	
SDRAM	16Mb	✓	✓	✓	✓
	64Mb	✓	✓	✓	✓
	128Mb			✓	✓
SDRAM DDR	64Mb	✓		✓	✓
SGRAM DDR	16Mb			✓	
SyncBurst™ SRAM	1Mb		✗	✓	✓
	2Mb	✓	✗	✓	✓
	4Mb	✓	✗	✓	✓
	8Mb			✓	✓
ZBT™ SRAM	2Mb		✗	✓	✓
	4Mb		✗	✓	✓
	8Mb			✓	✓
Flash	4Mb	✗	✗		
	8Mb	✓	✗		

Simulation models currently available.
Simulation models available upon request.
formation is subject to change. Please check our Web site (www.micron.com/mti/msp/models/index.html) for the latest model information.

outputs are verified, customers can use the logic models—along with a set of test vectors—to test, verify and finalize their own designs.

Micron models currently assist engineers in the design of memory controllers for 3D graphics chips, networking (LAN) products, board simulations and countless other designs. Customers can be assured that our analog and logic simulation model offering will continue to expand to meet their needs.

Table 1 shows Micron's current modeling support for selected memory devices. Visit Micron's Web site (www.micron.com/mti/msp/models/index.html) for the latest model information.

DRAM TECHNICAL NOTE SELECTION GUIDE

For the latest technical information on Micron products, read our quarterly technical newsletter *Design Line*.
Call 208-368-3900 to be added to our mailing list or visit our Web site (www.micron.com/mti/msp/html/dlindex.html).

TECHNICAL NOTE

OE#-CONTROLLED LATE WRITE CYCLES (DRAM)

This article was originally published in 1991.

INTRODUCTION

There are three cycles available to write to a DRAM: EARLY WRITE cycles, READ-MODIFY-WRITE cycles and LATE WRITE cycles. The industry-standard definitions for DRAM WRITE cycles are fairly consistent for both the EARLY WRITE and READ-MODIFY-WRITE cycles. An exception exists for the LATE WRITE cycle.

COMMON DQ DRAM (x4, x8, etc.)

A LATE WRITE cycle is a READ-MODIFY-WRITE (see Figure 1) except that the READ portion is not utilized. This is accomplished by keeping the output enable pin (OE#) HIGH throughout the cycle. The timing parameters ^{t}RWD, ^{t}AWD and ^{t}CWD no longer apply since OE# is HIGH.

This condition may be viewed as an EARLY WRITE with ^{t}WCS "sliding" past the CAS# time and violating the 0ns setup time (WE# going LOW prior to CAS# going LOW). However, since the output buffers are not being used (OE# is HIGH), ^{t}WCS and ^{t}CWD are no longer required.

If WE# transitions LOW after CAS# transitions LOW, do not bring OE# LOW (a noise spike may occur) because the output buffers could turn on and cause contention with the data bus, which could corrupt input data.

The term used for this type of a WRITE cycle varies throughout the industry. "OE#-controlled WRITE," "delayed WRITE" and "LATE WRITE" all signify the WRITE cycle being described.

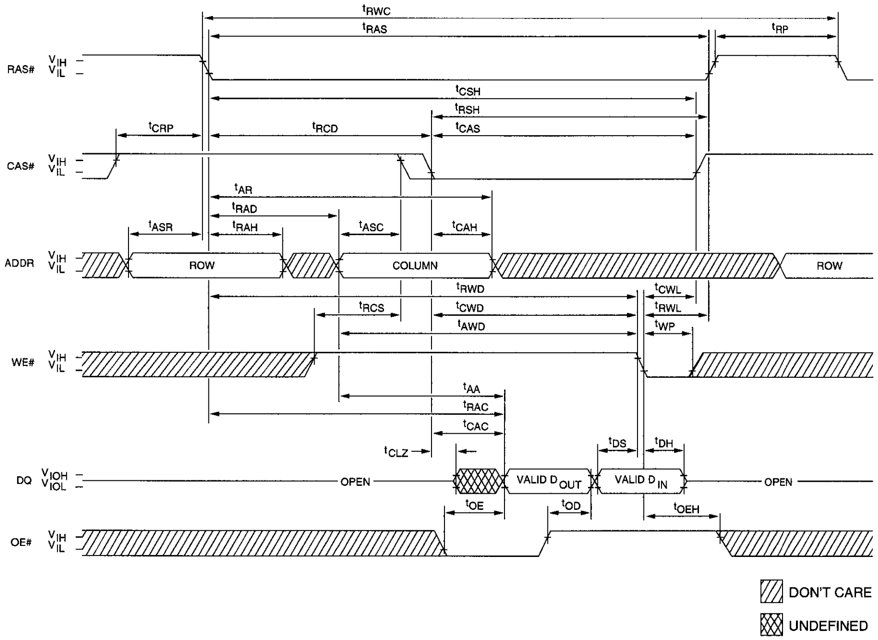


Figure 1
READ-MODIFY-WRITE (MULTIPLE DQ) TIMING

SPLIT D AND Q DRAM (x1)

A LATE-WRITE cycle is a READ-MODIFY-WRITE, except the READ portion is not guaranteed and the D and Q pins are separate paths (D and Q cannot be connected). This is accomplished by ignoring the timing parameters ^{t}RWD, ^{t}AWD and ^{t}CWD.

This condition can be viewed as an EARLY WRITE with ^{t}WCS "sliding" past the CAS# time and violating the 0ns setup time (WE# going LOW prior to CAS# going LOW). However, since the output buffers are "Don't Care," ^{t}WCS and ^{t}CWD are no longer required.

This cycle is not available on applications that have the D and Q connected together because the output will contend with the input.

SUMMARY

A LATE WRITE cycle is most useful on common DQ DRAMs. Use caution to ensure that the output enable pin is properly controlled.

TECHNICAL NOTE

DRAM TIMING PARAMETERS

This article was originally published in 1992.

INTRODUCTION

A DRAM has many timing parameters which are specified to help the memory designers define memory system timing. These parameters may be separated into several groups. This note separates these parameters as core parameters (COP) or calculated parameters (CAP).

The calculated parameters are tested by Micron prior to shipment. In cases where the summation of COP parameters is larger than the CAP parameter specification, the CAP parameter overrides the summation of COP parameters. Additionally, if an incoming test is required, the testing of the COP parameter is typically sufficient since CAP parameters are simply combinations of COP parameters.

The CAP parameters are listed below, showing how they are calculated. This will aid the memory designer's understanding of the parameters affected when a COP parameter is altered. Additionally, during testing of the COP parameters, the CAP parameters are also tested by default.

^{t}RC	=	^{t}RAS + ^{t}RP + 2^{t}T
^{t}PC	=	^{t}CPA
^{t}AR	=	^{t}RCD (MAX) + ^{t}CAH
^{t}RSH	≈	^{t}CAS
^{t}CSH	=	^{t}CAS + ^{t}RCD (MAX)
^{t}CPA	=	^{t}AA + ^{t}T
^{t}AA	≈	^{t}RAS/2
^{t}DHR	=	^{t}RCD (MAX) + ^{t}DH
^{t}WCH	=	^{t}WP - ^{t}WCS - ^{t}T
^{t}WCR	=	^{t}RCD (MAX) + ^{t}WCH
^{t}RAD (MIN)	=	^{t}RAH + ^{t}T
^{t}RAD (MAX)	=	^{t}RAC - ^{t}AA
^{t}RCD (MIN)	=	^{t}RAD + ^{t}ASC + ^{t}T = ^{t}RAH + ^{t}ASC + 2^{t}T
^{t}RCD (MAX)	=	^{t}RAS - ^{t}CAC
^{t}RWD (x1)	=	^{t}RAC
^{t}RWD (x4)	=	^{t}RAC + ^{t}OD + 3^{t}T + ^{t}DS
^{t}CWD (x1)	=	^{t}CAC
^{t}CWD (x4)	=	^{t}CAC + ^{t}OD + 2^{t}T + ^{t}DS
^{t}AWD (x1)	=	^{t}AA
^{t}AWD (x4)	=	^{t}AA + ^{t}OD + 2^{t}T
^{t}RWC (x1)	=	^{t}RWD + ^{t}RWL + ^{t}RP + 3^{t}T
^{t}RWC (x4)	=	^{t}RAC + ^{t}RWL + ^{t}RP + 4^{t}T + ^{t}OD + ^{t}DS
^{t}PRWC (x1)	=	^{t}CPA + ^{t}CWL + 2^{t}T + ^{t}DS
^{t}PRWC (x4)	=	^{t}CPA + ^{t}CWL + 4^{t}T + ^{t}OD + ^{t}DS

TECHNICAL NOTE

LPDRAM EXTENDED REFRESH CURRENT vs. RAS# ACTIVE TIME

This article was originally published in 1992.

INTRODUCTION

One of the most significant features of the low-power extended refresh DRAM (LPDRAM) is its cycle. Extended refresh is essentially a CAS#-BEFORE-RAS# (CBR) REFRESH at an extended refresh rate of 125µs per cycle.

RAS# pulse width (^{t}RAS) affects the extended refresh current and should be considered when designing a low-power system. The longer RAS# is held LOW, the more current an LPDRAM will consume while in the extended refresh mode. Therefore, keeping ^{t}RAS at a minimum will maximize power savings.

Figure 1, a typical curve of Micron's 4Mb LPDRAM (MT4C4001J S and MT4C1004J S) shows the relationship between its extended refresh standby current and the width of ^{t}RAS.

SUMMARY

The ^{t}RAS time should be kept as short as possible when designing memory array timing. This will result in lower standby currents, especially for the extended refresh cycle.

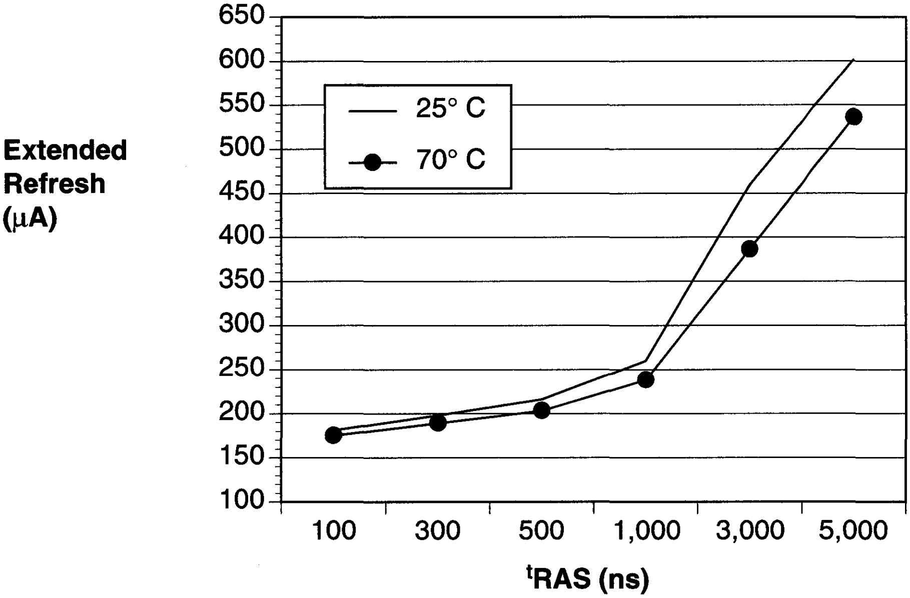


Figure 1
TYPICAL EXTENDED REFRESH CURRENT AS A FUNCTION OF ^{t}RAS

TECHNICAL NOTE

16Mb DRAM—2K vs. 4K REFRESH COMPARISON

This article was originally published in 1993.

INTRODUCTION

Micron Technology, Inc., offers its 4 Meg x 4 DRAM in one of two JEDEC-approved versions. One of the JEDEC versions requires 12 row-address bits and 10 column-address bits for 4,096 (4K) cycle refresh in 64ms. The other (Micron's MT4C4M4B1) requires 11 row-address bits and 11 column-address bits for 2,048 (2K) cycle refresh in 32ms. Excluding this difference, the timing and performance of the two devices are identical.

Industry demand for decreased power consumption led JEDEC to approve 4K refresh in addition to 2K refresh at the 16Mb level. At minimum random cycle time (^{t}RC = 110ns), a 4 Meg x 4 device with 4K refresh draws ≈30mA less operating current than a device with 2K refresh. The current is decreased by increasing the number of rows and decreasing the number of columns in the DRAM array. A 4 Meg x 4 with 4K refresh has 4,096 rows and 1,024 columns, whereas one with 2K refresh has 2,048 rows and 2,048 columns. The number of columns defines the "depth" of a page. The drawing below shows how 2K and 4K refresh devices are different. Notice that the 2K device has a page depth of 2,048, while the 4K device has a page depth of 1,024, or half the page depth of the 2K device.

CHOOSING 2K OR 4K REFRESH

There are several factors to consider when deciding which refresh standard is best for an application:

1. Addressing supported by your DRAM controller—11 row/11 column, 12 row/12 column, or both?
2. Frequency and length of page accesses
3. Average cycle rates

Some DRAM controllers have only 11 address drivers, so they are limited to 2K refresh. Many newer DRAM controllers, including some of the 3.3V controllers, are being designed to support both standards, so this limitation should be short-lived.

Your choice of 2K or 4K refresh will probably be based on the importance of power consumption versus page depth. A system requiring frequent page accesses may not benefit by sacrificing page depth in exchange for the power savings of a 4K refresh. In a portable system, the benefits of 20mA less current may easily override concerns about decreased page depth.

Additionally, the difference in power consumption decreases with longer cycle times. If the DRAMs spend much of their time idle, as in systems using SRAM caches, the power savings may be negligible. See Figure 2.

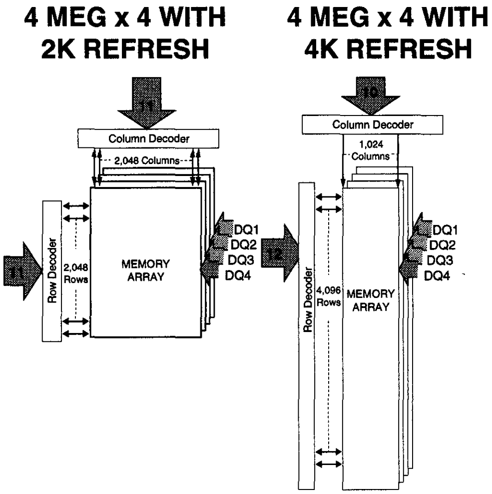


Figure 1

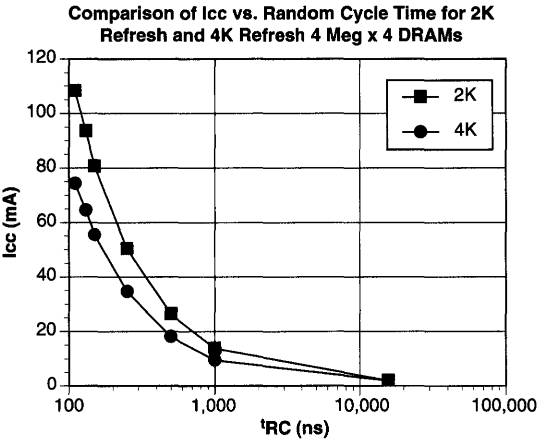


Figure 2

MODULES

Modules may use both 2K and 4K refresh depending on whether or not they have 12 address inputs. If a module uses parity, such as the 4 Meg x 9 or the 4 Meg x 36, it probably mixes 4 Meg x 4 and 4 Meg x 1 DRAMs on the same module. Because the 4 Meg x 1 DRAM requires symmetric addressing (11 row addresses and 11 column addresses), using a 4K refresh 4 Meg x 4 DRAM requires that the DRAM controller support both addressing decodes simultaneously. This is possible using "redundant addressing," whereby one of the address bits is duplicated as both a row address and as a column address. Most modules that have parity will simply use the 2K refresh 4 Meg x 4 DRAM in order to avoid changes to existing controllers. As shown in Figure 3, when a 4 Meg x 4 with 2K refresh is employed, the numbers of rows and columns match the 4 Meg x 1, allowing use of the 4 Meg x 1 for parity.

If the 4 Meg x 4 with 4K rows is implemented, redundant addressing must be employed, or use of the 4 Meg x 1 for parity becomes impossible because the number of rows and columns does not match. The shaded areas shown in Figure 4 are the portions of the DRAM that can't be used because of the difference in the number of rows and columns. Table 1 shows an example of redundant addressing. If bit 23 is set to equal bit 22, it can serve as both the 12th row address on the 16Mb and the 11th column address on the 4Mb.

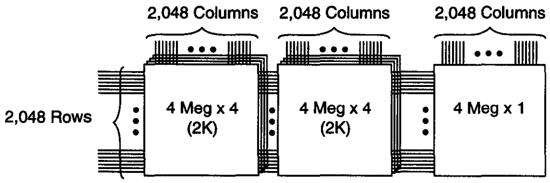


Figure 3

SUMMARY

1. JEDEC has approved two refresh standards at the 16Mb level, 2K and 4K.
2. 2K refresh is 2,048 cycles in 32ms; 4K refresh is 4,096 cycles in 64ms.
3. Devices with 4K refresh cut current consumption by 20mA under worst-case operating conditions.
4. Devices with 4K refresh have half the page depth of a 2K device.
5. Existing 5V standard modules generally will use the 2K refresh standard DRAM.

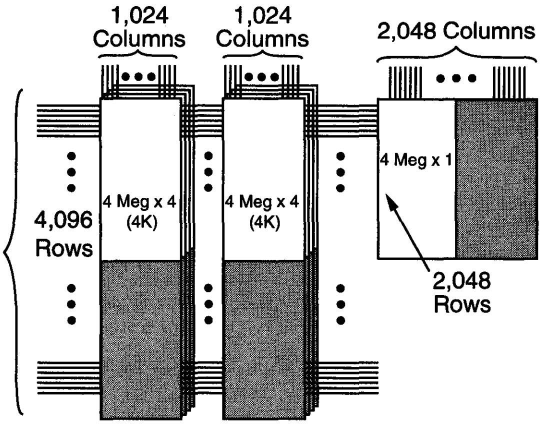


Figure 4

Table 1
ADDRESS MULTIPLEXING ASSIGNMENT FOR DRAM ROWS AND COLUMNS

DRAM Address		A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
Memory Controller Address	Column	1	2	3	4	5	6	7	8	9	20	23	
	Row	10	11	12	13	14	15	16	17	18	19	21	22

TECHNICAL NOTE

REDUCE DRAM CYCLE TIMES WITH EXTENDED DATA-OUT

his article was originally published in 1992. Micron no longer uggests using EDO/FPM memories for new design mplementation.

NTRODUCTION

As system speeds increase, DRAM manufacturers are leveloping methods to decrease the cycle times of RAMs. The most common version of DRAM is FAST AGE MODE (FPM), but the addition of a feature known s extended data-out (EDO) has become more common ecause it allows shorter page cycle times with only a ninor functional change from FPM. Because the device vith EDO doesn't turn off the output drivers when CAS# oes HIGH, it can have a shorter cycle time than FPM.

EDO ADVANTAGES

- The PAGE READ cycle time is shorter for EDO devices than for FPM devices.
  - The PAGE READ cycle time for a 70ns EDO device is the same as the cycle time for a 40/50ns FPM DRAM.
- Data is valid on the falling edge of CAS#, so that edge can be used to strobe data.
- Implementing EDO in place of FPM devices in a system can be as easy as knowing when the bus needs to be deactivated and using OE# or WE# instead of CAS# to accomplish it.

This article covers some basic differences between FPM and EDO during a PAGE READ cycle, compares cycle times between FPM and EDO, and offers a few examples under different address setup conditions. Also discussed is the slight timing difference between FPM and EDO when moving from a PAGE READ into a PAGE WRITE, as well as the issues involved when replacing an FPM device with an EDO device.

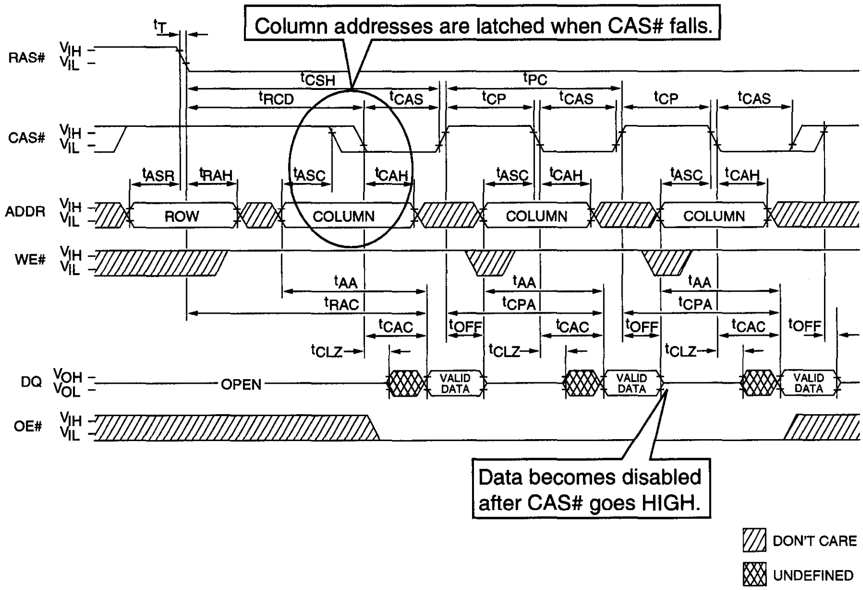


Figure 1
FPM READ CYCLE

BASIC DESCRIPTION

FPM and EDO allow fast data operations within a row. The differences are in the deactivation of data-out when CAS# goes HIGH and the operation of OE# and WE#. The following section highlights differences between the FPM and EDO when reading within a page.

FPM

Characteristics:

- The column address is latched when CAS# falls.
- The output drivers are turned off when CAS# goes HIGH.
- Minimum FPM READ cycle time is $^tPC = {}^tCPA + {}^tT$, $({}^tCPA = {}^tAA + {}^tT)$

The cycle begins with RAS# strobing in a row address, followed by CAS# strobing in a column address. To continue to access columns within that row, CAS# is toggled as addresses change.

Figure 1 shows a typical FPM READ cycle. The column address is latched into the part when CAS# falls, so column-address setup and hold times are referenced to the falling edge of CAS#. Notice ^tOFF; this specification tells you that CAS# going HIGH turns off the output drivers.

EDO

Characteristics:

- The column address is latched when CAS# falls.
- The output drivers are not turned off when CAS# goes HIGH.
- Minimum EDO READ cycle time is determined by the greater of the two equations below.

Equation 1: $^tPC = {}^tCAS + {}^tCP + 2{}^tT$
Equation 2: $^tPC = {}^tCPA - ({}^tCP + {}^tT)$

- OE# and CAS# work together to enable and disable the outputs.
- WE# can disable the outputs.

EDO allows fast access within a row and uses CAS# to latch the column address, as does FPM, but EDO does not turn off the output when CAS# goes HIGH. This last feature allows EDO to cycle faster than FPM because the user does not have to wait for valid data to appear before starting the next access. In other words, data can appear after CAS# has been pulled HIGH, and it will stay valid for 5ns after CAS# transitions LOW again (^tCOH), as shown in Figure 2. The output will deactivate when both RAS# and

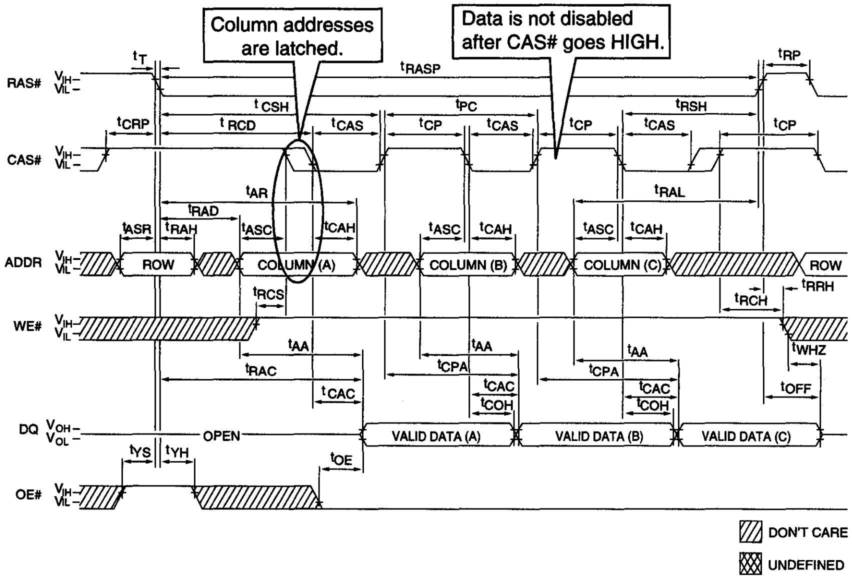
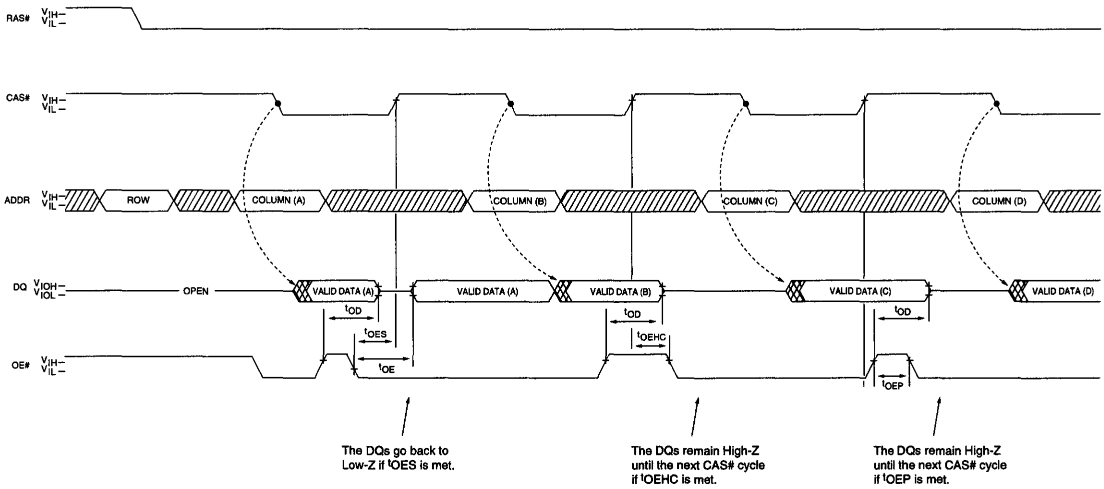


Figure 2
FPM READ WITH EDO

CAS# are HIGH, so ^{t}OFF will be referenced from the rising edge of RAS# or CAS#, whichever occurs last. OE# will also deactivate the outputs, as shown in Figure 3. In order to accommodate systems where OE# is tied LOW, WE# has the ability to turn off the output drivers as well (see Figure 4).

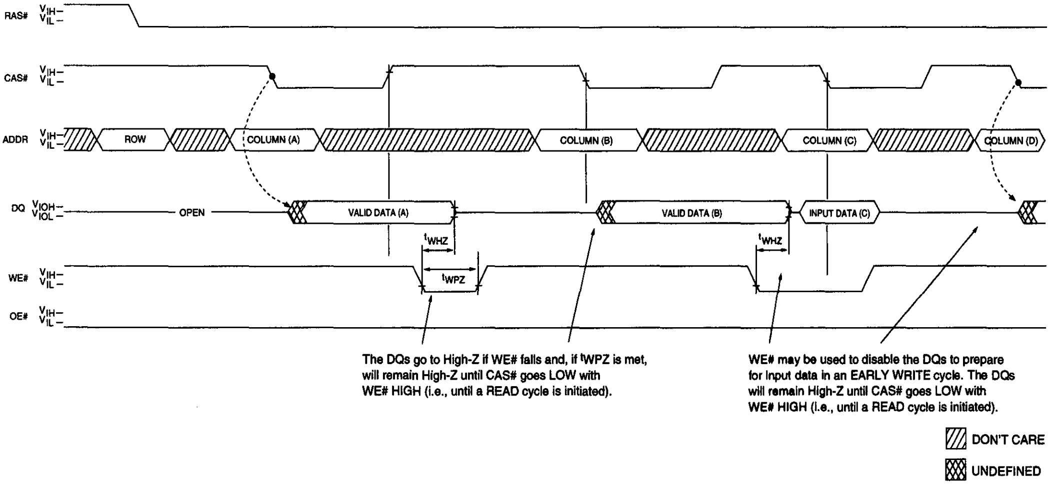


The DQs go back to Low-Z if ^{t}OES is met.

The DQs remain High-Z until the next CAS# cycle if ^{t}OEHC is met.

The DQs remain High-Z until the next CAS# cycle if ^{t}OEP is met.

Figure 3
OUTPUT ENABLE AND DISABLE USING OE#



The DQs go to High-Z if WE# falls and, if ^{t}WPZ is met, will remain High-Z until CAS# goes LOW with WE# HIGH (i.e., until a READ cycle is initiated).

WE# may be used to disable the DQs to prepare for input data in an EARLY WRITE cycle. The DQs will remain High-Z until CAS# goes LOW with WE# HIGH (i.e., until a READ cycle is initiated).

Figure 4
OUTPUT DISABLE USING WE#

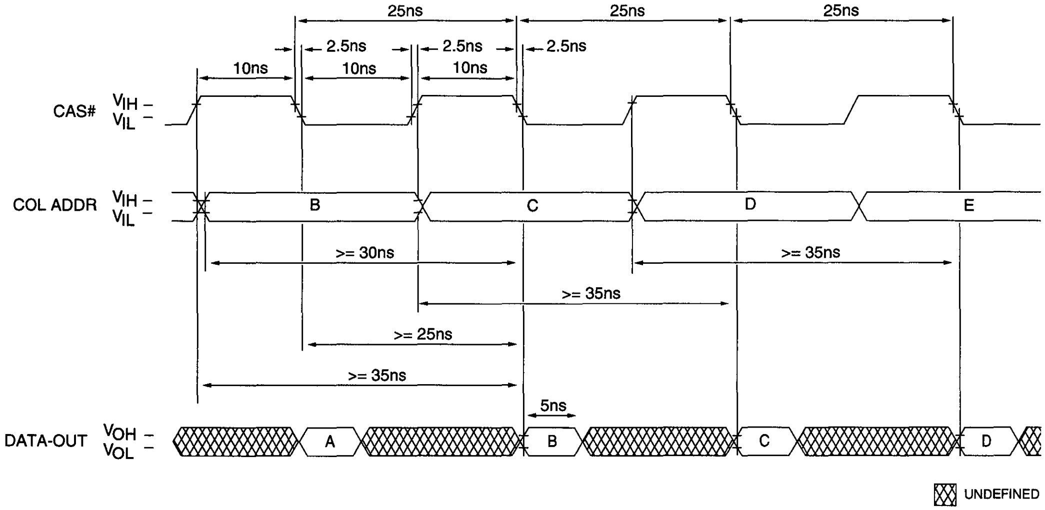


Figure 5
EDO MINIMUM FAST-PAGE-MODE READ CYCLE TIME AVAILABLE ON 60ns DRAMs

PAGE READ CYCLE TIMES

This section examines the different cycle times of FPM and EDO to see how they are generated. Figure 1 shows that CAS# must stay LOW until data-out becomes valid. (If CAS# goes HIGH before valid data, then the output buffers would turn off.) The longest access time specified for the device is from CAS# HIGH to data-out (^{t}CPA). CAS# can't go HIGH before ^{t}CPA, or data-out will not fire. Add a transition time to pull CAS# HIGH and you have the cycle time $^{t}PC_{FPM} = {}^{t}CPA + {}^{t}T$.

EDO works a bit differently. ^{t}CPA is still the longest access time but is no longer the limiting parameter in cycle time. This is because some of this access time includes CAS# precharge (CAS# HIGH time). With FPM, CAS# can't be brought HIGH before data is valid because CAS# HIGH turns data off. Since CAS# HIGH doesn't turn off data in the EDO device, you can bring CAS# HIGH before data is valid and begin precharging CAS# while you wait for data-out. This overlap of CAS# precharge and getting data out means ^{t}CPA is no longer the limiting parameter.

The theoretical minimum page mode cycle time is determined by one of the two equations below, whichever is greater (see Figure 2). ^{t}LH is the CAS# LOW-to-HIGH transition time, and the ^{t}HL is the CAS# HIGH-to-LOW transition time.

Equation 1: $^{t}PC = {}^{t}CAS + {}^{t}CP + {}^{t}LH + {}^{t}HL$
Equation 2: $^{t}PC = {}^{t}CPA - ({}^{t}CP + {}^{t}HL)$

The minimum cycle is achieved by providing valid column addresses early enough that ^{t}AA is not limiting. In the past, transition times were assumed to be 5ns each for the purpose of specifying cycle times. However, in many cases, the transitions between 0.8 and 2.4 volts do not require 5ns, so the EDO devices allow for 2ns transitions.

For example, a page mode cycle time of 25ns can be achieved using Micron 60ns EDO DRAMs with a ^{t}CPA of 35ns when transitions are 2.5ns or less (see Figure 5). This represents a 40 to 60 percent improvement over the same cycle times provided by 60ns devices with conventional FAST-PAGE-MODE operation. Similar improvements are provided on the 50ns and 70ns speed grades, which have theoretical minimum cycle times of 20ns and 30ns, respectively.

XAMPLES: EDO AND FPM

The table below compares page READ cycles of FPM and DO under two different conditions: minimum column-ddress setup and maximum column-address setup time. he timing diagrams for the following examples assume at RAS# is already LOW, WE# is HIGH and OE# is LOW. 70ns DRAM is used with the following timing:

DESCRIPTION	FPM	EDO
^{t}PC (MIN)	45	30
^{t}CAS (MIN)	20	12
^{t}CLZ (MIN)	0	0
^{t}OFF	0-20	0-20
^{t}T	5	5

Figures 6 and 7 show FPM and EDO cycles with plenty of address setup time. On an FPM device with plenty of address setup time, we can operate at ^{t}PC = 45ns (the minimum allowed) and data is valid for 5ns.

EDO under the same address setup time looks different (see Figure 5). Now the minimum cycle time is 32ns. Notice that data doesn't appear on the bus until you are already into the second access (8ns of CAS# precharge for the next cycle is already completed when data appears). This is the overlap that allows the shorter cycle time. ^{t}PC is 32ns and data is valid for 12ns.

Under these conditions, EDO cuts the cycle time over an FPM device by 29 percent or increases burst rate by 41 percent (22 MHz to 31 MHz). In addition, even with the shorter cycle time, data-out is valid for 12ns on the EDO, as

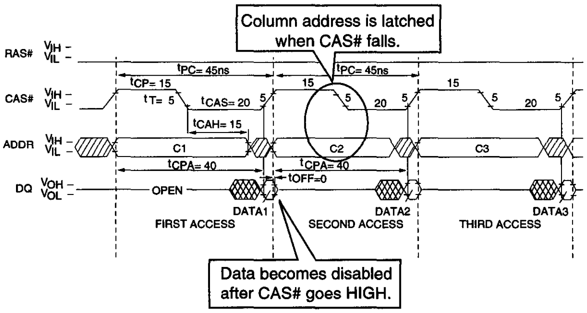


Figure 6
FPM PAGE READ CYCLE WITH MAXIMUM ADDRESS SETUP
^{t}PC = 45ns; DATA VALID FOR 5ns

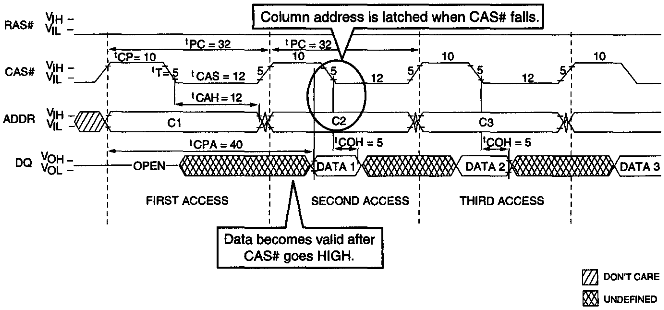


Figure 7
EDO PAGE READ CYCLE WITH MAXIMUM ADDRESS SETUP
^{t}PC = 32ns; DATA VALID FOR 12ns

opposed to only 5ns on the FPM device. We could get more performance by using shorter transition times on the EDO device; we used 5ns to make the comparison between FPM and EDO easy to understand.

Figures 8 and 9 show FPM and EDO cycles with minimum address setup time. In this case, the address becomes valid coincident with CAS# falling. For FPM, data won't be valid for ${}^tAA$ (35ns), so CAS# must be held LOW until that time (see Figure 8). Since the minimum CAS# HIGH time is 10ns, the cycle time is 50ns (${}^tAA + {}^tCP + {}^tT$). Data-out is valid for 5ns.

Looking at EDO under the same conditions (Figure 9), i still takes ${}^tAA$ (35ns) after the addresses are valid to ge valid data-out, but there is no wait before pulling CAS# HIGH. Notice that CAS# has been pulled HIGH an precharge has been completed for the next cycle before DATA 1 appears on the bus. Just before data becomes valid CAS# drops and the second address is latched. Again, there is an overlap of starting one cycle and finishing the other Now ${}^tPC$ = 32ns and data-out is valid for 7ns.

In this case, EDO cycle time is 36 percent less than the FPM cycle time (providing a 55 percent improvement i burst rate); EDO data is valid 2ns longer.

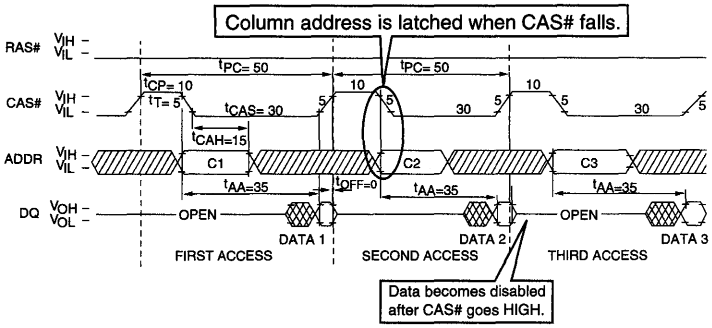


Figure 8
FPM PAGE READ CYCLE WITH MINIMUM ADDRESS SETUP
${}^tPC$ = 50ns; DATA VALID FOR 5ns

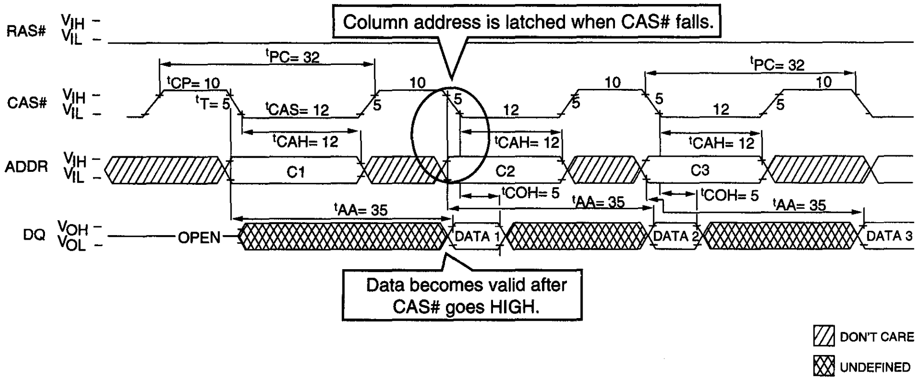


Figure 9
EDO PAGE READ CYCLE WITH MINIMUM ADDRESS SETUP
${}^tPC$ = 32ns; DATA VALID FOR 7ns

These examples illustrate another big advantage of EDO. Not only can you operate at shorter cycle times, but data is available longer for the system to sample. Since data is guaranteed to be valid as CAS# falls, that edge may be used to sample data.

70ns EDO INSTEAD OF 40/50ns DRAMs

EDO can provide the FPM READ speed of a 40/50ns DRAM. Even though a 40/50ns DRAM has a 40/50ns RAC, the FPM READ cycle time is 30-35ns, which is the same PAGE READ cycle time as that of a 70ns EDO device.

EASY TO IMPLEMENT

An additional benefit of EDO is the ease of implementation. PAGE READ or WRITE cycle time is cut, but the major difference between FPM and EDO is that the FPM device will stop driving data-out when CAS# goes HIGH, and the EDO device must have the correct combination of RAS#, CAS#, OE# and WE# to deactivate the output. This means that any time the designer is counting on CAS# by itself to turn off the output drivers, bus contention may occur if something else tries to drive the bus. This may occur in the following situations:

- Page interleave memory banks;
- Moving from PAGE READ directly into a PAGE WRITE (within the same page);
- Whenever anything other than the DRAM is driving the bus, and OE# and RAS# are LOW while CAS# is HIGH.

(This last case is uncommon and should not mandate a change for most systems.) Interleaved memory need only make use of OE# or WE# instead of CAS# when turning off the output drivers; then EDO can be used in place of FPM DRAMs.

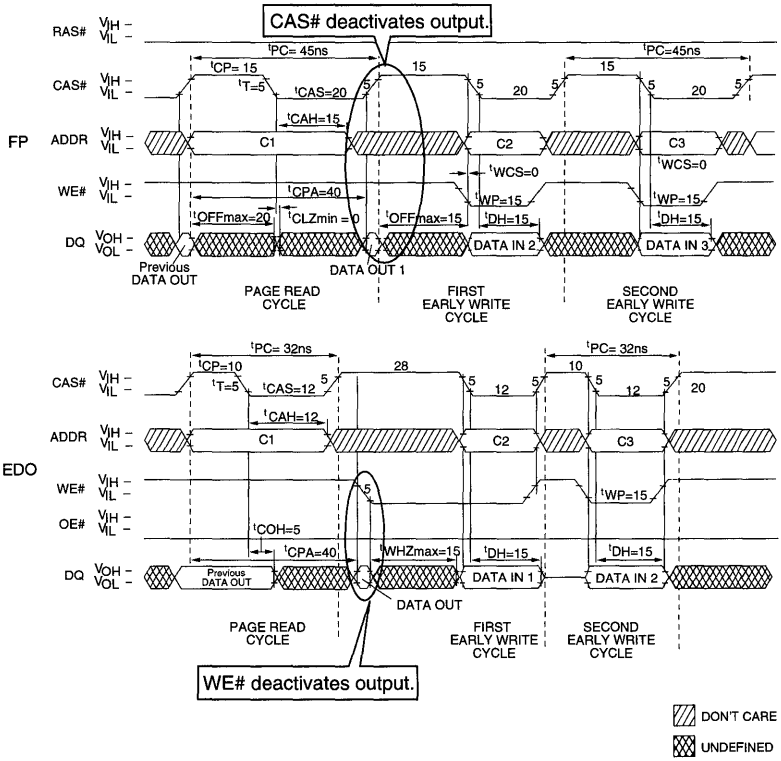


Figure 10
EXAMPLE FPM AND EDO READ TO WRITE CYCLES
^{t}PC = 45ns

READ TO WRITE CYCLES

Since CAS# doesn't turn off the output devices on an EDO device, caution should be used when turning the bus around on a shared I/O device. To demonstrate the difference, Figure 8 shows the transition from a PAGE READ to a PAGE EARLY WRITE on the same page. When using the FPM version, OE# can be tied LOW and CAS# can be used to deactivate the output. Notice that OE# is also tied low on the EDO device, and this cycle is still possible.

SUMMARY

EDO is simply a modified FPM cycle and can be used in systems to increase performance. It allows system designers to improve their cycle times and system performance since data is present for a much longer time, even during short cycle times. Because each generation device has different timing limitations, be sure to consult the data sheet for exact timing.

TECHNICAL NOTE

DRAM SOFT ERROR RATE CALCULATIONS

This article was originally published in 1994.

INTRODUCTION

Micron Technical Note TN-04-32, "Reduce DRAM Memory Cost With Cache," presents a discussion on the use of parity. This technical note may have led some readers to conclude that parity is no longer of value. Although this conclusion is understandable (see Figure 1), the fact is that the need for parity can be determined only after design goals have been thoroughly analyzed.

Herein lies the problem: how to get from point A (DRAM manufacturer's reported soft error rate [SER]) to point B (system mean time between failures [MTBF]). This article's purpose is to solve the problem by showing how to take SER data reported by the manufacturer and determine a system's memory susceptibility to DRAM soft errors.

The SER data for the Micron 4Mb DRAM, as reported in the Micron *16 Meg SDRAM Reliability Monitor* (dated 8/97), will be used throughout this article for illustrative purposes.

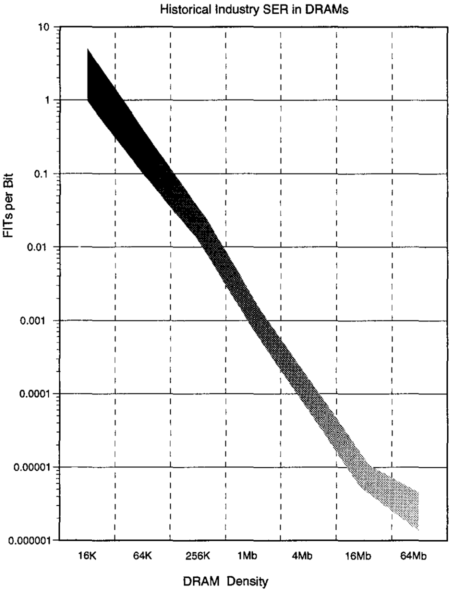


Figure 1
HISTORICAL DRAM SER

DRAM SER RATES

DRAM SER is a measurement of a DRAM's susceptibility to a nonrecurrent, single-bit output error. Although there is not a defined industry standard for measuring a component's SER, Micron has adopted a widely accepted methodology:

- Accelerated SER testing using an alpha radiation source.
- Real-time, system-level SER testing. Micron uses its AMBYX™ intelligent burn-in and test system.

The accelerated test data provides the only practical, real time means to determine the relative increase or decrease in the component's SER for various test conditions.

Micron records a DRAM's real time SER when the device is operating at a 3.3V Vcc with 15.625µs cycle rate (refresh rate). Micron's *16 Meg SDRAM Reliability Monitor* lists an SER of 97 FITs at a 90 percent confidence level. A FIT is a failure in time (1 billion device hours).

SER CALCULATIONS—REFRESH MODE

To begin, let's examine a memory buffer using only one 16Mb SDRAM (2 Meg x 8) at a 15µs refresh rate. The system's MTBF-due-to-soft-error rate is the DRAM's SER rate, 97 FITs. Mean time between failures is calculated by dividing one billion device hours by 97 FITs, which equals one error every 10,309,175 system hours, or 1,207 years.

Now, let's take the previous example and add seven additional 16Mb SDRAMs for a 32-bit-wide memory array (8MB). Since there are four components, the SER rate is increased by the same ratio in order to obtain a system hourly rating. The system's memory MTBF-due-to-soft-error rate is now one billion device hours divided by four devices (97 FITs per device), equaling one error every 2,577,294 system hours, or 302 years.

Seven, rather than three, additional 16Mb SDRAMs provide a 64-bit-wide memory array (16MB). In this case, the system's MTBF-due-to-soft-error rate is one billion device hours divided by eight devices (97 FITs per device), equaling one error every 1,288,646 system hours, or 151 years.

The previous calculations assume a single-bank architecture. If any of the above examples had two banks, then the SER would be twice as high and the MTBF would be half of the single-bank value. For example, a dual-bank, 64-bit-wide (16MB) memory system's MTBF-due-to-soft-error rate is one billion device hours divided by 16 devices (97 FITs per device), equaling one error every 644,323 system hours, or 75 years. Of course, this is continuous use.

SER CALCULATION—ACTIVE MODE

DRAM memory is not always in refresh mode. Rather, it is active (accessing data via READs and WRITEs) during a portion of its ON time. It is necessary to determine the memory's overall SER, or "operating SER," before determining a system's MTBF-due-to-soft-error rate during DRAM access.

First, the percentage of time the DRAMs are active and in refresh must be determined. The next step is to determine the refresh SER rate. As performed in the previous 64-bit, single-bank example using eight 16Mb SDRAMs, the refresh SER rate based on eight devices (97 FITs per device) is 776 FITs.

The active SER rate must now to be determined. This is where acceleration curves are required. Micron provides three types in the *16 Meg SDRAM Reliability Monitor:* checkerboard pattern, solid ones pattern and solid zeros pattern. The graph that provides the worst-case slope, typically the checkerboard pattern, is usually selected.

Referring to the checkerboard pattern curve from the Micron *16 Meg SDRAM Reliability Monitor* (Figure 2), let's assume the DRAMs are being cycled at a 200ns (0.2µs) cycle rate. The alpha hits at 15µs are selected from the checkerboard pattern curve—0.2 hits. The alpha hits at 200ns are then selected from the same curve—10 hits. Taking 10 hits and dividing by 0.2 hits gives a ratio of 50. Thus, the SER can be expected to increase by a factor of 50 times when operating at 200ns, as compared to refreshing at 15µs. By taking the real-time SER at 15µs and using the ratio from the acceleration curves just acquired, the SER at 200ns can be determined at 776 FITs times 50, which equals 38,800 FITs.

MTBF DUE TO SOFT ERRORS

Now, let's assume the 64-bit, single-bank DRAM memory array is active 15 percent of the time and is in refresh the remaining 85 percent of the time. The operating SER rate is now obtainable—15 percent of 38,800 FITs plus 85 percent of 776 FITs yields a FIT rate of 6,480 FITs. The system's memory MTBF for soft errors is obtained by dividing one billion device hours by 6,480 FITs for an MTBF of 154,330 system hours, or 18 years of continuous use.

For a dual-bank memory non-interleaved array, the operating SER rate would not be twice the single bank amount, as was the case with the refresh SER rate. This is because only one bank at a time is actively being written or read. The other bank(s) are in standby (refresh only). For example, let's determine the operating SER and MTBF for the 64-bit, dual-bank memory array. The operating SER rate is 6,480 FITs (active bank from previous example), plus 776 FITs (additional bank in standby), which equals 7,256 FITs. The system's memory MTBF for soft errors is 137,817 system hours, or 16 years of continuous use.

SYSTEM-INDUCED SOFT ERRORS

So far, this discussion has focused on DRAM-related soft errors (i.e., alpha particle induced). System-induced soft-error calculations are beyond the scope of this article but warrant some discussion.

System-induced soft errors are those not generated by the DRAM memory itself. They are most commonly due to noise sources such as undershoot/overshoot, as well as timing issues due to hardware and/or software problems. System-induced soft errors are usually overlooked because they have been negligible contributors on a well-designed, clean system. Improvements made in DRAM SER by quality DRAM manufacturers, as well as faster operating speeds and board design requirements, have shifted the primary cause of soft errors to the system design itself.

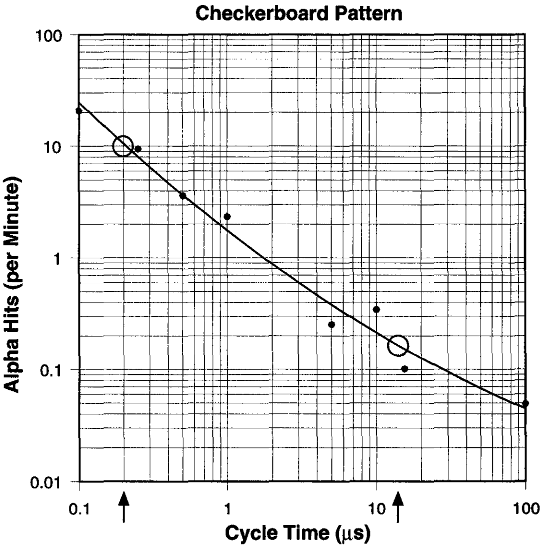


Figure 2
CHECKERBOARD PATTERN

Conventional parity-based systems check for soft errors stemming from the data, both alpha particles (DRAM) and data I/O bus noise (system). However, there are other sources of system-induced soft errors that are overlooked because they cannot be detected with conventional parity. For example, noise on the address bus can result in the wrong data being written to, or read from, the DRAM. The data itself will be unaffected by the address bus noise, but the wrong location is accessed. Even though these types of system soft errors are not checked for, they are just as harmful as data-I/O induced soft errors.

Parity checking can be useful in the prototype stage by helping to identify initial design problems. Such parity checking can include DRAM, address bus and data bus parity checking. There are strong arguments for eliminating DRAM parity memory and providing parity checking on the address and data bus only. In either case, the DRAM parity memory and bus parity checking circuits could be eliminated once the system's design has been qualified to meet overall system soft-error requirements.

Even if a DRAM memory's alpha-particle-induced soft-error rate is at an acceptable level, some sort of parity checking may be desired. Bus-parity checking circuits could remain in the system at a lower cost and provide a greater safeguard against soft errors than that obtainable with DRAM parity memory.

Many of today's systems are designed to offer upgradability from the low-end to high-end of the performance spectrum. For these systems, where the low-end version does not require DRAM parity memory but the high-end upgrade does, designing in flexibility to allow either choice is advantageous.

SUMMARY

In determining the parity requirements for a given memory system, the memory designer cannot assume parity is or is not required. Rather, the memory designer must analyze the system's reliability requirements and determine what soft error rate is expected and what MTBF for soft errors the system can tolerate.

The memory designer must "engineer" the SER numbers to his specific conditions to obtain numbers relevant to the design itself. Following the procedures outlined in this technical note will allow any memory system designer to determine expected memory MTBF-due-to-soft-error rates.

It should be noted that measured and accelerated SER data provides a "ballpark" number for general expectations. In the last example—a 64-bit, dual-bank memory array using 16Mb SDRAMs—the memory system was shown to experience one soft error every 16 years of continuous use.

If a system required an MTBF of at least 15 years per soft error, the system using 16Mb SDRAMs would suffice technically. But since the expected MTBF is a typical expectation and not an absolute minimum, the number should be guard-banded. There is no industry rule for what guard band to use, but a memory designer should feel safe in using a 25 percent guard band. For the foregoing example, any system specifying an MTBF of 12 years or less should not jeopardize its reliability to DRAM-related soft errors by eliminating parity memory.

TECHNICAL NOTE

MAXIMIZING EDO ADVANTAGES AT THE SYSTEM LEVEL

his article was originally published in 1994. Micron no longer ıggests using EDO/FPM memories for new design ıplementation.

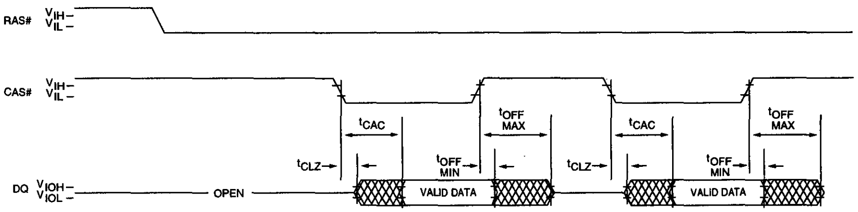
NTRODUCTION

Extended data-out (EDO) DRAMs, while representing nly a slight modification to conventional FAST PAGE IODE (FPM) components, can provide substantial advanıges at the system level. The primary benefit is that EDO llows for a shorter PAGE MODE cycle time (or faster data ıte) while accessing data within a single page in memory. ther advantages include relaxed system timing constraints nd, in some cases, less total overhead during page acesses. In general, the design complexity for an EDO-based ystem will be less than that for a system based on FPM omponents, and much less than that for systems based on evolutionary DRAM technologies now being introduced.

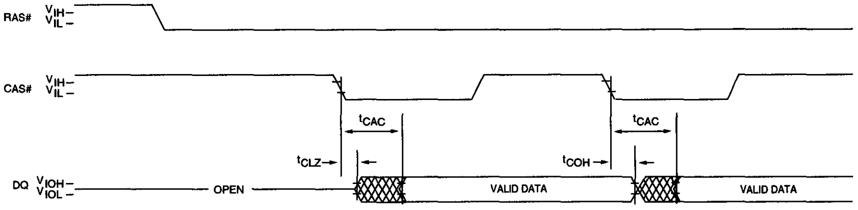
This article reviews the physical differences between DO and FPM components and then describes the timing implications of those differences. This discussion is then extended to cover the increase in performance and other advantages at the system level; examples using typical system timing are shown. Finally, additional system design implications are discussed.

EDO vs. FPM—COMPONENT LEVEL DIFFERENCES

Simply stated, EDO means that data is not disabled when CAS# goes HIGH during a PAGE-MODE READ access. Instead, data remains available until such time that data from the subsequent access begins to appear. This is indicated by the presence of a ^{t}COH specification and the lack of a ^{t}OFF specification when compared to conventional FPM (as shown in Figure 1). Other changes include related modifications to RAS#, OE# and WE# functionality, to provide for the disabling of data when necessary and when no longer accomplished by CAS# alone. This related operation is further detailed in subsequent sections of this article.



(a) Conventional FPM



(b) EDO

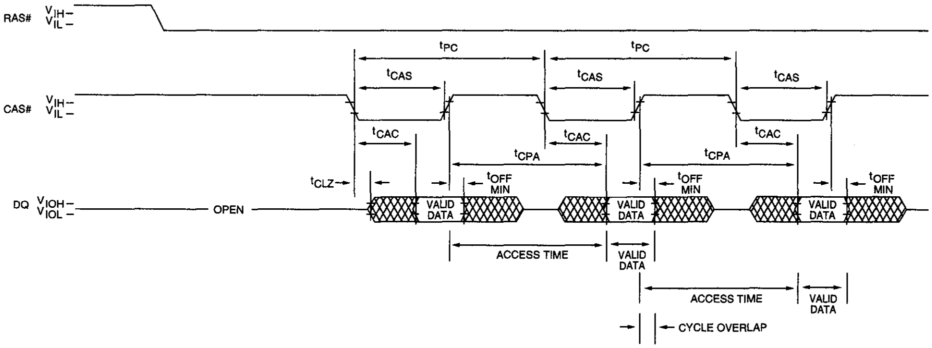
▨ UNDEFINED

Figure 1
PHYSICAL DIFFERENCE BETWEEN FPM AND EDO

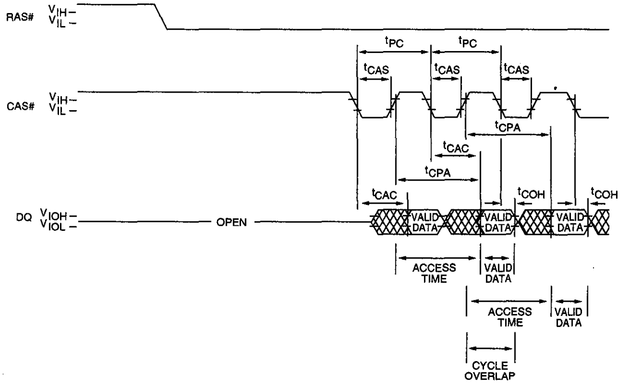
TIMING IMPLICATIONS

The real advantage of EDO is not necessarily that data can remain valid once CAS# goes HIGH, as shown in Figure 1, but that CAS# is allowed to go HIGH prior to valid data appearing on the outputs (this is shown, again compared to conventional FPM, in Figure 2). For FPM devices, the CAS# pulse width (^{t}CAS) is specified to be equal to ^{t}CAC since anything shorter would disable data before it became valid. In fact, ^{t}CAS typically must be longer than ^{t}CAC in the system because many DRAM vendors specify a minimum ^{t}OFF of 0ns. With EDO devices, ^{t}CAS is no longer limited by ^{t}CAC or the data valid time required by the system and is therefore typically specified at 10ns for the -6 speed grade.

The shorter ^{t}CAS specification associated with EDO allows the CAS# or PAGE MODE cycle time to be tightened As shown in Figure 2, EDO allows for a portion of the acces time in one cycle to overlap a part of the access time, as wel as all of the data valid time, for the previous cycle. I contrast, the only such overlap in a FPM access is th portion, if any, of the data valid time which is provided b a nonzero ^{t}OFF (MIN) specification. Specific system timin will determine the extent of the overlap that can be achieved but the following theoretical example will illustrate th point.



(a) Conventional FPM



(b) EDO

▨ UNDEFINED

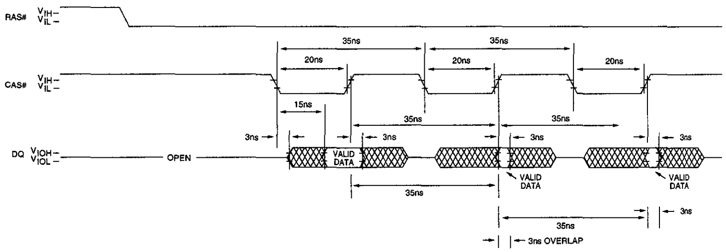
Figure 2
TIMING IMPLICATIONS OF EDO

Table 1
RELEVANT SPECIFICATIONS FOR MICRON 256K x 16 DRAMs

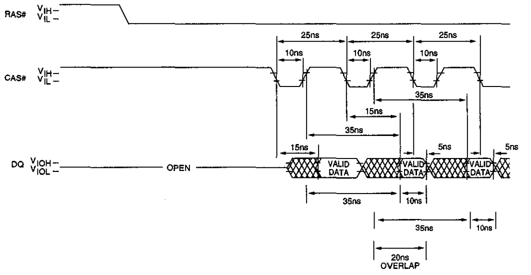
Parameter		MT4C16257 (FPM) (ns)	MT4C16270 (EDO) (ns)
^{t}CAC	MAX	15	15
^{t}CPA	MAX	35	35
^{t}AA	MAX	30	30
^{t}CP	MIN	10	10
^{t}OFF	MIN	3	3
^{t}CAS	MIN	15	10
^{t}CLZ	MIN	3	3
^{t}COH	MIN	–	5
^{t}PC	MIN	35	25
^{t}CSH	MIN	60	40
^{t}RSH	MIN	15	10
^{t}RAL	MIN	30	22
^{t}ASC	MIN	0	0
^{t}CAH	MIN	10	10
^{t}RP	MIN	40	35
^{t}DS	MIN	0	0
^{t}DH	MIN	10	10

For now, let's ignore propagation delays from the system clock, system clock resolution, address timing and signal transition times. Let's assume that we have a -6 FPM version and a -6 EDO version of an otherwise identical device. For illustration, the timing for Micron's 256K x 16 DRAMs will be used (see Table 1.) This timing will be used in all of the examples that follow.

The PAGE MODE cycle timing for the two devices is shown in Figure 3. The difference between the FPM cycle time (35ns) and the EDO cycle time (25ns) can be accounted for by noting that the FPM cycle can be computed as 35ns of access time (^{t}CPA), plus 3ns of data valid time, minus the 3ns of data valid time that overlaps the next access. The EDO cycle can be computed as 35ns of access time plus 10ns of data valid time, minus 20ns of overlap with the next access. Note in this case that in addition to a shorter cycle, the EDO device also provides a longer data valid window, thereby simplifying system design.



(a) Conventional FPM



(b) EDO

▨ UNDEFINED

Figure 3
EDO vs. FPM MINIMUM CYCLE TIMES

The overlapping of accesses described above leads to a pipelined effect in page mode read accesses, as shown in Figure 4. Ideally, data from one access is latched by the controller at the same time the controller fires CAS# for the next access. A page mode write access does not benefit fror EDO but can be executed with the same minimum cycl times as shown in Figure 5.

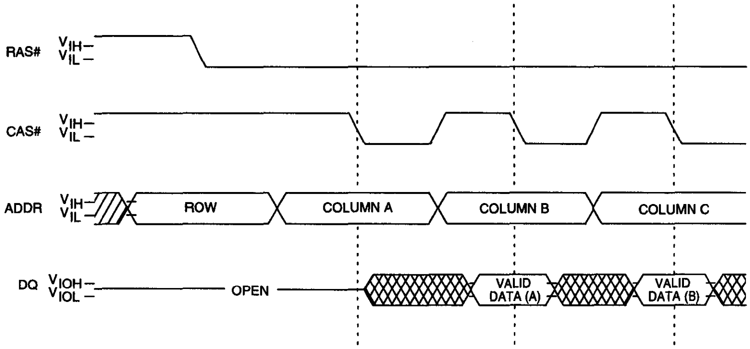


Figure 4
PIPELINED EFFECT IN EDO-PAGE-MODE READs

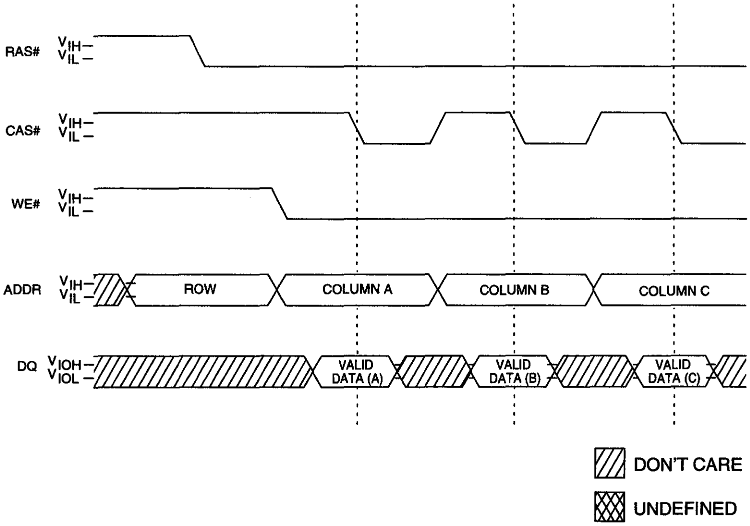


Figure 5
EDO-PAGE-MODE WRITEs

SYSTEM PERFORMANCE INCREASE FROM EDO

To examine the system performance advantage provided by EDO and factor system clock resolution into the discussion, a noninterleaved design based on a 66 MHz system clock driven by the positive clock edges only will be considered. Figures 6 and 7 show, respectively, the FPM and EDO-PAGE-MODE READ cycle timing resulting from the 15ns clock resolution (bursts of three locations were used strictly for the convenience of graphic illustration). Note that while a 30ns cycle time can be achieved with EDO, only a 45ns cycle can be achieved with FPM. Converting the cycle times to peak burst rates results in 33 MHz for EDO and 22 MHz for FPM. In this case, EDO provides a 50 percent improve-

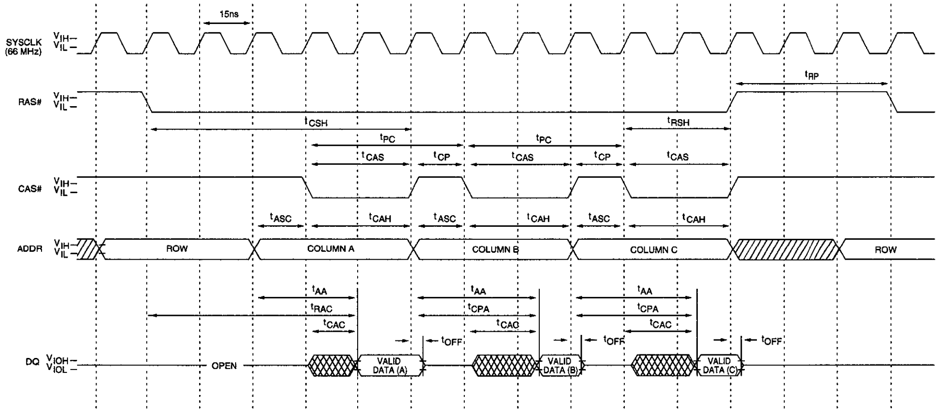


Figure 6
FPM READ CYCLE – 66 MHz SYSTEM CLOCK

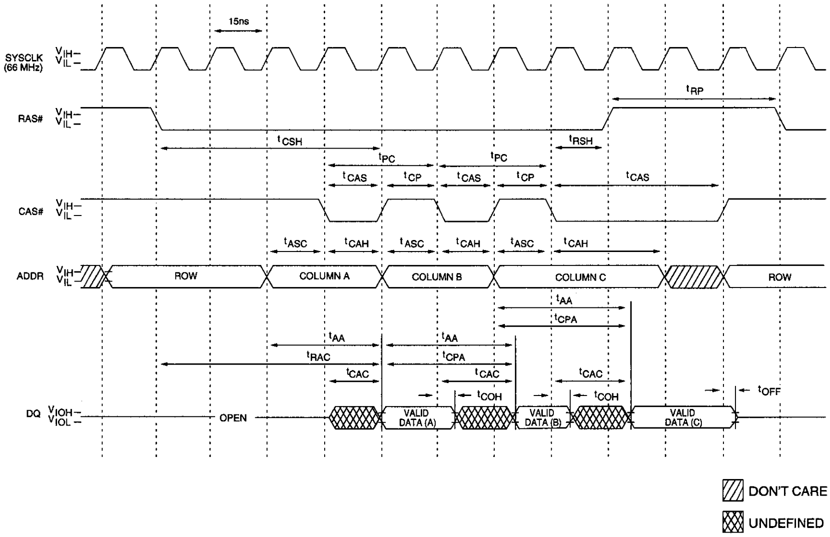


Figure 7
EDO READ CYCLE – 66 MHz SYSTEM CLOCK

ment in peak burst rate in the system. For reference, Figures 8 and 9 show the corresponding PAGE-MODE WRITE cycle timing. Figure 9 shows that although the WRITE cycles do not benefit from the EDO behavior itself, they can still match the cycle times for the EDO READs.

Also shown in Figure 7 is the fact that, unlike operation within a page access, once the page access is terminated by RAS# going HIGH, CAS# going HIGH will disable data. This results in the ability to hide some row precharge time, as discussed below.

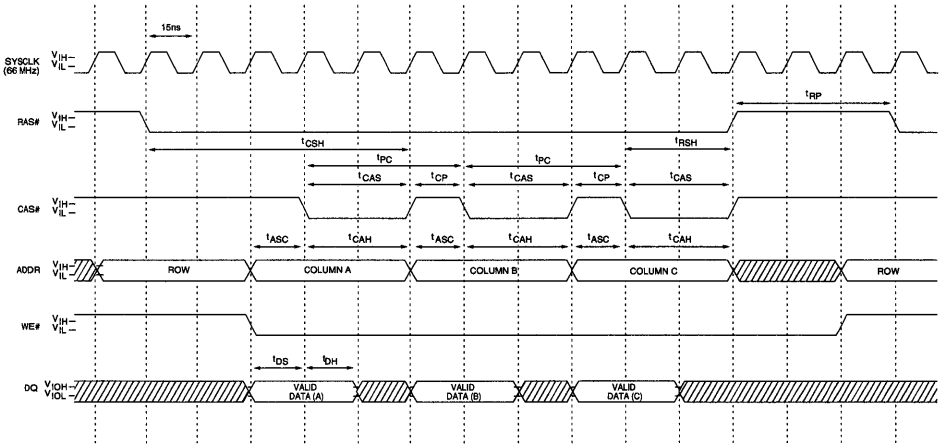


Figure 8
FPM WRITE CYCLE – 66 MHz SYSTEM CLOCK

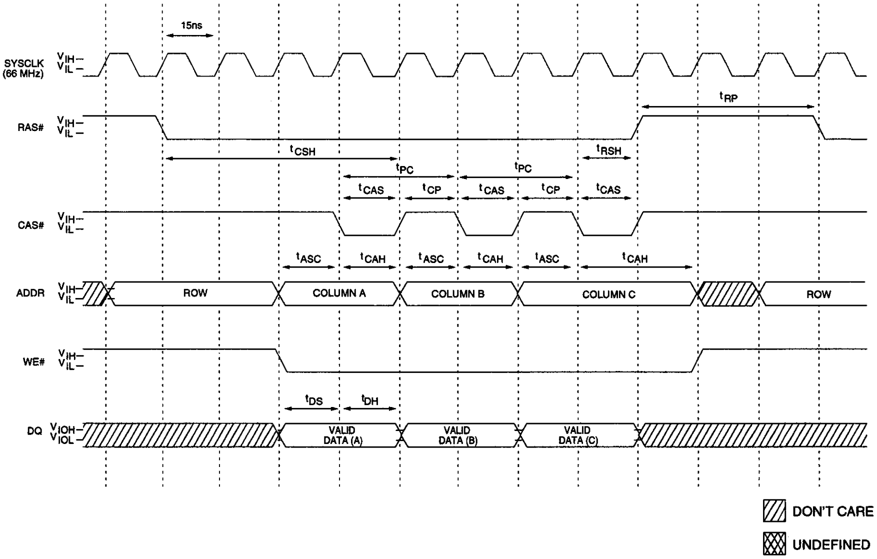


Figure 9
EDO WRITE CYCLE – 66 MHz SYSTEM CLOCK

Table 2
POPULAR SYSTEM CLOCK RATES AND RESULTING PAGE MODE CYCLE TIMES

SYSTEM CLOCK		PAGE MODE CYCLE TIME	
Frequency (MHz)	**Period (ns)**	**FPM (ns)**	**EDO (ns)**
50	20.0	40	40
60	16.7	50	33
66	15.0	45	30
80	12.5	50	25

Table 2 lists popular system clock rates along with the corresponding FPM and EDO-PAGE-MODE cycle times that would result from system clock resolution alone. Not only does EDO provide a faster peak data rate in almost every case, but an increase in system clock rate is much more likely to result in a corresponding faster peak burst rate (shorter PAGE MODE cycle time) when EDO devices are used. This continuous increase will extend to 90 and 100 MHz systems with the introduction in the near future of EDO parts which provide PAGE MODE cycle times down to 20ns.

Also related to system performance is the fact that the use of EDO typically results in the same total page mode overhead (row access time plus row precharge time) as with FPM. This is possible because ^{t}CSH, like ^{t}CAS, is not physically limiting on the devices as specified for FPM and would therefore be an artificial limiter if carried over directly from FPM and applied to EDO devices. Instead, Micron is adjusting the ^{t}CSH specification on EDO devices to allow for the first CAS# pulse to go HIGH earlier in the page access, and it is expected that other vendors will make this adjustment as well. This specification will typically be 40ns for -6 and -7 speed grades. Another parameter which would be a limiter if carried over is ^{t}RSH. This parameter will also be respecified for EDO; ideally, it would be set equal to the EDO ^{t}CAS specification. There are also several other parameters, many device- or vendor-specific, that will be adjusted to accommodate EDO designs.

Figures 7 and 9 reflect the adjusted ^{t}CSH and ^{t}RSH specifications, and the result is that the page mode overhead for the EDO devices is equal to that for the FPM devices. This is seen by noting that the total number of clock cycles for the page access for the FPM devices is 14. Three locations of data require three clocks each, for a total of nine, leaving five as overhead. For the EDO, 11 total cycles are needed, six of which are required for data, again leaving five as overhead.

SYSTEM ADVANTAGES OF EDO

After reviewing the theoretical FPM and EDO-PAGE-MODE cycle times listed in Table 2, the next logical question is, can those cycle times actually be achieved in a real system, and with how much effort? The answer is that achieving these cycle times with EDO devices will require equal or less design complexity than that required with FPM devices. The biggest problem in designing with FPM devices, once the propagation delays from the system clock are taken into consideration, has been trying to align the read data valid window around a system clock edge that can be used to latch that data into the memory controller.

A 50 MHz system clock and the device timing mentioned earlier will be used to illustrate this point. Typical propagation delays that might be found in a graphics subsystem with a controller implemented in an ASIC will also be used. These include a clock-to-Q delay for the controller plus routing delays, together totaling 12ns, and routing delays plus setup time back to the controller, together equaling 7ns.

In Figure 10, the FPM case, the data valid window for the controller starts 3ns before and ends 5ns after a negative system clock edge, which also means that the window ends 5ns prior to the next positive system clock edge. The choices here are to work with a skewed and/or inverted internal clock or with internal data delays to extend hold time to beyond the positive edge, or use an alternate external signal as a clock to the data input latch on the controller. Either way, these multiple/skewed clocks add design complexity.

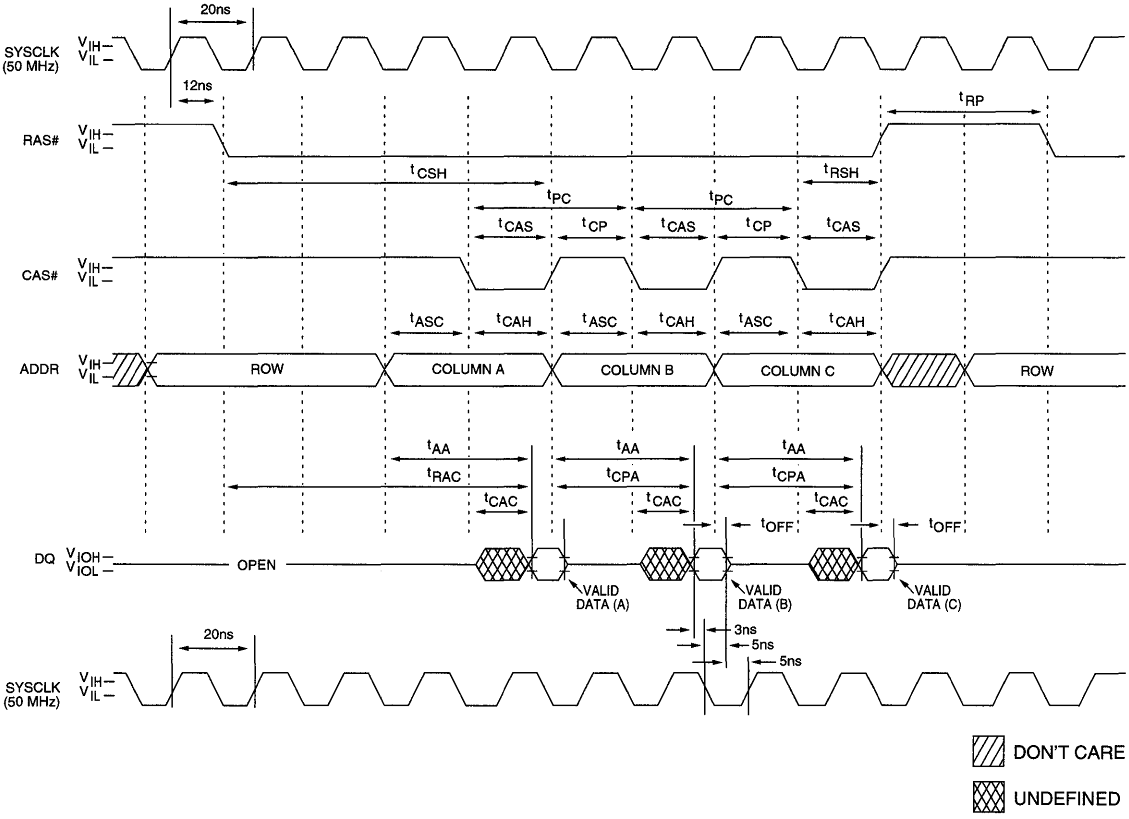


Figure 10
FPM READ CYCLE WITH PROPAGATION DELAYS – 50 MHz SYSTEM CLOCK

In contrast, when EDO devices are used with the same system timing, the data valid window begins at the same point but extends until ᵗCOH (5ns) after the next CAS# falling edge, shown in Figure 11. This total window is equal to 30ns or 1.5 system clock cycles; therefore, data can easily be latched in by an existing positive edge of the system clock with no additional design complexity.

Note that the page mode overhead for this example also happens to be less for EDO than for FPM. Since both methods use the same number of system clock cycles for each column (data) access, this overhead savings is seen by noting that the total number of clocks required for the page access is ten in the FPM case and nine in the EDO case.

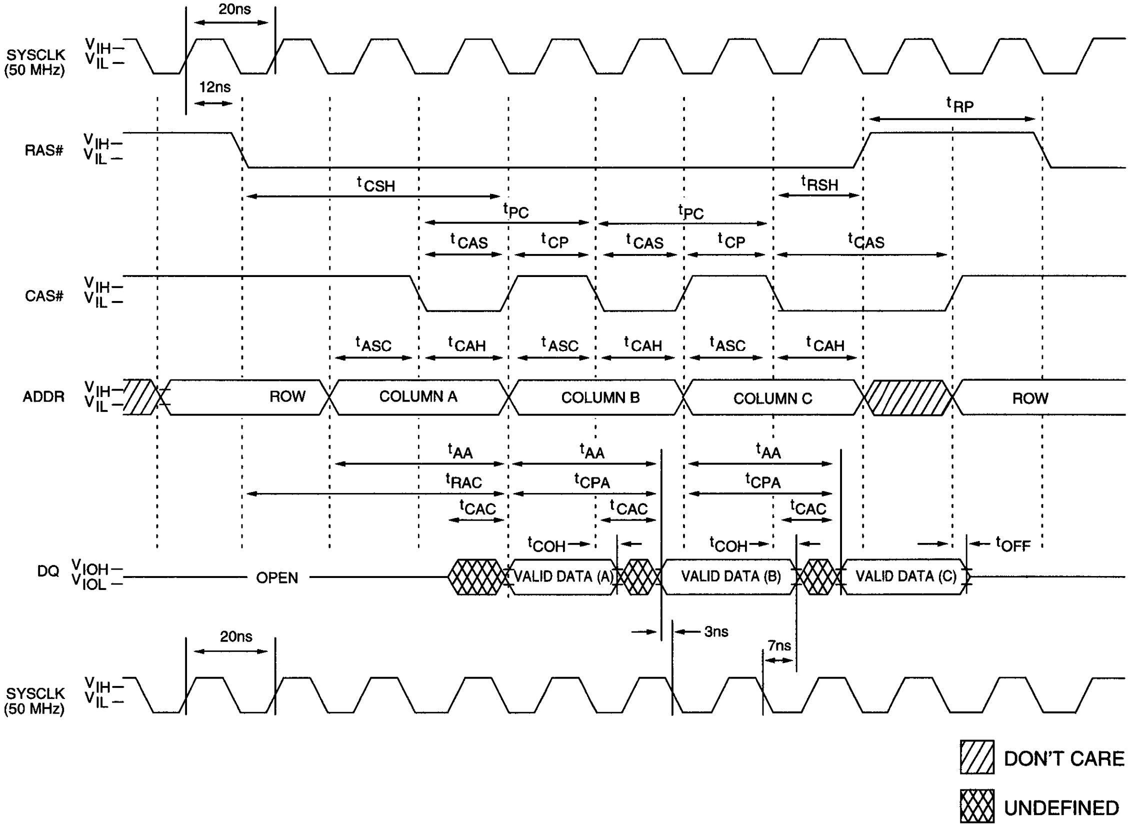


Figure 11
EDO READ CYCLE WITH PROPAGATION DELAYS – 50 MHz SYSTEM CLOCK

Now that we've shown that EDO can be substantially faster than FPM, and that at a given speed, an EDO-based system can be implemented with equal or less design complexity, the next question is, can an EDO-based system be designed to be faster with equal or less design complexity? The answer, again, is "yes." To see this, let's revisit the 66 MHz example (where EDO was previously shown to provide a 50 percent improvement in peak memory bandwidth), but now typical system propagation delays will be included. A system clock-to-Q plus trace delay of 9ns and a delay and setup time back to the controller of 5ns will be used. The resulting timing is shown in Figures 12 and 13.

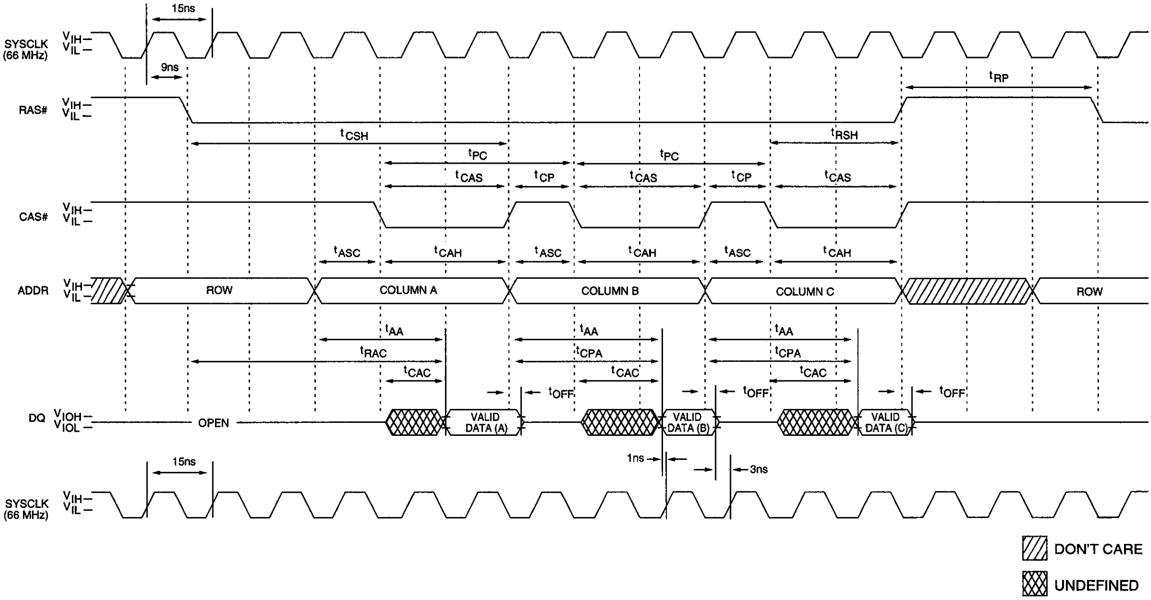


Figure 12
FPM READ CYCLE WITH PROPAGATION DELAYS – 66 MHz SYSTEM CLOCK

Once again for the FPM case, the data valid window (13ns) does not line up with an existing positive edge of the system clock (while meeting the required setup time) so one of the design techniques mentioned above will need to be employed. The data valid window for the EDO case also does not align with an existing positive clock edge and will require one of the above design techniques. However, in the EDO case, the data valid window is longer than for the FPM case (15ns vs. 13ns) and is therefore simpler to design for. Here we have a case where EDO provides a 50 percent improvement in peak memory bandwidth, but with reduced design complexity.

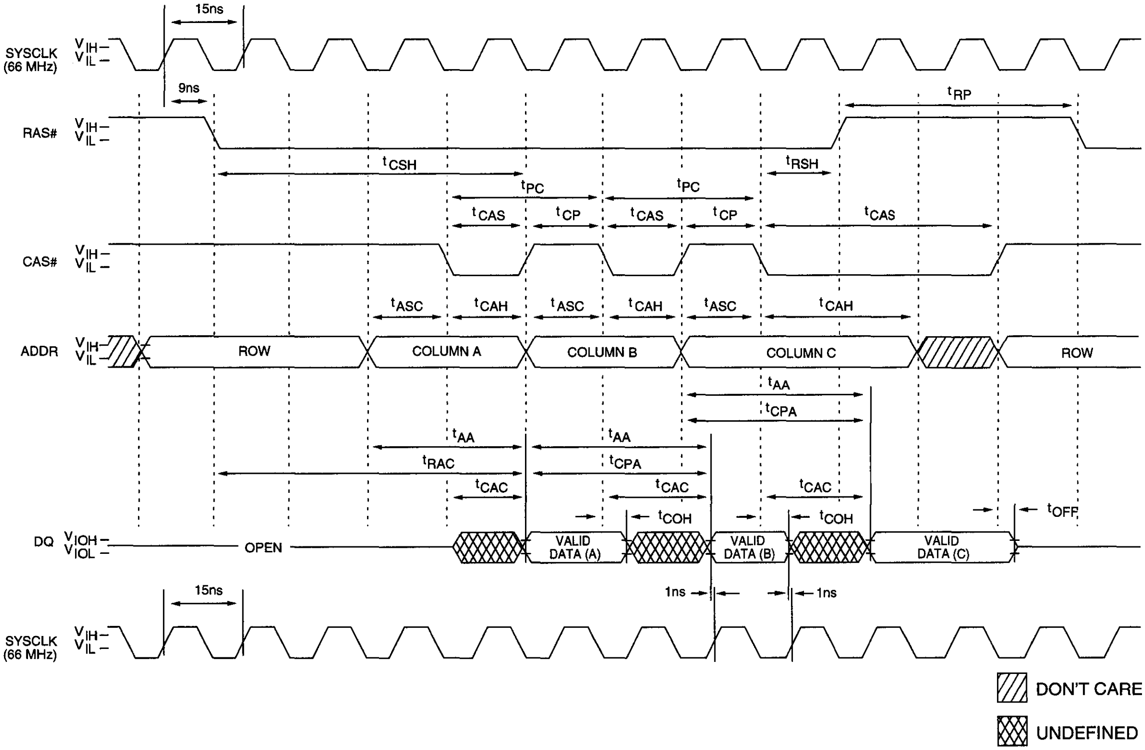


Figure 13
EDO READ CYCLE WITH PROPAGATION DELAYS – 66 MHz SYSTEM CLOCK

DESIGN IMPLICATIONS

Address Setup Time: In order to achieve maximum performance with EDO, it is necessary to provide valid column addresses with sufficient setup time to the falling edge of CAS# so that ^{t}AA is not a limiting parameter. This leaves ^{t}CPA as the limiting parameter for PAGE-MODE READ cycle times. This is true for FPM as well, but there, either ^{t}CAC or ^{t}CPA may be limiting.

With the device timing shown, the column addresses should transition after meeting the hold time (^{t}CAH) from the previous access. This means that the same system clock edge that drives CAS# HIGH will drive the new address. Since ^{t}CPA is typically specified to be 5ns longer than ^{t}AA, if the CAS# and column-address lines transition at the same time, ^{t}CPA will always be limiting. However, the address lines may be more heavily loaded and may transition later. This is not an issue unless the address signals take over 5ns longer than the CAS# signal to become valid and will actually provide additional guardband in meeting ^{t}CAH.

OE# and WE# Operation: In certain situations it is necessary to disable the data outputs while within a page mode access (for example, when switching from a READ cycle to a WRITE cycle or when interleaving banks of memory). For EDO, since CAS# alone will not disable the outputs, either OE# or WE# must be used.

As with FPM devices, the data outputs will be disabled whenever OE# goes HIGH. However, if this occurs (for a specified duration) while CAS# is HIGH, the EDO operation will be suspended. Specifically, the data outputs will be disabled and will remain that way, regardless of subsequent transitions on OE#, until CAS# goes LOW again for a READ cycle. This pulsed operation is beneficial in system implementations which include multiple banks of memory and which may have rows activated in more than one bank simultaneously. Instead of supplying a separate OE# signal for each bank, bank-specific CAS# signals can be used in conjunction with a common OE# signal to disable the data outputs for a given bank. Alternatively, WE# going LOW at any time will suspend EDO operation; the outputs will be disabled and will remain disabled until CAS# goes LOW for a READ cycle

Maximum page mode performance is achieved when executing strictly READ cycles (WE# remains HIGH) or strictly WRITE cycles (WE# remains LOW), as shown in the previous examples. Mixing READ and WRITE within a page is supported, but this usually requires additional clock cycles. For switching from a READ to a WRITE cycle, either OE# or WE# may be used to disable output data; depending on the individual device specification, one method may be faster than the other. In either case, WE# must go LOW to execute the WRITE. More detailed information on OE# and WE# operation can be found in the individual device data sheets.

SUMMARY

EDO is a minor modification over conventional FPM memory components, with major implications in terms of system performance and/or simplifying system design complexity. A very simple physical change at the component level (data not being disabled by CAS# going HIGH within a PAGE-MODE READ access) results in either a longer data valid window or a shorter PAGE MODE cycle time and often results in both. As with any component type, there are specific design factors to be considered but in general, the design complexity of an EDO-based system is equal to or less than that of an FPM-based system, resulting in a substantial performance increase with no added design cost. The performance increase is measured as an increase in peak memory bandwidth; and on components which are widely available today, this increase can be up to 60 percent based on device specifications and up to 100 percent when actual system clock timing is considered.

TECHNICAL NOTE

VARIOUS METHODS OF DRAM REFRESH

This article was originally published in 1994.

INTRODUCTION

DRAM refresh is the topic most misunderstood by lesigners due to the many ways refresh can be accomplished. This article addresses the most often asked quesions about refresh. The two basic means of performing efresh, distributed and burst, are explained first, followed by the various ways to accomplish refresh: RAS#-ONLY REFRESH, CAS#-BEFORE-RAS# REFRESH and HIDDEN REFRESH.

STANDARD AND EXTENDED REFRESH

DRAMs are often referred to as either "standard refresh" or "extended refresh." Dividing the specified refresh time by the number of cycles required will determine if the DRAM is a standard refresh or an extended refresh device. f the result is 15.6µs, it is a standard refresh device, while a result of 125µs indicates an extended refresh device.

Table 1 lists some of the standard DRAMs and their refresh specifications.

Table 1
STANDARD DRAMs AND REFRESH SPECIFICATIONS

DRAM	REFRESH TIME	NUMBER OF CYCLES	REFRESH RATE
4 Meg x 1	16ms	1,024	15.6µs
256K x 16	8ms	512	15.6µs
256K x 16 (L version)	64ms	512	125µs
4 Meg x 4 (2K)	32ms	2,046	15.6µs
4 Meg x 4 (4K)	64ms	4,096	15.6µs

DISTRIBUTED REFRESH

Distributing the refresh cycles so that they are evenly spaced is known as distributed refresh. To perform distributed refresh on a standard DRAM, execute a refresh cycle every 15.6µs such that all rows are turned on before repeating the task. When not being refreshed, the DRAM can be read from or written to.

BURST REFRESH

Refresh may be achieved in a burst method by performing a series of refresh cycles, one right after the other until all rows have been accessed. During refresh other commands are not allowed. Below is a drawing representing burst and distributed refresh.

For example: a 4 Meg x 1 requires 1,024 consecutive refresh cycles, each of which will use 130ns (^tRC) for a 70ns device:

$$1{,}024 \text{ cycles} \times 130\text{ns} = 133{,}120\text{ns} = 0.133\text{ms}$$
$$16\text{ms} - 0.133\text{ms} = 15.867\text{ms}$$

Approximately 0.13ms would be spent performing refresh, and the remaining 15.87ms could be spent reading and writing; then burst refresh would occur again, and so on.

Distributed refresh is the more common of the two refresh categories. The DRAM controller is set up to perform a refresh cycle every 15.6µs. Usually, this means the controller allows the current cycle to be completed and then holds off all instructions while a refresh is performed on the DRAM. The requested cycle is then allowed to resume.

REFRESH CYCLES

There are different cycles you can use to refresh DRAMs, all of which can be used in a distributed or burst method. There are three types listed in a standard data sheet:

- RAS#-ONLY REFRESH
- CAS#-BEFORE-RAS# REFRESH
- HIDDEN REFRESH

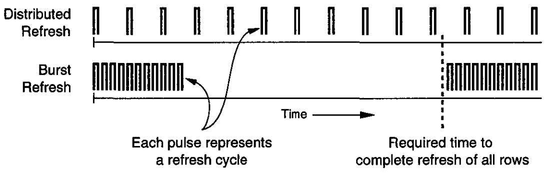


Figure 1
BURST AND DISTRIBUTED REFRESH

RAS#-ONLY REFRESH

To perform a RAS#-ONLY REFRESH, a row address is put on the address lines and then RAS# is dropped. When RAS# falls, that row will be refreshed and as long as CAS# is held HIGH, the DQs will remain open. (See Figure 2.)

It is the DRAM controller's function to provide the addresses to be refreshed and make sure that all rows are being refreshed in the appropriate amount of time. The row order of refreshing does not matter; what is important is that each row be refreshed in the specified amount of time.

CAS#-BEFORE-RAS# REFRESH

CAS#-BEFORE-RAS# REFRESH, also known as CBR REFRESH, is a frequently used method of refresh because it is easy to use and offers the advantage of a power savings. A CBR REFRESH cycle is performed by dropping CAS# and then dropping RAS#. One refresh cycle will be performed each time RAS# falls. WE# must be held HIGH while RAS# falls. The DQs will remain open during the cycle.

Here's how CBR REFRESH works. The die contains an internal counter which is initialized to a random count when the device is powered up. Each time a CBR REFRESH is performed, the device refreshes a row based on the counter, and then the counter is incremented. When CBR REFRESH is performed again, the next row is refreshed and the counter is incremented. The counter will automatically wrap and continue when it reaches the end of its count. There is no way to reset the counter. The user does not have to supply or keep track of row addresses. A drawing of one CBR REFRESH cycle is shown in Figure 3. CAS# must be held LOW before and after RAS# falls to meet ^{t}CSR and ^{t}CHR. Figure 4 shows three CBR REFRESH cycles. In this drawing, CAS# stays LOW and only RAS# toggles. Every time RAS# falls a refresh cycle is performed. CAS# may be toggled each time, but it's not necessary.

CBR POWER SAVINGS

Since CBR REFRESH uses the internal counter and not an external address, the address buffers are powered-down. For power-sensitive applications, this can be a benefit because there is no additional current used in switching address lines on a bus, nor will the DRAMs pull extra power if the address voltage is at an intermediate state.

CBR REFRESH IS EASY TO USE

Since CBR REFRESH uses its own internal counter, there is not a concern about the controller having to supply the refresh addresses. Virtually all DRAMs support CBR REFRESH and the 15.6µs refresh rate, so you can design for CBR REFRESH at the distributed rate of 15.6µs and plug in many different DRAMs without having to worry about refresh. For example, the 4 Meg x 4 comes in two versions:

- 2,048 cycles in 32ms
- 4,096 cycles in 64ms

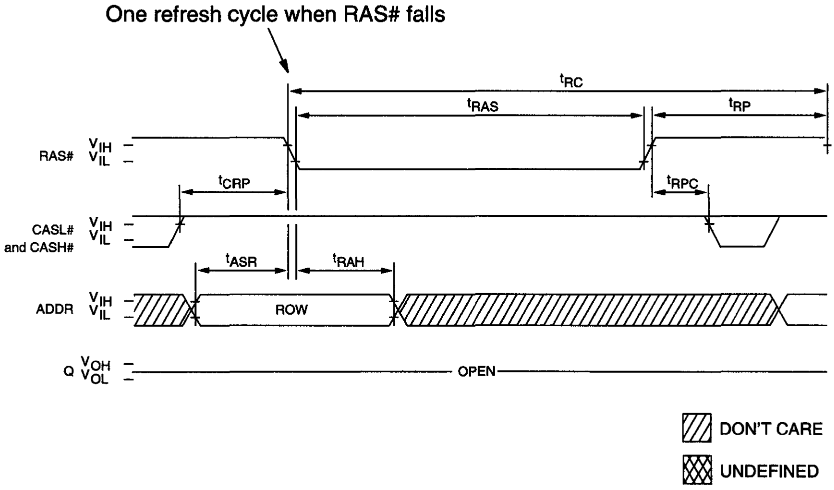


Figure 2
RAS#-ONLY REFRESH

If CBR REFRESH is used, simply maintain the standard 15.6µs refresh rate. If RAS#-ONLY REFRESH is used, addresses must be supplied as follows:

- A0-A10 for the 2,048 cycle refresh
- A0-A11 for the 4,096 cycle refresh

HIDDEN REFRESH

In HIDDEN REFRESH, the user does a READ or WRITE cycle and then, leaving CAS# LOW, brings RAS# HIGH (for minimum of ${}^tRP$) and then LOW. Since CAS# was LOW before RAS# went LOW, the part will execute a CBR REFRESH. In a READ cycle the output data will remain valid during the CBR REFRESH. The refresh is not "hidden" in the sense that you can hide the time it takes to refresh; instead, it is hidden in the sense that data-out will stay on the lines while performing the function. READ and HIDDEN REFRESH cycles will take the same amount of time: ${}^tRC$. The two cycles together take 2 x ${}^tRC$. If we were to do

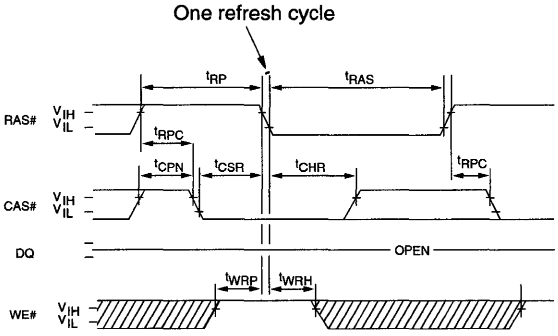


Figure 3
ONE CAS#-BEFORE-RAS# REFRESH CYCLE

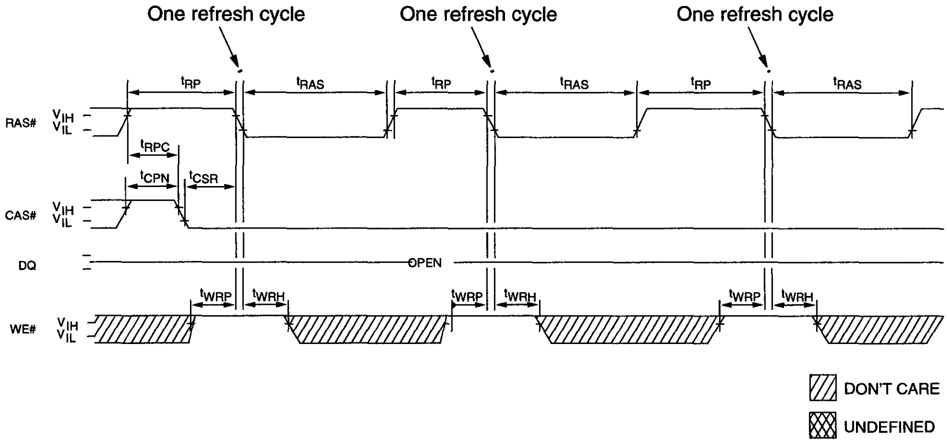


Figure 4
THREE CAS#-BEFORE-RAS# REFRESH CYCLES

a READ and then follow it with a standard CBR REFRESH (instead of a HIDDEN REFRESH), this would take the same amount of time: 2 x ᵗRC.

Figure 5 shows a READ followed by a HIDDEN REFRESH. Figure 6 shows a READ followed by a standard CBR REFRESH. The only difference between the two is that data-out is valid during the HIDDEN REFRESH.

SUMMARY

Three different cycles exist to perform refresh on a standard DRAM: RAS#-ONLY REFRESH, CBR REFRESH, and HIDDEN REFRESH. Each cycle can be used in a burst or distributed method, whichever best fits the designer's needs. It is strongly urged that CBR REFRESH be used to refresh the DRAM. Future DRAMs will most likely require CBR REFRESH only.

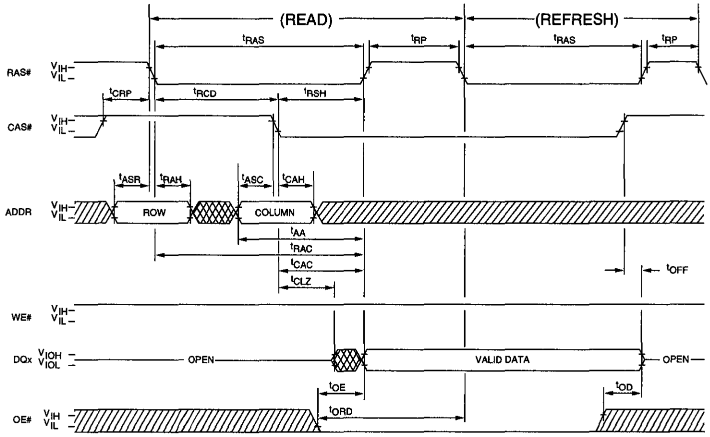


Figure 5
READ CYCLE FOLLOWED BY HIDDEN REFRESH

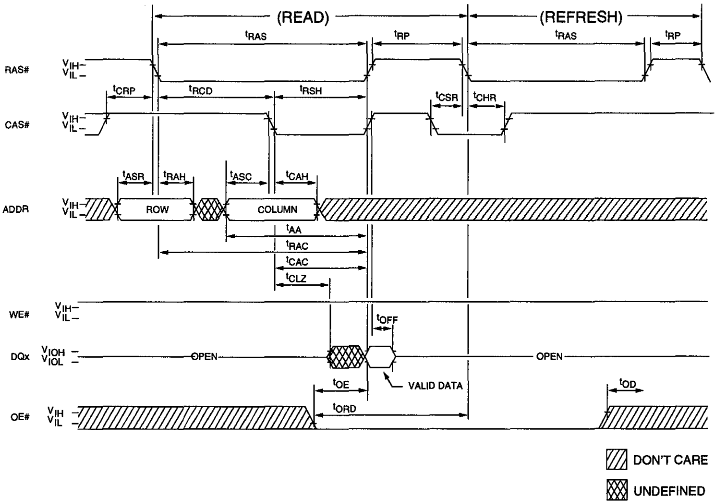


Figure 6
READ CYCLE FOLLOWED BY CBR REFRESH

TECHNICAL NOTE

REDUCE DRAM MEMORY COSTS WITH CACHE

This article was originally published in 1994.

INTRODUCTION

All PCs sold today (x486 and above) have cache memory, usually both internal to the processor (L1) and external to the processor (L2). The intended purpose of the cache memory is to minimize the number of wait-states the DRAM-based main memory imposes on the microprocessor. In other words, cache memory improves the speed of microprocessor accesses because it is significantly faster than DRAM-based main memory.

Today, the performance of the DRAM-based main memory is not nearly as important to the microprocessor accesses as it was before the use of cache memories—a side benefit of incorporating cache that is generally overlooked. Cache is used during most of the microprocessor accesses (80 to 96+ percent of the accesses). When cache memory is accessed, DRAM-based main memory is not accessed. This means DRAM-based main memory is accessed by the microprocessor a small percentage of the time. This is a dramatic shift from the previous generations of systems that did not incorporate cache memory.

Two performance factors of the DRAM which dramatically improve when the usage rate of the DRAM is reduced are speed and soft error rates (SER).

DRAM SPEED

Prior to the employment of cache memory, the DRAM speed had a significant effect on the microprocessor's performance and was generally considered to be the bottleneck in system performance. Figure 1 depicts the historical performance increases obtained as the DRAM speed has improved from 120ns to 80ns. The analysis assumes a 386 microprocessor (no L1 cache), no external cache and 10ns buffer/trace delay.

DRAM speed grade improvements generally provided significant microprocessor performance enhancements. This generated the demand for faster DRAMs and warranted the extra premium being charged for them.

With the introduction of primary (L1) and secondary (L2) cache memory, the number of microprocessor accesses to the DRAM main memory has been significantly reduced, as seen in Figure 2. A microprocessor with internal (L1) cache will generally require 15 to 20 percent of the memory accesses to go out of the microprocessor and access either an L2 cache memory or the DRAM main memory. With the addition of an L2 cache memory, just one to four percent of the memory accesses are required to go to the slower DRAM main memory.

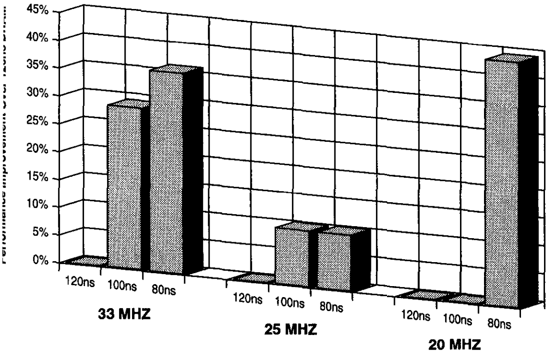


Figure 1
HISTORICAL DRAM MEMORY PERFORMANCE IN PCs

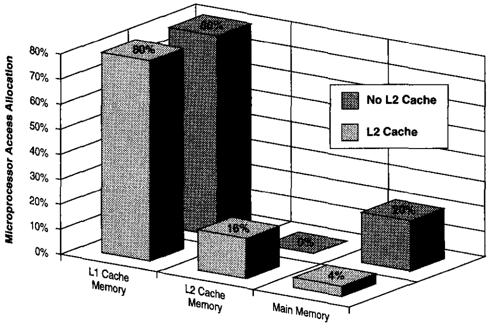


Figure 2
MICROPROCESSOR ACCESS ALLOCATION

With only one to four percent of the memory accesses now going to DRAM main memory, microprocessor performance improvements obtained by using today's faster DRAMs are greatly minimized, as is seen in Figure 3. For example, utilizing 50ns DRAMs in a 486-based PC with an L2 cache and both L1 and L2 caches obtaining an 80 percent hit rate, the microprocessor's performance would be improved by less than one percent over the employment of 70ns DRAMs.

Excluding cache memory effects, a more in-depth look into the DRAM's speed performance reveals that the perceived advantages of faster DRAMs in PCs are, in part, diminished due to the nature of data being clocked. So, the faster DRAM speed does not affect the microprocessor's performance unless it can eliminate a wait-state, as demonstrated in Figure 4.

It should be noted that a faster ^{t}RAC (sufficiently fast enough to eliminate a wait state) only improves the microprocessor's burst performance by one clock at best; whereas a sufficiently faster ^{t}CAC improves the microprocessor's burst performance by three clocks. Thus, the impetus behind the growing demand for EDO DRAMs (see technical note TN-04-29, "Maximizing EDO Advantages at the System Level").

A prudent system designer can generally deliver the best price/performance ratio by using 70ns DRAMs rather than pay speed premiums for 50 and 60ns DRAMs. With today's computing architectures, one should not assume a faster DRAM equates to noticeable microprocessor performance improvement.

MULTIPLE-CLOCKED MICROPROCESSORS

It is worth noting that the previous analysis is based on non-multiple-clocked microprocessors. That is, microprocessors in which the data bus is clocking at the same rate as the microprocessor. The performance effects of the DRAM are more pronounced on multiple-clocked microprocessors.

Although the percentage of DRAM main memory accesses remains the same, the amount of time a DRAM access slows the microprocessor is no longer a one-to-one ratio due to the multiple microprocessor clocks. This ratio is different because each wait-state the external memory imposes on the microprocessor equates to several clocks for the microprocessor (e.g., three clocks for a triple-clocked microprocessor).

A typical PC system with an L1 cache (assume L1 and L2 each have 80 percent hit rate) will retain 80 percent of the memory accesses internal to the microprocessor (L1) and direct the remaining to external memory. Of this, 80 percent of the external memory accesses (16 percent of the total memory accesses) go to the secondary cache. The remaining memory accesses (4 percent of the total memory accesses) go to DRAM memory. For a multiple-clocked microprocessor-based system, the L2 cache and DRAM memory accesses will require a higher percentage of execution time since each external clock translates to a multiple of the microprocessor's internal clocks.

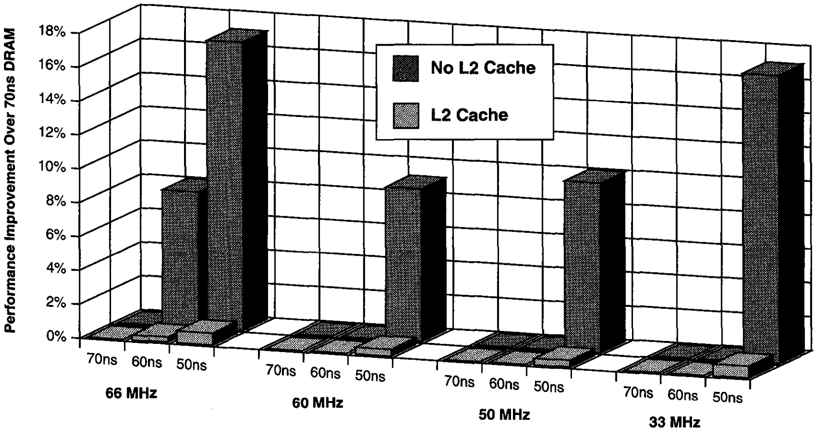


Figure 3
DRAM MEMORY PERFORMANCE IN PCs

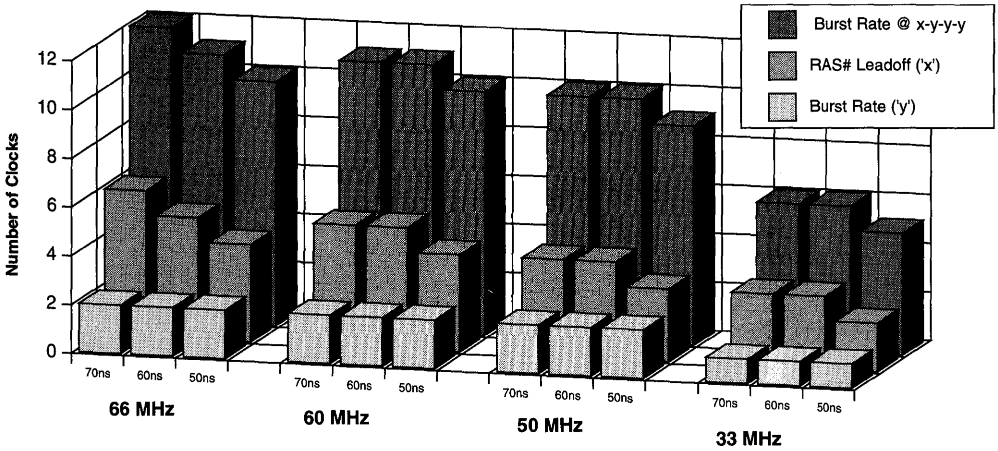


Figure 4
DRAM SPEED vs. CLOCKS IN PCs

The difference between a DX4-486 microprocessor (33 MHz external clock, 100 MHz internal clock) and a 33 MHz, DX-486 when using 50ns and 70ns DRAMs is evaluated in Table 1.

This analysis shows that clocked-multiplied microprocessors put more demand on the external memories. For example, 70ns DRAMs require 8 percent of the memory accessing time with a typical 33 MHz, 486DX, but the clock-tripled 33 MHz, 486DX4 requires 17 percent of the memory accessing time. Even with this additional demand on the DRAM memory performance, the performance improvement obtained from using a 50ns DRAM over a 70ns is negligible. The 50ns DRAM only improves the leadoff cycle (i.e., one clock and fails to improve the burst rate).

Table 1
EFFECTS OF MULTIPLE-CLOCKED MICROPROCESSORS

Memory Type	L1-Cache	L2-Cache	70ns DRAMs	50ns DRAMs
33 MHz-486DX				
Percent of accesses	80%	16%	4%	4%
Clocks per burst	5 (2-1-1-1)	5 (2-1-1-1)	11 (5-2-2-2)	10 (4-2-2-2)
Clocks seen by µP	5	5	11	10
Time allocation for burst	76.3%	15.3%	8.4%	n/a
Time allocation for burst	77%	15.3%	n/a	7.7%
100 MHz-486DX4				
Percent of accesses	80%	16%	4%	4%
Clocks per burst	5 (2-1-1-1)	5 (2-1-1-1)	11 (5-2-2-2)	10 (4-2-2-2)
Clocks seen by µP	5	15	33	30
Time allocation for burst	52%	31%	17%	n/a
Time allocation for burst	52.5%	31.5%	n/a	16%

PERIPHERAL COMPONENTS

Besides microprocessor accesses, DRAM memory is accessed by peripheral components. Non-cached peripheral components access the DRAM main memory over either the ISA or the local bus. As previously discussed, even without cache memory, faster DRAMs do not necessarily equate to increased performance.

Figure 5 depicts the leadoff and page mode cycles of today's faster DRAMs while being accessed by peripheral components over either the ISA or the local bus. As the DRAM speed improves, the burst rate does not improve since the speed improvement is not sufficient enough to reduce the number of clocks required. And in the bus speeds used, the burst rate is already at one clock.

In most cases the leadoff cycle does not change between speed versions either. The only improvement in DRAM memory accesses by peripheral components is obtained when using 50ns DRAMs over slower DRAMs at 33 MHz. Additionally, main memory accesses by peripheral components are typically long streams of data (i.e., page mode) which minimizes the improved leadoff time obtained from the faster DRAMs. For example, assume a burst of 128 words. The 50ns DRAM-based main memory would only be 0.8 percent faster than using 70ns DRAMs in a 33 MHz local bus. Such a negligible performance increase makes it difficult to justify speed premiums associated with fast DRAMs.

DRAM SOFT ERRORS

There has been much discussion regarding DRAM soft error rate (SER), with the common question being: "Do I need parity?" A previous technical note, TN-04-28, "DRAM Soft Error Rate Calculations," (1Q94), discusses the issue of parity in detail and provides system designers with the information needed to answer this question. However, it is worth noting that when L1 and L2 cache memory is utilized, DRAM is accessed only one to four percent of the time. This leaves the DRAM main memory in the standby mode the remainder of the time. As mentioned in the same technical note, SER is highly dependent on the DRAM cycle rate. A DRAM is less susceptible to soft errors (by approximately a factor of 20x) when in standby mode (only refresh cycles) than when being accessed at a fast cycle rate.

Figure 6 depicts a typical 32-bit-wide, 4MB, DRAM-based main memory's mean time between failures (MTBF) over various utilization rates (READ/WRITE accesses at 200ns). For example, for a system with cache memories obtaining a 96 percent hit rate (80 percent L1 and 80 percent L2 cache memory hit rates), designers can expect one DRAM soft error during 125 years of continuous use, because it sees only a four percent utilization rate.

The same DRAM memory would experience one DRAM soft error every 25 years if only L1 cache (80 percent hit rate or 20 percent utilization rate) was employed. On the other extreme, the same DRAM memory in a non-cached (no L1 or L2 cache memory) system would see a 50 to 70 percent utilization rate. These conditions would result in approximately one DRAM soft error every 10 years.

SUMMARY

The addition of cache memory not only achieves its objective of minimizing microprocessor wait states, but it also demands less of the DRAM main memory. With cache memory, the need for faster DRAMs and parity memory are all but eliminated in most designs.

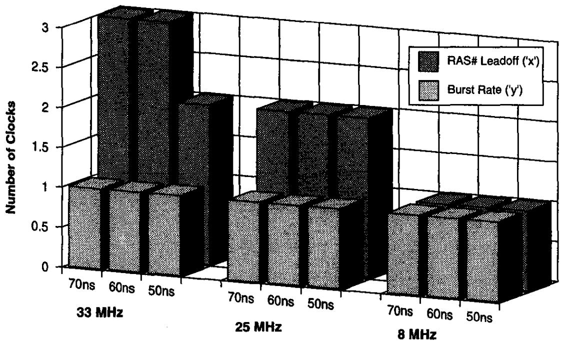


Figure 5
DRAM SPEED vs. LOCAL/ISA BUS ACCESSES

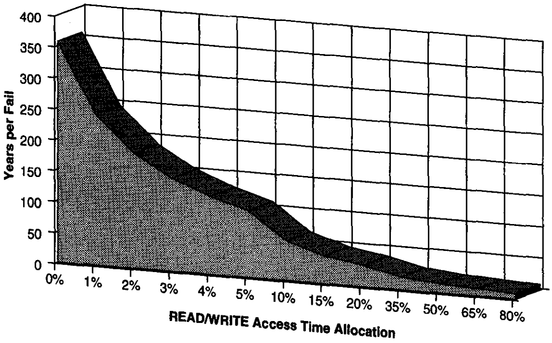


Figure 6
DRAM MTBF TO SOFT ERRORS vs. ACCESS RATE

TECHNICAL NOTE

DESIGNING IN THE RIGHT DRAM "REFRESH" CONFIGURATION

This article was originally published in 1995.

INTRODUCTION

Beginning with the 256K x 16 configuration of the 4Mb generation DRAM and continuing with all configurations of the 16Mb generation and beyond, dual standards have been set for the number of rows to be accessed and refreshed. This means that for a given DRAM configuration, there are two logical arrangements of rows and columns. The design engineer will need to consider a number of factors, including backward and forward compatibility, page size, power dissipation and controller pin count, when deciding which option(s) to support.

RELEVANT TERMINOLOGY

The term "refresh" in this context (e.g., 2K refresh vs. 4K refresh) actually refers to the number of rows in the DRAM array, and while the number of rows in the array does have implications in the actual refresh operation of the DRAM, it has implications in other areas as well.

If the dual standard for a given configuration specifies that one option (e.g., 4K) has twice the number of rows as the other (e.g., 2K), then it must have half the number of columns, and address assignments are redefined accordingly. If the number of row-address inputs for one option is equal to the number of column-address inputs for that option, it is said to have symmetrical addressing. For example, the two options for the 4 Meg x 4 configuration are 2K refresh (2,048 rows x 2,048 columns, or 11 row-address inputs x 11 column-address inputs) or 4K refresh (4,096 rows x 1,024 columns, or 12 row addresses x 10 column addresses). The former option is symmetrical, the latter is asymmetrical.

For some DRAM configurations (e.g., 2 Meg x 8), both options are asymmetrical (see Table 1). Throughout this article, arguments are presented as symmetrical versus asymmetrical. When these arguments are applied to a configuration such as the 2 Meg x 8, which is not available in a strictly symmetrical arrangement, symmetrical can be taken to mean the arrangement closest to being symmetrical.

Table 1
DRAM "REFRESH" CONFIGURATIONS

Configuration	Refresh	Number of Row Addresses	Number of Column Addresses	Page Size	Required Refresh Period at 15.6 µs/row
16Mb					
4 Meg x 4	2K	11	11	2,048	32ms
	4K	12	10	1,024	64ms
2 Meg x 8	2K	11	10	1,024	32ms
	4K	12	9	512	64ms
1 Meg x 16	1K	10	10	1,024	16ms
	4K	12	8	256	64ms
64Mb					
16 Meg x 4	4K	12	12	4,096	64ms
	8K	13	11	2,048	128ms
8 Meg x 8	4K	12	11	4,096	64ms
	8K	13	10	2,048	128ms
4 Meg x 16	4K	12	10	1,024	64ms
	8K	13	9	512	128ms

SUMMARY OF TRADE-OFF

In general, the decision to have more rows instead of more columns, or vice versa, affects power consumption, page size, DRAM design complexity, refresh requirements and also backward and future compatibility. Power consumption is discussed in more detail in the next section.

The page size is equal to the number of columns in a row, so asymmetrical arrangements (more rows) have a smaller page size. This means that fewer locations can be accessed at page mode speed before having to close that page to open a new one, and there is a lower probability of hitting that page on a subsequent access if it is left open.

DRAM design might be more difficult with the symmetrical arrangement (more columns) due to the fact that there are larger current spikes associated with row operations when there are more columns per row.

Refresh requirements are stated as either a refresh period or a refresh interval. The refresh period is the specified time period within which all rows in the DRAM array must be refreshed (activated and precharged). The refresh interval is the time interval between individual row refresh operations, assuming they are distributed evenly over time. With asymmetrical versions (more rows), either the refresh period is increased accordingly, or the refresh interval is decreased accordingly. The former increases DRAM manufacturing cost because of longer test times and lower yields that result from the fact that each cell in the DRAM array must retain data twice (or four times) as long and must be tested for that. The latter is an inconvenience since the industry has standardized on a 15.6µs interval. However, this standard is being reduced for higher-density DRAMs.

POWER CONSUMPTION

The dual standards were generated out of concern for operating current. The activation of circuitry after the falling edge of RAS# generates the single greatest current spike in a DRAM. With double the rows and half the columns, there are half the sense amps to be activated, so this current spike is reduced. In actual operation, this current spike is averaged over longer RAS# cycle times (indicative of page mode operation and the actual duty cycle of the memory), so the power advantages of having more rows and fewer columns is often overstated. Furthermore, the power dissipation delta between asymmetric and symmetric decreases with subsequent die shrinks. Figure 1 compares Icc versus average cycle time.

The larger number of rows can actually increase power consumption when using a low-power standby mode. Since the 1Mb generation, DRAMs have been available with an extended refresh period of up to 128ms, which remains a practical limit with the 4Mb and 16Mb generations. With fewer rows, the refresh pulses can be spaced further apart, reducing power consumption while a system is in standby mode. (The benefit of doubling the refresh interval more than offsets the power drawbacks of having twice as many columns.) When the CPU and logic, backlighting and a hard drive are consuming power, saving a few milliwatts of memory power doesn't significantly impact battery life. However, when in standby mode, the memory power is a more significant percentage of the system power budget. So, although it may seem ironic, most notebook PC designers are selecting the 2K (1K on the 1 Meg x 16) over the 4K refresh option. Additionally, many designers recognize

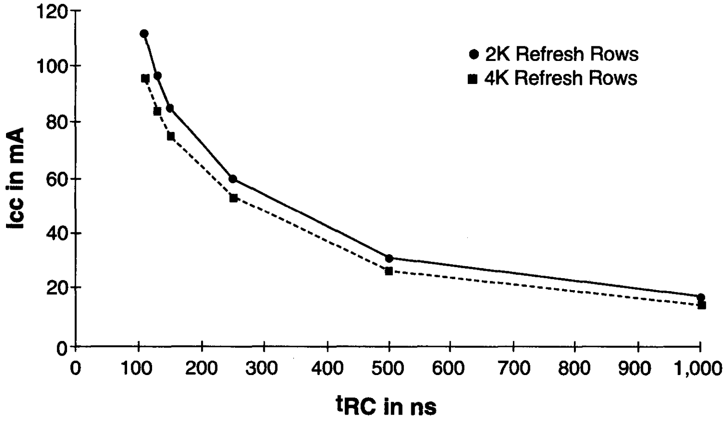


Figure 1
Icc vs. AVERAGE CYCLE TIME

that cache memory reduces the frequency of accesses to main memory, effectively reducing the average duty cycle of the DRAM, which in turn reduces the power consumed by the DRAM.

SELECTING MAINSTREAM DRAMs

Despite potential operating power benefits of asymmetrical addressing, there are several other criteria which must be considered. Due to the large number of DRAMs consumed in the PC business, understanding which DRAM versions the major PC companies select and what factors affect their decision can ensure that even the lowest-volume applications will use the most widely available DRAMs.

Early applications of the 16Mb DRAM included workstations with custom-designed DRAM controllers using the 4 Meg x 4 configuration. The relatively high power of first-generation, 400-mil-wide 4 Meg x 4 DRAMs made it worthwhile to design for the asymmetric versions. Many early users expected that higher-volume applications would follow suit, and some may have designed exclusively for he 12R/10C addressing of the 4K refresh version. But as price-per-bit crossover between 4Mb and 16Mb DRAM approaches, the higher-volume PC market is preparing to adopt the 16Mb DRAM in volumes that will far surpass that of workstation users, and the PC market prefers symmetric addressing for reasons explained below.

COMPATIBILITY WITH CONTROLLERS AND EXISTING PCs

Each chipset or DRAM controller is designed with a fixed number of address pins that provide multiplexed row and olumn addressing. Until recently, the majority of PC hipsets provided only 11 address bits. This means that only the symmetric versions of 16Mb DRAMs can be used with these chipsets.

Now, more and more chipsets are providing a 12th address pin, but the most efficient use of address pins is still the symmetric addressing. In other words, if the most significant bit is added as a row-address bit, the available memory address range can be doubled simply by defining it as a column-address bit as well. So the main benefit of the 12th bit is for the symmetrical versions of the 64Mb DRAMs, as opposed to the asymmetrical versions of the 16Mb DRAM. This allows memory capacity in a few deep banks as opposed to many shallow banks.

Even as the controllers with 12 address bits become more commonplace, it is doubtful that PC companies will use asymmetric DRAMs because they are not backward compatible. The large installed base of PCs is typically about three times that of the current year's production. Most of these systems use the standard 5V, 72-pin, single in-line memory module (SIMM). Shipping these SIMMs with a DRAM that is not backward compatible with all systems will result in special procedures to ensure asymmetric SIMMs are sold only for the new computers.

Nonetheless, asymmetric address DRAMs will continue to be offered. The gradual adoption of chipsets with flexible row and column decoding will eventually result in a large installed base of systems that accept these DRAMs. Perhaps by the time the 64Mb DRAM is available in production volumes, the 4 Meg x 16 DRAM will only be offered with 12R/10C addressing (4K refresh). This is due to the great design challenge in building a high-performance 64Mb DRAM with symmetric addressing (2K refresh cycles) and 32K sense amps activated with each RAS# pulse. Additionally, because the 64Mb DRAM will be available only with a 3.3V operating voltage, backward compatibility with 5V 4Mb DRAMs should no longer be an issue. The emerging 3.3V SIMM and DIMM standards provide an excellent starting point for asymmetric addressing.

Table 2
ASYMMETRICAL vs. SYMMETRICAL DRAMs

	ASYMMETRICAL	SYMMETRICAL
Power dissipation, random cycling	+	-
Power dissipation, page mode	=	=
Power dissipation, standby mode	-	+
Test time (due to ^{t}REF, % of tests in page mode)	-	+
Compatibility with installed base PCs, SIMMs	-	+
Pin count and utilization (controllers)	-	+
Adaptability to 64Mb (applies to 3.3V)	+	-
Page Size	-	+

COEXISTENCE

Due to the very large aftermarket for DRAMs to upgrade the installed base of PCs, symmetrical addressing will dominate over asymmetric addressing. However, the two can coexist, provided DRAM controllers are designed with the flexibility to support both options. A controller with 13 address bits can support 12R/12C addresses. But a controller with 12 address bits cannot support 13R/11C addressing. Therefore, the most universally applicable DRAM will have symmetric addressing. Table 2 highlights some of the advantages and disadvantages of the symmetric versus asymmetric DRAMs.

We offer these recommendations for design engineers developing a DRAM controller interface:

1. Design for asymmetry AND symmetry. If your design can accommodate it, add an additional 13th address pin to gain access to 64Mb DRAMs early in their life cycle.
2. Choose asymmetric for first-generation 64Mb products where 8K refresh may help to achieve sub-60ns yields. First-generation DRAMs are typically slower and use 20-30mA more current than second-generation DRAMs.
3. Be prepared to shift to symmetric as the DRAM process matures (coincides with package shrink, such as the 400 mil, 64Mb). There will always be controllers in the installed base short by one address pin, so the symmetric address part may become dominant.
4. Shift back to asymmetric when the next generation x16 becomes available at a cost comparable to the previous generation x4. For example, the 16 Meg x 16 will require asymmetric 13R/11C addressing. Because the 256Mb ramps four years later than the 64Mb, the 13th address bit will be commonly available.
5. Use a module if possible. This will allow you to take advantage of whichever generation technology or package width is available at the lowest price-per-bit.

TECHNICAL NOTE

EDO COMPATIBILITY WITH FPM DRAMs

This article was originally published in 1996. Micron no longer suggests using EDO/FPM memories for new design implementation.

INTRODUCTION

Various revolutionary and evolutionary DRAM offerings exist in the memory marketplace today. Whenever the semiconductor industry adopts a new DRAM standard, it is essential that users understand the new offering's compatibility with the previous device. Revolutionary DRAM offerings are not included within the scope of this article because they have not established a significant market share and are incompatible with the existing DRAM standard (i.e., the FAST-PAGE-MODE [FPM] DRAM).

Of the evolutionary DRAM offerings, the Extended Data-Out (EDO) DRAM has established itself as the next DRAM standard. The purpose of this article is to discuss compatibility of FPM and EDO DRAMs and assist designers in their transition to this new DRAM standard. FPM and EDO DRAM compatibility can be broken into two key issues: functionality and form-factor.

A brief discussion of the differences between EDO and FPM will be provided. Additional resources are available on EDO, such as Micron DRAM data sheets and technical notes TN-04-21 and TN-04-29. This information can be accessed through Micron's home page on the Internet (*www.micron.com/mti*).

OVERVIEW OF FPM AND EDO DRAMs

FPM has been the standard DRAM mode of operation for the past several years. EDO and FPM DRAMs are manufactured on the same die and require only a metal-mask, fuse or bond change to define the DRAM die as either FPM or EDO. Thus, the EDO DRAM is virtually the same as the FPM DRAM, having the same form-factor (i.e., same package and pinout) and very similar functionality. Specifically, EDO and FPM DRAMs function in the same manner except for one minor difference in how CAS# affects the DQ pins.

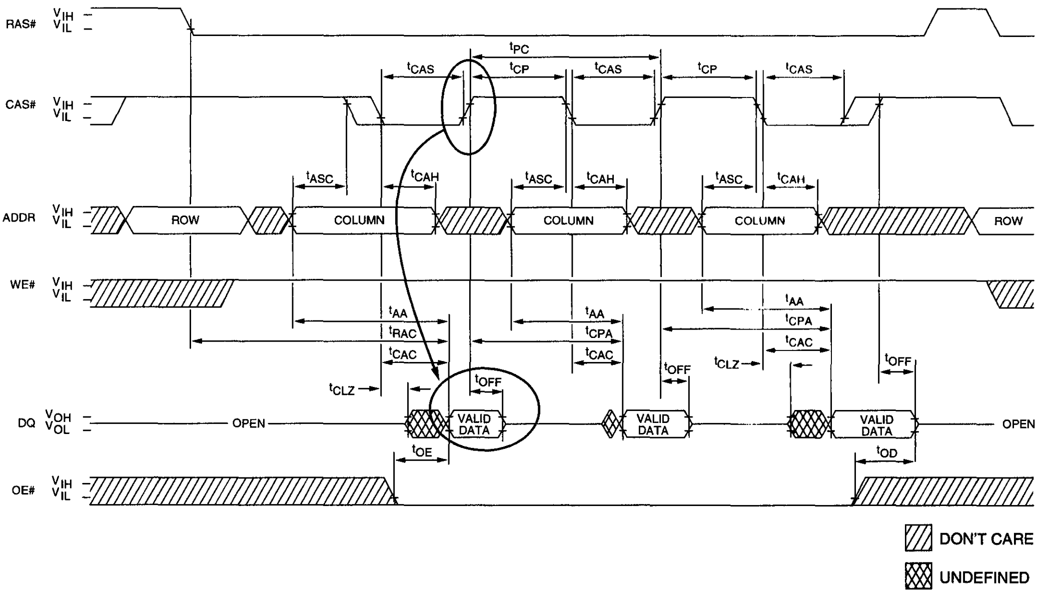


Figure 1
FPM DRAM PAGE MODE CYCLE

On FPM DRAMs, whenever CAS# transitions HIGH while the page is open (RAS# remains LOW), the DQs are automatically placed into High-Z and no longer drive data out, as shown in Figure 1. The advantage of CAS# placing the DQs into High-Z is that it allows the OE# pins to be grounded yet provides adequate READ and EARLY WRITE functionality to meet the requirements of the PC. In fact, this has become the accepted defacto standard in the PC market. However, this approach requires CAS# to remain LOW until the data being read out of the DRAM is latched by the next stage. This delay results in slower page cycle times and extra wait states in faster computer systems.

The EDO DRAM rectifies this loss of time. Whenever CAS# transitions HIGH on an EDO DRAM, the DQs are not placed into High-Z but continue to drive data out, as shown in Figure 2. The advantage with the DQs continuing to drive data out after CAS# transitions HIGH is a pseudo pipeline. That is, the CAS# precharge can be initiated while the data is being latched into the next stage, resulting in a faster page cycle. However, one possible disadvantage with this approach is that the DQs will continue to drive data until they are placed into High-Z by a method other than CAS# transitioning HIGH, which has been relied upon by FPM DRAM designs. Two such methods exist which are compatible with EDO DRAMs:

1. Both RAS# and CAS# transitioning HIGH (see Figure 2).
2. WE# pulsing LOW while CAS# is HIGH (see Figure 3).

DATA I/O CONTROL—COMPATIBILITY

For a given system already employing FPM DRAMs, an EDO DRAM may or may not be compatible as a direct replacement for an FPM DRAM, depending on the data bus requirements. Functional compatibility issues will become evident when an EDO DRAM replaces an FPM DRAM in a system that is designed for FPM and is not compatible with EDO DRAMs. However, even if the EDO DRAM is compatible, any performance improvement that it may have over an FPM DRAM will not be realized. This is because EDO DRAMs do not provide any improvement to memory accesses unless the system has been specifically developed to take advantage of EDO operation.

To determine if an EDO DRAM is compatible with an FPM-based system, the system's data bus constraints must first be defined. When data is accessed from a DRAM memory bank and RAS# remains LOW (page left open), if the system's data bus is accessed by other devices (such as

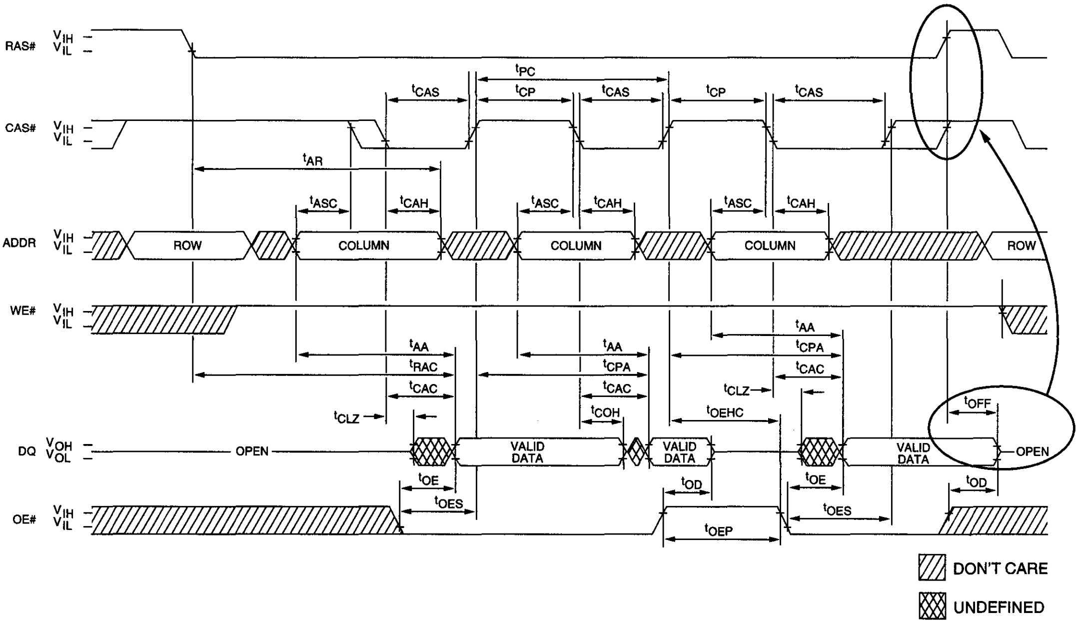


Figure 2
EDO DRAM PAGE MODE CYCLE

che, disk, etc.) or another memory bank (i.e., page inter-ave accesses), EDO DRAMs cannot be used (unless of urse WE# is pulsed LOW after CAS# goes HIGH). The DO DRAMs will not be compatible because their DQs will ntinue to drive data, resulting in contention; whereas the PM DRAMs' DQs will be placed in the High-Z state and ill not contend with the data bus. However, if either RAS# es HIGH with CAS#, or WE# is pulsed LOW after CAS# es HIGH, prior to accessing the data bus, then EDO RAMs may be used in place of FPMs because the DQs will placed in the High-Z state, just as they are when using the PM DRAMs.

YSTEM CONSIDERATIONS

The use of OE# to control the EDO DQs is generally not option. Most computer systems ground OE# and rely on AS# to place the DQs in the High-Z state. This is especially ue with the 72-pin SIMM standard of the PC market.

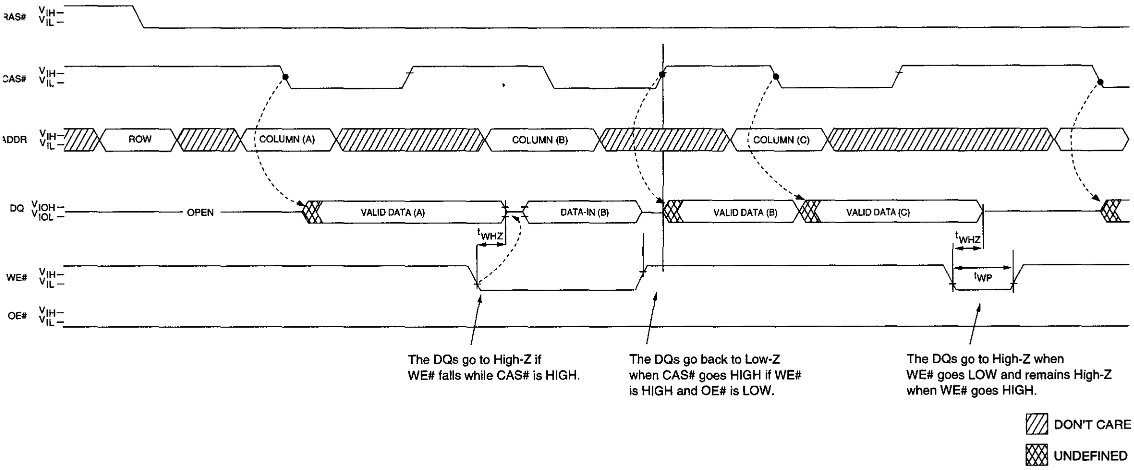
The older the computer system, the less likely it is that DO DRAMs will function in place of FPM DRAMs. For xample, a common practice used to be to leave the memory age open (RAS# LOW) after a memory access was made while the data bus was being accessed by another memory ank to perform page interleave accesses). These applica-ons relied on CAS# transitioning HIGH to place the DQs a High-Z state and prevent bus contention. As previously iscussed, an EDO DRAM will continue to drive data and ontend with the other device trying to use the data bus, us making EDO DRAMs incompatible with FPM DRAMs.

Newer computer system designs tend to close the memory page (RAS# HIGH) when the data bus is not required for the memory, and they also avoid using page interleave accesses. Studies have shown that hiding the precharge and only incurring the leadoff hit (rather than leaving the page open and incurring the precharge delay with page misses) tends to provide higher bandwidth. In these systems, EDO DRAMs can replace FPM DRAMs because when RAS# and CAS# both transition HIGH, either the FPM or EDO DQs will be placed in the High-Z state and prevent bus contention.

Generally, single- and multiple-bank memories with shared CAS# pins are good candidates for EDO compatibility. However, there is no guarantee. Consequently, it is necessary to determine how the memory controller handles the DRAM when it releases the data bus from the memory and whether page interleave accesses are employed. For EDO compatibility, either RAS# must go HIGH with CAS#, or WE# must be pulsed LOW after CAS# goes HIGH at the end of the DRAM memory access, prior to the data bus being accessed by another device.

COMPATIBILITY DETERMINATION

Inquiries to several PC chipset suppliers reveal that some FPM-based chipsets are compatible with EDO DRAMs and other PC chipsets are not. Even then, it depends on which version of the chipset is being used and whether cache is invoked. Of course, the newer the PC chipset, the higher the probability of EDO compatibility.



The DQs go to High-Z if WE# falls while CAS# is HIGH.

The DQs go back to Low-Z when CAS# goes HIGH if WE# is HIGH and OE# is LOW.

The DQs go to High-Z when WE# goes LOW and remains High-Z when WE# goes HIGH.

▨ DON'T CARE
▩ UNDEFINED

Figure 3
WE# CONTROLLED EDO-PAGE-MODE CYCLE

If one is unable to determine if the DRAM controller is compatible with EDO DRAMs, a less desirable but effective determination is to boot up the system with EDO DRAMs in place of the FPM DRAMs. If EDO DRAMs are compatible, the system will boot-up and operate fine. (The system will not experience even marginal problems due to EDO DRAMs being used.) If EDO DRAMs are not compatible, the system will not boot-up properly. Additionally, if the system operates with EDO DRAMs in the first bank of the FPM DRAM-based system, there is no guarantee the second bank will also work with additional memory at a later date.

Computer systems that only support FPM DRAMs due to page interleave accesses can sometimes support EDO DRAMs by having their CMOS setup altered to support standard page accesses. A similar alternative for computer manufacturers also exists. Working with the BIOS and the chipset supplier can provide EDO compatibility in FPM systems and resolve the contention issue outlined above.

Today's latest PC chipsets (usually Pentium-based), and consequently, the latest PC systems, generally provide for either FPM or EDO DRAM usage automatically. In fact most PC chipsets (but not all) now support the mixing o EDO and FPM DRAMs, by bank, in the same PC memory

SUMMARY

FPM and EDO DRAMs come from the same die and have the same pinouts and package dimensions, thus providing complete form-factor compatibility between EDO and FPM DRAMs. Functionally, the EDO DRAM operates much in the same manner as the FPM DRAM, with the exception o how the DQs are placed into the High-Z state.

Most, but not all, FPM-based applications are compatible with EDO DRAMs, and applications which are not directly compatible can generally be made compatible. This wil become more of an issue as the availability of FPM DRAMs decreases. It is important to note, however, that customers will not actually gain any performance advantage from using EDO DRAMs in their systems unless their systems are specifically designed to use EDO.

TECHNICAL NOTE

MEMORY MODULE SERIAL PRESENCE-DETECT

This article was originally published in 1997.

INTRODUCTION

As new memory technologies are developed and introduced to the industry, the need to incorporate these technologies in modular form becomes evident. Consequently, new memory technologies are being added to existing module standards. This presents a challenge since the existing parallel type presence-detect (PD) is unable to support these new variations. To allow greater flexibility, in expectation of these new technologies, the latest module standards are incorporating a serial type PD that can be expanded as needed. Serial presence-detect (SPD) has been standardized through JEDEC so that implementation will be consistent from one module standard to the next. This note will define the means to implement and utilize SPD.

SERIAL PRESENCE-DETECT vs. PARALLEL PRESENCE-DETECT

Parallel PD, the type of presence-detection used on 72-pin SIMMs, 168-pin buffered DIMMs and IC DRAM cards, utilizes 4 to 10 pins on the edge connector to set a combination of high and low signals which a system can detect. Each different combination of settings defines a unique module configuration. The PD settings define features such as density, speed, etc. A system can, in parallel, compare a module's settings with a standard settings table to determine the type of module that has been installed. The disadvantage of this parallel PD format is that as new features need to be detected, more pins have to be allocated from the module pinout . This proliferation of PD pins leads to unoptimized module sizes. By going with an SPD approach, new features can be added without increasing the number of module pins required. This is accomplished by using a nonvolatile memory device (typically a 256 word x 8 bit software lockable EEPROM) to store the module information in the form of lookup tables, binary data or ASCII data. Since the pins needed to read and write to the SPD memory device are already defined, no additional pins need to be added as new technologies are introduced. Instead, the new definitions can be included in the existing lookup tables.

DEFINITION

SPD is intended for use on any new memory module independent of memory technology or form factor. At the point of standardization of any given memory module, the standard will include the following pertinent information regarding SPD:

- SPD interface protocol
- Acceptable module configurations
- Legitimate architectures: depth, width, number of banks, addressing
- Acceptable error checking schemes (ECC and/or parity)
- SPD wiring diagram and module pin assignments

The interface protocol must be defined with each new module standard and remain constant. The IIC communication protocol has been used for past JEDEC SPD definitions. This two-wire protocol is designed to minimize device pin count and simplify PCB layout requirements. It allows synchronous bidirectional communication between a master and a slave (EEPROM storing SPD data) using CLOCK (SCL) and DATA I/O (SDA) lines. The master will always initiate data transfers and provide the clock for both transmit and receive operations.

The SPD data stored in the EEPROM is defined as bytes of information in a specific order. Much of the SPD data is organized as a series of table entries. Each table entry contains one or more bytes of information. Each table entry represents one particular characteristic pertinent to the memory module; e.g., Fast Page Mode DRAM will have specific tables for ^{t}RAC, ^{t}CAC, number of banks, number of row addresses, number of column addresses, error detection/correction, refresh rates, data width and interface standard. Each table entry corresponds to a position on a lookup table. The number of bytes needed to express a particular aspect of a module and the byte sequence are fixed and defined in the JEDEC SPD standard. Table 1 shows an example of a DRAM SPD matrix and Table 2 shows an example of an SDRAM SPD matrix. These types of matrices will be included in the module data sheets to show exactly how a specific module's SPD has been programmed.

SPD CONTENT AND ORDER

This section presents the order the SPD bytes should follow and shows how many bytes must be used to define a given SPD. Each table associated with bytes 0-127 below

SPD CONTENT AND ORDER (continued)

will show the valid settings that can be selected to identify specific modules.

Byte 0:	Total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information.
Byte 1:	Total SPD memory size used to hold the SPD data.
Byte 2:	Identifies the fundamental memory type implemented on the module. The type of memory may include FPM, EDO, SDRAM, etc.
Byte 3:	Defines the number of row addresses in the module's DRAM/SDRAM array.
Byte 4:	Defines the number of column addresses in the module's DRAM/SDRAM array.
Byte 5:	Defines the number of banks on the module.
Bytes 6 & 7:	Defines the data width on the module. If the data width is 255 bits or less, only byte 6 is used. Byte 7 is only used if the data width is 256 bits or greater.
Byte 8:	Defines the module's voltage interface.
Byte 9:	Defines the module's RAS# access time (DRAM) or the Cycle time at highest CAS latency (SDRAM).
Byte 10:	Defines the module's CAS# access time (DRAM) or the Access time from Clock at highest CAS latency (SDRAM).
Byte 11:	Defines the module's error detection and/or correction scheme.
Byte 12:	Defines the module's refresh rate and type.
Byte 13:	Defines the width of the primary DRAM/SDRAM used on the module.
Byte 14:	Defines the width of the error-checking DRAM/SDRAM used on the module.
Byte 15:	(SDRAM) Min. clock delay for back to back random column addresses.
Byte 16:	(SDRAM) Defines various burst lengths supported.
Byte 17:	(SDRAM) Defines the number of banks internal to the SDRAM devices.
Byte 18:	(SDRAM) Defines which CAS latencies are supported.
Byte 19:	(SDRAM) Defines which CS latencies are acceptable.
Byte 20:	(SDRAM) Defines which WE latencies are acceptable.
Byte 21:	(SDRAM) Defines various aspects of the module.
Byte 22:	(SDRAM) Defines various aspects of the SDRAMs on the module.
Byte 23:	(SDRAM) Defines the minimum cycle time (clock period) for the SDRAM at its 2nd highest CAS latency.
Byte 24:	(SDRAM) Defines the maximum clock to data out for the SDRAM (^{t}AC) at its 2nd highest CAS latency.
Byte 25:	(SDRAM) Defines the minimum cycle time (clock period) for the SDRAM at its 3rd highest CAS latency.
Byte 26:	(SDRAM) Defines the maximum clock to data out (^{t}AC) for the SDRAM at its 3rd highest CAS latency.
Byte 27:	(SDRAM) Defines the precharge to activate minimum (tRP).
Byte 28:	(SDRAM) Defines the minimum row activate to row activate delay (^{t}RRD).
Byte 29:	(SDRAM) Defines the minimum RAS to CAS delay (^{t}RCD).
Byte 30:	(SDRAM) Defines the minimum activate to precharge time (^{t}RAS).
Byte 31:	(SDRAM) Describes the memory capacity of each physical row on the module.
Byte 32:	(SDRAM) Describes the input setup time with respect to the rising edge of the clock input.
Byte 33:	(SDRAM) Describes the input hold time with respect to the rising edge of the clock input.
Byte 34:	(SDRAM) Describes the input setup time with respect to the rising edge of the clock input.
Byte 35:	(SDRAM) Describes the input hold time with respect to the rising edge of the clock input.
Bytes 36-61:	Reserved for future superset information.
Byte 62:	(SDRAM) Indicates the JEDEC SDRAM DIMM SPD data revision.
Byte 63:	Checksum for bytes 0-62. Suggested calculation method is modulo 256.
Bytes 64-125:	Manufacturer's JEDEC ID code, location, part number, revision code, date, assembly serial number and other manufacturer specific data.
Byte 126:	(SDRAM) Defines the clock frequency of the Intel SDRAM DIMM specification.
Byte 127:	(SDRAM) Defines the SDRAM component and clock interconnection details for the DIMM.
Bytes 128-255:	Unused storage locations.

;PD IMPLEMENTATION

As mentioned earlier, the SPD is typically implemented ısing a serial EEPROM. The module edge connector pins ısed to operate the EEPROM consist of the serial clock SCL), serial data (SDA), write protect (WP) and the three ıddress inputs (SA0-SA2). The SCL input is used to clock all lata into and out of the device. SDA is a bidirectional pin ısed to transfer data into and out of the device. It is an open lrain output and may be wire OR'd with any number of ›ther SDA pins. The WP pin is the hardware write protect ›in. The SA0, SA1 and SA2 address pins are connected to /cc or Vss to configure the EEPROM address.

Data states on the SDA line can change only during SCL .OW (Figure 1). SDA state changes during SCL HIGH are eserved for indicating start and stop conditions (Figure 2). \dditional operating and timing information on the :EPROM can be obtained from a 24xxS52 EEPROM data heet.

The serial EEPROM has a software write protect feature hat allows the lower half of the array (addresses 00h - 7Fh) o be permanently write protected. This feature is invoked ›y writing to the write protect register. Once the software vrite protect register has been written, the write protection s enabled and cannot be reversed, even if the device is ›owered down. For hardware write protection the WP pin :an be tied to Vcc and the entire array will be write proected, regardless of whether the software write protect egister has been written or not. If the WP pin is set to Vcc, t will prevent the software write protect register from being vritten.

The SPD can be incorporated into a system design several ways. The first configuration is referred to as Common Clock/Common Data (Figure 3). In this configuration, SA0-SA2 are wired at each DIMM socket in a binary sequence for a maximum of eight modules. All eight modules share a common clock and common data line. Pull-up resistors (4.7K typical) are required on all SCL and SDA signals due to their open drain interface. The second configuration is Common Clock/Separate Data (Figure 4). In this configuration, SA0-SA2 are wired at each DIMM socket to the same address (typically all to Vss). The SCL is wired to all positions. The SDA is unique for each position, allowing for greater than eight positions, but not permitting CMAX to exceed 400pf. Since the data pins are separate, eight positions could provide parallel data paths of one byte (8x speed improvement). The third configuration is the Common Data/Separate Clock (Figure 5). SA0-SA2 are wired at each DIMM to the same address. The SDA is wired to all positions. The SCL is unique for each position, allowing for greater than eight positions, but not permitting CMAX to exceed 400pF.

SUMMARY

The new SPD standard allows greater flexibility for incorporating identification of new features and technologies on memory modules. The older parallel PD format requires more edge connector pins to support new features and technologies. The new module standards being released are defined with the serial type of PD.

Table 1
SPD EXAMPLE FOR 144-PIN 4/8 MEG x 64 DRAM SODIMMs

BYTE	DESCRIPTION	ENTRY (VERSION)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
0	NUMBER OF BYTES USED BY MICRON	128	1	0	0	0	0	0	0	0	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	0	0	0	0	1	0	0	0	08
2	MEMORY TYPE	FAST PAGE MODE	0	0	0	0	0	0	0	1	01
		EDO PAGE MODE	0	0	0	0	0	0	1	0	02
3	NUMBER OF ROW ADDRESSES	12	0	0	0	0	1	1	0	0	0C
4	NUMBER OF COLUMN ADDRESSES	10 (32MB)	0	0	0	0	1	0	1	0	0A
		11 (64MB)	0	0	0	0	1	0	1	1	0B
5	NUMBER OF BANKS	1	0	0	0	0	0	0	0	1	01
6	MODULE DATA WIDTH	64	0	1	0	0	0	0	0	0	40
7	MODULE DATA WIDTH (continued)	0	0	0	0	0	0	0	0	0	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL	0	0	0	0	0	0	0	1	01
9	RAS# ACCESS TIME (^{t}RAC)	50ns (-5)	0	0	1	1	0	0	1	0	32
		60ns (-6)	0	0	1	1	1	1	0	0	3C
10	CAS# ACCESS TIME (^{t}CAC)	13ns (-5)	0	0	0	0	1	1	0	1	0D
		15ns (-6)	0	0	0	0	1	1	1	1	0F
11	MODULE CONFIGURATION TYPE	NONPARITY	0	0	0	0	0	0	0	0	00
12	REFRESH RATE/TYPE 15.6µs	NORMAL	0	0	0	0	0	0	0	0	00
13	DRAM WIDTH (PRIMARY DRAM)	x16 (32MB)	0	0	0	1	0	0	0	0	10
		x8 (64MB)	0	0	0	0	1	0	0	0	08
14	ERROR-CHECKING DRAM DATA WIDTH	NONE	0	0	0	0	0	0	0	0	00
62	SPD REVISION	REV. 0	0	0	0	0	0	0	0	0	00
63	CHECKSUM FOR BYTES 0-62		x	x	x	x	x	x	x	x	xx
64	MANUFACTURER'S JEDEC ID CODE	MICRON	0	0	1	0	1	1	0	0	2C
65-71	MANUFACTURER'S JEDEC CODE (CONT.)		1	1	1	1	1	1	1	1	FF
72	MANUFACTURING LOCATION		0	0	0	0	0	0	0	1	01
			0	0	0	0	0	0	1	0	02
			0	0	0	0	0	0	1	1	03
			0	0	0	0	0	1	0	0	04
73-90	MODULE PART NUMBER (ASCII)		x	x	x	x	x	x	x	x	xx
91	PCB REVSION CODE	A	0	0	0	0	0	0	0	1	01
		B	0	0	0	0	0	0	1	0	02
		C	0	0	0	0	0	0	1	1	03
		D	0	0	0	0	0	1	0	0	04
92	REVISION CODE (CONT.)	0	0	0	0	0	0	0	0	0	00
93	YEAR OF MANUFACTURE IN BCD		x	x	x	x	x	x	x	x	xx
94	WEEK OF MANUFACTURE IN BCD		x	x	x	x	x	x	x	x	xx
95-98	MODULE SERIAL NUMBER		x	x	x	x	x	x	x	x	xx
99-125	MANUFACTURER-SPECIFIC DATA (RSVD)		–	–	–	–	–	–	–	–	–

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

Table 2
SPD EXAMPLE FOR 168-PIN 8/16 MEG x 72 SDRAM DIMM

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
0	NUMBER OF BYTES USED BY MICRON	128		1	0	0	0	0	0	0	0	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256		0	0	0	0	1	0	0	0	08
2	MEMORY TYPE	SDRAM		0	0	0	0	0	1	0	0	04
3	NUMBER OF ROW ADDRESSES	12		0	0	0	0	1	1	0	0	0C
4	NUMBER OF COLUMN ADDRESSES	9		0	0	0	0	1	0	0	1	09
5	NUMBER OF BANKS	1 (64MB) 2 (128MB)		0 0	0 0	0 0	0 0	0 0	0 0	0 1	1 0	01 02
6	MODULE DATA WIDTH	64		0	1	0	0	0	0	0	0	40
7	MODULE DATA WIDTH (continued)	0		0	0	0	0	0	0	0	0	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL		0	0	0	0	0	0	0	1	01
9	SDRAM CYCLE TIME (CAS LATENCY = 3)	8 (-10B) 10 (-662)	^{t}CK	1 1	0 0	0 1	0 0	0 0	0 0	0 0	0 0	80 A0
10	SDRAM ACCESS FROM CLOCK (CAS LATENCY = 3)	6 (-10B) 7 (-662)	^{t}AC	0 0	1 1	1 1	0 1	0 0	0 0	0 0	0 0	60 70
11	MODULE CONFIGURATION TYPE	NONPARITY		0	0	0	0	0	0	0	0	00
12	REFRESH RATE/TYPE	15.6µs/SELF		1	0	0	0	0	0	0	0	80
13	SDRAM WIDTH (PRIMARY SDRAM)	8		0	0	0	0	1	0	0	0	08
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE		0	0	0	0	0	0	0	0	00
15	MINIMUM CLOCK DELAY FROM BACK-TO-BACK RANDOM COLUMN ADDRESSES	1	^{t}CCD	0	0	0	0	0	0	0	1	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE		1	0	0	0	1	1	1	1	8F
17	NUMBER OF BANKS ON SDRAM DEVICE	4		0	0	0	0	0	1	0	0	04
18	CAS LATENCIES SUPPORTED	2, 3		0	0	0	0	0	1	1	0	06
19	CS LATENCY	0		0	0	0	0	0	0	0	1	01
20	WE LATENCY	0		0	0	0	0	0	0	0	1	01
21	SDRAM MODULE ATTRIBUTES	NONBUFFERED		0	0	0	0	0	0	0	0	00
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E		0	0	0	0	1	1	1	0	0E
23	SDRAM CYCLE TIME (CAS LATENCY = 2)	13 (-10B) 15 (-662)	^{t}CK	1 1	1 1	0 1	1 1	0 0	0 0	0 0	0 0	D0 F0
24	SDRAM ACCESS FROM CLK (CAS LATENCY = 2)	9 (-10B/-662)	^{t}AC	1	0	0	1	0	0	0	0	90
25	SDRAM CYCLE TIME (CAS LATENCY = 1)	–	^{t}CK	0	0	0	0	0	0	0	0	00
26	SDRAM ACCESS FROM CLK (CAS LATENCY = 1)	–	^{t}AC	0	0	0	0	0	0	0	0	00
27	MINIMUM ROW PRECHARGE TIME	30 (-10B/-662)	^{t}RP	0	0	0	1	1	1	1	0	1E
28	MINIMUM ROW ACTIVE TO ROW ACTIVE	20	^{t}RRD	0	0	0	1	0	1	0	0	14
29	MINIMUM RAS# TO CAS# DELAY	20 (-10B) 30 (-662)	^{t}RCD	0 0	0 0	0 0	1 1	0 1	1 1	0 1	0 0	14 1E
30	MINIMUM RAS# PULSE WIDTH	50 (-10B) 60 (-662)	^{t}RAS	0 0	0 0	1 1	1 1	0 1	0 1	1 0	0 0	32 3C
31	MODULE BANK DENSITY	64MB		0	0	0	1	0	0	0	0	10
32	COMMAND AND ADDRESS SETUP TIME	2 (-10B) (-662)	^{t}AS,^{t}CMS	0 0	0 0	1 0	0 0	0 0	0 0	0 0	0 0	20 00
33	COMMAND AND ADDRESS HOLD TIME	1 (-10B) (-662)	^{t}AH,^{t}CMH	0 0	0 0	0 0	1 0	0 0	0 0	0 0	0 0	10 00

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

Table 2
SPD EXAMPLE FOR 168-PIN 8/16 MEG x 72 SDRAM DIMM (continued)

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
34	DATA SIGNAL INPUT SETUP TIME	2 (-10B)	^{t}DS	0	0	1	0	0	0	0	0	20
		(-662)		0	0	0	0	0	0	0	0	00
35	DATA SIGNAL INPUT HOLD TIME	1 (-10B)	^{t}DH	0	0	0	1	0	0	0	0	10
		(-662)		0	0	0	0	0	0	0	0	00
36-61	RESERVED			0	0	0	0	0	0	0	0	00
62	SPD REVISION	REV. 1.2 (-10B)		0	0	0	1	0	0	1	0	12
		REV. 1.0 (-662)		0	0	0	0	0	0	0	1	01
63	CHECKSUM FOR BYTES 0-62	64MB -10B		0	1	0	0	1	1	1	1	4F
		64MB -662		0	1	0	0	0	0	1	0	42
		128MB -10B		0	1	0	1	0	0	0	0	50
		128MB -662		0	1	0	0	0	0	1	1	43
64	MANUFACTURER'S JEDEC ID CODE	MICRON		0	0	1	0	1	1	0	0	2C
65-71	MANUFACTURER'S JEDEC ID CODE (CONT.)			1	1	1	1	1	1	1	1	FF
72	MANUFACTURING LOCATION			0	0	0	0	0	0	0	1	01
				0	0	0	0	0	0	1	0	02
				0	0	0	0	0	0	1	1	03
				0	0	0	0	0	1	0	0	04
				0	0	0	0	0	1	0	1	05
				0	0	0	0	0	1	1	0	06
73-90	MODULE PART NUMBER (ASCII)			x	x	x	x	x	x	x	x	x
91	PCB REVSION CODE	A		0	0	0	0	0	0	0	1	01
		B		0	0	0	0	0	0	1	0	02
		C		0	0	0	0	0	0	1	1	03
		D		0	0	0	0	0	1	0	0	04
92	REVISION CODE (CONT.)	0		0	0	0	0	0	0	0	0	00
93	YEAR OF MANUFACTURE IN BCD			x	x	x	x	x	x	x	x	x
94	WEEK OF MANUFACTURE IN BCD			x	x	x	x	x	x	x	x	x
95-98	MODULE SERIAL NUMBER			x	x	x	x	x	x	x	x	x
99-125	MANUFACTURER-SPECIFIC DATA (RSVD)			–	–	–	–	–	–	–	–	–
126	SYSTEM FREQUENCY	100 MHz (-10B)		0	1	1	0	0	1	0	0	64
		66 MHz (-662)		0	1	1	0	0	1	1	0	66
127	SDRAM COMPONENT & CLOCK DETAIL	64MB (-10B)		1	0	1	0	1	1	0	1	AD
		128MB (-10B)		1	1	1	1	1	1	0	1	FD
		(-662)		0	0	0	0	0	1	1	0	06

NOTE: 1. x = Variable Data.

BYTE 0: NUMBER OF BYTES USED BY MANUFACTURER

BYTE 0: NUMBER OF BYTES USED BY MFG.	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
–	–	–	–	–	–	–	–	–	–
128	1	0	0	0	0	0	0	0	80
–	–	–	–	–	–	–	–	–	–
255	1	1	1	1	1	1	1	1	FF

BYTE 1: TOTAL SPD MEMORY SIZE

BYTE 1: TOTAL SPD MEMORY SIZE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Reserved	0	0	0	0	0	0	0	0	00
–	–	–	–	–	–	–	–	–	–
32 Bytes	0	0	0	0	0	1	0	1	05
64 Bytes	0	0	0	0	0	1	1	0	06
128 Bytes	0	0	0	0	0	1	1	1	07
256 Bytes	0	0	0	0	1	0	0	0	08
512 Bytes	0	0	0	0	1	0	0	1	09
–	–	–	–	–	–	–	–	–	–

BYTE 2: FUNDAMENTAL MEMORY TYPE

BYTE 2: FUNDAMENTAL MEMORY TYPE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Reserved	0	0	0	0	0	0	0	0	00
Fast Page Mode DRAM	0	0	0	0	0	0	0	1	01
EDO Page Mode DRAM	0	0	0	0	0	0	1	0	02
–	–	–	–	–	–	–	–	–	–
Synchronous DRAM	0	0	0	0	0	1	0	0	04
–	–	–	–	–	–	–	–	–	–

BYTE 3: NUMBER OF ROW ADDRESSES

BYTE 3: NUMBER OF ROW ADDRESSES	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
–	–	–	–	–	–	–	–	–	–
8	0	0	0	0	1	0	0	0	08
9	0	0	0	0	1	0	0	1	09
10	0	0	0	0	1	0	1	0	0A
11	0	0	0	0	1	0	1	1	0B
12	0	0	0	0	1	1	0	0	0C
13	0	0	0	0	1	1	0	1	0D
14	0	0	0	0	1	1	1	0	0E
15	0	0	0	0	1	1	1	1	0F

IOTE: 1. “1”/“0”: Serial Data, “driven to HIGH”/“driven to LOW.”

BYTE 4: NUMBER OF COLUMN ADDRESSES

BYTE 4: NUMBER OF COLUMN ADDRESSES	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
–	–	–	–	–	–	–	–	–	–
8	0	0	0	0	1	0	0	0	08
9	0	0	0	0	1	0	0	1	09
10	0	0	0	0	1	0	1	0	0A
11	0	0	0	0	1	0	1	1	0B
12	0	0	0	0	1	1	0	0	0C
13	0	0	0	0	1	1	0	1	0D
14	0	0	0	0	1	1	1	0	0E
15	0	0	0	0	1	1	1	1	0F

BYTE 5: NUMBER OF MODULE BANKS

BYTE 5: NUMBER OF BANKS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
–	–	–	–	–	–	–	–	–	–

BYTE 6: MODULE DATA WIDTH

BYTE 6: MODULE DATA WIDTH	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
–	–	–	–	–	–	–	–	–	–
32	0	0	1	0	0	0	0	0	20
–	–	–	–	–	–	–	–	–	–
36	0	0	1	0	0	1	0	0	24
–	–	–	–	–	–	–	–	–	–
64	0	1	0	0	0	0	0	0	40
–	–	–	–	–	–	–	–	–	–
72	0	1	0	0	1	0	0	0	48
–	–	–	–	–	–	–	–	–	–

BYTE 7: MODULE DATA WIDTH (continued)

BYTE 7: MODULE DATA WIDTH (CONTINUED)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
0(+)	0	0	0	0	0	0	0	0	00
256(+)	0	0	0	0	0	0	0	1	01
512(+)	0	0	0	0	0	0	1	0	02
–	–	–	–	–	–	–	–	–	–

NOTE: 1. “1”/“0”: Serial Data, “driven to HIGH”/“driven to LOW.”

BYTE 8: MODULE VOLTAGE INTERFACE LEVELS

BYTE 8: MODULE VOLTAGE INTERFACE LEVELS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
5V/TTL	0	0	0	0	0	0	0	0	00
3.3V/LVTTL	0	0	0	0	0	0	0	1	01
–	–	–	–	–	–	–	–	–	–

BYTE 9: (DRAM) RAS# ACCESS TIME (^{t}RAC)

BYTE 9: RAS# ACCESS TIME (^{t}RAC)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
–	–	–	–	–	–	–	–	–	–
50ns	0	0	1	1	0	0	1	0	32
–	–	–	–	–	–	–	–	–	–
60ns	0	0	1	1	1	1	0	0	3C
–	–	–	–	–	–	–	–	–	–
70ns	0	1	0	0	0	1	1	0	46
–	–	–	–	–	–	–	–	–	–
80ns	0	1	0	1	0	0	0	0	50
–	–	–	–	–	–	–	–	–	–

BYTE 9: (SDRAM) CYCLE TIME, HIGHEST CAS LATENCY (^{t}CK)

BYTE 9:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	Cycle Time in ns				Cycle Time in tenth of a ns				
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 10: (DRAM) CAS# ACCESS TIME (^{t}CAC)

BYTE 10: CAS# ACCESS TIME (^{t}CAC)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
–	–	–	–	–	–	–	–	–	–
13ns	0	0	0	0	1	1	0	1	0D
14ns	0	0	0	0	1	1	1	0	0E
15ns	0	0	0	0	1	1	1	1	0F
–	–	–	–	–	–	–	–	–	–
25ns	0	0	0	1	1	0	0	1	19
–	–	–	–	–	–	–	–	–	–

BYTE 10: (SDRAM) ACCESS TIME FROM CLOCK, HIGHEST CAS LATENCY (^{t}AC)

BYTE 10:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	Access Time in ns				Access Time in tenth of a ns				
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

IOTE: 1. “1”/“0”: Serial Data, “driven to HIGH”/“driven to LOW.”

BYTE 11: MODULE CONFIGURATION TYPE

BYTE 11: MODULE CONFIGURATION TYPE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
None	0	0	0	0	0	0	0	0	00
Parity	0	0	0	0	0	0	0	1	01
ECC	0	0	0	0	0	0	1	0	02
–	–	–	–	–	–	–	–	–	–

BYTE 12: REFRESH RATE

BYTE 12: REFRESH RATE/TYPE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Normal (15.625µs)	0	0	0	0	0	0	0	0	00
–	–	–	–	–	–	–	–	–	–
Extended (4x)...62.5µs	0	0	0	0	0	1	0	0	04
Extended (8x)...125µs	0	0	0	0	0	1	0	1	05
–	–	–	–	–	–	–	–	–	–

BYTE 13: PRIMARY DRAM/SDRAM WIDTH

BYTE 13: PRIMARY DRAM/SDRAM WIDTH	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
4	0	0	0	0	0	1	0	0	04
8	0	0	0	0	1	0	0	0	08
16	0	0	0	1	0	0	0	0	10

BYTE 14: ERROR-CHECKING DRAM/SDRAM WIDTH

BYTE 14: ERROR CHECKING DRAM/SDRAM WIDTH	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
4	0	0	0	0	0	1	0	0	04
8	0	0	0	0	1	0	0	0	08
16	0	0	0	1	0	0	0	0	10

BYTE 15: (SDRAM) MIN CLOCK DELAY FOR BACK-TO-BACK RANDOM COL ADDRESSES

BYTE 15: MIN CLK DELAY, RANDOM COL ADDRESSES	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
–	–	–	–	–	–	–	–	–	–

NOTE: 1. “1”/“0”: Serial Data, “driven to HIGH”/“driven to LOW.”

BYTE 16: (SDRAM) BURST LENGTHS SUPPORTED

BYTE 16:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	Burst Length = Page	TBD	TBD	TBD	Burst Length = 8	Burst Length = 4	Burst Length = 2	Burst Length = 1	
	1 or 0	0	0	0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 17: (SDRAM) NUMBER OF BANKS ON SDRAM DEVICE

BYTE 17: NUMBER OF BANKS ON SDRAM DEVICE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
–	–	–	–	–	–	–	–	–	–

BYTE 18: (SDRAM) CAS LATENCY SUPPORTED

BYTE 18:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	TBD	CAS Latency = 7	CAS Latency = 6	CAS Latency = 5	CAS Latency = 4	CAS Latency = 3	CAS Latency = 2	CAS Latency = 1	
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 19: (SDRAM) CS LATENCY SUPPORTED

BYTE 19:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	TBD	CS Latency = 6	CS Latency = 5	CS Latency = 4	CS Latency = 3	CS Latency = 2	CS Latency = 1	CS Latency = 0	
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 20: (SDRAM) WE LATENCY SUPPORTED

BYTE 20:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	TBD	WE Latency = 6	WE Latency = 5	WE Latency = 4	WE Latency = 3	WE Latency = 2	WE Latency = 1	WE Latency = 0	
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 21: (SDRAM) VARIOUS MODULE ATTRIBUTES

BYTE 21:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	TBD	Redundant Row Addr	Differential Clock Input	Registered DQMB Inputs	Buffered DQMB Inputs	On-Card PLL (Clock)	Registered Addr/Ctrl *	Buffered Addr/Ctrl *	
	0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

* Address, RAS, CAS, WE, CKE, S0#-S3#

NOTE: 1. “1”/“0”: Serial Data, “driven to HIGH”/“driven to LOW.”

BYTE 22: (SDRAM) GENERAL DEVICE ATTRIBUTES

BYTE 22:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	TBD	TBD	Upper Vcc Tolerance: 0=10%,1=5%	Lower Vcc Tolerance: 0=10%,1=5%	Supports Write 1/Read Burst	Supports Precharge All	Supports Auto-Precharge	Supports Early RAS# Precharge	
	0	0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 23: (SDRAM) CYCLE TIME, 2ND-HIGHEST CAS LATENCY (^{t}CK)

BYTE 23:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	Cycle Time in ns				Cycle Time in tenth of a ns				
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 24: (SDRAM) ACCESS TIME FROM CLOCK, 2ND-HIGHEST CAS LATENCY (^{t}AC)

BYTE 24:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	Access Time in ns				Access Time in tenth of a ns				
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 25: (SDRAM) CYCLE TIME, 3RD-HIGHEST CAS LATENCY (^{t}CK)

BYTE 25:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	Cycle Time in ns				Cycle Time in tenth of a ns				
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 26: (SDRAM) ACCESS TIME FROM CLOCK, 3RD-HIGHEST CAS LATENCY (^{t}AC)

BYTE 26:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	Access Time in ns				Access Time in tenth of a ns				
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 27: (SDRAM) MIN ROW PRECHARGE TIME (^{t}RP)

BYTE 27: MIN ROW PRECHARGE TIME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
1ns	0	0	0	0	0	0	0	1	01
–	–	–	–	–	–	–	–	–	–
30ns	0	0	0	1	1	1	1	0	1E
–	–	–	–	–	–	–	–	–	–

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

BYTE 28: (SDRAM) MIN ROW ACTIVE TO ROW ACTIVE (^{t}RRD)

BYTE 28: MIN ROW ACTIVE TO ROW ACTIVE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
1ns	0	0	0	0	0	0	0	1	01
–	–	–	–	–	–	–	–	–	–
30ns	0	0	0	1	1	1	1	0	1E
–	–	–	–	–	–	–	–	–	–

BYTE 29: (SDRAM) MIN RAS TO CAS DELAY (^{t}RCD)

BYTE 29: MIN RAS TO CAS DELAY	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
1ns	0	0	0	0	0	0	0	1	01
–	–	–	–	–	–	–	–	–	–
30ns	0	0	0	1	1	1	1	0	1E
–	–	–	–	–	–	–	–	–	–

BYTE 30: (SDRAM) MIN RAS PULSE WIDTH (^{t}RAS)

BYTE 30: MIN RAS PULSE WIDTH	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Undefined	0	0	0	0	0	0	0	0	00
1ns	0	0	0	0	0	0	0	1	01
–	–	–	–	–	–	–	–	–	–
60ns	0	0	1	1	1	1	0	0	3C
–	–	–	–	–	–	–	–	–	–

BYTE 31: (SDRAM) MODULE BANK DENSITY

BYTE 31:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
Size	512MByte	256MByte	128MByte	64MByte	32MByte	16MByte	8MByte	4MByte	
Y/N	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 32: (SDRAM) COMMAND AND ADDRESS SETUP TIME (^{t}AS, ^{t}CMS)

BYTE 32:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	Positive/ Negative	Setup Time in ns			Setup Time in tenth of a ns				
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

IOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

BYTE 33: (SDRAM) COMMAND AND ADDRESS HOLD TIME (^{t}AH, ^{t}CMH)

BYTE 33:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	Positive/ Negative	Hold Time in ns			Hold Time in tenth of a ns				
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 34: (SDRAM) DATA SIGNAL INPUT SETUP TIME (^{t}DS)

BYTE 34:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	Positive/ Negative	Setup Time in ns			Setup Time in tenth of a ns				
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 35: (SDRAM) DATA SIGNAL INPUT HOLD TIME (^{t}DH)

BYTE 35:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	Positive/ Negative	Hold Time in ns			Hold Time in tenth of a ns				
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

BYTE 126: (SDRAM) SYSTEM FREQUENCY

BYTE 126: SYSTEM FREQUENCY	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
66 MHz	0	1	1	0	0	1	1	0	66
100 MHz	0	1	1	0	0	1	0	0	64
–	–	–	–	–	–	–	–	–	–

BYTE 127: (SDRAM) COMPONENT AND CLOCK DETAIL

BYTE 127:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
	CLK0	CLK1	CLK2	CLK3	Junction Temp	CAS Latency = 3	Cas Latency = 2	Intel "Concurrent AP"	
	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

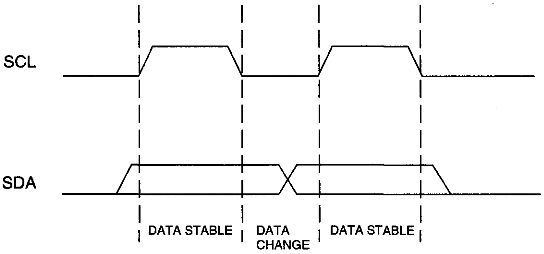


Figure 1
DATA VALIDITY

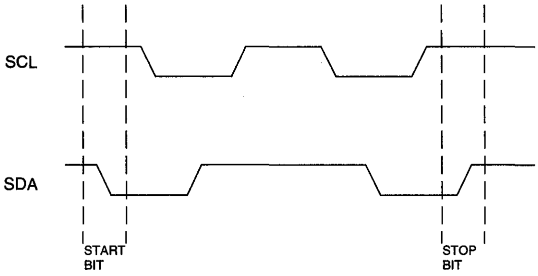


Figure 2
DEFINITION OF START AND STOP

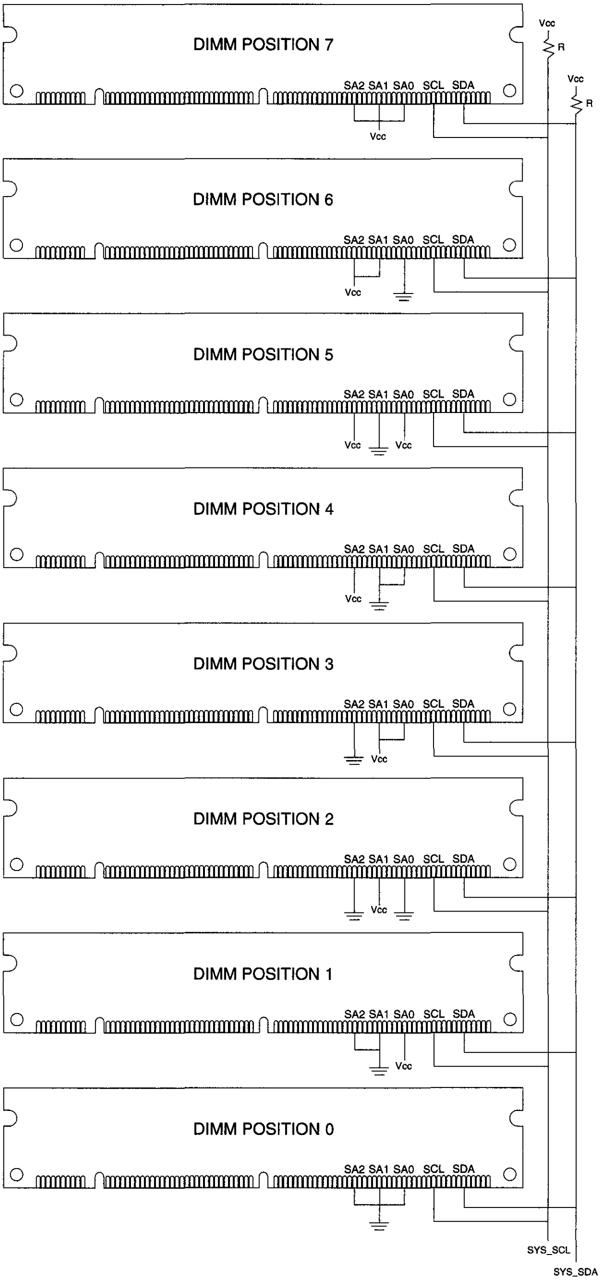


Figure 3
SPD BLOCK DIAGRAM (COMMON CLOCK/COMMON DATA)

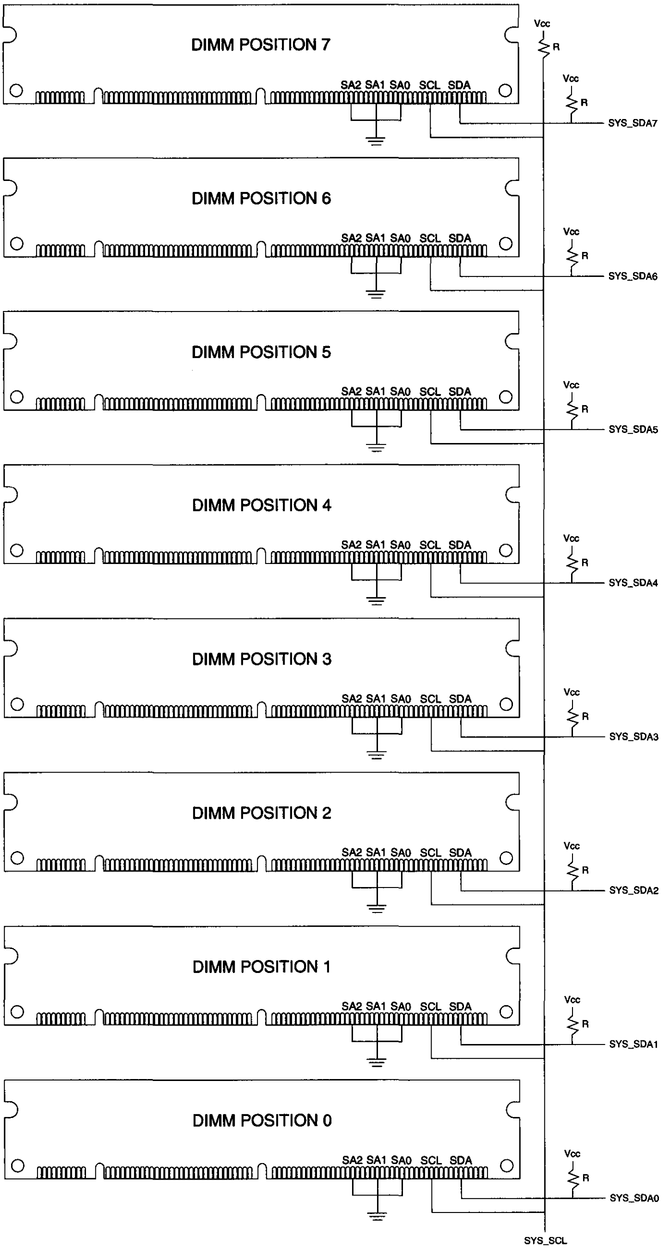


Figure 4
SPD BLOCK DIAGRAM (COMMON CLOCK/SEPARATE DATA)

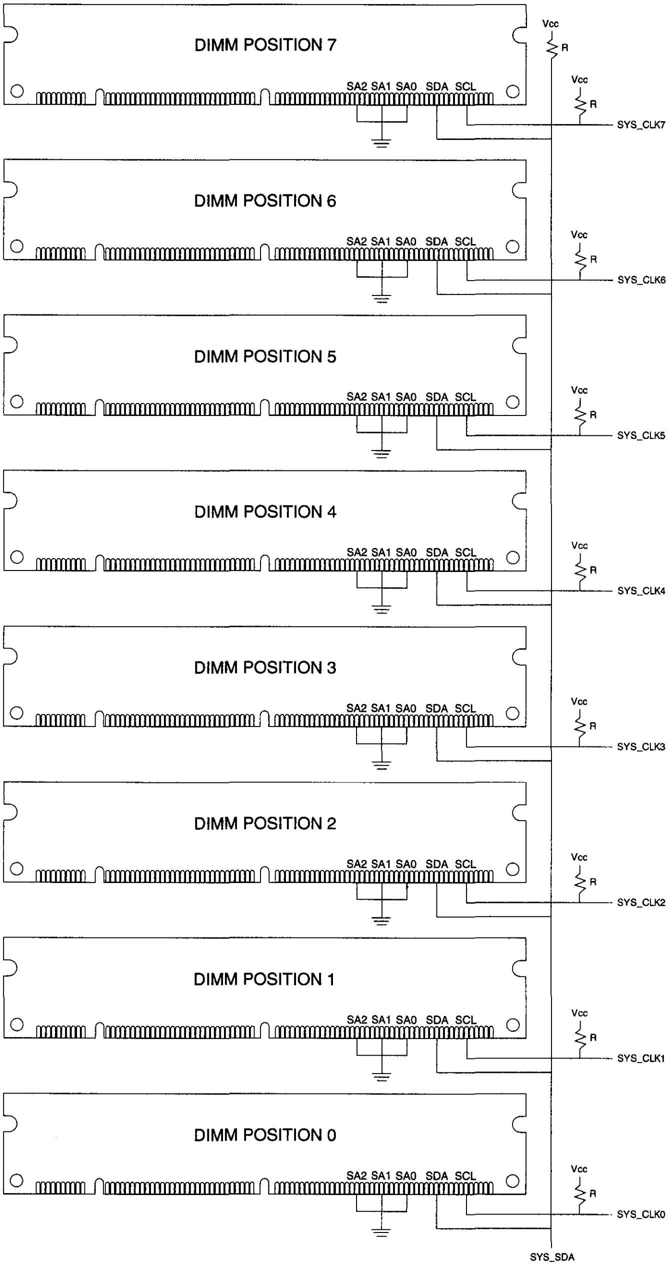


Figure 5
SPD BLOCK DIAGRAM (COMMON DATA/SEPARATE CLOCK)

TECHNICAL NOTE

1 MEG x 16 DRAM POWER SAVINGS: 1K vs. 4K ROW REFRESH

This article was originally published in 1996.

INTRODUCTION

The 1 Meg x 16 DRAM is offered as a 1K-addressable device (1,024 addressable rows and 1,024 addressable columns, i.e. symmetrical). Some DRAM manufacturers are also offering the 1 Meg x 16 DRAM as a 4K-addressable device (4,096 addressable rows and 256 addressable columns, i.e. asymmetrical). The impetus behind the 1K address offering is the requirement for compatibility support. Since a 1 Meg x 16 DRAM replaces four 1 Meg x 4 DRAMs, an addressing scheme that is the same as the 1 Meg x 4 DRAM is most desirable. With the 1 Meg x 4 being a symmetrical, 1K-addressable architecture, the 1K-addressable version of the 1 Meg x 16 DRAM is able to provide direct addressing compatibility when replacing 1 Meg x 4 DRAMs.

The perceived disadvantage in maintaining the 1K addressability on the 1 Meg x 16 DRAM is the increase in current consumption during each row access, i.e. READ or WRITE cycles, and this is the reason behind offering the 4K-address option. With more rows and fewer columns, a 4K-address version will require less current than a 1K-address version each time the row is opened.

POWER SAVINGS

The 1K-address version of the 1 Meg x 16 DRAM directly replacing four 1 Meg x 4 DRAMs reduces the overall DRAM current consumption, which results in significant power savings. However, a 1K-address version of the 1 Meg x 16 DRAM specifies a maximum Icc in the neighborhood of 150mA for a READ or WRITE cycle, *at the minimum cycle rate* for a -7 (see Table 1), whereas the 4K-address version of the 1 Meg x 16 DRAM specifies a maximum Icc in the neighborhood of 80mA for a READ or WRITE cycle (Table 1).

Table 1
1 MEG x 16 Icc LIMITS AT ^{t}RC (MIN)

CYCLE	70ns Icc LIMIT 1K ADDRESS	 4K ADDRESS
READ/WRITE	140mA	80mA
PAGE MODE	80mA	80mA
REFRESH	140mA	80mA

Power-sensitive systems are always looking for any additional reduction in power consumption. It would appear that using a 4K-address version of the 1 Meg x 16 DRAM rather than a 1K-address version of the 1 Meg x 16 DRAM would further reduce power consumption by approximately 40 percent! Let's evaluate the 1K- and 4K-address versions of the 1 Meg x 16 DRAM to determine which version actually provides the best power savings.

ACTIVE POWER DEMAND

As previously mentioned, the 4K-address version of the 1 Meg x 16 shows an approximate 40 percent reduction in current consumption over a 1K-address version while in the "active mode" (refresh, READ or WRITE cycle). The cost to change addressing schemes seems to be a reasonable penalty to significantly reduce current consumption. However, this 40 percent power savings is generally not obtainable in most system applications.

First, the 40 percent current delta between the 1K- and 4K-address versions only applies to single READ/WRITE cycles that cycle at the minimum cycle rate. If the 1K- and 4K-address versions are cycling at slower cycle rates, which is typically the case, the difference in current consumption is much smaller, generally in the 10 to 20 percent range, not 40 percent (see Figure 1).

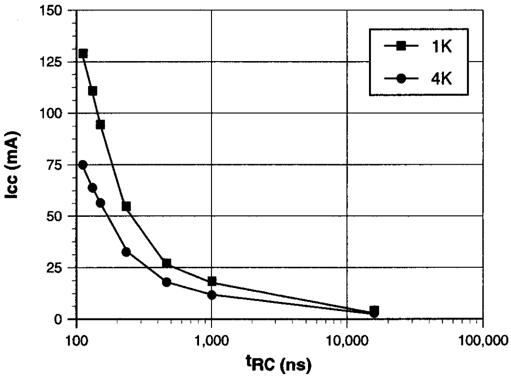


Figure 1
READ/WRITE Icc COMPARISON BETWEEN 1K AND 4K 1 MEG x 16 DRAM

Additionally, DRAM accesses tend to be PAGE MODE accesses. The current consumed during a page access is similar between a 1K-address and a 4K-address 1 Meg x 16 DRAM (see Table 1). There is no power savings with a 4K-address 1 Meg x 16 during PAGE accesses. Hence, the average power consumed by 1K-address 1 Meg x 16 during the active time is much closer to that of the 4K-address 1 Meg x 16.

For example, consider a -7, 1 Meg x 16 DRAM memory system being accessed by an initial READ cycle (i.e. page opened) and followed by three page accesses and then the page closed, all at the minimum rates permissible. The 4K-address 1 Meg x 16 would provide only a 15 percent savings in current consumption over the use of a 1K-address 1 Meg x 16, and not the 40 percent as first expected:

1K address:
140mA per 130ns + 3(80mA per 45ns) = 380ns per 265ns

4K address:
80mA per 130ns + 3(80mA per 45ns) = 320ns per 265ns

Unless the majority of memory accesses are single READs and WRITEs, at the minimum cycle rate, the 4K-address 1 Meg x 16 DRAM offers only a small power savings over a 1K-address 1 Meg x 16 DRAM during most memory accesses.

REFRESH REQUIREMENTS

An often overlooked issue when choosing between a 1K- or a 4K-addressed 1 Meg x 16 DRAM is the refresh requirements. There are two ways to view the refresh issue. On the one hand, the standard refresh period for a 1K-addressed 1 Meg x 16 DRAM is 16ms, while a 4K-addressed 1 Meg x 16 DRAM requires 64ms (the industry defacto standard refresh rate is 15.625µs per row). Once a row on the 1K-address version has been refreshed, it will be refreshed again 16ms later, at the 15.625µs per row distributed rate. Once a row on the 4K-address version has been refreshed, it will not be refreshed again until 64ms later at the 15.625µs per row distributed rate. The 4K-address version requires four times the refresh period. This additional refresh time demands either a more expensive process to build the 4K-addressed version, or that the 4K-addressed version will not provide near the yield and resistance to soft errors if manufactured on the same process as the 1K-refresh version.

On the other hand, any application that is concerned with power savings should use the extended refresh version. Both the 1K and 4K extended refresh 1 Meg x 16 versions have a 128ms refresh period (industry defacto standard). However, since the 1K refresh version has one-fourth the number of rows, the device requires a refresh cycle once every 125µs, whereas the 4K refresh version requires a refresh cycle once every 32.5µs, or four times as often as the 1K refresh version. So even though the 1K extended refresh version specifies a 40 percent higher Icc than the 4K extended refresh version at the minimum cycle rate, the 1K extended refresh version requires 75 percent fewer refresh cycles than the 4K extended refresh version. Since the current draw specified for a refresh cycle is similar to that of the READ/WRITE cycles, it can easily be deduced that a 1K extended refresh version uses over 50 percent less current than a 4K extended refresh version when refreshing:

1K address:
140mA per 125ns = 140mA per 125ns

4K address:
80mA per 32.5ns = 320mA per 125ns

This concept is especially important in battery-backed applications. While the system is in the active mode, the DRAM memory generally consumes only a small portion of the overall power consumption, generally in the 5 to 10 percent range (see Figure 2). Even a 50 percent reduction in DRAM power consumption translates to a system power savings of only 2 to 6 percent, which is hardly enough to justify redesigning the addressing scheme. However, when a system is in a battery-backed or data retention mode, the DRAM memory will account for approximately 50 to 80 percent of the overall power consumption (see Figure 2). A DRAM power savings of 50 percent by the 1K extended refresh version translates to a system power savings of 25 to 40 percent when in the battery-backed mode. Thus, the 1K extended refresh version actually reduces power usage when data retention is a major factor in battery life.

PUTTING IT TOGETHER

Combining the active and refresh power requirements tells the whole story on which version of the 1 Meg x 16 DRAM provides the best power savings. It can be argued that the data retention mode is most important to systems that require power management. Without question the 1K refresh version of the 1 Meg x 16 DRAM is the best choice for maximum power savings.

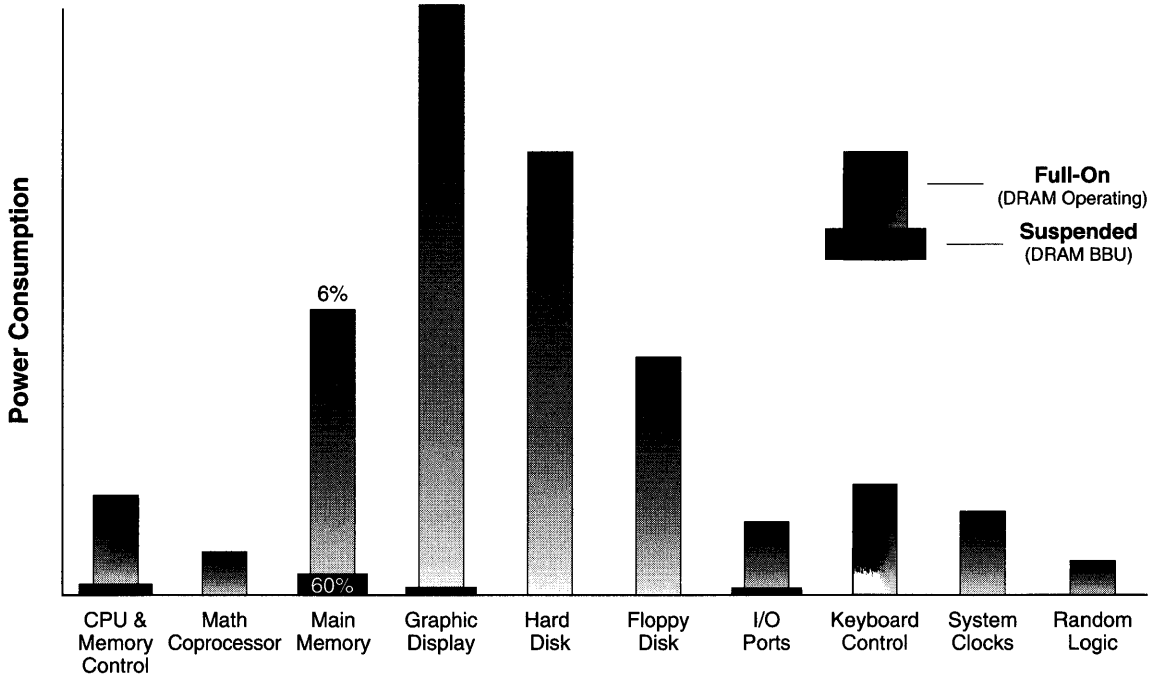
It is also important to realize that systems have a power budget during the active mode as well (when performing READs, WRITEs and refresh cycles). Generally, PAGE MODE accesses do not provide either the 1K refresh or the 4K refresh 1 Meg x 16 DRAM an advantage in power savings. The version that provides the lower current consumption will be dependent on the system application and how the refresh cycles relate to single READ/WRITE cycles.

In whichever version provides the higher active current consumption, the apparently large delta is greatly reduced when averaged over the whole time of the DRAM. (Figure 3 depicts the relationship in determining whether the 1K refresh version of the 1 Meg x 16 DRAM consumes less or more current than the 4K refresh version in the overall system application during the active mode).

For example, in Figure 3, with single READ and WRITE cycles performed at the minimum cycle rate and occurring 5 percent of the DRAM on time (DRAM in Standby/Refresh 95 percent of the on time), this would be the absolute worst-case scenario when cache is used. The 1K extended refresh version of the 1 Meg x 16 DRAM will add less than a 0.2 percent increase in system power usage over the 4K extended refresh version of the 1 Meg x 16 DRAM while in the active mode. This slight power savings of the 4K-address version during the active mode is greatly diminished with the addition of the PAGE MODE cycles factored in for the overall average power.

SUMMARY

When choosing between a 1K refresh or a 4K refresh version of the 1 Meg x 16 DRAM, a first glance would favor the 4K refresh version to obtain significant power savings. In all but a few limited applications, the power savings of the 4K refresh version of the 1 Meg x 16 DRAM is greatly minimized. In most applications, the risks and redesign efforts associated with using the 4K refresh version of the 1 Meg x 16 DRAM do not warrant its use. Additionally, any memory system requiring data retention mode will receive a significant power savings when employing the 1K refresh version of the 1 Meg x 16 DRAM.



Source: Intel Corp.

Figure 2
PC POWER DEMAND

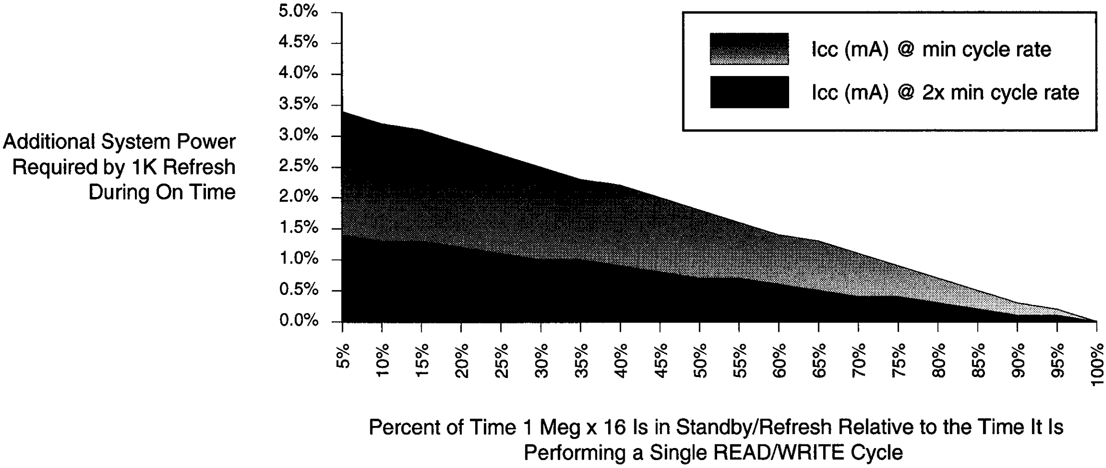


Figure 3
POWER SAVINGS OF 4K REFRESH 1 MEG x 16 OVER A 1K REFRESH 1 MEG x 16

TECHNICAL NOTE

MAXIMIZING DRAM VALID DATA-OUT WINDOW

This article was originally published in 1996.

INTRODUCTION

As data rates for the PC data bus increase, device specifications continue to become more critical. DRAMs are no exception, with today's data bus rates in the 50, 60 and 66 MHz range. The valid data-out window has been identified as one of the more critical system constraints on DRAM performance. This article will investigate the concern and provide some relief for designing around this parameter.

DATA-OUT WINDOW

Valid data-out window constraints apply equally to Fast Page Mode (FPM), Extended Data-Out (EDO) and Synchronous DRAMs (SDRAMs), with the only difference being that FPM DRAMs use ^{t}OFF rather than ^{t}COH for data hold time. A matrix of DRAM speed versus data bus rates (shown in Table 1) helps identify which scenarios result in narrow valid data-out windows (of interest within the scope of this article).

EDO DRAMs come from the same die as the FPM DRAM. The output delays (^{t}CAC) are also similar. In evaluating the valid data-out window, the SDRAM will be used (although the example equally applies to FPM and EDO DRAMs by substituting ^{t}CAC for ^{t}AC).

Evaluation of the -12 SDRAM specification indicates a valid data-out window of 8ns when operating with a 66 MHz data bus:

Data-Out Window = ^{t}CK - ^{t}CAC/^{t}AC + ^{t}COH
Data-Out Window = 15ns - 10ns + 3ns
Data-Out Window = 8ns

Although an 8ns window is reasonably sufficient to design with at 66 MHz, system designers prefer a slightly wider data-out window. Data-out windows of 10ns or more are most desirable and are considered fairly easy to work with. There are those who believe that a guaranteed data-out window of 8ns derived from the data sheet would suffice. However, the issue is compounded when system designers add guardband to the DRAM data sheet's worst-case numbers. Thus, the 8ns specified data-out window could be reduced to 6ns or 7ns—clearly a difficult task. System engineers that subscribe to this school of thinking are only robbing their designs of available performance.

Fortunately for high-performance designs, there is another school of thought that has become a PC industry trend. Some system designers design slightly beyond the

Table 1
VALID DATA-OUT WINDOWS

	FPM/EDO			SDRAM		
FREQUENCY	**50 MHz**	**60 MHz**	**66 MHz**	**50 MHz**	**60 MHz**	**66 MHz**
^{t}CK	20ns	16.7ns	15ns	20ns	16.7ns	15ns
^{t}CAC -7	20ns	→	→	n/a	n/a	n/a
^{t}COH -7	3ns	→	→	n/a	n/a	n/a
^{t}CAC -6/^{t}AC[3] -12	15ns	→	→	10ns	→	→
^{t}COH -6/^{t}COH -12	3ns	→	→	3ns	→	→
^{t}CAC -5/^{t}AC[3] -10	13ns	→	→	9ns	→	→
^{t}COH -5/^{t}COH -10	3ns	→	→	3ns	→	→
Valid Data-Out Windows -7	3ns[1]	0ns[1]	0ns[1]	n/a	n/a	n/a
Valid Data-Out Windows -6/-12	8ns[2]	4.4ns[1]	3ns[1]	13ns	9.7ns[2]	8ns[2]
Valid Data-Out Windows -5/-10	10ns	6.7ns[1]	6ns[1]	14ns	10.7ns	9ns[2]

NOTE: 1 = Requires an additional wait state for data-out.
2 = Valid data-out windows less than 10ns thought to require a wait state for data-out or restricted loads.
3 = CAS latency = 2.

actual data sheet specifications. They have come to realize that the DRAM memory is tested at the worst-case extremes and with guardbands by the supplier to ensure that the data sheet specifications will always be met. Additionally, they realize that the DRAM operating ranges are typically more restrictive than the PC system requirements (see Figure 1). At a minimum, a memory design should at least utilize the DRAM data sheet specification numbers and not restrict the design with extra guardbands.

SDRAM DATA-OUT WINDOW

Actual measured values for the SDRAM's data-out window are listed in Table 2 and graphed in Figure 2. Note that although the SDRAM data sheet specifications indicate an 8ns to 9ns data-out window, the measured data-out window is always 14ns or more over the worst-case extremes. Figure 3 depicts why the specified data-out window is shorter and the actual data-out window remains much greater. The two parameters that comprise the data-out

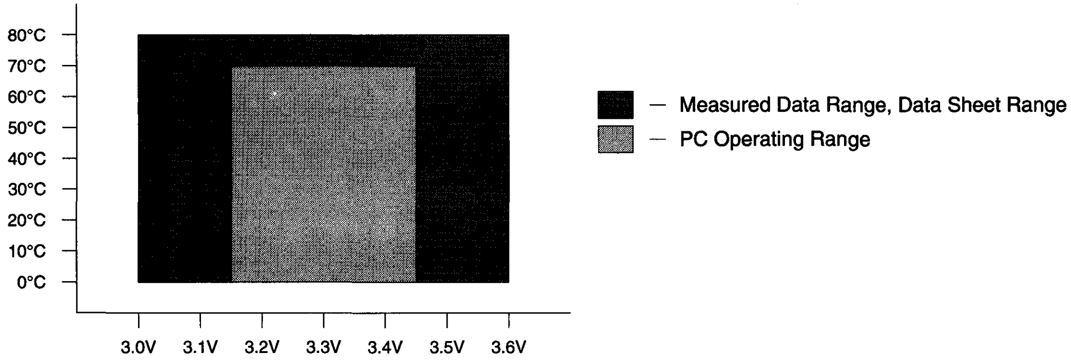


Figure 1
OPERATING CONDITIONS

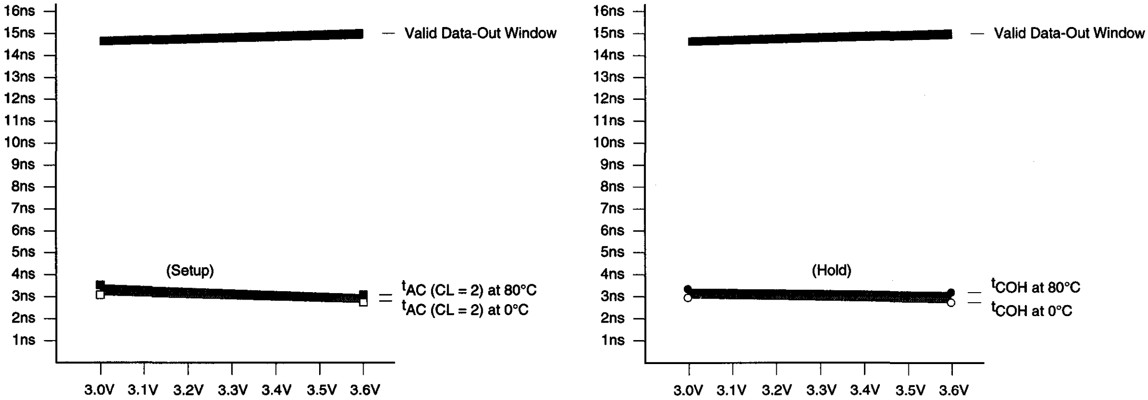


Figure 2
SDRAM MEASURED VALUES

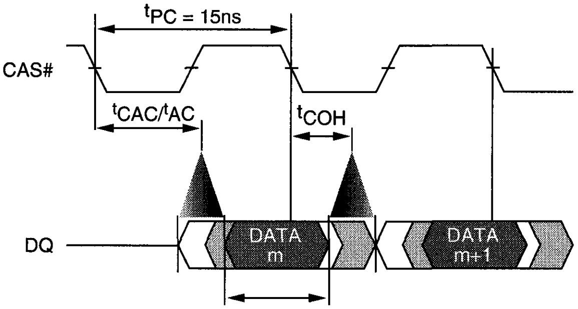


Figure 3
DATA-OUT WINDOW

window (^{t}AC and ^{t}COH) inversely track each other over the operating extremes (changes in voltage and temperature), but the data sheet specifications only specify the worst-case limit for each parameter. Thus, the two worst-case values will never occur at the same time. That is, they both speed up or both slow down over the various extremes, as seen in Figure 4. Since one is a setup (^{t}CAC/^{t}AC) and one a hold (^{t}COH) to the next stage, when one improves the other gets worse, and vice versa, as shown in Figure 3.

Although the actual data-out window is greater than 14ns and not the 8ns to 9ns implied by the data sheet, something in between the two generally has to be used. The practical data-out window for the SDRAM in a typical PC system would be 10ns to 11ns, as depicted in Figure 5. A safe guardband would be 7ns for ^{t}CAC and 3ns for ^{t}COH for a valid data-out window of 11ns (15ns - 7ns + 3ns). It is important to understand that the difference between the actual usable values and the specified values comes from the fact that the DRAM specifications require guardbands prior to shipping. The specifications with which the devices are shipped are guaranteed over a wider range than those with which PCs operate (see Figure 1).

Table 2
12ns SDRAM DATA-OUT WINDOW

		PARAMETER VALUES		DATA-OUT WINDOW
	TEST CONDITIONS	^{t}AC (ns)	^{t}COH (ns)	(15ns - ^{t}AC + ^{t}COH)
-12 Specification Limits	0°C to 70°C, 3V to 3.6V	10	3	8
Measured Data	0°C, 3.6V	2.8	2.8	15
	0°C, 3V	3.1	2.95	14.85
	80°C, 3.6V	3.1	3.2	15.1
	80°C, 3V	3.6	3.4	14.8

SUMMARY

Designing DRAMs in high-speed data bus systems is not as difficult as some first thought. For example, the minimum valid data-out window that can safely be designed for the SDRAM in a 66 MHz data bus is 8ns and no less. Anything less for the data-out window is a waste of device capability. Additionally, the SDRAM is more than capable of providing a valid data-out window in the 10ns to 11ns range for a PC with a 66 MHz data bus. Similar exercises performed on EDO or FPM DRAMs also will reveal wider valid data-out windows.

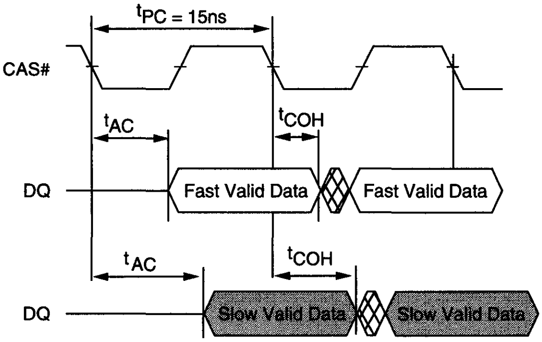


Figure 4
ACTUAL DATA-OUT WINDOW

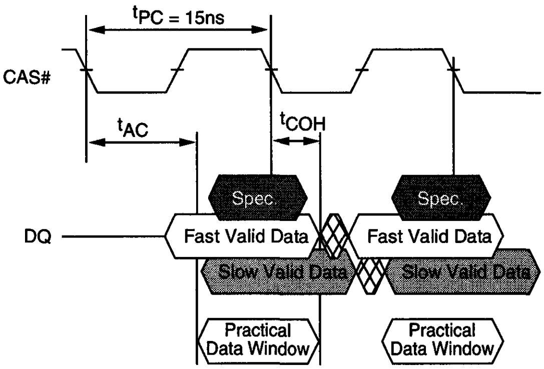


Figure 5
OPTIMUM DATA-OUT WINDOW

TECHNICAL NOTE

DRAM MODULE MEAN TIME BETWEEN FAILURES (MTBF)

his article was originally published in 1997.

NTRODUCTION

Prior to the release of this technical note, a DRAM memory nodule user would have had to spend a fair amount of ffort to determine a particular module's mean time beween failure (MTBF). First, the user would have to obtain he Reliability Monitors for the DRAM components being mployed on the particular module. Then, the individual ailure-in-time (FIT) rates would have to be calculated for ach device, and the FITs summarized to arrive at the nodule's MTBF.

This technical note provides MTBF for the DRAM nodules that are based on 16Mb DRAMs, which saves he user from having to calculate the MTBF. Here, we eference the 16Mb DRAM Reliability Monitor (D42 die, ev. 11/20/96) to obtain the DRAM's hard and soft error ates. Additionally, Technical Note TN-04-28, "DRAM Soft rror Rate Calculations," was followed when calculating he DRAM's soft error rates. Reviewing Technical Note TN-4-28 is an excellent primer for understanding DRAM soft rror rate calculations.

MODULE MEAN TIME BETWEEN FAILURES (MTBF)

Both the calculated hard error rate (HER) MTBF and the soft error rates (SER) MTBF have been summarized in Table 1. The HER MTBF is a first-order number as it is based soley on the DRAM's HER. A module's HER MTBF should also include failures resulting from PCB defects, DRAM mounting errors, etc. However, since these factors are an order of magnitude less than a DRAM's HER, they were ignored.

The SER MTBF is listed twice. The first, SER#1 MTBF, is stated in the standard format: the DRAM is strictly cycling at the standard refresh rate (15.625µs per row) and is not being accessed for READs or WRITES; i.e., 100 percent refresh time and 0 percent active time. The second, SER#2 MTBF, is stated for a PC which has both L1 cache and L2 cache and is being used continuously: the DRAM is cycling at the standard refresh rate 96 percent of the time and is being accessed by the CPU for READs or WRITEs 4 percent of the time; i.e., 96 percent refresh time and 4 percent active time.

Table 1
DRAM MODULE MEAN TIME BETWEEN FAILURE

MODULE PART NUMBER	HARD ERROR RATE MTBF	SOFT ERROR RATE#1 MTBF @ 100% REFRESH	SOFT ERROR RATE#2 MTBF @ 96% REFRESH
MT8D432	250 years	53 years	35 years
MT16D832	125 years	26 years	22 years
MT12D436	167 years	35 years	24 years
MT24D836	83 years	18 years	14 years
MT2D(T)132	1,001 years	211 years	142 years
MT4D232	501 years	106 years	71 years
MT4D(T)232D	501 years	106 years	86 years
MT4LD(T)164A	713 years	106 years	71 years
MT4LDT164H	713 years	106 years	71 years
MT8LD264A	357 years	53 years	35 years
MT8LDT264H	357 years	53 years	35 years
MT16LD464A	178 years	26 years	18 years
MT9LD272	<317 years*	47 years	31 years
MT9LD272A	317 years	47 years	31 years
MT18LD472	<159 years*	23 years	16 years
MT18LD472A	159 years	23 years	16 years

Buffers reduce Hard Error Rate MTBF slightly.

TECHNICAL NOTE

THE BEST GRAPHICS SOLUTION FOR 66 MHz: SGRAM OR EDO DRAM?

This article was originally published in 1996.

INTRODUCTION

With the introduction of "fast" 256K x 16 EDO DRAMs comes added confusion about the best memory choice for mainstream graphics systems. While the high-yielding SGRAM is an attractive new solution for graphics controllers and can reliably perform at the 66 MHz level and beyond, the 66 MHz 256K x 16 DRAM—despite being pushed to the limit—remains a popular choice. This article discusses some of the advantages and disadvantages of both technologies.

THE ABSENCE OF AN INDUSTRY STANDARD

To begin, it is important to note the actual timing needs of a 66 MHz system. To run at 66 MHz, a system must have a cycle time of 15ns (^{t}PC). ^{t}PC is the CAS# cycle time comprised of ^{t}CP (HIGH time) and ^{t}CAS (LOW time). These parameters are usually not of concern for the graphics controller that may latch data on the falling edge of CAS#; but for DRAMs, these timings are critical for proper function. The absence of industry-standard timing for the 256K x 16, however, means that these parameters vary based on each vendor's internal architecture. Micron recommends overcoming this challenge by having the controller designed with the duty cycle programmable.

The SGRAM does *not* have a ^{t}PC, but does have a ^{t}CK, which is the clock cycle time input with a duty cycle specified as 50 percent by all manufacturers. For the SGRAM, 66 MHz is also the lowest speed available and marks the beginning of this new technology, not the end. The DRAM, on the other hand, requires a bit of a stretch—an asynchronous, premium part—to achieve the 15ns cycle time.

The next difference to consider is leadoff latency (delay for the first data access). For the 256K x 16, the first access is longer than subsequent accesses within the same row address due to the precharge time of the row. After the first access is achieved, both the DRAM and the SGRAM can perform with single clock-cycle-to-data; however, the SGRAM has a leadoff latency of six clocks (CAS# latency of three), while the DRAM requires only three clocks for the first data. Figure 1 shows ^{t}RAC needs to be a minimum of 45ns to achieve the three-clock leadoff. Initial accesses for DRAMs vary by manufacturer and range from 35ns to 40ns. Granted, the 35ns is better than 40ns, but if you don't really need the extra 5ns, why pay for the yield loss associated with too tight of a parameter?

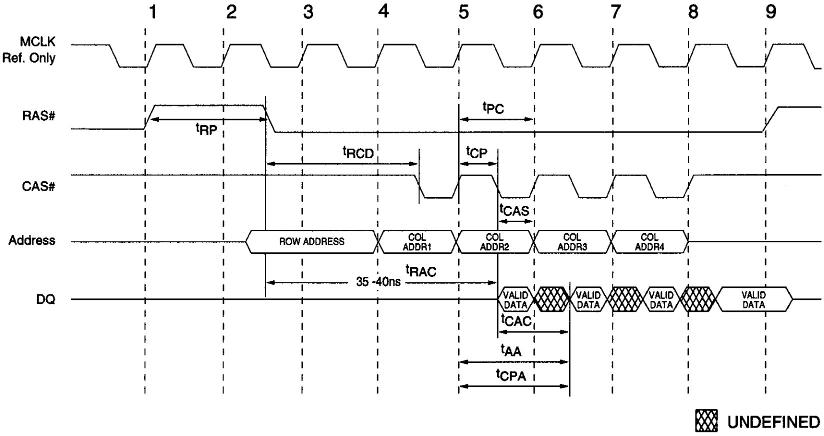


Figure 1
66 MHz READ CRITICAL TIMING PARAMETERS

On the other hand, while the DRAM receives a page-miss penalty of four to five clocks (precharge time and leadoff latency), the SGRAM can enjoy a continuous stream of data by hiding the precharge in between the two internal banks. Furthermore, the SGRAM's ability to respond as bus speeds increase is preferable to the DRAM, which becomes increasingly difficult to design for similar performance and difficult for a manufacturer to yield in volume. A lower-yielding part converts directly into higher cost.

LIMITING PARAMETERS WHICH VARY BY DRAM MANUFACTURER

While ^{t}PC may be the most critical parameter for cycling at 66 MHz, several other parameters are also pertinent to the DRAM interface. For proper cycling, the column address needs to be presented on the same clock edge that CAS# is brought HIGH, as shown in Figure 1. This will ensure that the address is latched and that ^{t}AA will not be violated. However, this brings ^{t}CPA into the equation, as well as ^{t}CAC. ^{t}CPA and ^{t}AA will be measured from the same clock edge, while ^{t}CAC will be measured from the next falling edge of CAS#. Assuming a 50 percent duty cycle of CAS#, ^{t}AA, ^{t}CPA or ^{t}CAC could all be limiting parameters for data-out, depending upon the manufacturer. If ^{t}CP is "cheated" by going shorter (asymmetric duty cycle), ^{t}CPA or ^{t}AA will limit data. Regardless of which parameter limits data being driven, the valid data window will be extremely short, as shown in Figure 2. This may not be of concern for 2MB (4-part) systems with lightly loaded busses, but for 4MB (8-part) systems, the extra load becomes an issue. Two SGRAMs provide a 64-bit bus with 2MB, while a 4MB system is only four parts, which reduces the load compared to EDO. Also, since the SGRAM's data window is longer and synchronized to the clock (as shown in Figure 3), the data-out is less susceptible to loading skew.

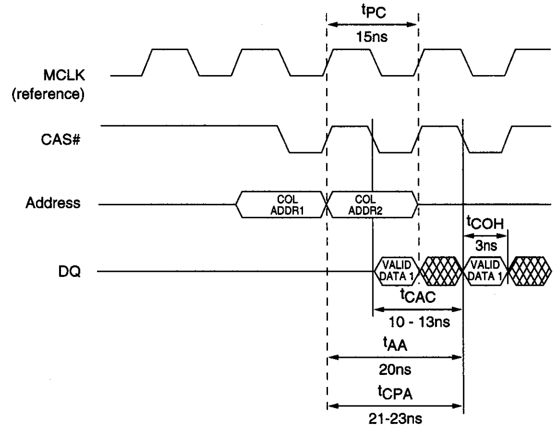


Figure 2
EDO DRAM VALID DATA-OUT WINDOW

The addition of dual banks as well as BLOCK WRITE (writes the same data to eight different locations in memory simultaneously) increases performance. While a few articles have stated that BLOCK WRITE is not needed in 3D applications, all graphics applications still need to do 2D acceleration, and BLOCK WRITE has been proven to enhance 2D performance. One of the uses of BLOCK WRITE in 3D is fast screen clears. If the two banks of the SGRAM are utilized to their full potential, along with BLOCK WRITE, the SGRAM will clearly outperform the DRAM at the same bus speed.

SUMMARY

Because a definitive memory choice for the evolving graphics market running at 66 MHz has yet to be made, Micron offers both 40ns 256K x 16 EDO DRAMs as well as SGRAMs to satisfy customers' needs. EDO is a familiar memory that performs well up to 66 MHz, but can it outperform the SGRAM at the same frequency? With DRAM technology approaching its asynchronous limits, SGRAM is an option which demands evaluation. Not only do SGRAMs perform reliably at the 66 MHz-level and beyond, but they are manufactured by virtually all of the major DRAM vendors and are therefore readily available. In addition, as 3D becomes the driving force for graphics, faster bus speeds needed to sustain bandwidth will require synchronous memory — which has common logic with the main memory interface of Intel's Accelerated Graphics Port (AGP) architecture. Consequently, the popularity of EDO's simple controller design for current systems must be weighed against the SGRAM's potential to offer the highest performance. As the market continues to evolve, Micron will work closely with our customers to chart the future path to 83 MHz, 100 MHz and beyond.

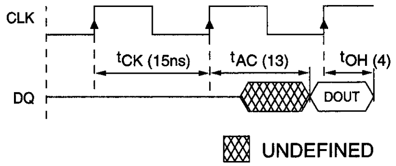


Figure 3
SGRAM VALID DATA-OUT WINDOW

TECHNICAL NOTE

DECREMENT BURSTING WITH THE SGRAM

his article was originally published in 1995.

NTRODUCTION

Decrement bursting is a useful operation in many graphcs applications, especially in a GUI environment. Any raphics memory device that facilitates this operation, such s the synchronous graphics RAM (SGRAM), provides ystem-level benefits including reduced design complexity nd increased performance.

There are several methods that can be used to achieve ull-speed decrement bursting in synchronous DRAM SDRAM)/SGRAM-based graphics memory implementaons. This note describes the various methods and the radeoffs associated with each.

DECREMENT BURSTING

There are several instances in graphics applications where is desired to access a series of pixels (in a line on the isplay) from right to left. This might occur when performng overlapping BITBLTs or when scrolling text horizonally within a window.

Pixels are typically mapped in memory such that moving rom right to left in a section of a line on the screen means moving from a column location with a higher address in a ow in memory to a column with a lower address. To perform the above operation requires the ability to burst sequentially from a starting column address to decreasing (or decrementing) column addresses within a row.

EXPLICIT COMMAND

One vendor of SDRAMs in a graphics configuration (256K x 16) has created an explicit command mode to accomplish decrement bursting; however, this approach has several drawbacks. One drawback is that this command mode is additional to the defined command set for SDRAMs/SGRAMs. This means that both the controller and the memory devices must contain additional logic to support the new command mode. Another drawback is that the new command must be executed every time there is a change in direction (from incrementing to decrementing, and vice versa). This results in additional overhead in the form of Mode Register accesses. In addition, this new command mode is not available from other vendors.

Alternatively, the methods described below can be achieved on any SDRAM/SGRAM with a pipelined architecture, which includes all SGRAMs and all SDRAMs tailored for graphics applications. In addition, these methods use the existing command sets defined for SDRAMs/SGRAMs and allow for operation at the maximum burst rate of the device.

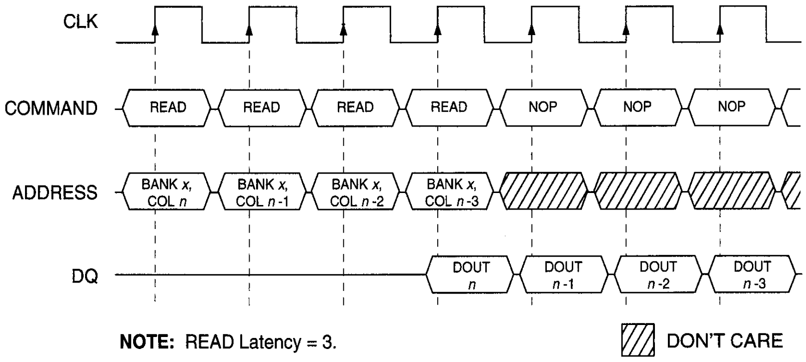


Figure 1
DECREMENT BURSTING – NEW COLUMN ADDRESS EVERY CYCLE

RANDOM COLUMN ACCESS

SDRAMs/SGRAMs with a pipelined architecture can accept a new READ or WRITE command and column address on each cycle during a burst access within a page. This provides the capability to sequentially access incrementing or decrementing column addresses, as well as to randomly access column locations within a page at the maximum burst rate of the device.

Providing a new READ or WRITE command and column address on each clock cycle is the most flexible way to achieve decrement bursting because it can be used regardless of the programmed burst length and burst type. In addition, this method does not require any Mode Register accesses, thereby avoiding that additional overhead. An example is shown in Figure 1.

The only drawback of random column access is that the address and command buses are used during every clock cycle. However, this is no different from the way these operations are performed with conventional FPM DRAMs or EDO DRAMs and full-speed random access is a significant benefit.

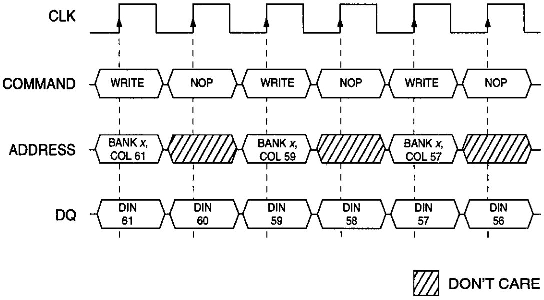


Figure 2
DECREMENT BURSTING WITH SUCCESSIVE BURSTS OF TWO – STARTING AT AN ODD COLUMN ADDRESS

SUCCESSIVE BURSTS OF TWO

The programmed burst length of two for SDRAMs/SGRAMs is inherently bidirectional. If the burst starts at the first location in the block of two, i.e., the least significant address bit is zero, then the address will increment for the next access. If the burst starts at the second location in the block of two, i.e., the least significant address bit is one, then the address will decrement for the next access. Longer incrementing bursts can be constructed by issuing successive READ or WRITE commands to incrementing even addresses every other clock cycle. Similarly, longer decrementing bursts can be constructed by issuing successive READ or WRITE commands to decrementing odd addresses on every other clock cycle.

In the case where a decrementing burst needs to start a an even address, the initial command issued for the even address simply needs to be followed immediately with the command to the previous (odd) address. After that, a command would be issued on every other cycle to the decrementing odd addresses. A similar procedure would be used to start an incrementing burst from an odd address

After this initial orientation, if necessary, the address and command buses are available every other cycle for other commands. Examples are shown in Figures 2 and 3.

Additional overhead in the form of Mode Register accesses is only required if the burst of two is not the preferred mode of operation for other accesses.

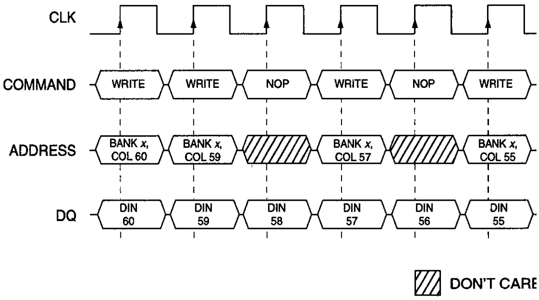


Figure 3
DECREMENT BURSTING WITH SUCCESSIVE BURSTS OF TWO – STARTING AT AN EVEN COLUMN ADDRESS

SUCCESSIVE BURSTS OF FOUR OR EIGHT

A programmed burst length of four (eight) is bidirectional if starting at either the first or last location in the block and the burst type is interleaved. If the burst starts at the first location in the block (the two [three] least significant address bits are all zeroes), then the address will increment for the next three (seven) accesses. If the burst starts at the last location in the block (the two [three] least significant address bits are all ones), then the address will decrement for the next three (seven) accesses. Longer incrementing bursts can be constructed by issuing successive READ or WRITE commands to every fourth (eighth) incrementing column address on every fourth (eighth) clock cycle, and similarly, longer decrementing bursts can be constructed by issuing successive READ or WRITE commands to every fourth (eighth) decrementing column address on every fourth (eighth) clock cycle.

In the case where a decrementing burst needs to start at a location other than the last in the block, individual commands must be issued on each clock until the lower boundary is reached. A command would then be issued on every fourth (eighth) cycle to every fourth (eighth) decrementing column address. A similar procedure would be used to start an incrementing burst from any address other than the first address in the block.

After this initial orientation, if necessary, the address and command buses are available three of four (seven of eight) clock cycles, for other commands. Examples are shown in Figures 4 and 5.

Additional overhead in the form of Mode Register accesses is only required if the interleaved burst of four (eight) is not the preferred mode of operation for other accesses.

SUMMARY

The SGRAM, with its pipelined architecture, provides high-speed burst access (66-100 MHz) while still offering the capability to change the column address for each access. This capability leads to full-speed, random incrementing or decrementing burst accesses within a row in memory.

Decrement bursting, in particular, can be achieved using one of several different methods which rely only on existing command modes defined for SDRAM/SGRAMs. Each method represents a different combination of flexibility, complexity, overhead, and command and address bus utilization. Regardless of the method selected in a given system, full-speed decrementing accesses can be achieved without a dedicated and additional command mode.

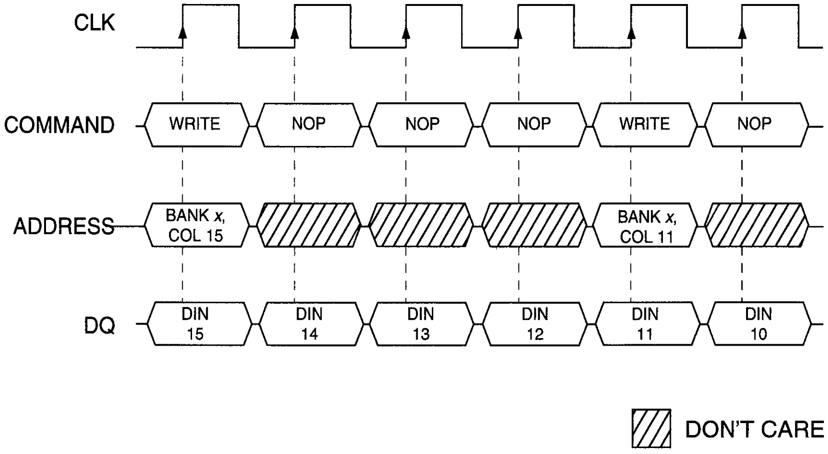


Figure 4
DECREMENT BURSTING WITH SUCCESSIVE BURSTS OF FOUR – STARTING AT THE LAST COLUMN ADDRESS IN THE BLOCK

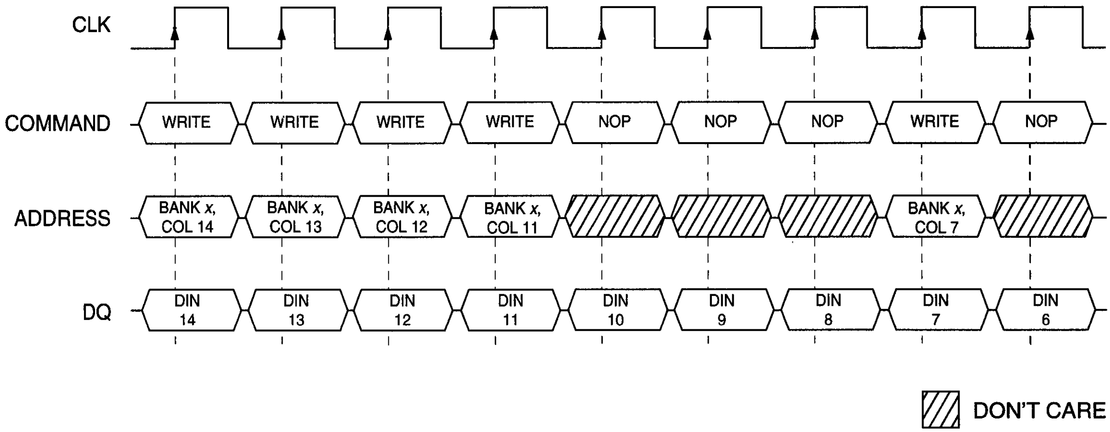


Figure 5
DECREMENT BURSTING WITH SUCCESSIVE BURSTS OF FOUR – STARTING AT THE SECOND COLUMN ADDRESS IN THE BLOCK

TECHNICAL NOTE

HIDING THE LOAD SPECIAL MODE REGISTER COMMAND IN THE SGRAM

This article was originally published in 1997.

INTRODUCTION

The Synchronous Graphics RAM (SGRAM) includes two features that facilitate the design of high-performance graphics subsystems. These features are known as Block Write and Masked Write (or Write-Per-Bit). Both of these features require preloading of a register internal to the SGRAM. This preloading is accomplished using the LOAD SPECIAL MODE REGISTER (LSMR) command. In most cases the use of this command is so infrequent that the effect on bus bandwidth is negligible. However, in cases where the use of the LSMR command will be more frequent, the graphics controller designer will want to issue the LSMR commands at times when the bus is otherwise idle (thereby "hiding" the command). This technical note provides several examples of hiding the LSMR command; other scenarios are also possible.

NOTE: Not all of the cases shown in the examples are tested in production test programs, and some may not be attractive for the system designers to use; however, they were chosen to best illustrate how the device was designed to operate.

LSMR COMMAND

When an LSMR command is executed, one of two registers internal to the SGRAM is loaded. Either the Color Register is loaded with color data for use in BLOCK WRITEs (whether masked or unmasked), or the Mask Register is loaded with mask data for use in MASKED WRITEs or MASKED BLOCK WRITEs. In either case, the data is provided on the DQ pins coincident with the LSMR command being applied on the command inputs (CS#, RAS#, CAS#, WE# and DSF). The logic values applied to the address inputs at that time are used to select either the Color Register or the Mask Register as the destination for the data.

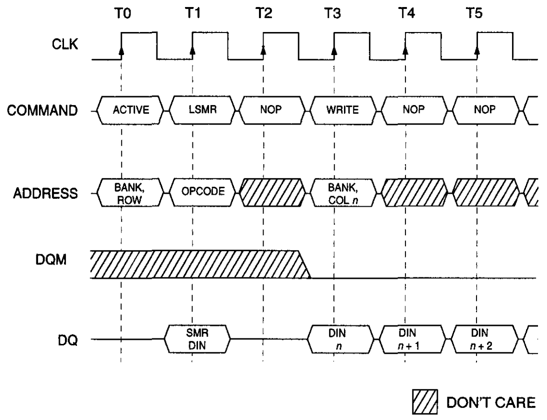
INDEPENDENT OPERATION

Loading data to either of these registers is independent of reading or writing data from or to the DRAM array (except for using the same pins), meaning that as long as bus contention is avoided, these two types of operations (special register loads and memory accesses) will not interfere with each other. The DQM inputs act as masks or enables for memory accesses only and have no effect on data being loaded into the Color or Mask Registers.

Because of this independence, there are several possibilities for interleaving these operations on the memory interface. Some examples follow.

ROW ACTIVATION TIME

Figure 1 illustrates the application of an LSMR command during the row activation (or ^tRCD) time in a row access.



ACTIVE = Either ACTIVE with WPB or ACTIVE without WPB
WRITE command (shown) can be READ, or BLOCK WRITE, etc.
Burst Length (shown) = 4 or greater
Sequential burst shown
LSMR = Load Special Mode Register
OPCODE: A0-A4,A7-A8,BA=0; A5 = 0, A6 = 1 for Color Data
A5 = 1, A6 = 0 for Mask Data
SMR DIN = Input data for either the Color Register or the Mask Register, depending on OPCODE

Figure 1
APPLYING AN LSMR COMMAND DURING ROW ACTIVATION TIME

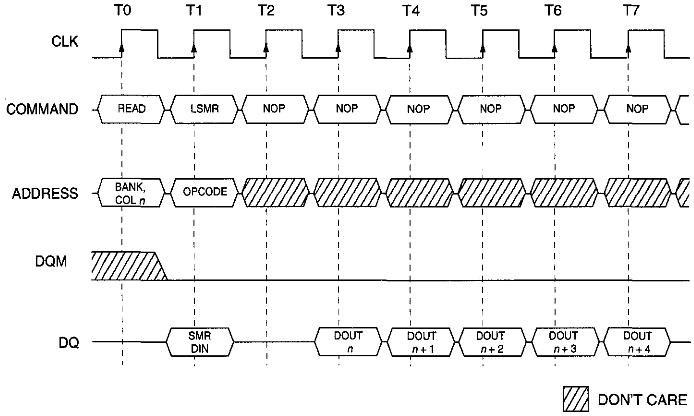
This assumes that there are no accesses in progress to the second bank. Cases where memory accesses are in progress are covered below.

READ LATENCY

Figure 2 shows the application of an LSMR command during the CAS# latency period following a READ command. Here a CAS# latency of three is shown, meaning that the output drivers do not turn on until after T2.

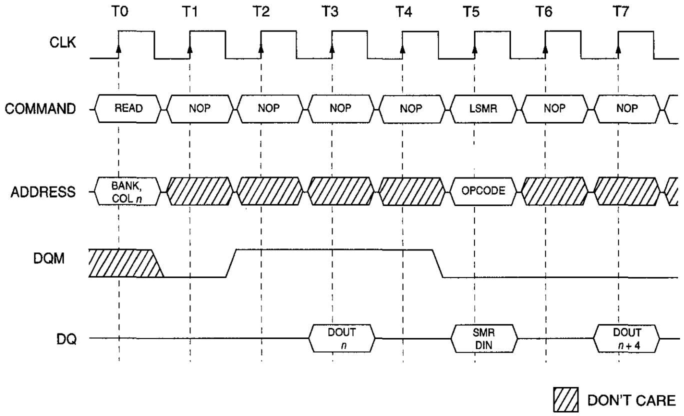
READ BURST

Figure 3 shows the application of an LSMR command during a READ burst at a point where the read data is not needed. Here the DQM inputs are used to turn off the output drivers so that mask or color data can be applied to the DQ pins (recall that the READ DQM latency is two).



Burst Length (shown) = 8 (or full page)
Sequential burst shown
CAS# Latency = 3
LSMR = Load Special Mode Register
OPCODE: A0-A4,A7-A8,BA=0; A5 = 0, A6 = 1 for Color Data
A5 = 1, A6 = 0 for Mask Data
SMR DIN = Input data for either the Color Register or the Mask Register, depending on OPCODE

Figure 2
APPLYING AN LSMR COMMAND DURING THE READ LATENCY PERIOD



Burst Length (shown) = 8 (or full page)
Sequential burst shown
CAS Latency (shown) = 3
LSMR = Load Special Mode Register
OPCODE: A0-A4,A7-A8,BA=0; A5 = 0, A6 = 1 for Color Data
A5 = 1, A6 = 0 for Mask Data
SMR DIN = Input data for either the Color Register or the Mask Register, depending on OPCODE

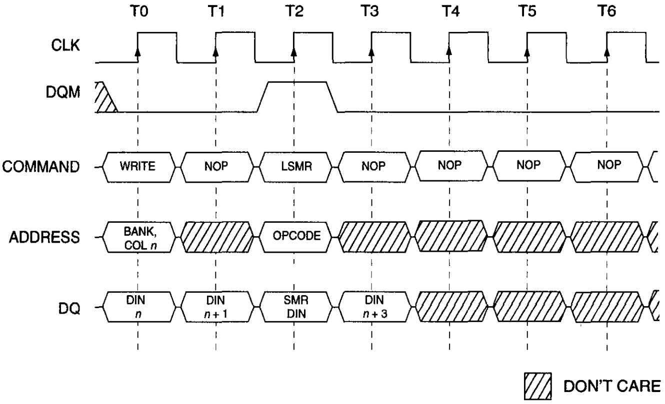
Figure 3
APPLYING AN LSMR COMMAND DURING A READ BURST

WRITE BURST

Figure 4 shows the application of an LSMR command during a WRITE burst at a point where no data needs to be written to the DRAM array. Here the DQM inputs are used to prevent the color or mask data from being written to the DRAM array (recall that the WRITE DQM latency is one).

SUMMARY

Loading of the Color or Mask Register in the SGRAM for use in BLOCK WRITEs and/or MASKED WRITEs is independent of accesses to the DRAM array, except for using the same pins. This means that as long as bus contention is avoided, there is a high level of flexibility in interleaving these operations. The examples provided in this technical note illustrate that flexibility.



Burst Length (shown) = 4
Sequential burst shown
LSMR = Load Special Mode Register
OPCODE: A0-A4,A7-A8,BA=0; A5 = 0, A6 = 1 for Color Data
A5 = 1, A6 = 0 for Mask Data
SMR DIN = Input data for either the Color Register or the Mask Register, depending on OPCODE

Figure 4
APPLYING AN LSMR COMMAND DURING A WRITE BURST

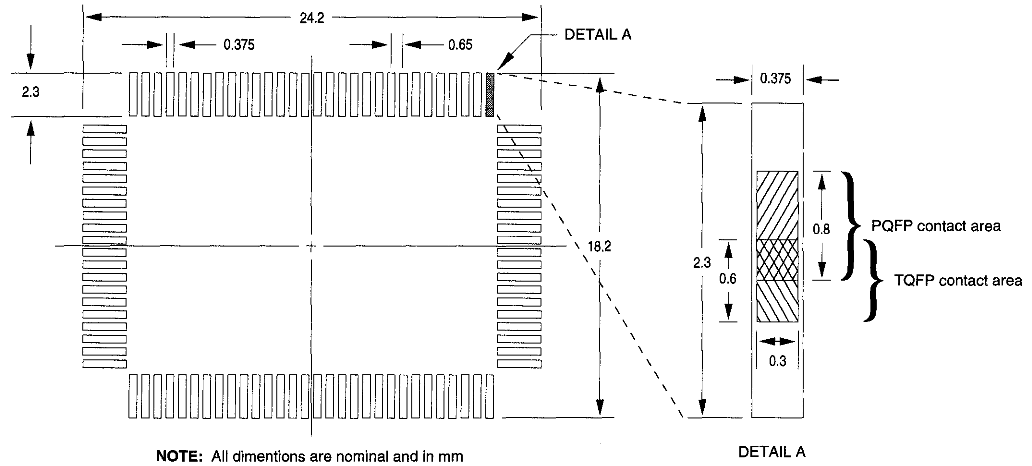
TECHNICAL NOTE

SGRAM PACKAGE COMPATIBILITY

This article was originally published in 1997.

PACKAGE AND PIN COMPATIBILITY

While some vendors are using the Plastic Quad Flat Pack (100-pin PQFP), Micron has elected to use a thinner package, the Thin Quad Flat Pack (100-pin TQFP). Both may be accommodated in a single design by making the pads long enough to accept either package. The thicker PQFP has a slightly broader footprint. This is due to the device lead vertical runs not being shaped perpendicularly to the package underside: hence, the taller the package, the wider the lead excursion. It is not desirable to use 90° lead bends due to reduced reliability. See Figure 1 for a recommended PCB land pattern which will accommodate either package thickness. The TQFP offers several advantages over the PQFP. The TQFP can be mounted in systems where height is restricted. (JEDEC specification MO-136 lists TQFP overall height as 1.60mm maximum, whereas the PQFP is 2.2mm or 3.0mm, depending upon package option.) The TQFP also has better speed capability since the thermal resistance is smaller for the thinner package.



NOTE: All dimentions are nominal and in mm

Figure 1
PCB LAND PATTERN FOR 100-PIN TQFP AND 100-PIN PQFP DEVICES

TECHNICAL NOTE

EXAMPLES OF READ-MODIFY-WRITE CYCLES WITH SYNCHRONOUS DRAMs

This article was originally published in 1997.

INTRODUCTION

The existing READ-MODIFY-WRITE (R-M-W) cycle used with asynchronous DRAMs can be emulated when using synchronous DRAMs. A brief comparison of asynchronous and synchronous access cycles is presented in this article, along with several examples of READ-to-WRITE cycles for synchronous DRAMs.

SYNCHRONOUS vs. ASYNCHRONOUS TIMING

First, compare a synchronous DRAM's access signalling to an asynchronous DRAM (Figure 1). A synchronous ACTIVE command opens the array row. Similarly, the RAS control line opens an array row (page) for an asynchronous DRAM. The sync READ command is analogous to the async CAS# signal falling with WE# at logic level HIGH. The sync WRITE command is similar to the async WE# signal falling with CAS# at logic LOW. In the case of a synchronous WRITE, the column address must be placed on the bus again unlike the R-M-W cycle of the async part. The DQM control line of the synchronous device can be considered the analog of OE# data bus control of the async device. The PRECHARGE command closes the row of the sync device just as bringing RAS# HIGH on the asynchronous device closes the row. Examples of the synchronous access cycles will be used for the remainder of this article.

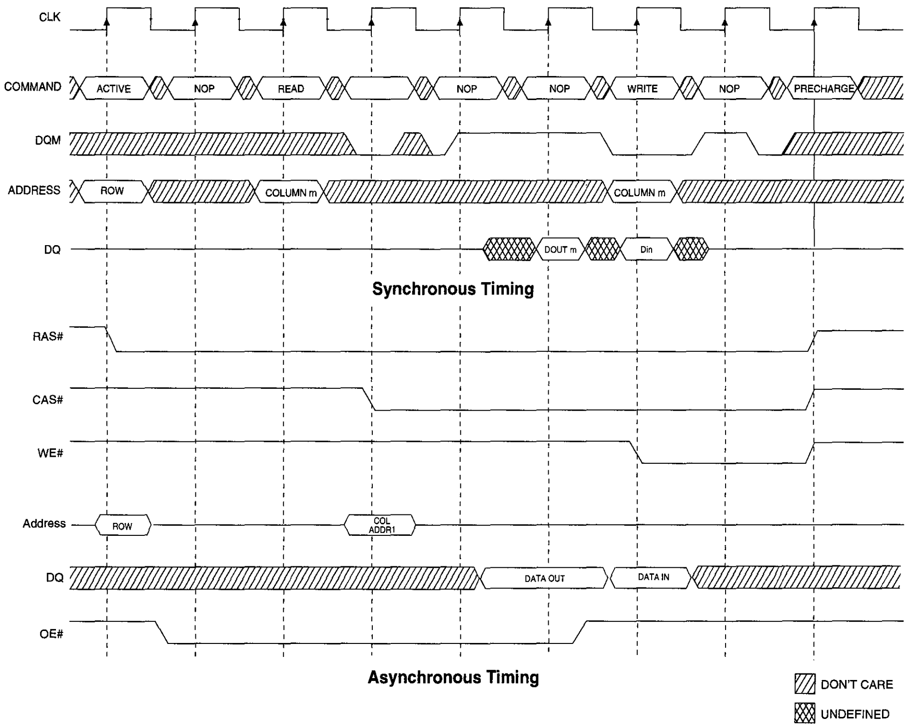
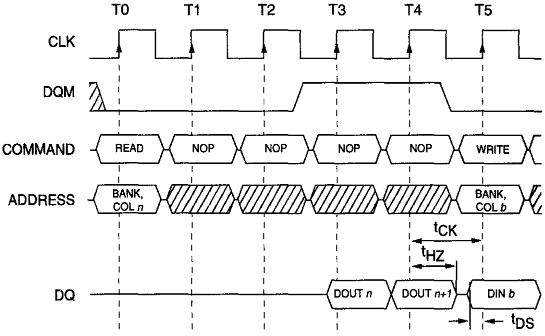


Figure 1
SYNCHRONOUS vs. ASYNCHRONOUS TIMING

READ INTERRUPTED BY A WRITE

A fixed-length or full-page READ burst may be truncated with a WRITE burst or BLOCK WRITE command (provided that AUTO PRECHARGE was not activated). The validity of performing a continuous READ-to-WRITE cycle is dependent upon the timing specifications for the synchronous DRAM and the operating frequency of the memory clock as shown in Figure 2. In this case, the WRITE cycle is initiated following the last (or last desired) data element from the READ burst. Figure 2 is the case where data contention is avoided without a dead access cycle. If the specifications for a given speed grade do not allow for contention to be avoided at a particular operating frequency, a single cycle delay must occur between the last READ data and the WRITE command as shown in Figure 3.

The DQM inputs are used to avoid I/O contention. The DQMs must be asserted (HIGH) at least two clocks (DQM latency is two clocks for output buffers) prior to the WRITE command to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z) regardless of the state of the DQM signals. The DQM signals must be de-asserted (DQM latency is zero clocks for input buffers) prior to the WRITE command to ensure that the written data is not masked. Figure 2 shows the case where the memory clock period is long enough that bus contention is avoided without adding a NOP cycle. Figure 3 shows the case where $^tCK < {}^tHZ + {}^tDS$, and thus an additional NOP cycle is needed to avoid I/O contention.



NOTE: A CAS latency of three is used for illustration.

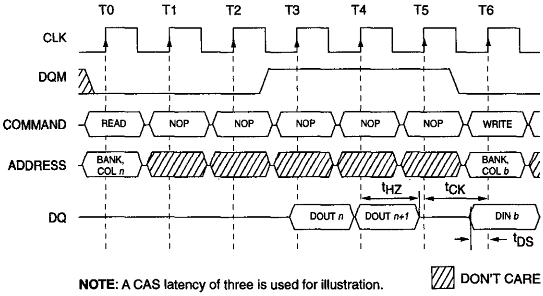
Figure 2
READ INTERRUPTED BY WRITE
($^tCK > {}^tHZ + {}^tDS$)

READ FOLLOWED BY A WRITE

A fixed-length READ burst may also be followed by a WRITE burst or BLOCK WRITE command. The WRITE burst can be initiated on the clock edge immediately following the last data element from the READ burst, provided that I/O contention can be avoided as previously shown in Figure 2. If I/O contention cannot be avoided, an extra NOP cycle will be required. Figure 4 shows a WRITE following a READ. Notice that the I/O transition occurs without the use of the DQM signals.

READ WITH AUTO PRECHARGE FOLLOWED BY A WRITE

A READ with AUTO PRECHARGE cannot be truncated in any manner. The burst must continue until the last data element is driven on the bus. Any command issued to the same bank is an illegal operation and is considered an undefined access. In this case a WRITE or BLOCK WRITE command can only be issued after $^tRP + {}^tRCD$ is met. Figure 5 demonstrates this access with a CAS# latency of three and burst length of four. The NOP issued after the READ burst allows time for ^tRP as the PRECHARGE starts at the clock where $^tRC - {}^tRP$ is met. Although no data is read or written during the transition cycles, the bus can be occupied with an access to the other bank since neither the address nor command buses are needed for the AUTO PRECHARGE.

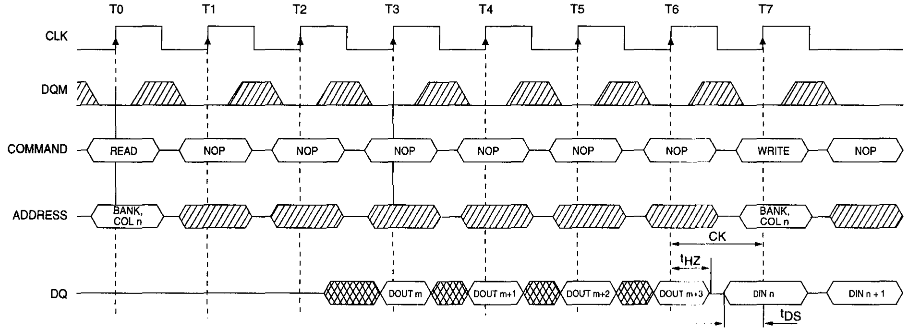


NOTE: A CAS latency of three is used for illustration.

Figure 3
READ INTERRUPTED BY WRITE
($^tCK < {}^tHZ + {}^tDS$)

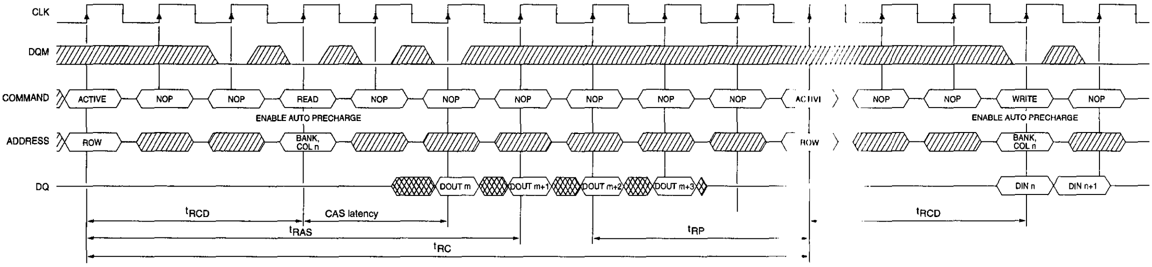
SUMMARY

The R-M-W used in asynchronous DRAMs is available when using synchronous DRAMs. R-M-W cycles for synchronous DRAMs can be executed as READ interrupted by WRITE; READ-to-WRITE transition; and READ with AUTO PRECHARGE, followed by a WRITE. The major difference between asynchronous R-M-W cycles and synchronous R-M-W cycles is that synchronous READ-to-WRITE transitions require that the address be registered on the bus for both the READ and WRITE portions of the R-M-W access cycle.



NOTE: For this example, the burst length = 4, the CAS latency = 3, and the READ burst is followed by a WRITE "manual" PRECHARGE.

Figure 4
READ FOLLOWED BY WRITE



NOTE: For this example, the burst length = 4 and the CAS latency = 2.

▨ DON'T CARE
▩ UNDEFINED

Figure 5
READ WITH AUTO PRECHARGE FOLLOWED BY A WRITE

TECHNICAL NOTE

ACHIEVE MAXIMUM COMPATIBILITY IN SDRAM/ SGRAM DESIGN

This article was originally published in 1997.

INTRODUCTION

With the synchronous memory interface gaining strong industry support, many designs in communications, graphics and embedded control are migrating rapidly toward synchronous memory. Synchronous designs for main memory, on the other hand, are migrating at a more gradual pace. The performance benefits of synchronous DRAM (SDRAM) in main memory—compared to more traditional memory interfaces such as Extended Data-Out (EDO)—have not yet been realized. However, new PC main memory designs that take advantage of a fully synchronous memory bus should begin emerging and are expected to result in SDRAM domination of the market. Designers of low-volume DRAM applications will need to be sensitive to the direction of the high-volume market and begin incorporating synchronous memory.

Micron is currently producing two distinct types of synhronous DRAM: SDRAM, targeted for PC main memory, nd synchronous graphics RAM (SGRAM), targeted for high-bandwidth video memory applications. Both devices have specific characteristics that make them well suited for heir primary applications. The SDRAM is designed to provide memory array depth as inexpensively as possible or high-volume PC designs, while the SGRAM is designed or high bandwidth, by virtue of a wide data bus, and ncludes special video-specific functions such as BLOCK WRITE and WRITE-PER-BIT (MASKED WRITE).

While there is a divergence in organization and special eatures for the SDRAM and SGRAM, they share a succinct subset of operations in common. Designs that are intended to se both device types, however, deserve careful analysis ecause of the functional differences among vendors of synhronous memory. This article assists with that analysis by ighlighting the subtle differences in operation between Micron's SDRAM and SGRAM devices and by offering some aveats with respect to other vendors' data sheets regarding DRAM/SGRAM operation.

The following discussion assumes a CAS latency of three which covers most applications), 83 MHz or 100 MHz devices unning at the maximum specified clock rate, and burst lengths hat are sufficiently long (4, 8 or full-page) to be interrupted as hown for each case. Discussion of the operation of synchro-ous devices, other than Micron's, is based on the interpretation of several other major vendors' data sheets. Please contact other vendors directly to verify operation of their devices.

DESIGNING TO A COMMON SUBSET

The major differences between Micron's SDRAM and SGRAM are related to burst terminations and feature sets. These differences have evolved because each device was designed to be compatible with standards that were prevalent when each was first introduced. Micron's SDRAM design follows the predominate functional subset of SDRAM for main memory applications; the SGRAM design is based on the most common subset of the synchronous memory family at the time of its introduction and continues to follow the standards adhered to by many high-volume producers.

Many of the specific differences between Micron's parts also carry over to other vendors' published functional specifications for SDRAM and SGRAM. It is important to be aware that the differences in operation between SDRAM and SGRAM go beyond the obvious special functions that are available on the SGRAM. When considering alternate memory sources for synchronous DRAM interface designs, designing for commonality will help ensure compatibility across vendors and product types.

FEATURE SET DIFFERENCES

The Micron® SDRAM offers a full set of features, including self refresh, that address the portable market. Other features include clock suspend and burst READ/single WRITE.

The current Micron SGRAM design does not include any of the above-referenced features. However, with SGRAM becoming increasingly popular for portable designs, self refresh and clock suspend features will be added to the next generation design. We do not foresee any need for burst READ/single WRITE in graphics applications, so this feature will not be added to Micron's SGRAM.

POWER-UP/INITIALIZATION

The Micron power-up sequence for both SDRAM and SGRAM includes a 100µs delay, a PRECHARGE (all banks) command, two AUTO REFRESH cycles and a LOAD MODE REGISTER command. Other vendors require a 200µs delay and/or eight AUTO REFRESH cycles, specify the LOAD MODE REGISTER command before the AUTO REFRESH cycles, and recommend that the DQMs and CKE go HIGH initially (track Vcc).

Since it is not a requirement that the AUTO REFRESH cycles occur before the LOAD MODE REGISTER command, the sequence shown in Figure 1 should work for all vendors.

CAS LATENCY

The SDRAM design supports a CAS latency of one, two and three, while the SGRAM only supports a CAS latency of two and three. This follows the industry trend for both devices. It should be noted that the CAS latency of one for the SDRAM is still at the mercy of the DRAM array, as is the case with asynchronous DRAMs. The access time for a latency of one reflects the address access time (^tAA) for the array and results in much lower clock frequencies. The benefits gained by a CAS latency of one are questionable unless the clock frequency for the application is much lower than the capability of the part.

WRITE INTERRUPT OF A READ BURST

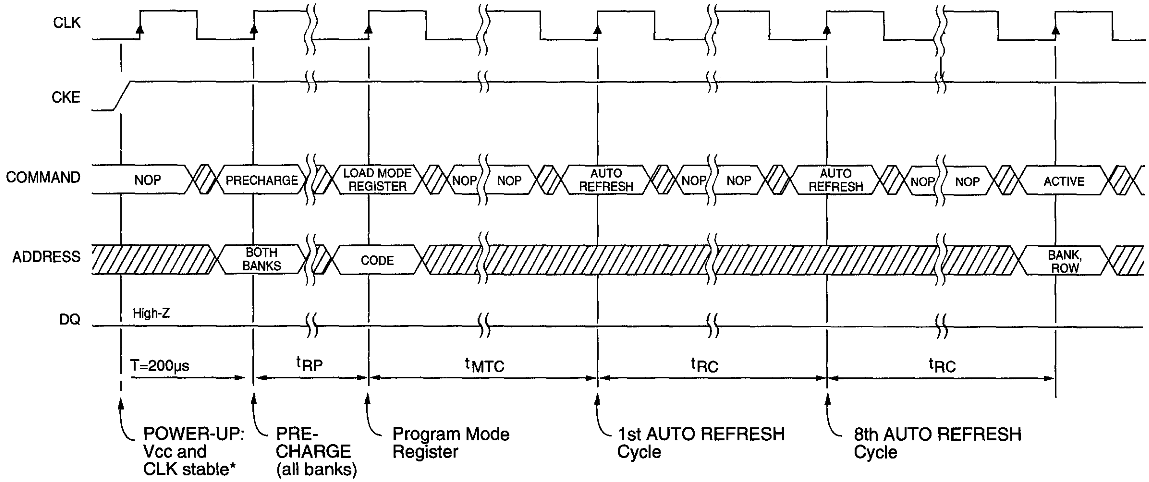
When interrupting a READ burst with a WRITE command using an SDRAM, the DQM (I/O mask enables) must be held HIGH through the positive clock edge, just prior to the WRITE command. This masking scheme is necessary because the WRITE command does not immediately terminate the READ command for many vendors' SDRAMs (including Micron's) and some vendors' SGRAMs.

Interrupting a READ with a WRITE is different for Micron's SGRAM. If the clock cycle time is greater than the clock to High-Z time, plus the data setup time ($^tCK > {}^tHZ + {}^tDS$), and the device driving the input data will not drive before ^tHZ (MAX), the DQM inputs only have to be asserted HIGH for a single cycle, two cycles prior to the WRITE command. (See Figure 13 in Micron's MT41LC256K32D4 data sheet for illustration.)

For applications designed to use SDRAM or SGRAM from several vendors, it is recommended that the DQMs be held HIGH up to the clock edge, just prior to the WRITE command, for a WRITE interrupting a READ burst. This access is shown in Figure 2.

PRECHARGE TERMINATION (OR BURST TERMINATE) OF A READ BURST

Between the PRECHARGE (or BURST TERMINATE) command and the DQs going high-impedance as a result, several data sequences are possible (depending on the vendor). Either one, two or three valid data elements (with no invalid data elements) may occur, or one valid data element, followed by either one or two invalid data elements, may occur. The common denominator here is that the first data element after the PRECHARGE (or BURST TERMINATE) command is valid for all vendors. Therefore for maximum compatibility, the two possible data elements that may follow on some SGRAMs should either be ignored (as shown in Figure 3) or masked via the DQM inputs. The latter would be required if a WRITE to the other bank was to follow as early as possible (on the second cycle after the



*CKE and DQM inputs ramping with Vcc and VccQ is recommended.

▨ DON'T CAR

Figure 1
POWER-UP/INITIALIZATION

last valid data). A command to the same bank is not allowed until ^{t}RP is met. The formula for determining the number of data locations following a PRECHARGE (or BURST TERMINATE) termination of a READ for Micron's SDRAM is X = CAS latency 1, where X is the number of data elements that follow the PRECHARGE (or BURST TERMINATE) command.

Presumably, if a READ to the opposite bank was known to be the next operation, it would be used instead of PRECHARGE to interrupt the current READ burst (since the controller could then come back to PRECHARGE the first bank during the READ latency to the second bank). Otherwise, if necessary, a READ command to the opposite bank could be issued on the clock edge immediately following the PRECHARGE command.

It is appropriate to note here that for some vendors (Micron included) the BURST TERMINATE command applies to any burst length, while for other vendors, it applies only to full-page bursts. So, for maximum compatibility, the BURST TERMINATE command should be used only for full-page bursts.

While some SGRAM vendors have a precharge time (^{t}RP) of four cycles (at maximum frequency), the majority of vendors (Micron included) require three cycles. If compatibility with all vendors is desired, the longer ^{t}RP shown in Figure 3 should be used. However, if performance is critical, a ^{t}RP of three

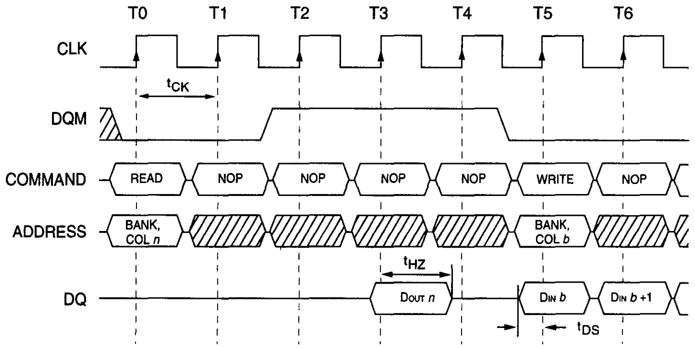


Figure 2
READ INTERRUPTED BY A WRITE

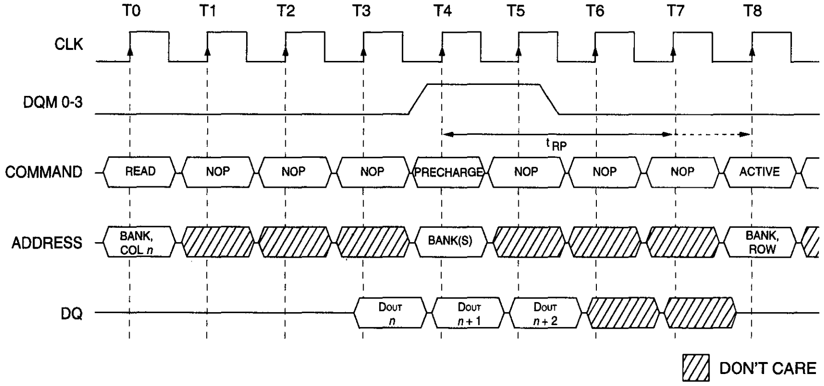


Figure 3
PRECHARGE TERMINATION OF A READ BURST

cycles may be used without sacrificing compatibility with the majority of vendors.

For applications designed to use either SDRAM or SGRAM, it is recommended that only one data location be used following a PRECHARGE (or BURST TERMINATE) and that the DQMs be asserted HIGH to mask any data that might be driven. See Figure 3 for an example of this sequence.

READ BURST WITH AUTO PRECHARGE COMMAND

Following directly from the implementation differences described in the previous section, it is clear that SGRAMs from different vendors begin and end their internal AUTO PRECHARGE periods at different times. For maximum compatibility, the controller should wait until the second positive clock edge, after the last data element in a burst (T8 in Figure 4), before issuing the next command in the same bank. This accounts for all possible combinations of ^{t}RP starting times and number of cycles to completion from the various vendors.

PRECHARGE TERMINATION AND BURST TERMINATE OF A WRITE BURST

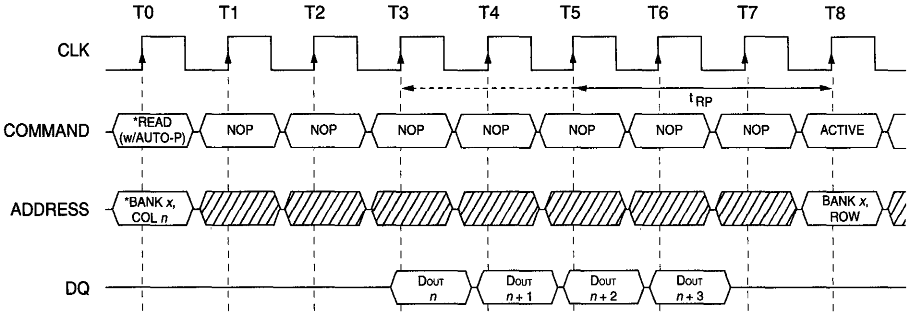
For a PRECHARGE interrupt of a WRITE burst, the WRITE recovery time (^{t}WR) can be either one or two clock cycles. However, for some vendors, the WRITE recovery time is dependent on the CAS latency programmed into the Mode Register. Micron's SDRAM has a ^{t}WR = 1, while Micron's SGRAM has a ^{t}WR = 2 cycles.

The DQMs must be used after the last valid data element to prevent invalid data from being written. The difference is that some vendors require that the DQMs be activated through the clock edge that registers the PRECHARGE command. Other vendors (Micron included) allow deactivation one clock earlier. For compatibility, the DQMs should be activated through the registration of the PRECHARGE command, as shown in Figure 5.

A BURST TERMINATE command issued during a WRITE burst is also different among vendors of SDRAM and SGRAM. Some vendors allow valid WRITEs on the same cycle that the BURST TERMINATE is issued, while other vendors ignore the data when a BURST TERMINATE is issued. To maintain compatibility, it is suggested that the DQMs mask the data on the BURST TERMINATE cycle.

POWER-DOWN ENTRY

Most vendors (Micron included) allow either a NO OPERATION (NOP) (CS# = LOW; RAS#, CAS# and WE# = HIGH) or a COMMAND INHIBIT (CS# = HIGH; others = "Don't Care") on the first clock after CKE switches from HIGH to LOW to go into the power-down mode. One vendor specifies a NOP, however; so for maximum compatibility, the latter implementation should be used. This is shown in Figure 6.



*AUTO PRECHARGE is enabled via address A8 at this time.

NOTE: Burst length = 4 in this example.

▨ DON'T CARE

Figure 4
READ BURST WITH AUTO PRECHARGE

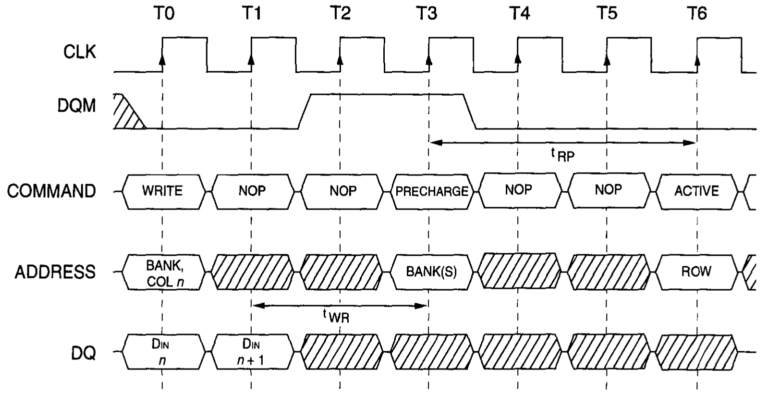
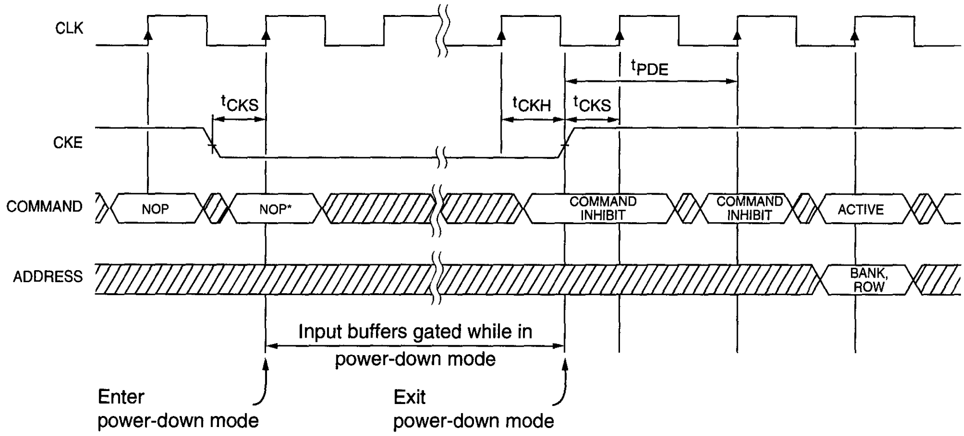


Figure 5
PRECHARGE TERMINATION OF A WRITE BURST



*In this figure, a NOP is specifically defined as CS# = LOW and RAS#, CAS#, WE# = HIGH.

▨ DON'T CARE
▩ UNDEFINED

Figure 6
POWER-DOWN ENTRY AND EXIT

POWER-DOWN EXIT

Again, most vendors (Micron included) allow either a NOP or a COMMAND INHIBIT as the first command after exiting power-down, but again there are exceptions. In this case, some vendors specify only a COMMAND INHIBIT.

Additionally, there are timing issues to consider. Some vendors specify a ^{t}PDE parameter that cannot be met within one clock cycle. For these vendors it must be assumed that having not met this parameter by a given clock edge will not cause any problems and that the device will respond appropriately on the subsequent clock edge. Micron prefers a less ambiguous approach and specifies both ^{t}CKH and ^{t}CKS. This way, the first command after exiting power-down and the clock edge on which it is registered are both known.

Note that the issues as discussed above are also relevant for self refresh. Check specific vendors' data sheets for particular timing requirements.

The combination of these differences in specifications means that an implementation such as the one shown in Figure 6 is needed for compatibility.

SUMMARY

The synchronous memory interface has been identified as the next standard memory solution for all aspects of PC design. This standard is relevant to product designs outside the PC market as well because using the next high-volume DRAM can ensure design longevity. In the PC market, designers and customers alike enjoy the benefits of broad-based support; therefore, controllers and systems will be designed with multiple vendor-compatibility in mind. As a result of the JEDEC standardization effort, all essential attributes and operating modes of the devices will be compatible among vendors. However, there are some fringe areas of operation where some differences in implementation and specification do occur. This article has summarized those differences so they can be accounted for in the design of the relevant controllers and systems, thereby maximizing compatibility.

TECHNICAL NOTE

DESIGNING FOR HIGH PERFORMANCE WITH SYNCHRONOUS DRAM MODULES

This article was originally published in 1997.

INTRODUCTION

With the memory market rapidly embracing synchronous DRAMs (SDRAMs), understanding the various SDRAM module configurations is very beneficial. SDRAM modules provide system designers the memory performance to support future processors' requirements of higher bandwidths. Because SDRAM modules use existing device technology, are JEDEC standard and can support bus speeds of 66 MHz through 100 MHz, they are a viable solution for higher performance. This article gives basic information about SDRAMs and the different 168-pin SDRAM DIMM versions available.

SYNCHRONOUS DRAMs

SDRAM modules are the latest volume solution for achieving improved memory performance. The SDRAM devices used on the module have the core of a standard DRAM with the important addition of synchronous control logic. Synchronizing all inputs and outputs to the system clock simplifies the design of the chipset/memory interface, enabling it to be based on simple state machine operation. In addition, using synchronous techniques improves the margin-to-system noise because inputs are latched by the system clock and are not level-driven. Since all timing is based on the same synchronous clock, designers can achieve tighter specification margins. Also, since the SDRAM access is programmable, designers can improve bus utilization because the SDRAM output can be synchronized to the processor.

These modules offer a burst mode with a burst cycle time that is considerably faster at higher frequencies than the cycle time associated with FAST-PAGE-MODE (FPM) or Extended Data-Out (EDO) operation. SDRAMs use a self-incrementing counter and a Mode Register to determine the column address sequence after the first memory location accessed on a page. Having predetermined addresses allows the DRAM operations to be performed faster (after the first access) since the time to set up subsequent column addresses in the external timing is removed. Also, the option of programmable burst length and latency enables designers to customize these critical functions for system requirements.

SDRAMs have multiple internal bank architectures that can increase data throughput and eliminate data gaps because the interleaved banks effectively hide the precharge time of one bank by accessing data through the other.

Table 1
BANDWIDTH FOR PIPELINED DEVICES

SDRAM ORGANIZATION	ROW ADDRESS	COLUMN ADDRESS	BANK ADDRESS	SDRAM BANKS	TOTAL ADDRESS BITS
1 Meg x 16	A0-A10	A0-A7	BA0	2	20
2 Meg x 8	A0-A10	A0-A8	BA0	2	21
4 Meg x 4	A0-A10	A0-A9	BA0	2	22
4 Meg x 16	A0-A11	A0-A7	BA0-BA1	4	22
8 Meg x 8	A0-A11	A0-A8	BA0-BA1	4	23
8 Meg x 16	A0-A11	A0-A8	BA0-BA1	4	23
16 Meg x 4	A0-A11	A0-A9	BA0-BA1	4	24
16 Meg x 8	A0-A11	A0-A9	BA0-BA1	4	24
32 Meg x 4	A0-A11	A0-A9, A11	BA0-BA1	4	25

Table 2
DRAM ADDRESSING OPTIONS

DRAM ORGANIZATION	ROW ADDRESS	COLUMN ADDRESS	REFRESH RATE	TOTAL ADDRESS BITS
1 Meg x 16	A0-A9	A0-A9	1K	20
2 Meg x 8	A0-A10	A0-A9	2K	21
4 Meg x 4	A0-A10	A0-A10	2K	22
4 Meg x 4*	A0-A11	A0-A9	4K	22
4 Meg x 16	A0-A11	A0-A9	4K	22
8 Meg x 8	A0-A12	A0-A9	8K	23
8 Meg x 8	A0-A11	A0-A10	4K	23
16 Meg x 4*	A0-A12	A0-A10	8K	24
16 Meg x 4*	A0-A11	A0-A11	4K	24

*Limited usage and availability

168-PIN SDRAM DIMMs

There are two versions of the 168-pin SDRAM DIMM, with the first version now available as the nonbuffered SDRAM DIMM. The second version to be introduced is the registered SDRAM DIMM. They are intended for use in 64-bit personal computers and workstations, respectively. Both versions are compatible with the nonbuffered EDO and FPM 168-pin DIMMs. Their form factors allow them to be inserted into the same socket as nonbuffered EDO and FPM DIMMs. However, care should be taken when setting up a system to take both DRAM and SDRAM DIMMs. It appears straightforward, but a difficulty arises with the way controllers handle the higher-order addresses and bank addresses of SDRAMs. The controller could have to support a four-bank 64Mb SDRAM-based DIMM, which has multiple addressing modes, a two-bank 16Mb SDRAM-based DIMM and the traditional DRAM addressing options (see Tables 1 and 2). In most cases, no additional multiplexing on the motherboard is needed to implement this concurrent support.

Table 3 shows the module pins that change functions between FPM/EDO and nonbuffered SDRAM and registered SDRAM DIMMs. For some controls, the DRAM signal is turned into an SDRAM signal, such as DRAM CAS# to SDRAM DQMB. On other pins, new lines are used, such as the SDRAM clock enable (CKE) where this pin was a DNU (do not use) on the DRAM version.

MODULE BANKING

Both one- and two-bank DIMMs have been defined. A DIMM bank is defined as being the depth of one SDRAM by the corresponding data bus width. DIMM banks are selected by the chip select (S0#-S3#) interface signals. For two-bank DIMMs, the corresponding data I/Os (DQs and CBs) are dotted together. Take care not to confuse the internal SDRAM device banks (selected by BA0-BA1) with the DIMM banks.

Table 3
PINOUT VARIATIONS

PIN NUMBER	DRAM DIMM	NONBUFFERED SDRAM DIMM	REGISTERED SDRAM DIMM
28	CAS0#	DQMB0	DQMB0
29	CAS1#	DQMB1	DQMB1
30	RAS0#	SO#	SO#
31	OE0#	DNU	DNU
39	A12	BA1	BA1
42	DNU	CK0	CK0
44	OE2#	DNU	DNU
45	RAS2#	S2#	S2#
46	CAS2#	DQMB2	DQMB2
47	CAS3#	DQMB3	DQMB3
48	WE2#	DNU	DNU
62	DNU	Vref, NC	Vref, NC
63	NC	CKE1	CKE1
79	NC	CK2	NC
111	DNU	CAS#	CAS#
112	CAS4#	DQMB4	DQMB4
113	CAS5#	DQMB5	DQMB5
114	RAS1#	S1#	S1#
115	DNU	RAS#	RAS#
122	A11	BA0	BA0
123	A13	A11	A11
125	DNU	CK1	CK1
126	DNU	A12	A12
128	DNU	CKE0	CKE0
129	RAS3#	S3#	S3#
130	CAS6#	DQMB6	DQMB6
131	CAS7#	DQMB7	DQMB7
132	DNU	A13	A13
146	DNU	Vref, NC	Vref, NC
147	DNU	DNU	REGE
163	NC	CK3	NC

DNU = Do Not Use

Table 4
SDRAM DIMM COMPARISON

	168-PIN NONBUFFERED SDRAM DIMM	168-PIN REGISTERED SDRAM DIMM
Voltage	3.3V	3.3V
Bus Width	x64 and x72 ECC	x72 ECC
Max. SDRAMs	20 SDRAMs	40 SDRAMs
Buffering	None	Registered Mode or Buffered Mode
Clocking	4 clock inputs, 5 SDRAMs max. per clock	4 clock inputs: 3 terminated, 1 tied to PLL which distributes multiple clocks

TYPICAL APPLICATIONS

The registered SDRAM module is typically used in systems using more than four memory sockets, while the nonbuffered version is used in systems using four or fewer sockets. This is primarily due to loading issues. The registered DIMMs permit high-end PCs and servers to get equivalent SDRAM densities currently available with EDO DIMMs. This is double the density that can be obtained with the nonbuffered SDRAM DIMMs (Table 4). The registered version is capable of double density due to the addition of a PLL, which can distribute twice the clock signals of the nonbuffered version. As a design limitation, any one clock input is limited to five SDRAMs or less.

Widespread adoption of the 168-pin registered DIMM is not expected until the first half of 1998. This is based on new PC chipsets that will have the appropriate timings to accommodate the added clock delay due to the register. At the initial introduction, both 66 MHz and 100 MHz system bus speeds can be supported. However, 100 MHz operation is expected to be in volume demand by the second half of 1998.

COMPONENT vs. MODULE SPEED

While the SDRAM module is in its infancy, its speed nomenclature is in somewhat of a state of disarray. No consistent definition is being used by the manufacturers or by the users. However, there is a common thread which, when understood, helps one correlate the various nomenclatures.

Where the FPM/EDO DRAM performance is governed by the DRAM timing parameters (i.e., ^{t}RAC, ^{t}CAC, etc.), the SDRAM, on the other hand, has two variables—clocking capabilities (^{t}CK) and the DRAM timing parameters. The de facto industry standard for SDRAM speed designations is to use clocking capabilities alone. Using 66 MHz, 83 MHz and 100 MHz (15ns, 12ns and 10ns, respectively) sounds a lot more impressive than -6 and -7 (60ns and 70ns, respectively). Thus, the clocking capabilities are used: -15 for 66 MHz, -12 for 83 MHz and -10 for 100 MHz, with the DRAM performance being buried within the specifications. Unfortunately, each manufacturer's DRAM timing parameters vary to some degree within the SDRAM. Care must be used in deferring the required number of clocks to be used for the DRAM parameters. If the least common denominator timings are not used, the user risks the possibilities of some SDRAM modules causing conflicts.

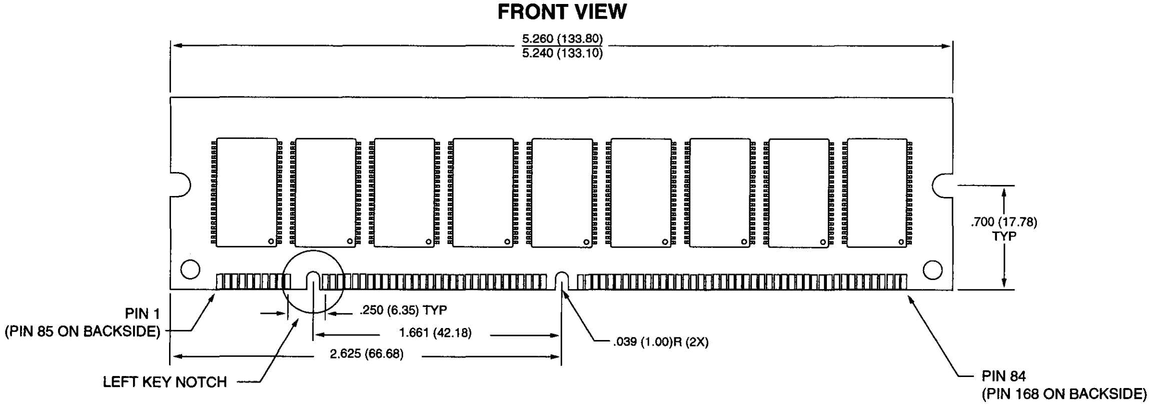


Figure 1
DIMENSIONAL DATA

To compound the issue, the SDRAM is programmable for either a CAS latency of two (^{t}AA limited, i.e., DRAM speed for data-out) or a CAS latency of three (^{t}CK limited, i.e., maximum clocking frequency). As can be observed in Figure 2, the 66 MHz data bus required a -10 SDRAM to provide a CAS latency of two at 66 MHz. The 66 MHz SDRAM could only support a 50 MHz data rate at a CAS latency of two. So, a 66 MHz system designer was driven to use a 100 MHz (-10) SDRAM at 66 MHz or had to add a clock latency to use a 66 MHz (-15) SDRAM in a 66 MHz system, with very little margin.

The difference in speed nomenclature between the target applications and the SDRAM is primarily due to support requirements for two CAS latency options. Figure 3 depicts how the de facto standard has settled. For a 66 MHz memory bus, -10 SDRAMs are used for CAS latency of two and -12 SDRAMs are used for CAS latency of three. For a 100 MHz memory bus, -8A, -8B, -8C SDRAMs are used for CAS latency of three and -8D and -8E are used for CAS latency of two.

MODULE SPEED DESIGNATION

Micron had two viable nomenclatures to use when defining an SDRAM module's speed. For example, when using -10 SDRAMs, the module could have been called a "-10 SDRAM module." However, the majority of system manufacturers referred to SDRAMs in relationship to their system applications. Thus, a -10 SDRAM module is referred to as 66 MHz, CL = 2 with a ^{t}AC of 9ns, or shortened to 66CL2. The DRAM specs are still those of a -10 device. In other words, an SDRAM module's speed designator generally refers to its target application rather than its maximum burst rate.

DIMENSIONAL CHARACTERISTICS

As mentioned earlier, the form factors for the DRAM/SDRAM nonbuffered and SDRAM registered 168-pin DIMMs are consistent to allow insertion into the same DIMM socket. More specifically, the left key notch in the edge connector is shifted to the right of center on all these

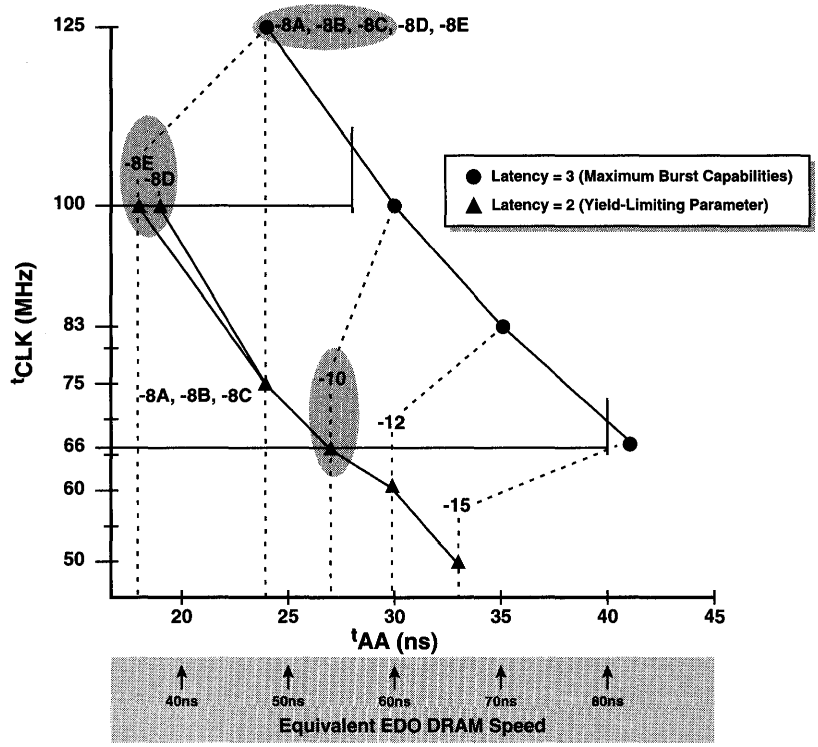


Figure 2
SDRAM LATENCY TIMING

module versions (Figure 1). Also, JEDEC has defined a range of module heights from 1.0 inch to 1.5 inches. Module heights can vary based on module density and configuration.

SERIAL PRESENCE-DETECT

All 168-pin DIMM standards except one (the buffered DRAM version) use a feature called serial presence-detect (SPD). The SPD is used to provide information from the module to the system regarding the module's properties and functionality. The ability to read this information allows the system to set up specifically for the type of module used. The SPD consists of a nonvolatile memory device (typically a 24C02 type 256 word x 8 bit EEPROM) which is used to store settings defined to identify specific parameters of the module. The EEPROM devices used conform to the IIC 2-wire protocol. This protocol defines any device that puts data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the transfer is referred to as the master, and the device that receives the data is referred to as the slave. The master will always start a data transfer and will provide the serial clock for synchronization. The EEPROM on the module is always the slave. The SPD interface consists of the following five signals: SA0-SA2, SCL and SDA. SA0-SA2 are the address inputs, SCL is the clock input and SDA is the serial data input/output.

The SPD data stored in the EEPROM is defined as bytes of information in a specific order (Table 5). The first 128 bytes are reserved for programming by the memory manufacturer, and the second 128 bytes are available for use by the system manufacturer.

Additional information regarding SPD can be found in Micron's Technical Note TN-04-42, "Memory Module Serial Presence-Detect."

System support should require use only of modules with SPD. If there is no SPD support, then worst-case settings could be defaulted or system performance/reliability could be in jeopardy.

SUMMARY

The design of a successful memory subsystem in today's high-performance systems requires a solid understanding of the various memory module solutions available. SDRAM DIMMs play an integral part in enabling memory speeds to increase memory bus speeds to 100 MHz. The nonbuffered and registered versions of the 168-pin SDRAM DIMM address a wide range of new high-speed memory applications. These DIMMs represent the latest volume solution for improving memory performance.

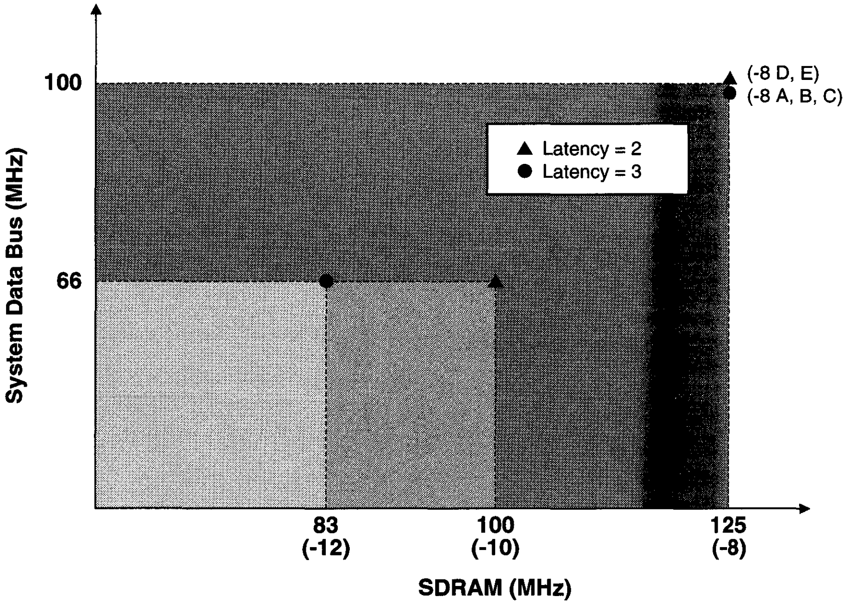


Figure 3
SDRAM DATA BUS vs. DEVICE SPEED

Table 5
SPD BYTE DESCRIPTION

BYTE NUMBER	FUNCTION DESCRIPTION
0	Number of SPD Bytes Used by Micron
1	Total Number of Bytes in SPD device
2	Memory Type (FPM, EDO, SDRAM, etc.)
3	Number of Row Addresses
4	Number of Column Addresses
5	Number of DIMM Banks
6	Data Width of Module
7	Data Width (continued)
8	Voltage Interface Level
9	SDRAM Cycle time (^{t}CK) at Highest CAS Latency
10	SDRAM Access from Clock (^{t}AC) at Highest CAS Latency
11	Module Configuration Type (Nonparity, Parity or ECC)
12	Refresh Rate/Type
13	Primary SDRAM Component Width
14	Error Checking SDRAM Component Width
15	SDRAM Device Attributes: Minimum Clock Delay, Back-to-Back Random Column Access
16	SDRAM Device Attributes: Burst Lengths Supported
17	SDRAM Device Attributes: Number of Banks on SDRAM Device
18	SDRAM Device Attributes: CAS Latency
19	SDRAM Device Attributes: CS# Latency
20	SDRAM Device Attributes: Write Latency
21	SDRAM Module Attributes (Nonbuffered, Registered, etc.)
22	SDRAM Device Attributes: General
23	SDRAM Cycle Time (^{t}CK) at Second-Highest CAS Latency
24	SDRAM Access from Clock (^{t}AC) at Second-Highest CAS Latency
25	SDRAM Cycle Time (^{t}CK) at Third-Highest CAS Latency
26	SDRAM Access from Clock (^{t}AC) at Third-Highest CAS Latency
27	Minimum Row Precharge Time (^{t}RP)
28	Minimum Row Active to Row Active Delay (^{t}RRD)
29	Minimum RAS# to CAS# Delay (^{t}RCD)
30	Minimum RAS# Pulse Width (^{t}RAS)
31	Module Bank Density
32-61	Superset Information (reserved for future use)
62	SPD Revision
63	Checksum for Bytes 0-62
64-71	Module Manufacturer's JEDEC ID Code
72	Module Manufacturing Location
73-90	Module Part Number
91-92	Module Revision Code
93	Year Manufactured
94	Week Manufactured
95-98	Module Serial Number
99-125	Manufacturer-Specific Data (reserved)
126-127	Reserved
128-255	Open for customer use

TECHNICAL NOTE

IS YOUR MODULE PC100?

This article was originally published in 1998.

INTRODUCTION

This technical note explains how to determine the application speed of a Micron® SDRAM module, and more specifically, how to determine if a module using Micron SDRAMs is PC100-compliant. This explanation is offered because the speed designator on the SDRAM component does not necessarily reflect the system application speed of the module itself.

PC100 COMPLIANCE

Intel® advanced the move from 66 MHz to 100 MHz by publishing an SDRAM specification that defined the AC and DC timing parameters for 100 MHz operation in a PC environment. As a result, SDRAMs mounted on a module must be specifically designed to meet Intel's PC100 requirements in order for the SDRAM module to be PC100-compliant.

Micron's -8 series of SDRAMs is designed to the PC100 specification; our -10 series is not. Not all PCs are PC100-compliant. Please refer to your system documentation to determine this.

COMPONENT vs. MODULE SPEED

The difference in speed nomenclature between the system application (module level) and the SDRAM (component level) is primarily due to the support requirements for two CAS latency options. For a 66 MHz memory bus, -10 SDRAMs (with a maximum frequency of 66 MHz at CL = 2) are used for a CAS latency of two. For a 100 MHz memory bus, -8A, -8B and -8C SDRAMs are used for a CAS latency of three, and -8E is used for a CAS latency of two.

Refer to Figure 1 for module and component mark examples.

MODULE SPEED DESIGNATION

Two viable nomenclatures can be used to define SDRAM module speed. For example, a module using -10 SDRAMs can be called a "-10 SDRAM module." However, the majority of system manufacturers commonly refer to SDRAMs in relationship to their system applications. Thus, a -10 SDRAM module is usually referred to as 66 MHz, CL = 2, or 662. (The SDRAM specs are still those of a -10 device.) In other words, an SDRAM module's speed designator generally refers to its target application rather than its maximum burst rate.

Refer to Table 1 for part number and speed designator examples.

SUMMARY

An SDRAM DIMM with -10 (100 MHz) components is designated for 66 MHz PC operation. This type of module is not guaranteed to run consistently in a PC100, 100 MHz system. In order for the module to be PC100-compatible, the components need to be marked as -8A, -8B, -8C or -8E (125 MHz). Modules with -8A, -8B or -8C components will run at 100 MHz at a CAS latency of three. Modules with -8E components will run at 100 MHz at a CAS latency of two.

Table 1
MICRON SDRAM MODULE SPEED DESIGNATORS (EXAMPLE)

MODULE PART NUMBER	MARKED SPEED OF COMPONENT	MARKED SPEED OF MODULE	CAS LATENCY	PC APPLICATION (SYSTEM BUS SPEED)
MT8LSDT864AG-662__ (64MB)	-10 (100 MHz)	-662 (66 MHz)	2	66 MHz
MT8LSDT864AG-10A__ (64MB)	-8A (125 MHz)	-10A (100 MHz)	3	PC100 (100 MHz)
MT8LSDT864AG-10B__ (64MB)	-8B (125 MHz)	-10B (100 MHz)	3	PC100 (100 MHz)
MT8LSDT864AG-10C__ (64MB)	-8C (125 MHz)	-10C (100 MHz)	3	PC100 (100 MHz)
MT8LSDT864AG-10E__ (64MB)	-8E (125 MHz)	-10E (100 MHz)	2	PC100 (100 MHz)

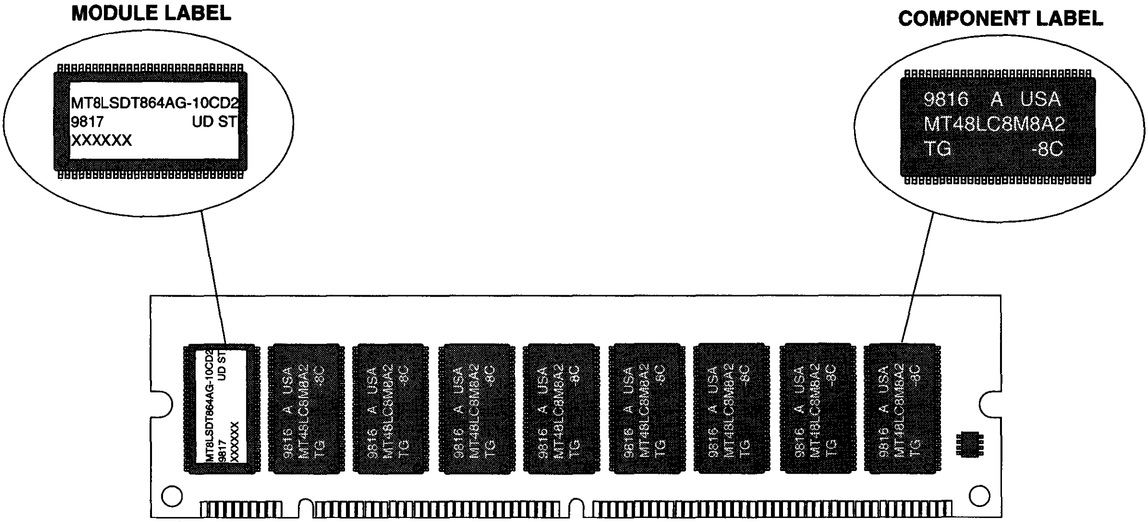


Figure 1
MICRON PC100 MODULE AND COMPONENT MARKS (EXAMPLE)

TECHNICAL NOTE

SDRAM WRITE TO ACTIVE COMMAND TIMING

This article was originally published in 1998.

INTRODUCTION

Once a row (page) has been opened to a particular bank within an SDRAM, the number of READ and/or WRITE commands that may be executed is limited only by the refresh and $^{t}RAS_{max}$ requirements. At some point, the open page must be closed, either to perform refresh or to activate another page.

The SDRAM requires the open page in a bank to be closed and precharged prior to an ACTIVE command being applied to open another page within the same bank. The precharge function is achieved manually by applying the PRECHARGE command or automatically via the AUTO PRECHARGE command in conjunction with the READ or WRITE command.

Another way to view the SDRAM precharge function is o compare it to an EDO/FPM DRAM. With an EDO/FPM DRAM, RAS# going LOW opens a page, and RAS# must be aken back HIGH and precharged prior to RAS# going LOW again to open another page. A similar function occurs with SDRAMs. The ACTIVE command will cause an internal RAS# to go LOW to open a page in the targeted bank. The internal RAS# must be taken back HIGH and precharged before another page can be opened. The PRECHARGE command is what causes the internal RAS# to go HIGH and perform the precharge function.

This article will analyze the precharge function, the mechanics involved in the transition from a WRITE to an ACTIVE command, and the two-clock ^{t}WR requirement for high frequency designs. The Micron® -8C SDRAM with a CAS latency of three (commonly referred to as a PC100 3-2-2 device) will be used to illustrate ^{t}WR operation.

PRECHARGING SDRAM

Applying the PRECHARGE command during read accesses is a relatively straightforward process covered in Micron SDRAM data sheets. However, applying the PRECHARGE command during write accesses is more complicated, especially if future compatibility is considered. Unlike READs, which require only ^{t}RP be met, WRITEs require both ^{t}WR and ^{t}RP to be met prior to application of another ACTIVE command. See Figure 1 for a diagram of ^{t}WR and ^{t}RP.

The ^{t}WR and ^{t}RP relationship tends to create confusion. Both parameters must be met, but many system designers have assumed ^{t}WR to be a "1 clock" requirement. That was true for 100 MHz and slower devices, especially with the slower ^{t}RPs (30ns to 40ns). ^{t}WR and ^{t}RP together should be 35ns or more for maximum yields. When ^{t}RP equaled 30ns, a ^{t}WR of 10ns was quite acceptable. With lots of ^{t}RP time, it was easy to allocate some of it to the ^{t}WR time to make it appear as if ^{t}WR were only one clock.

Table 1
FAIL-SAFE WRITE-BACK AND PRECHARGE VALUES

SDRAM Speed	Time (ns)		Clocks		Bus Speed	
	^{t}WR	^{t}RP	^{t}WR	^{t}RP	MHz	ns
-10[1]	10	30	1	1*	33	30
-10[2]	10-15	30	2	2	66	15
-8A/B	15	24	2	3	100	10
-8C	15	20	2	2	100	10
-8E	15	20	2	3	125	8
-75	15	20	2	3	133	7.5
-7	14	20	2	3	143	7

*As a general rule, PCs used 2 clocks. [1]PC66 [2]PC100

Early SDRAMs specified 10ns for ${}^tWR$, or one clock cycle, since the maximum speed was 100 MHz. Although the ${}^tWR$ specification is generally stated as 10ns, the device actually requires one clock, more specifically the clock edge, when AUTO PRECHARGE is used, regardless of the frequency. However, one clock ${}^tWR$s are not easily obtainable for devices faster than 100 MHz as ${}^tWR$ severely limits process yields when a ${}^tWR$ speed less than 10ns is sought in conjunction with fast ${}^tRP$s (less than 24ns). With the PC market requiring only a two clock ${}^tWR$ at bus speeds above 66 MHz, DRAM manufacturers can ill afford to provide volumes of high speed SDRAMs with a one clock ${}^tWR$ at these high frequencies.

Although it is possible to achieve a one clock ${}^tWR$ at bus speeds above 66 MHz, it is impractical since the market demand for the SDRAM requires only a two clock ${}^tWR$ to achieve the fastest ${}^tRP$ and, even more important, the lowest cost, highest volume, high speed SDRAM solution. Micron's two clock ${}^tWR$ SDRAM is actually one clock plus time to provide for two clocks at fast frequencies, but it functions as a one clock ${}^tWR$ for backward compatibility to slower systems. Table 1 summarizes market-standard ${}^tWR$ and ${}^tRP$.

PRECHARGING AFTER A WRITE

As previously mentioned, once the last WRITE is complete, the SDRAM must wait ${}^tWR$ prior to ${}^tRP$ being applied. The ${}^tWR$ is best specified in terms of clocks when AUTO PRECHARGE is employed, as the SDRAM must predict when to "fire" the PRECHARGE command internally. In a synchronous device, the clock edge provides the best control to enable this function. When PRECHARGE, also known as manual PRECHARGE, is used, only a time specification is relevant.

With PRECHARGE, the user must provide a sufficient amount of time (i.e., enough NOP clocks) to ensure ${}^tWR$ is satisfied prior to the PRECHARGE command actually being given. For example, if ${}^tWR$ was specified as 15ns and the clock rate was 8ns, then the PRECHARGE command could not be applied until the second clock after the last WRITE. A tighter ${}^tWR$ of 10ns still requires two clocks. See Figure 1. With AUTO PRECHARGE, the user must account for both ${}^tWR$ and ${}^tRP$ prior to the ACTIVE command being applied. Figure 2 demonstrates how the timing budget of the previous example is to be used when closing a WRITE.

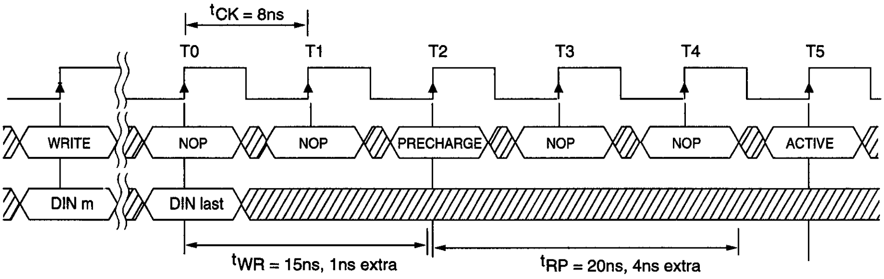


Figure 1
-8C WRITE TO PRECHARGE AT 125 MHz

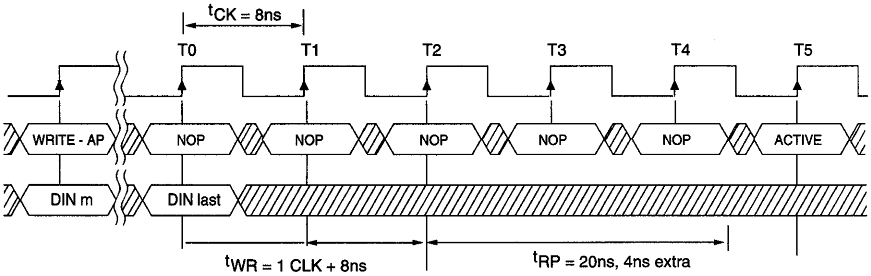


Figure 2
-8C WRITE WITH AUTO PRECHARGE AT 125 MHz

Although the SDRAM's ^{t}WR requires two clocks at fast frequencies (125 MHz), Figures 3, 4, 5 and 6 show both PRECHARGE and AUTO PRECHARGE requiring only one clock for ^{t}WR at slower frequencies. This is possible because Micron's two clock ^{t}WR SDRAMs employ a clock-plus-time specification rather than an actual two clocks of write-back time.

SUMMARY

SDRAM designs aiming for the lowest common denominator and supporting future SDRAM design constraints will use a ^{t}WR of two clocks. The Micron high speed SDRAMs are designed to provide the high speed devices for today and tomorrow, but also to support the legacy requirements of the slower bus speeds of yesterday.

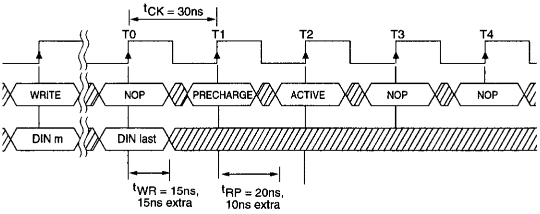


Figure 3
-8C WRITE TO PRECHARGE AT 33 MHz

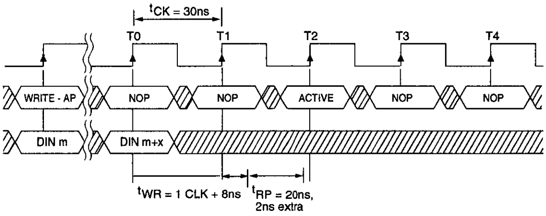


Figure 4
-8C WRITE WITH AUTO PRECHARGE AT 33 MHz

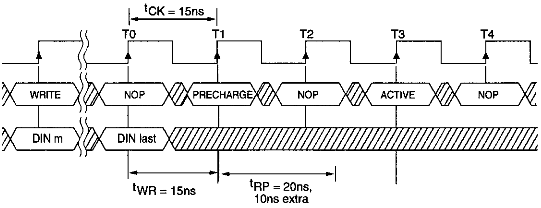


Figure 5
-8C WRITE TO PRECHARGE AT 66 MHz

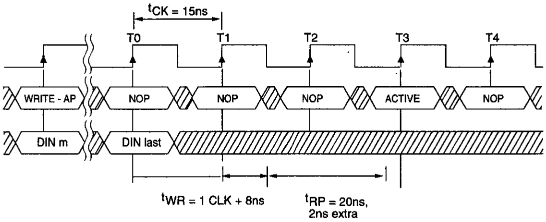


Figure 6
-8C WRITE WITH AUTO PRECHARGE AT 66 MHz

SRAM TECHNICAL NOTE SELECTION GUIDE

For the latest technical information on Micron products, read our quarterly technical newsletter *Design Line*.
Call 208-368-3900 to be added to our mailing list or visit our Web site (www.micron.com/mti/msp/html/dlindex.html).

TECHNICAL NOTE

SRAM THERMAL DESIGN CONSIDERATIONS

This article was originally published in 1993.

INTRODUCTION

As operating frequencies increase, memory components must dissipate more power to satisfy the needed reduction in permissible access time. SRAM thermal design considerations become increasingly important as power consumption approaches the package power dissipation limit. This technical note separately addresses thermal performance of Micron packaged SRAMs and SRAM die. Contact the factory for thermal information on any package not listed in this note.

DEFINITIONS

T_A = ambient air temperature (°C) at which the device is operated. The ambient temperature range of a device is listed under the "DC Electrical Characteristics and Operating Conditions" section of each SRAM data sheet. Commercial temperature range is 0°C to 70°C.

T_C = case temperature of the device (°C). In a packaged part this is the surface temperature at a point on the device package.

T_J = junction temperature of the active portion of the silicon die (°C). The absolute maximum recommended junction temperature of Micron SyncBurst SRAMs is 150°C (a lower maximum junction temperature is recommended for device operation). All Micron SRAMs are tested for high temperature operating life (HTOL) at 125°C ambient and 4.3V. Under HTOL conditions, the failure rate of a 2Mb SyncBurst SRAM is 280 FITs, compared with 5 FITs at 50°C ambient and 3.3V. The device will operate with junction temperatures in excess of 150°C, but much higher failure rates should be expected. Since the limiting factor in plastic components is the plastic mold compound, 155°C should never be exceeded anywhere in the plastic body.

P = average device power dissipation. Device power is dependent upon the operating conditions. SRAM data sheets indicate maximum IDD values that incorporate significant guardband (margin to guard against process changes, worst case VDD, etc.). Device power should be calculated to reflect the actual junction temperature, supply voltage, operating frequency and output loading conditions.

θ_{JC} = junction to case thermal resistance (°C/W). In a die-level product, the case is considered to be the surface of the die, which is bonded to the hybrid substrate. θ_{JC} is a function of the die thickness, area and number of bonds. In a packaged component, θ_{JC} is larger due to the extra thermal resistance of the package material thickness.

θ_{CA} = case to ambient thermal resistance (°C/W). In a die-level product, this is comprised of the θ_{CA} of the hybrid substrate plus packaging around the substrate if applicable. In a packaged component, this is a function of the surface area of the component (for convection and radiation) and the amount of heat conduction through the device leads. In applications where a heat sink is attached to the device, θ_{CA} is expressed as $\theta_{CS} + \theta_{SA}$, where θ_{CS} is the case to heat sink thermal resistance and θ_{SA} is the heat sink to ambient thermal resistance. θ_{CS} is normally very small, typically 0.3° C/W. θ_{SA} is mostly dependent upon the surface area of the heat sink. Under most circumstances, Micron SRAMs do not require heat sinks for reliable long-term operation.

θ_{JA} = junction to ambient thermal resistance. This is the sum of $\theta_{JC} + \theta_{CA}$.

Given the above parameters, T_J may be calculated using the following equation:

$$\begin{aligned} T_J &= T_A + P(\theta_{JC} + \theta_{CA}) \\ &= T_A + P\theta_{JA} \end{aligned}$$

DETERMINING THERMAL RESISTANCES

Micron's *Reliability Monitors,* published for each component family, detail the procedure used to determine thermal impedances. The procedure is summarized as follows: θ_{JC} and θ_{JA} are determined by mounting the IC package onto a four-layer PCB following the procedures outlined in JEDEC specification 51-2 using a K-type thermocouple glued to the top side of the package to measure the case temperature. The contact area is minimized so that the thermocouple does not act as a significant additional heat sink. Measurements are taken with the card socketed in a DIMM connector located in the center of a one-cubic-foot closed container that provides a still-air environment. The junction temperature is measured by characterizing the IC's input pin to substrate diode at various temperatures. The temperature-sensitive parameter (an input diode) is characterized by linear progression of temperature and V_T data. This regression equation is used to determine T_J, from which θ_{JC} and θ_{JA} are calculated. Characterization data generally indicate a 99.0 percent correlation to a linear curve fit.

The above discussion accounts for the determination of packaged component thermal properties. In actual applications, θ_{JA} is lower because printed circuit board traces conduct heat away from the package more efficiently than the test socket. θ_{JC} is essentially a constant; therefore, the user may determine the actual θ_{JA} by calculating θ_{CA}. This can be done by measuring the average device power, ambient air temperature and package surface temperature of the SRAM soldered in circuit and calculating as follows:

$$\theta_{CA} = (T_C - T_A)/P$$

θ_{JA} is simply the sum of the calculated θ_{CA} and the supplied θ_{JC}.

Table 1 summarizes the thermal resistances of Micron plastic package SRAMs rounded to two significant figures. Thermal resistance varies with die size. As shrink die become available, the thermal impedance may also vary. Contact Micron for the latest thermal resistance data.

TRUE SRAM POWER

SRAM power is determined by accounting for three components: power dissipation of internal operations, power dissipation due to transient output current (AC load current) and power dissipation due to steady state output current (DC load current). Data sheets generally contain worst-case numbers which, for IDD, usually occur at the fastest cycle time, coldest ambient temperature and highest voltage. Device data for specific operating voltages, temperatures and frequencies can be obtained from Micron, generally in the *Reliability Monitors*.

Table 1
PLASTIC SRAM THERMAL RESISTANCE OF A SYNCBURST SRAM SOLDERED ON A 108.0mm x 28.6mm, 4-LAYER PCB WITH STILL AIR

Device	Package	θ_{JC} °C/W	θ_{CA} °C/W	θ_{JA} °C/W
1Mb SyncBurst (x18, x32, x36)	100 TQFP	4	24	28
2Mb SyncBurst (x18, x32, x36)	100 TQFP	2	23	25

The following is a derivation from first principles, hopefully putting the issue to rest concerning how to calculate the extra power due to AC output load current:

$$P_L = \frac{1}{T}\int_0^T v\,i\,dt.$$

$$P_L = \frac{1}{T}\int_0^T (V_{DD} - V_L)\, I_L\, dt \text{ for LOW to HIGH case.}$$

$$P_L = \frac{1}{T}\int_0^T (V_L)\, I_L\, dt \text{ for HIGH to LOW case.}$$

Solving for the LOW to HIGH case
(substituting $I_L = C\frac{dV_L}{dt}$):

$$P_L = \frac{1}{T}\int_{V_{OL}}^{V_{OH}} (V_{DD} - V_L)\, C_L\, dV_L$$

$$= \frac{C_L}{T}\left(V_{DD}V_L - 0.5V_L^2\right)\Big|_{V_{OL}}^{V_{OH}}$$

$$= \frac{C_L}{T}\left(V_{DD}[V_{OH} - V_{OL}] - 0.5[V_{OH}^2 - V_{OL}^2]\right)$$

Solving for the HIGH to LOW case:

$$P_L = \frac{1}{T}\int_{V_{OL}}^{V_{OH}} V_L\, C_L\, dV_L$$

$$= \frac{C_L}{T}\left(0.5V_L^2\right)\Big|_{V_{OL}}^{V_{OH}}$$

$$= \frac{C_L}{T}\left(0.5[V_{OH}^2 - V_{OL}^2]\right)$$

where: C_L is the load capacitance.
VOH is the highest load voltage during the cycle.
VOL is the lowest load voltage during the cycle.
I_L is the load current resulting from C_L.
T is the device cycle time.
P_L is the power dissipation in the SRAM due to the output current on one DQ line.

These solutions make one important assumption: the output voltage waveform has no overshoot/undershoot. The presence of either overshoot or undershoot increases the SRAM power dissipation. True SRAM power for Micron synchronous devices is therefore:

$$P = V_{DD} \times I_{DD} + \sum P_{L} \text{ (for all output changes).}$$

The marginal power due to steady-state current flow into or out of the DQ pins (due to I/O leakage of connected devices) is ignored in the above equation because it is insignificant in most new design work. That extra power would be:

$$(V_{DD} - V_{OH})\, I_O N_H + V_{OL} I_I N_L$$

where VOH is the logic HIGH output voltage, I_O is output current on those DQ lines and N_H is the number of DQ lines that are HIGH; VOL is the actual logic LOW voltage, I_I is the resulting input current into the DQ line and N_L is the number of DQ lines that are LOW. Almost all CMOS devices have I_I or I_O less than 10µA (often 1 or 2µA); hence this calculation is inconsequential. If devices with high input currents are connected to the DQ lines, do not ignore this additional power component. For example, take the case where eight outputs are connected to loads having 10µA of leakage. The contribution to device power is (given that VOH is 3.8V during the average cycle):

$$(5V - 3.8V)\ 10\mu A\ (8) = 96\mu W$$

which can indeed be ignored. With higher leakage, VOH drops and power increases as a result of both increased current and greater voltage drop in the SRAM output driver.

DESIGN EXAMPLE

Use of thermal resistance information can be seen in the following example: An MT58LC64K36B3LG-10 SRAM operates up to an ambient temperature of 70°C with a 3.6V supply, READ and WRITE cycle times as fast as 15ns (66 MHz), continuous operation in still air and an output loading of 30pF. The following discussion demonstrates how this thermal resistance information is utilized.

In the MT58LC64K36B3 data sheet, the maximum device current at 15ns cycle time, 3.3V and 30°C is 200mA. The power is calculated as follows (assuming the worst case, all outputs switch from LOW to HIGH):

$$\begin{aligned} P &= I_{DD} \times V_{DD} + \frac{C_L}{T}\left(V_{DD}\,[V_{OH} - V_{OL}] - 0.5\,[V_{OH}^2 - V_{OL}^2]\right) \times 36 \\ &= 0.2(3.6) + \frac{30E\text{-}12}{15E\text{-}9}\left(3.6\,[3.0 - 0.1] - 0.5\,[3.0^2 - 0.1^2]\right) 36 \\ &= 0.72 + 0.428 \\ &= 1.148W \end{aligned}$$

The VOH used (3.0V) is typical for operation at 3.6V. At 3V and full-speed operation, VOH is approximately 3.0V. VOL is typically between 0.1V and 0V. If a lower voltage is used (for example, 3.3V vs. 3.6V), power dissipation curves vs. voltage and temperature can be used to give lower power values. These curves are available in the *Reliability Monitor*.

Given the true operating power of 1.148W, the case and junction temperatures can be predicted as follows:

$$\begin{aligned} T_C &= T_A + P\theta_{CA} \\ &= 70 + 1.148 \times 23 \\ &= 96.4^\circ C \\ T_J &= T_A + P\theta_{JA} \\ &= 70 + 1.148 \times 25 \\ &= 98.7^\circ C \end{aligned}$$

The calculated junction temperature is below the 150°C recommended limit demonstrating that the operating conditions are acceptable.

IMPROVING THERMAL PERFORMANCE

The motivation for achieving the lowest possible junction temperatures is twofold. Most AC timing parameters change adversely as junction temperature increases. This can be seen in any of the SRAM *Reliability Monitors* where AC timing specifications versus temperature are plotted. Another consideration is that component life decreases exponentially as temperature increases. Component life shows a strong correlation to the Arrhenius equation:

$$t_O = t_N \exp([Ea/k][1/T_O - 1/T_N])$$

where: t_O is the mean time to failure under the stress operating condition.
t_N is the mean time to failure under normal operating conditions.
Ea is the activation energy of failure modes, the most common one being dielectric defects, 0.3eV.
k is Boltzmann's constant, 8.617×10^{-5} eV/K.
T_N is the normal operating temperature (Kelvin).
T_O is the stress operating temperature (Kelvin).

Several considerations can improve thermal performance. Ground and power planes on a PCB can have a significant effect on conduction and therefore on power dissipation and safe operating temperatures. More power and ground leads on the device package produce greater relief. The addition of a thermal pad under the device with appropriate thermal bonding will also help conduct heat away from the device.

Airflow has a significant effect in reducing component temperatures. Table 2 shows test results for industry-standard packages, demonstrating the effective reduction in θ_{CA} as airflow increases (these results have *not* been verified by Micron). For example, a 1Mb SRAM in plastic SOJ having θ_{CA} of 48°C/W in still air would have a θ_{CA} of approximately 48°C/W x 0.75 or 36°C/W at 200fpm of airflow. The new θ_{JA} is approximately 36 + 2.0 = 38°C/W.

Table 2
EFFECTS OF AIRFLOW ON θ_{CA}

Package	Air Flow	θ_{CA} Multiplier
PDIP	200 fpm	0.7 - 0.75
PSOJ	200 fpm	0.7 - 0.75
PDIP	500 fpm	0.55 - 0.65
PSOJ	500 fpm	0.55 - 0.65

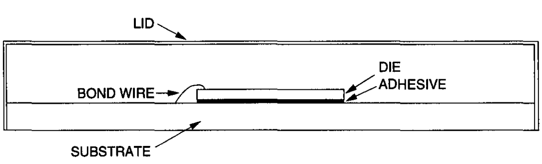


Figure 1
DIE APPLICATION

DIE THERMAL CONSIDERATIONS

Die-level thermal considerations are more complex for the user to handle because more factors are involved than with factory-packaged components. Figure 1 illustrates the thermal interfaces involved in a die application with ceramic substrate. Typical thermal resistances which need to be quantified are: die to adhesive, adhesive to substrate, substrate to lid, lid and/or substrate to ambient. The path is highly dependent upon the multichip module (MCM) construction. Heat radiation from die to lid could be an applicable factor. Thermal vias below the die would significantly reduce the total package thermal resistance and should be modeled appropriately.

An application which uses a ceramic substrate can use the θ_{JC} values provided for ceramic SRAMs as a conservative value. This accounts for thermal resistances from die to adhesive (assuming gold eutectic in ceramic packaged parts) and adhesive to substrate, and also for the effects of the bond wires. The value is conservative because the thermal resistance through the substrate material of Figure 1 is included, whereas this portion is actually unique to the substrate of each user. Without adjustment, this would be double-counting a portion of the thermal resistance.

Figure 2 illustrates the thermal resistances in a typical die application on silicon substrate. The following discussion uses a silicon substrate die application with four Micron 1Mb SRAM die mounted on the substrate. The die areas for

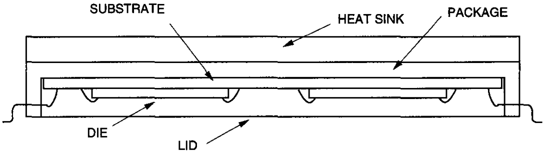


Figure 2
SILICON SUBSTRATE DIE APPLICATION

arious Micron SRAM die products are listed in Table 3. hermal resistance from junction to die backside for the Mb SRAM (S18A) is calculated as follows:

$$\theta = (0.0185 \text{ inch die thickness}) / (2.23\text{W}/°\text{C}/\text{inch}) \; / \; (0.107 \text{ sq. inches die area}) = 0.08°\text{C}/\text{W}$$

The remaining thermal resistance values are user-lependent and also dependent upon contact area. Some ypical values are 0.06°C cm^2/W for the die to silicon ubstrate interface, 0.2°C cm^2/W through the silicon subtrate, 0.7°C cm^2/W silicon substrate to module carrier, .6°C cm^2/W through the aluminum module carrier, 0.7°C m^2/W from module carrier to heat sink and 30°C cm^2/W rom heat sink to ambient. For an MCM with four SRAMs lissipating the 1.02W of the previous example with cm x 3cm dimensions, the calculations would be as follows assuming 70°C ambient is in still air):

$$_{\text{heat sink}} = 70°\text{C} + (30°\text{C}/\text{W}/9\text{cm}^2) \times 1.02\text{W} \times 4 = 83.6°\text{C}$$

$$_{\text{module carrier}} = 83.6°\text{C} + (0.6 + 0.7°\text{C cm}^2/\text{W})/9\text{cm}^2 \times 1.02\text{W} \times 4 = 84.19°\text{C}$$

$$_{\text{silicon substrate}} = 84.19°\text{C} + (0.2 + 0.7°\text{C cm}^2/\text{W})/9\text{cm}^2 \times 1.02\text{W} \times 4 = 84.60°\text{C}$$

$$_{\text{junction}} = 84.60°\text{C} + (0.06°\text{C cm}^2/\text{W}/0.691\text{cm}^2 + 0.08°\text{C}/\text{W}) \times 1.02\text{W} = 84.77°\text{C}$$

his MCM type, as seen from the example, is very well uited for much higher power dissipation devices than the our SRAMs used in this example. Eliminating the heat sink ould alter the analysis (using 170°C cm^2/W for the modle carrier package to air thermal resistance):

$$_{\text{module carrier}} = 70°\text{C} + (0.6 + 170°\text{C cm}^2/\text{W})/9\text{cm}^2 \times 1.02\text{W} \times 4 = 147.34°\text{C}$$

$$_{\text{junction}} = 147.51°\text{C}$$

Table 3
MICRON DIE INFORMATION

Configuration	Data Base	Dimensions (mils)	Area cm^2	θ^1 °C/W
32K x 8	S06	167 x 346	0.373	0.144
128K x 8	S01	241 x 544	0.846	0.063
128K x 8	S18A	210 x 510	0.691	0.078

NOTE: 1. This is the thermal resistance from junction to die backside (calculated value).

The junction temperature is calculated using the same methodology as before. This indicates that a heat sink can significantly help component lifetime in this example since component lifetime is exponentially related to temperature.

SUMMARY

Thermal analysis and design have become an important consideration in SRAM applications. The benefit to the end user when these considerations are properly accounted for is higher system reliability due to longer component life. For the designer, thermal design techniques result in knowledge of device junction temperatures over the operating temperature range, which directly leads to an understanding of device characteristics under the varying operating conditions. In die applications, thermal considerations are an essential part of the design task. Analysis tools based on finite element and finite difference techniques are frequently used to predict temperatures throughout MCM assemblies. Tables included in this note provide thermal resistance values which are useful in analyzing both die and packaged component applications.

TECHNICAL NOTE

HIGH-SPEED MEMORY DESIGN TECHNIQUES

This article was originally published in 1994.

NTRODUCTION

Over the last 20 years microprocessor clock speeds ave increased at an exponential rate. As we can see from igure 1 below, clock speeds have migrated from 1 MHz with the Intel® 4004 to 500 MHz with the latest version of the Alpha processor. A parallel increase in bus speeds has ccurred with current systems having cycle rates of 60 MHz nd 66 MHz and moving toward 75 MHz and 100 MHz.

Design techniques which were used at slower frequen-ies (33 MHz and lower) are no longer appropriate for these igher bus frequencies. More attention must be paid to oard layout, bus loading and termination to ensure that hort clock cycle times can be met without noise, ringing, rosstalk or ground bounce. This article discusses these issues and the choices a designer faces in high-speed memory ystem design.

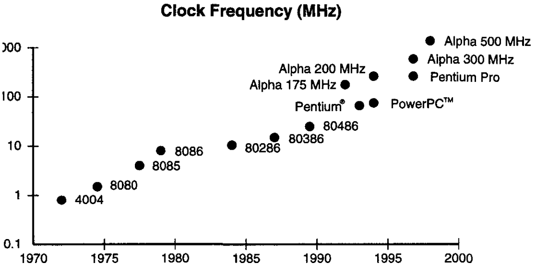


Figure 1
MICROPROCESSOR CLOCK SPEEDS

THE MEMORY HIERARCHY

Figure 2 shows the memory hierarchy conventionally used in a computer system. High-speed cache memory integrated with the microprocessor is used to store frequently accessed instructions and data and to avoid the time penalties associated with off-chip accesses. However, only a limited amount of cache can be included directly on the chip in the level one (L1) cache (sizes vary from 8KB to 32KB). High-speed secondary or level two (L2) cache is included in systems to increase system performance. Sizes for the L2 cache vary depending on the application software. The largest portion of data, stored in the DRAM bulk memory array, is significantly slower and has a large access time penalty. If a cache miss occurs, retrieving data from the DRAM array could take up to six or more processor clock cycles, drastically reducing system performance.

High-speed techniques must be used in evaluating data transfers between the cache SRAM and microprocessor. Timing between the cache and microprocessor is especially critical because of the short cycle and access time required. Bus frequencies are already at 66 MHz and require careful design to attain zero-wait-state performance. At these frequencies designers increasingly use synchronous SRAMs to help alleviate timing problems, but even synchronous SRAMs require a thorough timing analysis.

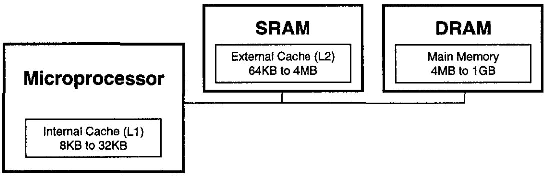


Figure 2
TYPICAL PC MICROPROCESSOR MEMORY CONFIGURATION

A CACHE TIMING EXAMPLE

The following example demonstrates how little timing margin is available for bus speeds exceeding 50 MHz and why it is important to analyze bus timing carefully when designing memory subsystems at these frequencies. For this example, we assume that the microprocessor operates at 60 MHz and is using a synchronous cache array organized as 64K x 72, with two 64K x 36 SyncBurst SRAMs (MT58LC64K36B3) as shown in Figure 3.

The timing of a READ cycle for this system is shown in Figure 4. The equation below shows how to calculate the amount of timing margin available in any design. The variable ^tCLK represents the clock cycle time of the external bus. For a 60 MHz system this represents a 16.7ns cycle time.

$$\begin{aligned} t_{margin} &= t_{clk} - t_{flight} - t_{setup} - t_{access} \\ &= 16.7 - 1.4 - 4 - 10 \\ &= 1.3\text{ns} \end{aligned}$$

In this example a READ cycle is being performed which sends data from the SRAM cache memory to the microprocessor. This example assumes that the address and control signals are valid during the positive edge of the clock pulse and exceed the setup time of the SRAM. In a synchronous system the memory clock cycle begins with the rising edge of the clock which signals the SRAM to use the address on the bus, find the data stored at this address and send it to the outputs. The data appears at the output t_{access}ns later (10ns for this example). Once data appears at the output, it must travel from the SRAM to the microprocessor through signal traces on the circuit board. This transfer time is called t_{flight} and can vary greatly. Lastly, the microprocessor must latch the data and it must be available to meet the processor setup time (t_{setup}). The hold time must also be met, but it occurs after the rising edge of CLK and does not have to be subtracted as part of the timing calculation.

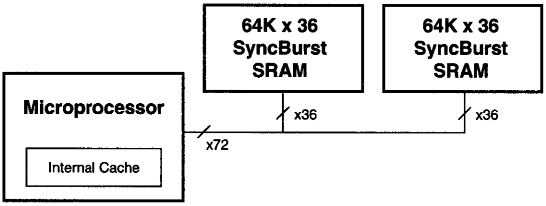


Figure 3
SYNCHRONOUS CACHE MEMORY DESIGN USING TWO MICRON 64K x 36 SRAMs

Altogether the total time is 15.4ns and the requiremen for 60 MHz operation is anything less than 16.7ns. Th margin for error is 1.3ns, and board layout or other factor can easily exceed this. In the next section we will discus how t_{flight} can vary. Even with careful design, a t_{flight} of les than 2ns may be very difficult to obtain. Typical times i some designs could be 3ns to 5ns or more. It is no longe sufficient just to connect components without considerin the timing impact to the system.

CALCULATING t_{flight}

t_{flight} consists of the components shown in the equatio below:

$$t_{flight} = t_{clock\ skew} + t_{propagation\ delay} + t_{rise\ time}$$

The first component, $t_{clock\ skew}$, can be defined as th skew between rising and falling edges of the clock signa for different components on the board. If a clock rises a time t = 0 on the microprocessor clock input, the clock inpu to the first SRAM might rise at time t = 0.25ns and t = 0.45n on the second. This skew in timing can be due to uneven lin lengths or varying load capacitances on the different lines If a series of buffers is used to distribute the clock signal

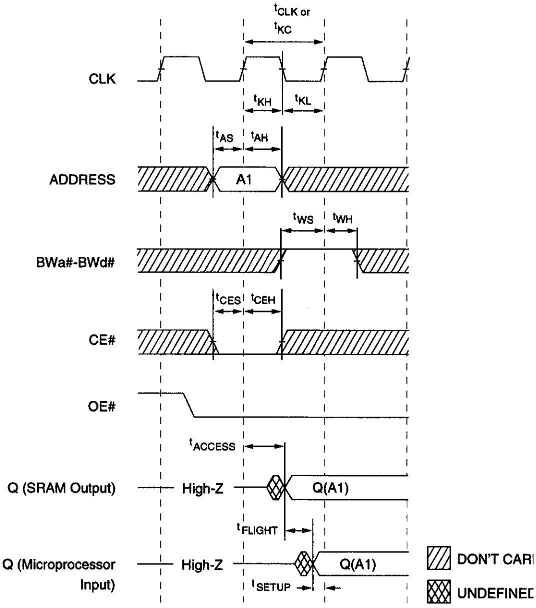


Figure 4
READ CYCLE TO CACHE MEMORY

lelay times through these buffers will also vary and add o the skew. These types of skew are frequently ignored or slower systems but must be accounted for in high-erformance ones.

The second component, $t_{propagation\ delay}$, is determined hrough the characteristics of the transmission line and line oad. The propagation delay now consumes a considerable ortion of the cycle time of a high-speed system and can no onger be ignored. Designers cannot assume that outputs lrive purely capacitive loads and must determine if inter-onnects should be treated as transmission lines. A purely apacitive load assumes an RC time constant delay consisting of trace resistance, output driver resistance and total lumped capacitance. Transmission line analysis, although more difficult, more accurately reflects actual conditions. Determining propagation delay is discussed in more detail in the next section.

The next component, $t_{rise\ time}$, is determined by the speed of the component driving the line. A faster rise time can help speed the cycle time of a system but may require a huge output driver with a large current dissipation. Rise times can also vary from component to component and worst-case times should be used for design analysis.

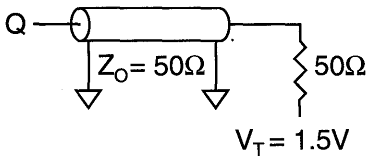


Figure 5
OUTPUT LOAD EQUIVALENT

A component that should not be ignored is circuit loading. The external capacitive loading is usually accounted for in the access time of the device (t_{access}). A device will have an access time rating that is valid up to a given loading. For example, high-speed synchronous SRAMs are usually rated with an AC loading as shown in Figure 5 with a capacitive rating of 30pF. Designers can modify their timing margin if the capacitive loading is less than or greater than the specified rating. The equation below shows how timing can vary with capacitive loading above or below the rated specification. The difference between the rated capacitive load and the actual capacitive load is represented by the variable ΔC_L ($\Delta C_L = C_{actual} - C_{rated}$).

$$\Delta T_{KQ} \cong 0.0195 \frac{ns}{pF} \times \Delta C_L\ pF + 0.0816ns$$

CIRCUIT TERMINATION

Unterminated Lines

Because electrical signals travel at a finite velocity through a circuit board, it is necessary to determine how long they take to propagate from driver to receiver. This length of time determines if the output circuit requires termination. As an example, assume that a circuit board uses a polyimide dielectric with a relative dielectric constant (ε_r) of 3.5. Common dielectric constants are shown in Table 1. If the circuit board has a strip conductor and a ground plane separated by a dielectric medium as shown in Figure 6a (microstrip line), we could use the following equation to calculate the signal speed:

$$T_d = 0.004\sqrt{0.45\varepsilon_r + 0.67}\ \text{ns per mm}$$

For this circuit board the equation gives us a signal velocity of 6ps/mm. If the signal conductor were instead sandwiched between two power planes (Figure 6b), we could use a stripline equation to calculate the signal velocity.

$$T_d = 0.004\sqrt{\varepsilon_r}\ \text{ns per mm}$$

For the same circuit board we now have a signal velocity of 7.5ps/mm. The equations above give valid results for reasonable values of trace widths, dielectric constants and dielectric thicknesses. Books are available on transmission line theory for a detailed analysis of propagation delay for various structures.

The purpose of calculating a delay time for signals is to determine if the circuit delay can be treated as an RC time constant. This can be done if the maximum trace length meets the following inequality:

$$L_{MAX} < \frac{t_r}{2T_d}$$

t_r = Rise time or fall time of the output driver

Table 1
VARIOUS DIELECTRIC CONSTANTS

Material	Relative Dielectric Constant (ε_r)
Ceramic - Alumina	9.4
FR-4	4.7
Glass Epoxy	4.0
Polyimide	3.5
Silicon	11.8

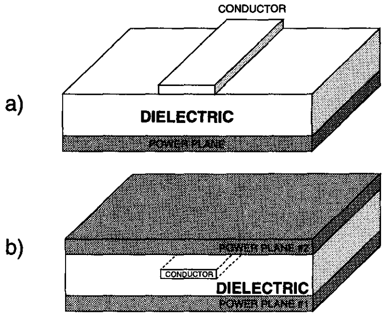


Figure 6
a) MICROSTRIP LINE, b) STRIPLINE

For our example we assume a rise or fall time of 2ns. This means that as long as the maximum line length is less than 133mm or 5.2 inches (for stripline), the circuit delay can be treated as an RC time constant. For a given capacitive load we can calculate the actual signal propagation time using the equation:

$$T_{ld} = T_d\sqrt{1+\frac{C_L}{C_o}}\text{ ns per mm}$$

C_L = Load Capacitance
C_O = Transmission Line Capacitance
where:

$$C_o < \frac{T_d}{Z_o}$$

Z_O = Characteristic impedance of the signal trace

For our stripline example, C_O = 1.5 pf/cm and the load is C_L = 50pf with a 5cm transmission trace length. The actual signal velocity is 22 ps/mm or 1.1ns for 5cm of line length. For this example we assumed a value of Z_O of 50Ω. This value can be calculated using the equations below, or supplied from a board vendor. It is recommended that a designer use computer software to determine Z_O instead of these equations which are only approximate.

For stripline:

$$Z_o = \frac{30\pi(1-t/b)}{\sqrt{\varepsilon_r}\,(W_e / b + C_f/\pi)}$$

where:

$$C_f = 2\ln\left(\frac{1}{1-t/b}+1\right)-\frac{t}{b}\ln\left\{\frac{1}{(1-t/b)^2}-1\right\}$$

$$W_e = W - \left\{\frac{(0.35 - W/b)^2}{1+12t/b}\right\}$$

W = width of strip conductor
t = thickness of strip conductor
b = dielectric thickness

These stripline equations are relatively accurate if the following limitations are met:

$$0.05 \le W/(b-t) \le 0.35$$
$$t/b \le 25$$

Terminated Lines

If line lengths are greater than L_{MAX}, the above equations can no longer be used and terminations should be considered. For these situations users should use simulation tools to define and analyze their distributed element circuit accurately. Several considerations for terminated lines are discussed in this section.

When transmission line analysis is used, the designer must determine if the design will use incidence-wave or reflected-wave switching. Incidence-wave switching is potentially the quickest way to drive external devices because it does not depend upon the reflected signal to exceed V_{IH} or V_{IL}.

Incidence-wave switching has the drawback that large amounts of power can be generated in the output driver of a chip. Let's calculate what the power of one I/O signal can be using this method. First, the effective characteristic impedance must be calculated using the equation below:

$$Z_L = \frac{Z_O}{\sqrt{1+\frac{C_L}{C_O}}}$$

For our example in the previous section, using a value of Z_o of 50Ω and a transmission line of 10cm, Z_L is equal to 24Ω. We can use this number and the output impedance of the driver to determine the instantaneous switching current of the outputs. If the output driver impedence is 25Ω, we will see an instantaneous current of 100mA. A circuit implementation using wide devices could generate a large noise spike that would be very difficult to decouple. The reflection at the end of the line must also be accounted for.

Reflected-wave switching can cut power and noise dramatically because the driving circuit needs to generate only half the output voltage upon switching as the incidence-wave solution. The signal initially propagates at half the required voltage level until it hits the end of the transmission line. Then the reflection causes the voltage level to double. Because the reflected-wave is used, time must be allotted for the reflected-wave propagation. This method was adopted for use in the Peripheral Component Interconnect (PCI) bus.

TYPES OF TERMINATION

Several types of termination are commonly used in designs. The first (shown in Figure 7a) is series-resistance termination. A resistor is connected between the output of a driver and the driven elements. A reflected wave from the load which reaches the output can again be reflected, generating noise in the output signal. The series-termination is used to prevent this type of reflection. This is done by making the output resistance (R_{device}) of the driver plus the series resistor (R_S) equal to the line impedance or:

$$R_S = Z_O - R_{device}$$

There is a potential disadvantage to the series termination resistor because of the associated voltage drop. This voltage drop could cause problems with noise margin to V_{OH} and V_{OL} and in a bidirectional signal with V_{IH} and V_{IL}. CMOS device inputs have a high impedance and only initial AC power is needed to charge/discharge capacitance. Once the output reaches the final level, current dissipation (and voltage drop) across R_S is minimal in CMOS circuits.

In addition to preventing reflection problems, series termination is commonly used in mixed-voltage systems to prevent high currents. In Figure 8, a 5V device is driving a 3.3V input. Many 3.3V devices contain a protection diode which is connected to 3.3V. If the input was driven to 5V, the diode would become forward-biased and would generate a low resistance path to V_{DD} which could result in potentially damaging currents. In this case, the series termination resistor has the added advantage of limiting the current in these mixed-voltage systems.

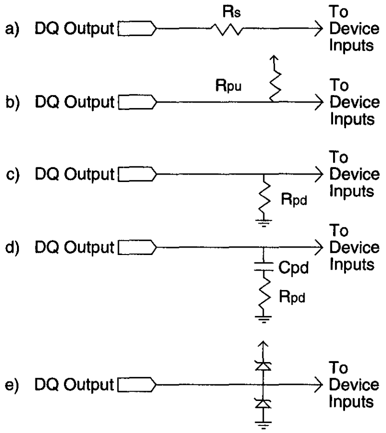


Figure 7
a) SERIES-RESISTANCE TERMINATION
b) PULL-UP TERMINATION
c) PULL-DOWN TERMINATION
d) RC TERMINATION
e) SCHOTTKY DIODE TERMINATION

Figures 7b and 7c show pull-up and pull-down termination. A pull-up and pull-down resistor could be also used simultaneously. The main disadvantage of this type of design is that there is a DC power dissipation associated with the devices. For instance, for the pull-up case, there is a DC current path when the output driver is low. This extra current is unacceptable in portable or notebook applications. Mixed 5V and 3.3V designs are recommended to use a pull-up to a 3.3V supply versus a 5V one wherever possible to reduce power consumption.

Another advantage of pull-ups is in connecting TTL-level outputs to CMOS-level inputs. TTL outputs have a V_{OH} specification of 2.4V versus a CMOS V_{IH} of 3.15V. CMOS input levels occur in low-power microprocessors and microcontrollers used in portable and hand-held applications. The pull-up to 5V will allow fast SRAMs with TTL-I/O to drive these CMOS circuits.

RC termination (Figure 7d) allows for proper termination without an associated DC current component. The disadvantage of this approach is that it requires an extra component, the capacitor. An advantage is that this circuit acts as a low-pass filter and can absorb unwanted glitches. Care must be taken in the choice of a capacitor since it must be large enough to absorb glitches that may occur in the system but small enough so it does not slow down the system.

Lastly, Schottky diode termination (Figure 7e) can be used to save power over resistance termination techniques. The advantage of this method is that it prevents overshoot and undershoot problems. The diode turns on if the voltage goes above $V_{DD} + V_{diode}$ or below $V_{SS} - V_{diode}$. The main advantage of this technique is in prototypes constructed with wire wrap or breadboards where line impedance may not be constant. These diodes provide termination without requiring detailed impedance matching calculations.

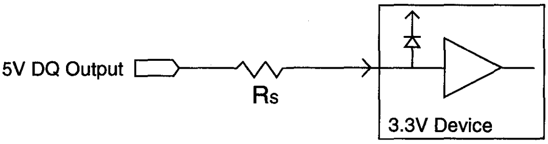


Figure 8
DIODE PROTECTION IN 3.3V CIRCUITS CAN CAUSE PROBLEMS IN MIXED 5V-3.3V SYSTEMS

FUTURE TRENDS

The computer industry always moves toward faster architectures. To meet the bus speeds of the future with 10ns bus cycle times (or faster), new I/O standards such as 2.5V I/O, HSTL (high-speed transceiver logic) need to be incorporated into designs to minimize output voltage swings and drive transmission lines. Even with these new standards, designers need to analyze their circuit thoroughly to ensure that cycle/access times are met.

CONCLUSION

As we have seen in this article, high-speed bus design requires detailed analysis to ensure that the system will work properly. A proper analysis of clock skew and propagation delay is essential to ensure that the system will work properly and with the required performance. This detailed analysis is essential for bus speeds over 50 MHz.

TECHNICAL NOTE

INTERFACING WITH LVTTL SRAMs

This article was originally published in 1992.

INTRODUCTION

High-speed 3.3V synchronous SRAMs use LVTTL I/O to communicate with other devices. However, not all of these other devices operate at LVTTL levels. In order to communicate with non-LVTTL components, additional interface logic may be required. This technical note describes how to use Micron SRAMs in these situations.

TYPES OF INTERFACE LEVELS

Most applications which use synchronous SRAMs require one of four different types of I/O: TTL, CMOS, LVTTL or LVCMOS. The voltage levels for these are shown in the table below. Because the majority of Micron's SRAM families operate with 3.3V LVTTL I/O, this note will discuss interfacing LVTTL to the three other types of I/O.

TTL- vs. CMOS-LEVEL OUTPUTS

There are advantages and disadvantages to both TTL- and CMOS-level I/Os. CMOS levels are used in systems to minimize DC power dissipation. CMOS outputs typically drive at VDD - 0.2V or higher for a logic one signal or 0.2V or ower for a logic zero signal. These CMOS levels ensure that he input buffer of any driven device has transistors which are in the cutoff region of operation and therefore have very ow current dissipation during steady-state operation. Beause of this, CMOS-level outputs are most desirable on ystems such as battery-powered devices which are conerned with minimizing power.

TTL-level outputs have a smaller output swing than CMOS devices and are most commonly used in high-speed systems. Minimizing the output swing is important in high-speed systems because it allows the outputs to transition quickly. For example, if the output swing is minimized from a 4V swing to a 3V swing and the ramp time is 2V/ns, 0.5ns can be saved in access time. Although this may seem insignificant, it is critical as microprocessor bus speeds approach 100 MHz and access times of 5ns. High-speed SRAMs use TTL or LVTTL output levels to maximize performance.

3.3V LVCMOS

The first situation to consider is the case of an LVTTL output driving an LVCMOS input. When LVCMOS runs at a nominal VDD supply of 3.3V, VIL is 0.2 VDD. For a VDD range of 3.1V to 3.6V, this means that VIL can range from 0.62V to 0.72V. The maximum VOL of an LVTTL device is 0.4V so the low end can be met.

For the output high voltage and for the same VDD range, VIH can range from 2.17V to 2.52V. The guaranteed VOH for the LVTTL device is 2.4V meaning that at the high VDD range, the VIH for the LVCMOS device will not be met.

To meet the VIH for the LVCMOS device, a pull-up resistor can be added to the output and connected to VDD. The pull-up will drive the output higher than VOH. It will be necessary to choose a resistor value that will drive the output RC time constant in a reasonable time, but not too low so that there is excessive current draw when the LVTTL device is driving to GND.

Table 1
FOUR DIFFERENT TYPES OF I/O SIGNAL LEVELS

I/O	TTL	CMOS	LVTTL	LVCMOS
VIL	0.8	0.3 × VDD	0.8	0.2 × VDD
VIL (MIN)	-0.5	-0.3	-0.3	-0.5
VIH	2.2	0.7 × VDD	2.0	0.7 × VDD
VIH (MAX)	VDD + 1V	VDD + 0.3	VDD + 0.3	VDD + 0.5
VOL (MAX)	0.4	0.2	0.4	0.1[1]
VOH (MIN)	2.4	VDD - 0.2	2.4	VDD - 0.1[1]

[1] Specified at 20µA.

5V TTL

Next, let's look at an LVTTL signal driving a 5V TTL input. In this case, VOH is at least 2.4V and VIH for TTL is 2.2V, VOL is 0.4V and VIL is 0.8V. So far, so good.

When TTL drives LVTTL, VOH is at least 2.4V and VIH is 2.0V, VOL is 0.4V and VIL is 0.8V. Although these levels meet the input requirements for LVTTL, the maximum voltage can frequently be a problem. TTL circuits can drive near the VDD rail (~5V) when in steady state. The JEDEC standard for maximum input voltage in LVTTL is VDD + 0.3V.

Buffering may be necessary between TTL outputs and LVTTL inputs. If the TTL circuit drives above VDD + 0.3V, then this could cause a reliability problem in the SRAM. Some TTL circuits have "3.3V-friendly I/O," meaning that they restrict the output high voltage of the device so that they can drive either TTL or LVTTL without buffering. Also, ASIC or gate array vendors may provide I/O that is 3.3V-friendly. Using this type of I/O to restrict VOH (MAX) is preferred when designing a memory interface.

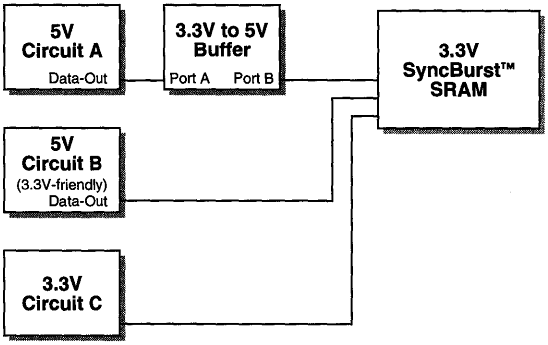


Figure 1
CONNECTING 5V CIRCUITRY TO
3.3V I/O SRAM

5V CMOS

5V CMOS I/O presents the same challenge as TTL when driving LVTTL because the output will drive to the VDD rail and may be destructive to the LVTTL circuit. Meeting the VIH and VIL of CMOS devices poses no problems, as CMOS drives at VOL of 0.2V and VOH of VDD - 0.2V. A buffer circuit of some sort will be required.

LVTTL driving 5V CMOS presents a challenge because of the input levels required. The VIH of a 5V CMOS can range from 3.15V to 3.85V, depending upon VDD, which is not readily met with LVTTL which has a VOH (MIN) of 2.4V. VIL is not a problem, as it ranges from 1.3V to 1.65V. One solution to this issue is a pull-up resistor or buffer circuit between the LVTTL output and CMOS input in order to meet the VOH requirements of the circuit.

BUFFER CIRCUITS

5V TTL or 5V CMOS I/O may require some buffering circuit between the circuit and the SRAM. Figure 1 shows three ways of connecting 5V circuitry (TTL or CMOS) to 3.3V SRAMs. If VIH is too high, a buffer must be used to protect the device. Some vendors' SRAMs may have protection diodes which will become forward-biased if VIH is too high. A current-limiting resistor should be used with those components. Lastly, 5V circuitry with 3.3V-friendly I/O can be connected directly to the SRAM.

HSTL AND 2.5V I/O

High-speed transceiver logic (HSTL) and 2.5V I/O SRAMs are starting to appear in some of Micron's SRAM product lines. To connect these I/O lines to other voltage levels, a similar analysis procedure should be followed as shown in this paper.

Micron 2.5V I/O SRAM inputs can directly take a 3.3V LVTTL signal since they are 3.3V-tolerant. The bidirectional I/O on the 2.5V I/O SRAMs is not 3.3V-tolerant, and any device driving a 2.5V DQ line should not exceed VDDQ + 0.3V.

CONCLUSION

SRAMs using TTL or LVTTL outputs can be connected t 3.3V or 5V devices if proper analysis is done with the circui In some cases this may require some type of buffer circuitry This article has shown how these SRAMs can be used i mixed-voltage systems or with CMOS-level devices.

TECHNICAL NOTE

DENSITY UPGRADES FOR MICRON® SRAM

This article was originally published in 1998.

INTRODUCTION

Because of Moore's Law, memory density is constantly increasing. Designers increase memory size by using the next generation device. The upgrade to higher densities, however, has not always been easy since pinouts vary between generations. Micron's synchronous SRAM product lines have easy upgrade paths that use compatible pinouts between generations; thus, one board design can accommodate multiple generations of memory. This article discusses the TQFP upgrade path for Micron's SRAM product family.

TQFP-PACKAGED DEVICES

ZBT™

The Micron® ZBT™ family is currently available in a 100-pin TQFP package. A density upgrade path has been defined from 2Mb to 16Mb (Figure 1), offering designers two clear advantages.

First, a designer needing a 2Mb (64K x 32) ZBT could use the 2Mb pinout as shown in Figure 1. The 4Mb, 8Mb and 16Mb ZBT SRAMs have identical pinouts except for the extra address pins (50, 83 and 84). If these pins are grounded, a board can accept any of these larger densities in place of a 2Mb device. If a product has a long life expectancy, higher-density devices can be used when lower-density devices become more difficult or impossible to obtain. The designer does not have to respin the board if an older generation product becomes obsolete.

Another advantage of common pinouts relates to memory upgrades. When a design uses 4Mb parts and a new software upgrade requires doubling the memory, the upgrade can be accomplished by replacing the 4Mb parts with 8Mb devices. No board redesign is required as long as the extra address lines for the higher-density device have been routed in the first design to accommodate higher-density parts later.

SYNCBURST™

The SyncBurst™ family of devices currently consists of memory densities from 1Mb to 8Mb, with a memory upgrade path defined through 16Mb. The 1Mb and 2Mb devices are available in a TQFP package, and the 4Mb, 8Mb, and 16Mb devices are available in TQFP and BGA packages.

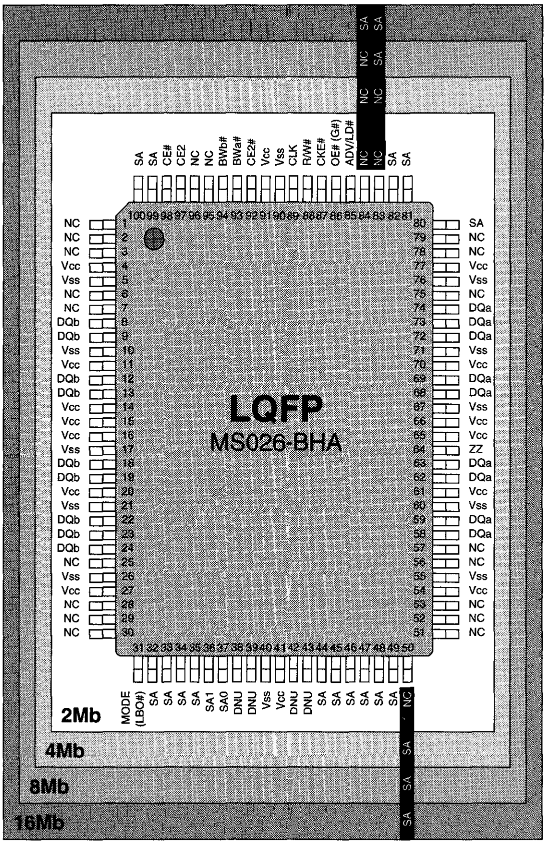


Figure 1
ZBT SRAM PINOUT

Two standard pinouts exist for 8Mb and 16Mb SyncBurst devices in a TQFP package (Figures 2 and 3). For the purposes of Micron's numbering system, Figure 2 is referred to as the "T" version and Figure 3 is referred to as the "S" version. Both of these standards are supported by Micron, as the market is split at this time.

The pinouts in Figures 2 and 3 are essentially the same, except for the address upgrade pins for the 8Mb and 16Mb densities. The T version uses pin 43 as the address upgrade pin for the 8Mb device, and pin 42 for the 16Mb device. The S version uses one of three chip enables as an address bit (the CE2# chip select becomes the additional address pin [pin 92]) for the 8Mb; CE2 becomes the additional address pin (pin 97) for the 16Mb, leaving only one chip select (pin 98). For banked applications at the 16Mb level, the additional chip selects will have to be implemented inside of the control ASIC or with a discrete inverter.

CONCLUSION

Standard upgrade paths allow engineers to design for future memory needs by routing all of the address lines on a board to accommodate higher-density memory, thus lengthening product life and improving supply options as lower-density markets tighten.

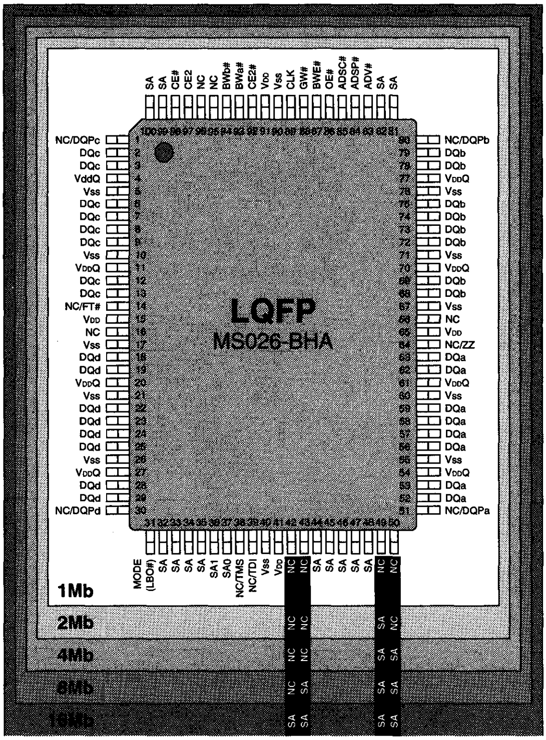


Figure 2
SYNCBURST SRAM (x32/x36)
T VERSION

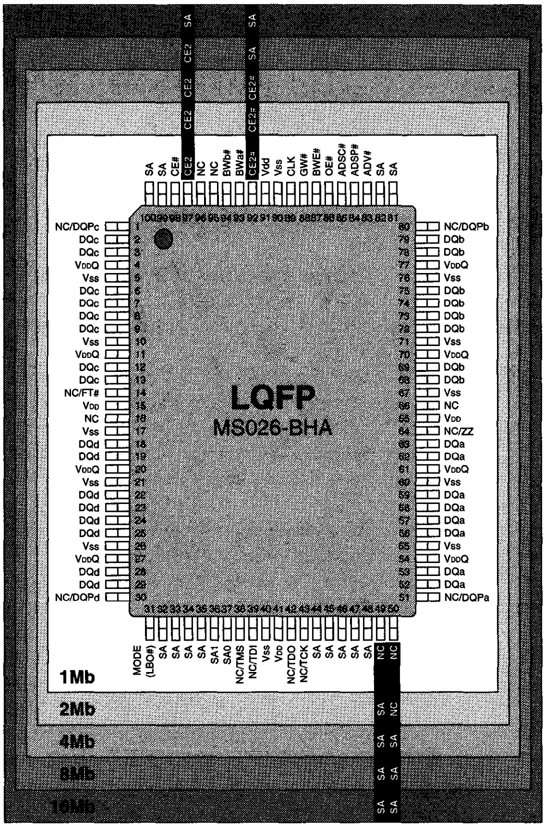


Figure 3
SYNCBURST SRAM (x32/x36)
S VERSION

TECHNICAL NOTE

DESIGNING WITH ZBT™ SRAMs

This article was originally published in 1997.

INTRODUCTION

Zero Bus Turnaround™ (ZBT™) SRAMs offer the ultimate in bus utilization because they can be used without any bus dead cycles, even when transitioning from READ to WRITE. In other words, ZBT SRAMs can read or write every clock cycle for 100 percent bus efficiency. They represent the next generation of SRAMs beyond SyncBurst™, incorporating simpler control logic and higher bandwidth at the same frequencies. This article describes why ZBT was developed and answers design questions regarding bus contention at high frequencies.

ZBT vs. SYNCBURST™

Micron developed SyncBurst SRAMs specifically for PC cache applications such as Pentium® and PowerPC™, but the use of SyncBurst SRAMs has not been limited to PCs. As the only widely available, high-speed SRAM solution, they have also been used extensively in non-PC applications, including networking, telecommunications, digital signal processing (DSP), and medical and test equipment. ZBT, on the other hand, is designed specifically for non-PC applications and optimized for ease of use and higher bandwidth. Current users of SyncBurst SRAMs may consider migrating to ZBT. The pinout of the ZBT SRAM is virtually identical to the SyncBurst SRAM; both devices have the same address and data pins and almost identical pins for control and voltage. Minimal redesign of a circuit board could be advantageous, considering the higher bandwidth of the ZBT.

SIMPLER CONTROL LOGIC

SyncBurst SRAMs have been used in non-PC applications despite drawbacks in terms of more complicated control logic. With the benefit of simplified control logic, ZBT uses fewer control signals than SyncBurst to accomplish the same basic operations. Figure 1 shows five SyncBurst control signals compressed into two ZBT signals.

The SyncBurst SRAM requires three signals (ADSP#, ADSC# and ADV#) to load commands and perform burst operations. In a cache application, both the processor and cache controller "talk" to the SRAM, and each has its own control signal to the SRAM. They also write differently to the SRAM. The processor uses a LATE WRITE cycle where data is required one cycle later than address and is controlled by ADSP#. The cache controller uses an EARLY WRITE cycle where data and address appear on the same clock edge and are controlled by ADSC#. ADV# is used to advance the burst logic counter in the SRAM.

ZBT uses one signal, the advance/load# pin (ADV/LD#), to perform the same commands as ADV#, ADSP# and ADSC#. When ADV/LD# is LOW, a READ or WRITE command is given to the SRAM, depending upon the state of the read/write# pin (R/W#). A DESELECT command may also be executed if one of the three chip enables is inactive. When ADV/LD# is HIGH, a BURST command is performed. (The BURST command is optional as many applications do not require it.)

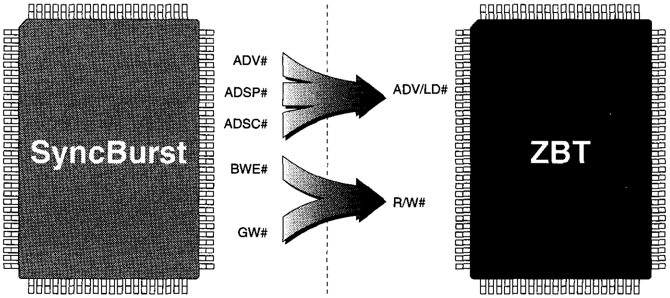


Figure 1
ZBT ELIMINATES CLUTTERED CONTROL LOGIC OF SYNCBURST DEVICES

The SyncBurst SRAM performs a WORD WRITE or GLOBAL WRITE by using the global write pin (GW#). It can also perform a BYTE WRITE with the byte write enable pin (BWE#) and individual byte write signals (BWx). The ZBT SRAM simplifies the writing task by only using a read/write pin (R/W#) and byte write enables (BWx#). This allows both BYTE WRITEs and GLOBAL WRITEs to be done with one less control signal. ZBT GLOBAL WRITEs are executed by setting all four byte writes active.

BANDWIDTH

One of the main disadvantages of the SyncBurst SRAM is that dead cycles, or NOPs, need to be inserted when transitioning from a READ cycle to a WRITE cycle. Figures 2a-2d show the inefficiencies associated with the SyncBurst family and the elimination of dead cycles by the ZBT family. Table 1 shows the number of cycles to turn around the bus (READ followed by WRITE, followed by READ).

Of course, faster turnaround time translates into increased bandwidth. Table 2 shows several different measures of bandwidth. The comparisons are made at 133 MHz for pipelined devices and 83 MHz for flow-through devices.

MAX bandwidth is a number that is frequently quoted for SRAMs and represents the bandwidth if continuous READs *or* continuous WRITEs are applied to the device. Since applications require a mixture of READs and WRITEs, this number is not very useful.

The next column shows bandwidth assuming the device is continually changing from READ to WRITE (or vice versa) every access. Notice that the dead cycles significantly affect the performance of the SyncBurst SRAM. The pipelined performance goes down by one-half compared to peak bandwidth. For ZBT there is no performance impact because there are no dead cycles.

The last column shows bandwidth if the device transitions between BURST READs and WRITEs of a length of four. This is a four-word READ followed by a four-word WRITE, followed by a four-word READ, etc. Since the bus turnaround does not occur as often, the SyncBurst SRAM recovers a great deal of its performance; however, it still cannot reach the level of the ZBT SRAM.

Table 1
MINIMUM NUMBER OF CLOCK CYCLES FOR READ FOLLOWED BY WRITE, FOLLOWED BY READ

SRAM	NUMBER OF CYCLES
Pipelined SyncBurst	7
Pipelined ZBT	5
Flow-Through SyncBurst	5
Flow-Through ZBT	4

BUS CONTENTION

One of the concerns of system designers is bus contention, especially at high frequencies. Of particular concern is the shift from a WRITE command to a READ command with no bus dead cycles. The WRITE being performed by the SRAM controller (DSP, ASIC, gate array) must go into High-Z before the SRAM output drivers turn on for the next READ cycle. Can bus contention always be eliminated? If not, is there an impact to the device?

Figure 3 shows how bus contention could occur. When performing a WRITE cycle, the data being driven to the SRAM (in this case from an ASIC) must meet the hold time of ^{t}KHDX, or 0.5ns. In order to guarantee 0.5ns of hold, to compensate for temperature, V_{DD} variation and clock skew, and to allow for timing margin, the ASIC must drive the bus longer than 0.5ns. If this time exceeds ^{t}NO_CONTENTION or 1ns after the hold-time is met, bus contention may occur. The length of time that an ASIC will drive the bus will be a function of the process technology of the ASIC and the output driver used. It is possible that there could be some bus contention between the ASIC trying to turn off and the SRAM trying to turn on.

Table 2
ZBT vs. SYNCBURST BANDWIDTH COMPARISON

DEVICE	FREQUENCY (MHz)	MAX BANDWIDTH (MB/SEC)	READ/WRITE CYCLE BANDWIDTH	READ/WRITE BURST OF 4 BANDWIDTH
Pipelined SyncBurst	133	532	267	426
Pipelined ZBT	133	532	532	532
Flow-Through SyncBurst	83	332	221	299
Flow-Through ZBT	83	332	332	332

Is some bus contention allowable? Yes. In some designs it will probably be impossible to completely avoid bus contention under all conditions of temperature and voltage. Certainly 1.5ns is a worst-case condition for the SRAM, and under most cases of temperature and voltage, ${}^tKHQX1$ will be longer than 1.5ns. However, the 1.5ns value must be used for worst-case calculations.

Suppose that the ASIC goes into High-Z 2.5ns after the clock rises. This means that under worst-case conditions there is 1ns of bus contention. The ZBT SRAM is running at 133 MHz, or a 7.5ns clock cycle. This contention only occurs when going from a WRITE cycle to a READ cycle. In the worst case this occurs once every two cycles. So worst-case bus contention occurs 1ns out of every two clock cycles (15ns), or 6.7 percent of the total cycle.

On the average, half of the DQ pins will be in bus contention with the SRAM (because the data bits can be at either a 1 or 0 value). So for a x36 SRAM, we will calculate the bus contention assuming that 18 pins will be in contention (on average). If we assume that during the period of contention the resistance of the SRAM driver is 32 ohms and that of the ASIC is 32 ohms, then there is a 64 ohm path between power and ground for each bit of the data bus in contention. Note that this assumption is only an approximation because the resistance of both the SRAM driver and ASIC driver is changing over time as one turns off and the

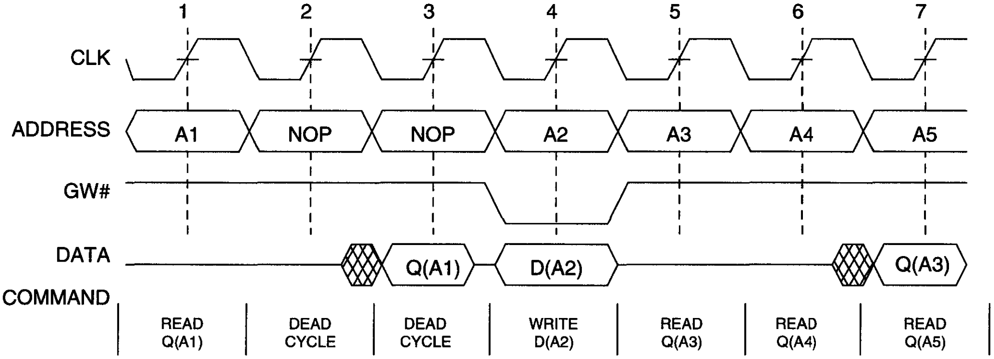


Figure 2a
BUS TURNAROUND TIME FOR PIPELINED SYNCBURST SRAM

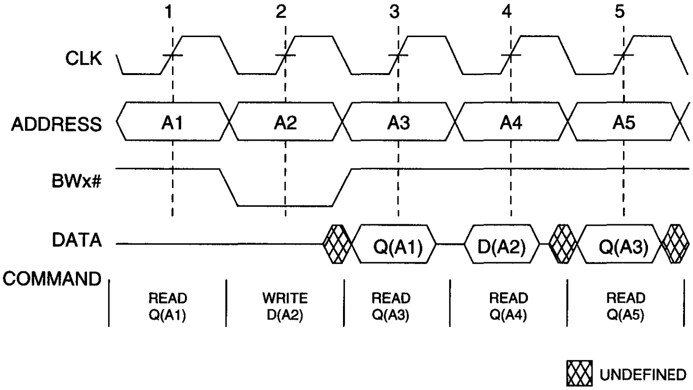


Figure 2b
BUS TURNAROUND TIME FOR PIPELINED ZBT SRAM

other turns on. For a V_{DD} (MAX) of 3.6V, 56mA will be sourced between power and ground. The current drive of 18 bits in contention is 1.013A, or 1.82W.

At first glance this appears to be an unacceptable amount of power. However, it only occurs for 6.7 percent of the total cycle. The current of a 133 MHz ZBT SRAM without bus contention is 350mA (MAX), or 1.26W. Adding in the power of the bus contention for 6.7 percent of the time makes the average power dissipation 1.38W, or a minimal increase.

What about junction temperature? At 70°C ambient temperature, the junction temperature of a ZBT SRAM dissipating 1.26W is 105.3°C (assuming a thermal impedance $[\theta_{JA}]$ of 28°C/W). If the power is increased to 1.38W, the junction temperature becomes 108.6°C, for a temperature increase of 3.4°C, which is acceptable.

In other words, it is acceptable to run with small amounts of bus contention. There will not be driver damage due to bus contention. The ZBT SRAM is designed with separate power pins for the I/Os and core so the core power supply remains isolated from the I/O ring and any current surges that occur on the I/O. The extra current will cause a small IR and LdI/dt voltage drop to the I/O ring, but not to the

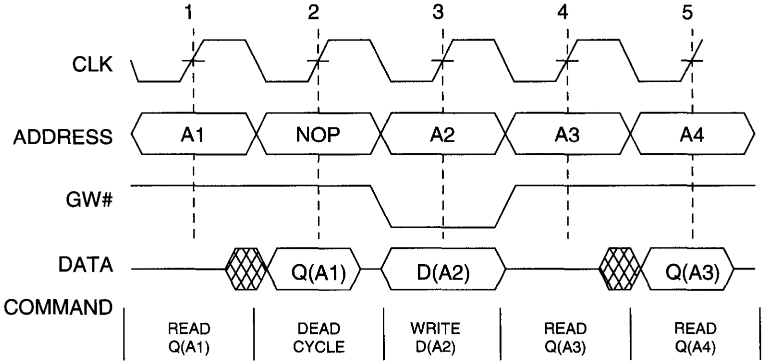


Figure 2c
BUS TURNAROUND TIME FOR FLOW-THROUGH SYNCBURST SRAM

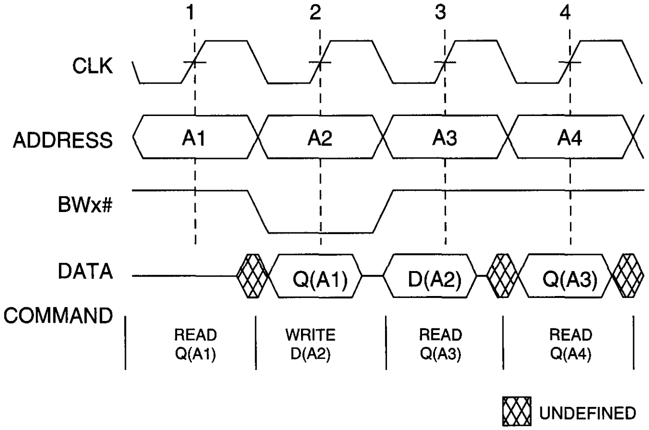


Figure 2d
BUS TURNAROUND TIME FOR FLOW-THROUGH ZBT SRAM

core logic. This architecture prevents voltage drops to the core of the SRAM due to small amounts of contention.

Note that the above calculation assumes that bus contention occurs once every two cycles, which is worst case. It also assumes that the resistance of the drivers is constant. Lastly, it assumes that the ASIC is at worst-case turn-off at the same time the SRAM is at worst-case turn-on. Typically these occur at opposite extremes of current and temperature, thus making the above scenario unlikely.

Other features on ZBT SRAMs help to minimize bus contention and will be the topic of a future article.

CONCLUSION

The ZBT SRAM represents a drastic improvement over the SyncBurst SRAM for many applications. At the same bus frequencies, ZBT can provide greater bandwidth than SyncBurst because there are no dead cycles during bus transitions from READ to WRITE or WRITE to READ. Also, the control logic for the ZBT is simplified, allowing users to easily control the SRAM with a minimal number of control pins. Lastly, ZBT is designed to operate with no dead cycles even if small amounts of bus contention occur. These features make the ZBT SRAM an excellent solution for high-performance applications such as telecommunications, networking and DSP.

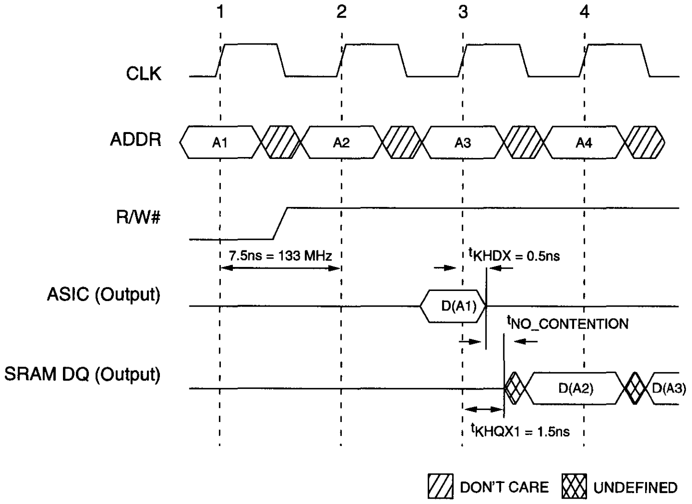


Figure 3
BUS CONTENTION CAN OCCUR IF THE TURN-OFF TIME OF THE ASIC IS LONGER THAN ^{t}NO_CONTENTION

The Future of ZBT

Micron will offer 2Mb and 4Mb versions of the ZBT SRAM in bus widths of x18, x32 and x36. Although these densities accommodate most users, there are customers with even larger memory requirements. For these customers it is important to note that ZBT will be available in larger densities.

Although ZBT will initially be produced in 2Mb and 4Mb versions, the functionality has already been defined for 8Mb and 16Mb versions. The packages and pinouts are all compatible. The only difference between densities is the address pins, which are already defined and can be compensated for in board layout.

In essence, ZBT customers can use four generations of parts. This can be especially important for products that have longer lifetimes than average. ZBT was developed for SRAM customers who need performance, simplicity and easy upgradeability.

TECHNICAL NOTE

DESIGNING FOR MULTIPLE SYNCBURST™ SRAM VENDORS

This article was originally published in 1994.

INTRODUCTION

Not all SyncBurst™ SRAMs are created equal. Just as with any memory product, SyncBurst vendors have minor differences in power dissipation or timing specifications. Beyond this, there are also differences among vendors in terms of functionality. Not accounting for these functional differences is the single most common reason why some "second source" parts fail in a system and others work. Fortunately, a single design can easily accommodate these differences. This technical note describes how.

SIGNALS MODIFIED BY JEDEC TO THE SYNCBURST SRAM ARCHITECTURE

The JEDEC specification has undergone several revisions since its conception, adding certain signals and deleting others. However, not all SRAM vendors implement these modifications since some are optional. Table 1 describes the signal additions and outlines their benefits.

Table 1
SYNCBURST PINS AFFECTED BY JEDEC CHANGES

FUNCTION	TQFP PIN	DESCRIPTION
MODE (LBO#)	31	Burst Mode Input. Also called LBO#. When this input is LOW, linear burst sequence is selected (used by Power PC and 680x0 applications). When this input is HIGH or left UNCONNECTED, interleaved burst sequence is selected (for 486 and Pentium applications). This signal is not intended to be altered dynamically. Some vendors do not implement the MODE pin and label it as No Connect. Others may not implement the internal pull-up resistor. For compatibility, connect this input to either V_{DD} or GND through a resistor. Micron implements an internal pull-up resistor to ease design compatibility with the original SyncBurst SRAM release. Some designs do not use burst at all, and this pin can be left unconnected or connected to a supply for reduced thermal impedence.
GW#	88	Global Write Input. This input allows a full bus-width device WRITE. This function is valuable to cache controllers which, during cache fill operations, modify the SRAM contents independent of the state of the BWx# signals. This pin, in concert with BWE#, permits direct connection of the BWx# lines to the microprocessor BEx# signals. Two system benefits result: one clock cycle can be eliminated from WRITE cycles because BEx# lines do not have to be conditioned in the ASIC and rebroadcast as BWx# signals, and the pin count of the controller ASIC can be reduced. If this function is not required, this pin should be tied HIGH (to V_{DD}).
BWE#	87	Byte Write Enable Input. In the initial JEDEC SyncBurst specifications, pin 87 was parity disable (PDIS) but was made obsolete by the addition of nonparity (x32) devices. This input, when LOW, allows the byte write signals (BWa#, BWb#, BWc# and BWd#) to control WRITE operations. This permits partial-bus WRITE operations to the SyncBurst SRAM. If the GW# function is not required, BWE# can be tied LOW (to GND). This permits WRITEs to be controlled solely by the BWx# signals as is the case with original 32K x 36 and 64K x 18 devices. See Figures 1 and 2 for connection examples.

Table 1 (continued)
SYNCBURST PINS AFFECTED BY JEDEC CHANGES

FUNCTION	TQFP PIN	DESCRIPTION
FT#	14	Flow-Through Input. A few vendors implement this optional feature allowing user selection of pipelined (FT# = HIGH) or flow-through operation (FT# = LOW). Other vendors make pin 14 a No Connect. This pin must be hardwired HIGH for Micron pipelined devices and LOW for Micron flow-through devices. Hardwiring HIGH or LOW accommodates all vendors whether they implement the pin as FT# or NC.
ZZ	64	Snooze Input. This input is available on all Micron SyncBurst SRAMs. Many vendors do not implement this feature, instead labelling the pin No Connect. When ZZ is HIGH, the device enters the lowest power standby mode within one clock cycle in the flow-through device and two clock cycles in the pipelined device (the industry standard requires this to occur within four clock cycles). The device takes an equal number of clock cycles to return to active operation when ZZ is LOW. Prior to implementation, lowest power standby current can be achieved if the clock is blocked from the SRAM and all control and data inputs are static and held near a rail voltage. The ZZ function is most useful to designers of mobile computer systems, but it is an optional feature. Where pin count is limited and does not permit, external clock blocking is an alternative and an equally effective choice to reduce power consumption. If SNOOZE mode is not used, this pin should be tied LOW.

BENEFITS OF THE BYTE WRITE INPUTS: PENTIUM® EXAMPLE

The descriptions in Table 1 outline some benefits of these newer features. More detail regarding WRITE functionality is necessary. Figure 1 shows the connection of two Micron 64K x 32 SyncBurst SRAMs (512KB cache) with a Pentium processor, without taking advantage of the GW# and BWE# signals. In this case, chipset logic must process eight byte enable (BE#) inputs from the processor and separately output eight byte write (BW#) signals, four to each SRAM. It is necessary in this case to separate the BEx# lines from BWx# lines because the byte enables from the processor will not be in the correct state during some operations such as external cache snoop cycles. The BEx# lines are not tri-

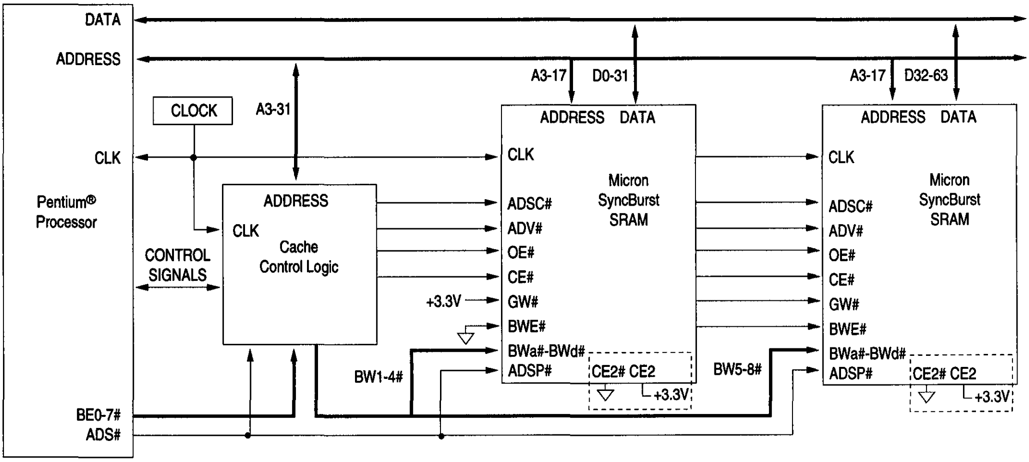


Figure 1
PENTIUM CONNECTION WITHOUT GW# AND BWE#

stated when the Pentium AHOLD input is asserted; hence the cache controller cannot simply redrive those signals to the desired states to cover those cases where the BEx# lines are in unacceptable states. The only way to overcome these constraints is for the cache controller to use eight inputs and eight outputs as described above.

Figure 2 shows the connection of two Micron 32K x 32 SyncBurst SRAMs with a Pentium processor while taking advantage of the GW# and BWE# signals. The cache controller pin count has been reduced from 16 in the previous example to only 10 pins in Figure 2. GW# forces all bytes to be written into the SRAM independent of the state of the BWx# inputs. This is the normal mode of operation during cache line fills. The BWE# signal permits the direct connection of the processor's BEx# signals to the SRAMs for ndividual processor-derived BYTE WRITE operations. Regardless of pipelined or flow-through operation, all BWx#, BWE# and GW# signals are required to be valid at the same clock rising edge that the data is valid.

Another important benefit of the direct-connection of the processor's BEx# signals to SRAM BWx# signals is the ability to reduce wait states during WRITE operations. The extra time for a BEx# to travel from the processor into the ASIC, propagate through the ASIC logic, drive through the output buffers and to the SRAM as in Figure 1, can induce an extra wait state during WRITE cycles if the tag SRAM is no longer the most speed-critical element. Figure 2 shows the direct path. Now, only the BWE# signal is on that critical timing path. Any ASIC designer will testify that a single critical signal can be speed-optimized far more easily than 16 signals.

Figure 3 illustrates how depth expansion from 32K x 64 to 64K x 64 is accomplished by adding two more 32K x 32 devices. This method has not been altered by the addition of any new signals. Figure 4 shows how this may be done using two devices on a motherboard and adding a dual in-line memory module (DIMM) to expand memory size. Note that no jumpers are required because the DIMM provides the additional necessary connection of A18 to the chip enables of the "HIGH SRAMs." The HIGH SRAMs normally function during all cache cycles but serve as the upper half of the cache when cache is depth-expanded. The depth expansion of memory can also be done using 2Mb versions of the SyncBurst SRAM to upgrade from 64K to 128K. It can also be done with 4Mb versions upgrading from 128K to 256K. Notice for cache memories this method is now rarely used because of the availability of 64K x 32 memories. The method is still used in noncache systems that require large amounts of memory (hence banking).

PACKAGE AND PIN COMPATIBILITY

While most vendors are joining in the use of the industry-standard Thin Quad Flat Pack (100-Pin TQFP), some have elected to use the thicker Plastic Quad Flat Pack (PQFP). Either may be accommodated in a single design by making the pads long enough to accept either package. The thicker PQFP has a slightly broader footprint. This is due to the

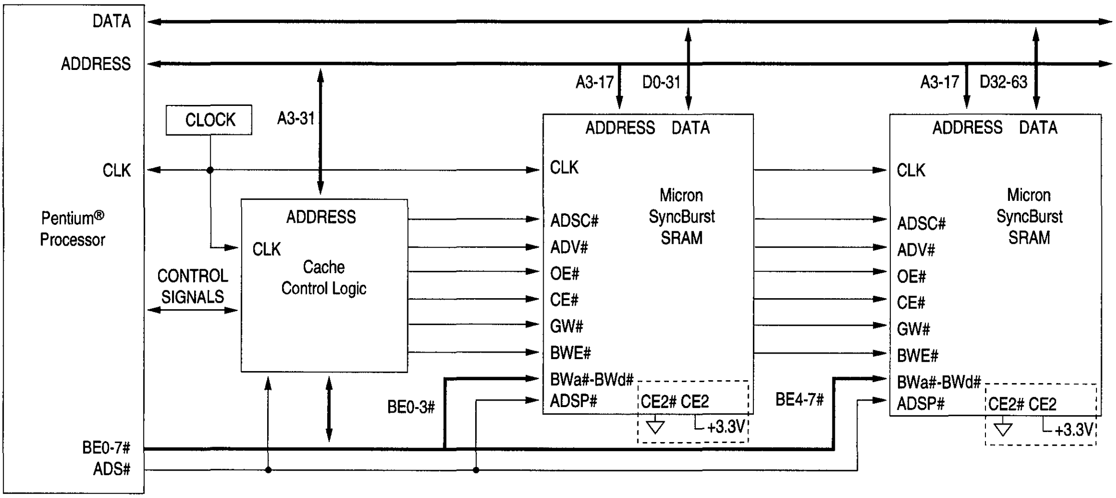


Figure 2
PENTIUM CONNECTION WITH GW# AND BWE#

device lead vertical runs not being shaped perpendicularly to the package underside. Hence, the taller the package, the wider the lead excursion. It is not desirable to use 90° lead bends due to reduced reliability. Figure 5 has a recommended PCB land pattern that accommodates either package thickness. The TQFP offers several advantages over the PQFP. The TQFP can be mounted in systems where height is restricted (JEDEC specification MS-026 BHA lists TQFP overall height as 1.60mm maximum, the PQFP is 2.2mm or 3.0mm depending upon package option). The TQFP is also more speed-capable because the thermal resistance is smaller for the thinner package. The JEDEC tray standard is CS-007.

Tables 3 and 4 summarize the signals designers need to be aware of when designing for multiple vendors. Figures 6 and 7 provide pictorial pin assignments for the 1Mb, 2Mb and 4Mb SyncBurst SRAMs in a TQFP package, accounting for industry compatibility requirements.

5V TOLERANCE

When the 3.3V SyncBurst SRAM was first introduced, most systems were mixed voltage (5V and 3.3V). It was not uncommon for some of the control inputs of the SRAM to be driven by a 5V component. 5V-tolerant inputs allowed these 5V components to directly drive the SRAM without buffering circuitry.

Now that 3.3V components are mainstream, the need for 5V tolerance is lessened. Also, the move to faster processes

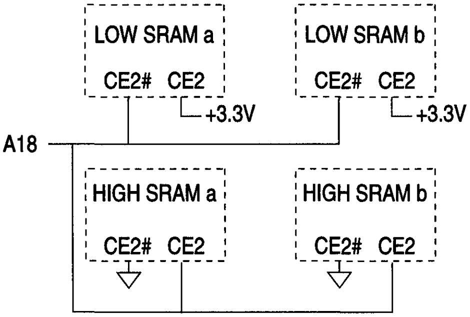


Figure 3
DEPTH EXPANSION

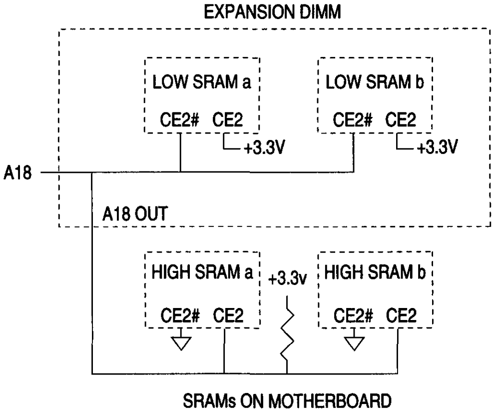
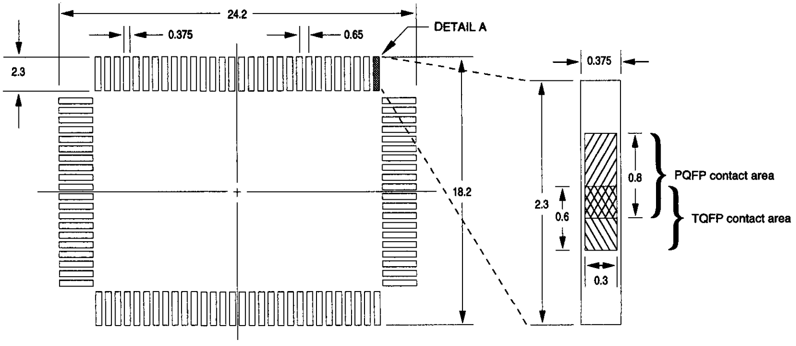


Figure 4
DEPTH EXPANSION USING DIMMs



NOTE: All dimentions are nominal and in mm

Figure 5
PCB LAND PATTERN FOR 100-PIN TQFP AND 100-PIN PQFP DEVICES

Table 3
DESIGNING FOR COMPATIBILITY: x36 AND x32

TQFP PIN	CONNECTION	PURPOSE
1, 30, 51, 80	NC or DQPx	Parity bit on x36. No Connect on x32.
14	LOW HIGH	If using flow-through, wire LOW; pipelined devices must be wired HIGH. Users cannot switch between flow-through and pipelined modes. Wiring HIGH or LOW allows all vendors to be used (even those with NC).
16, 66	NC	Although reserved for a reference voltage input, it is unlikely that vendors will implement this function.
31	LOW HIGH	MODE (LBO#) input. Wire HIGH or unconnected for interleaved burst sequence and LOW for linear burst sequence. If burst is not used in an application, this pin can be wired HIGH, LOW or left unconnected.
38, 39, 42, 43	Do Not Use (DNU)	These pins are currently reserved for JTAG or future functions. To improve package heat dissipation, these signals may be wired to GND.
49	NC or SA	SA on the 2Mb and 4Mb versions. NC on the 1Mb version.
50	NC or SA	SA on the 4Mb version. NC on the 1Mb and 2Mb versions.
64	LOW HIGH	ZZ pin. LOW allows normal mode of operation. HIGH causes device to enter SNOOZE mode. If unused, tie LOW to accommodate all vendors.
87	BWE#	BWE# input. If not used, tie LOW.
88	GW#	GW# input. If not used, tie HIGH.

mandates the removal of 5V-tolerance. For widest vendor choice, it is recommended that designers plan for SRAMs with 3.3V I/O or use buffering from 5V to 3.3V components. A more detailed description is given in Micron Technical Note TN-58-08, "Designing with 3.3V I/O Synchronous SRAMs."

CYCLE TIME vs. ACCESS TIME

Some vendors speed-grade their parts by access time. Others speed-grade by cycle time. Typically, flow-through devices are graded by access time, and pipelined by cycle ime. However, it is wise to carefully check the data sheet when comparing parts from different vendors.

EXISTING DESIGNS

Existing designs that use the original SyncBurst SRAM and do not need the new functionality must make a few modifications to accommodate the JEDEC changes. Pin 88 must be tied HIGH (formerly NC); pin 87 must be tied LOW (formerly PDIS); and MODE must be tied LOW if linear burst is desired, or tied HIGH or left unconnected for interleaved burst. In this configuration (x32 operation), the parity bits will not be disabled when using the original device functionality. Therefore, the parity lines (DQPa-d) should be left unconnected or supplied with weak pull-up or pull-down termination in nonparity designs.

SUMMARY

This article provides information which enables engineers to design with the synchronous burst SRAM architecture and avoid compatibility problems in the future. Recommended PCB pad dimensions are supplied to ensure package compatibility. The greatest performance and ease-of-use benefits are derived from the addition of global write and byte write enable inputs to the SRAM family and are described in detail.

Table 4
DESIGNING FOR COMPATIBILITY: x18

TQFP PIN	CONNECTION	PURPOSE
1-7, 25-30, 51-57, 75-80	NC or Vss	Not reserved for any established functions. Tie these pins LOW to assist in thermal conduction. They may also be left unconnected.
14	LOW HIGH	If using flow-through, wire LOW; pipelined devices must be wired HIGH. Users cannot switch between flow-through and pipelined modes. Wiring HIGH or LOW allows all vendors to be used (even those with NC).
16, 66	NC	Although reserved for a reference voltage input, it is unlikely that vendors will implement this function.
31	LOW HIGH	MODE (LBO#) input. Wire HIGH or unconnected for interleaved burst sequence and LOW for linear burst sequence. If burst is not used in an application, this pin can be wired HIGH, LOW or left unconnected.
38, 39, 42, 43	Do Not Use (DNU)	These pins are currently reserved for JTAG or future functions. To improve package heat dissipation these signals may be wired to GND.
49	NC or SA	SA on the 2Mb and 4Mb versions. NC on the 1Mb version.
50	NC or SA	SA on the 4Mb version. NC on the 1Mb and 2Mb versions.
64	LOW HIGH	ZZ pin. LOW allows normal mode of operation. HIGH causes device to enter SNOOZE mode. If unused, tie LOW to accommodate all vendors.
87	BWE#	BWE# input. If not used, tie LOW.
88	GW#	GW# input. If not used, tie HIGH.
92	NC	This pin is reserved for currently undefined future use.

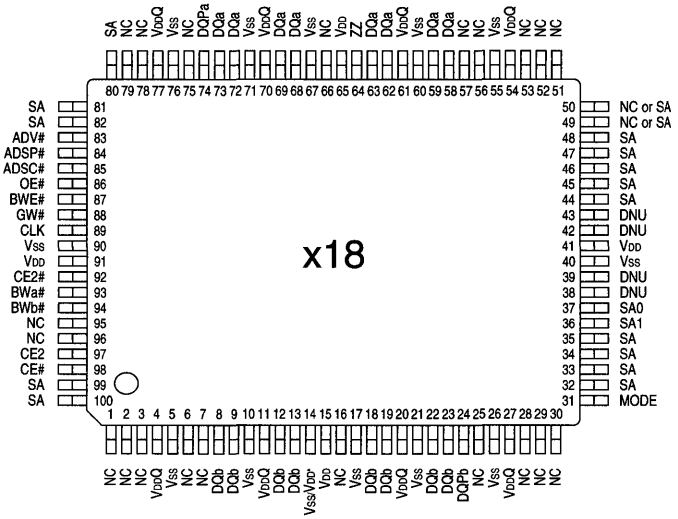


Figure 6
x18 COMPATIBLE PIN ASSIGNMENT

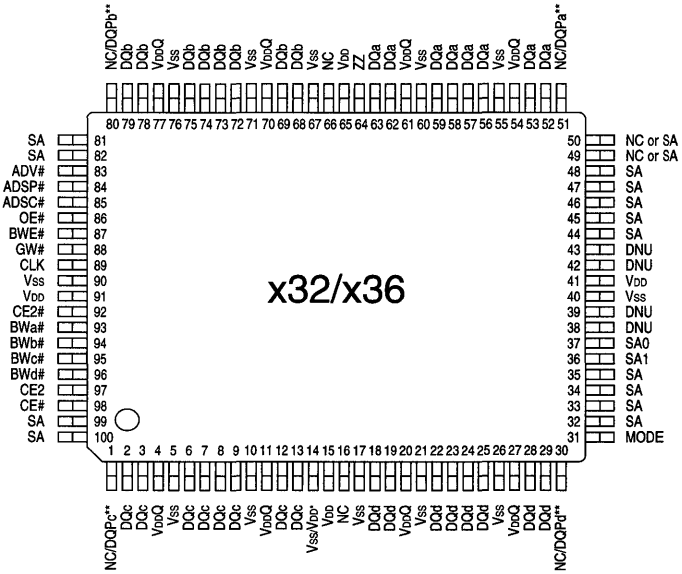


Figure 7
x32/x36 COMPATIBLE PIN ASSIGNMENT

* Vss is for flow-through parts; VDD is for pipelined.
** NC on x32 version; DQPx on x36.

TECHNICAL NOTE

DESIGNING WITH x36 SYNCBURST™ SRAMs

his article was originally published in 1993, with some revisions nade in 1997.

NTRODUCTION

New medium- and high-end personal computers all eed cache to reach a reasonable point on the price-erformance curve. The most desirable cache is one that liminates the most wait states. In workstation design, ache is mandatory. In personal computer design, cache is ssential, even in portable computer designs. Micron's yncBurst™ SRAMs provide the means to achieve the deired price-performance target. This technical note disusses the benefits of these parts and compares them to everal alternatives. The discussion focuses primarily on he x32 and x36 SyncBurst family members.

ICRON SYNCBURST SRAMs

Micron SyncBurst SRAMs are offered in three configuraions. 1Mb, 2Mb and 4Mb versions are available in 3.3V or .5V I/O versions. All versions come in a 100-pin TQFP ackage and are selectable between interleaved burst node for 486 and Pentium®, and linear burst mode for owerPC™ and 680x0 applications. Pipelined single-cycle eselect (SCD), pipelined double-cycle deselect (DCD) and low-through versions are available. These versions all use yte write inputs rather than byte enable inputs, enabling hem to functionally replace 32K x 9 synchronous burst RAMs. Hence, any cache controllers or chipsets that can se the 32K x 9 devices will function with an equivalent 32K 36 device from Micron.

32K-DEEP CACHE SYSTEMS WITH BURST

Zero-wait-state performance can be achieved in fast systems (bus speeds of 50 MHz and above) only by using SyncBurst SRAMs or multiple banks of fast SRAMs with extremely fast control logic. The latter solution will at least double the minimum cache size because a minimum of two banks is required. Also, buffers are generally added in the dual-bank solution because bus loading is doubled. Consequently, more timing pressure falls upon the SRAMs and control logic, which inevitably makes both more costly.

SyncBurst SRAMs are the solution to the zero-wait-state dilemma. If a larger cache size is needed, they provide the option of depth expansion or using the additional parts as a second set of associativity. Studies have shown that many new software applications benefit as much or more from partitioning the cache into the two-way set associative architecture as compared to doubling the direct-mapped cache size. In other words, a 64K x 72 two-way set associative cache will perform as well or better than a 128K x 72 direct-mapped cache. Although the two-way cache is more complex to control, only half the memory is needed for a given performance target. With new 128K x 36 SRAMs now available, a 128K x 72 cache can now be implemented as a single bank.

The available 32K-deep synchronous burst SRAM solutions in the industry are 32K x 9, 32K x 18 and 32K x 36. Because of its advantages, the x32/x36 SRAM has emerged as the dominant solution in cache designs. Table 2 compares these three devices. Since no 3.3V, x9 and x18 devices have been announced, the 5V versions are used for com-

Table 1
MICRON SYNCHRONOUS SRAM VERSIONS

DENSITIES	CONFIGURATION	PART # SUFFIX	FEATURES
1Mb, 2Mb, 4Mb	x18, x32, x36	B3/B4	Flow-Through
		C5/C6	Pipelined Single-Cycle Deselect (SCD)
		D8/D9	Pipelined Double-Cycle Deselect (DCD)

Table 2
32K x 72 DIRECT-MAPPED CACHE COMPARISON

	32K x 9	32K x 18	32K x 36
Quantity for 32K x 72	8	4	2
SRAM voltage (V)	5	5	3.3
Board area (sq. in.)	3.86	2.53	1.10
Address loading (pF)	24	16	8
Data loading (pF)	8	6	6
Power in 5V system 66 MHz (W)	7.0	5.3	2.5
Power in 3.3V system 66 MHz (W)	n/a	n/a	1.65
Power in 5V system 50 MHz (W)	5.8 (est)	4.3	2.2
Maximum height (mils)	180	180	63

parison. The 32K x 36, 3.3V SRAM is the clear winner in every category. The power dissipation in a 5V system using 32K x 36 devices includes the power dissipated by the 5V to 3.3V linear regulator, which is needed if 3.3V is not available anywhere. The regulator adds less than 0.4 square inches more board area than listed in Table 2. This still results in the least area used. None of the cases include I/O power. With the widespread availability of 3.3V power supplies, the regulator is now rarely required.

FUNCTIONAL DIFFERENCES

There are almost no differences in functionality between the various 32K-deep devices listed in Table 2. The 32K x 18 and 32K x 36 devices both use byte write signals. This means that four 32K x 9 devices may be replaced by two 32K x 18 devices or one 32K x 36 device. Any of these alternatives appear the same to cache control logic. The only functional difference lies within the ADSP#/CE# logic in the device. The 32K x 18 and 32K x 36, because they are newer devices, benefit from lessons learned in systems employing 32K x 9 parts. The ADSP# signal (which is typically fed directly from the microprocessor address/data strobe) is gated by CE# in the new wider devices. This permits address pipelining to function correctly, whereas in systems built using 32K x 9 devices, this becomes awkward.

For example, assume that the cache controller discovers an L2 cache READ miss. The controller initiates a cache line fill from main memory. ADSC# is used to latch in the address to the SRAM. While this fill is in progress, there is no reason to tie up the address bus since the main memory controller knows where data is needed from and the SRAM knows where it is going. The cache controller can issue a "next address" command to the microprocessor and begin the tag hit/miss comparison of the new address while the fill is still in progress. This potentially eliminates wait states when the system is ready to proceed with the next bus operation. A problem can arise using 32K x 9 SRAMs when the next address is requested because the microprocessor will issue a new ADSP# and address simultaneously. Since there is no way to block this command from that SRAM, the cache fill in progress would be terminated by the new ADSP# command.

The newer SRAMs (32K x 18 and 32K x 36) address this problem by the extra gate shown in Figure 1. This extra gate intercepts ADSP# before propagating inside the chip and conditions it with CE#. Figure 1 actually shows the 32K x 36, although the logic is independent of the device width. Also shown in Figure 1 are the additional chip enables in the 32K x 36, which will be addressed later. The cache controller can take CE# HIGH during the fill, which will block ADSP#

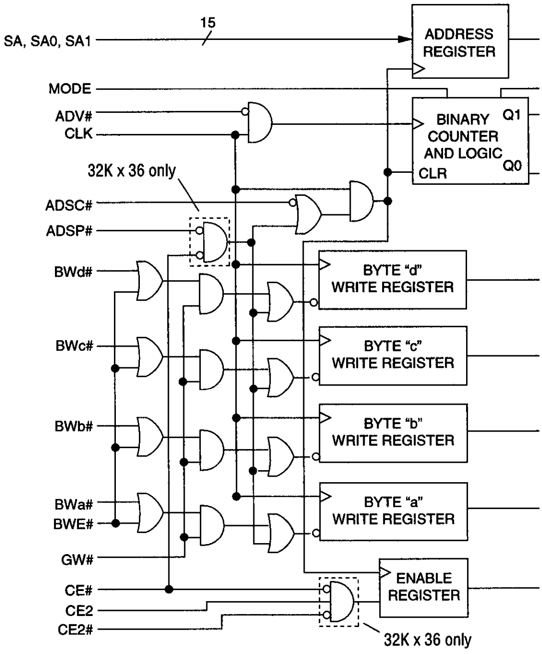


Figure 1
DIFFERENCE BETWEEN 32K x 9 AND 32K x 36

from terminating the fill in progress. In systems not utilizing this extra functionality, the extra gate does no harm and introduces no functional incompatibilities with existing designs.

PARITY ISSUES

One extra bit per byte has long been used as an easy method of detecting memory/data transmission errors. The main drawback to this method is a lack of choices in error response. If the error occurred in the L2 cache SRAM and the cache line has not been modified, a possible response is to flush the cache line and refill from main memory. Most systems do not bother and just shut down instead. More sophisticated systems use error correction circuitry to detect and correct all single-bit errors and some double-bit errors. This sounds obviously better than just using parity but causes extra delays in data delivery because of the error-checking logic. This compromise is essential in systems with high data-integrity requirements such as file servers, transaction processors, some data communications equipment and workstations.

Many systems have been and are being designed without parity or error correcting requirements. The rationale is fourfold. Error rates are low if the circuit design and printed circuit board layout are done expertly (i.e., low transmission error rate; however, transmission errors can be significant and will be left for future discussion). With cache systems, DRAM runs for a small percentage of the time, reducing its average cycle time and decreasing the DRAM Soft Error Rate (SER; see Micron Technical Note TN-04-28 "DRAM Soft Error Rate Calculations" for a detailed discussion of DRAM SER). SRAM soft error rate is very low (less than one failure per 50 years of continuous operation for a 256KB cache composed of two 3.3V 1Mb synchronous SRAMs). Ignoring transmission errors and adding the SRAM and 16Mb DRAM failure rates (using 4 Meg x 4 DRAMs) results in a combined system memory error rate of one per 25 years of continuous full-speed operation. The fourth rationale is cost. It is difficult for a system with parity and no innovative error handling to compete against one without parity.

In response to the low system error rates and customer demand for cost-effective solutions, Micron has a 32K x 32 organization of the SyncBurst SRAM. The 32K x 32 is pin- and function-compatible with the 32K x 36 SyncBurst version. The four DQPx lines (data parity bits) are no connects on the 32K x 32 device.

VOLTAGE CONSIDERATIONS

Practically all new memory designs use 3.3V devices. High-speed (high-power) requirements in microprocessors have made them very difficult to design at 5V. This is the main reason for 3.3V (and below) microprocessors such as Pentium, Alpha, PowerPC, 680X0, 486, etc. With the steady increase in system speed, there has also been a steady increase in SRAM power dissipation. The transition to 3.3V provides welcome relief—power dissipation is less than half in 3.3V devices, compared to 5V devices with identical speed. This enables SyncBurst devices to be placed into the space-efficient TQFP without requiring expensive thermal management.

SyncBurst SRAMs function in systems which are 3.3V only. Although original 1Mb devices functioned correctly in mixed-voltage systems (5V and 3.3V both present), all devices have moved to 3.3V-only I/O. A single 3.3V supply is needed for all VDD and VDDQ pins. All other I/O pins are 3.3V only. Hence, 5V or TTL CMOS logic driving inputs to a 3.3V SyncBurst SRAM may require buffering between the devices.

Micron has manufactured 5V-tolerant 1Mb SRAMs since 1993 to ease the migration of users to 3.3V systems. With that migration nearly complete, Micron no longer offers 5V-tolerant devices.

Another consideration is systems that do not have any 3.3V supplies available. Although at first glance it may seem that only 5V SRAMs should be considered, this may be a hasty judgment. Referring to Table 2, to implement a 32K x 72 cache, two 32K x 36 devices using 1.10 sq. in. of board area are required. If a 3.3V regulator is added, less than 0.4 additional square inches is needed, resulting in 1.50 square inches of board area. This is still less board area than four 32K x 18 devices (2.53 sq. in.) and results in less power dissipation than the 32K x 18 devices even with the inherent inefficiency of linear regulation. Since 3.3V regulators are inexpensive, this solution is very cost competitive as well.

SyncBurst SRAMs can be used in 3.6V systems as well. It is best to set the power supply voltage on the low side of 3.6V. With a reasonable tolerance, both microprocessor and SRAM will operate nominally. For example, at 3.5 ±0.1V both SRAM and microprocessor will operate within design specifications. In fact, the SRAM operates slightly faster than data sheet specifications (which are listed for the low voltage and high temperature case).

POWER CONSIDERATIONS

There is a great deal of confusion in the industry about how to accurately predict power, and we have all fallen victim to misconceptions at one time or another. The SRAM data sheets from any vendor exclude the current needed to switch the load capacitance from one state to another. The IDD given in the data sheet accounts for everything else. The IDD used in the calculation should be appropriate for the operating conditions; e.g., IDD (MAX) is specified for the lowest operating temperature and the highest recommended VDD, and has guardband added to it. For actual power, IDD should be looked up from published current versus voltage, temperature and cycle times. See the Micron Technical Note "SRAM Thermal Design Considerations" (TN-05-14) for a derivation of true SRAM power. True SRAM power for Micron synchronous devices is:

$$P = V_{DD}\,I_{DD} + \Sigma\, P_{LAC\ (\text{for all outputs that toggle})} + P_{LDC}$$

The incremental power due to steady-state current flow into or out of the DQ pins (P_{LDC} due to I/O leakage of connected devices) is generally ignored because it is small in systems employing CMOS devices. That extra power would be:

$$P_{LDC} = (V_{DD} - V_{OH})\, I_O\, N_H + V_{OL}\, I_I\, N_L$$

where VOH is the actual logic HIGH output voltage, I_O is output current on those DQ lines and N_H is the number of DQ lines that are HIGH; VOL is the actual logic LOW voltage, I_I is the resulting input current into the DQ line and N_L is the number of DQ lines that are LOW. Since almost all CMOS devices have I_I or I_O less than 10µA (often 1 or 2µA), this calculation is inconsequential. For example, take the case where 36 outputs are connected to loads having 10µA of leakage. The contribution to device power is:

$$(3.3\text{V} - 3.0\text{V})\ 10\mu\text{A}\ (36) = 108\mu\text{W}$$

With higher leakage, VOH drops and power increases as a result of both increased current and greater voltage drop in the SRAM output driver.

The AC load component is a different matter. For outputs which swing from logic LOW to logic HIGH, each output contributes the following to device power:

$$P_{LAC} = \frac{C_L}{T}\left(V_{DD}\,[V_{OH} - V_{OL}] - 0.5\,[V_{OH}^2 - V_{OL}^2]\right)$$

Assuming a load capacitance (C_L) of 30pF, VDD = +3.3V, clock period (T) of 20ns, dynamic VOH of 3.0V, and dynamic VOL of 0.1V, the incremental power for each output that swings from LOW to HIGH is 7.6mW. If 36 outputs did this, the output power component of the SRAM would be 274mW. The total power would be:

$$200\text{mA} \times 3.3\text{V} + 274\text{mW} = 0.934\text{W}$$

The HIGH to LOW transition case is less severe:

$$P_{LAC} = \frac{C_L}{T}\left(0.5\,[V_{OH}^2 - V_{OL}^2]\right)$$

Using the same load conditions as the logic LOW to logic HIGH example, the resulting AC power for each output that changes from logic HIGH to logic LOW is 6.7mW.

Using the logic LOW to logic HIGH calculated power, the device case and die temperature can be approximated. Micron uses an IC package mounted on a four-layer PCB 4.33 x 1.112 inches square to measure θ_{JC} (junction-to-case thermal impedance) and θ_{JA} (junction-to-ambient thermal impedance). Both measurements are taken with the PCB located in the center of a one cubic foot closed container that provides a still air environment. The thermal characteristics for Micron's 2Mb memory in a TQFP package are measured as having a θ_{JC} of 2°C/W and a θ_{JA} of 25°C/W giving a θ_{CA} of 25 - 2 = 23°C/W. With these values, the device case temperature is:

$$\begin{aligned} T_C &= T_A + P\,(\theta_{CA}) \\ &= 70°\text{C} + 0.934\text{W}\ (23°\text{C/W}) \\ &= 91.482°\text{C} \end{aligned}$$

The junction temperature is:

$$\begin{aligned} T_J &= T_A + P\,(\theta_{JA}) \\ &= 70°\text{C} + 0.934\text{W}\ (25°\text{C/W}) \\ &= 93.35°\text{C} \end{aligned}$$

which is less than the 150°C specification limit.

Actual device junction temperature will most likely be different depending on actual ambient temperature, cooling levels, PCB layers, dimensions and so forth.

DEPTH EXPANSION

Another major advantage of the SyncBurst SRAM family is the two extra chip enables. The extra active LOW and HIGH chip enables (CE2#, CE2) facilitate expansion from 32K to 64K memory depth for the 1Mb version, 64K to 128K for the 2Mb version and 128K to 256K for the 4Mb version without any additional logic. Depth expansion using 2Mb devices (128K x 36) is illustrated in Figure 2.

This expandability translates into greater flexibility in PC designs. For example, a 72-bit system which requires either a 256KB or a 512KB cache can be laid out for four 32K x 36 devices and then populated with either two or four devices, depending on the desired cache size—with no board changes and no sockets. The only other upgrade which is that simple is the change from 32K x 18 to 64K x 18. This has several

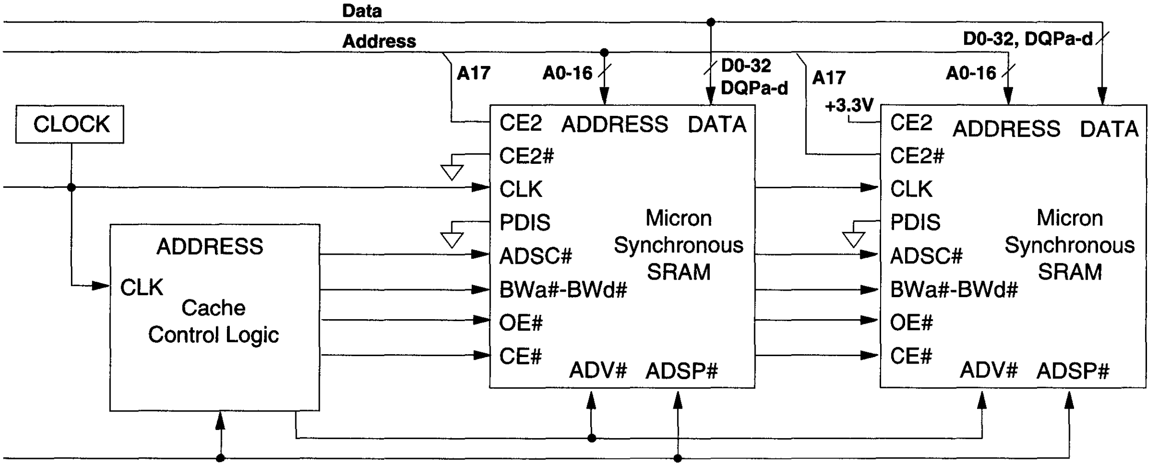


Figure 2
DEPTH EXPANSION FROM 128K x 36 TO 256K x 36

disadvantages by comparison: four devices are needed in either case, so the total board area needed is greater than the 32K x 36 devices (and greater still if sockets are required); power dissipation is higher; and two separate part types must be stocked by the manufacturer instead of just one.

Table 2 compares the 32K x 18 solution to the 32K x 36 assuming that sockets are not required. Table 3 compares the 64K x 72 cache configuration using four 32K x 36 devices versus four 64K x 18 devices. The Micron 64K x 18 solution is also shown for completeness. The one advantage that the 64K x 18 solution does offer is lower data bus loading, although the difference is small. In all other criteria, the 32K x 36 is a superior solution. Although it is clear why the 3.3V 32K x 36 results in lower power than the 5V 64K x 18, it may not be clear why the 32K x 36 system has lower power than the 3.3V 64K x 18. The reason is that only two of the four 32K x 36 devices are active at one time. At 66 MHz, the active current is 250mA, but the standby current is only 85mA with clock running and all inputs toggling. By contrast, the four 64K x 18 devices from Micron would each require 200mA. The 5V competing parts require 360mA at the higher voltage.

SUMMARY

The new family of Micron Synchronous SRAMs provides the optimal solution for high-performance cache systems. Caches of 32K depth can be created using the 32K x 36 devices and will result in the lowest board space, loading and power requirements of any alternative. Systems requiring the flexibility of cache depth doubling can also be satisfied using the extra available chip enables incorporated into the device. The resulting cache is twice as deep and requires no board changes.

Table 3
64K x 72 DIRECT-MAPPED CACHE COMPARISON

	64K x 18	TQFP Micron 32K x 36	TQFP Micron 64K x 18
Quantity for 64K x 72	4	4	4
SRAM voltage (V)	5	3.3	3.3
Board area (sq. in.)	5.06	4.40	4.40
Address loading (pF)	20	16	16
Data loading (pF)	8	12	6
Power in 5V system 66 MHz (W)	7.2	3.4*	4.1*
Power in 3.3V system 66 MHz (W)	n/a	2.2	2.6
Power in 3.3V system 50 MHz (W)	n/a	1.8	2.2
Maximum height (mils)	180	63	180

*Micron device power at 5V includes power dissipated by 3.3V regulator.

TECHNICAL NOTE

SYNCBURST™ SRAMs IN ASIC AND ASYNCHRONOUS DESIGNS

This article was originally published in 1994.

INTRODUCTION

The SyncBurst™ SRAM is the synchronous SRAM of choice in secondary cache designs, offering a small footprint, low-loading, high-performance cache data SRAM solution. A number of questions have been asked by individuals who need the wide architecture, yet use the device more like a conventional asynchronous SRAM in noncache applications. This article addresses the latter desire, with a discussion of basic device operation in synchronous sysems provided as background information.

SYNCHRONOUS BURST SRAM SYSTEM OPERATION

Although designed specifically for use in microprocessor econdary cache, the Micron® SyncBurst SRAM is by no means restricted to that function. Microprocessors such as he PowerPC™ and Intel® Pentium® and have two distinct modes of external bus operation: normal and burst. Normal bus operation consists of a two-clock-cycle external bus access. In the first cycle (labeled as T1), address and control ignals are set up. By the end of the next cycle (T2), the bus operation completes and a new external bus cycle may begin (Figure 1). The microprocessor bus is synchronous. During a READ cycle (at the end of T2), data is registered into the microprocessor at the rising edge of the system clock. During a WRITE cycle, data is made available to the memory device such that it can be registered at the end of T2. One of the many synchronous SRAM advantages is that WRITE pulses need not be generated. This advantage increases as bus frequency increases. Control signals are supplied at one clock's rising edge; data is supplied at the next rising edge.

Burst bus operation takes a shortcut by executing four consecutive external bus cycles. The first cycle requires the same setup and completion (T1 and T2). The next three cycles operate without the setup cycle (Figure 2). This is done by defining the sequence of addresses that follow the first issued address. PowerPC and Pentium differ in address sequence (PowerPC uses a linear burst sequence, whereas Pentium uses an interleaved sequence), but do not differ in the total burst length of four bus accesses. The Micron SyncBurst SRAM supports both linear and interleaved burst sequences by incorporating a two-bit burst counter that tracks the internal address generation of the target microprocessor. Note in Figure 2 that some microprocessors, such as Intel's 486, attempt to alter the address to reflect the burst sequence (only the two least significant external address lines change) but they don't do this fast enough to be useful. An SRAM without the burst counter must receive the lower two address bits long before the

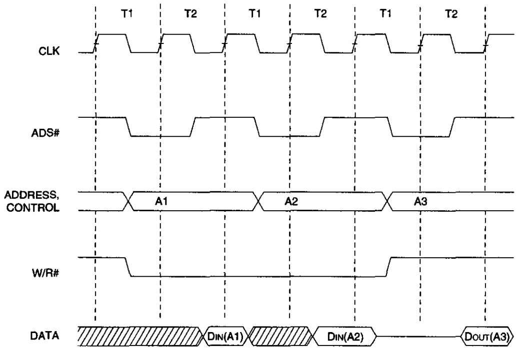


Figure 1
TWO-CYCLE MICROPROCESSOR BUS OPERATION

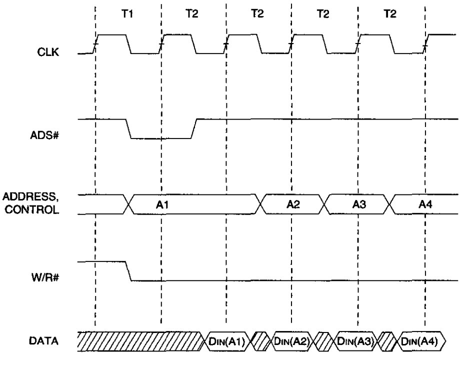


Figure 2
BURST CYCLE OPERATION

microprocessor can supply them. This requires logic external to the microprocessor and SRAM, resulting in additional system delays. The SyncBurst SRAM adds no such delay.

The foregoing describes just one of several SyncBurst SRAM advantages. Cache controller ASICs (application-specific integrated circuits) do not operate efficiently if they use the bus during WRITE cycles in the same manner as microprocessors. If address and data are both known, sending them simultaneously to the SRAM (this is called an EARLY WRITE) is better than having data follow the address by one clock cycle as the microprocessor does (this is called a LATE WRITE). The SyncBurst SRAM supports both EARLY WRITE (using ADSC# as the address control signal) and LATE WRITE (using ADSP# as the address control signal) so that both microprocessor and cache controller cycles are optimized. Figure 3 shows the difference between LATE WRITE (ADSP#-controlled) and EARLY WRITE (ADSC#-controlled). Note that EARLY WRITE cycles permit a new address to be used once every clock whereas LATE WRITE cycles only permit WRITEs to new addresses every second clock. READ cycles can actually be performed at the rate of one new access per clock regardless of being ADSP# or ADSC# initiated, although when using microprocessors such as PowerPC and Pentium the microprocessor is the limiting factor (recall the two-cycle normal bus operation).

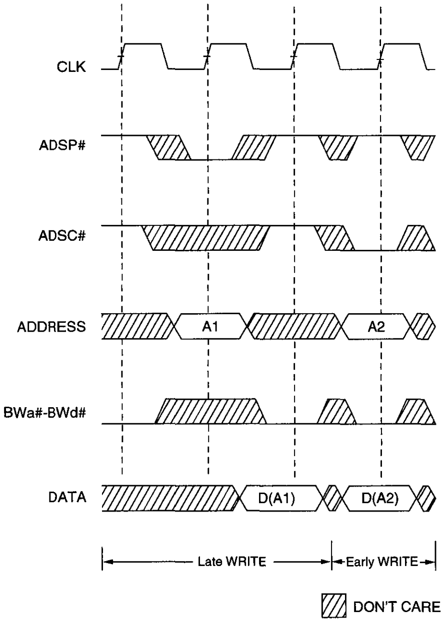


Figure 3
LATE WRITE AND EARLY WRITE IN THE SYNCBURST SRAM

ASIC DESIGNS

ASICs "want" to run synchronously. If their internal design is very small, synchronicity is less critical. But if the ASIC design is large enough to need an external SRAM, synchronicity becomes important to the system design. The first step in the design process is to "synchronize" the ASIC to the "outside world." This involves the use of registers or latches to make the interface signals appear to be synchronous whether or not they are. If the SRAM that interfaces with the ASIC is synchronous, then the task is already done. The OE# signal is the only one in Micron's SyncBurst family that is asynchronous, but it can easily be treated as synchronous. Figure 4 illustrates a low-pin-count circuit while Figure 5 shows the timing relationships between the ASIC and SyncBurst SRAM during READ and WRITE cycles. Minimal control signals are used in this application. OE# is toggled on CLK rising edges whereas the synchronous signals are toggled on CLK falling edges. The latter ensures that very generous setup and hold times are provided to the SyncBurst SRAM. In this example, the transition from READ cycles to WRITE cycles requires a dummy READ with OE# HIGH to allow the bus to make room for input data. The gap is apparent on the data bus at the transition from WRITE cycles to READ cycles.

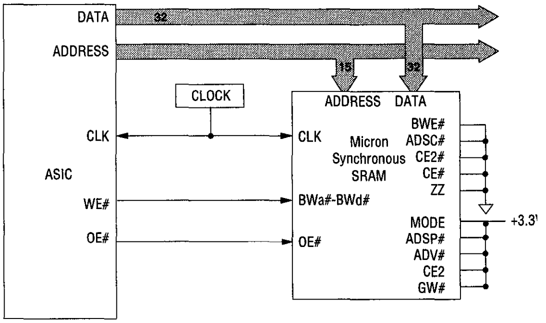


Figure 4
MINIMUM ASIC SYNCHRONOUS INTERFACE, OE#-CONTROLLED

USING SYNCBURST SRAMs IN PLACE OF ASYNCHRONOUS SRAMs

Whenever a clock signal is available, SyncBurst SRAMs can be used in place of asynchronous SRAMs through two distinct approaches. The first involves a design similar to he one illustrated in Figure 4. In this case, synchronous SRAMs are desired but without additional ASIC control pins that aren't needed for an asynchronous SRAM soluion. Often, solutions are I/O-bound and not gate-bound; herefore, extra pins can add cost to a product. The second approach involves the creation of a signal internal to the ASIC that helps speed up the bus frequency when READ nd WRITE cycles are intermixed frequently.

The only requirement for this first method to work is that a clock signal (CLK) must be available. The logic connecions of control signals that are static are shown in Figure 6. MODE is shown connected HIGH, but could also be LOW or even unconnected. Addresses are generated by the ASIC t the falling edges of CLK. The only signals that must be ontrolled are BWa# through BWd# and CE#. OE# can lways be LOW if bus contention with other devices is not a concern. The BW# signals can all be driven from a ingle ASIC pin if only full bus-width operations will be erformed. A minor performance reduction will be experinced using this control structure. One idle cycle will apear on the data bus (Figure 7) every time a transition from WRITE to READ (and not vice versa) occurs. If many WRITE cycles occur consecutively followed by many consecutive READ cycles, the performance change will be arely noticeable. If the system constantly changes between EAD and WRITE cycles, the bus speed will appear to be two thirds of the clock frequency. The actual number of control signals from the ASIC is the same as in the Figure 4 design solution. The difference lies only in which signals are selected. The Figure 6 solution is easier to implement because all ASIC outputs are produced at the falling edge of CLOCK whereas the Figure 4 solution mixes edges (due to OE# control).

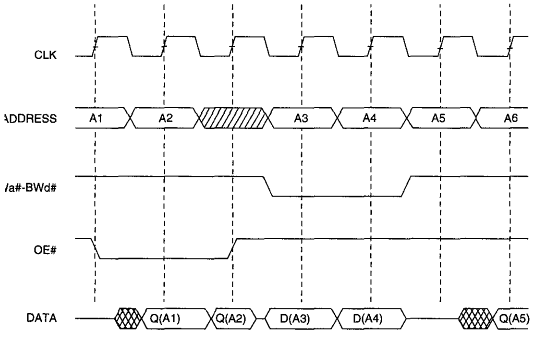


Figure 5
SYNCBURST SRAM TIMING IN ASIC APPLICATION

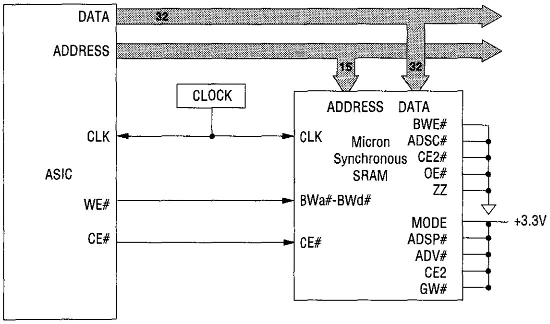


Figure 6
MINIMUM ASIC SYNCHRONOUS INTERFACE, CE#-CONTROLLED

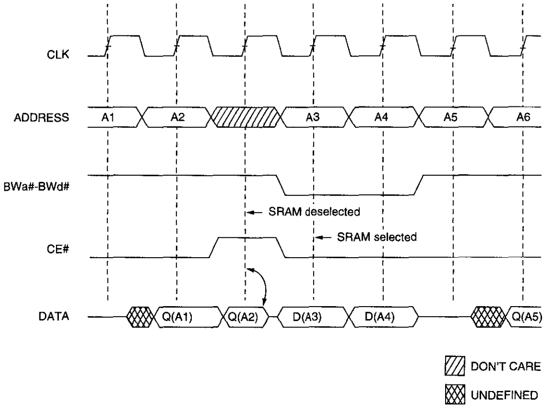


Figure 7
SYNCBURST SRAM TIMING, CE#-CONTROLLED ASIC APPLICATION

TREATING SYNCBURST SRAMs LIKE ASYNCHRONOUS SRAMs

Some designs can't tolerate any idle cycles on the bus. This can still be accommodated using the SyncBurst SRAM. There are two keys to making this work. The first is to ensure that the SyncBurst SRAM access time is sufficient. It will not have a full clock cycle to output data to the ASIC. The second is to design the ASIC such that it can register the input data before the rising edge of CLK. The bus must be clear before the next CLK rising edge so that either a READ or a WRITE may occur once per clock. This can be done by using extraneous gate delays with inversion from the falling edge of CLK in order to create an internal reference for registering input data inside the ASIC (see ICLK, Figure 8). OE# transitions must occur such that the SRAM tristates its data outputs before the ASIC drives the data bus to allow contention-free read-write transitions.

Figure 8 shows the relationship between signals. The critical path is the transition from READ to WRITE cycles: data must be registered into the ASIC before it can output data; OE# must be timed to tristate the data bus in time but not so soon that the data has insufficient time to be registered. This is clearly a more difficult internal ASIC design because the timing for the ASIC output signals is much more critical than in the previous examples. Care must be taken to account for maximum and minimum propagation delays inside the ASIC and also in the SRAM, particularly in the High-Z and Low-Z parameters. However, if idle cycles are to be avoided in the system, this does provide a means for accomplishing that goal with no more control pins than required by asynchronous SRAMs.

SUMMARY

The robustness of control inputs in the SyncBurst SRAM makes it versatile enough for use in almost any application. This article demonstrates how it may be applied in pin-count sensitive applications and applications which are pin-count sensitive but cannot tolerate data-bus idle cycles. The ASIC design using SyncBurst SRAMs is simplified by having a primarily synchronous external interface and a self-timed write: no timing-critical write pulses need to be generated.

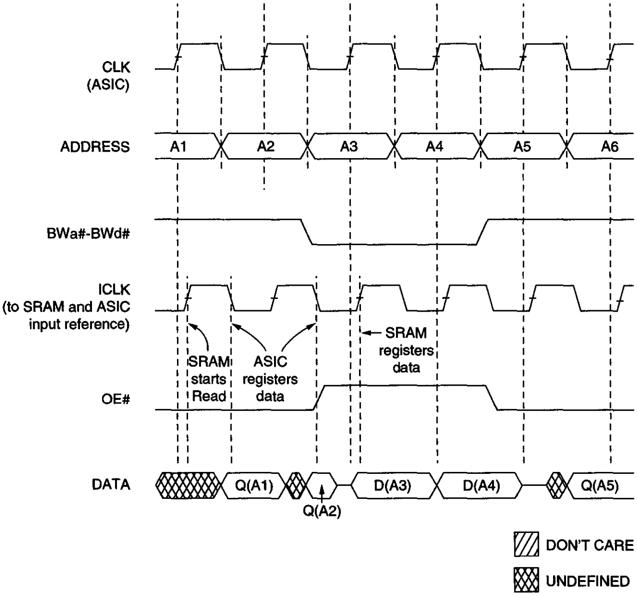


Figure 8
SYNCBURST SRAM TIMING, CE#-CONTROLLED ASIC APPLICATION

TECHNICAL NOTE

DESIGN TIPS: SYNCBURST™ SRAM STANDARDS

This article was originally published in 1994.

INTRODUCTION

Some users have the impression that there is no standard among SyncBurst™ SRAMs. This technical note deals with standardization issues as they pertain to PC designs: designing with today's parts, taking advantage of their features and avoiding redesign by taking into account all the JEDEC-defined features and options.

CHANGES SINCE ORIGINAL PART INTRODUCTION

Since the SyncBurst architecture was introduced and standardized through the JEDEC committee, many other vendors have decided to design and manufacture 1Mb, 2Mb and 4Mb devices in x18, x32 and x36 configurations. Most vendors have versions that vary from the original JEDEC pin assignment. The original JEDEC standard has undergone changes since its introduction, and Figure 1 illustrates the final standard.

32K/64K/128K x 32/36 SYNCHRONOUS BURST SRAM

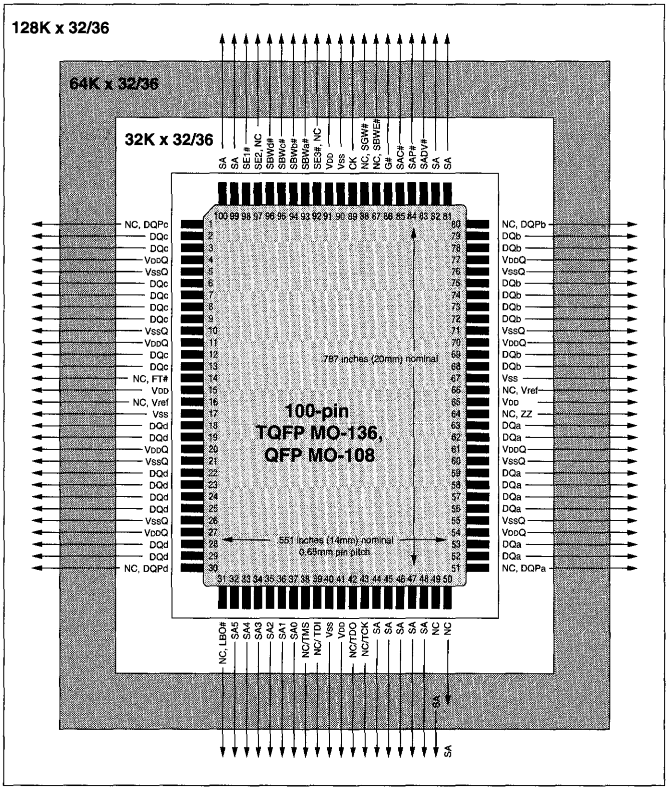


Figure 1
REVISED JEDEC STANDARD FOR x32/x36 SYNCHRONOUS SRAMs

The changes from the original standard are: remove PDIS from pin 87; add GW# on pin 88, BWE# on pin 87, FT# on pin 14, MODE or LBO# (optional) on pin 31 and ZZ (optional) on pin 64. Not all vendors support every function on these devices. But reserving a position for all anticipated functions allows designers to lay out their PCBs so that any vendor's part will work in their application. If a vendor chooses not to implement a function, the corresponding pin is a no connect and will not conflict with whatever logic level the pin has been tied to.

BENEFITS OF NEW SIGNALS

Linear burst order (LBO#), also called MODE in Micron devices, permits the user to select the burst sequence (pin 31). This is a static input; therefore, its state may not be changed during device operation. A LOW on this input selects linear burst sequence. A HIGH selects interleaved burst sequence. Linear and interleaved burst operate differently when the starting address is odd. Linear burst sequence is a simple modula-4 up-counter with wraparound whereas in interleaved burst, the least significant address bit toggles every cycle and the next significant bit toggles every other cycle. This is detailed in the device data sheets.

The benefit to the manufacturer for supporting this input is that fewer part types have to be supported. The benefit to the user is that more design flexibility is permitted, allowing a variety of microprocessors or ASIC designs to be considered with no cost penalties.

Global write (GW#) synchronous input provides a means to perform a full bus-width WRITE to the SRAM using a single pin. It is valuable to cache controllers when performing a line fill, since line fills are always in integer numbers of the full bus width. ASIC designs benefit from the reduction of load. Prior to this input, the byte write signals must all be brought LOW to perform a full-width WRITE resulting in a load of four signals per 32-bit bus width. If GW# input is not needed, it may be tied HIGH.

Byte write enable (BWE#) synchronous input works as a logical OR with the BWx# signals. The latter signals are ignored unless BWE# is LOW. This signal permits direct connection of microprocessor byte enables to the byte write lines of the SRAM (Figure 2). This results in two major benefits: zero-wait-state WRITEs and ASIC pin-count reduction. WRITE cycles are faster because ASIC logic delays, I/O buffers and extra PCB propagation delays are eliminated by directly connecting the microprocessor signals to the SRAM. Only a single critical path persists instead of eight input and eight output critical signal paths as is the case when the ASIC must translate the byte enables into byte writes for the SRAM (Figure 3). The single critical path is now converting the microprocessor read/write signal into a BWE# input to the SRAM. The single path is easier to manage and can be done without inducing wait-states. The second benefit is pin-count reduction in the ASIC (i.e., cache controller). Previously, eight input and eight output signals were needed for WRITEs. Now, only eight bidirectional signals and two outputs are needed to replace the function of 16 lines: a net savings of six pins in 64-bit applications. Figures 2 and 3 show the difference between systems that take advantage of GW# and BWE# and those that do not.

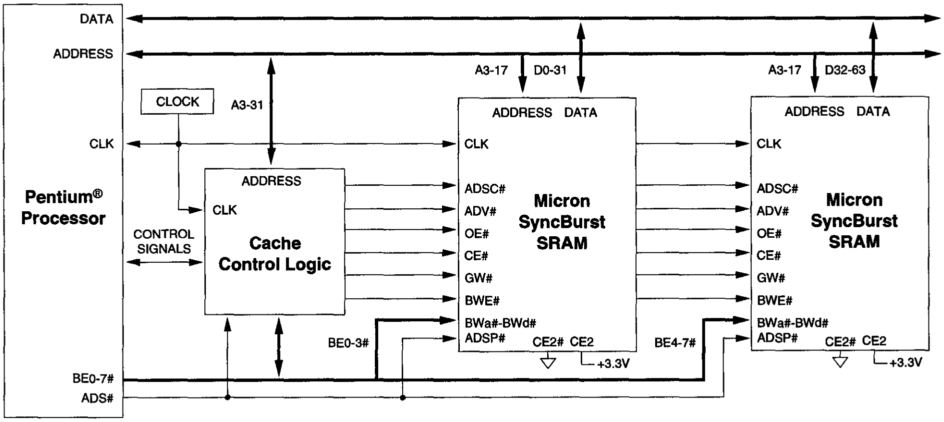


Figure 2
SYNCBURST SRAM DESIGN UTILIZING GW# AND BWE#

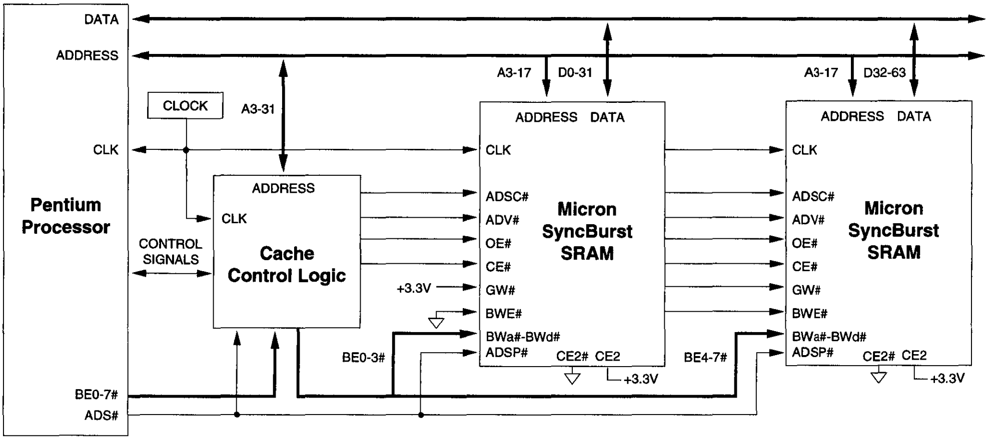


Figure 3
SYNCBURST SRAM DESIGN WITHOUT DIRECT CONNECTION OF BE# SIGNALS TO BW# SIGNALS

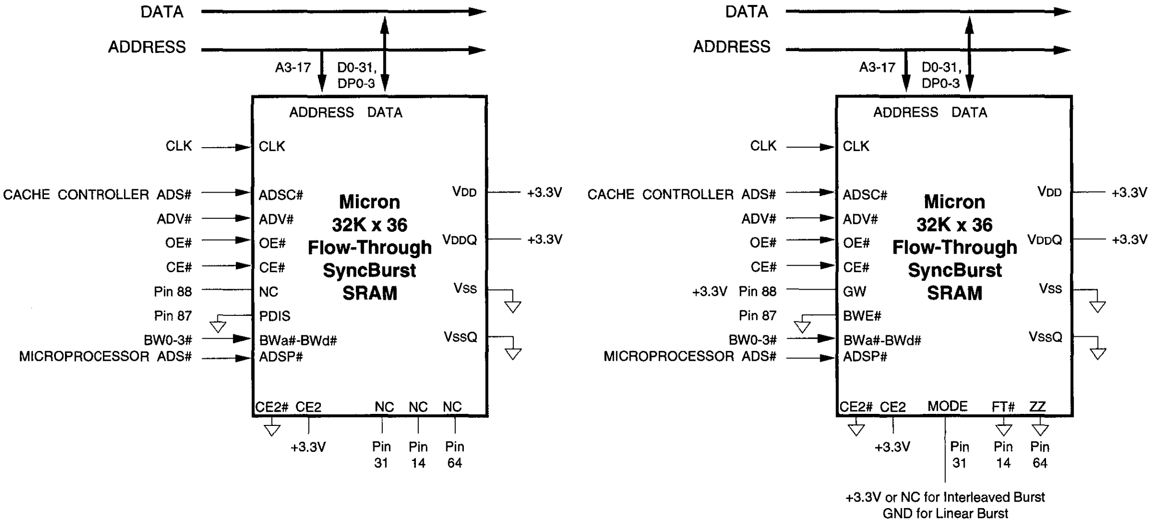
Flow-through (FT#) input is another static input. Some vendors will implement this input to allow user selection of pipelined (FT# = HIGH) or nonpipelined designs also called flow-through; i.e., no registers in series with device outputs. While vendor support of this additional mode-select input allows the same device to work in either regular or pipelined designs, many vendors do not plan to support it. Designers must strap the FT# pin to the logic level appropriate for the design to ensure that a wide selection of sources will operate in the design.

Snooze (ZZ) input is available from Micron. It will be included by some vendors to provide a way to put the SRAM into the lowest power standby mode (see I_{SB2Z} specification in the data sheets). Currently, the clock must be stopped and all inputs held within 0.2V of V_{DD} or V_{SS} to lower the standby power to the lowest level possible. ZZ held HIGH in the Micron device will cause the SRAM to enter into "sleep" mode in approximately two clock cycles in nonpipelined devices. Pipelined devices will take one extra clock cycle. After the device is "sleeping," the clock and all other inputs are ignored. To wake up the device, ZZ must be returned LOW. This permits the input registers and clock to respond to inputs. It is recommended that users plan for four clock cycles to go into sleep mode and four clocks to emerge from sleep mode to ensure no data is lost.

CONVERTING EXISTING DESIGNS TO ACCOMMODATE NEW FUNCTIONS

Figure 4 shows the connections for original and new devices in x36 nonpipelined applications. The differences on pins (mode) can be ignored when using the Micron devices in interleaved burst sequence operation. If linear burst is required, pin 31 must be connected to ground to enable use of new devices. It is recommended, however, that all connections shown in the "New Functionality" illustration be adhered to if multiple vendors' devices will be used. Pin 88 must be connected differently than in the original design. Pipelined applications differ only in the connection of FT# (pin 14) if multiple vendor support is desirable. Specifically, FT# should be tied to 3.3V to conform to the JEDEC standard.

Figure 5 shows the connections for original and new devices in x32 applications where x36 devices were the only available parts at the time. The same discussion as above applies except that pin 87 (formerly PDIS, now BWE#) must revert from a 3.3V connection to a ground connection.



x36 ORIGINAL FUNCTIONALITY

x36 NEW FUNCTIONALITY

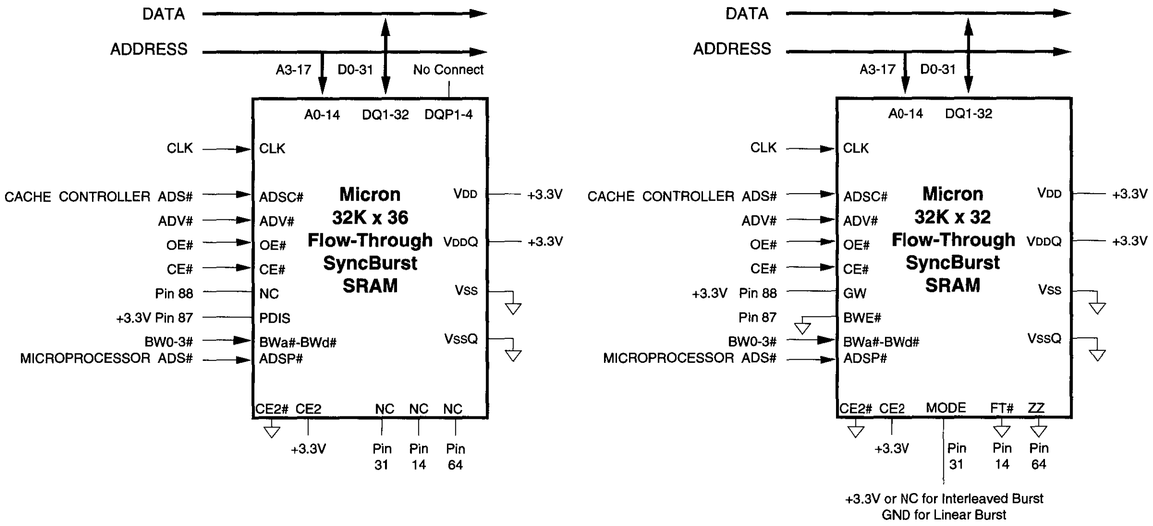
Figure 4
CONVERTING FROM ORIGINAL x36 DESIGNS TO NEW FUNCTIONALITY

NON-PC APPLICATIONS

Many non-PC applications use the devices in a different manner. For example, byte operations may not be required. In this case, all BW# signals are tied together in designs employing the original functionality. For compatibility, GW# should be tied HIGH and BWE# tied LOW. In the new designs, GW# can be used to reduce signal loading. GW# would be used to control WRITEs while BWE# and BWa# through BWd# would be tied HIGH. This reduces the control signal load from four to one for the WRITE control function.

SUMMARY

This article provides information which will enable designers to convert existing designs to be compatible with functional enhancements to the SyncBurst SRAM architecture. Further information is provided in Micron Technical Note TN-58-01, "Designing for Multiple SyncBurst SRAM Vendors."



x36 USED AS x32
ORIGINAL FUNCTIONALITY

x32 NEW FUNCTIONALITY

Figure 5
CONVERTING FROM ORIGINAL x36 USED AS x32 TO NEW FUNCTIONALITY

TECHNICAL NOTE

SYNCBURST™ SRAMs IN DSP APPLICATIONS

This article was originally published in 1995.

INTRODUCTION

The Micron® SyncBurst™ SRAM is not just for cache applications; it is also an excellent memory choice for digital signal processors (DSPs), embedded processors, gate array, and ASIC applications. Because the SyncBurst SRAM can provide advantages in performance board area, upgradeability and reduced package count, it should be considered for these applications.

WHY USE A SYNCHRONOUS SRAM?

Many DSPs are designed to operate with asynchronous memory. However, this does not mean that they can't use synchronous SRAMs. With careful design these applications can benefit by using SyncBurst SRAM. Systems designed to use asynchronous memory should use the flow-through or B3/B4 version of Micron's SyncBurst SRAM. This version has registered inputs and unregistered outputs. The flow-through device comes in 1Mb, 2Mb and 4Mb versions with x18, x32 and x36 bus widths. The pipelined version of the SRAM, which has both registered inputs and registered outputs, can also be used. However, the extra cycle delay due to the output registers frequently makes the flow-through device a better choice.

In many cases it is preferred to use synchronous over asynchronous parts. This could be due to reduced board area and height through the use of the space-efficient, 100-pin TQFP package. Due to its low height (1.5mm), this package should be considered for use on the reverse side of boards populated with chip capacitors and resistors only. For designs with modest memory requirements, the 64K x 32 or 128K x 32 SRAM can provide a single-chip memory solution and takes up only 3.5cm^2. Upgradeability is already defined through several generations with JEDEC-standardized pinouts for the 1Mb, 2Mb and 4Mb versions.

DSP MEMORY AND SYNCHRONOUS MEMORY

Numerous vendors produce DSP processors. These processors and their memory interfaces differ significantly so that there is not a generic method of connecting the SRAM to the processor. Designs must be carefully analyzed to ensure that the timing requirements of both the processor and memory are met.

Although there are a number of control signals on the SRAM itself, only a few are required in most designs. For example, functions such as synchronous address advance (ADV#) and burst sequence select (MODE) were developed for use with cache memories and can be ignored in systems that do not require the internal burst counter.

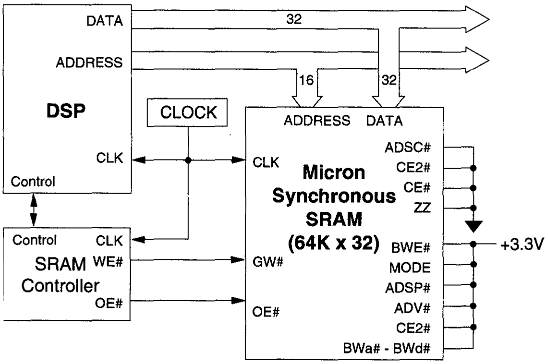


Figure 1
CONNECTING THE SYNCHRONOUS SRAM WITH A DSP PROCESSOR

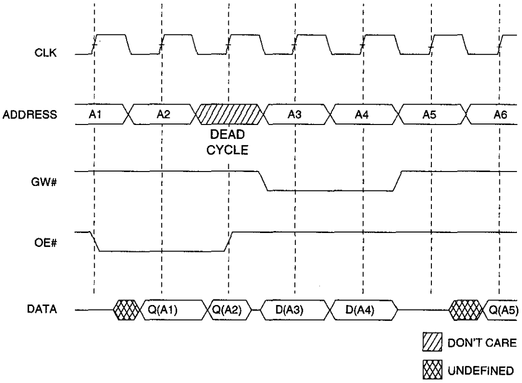


Figure 2
READ AND WRITE TIMING FOR THE SRAM

Wiring these signals inactive will minimize the pin count on the SRAM controller chip.

Figure 1 shows a typical method of connecting a synchronous flow-through SRAM to a DSP processor using a single-chip 64K x 36 device. Notice that only three active signals are required, including the clock (CLK), output enable (OE#) and global write (GW#). Figure 2 shows the timing for this setup. The global write signal toggles between READs and WRITEs and the output enable ensures that the output buffers enter a High-Z state before data is driven on the bus during a WRITE cycle. Notice that a dummy READ cycle is required when transitioning from READs to WRITEs. This is necessary in order to prevent bus contention. As shown in Figure 2, an idle cycle is required when transitioning from a READ to a WRITE cycle. Some designs may not be able to tolerate an idle cycle. Designing without an idle cycle is treated in Technical Note TN-58-03, "SyncBurst SRAMs in ASIC and Asynchronous Designs."

An alternative method of connecting the processor and SRAM is to use one of the chip enables (CE#) and the global write (GW#). OE# will be wired inactive. This method is also described in Technical Note TN-58-03.

Depth expansion may be required in order to obtain more words of memory. It is then necessary to separately control the two or more CE# signals in a CE#-controlled design or the OE# signals in an OE#-controlled design. This prevents bus contention on the DQ lines. Alternatively, output enable signals could be used to prevent contention.

AN EXAMPLE: THE TMX320C44 DSP PROCESSOR

To demonstrate DSP with SyncBurst memory, two processors have been chosen. The first is the TMX320C44 from Texas Instruments. This 32-bit processor is part of the '320 family of digital signal processors and is used in a wide variety of applications ranging from speech and image processing to digital control and parallel processing. A single-chip memory solution is demonstrated using a 64K x 32 SRAM (MT58LC64K32B3).

Connecting the Micron SyncBurst SRAM to the C44 processor will be as shown in Figure 1 with two exceptions. The clock used (H1) is generated internally on the processor and CE# versus OE# is used to control the SRAM (OE# is active). A number of control signals go from the DSP to the SRAM controller. These include data bus enable (DE#), address bus enable (AE#), status signals (STAT3-STAT0), lock signal (LOCK#), access strobes (STRB0#,1#), read/write signals (R/W0#,1#), page signals (PAGE0,1), ready signals (RDY0#,1#) and control enables (CE0#,1#). Although a number of signals may need to be evaluated to determine if the SRAM is being accessed, for a timing analysis, the most important signals to analyze are the R/W# and the CE# pins.

The timing diagram shown in Figure 3 has three sets of signals from the DSP: read/write (R/W#), address (A[23:0]) and data (D[31:0]). Two additional signals are shown which are generated from an ASIC or PAL which are the chip enable (CE#) and global write (GW#) signals to the SRAM.

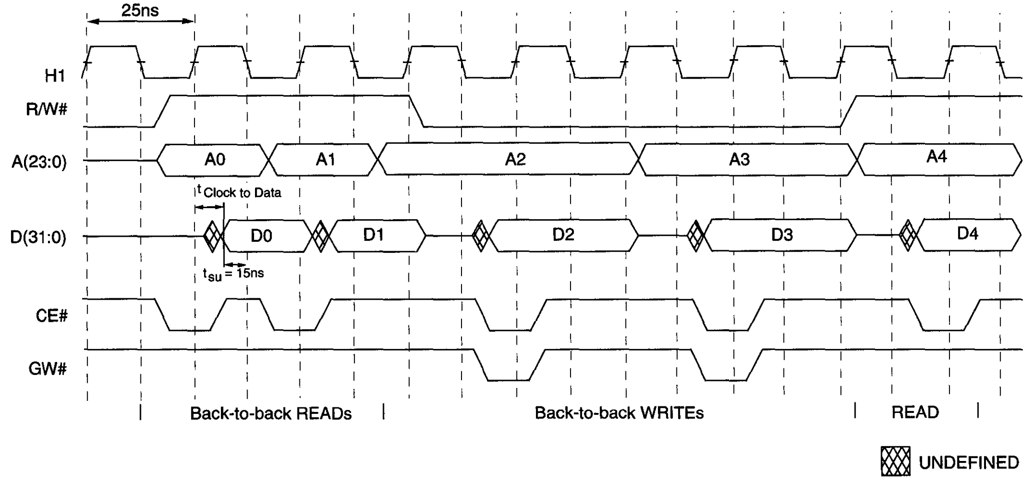


Figure 3
READ AND WRITE TIMING FOR THE TMX320C44 DSP PROCESSOR RUNNING AT 40 MHz

Two READs are performed followed by two immediate WRITEs and then another READ cycle. The SRAM controller generates both the CE# and R/W# to the SRAM. The critical timing occurs during the READ cycles. The rising edge of the H1 clock begins the READ cycle in the synchronous SRAM. The address is registered and data appears ^{t}KQ nanoseconds later. The data setup time for the DSP is 15ns for a 40 MHz signal. Assuming a flight time of 2ns, the SRAM must have a ^{t}KQ of 8ns. At 50 MHz, the setup time for the DSP changes to 10ns, but the cycle time also shortens so the SRAM must still have a ^{t}KQ of 8ns. Because such a fast device is required, it is important to minimize trace length and bus capacitive loading.

In practice, most users will probably insert a wait state to all READ and WRITE cycles. Even though 8ns devices are the fastest speed grade at this time, they are prohibitively expensive in most applications. All the above analysis takes into account a very fast flight time which can easily be exceeded by one or two nanoseconds of delay requiring an even faster ^{t}KQ. Flow-through SyncBurst SRAMs are not available with ^{t}KQs of 6ns or 7ns, so a wait-state should be inserted into the design.

Notice that the timing for the SyncBurst part is much tighter than that for an asynchronous one. An asynchronous part receives the address and does not wait for a rising edge of the clock to start a READ cycle like the SyncBurst part. Instead it immediately begins the READ cycle. During a READ cycle at 40 MHz, the address bits are valid 5ns before the rising edge of the clock so a total of 15ns are required from the time address goes valid to the time that data is needed at the processor. The SyncBurst SRAM has to wait for the rising edge of the clock before starting the READ cycle and loses 5ns. The benefit of this approach is simplified WRITE control (no write pulse).

A number of READ and WRITE cycles are shown in this example to demonstrate that the SRAM is never asked to perform a WRITE cycle immediately after a READ cycle. As mentioned earlier, it is easier to control the SRAM if there is at least one clock cycle between a WRITE and a READ cycle.

AN EXAMPLE: THE AMD AM29050 PROCESSOR

The AM29050, part of the AMD 29K family of RISC processors, is a 32-bit processor that operates at clock frequencies up to 40 MHz. It provides another excellent example of how to use the SyncBurst in a system originally designed for asynchronous components.

For this example, the 40 MHz version of the AM29050 will be used. To attain maximum performance, zero-wait-state READ and WRITE cycles are desired. Attaining this is difficult for both asynchronous or SyncBurst parts at this frequency. Figure 4 shows a waveform for a READ and WRITE cycle with no wait states. SYSCLK is the output clock from the microprocessor. To use the SRAM, an inverted clock called SYSCLK# must be generated. In this example, the delay through the inverter is assumed to be around 4ns. In the SyncBurst a READ begins on the rising edge of a clock cycle. However, valid data is expected 3.5ns before the rising edge of SYSCLK. This means SYSCLK must be inverted into the SRAM so the rising edge appears one-half clock cycle earlier and starts the READ cycle before data is required. Data ready or DRDY# is a signal that tells the AM29050 that data is valid. This signal can be delayed if wait states are necessary.

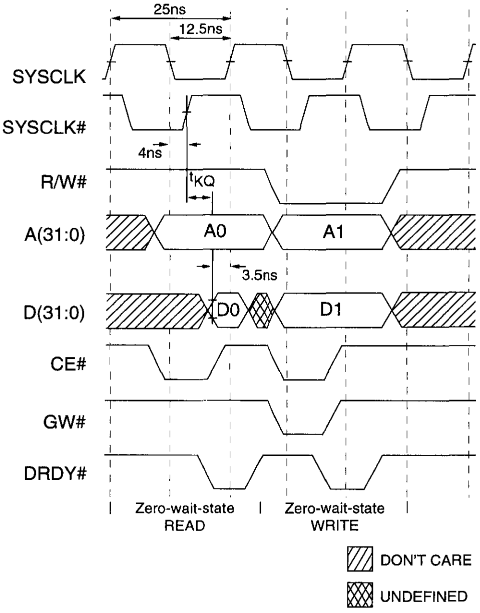


Figure 4
PERFORMING A ZERO-WAIT-STATE READ AND WRITE ON THE AM29050 PROCESSOR

The required speed grade of the SRAM can be determined from the drawing. Data must meet the setup time of the processor (3.5ns) before the rising edge of SYSCLK and the SRAM cannot begin the READ until the rising edge of SYSCLK# or 4ns after SYSCLK goes low. This means that ^{t}KQ and flight time cannot exceed 5ns. The fastest speed grades of flow-through SRAMs currently available have ^{t}KQs of 8ns and 9ns and cannot meet this timing. A wait state must be inserted.

Figure 5 shows a single wait-state READ and WRITE cycle. Notice that the timing is considerably relaxed from Figure 4. The time from the rising edge of SYSCLK# to the time data must be valid to the processor is 17.5ns. Even with a flight time of 5ns, a ^{t}KQ of 12ns can be used. Since multiple manufacturers produce a 12ns part, this part can be easily procured. The WRITE timing can also be met using this speed grade.

Notice that ^{t}X is used in Figure 5 versus ^{t}KQ in Figure 4. In Figure 4 only one clock rising edge occurs before data must be valid, but in Figure 5 two rising clock edges are presented to the SRAM before data is valid. Since ^{t}X is more than a full cycle time, ^{t}KQ is not really a valid term to use in the diagram.

CONCLUSION

The Micron SyncBurst family of SRAMs gives users an additional choice of high-speed memory for DSPs, embedded processors, RISC and ASIC applications. Although these applications have been designed for asynchronous SRAMs, they can be modified to use the SyncBurst family of SRAMs. SyncBurst offers the advantage of reducing board area and allowing upgradeability to 2Mb and 4Mb versions.

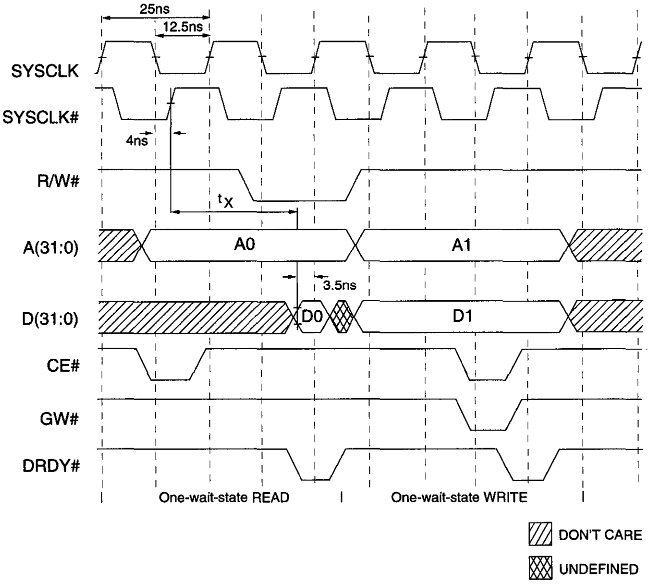


Figure 5
PERFORMING A SINGLE WAIT-STATE READ AND WRITE ON THE AM29050 PROCESSOR

TECHNICAL NOTE

CHOOSING THE RIGHT SYNCBURST™ SRAM

This article was originally published in 1995.

INTRODUCTION

Three different versions of the Micron® SyncBurst™ SRAM are available (flow-through, single-cycle deselect [SCD] pipelined and double-cycle deselect [DCD] pipelined). Choosing between the different versions is based upon a number of factors. The purpose of this article is to provide a means to determine which SyncBurst part to choose for a particular application.

CHOOSING PIPELINED vs. FLOW-THROUGH

Micron offers two different pipelined versions and one flow-through version of the SyncBurst SRAM as shown in Table 1. The pipelined versions have input registers and output registers. The flow-through or nonpipelined versions only have input registers. Because of the output register, pipelined parts have an extra cycle of delay before data is valid (during a READ) versus flow-through devices. (See Table 1.)

For cache applications, choosing an SRAM also includes choosing the chipset. This decision is usually based upon system price, performance and chipset support. Table 2 shows the performance for cache applications at various bus frequencies and assumes a cache architecture similar to that shown in Figure 1.

High-performance microprocessors such as Pentium® and PowerPC™ burst four words of data from the cache at a time. In Table 2, the READ and WRITE performance of the cache is the number of cycles required for each of those four accesses. For instance, a pipelined device operating at 66 MHz takes three cycles to do the first READ, but only one cycle for each additional READ or a total of six cycles to access four words (3-1-1-1).

The bolded text in Table 2 represents the highest performing option for each frequency. Although not shown, asynchronous parts are equivalent in performance to flow-through parts at frequencies below 50 MHz. These bus frequencies are not shown since most current designs operate above 50 MHz. From 50 MHz to 66 MHz, flow-through devices are the highest-performing solution, allowing four accesses in five cycles versus six for a pipelined READ and nine for asynchronous devices. Above 66 MHz, the pipelined devices offer a clear advantage by allowing single-cycle access for burst cycles after the first READ. Remember that this is the performance of the SRAM alone and assumes that the rest of the system (especially the tag match) operates quickly enough to take advantage of this performance.

For ASIC or DSP applications, the flow-through device is frequently used. This is because many of these applications cannot tolerate the extra cycle of delay associated with pipelined parts when retrieving data. Pipelined parts do have a place in applications where maximizing bandwidth is critical. Users need to be aware that pipelined parts require a one-cycle delay when switching from READs to WRITEs in order to prevent bus contention.

Table 1
SYNCBURST SRAM VERSIONS

VERSION	DESCRIPTION
Flow-Through	A synchronous SRAM with registers on the input signals.
Pipelined with Single-Cycle Deselect (SCD)	A synchronous SRAM with registers on both the input and output signals. Single-cycle deselect. Conforms to the Intel® BSRAM specification.
Pipelined with Double-Cycle Deselect (DCD)	A synchronous SRAM with registers on both the input and output signals. Double-cycle deselect.

Table 2
SRAM PERFORMANCE COMPARISON

	3.3V 32K x 8				**32K x 32 PIPELINED**			**32K x 32 NONPIPELINED**			
Bus Frequency	Speed	Banks	Performance Read	Performance Write	Cycle Time	Performance Read	Performance Write	Access Time	Cycle Time	Performance Read	Performance Write
50	20ns	1	3-2-2-2	4-2-2-2	20	3-1-1-1	2-1-1-1	**12**	**20**	**2-1-1-1**	**2-1-1-1**
60	15ns	1	3-3-3-3	4-3-3-3	16.7	3-1-1-1	2-1-1-1	**10**	**16.7**	**2-1-1-1**	**2-1-1-1**
		2	3-2-2-2	4-2-2-2							
66	12ns	1	3-3-3-3	4-4-4-4	15	3-1-1-1	2-1-1-1	**9**	**15**	**2-1-1-1**	**2-1-1-1**
	15ns	2	3-2-2-2	4-2-2-2							
75	15ns	2	3-2-2-2	4-2-2-2	**13.3**	**3-1-1-1**	**2-1-1-1**	9	13.3	3-2-2-2	3-2-2-2
83	12ns	2	3-2-2-2	4-2-2-2	**12**	**3-1-1-1**	**2-1-1-1**	9	12	3-2-2-2	3-2-2-2
100	10ns	2	3-2-2-2	4-2-2-2	**10**	**3-1-1-1**	**2-1-1-1**	9	10	3-2-2-2	3-2-2-2
125	8ns	2	3-2-2-2	4-2-2-2	**8**	**3-1-1-1**	**2-1-1-1**	9	8	3-2-2-2	3-2-2-2

CHOOSING THE RIGHT PIPELINED VERSION

Because Micron has two different types of pipelined SRAMs, it is important for designers to choose the version that best meets their needs. Figure 2 shows the difference between the C5/C6 and D8/D9 versions of the pipelined SRAMs. This diagram shows a READ cycle followed by three advance cycles and then a deselect cycle. The C5/C6 device reads out all four words, but the D8/D9 cuts off the last word. To read all four words out of the D8/D9 device, the deselect command must be delayed one cycle.

Micron designed the D8/D9 version to be compatible with the Intel® BSRAM specification. This specification was developed to ensure that there is no possibility of bus contention in a system with multiple banks of SRAM. This could occur when switching between two or more banks of SRAMs if parts from different vendors are used, or if the banks are separated by electrically long paths. This bus contention could occur during the READ transition if the turn-on and turn-off times for the DQ lines vary significantly among manufacturers.

Although we do not recommend mixing parts from different vendors on the same board, this may be difficult to implement in practice. Take for example the system shown in Figure 1. Assume this system is implemented using 32K x 36 SRAMs. Then the Low Memory and High Memory boxes each represent two 32K x 36 SRAMs. The Low Mem box is comprised of two parts soldered onto the motherboard and shipped in a product with a 256KB cache memory. High Mem is located on a module that was added by the customer to increase cache size to 512KB. Because multiple manufacturers are producing SyncBurst parts, it is unlikely that the parts on the module will be from the same vendor as those on the motherboard. This is especially true if a customer buys a module from an aftermarket supplier of modules.

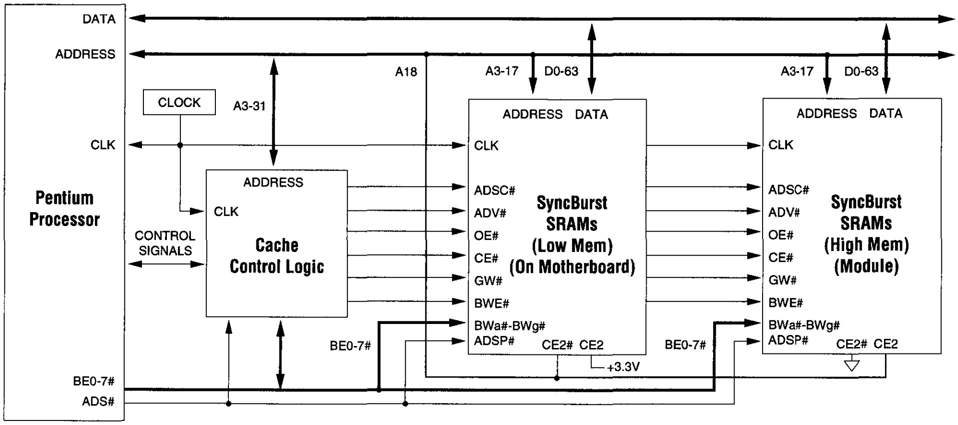


Figure 1
A TYPICAL PENTIUM AND CACHE MEMORY SYSTEM

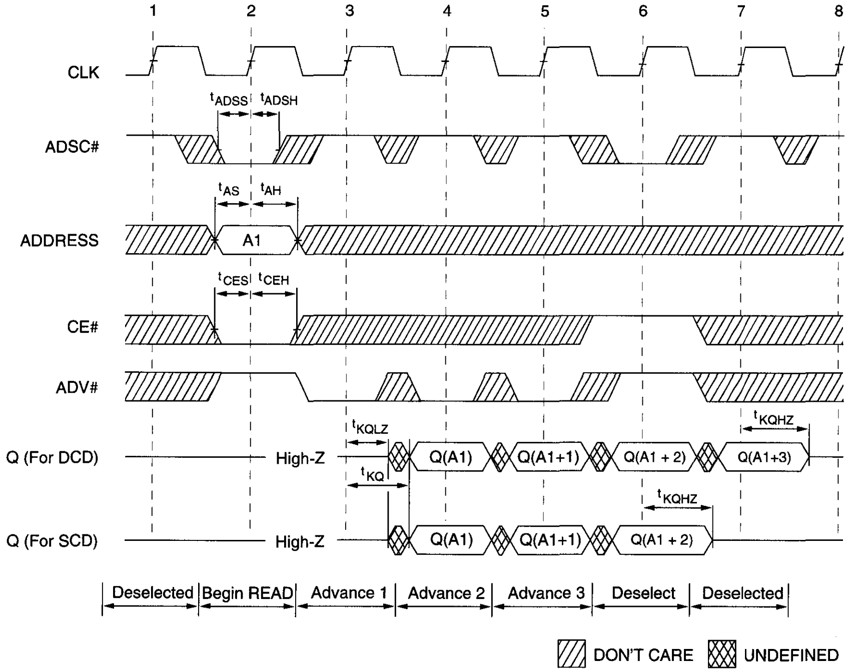
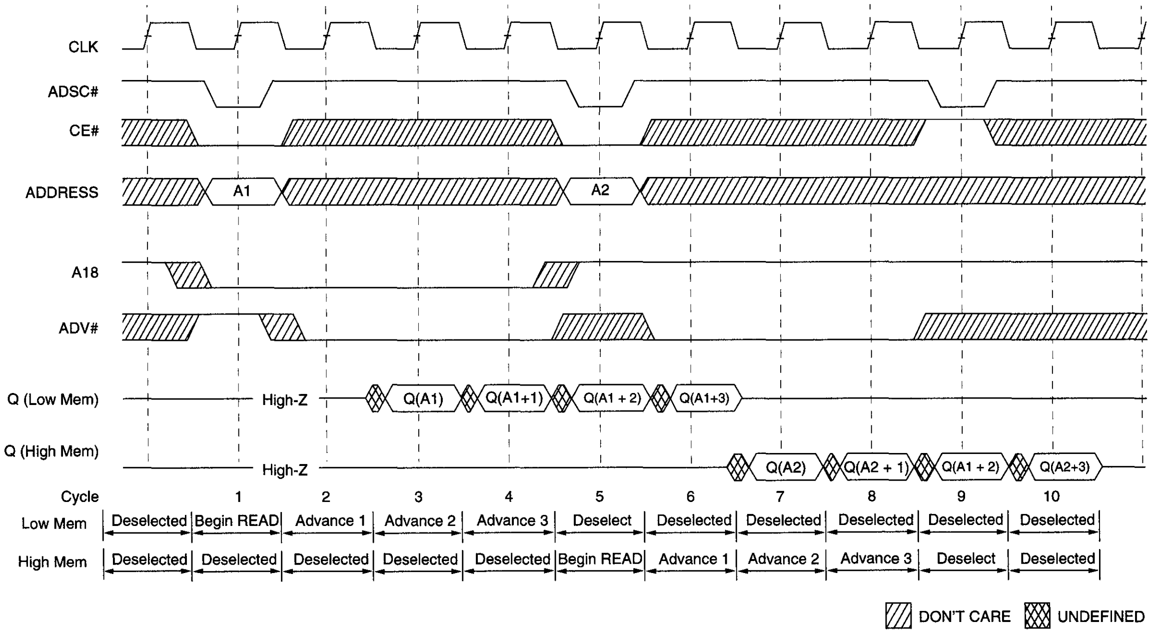


Figure 2
SINGLE-CYCLE DESELECT (D8/D9) vs. DOUBLE-CYCLE DESELECT (C5/C6)

Figures 3 and 4 show how to execute two sequential burst READs using the implementation shown in Figure 1. The first burst READ occurs in the Low Mem, the second in High Mem. Selecting a bank is done by connecting A18 to CE2 on High Mem and CE2# on Low Mem. As you can see, using the C5/C6 part allows eight words to be read out in 10 cycles (3-1-1-1, 1-1-1-1) versus 11 cycles (3-1-1-1, 2-1-1-1) for the D8/D9 part.

The extra delay is required because A18 is used to select banks. Cache controllers output only one ADSC# to keep pin count to an absolute minimum. It is possible to use D8/D9 parts and perform two burst READs in 10 cycles, but the design must be modified. Using D8/D9 parts, the deselect to one bank must be delayed one cycle after the select signal for the other bank so that two signals are necessary. Chipset vendors will probably not choose this implementation in order to save pins.

For cache users it is important to select an SRAM and a chipset that are compatible and provide the required performance. For greatest availability of parts, a chipset might be chosen that supports both C5/C6 and D8/D9. For best performance on a single bank only system, a C5/C6 might be the best solution. It is important for cache designers to check with their chipset vendor to verify the type(s) of SyncBurst SRAM they support. Most chipsets only support the BSRAM standard and can only use D8/D9 parts. Other chipsets may be able to use both C5/C6 and D8/D9 parts, but leave a dead cycle between bank switching, so even if you use the C5/C6 versions, there is no performance advantage. Others may support both C5/C6 and D8/D9, but give a performance advantage if the C5/C6 parts are chosen.



Cycle		1	2	3	4	5	6	7	8	9	10
Low Mem	Deselected	Begin READ	Advance 1	Advance 2	Advance 3	Deselect	Deselected	Deselected	Deselected	Deselected	Deselected
High Mem	Deselected	Deselected	Deselected	Deselected	Deselected	Begin READ	Advance 1	Advance 2	Advance 3	Deselect	Deselected

Figure 3
BACK-TO-BACK BURST READS USING A C5/C6 PIPELINED PART

DESIGNING FOR BOTH C5/C6 AND D8/D9 VERSIONS

To have the widest supply base or when fastest performance is not an issue, users can create a design that can use both C5/C6 and D8/D9. One way of doing this is to detect what type of SRAM (C5/C6 or D8/D9) is in the system and then configure the DESELECT cycle accordingly. During boot-up/power-up, the system can test to see if a C5/C6 or D8/D9 SRAM is present. This can be done by writing four sequential words into the SRAM and then burst reading them out with a DESELECT cycle occurring after the last ADV# cycle (See Figure 2). If a C5/C6 is in the system, all four words will be read correctly; if D8/D9, only three words will be read correctly. A pattern of words such as FFFF, 0000, AAAA, 5555 should be chosen. This type of test could be advantageous when interfacing to an ASIC.

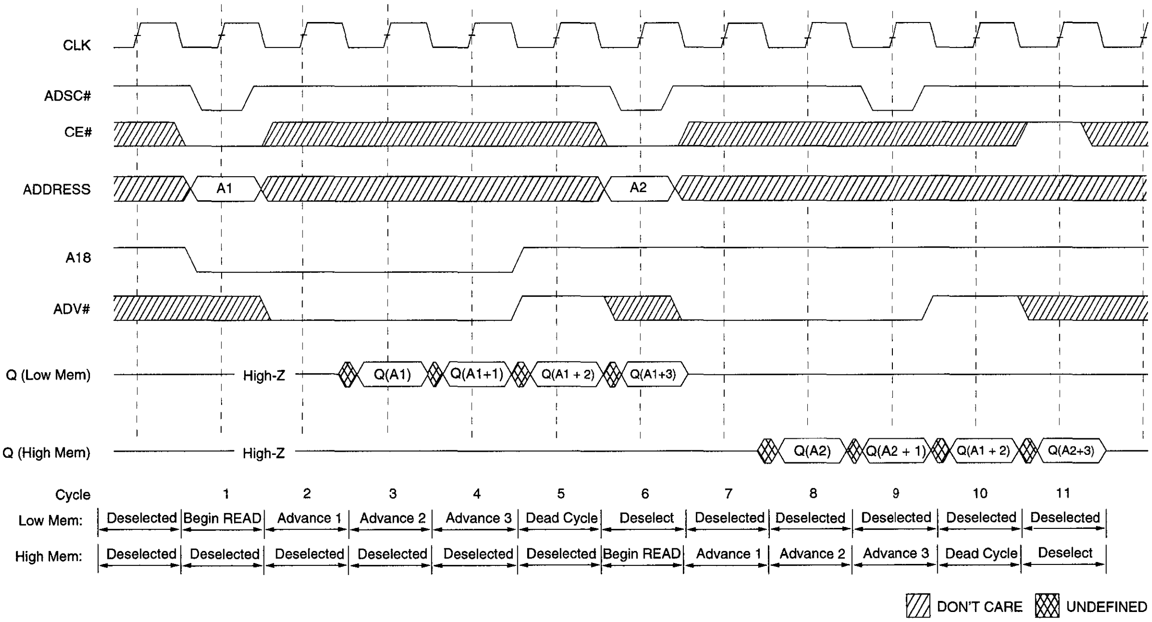


Figure 4
BACK-TO-BACK BURST READS USING A D8/D9 PIPELINED PART

Another method is to design a memory interface that can accommodate either the C5/C6 or D8/D9 versions without any modifications during power-up or boot-up. This can be done using the setup shown in Figure 1 and always inserting a dead cycle. This method allows the simplest and lowest pin count interface, but does take a performance hit when doing back-to-back READs. An example of how this system will operate with C5/C6 or D8/D9 parts is shown in Figure 5.

TO BANK OR NOT TO BANK

With the widespread availability of 64K x 32 SyncBurst parts, there is no need to bank in PC cache designs because two of these chips now make up a single-bank solution. Banking will still be used in many systems (typically noncache applications) that require large memory arrays.

CONCLUSION

Choosing the right SyncBurst SRAM is usually a matter of price versus performance. For cache users, the chipset choice also influences the SRAM selection. The new D8/D9 versions complement the product lineup by offering a device that is compatible with Intel's BSRAM specification. Micron offers a wide variety of synchronous SRAMs to meet the needs of the cache, telecommunications and ASIC user.

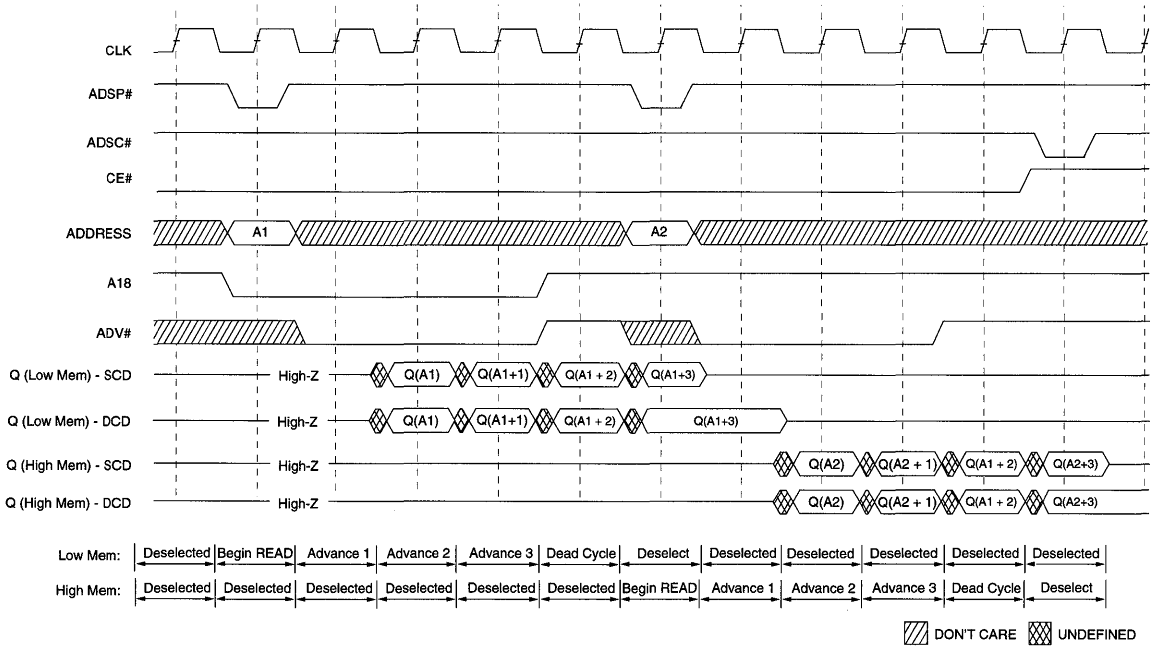


Figure 5
DESIGNING FOR BOTH C5/C6 AND D8/D9 VERSIONS

TECHNICAL NOTE

BANKING SYNCBURST™ SRAMs

This article was originally published in 1997.

INTRODUCTION

SyncBurst™ SRAMs have become the memory of choice in many applications that require an excellent price/performance ratio. Many of these applications may need to have multiple banks of SRAMs because the number of addresses required exceeds the size of the memory. This article discusses implementation of banked/unbanked cache for Pentium® as well as telecommunications, networking and other noncache applications.

IMPLEMENTATION OF CACHE MEMORY IN PENTIUM SYSTEMS

Cache memory used with microprocessors provides quick access to frequently used information and is implemented using SRAMs. The use of SyncBurst SRAMs improves system performance because SRAM processor frequencies greatly exceed main memory (DRAM) speeds. Microprocessors such as Pentium and PowerPC™ typically have a x64-wide or x72-wide data bus. The most popular cache memory sizes have been 256KB (32K x 64/72) and 512KB (64K x 64/72).

Early in the production of Pentium systems, cache SRAM memory was relatively scarce and a number of different solutions existed. Users could choose from the 3.3-volt 32K x 8, 5-volt 32K x 8, 5-volt 64K x 18, 3.3-volt 64K x 18 or 3.3-volt 32K x 32 configurations. Rather than implement a multitude of various motherboard designs to accommodate each of these versions, manufacturers chose a module solution using Intel's Cache-on-a-Stick (COASt) standard (see options A and B in Figure 1). Option A includes footprints for 256KB of cache (two 1Mb SyncBurst SRAMs) and a tag as well as the module. The idea here is that the manufacturer will provide 256KB of memory and the user can upgrade using a memory module. Option B exclusively uses a module. A 32K x 8 asynchronous tag is used throughout Figure 1.

The optimal solution for 256KB cache memory is two 32K x 32 SRAMs. But implementing this solution using option A or B is not efficient in terms of board space. There is the added penalty of increased cost due to the connector and circuit board required for the module. Now that SyncBurst SRAMs are readily available and cost effective, there is little point in providing for modules on the motherboard.

The best choice when using only 1Mb SRAMs is option C. In this method, two SRAMs are used for 256KB of cache memory (32K x 64/72) or four SRAMs for 512KB of cache memory (64K x 64/72). The connector and board are eliminated.

Although option C provides an advantage in terms of cost, it is still not the most efficient alternative now that 2Mb SRAMs are available. Option D uses the same two 100-pin TQFP footprints for either 1Mb or 2Mb devices. Option D requires only three footprints per board for a

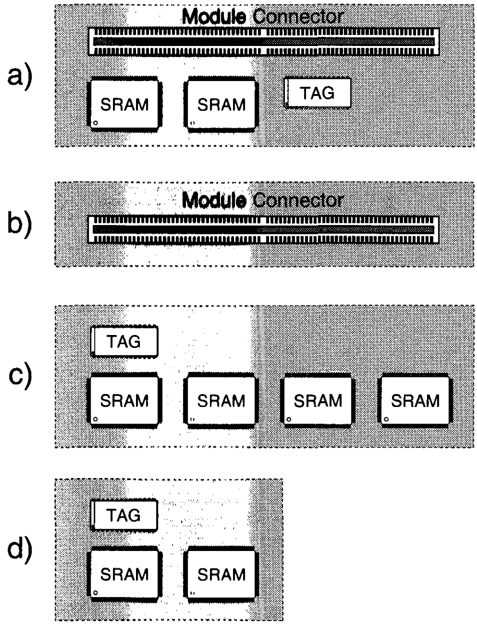


Figure 1
MOTHERBOARD LAYOUTS FOR CACHE MEMORY:
a) MODULE AND FOOTPRINTS
b) MODULE-ONLY
c) FOOTPRINTS FOR 1Mb SRAMs
d) FOOTPRINTS FOR 1Mb AND 2Mb SRAMs

minimal board area of 1.33 in^2. For a 256KB cache solution, only two 1Mb SRAMs are required. For a 512KB cache solution, two 2Mb SRAMs are required. Since they use the same package, the 512KB solution takes no more space than the 256KB solution.

Table 1 shows the four cache solutions and compares them in terms of motherboard area, power, address loading and data loading for both 256KB and 512KB requirements. Note that capacitive loading does not include the loading of the microprocessor but only trace routing, connector and memory devices (including tag for address).

512KB solutions (Table 1b) are implemented using four 1Mb chips on a module (options A1 and B1) and two 2Mb chips (A2 and B2). Just as the option in Figure 1d can be implemented on a motherboard with either two 1Mb SRAMs (256KB) or two 2Mb SRAMs (512KB), a module can also be made with just two footprints.

There are several advantages to implementing a module with only two footprints. Similar to the motherboard, the trace lengths are shorter, resulting in less resistance, inductance and capacitance. The Intel COASt module standard states that transmission line termination can be avoided if the module trace lengths are kept to less than 1.5 inches. This is difficult, at best, in a 512KB module implementation that uses four 1Mb SRAMs.

BANKING OF MEMORY IN PENTIUM SYSTEMS

Banking of memory is done when the depth of memory required exceeds the depth of the memory device. For example, using 1Mb SRAMs, the deepest x32 device available is 32K x 32. If a 64K x 64 memory is required, then four devices must be used (as shown in Figure 2a). In this implementation, the high order address bit (A15) is used to select between one bank and the other.

One of the challenges in banking memory is ensuring that there is no bus contention between parts when switching from one bank to another during READ cycles. A guaranteed way of dealing with this is to insert a dead cycle whenever switching between banks (as shown in Figure 3). This is typically the method in which a dual-banked 512KB memory in Pentium systems avoids bus contention. A full description of this method is included in Micron Technical Note TN-58-06, "Choosing the Right SyncBurst SRAM."

The penalty with the method shown in Figure 3 is an extra cycle, or nine cycles for reading eight words, versus eight cycles. This is an overhead of 12.5 percent during the READ cycles. However, this penalty can be completely avoided by using a 2Mb SRAM (64K x 32). A single-bank 512KB cache eliminates the dead cycle between bank

Table 1a
256KB CACHE SOLUTIONS

	A	B	C	D
Board Area (in^2)	2.90	1.56	2.42	1.33
Address Loading (pF)	19.5	18.5	15.5	14.5
Data Loading (pF)	14	13	11.5	10.5
Power Dissipation (watts, 66 MHz)	1.88	1.88	1.88	1.88

Table 1b
512KB CACHE SOLUTIONS

	A1	A2	B1	B2	C	D
Board Area (in^2)	2.90	2.90	1.56	1.56	2.42	1.33
Address Loading (pF)	26	19.5	25	18.5	21.5	14.5
Data Loading (pF)	22.5	14	21.5	13	19.5	10.5
Power Dissipation (watts, 66 MHz)	3.4	1.88	3.4	1.8	3.4	1.8

accesses. Chipsets can exploit the advantage of a single-banked 512KB memory and eliminate the extra wait state. The overall system performance increase from 512KB dual bank to 512KB single bank is expected to be around one or two percent in a Pentium system.

Although Pentium systems using two banks choose to add a wait state between banks, there is no inherent reason to do so in non-Pentium applications. Pentium designers have been concerned about bus contention between banks in a 512KB system since each bank could be from a different memory vendor. For instance, a consumer might buy a system with 256KB of cache memory on the motherboard and upgrade with a module later (Figure 1a). There was a concern that bus contention could occur since turn-on and turn-off times may differ between vendors.

However, in many noncache applications (such as telecommunications or DSP), there is no reason to have components from multiple vendors on the same board. For a given vendor, turn-off times are guaranteed to be faster than turn-on times (^{t}KQHZ is less than ^{t}KQLZ). Banking of memory in these applications can skip the dead cycle and provide a performance improvement.

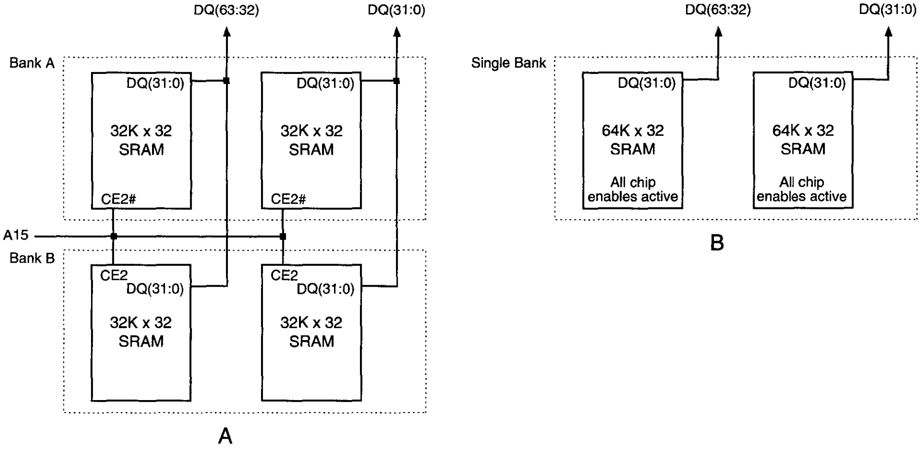


Figure 2
512KB CACHE MEMORY USING: A) FOUR 1Mb SRAMs B) TWO 2Mb SRAMs

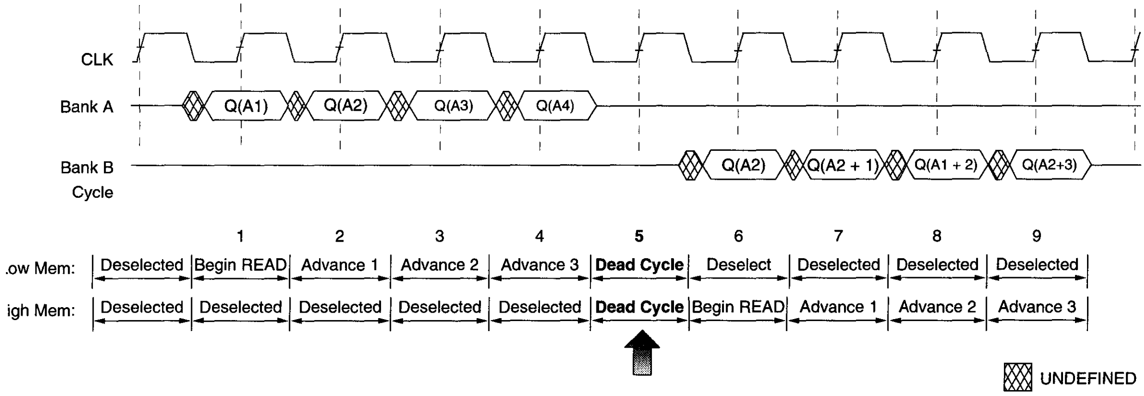


Figure 3
BANKING WITH A DEAD CYCLE

BANKING OF MEMORY IN NETWORK/ SWITCHING SYSTEMS

Many applications such as telecommunications or DSP use arrays of SRAM memory for applications. Certainly these implementations will benefit from the use of the 2Mb SRAM. In moving from 1Mb to 2Mb devices, some applications can go from two banks to one bank and simplify the system design.

However, even with a 2Mb device, some systems still have to use multiple banks of SRAMs. First, there should be no need to insert a wait state when going from bank to bank. For instance, when performing a READ in bank 0 and then a READ in bank 1, they can be done in sequential cycles. This is because the turn-off time of an SRAM is faster than the turn-on time. It is recommended that only one manufacturer's part be used in any given memory array.

Another issue of concern is that SyncBurst SRAMs may need a dummy cycle to be inserted when switching from a READ to a WRITE (see Figure 4). In this case a flow-through SRAM is used, and WRITEs are performed using an EARLY WRITE cycle. This cycle of delay can be a problem in system designs that require a READ or WRITE cycle on every clock edge. However, in some cases it can be overcome. The following example shows how using two banks of memory can allow READs and WRITEs of data to be done without any wasted cycles.

EXAMPLE: USING TWO BANKS WITH PACKET DATA

Figure 5 shows an implementation of a two-bank memory array using two flow-through SRAMs. Although this configuration uses two 64K x 32 SRAMs, any configuration of 1Mb, 2Mb or 4Mb SRAMs could be banked to arrive at a depth of 64K to 512K.

The example in Figure 5 assumes that packets of data will be stored. This scheme will work for any packet size that is in multiples of two words. It assumes that any access of information will always begin in bank 0 and end in bank 1. For simplicity, the timing here shows packets consisting of four words. Burst mode is not required in this example; therefore ADV# is wired HIGH.

Notice that an address can be given in every cycle, and that there are no unused or wasted cycles. For a flow-through device, this allows the data rate to be at the maximum available from the part (83 MHz). This is possible because a LATE WRITE cycle is used in each of the devices. Each one of these LATE WRITE cycles takes two clock cycles to complete. But since there are two banks of memory, WRITEs can be done on every cycle.

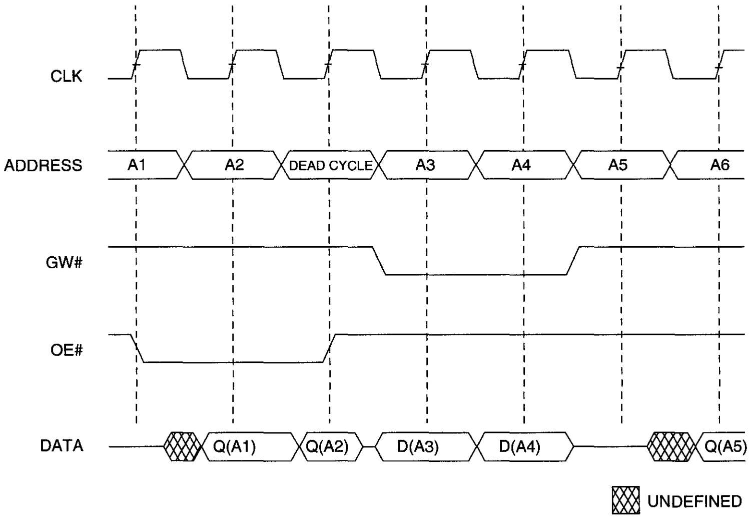


Figure 4
SYNCBURST SRAM TIMING: READ TO WRITE

CONCLUSION

The 2Mb synchronous SRAM allows both cache and noncache users to take advantage of a higher-density part. This gives the user an advantage in terms of reduced capacitance, resistance and inductance. For Pentium systems, it allows a minimum board area solution for 256KB or 512KB cache sizes. Some applications may reduce two banks of SRAM into a single bank (i.e., Pentium 512KB cache). The need for banking may still exist in some systems and a method of improving performance for packet data is presented in this article.

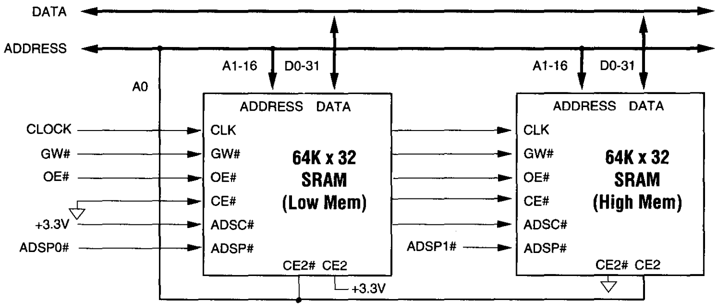


Figure 5
A TWO-BANK MEMORY ARRAY (128K x 32) USING FLOW-THROUGH SRAMs

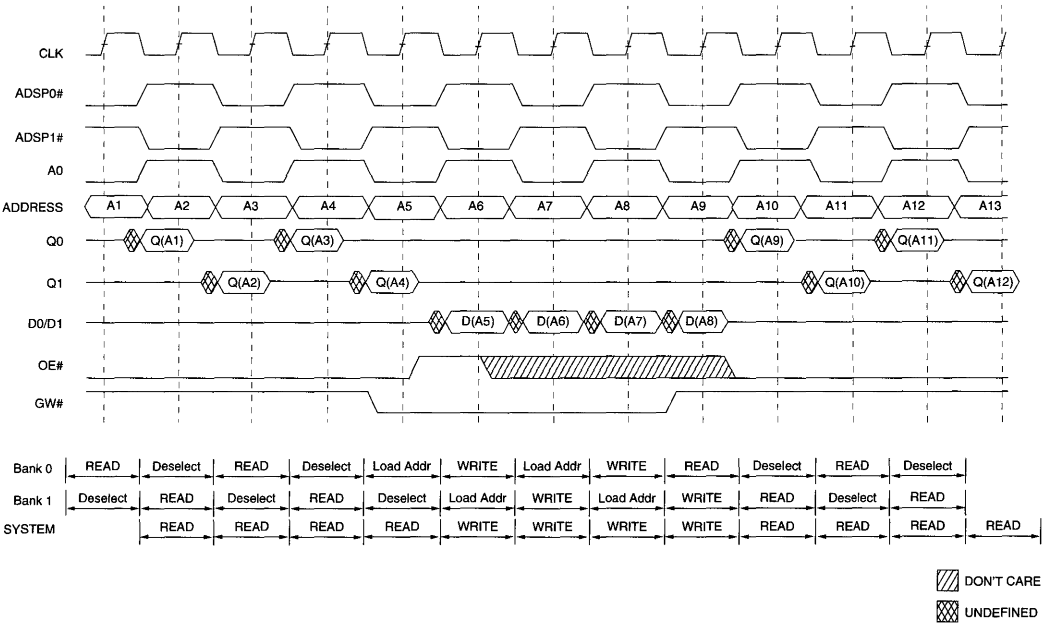


Figure 6
TIMING FOR THE TWO-BANK MEMORY ARRAY

MICRON TECHNOLOGY, INC.

TN-58-08
DESIGNING WITH 3.3V I/O SYNCHRONOUS SRAMs

TECHNICAL NOTE

DESIGNING WITH 3.3V I/O SYNCHRONOUS SRAMs

This article was originally published in 1997.

INTRODUCTION

When they first appeared, 3.3V components were used only when necessary, either when a 3.3V I/O was absolutely necessary or to save power. Now the use of lower-voltage components is widespread as the process for fabricating high-speed SRAMs and other devices has forced a move to 3.3V supplies. Many 5V components and applications are still around and will continue to be used. Consequently, this note discusses some of the considerations designers must take into account when interfacing Micron SRAMs with 5V components, or when using them in 5V systems.

REASONS FOR 3.3V LOGIC

Several issues are accelerating the use of 3.3V components in computer systems. These reasons form a powerful argument for converting new designs to 3.3V. They are listed briefly below.

When offered a choice of 5V and 3.3V components, designers pick 3.3V because (1) they represent the best longevity since processes have migrated to 3.3V, and (2) they help extend battery life or reduce the size and weight of batteries and power supplies.

Many 3.3V microprocessors (Intel®, PowerPC™, Alpha and others), microcontrollers and DSPs have appeared and have 3.3V memory busses. Although not all of them require 3.3V SRAMs, the high-power demands of these processors make lower-power (and lower-heat) 3.3V components welcome on the motherboard.

The EPA has formed the Energy Star Program to reduce power consumption in computers. The use of 3.3V components allows manufacturers to more readily meet these requirements.

Because 3.3V logic reduces power consumption, devices run cooler than their higher-voltage counterparts, and junction temperatures are reduced. Reliability is exponentially related to junction temperature, and a reduction in junction temperature increases the long-term reliability of the component.

3.3V SRAM MEMORIES

Initially, 3.3V SRAMs were recharacterized 5V products. They suffered a significant speed loss and reduced noise margins operating at 3.3V. Except for systems requiring the power savings, this generation was not widely used.

The second generation of devices was designed to operate at 3.3V and did not have the drawbacks of the recharacterized parts. They had inputs which tolerated voltages up to 5.5V (typical). This allowed them to communicate with either 3.3V or 5V devices without any buffering to ease the transition of the marketplace from 5V to 3.3V.

The third generation of devices has removed 5V-tolerance and offers 3.3V-only I/O. Although there are still applications that would benefit from a 5V-tolerant SRAM, many design engineers have added flexibility to their systems by designing them to operate with either 3.3V-only I/O or 5V-tolerant I/O. This gives them the greatest vendor choice and longevity of their products.

3.3V JEDEC STANDARDS

To ensure conformity of 3.3V interfaces among manufacturers, the JEDEC committee adopted protocol 8-1, "Interface Standard for 3.3V ±0.3V Supply Digital Integrated Circuits." The voltage requirements for this specification are shown in Table 1.

Some confusion has existed because another class of ICs operates with a wider voltage range (2.7V to 5.5V). This voltage range is used in battery-powered applications where battery life is more important than speed. These designs pay a significant speed penalty. These systems are unregulated because they can be designed without voltage regulators due to the wide voltage range.

A third voltage range exists for high-speed systems. Some microprocessors run with a higher V_{DD} (up to 3.6V) to

Table 1
JEDEC STANDARD 8-1 FOR 3.3V LOGIC

DC Operating Conditions			
Parameter	**Condition**	**MIN**	**MAX**
V_{DD}	–	3.0V	3.6V
V_{OH}	-2mA	2.4V	–
V_{OL}	2mA	–	0.4V
V_{IH}	–	2.0V	V_{DD} + 0.3V
V_{IL}	–	-0.3V	0.8V
Absolute Maximum Conditions			
V_{DD}	–	-0.5V	4.6V
V_{IN}	–	-0.5V	V_{DD} + 0.5V (4.6V MAX)

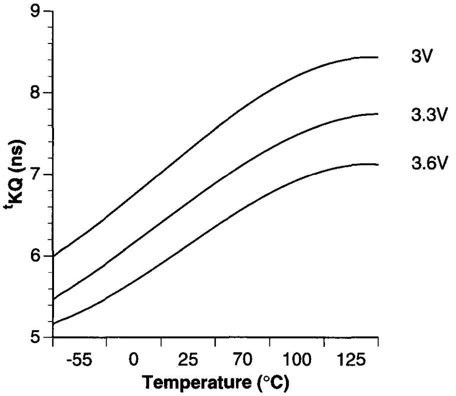


Figure 1
ACCESS TIME vs. TEMPERATURE AND VOLTAGE

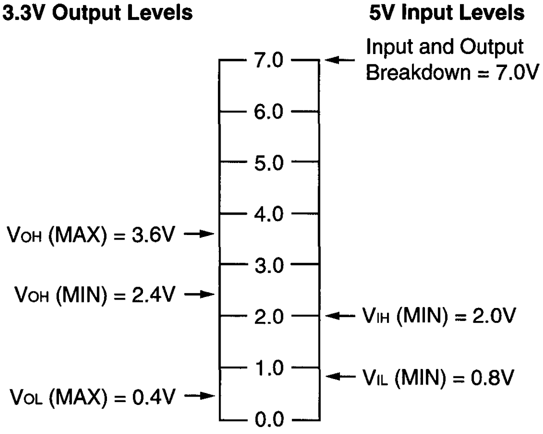


Figure 2
3.3V DEVICES DRIVING 5V LOGIC

eke out more performance. The voltage supply of the microprocessor is shared with the cache memory and the SRAM can benefit from the increased timing margins due to only a five percent variance.

Micron® SRAMs can operate in systems that are 3.3V +5%/-5%, or with microprocessors (such as Intel's V_{RE} products) that operate at 3.3V +10%/+5% VDD. This is because Micron SyncBurst™ SRAMs run at 3.3V +10%/-5%.

Figure 1 shows how access time varies versus temperature and voltages for the 3.3V 1Mb SyncBurst SRAM. For the part shown here, the increase in low-end VDD increases the speed of the part. By increasing the low-end voltage to the SRAM, timing margins or performance can be improved.

3.3V SRAMS DRIVING 5V COMPONENTS

3.3V SRAMs can drive 5V TTL inputs directly. However, this can be done only if 3.3V levels are driven on the bus and VDD + 0.3V is not exceeded. Figure 2 shows how 3.3V output logic levels can be used to drive 5V TTL levels. These logic levels guarantee a minimum noise margin of 400mV when driving HIGH or LOW output levels (typical values provide more margin). 5V device inputs require a maximum VIL of 0.8V, and 3.3V devices supply less than 0.4V. Similarly, inputs require a minimum VIH of 2.0V and are supplied with 2.4V or greater.

There is some concern that 3.3V parts driving 5V inputs will cause a slightly higher power dissipation because the inputs are not driven to a full voltage rail. Because most 5V TTL memories do not drive to full voltage rails, 3.3V components have similar power dissipation driving 5V inputs.

3.3V outputs can drive 5V TTL circuits, but they should not be used to directly drive 5V CMOS level inputs on true CMOS devices. To reach VIH (MIN), 5V CMOS devices with CMOS thresholds require a greater logic-HIGH input voltage than can be supplied by 3.3V devices. Designs requiring 5V CMOS levels need a voltage translation, buffer circuit or pull-up device. This restriction of driving 5V CMOS inputs is also present on 5V TTL outputs.

Some manufacturers specify an absolute maximum input HIGH of VDD + 0.5V on their 3.3V products. This limitation is critical when the outputs are connected to a bus with 5V drivers. Although 3.3V devices can drive 5V inputs, the 5V bus may overdrive the maximum allowable voltage during High-Z. Outputs exceeding the maximum voltage require buffering to prevent damage to the SRAM. This buffering may be a current limiting resistor for 3.3V components that would have excessive current through a clamping diode or a register latch buffer for devices that suffer from latchup problem when overdriven.

To enable the transition to 3.3V, Micron initially produced 5V-tolerant devices that handled input voltages up to 6V. As mentioned earlier, 5V-tolerant devices have been discontinued in lieu of 3.3V-only I/O. For the greatest flexibility and largest vendor base, it is recommended that designs use 3.3V-only I/O components.

5V COMPONENTS DRIVING 3.3V SRAMs

JEDEC standard 8-1 specifies that 3.3V input voltages can range from -0.5V to VDD + 0.5V (4.6V [MAX]). This range was reduced by JEDEC from the 1984 standard, which had a maximum input voltage of 5.5V, allowing 5V devices to directly drive 3.3V inputs. JEDEC modified the standard because the transition period to 3.3V was much shorter than originally envisioned.

Designers must be careful when considering 3.3V components because many SRAMs (including Micron's) have a +4.6V MAX (V_{IN}) specification. Driving these 3.3V components with 5V parts will exceed V_{IN} (MAX) and could cause a latchup failure. Mismatched impedances worsen the problem since ringing will occur and drive the voltages higher than their steady-state values. A number of companies including IDT, National Semiconductor, Texas Instruments and Toshiba offer buffering/transceiver components specifically designed to address the buffering issues encountered in mixed-voltage systems. Figures 3 and 4 show how to connect circuits and how the voltage levels interact when 5V components drive 3.3V circuits.

POWER-UP DESIGN CONSIDERATIONS

Mixed-voltage designers need to be especially careful during the power-up and power-down sequence to ensure that 5V parts do not violate the input specifications of 3.3V parts. For instance, the Alpha processor can tolerate direct 5V inputs, according to the *Hardware Reference Manual,* but no input or bidirectional pin can rise above 4V until the 3.3V supply is stable. Failure to meet this rule can cause damage to the Alpha. This is because a 5V part could drive an input to a 3.3V part with a V_{DD} of 0V, exceeding breakdown voltages and permanently damaging the device.

Three solutions are available to minimize problems during power-up and power-down in mixed-voltage systems. The first is to use power supply sequencing to ensure that the 3.3V power supply is stable before any 5V signals are applied. The second is to use tristate outputs to drive 3.3V logic, and ensure that all inputs remain in tristate until the 3.3V supply is stable. Power supply designs that sample the 3.3V power supply and generate a tristate signal based on it offer the safest design approach because the tristate will be removed only when power is stable.

The third solution is to use a 3.3V product with 5V tolerance. Because many manufacturers do not have 5V-tolerant products, it is recommended that the designer plan for 3.3V I/O only.

POWER SUPPLY CONSIDERATIONS

Power supply manufacturers are developing a wide array of products simplifying mixed-voltage designs and power-up considerations. Power supply chips that supply multiple output voltages are now available, such as Maxim's MAX782 supply. These chips can be used to generate the voltage supplies of mixed-voltage systems and support power supply sequencing per the designer's specifications.

Some designers haven't considered lower-voltage parts because a 3.3V supply is unavailable. Some expansion slots in computers only have a 5V supply, and 3.3V has to be generated on the card. A 3.3V supply can easily be gener-

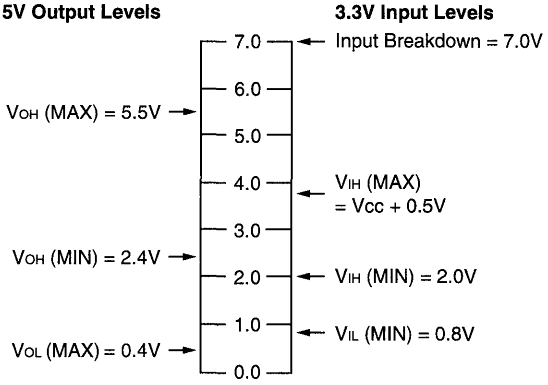


Figure 3
5V DEVICES DRIVING 3.3V LOGIC

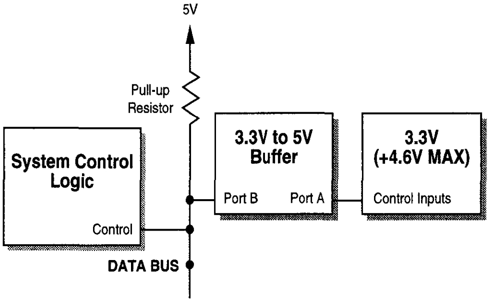


Figure 4
5V DEVICES DRIVING 3.3V LOGIC

ated with a voltage regulator as shown in Figure 5. Regulators are inexpensive and take up minimal area (typically < 0.4in^2). The additional power drawn by the regulator is insignificant given the power savings of the 3.3V components.

OVERSHOOT/UNDERSHOOT CONCERNS

One last concern with 3.3V-only I/O is tolerance to undershoot and overshoot. With a 5V-tolerant part, overshoot could be handled up to 6V and undershoot around -2V. Usually most designs would fall well within this range.

With 3.3V-only I/O it is more important to understand the overshoot/undershoot in a system. This is because the tolerance to overshoot is +4.6V, and -0.7V for undershoot. Some designs may fall outside this range and should be carefully checked to be sure that an impedence mismatch does not cause ringing to fall outside this range.

CONCLUSION

3.3V microprocessors, memories and other components are forcing designs to quickly move to 3.3V. Synchronous SRAMs are ideal for these systems, offering high density with small board area. Designers of mixed-voltage systems must look carefully at manufacturers' specifications to determine if external buffering is required and how to gain maximum power savings from the devices. Micron 3.3V SRAMs are an excellent choice for 3.3V systems because they have been designed to minimize design difficulties.

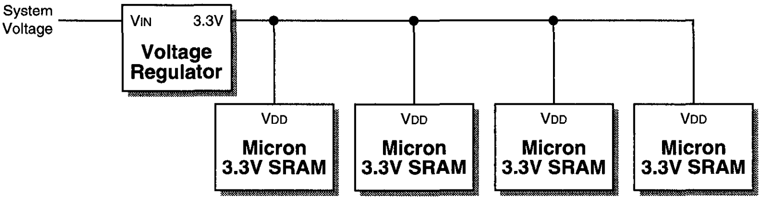


Figure 5
GENERATING 3.3V IN A 5V SYSTEM OR PERIPHERAL

TECHNICAL NOTE

SYNCHRONOUS SRAM BUS CONTENTION DESIGN CONSIDERATIONS

This article was originally published in 1997.

INTRODUCTION

High-speed SRAM memory systems may share a common data bus with other memory devices, processors and memory management or caching devices. As cache applica-ions require more memory, two or more banks of SRAM may be used in a system. All of these devices are required o control the data bus at one time or another. Turning off a device that is driving the bus before a new device takes control of the bus can be a difficult design problem when hese systems are operating at minimum cycle times.

When two or more devices are driving the bus at the same ime, a conflict known as "bus contention" occurs. This echnical note discusses bus contention design issues and points out design features of Micron's fast SRAMs that help minimize bus contention problems.

BUS CONTENTION EFFECTS

System design problems caused by bus contention are difficult to analyze. The effects are transient, normally not longer than 5ns. The most visible result of bus contention is observed as noise on power-supply lines and data lines connecting the contending devices. While these conflicts are not destructive, they potentially reduce long-term system reliability. To ensure long-term reliability, the system should be designed to eliminate any possibility of bus contention.

Figure 2 is a schematic diagram of two contending SRAM output buffers. A high current path has been created by two SRAM output buffers. The current is flowing between the "on" transistor connected to VDD in the buffer on the left and the transistor connected to ground in the buffer on the right.

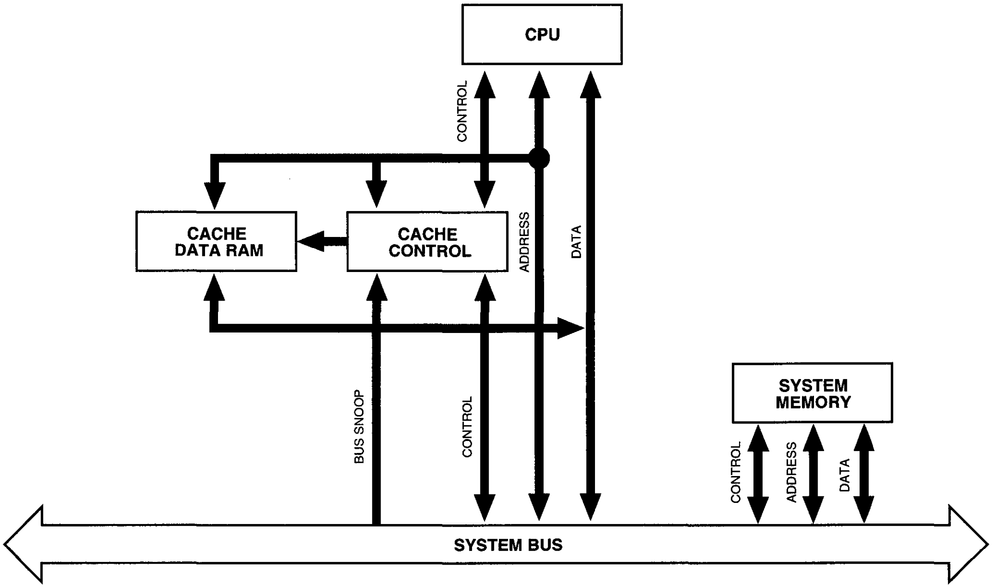


Figure 1
BLOCK DIAGRAM OF A CACHE MEMORY SYSTEM

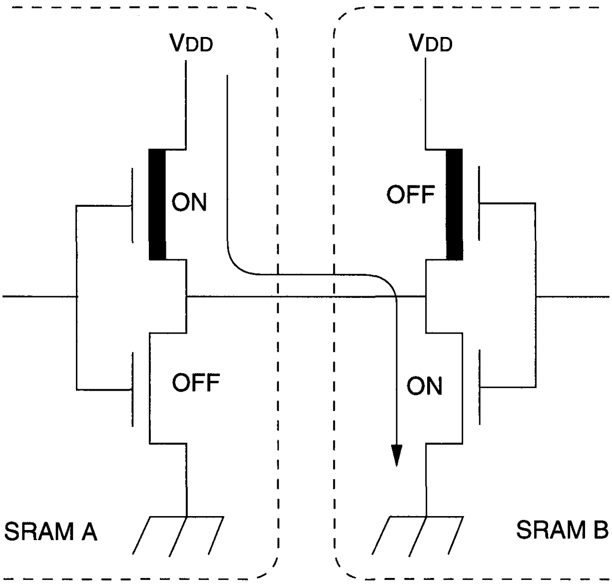


Figure 2
BUS CONTENTION CURRENT PATH

SRAM SPECIFICATIONS

This section deals primarily with bus contention between two or more banks of SRAMs. This same analysis can be used with SRAM bus contention with another device and substituting the turn-on/turn-off times of that device into the equation.

The critical parameter for calculating the amount of bus contention for a high-speed SRAM system design is the time it takes for a device to go to low impedance (logic 1 or 0) on its output versus the time required for a contending output to go to high impedance. The output of a synchronous SRAM will usually turn on/off relative to a clock edge (^{t}KQLZ, ^{t}KQHZ). A READ timing diagram (Figure 3) shows both these timing parameters. A preliminary review of a fast synchronous SRAM data sheet would imply that the worst case for bus contention could be calculated from the equation:

$$^{t}\text{CONTENTION} = \text{turn-off time} - \text{turn-on time}$$
$$= {}^{t}\text{KQHZ} - {}^{t}\text{KQLZ}$$

^{t}CONTENTION is equal to the bus-contention overlap time. For a synchronous flow-through SRAM with an access time of 8.5ns, ^{t}KQHZ = 5ns and ^{t}KQLZ = 4ns; therefore ^{t}CONTENTION = 1ns. If this calculation is correct, there would be a bus contention problem. Thus, for a system running with a 12ns cycle, about 8 percent of the total cycle would be lost to bus contention and there would be an increase in power dissipation in the output buffers.

Fortunately, the previous analysis is not valid because ^{t}KQHZ is a MAX parameter and ^{t}KQLZ is a MIN parameter. ^{t}KQHZ maximum occurs under completely different tes conditions than ^{t}KQLZ. ^{t}KQHZ maximum is worst-case a the highest operating temperature and the lowest power-supply voltage (70°C and 3.135V). ^{t}KQLZ is worst-case a the lowest operating temperature and the highest voltage (0°C and 3.6V). It is not possible for two SRAMs on the same board to be at such diverse temperatures and voltages.

Micron® Synchronous SRAMs are designed to be operated in systems requiring two or more banks of SRAM memory without bus contention problems. Tests run on these devices by Micron show that the user need not be concerned abou bus contention between turn-on and turn-off times as long as both banks are enabled/disabled at the same time. Since multiple banks of SRAM are normally mounted on the same board (so that temperature and voltage are similar), bus contention problems are eliminated.

Care must be taken when multiple vendors' SRAMs share the bus. An analysis of the output turn-off time mus e done under the same operating and temperature onditions to ensure that bus contention between the evices is minimized. Because of this, it is strongly ecommended that users do not mix SRAMs from multiple endors on the same board. A design that has eight SRAMs n a board should have eight parts from vendor A or eight arts from vendor B. It should not have four parts from endor A and four parts from vendor B.

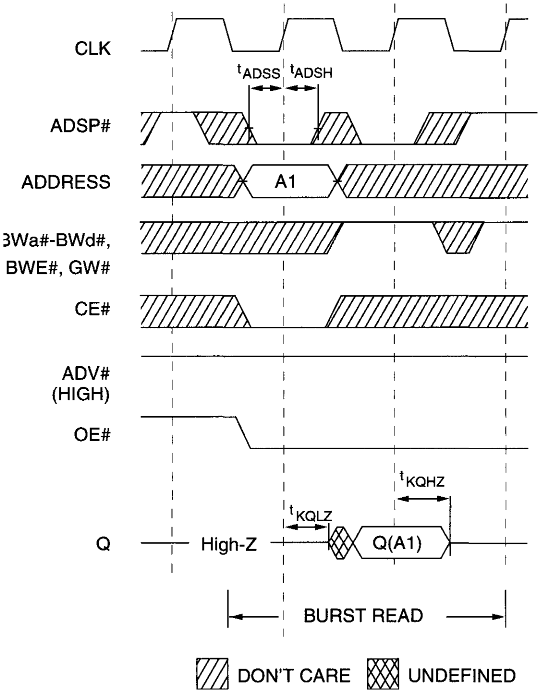


Figure 3
A READ TIMING DIAGRAM FOR A FLOW-THROUGH SYNCBURST SRAM (ADSC# IS HIGH)

SYNCBURST™ SRAM EXAMPLE

As an example, consider a two-bank system using pipelined SyncBurst SRAMs running at 133 MHz. In this system banking will be done with zero wait states so that one bank will be turning on while the other is turning off. What is the actual amount (if any) of bus contention? That depends on the product family. For instance, the current generation of pipelined 2Mb SyncBurst SRAM (C6, D9) will have different amounts of bus contention depending upon several parameters including temperature and VDD voltage. Best case, there will be no bus contention whatsoever. Worst case, there will be around 100ps of contention. These cases assume no clock skew. If 100ps of clock skew existed, it could make the bus contention extend out to 200ps.

What does this amount of contention actually mean? If we assume approximately 30 ohm pull-up impedance and 30 ohm pull-down impedance, a 60 ohm path will exist from VDD to GND for 200ps. In actuality, this is worst case because the impedances of both bank drivers are changing during the turn-on and turn-off period and the resistance will not be 60 ohms during the whole cycle. For a 3.3V VDD, this means 55mA of current for the 200ps period. If the devices cycle at 133 MHz, and you were doing READs and switching banks every cycle, this means 0.2ns of bus contention every 7.5ns. In other words, 2.7 percent of the time you would have bus contention. Of course, you would not be switching banks every cycle and probably not reading every cycle so again this is a worst-case calculation. If on average 50 percent of the I/O has bus contention, this would increase the power by 87mW. With a thermal impedance of 25°C/W the junction temperature would only rise 2.18°C. The junction temperature rise is very minimal and banking under these conditions is acceptable.

TECHNICAL NOTE

USING PARITY SRAMs IN NONPARITY APPLICATIONS

his article was originally published in 1997.

NTRODUCTION

Numerous applications require nonparity synchronous RAMs (x16 or x32). It is recommended, however, that esigns for x16 or x32 SRAM applications be capable of sing either nonparity or parity SRAMs. Flexibility in the esign can increase component availability (i.e., a x16 appli-ation could use either a x16 or x18 SRAM).

ARITY vs. NONPARITY SRAMS

Micron offers parity SRAMs (x18 and x36) which allow arity checking to be done in x16, x32 or wider systems. The arity check must be performed external to the SRAMs. The arity bits act identically to nonparity or data bits. No pecial circuitry is added or associated with the parity bits.

ESISTORS

It is recommended that the parity pins not be left floating unused. Floating pins can increase the power dissipation f the device during WRITE cycles.

Figures 1 and 2 show the recommended connection of the parity pins to GND. Note that these pins could be connected to VDD (3.3V) instead. Although a 1KΩ resistor is shown in the diagram, other values can be used. The recommended range of resistance is 1KΩ to 10KΩ.

Choosing a resistor closer to 1KΩ provides a lower impedance to the power plane and makes the pin less susceptible to noise. The 1KΩ resistor is the preferred value because the power difference between 1KΩ and 10KΩ only occurs until the entire memory array is written. The resistors dissipate power if the parity bit read out is HIGH and the resistor is connected to GND. As the memory array gets written with data (GND), this contention goes away.

A separate resistor is recommended for each parity pin (DQP). The SRAM powers up with the memory array set in a random state. If all parity pins are connected to a single resistor, bus contention may initially occur during READ cycles until all of the address locations are written. Separate resistors alleviate this problem.

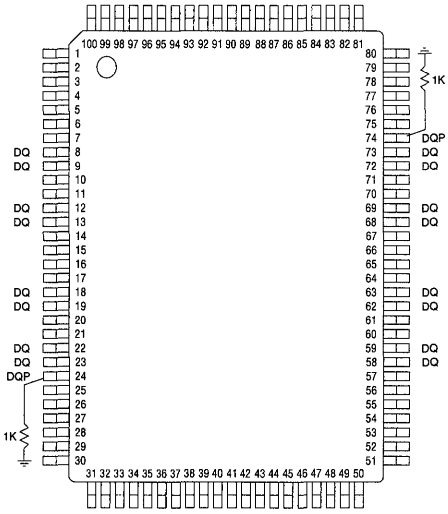


Figure 1
USING A x18 SRAM IN A x16 APPLICATION

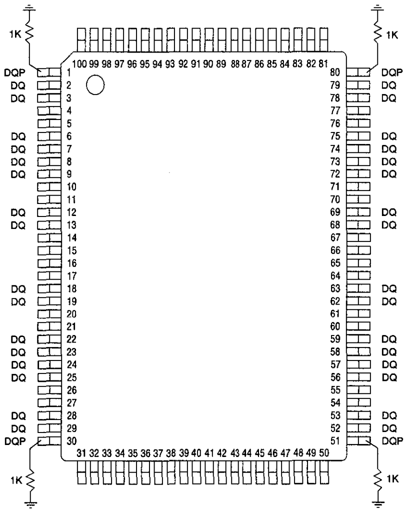


Figure 2
USING A x36 SRAM IN A x32 APPLICATION

TECHNICAL NOTE

USING SYNCBURST™ SRAMs WITH THE TI C6x DSP FAMILY

This article was originally published in 1998.

INTRODUCTION

Texas Instruments has developed the TMS320C6x digital signal processor (DSP) family for use in high-speed data and telecommunications processing areas. A high-speed synchronous SRAM interface is used with this device in order to feed the DSP data at a very high rate. This article discusses the synchronous SRAM interface and how to design for its use with Micron® SyncBurst™ SRAMs.

APPLICATIONS

Users of the C6x family will be interested in an extremely high-performance DSP. TI publications indicate that applications for this processor will include wireless base stations, pooled modems, digital subscriber loop (xDSL) systems, high-performance telephony, multimedia systems and multi-peripheral applications, among others.

EXTERNAL MEMORY INTERFACE (EMIF)

The TMS320C6201 is the first product in this family. The 6201 is designed for use with synchronous DRAM, asynchronous SRAM or SyncBurst SRAM. Because it can operate at high frequencies, the SyncBurst SRAM is able to feed information to the DSP at the highest bandwidths for ncreased performance.

TI has developed two revisions of the 6201 DSP, Revision and Revision 2, with different interfaces to the SRAM. This article discusses how to connect to the SRAM using these revisions.

TI has implemented an external memory interface (EMIF) o interface with the SRAM. In Revision 1, three memory paces are available, each with a dedicated chip enable CEn#) signal (Table 1a). The SyncBurst SRAM can only be connected to the memory spaces controlled by CE0# and CE2#.

Revision 2 has an additional CEn# signal, for a total of four memory spaces. Any of these memory spaces can control the SyncBurst SRAM (Table 1b).

Figure 1 shows the connection between the TI DSP and the SyncBurst SRAM. In Revision 1, either CE0# or CE2# is connected to the CE# input of the SRAM because only these memory spaces support SyncBurst. Because the processor is designed to work with SyncBurst SRAM memory, the memory interface is simply a point-to-point connection of several signals. In Revision 2, any of the chip enables can be connected to the SRAM.

The SyncBurst SRAM has three chip enables: CE#, CE1 and CE2#. Only CE# should be connected to the processor. The other two chip enables should be connected active because they are unnecessary in this application.

The two versions of the DSP also differ in the way they burst words. Revision 1 has an SSADV# signal that is connected to the ADV# input of the SRAM (Figure 1). The processor can burst words, and the ADV# is used to make the SRAM increment its own internal address counter up to burst lengths of four words.

Revision 2 eliminates the SSADV# signal. The ADV# input on the SRAM is connected inactive (VDD) because it is unused. In Revision 2, the processor generates the address signals as quickly as needed, so the SSADV# signal is no longer necessary.

CLOCK RATE (1x vs. 1/2x)

Revision 2 of the 6201 is designed to operate with one of two different clock rates for the SyncBurst SRAM. For fastest operation, the clock can be set to run at the same rate as the CPU clock (1x). This means that if the CPU is operat-

Table 1a
TYPES OF MEMORY SUPPORTED BY C6201, REVISION 1

MEMORY SPACE	TYPES OF MEMORY SUPPORTED
CE0#, CE2#	Asynchronous, Synchronous SRAM/DRAM
CE1#	Asynchronous SRAM Only

Table 1b
TYPES OF MEMORY SUPPORTED BY C6201, REVISION 2

MEMORY SPACE	TYPES OF MEMORY SUPPORTED
CE0#, CE1#, CE2#, CE3#	Asynchronous, Synchronous SRAM/DRAM

ing at 200 MHz, it expects to have a SyncBurst SRAM memory operating at the same frequency.

The other mode of operation is 1/2x mode. In this mode, the SyncBurst SRAM operates at half the processor frequency. In the above example, the processor would expect a 100 MHz SyncBurst memory. In Revision 1, only a 1x clock is implemented.

The DSP is programmed for the clock mode through the EMIF global control register. The SSCRT field allows the SyncBurst SRAM clock rate to be selected. If this bit is set to 0, the SSCLK operates at 1/2x the CPU clock rate. If set to 1, the SSCLK operates at 1x the CPU clock rate.

HIGH-FREQUENCY OPERATION BALL GRID ARRAY (BGA)

For the highest clock frequency operation, Micron will offer the SyncBurst SRAM in BGA packages. Until recently, the SyncBurst SRAM package of choice was the TQFP. TQFP is excellent for frequencies up to 150 MHz. Above 150 MHz, however, BGA is superior because it provides less inductance on the I/O and improved thermal performance. For higher bus frequencies, the BGA package is recommended.

WHAT TYPES OF SRAM TO USE?

The Synchronous SRAM interface (referred to as the SBSRAM in TI literature) uses pipelined, single-cycle deselect (SCD) SyncBurst SRAMs manufactured by Micron. The Micron D8/D9 series of SyncBurst SRAMs is recommended for use in the 6201.

Micron produces two different densities of SyncBurst SRAM. The 2Mb and 4Mb parts are excellent choices for use with the TI DSP processor. An 8Mb part is in development and will provide even greater memory density.

FOR MORE INFORMATION

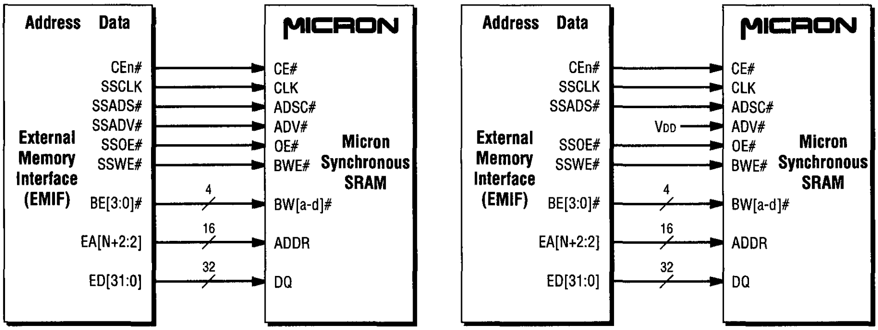
More information on the TI C6X families is available on TI's DSP home page: www.ti.com/sc/docs/dsps/dsphome.htm. Two documents in particular describe the SRAM/DSP interface in more detail: TMX320C6201 data sheet, TMS320C62XX PERIPHERALS REFERENCE GUIDE.

NEXT GENERATION: TMS320C67X

In 1997, TI announced a new generation of the C6 family called the C67. This DSP processor core, unlike the 6201, includes floating-point capabilities. No specific products using the C67 core have been announced at the time of printing this article. The C67 core is code compatible with the 6201, and it is anticipated that C67 products will use a memory interface similar, if not identical, to the memory interface of the 6201. SyncBurst SRAMs are likely to play a role in the C6x family for some time to come.

CONCLUSION

The new family of C6x DSPs from TI represents improved performance over past generations of DSPs. TI attains this level of performance by using synchronous DRAMs and SRAMs to eliminate the memory bottleneck at high frequencies. Micron SyncBurst SRAMs and Synchronous DRAMs are an optimal choice for memory implementation with this processor.



6201, Revision 1 **6201, Revision 2**

Figure 1
SIGNAL CONNECTION BETWEEN 6201 AND MICRON 64K x 32 SYNCBURST SRAM

TECHNICAL NOTE

SRAMs FOR THE POWERPC 750 ARTHUR PROCESSOR

This article was originally published in 1998.

INTRODUCTION

The PowerPC 750 Arthur processor is used primarily in high-speed, performance-oriented embedded applications such as telecom, networking, disk array (RAID) and VME-based systems. Because of the performance requirement of these applications, most use SRAM cache memory to boost the performance of the processor.

CACHE MEMORY SOLUTIONS

To obtain the highest level of cache performance possible, Arthur was designed to use cache memory with a backside Level-2 or L2 bus. Only the cache is connected on this bus so the processor can take full advantage of the high bandwidth of the SRAM. Because the processor has an on-chip, two-way set associative tag memory, no external tag is required.

Table 1
TWO-CHIP FLOW-THROUGH SYNCBURST CACHE SOLUTION[1]

CACHE SIZE	RECOMMENDED SRAM		PROCESSOR ADD. PINS
	PARITY	NONPARITY	
256KB	MT58LC32K36B3LG	MT58LC32K32B3LG	14:0
512KB	MT58LC64K36B4LG	MT58LC64K32B4LG	15:0
1MB	MT58LC128K36B4LG MT58LC128K36B4BG	MT58LC128K32B4LG MT58LC128K32B4B	16:0

Table 2
TWO-CHIP PIPELINED SYNCBURST CACHE SOLUTION[1]

CACHE SIZE	RECOMMENDED SRAM		PROCESSOR ADD. PINS
	PARITY	NONPARITY	
256KB	MT58LC32K36D8LG	MT58LC32K32D8LG	14:0
512KB	MT58LC64K36D9LG	MT58LC64K32D9LG	15:0
1MB	MT58LC128K36D9LG MT58LC128K36D9BG	MT58LC128K32D9LG MT58LC128K32D9B	16:0

NOTE: 1. LG = TQFP package, B = BGA package.

Three cache sizes are possible: 256KB, 512KB and 1MB. Although the Arthur cache bus can handle up to four bus loads, Micron's parts allow cache to be implemented with only two loads. The recommended Micron part number is shown in Tables 1-2.

Flow-through and pipelined SyncBurst™ SRAMs can be used with the Arthur processor. SyncBurst chips are available in both parity and nonparity versions.

Figure 1 and Table 3 show how the SRAM memory should be connected to the processor. The processor does not use all the features of the SyncBurst SRAM (such as BURST READ/WRITE or BYTE WRITE operations), and consequently a number of control pins will not be toggled.

Note also that routing of the address and data can be optimized since the processor only performs 64-bit READs and WRITEs. For example, data bit LDDATA[7] can be wired to any DQ pin of either SRAM. This flexibility allows a signal router to optimize for the shortest board traces.

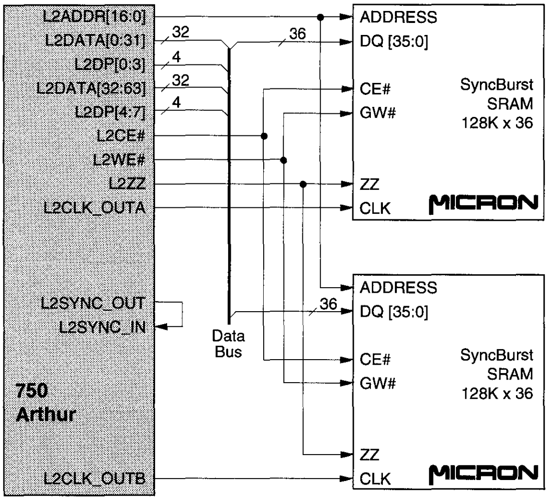


Figure 1
CONNECTING SYNCBURST SRAMs TO ARTHUR

Table 3a
CONNECTING THE 750 TO THE SYNCBURST SRAM[1]

750 PROCESSOR		SYNCBURST SRAM (TQFP)		SYNCBURST SRAM (BGA) 1MB CACHE ONLY	
PIN NUMBER	**NAME**	**PIN NUMBER**	**NAME**	**PIN NUMBER**	**NAME**
G18, H17, H18, H19, J13, J14, J16 J17, J18, J19, K15, K17, K18, L17 L18, L19, M19	L2ADDR[16:0]	50 (1MB cache only) 49 (512KB and 1MB cache only) 32, 33, 34, 35, 36, 37, 44 45, 46, 47, 48, 81, 82, 99 100	ADDR[16:0]	2A, 2C, 2R, 3A, 3B, 3C, 3T 4N, 4P, 4T, 5A, 5B, 5C, 5T 6A, 6C, 6R	ADDR[16:0]
A14, A15, A16, A17, A18, B14, B16 B17, B18, B19, C14, C15, C16, C17 C18, D17, D18, D19, E13, E15, E17 E18, E19, F13, F18, F19, G13, G14 G15, G16, G19, H13, M13, M17 M18, N13, N14, N17, N19, P13 P18, P19, R13, R15, R17, R18, R19 T17, T18, U14, U15, U17, U18, U19 V15, V16, V17, V18, V19, W14, W15 W16, W17, W18	L2DATA[0:63]	2, 3, 6, 7, 8, 9, 12, 13, 18 19, 22, 23, 24, 25, 28, 29 52, 53, 56, 57, 58, 59, 62 63, 68, 69, 72, 73, 74, 75 78, 79	DQ[31:0] Chip #2	1D, 1E, 1G, 1H, 1K, 1L, 1N 1P, 2E, 2F, 2G, 2H, 2K, 2L 2M, 2N, 6K, 6L, 6M, 6N, 6E 6F, 6G, 6H, 7D, 7E, 7G, 7H 7K, 7L, 7N, 7P	DQ[31:0] Chip #2
		1, 30, 51, 80	DQ[35:32] Chip #2	6P, 6D, 2D, 2P	DQ[35:32] Chip #2
		2, 3, 6, 7, 8, 9, 12, 13, 18 19, 22, 23, 24, 25, 28, 29 52, 53, 56, 57, 58, 59, 62 63, 68, 69, 72, 73, 74, 75 78, 79	DQ[31:0] Chip #1	1D, 1E, 1G, 1H, 1K, 1L, 1N 1P, 2E, 2F, 2G, 2H, 2K, 2L 2M, 2N, 6K, 6L, 6M, 6N, 6E 6F, 6G, 6H, 7D, 7E, 7G, 7H 7K, 7L, 7N, 7P	DQ[31:0] Chip #1
B15, C19, F17, H14, N18, T19 U16, V14	L2DP[0:7]	1, 30, 51, 80	DQ[35:32] Chip #1	6P, 6D, 2D, 2P	DQ[35:32] Chip #1
P17	L2CE#	98	CE#	4E	CE#
N16	L2WE#	88	GW#	4H	GW#
G17	L2ZZ (optional)	64	ZZ	7T	ZZ
N15	L2CLK_OUTA	89	CLK Chip #1	4K	CLK Chip #1
L16	L2CLK_OUTB	89	CLK Chip #2	4K	CLK Chip #2

Table 3b
SYNCBURST SRAM CONTROL PINS NOT CONNECTED TO PROCESSOR

	SYNCBURST SRAM (TQFP)		SYNCBURST SRAM (BGA) 1MB CACHE ONLY	
SRAM CONNECTS TO:	**PIN NUMBER**	**NAME**	**PIN NUMBER**	**NAME**
VDD	87	BWE#	4M	BWE#
	93, 94, 95, 96	BWa-d#	3G, 3L, 5G, 5L	BWa-d#
	84	ADSP#	4A	ADSP#
	97	CE2	2B	CE2
	83	ADV#	4G	ADV#
GND	85	ADSC#	4B	ADSC#
	92	CE2#	6B	CE2#
	86	OE#	4F	OE#
VDD or GND	31	MODE	3R	MODE

NOTE: 1. The pinout and data sheet information used throughout this paper for the Arthur/PowerPC 750 was obtained from the 1/98 Rev 1.0 version of the PowerPC 740 and PowerPC 750 SCM RISC Microprocessor: Hardware Specifications, copyright IBM Corporation, 1997. This is advance information and is subject to change.

CHOOSING THE RIGHT SRAM FUNCTIONALITY

Users of the Arthur PowerPC will need to choose an SRAM memory that is appropriate for their application. Table 4 shows the number of cycles required by the cache memory for certain operations.

Figure 2 compares the available frequencies for each of the devices. Until recently, the flow-through SRAM was only available with frequencies up to 83 MHz. Flow-through is now an excellent choice for bus speeds running up to 125 MHz. Note from Table 4 that the flow-through requires the same number of cycles as the pipelined SRAM to perform operations. However, the data arrives at the processor one cycle earlier. This means that the processor can operate on that data much quicker.

SPEED GRADE

Determining the speed grade of the SRAM required begins with the clock frequency of the cache bus. In this example, assume a processor running with a 275 MHz core frequency with an SRAM frequency of 138 MHz. Pipelined SyncBurst SRAMs are used in this example.

At a 138 MHz clock frequency, the clock cycle time is 7.2ns. A designer must analyze the processor input and output timing specifications for the L2 cache. During a READ from the SRAM to the processor, the processor requires a 2ns setup time, leaving 5.2ns for the SRAM to drive the data from the rising edge of the clock. A -6.6 speed grade will be required to meet the 138 MHz frequency. This speed grade has an access time of 3.8ns, leaving 1.4ns left for flight time as shown in Equation 1. A similar analysis can be performed to ensure that the SRAM will meet the data and parity input hold time.

tmargin = tclk - tsetup - taccess
tmargin = 7.2 - 2 - 3.8
tmargin = 1.4ns

EQUATION 1

Table 4
CACHE CYCLES REQUIRED TO PERFORM VARIOUS OPERATIONS

OPERATIONS PERFORMED	FLOW-THROUGH SYNCBURST	PIPELINED SYNCBURST
Burst of 4 READ-WRITE-READ	18	18
Burst of 4 READ-MODIFY-WRITE	19	19
Burst of 4 READ-WRITE-WRITE	19	19

For WRITE operations to the cache memory, it is also necessary to determine if the setup and hold times of the data and control signals are met at the SRAM. The setup time of the -6.6 speed grade SRAM is 1.7ns and the access time of the processor is 4.5ns, leaving 1ns for flight time as shown in Equation 2. A similar analysis can be applied to the hold time of the SRAM.

tmargin = tclk - tsetup - taccess
tmargin = 7.2 - 1.7 - 4.5
tmargin = 1ns

EQUATION 2

This analysis is valid no matter which type of SRAM (pipelined or flow-through SyncBurst) is used. Note that the processor can be set to have an output hold time of 0.5ns.

CONFIGURING THE CACHE CONTROL REGISTER

The cache memory must be configured correctly by setting the cache control register inside the processor as shown in Table 5. Numerous cache attributes are controlled by this register, including the cache bus frequency, output hold time to cache memory, snooze mode, etc. During power-up, the contents of the L2CR register are cleared so that unless the operating system enables the cache through the L2CR register, the cache is not activated.

The SyncBurst SRAM uses a single-ended clock. In order for Arthur to generate the correct type of clock signal, the cache control register must be programmed properly.

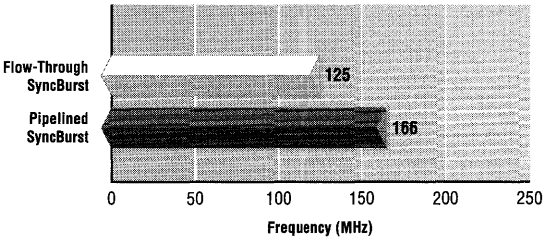


Figure 2
SPEEDS OF SRAM MEMORIES

Table 5
32-BIT L2 CACHE CONTROL REGISTER INTERNAL TO ARTHUR

BIT	NAME	DESCRIPTION
0	L2E	L2 Enable. Set this bit to one when using cache. This bit cannot be active until the L2 clock is configured (through L2CR[2CLK]) and the L2 DLL is stabilized.
1	L2PE	Parity Generation and Checking Enable. Enable this bit if the L2 cache has parity bits and parity is desired; otherwise disable.
2-3	L2SIZ	L2 Size. Set these bits based upon the size of the L2 cache. 00 RESERVED (Do not use) 01 256KB cache (32K x 64 or 32K x 72) 02 512KB cache (64K x 64 or 64K x 72) 03 1MB cache (128K x 64 or 128K x 72)
4-6	L2CLK	L2 Clock Ratio (core clock to L2 clock frequency divider). When cleared (set to 000), the L2 clock is stopped and the on-chip DLL for the L2 interface is disabled. When setting to a non-zero value, the L2 clock is active and the on-chip DLL is enabled. For instance, if the processor operates at 200 MHz and the L2CLK is set at '100', the cache frequency is 100 MHz. 000 L2 clock and DLL disabled 001 Divide by 1 010 Divide by 1.5 011 RESERVED 100 Divide by 2 101 Divide by 2.5 110 Divide by 3 111 RESERVED
7-8	L2RAM	L2 RAM Type. Chooses the type of SRAM memory used for L2 cache. 00 Flow-through (register-buffer) SyncBurst SRAM 01 RESERVED 10 Pipelined (register-register) SyncBurst SRAM
9	L2DO	L2 Data Only. The L2 cache can be used for caching both instructions and data. If this bit is set, only data will be stored in the SRAM cache. This function is typically used for L2 testing only.
10	L2I	L2 Global Invalidate. Setting this bit invalidates the L2 cache globally by clearing the L2 bits, including status bits. Do not set this while the L2 cache is enabled.
11	L2CTL	L2 ZZ Enable. When enabled, this bit tells the processor to use the low-power ZZ or Snooze Mode of the SRAM when the processors enters nap or sleep mode. Micron SRAMs support ZZ.
12	L2WT	L2 Write-Through. Set this bit to select write-through mode versus the default write-back mode. In write-through mode all data is written to the cache and to the 60x bus.
13	L2TS	L2 Test Support. Refer to the MPC750 Microprocessor User's Manual for more information.
14-15	L2OH	L2 Output Hold. Set to 00 for SyncBurst. 00 0.5ns 10 RESERVED
16	L2SL	L2 DLL Slow. In general this bit should be set for L2 SRAM frequencies below 100 MHz.
17	L2DF	L2 Differential Clock. Do not set this bit, and the two output clocks operate in tandem.
18	L2BYP	L2 DLL Bypass. Refer to the MPC750 Microprocessor User's Manual for more information.
19-30	RESERVED	Reserved for future use.
31	L2IP	L2 Global Invalidate in Progress (READ ONLY). This bit of the register cannot be set. When read out active, it indicates an L2 global invalidate is occurring.

FOR MORE INFORMATION

This paper is intended to provide an introduction to how SRAM memory should be connected to the Arthur processor. For more detailed cache information, refer to the following documents:

- PowerPC 750 SCM RISC Microprocessor: Hardware Specifications from IBM (1/98, Rev 1.0).
- PowerPC 750 RISC Microprocessor User's Manual. (Chapter 9 on L2 Cache Interface Operation is especially useful.)

CONCLUSION

Using cache SRAM with the Arthur PowerPC processor provides a powerful boost in performance by minimizing the time that the processor has to wait for data. This article provides an easy method of determining the correct SRAM to use, how to connect it to the 750 and how to configure the cache control register.

TECHNICAL NOTE

USING SRAMs WITH POWERPC MPC505 & MPC509 MICROCONTROLLERS

This article was originally published in 1998.

INTRODUCTION

With the help of this article, microcontroller board designers can easily interface SyncBurst™ SRAMs with high-end microcontrollers such as Motorola's PowerPC MPC505 and MPC509. Synchronous SRAMs are used for this application because they offer the best cost-performance with these microcontrollers. The only difference between the MPC505 and the MPC509 is the amount of on-chip SRAM memory; the 505 has 4KB and the 509 has 22KB. Both are offered in the same 160-pin quad flat package.

APPLICATIONS

Potential applications for the PowerPC microcontrollers range from car engine controllers, to personal communicators (such as personal digital assistants and smart cellular phones), to set-top converters, control systems, high-end disk drives, fast laser printers and plotters.

Table 1
SINGLE-CHIP SYNCBURST MEMORY SOLUTIONS

DENSITY	x16 SOLUTION	x32 SOLUTION
1Mb	64K x 16	32K x 32
2Mb	128K x 16	64K x 32
4Mb	256K x 16	128K x 32
8Mb	512K x 16	256K x 32
16Mb	1 Meg x 16	512K x 32

BLOCK DIAGRAM

The MPC505 and MPC509 microcontrollers have two internal buses: the instruction bus (I-bus) and the load/store bus (L-bus). These buses are connected to the external bus (E-bus) through the external bus interface (EBI). Figure 1 shows the EBI signal names and how they connect to the SyncBurst SRAM. The EBI interfaces the E-bus with the two internal buses (the I-bus and the L-bus).

The PowerPC microcontroller can use two different widths of SRAM memory (x16 or x32), depending on the application. Table 1 lists single-chip SyncBurst solutions. Using 32-bit words provides more bandwidth to the processor in any SRAM access cycle and is probably the pre-

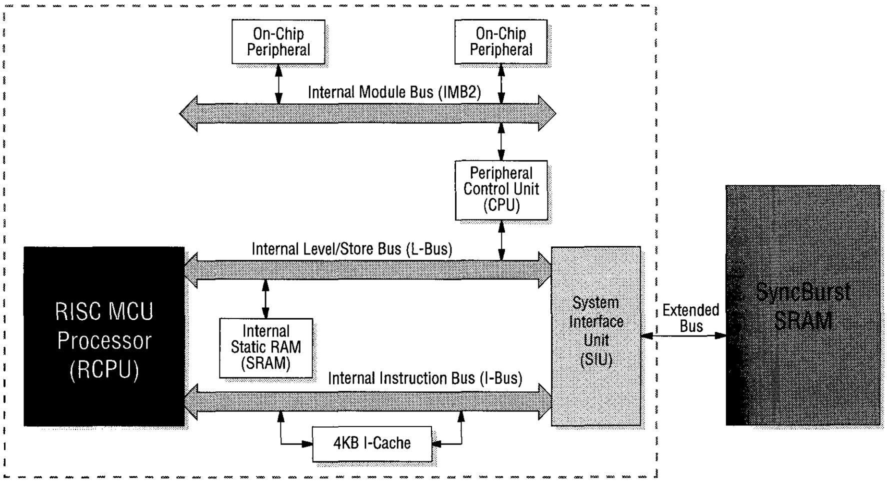


Figure 1
CONNECTING THE MICROCONTROLLER TO THE SYNCBURST™ SRAM

ferred implementation for most applications since it can be implemented in a single chip.

USING SYNCBURST SRAMs

The EBI supports several different memory categories (SRAM, EEPROM) and types (asynchronous, synchronous, pipelined and burst). The bus is synchronous—all signals are referenced to the rising edge of the bus clock.

To connect the SyncBurst SRAM to the microcontroller, the user first needs to determine the size of memory space and the location in the address space where the SRAM memory will reside.

There may be some confusion about which MPC50x address bits connect to which SyncBurst SRAM address bits. ADDR[29] must be connected to SA0 and ADDR[28], to SA1 (Figure 2). Those two bits from the microprocessor must be connected to the lower two address bits on the SRAM so that bursting of the addresses is done properly. However, the connection of the remaining address bits from the microcontroller to the SRAM is arbitrary; it is best to choose a connection that makes board routing easy (Tables 2 and 3).

Similarly, when connecting a byte of data (i.e., DATA[0] to DATA[7]) from the microcontroller to DQa's, the connection is arbitrary. Data is always addressed in bytes, so bits within a byte can be swapped to minimize routing difficulty.

One thing to note: In this example, DATA[0:7] is connected to the DQa's and BE0# is connected to BWa#. This is not the only possible choice. If it would make the routing easier, DATA[0:7] could be connected to the DQb's and BE0# to BWb#. Then the other three bytes and associated byte enables could be shuffled, as desired by the user, to minimize routing problems. Bytes may be switched as long as the correct byte enable connections are made.

The pins that control the burst function, BDIP# and TS#, also need to be connected to the SRAM. BDIP# should be connected to the ADV# pin and TS# should be connected to

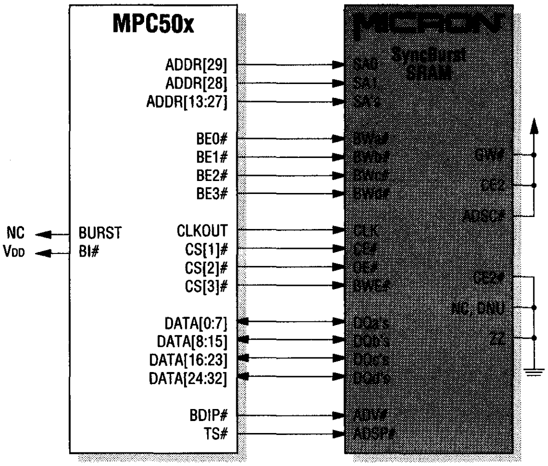


Figure 2
CONNECTING THE MPC505/MPC509 TO THE SYNCBURST SRAM

Table 2
CONNECTING SYNCBURST SRAM CONTROL SIGNALS TO THE MPC505/MPC509

MPC50X SIGNAL NAME	SYNCBURST SIGNAL NAME
ADDR[29]	SA0
ADDR[28]	SA1
ADDR[13] to ADDR[27]	SA's
BE0#	BWa#
BE1#	BWb#
BE2#	BWc#
BE3#	BWd#
CLKOUT	CLK
CS[1]#	CE#
CS[2]#	OE#
CS[3]#	BWE#
DATA[0] to DATA[7]	DQa's
DATA[8] to DATA[15]	DQb's
DATA[16] to DATA[23]	DQc's
DATA[24] to DATA[32]	DQd's
TS#	ADSP#
BDIP#	ADV#

Table 3
HARDWIRING UNUSED CONTROL INPUTS ON THE SRAM

SYNCBURST SIGNAL NAME	CONNECT TO
GW#	VDD
CE2	VDD
CE2#	GND
ADSC#	VDD
NC, DNU	GND*
ZZ	GND

*GND is recommended, but these pins may be left unconnected.

the ADSP# pin. Because the chip selects handle all burst times, BI# (burst inhibit) should be tied to V DD and the burst pin should be left floating.

PROGRAMMING THE BASE ADDRESS OF THE SRAM MEMORY AND SETTING CHIP SELECT OPTIONS

The MPC microcontrollers have programmable chip select pins (up to 11; CS[0:11]) that can control the SRAM. These pins can be configured as chip enables, write enables or output enables. The choice of which pin to use is left to the user, who might have several different types of memory (EPROM/SRAM), depending upon the actual application.

For this application it is assumed that CS1# on the microcontroller is used for CE# on the SRAM. CS2# will be configured as R/W# and CS3# will be OE. Table 4 shows the addresses of the registers that need to be programmed for this operation.

For this application it is also assumed that the memory depth is 128KB. The optimal memory for this depth is Micron's 128K x 32 SRAM (MT58LC128K32B4). Several fields are described below for the optional register settings for the SRAM. (Also see Tables 5 and 6.)

- ✔ BSIZE: Determines the depth of the memory assigned to a particular memory space. For a depth of 128KB, BSIZE equals 0110.
- ✔ ACKEN or Acknowledge Enable: Disabled in this example (set to 0) since the SRAM is not designed to return signals back to the microcontroller.
- ✔ PS or Port Size: 32 bits (PA = 10).
- ✔ PCON: Set to 00 for chip enable, 01 for write enable and 10 for output enable.
- ✔ BYTE: This applies to pins configured as byte write enables. Since the memory in this example has a width of x32, the value of this field is "Don't Care."
- ✔ MEMORY REGION: For WE# or OE# pins, this tells which chip enable they work with (001 = CS1#).
- ✔ ITYPE or Interface Type: For this example, the SRAM is assumed to be synchronous with asynchronous OE#; ITYPE = 0101.

Table 4
BASE ADDRESS REGISTERS USED

REGISTER	ADDRESS
CS1# Base Address Register (CSBAR1)	0x8007 FDE0
CS2# Base Address Register (CSBAR2)	0x8007 FDD8
CS3# Base Address Register (CSBAR3)	0x8007 FDD0

Table 5
OPTIONAL REGISTERS

REGISTER	ADDRESS
CS1# Option Register (CSOR1)	0x8007 FDE4
CS2# Option Register (CSOR2)	0x8007 FDDC
CS3# Option Register (CSOR3)	0x8007 FDD4

Table 6
OPTIONAL REGISTER FIELD SETTINGS (CSOR1 TO CSOR3)

Register	BSIZE	ACKEN	PA	PCON	BYTE	REGION	ITYPE
CSOR1	0110	0	10	00	xx	xx	0101
CSOR2	0110	0	10	01	xx	001	0101
CSOR3	0110	0	10	10	xx	001	0101

CONFIGURING THE SIU MODULE CONFIGURATION REGISTER (SIUMCR)

The SIU module configuration register allows the user to configure various aspects of the SIU interface. One of the fields that applies to the SRAM memory (LST) is shown in Table 7. Because burst is used, burst must be set as the type of memory.

CONFIGURING FOR A x16 DATABUS WIDTH VERSUS x32

This article is based on an application using a x32 SRAM; however, the bus can also be configured to a x16 width. To configure the bus as x16 versus x32 requires the use of only two of the byte enable signals from the microcontroller and the connection of an extra address bit (BE2#/ADDR30) to the SRAM.

Although the bus requires a x16 width, SyncBurst SRAMs are only made in a x18 configuration. The x18 device is the recommended device for x16 applications. Technical Note TN-58-12, "Using Parity SRAMs in Nonparity Applications," describes how to use x18 devices in x16 applications.

CONCLUSION

The MPC family of microcontrollers, along with Micron's SyncBurst SRAMs, offers an excellent solution for many applications. Given the depth of Micron's SRAM product family, there is an SRAM to fit the memory requirements of almost any application.

Table 7
SIUMCR[0:31] FIELDS THAT AFFECT THE SYNCBURST SRAM

FIELD NAME	BIT LOCATION	DESCRIPTION
LST	4	Chooses between BDIP# and LAST#. Timing for SyncBurst operation, choose LAST#.

FLASH TECHNICAL NOTE SELECTION GUIDE

For the latest technical information on Micron products, read our quarterly technical newsletter *Design Line*.
Call 208-368-3900 to be added to our mailing list or visit our Web site (www.micron.com/mti/msp/html/dlindex.html).

TECHNICAL NOTE

BOOT BLOCK FLASH MEMORY TECHNOLOGY

INTRODUCTION

Flash memory is a programmable, read-only, nonvolatile memory similar to EPROM and EEPROM. Although flash memory is a derivative of EPROM and EEPROM, it possesses many advantages that make it a more attractive nonvolatile memory choice. This technical note describes these advantages, as well as other characteristics inherent to Micron's boot block flash memory technology.

GENERAL FLASH CHARACTERISTICS

Although flash shares many characteristics with EPROM and EEPROM, current-generation flash differs in that erase operations are done in blocks. Flash, EPROM and EEPROM all must be erased before being written. When erasing EPROM, the entire chip is erased with a UV light source. EEPROM is automatically erased before a WRITE on a byte basis. Flash is either erased in blocks (boot block or sectored erase block flash) or the entire chip at once (bulk erase flash).

Boot block devices have erase blocks that vary in size from 4KB to 128KB. A hardware-protected boot block (typically 16KB) provides maximum security for core firmware. To write or erase the boot block, the reset pin must be brought to a super-voltage (V_{HH} = 12V) or the write protect pin (WP#) brought to V_{IH} in addition to the normal WRITE or ERASE sequences. Sectored erase block flash has blocks of equal size, some with no additional hardware protection. This configuration is suited for mass storage or firmware applications. Although flash is erased on a block basis, WRITE and READ operations are done on a random byte or word basis.

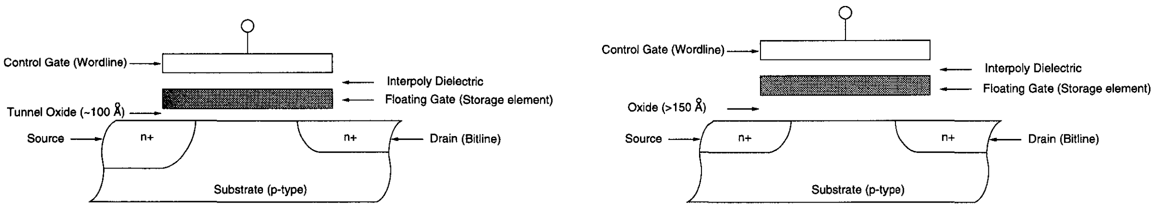
AUTOMATED WRITE AND ERASE

One feature that many current-generation flash devices have is an on-chip state machine that automates WRITE and ERASE. First-generation flash and EPROM typically require the host system or programmer to execute complex algorithms to write and erase. These algorithms are required to write any flash cell, but on current-generation flash the algorithms are executed internally by a state machine. This frees the host system to do other tasks while the state machine writes or erases the flash memory and simplifies design-in of flash by reducing software overhead necessary to write or erase the device.

During a WRITE, the state machine controls the WRITE pulse timing to the cell, tracks the number of pulses issued, controls the voltages applied to the cell and verifies that the data was written correctly. When executing an ERASE, the state machine first writes all locations within the block to 0 so that each cell contains uniform charge. The state machine then issues the ERASE pulses to the cells within the block and monitors the ERASE for completion. At any time during a WRITE or ERASE, the status register may be read to monitor the WRITE or ERASE in progress or to check for the completion of the WRITE or ERASE cycle.

FLASH CELL STRUCTURE

Most flash devices share basically the same cell structure as the EPROM cell. Both the flash and EPROM cells are dual polysilicon (poly), floating-gate CMOS field effect transistors. The first poly layer is isolated from the control gate by an interpoly dielectric layer and from the substrate by a thin



Flash Cell **EPROM Cell**

Figure 1
FLASH CELL vs. EPROM CELL

oxide layer. This isolation allows the first poly layer (floating gate) to store charge. The second poly layer is connected to the wordline and functions as the control gate. However, there are two main differences between a flash cell and an EPROM cell that allow for electrical erase of the flash cell. Flash has a thinner oxide layer of approximately 100 angstroms to enable Fowler-Nordheim tunneling of electrons from the floating gate during an ERASE. In addition, flash has a deeper source diffusion to further enhance ERASE performance. Figure 1 compares the two types of memory cells.

WRITE

Flash and EPROM implement hot electron injection to place charge on the floating gate during a WRITE. During a WRITE, a high programming voltage ($V_{PP} = 12V$) is placed on the control gate. This forces an inversion region to form in the p-type substrate. The drain voltage is increased to approximately half the control gate voltage (6 volts) while the source is grounded (0 volts), increasing the voltage drop between the drain and source. (See Figure 2.) With the inversion region formed, the current between drain and source increases. The resulting high electron flow from source to drain increases the kinetic energy of the electrons. This causes the electrons to gain enough energy to overcome the oxide barrier and collect on the floating gate.

After the WRITE is completed, the negative charge on the floating gate raises the cell's threshold voltage (V_T) above the wordline logic 1 voltage. When a written cell's wordline is brought to a logic 1 during a READ, the cell will not turn on. The sense amps detect and amplify the cell current and output a 0 for a written cell.

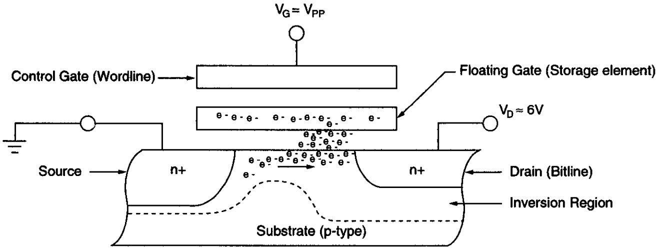


Figure 2
FLASH CELL DURING A WRITE

ERASE

Flash employs Fowler-Nordheim tunneling to remove charge from the floating gate to bring it to the erased state. Using high-voltage source erase, the source is brought to a high voltage (V_{PP} = 12V), the control gate grounded (0 volts) and the drain left unconnected. (See Figure 3.) The large positive voltage on the source, as compared to the floating gate, attracts the negatively charged electrons from the floating gate to the source through the thin oxide. Because the drain is not connected, the ERASE function is a much lower current-per-cell operation than a WRITE that uses hot electron injection.

After the ERASE is completed, the lack of charge on the floating gate lowers the cell's V_T below the wordline logic 1 voltage. When an erased cell's wordline is brought to a logic 1 during a READ, the transistor will turn on and conduct more current than a written cell. Some flash devices use Fowler-Nordheim tunneling for WRITEs as well as ERASEs.

ARRAY ARCHITECTURE

Micron's flash product line implements NOR architecture for the highest random-access performance. This architecture is optimal for systems requiring updatable firmware storage. See Figure 4 for more detail on the NOR architecture.

READING

During a READ of a byte or word of data, the addressed row (wordline) is brought to a logic 1 level (> V_T of an erased cell). This condition turns on erased cells which allow current to flow from drain to source, while written cells remain in the off state with little current flow from drain to source. The cell current is detected by the sense amps and amplified to the appropriate logic level to the outputs. All other wordlines within the array remain low. Because only one wordline needs to be controlled at a time during a READ, the decode overhead is minimized. As a result, high random-access READ performance is achieved with the NOR architecture.

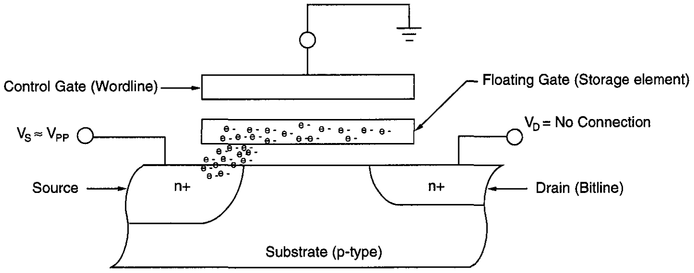


Figure 3
FLASH CELL DURING HIGH-VOLTAGE SOURCE ERASE

WRITING

Similar to READs, WRITEs are also done on a random-access basis. The addressed wordline is brought to a super-voltage of 12 volts, the bitline (drain) is brought to approximately 6 volts, while the source remains at 0 volts. All other wordlines within the array remain low.

ERASING

ERASE operations are done on a block basis in NOR flash memory. The source of a cell is common to each cell within a given erase block. During an ERASE, the bitlines are left open, all the wordlines are at 0 volts, and the source is brought to 12 volts, erasing all cells within the block. The other blocks in the device are not exposed to high voltages, reducing the chance for data corruption of other blocks during an ERASE.

SUMMARY

Micron's boot block flash memory family provides designers with secure, updatable firmware storage. WRITE operations implement hot electron injection similar to EPROM, and ERASE operations use Fowler-Nordheim tunneling similar to EEPROM. However, by automating the write and erase algorithms, the state machine simplifies design-in of flash memory. With the NOR architecture, the highest random-access WRITE and READ performance is achieved.

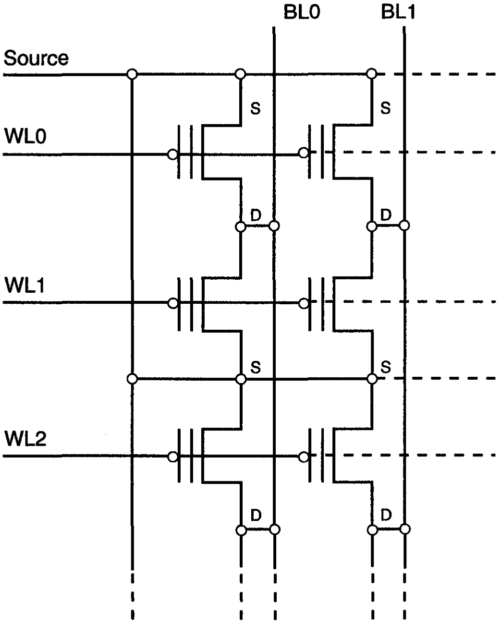


Figure 4
NOR FLASH CELL ARRAY

TECHNICAL NOTE

BULK ERASE TO BOOT BLOCK CONVERSION

NTRODUCTION

With multiple erase blocks, hardware-protected boot lock, higher densities, and simplified write and erase lgorithms, boot block flash memory is fast becoming preerred over bulk erase flash for firmware storage. Because of hese advantages and since many suppliers are phasing out ulk erase in favor of newer technology boot block, designrs are changing new and existing designs from bulk erase o boot block flash.

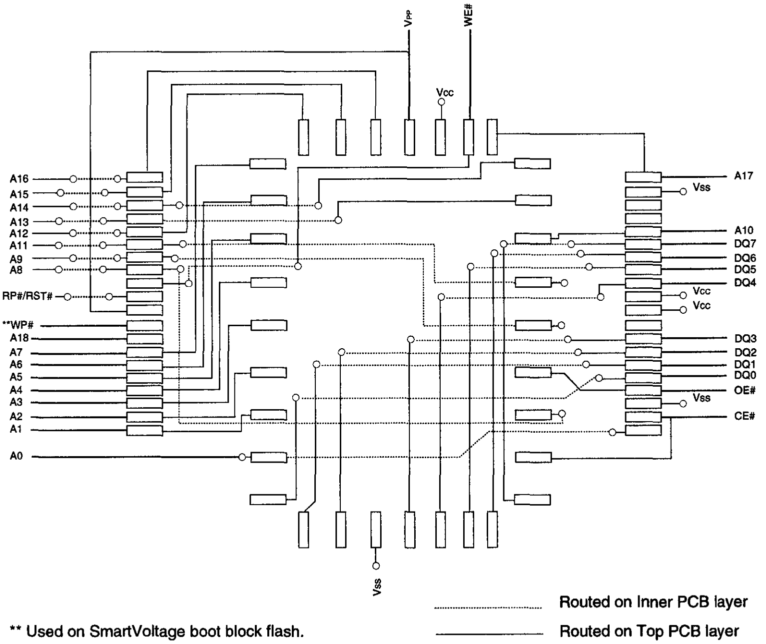
To simplify this transition, Micron has created a dual omponent pad layout that can accept either a 32-lead LCC (1Mb or 2Mb bulk erase) or a 40-lead TSOP Type I 2Mb or 4Mb boot block). This allows the use of either evice now and a full conversion to boot block devices ater. A plot or gerber file of this layout may be obtained by alling Micron applications engineering at 208-368-3900.

DESIGN ISSUES

PINOUT DIFFERENCES

The pin functions are identical between bulk erase flash and boot block flash, with the addition of the reset pin (RST# on 12V VPP flash or RP# on SmartVoltage Technology flash) on the boot block devices. This pin clears the status register and resets the state machine when LOW, and unlocks the boot block when brought to a super-voltage (12 volts). The reset pin must be held HIGH during all other modes of operation.

On SmartVoltage boot block flash, the WP# (write protect) function is added to pin 12. Bringing this pin HIGH or RP# to a super-voltage unlocks the boot block. Pin 12 may be driven on Micron's 12V VPP flash since this pin is a no connect. See Technical Note TN-28-04 for more information on SmartVoltage and 12V VPP boot block flash compatibility.



** Used on SmartVoltage boot block flash.

Figure 1
PLCC-TSOP DUAL PAD LAYOUT (NOT TO SCALE)

COMMAND DIFFERENCES

Both the bulk erase flash and boot block flash use similar commands and command sequences to control device operation. However, boot block flash implements a state machine to execute and monitor WRITE and ERASE operations. Tasks such as verifying WRITE and ERASE operations and writing all locations to 0s before erasing must be performed by the host system with bulk erase flash. These functions are automatically performed by the state machine with boot block flash, thereby greatly reducing overhead required to write and erase the memory. Table 1 lists the commands for bulk erase and boot block flash.

BOOT BLOCK

The boot block (16KB) is hardware-protected for additional security against inadvertent code modification. READ operations on locations within the boot block are the same as for any other location in the memory array. However, to write or erase the boot block, the reset pin (RST# or RP#) must be brought to a super-voltage (12 volts) in addition to the normal WRITE or ERASE sequences. The remaining erase blocks vary in size and do not require a super-voltage on RST# or RP# to write or erase.

SUMMARY

Micron's dual component pad layout accepts either a 32-pin PLCC (bulk erase) or a 40-pin TSOP-I (boot block). This eases the transition from bulk erase to boot block. With an internal state machine to handle WRITE and ERASE operations and a hardware-protected boot block, boot block flash is an easy-to-design-in, superior firmware memory. To obtain a gerber file or plot of the dual component layout, please call Micron Applications Engineering at 208-368-3900.

Table 1
COMMAND SEQUENCES FOR BULK ERASE AND BOOT BLOCK FLASH

COMMANDS	BUS CYCLES REQ'D	1ST CYCLE			2ND CYCLE			NOTES
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA	
READ ARRAY								
Bulk Erase Flash	1	WRITE	X	00H				
Boot Block Flash	1	WRITE	X	FFH				
IDENTIFY DEVICE								
Bulk Erase Flash	3	WRITE	X	90H	READ	IA	ID	1, 2
Boot Block Flash	3	WRITE	X	90H	READ	IA	ID	1, 2
READ STATUS REGISTER								
Bulk Erase Flash	STATUS REGISTER NOT SUPPORTED							
Boot Block Flash	2	WRITE	X	70H	READ	X	SRD	3
CLEAR STATUS REGISTER								
Bulk Erase Flash	STATUS REGISTER NOT SUPPORTED							
Boot Block Flash	1	WRITE	X	50H				
ERASE SETUP/CONFIRM								
Bulk Erase Flash	2	WRITE	X	20H	WRITE	X	20H	
Boot Block Flash	2	WRITE	X	20H	WRITE	BA	D0H	4
ERASE VERIFY								
Bulk Erase Flash	2	WRITE	VA	A0H	READ	X	VD	5, 6
Boot Block Flash	OPERATION DONE BY STATE MACHINE							
ERASE SUSPEND/RESUME								
Bulk Erase Flash	OPERATION NOT SUPPORTED							
Boot Block Flash	2	WRITE	X	B0H	WRITE	X	D0H	
WRITE SETUP/WRITE								
Bulk Erase Flash	2	WRITE	X	40H	WRITE	WA	WD	7
Boot Block Flash	2	WRITE	X	40H	WRITE	WA	WD	7
WRITE VERIFY								
Bulk Erase Flash	2	WRITE	X	C0H	READ	X	VD	6
Boot Block Flash	OPERATION DONE BY STATE MACHINE							
ALTERNATE WRITE								
Bulk Erase Flash	OPERATION NOT SUPPORTED							
Boot Block Flash	2	WRITE	X	10H	WRITE	WA	WD	7

NOTE:

1. IA = Identify Address: 00H for manufacturer ID, 01H for device ID.
2. ID = Identify Data.
3. SRD = Status Register Data.
4. BA = Block Address.
5. VA = Address to be verified.
6. VD = Verify Data.
7. WA = Address to be written; WD = Data to be written to WA.

TECHNICAL NOTE

DESIGNING FOR SMARTVOLTAGE TECHNOLOGY FLASH

This article was originally published in 1995.

INTRODUCTION

As system operating voltages decrease with the increasing need for updatable firmware in both battery and plug-in computing products, designers must consider the present and future operating voltages of components used in their designs. With higher voltage requirements for WRITE and ERASE operations versus READ operations, many of today's flash memories pose an even greater challenge to design into a low- or single-voltage system. Micron's SmartVoltage Technology (SVT) flash memory provides several benefits to the system designer, maximizing design-in flexibility for any application. This article will describe these benefits, show various methods to upgrade a design using 12V VPP (WRITE/ERASE voltage) boot block flash to SVT flash, and describe techniques that can be employed to further utilize SVT flash flexibility.

SMARTVOLTAGE TECHNOLOGY (SVT)

SVT provides industry-standard, dual-supply operation for flash memory, with the added option of single-voltage operation. All operations can be done with a VCC voltage of 3.3V or 5V, while WRITE and ERASE operations can be performed with 5V or 12V on the VPP pin. Future generations of SVT flash will operate with a VCC and VPP voltage as low as 2.7V (MIN). Micron's SVT boot block flash pinout provides an upgrade path from 2Mb to 8Mb and is also backward-compatible with 12V-only VPP boot block flash. See Figure 1 for SVT pinouts.

VOLTAGE CONSIDERATIONS

Flash memory inherently requires different voltages to write or erase than to read. Single-supply flash (with only a VCC pin) implements internal charge pumps to pump the VCC voltage to the higher (10V-12V) voltage levels supplied to the flash cells during a WRITE. The charge pump's ability to pump the WRITE or ERASE voltage from VCC limits the minimum allowable VCC voltage. Internal charge pumps are typically less efficient (30-50 percent) than external charge pumps (60-80 percent).

SVT retains the dual-supply pinout of the 12V VPP flash family and adds 5V VPP WRITE/ERASE capability. Separate pins for VCC and VPP mean the minimum VCC operating voltage is not limited by the minimum voltage required to write or erase the flash cells on VPP. This allows VCC to be scaled to lower voltages sooner than operating voltages of single-supply flash memory. Without this limitation, SVT flash can be designed into 3.3V systems today, with the option of an external 5V supply for VPP. In future generations of SVT flash, the VPP voltages will "catch up" to the VCC voltages to allow for 3.3V WRITE and ERASE.

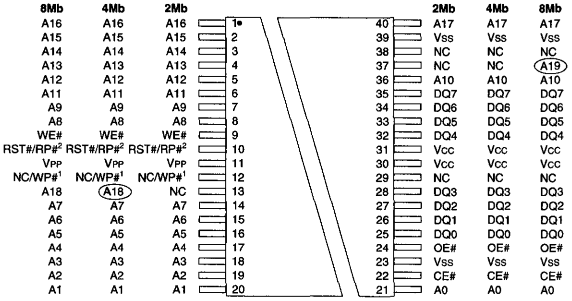
BOOT BLOCK

SVT boot block flash operates identically to the 12V VPP boot block, with an additional method for unlocking the hardware-protected boot block. To unlock the boot block, the RST# (renamed to RP# on SVT) is brought to 12V in addition to the normal WRITE or ERASE sequences. The WP# (write protect) pin is added to the SVT boot block pinout to allow for unlocking the boot block in systems without 12V. When the WP# pin is LOW, WRITE or ERASE of the boot block is prohibited, and when WP# is HIGH, the boot block is unlocked for WRITE or ERASE. Either method of unlocking the boot block works on SVT boot block flash.

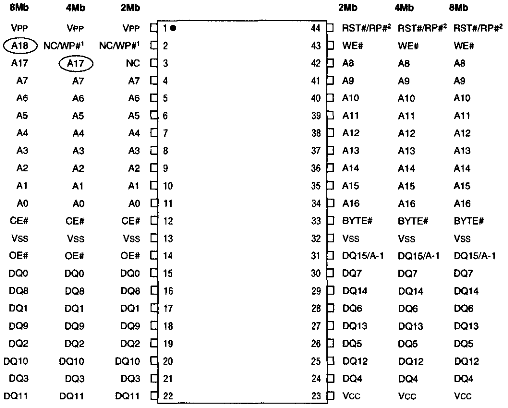
UPGRADING TO SVT FROM 12V VPP FLASH

SVT provides for an easy transition from 12V VPP flash to SVT boot block flash. Present users of 12V VPP flash can easily modify existing designs to accept SVT boot block flash depending on system requirements.

40-PIN TSOP



44-PIN SOP



48-PIN TSOP

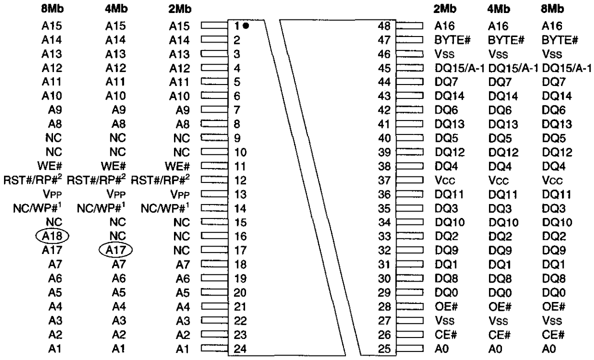


Figure 1
SVT PACKAGE PINOUTS

NOTE: 1. No connect (NC) for 12V boot block; write protect (WP#) for SVT boot block.
2. Reset (RST#) for 12V boot block; reset/power-down (RP#) for SVT boot block.

CASE 1: MAINTAINING 12V VPP OPERATION

For systems that require the highest WRITE/ERASE performance, both SVT and 12V VPP flash can be designed in to operate identically with a 12V WRITE/ERASE voltage. This also provides the added benefit of an alternate source during the transition from 12V VPP flash to SVT. All commands and WRITE/ERASE timings are identical between Micron's SVT boot block and its 5V VCC/12V VPP equivalent. In addition, all electronic IDs are identical between Intel® and Micron® SVT boot block flash. Besides SVT's 5V WRITE/ERASE option, the only difference between the two types of flash is the addition of the WP# pin on SVT.

By hard-wiring the WP# pin to VSS, SVT boot block flash becomes operationally equivalent to 12V VPP flash, and the boot block can be unlocked only when RP# is brought to a super-voltage (12V). On previous versions of Micron's flash data sheets, the pin corresponding to WP# on the 12V VPP boot block was listed as a "DU" (don't use). However, this pin is a no connect and is currently specified as such on Micron's latest data sheets.

Systems requiring the highest degree of data security should switch VPP to VSS when a WRITE or ERASE is not being executed to prevent inadvertent data modification on all blocks. Switching VPP to VCC (5V) will prevent WRITE or ERASE operations on 12V VPP flash, but driving VPP to VSS will work on both types. A simple circuit consisting of two FETs can be implemented to switch VPP between 12V and VSS. See Figure 2 for a VPP switch example.

CASE 2: FULL CONVERSION TO 5V-ONLY OPERATION

If 12V is used in the system solely for flash WRITE and ERASE, the 12V power supply may be eliminated with a small reduction in WRITE/ERASE performance by switching to SVT. Systems can be designed to use a 12V WRITE/ERASE voltage now and have the simplicity of 5V-only operation later without a PCB redesign. The following steps illustrate how to accomplish this:

1. VPP should be jumper-selectable between VCC (5V) and the 12V supply, allowing for the future elimination of the 12V supply without a board revision. If absolute WRITE/ERASE protection for all blocks is desired, the VPP pin should be switchable between either power supply and VSS.

2. If the boot block is to be unlocked in-system, RP# should be switchable between a super-voltage (unlock boot block) and VCC (normal operation for both 12V VPP and SVT). Designers may want to implement this switch with a jumper that can be set by a user when boot block modification is desired, further reducing the chance of boot block corruption. To add the capability to reset the part or implement SVT's deep power-down mode (ICC = 8µA MAX), the RP# pin must also be switchable to VSS ±0.2V. A circuit that can switch between the three voltages is shown in Figure 3. Note that when RP# is brought to a super-voltage, the voltage at the pin is 12V minus the drop across R1. R1 is necessary to limit the current from the 12V supply in case a system reset occurs during boot block modification (RP# brought to VSS). The switch for 12V (in dashed box) can be removed when SVT is used.

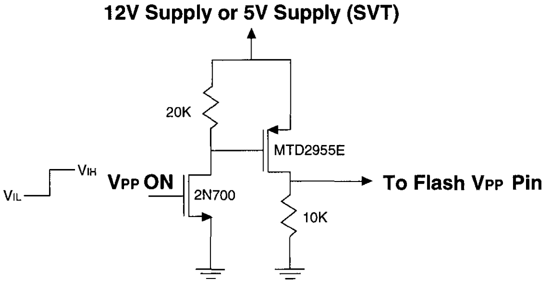


Figure 2
VPP SWITCH EXAMPLE

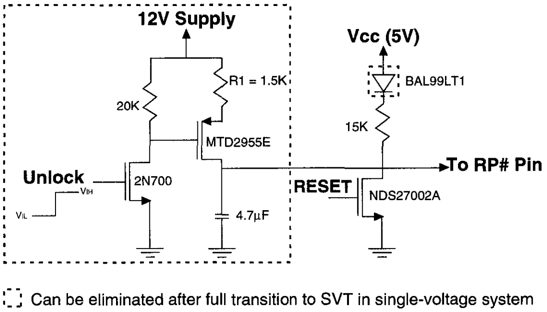
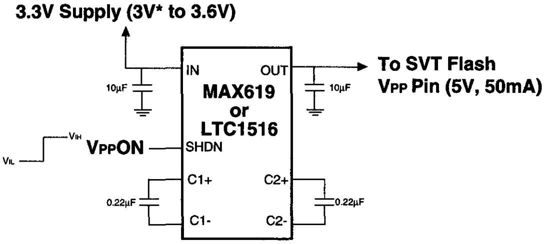


Figure 3
RP# SWITCH EXAMPLE

3. The WP# pin should be tied to a write-protect control signal if the boot block is to be unlocked in-system; it should be tied to Vcc for systems that do not require additional protection for the boot block; or it should be tied to Vss for permanent in-system boot block protection. WP# must not be left floating. Since the corresponding pin on 12V VPP boot block is a no connect, these changes can be done without affecting the functionality of Micron's 12V VPP boot block flash used in the same design.

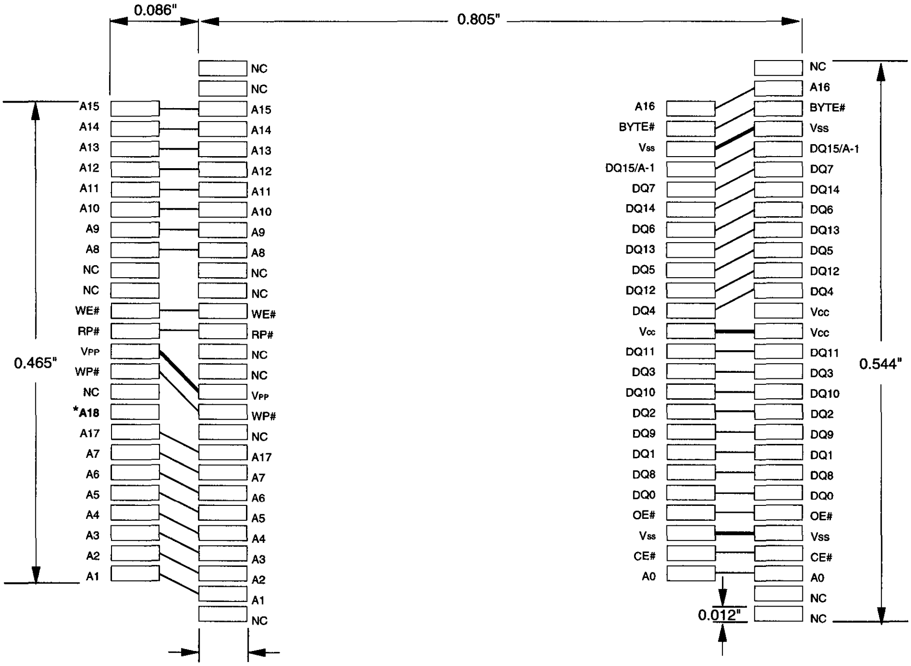
CASE 3: DESIGNING SVT INTO A 3.3V SYSTEM

In 3.3V systems without a 5V or 12V supply, a charge pump DC-DC converter can be implemented to supply the WRITE/ERASE voltage. Charge pumps are relatively inexpensive, consume little power when in shutdown mode (1µA typical) and require little board space. The charge pump can eventually be eliminated when converting to future SVT flash that can operate with a VPP voltage of 3.3V. By providing a jumper to bypass the power supply and having VPP switchable to Vcc (3.3V), this future transition can be implemented without a PCB redesign. An example using Maxim's MAX619 or Linear Technology's LTC1516 regulated 5V charge pump is shown in Figure 4. This scheme can be implemented using as little as 0.1 square inches of board space.



*Output will be 5V, 20mA with 2V ≤ VIN < 3V

Figure 4
3V to 5V CHARGE PUMP EXAMPLE



***A18 used for 8Mb boot block**

Figure 5
48-LEAD/56-LEAD TSOP-I DUAL-PAD LAYOUT

PACKAGING CONSIDERATIONS

In addition to the 40-lead TSOP-I (x8 data path), 56-lead (x8 or x16) TSOP-I and 44-lead SOP (x8 or x16), the 48-lead (x8 or x16) TSOP-I has been introduced for SVT boot block flash. With an even larger offering of packages, designers must consider issues such as data path width and board space when choosing the appropriate package. However, since the number of different packages may push suppliers' back-end capacities, the most important issue may be package availability. Micron believes the 48-lead TSOP-I will be the package of choice for space-constrained applications because it maintains the x8/x16 functionality of the 56-lead in a 12 percent smaller package (0.063" narrower), it has pending JEDEC standardization, and it can easily be configured to run in x8 systems. For applications where board space is not a factor or TSOP-I handling in production is not desirable, the SOP will remain the package of choice.

Since the same die is used in both the 56-lead and 48-lead TSOPs, the pin rotations of the two packages are identical. This simplifies the redesign when converting from the 56-lead to 48-lead TSOP. Traces require only minimal rerouting, and the removed pads provide for additional signal routing space. Via relocation or addition should be minimal, further reducing PCB retooling costs. All operational features are identical between the two packages.

To achieve an even greater degree of component sourcing flexibility, both the 48-lead and 56-lead TSOPs can be designed to operate in the same system. By offsetting the pad layouts for both parts, only 11 percent (47 square mils) additional board space is required. Since all operations are identical between both packages, no production test changes are necessary on the PCB assembly. See Figure 5 for more detail.

With the BYTE# pin on all x16 boot block flash, the 48-lead TSOP can be designed into 8-bit systems where board space is not at a premium. To accomplish this, BYTE# (pin 47) should be tied to Vss, the data bus should be connected to DQ0-DQ7, and the dual-use pin DQ15/A-1 (pin 45) should be connected to the lowest order address line. DQ8-DQ14 become no connects and can be utilized as "pass-throughs" to route other signals. See Figure 6 for a block diagram of this implementation.

SUMMARY

SVT offers the maximum design-in flexibility for boot block flash memory. By maintaining the dual-supply pinout of 12V VPP flash, SVT remains backward-compatible to 12V VPP and will be forward-compatible with tomorrow's operating voltages. The pinout compatibility between 12V VPP and SVT flash provides an easy upgrade path to SVT. Systems can be designed to accommodate both SVT and 12V VPP without any future changes, or be designed to move from 12V VPP to SVT with only minor jumper modifications. With SVT comes the introduction of the 48-lead TSOP-I. Since it is functionally identical to the 56-lead part in a smaller package and has pending JEDEC standardization, designers should consider the 48-lead TSOP-I for new, space-constrained applications.

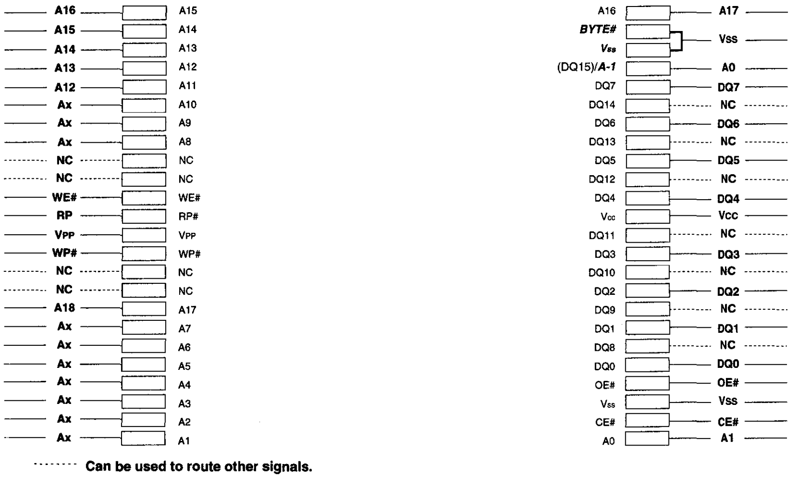


Figure 6
48-LEAD TSOP-I x8 IMPLEMENTATION

TECHNICAL NOTE

MICRON®-INTEL® FLASH COMPATIBILITY

his article was originally published in 1997.

NTRODUCTION

The Micron® boot block flash memory family features full ompatibility with the industry standard for boot block lash memory. Micron's boot block flash memory incorpoates SmartVoltage Technology (SVT) to maximize voltage ompatibility throughout a wide range of applications. By eaturing 100 percent drop-in compatibility with the Intel® martVoltage boot block flash memory family, Micron's oot block flash devices provide flash customers with an lternate source that requires no hardware or software hanges to use. This technical note examines the issues ddressed by Micron to ensure full drop-in compatibility ith the Intel device.

ACKAGE CONSIDERATIONS

Micron offers packages identical to Intel's for the 2Mb, Mb and 8Mb boot block flash memories. The Micron 44-pin SOP, 40-pin TSOP-I and 48-pin TSOP-I require the same pad layout as the Intel equivalents. In addition, the Micron devices are fully pin-compatible. Micron and Intel flash are interchangeable in a socket designed around either device, with no hardware or PCB layout changes.

COMMANDS AND FUNCTIONS

The command set used by the Micron boot block flash memory is identical to the command set used by Intel. None of the Intel command set has been omitted or modified by Micron. This allows programming and erase algorithms developed for the Intel device to be used with the Micron part as well. Table 1 lists the command sequences for the Micron and Intel boot block devices.

Micron's boot block flash features the same erase block architecture as the Intel devices. Both top and bottom boot block organizations are available in all densities.

Table 1
MICRON AND INTEL COMMAND SEQUENCES

COMMANDS	BUS CYCLES REQ'D	1ST CYCLE OPERATION	1ST CYCLE ADDRESS	1ST CYCLE DATA	2ND CYCLE OPERATION	2ND CYCLE ADDRESS	2ND CYCLE DATA	NOTES
READ ARRAY	1	WRITE	X	FFH				1
IDENTIFY DEVICE	3	WRITE	X	90H	READ	IA	ID	2, 3
READ STATUS REGISTER	2	WRITE	X	70H	READ	X	SRD	4
CLEAR STATUS REGISTER	1	WRITE	X	50H				
ERASE SETUP/CONFIRM	2	WRITE	X	20H	WRITE	BA	D0H	5, 6
ERASE SUSPEND/RESUME	2	WRITE	X	B0H	WRITE	X	D0H	
WRITE SETUP/WRITE	2	WRITE	X	40H	WRITE	WA	WD	6, 7
ALTERNATE WORD/BYTE WRITE	2	WRITE	X	10H	WRITE	WA	WD	6, 7

NOTE:
1. Must follow WRITE or ERASE CONFIRM commands in order to enable flash array READ cycles.
2. IA = Identify Address: 00H for manufacturer compatibility ID; 01H for device ID.
3. ID = Identify Data.
4. SRD = Status Register Data.
5. BA = Block Address.
6. Addresses are "Don't Care" in first cycle but must be held stable.
7. WA = Address to be written; WD = Data to be written to WA.

All of the pin functions of the Intel boot block devices are supported on the Micron device. Deep power-down, RP# at super-voltage and WP# HIGH boot block unlock, and A9 at super-voltage device ID mode are among the pin functions supported by the Intel and Micron boot block devices.

ALGORITHMS

As mentioned previously, programming and erase algorithms developed for the Intel device can also be used on the Micron device. The Appendix lists flow charts for WRITE and ERASE operations for Micron and Intel devices. To enhance drop-in use of the Micron device, the device and manufacturer IDs of the Micron part match those of the equivalent Intel device. This allows the Micron device to be used in existing designs without any software changes Table 2 lists the electronic IDs for the Micron and Intel boo block devices.

Table 2
MICRON AND INTEL ELECTRONIC IDs

DEVICE	MICRON (TOP)	INTEL (TOP)	MICRON (BOTTOM)	INTEL (BOTTOM)
28F800	889CH	889CH	889DH	889DH
28F008	98H	98H	99H	99H
28F400	4470H	4470H	4471H	4471H
28F004	78H	78H	79H	79H
28F200	2274H	2274H	2275H	2275H
28F002	7CH	7CH	7DH	7DH
Manufacturer Compatibility: 89H (All Micron and Intel Parts)				

When programming Micron flash on a device programmer, users can select an Intel or Micron algorithm. Although the Intel algorithm will work seamlessly, having a Micron-specific algorithm allows users to avoid any confusion or uncertainty whatsoever when programming a Micron device. Since the electronic IDs and all other functions are identical, either algorithm will work for either device.

PERFORMANCE

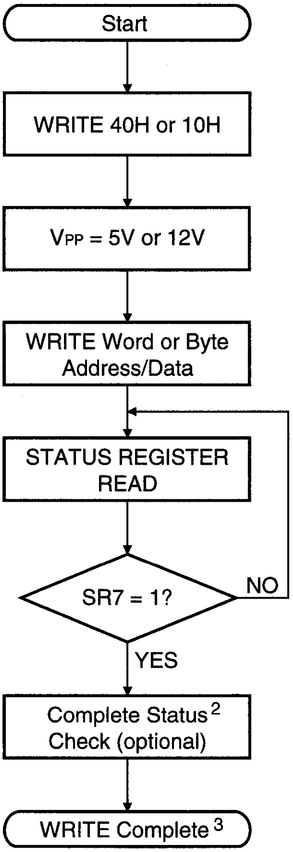
All timing and DC characteristics are comparable to the Intel device. Refer to the Intel or Micron data sheets for more information.

CONCLUSION

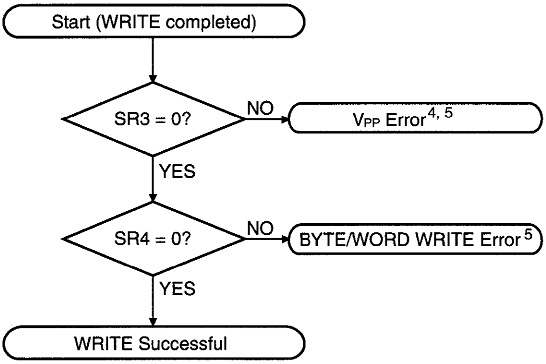
Micron's SmartVoltage boot block flash memory family is 100 percent drop-in compatible with Intel's SmartVoltage boot block family. By offering the same packages as Intel and matching Intel's programming algorithms, Micron flash memory can be used in any existing system designed around the Intel device with no hardware or software changes.

PPENDIX
RITE/ERASE ALGORITHM FLOWCHARTS

SELF-TIMED WRITE SEQUENCE (WORD or BYTE WRITE)[1]



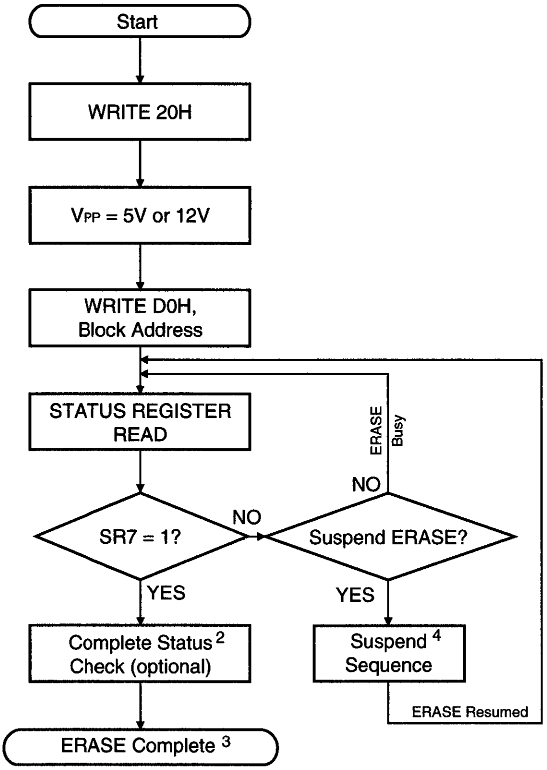
COMPLETE WRITE STATUS-CHECK SEQUENCE



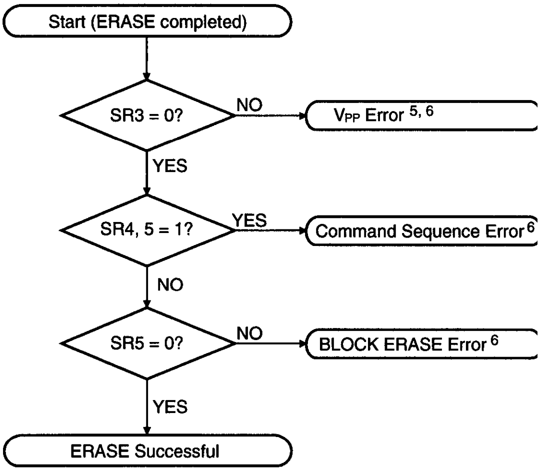
OTE:
1. Sequence may be repeated for additional BYTE or WORD WRITEs.
2. Complete status check is not required. However, if SR3 = 1, further WRITEs are inhibited until the status register is cleared.
3. Device will be in status register read mode. To return to the array read mode, the FFH command must be issued.
4. If SR3 is set during a WRITE or BLOCK ERASE attempt, CLEAR STATUS REGISTER must be issued before further WRITE or ERASE operations are allowed by the CEL.
5. Status register bits 3-5 must be cleared using CLEAR STATUS REGISTER.

APPENDIX
WRITE/ERASE ALGORITHM FLOWCHARTS (continued)

SELF-TIMED BLOCK ERASE SEQUENCE[1]



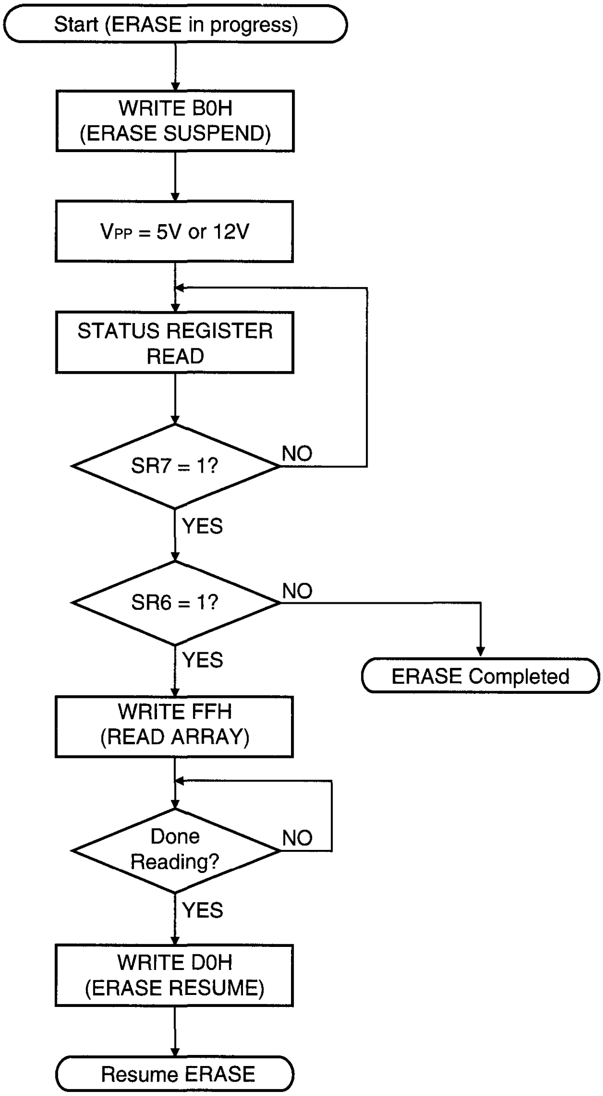
COMPLETE BLOCK ERASE STATUS-CHECK SEQUENCE



NOTE:
1. Sequence may be repeated to erase additional blocks.
2. Complete status check is not required. However, if SR3 = 1, further ERASEs are inhibited until the status register is cleared.
3. To return to the array read mode, the FFH command must be issued.
4. Refer to the ERASE SUSPEND flowchart for more information.
5. If SR3 is set during a WRITE or BLOCK ERASE attempt, CLEAR STATUS REGISTER must be issued before further WRITE or ERASE operations are allowed by the CEL.
6. Status register bits 3-5 must be cleared using CLEAR STATUS REGISTER.

APPENDIX
WRITE/ERASE ALGORITHM FLOWCHARTS (continued)

ERASE SUSPEND/RESUME SEQUENCE



TECHNICAL NOTE

DESIGNING FOR MULTIPLE BOOT BLOCK FLASH MEMORY SOURCES

INTRODUCTION

With the rapid growth of the nonvolatile memory market, various vendors have introduced flash memory. Though many of the standards differ from vendor to vendor, systems can be designed to accommodate flash from multiple vendors in a single socket. This article examines designing a system to implement two types of boot block flash memory: single-supply boot code sector flash memory from AMD (AM29Fx00) and dual-supply boot block flash memory from Micron (MT28Fx00). AMD also manufactures even-sectored devices (29F0x0), which have a comparable command interface to the AMD boot code sector devices. However, the pinouts of the even-sectored devices differ considerably from the pinouts of the boot code sector devices, making it difficult for a board layout to accommodate both standards in a single socket.

Since the Micron® boot block devices are 100 percent compatible with Intel® boot block flash memory, this article applies to compatibility between AMD and Intel as well. See Micron Technical Note TN-28-05, "Micron-Intel Flash Compatibility," for more information.

PINOUT AND PACKAGE CONSIDERATIONS

Both the Micron MT28F200/400/800 and AMD AM29F200/400/800 are available in 44-pin SOP and 48-pin TSOP Type I packages. The 48-pin TSOP-I gives designers the smallest x16 form factor for portable designs, while the 44-pin SOP is the easier of the two packages to handle in manufacturing. For x8 applications that require the smallest available package, Micron also offers a 40-pin TSOP-I.

Since the Micron MT28Fx00 is a dual-supply (VCC and VPP) device, while the AMD AM29Fx00 is a single-supply device (VCC), the pinouts will be inherently different. However, most of the pins are defined identically between the two standards. There are only three pins that are not common to both standards: VPP and WP# on the Micron device, and RY/BY# on the AMD device. The VPP and WP# pins can be tied to a supply without affecting the AMD device, while the RY/BY# pin should be left unused.

48-PIN TSOP-I

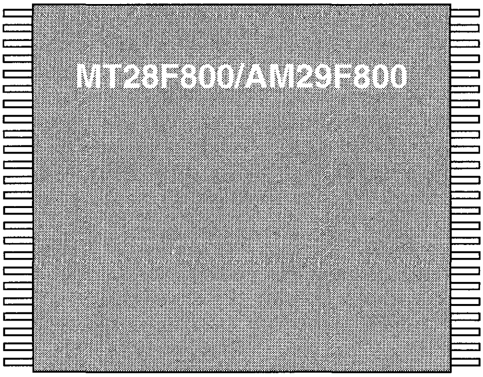
In addition to being the smallest available common package for the Micron and AMD devices, the 48-pin TSOP-I is the easiest package to design with for compatibility across both standards. All of the pins specific to one standard are no connects on the other standard. Therefore, these pins can be connected to a signal or supply without affecting operation of the device that does not use them. Because of this, a socket can be designed to accommodate either a Micron or AMD device without the need for jumpering pins.

The RY/BY# pin (pin 15) should be unused and left as a no connect; the VPP pin (pin 13) should be connected to VCC; and the WP# pin (pin 14) should be connected to VSS or VCC, depending on the desired boot block protection. Justification of these connections will be described in later sections of this article. Figure 1 shows the 48-pin TSOP-I pinout and the recommended connections for the AMD- and Micron-specific pins.

44-PIN SOP

Designing in the 44-pin SOP for compatibility across both standards is slightly more complex than implementing the 48-pin TSOP-I. First, the 44-pin SOP does not provide a seamless migration path from 2Mb to 8Mb boot block within either standard. With the Micron standard, pin 2 is the WP# pin on the 2Mb and 4Mb, but WP# goes away and becomes address 18 on the 8Mb. On the AMD standard, pin 1 is a no connect and pin 2 is the RY/BY# pin on the 2Mb and 4Mb, but the RY/BY# pin moves from pin 2 to pin 1 and pin 2 becomes address 18 on the 8Mb. Because of these issues, Micron does not recommend designing in the 44-pin SOP for both the Micron and AMD standard in applications that require an upgrade path from 2Mb or 4Mb to 8Mb.

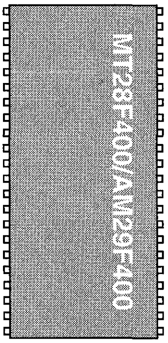
However, designing in the 44-pin SOP for only a 2Mb or 4Mb or only an 8Mb is much easier to do. The same recommendations for the V_{PP}, WP# and RY/BY# pins for the 48-pin TSOP-I still apply to the 44-pin SOP. However, the AMD RY/BY# pin must be jumpered so it can be configured based on which device is used. Figure 2 shows the recommended pin connections for designs using a Micron or AMD 2Mb or 4Mb device, and Figure 3 displays the recommended pin connections for using a Micron or AMD 8Mb device.



Recommended Connection	AMD	Micron	Pin	Pin	Micron	AMD	Recommended Connection
A15	A15	A15	1	48	A16	A16	A16
A14	A14	A14	2	47	BYTE#	BYTE#	Vcc (x16) or Vss (x8)
A13	A13	A13	3	46	Vss	Vss	Vss
A12	A12	A12	4	45	DQ15/A-1	DQ15/A-1	DQ15 (x16) or A-1 (x8)
A11	A11	A11	5	44	DQ7	DQ7	DQ7
A10	A10	A10	6	43	DQ14	DQ14	DQ14
A9	A9	A9	7	42	DQ6	DQ6	DQ6
A8	A8	A8	8	41	DQ13	DQ13	DQ13
NC	NC	NC	9	40	DQ5	DQ5	DQ5
NC	NC	NC	10	39	DQ12	DQ12	DQ12
WE#	WE#	WE#	11	38	DQ4	DQ4	DQ4
System Reset	RESET#	RP#	12	37	Vcc	Vcc	Vcc
Vcc	NC	V_{PP}	13	36	DQ11	DQ11	DQ11
Vcc or Vss	NC	WP#	14	35	DQ3	DQ3	DQ3
NC	RY/BY#	NC	15	34	DQ10	DQ10	DQ10
A18*	A18*	A18*	16	33	DQ2	DQ2	DQ2
A17**	A17**	A17**	17	32	DQ9	DQ9	DQ9
A7	A7	A7	18	31	DQ1	DQ1	DQ1
A6	A6	A6	19	30	DQ8	DQ8	DQ8
A5	A5	A5	20	29	DQ0	DQ0	DQ0
A4	A4	A4	21	28	OE#	OE#	OE#
A3	A3	A3	22	27	Vss	Vss	Vss
A2	A2	A2	23	26	CE#	CE#	CE#
A1	A1	A1	24	25	A0	A0	A0

*A18 is a NC for the 28F200/400
**A17 is a NC for the 28F200

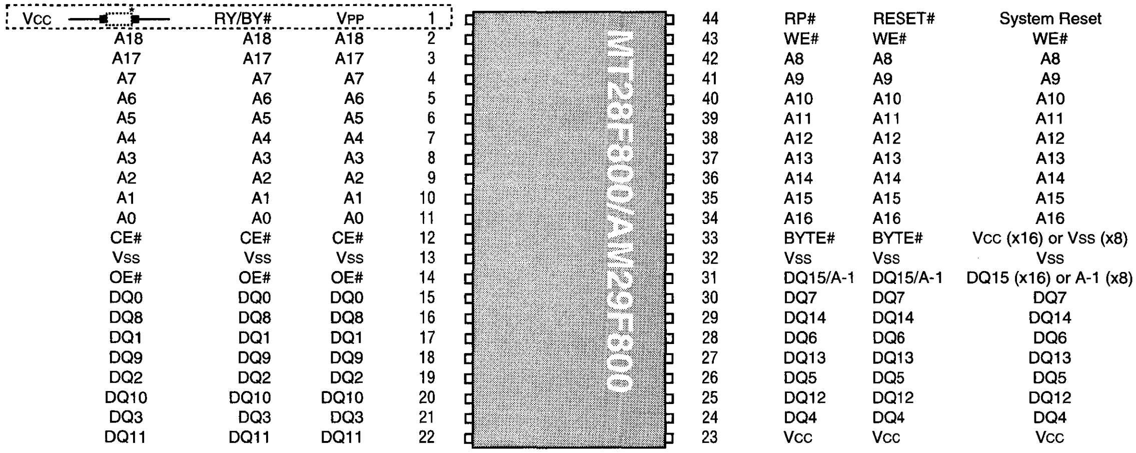
Figure 1
48-PIN TSOP-I PINOUT



Recommended Connection	AMD	Micron	Pin	Pin	Micron	AMD	Recommended Connection
Vcc	NC	V_{PP}	1	44	RP#	RESET#	System Reset
Vcc or Vss	RY/BY#	WP#	2	43	WE#	WE#	WE#
A17**	A17**	A17**	3	42	A8	A8	A8
A7	A7	A7	4	41	A9	A9	A9
A6	A6	A6	5	40	A10	A10	A10
A5	A5	A5	6	39	A11	A11	A11
A4	A4	A4	7	38	A12	A12	A12
A3	A3	A3	8	37	A13	A13	A13
A2	A2	A2	9	36	A14	A14	A14
A1	A1	A1	10	35	A15	A15	A15
A0	A0	A0	11	34	A16	A16	A16
CE#	CE#	CE#	12	33	BYTE#	BYTE#	Vcc (x16) or Vss (x8)
Vss	Vss	Vss	13	32	Vss	Vss	Vss
OE#	OE#	OE#	14	31	DQ15/A-1	DQ15/A-1	DQ15 (x16) or A-1 (x8)
DQ0	DQ0	DQ0	15	30	DQ7	DQ7	DQ7
DQ8	DQ8	DQ8	16	29	DQ14	DQ14	DQ14
DQ1	DQ1	DQ1	17	28	DQ6	DQ6	DQ6
DQ9	DQ9	DQ9	18	27	DQ13	DQ13	DQ13
DQ2	DQ2	DQ2	19	26	DQ5	DQ5	DQ5
DQ10	DQ10	DQ10	20	25	DQ12	DQ12	DQ12
DQ3	DQ3	DQ3	21	24	DQ4	DQ4	DQ4
DQ11	DQ11	DQ11	22	23	Vcc	Vcc	Vcc

*Jumper is removed with AMD device installed
**A17 is a NC for the 28F200

Figure 2
2Mb/4Mb PIN CONNECTIONS FOR MICRON AND AMD 44-PIN SOP



Recommended Connection	AMD	Micron	Pin	Pin	Micron	AMD	Recommended Connection
Vcc ——*——	RY/BY#	VPP	1	44	RP#	RESET#	System Reset
A18	A18	A18	2	43	WE#	WE#	WE#
A17	A17	A17	3	42	A8	A8	A8
A7	A7	A7	4	41	A9	A9	A9
A6	A6	A6	5	40	A10	A10	A10
A5	A5	A5	6	39	A11	A11	A11
A4	A4	A4	7	38	A12	A12	A12
A3	A3	A3	8	37	A13	A13	A13
A2	A2	A2	9	36	A14	A14	A14
A1	A1	A1	10	35	A15	A15	A15
A0	A0	A0	11	34	A16	A16	A16
CE#	CE#	CE#	12	33	BYTE#	BYTE#	Vcc (x16) or Vss (x8)
Vss	Vss	Vss	13	32	Vss	Vss	Vss
OE#	OE#	OE#	14	31	DQ15/A-1	DQ15/A-1	DQ15 (x16) or A-1 (x8)
DQ0	DQ0	DQ0	15	30	DQ7	DQ7	DQ7
DQ8	DQ8	DQ8	16	29	DQ14	DQ14	DQ14
DQ1	DQ1	DQ1	17	28	DQ6	DQ6	DQ6
DQ9	DQ9	DQ9	18	27	DQ13	DQ13	DQ13
DQ2	DQ2	DQ2	19	26	DQ5	DQ5	DQ5
DQ10	DQ10	DQ10	20	25	DQ12	DQ12	DQ12
DQ3	DQ3	DQ3	21	24	DQ4	DQ4	DQ4
DQ11	DQ11	DQ11	22	23	Vcc	Vcc	Vcc

* Jumper is removed with AMD device installed

Figure 3
8Mb PIN CONNECTIONS FOR MICRON AND AMD 44-PIN SOP

BLOCK ARCHITECTURE

Both the Micron MT28F200/400/800 and AMD AM29F200/400/800 feature a 16KB boot block and two 8KB parameter blocks adjacent to the boot block. Both the Micron and AMD boot block devices are available in top boot (boot block located at the top of addressable space) or bottom boot configurations. The boot block provides an ideal storage location for core firmware and/or recovery code that requires higher security against inadvertent modification, while the smaller 8KB parameter blocks provide easy-to-manage locations for more frequently changing portions of code or data.

The only difference in block architecture between Micron and AMD is the size of the remaining larger main blocks. With Micron's block architecture, the remaining blocks consist of one 96KB block and either one (MT28F200), three (MT28F400) or seven (MT28F800) 128KB blocks. The AMD boot code sector family has one 32KB block, with three (AM29F200), seven (AM29F400) or fifteen (AM29F800) 64KB blocks. When erasing larger portions of code on the AMD device, systems will need to accommodate the differently sized main blocks. However, frequently changing portions of code can be stored in the two 8KB parameter blocks on both the Micron and AMD devices. Figure 4 compares the block architecture of the Micron and AMD 4Mb bottom boot block devices.

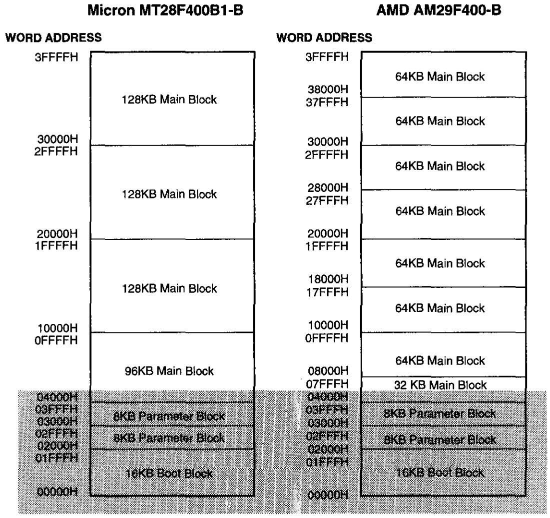


Figure 4
MICRON AND AMD 4Mb
BOTTOM BOOT BLOCK ORGANIZATION

BLOCK LOCKING

To provide additional protection against inadvertent code modification, both the Micron and AMD boot block devices feature block locking capability. Micron's 16KB boot block requires that WP# be driven HIGH or that the RP# (reset/power-down) pin be driven to a super-voltage (12V) before its contents can be modified. On the AMD device, all blocks are unprotected by default. However, any one or combination of blocks can be protected through a command sequence that requires the RESET# pin to be driven to a super-voltage (12V) before being modified. This command sequence is typically executed on a device programmer and not in-system. If block locking is implemented, the RESET# at super-voltage block unlock should be used since it is common to both the Micron and AMD devices.

As discussed in the previous pinout and packaging section, the WP# pin must be tied LOW or HIGH, depending on the desired boot block locking. WP# should be connected to Vss (LOW) if the boot block is to be protected with the Micron and AMD device. By limiting the protected blocks on the AMD device to the 16KB block, the Micron and AMD devices will feature the identical protected blocks. In this case, RESET# must be driven to a super-voltage if the boot block contents are to be modified.

If no additional boot block protection is required for the Micron device, the WP# pin may be connected to Vcc (HIGH). This will unlock the boot block on the Micron device, thus providing the same level of protection to the boot block as to the other blocks.

COMMAND DIFFERENCES

Both the Micron and AMD boot block devices feature a state machine to simplify WRITE and ERASE operations. Though the command interfaces for both part types are simple and require little system overhead, they do require different algorithms to perform certain functions. However, by using the electronic IDs to differentiate between the two devices, the correct command set can be implemented for the device used.

There are two ways to read the electronic IDs. One requires the address 9 pin (A9) to be driven to a super-voltage. This method is not practical to use in-system since it requires a high voltage switch on an address line. The A9 super-voltage is typically used in device programmers. Another method to check the electronic IDs is to issue the 90 (Hex) command to either device type. However, two consecutive cycles with alternating 1s and 0s (AAH-55H) on the data and address lines must be issued on the AMD device

Table 1
BUS CYCLES REQUIRED TO READ 2Mb, 4Mb AND 8Mb IDs

1st BUS CYCLE (WRITE)		2nd BUS CYCLE (WRITE)		3rd BUS CYCLE (WRITE)		4th BUS CYCLE (READ)		
ADDRESS	DATA	ADDRESS	DATA	ADDRESS	DATA	ADDRESS	DATA	DEVICE
5555H	AAH	2AAAH	55H	5555H	90H	00H	2275H	MT28F200B1-B
							2274H	MT28F200B1-T
							2257H	AM29F200-B
							2251H	AM29F200-T
							4471H	MT28F400B1-B
							4470H	MT28F400B1-T
							22ABH	AM29F400-B
							2223H	AM29F400-T
							889DH	MT28F800B1-B
							889CH	MT28F800B1-T
							2258H	AM29F800-B
							22D6H	AM29F800-T
						01H	xx01H	AMD mfg ID
							xx89H	Micron mfg ID

prior to issuing the 90H command. Since the two alternating AAH-55H commands will not affect the Micron device, the AMD method of reading electronic IDs should be used for both devices. After the 90H command has been issued on either device, a READ operation at address 00H outputs the manufacturer compatibility ID, while a READ at address 01H outputs the device ID. Though the upper 8 bits are output by both the Micron and AMD devices, they should be ignored since only the lower 8 bits are used for the device-specific IDs. Table 1 details the bus cycles required to read the electronic IDs for the Micron or AMD boot block devices.

COMMAND SEQUENCING

To execute operations, both devices require 8-bit commands to be written on the lower 8 data bits. Certain operations also require a valid address on the address inputs. To input a command to either device, OE# must be HIGH, CE# and WE# must be LOW, and the 8-bit command must be input on DQ0-DQ7. With the Micron device, addresses and data are latched on the rising edge of WE# (WE#-controlled) or CE# (CE#-controlled), whichever occurs first. The AMD device differs in that addresses and data are always latched on the rising edge of WE#. Refer to manufacturers' data sheets for a full listing of the Micron and AMD command sets.

POLLING FOR WRITE/ERASE COMPLETION

One aspect of command operations that differs between the AMD and Micron standards is that of polling for WRITE and ERASE completion. The Micron device features a status register that may be checked for WRITE or ERASE completion and any associated errors. The AMD device has a RY/BY# pin that may be polled for WRITE or ERASE completion, as well as DQ7 DATA# polling, DQ6 toggle bit, DQ5 timeout, and DQ3 sector erase timer. As previously mentioned, the RY/BY# pin is not common between both standards and thus should be unused and left as a no connect.

DQ7 POLLING

After the WRITE or ERASE command sequence has been executed on Micron's device, any READ operation will output the status register contents on DQ0-DQ7. DQ7 is the state machine status bit and indicates whether the device is busy executing an operation or is ready for another command. The remaining bits may be polled to view WRITE or ERASE error status, WRITE or ERASE suspend status and V_{PP} status. The device will remain in the status register read mode until another command is issued. To return to reading the array, the FFH command must be issued.

The AMD device does not use a status register. However, the AMD device may be polled in a similar manner to the Micron device to determine WRITE or ERASE completion. Several methods are implemented on the AMD device to poll for completion of WRITE or ERASE: RY/BY# pin, DQ7 DATA# polling, DQ6 toggle bit, DQ5 timeout and DQ3 sector erase timer.

Data polling is similar to status register polling since the same bit (DQ7) is used to determine WRITE or ERASE completion. With the Micron device, DQ7 is at V_{OL} while a WRITE or ERASE is executed and at V_{OH} when the device is ready for another command. With the AMD device, DQ7 is the complement of the data written while a WRITE is being executed and becomes the true data last written when the device is ready for another command. During an ERASE, DQ7 on the AMD device is at V_{OL} and transitions to V_{OH} when the device is ready for another command. While reading DQ7 on the AMD device, the WRITE or ERASE address must be asserted. Once DQ7 reflects the true data written or is at V_{OH} after an ERASE, subsequent READ operations will output the array data.

The AMD toggle bit, DQ5 timeout and DQ3 sector erase timer should not be used to poll for WRITE or ERASE. These functions are not compatible with the status register used on the Micron device.

CONCLUSION

Systems can be easily designed to accept both a Micron and AMD boot block flash memory in the same socket. By connecting the V_{PP} pin to V_{CC} and the WP# pin to V_{CC} or V_{SS}, a PCB layout can accept either a Micron or AMD boot block flash memory. Although the algorithms differ between the two devices, the electronic IDs can be read and then the proper algorithm set implemented for either device. After a WRITE or ERASE has been initiated, DQ7 can be polled on either device to check for WRITE or ERASE completion.

TECHNICAL NOTE

DUAL-SUPPLY BOOT BLOCK FLASH ADVANTAGES

INTRODUCTION

The flash memory market is one of the fastest growing memory markets today. With this growth has come the introduction of various types and standards of flash memory. One of the fundamental differences among the main flash suppliers is dual-supply vs. single-supply flash memory. Though the single-supply approach may initially appear simpler, the dual-supply approach provides cost savings and performance advantages to the end user. This article describes how a higher-voltage programming option, streamlined command interface and boot block security can reduce production costs and enhance system performance and reliability.

WRITE SPEED

Both single- and dual-supply flash memory require a high voltage to write. Figure 1 shows the voltages required to write a flash cell with hot electron injection, which is used by the majority of single- and dual-supply flash. For more detail on WRITE and ERASE operations from a flash cell standpoint, please refer to Micron Technical Note TN-28-01, "Boot Block Flash Memory Technology."

Single-supply flash must generate high gate voltage with an internal charge pump, which adds time to a WRITE. SmartVoltage dual-supply flash memory can supply this high voltage two different ways. If a low voltage (5V) is supplied to the programming supply pin (VPP), an internal charge pump outputs the higher voltage to the cells to be written. In this case, the charge pump adds time to WRITE operations, as it does with the single-supply devices. If a high voltage (12V) is supplied to VPP, the internal charge pump is bypassed, and the VPP voltage is given to the gate. This method eliminates the latency of the charge pump, and thus the write time is minimized. Typically, dual-supply flash writes 50 percent faster with a 12V VPP than single-supply flash.

Since SmartVoltage boot block flash memory can write at two different VPP voltages, users can choose to write with either voltage based on the desired performance and available voltages. Because of this, SmartVoltage boot block flash is optimal for systems in high-volume production. Users can place blank devices on boards and utilize 12V for in-circuit programming. This provides faster writing and maximizes production throughput, thus lowering production cost. Once the system is shipped to the field, 5V VPP can be used if a 12V supply is not available. Because single-supply flash limits in-circuit programming to a lower voltage, production cost is increased and throughput is sacrificed.

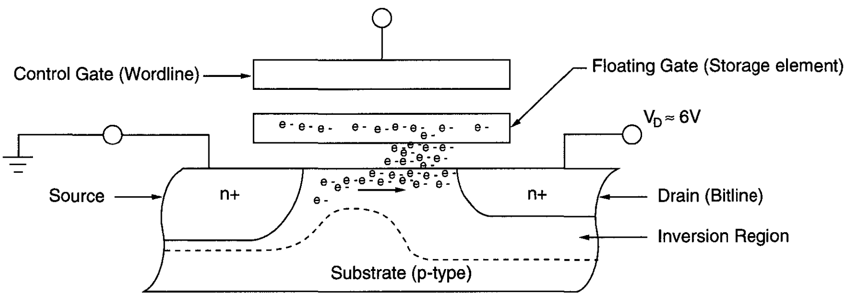


Figure 1
FLASH CELL WRITING

In applications where the flash is written on a device programmer before placement on a board, dual-supply flash memory also provides superior throughput. Regardless of the voltage used in the end application, device programmers can implement 12V for the fastest writing. But single-supply flash is limited to only one voltage, whether it is written in-system or on a device programmer. Since the device programmer command cycle times are typically long, the fact that the single-supply flash requires so many more bus cycles to write further lengthens the write duration.

COMMAND INTERFACE

All single- and dual-supply boot block flash memory utilizes a state machine to automate WRITE and ERASE operations. Tasks such as prewriting all cells before an ERASE, verifying WRITEs and ERASEs, and sequencing the programming voltages are all handled by the state machine. When compared to bulk erase flash, boot block flash memory provides simplified system implementation. Many of the tasks handled automatically by the state machine with boot block flash must be executed by the host system with bulk erase flash. Thus, by using boot block flash memory, system overhead is reduced, and write and erase algorithms are greatly simplified.

However, many WRITE and ERASE differences exist between single- and dual-supply boot block flash. Though the state machine does simplify WRITE and ERASE operations for either device, especially when compared to bulk erase flash, single-supply flash requires many more command cycles to execute WRITE or ERASE operations.

To write single-supply flash memory requires four bus cycles, and an ERASE requires six bus cycles. For dual-supply boot block flash, WRITE or ERASE operations take only two bus cycles to execute. The single-supply write and erase sequences have two command cycles in each, as do the dual-supply write and erase sequences. However, the single-supply write and erase sequences also have numerous "software unlock" cycles that must be issued, in addition to the two command cycles. Figure 2 shows an example of a dual-supply write or erase sequence, and Figure 3 shows an example of a single-supply erase sequence.

With the single-supply erase sequence, the four additional cycles (besides the 80H and 10H) consist of alternating 1s and 0s (AAAAH/5555H) that provide additional security against inadvertent ERASE. The dual-supply approach is simpler and consists of fewer bus cycles, but still provides a significant amount of security. If the 20H (ERASE SETUP) command is not followed by a D0H (ERASE CONFIRM), the device will prohibit an ERASE, and a command sequencing error will be reported in the status register.

SECURITY

Because dual-supply flash memory utilizes a separate pin (VPP) to provide the write and erase voltage, it inherently provides a higher degree of security over single-supply flash. This pin can be switched to ground to prevent the modification or corruption of code. With single-supply flash memory, no method exists to "lock" the entire device unless all of the blocks are locked on a programmer using the programmable sector lock feature.

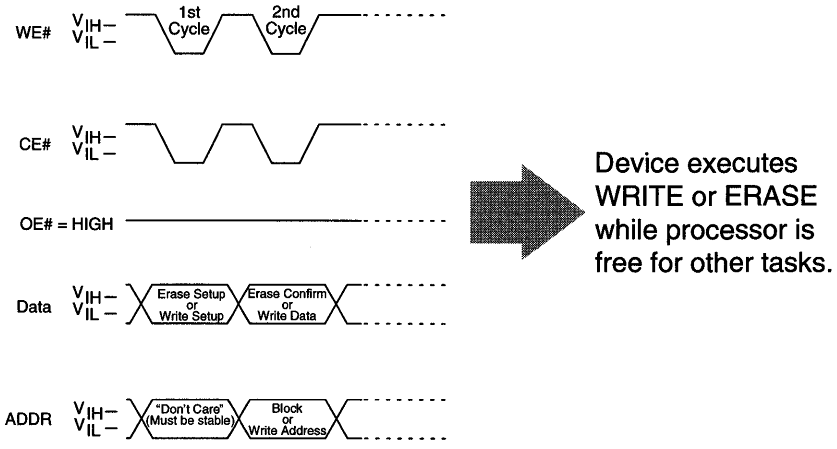
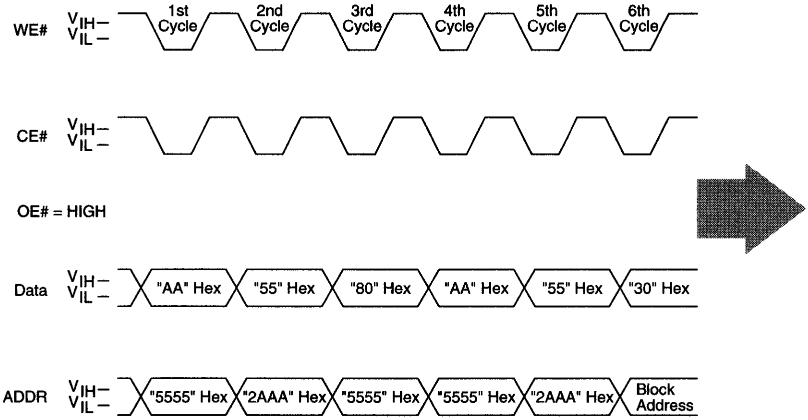


Figure 2
DUAL-SUPPLY WRITE OR ERASE OPERATION



Device executes ERASE while processor is free for other tasks.

Figure 3
SINGLE-SUPPLY ERASE OPERATION

Another security advantage that dual-supply boot block flash provides is a factory-locked boot block. The boot block is always locked and therefore can only be written or erased when the WP# pin (write protect) is driven HIGH or the RP# pin (reset/power-down) is driven to a super-voltage. Because of this, the boot block is an ideal area to store critical firmware or recovery code.

With single-supply boot block flash, none of the blocks is locked from the factory. To lock a block, an algorithm requiring high voltages (12V) on one or more pins must be run on a programmer. Because of this high-voltage sequencing, it is impractical to solder a blank device to a board, perform in-circuit programming and then lock blocks as part of the board assembly process. Doing so would add unnecessary cost to the board design by requiring high-voltage switches that would only be used during the board assembly and not in the end application.

SYSTEM AND PRODUCTION FLEXIBILITY

By taking advantage of dual-supply flash memory, users can maximize not only their system performance but their production throughput as well. Portable applications such as digital cellular phones and PDAs are migrating toward lower operating voltages to conserve battery life. Initially, a 3V-only, single-supply flash memory may seem like an obvious solution. However, the simplicity of a single operating voltage should be weighed against the benefits of faster write time and maximum security.

For example, many cellular phones today utilize flash for firmware storage and EEPROM for storing parameters such as speed-dial phone numbers and subscriber information. Since firmware seldom changes and is only updated at the factory or a service outlet, the main priority for the flash once the phone is shipped is low-voltage operation. In normal operation, V_{PP} can be switched to V_{SS} to prevent inadvertent modification of firmware, while V_{CC} is run at 2.7V to 3.6V. However, during manufacturing, 12V V_{PP} can be utilized for the faster writing, maximized production throughput and lower production cost. Designers who wish to use flash for both firmware and parameter storage and prefer to eliminate the EEPROM can write with 5V V_{PP}. In most cellular phones today, even if the baseband processing unit is run at 3V, the RF unit still requires 5V.

CONCLUSION

Dual-supply boot block SmartVoltage flash memory offers definite advantages to designers. With a high-voltage WRITE option and simpler command interface, users can minimize writing time and thus maximize production throughput and cost savings. In addition, the boot block on dual-supply flash comes from the factory locked, so data can be easily written and secured on a board instead of being written on a device programmer first. Even though a 3V-only, single-supply device initially appears to be a logical choice for certain applications, the simplicity of a single power supply must be weighed against the many advantages of dual-supply flash memory.

TECHNICAL NOTE

HIGH-VOLTAGE SWITCHING FOR FLASH MEMORY PROGRAMMING

INTRODUCTION

Dual-supply flash provides voltage flexibility, security and the fastest programming when 12V VPP is utilized. As flash vendors migrate to smaller process geometries, devices become more sensitive to voltage stress beyond maximum ratings. Since the VPP pin may require the highest possible voltage, it deserves special attention to guard against voltage overstress. This article examines several methods to switch 12V to the VPP pin so that the fastest programming can be achieved without compromising device reliability.

OVERVOLTAGE ISSUES

Voltage overstress damage to the VPP pin typically does not occur under DC conditions. The biggest potential cause of voltage overstress results from the AC characteristics of VPP when the pin is switched. Excess overshoot on the rising edge of VPP can violate maximum voltage levels for flash devices and damage the part. Typically the maximum transient voltage on the VPP pin is specified at 14V for <20ns. Regardless of the power supply, factors such as board layout and AC characteristics of the switching device can contribute to overshoot.

RELAYS

Although relays are useful for switching and multiplexing address, data and control input signals to device inputs, they should not be used to switch high-voltage power supplies. A relay's nearly instantaneous switching characteristics create a very fast rise time. The fast rise time, combined with a high voltage being switched, creates a very high overshoot. If a relay must be used, a very small series resistor with a capacitor to Vss should be implemented to slow down the rising edge of VPP. Figure 1 shows an example of 12V switched with a relay.

HOT SWITCHING

Dual-supply flash memory provides superior data security compared to single-supply flash memory, since the VPP pin can be switched to ground to absolutely prevent data modification. Jumpers may be used to switch the VPP pin between the programming voltage (5V or 12V) and ground (Vss). However, a jumper should not be switched while power is on. "Hot switching" such as this creates a nearly instantaneous rising edge and thus overshoot. The jumper should only be moved when power to the system is off.

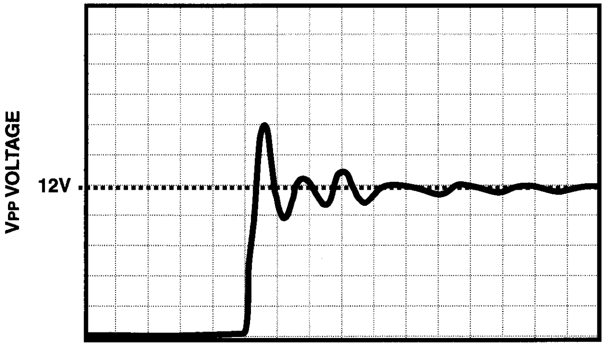


Figure 1
12V SWITCHED BY A RELAY

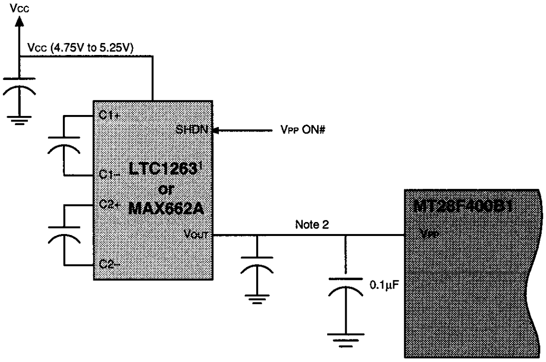
12V FLASH POWER SUPPLIES

There are many commercially available 12V power supplies (charge pump DC to DC converters) designed specifically for flash memory programming. These power supplies typically provide a regulated 12V ±5% output, require only a small number of capacitors to implement and consume little board space. The feedback loop used to regulate the DC level also controls the rise time, minimizing the chance for overshoot as long as good PCB layout practices are used and transmission line effects are minimized.

As an example, Figure 2 shows the circuit implementation for a Linear Technology LTC12633 or Maxim MAX662A, 12V, 60mA flash memory programming supply. The circuit only requires four capacitors, and the small-outline package only requires 44 mils^2 of board space.

USING FIELD-EFFECT TRANSISTORS (FETS) TO SWITCH 12V

FETs can be used to switch 12V to VPP. However, FETs typically feature fast rise times and turn-on times (ns range). Unless these transition times are slowed and good board layout is utilized, damaging overshoot may occur. One way to slow the rise time of VPP when switching with a FET is to add capacitive load to the gate of the FET. This load should be adjusted, depending on the PCB transmission line characteristics, to slow the rising edge and eliminate overshoot. FETs should be selected based on RDS (ON) and VDS (MAX) to ensure 12V can be switched without significant voltage drop so that 12V -5% can be met. Figure 3 is an example of a circuit using a FET to switch 12V to VPP.



NOTE:
1. Capacitance values used differ between manufacturers. Refer to data sheets for capacitor values.
2. Distance between power supply and flash should be as short as possible.

Figure 2
12V CHARGE PUMP EXAMPLE

BOARD LAYOUT ISSUES

Since the VPP pin supplies the flash device with the programming current as well as voltage, the pin must be routed on the PCB so that noise is minimized. Each flash device should have a 0.1µF ceramic decoupling capacitor between VPP and VSS to filter transients. To minimize inductance from long lead lengths, the capacitor should be located as close to the VPP pin as possible. Trace lengths between the VPP pin and the 12V supply should also be minimized to reduce transmission line effects.

CONCLUSION

With process geometries shrinking, flash devices are becoming more sensitive to voltage stress beyond maximum ratings. The VPP pin deserves special attention since 12V is required to switch to it. Anything that switches with a very fast rise time, such as relays, should not be used due to the large overshoot that results from the fast rise time. There are many flash-specific programming power supplies available that have controlled rise times to prevent voltage overstress of the VPP pin. FETs may be used to switch VPP, but the inherent fast rise time must be slowed to prevent overshoot and damage to the VPP pin.

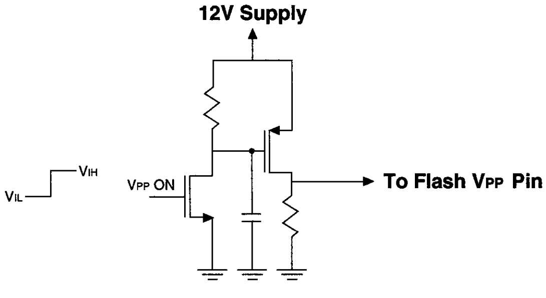


Figure 3
VPP SWITCH EXAMPLE

RELIABILITY/CHARACTERIZATION/MODELS GENERAL INFORMATION

NTRODUCTION

Micron Technology performs extensive testing and analyis on each memory product we offer. The data collected rom our testing and analysis aids in both the internal and ustomer qualification of the product and provides the user vith detailed knowledge of Micron component characterisics. Micron also offers device simulation models for products it offers. A brief overview of our product reliability rogram is included in this section.

NTERNAL QUALIFICATION/RELIABILITY

Micron's Internal Qualification document is a summary f the data collected during the process of qualifying a new roduct for production. Reliability data provided in the ocument includes ESD and latch-up test results, as well as esults from environmental tests such as high temperature perating life, temperature and humidity bias, temperature ycle, etc. The report also contains information on topos and rchitecture, thermal impedances, typical electrical characeristics and schmoo plots of electrical parameters. The ocument is updated as Micron continues to monitor the roduct characteristics and gathers additional reliability ata.

An Internal Qualification/Reliability document is generally published for each die revision Micron releases to production. Customers may request copies through their local Micron sales office or the Quality and Reliability Assurance Department (208-368-4387).

CHARACTERIZATION DATA

Characterization data on each device is contained in Micron's Internal Qualification/Reliability documents. Additional characterization data is available on a case-by-case basis.

DEVICE SIMULATION MODELS

Micron provides simulation models for each DRAM and SRAM manufactured. These models are revised as new die revisions and interface technologies are developed. Models for Flash products may be requested; they are developed as needed. Models can be obtained by contacting Micron's Applications Engineering Department at 208-368-3950 or by downloading them from our Web site (www.micron.com/mti/msp/models/index.html).

OVERVIEW

Product reliability is a product's ability to function within given performance limits under specified operating conditions over time. This section contains an overview of some of the issues that affect the reliability of IC devices and briefly describes Micron's reliability program.

For a more in-depth discussion of reliability, please refer to Micron's Quality/Reliability literature.

RELIABILITY GOALS

When we discuss reliability goals of semiconductor ICs, we typically refer to the traditional reliability curve of component life. The reliability curve, or "bathtub curve," appears below, where h(t) is the hazard rate or the probability of a component failing at $t_0 + 1$ in time if it has survived at time t_0.

The reliability curve in Figure 1 is divided into three segments: infant mortality, random failures and wearout. The term "infant mortality" refers to those ICs that would fail early in their lives due to manufacturing defects. To screen out such failures, Micron evaluates all of our products using intelligent burn-in. This unique AMBYX™ intelligent burn-in/test system, developed by Micron, is described in the following section.

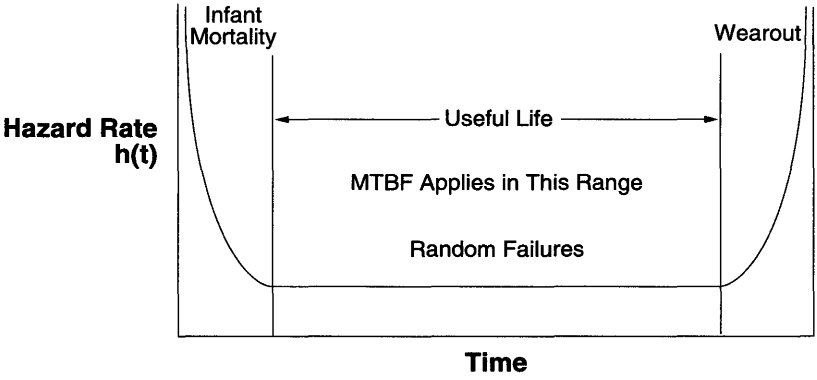


Figure 1
RELIABILITY CURVE

MICRON'S AMBYX™ INTELLIGENT BURN-IN AND TEST SYSTEM

Burn-in refers to the process of accelerating failures that occur during the infant mortality phase of component life o remove the inherently weaker devices. The process has been regarded as critical for ensuring product reliability since the beginning of the semiconductor industry. To screen out infant mortalities effectively, Micron believes it s critical to test devices for functionality several times during the burn-in cycle without removing them from the burn-in oven. In 1986, when we were unable to find a system that met our requirements, we introduced the concept of "intelligent" burn-in and developed the AMBYX ntelligent burn-in and test system. Today, we use AMBYX o test every component product we make.

With AMBYX, we can determine if the failure rate curves of individual product lots reach the random failure region of the bathtub curve by the end of the burn-in cycle. We subject product lots that do not exhibit a stable failure rate to additional burn-in. This burn-in flow also brings to our attention the slightest variation in a product's failure rate.

Since AMBYX allows us to test devices for functionality without removing them from the burn-in oven, we effectively eliminate failures resulting from handling, thereby minimizing "noise" from the test results. During the test phase, output produced by the devices under test s compared to the pattern expected. If a discrepancy occurs, AMBYX records the failure and provides the bit address, device address, board address, temperature, Vcc voltage, test pattern and time set.

The AMBYX intelligent burn-in procedure includes several test functions that are conducted during the burn-n session. The sequence begins with the testing of all components at room temperature to ensure all are functional. Functional testing continues as the oven temperature is ramped to 85°C. This enables us to detect thermal intermittent failures, another unique feature of ntelligent burn-in. We conduct the next test at 125°C; any device that does not pass is removed. The AMBYX sequence then enters a stress period during which the devices are dynamically stressed at high temperature and voltage. At regular intervals during this stress period, the devices are functionally tested at stress conditions. Next, the sequence enters a latency period where the devices continue to be stressed at high temperature but at a reduced voltage. Again, the devices are functionally tested at regular intervals. These test results allow us to identify individual failures during the burn-in periods. Following the burn-in periods, the devices are functionally tested as the oven temperature is ramped down to 85°C and then to 25°C. Repeated on every device in every production lot, this sequence of stress and functional testing enables us to construct the first portion of the bathtub curve of component reliability (infant mortality and the first part of the random portion).

Micron conducts the latency burn-in period and subsequent interval tests at lower Vcc than the preceding stress period for two important reasons. First, we want the several million device hours that we accumulate weekly on production lots to be conducted at stress conditions identical to the conditions for the extended high temperature operating life (HTOL) test used by IC manufacturers to compute random field failure rates. Second, we want to be sure we are not introducing new failure modes unrelated to normal wearout, such as VOS, by testing them at extremely elevated conditions.

Trend charts, such as the one shown in Figure 2, alert us to trends in lot failure rates. When we detect an upward trend in a failure rate, we correlate the lots that need additional burn-in with all the variables that might be influencing the increased rate.

The overall benefits of intelligent burn-in are wide ranging. Intelligent burn-in allows us to identify early-life failures and failure mechanisms as they would actually occur in customer applications. It also allows us to identify problem lots that, if undetected, could contribute substantially to infant mortalities.

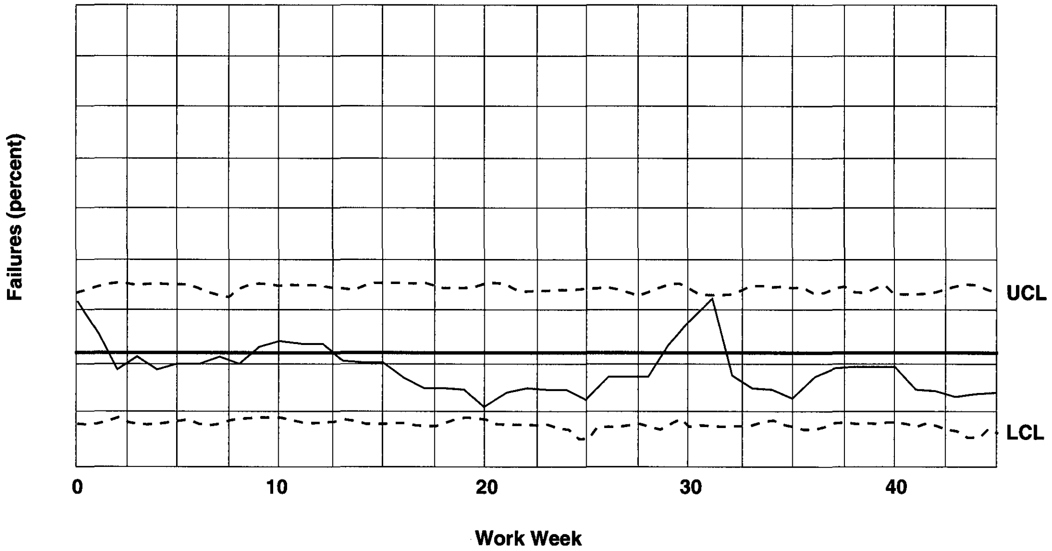


Figure 2
AMBYX LATENCY PERIOD FAILURES

ENVIRONMENTAL PROCESS MONITOR (EPM) PROGRAM

Micron's EPM program is designed to ensure the reliability of our standard products. Under this program, we subject weekly samples of our various product and package types to a battery of stress tests.

During these tests, we stress the devices for many hours under conditions designed to simulate years of normal field use. We then apply equations derived from intricate engineering models to the data collected from the accelerated tests. From these calculations, we are able to predict failure rates under normal use.

High Temperature Operating Life (HTOL)

The HTOL test, also known as high temperature bias (HTB), is the most important stress test for determining product field reliability. The test is used to determine the failure rate of the device in the random portion of the bathtub curve for component reliability, discussed previously in this section. During HTOL, devices are subjected to 125°C temperatures and are biased using checkerboard and checkerboard-complement test patterns. The test voltage applied is dependent upon the product type. Because these conditions have proven to be effective accelerators of oxide and silicon defects, as well as ionic contamination, we are able to predict hard error rates for our various products using the results from this stress test. Before beginning the stress test, all sample devices are tested for functionality. The devices are then stressed for 1,008 hours in 168-hour intervals and are retested for functionality after each interval. Extrapolation from stress conditions to operating conditions is done using acceleration factors for temperature and voltage stress described subsequently in this section.

Low Temperature Operating Life (LTOL)

The low temperature operating life test is used to evaluate the effect of hot electrons on critical parameters such as threshold voltage, transconductance and drive current that, in turn, affect device performance and refresh characteristics in DRAMs. The test is conducted at -25°C with dynamic bias. The voltage applied is dependent upon the product type. Before beginning the stress test, all sample devices are tested for functionality. The devices are then stressed for 1,008 hours in 168-hour intervals and retested for functionality after each interval.

Autoclave (AC)

Autoclave, also referred to as pressure-cooker test, is designed to accelerate moisture-induced failures for plastic packaged devices. The test provides a good measure of mobile ionic contamination, such as chlorine, sodium, etc. present in the process. Common failure modes associated with this stress test include metal line corrosion (often associated with passivation integrity) and bond pad corrosion (often associated with mobile ion contaminants). The test is conducted at 121°C, 100 percent relative humidity, 15 psi and is unbiased. Before beginning the stress test, all sample devices are tested for functionality. The devices are then stressed for 96 hours and are tested for functionality following stressing.

Temperature and Humidity Bias (THB)

The temperature and humidity test, also known as 85/85, is a moisture stress test for plastic packaged devices. This test is less accelerated than the autoclave stress test but includes a bias on alternating pins. The voltage applied is dependent upon the product type. Although the test takes longer to complete than autoclave, it provides more realistic results with regard to field reliability of the device relative to moisture performance. In addition, the applied bias promotes galvanic reactions. The test is conducted at 85°C, 85 percent relative humidity and alternating bias. The test voltage applied is dependent upon the product type. Before beginning the stress test, all sample devices are tested for functionality. The devices are then stressed for 1,008 hours in 504-hour intervals and are retested for functionality after each interval.

Temperature Cycle (TC)

The temperature cycle test accelerates package defects that are sensitive to thermomechanical stress. All sample devices are tested for functionality before the stress test begins. During temperature cycling, the sample devices are alternately subjected to extremely low and then extremely high temperatures. Depending upon the device and package type, the test conditions are -65°C for 15 minutes and 150°C for 15 minutes or -40°C for 15 minutes and 85°C for 15 minutes. The devices are exposed to a maximum of 1,000 of these 30-minute cycles in 250-cycle intervals and are retested for functionality after each interval.

Thermal Shock (TS)

Like temperature cycle, thermal shock is used to test package integrity under thermomechanical stress. Die attach and wire bond defects, as well as package cracks, are accelerated by the test conditions. All sample devices are tested for functionality before the stress test begins. During thermal shock, sample devices are alternately submerged in liquid at -55°C for 5 minutes and at +125°C for 5 minutes. The devices are exposed to a maximum of 700 of these 10-minute cycles in 350-cycle intervals. Devices are retested for functionality after each interval.

High Temperature Storage (HTS)

The high temperature storage test, which is conducted at 150°C (no bias), accelerates mechanical package stresses and assembly defects. Before beginning the stress test, all sample devices are tested for functionality. Sample devices are then stressed for 1,008 hours in 504-hour intervals and are retested for functionality after each interval.

Data Retention Bake (DRB)

The data retention bake test is conducted at 150°C (no bias). This test evaluates the data retention characteristics of the devices at high temperatures. Before beginning the stress test, all sample devices are tested for functionality. Sample devices are programmed for solid zeros and then baked. The devices are then stressed for 1,008 hours in 168-hour intervals. They are tested for parametric and data integrity after each interval and for functionality after the final interval.

Program and Erase Cycling

Program and erase cycling is conducted at 0°C or 70°C, 3V Vcc/4.7V VPP or 5.5V Vcc/12.6V VPP, depending upon product type. The test evaluates cell gate oxide endurance. Before cycling, the sample devices are evaluated at 0°C and 70°C for speed programming, erase, and read performance. Devices are then block-cycled (programmed and erased) one thousand, ten thousand or one hundred thousand times using solid zeros and ones patterns. Devices are tested for data sheet functionality after cycling is complete.

Electrostatic Discharge (ESD)

Micron's ESD test circuit setup and waveforms are in accordance with MIL-STD-883, test method 3015 and JESD22-A114A requirements. ESD qualification consists of three tests. In the first test, each pin is pulsed with respect to Vss, with all other pins floating. This is followed by a second test in which each pin is pulsed with respect to Vcc(s) and Vss(s), with all other pins floating. In the third test, each pin is pulsed with all other pins tied together. In each of the three tests, pins are pulsed six times at each voltage level: three pulses at the positive polarity and then three pulses at the negative polarity.

A Micron device undergoes all three tests at one voltage. It is then evaluated for functionality and leakage. If the device passes both functionality and leakage, it is returned to the ESD tester and the voltage is increased by one step (500V). All three tests are repeated, followed again by the electrical tests. This continues until the device fails either functionality or leakage requirements. When the device fails, it is considered qualified through the last voltage step at which it passed both functionality and leakage requirements.

Soft Error

A soft error occurs when a device fails to retain data, yet performs to all specifications when rechecked after the failure. Sample devices are tested for soft errors using Micron's AMBYX TBT32000 test system. The test is conducted with a 1ms refresh period and checkerboard/checkerboard complement test patterns. The test voltage applied is dependent upon the product type. Any degradation in refresh performance that would appear as a soft error is ruled out by testing the device before and after the soft error rate test for more stringent refresh characteristics than required during the soft error test period.

Vcc Latch-Up

The purpose of the Vcc latch-up test is to determine the maximum voltage that a device can tolerate. For operating mode the test is conducted using an external power supply and an ammeter to monitor the Icc current. The device is exercised using READ-MODIFY-WRITE or WRITE-READ cycles (depending upon the product type) of 200ns with a row fast checkerboard pattern. All inputs and clocks are set at CMOS levels and Vcc is increased to progressively higher voltages until the device latches. The same procedure is used for standby as is used for operating mode, except that the device is not cycled. Vcc is increased until the device latches.

MODULE ENVIRONMENTAL PROCESS MONITOR (MEPM) PROGRAM

The purpose of the MEPM program is to ensure that the memory module assembly is reliable. Under this program, samples of Micron's various module products are subjected to visual inspection, electrical test and temperature cycling. Samples are pulled from finished goods inventory at each module manufacturing site and subjected to MEPM testing at Micron Technology, Inc., on a regular basis. Should any modules fail due to workmanship issues or device failure, the respective manufacturing site is notified and failure analysis is conducted to determine the cause of the failure.

Visual Inspection

Modules are inspected in accordance with the Class 2 requirements of IPC-A-610B, "Acceptability of Electronic Assemblies," for assembly workmanship. Mechanical inspection of critical dimensions (e.g., overall thickness, overall length, polarity notch dimensions, etc.) ensures compliance with Micron dimensional specifications (specification 685016, Printed Circuit Requirements).

Electrical Test

All test readouts are performed using product-specific QA test programs (parametric testing, including input and output leakage tests and full array functional testing under various conditions).

Temperature Cycle "C" (-65°C to 150°C)

Temperature cycle "C" consists of 25 cycles, each approximately 30 minutes in duration. The temperature is dropped from room temperature to -65°C at a ramp rate of 20°C per minute and stabilized at -60°C, with approximately 15 minutes dwell time. The temperature is then ramped from -65°C to 150°C at a ramp rate of 20°C per minute and stabilized at 150°C for approximately 15 minutes, before repeating the ramp down to -65°C. Functionality testing and visual inspection are performed upon completion of 25 cycles.

PC Boot-Up Test

Module samples are tested in motherboards to ensure proper boot-up and operation in typical PC applications.

AILURE RATE CALCULATION

The failure rate during the useful life of a device is expressed s either the percentage of failures per thousand device ours, or as failures in time, per billion device hours (FITs). sing Micron's 64Mb DRAM as an example, the failure rate calculated as follows:

$$\text{ailure Rate} = \frac{\text{Pn}}{\text{Device hours} \times \text{AF}}$$

here: Pn = Poisson Statistic (at a given confidence level). For the HTOL data presented, Pn = 6.292 at a 60 percent confidence level.

Device hours = Sample size multiplied by test time (in hours). From the table below, device hours equal:

$(2{,}439 \times 168) + (2{,}422 \times 168) + (981 \times 168) + (961 \times 168) + (961 \times 168) + (586 \times 168) = 1{,}402{,}800$ or 1.403×10^6

AF = Acceleration factor between the stress environment and typical use conditions. For the 64Mb DRAM, the acceleration factor between 125°C, 4.8V (HTOL stress conditions) and 50°C, 3.3V (typical operating conditions) equals 113. (Acceleration factor values vary with each product. An explanation of how this factor was calculated is provided in the following section.)

Thus, the failure rate of the Micron 64Mb DRAM family is computed as follows:

$$\text{Failure Rate} = \frac{6.292}{(1.403 \times 10^6)\,113} = 3.969 \times 10^{-8}$$

where: Total device hours at test conditions = 1.403×10^6. Equivalent device hours at typical use conditions (50°C, 3.3V Vcc) using an acceleration factor of 113 equal: $113\,(1.403 \times 10^6) = 159 \times 10^6$.

To state the failure rate in FITs, we multiply the failure rate obtained from the equation above by 10^9:

Failure Rate = $(3.969 \times 10^{-8}) \times 10^9 = 39.69$ or 40 FITs.

Table 2
DRAM HIGH TEMPERATURE OPERATING LIFE (HTOL)

Sample No.	168 Hours	336 Hours	504 Hours	672 Hours	840 Hours	1,008 Hours
1	1/0283	0/0279	0/0279	0/0270	0/0270	0/0270
2	0/0087	0/0086	0/0086	0/0085	0/0085	0/0085
3	0/0048	0/0048	0/0048	0/0048	0/0048	0/0048
4	0/0012	0/0012	0/0012	0/0012	0/0012	0/0012
5	0/0033	0/0033	0/0033	0/0033	0/0033	0/0033
6	0/0043	0/0043	0/0043	0/0043	0/0043	0/0043
7	0/0100	0/0097	0/0096	0/0095	0/0095	0/0095
8	2/0394	0/0387	0/0384	0/0375	0/0375	–
9	0/0647	1/0647	–	–	–	–
10	0/0249	0/0249	–	–	–	–
11	1/0307	0/0306	–	–	–	–
12	0/0236	0/0235	–	–	–	–
Total	4/2439	1/2422	0/0981	0/0961	0/0961	0/0586

ACCELERATION FACTOR CALCULATION

Again, using the 64Mb DRAM as our example, the acceleration factor between HTOL stress conditions (125°C, 4.8V) and typical operating conditions (50°C, 3.3V) is computed using the following models:

ACCELERATION FACTOR DUE TO TEMPERATURE STRESS

The acceleration factor due to temperature stress is computed using the Arrhenius equation, which is stated as follows:

$$AF_T = e^{\frac{E_a}{k}\left[\frac{1}{T_O} - \frac{1}{T_S}\right]}$$

where: k = Boltzmann's constant, which is equal to 8.617×10^{-5} eV/K.

T_O and T_S = Typical operating and stress temperatures, respectively, in degrees Kelvin.

E = Activation energy in eV. For oxide defects, which is the most common failure mechanism for the 64Mb DRAM used in our example, the activation energy is determined to be 0.3eV.*

Using these values, the temperature acceleration factor between 125°C and 50°C is computed to be 7.62.

ACCELERATION FACTOR DUE TO VOLTAGE STRESS**

The acceleration factor due to voltage stress is computed using the following model:

$$AF_V = e^{\beta (V_S - V_O)}$$

where:

V_S and V_O = Stress voltage and typical operating voltage, respectively, in volts

β = Constant, the value of which was derived experimentally (for the 64Mb DRAM used in our example, β equals 3***).

Thus, the voltage acceleration factor for the 64Mb DRAM between 3.5V (internal voltage under 4.8V stress conditions) and 2.6V (internal voltage under typical operating conditions) is computed to be 14.880.

Finally, the overall acceleration factor due to temperature and voltage stress is calculated as the product of the two respective acceleration factors or:

$$\begin{aligned} AF_{overall} &= AF_{temperature} \times AF_{voltage} \\ &= 7.62 \times 14.880 \\ &= 113 \end{aligned}$$

---

* Flash products use temperature stress to accelerate single-bit charge loss. The industry-accepted activation energy for this failure mechanism is 0.6eV.

** Acceleration factors used to calculate failure rates for noncharge loss failures in Flash products are based on both temperature and voltage stress, similar to the example provided here. However, failure rates for single-bit charge loss are calculated using acceleration factors based on thermal stress only.

***For Micron's Flash products, $\beta = 2$.

OUTGOING PRODUCT QUALITY

Before being sent to our finished goods area, where products are prepared for shipping, a special unit within the Quality Assurance Department samples the production population according to a sampling plan. These samples are subjected to visual and electrical testing to measure the acceptable quality level (AQL) of all outgoing product. Test flows for new products that have not met required production volume are more comprehensive than for mature products. Over a period of time, as a product matures, the objective is to eliminate those tests that devices never fail. The AQL test flow, although it is performed on only a small percentage of each product, is much more exhaustive. Conducted at spec conditions using a wide range of test algorithms and data background, the AQL test flow validates the effectiveness of the production test flow. Its purpose is to detect subtle shifts in defect mechanisms that the production test flow may not catch.

Visual testing for mechanical defects consists of visual inspection of the sample devices for any physical irregularities that could negatively affect device performance. If a sample device is found to have, for example, a bent lead, a package irregularity or excess solder, the entire lot is returned to our test area for a 100 percent visual inspection.

Electrical testing of the sample devices is performed using automatic test equipment (ATE) systems. Testing is conducted at 0°C and at 70°C. Should an electrical failure occur, a quality assurance engineer further evaluates the failing device. After completing this analysis, the quality assurance engineer determines which production monitor/ test should have caught the failure, and corrective action is implemented. These steps are important in preserving the integrity of our test process.

AUTOMATED DATA CAPTURE AND ANALYSIS

Micron has developed a sophisticated data capture and analysis system with a computer network tailored to the needs of quality IC manufacturing. Figure 3 shows the primary components for our distributed computing environment.

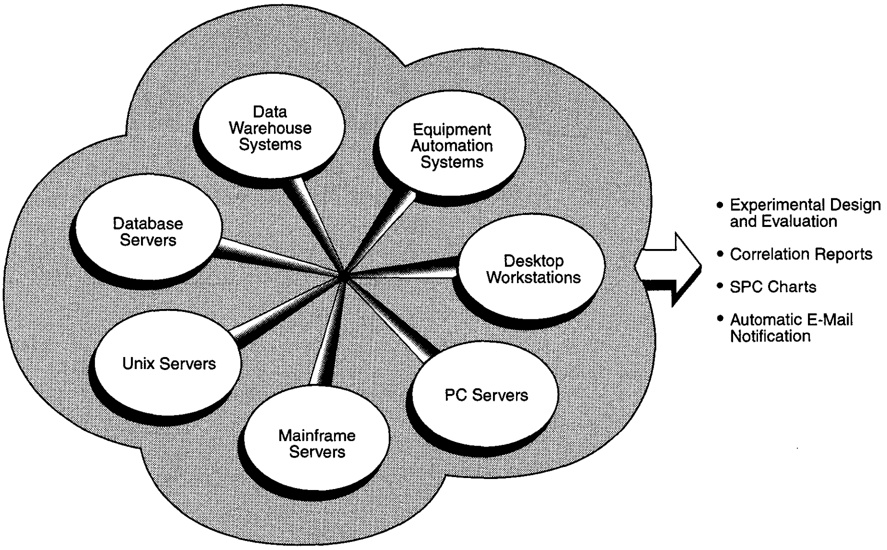


Figure 3
MICRON'S DISTRIBUTED COMPUTING ENVIRONMENT

DATA CAPTURE

Automated, real-time data capture makes real-time charting (X-bar and R charts, etc.) of all critical operations and processes possible and ensures that appropriate personnel know of any unexpected variation in a timely manner. As production lots move through each manufacturing step, detailed information (including step number, lot number, machine number, date/time, and operator number) is entered into the production database. Automated, highly-programmable measurement systems capture a host of parameters associated with equipment, on-line process material and environmental variables.

STATISTICAL TECHNIQUES AND TOOLS

By using highly flexible, on-line data extraction programs, system users can tap this vast database and design their own correlation and trend analyses. Because we can correlate process variables to product performance, we can make online projections of the quality of our finished product for a given lot or process run. In addition, we can estimate the impact of process improvements on quality well in advance and can make the impact of process deviations more visible to our engineers. This approach allows us to model yield and quality parameters based on on-line parameters. We can then use the model to predict the final product results through the following means.

GROUP SUMMARIES

Summaries, which provide the means and standard deviations of user-defined parametrics, enable system users to compare the parametric values of production lots as well as special engineering lots.

TREND ANALYSIS

Trend charts are routinely generated for critical parameters. System users can plot the means and ranges of any probe or parametric data captured throughout the manufacturing process.

STATISTICAL PROCESS CONTROL (SPC) CHARTS

Micron employs SPC control charts throughout the company to monitor and evaluate critical process parameters, such as critical dimensions (CDs), film thickness, particle counts, temperature and humidity, and many other critical process and product quality parameters.

OVERLAYS OR WAFER MAPS

Maps, which are produced for all wafers during probe, show various parameters as a function of position on the wafer and are very useful for problem isolation. Maps may be analyzed individually or in groups. For example, wafers from an entire lot may be analyzed in relation to one particular parameter.

MULTIPLE REGRESSION

Multiple regression allows us to determine complex relationships between processing parameters and product quality. Using multiple regression analysis we are able to predict, for example, the relationship between interrelated processing steps (such as photo mask size, implant dose, and etch time) and device speed.

GAUGE CAPABILITY STUDIES

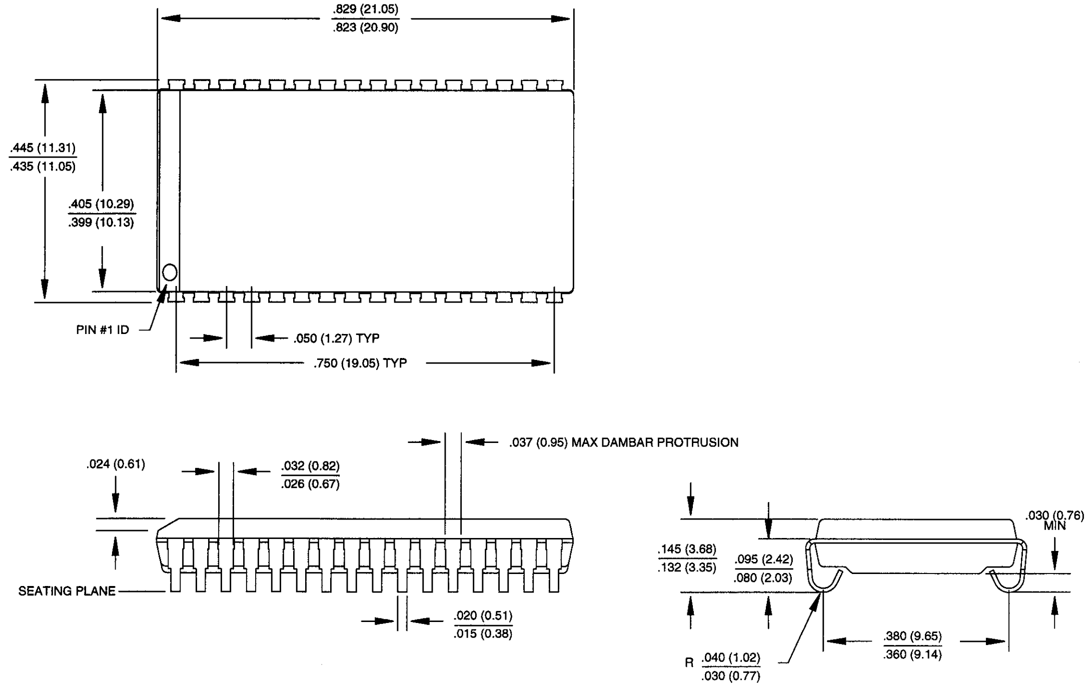
These studies, performed on both new and existing equipment, help us to determine the amount of variation in a measurement system.

COMPONENT PACKAGE SELECTION GUIDE

PACKAGE TYPE	REFERENCE CODE	PIN/BUMP COUNT	DIMENSION	PAGE
PLASTIC SOJ				
	A-1	32	400 mil	6-1
PLASTIC SOP				
	B-1	44	600 mil	6-2
PLASTIC TSOP				
	C-1	32	400 mil	6-3
	C-2	40	10mm x 20mm	6-4
	C-3	48	12mm x 20mm	6-5
	C-4	50	400 mil	6-6
	C-5	54	400 mil	6-7
	C-6	66	400 mil	6-8
	C-7	86	400 mil	6-9
PLASTIC TQFP				
	D-1	100	14mm x 20mm	6-10
PLASTIC FBGA				
	E-1	48	7mm x 12mm	6-11
PLASTIC BGA				
	F-1	119	14mm x 22mm	6-12
COMPACT FLASH CARD				
	G-1			6-13

32-PIN PLASTIC SOJ (400 mil)

A-1

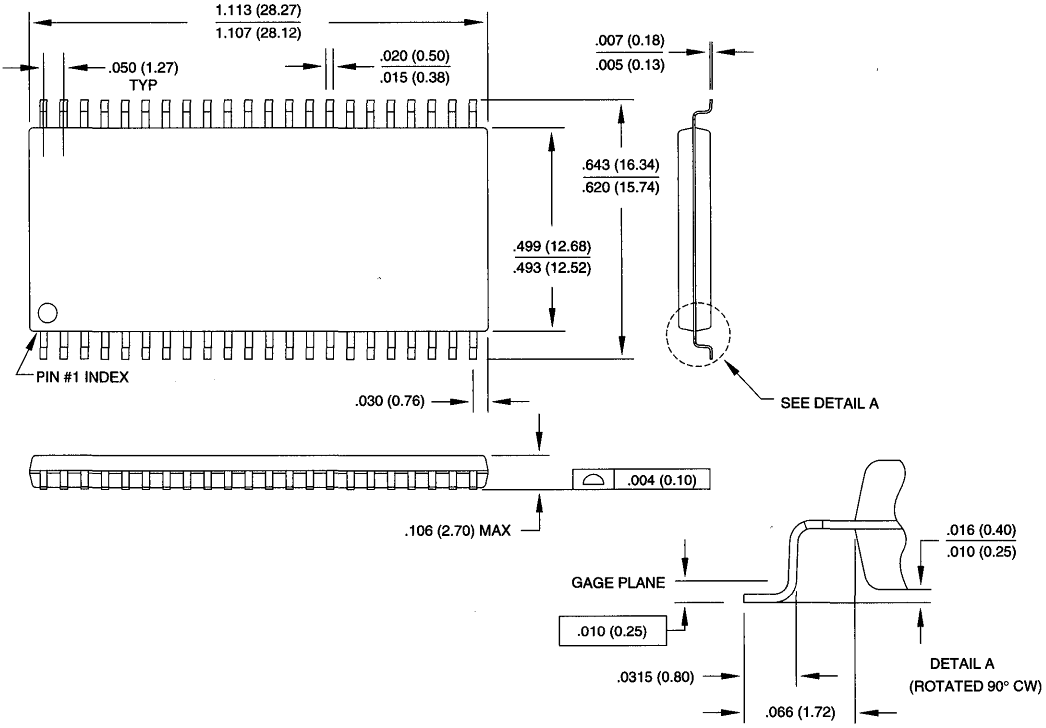


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

44-PIN PLASTIC SOP (600 mil)

B-1

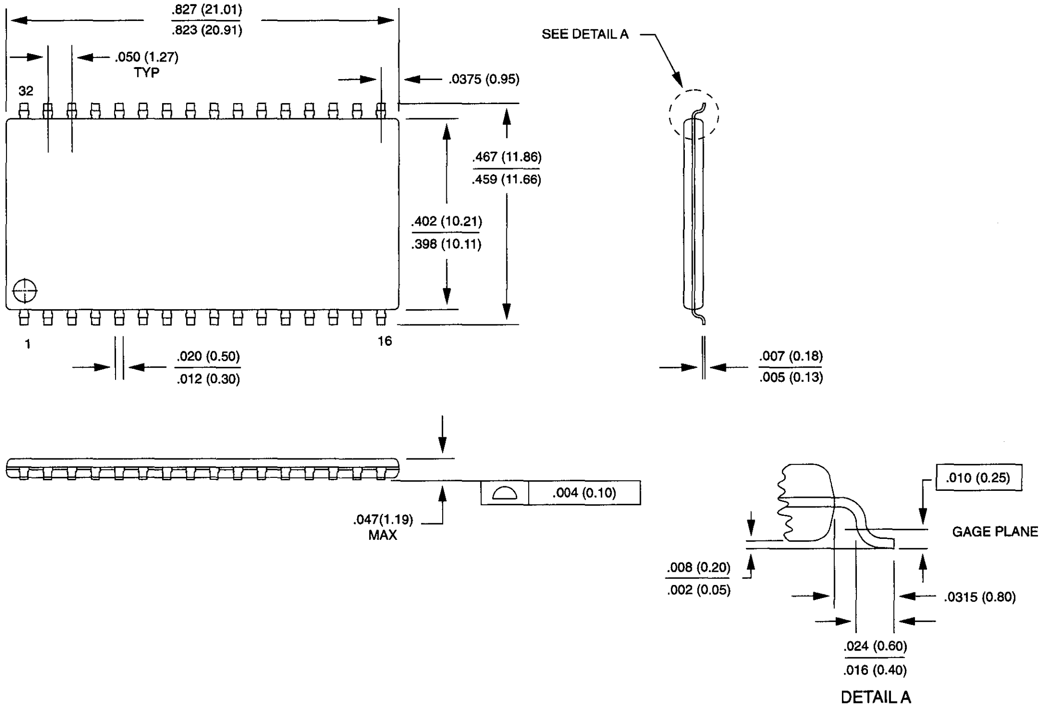


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01” per side.

32-PIN PLASTIC TSOP (400 mil)

C-1

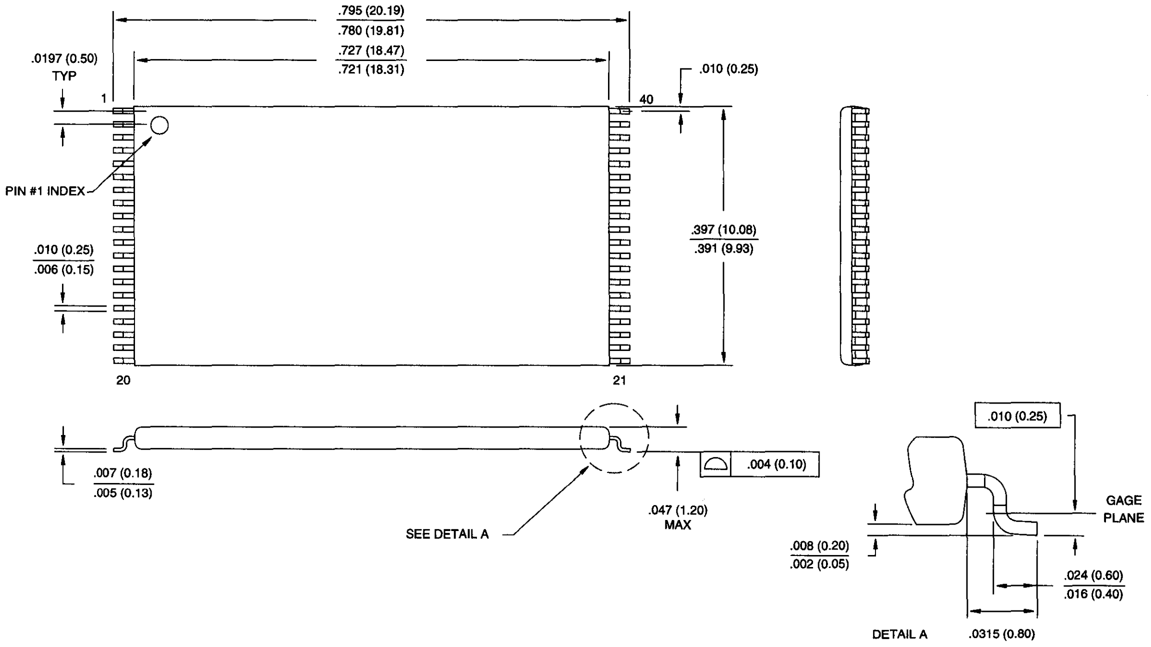


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

40-PIN PLASTIC TSOP I (10mm x 20mm)

C-2

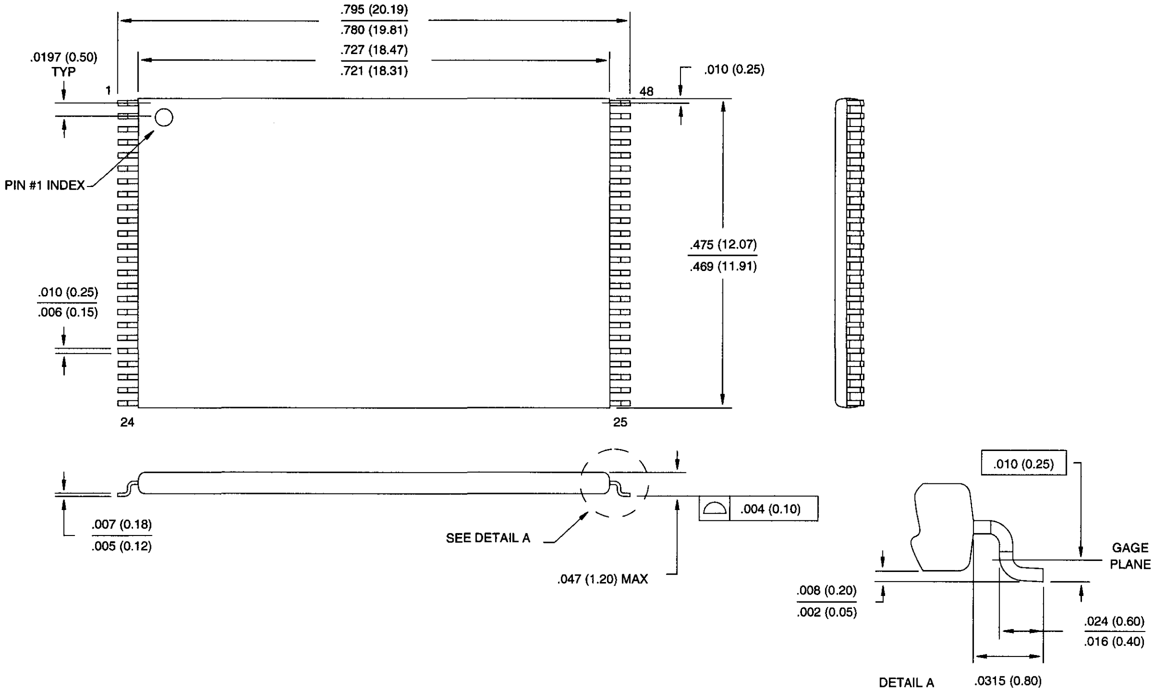


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

48-PIN PLASTIC TSOP I (12mm x 20mm)

C-3

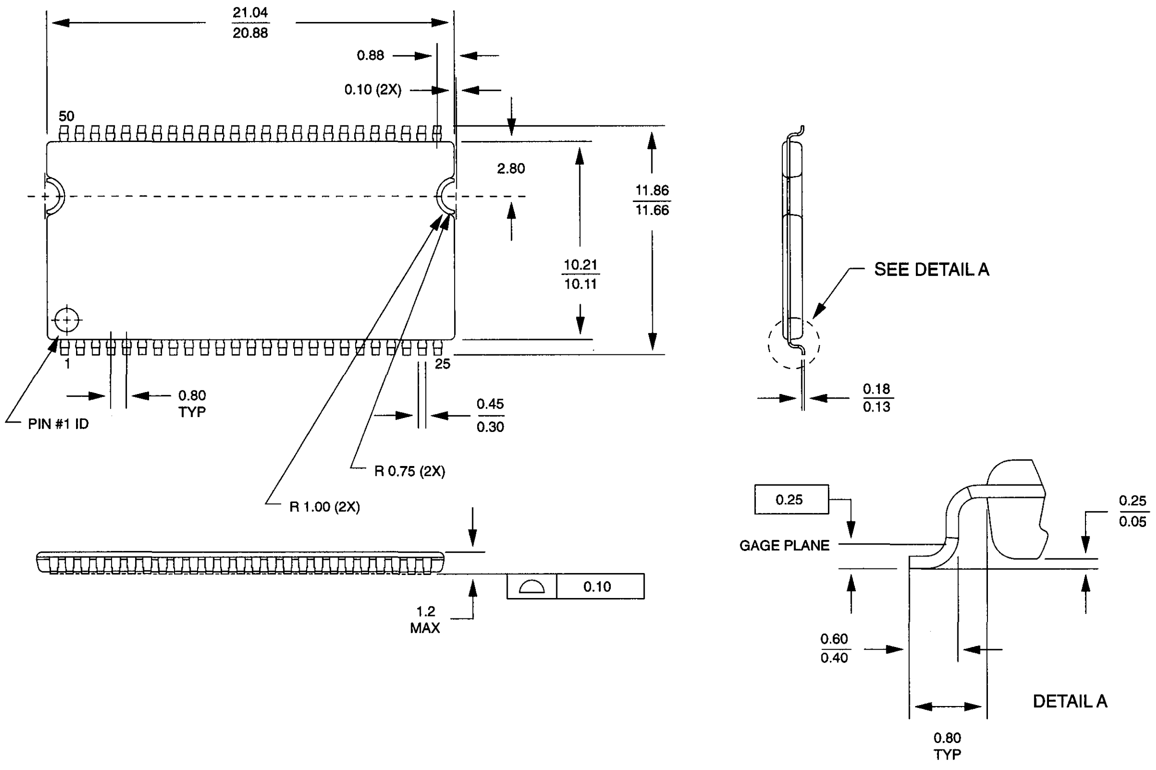


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

50-PIN PLASTIC TSOP (400 mil)

C-4

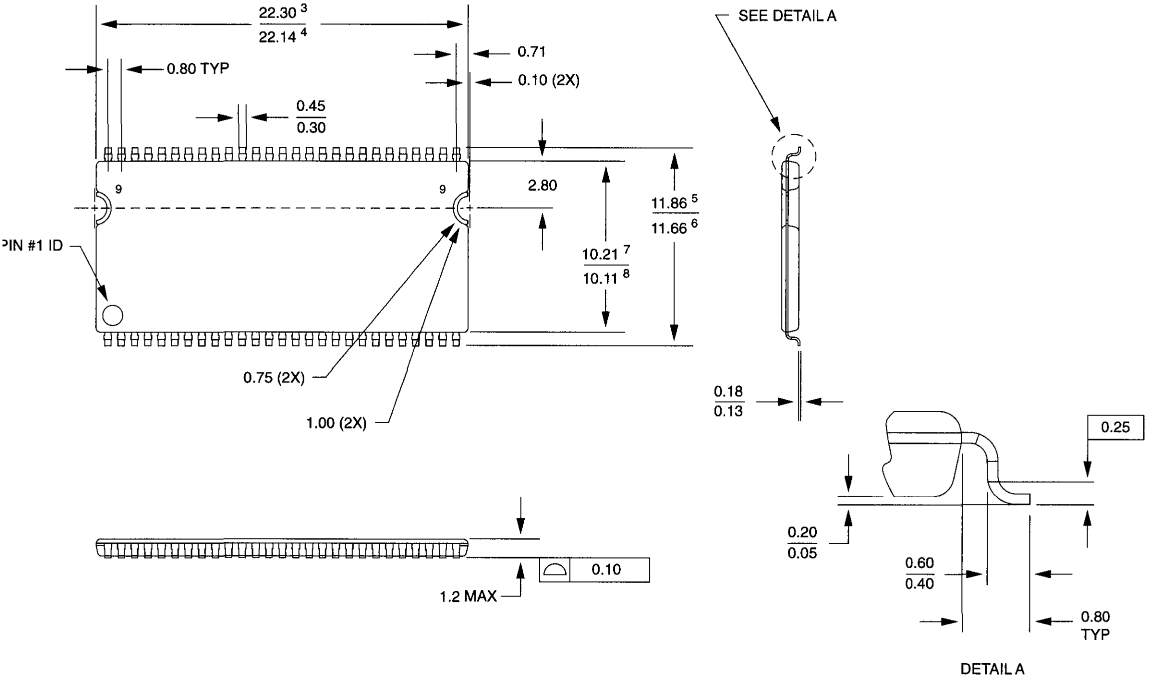


NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

54-PIN PLASTIC TSOP (400 mil)

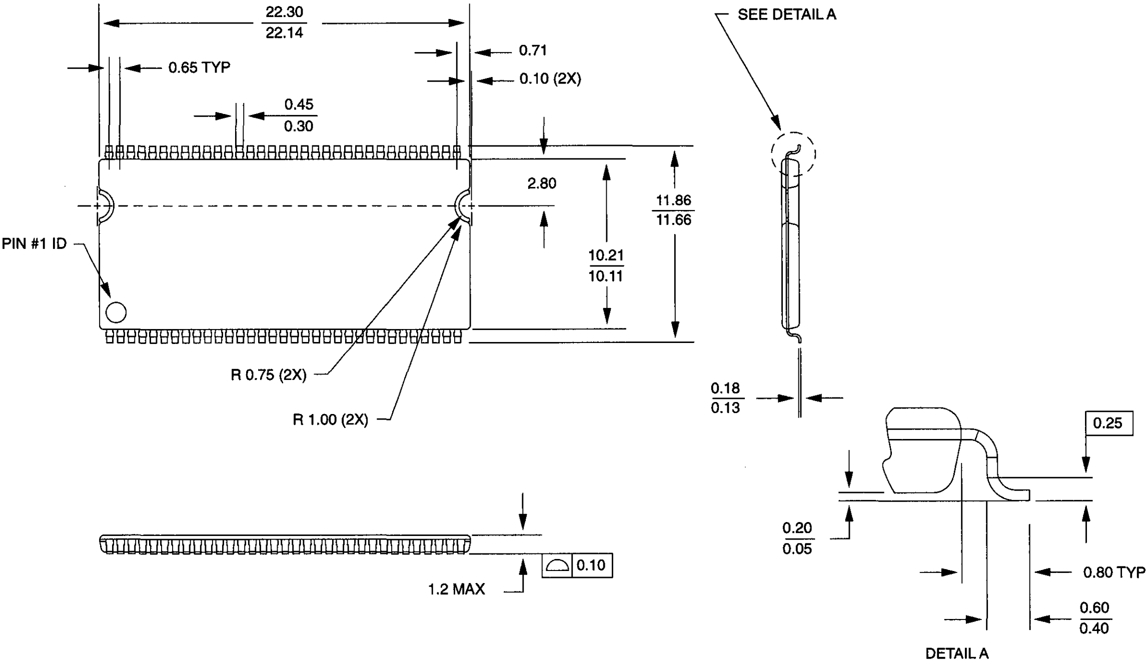
C-5



NOTE:
1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.
3. 22.35mm for some versions.
4. 22.09mm for some versions.
5. 11.96mm for some versions.
6. 11.56mm for some versions.
7. 10.29mm for some versions.
8. 10.03mm for some versions.
9. Notch is optional.

66-PIN PLASTIC TSOP (400 mil)

C-6

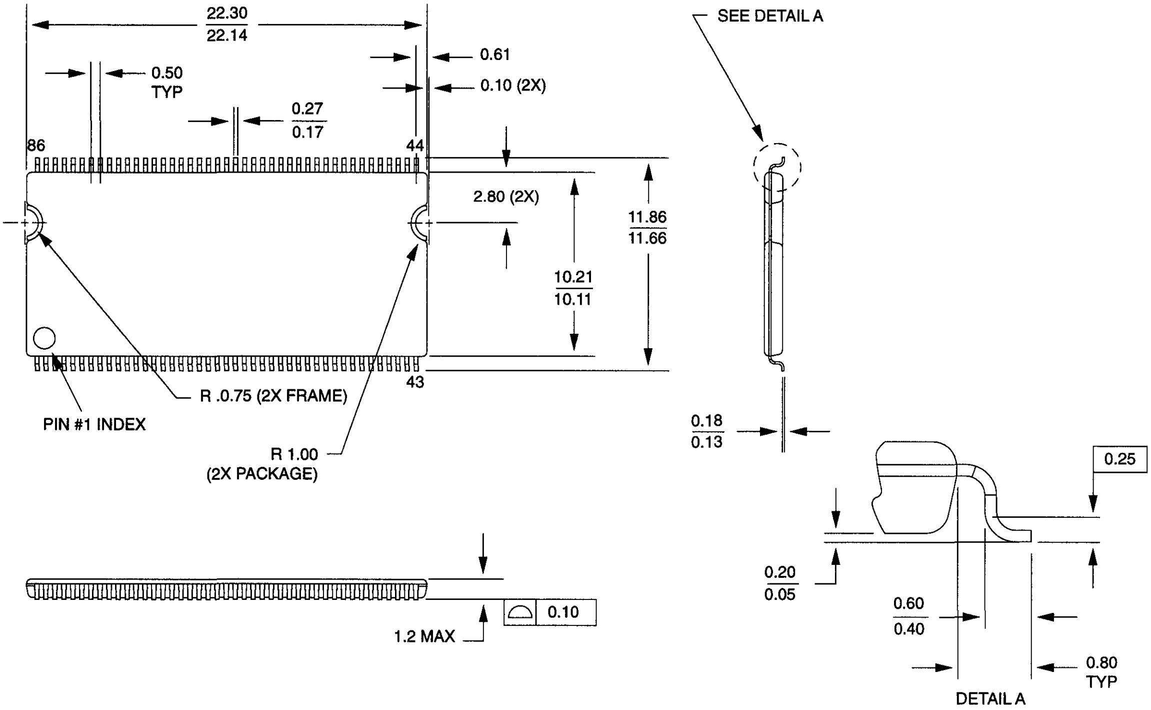


NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

86-PIN PLASTIC TSOP (400 mil)

C-7

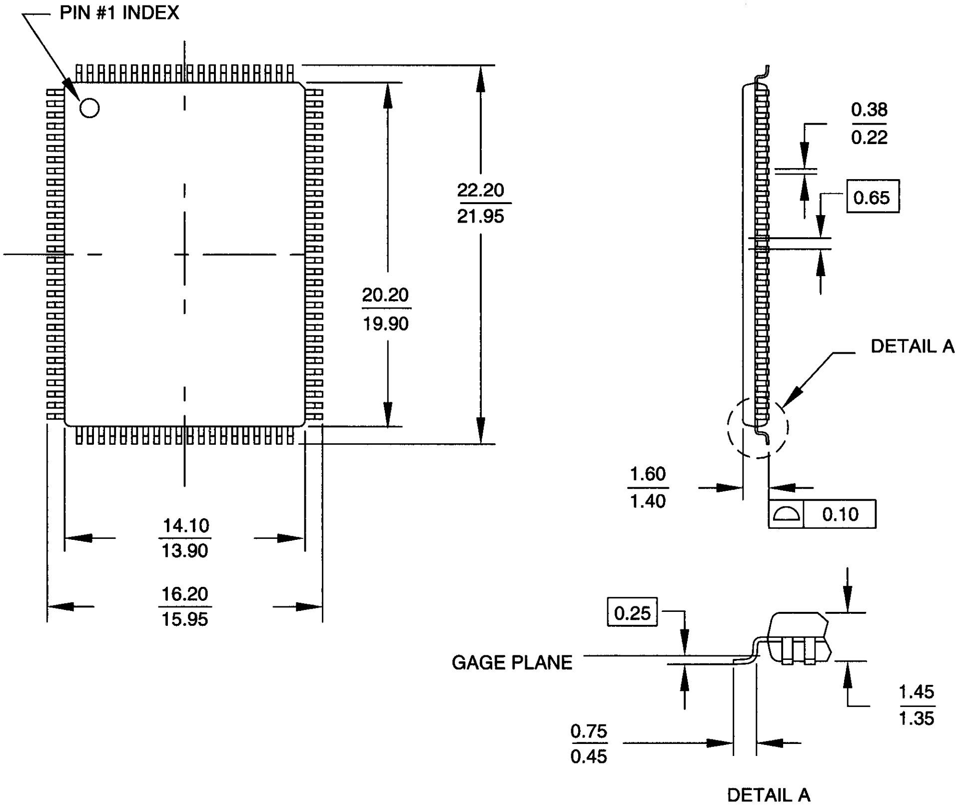


NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

100-PIN PLASTIC TQFP (JEDEC LQFP)

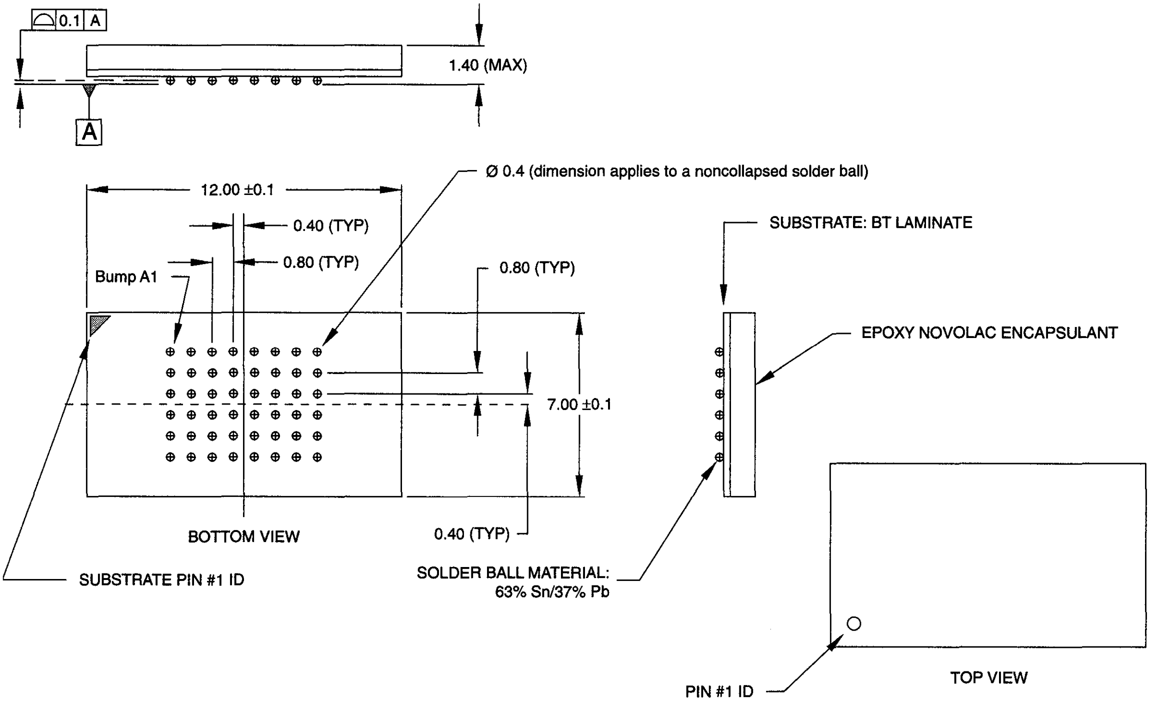
D-1



NOTE:
1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

48-BUMP FBGA

E-1

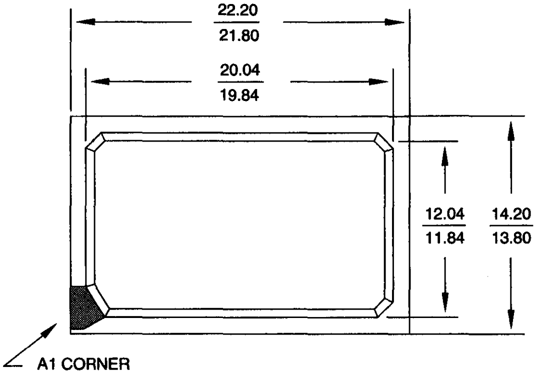


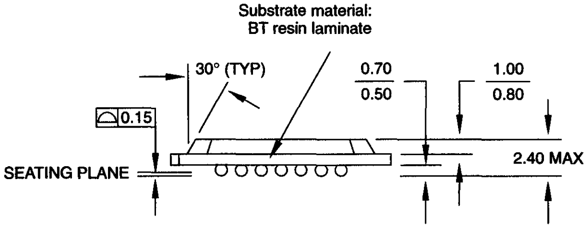
NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

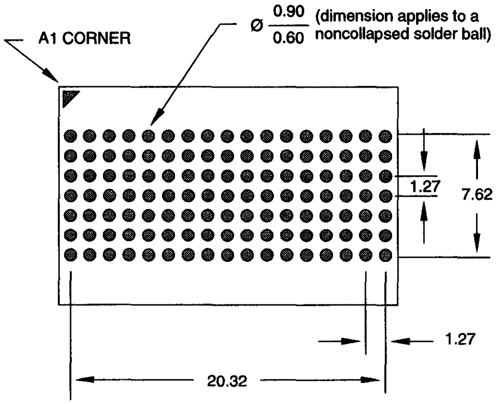
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.01" per side.
3. Solder ball land pad is 0.3mm.

119-BUMP BGA

F-1





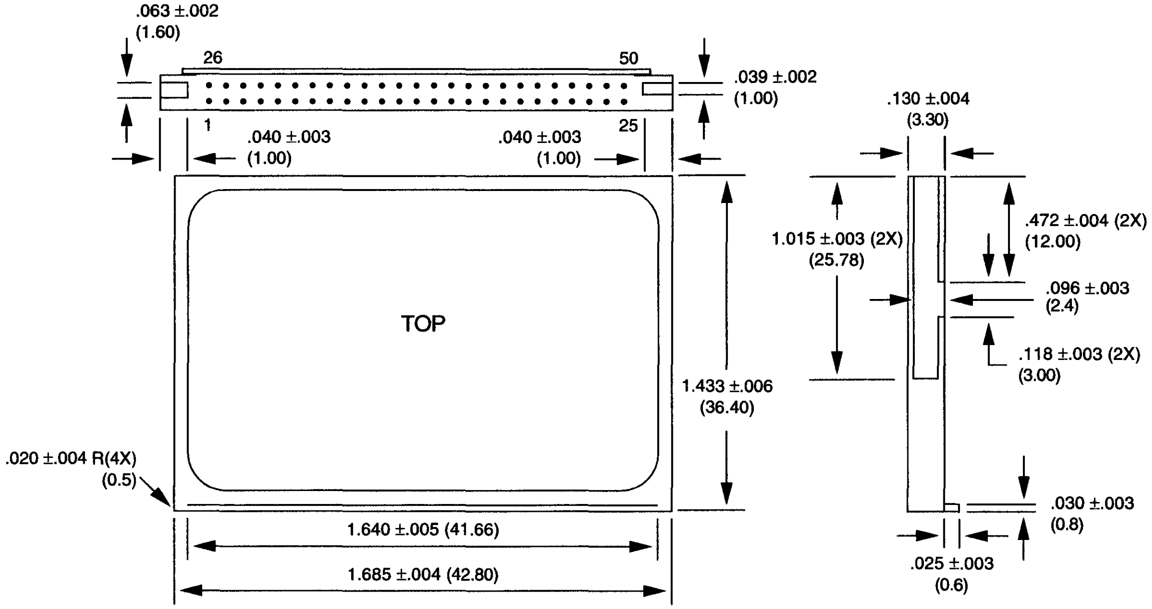


NOTE:

1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.01" per side.
3. Solder ball land pad is 0.6mm.

COMPACTFLASH CARD

G-1



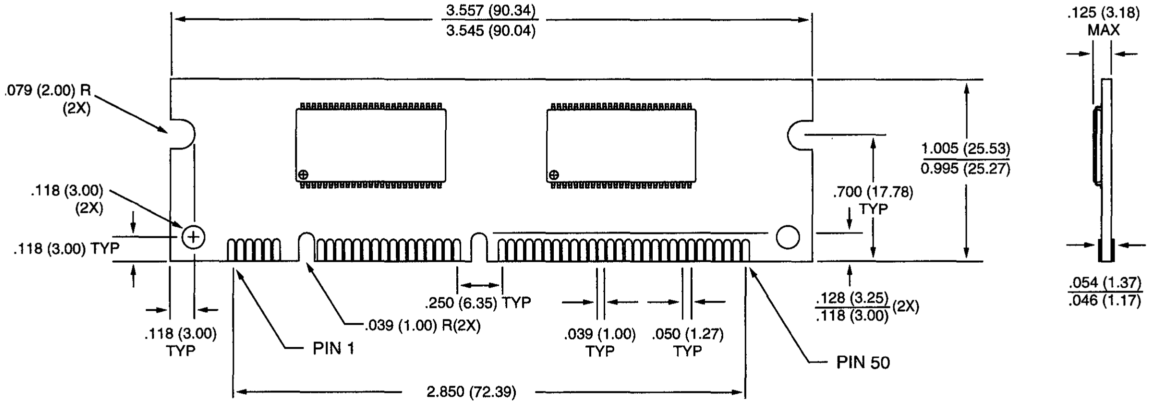
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

MODULE PACKAGE SELECTION GUIDE

PACKAGE TYPE	REFERENCE CODE	PIN COUNT	HEIGHT	PAGE
MODULE – DIMM				
	H-1 to H-6	100	1.0"	6-15
	H-7	100	1.15"	6-18
	H-8 to H-11	168	1.0"	6-18
	H-12 to H-14	168	1.1"	6-20
	H-15 to H-19	168	1.25"	6-22
	H-20	168	1.35"	6-24
	H-21 to H-24	168	1.375"	6-25
	H-25 to H-26	168	1.5"	6-27
	H-27	168	1.7"	6-29
	H-28 to H-32	168	2.0"	6-30
MODULE – SODIMM				
	I-1 to I-4	144	1.0"	6-33
	I-5	144	1.05"	6-35
	I-6 to I-8	144	1.15"	6-35
	I-9	144	1.25"	6-37

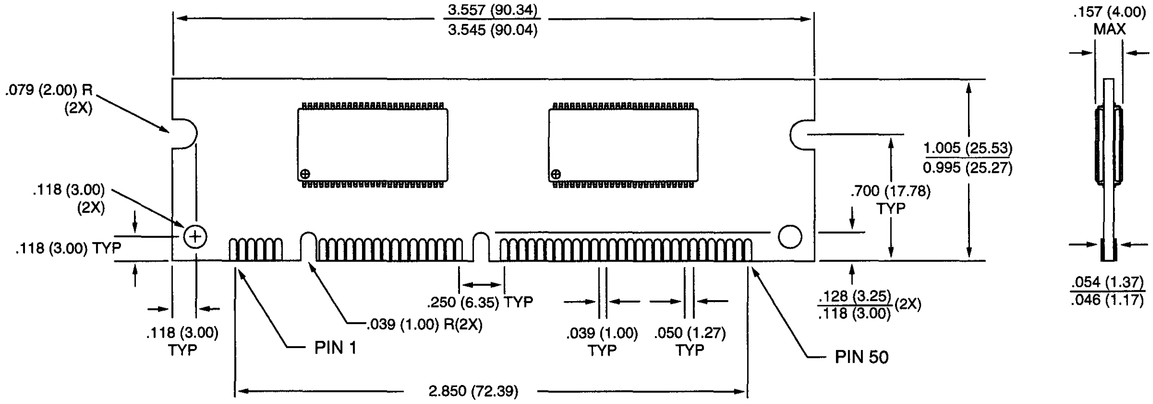
100-PIN DIMM

H-1



100-PIN DIMM

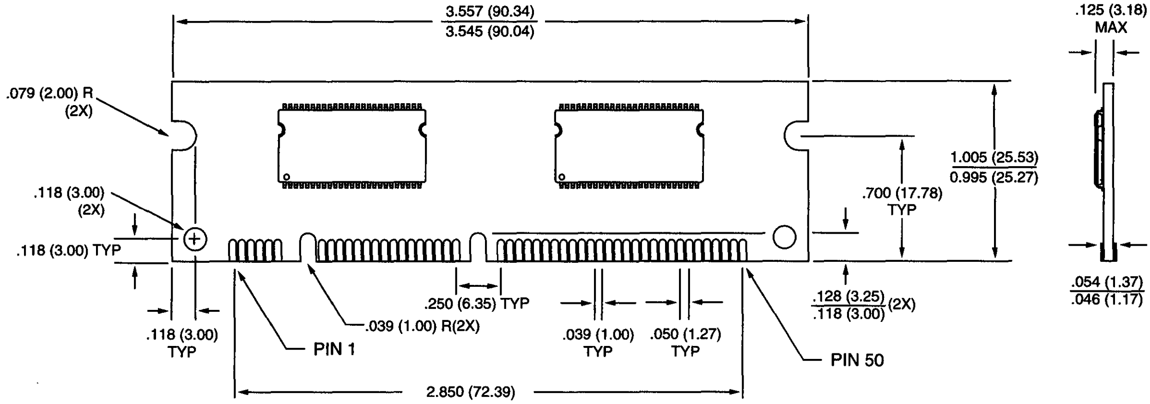
H-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

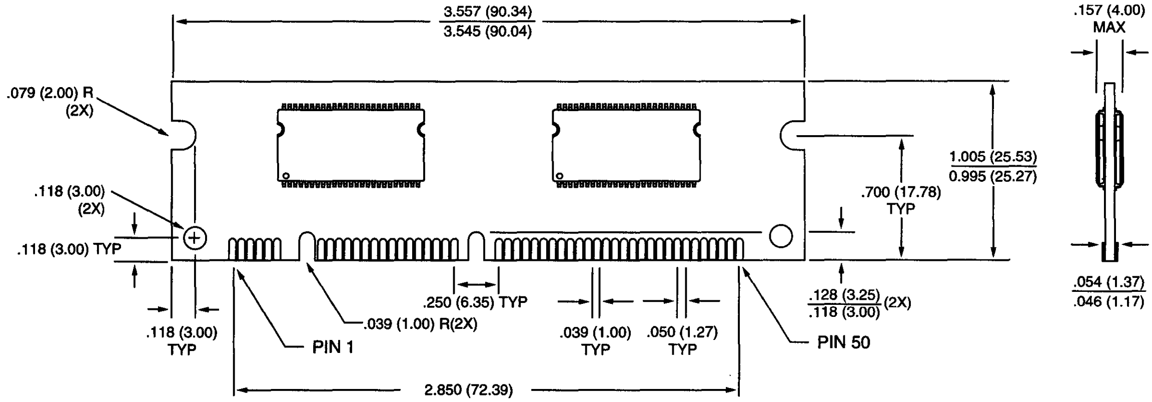
100-PIN DIMM

H-3



100-PIN DIMM

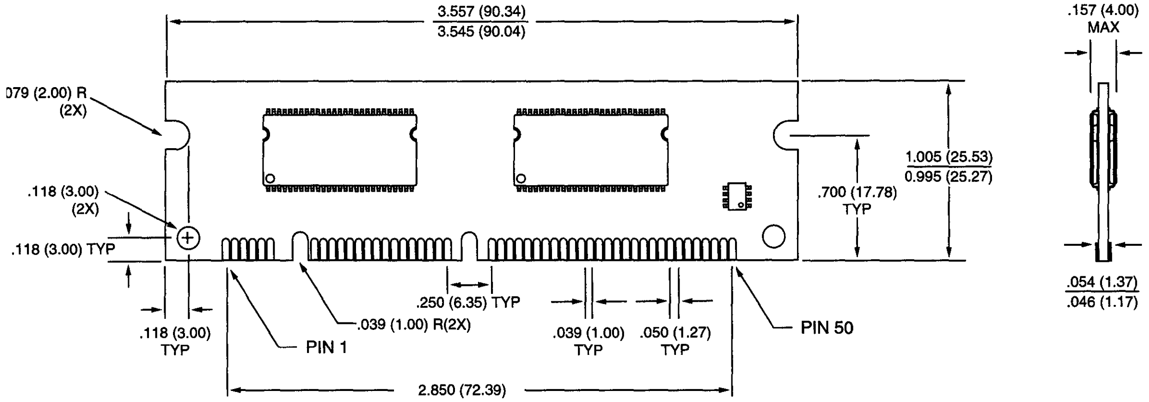
H-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

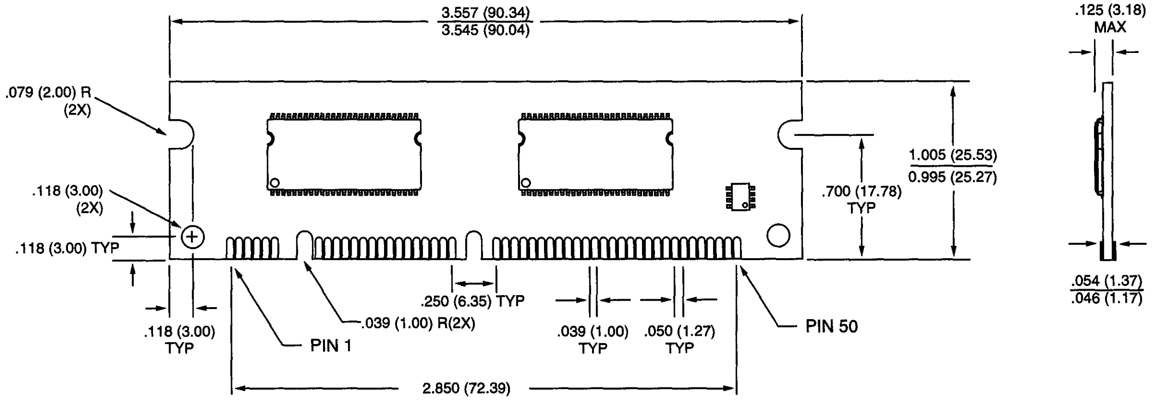
100-PIN DIMM

H-5



100-PIN DIMM

H-6

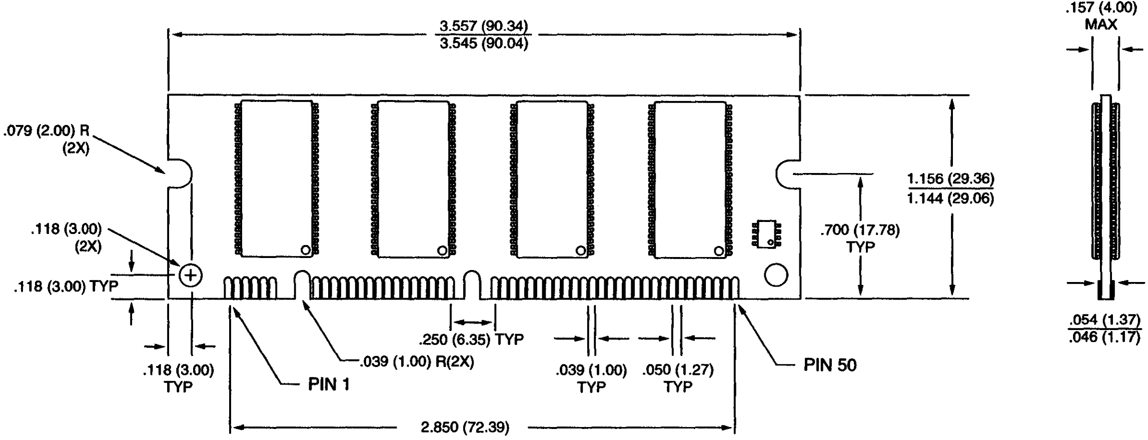


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

100-PIN DIMM

H-7

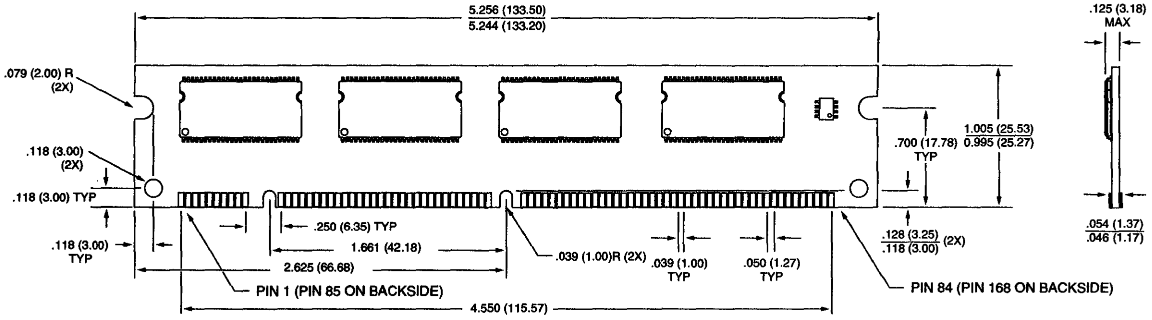
FRONT VIEW



168-PIN DIMM

H-8

FRONT VIEW

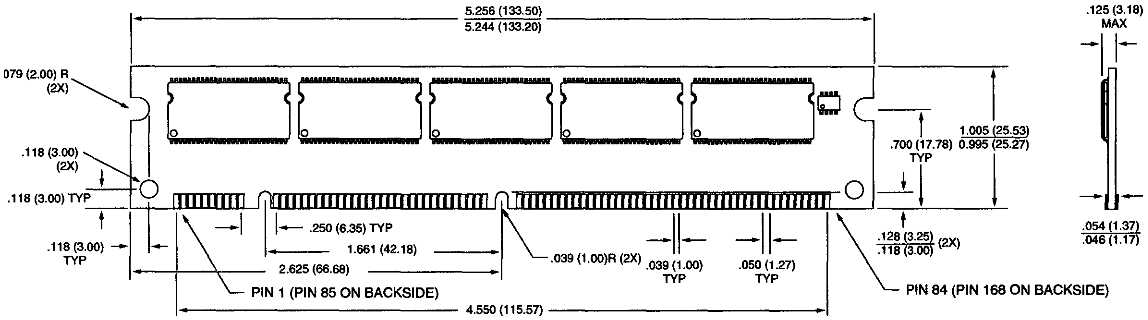


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

168-PIN DIMM

H-9

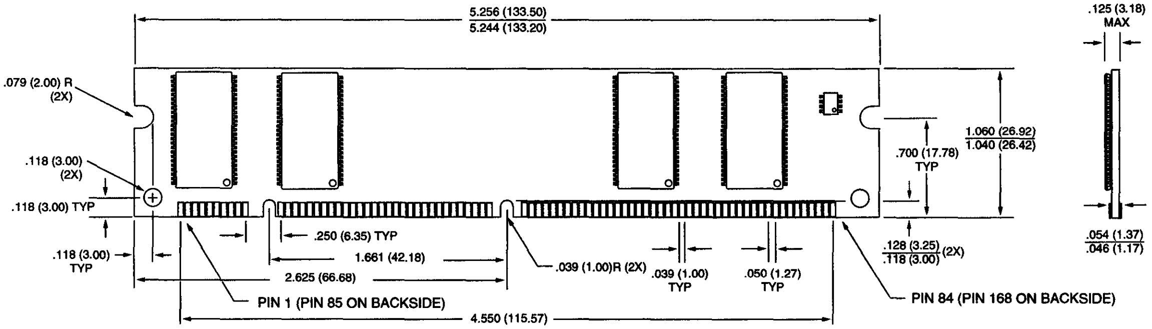
FRONT VIEW



168-PIN DIMM

H-10

FRONT VIEW

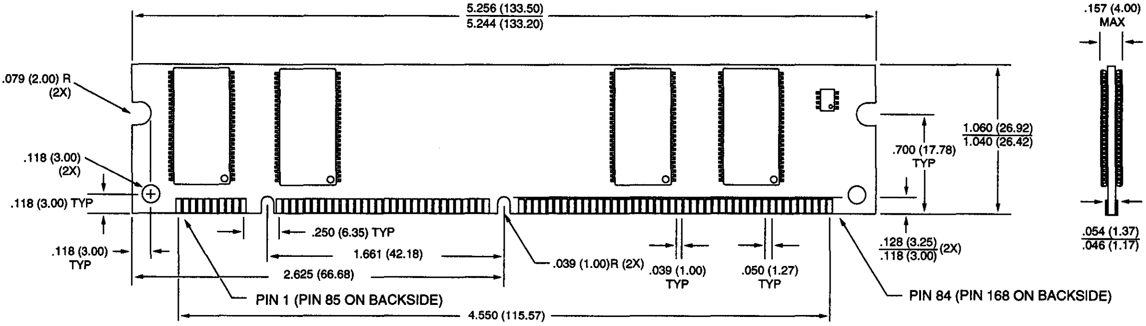


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

168-PIN DIMM

H-11

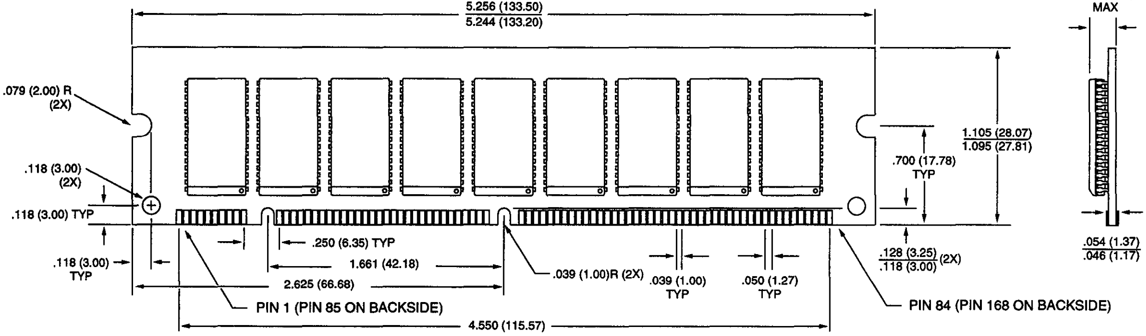
FRONT VIEW



168-PIN DIMM

H-12

FRONT VIEW

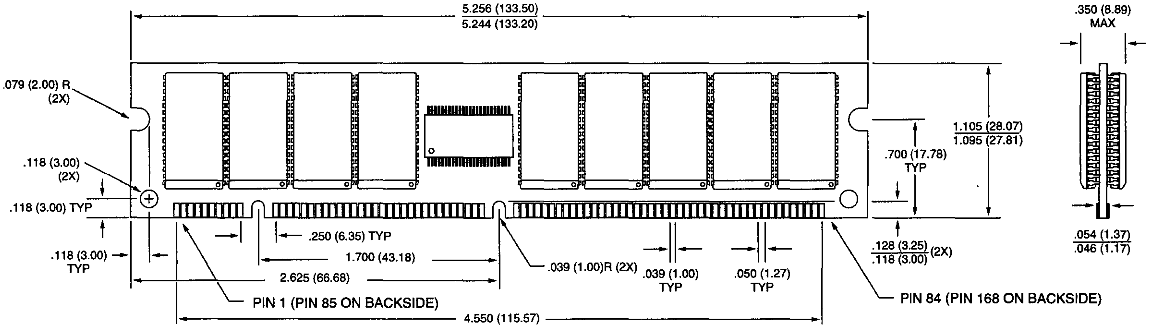


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

168-PIN DIMM

H-13

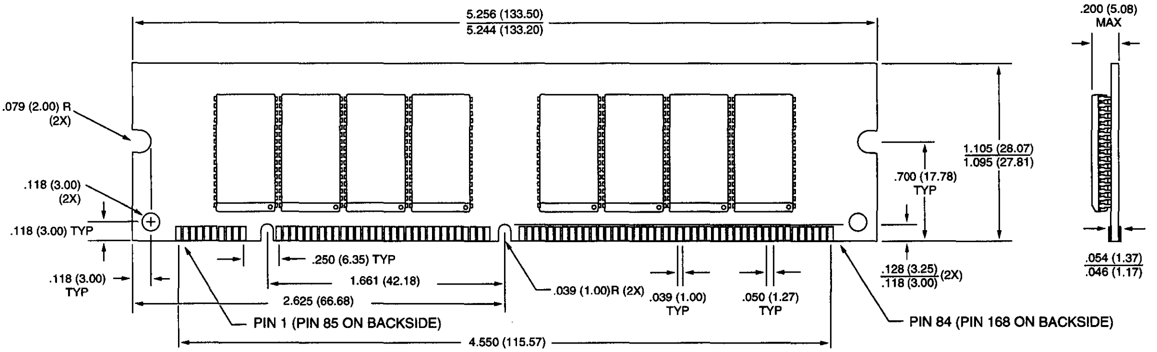
FRONT VIEW



168-PIN DIMM

H-14

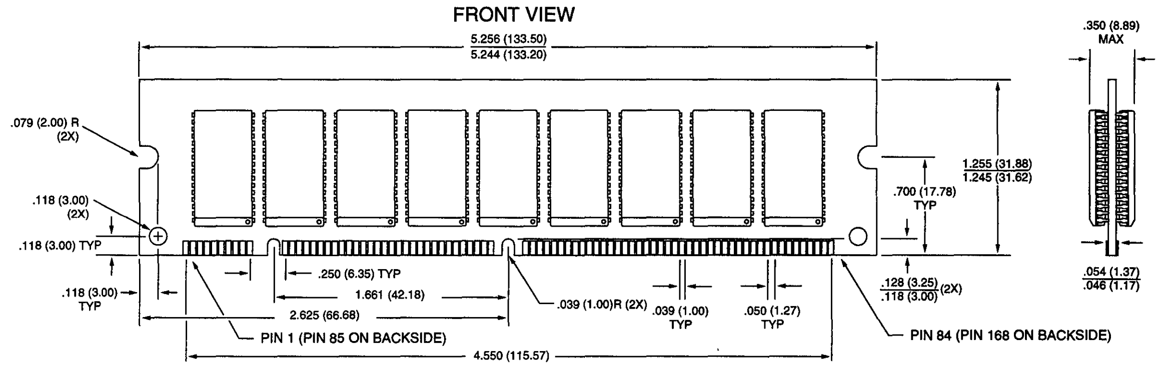
FRONT VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

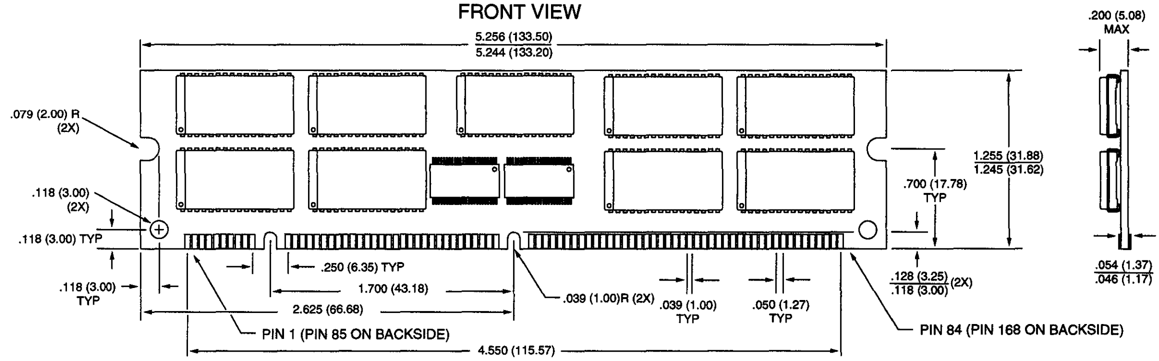
168-PIN DIMM

H-15



168-PIN DIMM

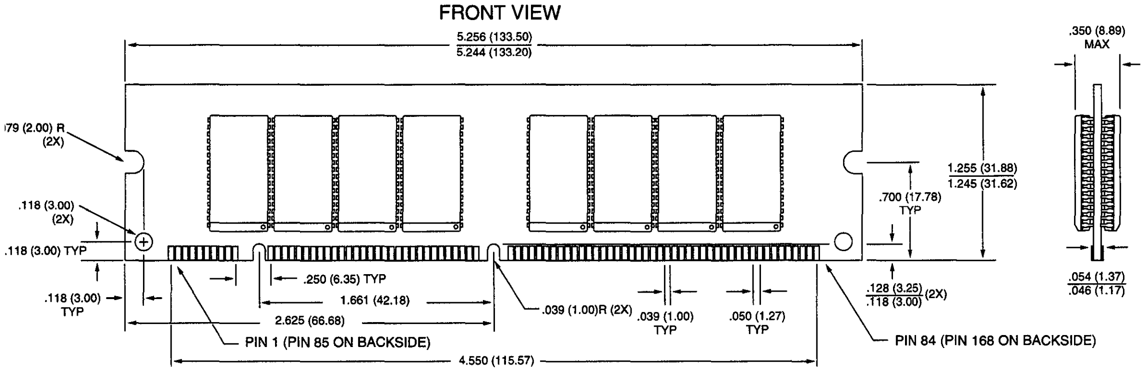
H-16



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

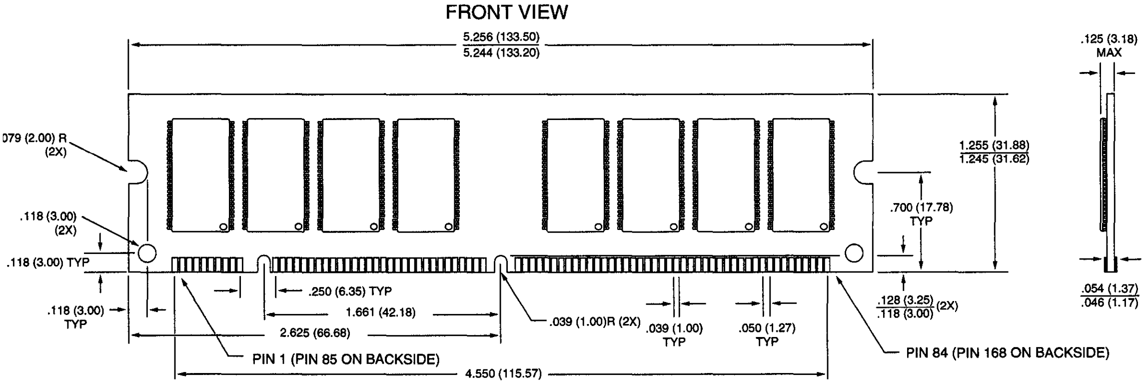
168-PIN DIMM

H-17



168-PIN DIMM

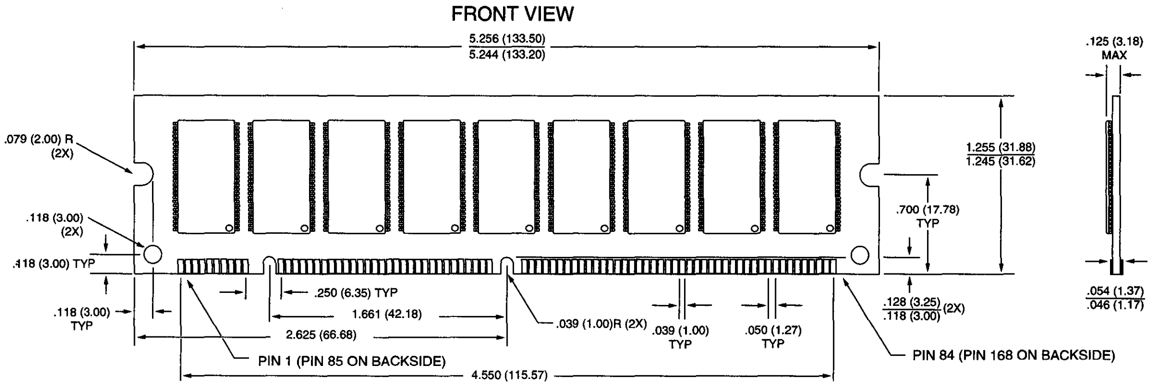
H-18



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

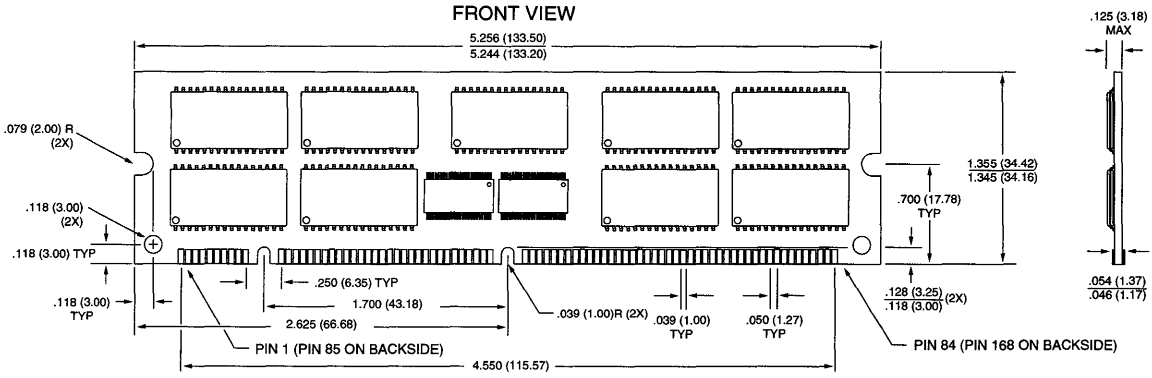
168-PIN DIMM

H-19



168-PIN DIMM

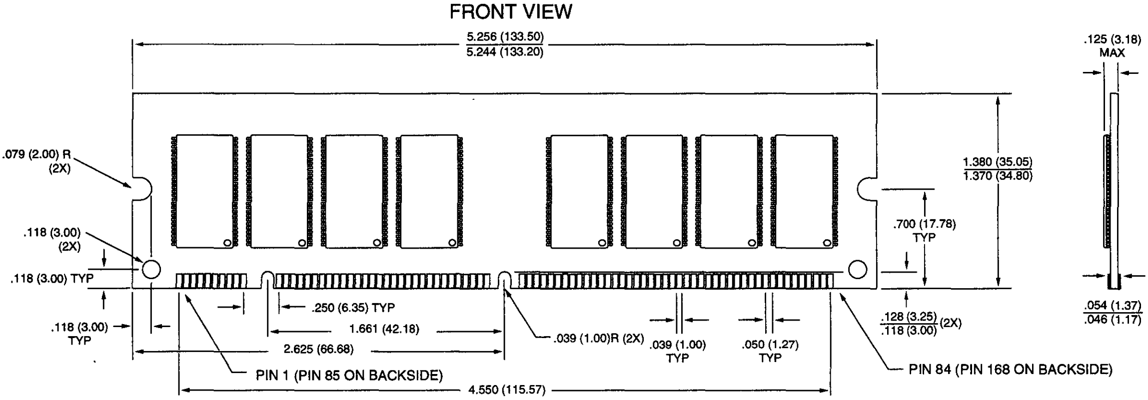
H-20



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

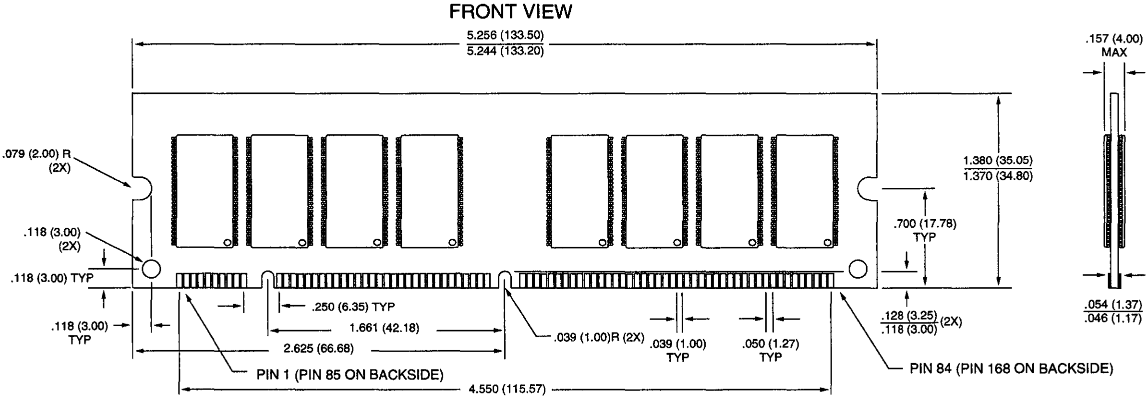
168-PIN DIMM

H-21



168-PIN DIMM

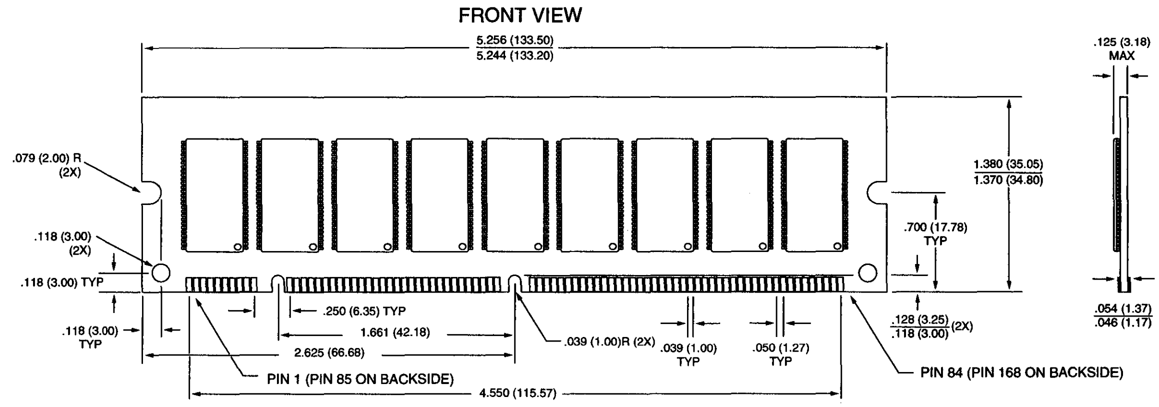
H-22



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

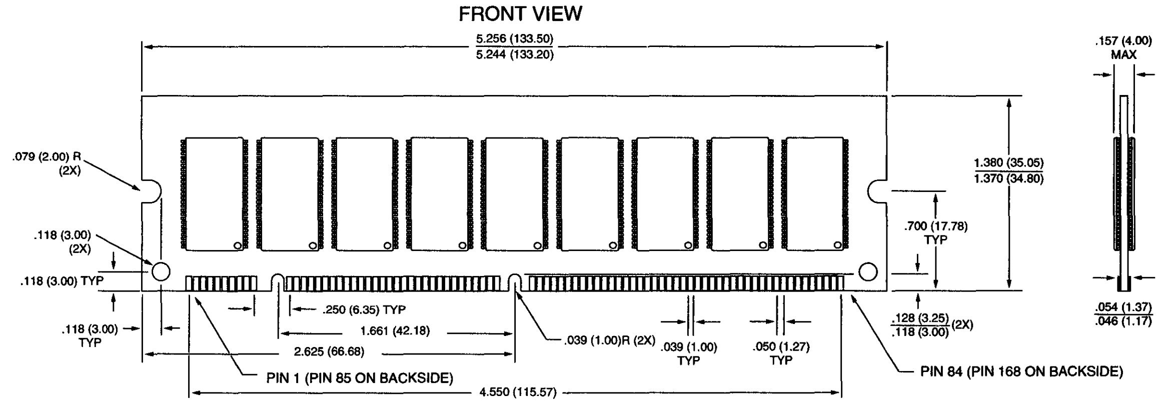
168-PIN DIMM

H-23



168-PIN DIMM

H-24

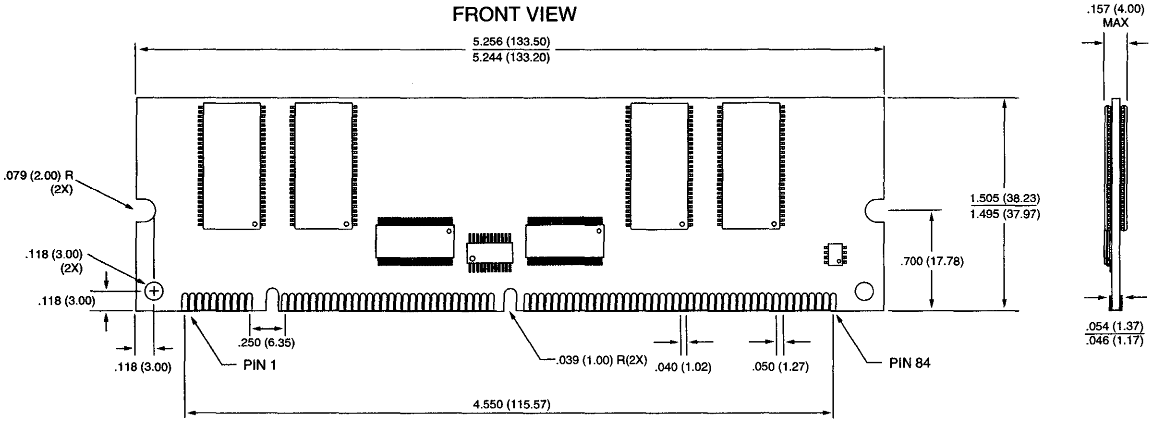


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

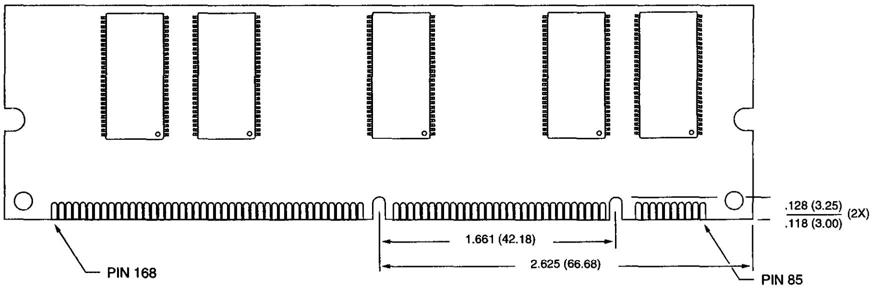
168-PIN DIMM

H-25

FRONT VIEW



BACK VIEW

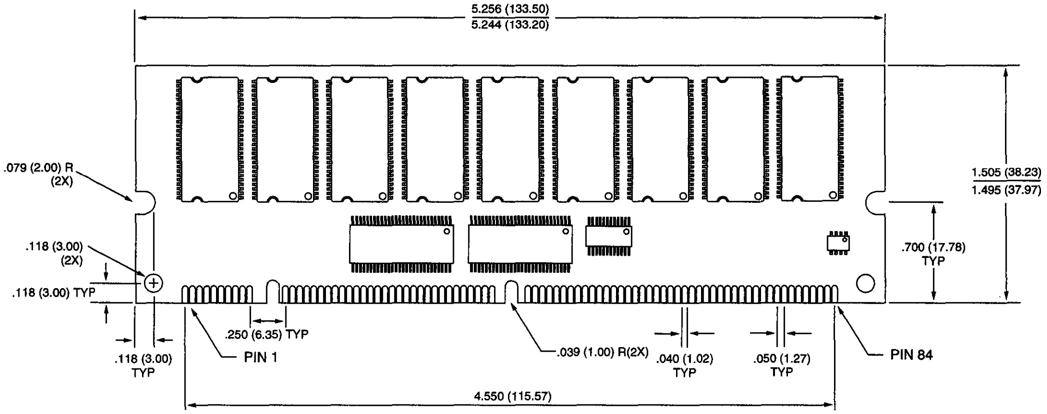


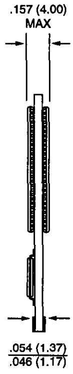
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

168-PIN DIMM

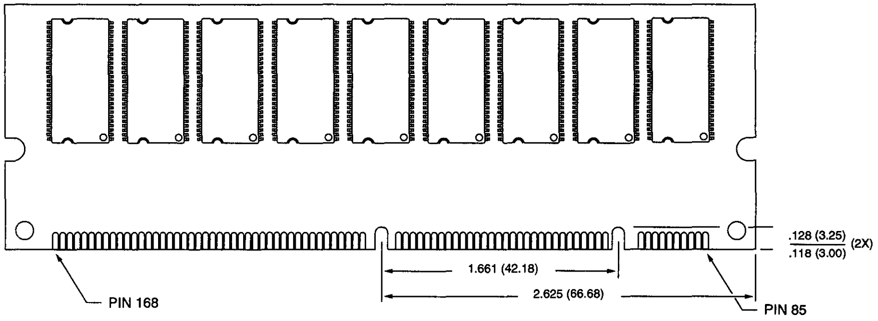
H-26

FRONT VIEW





BACK VIEW

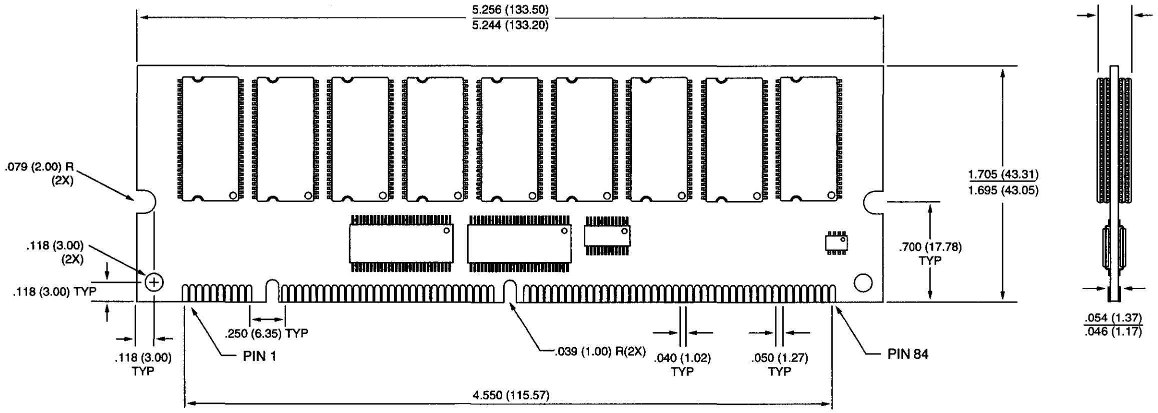


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

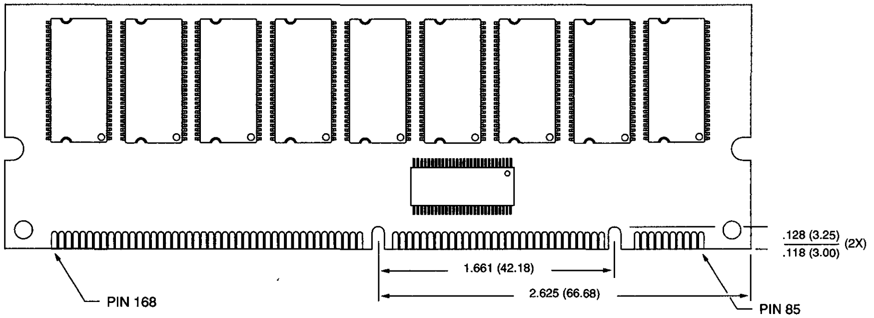
168-PIN DIMM

H-27

FRONT VIEW



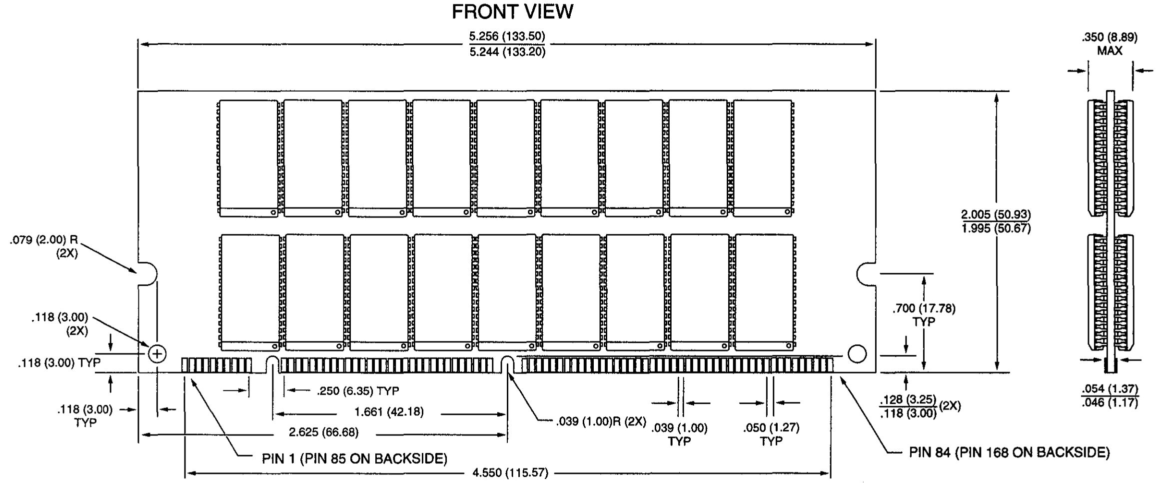
BACK VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

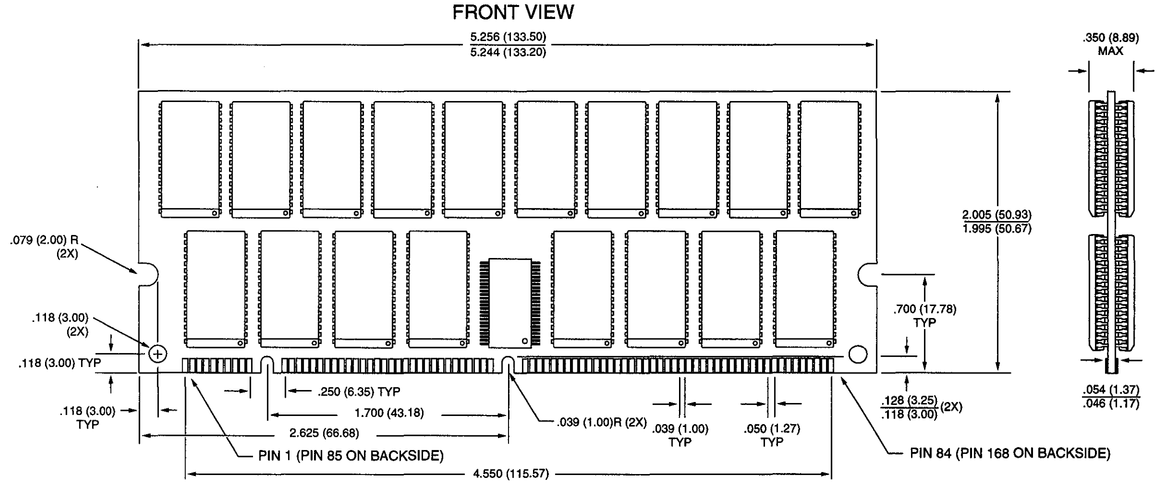
168-PIN DIMM

H-28



168-PIN DIMM

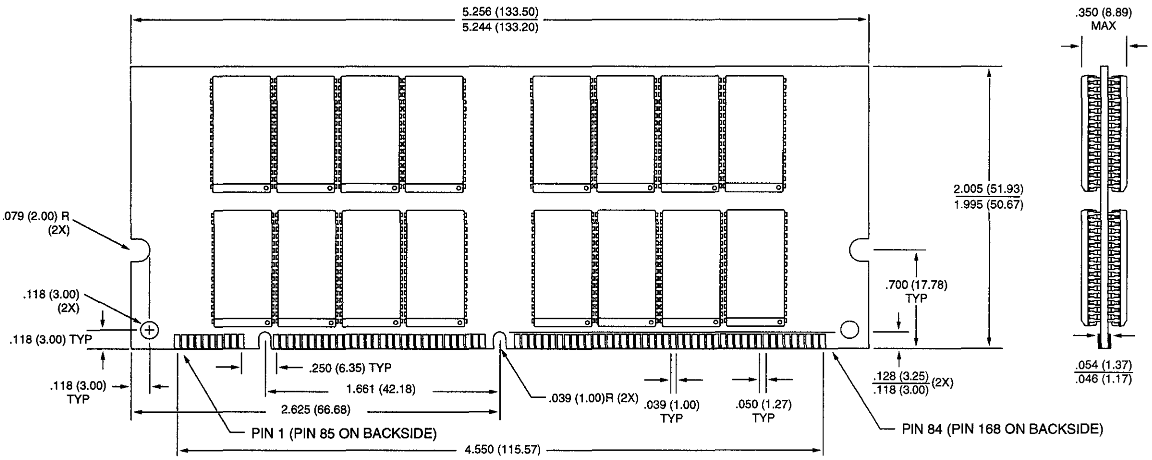
H-29



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

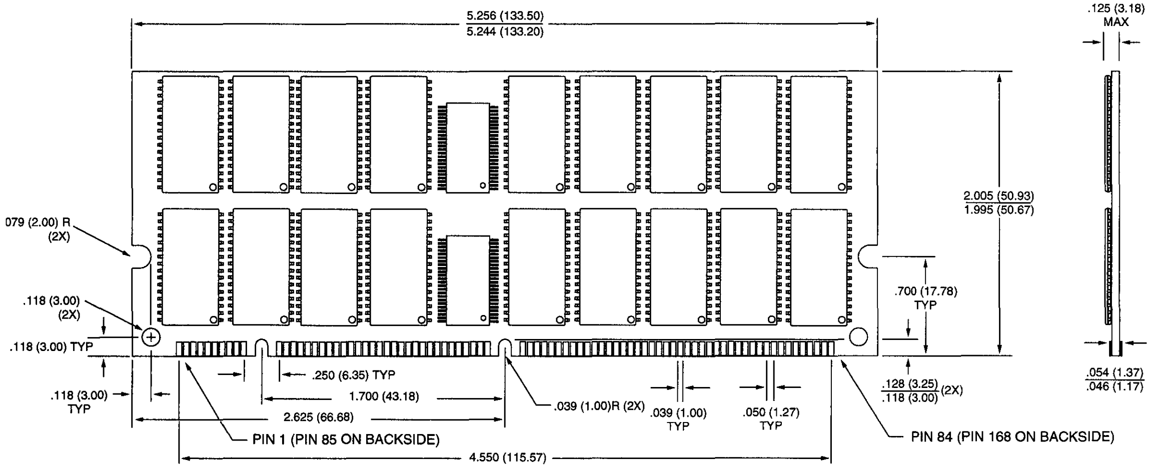
168-PIN DIMM

H-30


FRONT VIEW

168-PIN DIMM

H-31

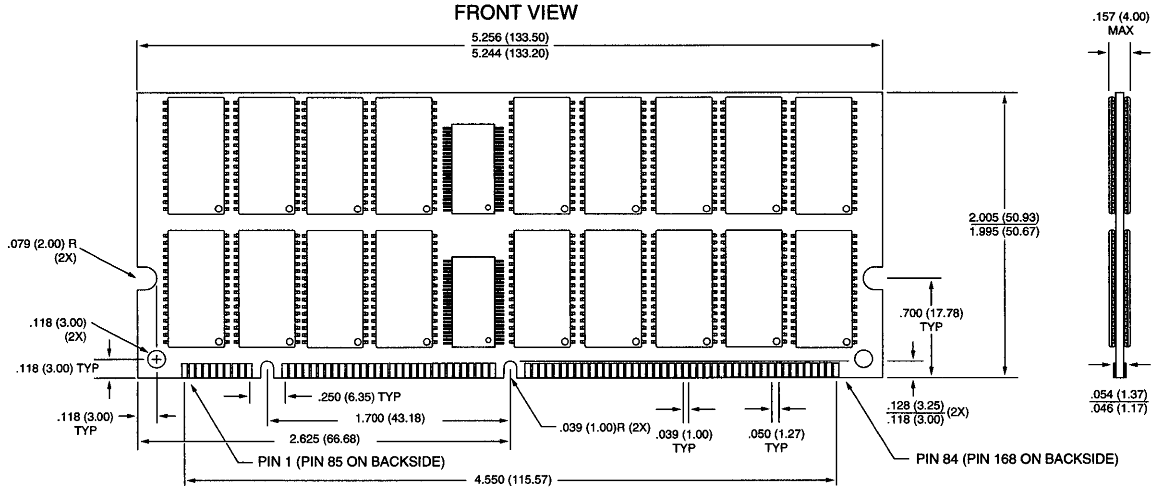

FRONT VIEW

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Micron Technology, Inc., reserves the right to change products or specifications without notice.

168-PIN DIMM

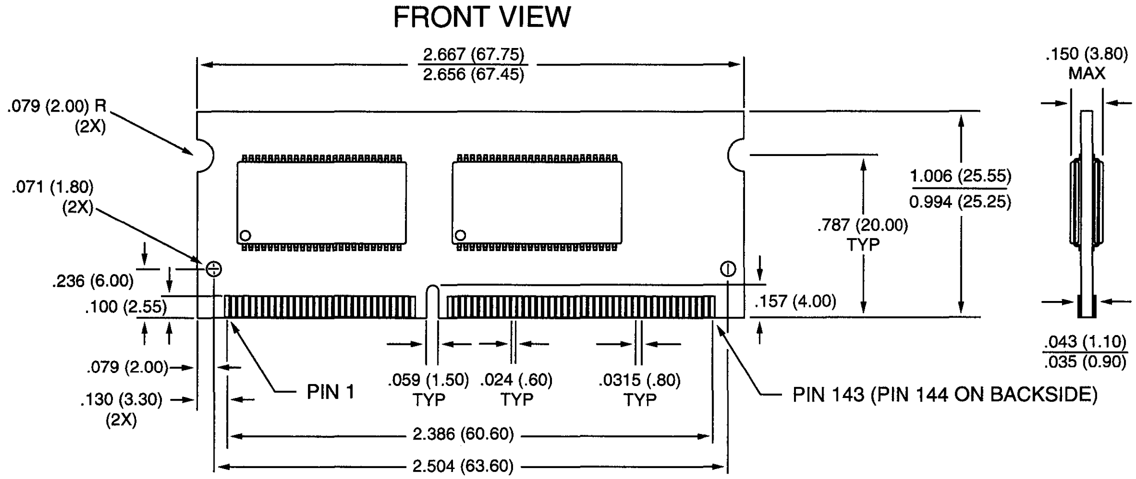
H-32



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

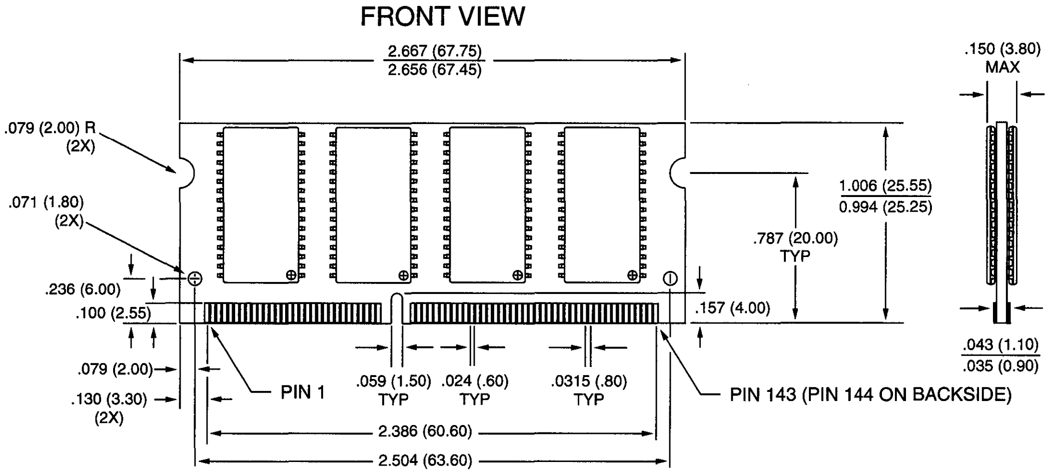
144-PIN SODIMM

I-1



144-PIN SODIMM

I-2

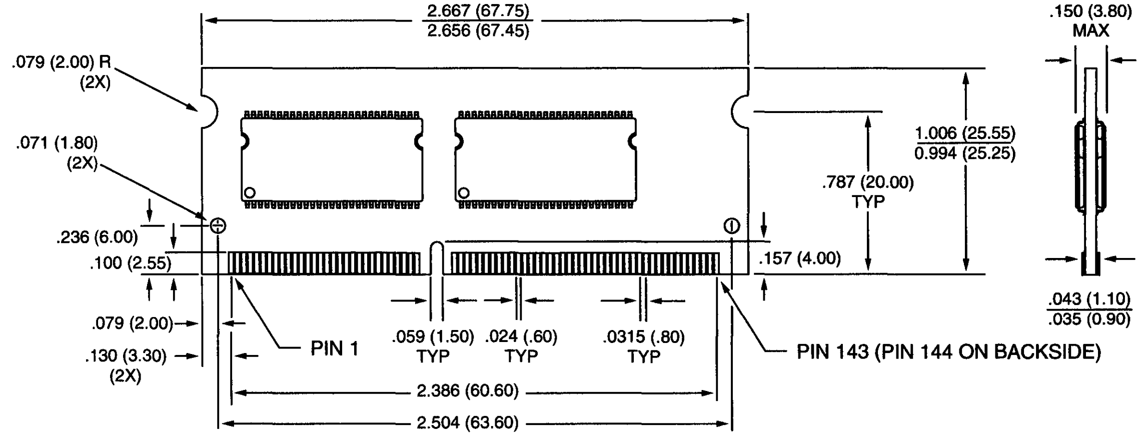


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

144-PIN SODIMM

I-3

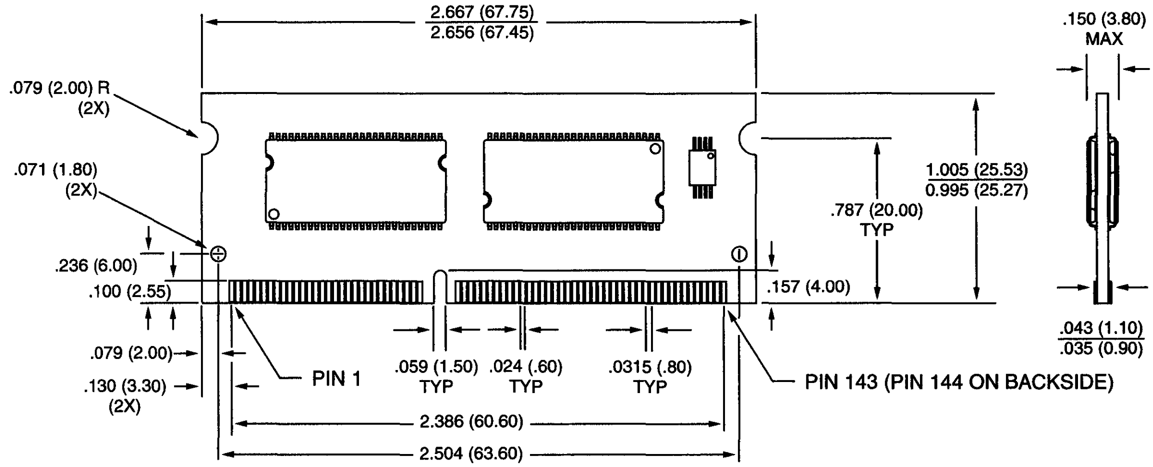
FRONT VIEW



144-PIN SODIMM

I-4

FRONT VIEW

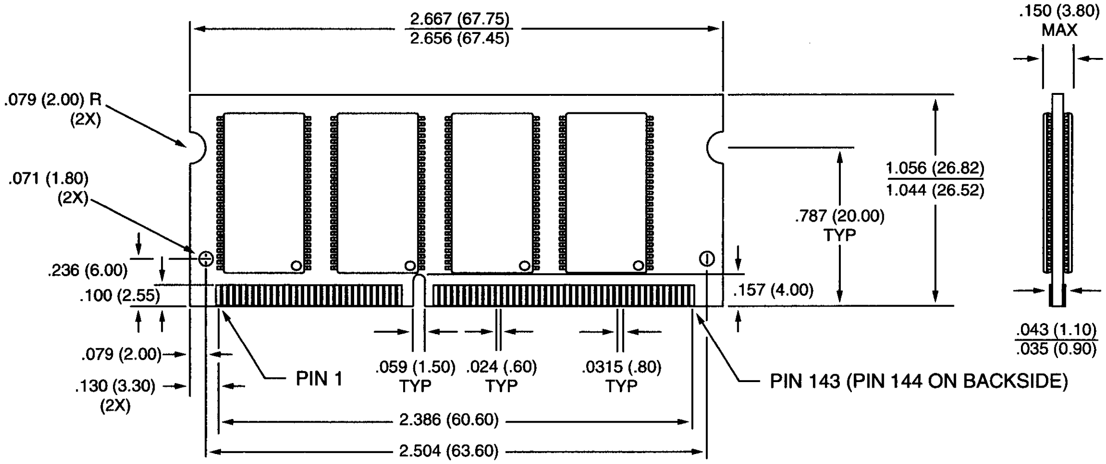


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

144-PIN SODIMM

I-5

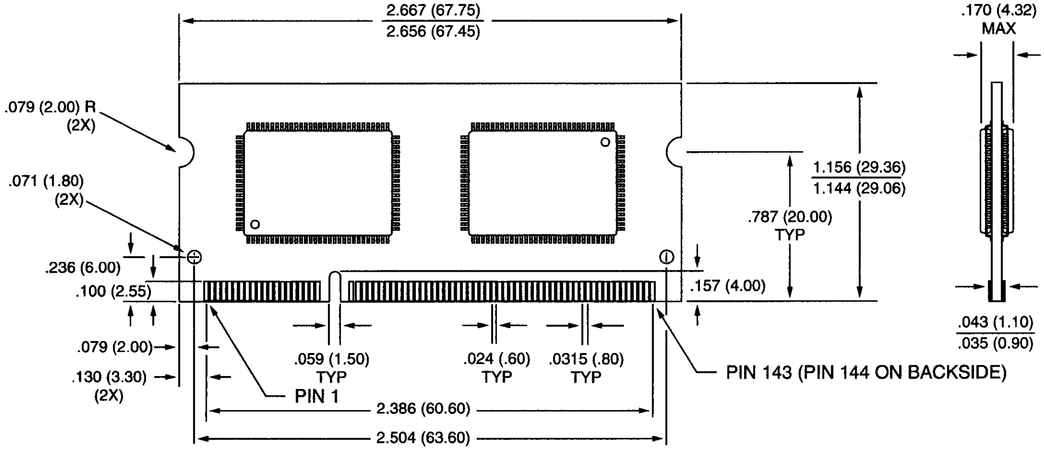
FRONT VIEW



144-PIN SODIMM

I-6

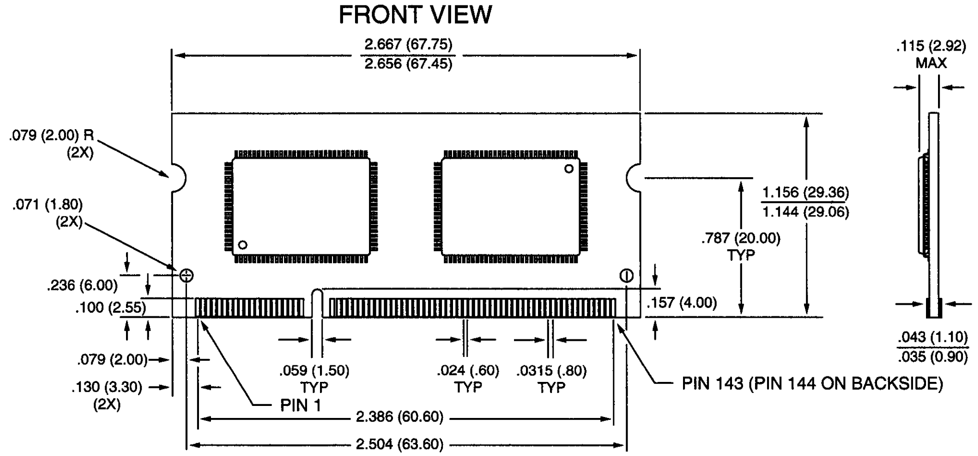
FRONT VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

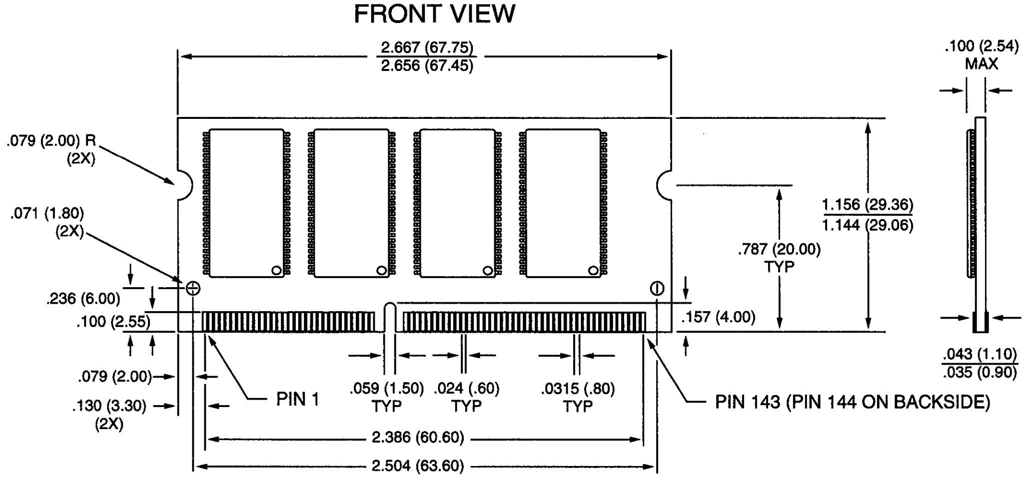
144-PIN SODIMM

I-7



144-PIN SODIMM

I-8

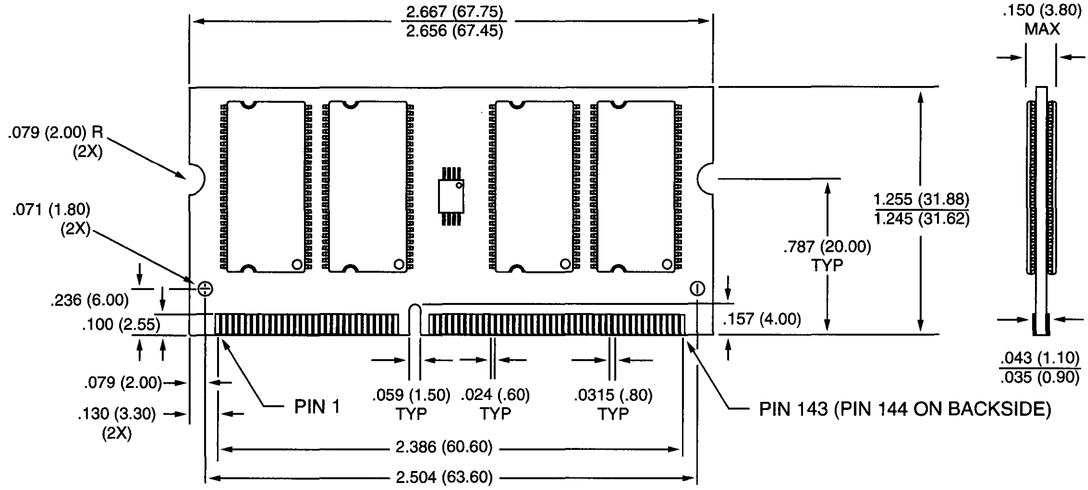


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

144-PIN SODIMM

I-9

FRONT VIEW



IOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

SALES AND SERVICE SELECTION GUIDE

CUSTOMER SERVICE NOTE

MASTER CONTAINER BAR CODE LABELS

INTRODUCTION

Micron Technology, Inc., uses standard bar code labels that conform to EIA Standard 556 for all shipments.

The bar code labels allow customers to scan Micron containers for quick order verification. Figure 1 shows an example of the standard bar code label used on master containers. Each individual box also has its own bar code label (see CSN-02).

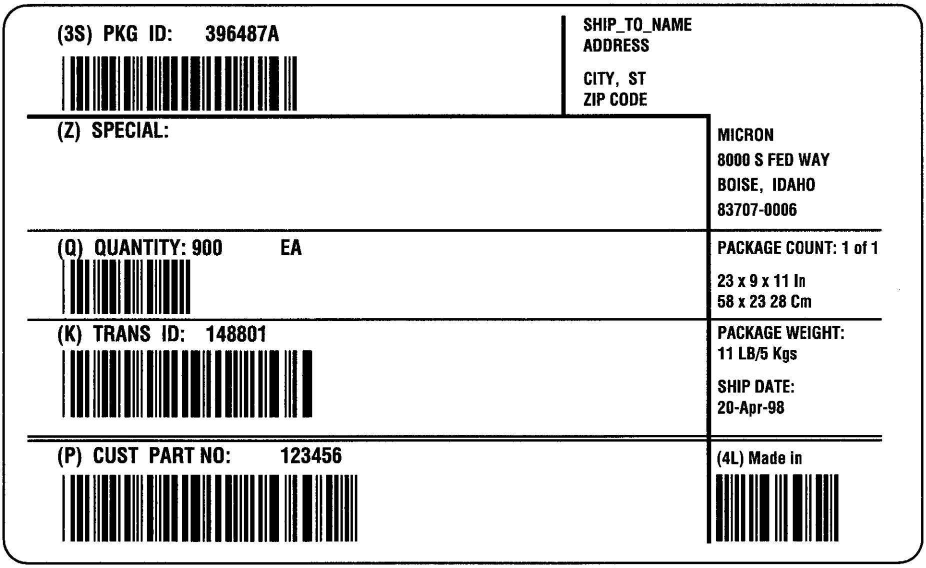
BAR CODE INFORMATION

The following information is provided on the master container label:

(3S) — Invoice/Packing Slip Number
(Z) — Special: Reserved for individual customer requirements
(Q) — Quantity in master container
(K) — Trans ID: Customer purchase order number
(P) — Customer Part Number: If a customer part number is not designated, the Micron part number will be printed
(4L) — Made in

ADDITIONAL SALES INFORMATION

Ship-to Name:	Customer's name and ship-to address
Ship-from Name:	Micron name and address
	Master container package count
	Package size
	Package weight
	Ship date



(3S) PKG ID: 396487A

SHIP_TO_NAME
ADDRESS
CITY, ST
ZIP CODE

(Z) SPECIAL:

MICRON
8000 S FED WAY
BOISE, IDAHO
83707-0006

(Q) QUANTITY: 900 EA

PACKAGE COUNT: 1 of 1
23 x 9 x 11 In
58 x 23 28 Cm

(K) TRANS ID: 148801

PACKAGE WEIGHT:
11 LB/5 Kgs
SHIP DATE:
20-Apr-98

(P) CUST PART NO: 123456

(4L) Made in

Figure 1
STANDARD BAR CODE LABEL

CUSTOMER SERVICE NOTE

INDIVIDUAL BOX BAR CODE LABELS

INTRODUCTION

Micron Technology, Inc., provides a standard bar code label on each individual box for quick order verification.

Figure 1 shows an example of the standard bar code label used on individual boxes. Each master container also has its own bar code label (see CSN-01).

Micron

PART NUMBER: MT28F002B1VG-6 T

SPEED: -06 QUANTITY: 10 DATE CODE: 9801*

56876073097

Figure 1
INDIVIDUAL BOX LABEL

*Date code of the oldest lot in the box.

CUSTOMER SERVICE NOTE

PRODUCT DRY PACK LABELING

INTRODUCTION

Micron Technology, Inc., provides a humidity indicator card (HIC) with all surface-mount products and small-quantity module shipments.

Figure 1 shows approximate labeling of the moisture-barrier bag (refer to Micron Technical Note TN-00-01, "Moisture Absorption in Plastic Packages") and an example of a standard HIC. The HIC is hermetically sealed in drypack and provides an indication of the RH level of the contents.

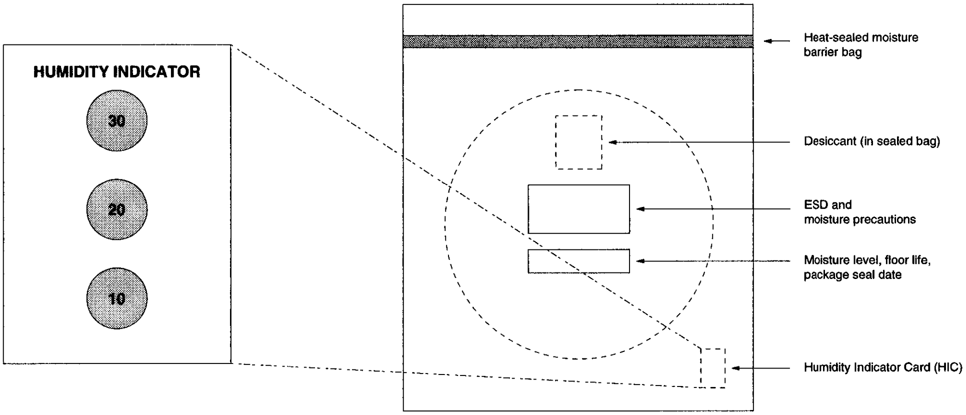


Figure 1
MOISTURE BARRIER BAG WITH HUMIDITY INDICATOR CARD

MICRON TECHNOLOGY, INC.

SALES AND SERVICE INFORMATION
CSN-04

CUSTOMER SERVICE NOTE

SHIPPING QUANTITY AND WEIGHT CHARTS

INTRODUCTION

Micron encourages customers to place orders in standard quantities whenever possible. The following charts will help determine order quantities.

Benefits to Micron's customers who order in standard quantities include:

1. Cost Savings: It is less expensive to send a shipment containing full boxes.
2. Process Control: Micron's production tracking system automatically checks speeds, die, customer codes and quantities. When standard box quantities are ordered, manual errors are eliminated, thus ensuring error-free shipments.
3. Lot Integrity: Lot integrity is kept intact when box quantities are not broken up.
4. Fewer Returns: Fewer errors equal fewer complaints and returns.

DRAM MODULE QUANTITY AND WEIGHT CHART

PART TYPE	TRAY QUANTITY	BOX QUANTITY	LBS PER BOX[1]
DRAM MODULES			
MT8D432G/M	50	250	NYA
MT16D832G/M	50	250	NYA
MT4D51232G/M	50	250	NYA
MT2D25632G/M	50	250	NYA
MT18LD472(A)G	50	250	22
MT4LDT164(A)G	50	250	NYA
MT8LD264(A)G	50	250	16
MT16LD464(A)G	50	250	NYA
MT9LD272(A)G	50	250	NYA
MT2LDT132HG	50	250	NYA
MT4LDT232HG	50	250	NYA
MT8LDT432HG	50	250	5.5
MT4LDT164HG	50	250	NYA
MT8LDT264HG	50	250	7.5
MT18D836	50	250	NYA
MT9D436	50	250	NYA
MT2D132G/M	50	250	NYA
MT4D232DG/DM	50	250	NYA
MT2LDT432HG	50	250	NYA
MT4LDT832HG	50	250	NYA
MT4LDT464AG	50	250	NYA
MT5LDT472(A)G	50	250	NYA
MT36LD(T)3272G	50	250	NYA
MT9LD(T)872(A)G	50	250	19.9
MT8LD864AG	50	250	18.85
MT16LD1664AG	50	250	NYA
MT18LD(T)1672(A)G	50	250	26.7
MT2LD132UG	50	250	NYA
MT4LD232UG	50	250	NYA
MT4LDT464HG	50	250	NYA
MT2LD432UG	50	250	NYA
MT4LD832UG	50	250	NYA

PART TYPE	TRAY QUANTITY	BOX QUANTITY	LBS PER BOX[1]
SYNC DRAM MODULES			
MT8LSDT264AG	50	250	16.0
MT9LSDT272AG	50	250	NYA
MT16LSDT464AG	50	250	18
MT18LDT472AG	50	250	NYA
MT8LSDT264HG	50	250	8.1
MT8LSDT864AG	50	250	15.95
MT9LSDT872(A)G	50	250	17.3
MT16LSDT1664AG	50	250	NYA
MT18LSDT1672(A)G	50	250	19.8
MT4LSDT232UDG	50	250	NYA
MT8LSDT432UG	50	250	NYA
MT4LSDT832UG	50	250	NYA
MT4LSDT464AG	50	250	NYA
MT5LSDT472AG	50	250	NYA
MT4LSDT464HG	50	250	NYA
MT8LSDT864HG	50	250	NYA
MT2LSDT132UG	50	250	NYA
SGRAM MODULES			
MT2LG25664HG	50	250	NYA
MT4LG51264HG	50	250	NYA

NOTE: 1. NYA = Not Yet Available

MICRON TECHNOLOGY, INC.

SALES AND SERVICE INFORMATION CSN-04

DRAM COMPONENT QUANTITY AND WEIGHT CHART

PART TYPE[1, 2]	PINS	PACKAGE WIDTH (mil)	QUANTITY PER TRAY	QUANTITY PER BOX	LBS PER BOX[3]	QUANTITY PER TUBE	TAPE-AND-REEL QUANTITY[4]	LBS PER REEL[3]	TAPE SIZE (mm)[5]
FPM/EDO DRAM									
16Mb									
MT4LC1M16C3TG/E5TG	44/50	400	117	500	3.3	—	500	2.5	32 x 16
MT4LC1M16C3DJ/E5DJ	42	400	—	1500	10.6	15	500	4.1	44 x 16
MT4LC4M4E8TG/E9TG	24/26	300	176	1,000	4.7	—	1,000	2.6	24 x 12
MT4LC4M4E8DJ/E9DJ	24/26	300	—	4,000	12.1	25	1,000	3.7	24 x 12
MT4LC4M4A1TG/B1TG	24/26	300	176	1,000	4.7	—	1,000	2.6	24 x 12
MT4LC4M4A1DJ/B1DJ	24/26	300	—	4,000	12.1	25	1,000	3.7	24 x 12
64Mb									
MT4LC16M4G3DJ/H9DJ	32	400	—	2,000	10.7	20	500	3.5	44 x 16
MT4LC16M4A7DJ/T8DJ	32	400	—	2,000	10.7	20	500	3.5	44 x 16
MT4LC8M8P4DJ/C2DJ	32	400	—	2,000	NYA	20	500	3.5	44 x 16
MT4LC8M8E1DJ/B6DJ	32	400	—	2,000	NYA	20	500	3.5	44 x 16
MT4LC4M16R6TG	50	400	117	500	NYA	—	500	NYA	44 x 16
MT4LC4M16F5TG	50	400	117	500	NYA	—	500	NYA	44 x 16
SYNC DRAM									
16Mb									
MT48LC1M16A1TG	50	400	135	500	NYA	—	1,000	NYA	32 x 16
64Mb									
MT48LC16M4A2TG	54	400	—	500	NYA	—	1,000	NYA	44 x 16
MT48LC8M8A2TG	54	400	—	500	NYA	—	1,000	NYA	44 x 16
MT48LC4M16A2TG	54	400	—	500	NYA	—	1,000	NYA	44 x 16
128Mb									
MT48LC32M4A2TG	54	400	—	500	NYA	—	1,000	NYA	44 x 16
MT48LC16M8A2TG	54	400	—	500	NYA	—	1,000	NYA	44 x 16
MT48LC8M16A2TG	54	400	—	500	NYA	—	1,000	NYA	44 x 16
SGRAM									
MT41LC256K32D4LG	100	14 x 20 (mm)	72	500	5.0	—	500	3.5	44 x 24

FLASH MEMORY QUANTITY AND WEIGHT CHART

PART TYPE[1, 6]	QUANTITY PER TRAY	QUANTITY PER BOX	LBS PER BOX[3]	QUANTITY PER TUBE[3]	TAPE-AND-REEL QUANTITY[4]	LBS PER REEL[3]	TAPE SIZE (mm)[5]
MT28F002VG	120	500	3.1	—	1,000	2.9	32 x 16
MT28F200SG	—	1,500	11.3	15	500	4.2	44 x 24
MT28F200WG	96	500	3.5	—	1,000	3.1	32 x 16
MT28F004VG	120	500	3.1	—	1,000	2.9	32 x 16
MT28F400SG	—	1,500	11.3	15	500	4.2	44 x 24
MT28F400WG	96	500	3.5	—	1,000	3.1	32 x 16
MT28F008VG	120	500	3.1	—	1,000	2.9	32 x 16
MT28F800SG	–	1500	11.3	15	500	4.2	44 x 24
MT28F800WG	96	500	3.5	—	1,000	3.1	32 x 16
MT28F800FB	96	500	NYA	NYA	1,000	NYA	32 x 16

NOTE:

1. When ordering tape-and-reel carrier, TR must be added to the ordering part number.
2. TG = TSOP Type II; DJ = SOJ; LG = TQFP
3. NYA = Not Yet Available
4. 13-inch reel
5. Tape width x pitch
6. VG = 40-pin TSOP Type I; SG = 44-pin SOP; WG = 48-pin TSOP Type I; FB = FBGA

SRAM COMPONENT QUANTITY AND WEIGHT CHART

PART TYPE[1, 2]	QUANTITY PER TRAY	QUANTITY PER BOX	LBS PER BOX	TAPE-AND-REEL QUANTITY[3]	LBS PER REEL	TAPE SIZE (mm)[4]
SYNCBURST™ SRAM						
MT58LC32K32B4/C6/D9LG	72	500	5.0	500	3.3	44 x 24
MT58LC32K36B4/C6/D9LG	72	500	5.0	500	3.3	44 x 24
MT58LC64K18B4/C6/D9LG	72	500	5.0	500	3.3	44 x 24
MT58LC64K32B4/C6/D9LG	72	500	5.0	500	3.3	44 x 24
MT58LC64K36B4/C6/D9LG	72	500	5.0	500	3.3	44 x 24
MT58LC128K18B4/C6/D9LG	72	500	5.0	500	3.3	44 x 24
MT58L128L32FT/PT/DT	72	500	5.0	500	3.3	44 x 24
MT58L128L32FS/PS/DS	72	500	5.0	500	3.3	44 x 24
MT58L128L36FT/PT/DT	72	500	5.0	500	3.3	44 x 24
MT58L128L36FS/PS/DS	72	500	5.0	500	3.3	44 x 24
MT58L256L18FT/PT/DT	72	500	5.0	500	3.3	44 x 24
MT58L256L18FS/PS/DS	72	500	5.0	500	3.3	44 x 24
MT58L256L32FT/PT/DT	72	500	5.0	500	3.3	44 x 24
MT58L256L32FS/PS/DS	72	500	5.0	500	3.3	44 x 24
MT58L256L36FT/PT/DT	72	500	5.0	500	3.3	44 x 24
MT58L256L36FS/PS/DS	72	500	5.0	500	3.3	44 x 24
MT58L512L18FT/PT/DT	72	500	5.0	500	3.3	44 x 24
MT58L512L18FS/PS/DS	72	500	5.0	500	3.3	44 x 24
ZBT™ SRAM						
MT55L64L32FT/PT	72	500	5.0	500	3.3	44 x 24
MT55L64L36FT/PT	72	500	5.0	500	3.3	44 x 24
MT55L128L18FT/PT	72	500	5.0	500	3.3	44 x 24
MT55L128L32FT/PT	72	500	5.0	500	3.3	44 x 24
MT55L128L36FT/PT	72	500	5.0	500	3.3	44 x 24
MT55L256L18FT/PT	72	500	5.0	500	3.3	44 x 24
MT55L256L32FT/PT	72	500	5.0	500	3.3	44 x 24
MT55L256L36FT/PT	72	500	5.0	500	3.3	44 x 24
MT55L512L18FT/PT	72	500	5.0	500	3.3	44 x 24

NOTE:
1. When ordering tape-and-reel carrier, TR must be added to the ordering part number.
2. LG = TQFP; T = TQFP (2-chip enable); S = TQFP (3-chip enable)
3. 13-inch reel
4. Tape width x pitch

MICRON TECHNOLOGY, INC.

SALES AND SERVICE INFORMATION
CSN-05

CUSTOMER SERVICE NOTE

ENVIRONMENTAL PROGRAMS

INTRODUCTION

Micron Technology, Inc., is certified to the ISO 14001 Environmental Management standard. Micron believes that environmental protection is a fundamental and integral part of doing business in the world today. Our environmental policy reflects this commitment:

The mission of Micron Technology, Inc., is to become a world-class team developing advantages for our customers. An integral part of this mission is a proactive approach to environmental compliance and protection that serves our team members, our customers, and the communities in which we operate.

Compliance with applicable environmental regulations is considered a minimum standard. Micron implements additional programs where appropriate to provide greater environmental protection. In developing environmental programs that go beyond legal compliance, Micron continually demonstrates the responsibility it feels toward its local and global communities.

An environmental team, which includes executive management and key operations personnel, is responsible for setting the goals of Micron's environmental effort and measuring our progress. The team implements our environmental goals and serves as a catalyst for all compliance and pollution prevention activities.

Micron has an active program for continuous reduction of chemicals in the manufacturing process. A chemical approval system is in place to review chemicals and their effects on associated waste streams prior to purchase and use. Micron identifies at the earliest stages those potential waste streams that should be eliminated or targeted for recycling.

Micron's pollution prevention, reclamation and recycling efforts not only benefit the environment but reduce material, energy and waste disposal costs. A significant part of Micron's recycling effort is the early evaluation of chemicals and equipment used in manufacturing. Micron has implemented aggressive, self-funded reclamation programs and continues to explore new ideas and technology as they emerge.

Micron strives to reduce the burden on air, water and land resources. Continuous improvement of our environmental performance is a long-term commitment of Micron's business mission and helps protect the future community.

In 1997 the EPA presented Micron with the Evergreen Award stating, "Through their significant corporate commitment to pollution reduction over the past decade, Micron Technology has earned an outstanding environmental track record. EPA Region 10 selects Micron Technology as a 1997 Evergreen Award recipient." This award was based on our pollution prevention, commitment to environmental quality and environmental leadership.

In 1998, Micron was presented with Boise, Idaho's new Enviroguard Award for promoting pollution prevention.

AIR QUALITY

Fugitive emissions represent one of the larger components of Micron's volatile organic compound (VOC) air emissions. Fugitive emissions result when a source material freely evaporates without being collected by an exhaust. At Micron, fugitive VOCs result primarily from solvents used to clean and to wipe down equipment.

Recognizing the problems posed by fugitive emissions, we explored measures to cut down on their release. An interdepartmental team, including members of our chemistry lab, contamination control group, production support and garment support services worked to find a solution. Instead of a solvent-based cleaner, we now use a water-based solution. In implementing this change, we not only succeeded in reducing our fugitive VOC emissions by 90 percent but also found the new cleaning procedure to be more effective than the previous method.

Over the years, Micron's ongoing effort to reduce air pollution has lead to the evaluation of several different pollution prevention and pollution control methods. We have completely eliminated Class I chlorofluorocarbons from our manufacturing process and have substituted a solvent in the manufacturing process that is approximately 80 percent less volatile. Micron has installed VOC abatement systems that are capable of achieving approximately 99 percent removal of remaining solvent VOC emissions.

Micron is continuing to look for innovative and effective means of eliminating air pollution. Over the past several years, prior to any established standards or proposed emission guidelines, we spent over $1 million to reduce air pollutant emissions.

WATER CONSERVATION

Semiconductor manufacturing requires pure water to clean semiconductor chips between production steps. Removing natural impurities from water to make it sufficiently pure for semiconductor manufacturing is costly. Therefore, it is not only environmentally sound but economically sound for Micron to look for innovative ways to reduce its dependence on outside water supplies. We now reclaim a large portion of the water needed for production processes and are conducting research and development in additional water reclamation processes.

The program began in 1986 with the segregation of very clean waste water sources and direct reuse of as much as 40 percent of the water used in production, nearly 25 percent of all water used on site. This program is ongoing and continues to capture and reuse up to 60 percent of the high purity water used in production.

Beginning in 1991 with a cost of over $9 million, the second step of the program resulted in recycling of an additional 25 percent of the water used throughout the plant by treating and recovering more contaminated waste water streams. This also resulted in the removal of 90 percent of the fluoride contained in our waste water discharges.

Micron's reclamation system is a model for change in the water use habits of the semiconductor manufacturing industry and earned Micron an award from the Pacific Northwest section of the American Water Works Association for innovation and commitment to water conservation.

POLLUTION PREVENTION

Micron's pollution prevention efforts include identification of those chemicals that are the largest contributors to emissions and hazardous waste. A team evaluates possible solutions for reduction, elimination or substitution of the chemicals. Substitution of a photolithography chemical has resulted in an 80 percent reduction in emissions.

All new chemicals must pass Micron's chemical review board before being introduced into the workplace. The board ensures compliance with OSHA and EPA reporting requirements by evaluating the chemical's effect and determining whether there is an alternative to its use.

RECLAMATION AND REUSE

Micron has installed a sulfuric acid reprocessing system that allows us to recover up to 380 gallons per day of used sulfuric acid from our fabrication areas. The acid reprocessors use distillation to reduce contaminants in the used acid to the part-per-billion levels, making the acid cleaner than when originally purchased. The purified acid is then returned to our sulfuric acid distribution system for reuse in the fabrication area.

We have also installed another new waste collection system to recover used phosphoric acid from our fabrication areas. The phosphoric acid is used by another company to produce a cleaning compound.

The result of these acid reclamation and reuse projects has been to reduce the amount of sulfates and phosphates in the waste water that Micron discharges and to reduce manufacturing costs.

WASTE RECYCLING AND REDUCTION

Among the materials included in Micron's existing recycling program are scrap metal, plastics, paper, cardboard, wafer boats and other scrap components. In addition, Micron is continuously searching for additional waste reduction opportunities. In 1996 the Idaho Division of Environmental Quality recognized Micron's waste minimization efforts for 1990-1995 with a Pollution Prevention Award.

NOTE: See CSN-08 for Micron's compliance with the ISO 14001 standard.

MICRON TECHNOLOGY, INC.

SALES AND SERVICE INFORMATION
CSN-06

CUSTOMER SERVICE NOTE

ELECTRONIC DATA INTERCHANGE

INTRODUCTION

Electronic Data Interchange (EDI) has become an important data transmission element in today's marketplace. Micron is ready to serve your EDI needs and encourages customer participation.

STANDARDS SUPPORTED

X.12

Micron supports versions 002000 through 003070 for all implemented transaction sets.

EDIFACT

Micron supports EDIFACT under the 90.1 EDIFICE guidelines (for the Purchase Order [PO], PO Acknowledgment, PO Change and PO Change Acknowledgment messages) and EDIFACT version 92.1 for all implemented messages.

TRANSACTION SETS

Inbound	Outbound
850 - PO	855 - PO Acknowledgment
860 - PO Change	865 - PO Change Acknowledgment
840 - Request For Quote (RFQ)	843 - Response to RFQ
830 - Forecast	856 - Advanced Ship Notice
846 - Inventory Inquiry/ Advice	810 - Invoice
867 - Product Transfer and Resale	832 - Price/Sales Catalog
844 - Product Transfer Account Adjustment (PTAA)	849 - Response to PTAA
997 - Functional Acknowledgment	845 - Ship and Debit Report
861 - Shipping Schedule Response	862 - Shipping Schedule
ORDERS - PO Message	ORDRSP - PO Response Message
ORDCHG - PO Change Request Message	INVOIC - Invoice Message
DELFOR - Delivery Schedule Message	DESADV - Despatch Advice Message
INVRPT - Inventory Inquiry/Advice	PRICAT - Price/Sales Catalog
RESRPT - POS and Credit Requests	

EDI TRANSMISSION PROTOCOL

These networks send EDI documents via standard protocol or X.400 (e-mail protocol).

AT&T

- Standard protocol
- X.400 (e-mail protocol)

IBM Global Service

- Standard protocol

TRANSMISSION TIMES

Transmissions occur every 15 minutes, 24 hours a day. Additional transmission times can easily be added as circumstances warrant.

MICRON EDI CONTACTS

Tanya Fries: 208-368-3249
Travis Nelson: 208-368-1084
E-mail: edi@micron.com

STEPS TO IMPLEMENTATION

The following are typical steps taken when Micron begins exchanging EDI data with a new trading partner:

- Micron receives an implementation guide from a trading partner
- Micron's EDI team contacts the trading partner's EDI coordinator to set up a trading partnership and coordinate the transmission and receipt of test documents
- Micron receives a test EDI document from the partner and responds with the necessary acknowledgments
- Once both parties agree everything is working properly, parallel testing with EDI and paper documents begins
- Micron ensures an EDI agreement has been signed and returned to the trading partner
- Paper documents are replaced with EDI documents (full production).

LEAD TIMES FOR FULL PRODUCTION

X.12	EDIFACT
One Month	One Month

CUSTOMER SERVICE NOTE

RETURNED MATERIAL AUTHORIZATION (RMA) PROCEDURES

HOW TO RETURN PRODUCT TO MICRON

- Obtain an RMA number. (See "How to Obtain an RMA" below.)
- Package product using all antistatic precautions.
- Package any die product being returned in a Gel-Pak. (See Micron Technical Note TN-00-03.)
- Write RMA number on outside of box for proper routing.
- Ship package prepaid to:
    Micron Semiconductor Products, Inc.
    Attn: RMA Dept., RMA #
    8000 S. Federal Way, Dock 21A
    Boise, ID 83716
- If RMA is being shipped from outside of the United States, please note that Boise, Idaho, is a customs port city; refer to Port City Code 2907.

HOW TO OBTAIN AN RMA

NONFAILURE-RELATED RETURNS:

- If you buy direct, contact your Micron sales representative at 208-368-3900.
- If you buy through a Micron sales representative, contact that sales representative.
- If you buy through distribution, contact the distributor.
- Provide the following information:
  1. Micron part number, including speed and package
  2. Reason for return
  3. One of the following: PO number, invoice number or sales order number
  4. Preferred reimbursement method: replacement parts, credit only or refund.

FAILURE-RELATED RETURNS AND/OR APPLICATION PROBLEMS:

- Contact Micron Applications Engineering Department at 208-368-3950.
- Provide the following information:
  1. Micron part number, including speed and package
  2. Type of failure
  3. Name of engineer who witnessed failure or requested failure analysis report
  4. One of the following: PO number, invoice number or sales order number
  5. Preferred reimbursement method: replacement parts, credit only or refund.

FAILURE ANALYSIS STANDARDS FOR RMAs:

- Upon receipt of an RMA for failure analysis, Micron's Quality Assurance Department will contact the customer with the preliminary test results within two business days of the receipt of the returned material.
- Micron's Quality Assurance Department will issue a completed failure analysis report within three weeks of receiving an RMA.
- Replacement or noncorrelate parts will be shipped upon completion of analysis.

MICRON ACCOUNTING PROCEDURES FOR RMAs

A credit memo is sent upon receipt of the RMA parts, unless a refund has been requested. Micron will issue a refund check for the amount of the return upon arrival of the RMA parts, provided all invoices are paid and no future business is expected. Replacement parts are shipped after receipt of the RMA parts, and a billing invoice is sent out the day after shipment.

In order to maintain clear communication between accounting departments, please refer to RMA and credit memo numbers as much as possible.

CUSTOMER SERVICE NOTE

ISO STANDARDS

ISO 9001

Micron Technology, Inc., was certified to ISO 9001 standards on February 1, 1994, by KEMA Registered Quality, Inc. KEMA Registered Quality, Inc., has been accredited by ANSI-RAB in the United States and the RvA in the Netherlands.

ISO 9001 is one of a series of three international standards dealing with quality systems. It is a model for quality control in design/development, manufacturing, testing, installation and servicing. It is the most comprehensive level of registration in the internationally recognized ISO 9000 family for quality system management.

ISO 9001 gives customers and suppliers a single set of guidelines that is accepted worldwide and that can be followed to achieve a definable level of quality. The third-party certification confirms that a company's systems for accepting orders, reviewing customers' specifications, manufacturing and testing products, and delivering those products to its customers are quality controlled and should produce consistent results.

A supplier's ability to conform to the ISO 9001 standard is assessed via the standard's Quality System Requirements—a set of twenty clauses, each designed to address a specific portion of a quality system: management responsibility; quality system; contract review; design control; document control; purchasing; purchaser-supplied product; product identification and traceability; process control; inspection and testing; inspection measuring and test equipment; inspection and test status; control of nonconforming product; corrective action; handling, storage, packaging and delivery; quality records; internal quality audits; training; servicing; and statistical techniques.

Micron's ISO 9001 certificate, number 10017.01, was renewed January 28, 1997, and is valid until February 1, 2000. The scope of the conformity assessment includes Micron's semiconductor business, including the design, manufacturing, electrical and environmental testing, and marketing of semiconductor memory components; the Systems Integration group's operation, including the design, manufacturing and electrical testing of memory modules; and the International Sales offices in the U.K., Germany, Singapore and Taiwan.

ISO 14001

Micron is in compliance with the state-of-the-art ISO 14001 standard. ISO 14001 Environmental Management System standards establish a comprehensive, internationally recognized system for managing and improving sound environmental performance. Micron selected this standard for the system principles that it shares with the ISO 9000 series of quality standards and for the compatibility it offers with Micron's historical environmental management and continual improvement philosophies. We also believed that third-party certification would be regarded as an asset by customers and an objective measurement by other interested parties.

The environmental management system certification is the assessment and audit of the organization's environmental management system by the Registrar. The assessment includes an examination of the company's environmental policy, environmental management system and its documentation, EMS auditing program and procedures, and environmental records. It also includes a thorough on-site audit to determine conformance to the ISO 14001 standard.

An audit of Micron Technology's Boise site was performed in December 1996 and was witnessed by representatives from the RAB and the Idaho Division of Environmental Quality (DEQ).

Micron's ISO 14001 certificate, number 10017.05, is valid for a three-year period, until February 17, 2000, pending continuing successful surveillance visits.

NOTE: See CSN-05 for more information on Micron's environmental programs.

CUSTOMER SERVICE NOTE

CUSTOMER COMMENT

INTRODUCTION

Micron is committed to achieving the highest standard in customer satisfaction, and we believe that giving our customers the opportunity to voice comments and complaints will help us discover ways to better serve them. To achieve continuous improvement, we need ongoing constructive customer feedback so we know exactly what our customers expect and need.

CUSTOMER COMMENTS

If you have experienced a recent transaction with Micron that requires immediate assistance, if you want to provide feedback, or if you need information on local sales representatives in your area, please phone, fax or e-mail one of our customer satisfaction representatives.

Micron's Comment Line (800-932-4992 [U.S.]; 01-208-368-5090 [Intl.]) is answered by Customer Service personnel from 7:30 a.m. to 6:00 p.m. MST weekdays and is transferred to voice mail during off hours, weekends and holidays. You may also fax your comments to us any time at 208-368-5018. We are also available via the internet. Contact us online at:

www.micron.com/mti/msp/html/cssform.html

RESPONSE STANDARDS

At Micron, we are dedicated to serving our customers and have set a 24-hour standard of returning all calls, faxes, and e-mails. If we can't solve the matter at the time of your initial inquiry, we will respond with an update to your question or concern within 24 hours.

CUSTOMER SERVICE NOTE

PRODUCT MARK/ LABEL

INTRODUCTION

As technology changes and components get smaller and smaller, it becomes increasingly challenging to provide a part mark that can be easily read with the human eye. Micron now has two part mark variations to accommodate smaller components and different package sizes (i.e., FBGA, CSP). Both part marks are right and left justified and have a character size of 0.045 inches. Both marks also include a unique, laser-scribed identification number on the top side of the part which is used for traceability purposes.

COMPONENT MARK INFORMATION

Most component marks contain the following details (as shown in Figure 1):

- Date code (work week and year)
- Country of diffusion
- Country of encapsulation
- Micron logo
- Product family
- Process technology
- Device number
- Device versions
- Package type
- Subsidiary designator (if relevant)
- Speed
- Special test option (if relevant)
- Die revision

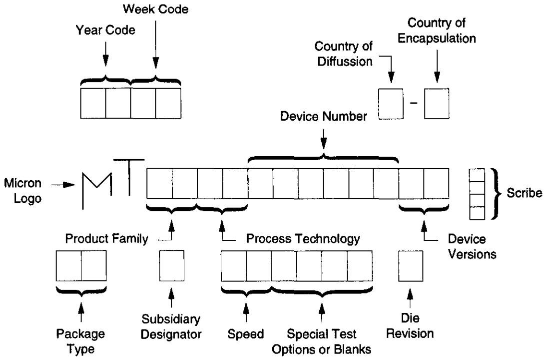


Figure 1
COMPONENT MARK

ABBREVIATED COMPONENT MARK INFORMATION

Due to space limitations, some component marks may contain the following abbreviated details (as shown in Figure 2):

- Date code (work week)
- Die revision
- Country of diffusion
- Country of encapsulation
- Micron logo/Pin 1 designator
- Product group
- Product type
- Density/size
- Width
- Speed and special test options

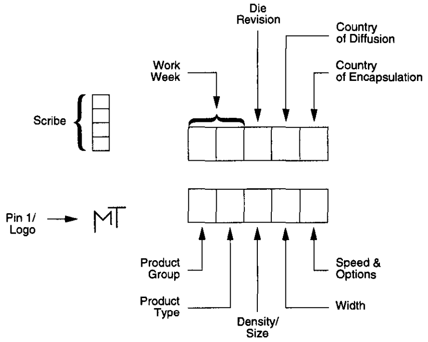
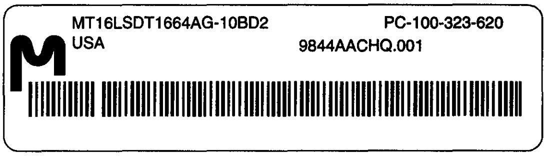


Figure 2
ABBREVIATED COMPONENT MARK

MODULE LABEL INFORMATION

Labels typically used for module production have standard requirements for each line printed on the label (see Figure 3 for an example):

- Line 1: Marketing part number/special request information
- Line 2: Module assembly country of origin, date code/lot ID code
- Line 3: Bar code of Micron part number (excludes "MT").



MT16LSDT1664AG-10BD2 PC-100-323-620
USA 9844AACHQ.001

Figure 3
MODULE LABEL

CUSTOMER SERVICE NOTE

PRODUCT CHANGE NOTIFICATION (PCN) SYSTEM

MICRON'S PCN SYSTEM

Micron's automated Product Change Notification (PCN) ystem provides notice to customers, per EIA/JESD46-A, f Micron product or process changes affecting form, fit or unction.

CHANGES REQUIRING NOTIFICATION

Module and component modifications that require cus-omer notification include:

- Data sheet
- Die and module design
- Geographic location
- Lead frame and plating
- Mark/Label
- SPD
- Metallization
- Packaging material and process
- Passivation
- Product obsolescence
- Shipping material
- Wafer material

PCN LETTER DOCUMENTATION

PCN letters include the following information:

- PCN number
- A detailed description of the change
- The reason for the change
- Supporting qualification data if appropriate
- A description of Micron product(s) affected by the change
- A list of each Micron part number purchased (along with the corresponding customer number if available) or for which there is current backlog

DISTRIBUTION CUSTOMER NOTIFICATION

Micron also issues PCN letters for customers who purchase solely through distribution. These letters are sent in care of local distributors for disbursement to their customers.

CUSTOMER SERVICE NOTE

DIE RETURNED MATERIAL AUTHORIZATION (RMA) PROCEDURES

INTRODUCTION

Die Returned Material Authorizations (RMAs) are very similar to RMAs for packaged parts and basically follow the procedures outlined in Customer Service Note CSN-07, "RMA Procedures." However, there are unique aspects to die products that require slightly different procedures for RMAs. The purpose of this customer service note is to describe the differences associated with die RMAs.

ACCEPTABLE DIE RMAs

Approval is required for all die RMAs, regardless of whether they are nonfailure-related, failure-related or application-related problems. See CSN-07 for details.

Die users have varying packaging techniques and procedures. When die exhibit failures or application problems, users need to fill out the form, "Die Processing/Handling Checklist." (Call 1-800-932-4992 to get this form.) Its purpose is to ensure that die RMAs are treated properly when functional testing or failure analysis is performed at Micron.

Contact Micron Marketing at 208-368-3950 for information about die warranties.

NOTE: If die was purchased through distribution, please contact your distributor.

RETURNING DIE IN GEL-PAKS

Micron ships all die products in Gel-Pak containers. Unused die must be reattached to the original Gel-Pak with a vacuum tool and returned to Micron. Items not returned in Gel-Pak or not reattached correctly may void the warranty. Proper precautions should be taken for both ESD and humidity when reattaching the die to these Gel-Pak containers.

It is very easy to damage die when reattaching them to Gel-Paks. A vacuum pickup tool is usually used to remove die from the Gel-Pak and should not damage the die if used properly. If possible, this tool should also be used to reattach the die. Tweezers can be used to reattach die in Gel-Paks, but can easily scratch or crack the die, which may void the warranty. Any scratched or cracked die received by Micron will be returned to the customer.

RETURNING PACKAGED PARTS

If failures or application problems occur after the die have been post-processed by the user, it may be necessary to return a packaged part to Micron for failure analysis.

If the packaging technology allows for rework, the die must be removed and returned in a Gel-Pak container to Micron. Users that cannot easily rework die should send the module or hybrid package back to Micron in appropriate packaging that will prevent shipping damage as well as provide for proper ESD protections. Micron's Quality Assurance Department will decapsulate the die and perform failure analysis on the device. The Die Processing/Handling Checklist and any special instructions for deprocessing should accompany the part.

CONCLUSION

Die product RMAs require different procedures from packaged product RMAs because die can be damaged very easily if not properly handled. Make sure the Die Processing/Handling Checklist is filled out and sent to Micron prior to returning die product.

CUSTOMER SERVICE NOTE

TAPE-AND-REEL PROCEDURES

INTRODUCTION

Micron supports the Electronic Industries Association's (EIA) standardization of tape-and-reel specifications number 481A. Specifications for Micron's tape-and-reel offerings are detailed in the following figures and tables.

When ordering tape-and-reel carriers, "TR" must be added to the ordering part number.

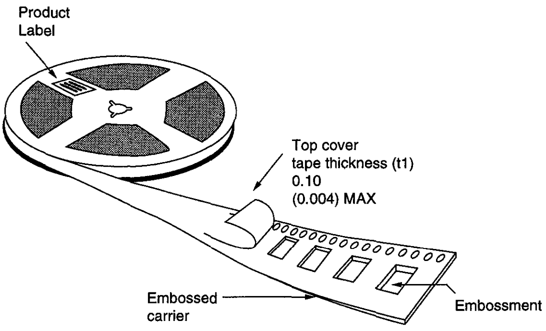


Figure 1
REEL

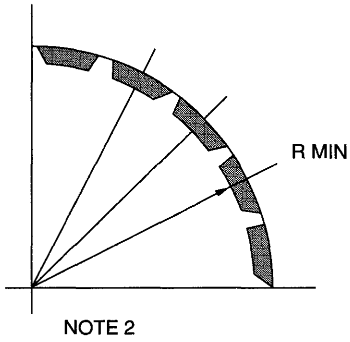
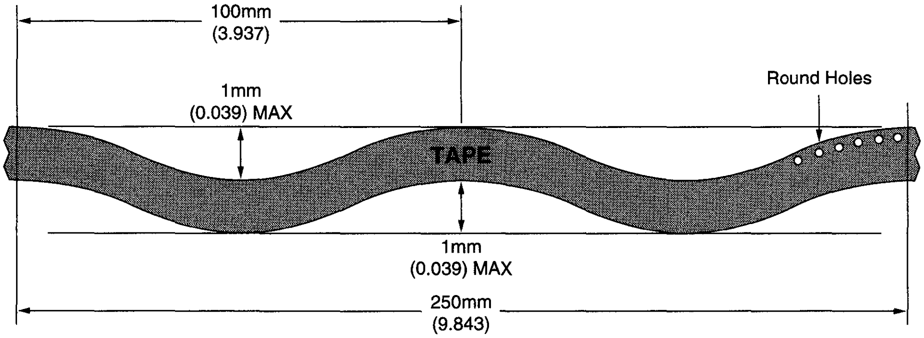


Figure 2
BENDING RADIUS



Allowable camber to be 1mm/100mm nonaccumulative over 250mm.

Figure 3
CAMBER
(top view)

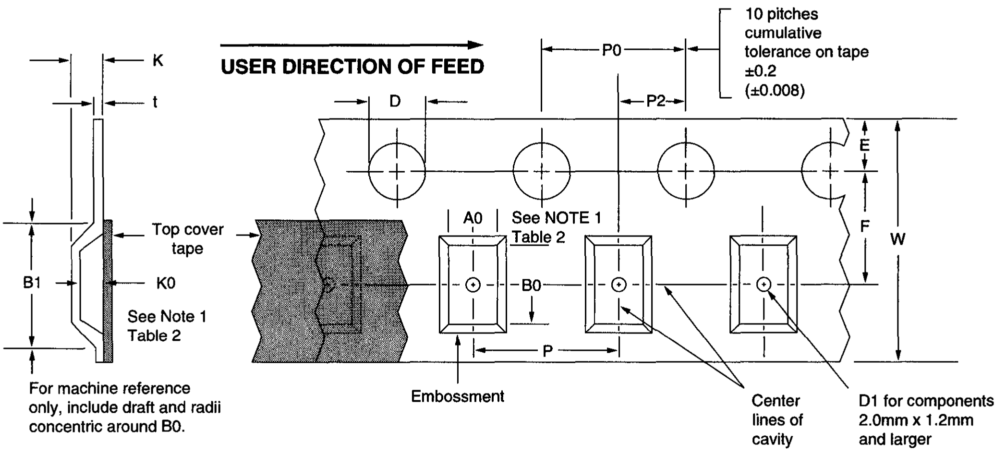


Figure 4
EMBOSSED CARRIER DIMENSIONS
(24mm tape only)

Table 1
24mm EMBOSSED TAPE DIMENSIONS[3]

TAPE SIZE	D	E	P0	t (MAX)	A0, B0, K0
24mm	1.5 $^{+0.10}_{-0.00}$ (0.59) $^{+0.004}_{-0.000}$	1.75 (0.069 ±0.004)	4 (0.157 ±0.004)	0.600 (0.024)	NOTE 1

TAPE SIZE	B1 (MAX)	D1 (MIN)	F	K (MAX)	P2	R (MIN)[2]	W
24mm	20.1 (0.791)	1.5 (0.059)	11.5 ±0.10 (0.453 ±0.004)	6.5 (0.256)	2 ±0.10 (0.079 ±0.004)	50 (1.969)	24 ±0.30 (0.945 ±0.012)

TAPE SIZE	P					
	4 ±0.10 (0.157 ±0.004)	**8 ±0.10 (0.315 ±0.004)**	**12 ±0.10 (0.472 ±0.004)**	**16 ±0.10 (0.630 ±0.004)**	**20 ±0.10 (0.787 ±0.004)**	**24 ±0.10 (0.945 ±0.004)**
24mm			x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters (inches).

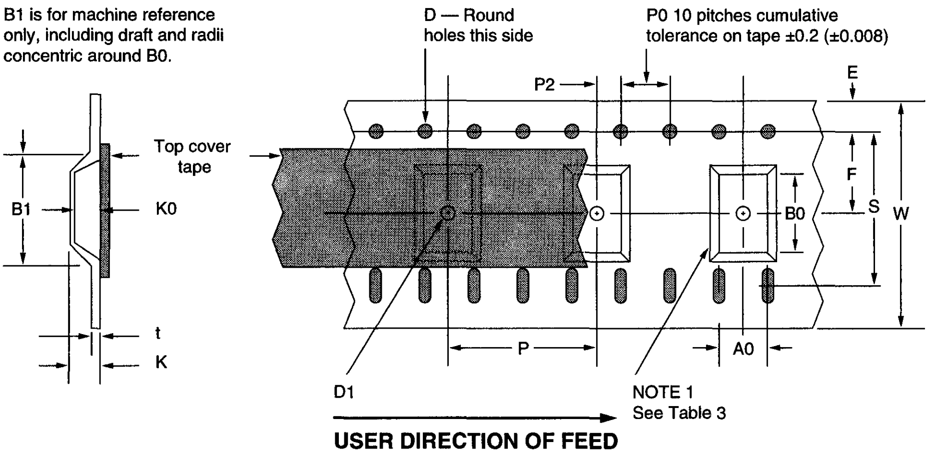


Figure 5
EMBOSSED CARRIER DIMENSIONS
(32mm and 44mm tape only)

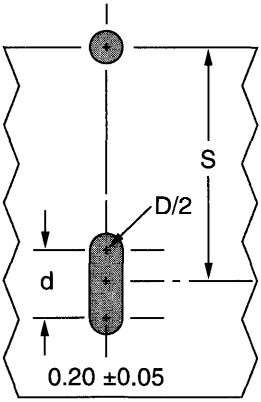


Figure 6
DETAIL ELONGATED HOLE

Table 2
32mm AND 44mm EMBOSSED TAPE [3]

TAPE SIZE	D	D1 (MIN)	E	K (MAX)	P0	t (MAX)	A0, B0, K0
32mm and 44mm	$1.5^{+0.10}_{+0.00}$ $(0.059)^{+0.004}_{+0.000}$	2 (0.079)	1.75 ±0.10 (0.069 ±0.004)	10 (0.394)	4 ±0.10 (0.156 ±0.004)	0.500 (0.20)	NOTE 1

TAPE SIZE	B1 (MAX)	F	P2	S	W	R (MIN) [2]
32mm	23 (0.906)	14.2 ±0.10 (0.559 ±0.004)	2 ±0.10 (0.079 ±0.004)	28.4 ±0.10 (1.118 ±0.004)	32 ±0.30 (1.26 ±0.012)	50 (1.973)
44mm	35 (1.378)	20.2 ±0.15 (0.795 ±0.006)	2 ±0.15 (0.079 ±0.006)	40.4 ±0.10 (1.591 ±0.004)	44.8 ±0.30 (1.732 ±0.12)	50 (1.973)

TAPE SIZE	P							
	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)	28 ±0.10 (1.102 ±0.004)	32 ±0.10 (1.26 ±0.004)	36 ±0.10 (1.417 ±0.004)	40 ±0.10 (1.575 ±0.004)	44 ±0.10 (1.732 ±0.004)
32mm	x	x	x	x	x			
44mm			x	x	x	x	x	x

NOTE:

1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.15 (0.006) MIN to 1.00 (0.039) MAX for 32mm and 44mm tape. The component cannot rotate more than 10° within the determined cavity.
2. Tape and components shall pass around radius “R” without damage.
3. All dimensions in millimeters (inches).

ORDERING INFORMATION

Micron components are manufactured and quality controlled using Micron's low-power, high-performance CMOS silicon-gate process. Micron products meet JEDEC and industry standards. Device functionality is consistently ensured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous system-level testing during many hours of accelerated burn-in prior to final test and shipment. This testing is performed with Micron's exclusive AMBYX™ intelligent burn-in and test system.

Micron's policy is to provide prompt, accurate and courteous service, while ensuring reliability and quality. Please contact us for technical, test and application assistance or to find out the name and location of the sales representative and distributor nearest you.

Telephone: 208-368-3900
Fax: 208-368-4617

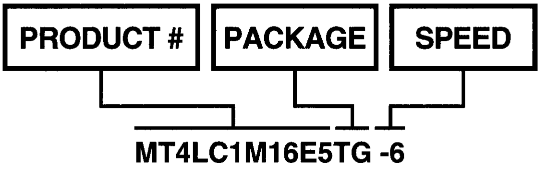
Customer Comment Line:
U.S.A. 800-932-4992
Intl. 01-208-368-5090
Fax 01-208-368-5018

Internet: www.micron.com/mti/msp/html/cssform.html

ORDER EXAMPLES

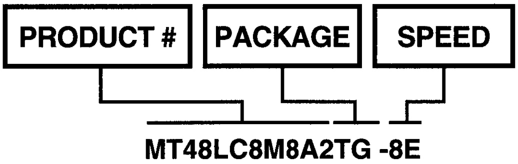
DRAM

1 Meg x 16 EDO, 60ns in Plastic TSOP



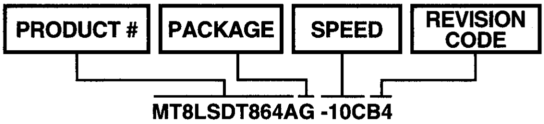
SDRAM

8 Meg x 8, 125 MHz in Plastic TSOP



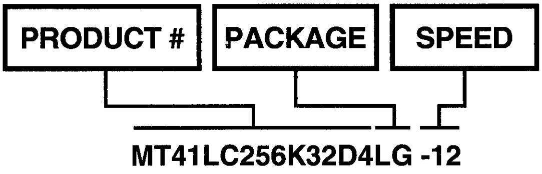
SDRAM MODULE

8 Meg x 64, nonbuffered PC100 (3-2-2 SPD) in 168-pin DIMM Module



SGRAM

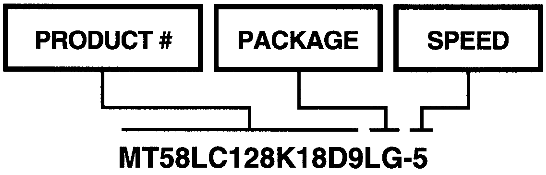
256K x 32, 12ns in Plastic TQFP



ORDER EXAMPLES (continued)

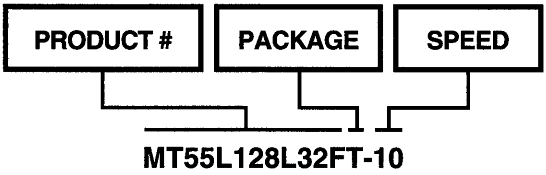
1Mb/2Mb SyncBurst™ SRAM

128K x 18 Pipelined, 5ns in Plastic TQFP (JEDEC LQFP)



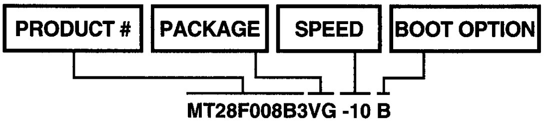
SyncBurst and ZBT™ SRAM

128K x 32 Flow-Through, 10ns in Plastic TQFP (JEDEC LQFP)



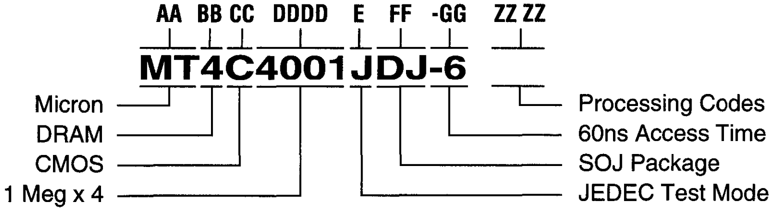
Boot Block Flash Memory

256K x 16; 3.3V V_{CC}; 3.3V, 5V or 12V V_{PP}; 100ns; bottom boot; in Plastic TSOP



ZBT and Zero Bus Turnaround are trademarks of Integrated Device Technology, Inc., and the architecture is supported by Micron Technology, Inc., and Motorola Inc.
SyncBurst is a trademark of Micron Technology, Inc.

EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product	MT

BB – PRODUCT FAMILY

DRAM	4
SRAM	5

CC – PROCESS TECHNOLOGY

CMOS	C
Low-Voltage CMOS	LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM/SRAM	Width, Density

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required.)

JEDEC Test Mode (4 Meg DRAM)	J
Errata on Base Part	Q

FF – PACKAGE CODES

PLASTIC	
DIP	Blank
DIP (Wide Body)	W
ZIP	Z
LCC	EJ
SOP/SOIC	SG
QFP	LG
TSOP (Type I)	VG
TSOP (Type I, Reversed)	XG
TSOP (Type II)	TG
TSOP (Reversed)	RG
TSOP (Longer)	TL
SOJ	DJ
SOJ (Reversed)	DR
SOJ (Longer)	DL

GG – ACCESS TIME

-4	4ns or 40ns
-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V).

Interim	I
DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh/Extended Refresh)	S
SRAMs	
Low Power	P
Low Power, Low Volt Data Retention	LP
EPI Wafer	E
Operating Temperature Range	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

---

* Used in device order codes; this code is not marked on device.

DRAM, SDRAM, SGRAM, SLDRAM AND RAMBUS™ COMPONENT NUMBERING SYSTEM

MT48LC8M8A2TG-8E ES

Micron Technology

Product Family
4 = DRAM
41 = SGRAM
45 = DDR SGRAM
46 = DDR SDRAM
48 = SDRAM
49 = SLDRAM
6 = Direct Rambus™

Process Technology
C = 5V V_{CC} CMOS
LC = 3.3V V_{DD} CMOS
V = 2.5V V_{DD} CMOS

Device Number
Depth, Width
No Letter = Bits
K = Kilobits
M = Megabits
G = Gigabits

Device Version
(For DRAM, SGRAM and SDRAM, the first character is an alphabetic character only; the second character is a numeric character only. For Rambus, DDR SGRAM, DDR SDRAM and SLDRAM, a single alphabetic character indicates database revision.)

Specified by individual data sheet.

Special Processing
ES = Engineering Sample
MS = Mechanical Sample
IT = Industrial Temperature

Refresh Option
(Multiple processing codes are separated by a space and are listed in hierarchical order.)

L = Low Power
S = Self Refresh (Designated on EDO/FPM, 16Mb SDRAM only)

Access/Cycle Time

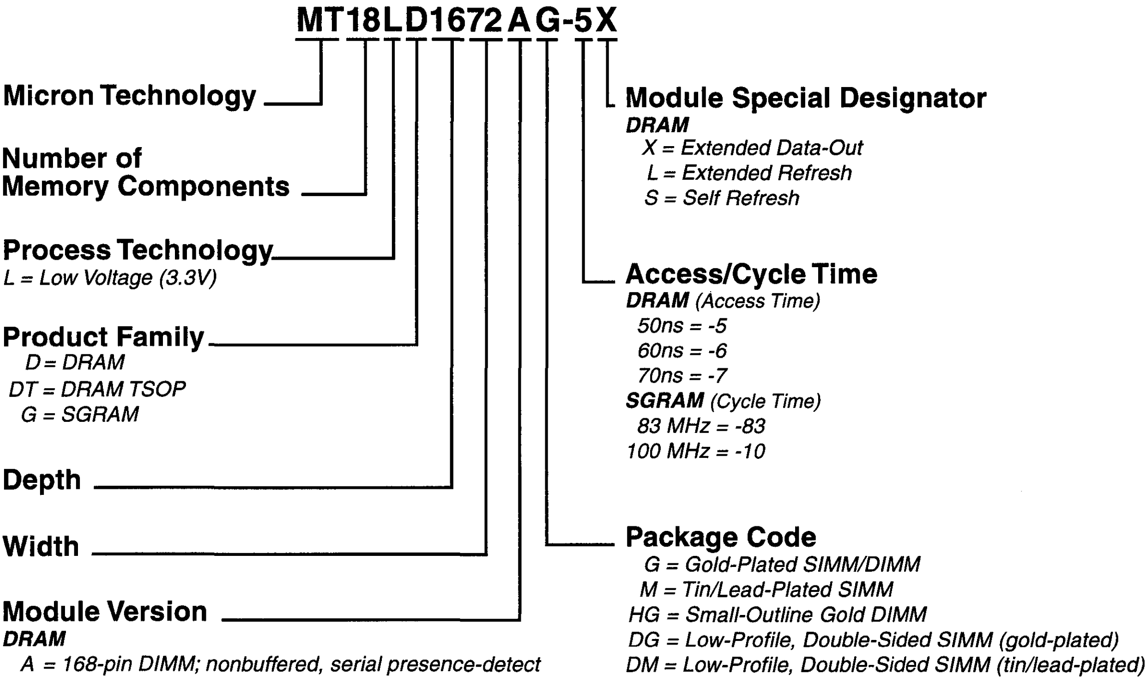
DRAM	***SGRAM, SDRAM and DDR SGRAM***
(Access Time)	*-15 = 66 MHz*
-4 = 40ns	*-12 = 83 MHz*
-5 = 50ns	*-10 = 100 MHz*
-6 = 60ns	*-8x = 125 MHz*
-7 = 70ns	*-75 = 133 MHz*
	-7 = 143 MHz
	-6 = 167 MHz

DDR SDRAM	***SLDRAM***	***Rambus***
(Cycle Time @ CL = 2)	*(Data Rate per Pin)*	*(Clock Rate)*
-10 = 100 MHz	*-400 = 400 MHz*	*-3x = 300 MHz*
-12 = 83 MHz		*-4x = 400 MHz*

Package Code
LG = TQFP
TG = TSOP (Type II)
DJ = SOJ
DW = SOJ (Wide)
FB = FBGA (CSP)
U = μBGA (CSP)

Micron Technology, Inc., reserves the right to change products or specifications without notice.

DRAM AND SGRAM MODULE NUMBERING SYSTEM



MT18LD1672AG-5X

Micron Technology

Number of Memory Components

Process Technology
L = Low Voltage (3.3V)

Product Family
D = DRAM
DT = DRAM TSOP
G = SGRAM

Depth

Width

Module Version
DRAM
A = 168-pin DIMM; nonbuffered, serial presence-detect

Module Special Designator
DRAM
X = Extended Data-Out
L = Extended Refresh
S = Self Refresh

Access/Cycle Time
***DRAM** (Access Time)*
50ns = -5
60ns = -6
70ns = -7
***SGRAM** (Cycle Time)*
83 MHz = -83
100 MHz = -10

Package Code
G = Gold-Plated SIMM/DIMM
M = Tin/Lead-Plated SIMM
HG = Small-Outline Gold DIMM
DG = Low-Profile, Double-Sided SIMM (gold-plated)
DM = Low-Profile, Double-Sided SIMM (tin/lead-plated)

SDRAM MODULE NUMBERING SYSTEM

MT 18 L SDT 1672 A G - 10E B 4

Micron Technology

Number of Memory Components

Process Technology
L = 3.3V
V = 2.5V

Product Family
SD = SDRAM
SDT = SDRAM TSOP
DDT = DDR SDRAM TSOP
VR = Rambus™

Depth

Width

Module Version
SDRAM
A = 168-pin and 184-pin DIMMs; nonbuffered, serial presence-detect
U = 100-pin DIMM; nonbuffered, serial presence-detect
G = 144-pin graphics SODIMM

Printed Circuit Board Revision Designator

Die Revision Designator

Memory Bus Speed
66 MHz CAS Latency 2 (-10 SDRAMs) = -662
100 MHz CAS Latency 3 (-8A SDRAMs) = -10A
100 MHz CAS Latency 3 (-8B SDRAMs) = -10B
100 MHz CAS Latency 3 (-8C SDRAMs) = -10C
100 MHz CAS Latency 2 (-8E SDRAMs) = -10E
133 MHz CAS Latency 3 (-75 SDRAMs) = -133
600 MHz data rate, 53ns access time = -653
600 MHz data rate, 45ns access time = -645
600 MHz data rate, 40ns access time = -640
800 MHz data rate, 53ns access time = -853
800 MHz data rate, 45ns access time = -845
800 MHz data rate, 40ns access time = -840

Package Code
G = Gold-Plated SIMM/DIMM
HG = Small-Outline Gold DIMM
DG = Low-Profile, Double-Sided DIMM

0.42µm PROCESS TECHNOLOGY
FLASH MEMORY COMPONENT NUMBERING SYSTEM

MT 28F 004 B1 VG -10 B V ET

Micron

Dual Supply Flash

28F = Dual Supply

Density/Organization

00X = x8 only (X = 2, 4, 8)
X00 = x8/x16 selectable (X = 2, 4, 8)

Voltage/Block Organization

B1 = SVT (3.3V or 5V Vcc/5V or 12V VPP), Boot Block
- *100% drop-in compatible with Intel® "BV" and "B5"*

B5 = Smart 5 (5V Vcc/5V or 12V VPP), Boot Block
- *100% drop-in compatible with Intel "B5"*

C1 = BIOS-Optimized (5V Vcc/12V VPP), Top Boot Block
- *100% drop-in compatible with Intel "BC"*
- *Also 100% drop-in compatible with Intel "BX" (top boot only)*

Package Code

VG = 40-lead TSOP Type 1
WG = 48-lead TSOP Type 1
SG = 44-lead SOP

Operating Temperature Option

Blank = Commercial (0°C to 70°C)
ET = Extended Temperature (Refer to specification)
- *Smart 5 ET*
  -40°C to +85°C
- *Low Voltage ET*
  -40°C to +85°C (3V to 3.6V)

Special Voltage Screen

Blank = None
V = 3V–3.6V Vcc Voltage

Boot Block Starting Address

T = Top Boot
- *For Intel Pentium® and x86 Processors*
- *Most 2Mb*

B = Bottom Boot
- *Most other applications*

Access Time

6 = 60ns @ 5V/90ns @ 3.3V (SmartVoltage)
8 = 80ns @ 5V/110ns @ 3.3V (SmartVoltage)
10 = 100ns

NOTE:
1. This part numbering example is provided as a reference. Please refer to the Smart 3/Smart 5 example for new design-ins and for compatibility with existing designs.
2. A cross-reference between SmartVoltage and Smart 3/Smart 5 will be available on our Web site.

0.3µm PROCESS TECHNOLOGY
FLASH MEMORY COMPONENT NUMBERING SYSTEM

MT 28F 008 B3 VG - 12 B V ET

Micron

Dual Supply Flash
28F = Dual Supply

Density/Organization
00X = x8 only (X = 2, 4, 8)
X00 = x8/x16 selectable (X = 2, 4, 8)

Voltage/Block Organization
B3 = Smart 3 (3.3V Vcc/3.3V, 5V or 12V VPP), Boot Block
B5 = Smart 5 (5V Vcc/5V or 12V VPP), Boot Block
- *100% drop-in compatible with Intel "B5"*

C5 = BIOS-Optimized (5V Vcc/12V VPP), Top Boot Block
- *100% drop-in compatible with Intel "BC"*
- *Also 100% drop-in compatible with Intel "BX" (top boot only)*

Package Code
VG = 40-lead TSOP Type 1
WG = 48-lead TSOP Type 1
SG = 44-lead SOP
FB = FBGA (6 x 8 grid, 0.8mm pitch)

Operating Temperature Option
Blank = Commercial (0°C to 70°C)
ET = Extended Temperature (Refer to specification)
- *-40°C to +85°C*

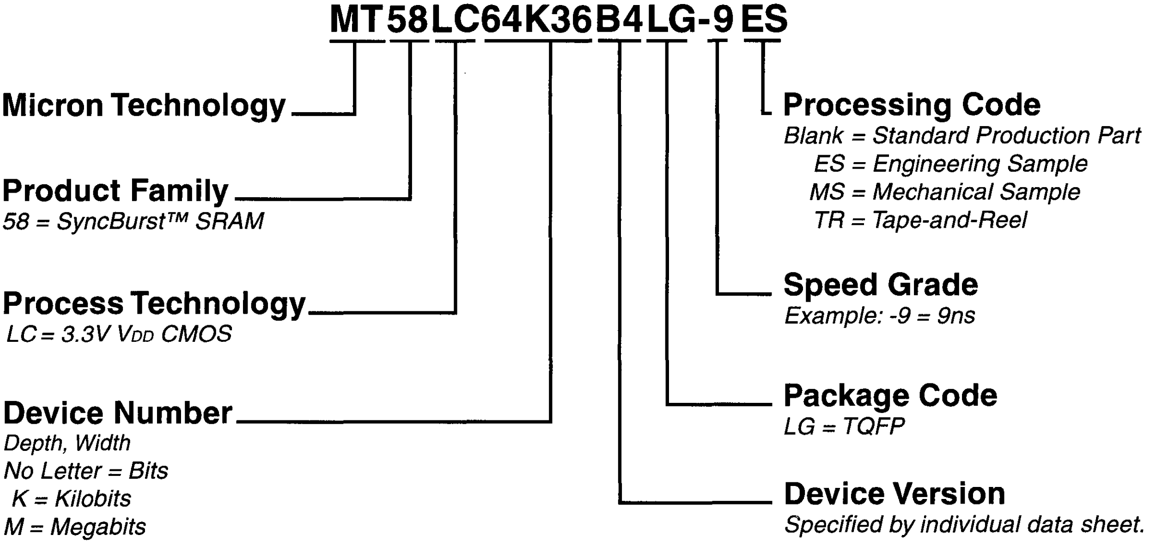
Special Voltage Screen
Blank = None
V = 2.7V–3.6V Vcc Voltage

Boot Block Starting Address
T = Top Boot
- *For Intel Pentium® and x86 Processors*
- *Most 2Mb*

B = Bottom Boot
- *Most other applications*

Access Time
Smart 3
9 = 90ns
10 = 100ns
12 = 120ns (2.7V operation only)
Smart 5
6 = 60ns
8 = 80ns

1Mb/2Mb SYNCBURST™ SRAM COMPONENT NUMBERING SYSTEM



MT58LC64K36B4LG-9ES

Micron Technology

Product Family
58 = SyncBurst™ SRAM

Process Technology
LC = 3.3V V_{DD} CMOS

Device Number
Depth, Width
No Letter = Bits
K = Kilobits
M = Megabits

Processing Code
Blank = Standard Production Part
ES = Engineering Sample
MS = Mechanical Sample
TR = Tape-and-Reel

Speed Grade
Example: -9 = 9ns

Package Code
LG = TQFP

Device Version
Specified by individual data sheet.

SYNCBURST™AND ZBT™
SRAM COMPONENT NUMBERING SYSTEM

MT58L128L36PxT-5 ES

Micron Technology

Product Family
55 = ZBT™
58 = SyncBurst

Core Voltage (VDD)
L = 3.3V
V = 2.5V

Device Depth

I/O Voltage
L = LVTTL or 3.3V
V = 2.5V

Device Width

Processing Code
Blank = Standard Production Part
ES = Engineering Sample
MS = Mechanical Sample
TR = Tape-and-Reel

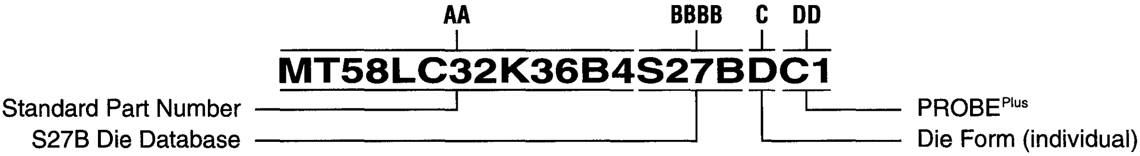
Speed Grade

Package Code
B = BGA
T = TQFP (2-chip enable)
S = TQFP (3-chip enable)

Revision *(optional)*
none, 1, 2, 3, . . .

Device Version
F = Flow-Through
P = Pipelined SCD
D= Pipelined DCD

DIE PRODUCT NUMBERING SYSTEM



AA – STANDARD PART NUMBER
(See SRAM numbering systems on previous two pages.)

BBBB – DIE DATABASE REVISION

C – FORM

Die Form	D
Wafer Form (8" Wafer)	W

DD – TESTING LEVELS (0° to 70°C)

Standard Probe	C1

Micron distributes die products through Chip Supply, Inc. For ordering information, visit their Web site (www.chipsupply.com) or call them at 407-298-7100.

ALABAMA

Sales Office

Micron Semiconductor Products, Inc.
One Cypresswood Building
9950 Cypresswood Drive, Suite 380
Houston, TX 77070
Phone - 281-970-3202
Fax - 281-970-3205

Representative

Southeast Technical Group
101 Washington Street, Suite 6
Huntsville, AL 35801
Phone - 256-534-2376
Fax - 256-534-2384

Distributors

Arrow Semiconductor Group
4930 Corporate Drive N.W., Suite G
Huntsville, AL 35805
Phone - 205-864-3300
Fax - 205-864-3349

Avnet, Inc.
4975 Bradford Drive, Suite 100
Huntsville, AL 35805
Phone - 205-837-8700
Fax - 205-830-2565

Marshall Industries
3313 Memorial Parkway South
Huntsville, AL 35801
Phone - 205-881-9235
Fax - 205-881-1490

Wyle Electronics
7800 Governors Drive West
Huntsville, AL 35806-2057
Phone - 256-830-1119
Phone - 800-964-9953
Fax - 256-830-1520

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ARIZONA

Representative

Quatra Associates, Inc.
10235 S. 51st Street, Suite 160
Phoenix, AZ 85044
Phone - 602-753-5544
Fax - 602-753-0640

Distributors

Arrow Semiconductor Group
1406 W. 14th Street, Suite 101
Tempe, AZ 85281-6909
Phone - 602-966-6600
Fax - 602-966-4826

Avnet, Inc.
2617 S. 46th Place
Phoenix, AZ 85034
Phone - 602-736-7000
Phone - 800-528-8471
Fax - 602-736-7070

Marshall Industries
9831 S. 51st Street, #C107-109
Phoenix, AZ 85044
Phone - 602-496-0290
Fax - 602-893-9029

Wyle Electronics
4602 E. University Drive, Suite 100
Phoenix, AZ 85034-7422
Phone - 602-804-7000
Fax - 602-804-0390

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ARKANSAS

Sales Office

Micron Semiconductor Products, Inc.
One Chisholm Trail, Suite 3200
Round Rock, TX 78681
Phone - 512-248-5122
Fax - 512-248-5192

Distributors

Avnet, Inc.
12206 E. 51st Street, Suite 103
Tulsa, OK 74146
Phone - 918-459-6000
Fax - 918-459-6060

Wyle Electronics
1810 N. Greenville Avenue
Richardson, TX 75081-1876
Phone - 972-235-9953
Fax - 972-644-5064

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

BRITISH COLUMBIA

Representative

Cascade Technical Sales
25 Central Way, #200
Kirkland, WA 98033
Phone - 425-822-7299
Fax - 425-822-7479

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

CALIFORNIA - NORTHERN

Sales Office

Micron Semiconductor Products, Inc.
4051 Burton Drive
Santa Clara, CA 95054
Phone - 408-588-1309
Fax - 408-588-1316

Representatives

Bay Area Electronics Sales, Inc.
9119 Eden Oak Circle
Granite Bay, CA 95746
Phone - 916-652-6777
Fax - 916-652-5678

Bay Area Electronics Sales, Inc.
2001 Gateway Place, Suite 315 W.
San Jose, CA 95110
Phone - 408-452-8133
Fax - 408-452-8139

Distributors

Arrow Semiconductor Group
1350 McCandless Drive
Milpitas, CA 95035
Phone - 408-935-4712
Fax - 408-935-4688

Arrow Semiconductor Group
1680 McCandless Drive, Bldg. 3
Milpitas, CA 95035-8000
Phone - 408-453-1200
Fax - 408-441-4504

Arrow Semiconductor Group
580 Menlo Drive, Suite 8
Rocklin, CA 95765-3706
Phone - 916-624-9744
Fax - 916-624-9750

Avnet, Inc.
580 Menlo Drive, Suite 2
Rocklin, CA 95765
Phone - 916-624-9781
Fax - 916-961-0922

Avnet, Inc.
2105 Lundy Avenue
San Jose, CA 95131-1849
Phone - 408-435-3500
Fax - 408-435-3765

Marshall Industries
336 Los Coches Street
Milpitas, CA 95035
Phone - 408-942-4600
Fax - 408-262-1224

Marshall Industries
2941 Sunrise Blvd., Suite 130
Rancho Cordova, CA 95742
Phone - 916-635-9700
Fax - 916-635-6044

Wyle Electronics
3000 Bowers Avenue
Santa Clara, CA 95051-0942
Phone - 408-727-2500
Phone - 800-866-9953
Fax - 408-988-2747

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

CALIFORNIA - SOUTHERN

Sales Office

Micron Semiconductor Products, Inc.
San Diego, CA 92121
Phone - 619-452-2042
Fax - 619-452-1683

Representatives

Platinum Associates
30 Corporate Park, Suite 106
Irvine, CA 92606
Phone - 949-851-2477
Fax - 949-851-2252

Platinum Associates
6540 Lusk Blvd., Suite C241
San Diego, CA 92121
Phone - 619-824-0077
Fax - 619-824-2957

Platinum Associates
5743 Corsa Avenue, Suite 112
Westlake Village, CA 91362
Phone - 818-879-5900
Fax - 818-879-5905

Distributors

Arrow Semiconductor Group
Malibu Canyon Business Park
26677 W. Agoura Road
Calabasas, CA 91302-1959
Phone - 818-880-9686
Fax - 818-880-4687

Arrow Semiconductor Group
6 Cromwell Street, Suite 100
Irvine, CA 92618-1816
Phone - 714-587-0404
Fax - 714-454-4206

Arrow Semiconductor Group
9511 Ridgehaven Court
San Diego, CA 92123-1688
Phone - 619-565-4800
Fax - 619-279-0862

Avnet, Inc.
140 Technology Drive, Suite 400
Irvine, CA 92618
Phone - 714-789-4100
Fax - 714-789-6064

Avnet, Inc.
4545 Viewridge Avenue
San Diego, CA 92123
Phone - 619-571-7540
Fax - 619-277-6136

Avnet, Inc.
21155 Califa Street
Woodland Hills, CA 91367
Phone - 818-594-8292
Fax - 818-594-8293

Marshall Industries
9320 Telstar Avenue
El Monte, CA 91731
Phone - 626-307-6000
Fax - 626-307-6173

Marshall Industries
One Morgan
Irvine, CA 92618
Phone - 949-458-5301
Fax - 949-581-5255

Marshall Industries
5961 Kearny Villa Road
San Diego, CA 92123
Phone - 619-627-4140
Fax - 619-627-4163

Marshall Industries
558 St. Charles Drive, Suite 200
Thousand Oaks, CA 91360-3903
Phone - 805-370-5100
Fax - 805-370-1988

Wyle Electronics
26010 Mureau Road, Suite 150
Calabasas, CA 91302-3171
Phone - 818-880-9000
Phone - 800-288-9953
Fax - 818-880-5510

Wyle Electronics
29A Technology Drive
Irvine, CA 92618-2302
Phone - 949-789-9953
Fax - 949-789-9960

Wyle Electronics
165 Technology Drive
Irvine, CA 92618-2402
Phone - 949-789-9953
Fax - 949-789-9877

Wyle Electronics
3300 Douglas Blvd., Suite 105
Roseville, CA 95661
Phone - 916-783-9953
Fax - 916-772-4220

Wyle Electronics
6165 Greenwich Drive, Suite 110
San Diego, CA 92122-5910
Phone - 619-558-6600
Fax - 619-558-2210

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

CANADA - EASTERN

Representatives

Tech-Trek Ltd.
155 Terrace Matthews Cres., Unit 7
Kanata, ON K2M 2A8
Phone - 613-599-8787
Fax - 613-599-8931

Tech-Trek Ltd.
1015 Matheson Blvd., Unit 6
Mississauga, ON L4W 3A4
Phone - 905-238-0366
Fax - 905-238-0319

Tech-Trek Ltd.
2271 Guenette Street
Ville St. Laurent, PQ H4R 2E9
Phone - 514-337-7540
Fax - 514-337-7544

Distributors

Arrow Semiconductor Group
1255 Trans Canada Hwy., Suite 100
Dorval, PQ H9P 2V4
Phone - 514-421-7411
Fax - 514-421-7430

Arrow Semiconductor Group
1093 Meyerside Drive, Unit 2
Mississauga, ON L5T 1M4
Phone - 905-670-7769
Fax - 905-670-7781

Arrow Semiconductor Group
36 Antares Drive, Unit 100
Nepean, ON K2E 7W5
Phone - 613-226-6903
Fax - 613-723-2018

Avnet, Inc.
190 Colonnade Road
Nepean, ON K2E 7J5
Phone - 613-226-1700
Fax - 613-226-1184

Avnet, Inc.
7575 Trans Canada Hwy., Suite 600
Ville St. Laurent, PQ H4T 1V6
Phone - 514-335-1000
Fax - 514-335-2481

Marshall Industries
6285 Northam Drive, Suite 112
Mississauga, ON 14V 1X5
Phone - 905-612-1771
Fax - 905-612-1988

Marshall Industries
148 Brunswick Blvd.
Pointe Claire, Quebec H9R 5P9
Phone - 514-694-8142
Fax - 514-694-6989

Marshall Industries
2620 Dalton Street, Unit 103
Ste Foy, Quebec G1P 3S4
Phone - 418-656-1162
Fax - 418-656-1067

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

CANADA - WESTERN

Sales Office

Micron Semiconductor Products, Inc.
1600 N.W. Compton Drive, Suite 206
Beaverton, OR 97006
Phone - 503-531-2010
Fax - 503-531-2011

Representative

Tech-Trek Ltd.
1725 30th Ave., NE. Bay 5
Calgary, AB T2E 7P6
Phone - 403-291-6866
Fax - 403-291-6838

Distributors

Arrow Semiconductor Group
8555 Commerce Court
Burnaby, BC V5A 4N4
Phone - 604-421-2333
Fax - 604-421-5030

Avnet, Inc.
8610 Commerce Court
Burnaby, BC V5A 4N6
Phone - 604-420-4101
Fax - 604-420-5376

Marshall Industries
4170 Still Creek Drive, Suite 200
Burnaby, BC V5C 6C6
Phone - 604-294-6506
Fax - 604-294-6520

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

COLORADO

Representative

Wescom Marketing
11907 West I-70 Frontage Road
Wheat Ridge, CO 80033
Phone - 303-432-6809
Fax - 303-422-9892

Distributors

Arrow Semiconductor Group
7459 S. Lima Street
Englewood, CO 80112-5816
Phone - 303-799-0258
Fax - 303-799-0730

Avnet, Inc.
12600 E. Arapahoe Road
Englewood, CO 80112
Phone - 303-790-1662
Fax - 303-790-4991

Marshall Industries
7575 West 103rd Avenue, Suite 100
Westminister, CO 80021
Phone - 303-460-0477
Fax - 303-460-0083

Wyle Electronics
451 E. 124th Avenue
Thornton, CO 80241-2402
Phone - 303-457-9953
Phone - 800-933-9953
Fax - 303-457-4831

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

CONNECTICUT

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

Advanced Tech Sales, Inc.
Bldg. 2, Suite 1C
850 N. Main Street Extension
Wallingford, CT 06492
Phone - 203-284-9762
Fax - 203-284-8232

Distributors

Arrow Semiconductor Group
860 N. Main Street Ext.
Wallingford, CT 06492-2419
Phone - 203-265-7741
Fax - 203-265-7988

Avnet, Inc.
1157 Highland Ave., Suite 207
Cheshire, CT 06410
Phone - 203-271-2844
Fax - 203-272-1704

Marshall Industries
Barnes Industrial Park North
20 Sterling Drive
Wallingford, CT 06492-0200
Phone - 203-265-3822
Fax - 203-284-9285

Wyle Electronics
1062 Barnes Road, Suite 300
Wallingford, CT 06492-2576
Phone - 203-269-8077
Fax - 203-269-7507

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

DELAWARE

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

Delta Technical Sales, Inc.
122 North York Road, Suite 9
Hatboro, PA 19040
Phone - 215-957-0600
Fax - 215-957-0920

Distributors

Avnet, Inc.
7000 Atrium Way, Suite 6
Mt. Laurel, NJ 08054
Phone - 609-222-6400
Fax - 609-222-6464

Marshall Industries
Barnes Industrial Park North
20 Sterling Drive
Wallingford, CT 06492-0200
Phone - 203-265-3822
Fax - 203-284-9285

Wyle Electronics
815 East Gate Drive
Mt. Laurel, NJ 08054-1208
Phone - 800-871-9953
Fax - 609-439-9020

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

DISTRICT OF COLUMBIA

Representative

EES, Inc.
4302 Mountain Road, Suite B
Pasadena, MD 21122
Phone - 410-255-9686
Fax - 410-255-9688

Distributors

Avnet, Inc.
7134 Columbia Gateway Drive, Suite 100
Columbia, MD 21046
Phone - 410-988-9800
Phone - 800-638-5988
Fax - 410-720-3421

Wyle Electronics
7180 Columbia Gateway Drive, Suite 100
Columbia, MD 21046-2132
Phone - 410-312-4844
Phone - 800-863-9953
Fax - 410-312-4953

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

FLORIDA

Sales Office

Micron Semiconductor Products, Inc.
One Cypresswood Building
9950 Cypresswood Drive, Suite 380
Houston, TX 77070
Phone - 281-970-3202
Fax - 281-970-3205

Representatives

Mega Technologies, Inc.
Phone - 813-797-8222
Fax - 813-797-8375

Mega Technologies, Inc.
Phone - 954-563-1882
Fax - 954-563-9825

Mega Technologies, Inc.
1600 Sarno Road, Suite 21
Melbourne, FL 32935
Phone - 407-752-6767
Fax - 407-752-7484

Distributors

Arrow Semiconductor Group
400 Fairway Drive, Suite 101-104A
Deerfield Beach, FL 33441-1884
Phone - 954-429-8200
Fax - 954-428-3991

Arrow Semiconductor Group
Bldg. D
37 Skyline Drive, Suite 3101-3
Lake Mary, FL 32746-6200
Phone - 407-333-9300
Fax - 407-333-9320

Avnet, Inc.
5516 Rio Vista Drive
Clearwater, FL 33760
Phone - 813-507-5000
Fax - 813-507-5050

Avnet, Inc.
3350 N.W. 53rd Street, Suite 105
Ft. Lauderdale, FL 33309
Phone - 954-484-5482
Fax - 954-484-4740

Avnet, Inc.
7079 University Blvd.
Winter Park, FL 32792
Phone - 407-657-3300
Fax - 407-678-4414

Marshall Industries
380 S. Northlake Blvd., #1024
Altamonte Springs, FL 32701
Phone - 407-767-8585
Fax - 407-767-8676

Marshall Industries
Hillsboro Executive Center North
600 Fairway Drive, Suite 210
Deerfield Beach, FL 33441
Phone - 954-422-8600
Fax - 954-571-9844

Marshall Industries
2840 Scherer Drive, #410
St. Petersburg, FL 33716
Phone - 813-573-1399
Fax - 813-573-9252

Wyle Electronics
5665 Rio Vista Drive
Clearwater, FL 33760
Phone - 727-533-0445
Phone - 800-395-9953
Fax - 727-533-0454

Wyle Electronics
Bldg. 1, Suite 101
700 W. Hillsboro Blvd.
Deerfield Beach, FL 33441
Phone - 954-420-0500
Fax - 954-428-2134

Wyle Electronics
100 E. Sybelia Avenue, Suite 380
Maitland, FL 32751
Phone - 407-740-7450
Fax - 407-740-8037

Wyle Electronics
1000 112th Circle N., Suite 800
St. Petersburg, FL 33716-2306
Phone - 813-576-3004
Fax - 813-579-1518

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

GEORGIA

Sales Office

Micron Semiconductor Products, Inc.
One Cypresswood Building
9950 Cypresswood Drive, Suite 380
Houston, TX 77070
Phone - 281-970-3202
Fax - 281-970-3205

Representative

Southeast Technical Group
6045 Atlantic Blvd.
Norcross, GA 30071
Phone - 770-239-7576
Fax - 770-239-7589

Distributors

Arrow Semiconductor Group
4250E River Green Pkwy., Suite E
Duluth, GA 30136-2562
Phone - 770-497-1300
Fax - 770-476-1493

Avnet, Inc.
3475 Corporate Way, Suite D
Duluth, GA 30136
Phone - 770-623-4400
Fax - 770-476-8806

Marshall Industries
4500 River Green Pkwy., #100
Duluth, GA 30096
Phone - 770-814-9393
Fax - 770-814-9619

Wyle Electronics
11465 Johns Creek Parkway, Suite 160
Duluth, GA 30097
Phone - 770-495-9770
Phone - 800-876-9953
Fax - 770-495-1915

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

HAWAII

Representative

Bay Area Electronics Sales, Inc.
2001 Gateway Place, Suite 315 W.
San Jose, CA 95110
Phone - 408-452-8133
Fax - 408-452-8139

Distributors

Avnet, Inc.
2105 Lundy Avenue
San Jose, CA 95131-1849
Phone - 408-435-3500
Fax - 408-435-3765

Wyle Electronics
3000 Bowers Avenue
Santa Clara, CA 95051-0942
Phone - 408-727-2500
Phone - 800-866-9953
Fax - 408-988-2747

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

IDAHO

Sales Office

Micron Semiconductor Products, Inc.
8000 S. Federal Way
P. O. Box 6
Boise, ID 83707-0006
Phone - 208-368-3900
Fax - 208-368-4617

Representative

Wescom Marketing
10378 Fairview Avenue #246
Boise, ID 83704
Phone - 208-377-5585
Fax - 208-378-0228

Distributors

Avnet, Inc.
2105 Lundy Avenue
San Jose, CA 95131-1849
Phone - 408-435-3500
Fax - 408-435-3765

Wyle Electronics
1325 W. 2200 S., Suite E
West Valley City, UT 84119-1467
Phone - 801-974-9953
Fax - 801-972-2524

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ILLINOIS - NORTHERN

Representative

High Technology Sales
1111 Plaza Drive, Suite 102
Schaumburg, IL 60173
Phone - 847-517-7655
Fax - 847-517-7656

Distributors

Avnet, Inc.
3030 Salt Creek Lane, Suite 300
Arlington Heights, IL 60005
Phone - 847-797-7300
Fax - 847-797-7713

Marshall Industries
50 E. Commerce Drive, Unit 1
Schaumburg, IL 60173
Phone - 847-490-0155
Fax - 847-490-0569

Wyle Electronics
2055 Army Trail Road, Suite 140
Addison, IL 60101-1478
Phone - 630-620-0969
Fax - 630-620-1610

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ILLINOIS - SOUTHERN

Representative

CenTech, Inc.
3751 Pennridge Drive, Suite 107
Bridgeton, MO 63044
Phone - 314-291-4230
Fax - 314-291-4232

Distributors

Arrow Semiconductor Group
1166 Springlake Drive
Itasca, IL 60143-2062
Phone - 630-285-0043
Fax - 630-860-8598

Avnet, Inc.
3030 Salt Creek Lane, Suite 300
Arlington Heights, IL 60005
Phone - 847-797-7300
Fax - 847-797-7713

Marshall Industries
50 E. Commerce Drive, Unit 1
Schaumburg, IL 60173
Phone - 847-490-0155
Fax - 847-490-0569

Wyle Electronics
2055 Army Trail Road, Suite 140
Addison, IL 60101-1478
Phone - 630-620-0969
Fax - 630-620-1610

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

INDIANA

Representative

MaxTech Marketing
4 Sycamore Creek Drive
Springboro, OH 45066
Phone - 724-775-4413
Fax - 724-775-4418

Distributors

Arrow Semiconductor Group
7108 Lakeview Parkway W. Drive
Indianapolis, IN 46268-4104
Phone - 317-299-2071
Fax - 317-299-2379

Avnet, Inc.
655 West Carmel Drive, Suite 160
Carmel, IN 46032
Phone - 317-575-3555
Fax - 317-575-3535

Marshall Industries
5933 Lakeside Blvd.
Indianapolis, IN 46278
Phone - 317-388-9069
Fax - 317-388-9073

Wyle Electronics
2055 Army Trail Road, Suite 140
Addison, IL 60101-1478
Phone - 630-620-0969
Fax - 630-620-1610

Wyle Electronics
237 Airport North Office Park
Ft. Wayne, IN 46825
Phone - 219-490-2323
Fax - 219-497-8235

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

IOWA

Representative

High Technology Sales
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
Fax - 612-844-9930

Distributors

Avnet, Inc.
2335-A Blairs Ferry Road N.E.
Cedar Rapids, IA 52402
Phone - 319-393-0033
Fax - 319-393-7050

Wyle Electronics
1325 E. 79th Street, Suite 1
Bloomington, MN 55425
Phone - 612-853-2280
Fax - 612-853-2298

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

KANSAS

Representative

CenTech, Inc.
10312 E. 63rd Terrace
Raytown, MO 64133
Phone - 816-358-8100
Fax - 816-358-8107

Distributors

Avnet, Inc.
9200 Indian Creek Pkwy., Suite 200
Overland Park, KS 66210
Phone - 913-663-7900
Fax - 913-663-7979

Marshall Industries
Pine Ridge Business Park
10413 W. 84th Terrace
Lenexa, KS 66214
Phone - 913-492-3121
Fax - 913-492-6205

Wyle Electronics
2055 Army Trail Road, Suite 140
Addison, IL 60101-1478
Phone - 630-620-0969
Fax - 630-620-1610

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

KENTUCKY - EASTERN

Representative

MaxTech Marketing
4 Sycamore Creek Drive
Springboro, OH 45066
Phone - 724-775-4413
Fax - 724-775-4418

Distributors

Avnet, Inc.
777 Dearborn Park Lane, Suite L
Worthington, OH 43085
Phone - 614-888-3313
Fax - 614-888-0767

Marshall Industries
5933 Lakeside Blvd.
Indianapolis, IN 46278
Phone - 317-388-9069
Fax - 317-388-9073

Wyle Electronics
3493 Newmark Drive
Miamisburg, OH 45342-5426
Phone - 937-436-9953
Fax - 937-436-1780

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

KENTUCKY - WESTERN

Representative

MaxTech Marketing
4 Sycamore Creek Drive
Springboro, OH 45066
Phone - 724-775-4413
Fax - 724-775-4418

Distributors

Avnet, Inc.
655 West Carmel Drive, Suite 160
Carmel, IN 46032
Phone - 317-575-3555
Fax - 317-575-3535

Marshall Industries
5933 Lakeside Blvd.
Indianapolis, IN 46278
Phone - 317-388-9069
Fax - 317-388-9073

Wyle Electronics
2055 Army Trail Road, Suite 140
Addison, IL 60101-1478
Phone - 630-620-0969
Fax - 630-620-1610

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

LOUISIANA

Sales Office

Micron Semiconductor Products, Inc.
One Chisholm Trail, Suite 3200
Round Rock, TX 78681
Phone - 512-248-5122
Fax - 512-248-5192

Distributor

Wyle Electronics
1810 N. Greenville Avenue
Richardson, TX 75081-1876
Phone - 972-235-9953
Fax - 972-644-5064

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MAINE

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

Advanced Tech Sales, Inc.
352 Park Street, Suite 102
North Reading, MA 01864
Phone - 978-664-0888
Fax - 978-664-5503

Distributors

Avnet, Inc.
10 M Centennial Drive
Peabody, MA 01960
Phone - 508-532-9893
Phone - 800-845-8416
Fax - 508-532-9713

Wyle Electronics
5 Oak Park Drive
Bedford, MA 01730-1413
Phone - 781-271-9953
Fax - 781-275-3809

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MARYLAND

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

EES, Inc.
4302 Mountain Road, Suite B
Pasadena, MD 21122
Phone - 410-255-9686
Fax - 410-255-9688

Distributors

Arrow Semiconductor Group
9800J Patuxent Woods Drive
Columbia, MD 21046-1561
Phone - 410-309-0686
Fax - 410-309-0699

Avnet, Inc.
7134 Columbia Gateway Drive, Suite 100
Columbia, MD 21046
Phone - 410-988-9800
Phone - 800-638-5988
Fax - 410-720-3421

Marshall Industries
9130 Guilford Road, #B
Columbia, MD 21046
Phone - 410-880-3030
Fax - 410-880-3202

Wyle Electronics
7180 Columbia Gateway Drive, Suite 100
Columbia, MD 21046-2132
Phone - 410-312-4844
Phone - 800-863-9953
Fax - 410-312-4953

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MASSACHUSETTS

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

Advanced Tech Sales, Inc.
352 Park Street, Suite 102
North Reading, MA 01864
Phone - 978-664-0888
Fax - 978-664-5503

Distributors

Arrow Semiconductor Group
25 Upton Drive
Wilmington, MA 01887
Phone - 508-658-0900
Fax - 508-694-1754

Avnet, Inc.
10 M Centennial Drive
Peabody, MA 01960
Phone - 508-532-9893
Phone - 800-845-8416
Fax - 508-532-9713

Marshall Industries
33 Upton Drive
Wilmington, MA 01887
Phone - 978-658-0810
Fax - 978-657-5931

Wyle Electronics
5 Oak Park Drive
Bedford, MA 01730-1413
Phone - 781-271-9953
Fax - 781-275-3809

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MICHIGAN

Representative

Rathsburg Associates, Inc.
41100 Bridge Street
Novi, MI 48375
Phone - 248-615-4000
Fax - 248-615-4001

Distributors

Arrow Semiconductor Group
44720 Helm Street
Plymouth, MI 48170-6019
Phone - 734-455-0850
Fax - 734-455-6656

Avnet, Inc.
44191 Plymouth Oaks Blvd., #1300
Plymouth, MI 48170
Phone - 313-416-5800
Fax - 313-416-4106

Marshall Industries
44099 Plymouth Oaks Blvd., Suite 102
Plymouth, MI 48170
Phone - 734-254-0943
Fax - 734-254-0967

Wyle Electronics
26200 Town Center Drive
Novi, MI 48375
Phone - 248-374-9953
Fax - 248-374-1140

Wyle Electronics
Solon Business Park, Bldg. B
30600 Aurora Road, Suite 180
Solon, OH 44139-2761
Phone - 440-248-9996
Phone - 800-763-9953
Fax - 440-248-5490

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MINNESOTA

Representative

High Technology Sales
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
Fax - 612-844-9930

Distributors

Arrow Semiconductor Group
7690 Golden Triangle Drive
Eden Prairie, MN 55344-3732
Phone - 612-944-5454
Fax - 612-944-3045

Avnet, Inc.
9401 James Avenue S., Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
Fax - 612-881-9461

Marshall Industries
14800 28th Avenue North, #175
Plymouth, MN 55447
Phone - 612-559-2211
Fax - 612-559-8321

Wyle Electronics
1325 E. 79th Street, Suite 1
Bloomington, MN 55425
Phone - 612-853-2280
Fax - 612-853-2298

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MISSISSIPPI

Sales Office

Micron Semiconductor Products, Inc.
One Cypresswood Building
9950 Cypresswood Drive, Suite 380
Houston, TX 77070
Phone - 281-970-3202
Fax - 281-970-3205

Representative

Southeast Technical Group
101 Washington Street, Suite 6
Huntsville, AL 35801
Phone - 256-534-2376
Fax - 256-534-2384

Distributors

Avnet, Inc.
7079 University Blvd.
Winter Park, FL 32792
Phone - 407-657-3300
Fax - 407-678-4414

Wyle Electronics
7800 Governors Drive West
Huntsville, AL 35806-2057
Phone - 256-830-1119
Phone - 800-964-9953
Fax - 256-830-1520

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MISSOURI

Representatives

CenTech, Inc.
3751 Pennridge Drive, Suite 107
Bridgeton, MO 63044
Phone - 314-291-4230
Fax - 314-291-4232

CenTech, Inc.
10312 E. 63rd Terrace
Raytown, MO 64133
Phone - 816-358-8100
Fax - 816-358-8107

Distributors

Avnet, Inc.
3783 Rider Trail S.
Earth City, MO 63045
Phone - 314-770-6300
Fax - 314-770-6363

Marshall Industries
514 Earth City Expressway, Suite 131
Earth City, MO 63045
Phone - 314-770-1749
Fax - 314-770-1486

Wyle Electronics
2055 Army Trail Road, Suite 140
Addison, IL 60101-1478
Phone - 630-620-0969
Fax - 630-620-1610

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MONTANA

Sales Office

Micron Semiconductor Products, Inc.
8000 S. Federal Way
P. O. Box 6
Boise, ID 83707-0006
Phone - 208-368-3900
Fax - 208-368-4617

Distributors

Avnet, Inc.
2105 Lundy Avenue
San Jose, CA 95131-1849
Phone - 408-435-3500
Fax - 408-435-3765

Wyle Electronics
451 E. 124th Avenue
Thornton, CO 80241-2402
Phone - 303-457-9953
Phone - 800-933-9953
Fax - 303-457-4831

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEBRASKA

Representative

CenTech, Inc.
10312 E. 63rd Terrace
Raytown, MO 64133
Phone - 816-358-8100
Fax - 816-358-8107

Distributors

Avnet, Inc.
9200 Indian Creek Pkwy., Suite 200
Overland Park, KS 66210
Phone - 913-663-7900
Fax - 913-663-7979

Wyle Electronics
451 E. 124th Avenue
Thornton, CO 80241-2402
Phone - 303-457-9953
Phone - 800-933-9953
Fax - 303-457-4831

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEVADA - NORTHERN

Representatives

Bay Area Electronics Sales, Inc.
9119 Eden Oak Circle
Granite Bay, CA 95746
Phone - 916-652-6777
Fax - 916-652-5678

Bay Area Electronics Sales, Inc.
2001 Gateway Place, Suite 315 W.
San Jose, CA 95110
Phone - 408-452-8133
Fax - 408-452-8139

Distributors

Avnet, Inc.
2105 Lundy Avenue
San Jose, CA 95131-1849
Phone - 408-435-3500
Fax - 408-435-3765

Marshall Industries
#4 Sunset Way, Bldg. C
Henderson, NV 89014
Phone - 702-436-1800
Fax - 702-436-1860

Wyle Electronics
3300 Douglas Blvd., Suite 105
Roseville, CA 95661
Phone - 916-783-9953
Fax - 916-772-4220

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEVADA - SOUTHERN

Representative

Quatra Associates, Inc.
10235 S. 51st Street, Suite 160
Phoenix, AZ 85044
Phone - 602-753-5544
Fax - 602-753-0640

Distributors

Avnet, Inc.
2617 S. 46th Place
Phoenix, AZ 85034
Phone - 602-736-7000
Phone - 800-528-8471
Fax - 602-736-7070

Marshall Industries
#4 Sunset Way, Bldg. C
Henderson, NV 89014
Phone - 702-436-1800
Fax - 702-436-1860

Wyle Electronics
2785 E. Desert Inn Road, Suite 170
Las Vegas, NV 89121-3623
Phone - 702-765-7117
Fax - 702-765-7130

Wyle Electronics
4602 E. University Drive, Suite 100
Phoenix, AZ 85034-7422
Phone - 602-804-7000
Fax - 602-804-0390

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEW HAMPSHIRE

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

Advanced Tech Sales, Inc.
352 Park Street, Suite 102
North Reading, MA 01864
Phone - 978-664-0888
Fax - 978-664-5503

Distributors

Avnet, Inc.
10 M Centennial Drive
Peabody, MA 01960
Phone - 508-532-9893
Phone - 800-845-8416
Fax - 508-532-9713

Wyle Electronics
5 Oak Park Drive
Bedford, MA 01730-1413
Phone - 781-271-9953
Fax - 781-275-3809

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEW JERSEY - NORTHERN

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

Parallax, Inc.
734 Walt Whitman Road, Suite 209
Melville, NY 11747
Phone - 516-351-1000
Fax - 516-351-1606

Distributors

Arrow Semiconductor Group
26 Chapin Road, Unit 1112
Pine Brook, NJ 07058-4416
Phone - 973-227-7960
Fax - 201-227-9246

Avnet, Inc.
7000 Atrium Way, Suite 6
Mt. Laurel, NJ 08054
Phone - 609-222-6400
Fax - 609-222-6464

Avnet, Inc.
10 Lanidex Plaza West
Parsippany, NJ 07054
Phone - 201-515-1641
Fax - 201-515-1600

Marshall Industries
101 Fairfield Road
Fairfield, NJ 07006
Phone - 973-882-0320
Fax - 973-882-0095

Marshall Industries
158 Gaither Drive, #100
Mt. Laurel, NJ 08054
Phone - 609-234-9100
Fax - 609-778-1819

Wyle Electronics
20 Chapin Road, Suite 1013
Pinebrook, NJ 07058-9718
Phone - 973-882-8358
Fax - 973-882-9109

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEW JERSEY - SOUTHERN

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

Delta Technical Sales, Inc.
122 North York Road, Suite 9
Hatboro, PA 19040
Phone - 215-957-0600
Fax - 215-957-0920

Distributors

Avnet, Inc.
7000 Atrium Way, Suite 6
Mt. Laurel, NJ 08054
Phone - 609-222-6400
Fax - 609-222-6464

Marshall Industries
101 Fairfield Road
Fairfield, NJ 07006
Phone - 973-882-0320
Fax - 973-882-0095

Marshall Industries
158 Gaither Drive, #100
Mt. Laurel, NJ 08054
Phone - 609-234-9100
Fax - 609-778-1819

Wyle Electronics
815 East Gate Drive
Mt. Laurel, NJ 08054-1208
Phone - 800-871-9953
Fax - 609-439-9020

Wyle Electronics
660 Kinderkamack Road
Oradell, NJ 07649
Phone - 201-261-3200
Fax - 201-261-2729

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEW MEXICO

Representative

Quatra Associates, Inc.
600 Autumnwood Place S.E.
Albuquerque, NM 87123
Phone - 505-296-6781
Fax - 505-292-2092

Distributors

Avnet, Inc.
2601 Wyoming N.E., Suite 110
Albuquerque, NM 87112
Phone - 505-293-5119
Phone - 800-489-7654
Fax - 505-293-7512

Avnet, Inc.
2617 S. 46th Place
Phoenix, AZ 85034
Phone - 602-736-7000
Phone - 800-528-8471
Fax - 602-736-7070

Wyle Electronics
4602 E. University Drive, Suite 100
Phoenix, AZ 85034-7422
Phone - 602-804-7000
Fax - 602-804-0390

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEW YORK - NORTHERN

Representatives

Electra Sales Corporation
6057 Corporate Drive
East Syracuse, NY 13057
Phone - 315-463-1248
Fax - 315-463-1717

Electra Sales Corporation
333 Metro Park
Rochester, NY 14623
Phone - 716-427-7860
Fax - 716-427-0614

Distributors

Arrow Semiconductor Group
47 Mall Drive
Commack, NY 11725-5717
Phone - 516-864-6600
Fax - 516-493-2244

Arrow Semiconductor Group
3375 Brighton-Henrietta Townline Road
Rochester, NY 14623-2898
Phone - 716-427-0300
Fax - 716-427-0735

Avnet, Inc.
1057 E. Henrietta Road
Rochester, NY 14623
Phone - 716-475-9130
Fax - 716-475-9119

Marshall Industries
100 Marshall Drive
Endicott, NY 13760
Phone - 607-785-2345
Fax - 607-785-5546

Marshall Industries
1250 Scottsville Road
Rochester, NY 14624
Phone - 716-235-7620
Fax - 716-235-0052

Wyle Electronics
395 Summit Point Drive, Suite 1
Henrietta, NY 14467-9609
Phone - 716-334-5970
Fax - 716-334-6607

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEW YORK - SOUTHERN

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

Parallax, Inc.
734 Walt Whitman Road, Suite 209
Melville, NY 11747
Phone - 516-351-1000
Fax - 516-351-1606

Distributors

Avnet, Inc.
390 Rabro Drive
Hauppauge, NY 11788
Phone - 516-434-7400
Fax - 516-434-7491

Marshall Industries
3555 Veterans Memorial Hwy., Suite J
Ronkonkoma, NY 11779
Phone - 516-737-9300
Fax - 516-737-9302

Wyle Electronics
330 Motor Parkway, Suite 108
Hauppauge, NY 11788-5117
Phone - 516-231-7850
Fax - 516-231-8079

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NORTH CAROLINA

Sales Office

Micron Semiconductor Products, Inc.
One Cypresswood Building
9950 Cypresswood Drive, Suite 380
Houston, TX 77070
Phone - 281-970-3202
Fax - 281-970-3205

Representative

Southeast Technical Group
207 New Edition Court
Cary, NC 27511
Phone - 919-468-1524
Fax - 919-468-1534

Distributors

Arrow Semiconductor Group
1517 October Road
Raleigh, NC 27614
Phone - 919-676-5782
Fax - 919-518-1205

Arrow Semiconductor Group
5240 Greens Dairy Road
Raleigh, NC 27616-4600
Phone - 919-876-3132
Fax - 919-878-9517

Avnet, Inc.
5234 Greens Dairy Road
Raleigh, NC 27604
Phone - 919-872-0712
Phone - 800-662-7947
Fax - 919-878-8729

Marshall Industries
5224 Greens Dairy Road
Raleigh, NC 27616
Phone - 919-878-9882
Fax - 919-872-2431

Wyle Electronics
2200 Gateway Centre Blvd., Suite 208
Morrisville, NC 27560-9122
Phone - 919-469-1502
Fax - 919-469-0424

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NORTH DAKOTA

Representative

High Technology Sales
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
Fax - 612-844-9930

Distributors

Avnet, Inc.
9401 James Avenue S., Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
Fax - 612-881-9461

Wyle Electronics
1325 E. 79th Street, Suite 1
Bloomington, MN 55425
Phone - 612-853-2280
Fax - 612-853-2298

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

OHIO

Representatives

MaxTech Marketing
10930 Johnnycake Ridge Road
Concord, OH 44077
Phone - 440-350-6230
Fax - 440-350-6231

MaxTech Marketing
4 Sycamore Creek Drive
Springboro, OH 45066
Phone - 724-775-4413
Fax - 724-775-4418

Distributors

Arrow Semiconductor Group
8200 Washington Village Drive, Suite A
Centerville, OH 45458-1877
Phone - 937-435-5563
Fax - 937-435-2049

Arrow Semiconductor Group
6573 E. Cochran Road
Solon, OH 44139-3916
Phone - 440-248-3990
Fax - 440-248-1106

Avnet, Inc.
30775 Bainbridge Road, Suite 130
Solon, OH 44139
Phone - 440-349-7601
Fax - 440-248-4803

Avnet, Inc.
777 Dearborn Park Lane, Suite L
Worthington, OH 43085
Phone - 614-888-3313
Fax - 614-888-0767

Marshall Industries
3520 Park Center Drive
Dayton, OH 45414
Phone - 937-898-4480
Fax - 937-898-9363

Marshall Industries
30700 Bainbridge Road, Unit A
Solon, OH 44139
Phone - 440-248-1788
Fax - 440-248-2312

Wyle Electronics
2055 Army Trail Road, Suite 140
Addison, IL 60101-1478
Phone - 630-620-0969
Fax - 630-620-1610

Wyle Electronics
3493 Newmark Drive
Miamisburg, OH 45342-5426
Phone - 937-436-9953
Fax - 937-436-1780

Wyle Electronics
Solon Business Park, Bldg. B
30600 Aurora Road, Suite 180
Solon, OH 44139-2761
Phone - 440-248-9996
Phone - 800-763-9953
Fax - 440-248-5490

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

OKLAHOMA

Sales Office

Micron Semiconductor Products, Inc.
One Chisholm Trail, Suite 3200
Round Rock, TX 78681
Phone - 512-248-5122
Fax - 512-248-5192

Distributors

Avnet, Inc.
12206 E. 51st Street, Suite 103
Tulsa, OK 74146
Phone - 918-459-6000
Fax - 918-459-6060

Wyle Electronics
1810 N. Greenville Avenue
Richardson, TX 75081-1876
Phone - 972-235-9953
Fax - 972-644-5064

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

OREGON

Sales Office

Micron Semiconductor Products, Inc.
1600 N.W. Compton Drive, Suite 206
Beaverton, OR 97006
Phone - 503-531-2010
Fax - 503-531-2011

Representative

Cascade Technical Sales
15455 N.W. Greenbrier Pky., Suite 244
Beaverton, OR 97006
Phone - 503-645-9660
Fax - 503-645-6363

Distributors

Arrow Semiconductor Group
9500 S.W. Nimbus Avenue, Bldg. E
Beaverton, OR 97008-7163
Phone - 503-629-8090
Fax - 503-645-0611

Avnet, Inc.
15580 S.W. Jay Street
Beaverton, OR 97006
Phone - 503-526-6200
Fax - 503-641-5939

Marshall Industries
9705 S.W. Gemini Drive
Beaverton, OR 97008
Phone - 503-644-5050
Fax - 503-646-8256

Wyle Electronics
10300 S.W. Nimbus, Bldg. B, #3
Portland, OR 97223-4345
Phone - 503-598-9953
Fax - 503-684-6620

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

PENNSYLVANIA - EASTERN

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

Delta Technical Sales, Inc.
122 North York Road, Suite 9
Hatboro, PA 19040
Phone - 215-957-0600
Fax - 215-957-0920

Distributors

Arrow Semiconductor Group
4 E. Stow Road, Unit 11
Marlton, NJ 08053-3152
Phone - 609-596-8000
Fax - 609-596-9632

Avnet, Inc.
7000 Atrium Way, Suite 6
Mt. Laurel, NJ 08054
Phone - 609-222-6400
Fax - 609-222-6464

Marshall Industries
158 Gaither Drive, #100
Mt. Laurel, NJ 08054
Phone - 609-234-9100
Fax - 609-778-1819

Wyle Electronics
815 East Gate Drive
Mt. Laurel, NJ 08054-1208
Phone - 800-871-9953
Fax - 609-439-9020

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

PENNSYLVANIA - WESTERN

Representative

MaxTech Marketing
1228 Lovi Road
Freedom, PA 15042
Phone - 724-775-4413
Fax - 724-775-4418

Distributors

Arrow Semiconductor Group
3245 Old Frankstown Road
Pittsburgh, PA 15239-2909
Phone - 412-327-1130
Fax - 412-327-4181

Avnet, Inc.
30775 Bainbridge Road, Suite 130
Solon, OH 44139
Phone - 440-349-7601
Fax - 440-248-4803

Wyle Electronics
Solon Business Park, Bldg. B
30600 Aurora Road, Suite 180
Solon, OH 44139-2761
Phone - 440-248-9996
Phone - 800-763-9953
Fax - 440-248-5490

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

PUERTO RICO

Sales Office

Micron Semiconductor Products, Inc.
One Cypresswood Building
9950 Cypresswood Drive, Suite 380
Houston, TX 77070
Phone - 281-970-3202
Fax - 281-970-3205

Representatives

Mega Technologies, Inc.
2510 Cypress Bend Drive East
Clearwater, FL 33761
Phone - 813-797-8222
Fax - 813-797-8375

Mega Technologies, Inc.
1600 Sarno Road, Suite 21
Melbourne, FL 32935
Phone - 407-752-6767
Fax - 407-752-7484

Distributors

Avnet, Inc.
3350 N.W. 53rd Street, Suite 105
Ft. Lauderdale, FL 33309
Phone - 954-484-5482
Fax - 954-484-4740

Wyle Electronics
Bldg. 1, Suite 101
700 W. Hillsboro Blvd.
Deerfield Beach, FL 33441
Phone - 954-420-0500
Fax - 954-428-2134

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

RHODE ISLAND

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

Advanced Tech Sales, Inc.
352 Park Street, Suite 102
North Reading, MA 01864
Phone - 978-664-0888
Fax - 978-664-5503

Distributors

Avnet, Inc.
10 M Centennial Drive
Peabody, MA 01960
Phone - 508-532-9893
Phone - 800-845-8416
Fax - 508-532-9713

Wyle Electronics
5 Oak Park Drive
Bedford, MA 01730-1413
Phone - 781-271-9953
Fax - 781-275-3809

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SOUTH CAROLINA

Sales Office

Micron Semiconductor Products, Inc.
One Cypresswood Building
9950 Cypresswood Drive, Suite 380
Houston, TX 77070
Phone - 281-970-3202
Fax - 281-970-3205

Distributors

Arrow Semiconductor Group
5240 Greens Dairy Road
Raleigh, NC 27616-4600
Phone - 919-876-3132
Fax - 919-878-9517

Avnet, Inc.
5234 Greens Dairy Road
Raleigh, NC 27604
Phone - 919-872-0712
Phone - 800-662-7947
Fax - 919-878-8729

Marshall Industries
5224 Greens Dairy Road
Raleigh, NC 27616
Phone - 919-878-9882
Fax - 919-872-2431

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SOUTH DAKOTA

Representative

High Technology Sales
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
Fax - 612-844-9930

Distributors

Avnet, Inc.
9401 James Avenue S., Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
Fax - 612-881-9461

Wyle Electronics
1325 E. 79th Street, Suite 1
Bloomington, MN 55425
Phone - 612-853-2280
Fax - 612-853-2298

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

TENNESSEE

Sales Office

Micron Semiconductor Products, Inc.
One Cypresswood Building
9950 Cypresswood Drive, Suite 380
Houston, TX 77070
Phone - 281-970-3202
Fax - 281-970-3205

Representative

Southeast Technical Group
101 Washington Street, Suite 6
Huntsville, AL 35801
Phone - 256-534-2376
Fax - 256-534-2384

Distributors

Avnet, Inc.
3475 Corporate Way, Suite D
Duluth, GA 30136
Phone - 770-623-4400
Fax - 770-476-8806

Wyle Electronics
7800 Governors Drive West
Huntsville, AL 35806-2057
Phone - 256-830-1119
Phone - 800-964-9953
Fax - 256-830-1520

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

TEXAS

Sales Office

Micron Semiconductor Products, Inc.
One Chisholm Trail, Suite 3200
Round Rock, TX 78681
Phone - 512-248-5122
Fax - 512-248-5192

Representative

Quatra Associates, Inc.
600 Autumnwood Place S.E.
Albuquerque, NM 87123
Phone - 505-296-6781
Fax - 505-292-2092

Distributors

Arrow Semiconductor Group
Braker Center III, Bldg. M1
11500 Metric Blvd., Suite 160
Austin, TX 78758-4079
Phone - 512-835-4180
Fax - 512-832-9875

Arrow Semiconductor Group
3220 Commander Drive
Carrollton, TX 75006-2585
Phone - 972-380-6464
Fax - 972-447-2211

Arrow Semiconductor Group
Westgate Center, Bldg. B
19416 Park Row, Suite 190
Houston, TX 77084-4860
Phone - 281-647-6868
Fax - 281-492-8722

Arrow Semiconductor Group
1000 Coit Road
Plano, TX 75075
Phone - 972-477-2090
Fax - 972-519-5195

Arrow Semiconductor Group
3400 Plano Parkway
Plano, TX 75075
Phone - 972-519-5528
Fax - 972-519-5195

Avnet, Inc.
12211 Technology Blvd.
Austin, TX 78727
Phone - 512-219-3700
Fax - 512-219-3737

Avnet, Inc.
3505 Boca Chica Blvd., Suite 201
Brownsville, TX 78521
Phone - 956-546-6411
Fax - 956-546-6419

Avnet, Inc.
11333 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
Fax - 214-553-4395

Avnet, Inc.
10500 Richmond Avenue, Suite 112
Houston, TX 77042
Phone - 713-781-6100
Fax - 713-953-8420

Marshall Industries
8504 Cross Park Drive
Austin, TX 78754
Phone - 512-837-1991
Fax - 512-832-9810

Marshall Industries
10681 Haddington Drive, #160
Houston, TX 77043
Phone - 713-467-1666
Fax - 713-467-9805

Marshall Industries
1551 N. Glenville Drive
Richardson, TX 75081
Phone - 972-705-0600
Fax - 972-705-0675

Wyle Electronics
9208 Waterford Center Blvd., Suite 150
Austin, TX 78758-7682
Phone - 512-833-9953
Fax - 512-873-0674

Wyle Electronics
2901 Wilcrest Drive, Suite 120
Houston, TX 77042-3359
Phone - 713-784-9953
Fax - 713-953-9953

Wyle Electronics
1810 N. Greenville Avenue
Richardson, TX 75081-1876
Phone - 972-235-9953
Fax - 972-644-5064

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

UTAH

Representative

Wescom Marketing
3500 S. Main Street, Suite 100
Salt Lake City, UT 84115
Phone - 801-269-0419
Fax - 801-269-0665

Distributors

Arrow Semiconductor Group
2440 South 1070 West, Suite A
Salt Lake City, UT 84119-1554
Phone - 801-973-8555
Fax - 801-973-8909

Avnet, Inc.
2855 E. Cottonwood Pkwy., Suite 220
Salt Lake City, UT 84121
Phone - 801-365-3800
Fax - 801-365-3821

Marshall Industries
2355 South 1070 West, Suite D
Salt Lake City, UT 84119
Phone - 801-973-2288
Fax - 801-973-2296

Wyle Electronics
170 W. Election Drive, Suite 100
Draper, UT 84020-9493
Phone - 801-523-2335
Fax - 801-523-8557

Wyle Electronics
1325 W. 2200 S., Suite E
West Valley City, UT 84119-1467
Phone - 801-974-9953
Fax - 801-972-2524

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

VERMONT

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

Advanced Tech Sales, Inc.
352 Park Street, Suite 102
North Reading, MA 01864
Phone - 978-664-0888
Fax - 978-664-5503

Distributors

Avnet, Inc.
10 M Centennial Drive
Peabody, MA 01960
Phone - 508-532-9893
Phone - 800-845-8416
Fax - 508-532-9713

Wyle Electronics
5 Oak Park Drive
Bedford, MA 01730-1413
Phone - 781-271-9953
Fax - 781-275-3809

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

VIRGINIA

Sales Office

Micron Semiconductor Products, Inc.
8A Franklin Street
Longblock Bldg.
Exeter, NH 03833
Phone - 603-772-2133
Fax - 603-772-3213

Representative

EES, Inc.
4302 Mountain Road, Suite B
Pasadena, MD 21122
Phone - 410-255-9686
Fax - 410-255-9688

Distributors

Avnet, Inc.
7134 Columbia Gateway Drive, Suite 100
Columbia, MD 21046
Phone - 410-988-9800
Phone - 800-638-5988
Fax - 410-720-3421

Wyle Electronics
7180 Columbia Gateway Drive, Suite 100
Columbia, MD 21046-2132
Phone - 410-312-4844
Phone - 800-863-9953
Fax - 410-312-4953

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

WASHINGTON

Sales Office

Micron Semiconductor Products, Inc.
1600 N.W. Compton Drive, Suite 206
Beaverton, OR 97006
Phone - 503-531-2010
Fax - 503-531-2011

Representative

Cascade Technical Sales
25 Central Way, #200
Kirkland, WA 98033
Phone - 425-822-7299
Fax - 425-822-7479

Distributors

Arrow Semiconductor Group
Bldg. B
3310 146th Place S.E., Suite A
Bellevue, WA 98007
Phone - 206-643-9992
Fax - 206-643-9709

Avnet, Inc.
8214 - 154th Avenue N.E.
Redmond, WA 98052
Phone - 206-882-7000
Phone - 800-548-3976
Fax - 206-882-7070

Marshall Industries
11715 N. Creek Pkwy. South, #112
Bothell, WA 98011
Phone - 425-486-5747
Fax - 425-486-6964

Wyle Electronics
15385 N.E. 90th Street
Redmond, WA 98052-3582
Phone - 425-881-1150
Phone - 800-248-9953
Fax - 425-881-1567

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

WEST VIRGINIA

Representative

MaxTech Marketing
4 Sycamore Creek Drive
Springboro, OH 45066
Phone - 724-775-4413
Fax - 724-775-4418

Distributors

Avnet, Inc.
7134 Columbia Gateway Drive, Suite 100
Columbia, MD 21046
Phone - 410-988-9800
Phone - 800-638-5988
Fax - 410-720-3421

Wyle Electronics
7180 Columbia Gateway Drive, Suite 100
Columbia, MD 21046-2132
Phone - 410-312-4844
Phone - 800-863-9953
Fax - 410-312-4953

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

WISCONSIN - EASTERN

Representatives

High Technology Sales
2525 South Shore Drive, #1D
Milwaukee, WI 53207
Phone - 414-769-7655
Fax - 414-769-7656

High Technology Sales
1111 Plaza Drive, Suite 102
Schaumburg, IL 60173
Phone - 847-517-7655
Fax - 847-517-7656

Distributors

Avnet, Inc.
W232, N296 Roundy Circle West, Suite 200
Pewaukee, WI 53072
Phone - 414-780-7200
Fax - 414-780-7201

Marshall Industries
Crossroads Corporate Center 1
20900 Swenson Drive, #150
Waukesha, WI 53186
Phone - 414-797-8400
Fax - 414-797-8270

Wyle Electronics
150 N. Patrick Blvd., Suite 150
Brookfield, WI 53045-5854
Phone - 414-879-0434
Phone - 800-867-9953
Fax - 414-879-0474

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

WISCONSIN - WESTERN

Representatives

High Technology Sales
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
Fax - 612-844-9930

High Technology Sales
2525 South Shore Drive, #1D
Milwaukee, WI 53207
Phone - 414-769-7655
Fax - 414-769-7656

Distributors

Avnet, Inc.
9401 James Avenue S., Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
Fax - 612-881-9461

Marshall Industries
Crossroads Corporate Center 1
20900 Swenson Drive, #150
Waukesha, WI 53186
Phone - 414-797-8400
Fax - 414-797-8270

Wyle Electronics
1325 E. 79th Street, Suite 1
Bloomington, MN 55425
Phone - 612-853-2280
Fax - 612-853-2298

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

WYOMING

Sales Office

Micron Semiconductor Products, Inc.
8000 S. Federal Way
P. O. Box 6
Boise, ID 83707-0006
Phone - 208-368-3900
Fax - 208-368-4617

Distributor

Wyle Electronics
1325 W. 2200 S., Suite E
West Valley City, UT 84119-1467
Phone - 801-974-9953
Fax - 801-972-2524

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ARGENTINA

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

AUSTRALIA

Distributor

Reptechnic Pty. Ltd.
3/36 Bydown Street
Neutral Bay, NSW 2089
Phone - 612-9953-9844
Fax - 612-9953-9683

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

AUSTRIA

Representative

Thomas Neuroth GmbH
Hitzinger Hauptstrasse 22
A-1130 Wien
Phone - 43-1-877-5645
Fax - 43-1-876-4920

Distributor

Avnet EMG GmbH
Waidhausenstrasse 19
A-1140 Wien
Phone - 43-1-911-2847
Fax - 43-1-911-3853

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

BALTIC STATES

Distributors

Avnet Baltronic AS
Maskavas Iela 40-42 - 513
LV-1018 Riga
Phone - 00371-7211109
Fax - 00371-7821118

Avnet Baltronic AS
Akadeemia tee 21F
EW-0026 Tallinn
Phone - 0037/26 39 70 00
Fax - 0037/26 39 70 09

Integrated Electronics Oy Ab
Ulvsundavagen 106 C
Box 11113
S-161 11 Bromma
Phone - 46-8-804-685
Fax - 46-8-262-286

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

BELGIUM

Representative

Microtron N.V.
Generaal De Wittelaan 7
B-2800 Mechelen
Phone - 32-15-292929
Fax - 32-15-292900

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

BELIZE

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

BOLIVIA

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

BRAZIL

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

CHILE

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

COLUMBIA

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

COSTA RICA

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

CZECH REPUBLIC

Representative

Thomas Neuroth GmbH
Hitzinger Hauptstrasse 22
A-1130 Wien
Phone - 43-1-877-5645
Fax - 43-1-876-4920

Distributor

Avnet E2000 setron
Slevacska 744/1
Hloibetin
CZ-19400 Praha 9
Phone - 0042/02/86 11 42
Fax - 0042/02/81 86 14 42

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

DENMARK

Distributors

Avnet Nortec AS
Transformervej 17
DK-2730 Herlev
Phone - 0045 / 44-88-0800
Fax - 0045 / 44-88-8088

Integrated Electronics Oy Ab
Ulvsundavagen 106 C
Box 11113
S-161 11 Bromma
Phone - 46-8-804-685
Fax - 46-8-262-286

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ECUADOR

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

EL SALVADOR

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

FINLAND

Distributors

Avnet Nortec Oy
Italahdenkatu 18 A
FIN-00210 Helsinki
Phone - 0035/80 61 31 81
Fax - 0035/80 69 22 326

Integrated Electronics Oy Ab
Laurinmaenkuja 3
FIN-00440 Helsinki
Phone - 358-0-586-1770
Fax - 358-9-253-54450

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

FRANCE

Representative

Rep'Tronic, S.A.
1 bis, rue Marcel Paul
Z.I. de la Bonde
91742 Massy Cedex
Phone - 33-160-139300
Fax - 33-160-139198

Distributors

Avnet EMG SA
79, Rue Pierre Semard
F-92322 Chatillon Cedex
Phone - 33-149-652500
Fax - 33-149-652630

CK Electronique
25, Boulvard Pre' Pommier
F-282000 Bourgoin J.
Phone - 33-167-4438-045
Fax - 33-167-4286-911

Paris SUD Electronique Composants
12, rue Rene Cassin
F-91742 Massy Cedex
Phone - 33-169-812020
Fax - 33-169-207532

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

FRENCH GUIANA

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

GERMANY

Sales and Customer Service Office

Micron Semiconductor (Deutschland) GmbH
Sternstrasse 20
D-85609 Aschheim
Phone - 49-89-904-8720
Fax - 49-89-904-87250

Distributors

Avnet EMG GmbH
Schmidtstrasse 49
D-60326 Frankfurt
Phone - 49-69-973804-0
Fax - 49-69-7380712

Avnet EMG GmbH
Max-Planck-Strasse 15 b
D-40699 Erkrath
Phone - 49-211-92003-0
Fax - 49-211-92003-99

Avnet EMG GmbH
Stahlgruberring 12
D-81829 Muenchen
Phone - 49-89-45110-0
Fax - 49-89-45110-210

Avnet EMG GmbH
Friedrich-Seele-Strasse 3a
D-38122 Braunschweig
Phone - 49-531-8098-112
Fax - 49-531-8098-134

Avnet EMG GmbH
Friedrich-Ebert-Damm 145
D-22047 Hamburg
Phone - 49-40-696952-0
Fax - 49-40-6962787

Avnet EMG GmbH
Kurfurstenstrasse 130
D-10785 Berlin
Phone - 49-30-214882-0
Fax - 49-30-2141728

Avnet EMG GmbH
Benzstrasse 1
70839 Gerlingen
Phone - 49-7156-439-0
Fax - 49-7156-439-111

MSC-Vertriebs GmbH
Konrad-Zuse-Strasse 5
07745 Jena/Goschwitz
Phone - 49-3641-607524
Fax - 49-3641-607581

MSC-Vertriebs GmbH
Pascalkehre 13
D-25451 Quickborn
Phone - 49-4106-7764-0
Fax - 49-4106-7764-88

MSC-Vertriebs GmbH
Industriestrasse 16
D-76297 Stutensee
Phone - 49-7249-910-0
Fax - 49-7249-7993

MSC-Vertriebs GmbH
Max-Plank-Strasse 5
D-85609 Dornach b. Aschheim
Phone - 49-89-94 55 32-0
Fax - 49-89-94 55 32-90

MSC-Vertriebs GmbH
Schraderstrasse 44
D-67227 Frankenthal
Phone - 49-6233-344-0
Fax - 49-6233-344-210

MSC-Vertriebs GmbH
Max-Planck-Strasse 5 c
D-40699 Erkrath
Phone - 49-211-92593-0
Fax - 49-211-92594-88

MSC-Vertriebs GmbH
Friedrich-Bergius-Strasse 9
D-65203 Wiesbaden-Erbenh.
Phone - 49-611-97320-0
Fax - 49-611-97320-88

MSC-Vertriebs GmbH
Sperberstrasse 47
D-90461 Nuernberg
Phone - 49-911-43970-0
Fax - 49-911-43970-30

SIMOS Elektronik Vertriebs GmbH
Hauptstrasse 16
D-70563 Stuttgart
Phone - 49-711-733723-25
Fax - 49-711-733026

SIMOS Elektronik Vertriebs GmbH
Ohmstrasse 12
D-85757 Karlsfeld b. Munchen
Phone - 49-8131-506250
Fax - 49-8131-506252

SIMOS Elektronik Vertriebs GmbH
Falkenstrasse 6
D-90602 Pyrbaum
Phone - 49-9180-1059
Fax - 49-9180-1493

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

GUATEMALA

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

GUYANA

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

HONDURAS

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

HONG KONG

Sales and Customer Service Office

Micron Semiconductor Asia, Pte. Ltd.
5 Upper Aljunied Link #06-06
Quartz Industrial Bldg.
Singapore 367903
Phone - 65-287-6006
Fax - 65-287-6556

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

HUNGARY

Representative

Thomas Neuroth GmbH
Hitzinger Hauptstrasse 22
A-1130 Wien
Phone - 43-1-877-5645
Fax - 43-1-876-4920

Distributor

setron Elektronika Kft.
Toboz u. 6
H-1037 Budapest
Phone - 361-2504618
Fax - 361-2507646

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

INDIA

Distributor

Silicon Electronics
1148 Sonora Court
Sunnyvale, CA 94086
Phone - 408-738-8235
Fax - 408-738-0698

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

INDONESIA

Distributor

Desner Electronics (FE) Pte Ltd
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 368086
Phone - 65-285-1566
Fax - 65-284-9466

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

IRELAND

Representative

New England Technical Sales
The Diamond
Malahide
Co. Dublin
Phone - 353-18-450635
Fax - 353-18-453625

Distributor

Avnet - Lyco
Chapel Lane
Swords
County Dublin
Phone - 0035/318 90 10 00
Fax - 0035/318 90 10 10

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ISRAEL

Distributor

C.R.G. Electronics Ltd.
Industrial Park, P.O. B. 590
Carmiel 20101
Phone - 972-49-887-877
Fax - 972-49-887-588

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ITALY

Representative

Acsis srl
via Alberto Mario, 26
I-20149 Milano
Phone - 39-248-022522
Fax - 39-0248-012289

Distributor

Avnet EMG SRL
Via Novara 570
I-20153 Milano
Phone - 0038/2/38 19 01
Fax - 0038/2/38 00 29 88

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

JAPAN

Field Sales Office

Micron Technology Japan, K.K.
4-30, Shiba Koen 3-chome
32 Mori Building, 8F, Minato-ku
Tokyo, Japan 105-0011
Phone - 81-3-3436-5666
Fax - 81-3-3436-1444

Representative

Dia Semicon Systems
Sumitomo Seimei Bldg. 6F, Yayoi 2-44
Kumagaya-Shi Saitama 360
Phone - 0485-22-3530
Fax - 0485-22-0052

Distributors

Inno Micro Corporation
2-13-13, Shinyokohama
Kouhoku-ku, Yokohama City
Kanagawa, 222
Phone - 81-045-476-7500
Fax - 81-045-476-7516

Macnica, Inc.
Hakusan High-Tech Park,
1-22-2 Hakusan, Midori-ku,
Yokohama City 226
Phone - 81-45-939-6140
Fax - 81-45-939-6141

Tokyo Musen Kizai Co., Ltd.
3-7, Sotokanda 2-chome
Chiyoda-ku, Tokyo 101-0021
Phone - 81-3-3253-0541
Fax - 81-3-3255-3217

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

KOREA

Representative

I&C Microsystems Co. Ltd.
801, 8F, Bethel Bldg.
324-1 Yangjae-Dong
Seocho-Ku, Seoul
Phone - 822-577-9131
Fax - 822-577-9130

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

LUXEMBOURG

Representative

Microtron N.V.
Generaal De Wittelaan 7
B-2800 Mechelen
Phone - 32-15-292929
Fax - 32-15-292900

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MALAYSIA

Distributor

Desner (Malaysia) Sdn. Bhd.
36 Jalan Gangsa SD 5/3C
Bandar Sri Damansara
52200 Kuala Lumpur
Phone - 60-03-6322323
Fax - 60-03-6342323

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MEXICO

Representative

LatinRep
San Uriel #608
Guadalajara Jalisco 45042
Phone - 523-6474250
Fax - 523-6473433

Distributor

Wyle Electronics
Prol. Americas 1612-6, Country Club
Guadalajara, Jalisco 44619
Phone - 52 3 6789 239
Fax - 52 3 6789 289

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEW ZEALAND

Distributor

Maxbyte Technologies
35 Kaihuia Street
P.O. Box 28-096
Wellington, 6001
Phone - 642-542-7799
Fax - 644-475-3856

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NICARAGUA

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NORWAY

Distributors

Avnet Nortec AS
Smedisvingen 4B
P.O. Box 274
N-1364 Hvalstad
Phone - 47-66 84 62 10
Fax - 47-66 84 65 45

Integrated Electronics Oy Ab
Ulvsundavagen 106 C
Box 11113
S-161 11 Bromma
Phone - 46-8-804-685
Fax - 46-8-262-286

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

PANAMA

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

PARAGUAY

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

PERU

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

PHILIPPINES

Distributor

Desner Electronics (FE) Pte Ltd
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 368086
Phone - 65-285-1566
Fax - 65-284-9466

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

POLAND

Representative

Thomas Neuroth GmbH
Hitzinger Hauptstrasse 22
A-1130 Wien
Phone - 43-1-877-5645
Fax - 43-1-876-4920

Distributor

Avnet E2000 setron
Ul. Port Wola 22
Biurowiec PZL Wola, pok. 15p.IX
PF-00961 Warszawa
Phone - 0048/022/634/47 36
Fax - 0048/022/634/47 38

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

RUSSIAN FEDERATION

Representative

Thomas Neuroth GmbH
Hitzinger Hauptstrasse 22
A-1130 Wien
Phone - 43-1-877-5645
Fax - 43-1-876-4920

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SINGAPORE

Sales and Customer Service Office

Micron Semiconductor Asia, Pte. Ltd.
5 Upper Aljunied Link #06-06
Quartz Industrial Bldg.
Singapore 367903
Phone - 65-287-6006
Fax - 65-287-6556

Distributor

Desner Electronics (FE) Pte Ltd
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 368086
Phone - 65-285-1566
Fax - 65-284-9466

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SLOVENIA

Representative

Thomas Neuroth GmbH
Hitzinger Hauptstrasse 22
A-1130 Wien
Phone - 43-1-877-5645
Fax - 43-1-876-4920

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SOUTH AFRICA

Distributor

Computer Parts (Pty) LTD
CNR Athol and Louis Botha Avenues
Highlands North
Johannesburg 2037
Phone - 27-11-887-2438
Fax - 27-11-887-2514

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SURINAME

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SWEDEN

Distributors

Avnet Nortec AB
P.O. Box 1392
Englundavagen 7
S-171 27 Solna
Phone - 46-8-629-1400
Fax - 46-8-627-5156

Integrated Electronics Oy Ab
Ulvsundavagen 106 C
Box 11113
S-161 11 Bromma
Phone - 46-8-804-685
Fax - 46-8-262-286

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SWITZERLAND

Distributor

Avnet EMG GmbH
Boehnirainstrasse 11
CH-8801 Tahlwil
Phone - (0041) 1 7221330
Fax - (0041) 1 7221340

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

TAIWAN R.O.C.

Sales and Customer Service Office

Micron Technology Asia Pacific, Inc.
Suite 1010, 10th Floor
333 Keelung Road, Sec 1
Taipei, 110
Phone - 886-2-2757-6622
Fax - 886-2-2757-6656

Distributor

ASEC International
4F, 223, Chung Yang Road
Nan Kang District
Taipei
Phone - 886-2-786-6677
Fax - 886-2-651-0600

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

THE NETHERLANDS

Representative

Microtron N.V.
Beneluxweg 37
Postbus 4336
NL-4904 SJ Oosterhout
Phone - 31-162-060-308
Fax - 31-162-060-633

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

UNITED KINGDOM

Sales and Customer Service Office

Micron Europe Limited
Micron House, Wellington Business Park
Dukes Ride, Crowthorne
Berkshire RG45 6LS
Phone - 44-1344-750750
Fax - 44-1344-750710

Distributors

Avnet Access Ltd.
Avnet House
Rutherford Close, Meadway
Stevenage, Hertfordshire SG1 2EF
Phone - 44-1438-788500
Fax - 44-1438-788270

MACRO GROUP

Burnham Lane
Slough, Berkshire SL1 6LN
Phone - 44-1628-604383
Fax - 44-1628-666873

MSC-Vertriebs GmbH
Pavillion House, 6/7 Old Steine
Brighton Sussex BN1 1CJ
Phone - 44-1273-622446
Fax - 44-1273-622533

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

URUGUAY

Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

VENEZUELA

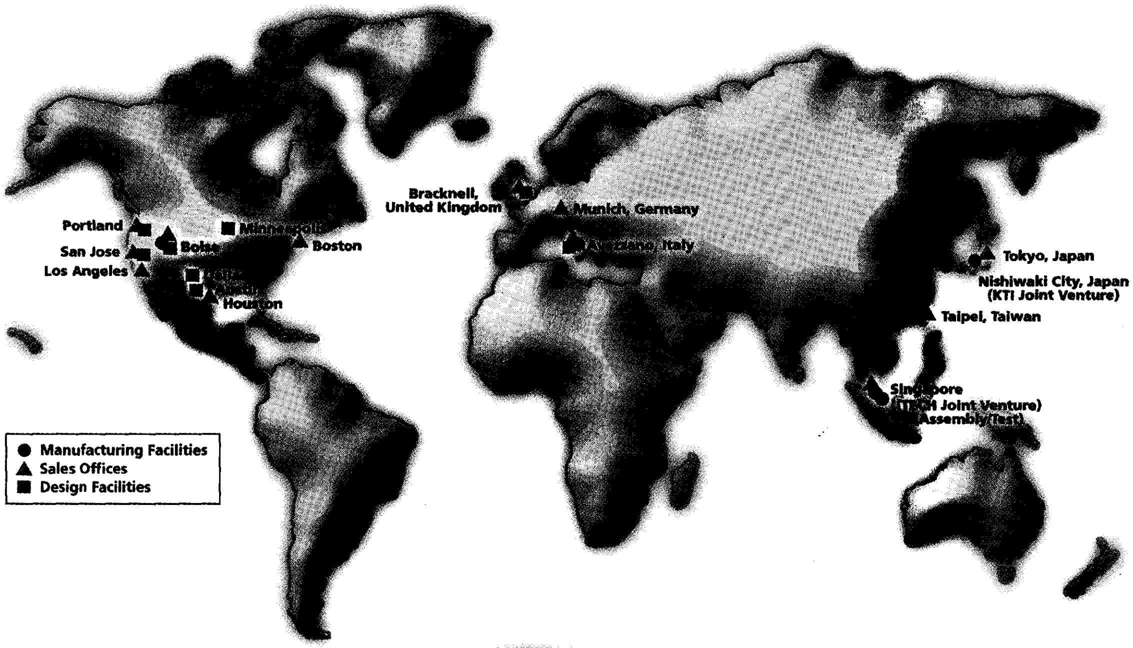
Distributor

CHS, Inc.
2804 N.W. 72nd Avenue
Miami, FL 33122
Phone - 305-594-4756
Fax - 305-592-5513

Die Distributor

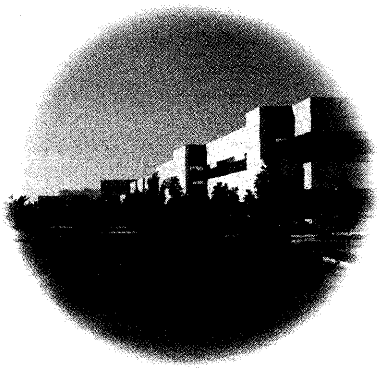
Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

WORLDWIDE LOCATION



MICRON TECHNOLOGY, INC. HEADQUARTERS

8000 S. Federal Way
P.O. Box 6
Boise, Idaho 83707-0006
Tel: 208-368-3900
Fax: 208-368-4617
Internet: www.micron.com/mti
E-mail: prodmktg@micron.com
Customer Comment Line:
800-932-4992
Fax 01-208-368-5018



www.micron.com/mti

MANUFACTURING SITES

Boise, Idaho
Avezzano, Italy
Singapore (Assembly/Test)
Nishiwaki City, Japan (Joint Venture)
Singapore (Joint Venture)

DESIGN FACILITIES

Boise, Idaho
San Jose, California
Minneapolis, Minnesota
Portland, Oregon
Austin, Texas
Dallas, Texas
Avezzano, Italy
Bracknell, United Kingdom

U.S. SALES OFFICES

Boise, Idaho
Los Angeles, California
San Jose, California
Boston, Massachusetts
Portland, Oregon
Houston, Texas

INTERNATIONAL SALES OFFICES

Munich, Germany
Avezzano, Italy
Tokyo, Japan
Singapore
Taipei, Taiwan
Bracknell, United Kingdom

Rev. 2/99
Printed in the USA