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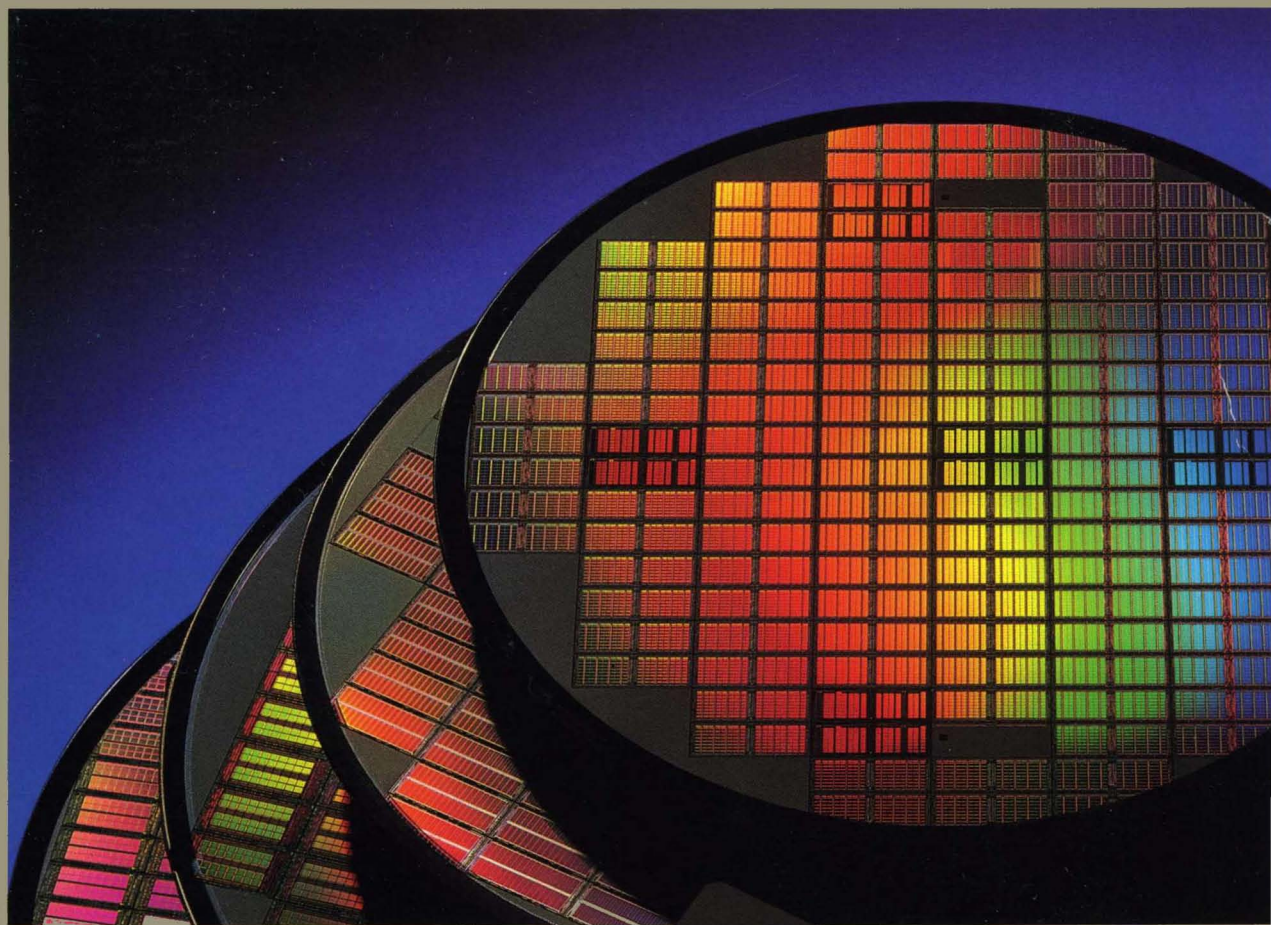
MOS DATA BOOK

1991

MOS DATA BOOK



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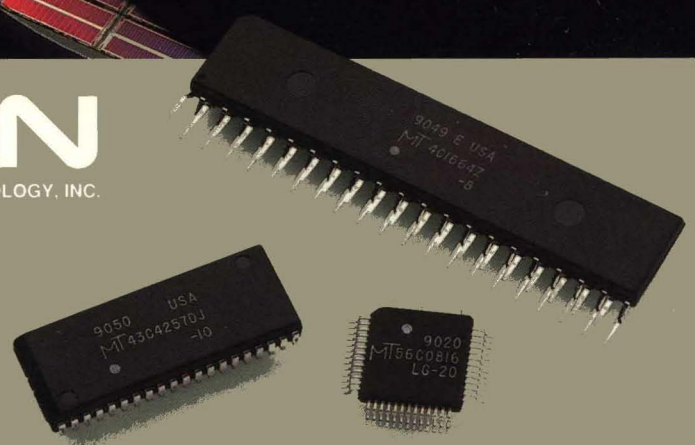

MICRON TECHNOLOGY, INC.

MICRON
TECHNOLOGY, INC.

MOS DATA BOOK

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The MOS Data Book has been organized into 11 sections and includes complete detailed specifications on our growing, high-performance CMOS and NMOS product line.

Sections 1 through 8 cover individual product families. Each section contains a product selection guide followed by data sheets. Three different types of data sheets are used: Advance Information, which contains initial descriptions of products still under development; Preliminary Information, which contains initial device characterization limits that are subject to change upon full characterization of production devices; and Final Information, which contains minimum and maximum limits specified over the complete power supply and temperature range for production devices.

Section 9 contains application and technical information.

Section 10 contains selected information about Micron's growing Defense Electronics product offering.

Section 11 contains packaging information.

Section 12 contains ordering information, product quality and reliability information and a list of sales representatives and distributors by geographical location for the North American Continent, Europe and Asia.

Additional or updated information on any Micron product is available from:

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DYNAMIC RAMS

PAGE

Product Selection Guide

PM	PAGE MODE	**QCP**	QUAD CAS PARITY
FPM	FAST PAGE MODE	**WPB**	WRITE-PER-BIT
SC	STATIC COLUMN	**DW**	DUAL WE
LP	LOW POWER	**DC**	DUAL CAS

DRAM MODULES

MULTIPORT DYNAMIC RAMS

MICRON TECHNOLOGY, INC.

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STATIC RAMS

CE ..... CHIP ENABLE
OE ..... WITH OUTPUT ENABLE
OT ..... OUTPUTS TRACK INPUTS DURING WRITE
SI/O ..... SEPARATE DATA INPUTS AND OUTPUTS
HZ ..... HIGH IMPEDANCE OUTPUTS DURING WRITE

SYNCHRONOUS SRAMS

SR ..... SYNCHRONOUS READS
STW ..... SELF-TIMED WRITES

SRAM MODULES

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MILITARY INFORMATION

PACKAGE INFORMATION

SALES INFORMATION

NUMERICAL INDEX

Part # PAGE

NUMERICAL INDEX (Continued)

NUMERICAL INDEX (Continued)

MICRON TECHNOLOGY, INC.

DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package and Number of Pins						Process	Page
				Standby	Active	PDIP	ZIP	PLCC	SOJ	CDIP	TSOP		
64K x 1	PM	MT4264	100, 120, 150	15mW	75mW	16	-	-	-	16	-	NMOS	1-1
256K x 1	PM	MT1259	100, 120, 150	15mW	150mW	16	16	18	-	16	-	NMOS	1-9
1 Meg x 1	FPM	MT4C1024	70, 80 ,100	3mW	175mW	18	20	-	20	18	*	CMOS	1-19
1 Meg x 1	SC	MT4C1026	70, 80, 100	3mW	175mW	18	20	-	20	18	*	CMOS	1-31
1 Meg x 1	FPM, LP	MT4C1027	70, 80, 100	1mW	150mW	18	20	-	20	18	*	CMOS	1-43
4 Meg x 1	FPM	MT4C1004	60, 70, 80	3mW	225mW	-	20	-	20	18	*	CMOS	1-55
4 Meg x 1	SC	MT4C1006	60, 70, 80	3mW	225mW	-	20	-	20	18	*	CMOS	1-67
16 Meg x 1	FPM	MT4C10016	50, 60, 70, 80	3mW	250mW	-	24	-	24	*	*	CMOS	1-79
16 Meg x 1	SC	MT4C10017	50, 60 ,70, 80	3mW	250mW	-	24	-	24	*	*	CMOS	1-79
64K x 4	PM	MT4067	100, 120, 150	15mW	150mW	18	20	18	-	18	-	NMOS	1-81
256K x 4	FPM	MT4C4256	70, 80, 100	3mW	175mW	20	20	-	20	20	*	CMOS	1-91
256K x 4	SC	MT4C4258	70, 80, 100	3mW	175mW	20	20	-	20	20	*	CMOS	1-103
256K x 4	FPM, QCP	MT4C4259	70, 80, 100	3mW	175mW	20	20	-	20	20	*	CMOS	1-115
256K x 4	FPM, LP	MT4C4260	70, 80, 100	1mW	150mW	20	20	-	20	20	*	CMOS	1-129
1 Meg x 4	FPM	MT4C4001	60, 70, 80	3mW	225mW	-	20	-	20	20	*	CMOS	1-141
1 Meg x 4	SC	MT4C4003	60, 70, 80	3mW	225mW	-	20	-	20	20	*	CMOS	1-153
1 Meg x 4	FPM, QCP	MT4C4004	60, 70, 80	3mW	225mW	-	20	-	20	20	*	CMOS	1-165
1 Meg x 4	FPM, WPB	MT4C4005	60, 70, 80	3mW	225mW	-	20	-	20	20	*	CMOS	1-179
4 Meg x 4	FPM	MT4C40004	50, 60, 70, 80	3mW	250mW	-	20	-	20	20	*	CMOS	1-191
4 Meg x 4	SC	MT4C40005	50, 60, 70, 80	3mW	250mW	-	24	-	24	*	*	CMOS	1-191
512K x 8	FPM	MT4C8512	70, 80, 100	3mW	350mW	-	-	-	24	*	*	CMOS	1-193
512K x 8	FPM, WPB	MT4C8513	70, 80, 100	3mW	350mW	-	-	-	28	-	*	CMOS	1-193
64K x 16	FPM, DW	MT4C1664	70, 80, 100	3mW	225mW	-	40	-	40	-	*	CMOS	1-207
64K x 16	FPM, WPB	MT4C1665	70, 80, 100	3mW	225mW	-	40	-	40	-	*	CMOS	1-207
64K x 16	FPM, LP, DW	MT4C1668	70, 80, 100	2mW	200mW	-	40	-	40	-	*	CMOS	1-223
64K x 16	FPM, LP, WPB	MT4C1669	70, 80, 100	2mW	200mW	-	40	-	40	-	*	CMOS	1-223
64K x 16	SC, DW	MT4C1670	70, 80, 100	3mW	225mW	-	40	-	40	-	*	CMOS	1-239
64K x 16	SC, WPB	MT4C1671	70, 80, 100	3mW	225mW	-	40	-	40	-	*	CMOS	1-239
64K x 16	FPM, DC	MT4C1672	70, 80, 100	3mW	350mW	-	40	-	40	-	*	CMOS	1-257
256K x 16	FPM, DW	MT4C16256	70, 80, 100	3mW	350mW	-	*	-	40	-	*	CMOS	1-259
256K x 16	FPM, DW, WPB	MT4C16257	70, 80, 100	3mW	350mW	-	*	-	40	-	*	CMOS	1-259
256K x 16	FPM, DC	MT4C16258	70, 80, 100	3mW	350mW	-	*	-	40	-	*	CMOS	1-259
256K x 16	FPM, DC, WPB	MT4C16259	70, 80, 100	3mW	350mW	-	*	-	40	-	*	CMOS	1-259

PM = Page Mode, FPM = Fast Page Mode, SC = Static Column, LP = Low Power, QCP = Quad CAS Parity, WPB = Write Per Bit, DW = Dual WE, DC = Dual CAS
*Consult factory on availability of TSOP packages

MICRON TECHNOLOGY, INC.

DRAM

64K x 1 DRAM

PAGE MODE

FEATURES

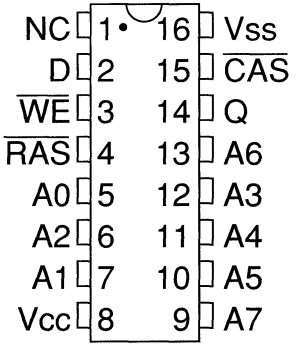
- Industry standard pinout, functions and timing
- Single +5V ±10% power supply
- Low power, 15mW standby; 75mW active, typical
- Common I/O using EARLY-WRITE
- Q held indefinitely by $\overline{CAS}$
- 256-cycle refresh in 4ms
- Fully compatible with MT1259 (256K)
- Optional PAGE MODE access cycle

OPTIONS

OPTIONS	MARKING
• Timing	
100ns access	-10
120ns access	-12
150ns access	-15
200ns access	-20
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

16-Pin DIP
(A-1, B-1)



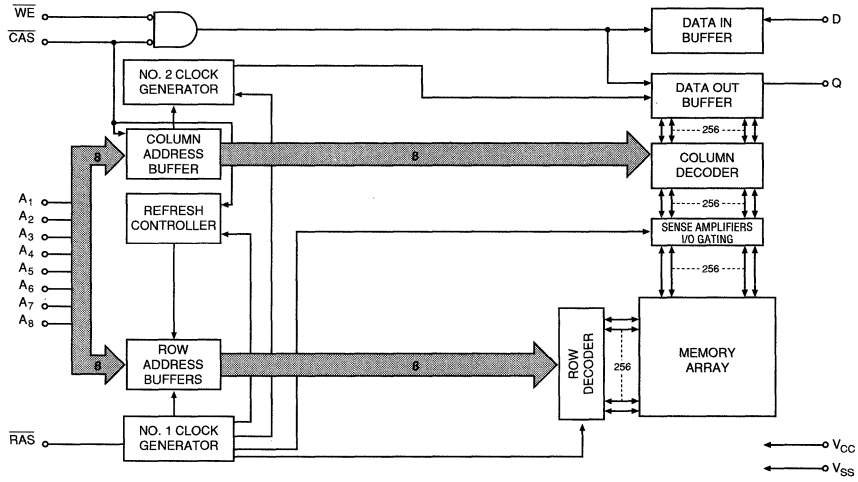
GENERAL DESCRIPTION

The MT4264 is a randomly accessed solid-state memory containing 65,536 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 16 address bits, which are entered 8 bits (A0-A7) at a time. $\overline{RAS}$ is used to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY or HIDDEN REFRESH) so that all 256 combinations of $\overline{RAS}$ addresses (A0-A7) are executed at least every 4ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses		
				t_R	t_C	
Standby	H	X	X	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In
$\overline{RAS}$-ONLY REFRESH	L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 4, 6) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}); I all other pins not under test = 0V	I_I	-10	10	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled; 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}		4	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ Cycling)	I_{CC2}		30	mA	2
$\overline{RAS}$-ONLY REFRESH CURRENT ($\overline{CAS}$ = V_{IH})	I_{CC3}		20	mA	2
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling)	I_{CC4}		30	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7, D	C_{I1}		5	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		8	pF	18
Output Capacitance: Q	C_O		8	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

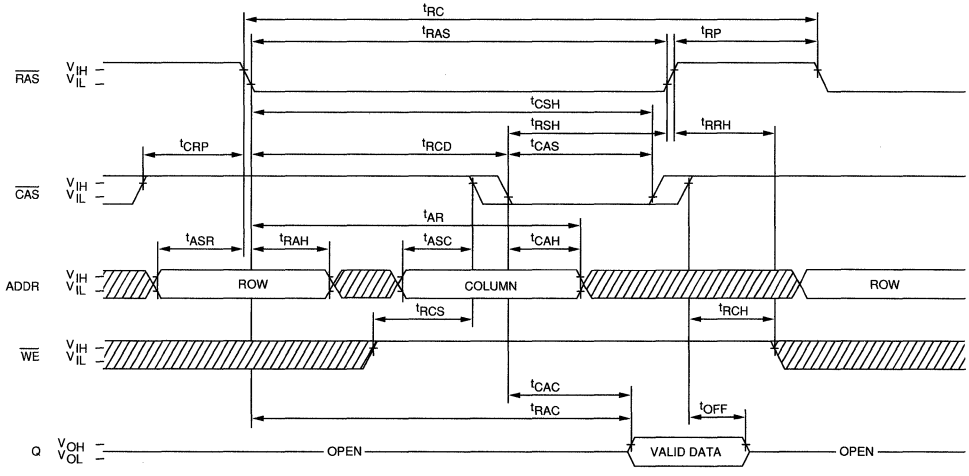
(Notes: 3, 4, 5, 10, 11, 17, 18) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-10		-12		-15		-20			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	195		230		260		330		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	220		255		295		370		ns	
PAGE-MODE cycle time	^tPC	90		100		120		170		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		100		120		150		200	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		50		60		75		120	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	50		60		75		100		ns	
$\overline{RAS}$ precharge time	^tRP	80	20,000	90	20,000	100	20,000	120	20,000	ns	
$\overline{CAS}$ pulse width	^tCAS	50	10,000	60	10,000	75	10,000	120	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		200		ns	
$\overline{CAS}$ precharge time	^tCPN	25		25		30		35		ns	19
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	30		30		35		40		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	25	50	25	60	25	75	30	80	ns	13
Row address setup time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		20		25		ns	
Column address setup time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	20		20		25		50		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	70		80		100		130		ns	
READ command setup time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	30	0	30	0	35	0	40	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	35		40		45		60		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	85		100		120		140		ns	
WRITE command pulse width	^tWP	35		40		45		50		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		40		45		55		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		40		45		55		ns	
Data-in setup time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	35		40		45		55		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	85		100		120		135		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	40		50		60		100		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	90		110		135		180		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh period (256 cycles)	^tREF		4		4		4		4	ms	
$\overline{CAS}$ to $\overline{RAS}$ setup time	^tCRP	10		15		20		20		ns	

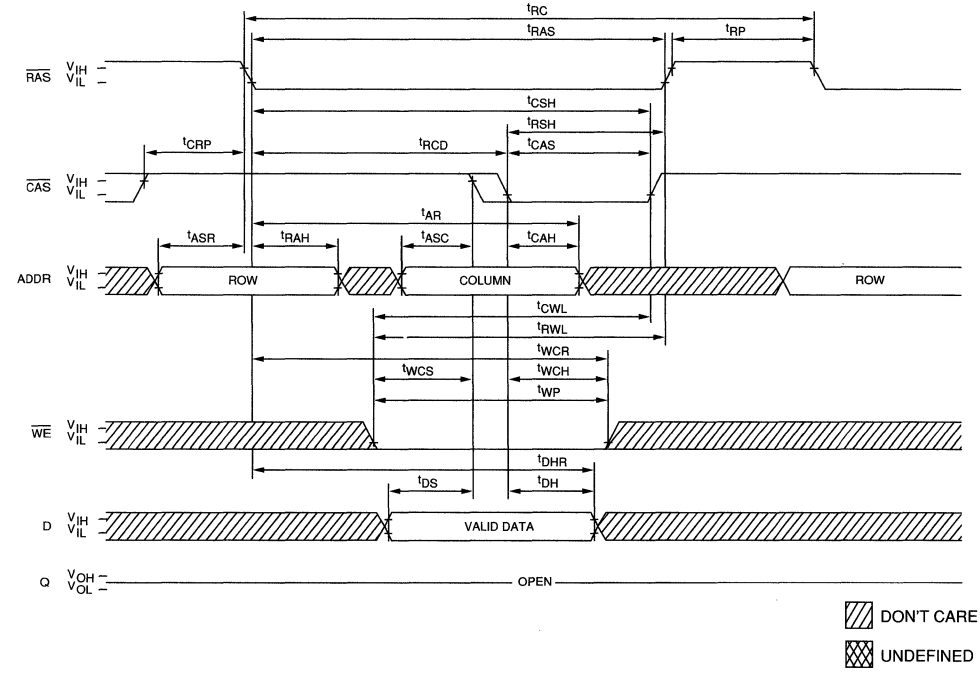
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS} = V_{IH}$, data output is high impedance.
11. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
16. ^tWCS, ^tRWD and ^tCWD are restrictive operating parameters in late READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge ^tCWD$ (MIN) and $^tRWD \ge ^tRWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. This parameter is sampled. Capacitance is calculated from the equation $C = I\,^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.

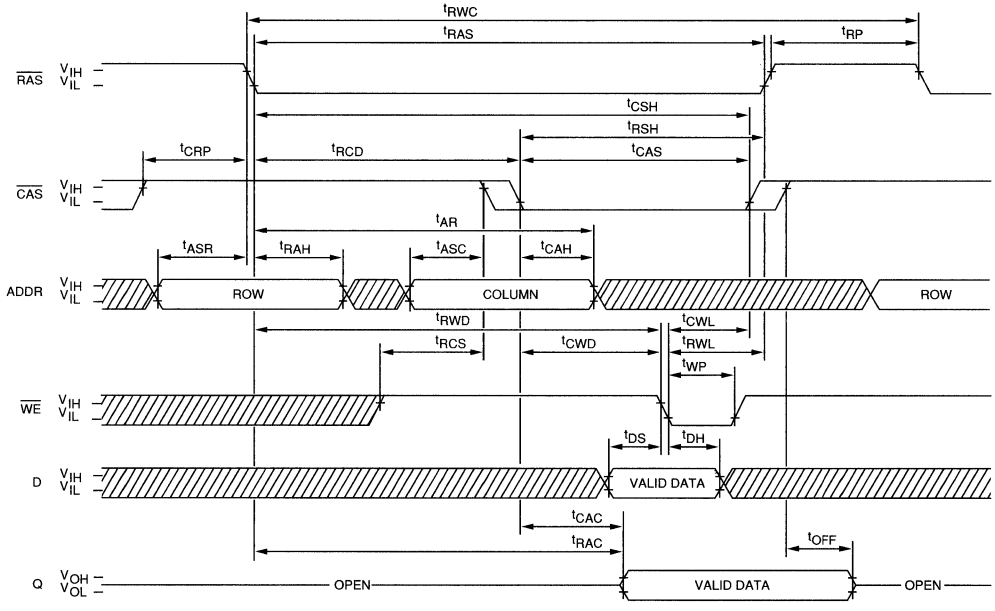
READ CYCLE



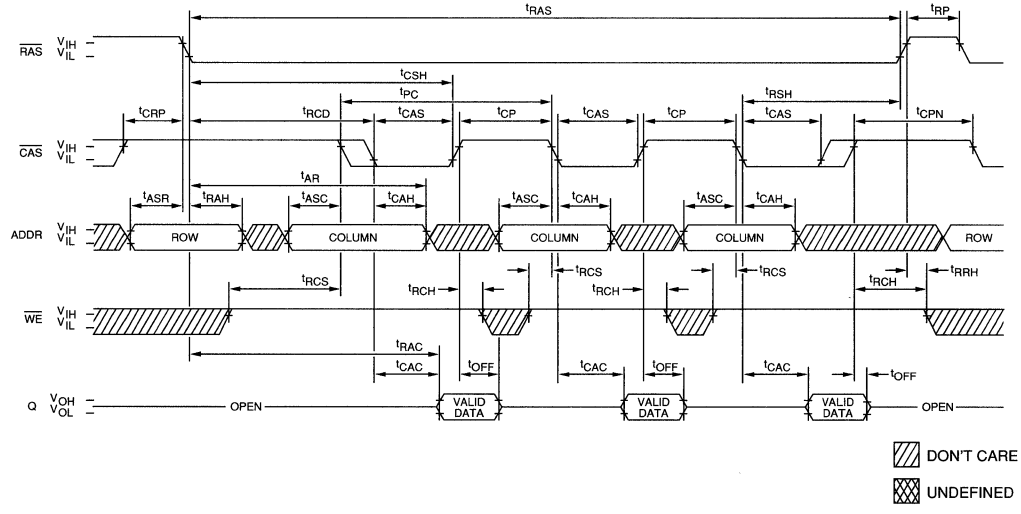
EARLY-WRITE CYCLE



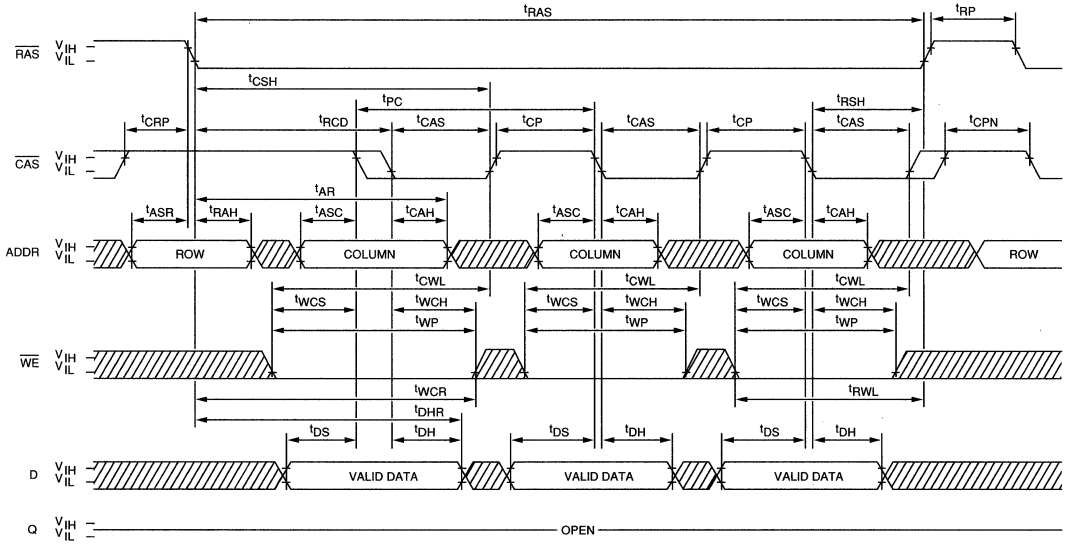
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

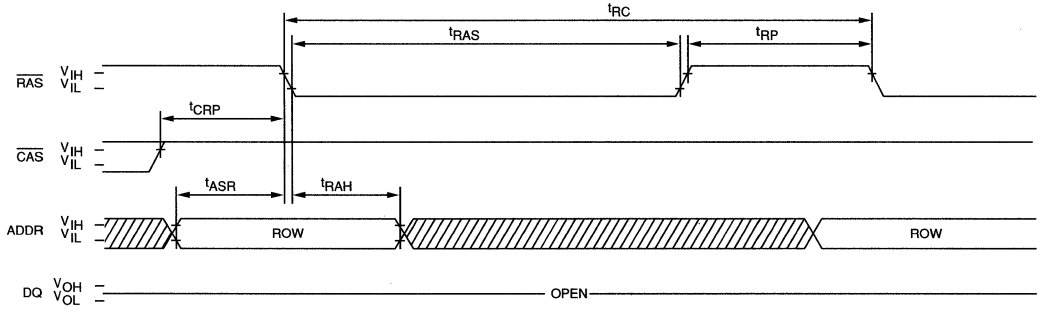


PAGE-MODE EARLY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE

(ADDR = A_0 - A_7)



DON'T CARE

UNDEFINED

DRAM

256K x 1 DRAM

PAGE MODE

FEATURES

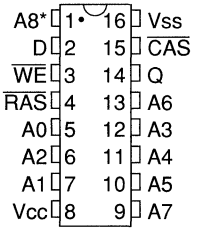
- Industry standard pinout, timing and functions
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby; 150mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256-cycle refresh in 4ms
- Optional PAGE MODE access cycle

OPTIONS

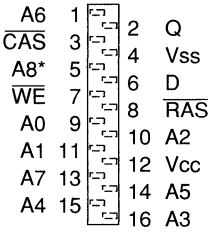
	MARKING
• Timing	
100ns access	-10
120ns access	-12
150ns access	-15
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
PLCC	EJ

PIN ASSIGNMENT (Top View)

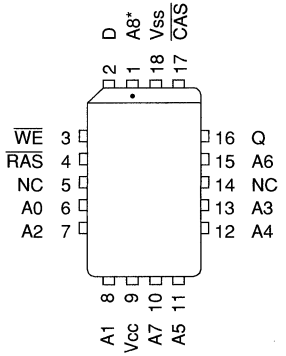
16-Pin DIP
(A-1, B-1)



16-Pin ZIP
(C-1)



18-Pin PLCC
(D-1)



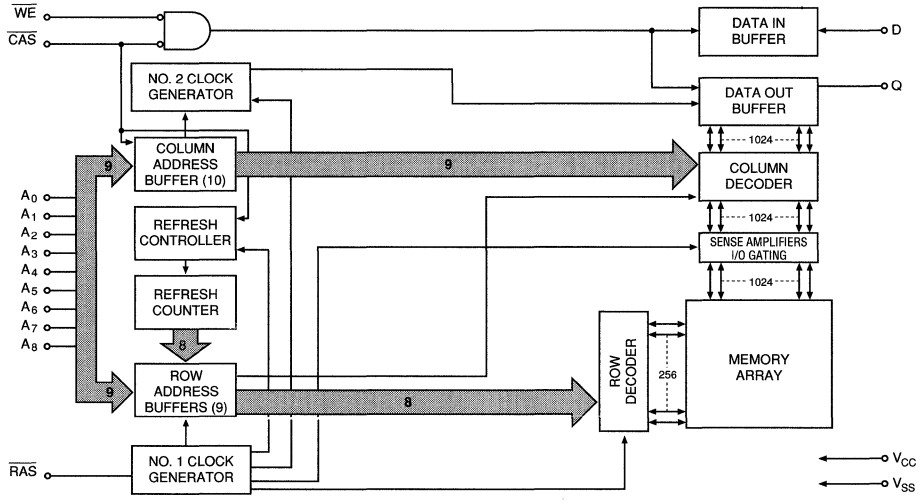
*Address not used for $\overline{RAS}$-ONLY refresh

GENERAL DESCRIPTION

The MT1259 is a randomly accessed solid-state memory containing 262,144 bits organized in a x1 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, the output pin is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-MODIFY-WRITE cycle. Data-in (D) is latched when $\overline{WE}$ strobes LOW.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ, WRITE, LATE-WRITE or READ-MODIFY-WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



TRUTH TABLE

Function	RAS	CAS	WE	Addresses		
				tR	tC	
Standby	H	X	X	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In
RAS-ONLY REFRESH	L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 4, 6) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0V	I_I	-10	10	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	5	5	5	mA	
OPERATING CURRENT: Random READ/WRITE ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC2}	55	55	45	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC3}	55	55	45	mA	2
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH}; ^tRC = ^tRC (MIN))	I_{CC4}	40	40	35	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC5}	55	55	45	mA	2, 20

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8, D	C_{I1}		5	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		8	pF	18
Output Capacitance: Q	C_O		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

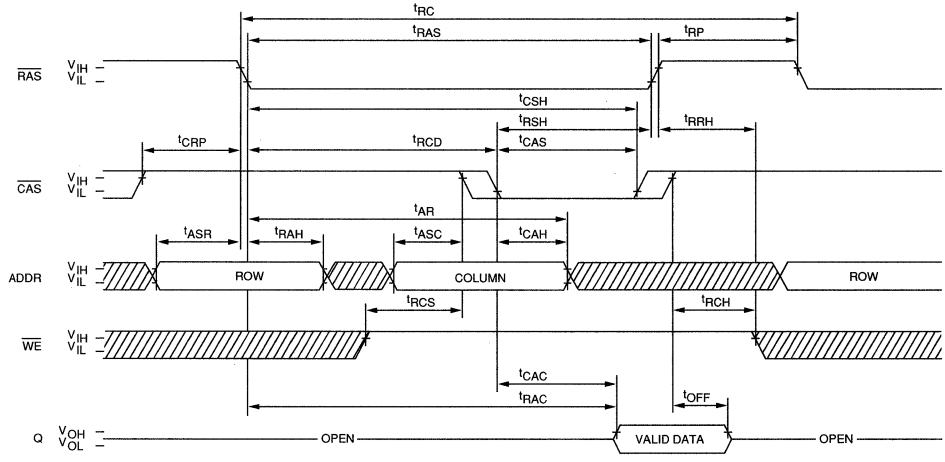
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	tRWC	220		255		295		ns	
PAGE-MODE cycle time	tPC	90		100		120		ns	6, 7
Access time from $\overline{RAS}$	tRAC		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	tCAC		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	tRSH	50		60		75		ns	
$\overline{RAS}$ precharge time	tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	tCAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	tCPN	25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE MODE)	tCP	30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	tCRP	15		20		20		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	15		15		15		ns	
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	70		80		100		ns	
READ command setup time	tRCS	0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	30	0	30	0	35	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	1
WRITE command hold time	tWCH	35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	tWCR	85		100		120		ns	
WRITE command pulse width	tWP	35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	tRWL	35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	tCWL	35		40		45		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	tDHR	85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	tCWD	40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	tRWD	90		110		135		ns	16
Transition time (rise or fall)	tT	3	100	3	100	3	100	ns	5, 17
Refresh period (256 cycles)	tREF		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	20		25		30		ns	20
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	tCSR	15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	20

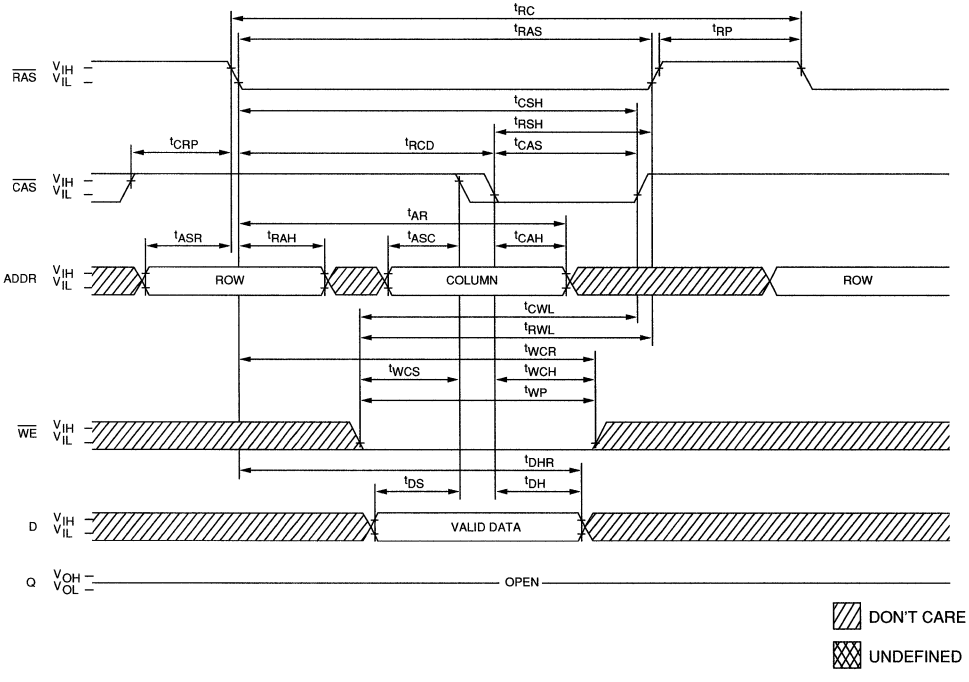
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge ^tCWD$ (MIN) and $^tRWD \ge ^tRWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. This parameter is sampled. Capacitance is calculated from the equation $C = I\,^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.

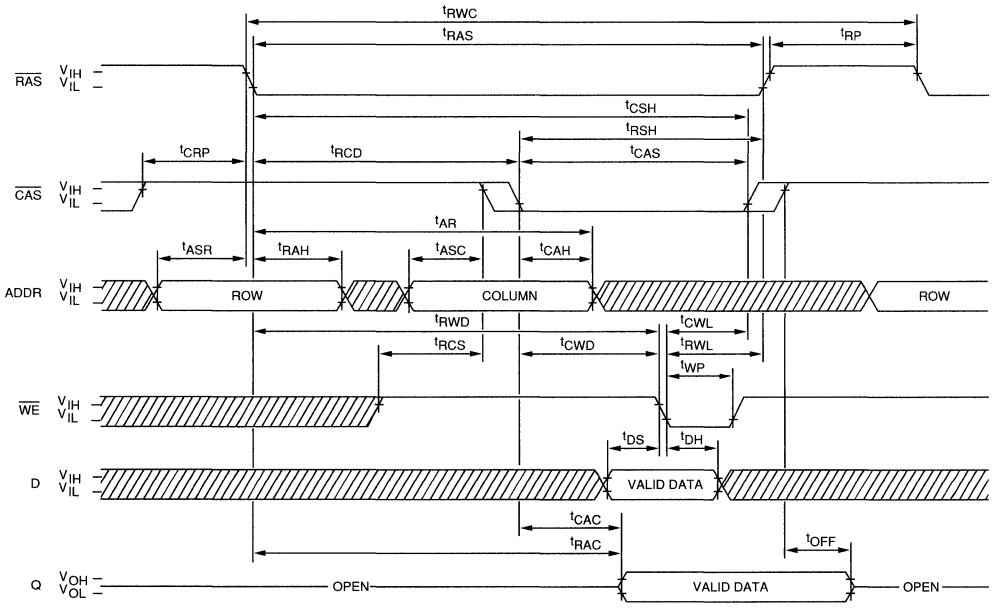
READ CYCLE



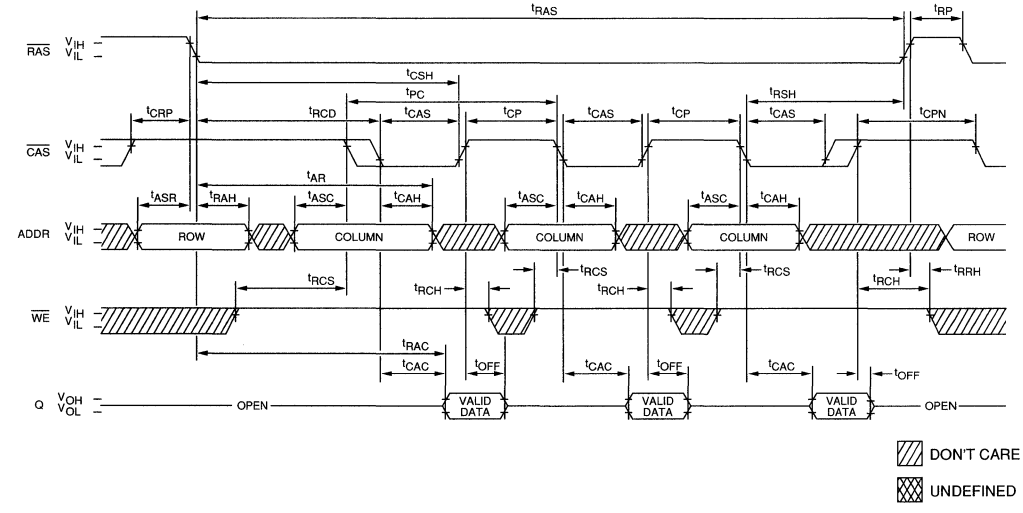
EARLY-WRITE CYCLE



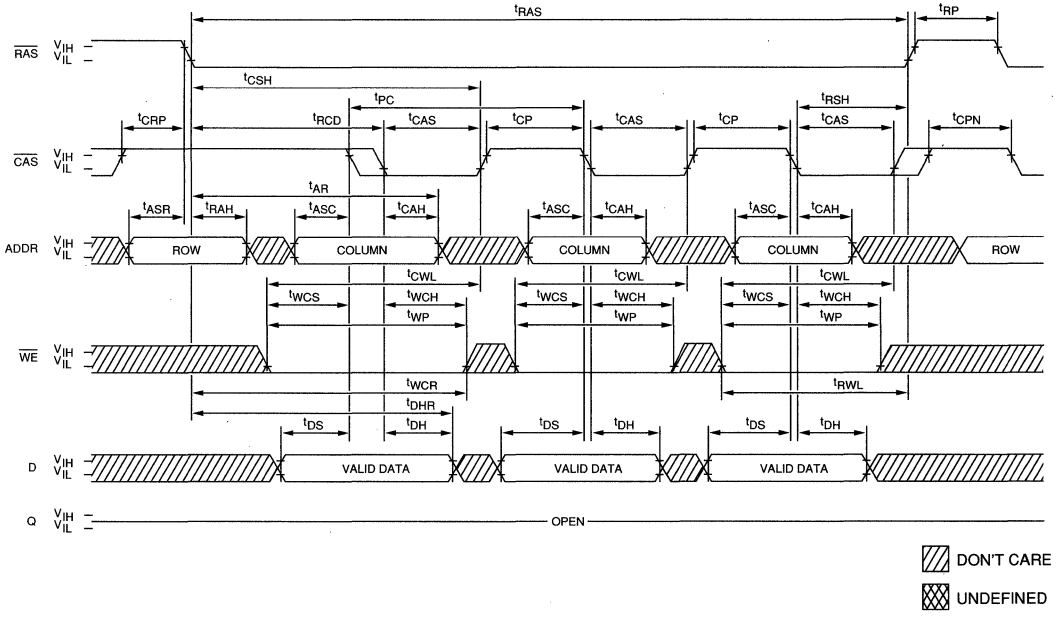
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

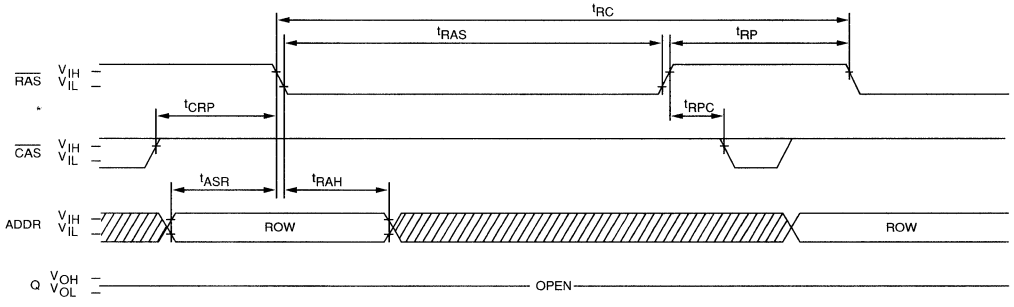


PAGE-MODE EARLY-WRITE CYCLE



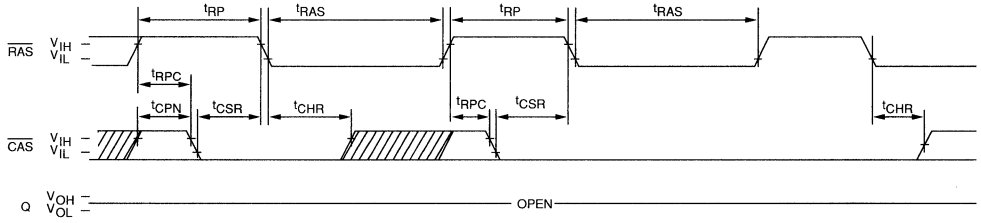
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{\text{WE}}$ = DON'T CARE)



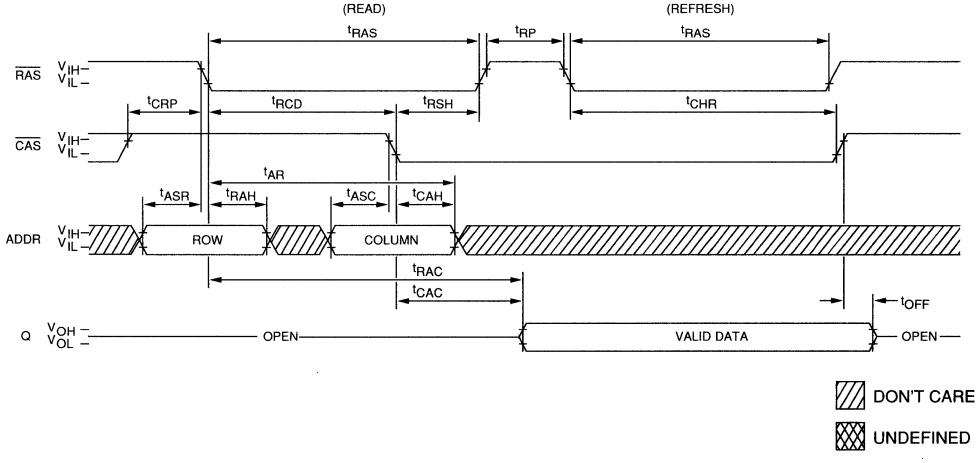
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE

(A_0 - A_8 and $\overline{\text{WE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{\text{WE}}$ = HIGH) [21]



DRAM

1 MEG x 1 DRAM

FAST PAGE MODE

FEATURES

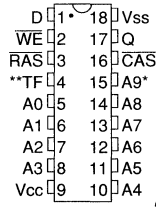
- Industry standard x1 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512-cycle refresh in 8ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional FAST PAGE MODE access cycle

OPTIONS

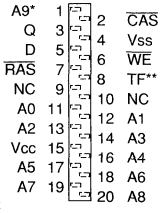
	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Plastic DIP (300mil)	None
Ceramic DIP (300mil)	C
Plastic ZIP (350mil)	Z
Plastic SOJ (300mil)	DJ
Plastic TSOP (***)	VG
• Operating Temperature, T_A	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

PIN ASSIGNMENT (Top View)

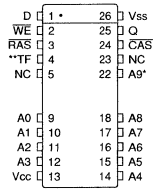
18-Pin DIP
(A-3, B-2)



20-Pin ZIP
(C-2)



20-Pin SOJ
(E-1)



*Address not used for $\overline{RAS}$-ONLY refresh
**TF = Test Function, V_{IN} must not exceed Vcc+1V for normal operation
***Consult factory on availability of TSOP packages

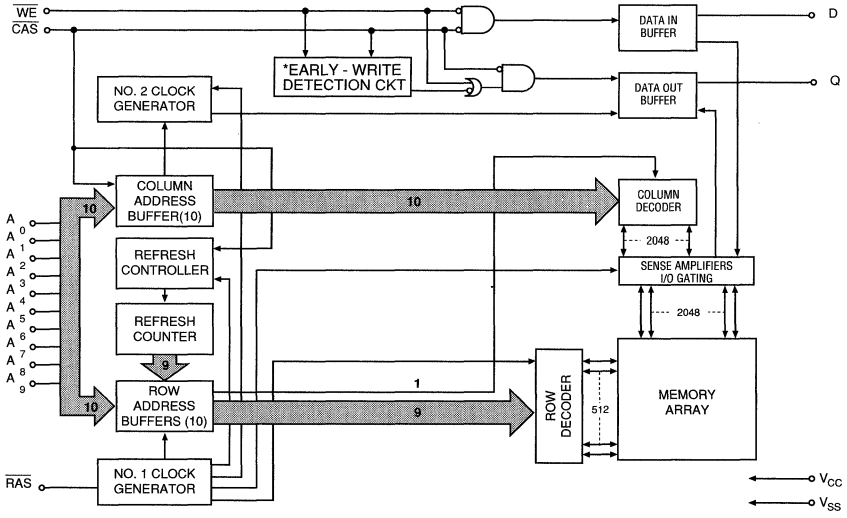
GENERAL DESCRIPTION

The MT4C1024 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin, data out (Q), remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh will increment the refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection CKT output is a HIGH (EARLY WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address		DATA	
					^tR	^tC	D (Data In)	Q (Data Out)
Standby		H	X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Valid Data In	Valid Data Out
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Don't Care	Valid Data Out
	2nd Cycle	L	H→L	H	n/a	COL	Don't Care	Valid Data Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Valid Data In	High-Z
	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In	High-Z
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Valid Data In	Valid Data Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Valid Data In	Valid Data Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Don't Care	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In	High-Z
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -55°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 600mW
Soldering Temperature (soldering 10 sec) ..... 260°C
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-2.0	0.8	V	1, 25
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	80	70	60	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	60	50	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	80	70	60	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	80	70	60	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	155		175		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		45		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	65		70		85		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Access time from column address	t_{AA}		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

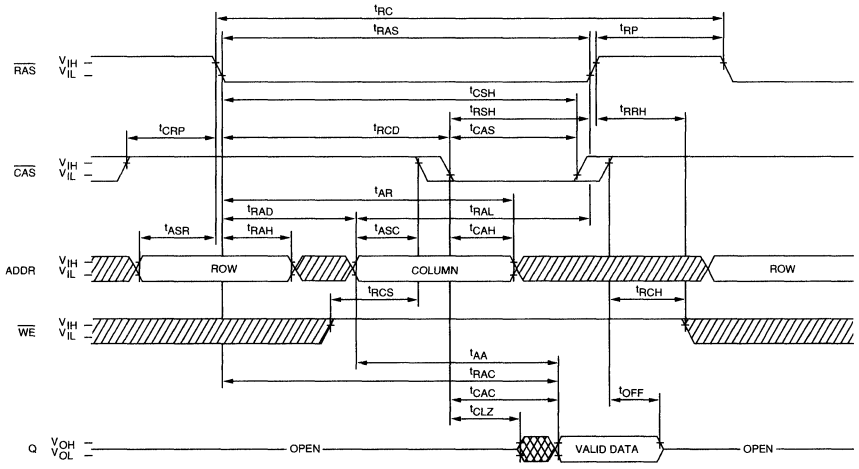
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^{t}WCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	55		60		75		ns	
Write command pulse width	^{t}WP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^{t}RWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^{t}CWL	20		20		25		ns	
Data-in setup time	^{t}DS	0		0		0		ns	22
Data-in hold time	^{t}DH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	70		80		100		ns	21
Column address to $\overline{WE}$ delay time	^{t}AWD	35		40		50		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	20		20		25		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	9, 10
Refresh period (512-cycles)	^{t}REF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CHR	15		15		15		ns	5

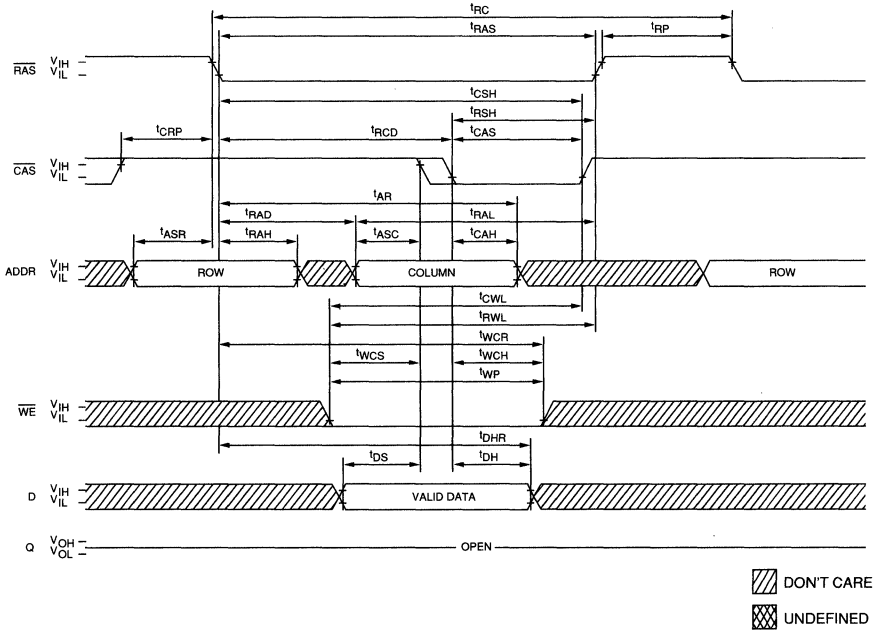
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ${}^{t}T$ = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that ${}^{t}RCD < {}^{t}RCD$ (MAX). If ${}^{t}RCD$ is greater than the maximum recommended value shown in this table, ${}^{t}RAC$ will increase by the amount that ${}^{t}RCD$ exceeds the value shown.
15. Assumes that ${}^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ${}^{t}CPN$.
17. Operation within the ${}^{t}RCD$ (MAX) limit ensures that ${}^{t}RAC$ (MAX) can be met. ${}^{t}RCD$ (MAX) is specified as a reference point only; if ${}^{t}RCD$ is greater than the specified ${}^{t}RCD$ (MAX) limit, then access time is controlled exclusively by ${}^{t}CAC$.
18. Operation within the ${}^{t}RAD$ (MAX) limit ensures that ${}^{t}RCD$ (MAX) can be met. ${}^{t}RAD$ (MAX) is specified as a reference point only; if ${}^{t}RAD$ is greater than the specified ${}^{t}RAD$ (MAX) limit, then access time is controlled exclusively by ${}^{t}AA$.
19. Either ${}^{t}RCH$ or ${}^{t}RRH$ must be satisfied for a READ cycle.
20. ${}^{t}OFF$ (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ${}^{t}WCS$, ${}^{t}RWD$, ${}^{t}AWD$ and ${}^{t}CWD$ are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If ${}^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^{t}RWD \geq {}^{t}RWD$ (MIN), ${}^{t}AWD \geq {}^{t}AWD$ (MIN) and ${}^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the cycle is a LATE-WRITE and the state of Q is indeterminate. (at access time and until $\overline{CAS}$ goes back to V_{IH})
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. All other inputs equal Vcc -0.2V.
25. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

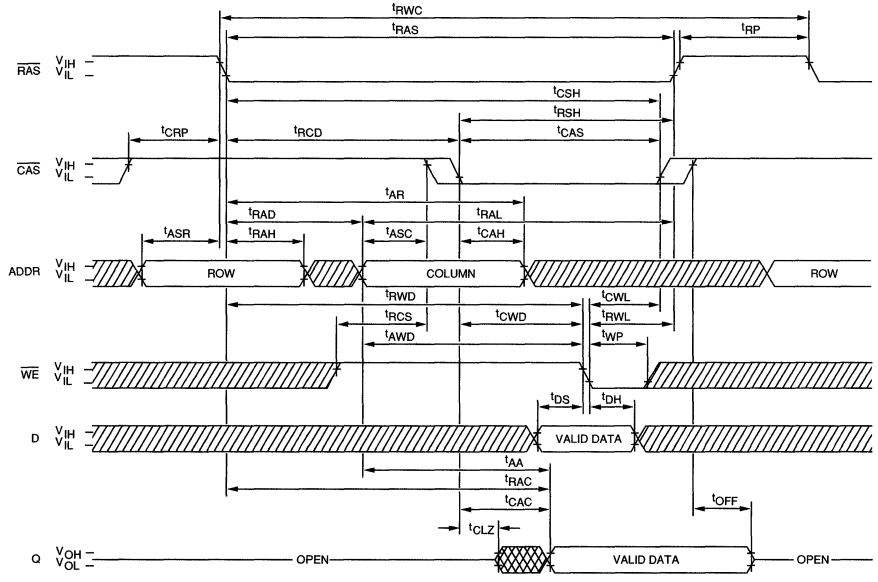
READ CYCLE



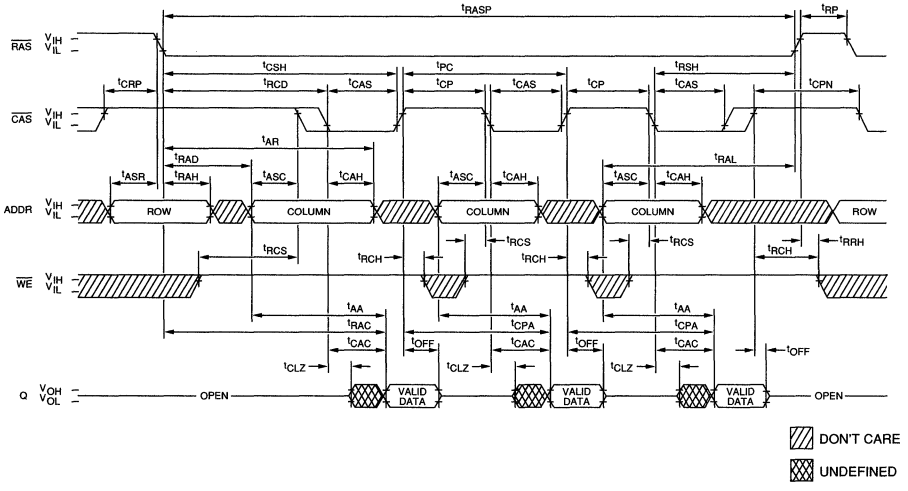
EARLY-WRITE CYCLE



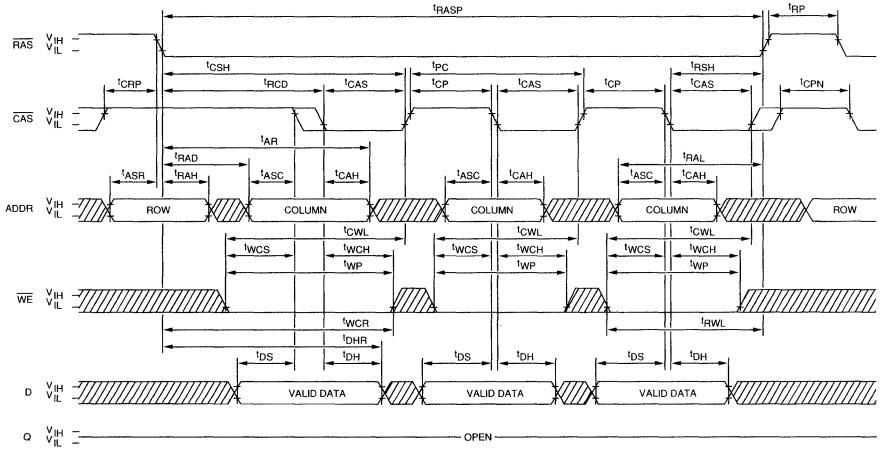
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



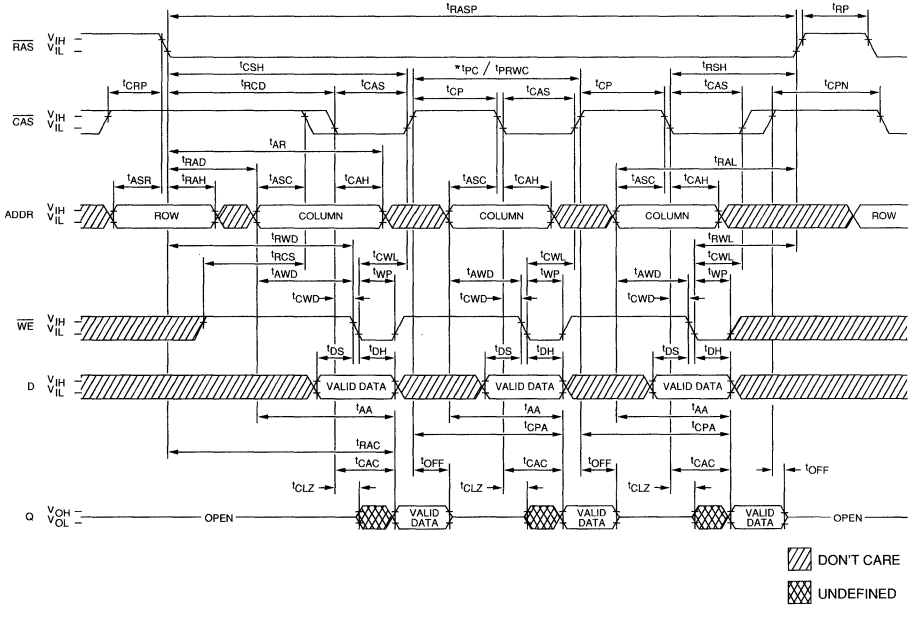
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

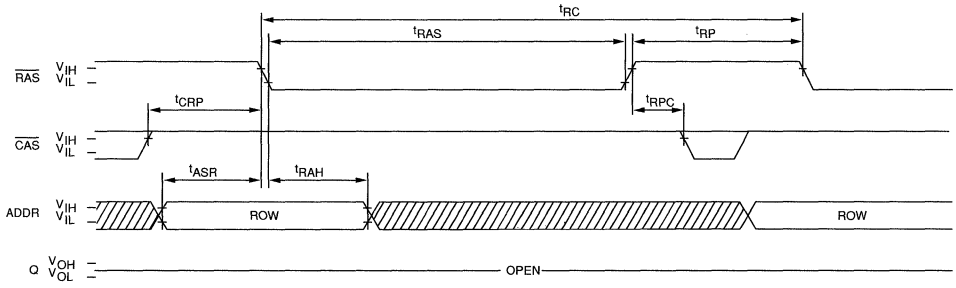


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

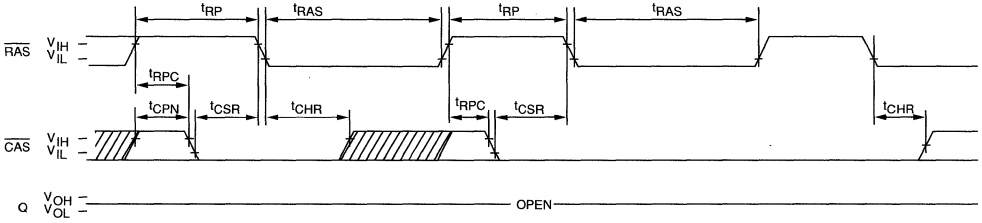


*tPC is for LATE-WRITE only.

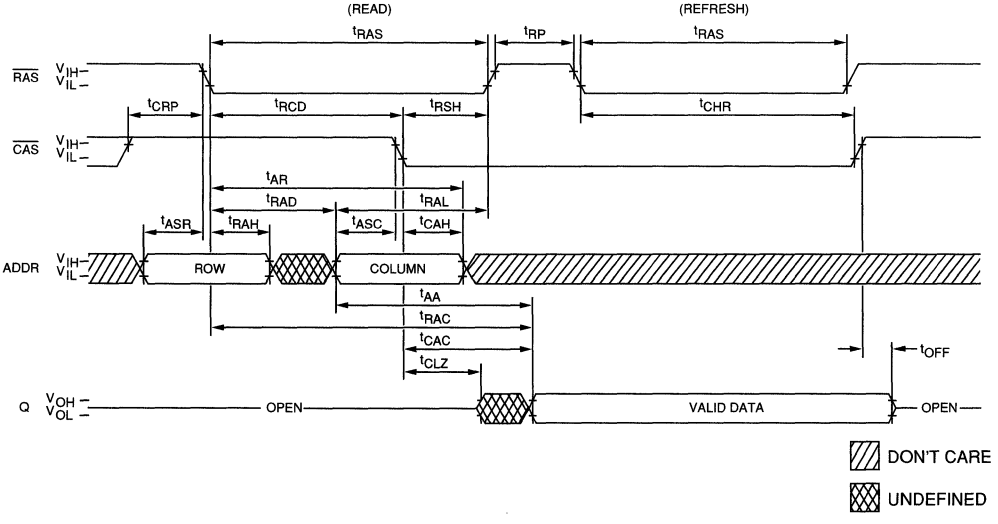
RAS-ONLY REFRESH CYCLE
(ADDR = A_0 - A_8; A_9 and WE = DON'T CARE)



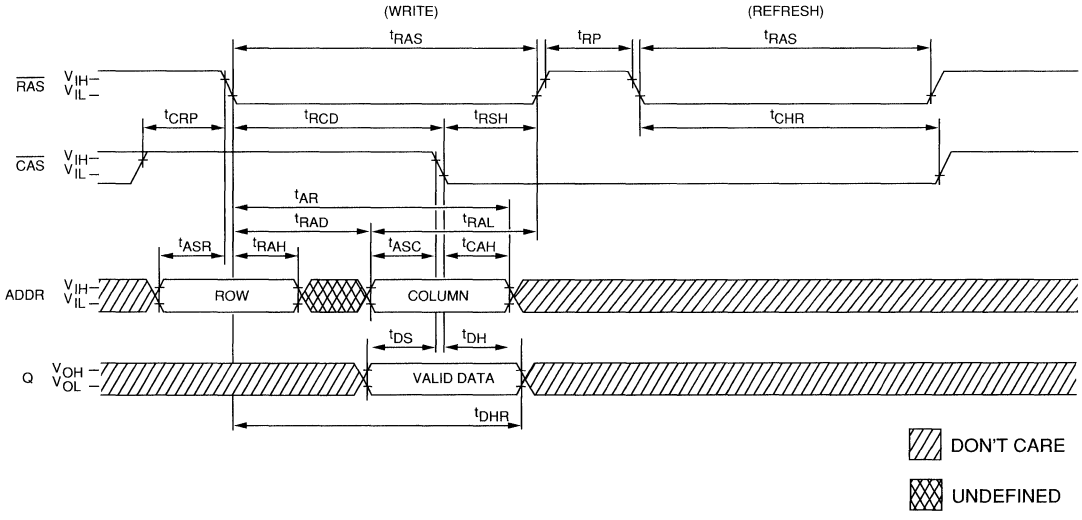
CAS-BEFORE-RAS REFRESH CYCLE
(A_0 - A_9 and WE = DON'T CARE)



HIDDEN REFRESH CYCLE
(WE = HIGH) [23]



HIDDEN REFRESH CYCLE
($\overline{WE}$ = LOW)



DRAM

1 MEG x 1 DRAM

STATIC COLUMN

FEATURES

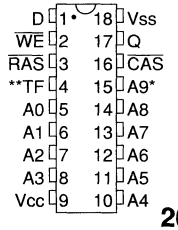
- Industry standard x1 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512-cycle refresh in 8ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, and HIDDEN
- Optional STATIC COLUMN access cycle

OPTIONS / MARKING

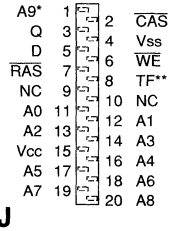
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Plastic DIP (300mil)	None
Ceramic DIP (300mil)	C
Plastic ZIP (350mil)	Z
Plastic SOJ (300mil)	DJ
Plastic TSOP (***)	VG
• Operating Temperature, TA	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

PIN ASSIGNMENT (Top View)

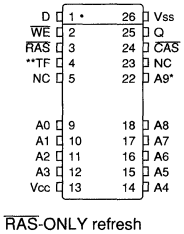
18-Pin DIP (A-3, B-2)



20-Pin ZIP (C-2)



20-Pin SOJ (E-1)



*Address not used for RAS-ONLY refresh
**TF = Test Function, VIN must not exceed Vcc+1V for normal operation
***Consult factory on availability of TSOP packages

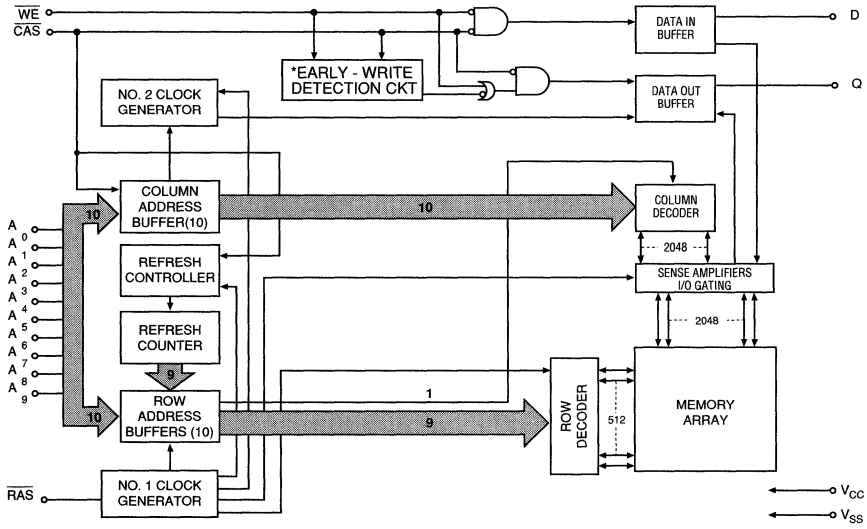
GENERAL DESCRIPTION

The MT4C1026 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin, data out (Q) remains open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the STATIC COLUMN operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CAS-BEFORE-RAS refresh will increment the refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection CKT output is a HIGH (EARLY WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address ^tR	Address ^tC	DATA D (Data In)	DATA Q (Data Out)
Standby		H	X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Valid Data In	Valid Data Out
STATIC COLUMN READ	1st Cycle	L	L	H	ROW	COL	Don't Care	Valid Data Out
	2nd Cycle	L	L	H	n/a	COL	Don't Care	Valid Data Out
STATIC COLUMN EARLY-WRITE	1st Cycle	L	L	L	ROW	COL	Valid Data In	High-Z
	2nd Cycle	L	L	H→L	n/a	COL	Valid Data In	High-Z
STATIC COLUMN READ-WRITE	1st Cycle	L	L	H→L	ROW	COL	Valid Data In	Valid Data Out
	2nd Cycle	L	L	H→L	n/a	COL	Valid Data In	Valid Data Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Don't Care	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In	High-Z
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -55°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 600mW
Soldering Temperature (soldering 10 sec) ..... 260°C
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-2.0	0.8	V	1, 25
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	80	70	60	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	60	50	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	80	70	60	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	80	70	60	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	155		175		205		ns	
STATIC-COLUMN READ or WRITE cycle time	t_{SC}	40		45		55		ns	
STATIC-COLUMN READ-WRITE cycle time	t_{SRMC}	70		80		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Access time from column address	t_{AA}		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

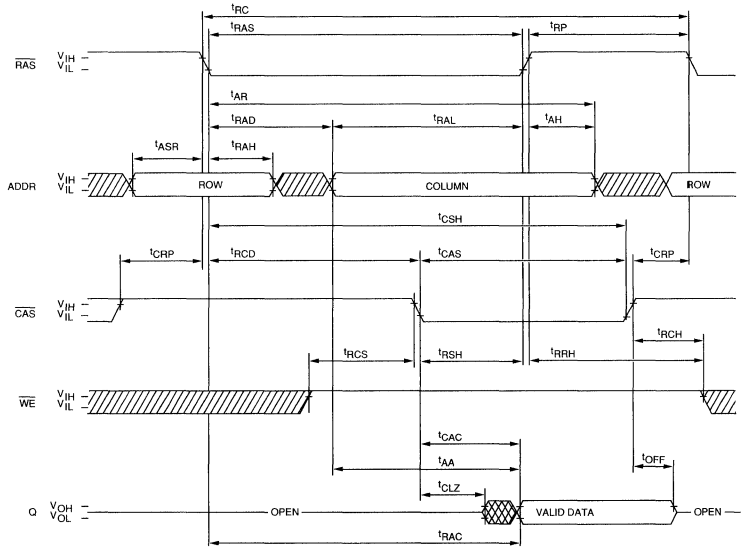
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	70		80		100		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	35		40		50		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		20		25		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
Write inactive time	^tWI	10		10		10		ns	
Last WRITE to column address delay time	^tLWAD	20	30	20	35	25	45	ns	
Last WRITE to column address hold time	^tAHLW	65		75		95		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	10		10		10		ns	
Output data hold time from column address	^tAOH	5		5		5		ns	
Output data enable from WRITE	^tOW	^tAA		^tAA		^tAA		ns	
Access time from last WRITE	^tALW	65		75		95		ns	
Column address hold time referenced to $\overline{RAS}$ HIGH	^tAH	5		5		10		ns	
CAS pulse width in STATIC-COLUMN mode	^tCSC	^tCAS		^tCAS		^tCAS		ns	
Output data hold from WRITE	^tWOH	0		0		0		ns	

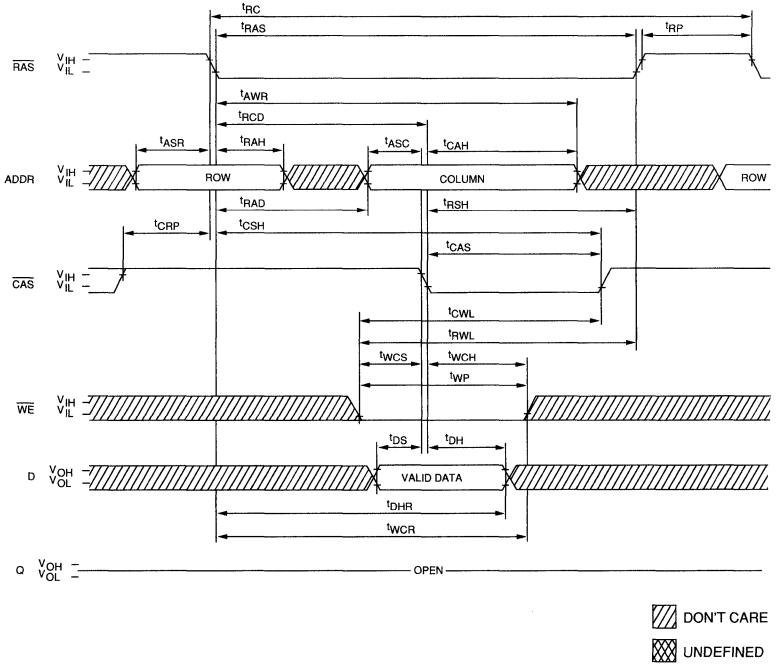
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ${}^{t}T$ = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that ${}^{t}RCD < {}^{t}RCD$ (MAX). If ${}^{t}RCD$ is greater than the maximum recommended value shown in this table, ${}^{t}RAC$ will increase by the amount that ${}^{t}RCD$ exceeds the value shown.
15. Assumes that ${}^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ${}^{t}CPN$.
17. Operation within the ${}^{t}RCD$ (MAX) limit ensures that ${}^{t}RAC$ (MAX) can be met. ${}^{t}RCD$ (MAX) is specified as a reference point only; if ${}^{t}RCD$ is greater than the specified ${}^{t}RCD$ (MAX) limit, then access time is controlled exclusively by ${}^{t}CAC$.
18. Operation within the ${}^{t}RAD$ (MAX) limit ensures that ${}^{t}RCD$ (MAX) can be met. ${}^{t}RAD$ (MAX) is specified as a reference point only; if ${}^{t}RAD$ is greater than the specified ${}^{t}RAD$ (MAX) limit, then access time is controlled exclusively by ${}^{t}AA$.
19. Either ${}^{t}RCH$ or ${}^{t}RRH$ must be satisfied for a READ cycle.
20. ${}^{t}OFF$ (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ${}^{t}WCS$, ${}^{t}RWD$, ${}^{t}AWD$ and ${}^{t}CWD$ are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If ${}^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^{t}RWD \geq {}^{t}RWD$ (MIN), ${}^{t}AWD \geq {}^{t}AWD$ (MIN) and ${}^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the cycle is a LATE-WRITE and the state of Q is indeterminate. (at access time and until $\overline{CAS}$ goes back to V_{IH})
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. All other inputs equal Vcc -0.2V.
25. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

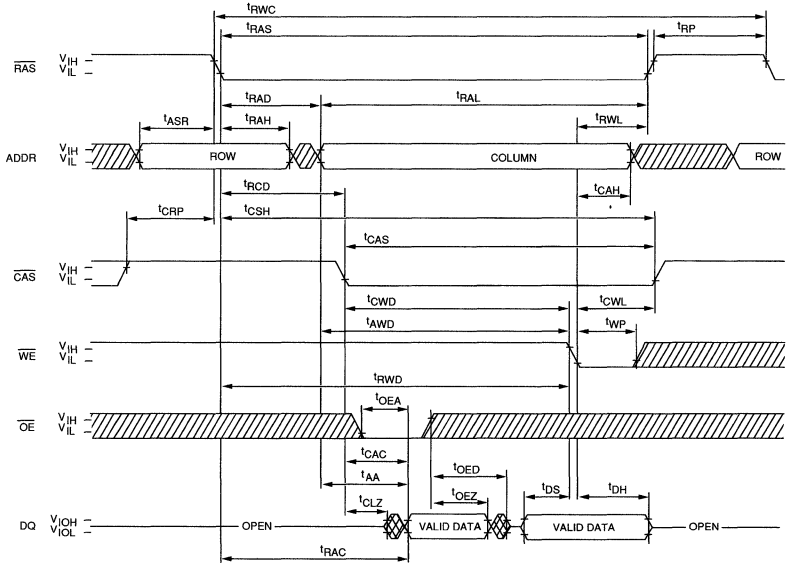
READ CYCLE



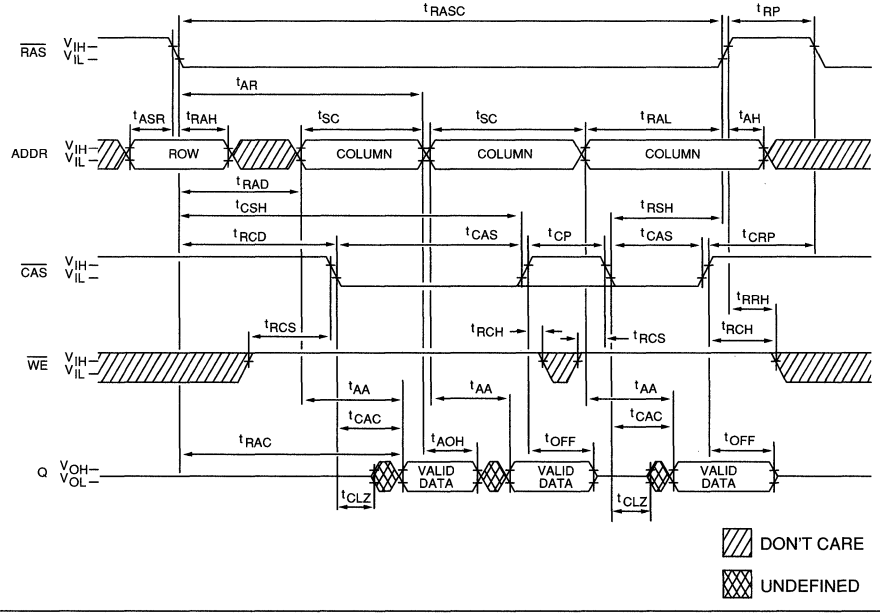
EARLY-WRITE CYCLE



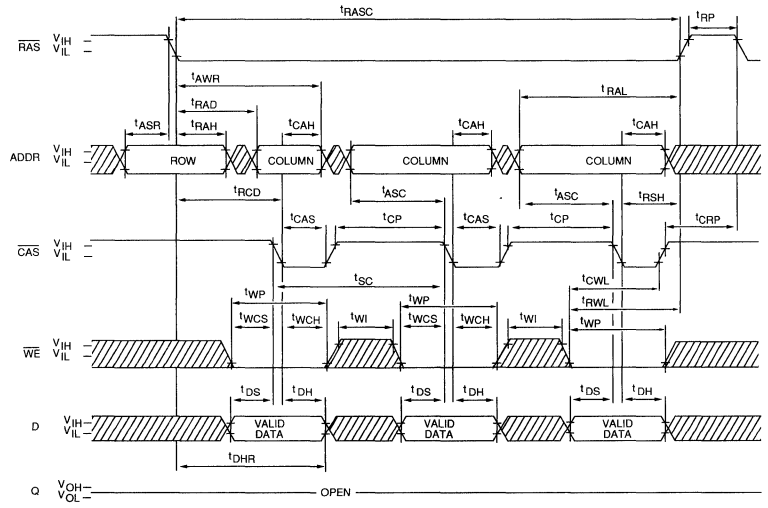
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



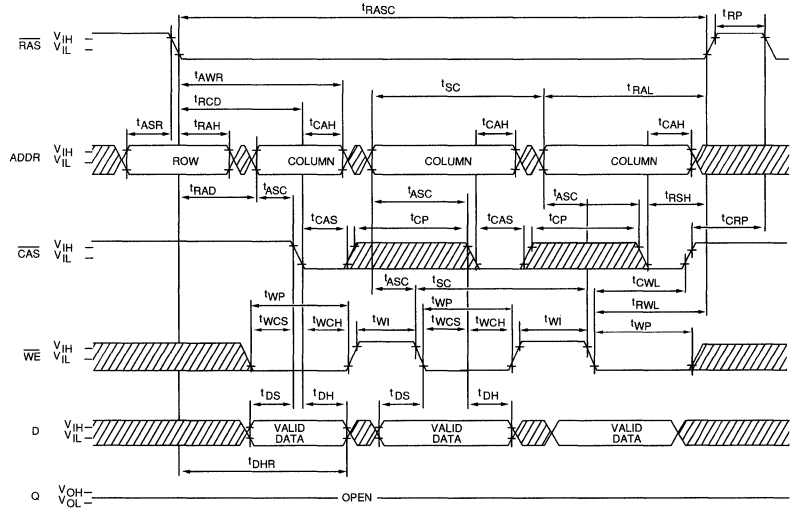
STATIC-COLUMN READ CYCLE



STATIC-COLUMN EARLY-WRITE CYCLE
(CAS Controlled)



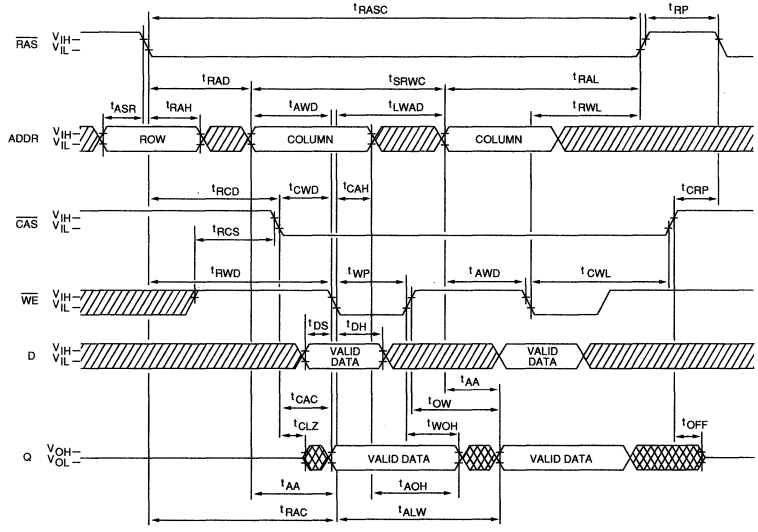
STATIC-COLUMN EARLY-WRITE CYCLE
(WE Controlled)



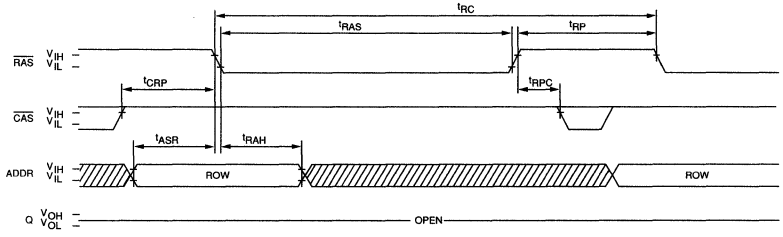
DON'T CARE

UNDEFINED

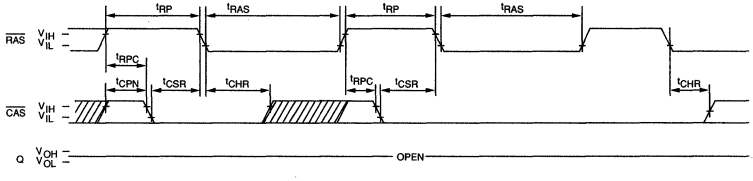
STATIC-COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



RAS-ONLY REFRESH CYCLE
(ADDR = A_0 - A_8; A_9 and WE = DON'T CARE)

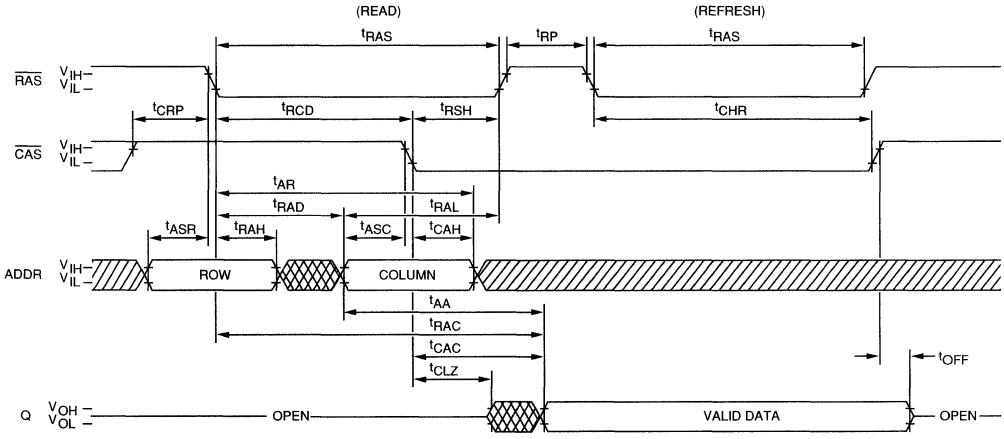


CAS-BEFORE-RAS REFRESH CYCLE
(A_0 - A_9 and WE = DON'T CARE)

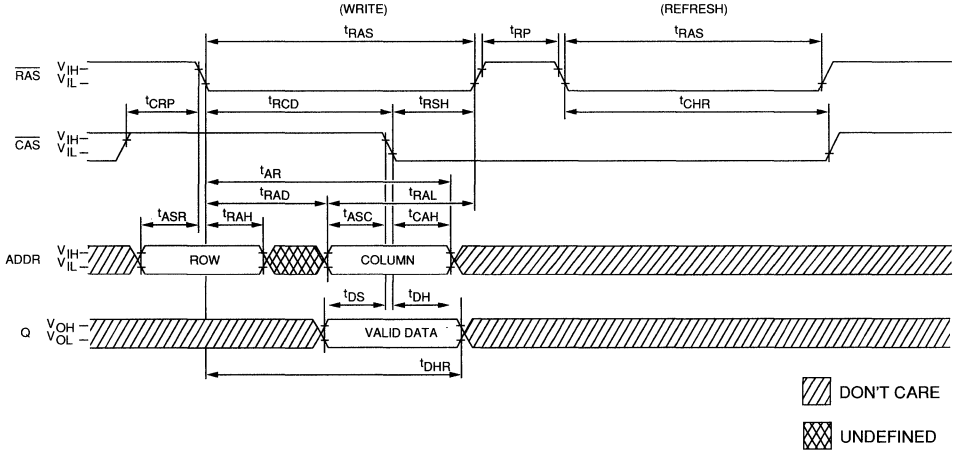


DON'T CARE
UNDEFINED

HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH) [23]



HIDDEN REFRESH CYCLE
($\overline{WE}$ = LOW)



DRAM

1 MEG x 1 DRAM

LOW POWER, FAST PAGE MODE

FEATURES

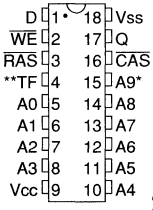
- Industry standard x1 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 1.0mW standby; 150mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512-cycle refresh in 64ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional FAST PAGE MODE access cycle
- Low CMOS STANDBY CURRENT, 200µA maximum

OPTIONS

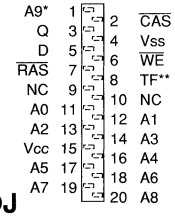
	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Plastic DIP (300mil)	None
Ceramic DIP (300mil)	C
Plastic ZIP (350mil)	Z
Plastic SOJ (300mil)	DJ
Plastic TSOP (***)	VG
• Operating Temperature, TA	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

PIN ASSIGNMENT (Top View)

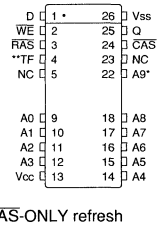
18-Pin DIP
(A-3, B-2)



20-Pin ZIP
(C-2)



20-Pin SOJ
(E-1)



*Address not used for $\overline{RAS}$-ONLY refresh
**TF = Test Function, VIN must not exceed Vcc+1V for normal operation
***Consult factory on availability of TSOP packages

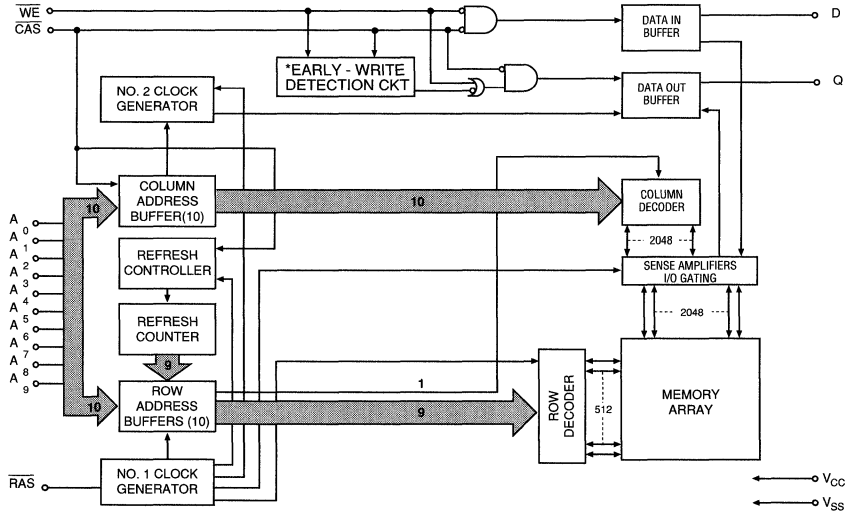
GENERAL DESCRIPTION

The MT4C1027 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin, data out (Q), remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 64ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh will increment the refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
LOW POWER, FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection CKT output is a HIGH (EARLY WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address		DATA	
					^tR	^tC	D (Data In)	Q (Data Out)
Standby		H	X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Valid Data In	Valid Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Don't Care	Valid Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Don't Care	Valid Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Valid Data In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Valid Data In	Valid Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Valid Data In	Valid Data Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Don't Care	Valid Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Valid Data In	High-Z
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -55°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 600mW
Soldering Temperature (soldering 10 sec) ..... 260°C
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-2.0	0.8	V	1, 25
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	75	65	60	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	55	45	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	200	200	200	µA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	75	65	60	mA	3, 5
BATTERY BACKUP REFRESH CURRENT Average power supply current during battery backup refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) of 1µs; $\overline{WE}$, A0-A9 and D in = Vcc -0.2V or 0.2V (D in may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	200	200	200	µA	5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	155		175		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	65		70		85		ns	
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	15
Access time from column address	^tAA		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		50	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	35	15	40	20	50	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

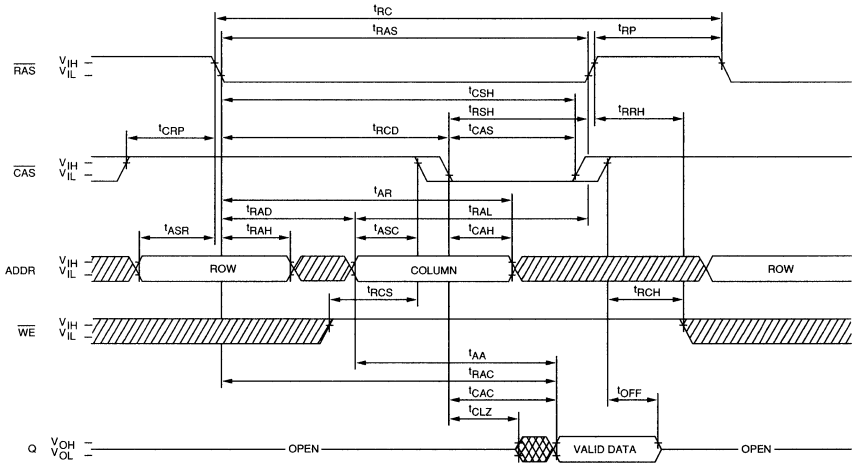
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	70		80		100		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	35		40		50		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		20		25		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512-cycles)	^tREF		64		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5

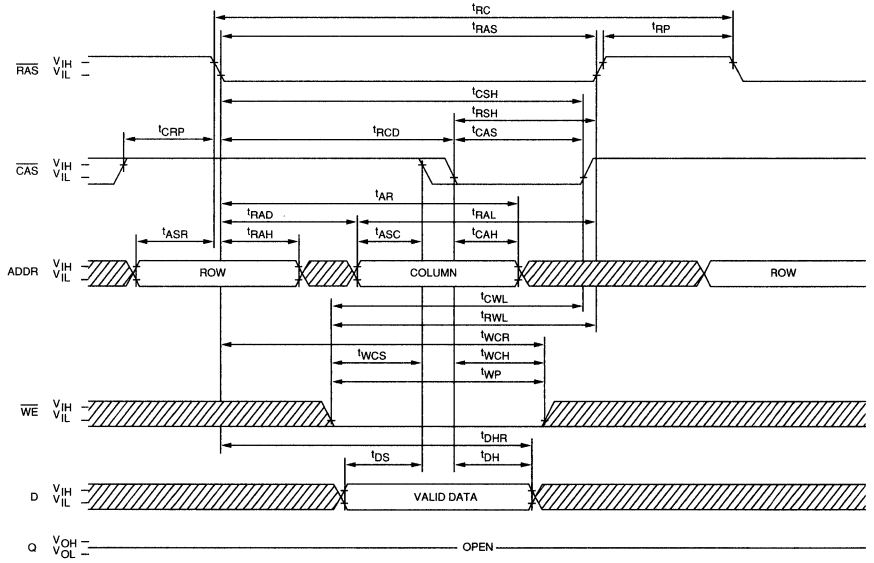
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 64ms refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the cycle is a LATE-WRITE and the state of Q is indeterminate. (at access time and until $\overline{CAS}$ goes back to V_{IH})
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. All other inputs equal Vcc -02V.
25. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

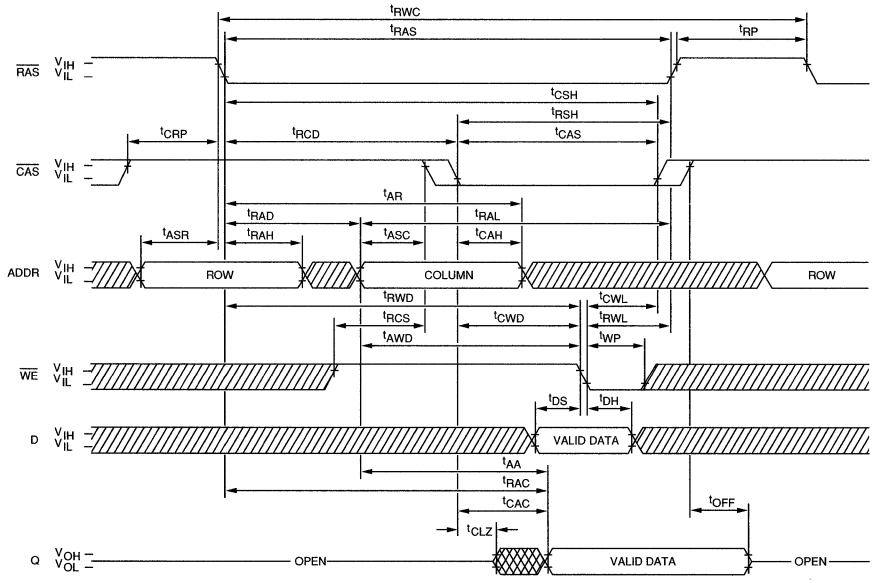
READ CYCLE



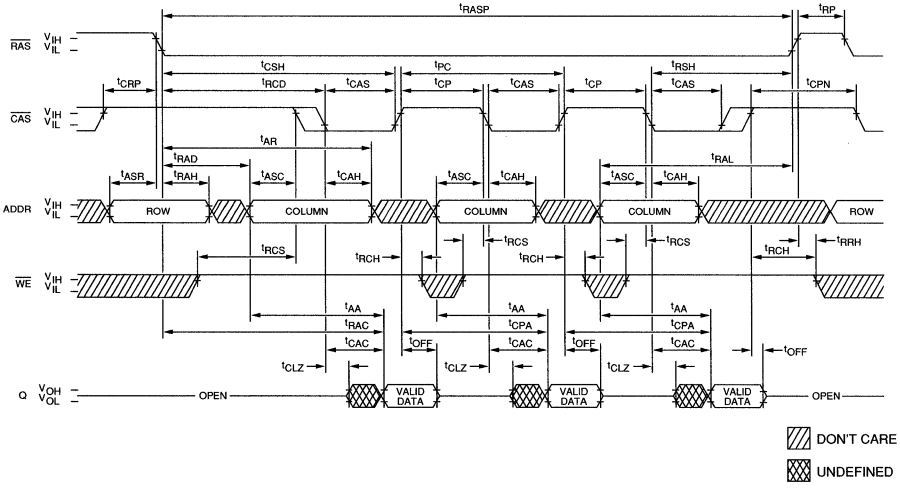
EARLY-WRITE CYCLE



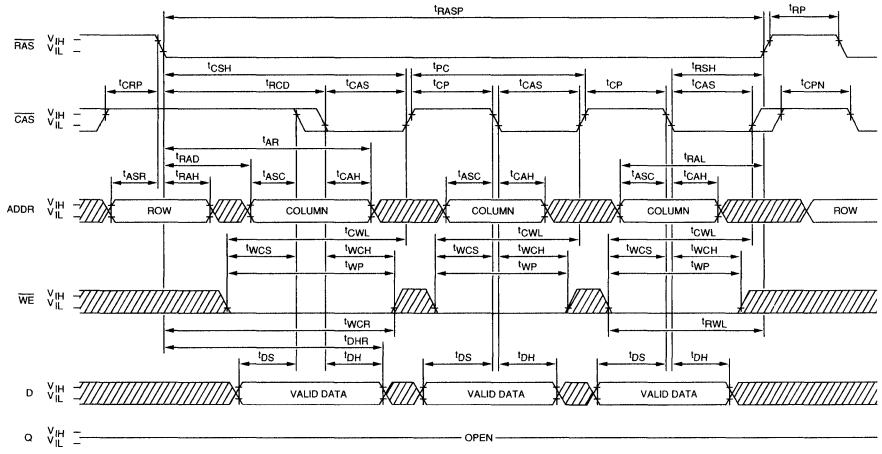
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



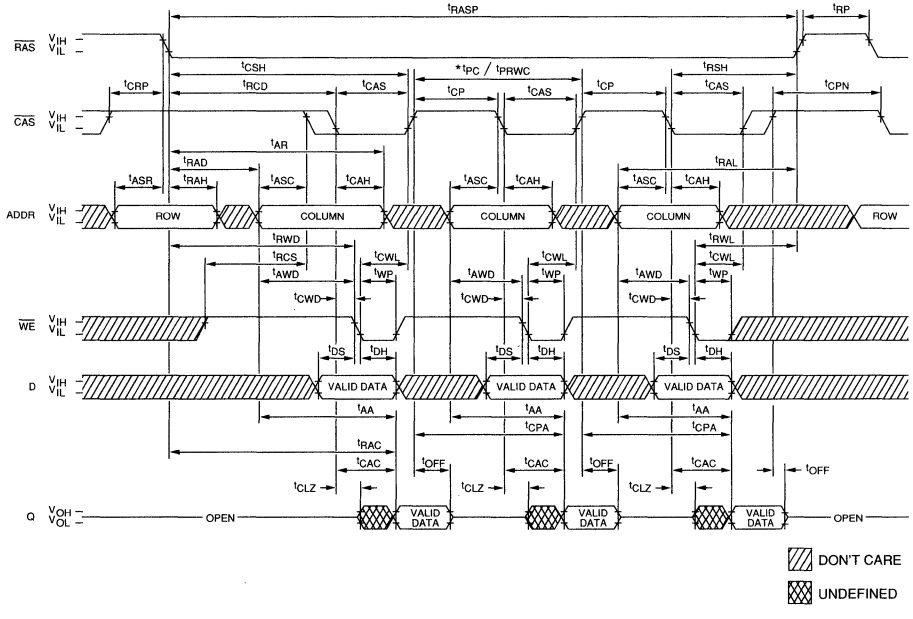
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

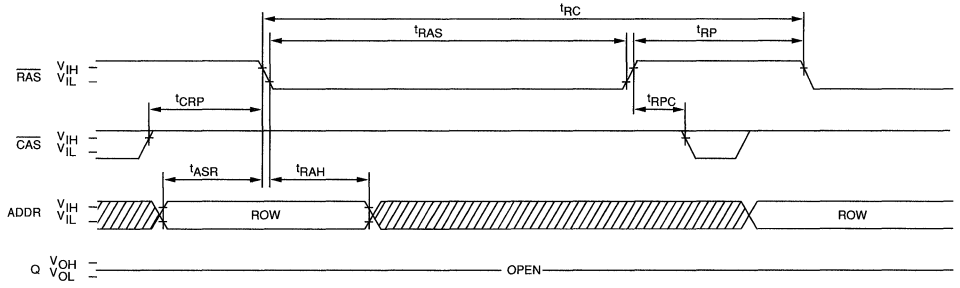


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

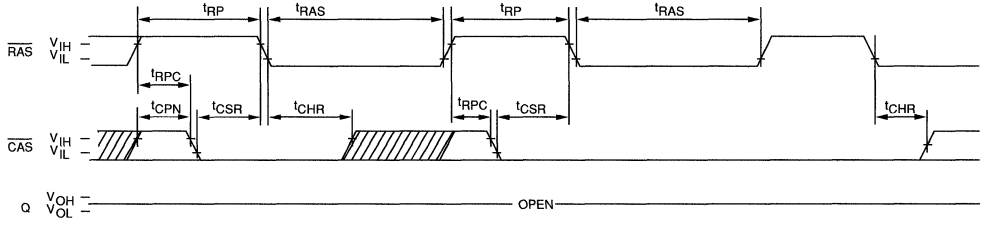


*tPC is for LATE-WRITE only.

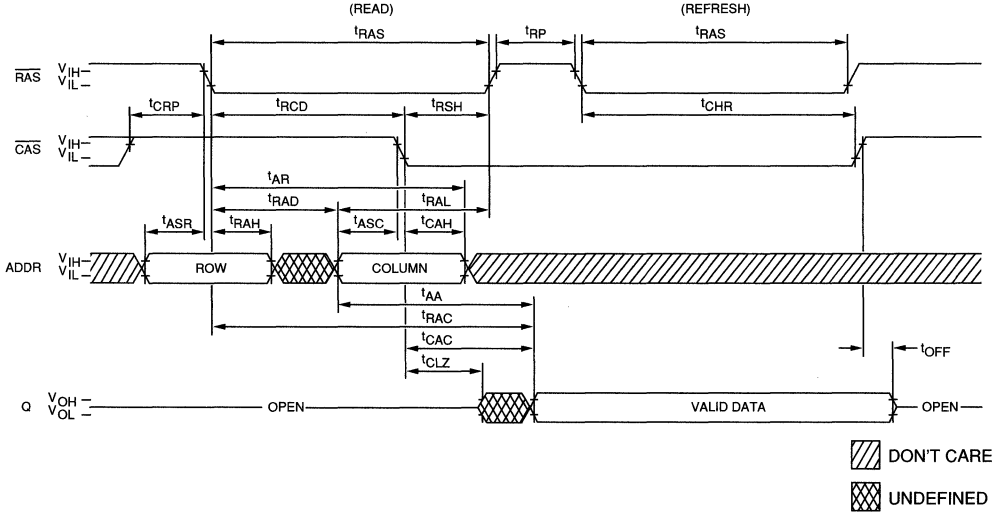
$\overline{RAS}$-ONLY REFRESH CYCLE
($ADDR = A_0 - A_8$; A_9 and $\overline{WE}$ = DON'T CARE)



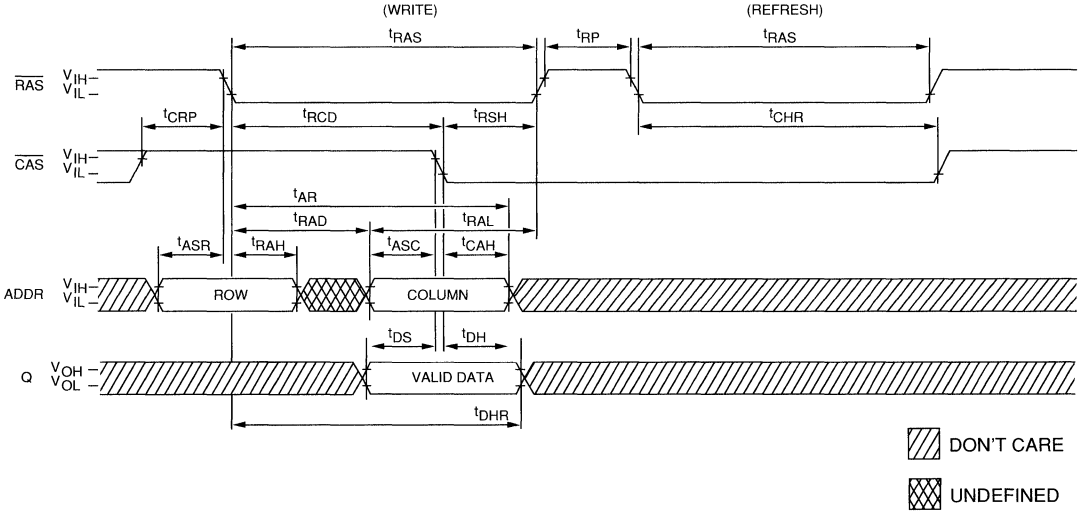
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
($A_0 - A_9$ and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH)[23]



HIDDEN REFRESH CYCLE
($\overline{WE}$ = LOW)



DRAM

4 MEG x 1 DRAM

FAST PAGE MODE

FEATURES

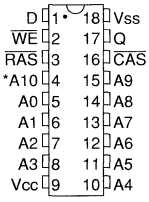
- Industry standard x1 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{CBR}$), and HIDDEN
- FAST PAGE MODE access cycle
- 300 and 350 mil wide SOJ packages
- Two $\overline{CBR}$ options: $\overline{CBR}$ with $\overline{WE}$ a don't care (1 Meg compatible) and $\overline{CBR}$ with $\overline{WE}$ a HIGH (JEDEC test mode capable via WCBR)

OPTIONS / MARKING

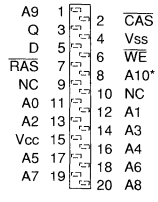
- Timing
  - 60ns access -6
  - 70ns access -7
  - 80ns access -8
- Packages
  - Ceramic DIP (300mil) CN
  - Ceramic DIP (400mil) C
  - Plastic ZIP (350mil) Z
  - Plastic SOJ (300mil) DJ
  - Plastic SOJ (350mil) DJW
  - Plastic TSOP (**) TG
- $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh
  - $\overline{CBR}$ with $\overline{WE}$ a don't care None
  - $\overline{CBR}$ with $\overline{WE}$ a HIGH J

PIN ASSIGNMENT (Top View)

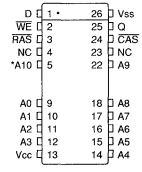
18-Pin CDIP (B-2, B-3)



20-Pin ZIP (C-3)



20-Pin SOJ (E-1, E-2)



*Address not used for $\overline{RAS}$-ONLY refresh
**Consult factory on availability of TSOP packages

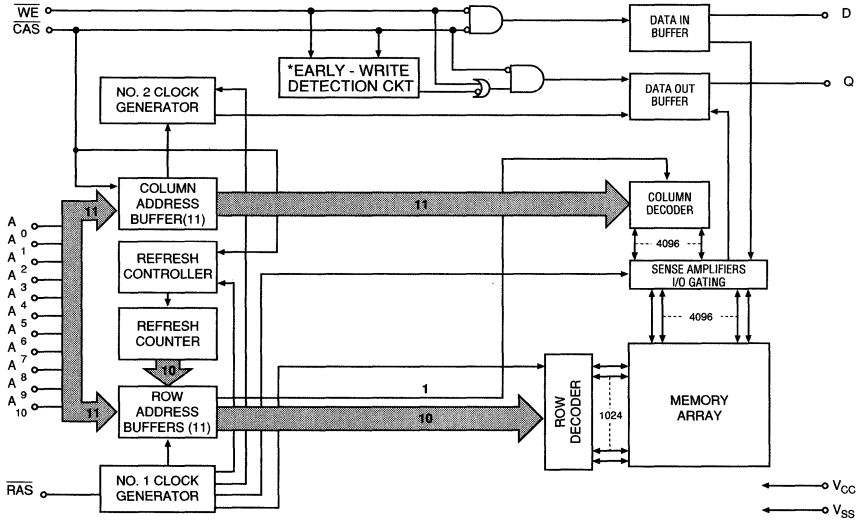
GENERAL DESCRIPTION

The MT4C1004 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection CKT output is a HIGH (EARLY WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address		DATA	
					^tR	^tC	D (Data In)	Q (Data Out)
Standby		H	X	X	X	X	Don't Care	High Impedance
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High Impedance
READ-WRITE		L	L	H→L	ROW	COL	Valid Data In	Valid Data Out
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Don't Care	Valid Data Out
	2nd Cycle	L	H→L	H	n/a	COL	Don't Care	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Valid Data In	High Impedance
	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In	High Impedance
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Valid Data In	Valid Data Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Valid Data In	Valid Data Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Don't Care	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In	High Impedance
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	Standard	H→L	L	X	X	X	Don't Care	High Impedance
	"J" Option	H→L	L	H	X	X	Don't Care	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} .....-1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	135		155		175		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	60		65		70		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		40		45	ns	25
$\overline{RAS}$ pulse width	^tRAS	60	100,00	70	100,00	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,00	70	100,00	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

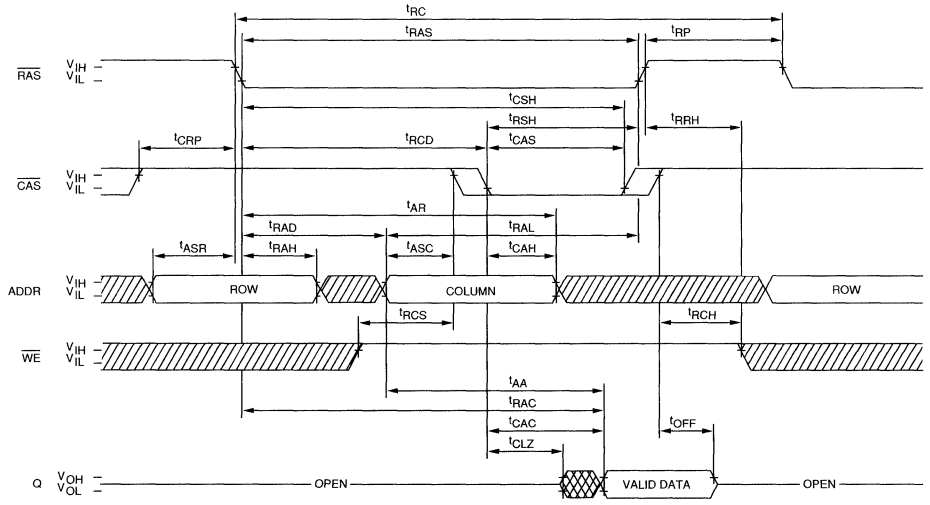
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^{t}WCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		60		ns	
Write command pulse width	^{t}WP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		20		ns	
Data-in setup time	^{t}DS	0		0		0		ns	22
Data-in hold time	^{t}DH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	60		70		80		ns	21
Column address to $\overline{WE}$ delay time	^{t}AWD	30		35		40		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	15		15		20		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	^{t}REF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}WRH	10		10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}WRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	^{t}WTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	^{t}WTS	10		10		10		ns	24

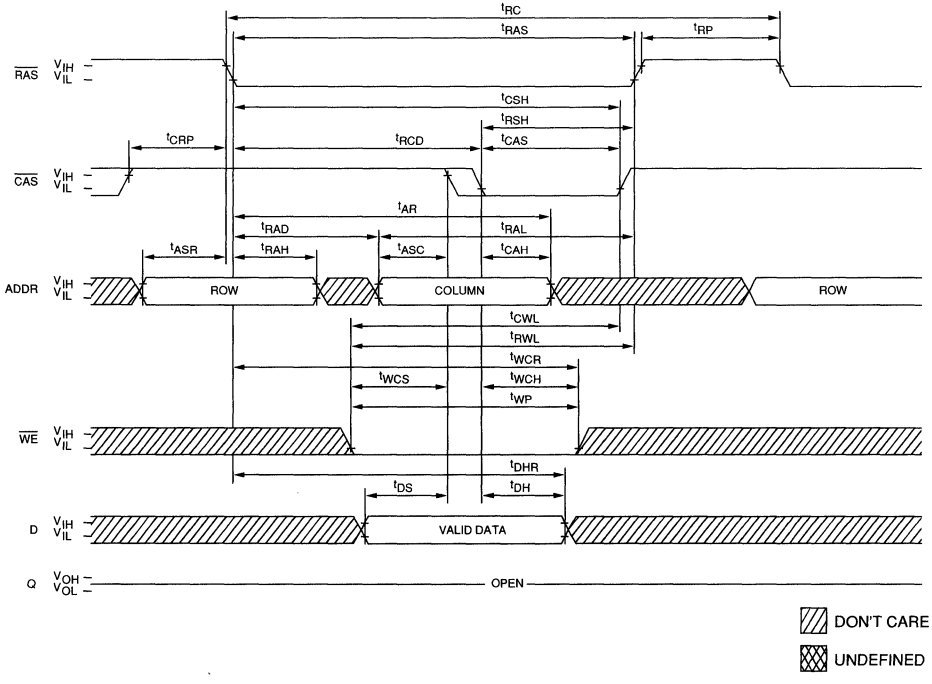
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the cycle is a LATE-WRITE and the state of data out is indeterminate. (at access time and until $\overline{CAS}$ goes back to V_{IH})
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. ^tWTS and ^tWTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.

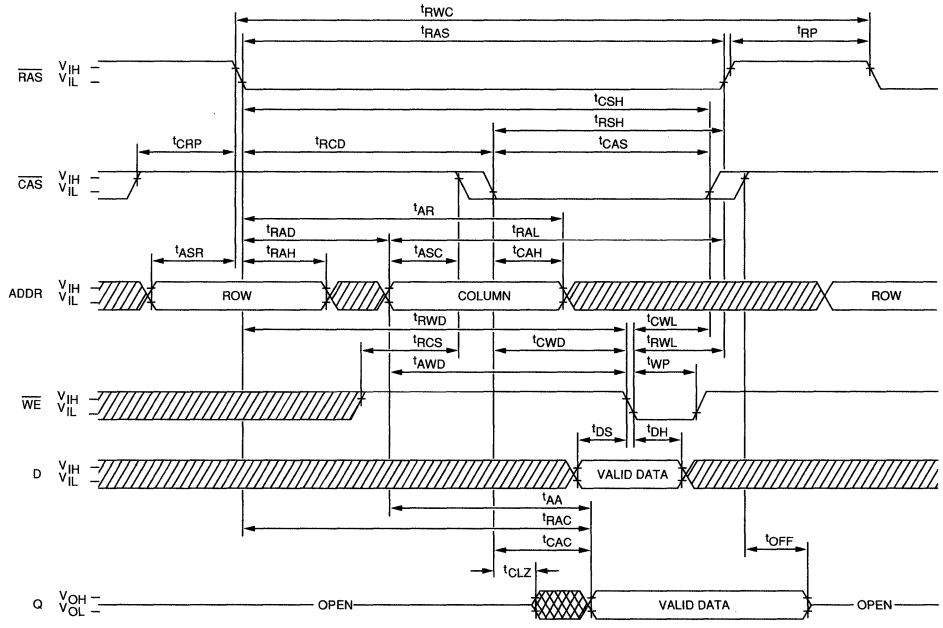
READ CYCLE



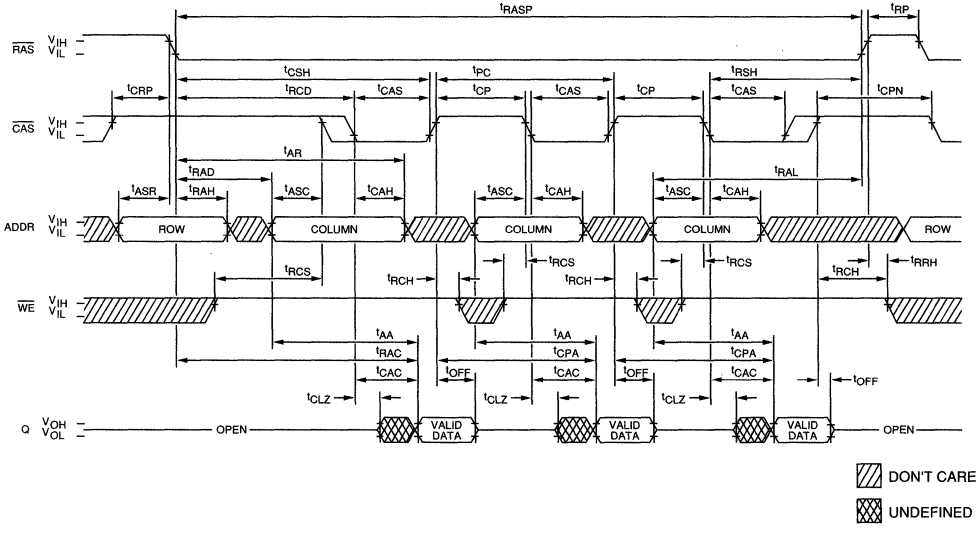
EARLY-WRITE CYCLE



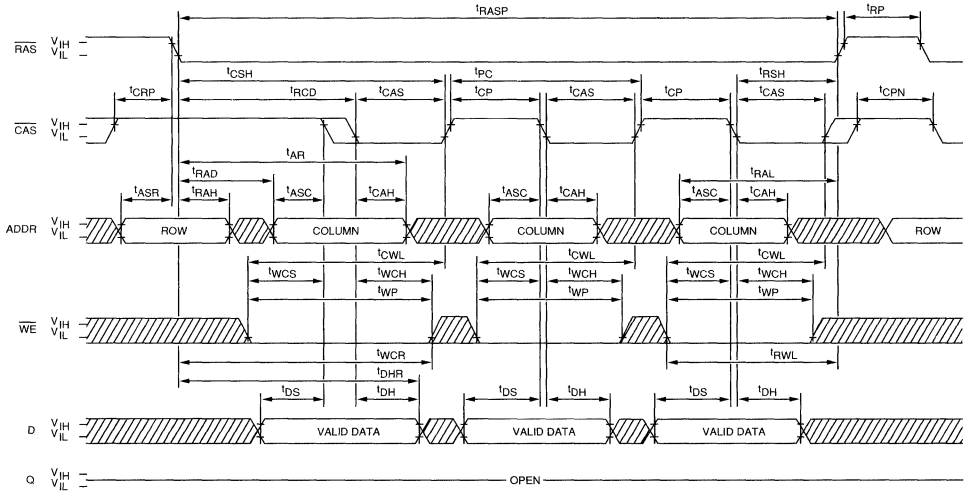
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



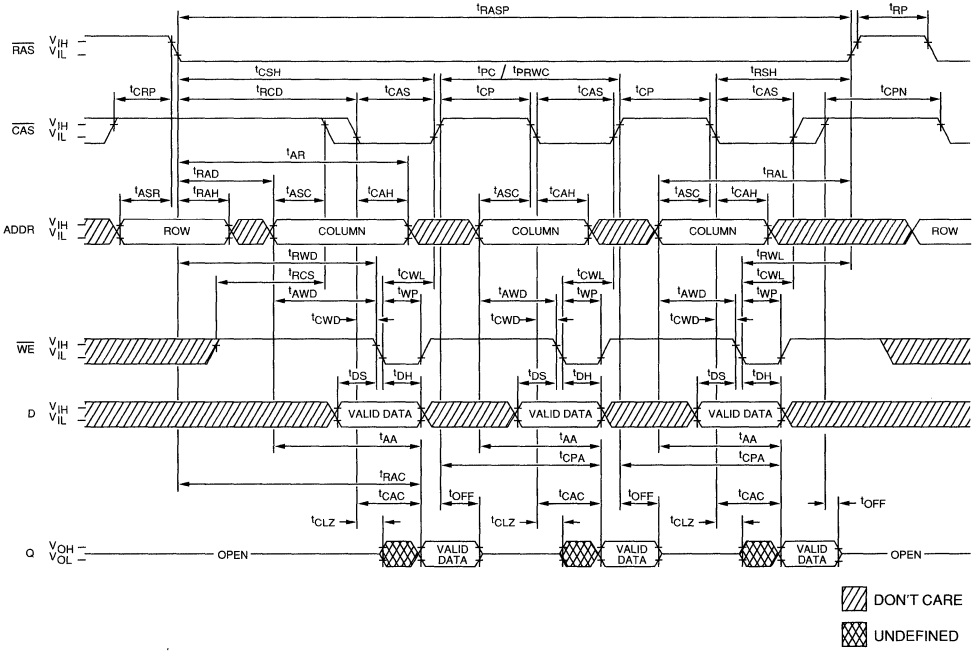
FAST-PAGE-MODE READ CYCLE



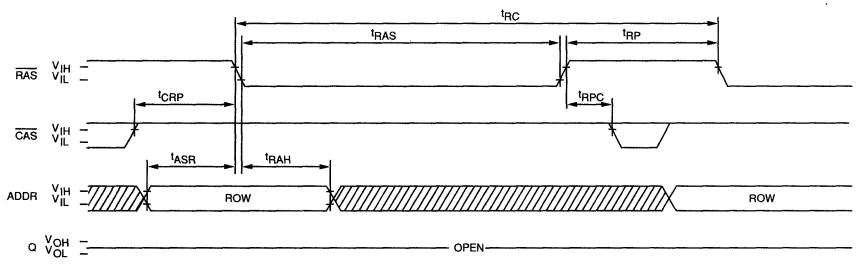
FAST-PAGE MODE EARLY-WRITE CYCLE



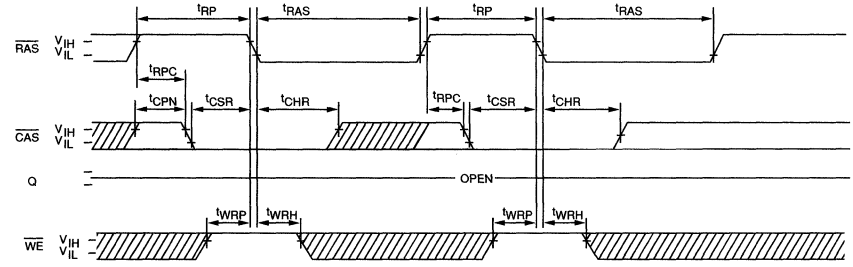
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



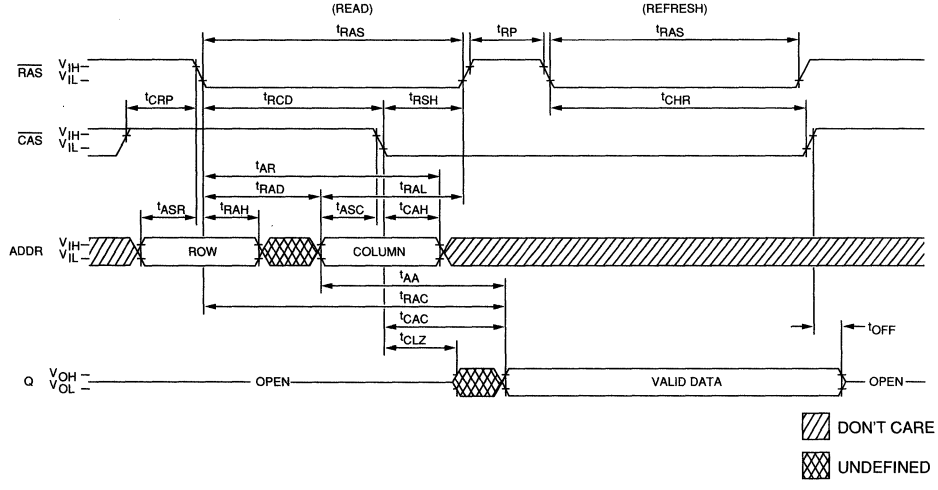
$\overline{RAS}$-ONLY REFRESH CYCLE
($ADDR = A_0 - A_9$; A_{10} and $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
($A_0 - A_{10}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH) [23]



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a don't care. The 4 Meg, on the other hand, specifies the CBR REFRESH mode to be a $\overline{W}$CBR, which is CBR with the $\overline{WE}$ pin held at a logical HIGH level.

The reason for $\overline{W}$CBR instead of CBR on the 4 Meg is that a CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode ($\overline{W}$CBR). In contrast, the 1 Meg test mode is entered by applying a HIGH signal to the test pin (pin 4 on DIP, pin 5 on SOJ and pin 8 on ZIP). This HIGH signal is usually a "supervoltage" (V in ≥ 7.5V) so normal TTL or CMOS HIGH levels will not cause the part to enter the test mode.

POWER-UP

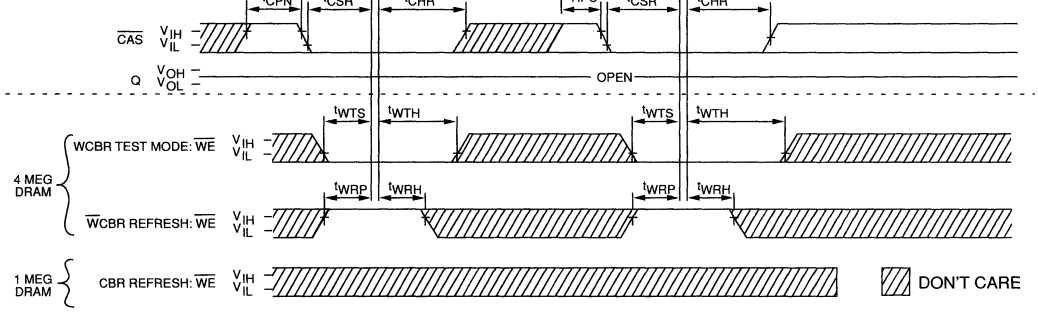
The 4 Meg $\overline{W}$CBR constraint may also introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any 8 $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that 8 $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a $\overline{W}$CBR REFRESH cycle.

SUMMARY

1. The optional 1 Meg test pin is the A10 pin on the 4 Meg .
2. For optional test mode, the 1 Meg requires a valid HIGH on the test pin while the 4 Meg requires a CBR cycle with $\overline{WE}$ LOW.
3. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH ($\overline{W}$CBR).
4. The 8 $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or $\overline{W}$CBR REFRESH cycles.

SPECIAL FEATURE

A memory system currently using 1 Meg DRAMs with $\overline{WE}$ as a don't care during CBR REFRESH does not allow for direct upgrading to 4 Meg DRAMs. Micron, realizing some applications will have this situation, provides a special feature on its 4 Meg DRAM, that requires "supervoltage" to access the 4 Meg JEDEC WCBR test function. This allows the Micron 4 Meg DRAM to be refreshed in the same manner as any 1 MEG DRAM. Note that the eight power-up cycles should only be refresh cycles in order to guarantee that any 4 Meg DRAM, including Micron's, does not inadvertently power-up in the test mode.



COMPARISON OF 4 MEG TEST MODE AND $\overline{W}$CBR TO 1 MEG CBR

DRAM

4 MEG x 1 DRAM

STATIC COLUMN

FEATURES

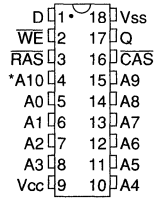
- Industry standard x1 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{CBR}$), and HIDDEN
- STATIC COLUMN access cycle
- 300 and 350 mil wide SOJ packages
- Two $\overline{CBR}$ options: $\overline{CBR}$ with $\overline{WE}$ a don't care (1 Meg compatible) and $\overline{CBR}$ with $\overline{WE}$ a HIGH (JEDEC test mode capable via WCBR)

OPTIONS — MARKING

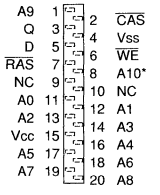
- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Ceramic DIP (300mil) — C
  - Ceramic DIP (400mil) — CN
  - Plastic ZIP (350mil) — Z
  - Plastic SOJ (300mil) — DJ
  - Plastic SOJ (350mil) — DJW
  - Plastic TSOP (**) — TG
- $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh
  - $\overline{CBR}$ with $\overline{WE}$ a don't care — None
  - $\overline{CBR}$ with $\overline{WE}$ a HIGH — J

PIN ASSIGNMENT (Top View)

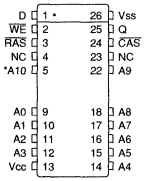
18-Pin CDIP (B-2, B-3)



20-Pin ZIP (C-3)



20-Pin SOJ (E-1, E-2)



*Address not used for $\overline{RAS}$-ONLY refresh
**Consult factory on availability of TSOP packages

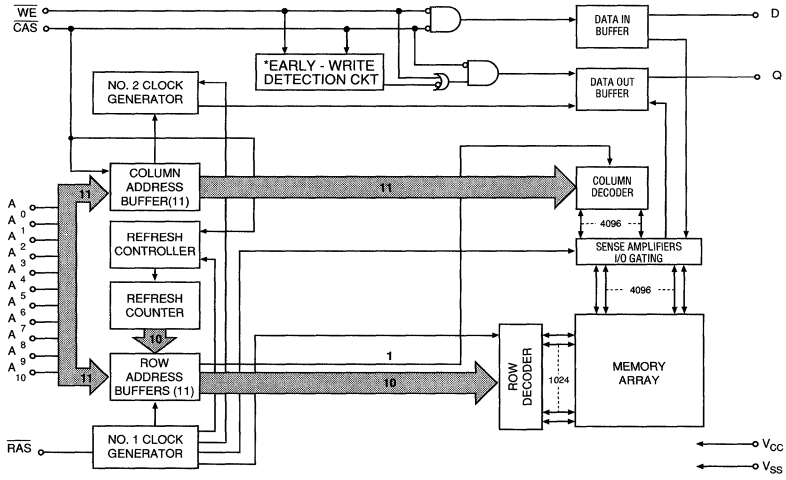
GENERAL DESCRIPTION

The MT4C1006 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A10) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection CKT output is a HIGH (EARLY WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address		DATA	
					^tR	^tC	D (Data In)	Q (Data Out)
Standby		H	X	X	X	X	Don't Care	High Impedance
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High Impedance
READ-WRITE		L	L	H→L	ROW	COL	Valid Data In	Valid Data Out
STATIC COLUMN READ	1st Cycle	L	L	H	ROW	COL	Don't Care	Valid Data Out
	2nd Cycle	L	L	H	n/a	COL	Don't Care	Valid Data Out
STATIC COLUMN WRITE	1st Cycle	L	L	L	ROW	COL	Valid Data In	High Impedance
	2nd Cycle	L	L	H→L	n/a	COL	Valid Data In	High Impedance
STATIC COLUMN READ-WRITE	1st Cycle	L	L	H→L	ROW	COL	Valid Data In	Valid Data Out
	2nd Cycle	L	L	H→L	n/a	COL	Valid Data In	Valid Data Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Don't Care	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In	High Impedance
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	Standard	H→L	L	X	X	X	Don't Care	High Impedance
	"J" Option	H→L	L	H	X	X	Don't Care	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	135		155		175		ns	
STATIC-COLUMN READ or WRITE cycle time	^tSC	40		40		45		ns	
STATIC-COLUMN READ-WRITE cycle time	^tSRMC	65		70		75		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		40		45	ns	25
$\overline{RAS}$ pulse width	^tRAS	60	100,00	70	100,00	80	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	60	100,00	70	100,00	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

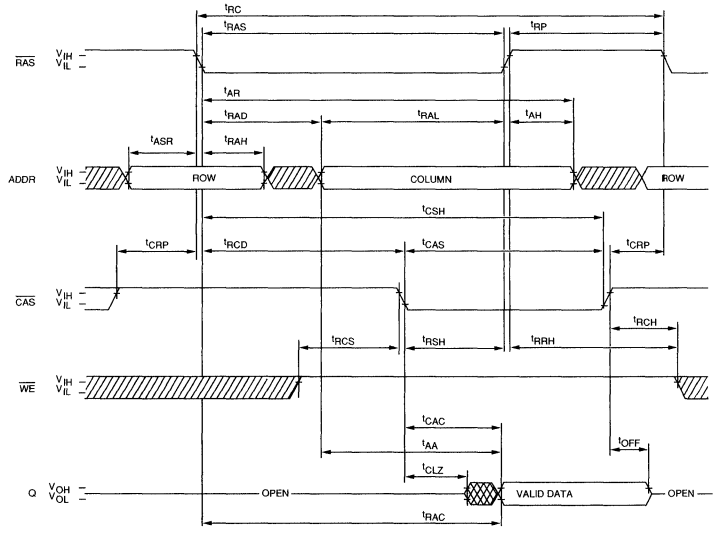
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	60		70		80		ns	21
Column address to $\overline{WE}$ delay time	tAWD	30		35		40		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	15		15		20		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	10		10		10		ns	24
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	10		10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	tWTS	10		10		10		ns	24
Write inactive time	tWI	10		10		10		ns	
Last WRITE to column address delay time	tLWAD	15	25	20	30	20	35	ns	
Last WRITE to column address hold time	tAHLW	55		65		75		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	10		10		10		ns	
Output data hold time from column address	tAOH	5		5		5		ns	
Output data enable from WRITE	tOW	20		20		20		ns	
Access time from last WRITE	tALW	55		65		75		ns	
Column address hold time referenced to RAS HIGH	tAH	5		5		10		ns	
CAS pulse width in STATIC-COLUMN mode	tCSC	tCAS		tCAS		tCAS		ns	
Output data hold from WRITE	tWOH	0		0		0		ns	

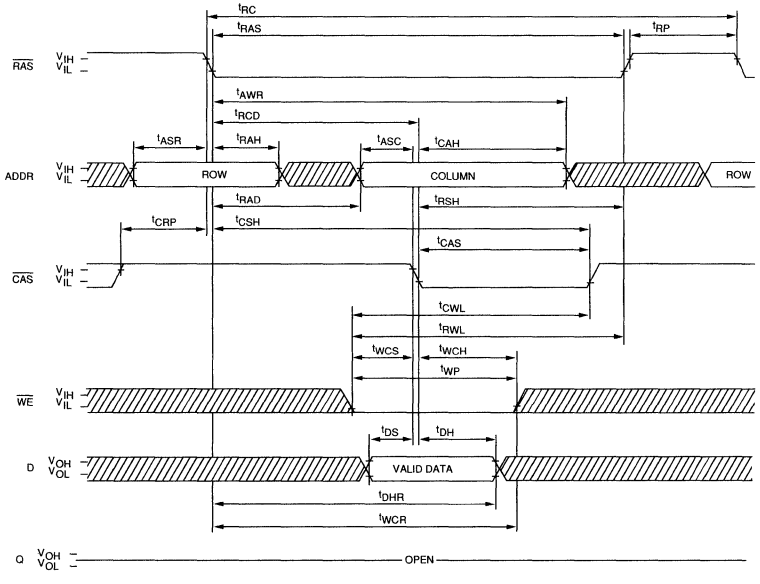
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ${}^tT$ = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that ${}^tRCD < {}^tRCD$ (MAX). If ${}^tRCD$ is greater than the maximum recommended value shown in this table, ${}^tRAC$ will increase by the amount that ${}^tRCD$ exceeds the value shown.
15. Assumes that ${}^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ${}^tCPN$.
17. Operation within the ${}^tRCD$ (MAX) limit ensures that ${}^tRAC$ (MAX) can be met. ${}^tRCD$ (MAX) is specified as a reference point only; if ${}^tRCD$ is greater than the specified ${}^tRCD$ (MAX) limit, then access time is controlled exclusively by ${}^tCAC$.
18. Operation within the ${}^tRAD$ (MAX) limit ensures that ${}^tRCD$ (MAX) can be met. ${}^tRAD$ (MAX) is specified as a reference point only; if ${}^tRAD$ is greater than the specified ${}^tRAD$ (MAX) limit, then access time is controlled exclusively by ${}^tAA$.
19. Either ${}^tRCH$ or ${}^tRRH$ must be satisfied for a READ cycle.
20. ${}^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ${}^tWCS$, ${}^tRWD$, ${}^tAWD$ and ${}^tCWD$ are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ${}^tWCS \geq {}^tWCS$ (MIN), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^tRWD \geq {}^tRWD$ (MIN), ${}^tAWD \geq {}^tAWD$ (MIN) and ${}^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the cycle is a LATE-WRITE and the state of data out is indeterminate. (at access time and until $\overline{CAS}$ goes back to V_{IH})
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. ${}^tWTS$ and ${}^tWTH$ are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ${}^tWRP$ and ${}^tWRH$ in the CBR refresh cycle.

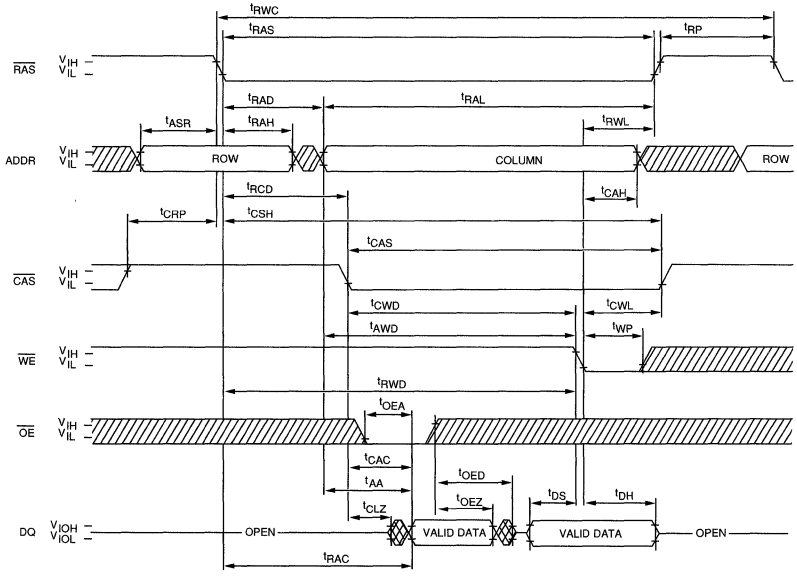
READ CYCLE



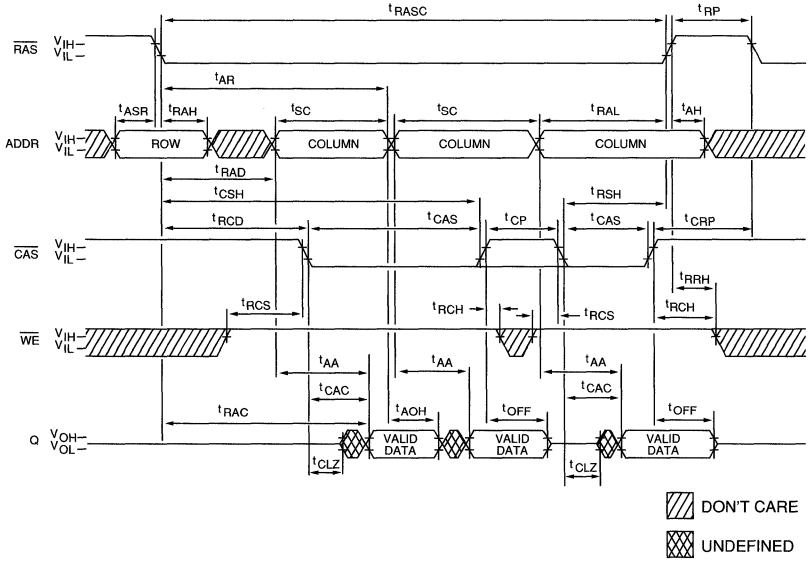
EARLY-WRITE CYCLE



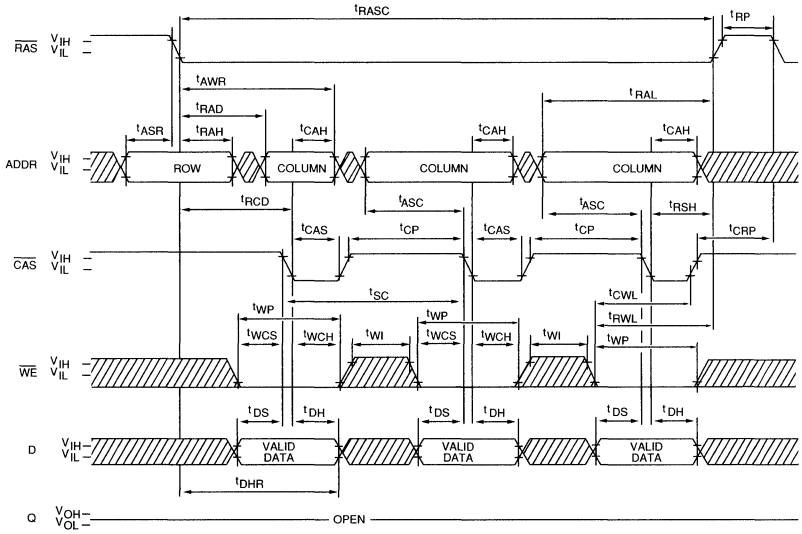
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



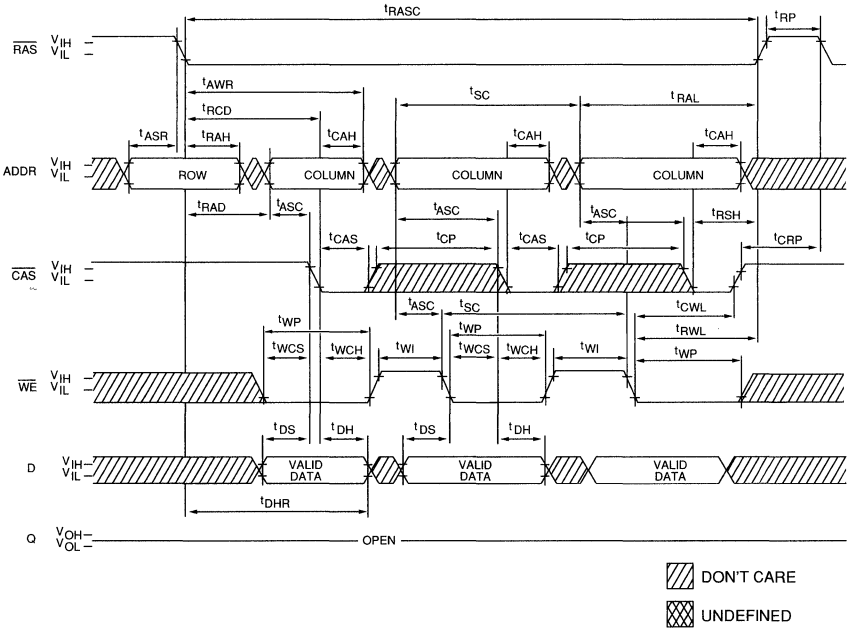
STATIC-COLUMN READ CYCLE



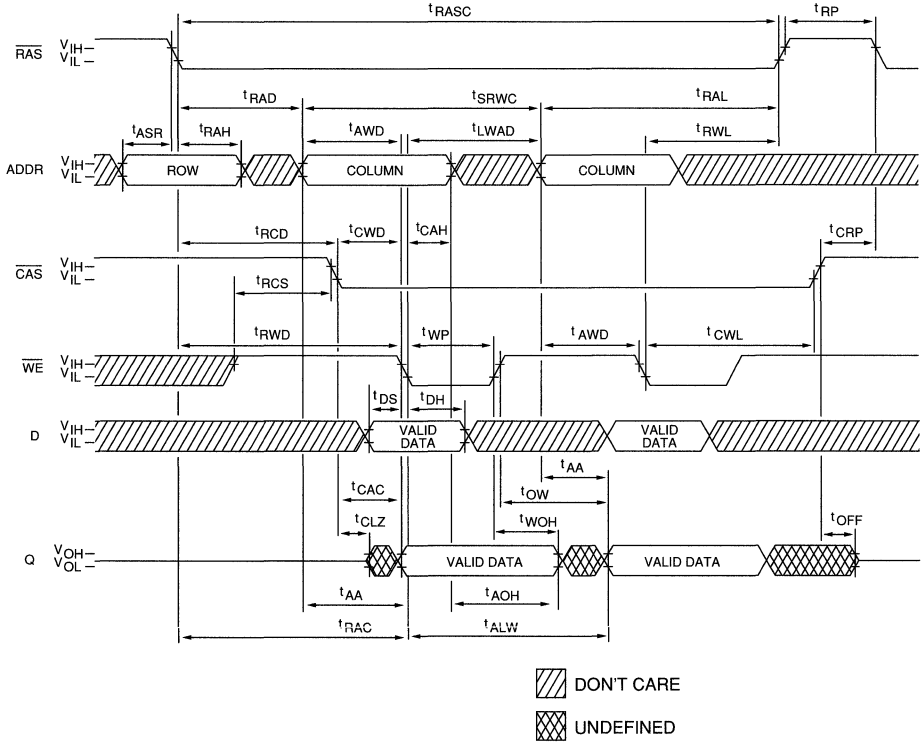
STATIC-COLUMN EARLY-WRITE CYCLE
($\overline{CAS}$ controlled)



STATIC-COLUMN EARLY-WRITE CYCLE
($\overline{WE}$ controlled)

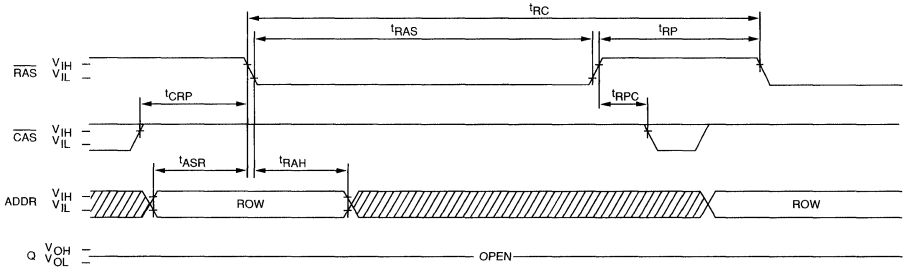


STATIC-COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



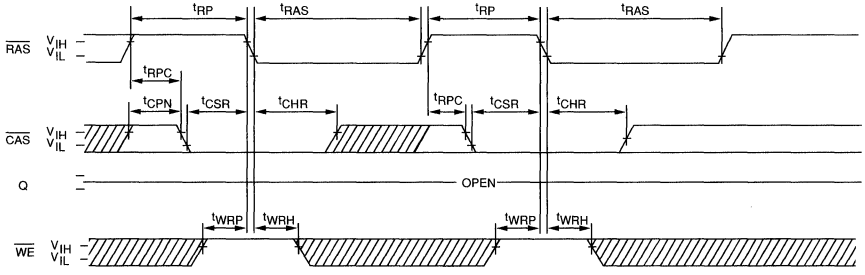
$\overline{RAS}$-ONLY REFRESH CYCLE

(ADDR = A_0 - A_9; A_{10} and $\overline{WE}$ = DON'T CARE)



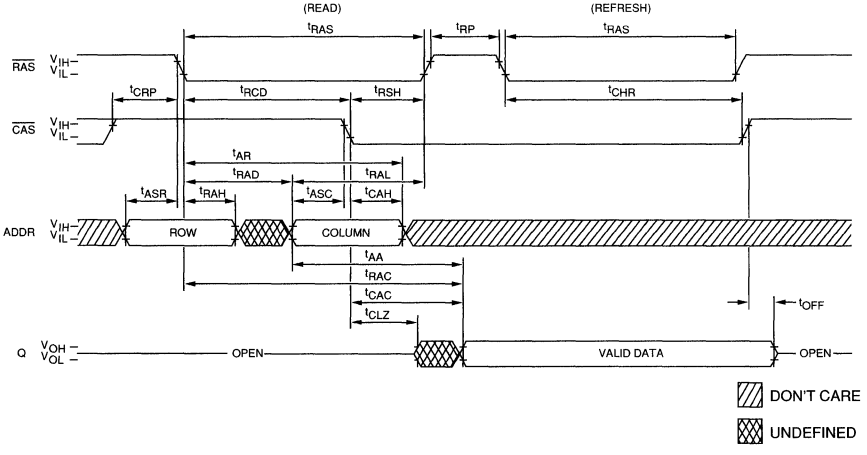
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_{10} = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH) [23]



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a don't care. The 4 Meg, on the other hand, specifies the CBR REFRESH mode to be a $\overline{W}$CBR, which is CBR with the $\overline{WE}$ pin held at a logical HIGH level.

The reason for $\overline{W}$CBR instead of CBR on the 4 Meg is that a CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode ($\overline{W}$CBR). In contrast, the 1 Meg test mode is entered by applying a HIGH signal to the test pin (pin 4 on DIP, pin 5 on SOJ and pin 8 on ZIP). This HIGH signal is usually a "supervoltage" (V in ≥ 7.5V) so normal TTL or CMOS HIGH levels will not cause the part to enter the test mode.

POWER-UP

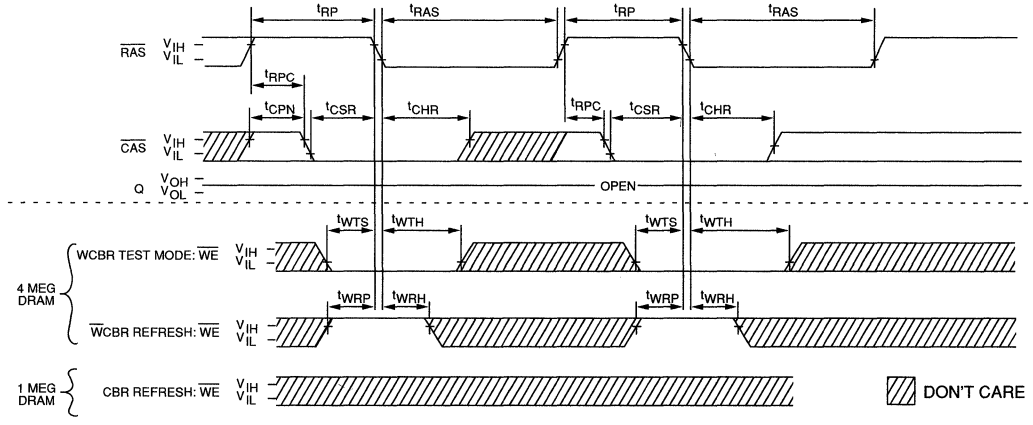
The 4 Meg $\overline{W}$CBR constraint may also introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any 8 $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that 8 $\overline{RAS}$-ONLY or $\overline{W}$CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a $\overline{W}$CBR REFRESH cycle.

SUMMARY

1. The optional 1 Meg test pin is the A10 pin on the 4 Meg .
2. For optional test mode, the 1 Meg requires a valid HIGH on the test pin while the 4 Meg requires a CBR cycle with $\overline{WE}$ LOW.
3. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH ($\overline{W}$CBR).
4. The 8 $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or $\overline{W}$CBR REFRESH cycles.

SPECIAL FEATURE

A memory system currently using 1 Meg DRAMs with $\overline{WE}$ as a don't care during CBR REFRESH does not allow for direct upgrading to 4 Meg DRAMs. Micron, realizing some companies will have this situation, provides a special feature on its 4 Meg DRAM, that requires "supervoltage" to access the 4 Meg JEDEC WCBR test function. This allows the Micron 4 Meg DRAM to be refreshed in the same manner as any 1 MEG DRAM. Note that the eight power-up cycles should only be refresh cycles in order to guarantee that any 4 Meg DRAM, including Micron's, does not inadvertently power-up in the test mode.



COMPARISON OF 4 MEG TEST MODE AND $\overline{W}$CBR TO 1 MEG CBR

DRAM

16 MEG x 1 DRAM

FAST PAGE MODE: MT4C10016
STATIC COLUMN: MT4C10017

FEATURES

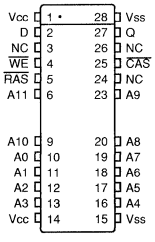
- Industry standard x1 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single power supply: +5V±10% or +3.3V±10%
- Low power, 3mW standby; 250mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), and HIDDEN
- 4096-cycle refresh distributed across 64ms

OPTIONS

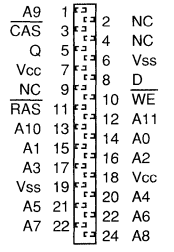
	MARKING
• Timing	
50ns access	-5
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Plastic ZIP (475mil)	Z
Plastic SOJ (400mil)	DJ
Plastic TSOP (*)	TG
• Refresh Period	
4096 cycles @ 64ms	None
• Operating Temperature, TA	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
• Power Supply	
+5V±10%	None
+3.3V±10%	V

PIN ASSIGNMENT (Top View)

24-Pin SOJ (E-7)



24-Pin ZIP



*Consult factory on availablity of TSOP packages

GENERAL DESCRIPTION

The MT4C10016/7 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 24 address bits, which are entered 12 bits (A0-A11) at a time. $\overline{RAS}$ is used to latch the first 12 bits and $\overline{CAS}$ the latter 12 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), or HIDDEN REFRESH) so that all 2048/4096 combinations of $\overline{RAS}$ addresses (A0-A10/A11) are executed at least every 32ms/64ms, regardless of sequence. The CBR refresh cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

The MT4C10016/7 are available with either 2048 cycles or 4096 cycles of refreshing. If CBR refresh is used, the 2048-cycle version will work in either a 2048 or a 4096 cycle application.

DRAM

64K x 4 DRAM

PAGE MODE

FEATURES

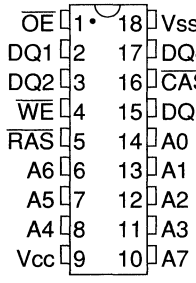
- Industry standard pinout, timing and functions
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby; 150mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, and HIDDEN
- 256-cycle refresh in 4ms
- Optional PAGE MODE access cycle

OPTIONS

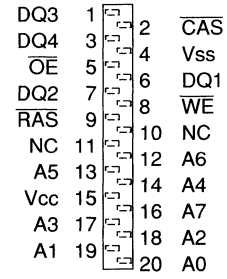
	MARKING
• Timing	
100ns access	-10
120ns access	-12
150ns access	-15
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
PLCC	EJ

PIN ASSIGNMENT (Top View)

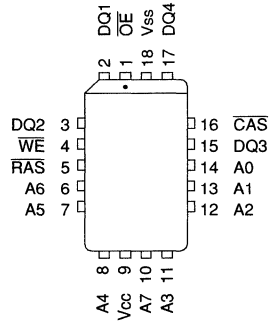
18-Pin DIP
(A-2, B-2)



20-Pin ZIP
(C-2)



18-Pin PLCC
(D-1)

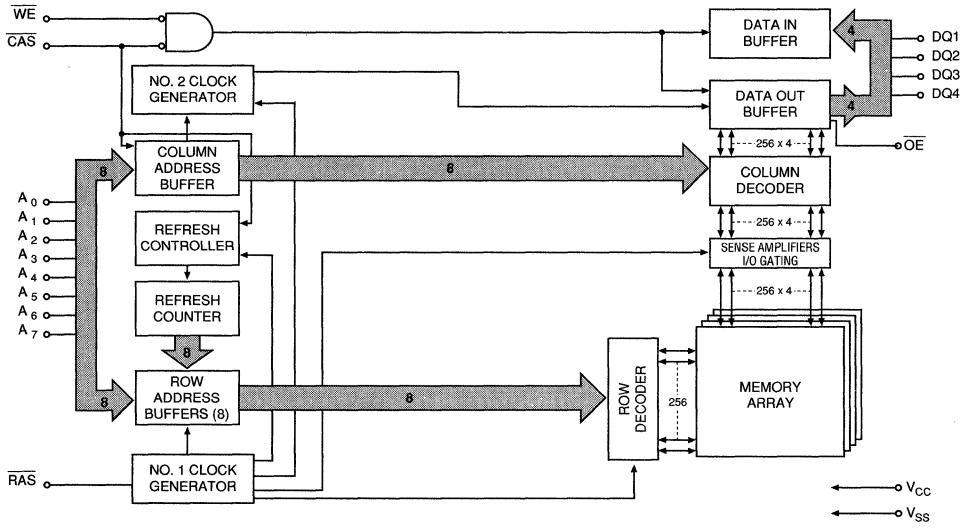


GENERAL DESCRIPTION

The MT4067 is a randomly accessed solid-state memory containing 262,144 bits organized in a x4 configuration. The 16 address bits are entered 8 bits at a time using RAS to latch the first 8 bits and CAS the latter 8 bits. If the WE pin goes LOW prior to CAS going LOW, the output pin remains open until the next CAS cycle. If WE goes LOW after data reaches the output pin, the output pin is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-MODIFY-WRITE cycle. Data-in (D) is latched when WE strobes LOW.

By holding RAS LOW, CAS may be toggled to execute several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the RAS address defined page boundary. Returning RAS HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing a RAS (refresh) cycle so that all 256 combinations of RAS addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



TRUTH TABLE

Function	RAS	CAS	WE	OE	Addresses tR	Addresses tC	
Standby	H	X	X	X	X	X	High Impedance
READ	L	L	H	L	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	X	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE-MODE READ	L	H→L→H	H	L	ROW	COL	Valid Data Out, Valid Data Out
PAGE-MODE WRITE	L	H→L→H	L	H	ROW	COL	Valid Data In, Valid Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	L→H	ROW	COL	Valid Data Out, Valid Data In
RAS-ONLY REFRESH	L	H	X	H	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	X	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	X	H	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2 ,3, 4, 6) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0V	I_I	-10	10	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	5	5	5	mA	
OPERATING CURRENT: Random READ/WRITE ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC2}	55	55	45	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC3}	55	55	45	mA	2
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC4}	40	40	35	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC5}	55	55	45	mA	2, 22

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		8	pF	18
Input/Output Capacitance: DQ	C_{IO}		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

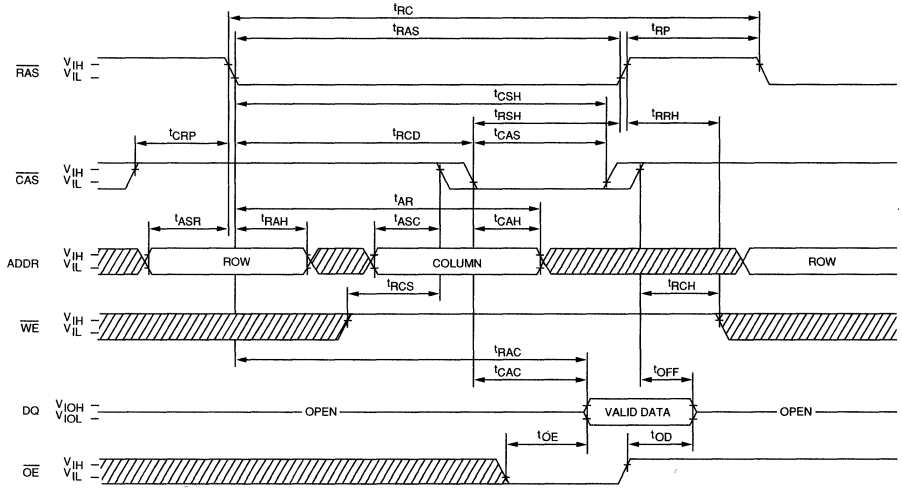
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	tRWC	250		295		345		ns	
PAGE-MODE cycle time	tPC	90		100		120		ns	6, 7
Access time from $\overline{RAS}$	tRAC		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	tCAC		50		60		75	ns	7, 9
Output Enable	tOE		25		30		40	ns	
$\overline{RAS}$ pulse width	tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	tRSH	50		60		75		ns	
$\overline{RAS}$ precharge time	tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	tCAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	tCPN	25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE MODE)	tCP	30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	tCRP	15		20		20		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	15		15		15		ns	
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	70		80		100		ns	
READ command setup time	tRCS	0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	30	0	30	0	35	ns	12
Output Disable	tOD		30		30		35	ns	
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	16
WRITE command hold time	tWCH	35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	tWCR	85		100		120		ns	
WRITE command pulse width	tWP	35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	tRWL	35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	tCWL	35		40		45		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	tDHR	60		65		70		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	tCWD	70		90		110		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	tRWD	120		150		185		ns	16
Transition time (rise or fall)	tT	3	100	3	100	3	100	ns	5, 17
Refresh period (256 cycles)	tREF		4		4		4	ms	22
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	20		25		30		ns	21
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	tCSR	15		20		20		ns	21
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	21

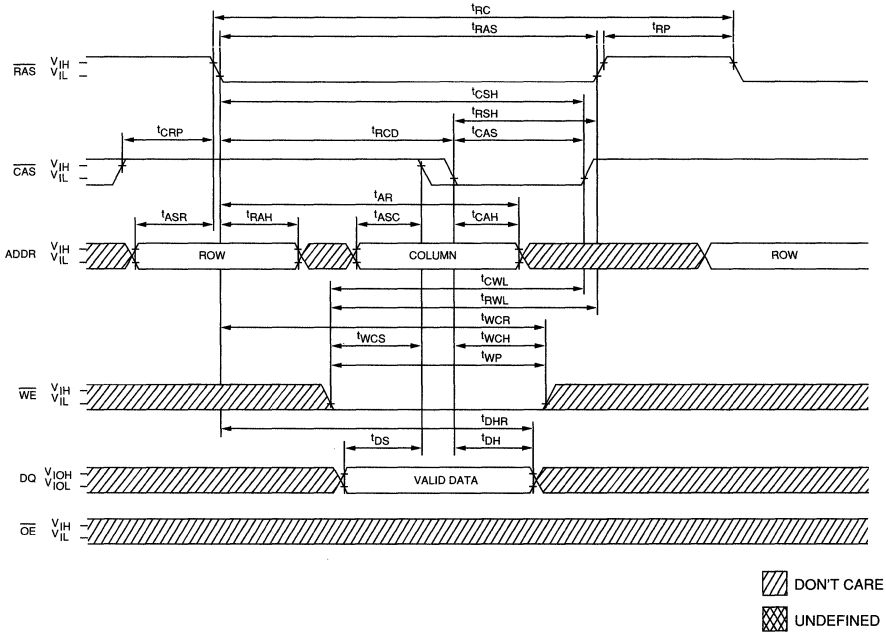
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH})
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. This parameter is sampled. Capacitance is calculated from the equation $C = I\,^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, (V_{IH}) Q goes open. If $\overline{OE}$ is tied permanently LOW, a READ-MODIFY-WRITE operation is not possible.
21. On-chip refresh and address counters are enabled.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.

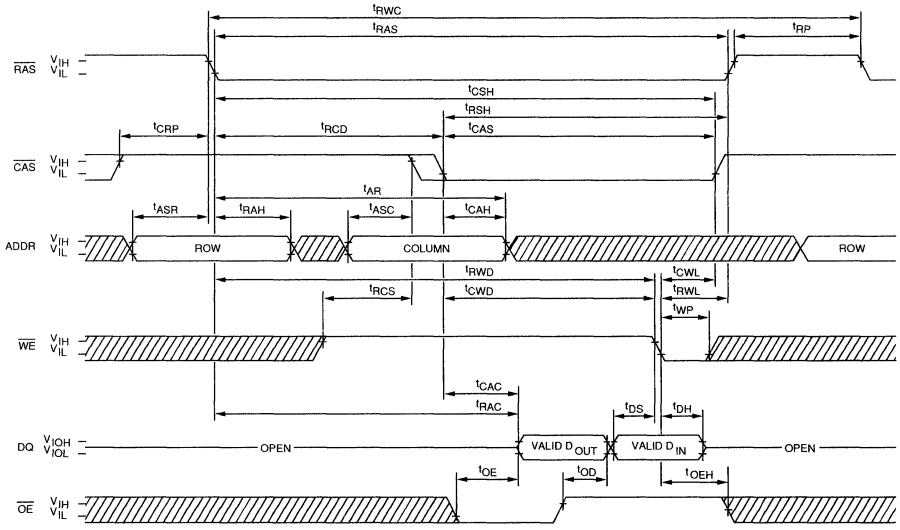
READ CYCLE



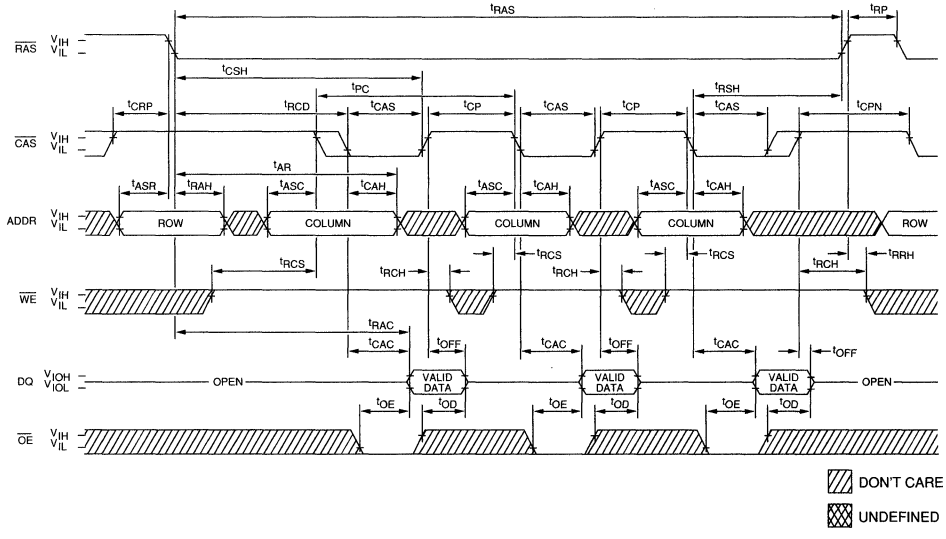
EARLY-WRITE CYCLE



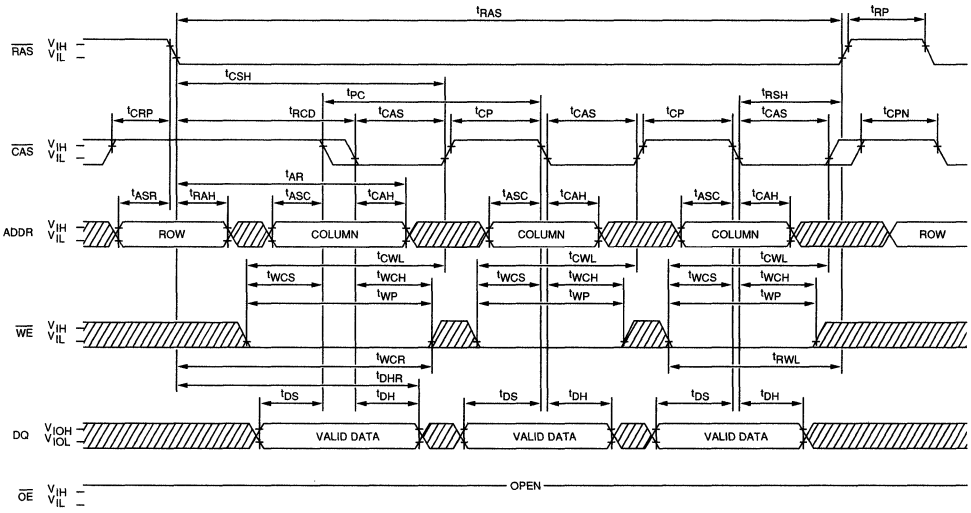
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



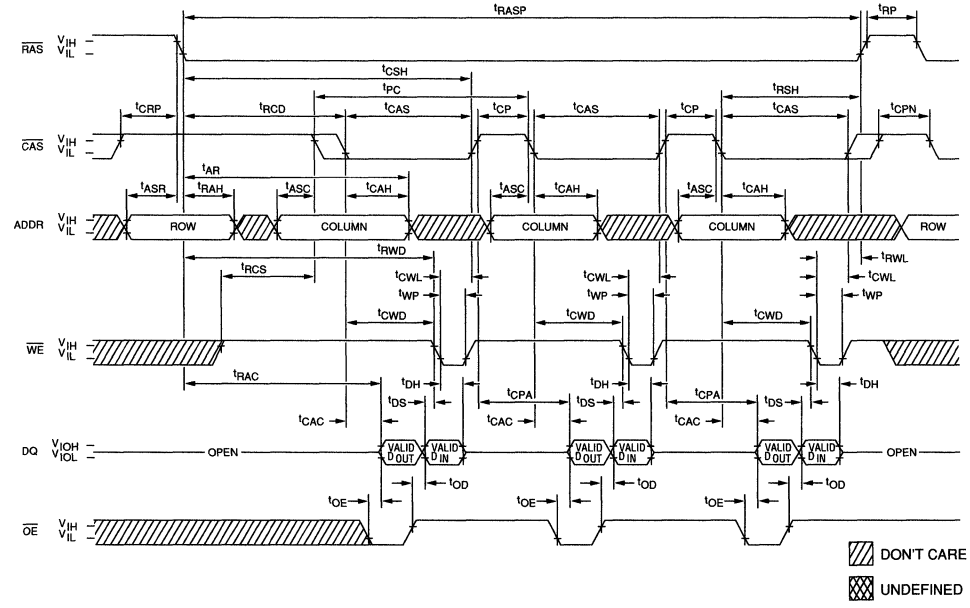
PAGE-MODE READ CYCLE



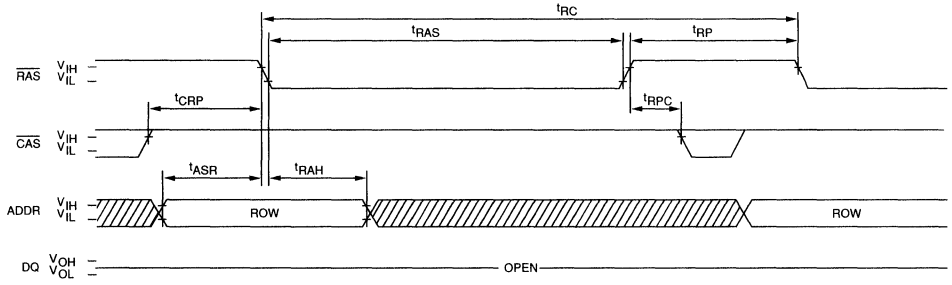
PAGE-MODE EARLY-WRITE CYCLE



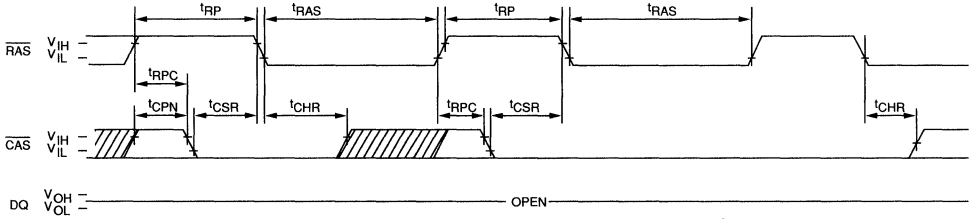
PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



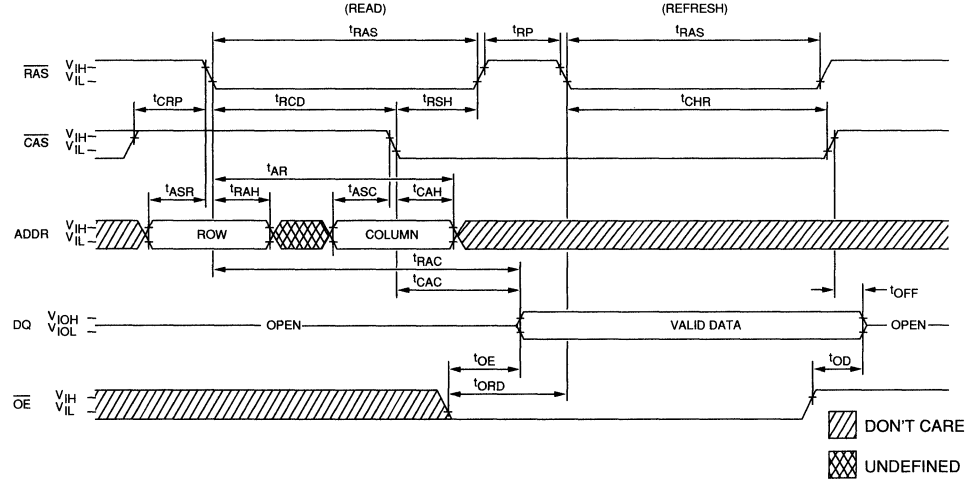
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A_0 - A_7; $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A_0 - A_7, $\overline{WE}$, $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH) [22]



DRAM

256K x 4 DRAM

FAST PAGE MODE

FEATURES

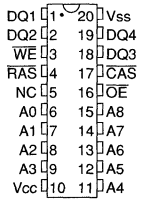
- Industry standard x4 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512-cycle refresh in 8ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional FAST PAGE MODE access cycle

OPTIONS

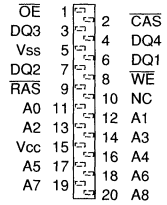
	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Plastic DIP (300mil)	None
Ceramic DIP (300mil)	C
Plastic ZIP (350mil)	Z
Plastic SOJ (300mil)	DJ
Plastic TSOP (*)	VG
• Operating Temperature, TA	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

PIN ASSIGNMENT (Top View)

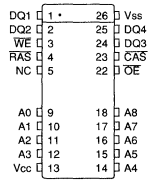
20-Pin DIP (A-5, B-4)



20-Pin ZIP (C-2)



20-Pin SOJ (E-1)



*Consult factory on availability of TSOP packages

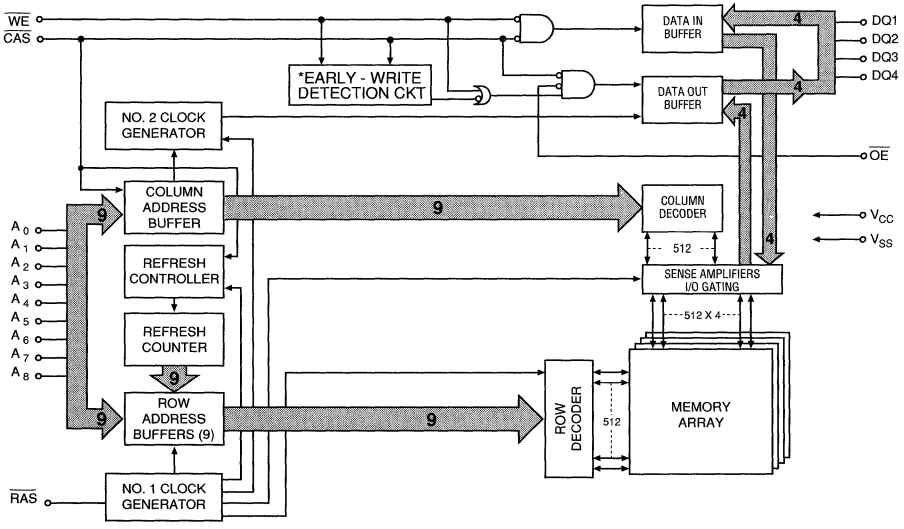
GENERAL DESCRIPTION

The MT4C4256 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh will increment the refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection CKT output is a HIGH (EARLY WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address ^tR	Address ^tC	$\overline{OE}$	DATA IN / OUT DQ1-4 (IO)
Standby		H	X	X	X	X	X	High-Z
READ		L	L	H	ROW	COL	L	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	X	Valid Data In
READ-WRITE		L	L	H→L	ROW	COL	L→H	Valid Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	L	Valid Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	L	Valid Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	X	Valid Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	X	Valid Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	L→H	Valid Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	L→H	Valid Data Out, Data In
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	X	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	L	Valid Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	X	Valid Data In
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-2.0	0.8	V	1, 28
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT: (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	80	70	60	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	60	50	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	80	70	60	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	80	70	60	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	185		205		245		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		45		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	95		100		115		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Output Enable	t_{OE}		20		20		25	ns	
Access time from column address	t_{AA}		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

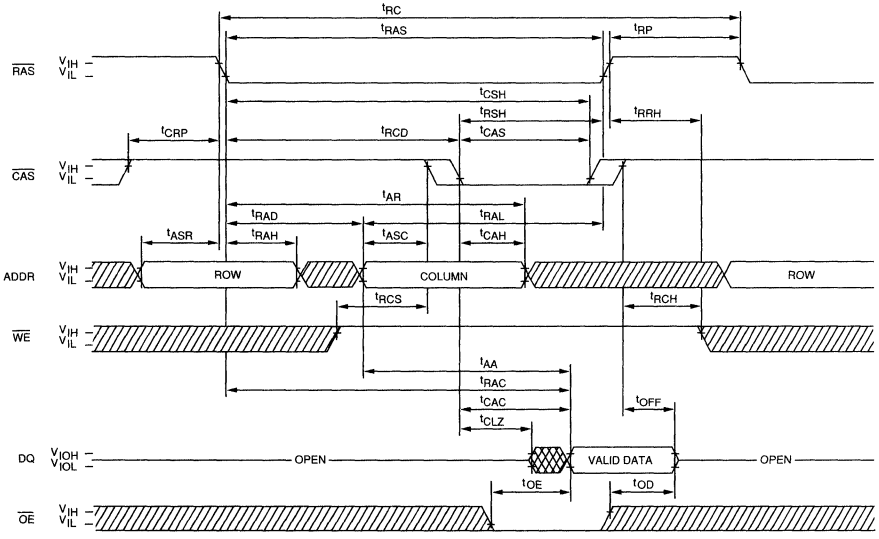
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^{t}OFF	0	20	0	20	0	20	ns	20, 27
Output Disable	^{t}OD		20		20		20	ns	27
$\overline{WE}$ command setup time	^{t}WCS	0		0		0		ns	21
Write command hold time	^{t}WCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	55		60		75		ns	
Write command pulse width	^{t}WP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^{t}RWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^{t}CWL	20		20		25		ns	
Data-in setup time	^{t}DS	0		0		0		ns	22
Data-in hold time	^{t}DH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	100		110		130		ns	21
Column address to $\overline{WE}$ delay time	^{t}AWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	50		55		60		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^{t}REF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CHR	15		15		15		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^{t}OEH	20		20		20		ns	26
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	24

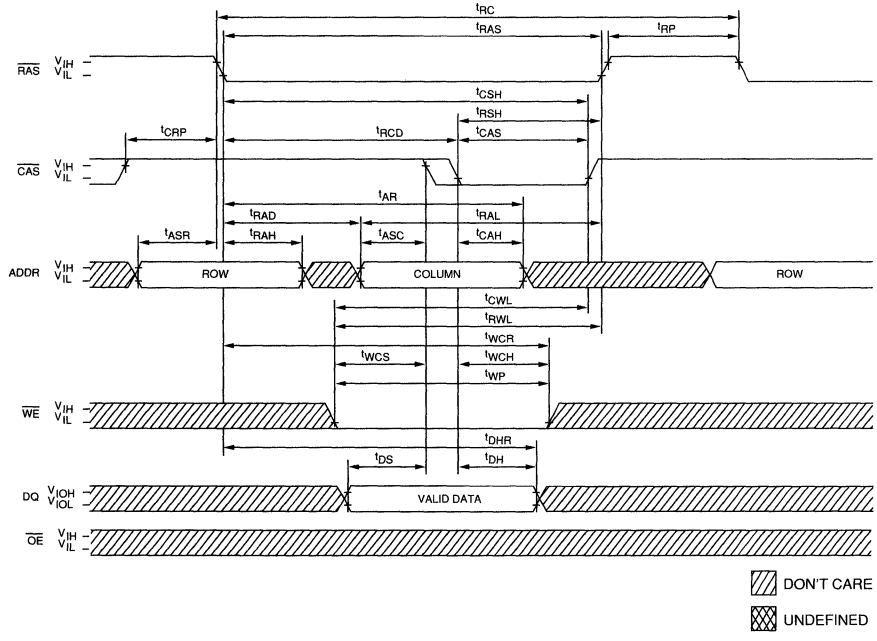
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. All other inputs at Vcc -0.2V.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
28. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

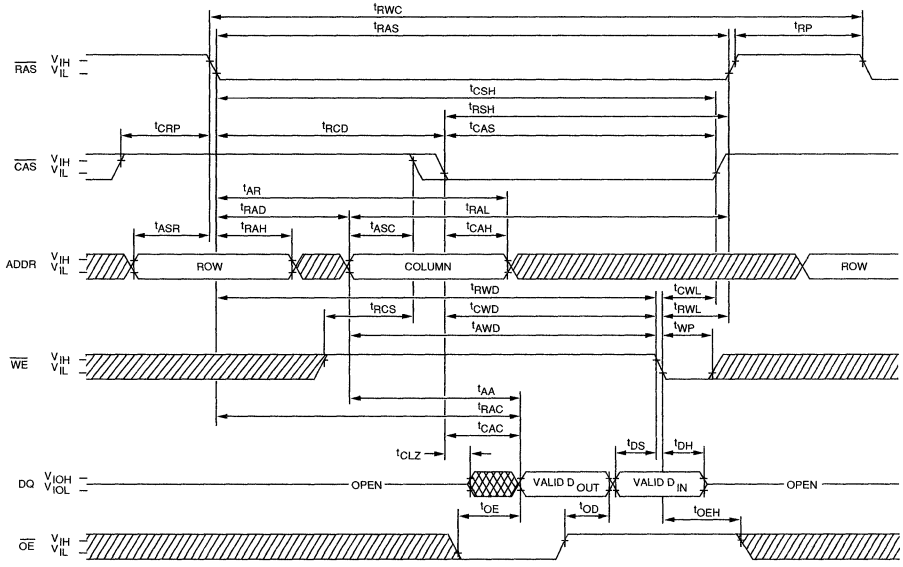
READ CYCLE



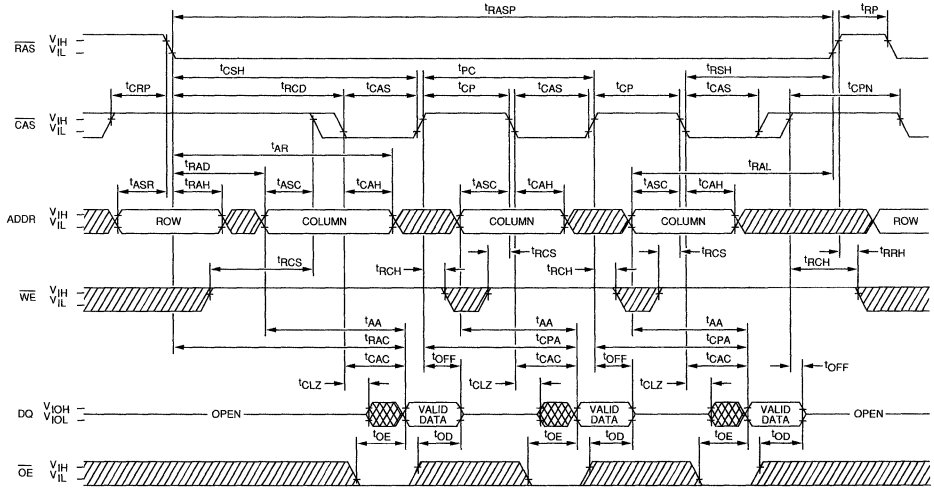
EARLY-WRITE CYCLE



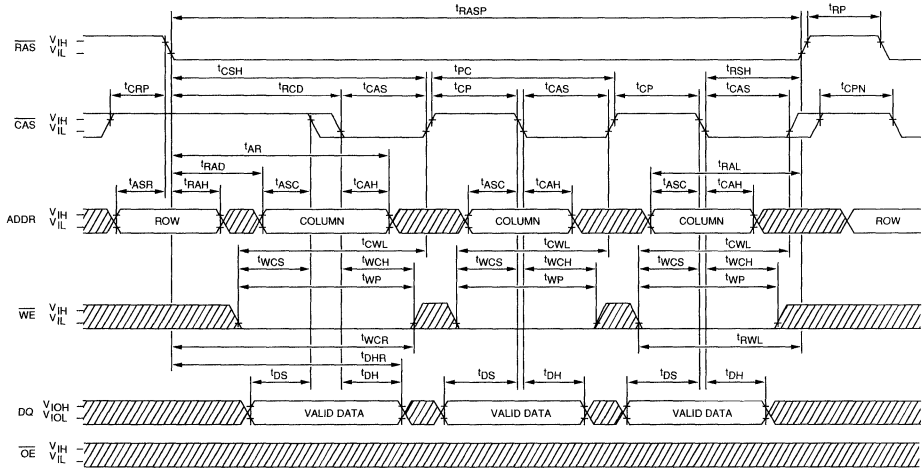
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



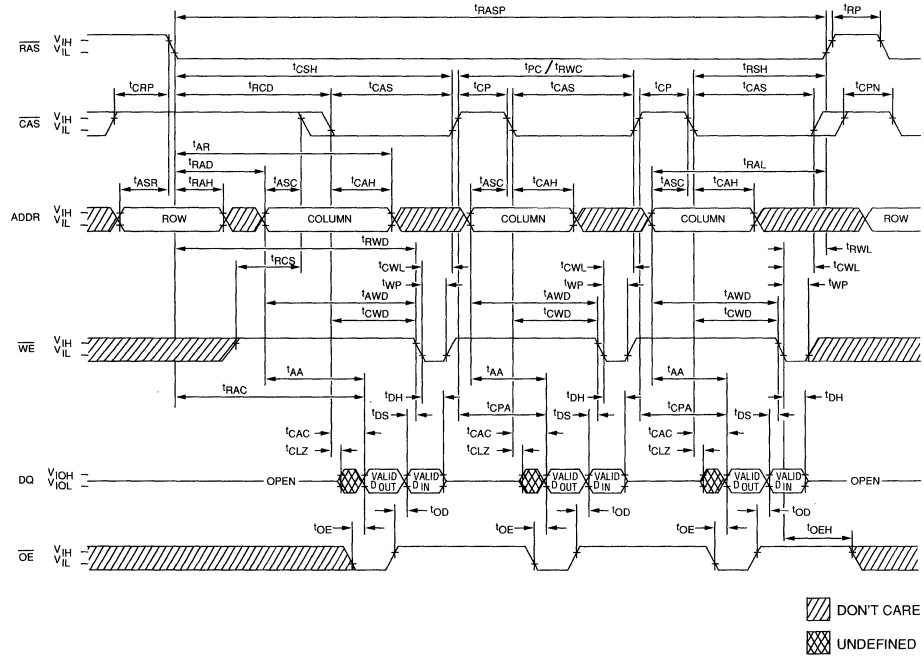
FAST-PAGE-MODE READ CYCLE



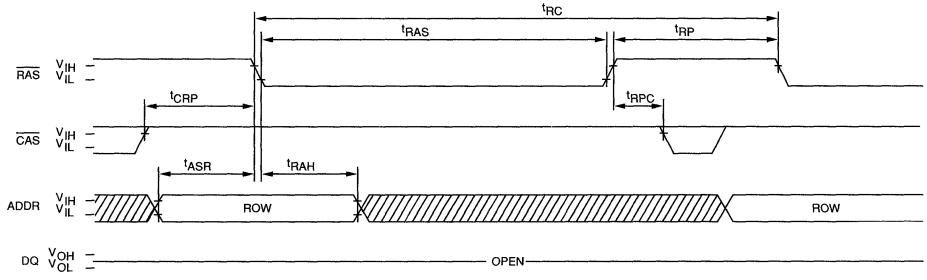
FAST-PAGE-MODE EARLY-WRITE CYCLE



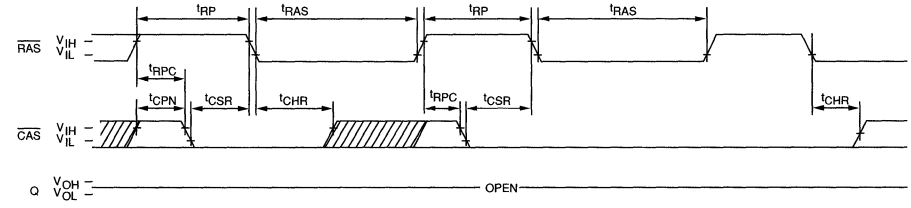
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



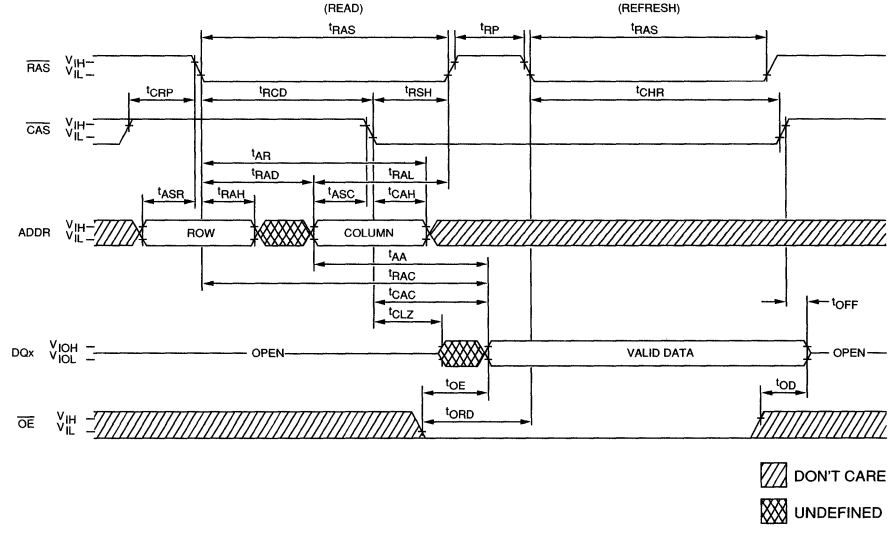
$\overline{RAS}$-ONLY REFRESH CYCLE
($ADDR = A_0 - A_8$; $\overline{WE}$ = DON'T CARE)



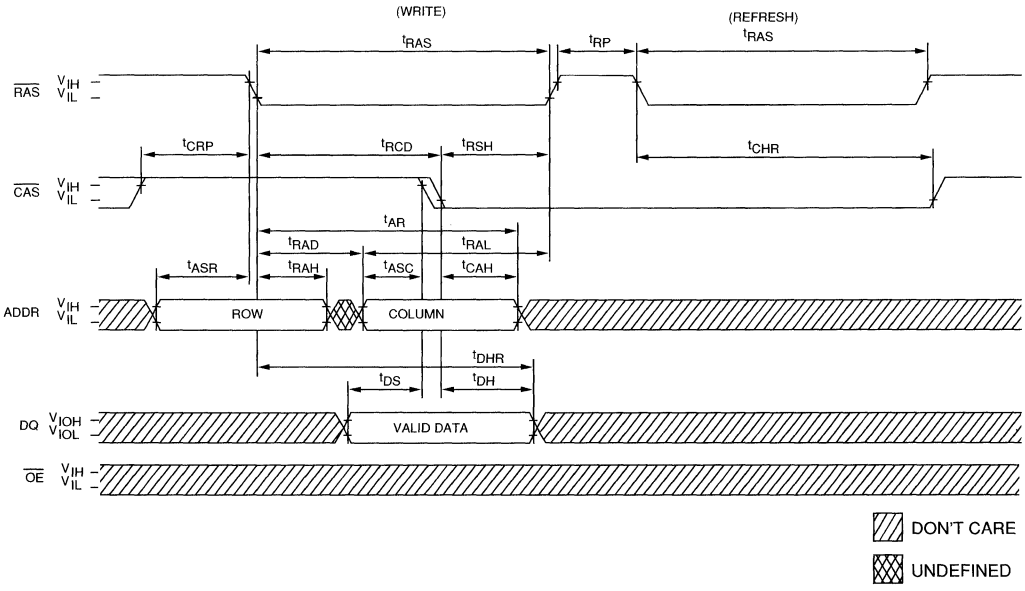
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
($A_0 - A_8$, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH, $\overline{OE}$ = LOW) [24]



HIDDEN REFRESH CYCLE
($\overline{WE}$ = LOW)



DRAM

256K x 4 DRAM

STATIC COLUMN

FEATURES

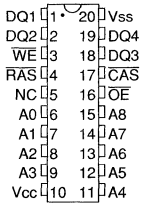
- Industry standard x4 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512-cycle refresh in 8ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional STATIC COLUMN access cycle

OPTIONS

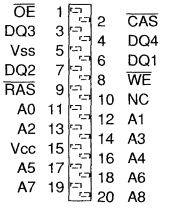
	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Plastic DIP (300mil)	None
Ceramic DIP (300mil)	C
Plastic ZIP (350mil)	Z
Plastic SOJ (300mil)	DJ
Plastic TSOP (*)	VG
• Operating Temperature, T_A	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

PIN ASSIGNMENT (Top View)

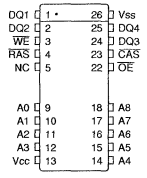
20-Pin DIP
(A-5, B-4)



20-Pin ZIP
(C-2)



20-Pin SOJ
(E-1)



*Consult factory on availability of TSOP packages

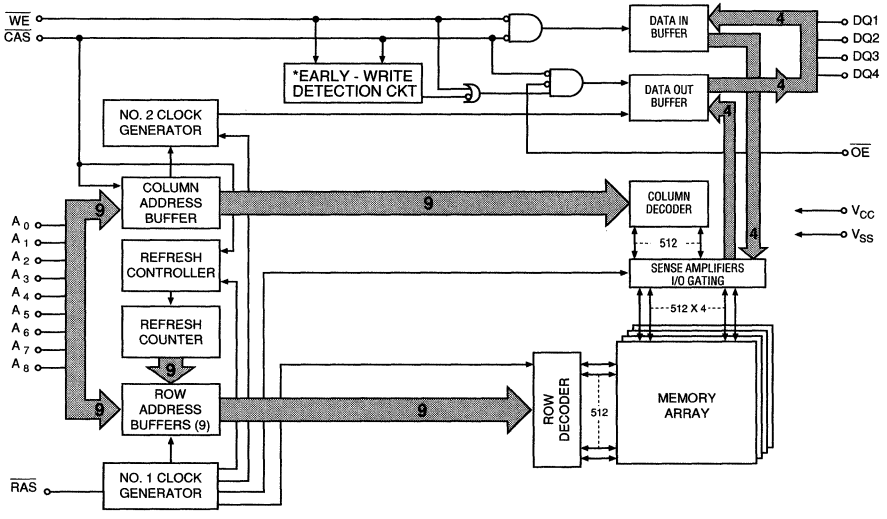
GENERAL DESCRIPTION

The MT4C4258 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh will increment the refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection CKT output is a HIGH (EARLY WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address ^tR	Address ^tC	$\overline{OE}$	DATA IN / OUT DQ1-4 (IO)
Standby		H	X	X	X	X	X	High-Z
READ		L	L	H	ROW	COL	L	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	X	Valid Data In
READ-WRITE		L	L	H→L	ROW	COL	L→H	Valid Data Out, Data In
STATIC COLUMN READ	1st Cycle	L	L	H	ROW	COL	L	Valid Data Out
	2nd Cycle	L	L	H	n/a	COL	L	Valid Data Out
STATIC COLUMN EARLY-WRITE	1st Cycle	L	L	L	ROW	COL	X	Valid Data In
	2nd Cycle	L	L	H→L	n/a	COL	X	Valid Data In
STATIC COLUMN READ-WRITE	1st Cycle	L	L	H→L	ROW	COL	L→H	Valid Data Out, Data In
	2nd Cycle	L	L	H→L	n/a	COL	L→H	Valid Data Out, Data In
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	X	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	L	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	X	Valid Data In
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-2.0	0.8	V	1, 28
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	80	70	60	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	60	50	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	80	70	60	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	80	70	60	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	185		205		245		ns	
STATIC-COLUMN READ or WRITE cycle time	^tSC	40		45		55		ns	
STATIC-COLUMN READ-WRITE cycle time	^tSRMC	100		110		135		ns	
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	15
Output Enable	^tOE		20		20		25	ns	
Access time from column address	^tAA		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		50	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	20	50	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

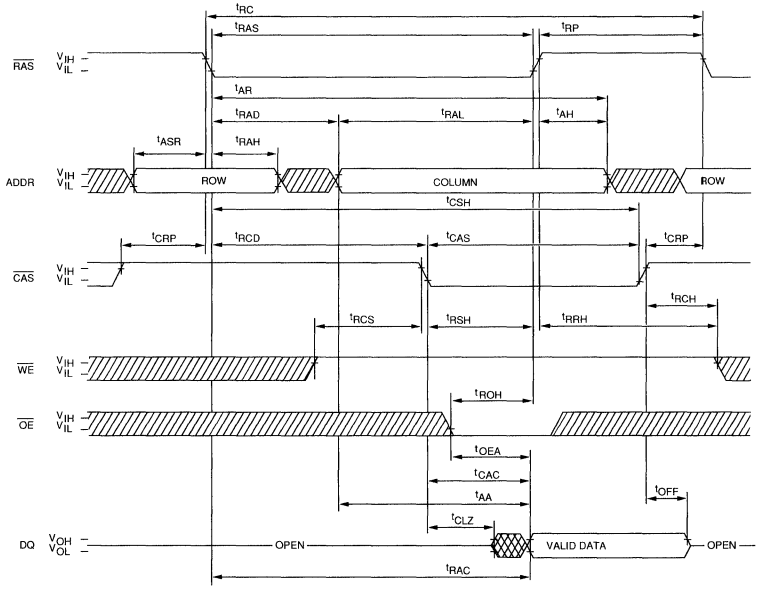
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 27
Output Disable	^tOD		20		20		20	ns	27
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	100		110		130		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		60		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		20		ns	26
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	24
Write inactive time	^tWI	10		10		10		ns	
Last WRITE to column address delay time	^tLWAD	20	30	20	35	25	45	ns	
Last WRITE to column address hold time	^tAHLW	65		75		95		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	10		10		10		ns	
Output data hold time from column address	^tAOH	5		5		5		ns	
Output data enable from WRITE	^tOW	^tAA		^tAA		^tAA		ns	
Access time from last WRITE	^tALW	65		75		95		ns	
Column address hold time referenced to $\overline{RAS}$ HIGH	^tAH	5		5		10		ns	
CAS pulse width in STATIC-COLUMN mode	^tCSC	^tCAS		^tCAS		^tCAS		ns	

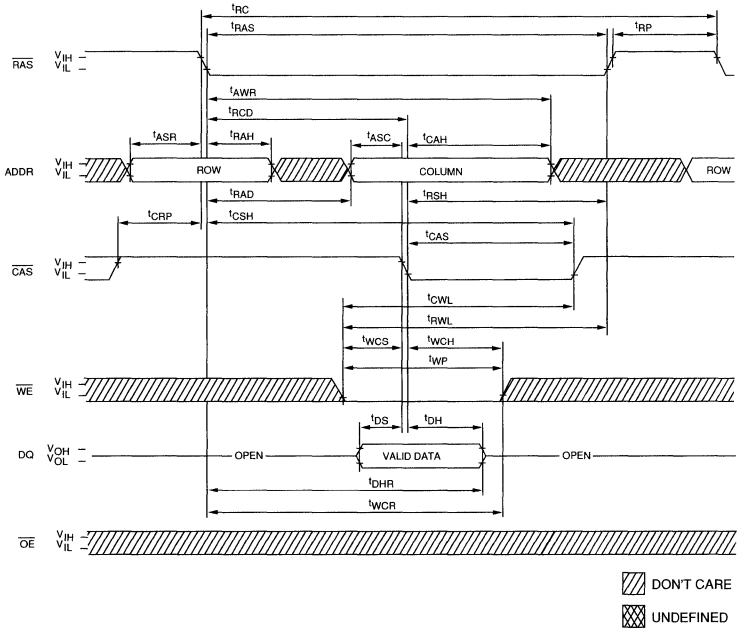
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. All other inputs at Vcc -0.2V.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
28. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

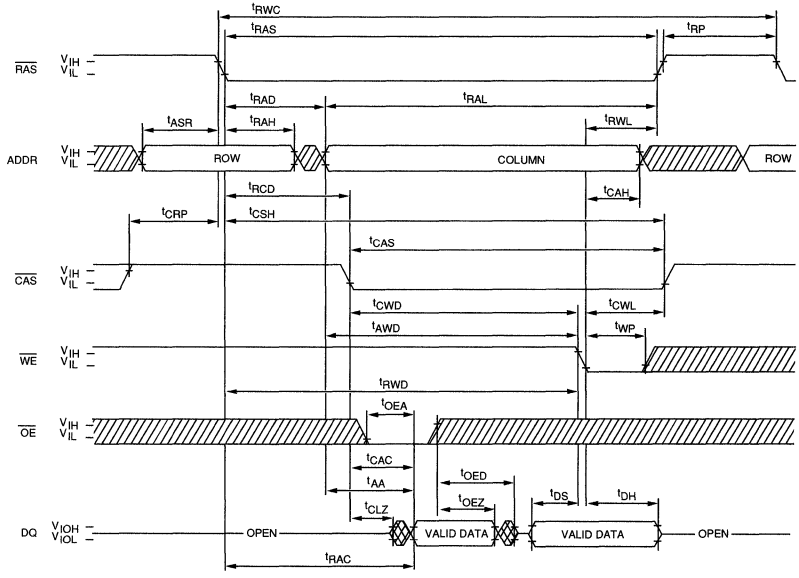
READ CYCLE



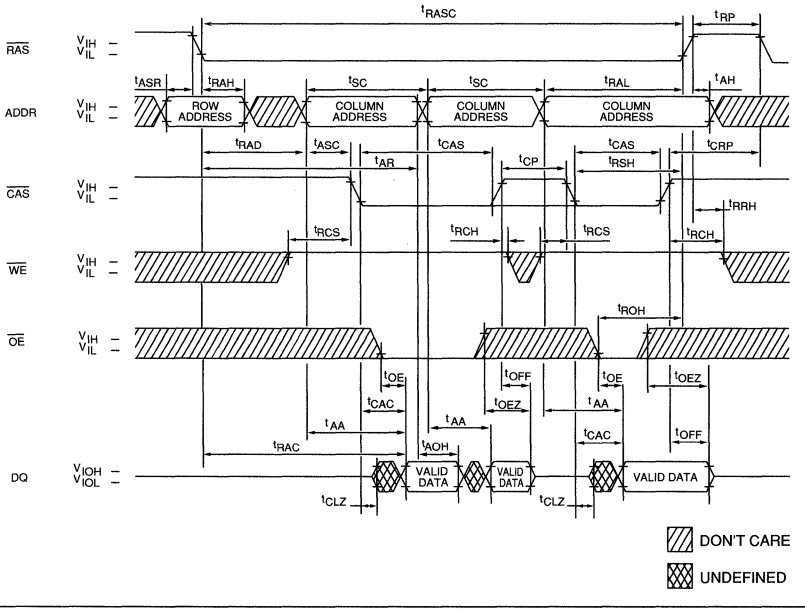
EARLY-WRITE CYCLE



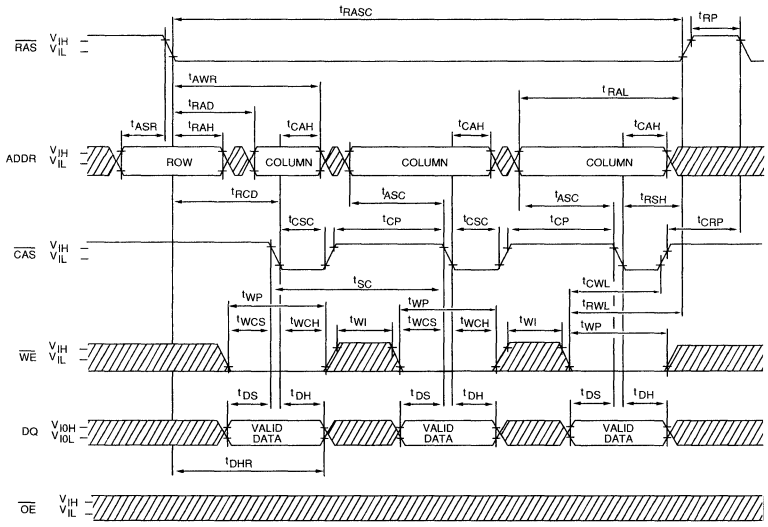
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



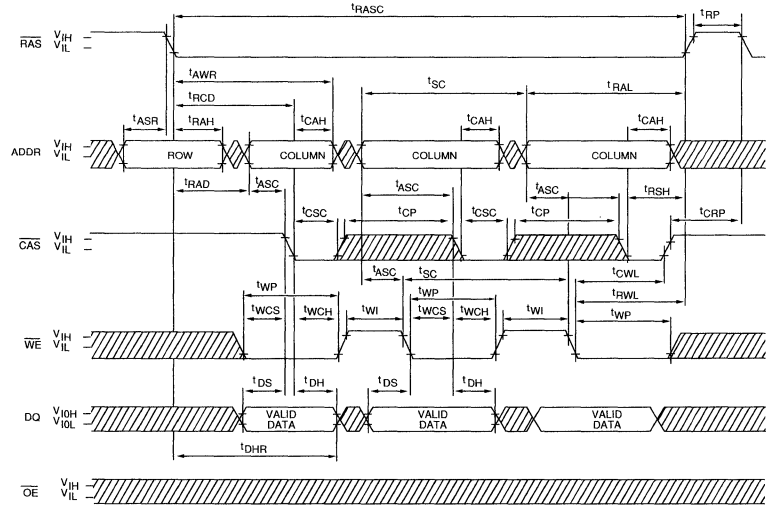
STATIC-COLUMN READ CYCLE



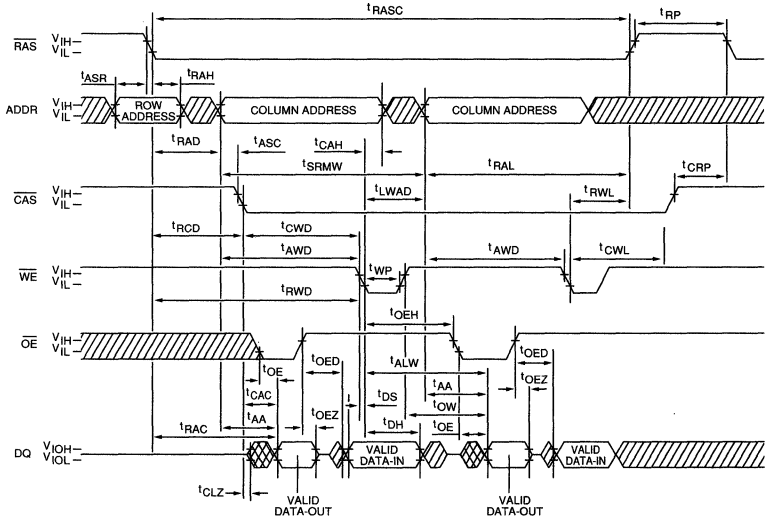
STATIC-COLUMN EARLY-WRITE CYCLE
(CAS controlled)



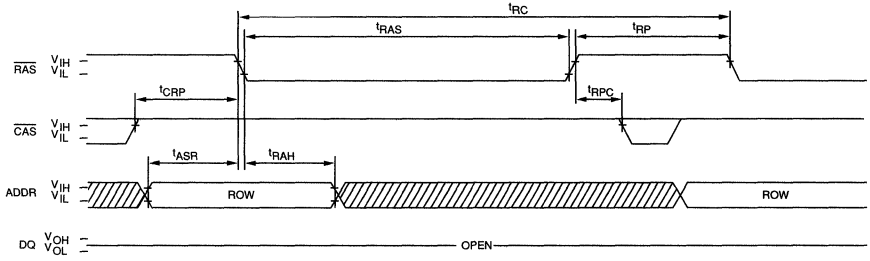
STATIC-COLUMN EARLY-WRITE CYCLE
(WE controlled)



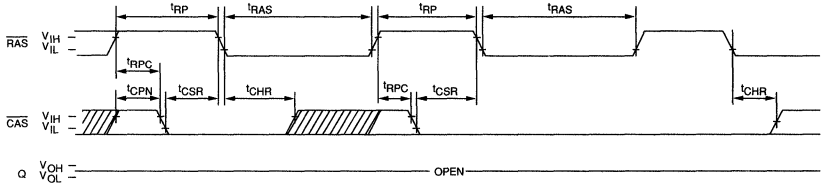
STATIC-COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



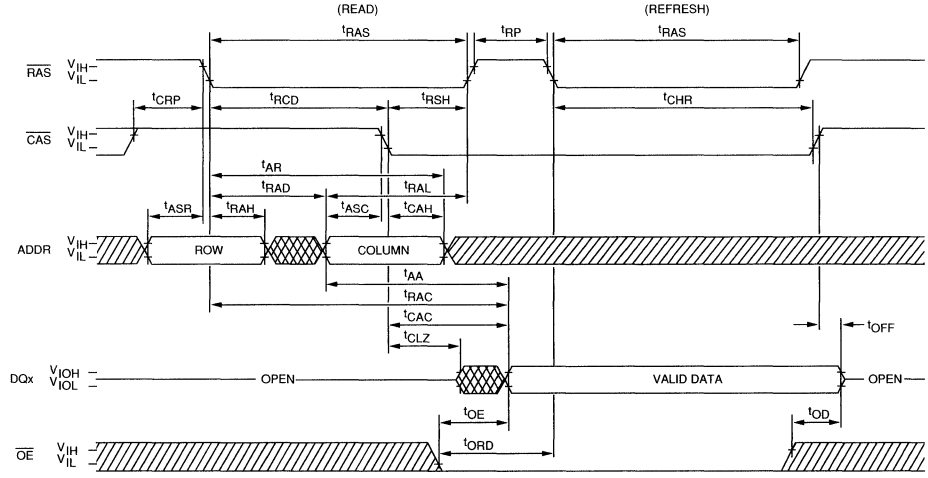
RAS-ONLY REFRESH CYCLE
(ADDR = A_0 - A_8; WE = DON'T CARE)



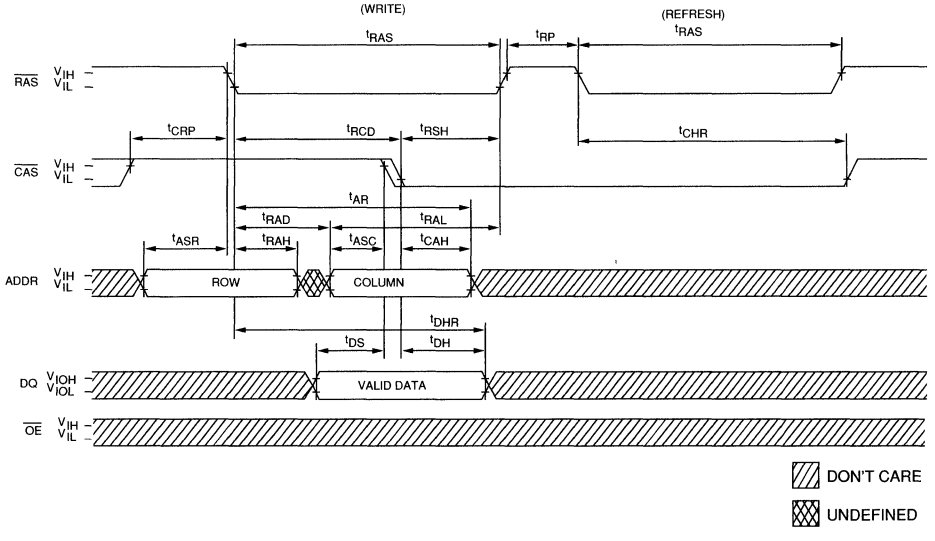
CAS-BEFORE-RAS REFRESH CYCLE
(A_0 - A_8, WE and OE = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH, $\overline{OE}$ = LOW) [24]



HIDDEN REFRESH CYCLE
($\overline{WE}$ = LOW)



DRAM

256K x 4 DRAM

QUAD CAS PARITY, FAST PAGE MODE

FEATURES

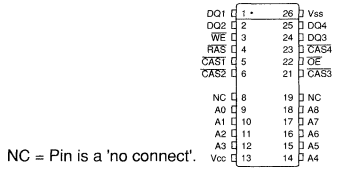
- Four independent $\overline{CAS}$ controls offer individual manipulation to each of the four data Input/Output ports (DQ1 through DQ4).
- Offers a single-chip solution to byte-level parity for 36-bit words when using 256K x 4 DRAMs for memory.
- Emulates write-per-bit, at design-in level, with simplified timing constraints.
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512-cycle refresh in 8ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional FAST PAGE MODE access cycle

OPTIONS / MARKING

• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Plastic SOJ (300mil)	DJ
• Operating Temperature, T_A	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

PIN ASSIGNMENT (Top View)

24-Pin SOJ (E-5)



NC = Pin is a 'no connect'.

GENERAL DESCRIPTION

The MT4C4259 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. This 256K x 4 DRAM is unique in that each $\overline{CAS}$ ($\overline{CAS1}$ through $\overline{CAS4}$) controls its corresponding data I/O port in conjunction with $\overline{OE}$ (eg. $\overline{CAS1}$ controls DQ1 I/O port, $\overline{CAS2}$ controls DQ2, $\overline{CAS3}$ controls DQ3 and $\overline{CAS4}$ controls DQ4).

The best way to view the Quad $\overline{CAS}$ function is to imagine the $\overline{CAS}$ inputs going into an AND gate to obtain an internally generated $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on a standard 256K x 4 DRAM device. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$) on the Quad $\overline{CAS}$ DRAM.

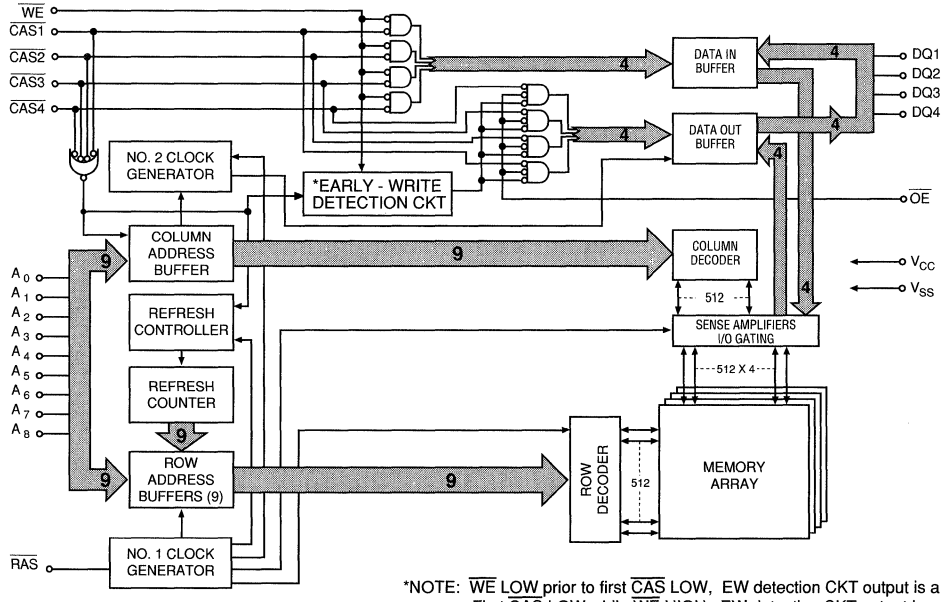
During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and the first $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode.

During a WRITE cycle, data in (Dx) is latched by the falling edge of $\overline{WE}$ or the first $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to the first $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output buffer, data out (Q) is activated and retains the selected cell data until the trailing edge of its corresponding $\overline{CAS}$ occurs (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle ($\overline{OE}$ switching the device from a READ to a WRITE function). The four data inputs and four data outputs are routed through four pins using common I/O, with pin direction controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by the first $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation features.

Returning $\overline{RAS}$ and all four $\overline{CAS}$ controls HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycle will invoke the refresh counter for automatic and sequential row addressing.

FUNCTIONAL BLOCK DIAGRAM
QUAD CAS



*NOTE: WE LOW prior to first CAS LOW, EW detection CKT output is a 1.
First CAS LOW while WE HIGH, EW detection CKT output is a 0,
(OE will now determine I/O).

TRUTH TABLE

Function		RAS	CASx	CASy	WE	OE	Addresses tR	Addresses tC	DQx (DQy always High-Z)
Standby		H	X	X	X	X	X	X	High-Z
READ		L	L	H	H	L	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	H	L	X	ROW	COL	Valid Data In
READ-WRITE		L	L	H	H→L	L→H	ROW	COL	Valid Data Out, Data In
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Valid Data Out
PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	H	L	X	ROW	COL	Valid Data In
	2nd Cycle	L	H→L	H	L	X	n/a	COL	Valid Data In
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H	H→L	L→H	ROW	COL	Valid Data Out, Data In
	2nd Cycle	L	H→L	H	H→L	L→H	n/a	COL	Valid Data Out, Data In
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	H	L	X	ROW	COL	Valid Data In
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} .....-1.0V to +7.0V
Storage Temperature (Ceramic) .....-65°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-2.0	0.8	V	1, 39
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	26
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	80	70	60	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	60	50	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	80	70	60	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	80	70	60	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$1-4, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	185		205		220		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		45		55		ns	31
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	95		100		115		ns	31
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15, 29
Output Enable	t_{OE}		20		20		25	ns	33
Access time from column address	t_{AA}		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	29
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	27
$\overline{RAS}$ precharge time	t_{RP}	55		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	34
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	28
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16, 32
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	32
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17, 27
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	28
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	27
Column address hold time	t_{CAH}	15		15		20		ns	27
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	27
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19, 28
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	29

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 29, 38
Output disable	^tOD		20		20		20	ns	34, 38
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 27
Write command hold time	^tWCH	15		15		20		ns	36
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	28
Data-in setup time	^tDS	0		0		0		ns	22, 29
Data-in hold time	^tDH	15		15		20		ns	22, 29
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	100		110		130		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		60		ns	21, 27
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5, 27
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5, 28
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		10		ns	30
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		20		ns	37
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	

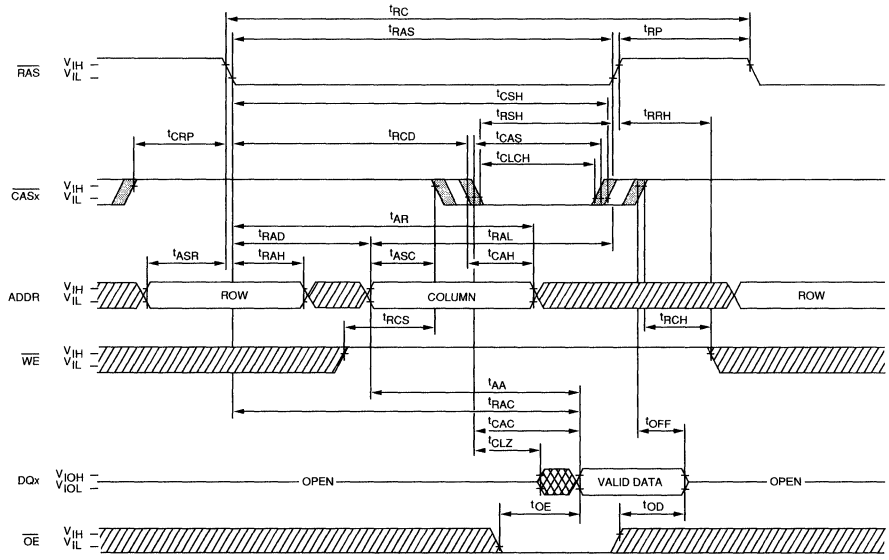
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial 100µs pause is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$x = V_{IH}, data output (x) is high impedance.

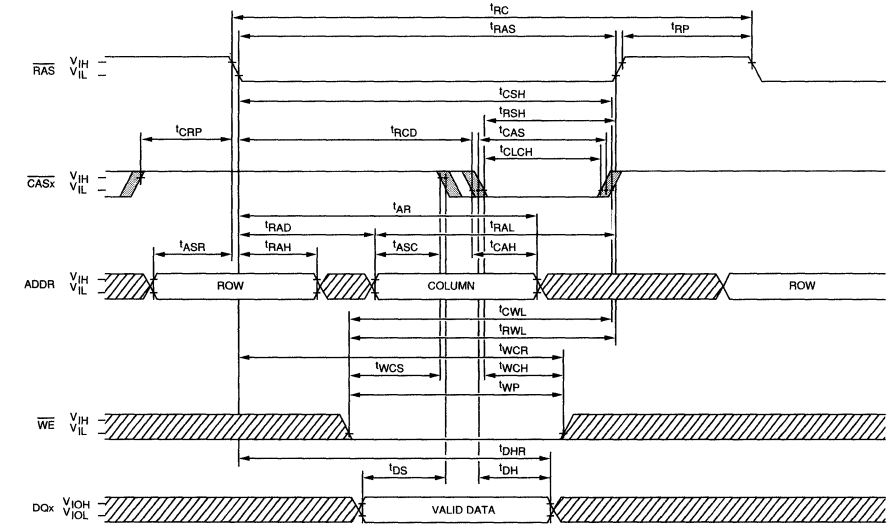
NOTES

12. If $\overline{CAS}$x = VIL, data output (x) may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If at least one $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, all four $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in EARLY-WRITE and READ-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-WRITE CYCLE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$x leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, READ-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. One to three $\overline{CAS}$ controls may be HIGH throughout any given $\overline{CAS}$ cycle, even though the timing waveforms show all $\overline{CAS}$ going LOW. If any one does go LOW, it must meet all the timing requirements listed or the data for that I/O buffer may be invalid. At least one of the four $\overline{CAS}$ controls must be LOW for a valid $\overline{CAS}$ cycle to occur.
26. All other inputs at Vcc -0.2V.
27. The first $\overline{CAS}$x edge to transition LOW.
28. The last $\overline{CAS}$x edge to transition HIGH.
29. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$x input; DQ1 by $\overline{CAS1}$, DQ2 by $\overline{CAS2}$ etc.
30. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
31. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
32. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
33. First DQx controlled by the first $\overline{CAS}$x to go LOW.
34. Last DQx controlled by the last $\overline{CAS}$x to go HIGH.
35. Each $\overline{CAS}$x must meet minimum pulse width.
36. Last $\overline{CAS}$x to go LOW.
37. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If the last $\overline{CAS}$x goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
38. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If the last $\overline{CAS}$x goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$x stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$x remains LOW).
39. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

READ CYCLE



EARLY-WRITE CYCLE



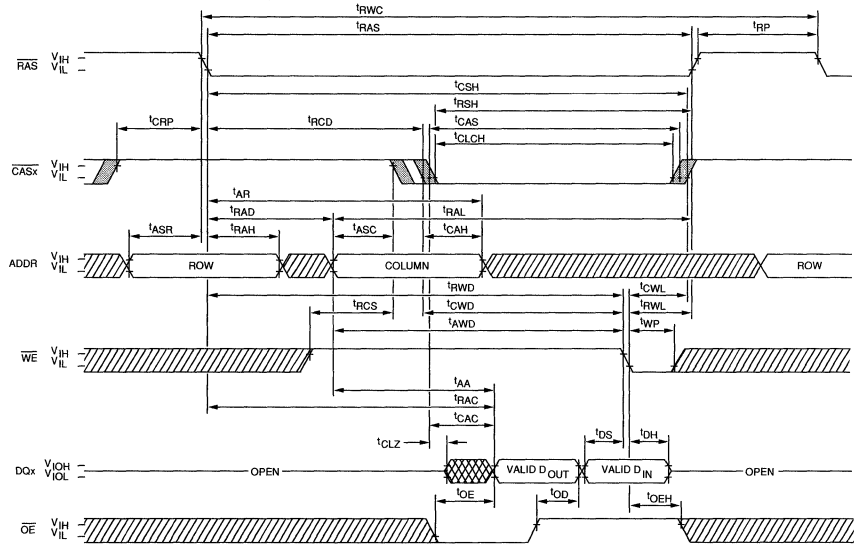
OE = DON'T CARE

DON'T CARE

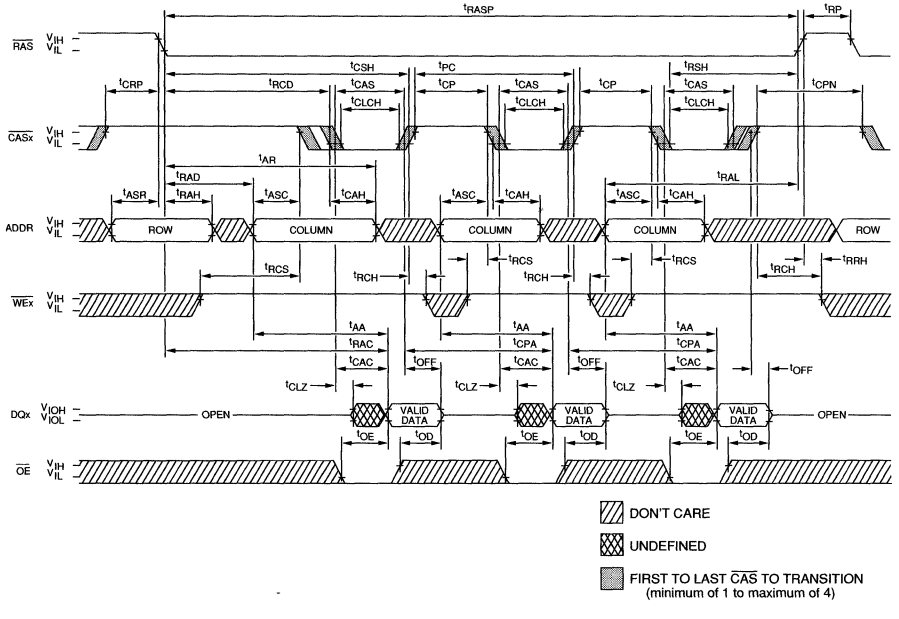
UNDEFINED

FIRST TO LAST $\overline{CAS}$ TO TRANSITION
(minimum of 1, maximum of 4)

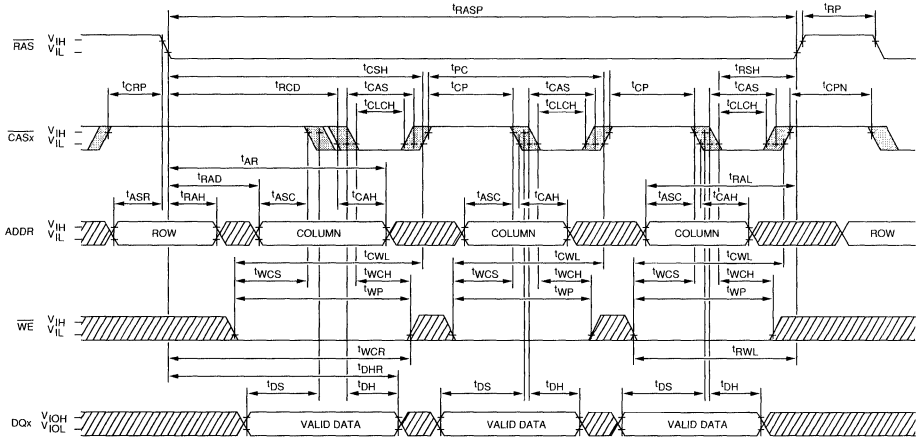
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



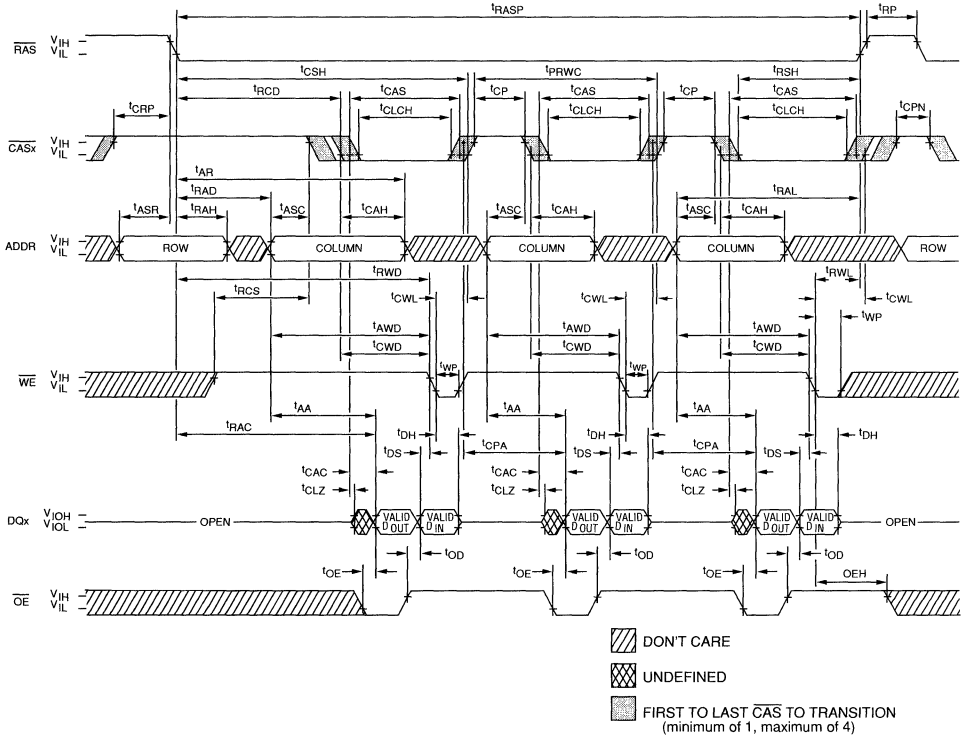
FAST-PAGE-MODE READ CYCLE



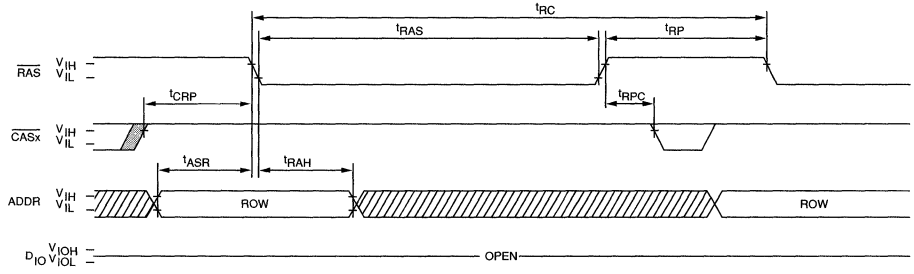
FAST-PAGE-MODE EARLY-WRITE CYCLE



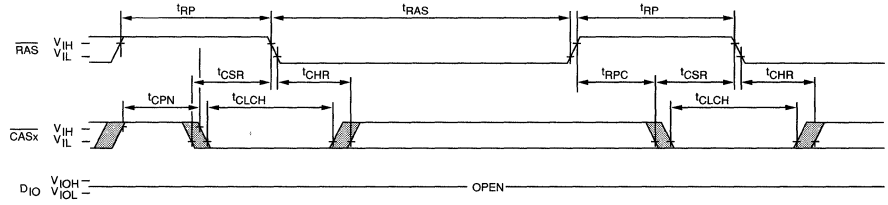
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



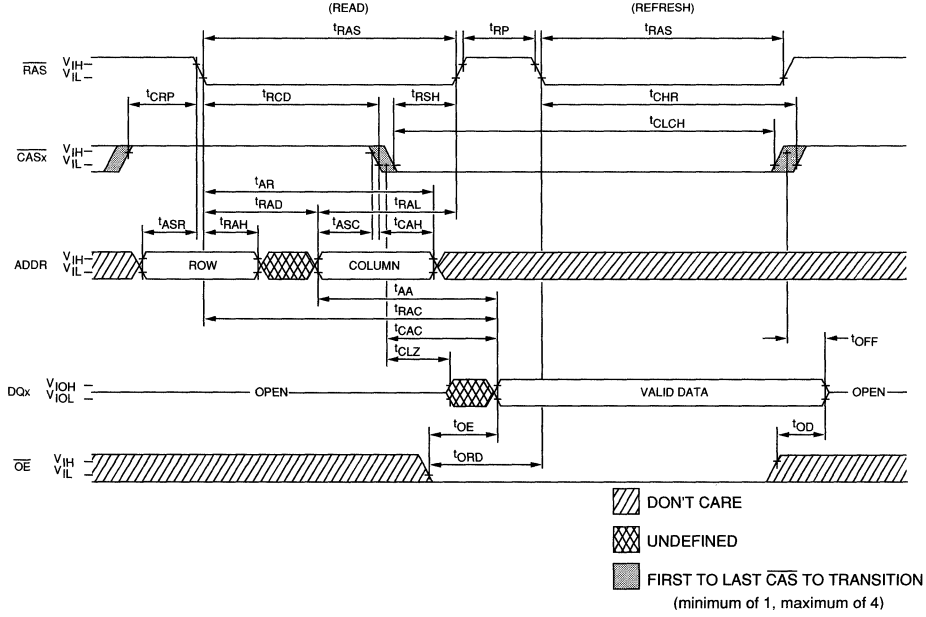
RAS-ONLY REFRESH CYCLE
(ADDR = A_0 - A_8; WE and OE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A_0 - A_8, WE and OE = DON'T CARE)



HIDDEN REFRESH CYCLE
(WE = HIGH, OE = LOW) [24]

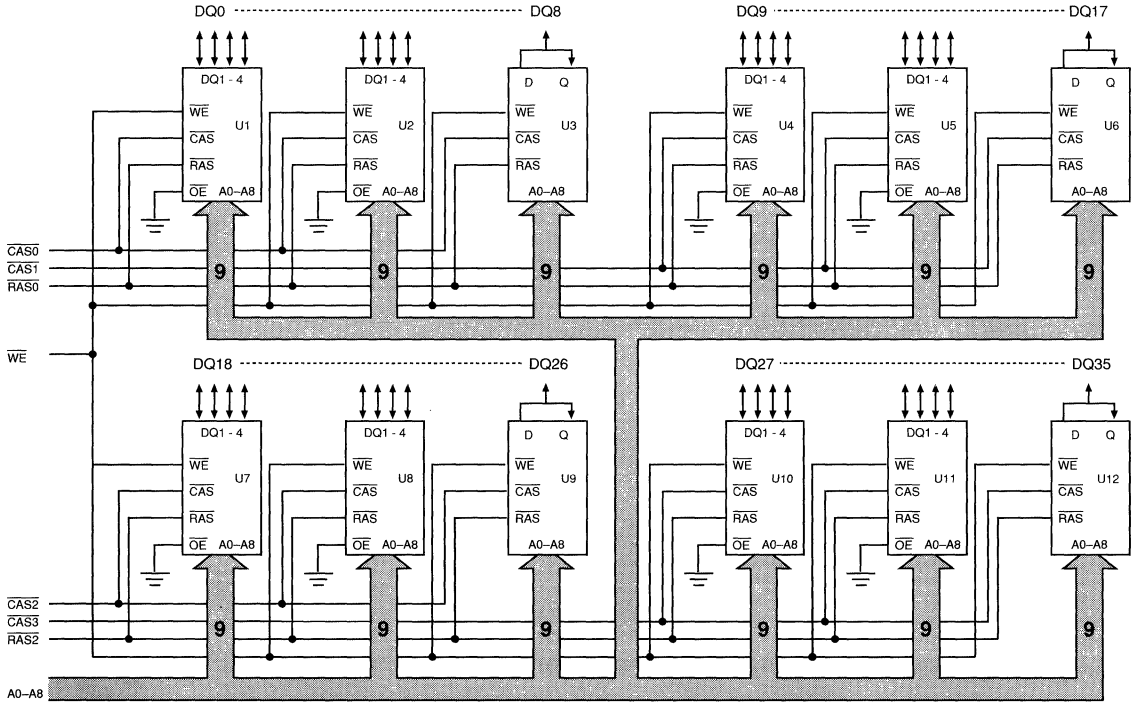


QUAD CAS MODULE UPGRADE

The MT4C4259 (QUAD CAS DRAM) was developed to eliminate the 256K DRAMs used in the current 256K and 512K x 36 DRAM modules and to add total CMOS performance (FAST-PAGE-MODE and faster access speeds: 70ns and 80ns). The MT4C4259 is a 256K x 4 CMOS FAST-PAGE-MODE DRAM with four $\overline{CAS}$ input controls. The four individual $\overline{CAS}$ inputs allow each I/O buffer (DQ) to be separately controlled, just as if there were four separate 256K x 1 DRAMs. Most 256K x 1 DRAMs use older NMOS technology and do not have the access speeds of the newer CMOS 1 Meg (256K x 4), nor FAST-PAGE-MODE capability.

The MT4C4259 will reduce chip count on a x36 module, improving reliability, reducing power consumption and lowering cost. The 256K x 36 will have four 256K x 1 DRAMs replaced by either one or two QUAD CAS DRAMs, depending on whether $\overline{RAS0}$ and $\overline{RAS1}$ must be separate or can be connected together. The 512K x 36 will have eight 256K x 1 DRAMs replaced by either two or four QUAD CAS DRAMs, depending on whether $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, and $\overline{RAS3}$ must be split or can be connected together.

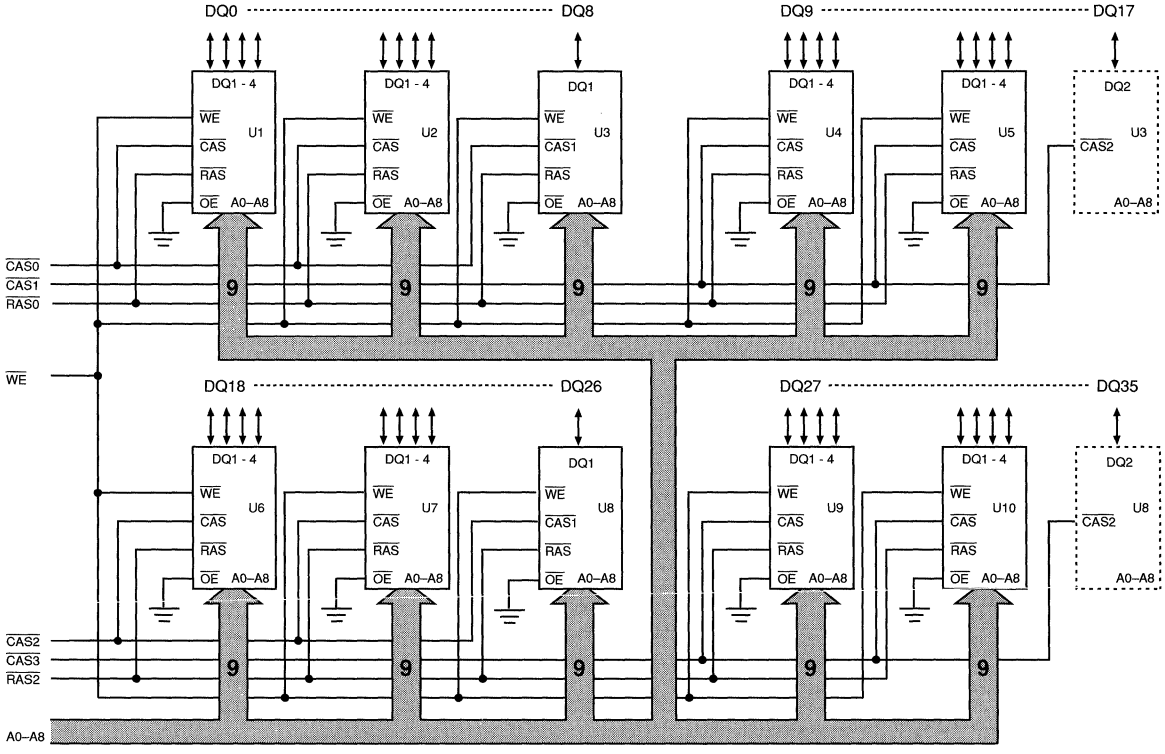
The current 256K x 36 DRAM Module is shown with 256K x 1 DRAMs in Figure 1 below. Figures 2 and 3 show how the same module will be realized with the QUAD CAS DRAM for both the split $\overline{RAS}$ (Figure 2) and the common $\overline{RAS}$ (Figure 3) modules.



U1, U2, U4, U5, U7, U8, U10, U11 = MT4C4256DJ
U3, U6, U9, U12 = MT1259EJ

Figure 1
256K x 36 WITH 256K x 1 FOR PARITY BIT

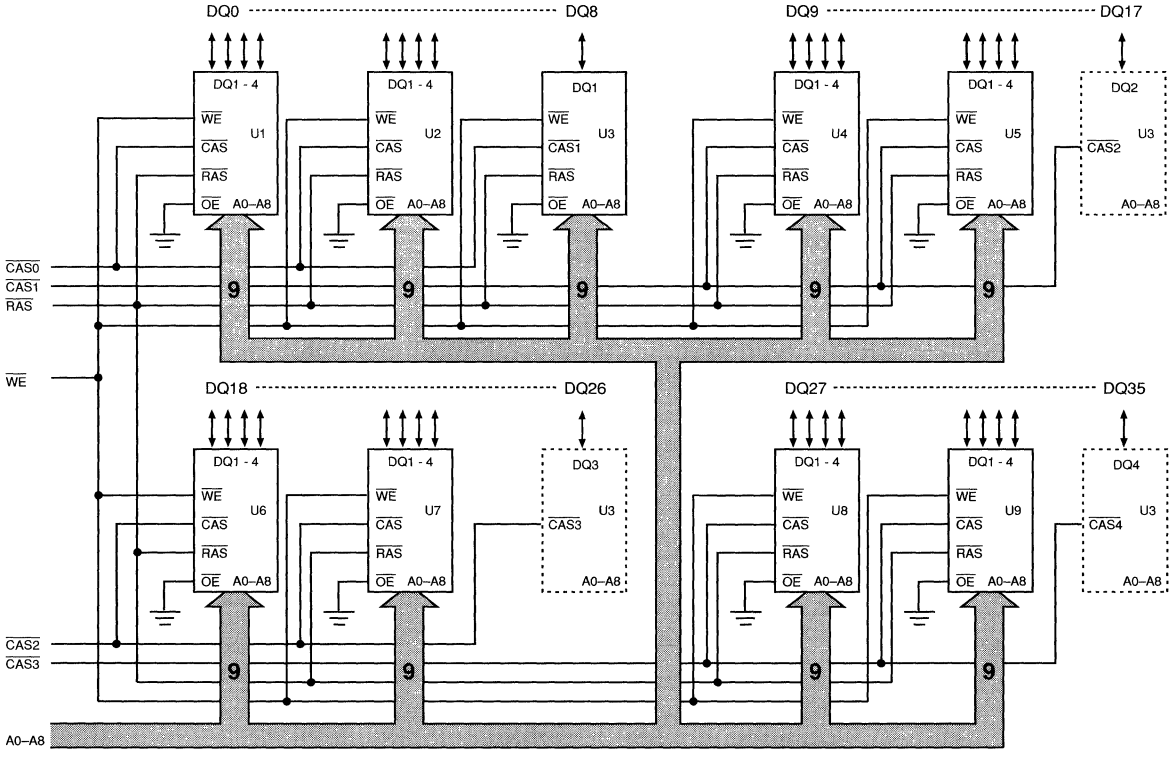
QUAD CAS ENHANCED x36 MODULES



U1, U2, U4, U5, U6, U7, U9, U10 = MT4C4256DJ
U3, U8 = MT4C4259EJ

Figure 2
256K x 36 WITH QUAD $\overline{CAS}$ FOR PARITY BIT AND SPLIT $\overline{RAS}$ CONTROL

QUAD CAS ENHANCED x36 MODULES



U1, U2, U4, U5, U6, U7, U8, U9 = MT4C4256DJ
U3, = MT4C4259EJ

Figure 3
256K x 36 WITH QUAD $\overline{CAS}$ FOR PARITY BIT AND COMMON $\overline{RAS}$ CONTROL

DRAM

256K x 4 DRAM

LOW POWER, FAST PAGE MODE

FEATURES

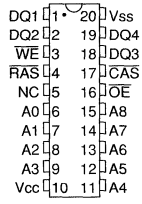
- Industry standard x4 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 1mW standby; 150mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512-cycle refresh in 64ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, and HIDDEN
- Optional FAST PAGE MODE access cycle
- Low CMOS STANDBY CURRENT, 200µA Maximum

OPTIONS

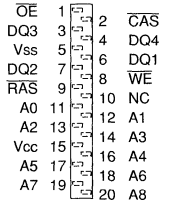
	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Plastic DIP (300mil)	None
Ceramic DIP (300mil)	C
Plastic ZIP (350mil)	Z
Plastic SOJ (300mil)	DJ
Plastic TSOP (*)	VG
• Operating Temperature, T_A	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

PIN ASSIGNMENT (Top View)

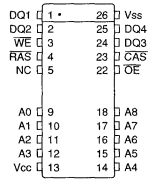
20-Pin DIP
(A-5, B-4)



20-Pin ZIP
(C-2)



20-Pin SOJ
(E-1)



*Consult factory on availability of TSOP packages

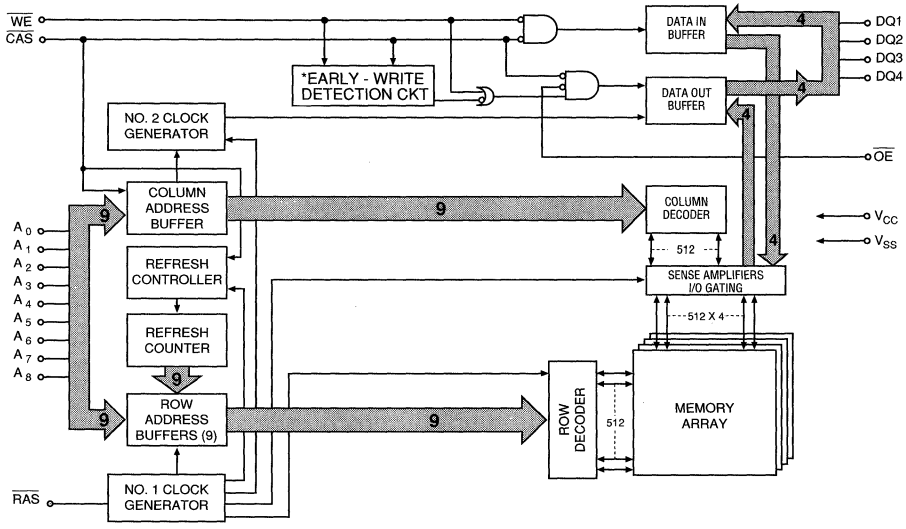
GENERAL DESCRIPTION

The MT4C4260 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE cycle.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 64ms, regardless of sequence. The CAS-BEFORE-RAS refresh will increment the refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection CKT output is a HIGH (EARLY WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address ^tR	Address ^tC	$\overline{OE}$	DATA IN / OUT DQ1-4 (IO)
Standby		H	X	X	X	X	X	High-Z
READ		L	L	H	ROW	COL	L	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	X	Valid Data In
READ-WRITE		L	L	H→L	ROW	COL	L→H	Valid Data Out, Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	L	Valid Data Out
	2nd Cycle	L	H→L	H	n/a	COL	L	Valid Data Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	X	Valid Data In
	2nd Cycle	L	H→L	L	n/a	COL	X	Valid Data In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	L→H	Valid Data Out, Data In
	2nd Cycle	L	H→L	H→L	n/a	COL	L→H	Valid Data Out, Data In
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	X	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	L	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	X	Valid Data In
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-2.0	0.8	V	1, 28
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT: (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	200	200	200	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	75	65	55	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	55	45	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	75	65	55	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	75	65	60	mA	3, 5
BATTERY BACKUP REFRESH CURRENT: Average power supply current during battery backup refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) of 1µs; $\overline{WE}$, A0-A9 and D in = Vcc -0.2V or 0.2V (D in may be left OPEN), ^tRC = 125µs (512 rows at 125us = 64ms)	I_{CC7}	200	200	200	µA	3, 5, 7

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	185		205		245		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		45		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	95		100		115		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Output Enable	t_{OE}		20		20		25	ns	
Access time from column address	t_{AA}		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

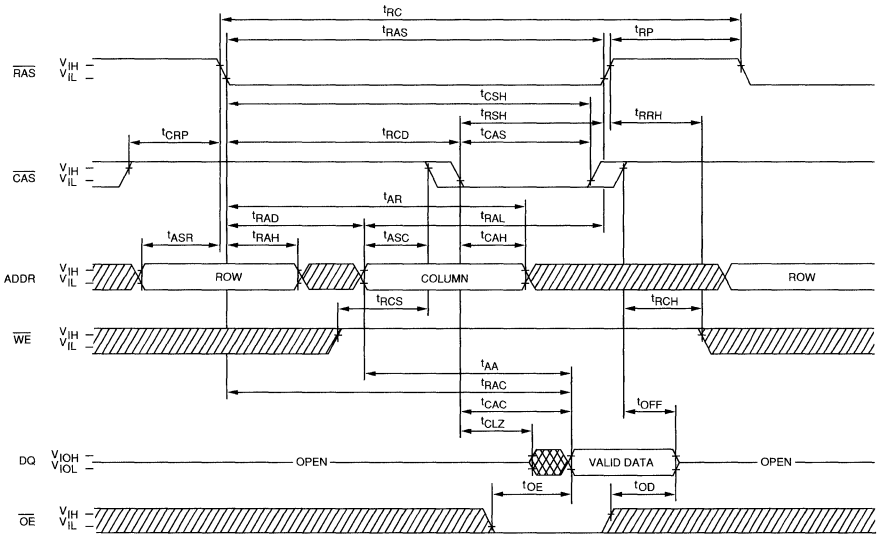
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 27
Output Disable	^tOD		20		20		20	ns	27
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	100		110		130		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		60		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		64		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		20		ns	26
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	24

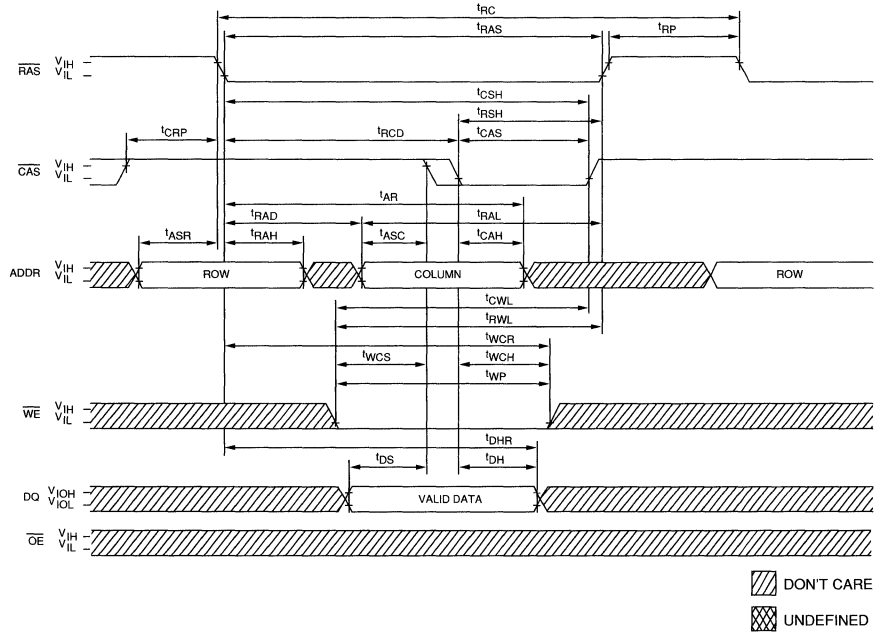
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 64ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. All other inputs at Vcc -0.2V.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
28. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

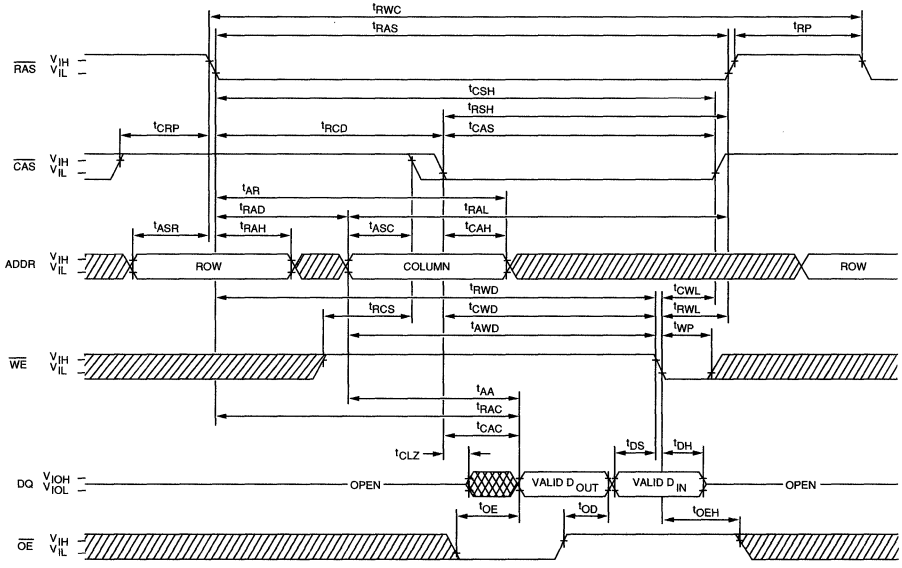
READ CYCLE



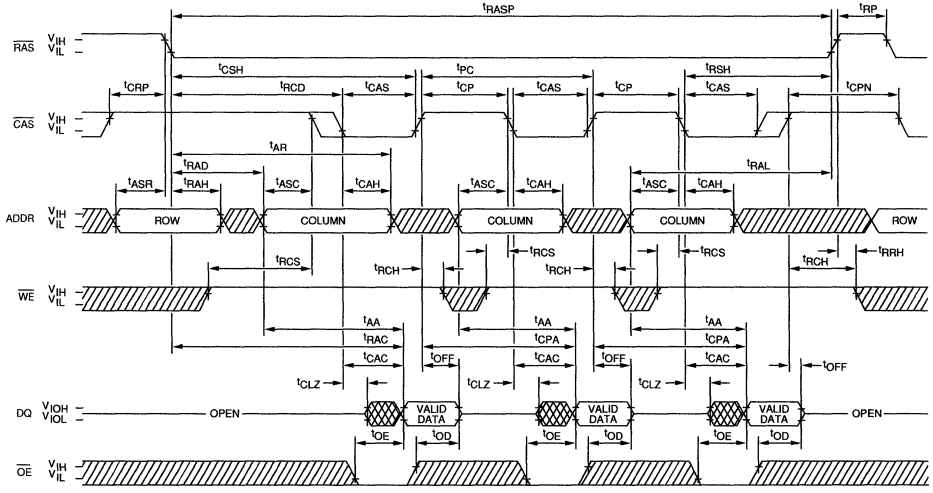
EARLY-WRITE CYCLE



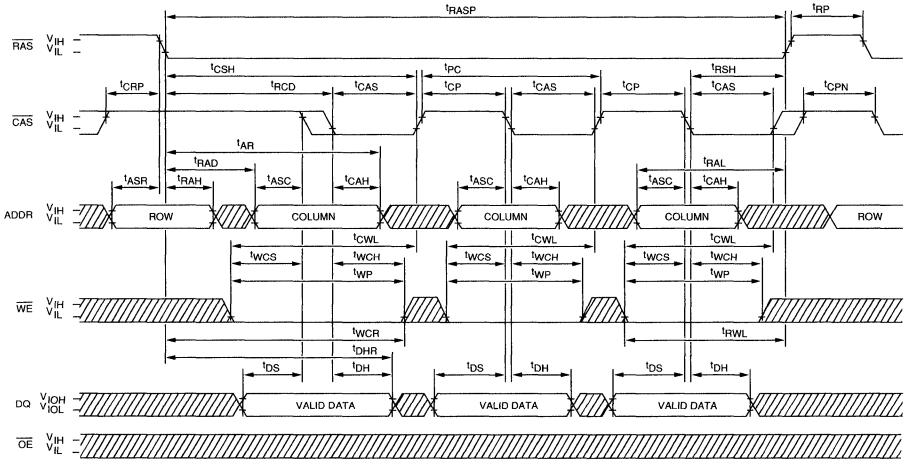
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



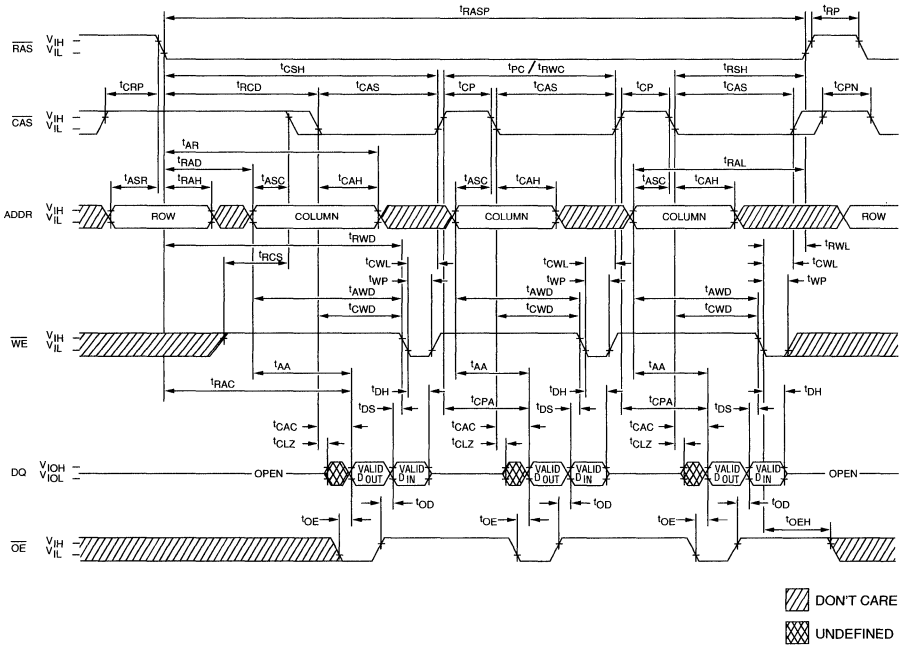
FAST-PAGE-MODE READ CYCLE



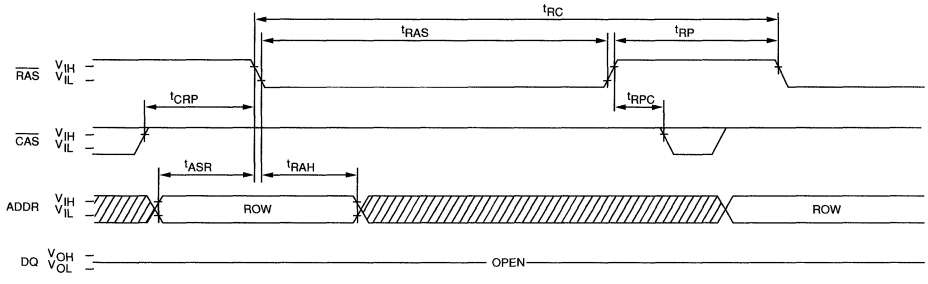
FAST-PAGE-MODE EARLY-WRITE CYCLE



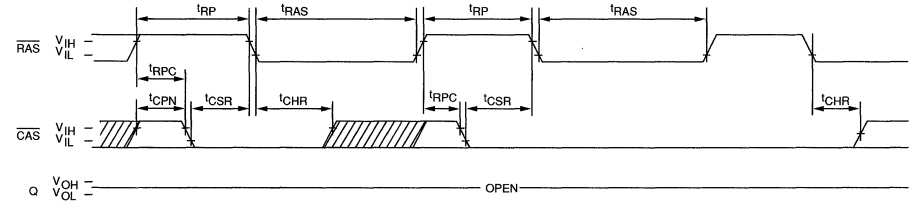
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



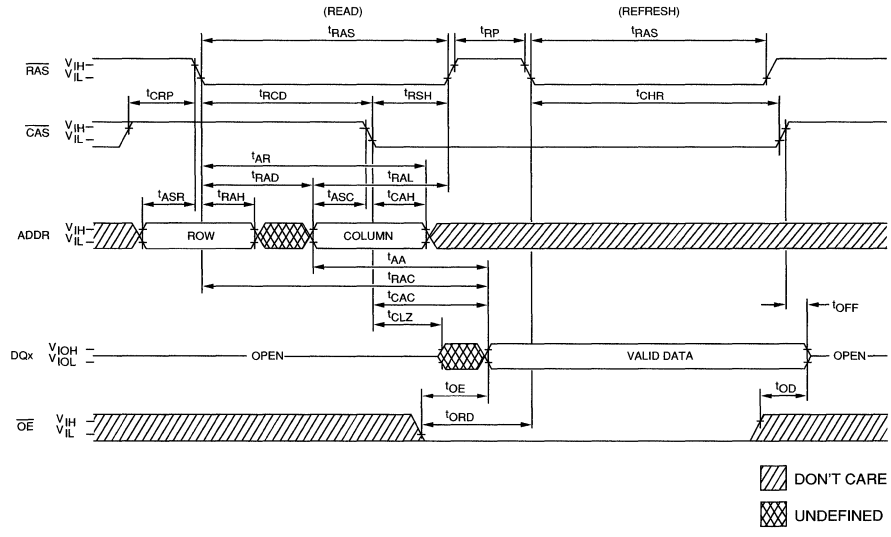
$\overline{RAS}$-ONLY REFRESH CYCLE
($ADDR = A_0 - A_8$; $\overline{WE}$ = DON'T CARE)



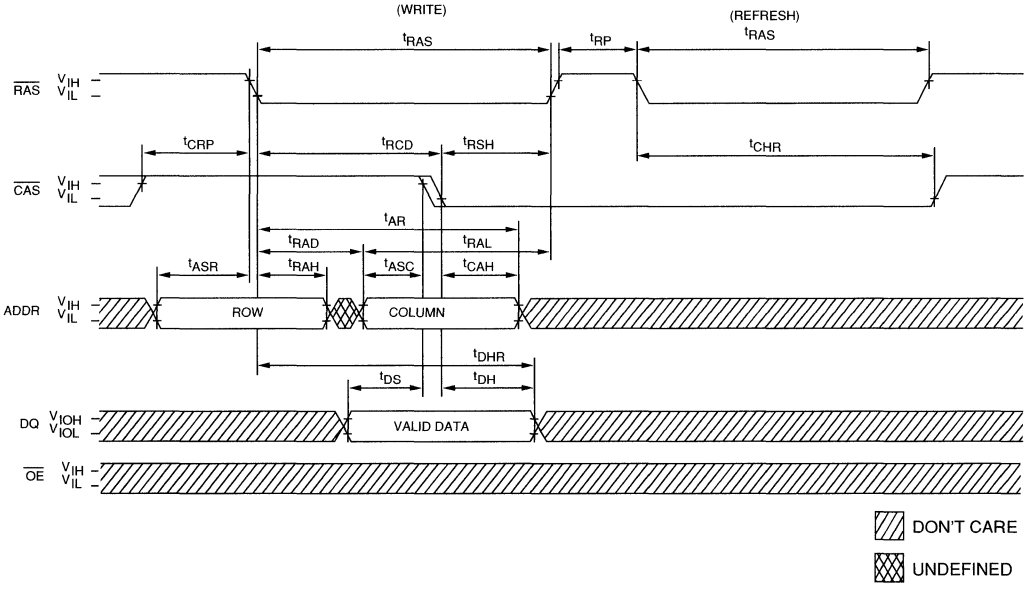
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
($A_0 - A_8$, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH, $\overline{OE}$ = LOW) [24]



HIDDEN REFRESH CYCLE
($\overline{WE}$ = LOW)



DRAM

1 MEG x 4 DRAM

FAST PAGE MODE

FEATURES

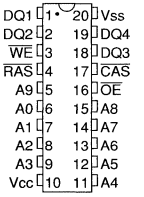
- Industry standard x4 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{CBR}$), and HIDDEN
- FAST PAGE MODE access cycle
- 300 and 350 mil wide SOJ packages
- Two CBR options: CBR with $\overline{WE}$ a don't care (1 Meg compatible) and CBR with $\overline{WE}$ a HIGH (JEDEC test mode capable via WCBR)

OPTIONS

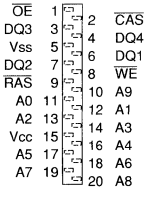
	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Ceramic DIP (300mil)	CN
Ceramic DIP (400mil)	C
Plastic ZIP (350mil)	Z
Plastic SOJ (300mil)	DJ
Plastic SOJ (350mil)	DJW
Plastic TSOP (*)	TG
• $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh	
CBR with $\overline{WE}$ a don't care	None
CBR with $\overline{WE}$ a HIGH	J
• Operating Temperature, TA	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

PIN ASSIGNMENT (Top View)

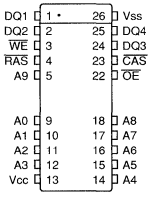
20-Pin CDIP (B-4, B-5)



20-Pin ZIP (C-3)



20-Pin SOJ (E-1, E-2)



*Consult factory on availability of TSOP packages

GENERAL DESCRIPTION

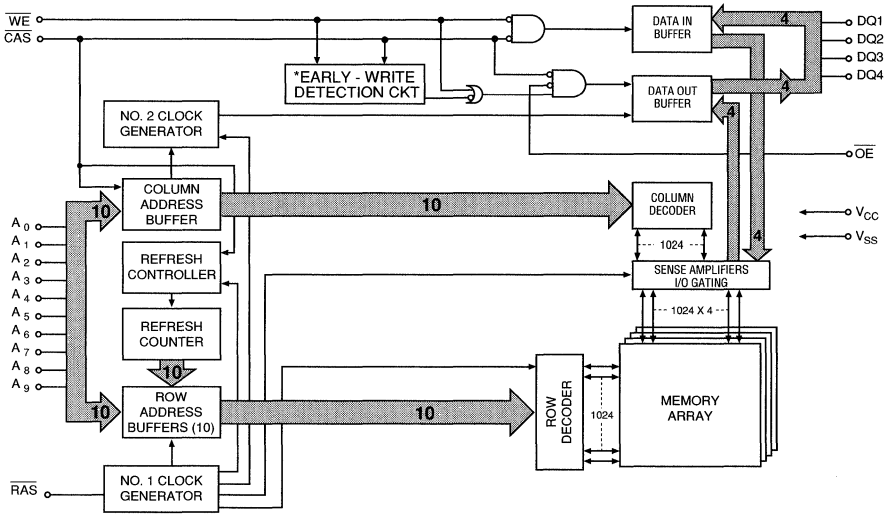
The MT4C4001 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode.

During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), The Qs are activated and retain the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: WE LOW prior to CAS LOW, EW detection CKT output is a HIGH (EARLY WRITE)
CAS LOW prior to WE LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		RAS	CAS	WE	Address tR	Address tC	OE	DATA IN / OUT DQ1-4
Standby		H	X	X	X	X	X	High-Z
READ		L	L	H	ROW	COL	L	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	X	Valid Data In
READ-WRITE		L	L	H→L	ROW	COL	L→H	Valid Data Out, Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	L	Valid Data Out
	2nd Cycle	L	H→L	H	n/a	COL	L	Valid Data Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	X	Valid Data In
	2nd Cycle	L	H→L	L	n/a	COL	X	Valid Data In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	L→H	Valid Data Out, Data In
	2nd Cycle	L	H→L	H→L	n/a	COL	L→H	Valid Data Out, Data In
RAS-ONLY REFRESH		H	X	X	ROW	n/a	X	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	L	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	X	Valid Data In
CAS-BEFORE-RAS REFRESH	Standard	H→L	L	X	X	X	X	High-Z
	"J" Option	H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	90		95		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 27

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

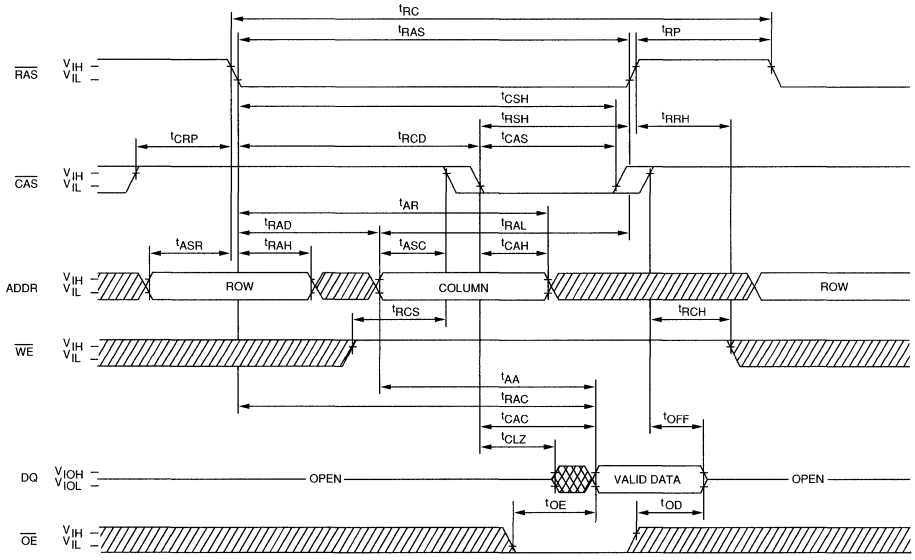
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		110		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	60		65		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		50		50		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRH	10		10		10		ns	25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tWRP	10		10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	25
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Output disable	^tOD	15		20		20		ns	27
Output enable	^tOE	15		20		20		ns	23
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	26

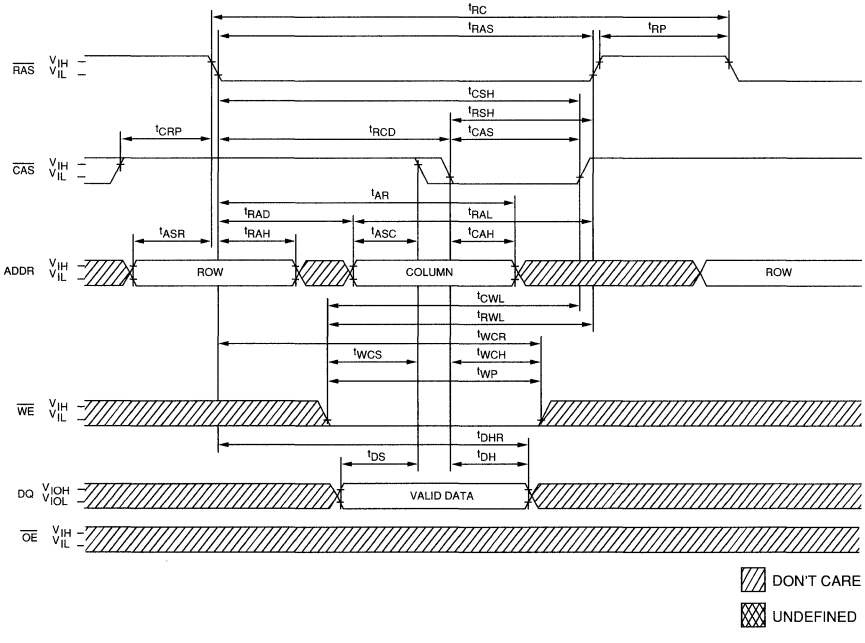
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

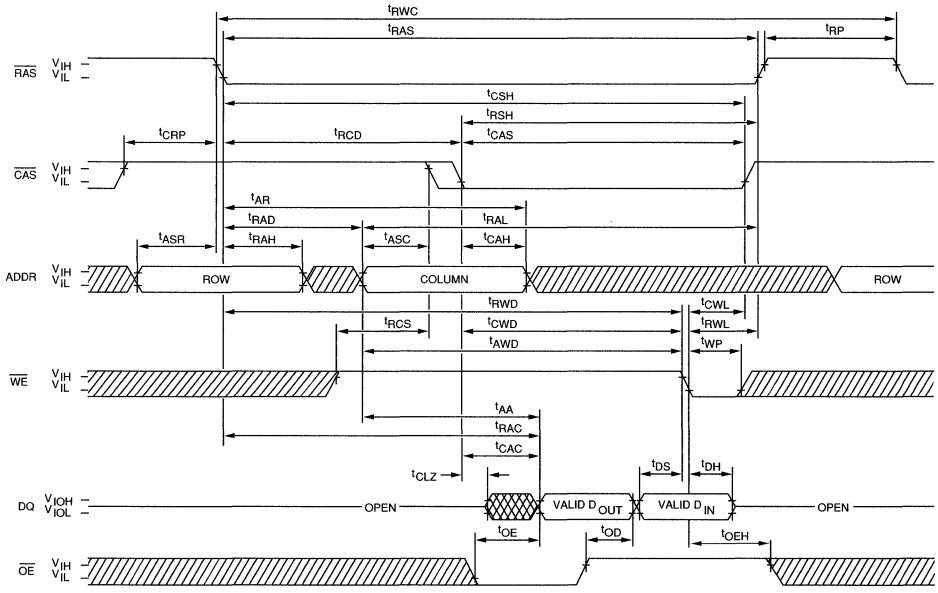
READ CYCLE



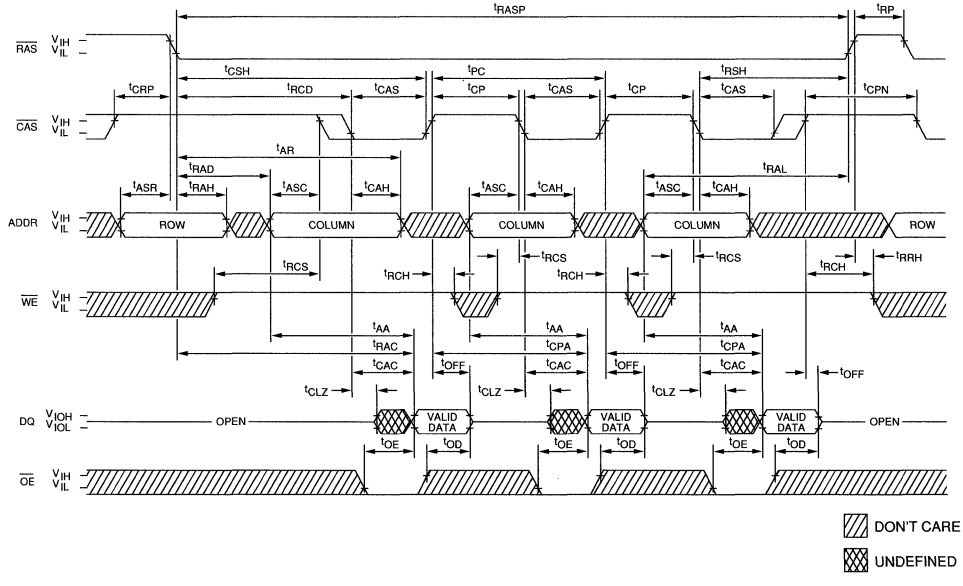
EARLY-WRITE CYCLE



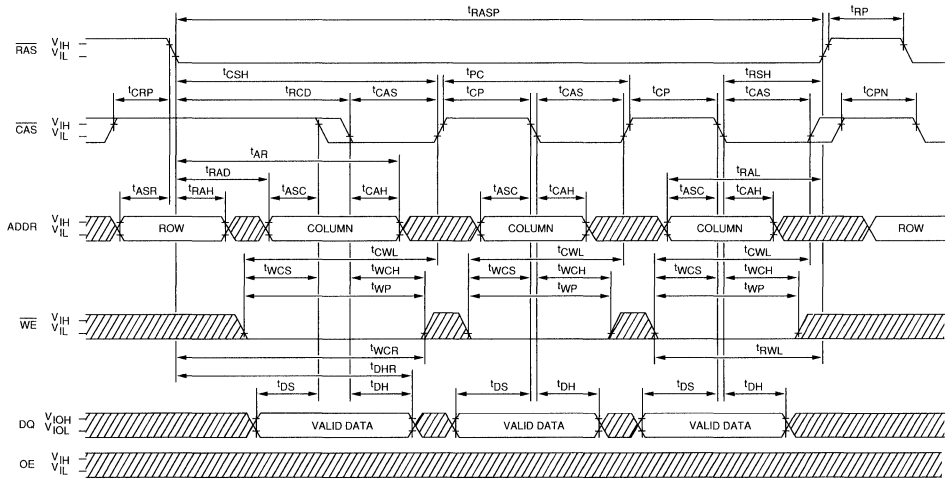
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



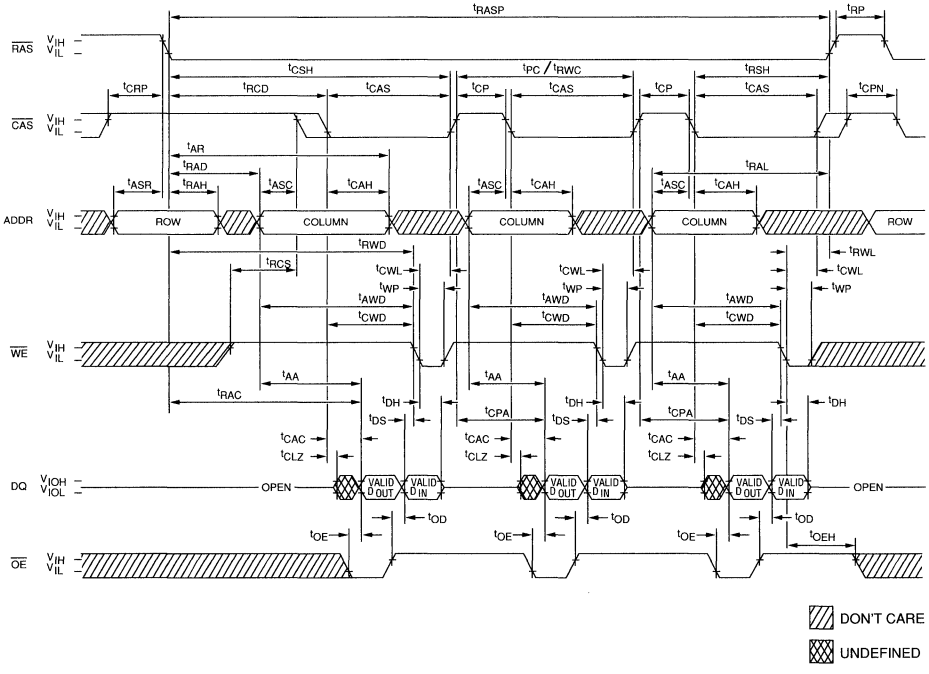
FAST-PAGE-MODE READ CYCLE



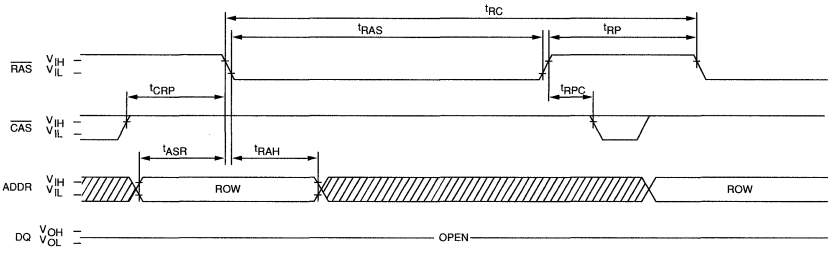
FAST-PAGE-MODE EARLY-WRITE CYCLE



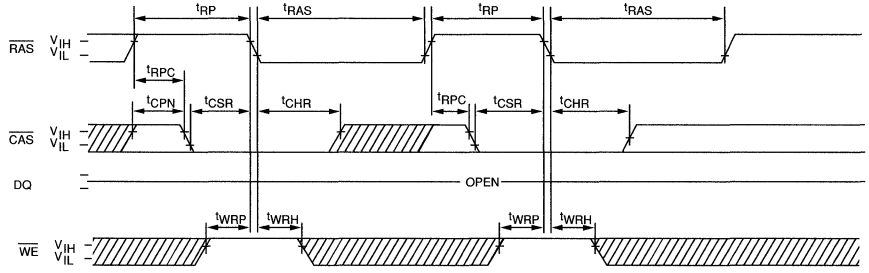
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



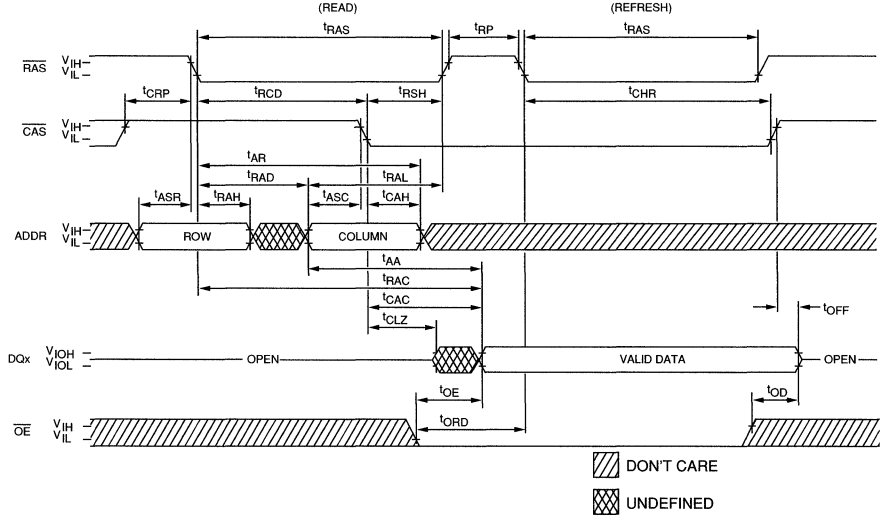
$\overline{RAS}$-ONLY REFRESH CYCLE
($ADDR = A_0 - A_9$; $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
($A_0 - A_9$, and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW) [24]



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a don't care. The 4 Meg, on the other hand, specifies the CBR REFRESH mode to be a $\overline{W}$CBR, which is CBR with the $\overline{WE}$ pin held at a logical HIGH level.

The reason for $\overline{W}$CBR instead of CBR on the 4 Meg is that a CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode ($\overline{W}$CBR). In contrast, the 1 Meg test mode is entered by applying a HIGH signal to the test pin (pin 4 on DIP, pin 5 on SOJ and pin 8 on ZIP). This HIGH signal is usually a "supervoltage" (V in ≥ 7.5V) so normal TTL or CMOS HIGH levels will not cause the part to enter the test mode.

POWER-UP

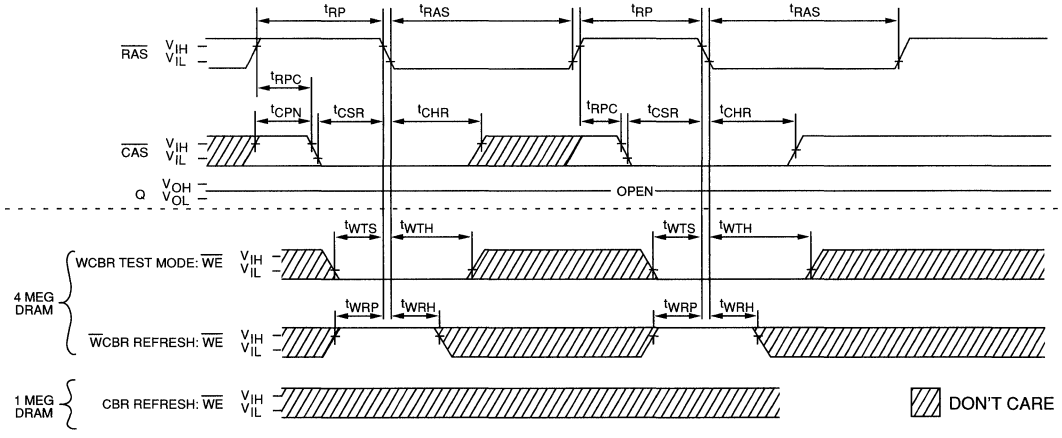
The 4 Meg $\overline{W}$CBR constraint may also introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any 8 $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that 8 $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a CBR REFRESH cycle.

SUMMARY

1. The optional 1 Meg test pin is the A10 pin on the 4 Meg .
2. For optional test mode, the 1 Meg requires a valid HIGH on the test pin while the 4 Meg requires a CBR cycle with $\overline{WE}$ LOW.
3. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be don't care while the 4 Meg CBR requires $\overline{WE}$ to be HIGH ($\overline{W}$CBR).
4. The 8 $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or CBR REFRESH cycles.

SPECIAL FEATURE

A memory system currently using 1 Meg DRAMs with $\overline{WE}$ as a don't care during CBR REFRESH does not allow for direct upgrading to 4 Meg DRAMs. Micron, realizing some companies will have this situation, provides a special feature on its 4 Meg DRAM, that requires "supervoltage" to access the 4 Meg JEDEC WCBR test function. This allows the Micron 4 Meg DRAM to be refreshed in the same manner as any 1 MEG DRAM. Note that the eight power-up cycles should only be refresh cycles in order to guarantee that any 4 Meg DRAM, including Micron's, does not inadvertently power-up in the test mode.



COMPARISON OF 4 MEG TEST MODE AND $\overline{W}$CBR TO 1 MEG CBR

DRAM

1 MEG x 4 DRAM

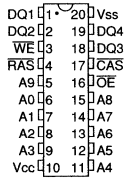
STATIC COLUMN

FEATURES

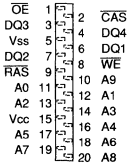
- Industry standard x4 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), and HIDDEN
- STATIC COLUMN access cycle
- 300 and 350 mil wide SOJ packages
- Two CBR options: CBR with $\overline{WE}$ a don't care (1 Meg compatible) and CBR with $\overline{WE}$ a HIGH (JEDEC test mode capable via WCBR)

PIN ASSIGNMENT (Top View)

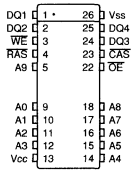
20-Pin CDIP (B-4, B-5)



20-Pin ZIP (C-3)



20-Pin SOJ (E-1, E-2)



*Consult factory on availability of TSOP packages

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Ceramic DIP (300mil) — CN
  - Ceramic DIP (400mil) — C
  - Plastic ZIP (350mil) — Z
  - Plastic SOJ (300mil) — DJ
  - Plastic SOJ (350mil) — DJW
  - Plastic TSOP (*) — TG
- $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh
  - CBR with $\overline{WE}$ a don't care — None
  - CBR with $\overline{WE}$ a HIGH — J
- Operating Temperature, T_A
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT

GENERAL DESCRIPTION

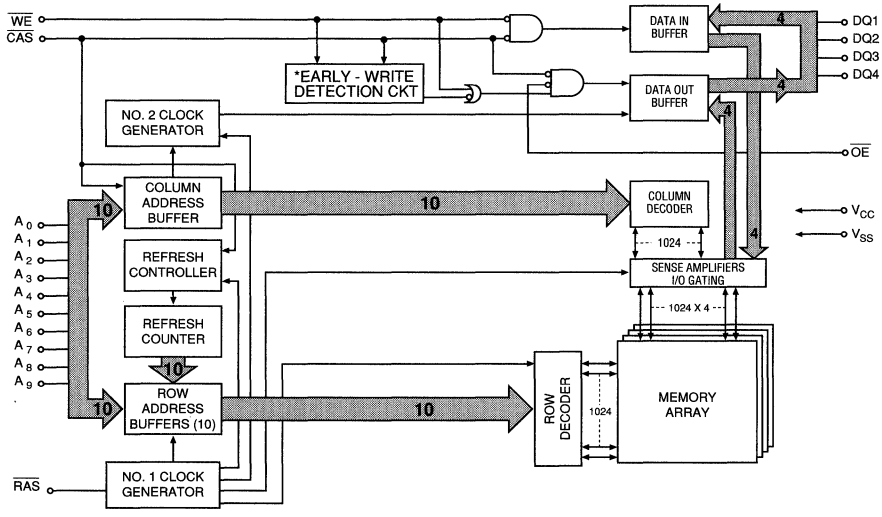
The MT4C4003 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode.

During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection CKT output is a HIGH (EARLY WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address ^tR	Address ^tC	$\overline{OE}$	DATA IN / OUT DQ1-4
Standby		H	X	X	X	X	X	High-Z
READ		L	L	H	ROW	COL	L	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	X	Valid Data In
READ-WRITE		L	L	H→L	ROW	COL	L→H	Valid Data Out, Data In
STATIC COLUMN READ	1st Cycle	L	L	H	ROW	COL	L	Valid Data Out
	2nd Cycle	L	L	H	n/a	COL	L	Valid Data Out
STATIC COLUMN EARLY-WRITE	1st Cycle	L	L	L	ROW	COL	X	Valid Data In
	2nd Cycle	L	L	H→L	n/a	COL	X	Valid Data In
STATIC COLUMN READ-WRITE	1st Cycle	L	L	H→L	ROW	COL	L→H	Valid Data Out, Data In
	2nd Cycle	L	L	H→L	n/a	COL	L→H	Valid Data Out, Data In
$\overline{RAS}$-ONLY REFRESH		H	X	X	ROW	n/a	X	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	L	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	X	Valid Data In
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	Standard	H→L	L	X	X	X	X	High-Z
	"J" Option	H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	165		185		205		ns	
STATIC-COLUMN READ or WRITE cycle time	^tSC	40		40		45		ns	
STATIC-COLUMN READ-WRITE cycle time	^tSRMC	95		100		110		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 27
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

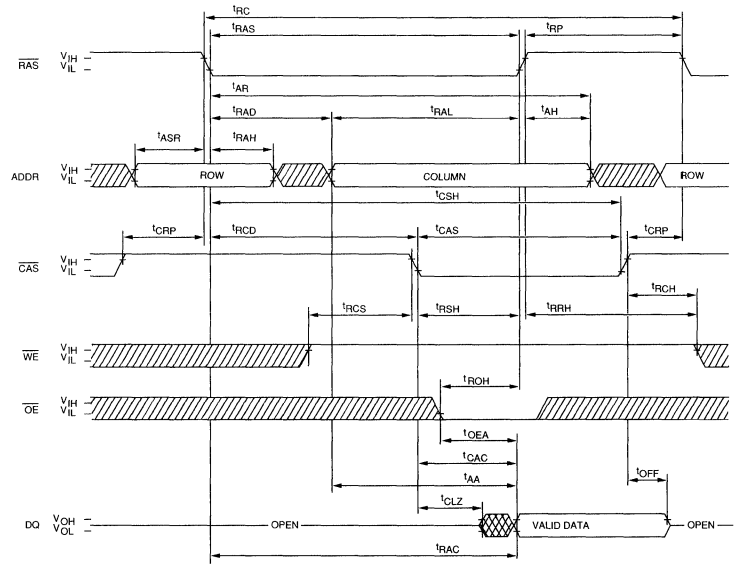
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Data-in setup time	^{t}DS	0		0		0		ns	22
Data-in hold time	^{t}DH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	90		100		110		ns	21
Column address to $\overline{WE}$ delay time	^{t}AWD	60		65		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	45		50		50		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	^{t}REF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}CHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}WRH	10		10		10		ns	25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^{t}WRP	10		10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	^{t}WTH	10		10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	^{t}WTS	10		10		10		ns	25
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
Output disable	^{t}OD	15		20		20		ns	27
Output enable	^{t}OE	15		20		20		ns	23
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^{t}OEH	15		20		20		ns	26
Write inactive time	^{t}WI	10		10		10		ns	
Last WRITE to column address delay time	^{t}LWAD	15	25	20	30	20	35	ns	
Last WRITE to column address hold time	^{t}AHLW	55		65		75		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^{t}ROH	10		10		10		ns	
Output data hold time from column address	^{t}AOH	5		5		5		ns	
Output data enable from WRITE	^{t}OW	20		20		20		ns	
Access time from last WRITE	^{t}ALW	55		65		75		ns	
Column address hold time referenced to $\overline{RAS}$ HIGH	^{t}AH	5		5		10		ns	
CAS pulse width in STATIC-COLUMN mode	^{t}CSC	^{t}CAS		^{t}CAS		^{t}CAS		ns	

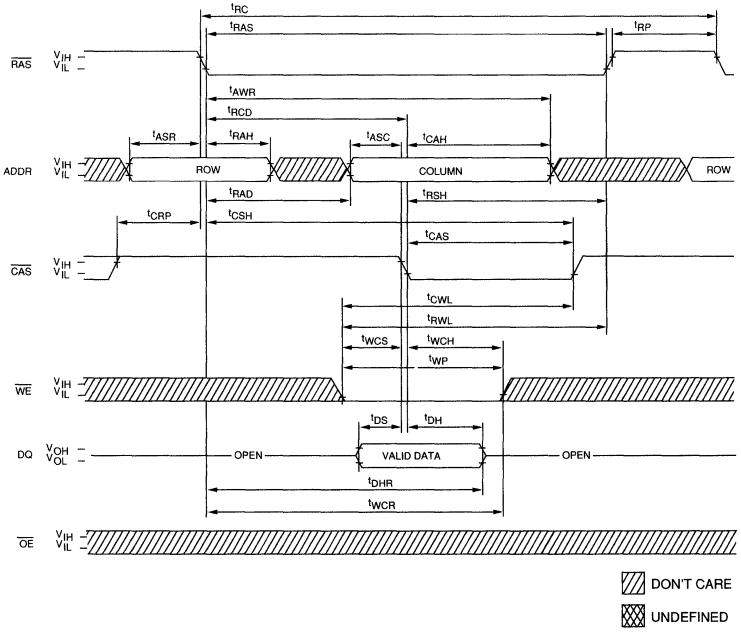
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

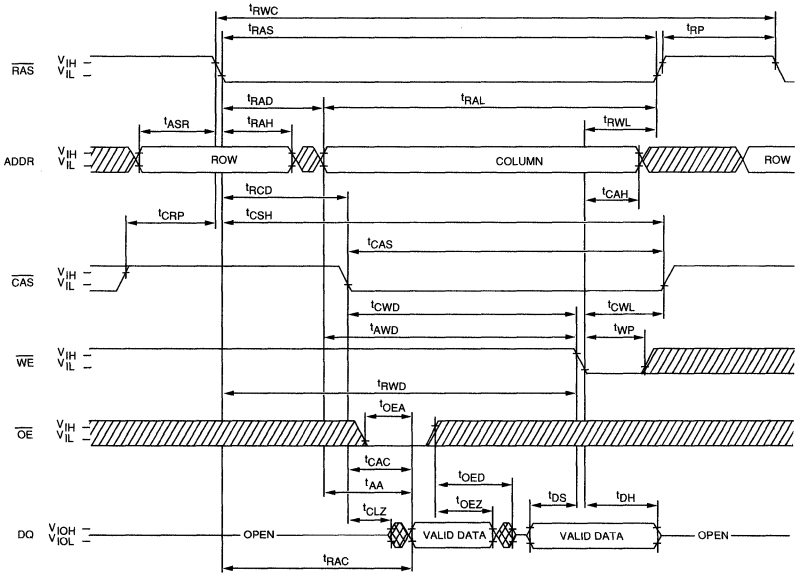
READ CYCLE



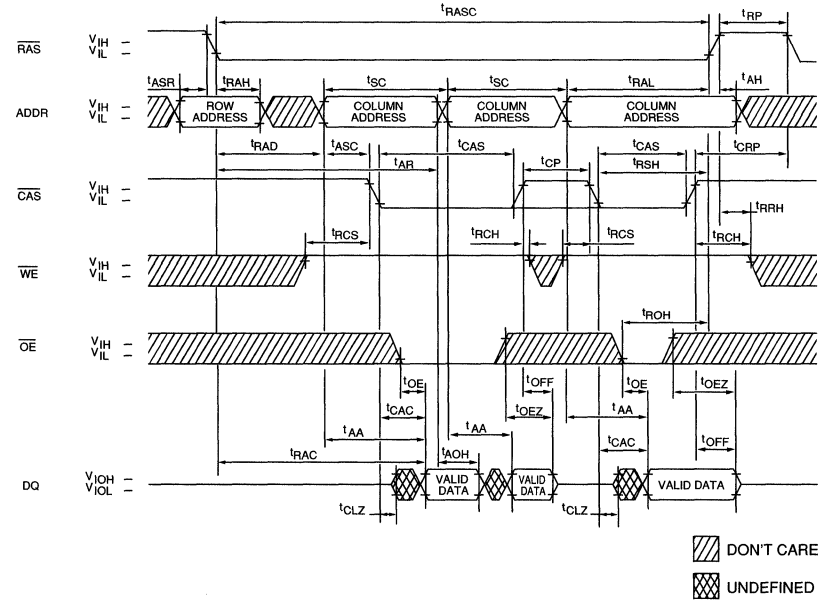
EARLY-WRITE CYCLE



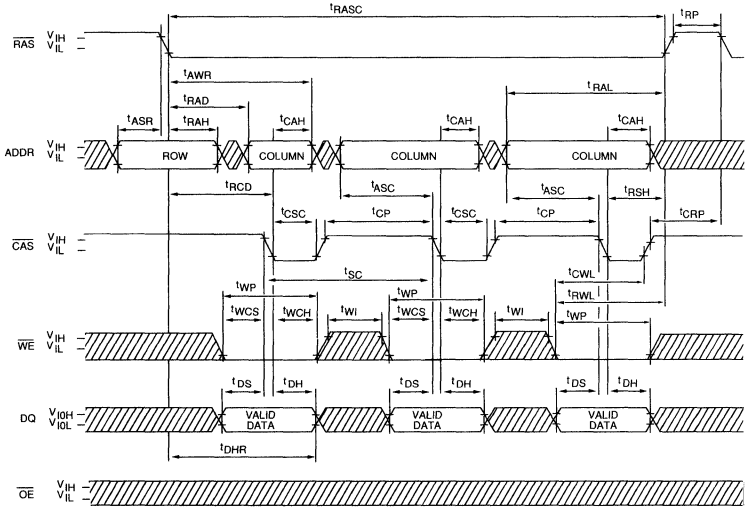
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



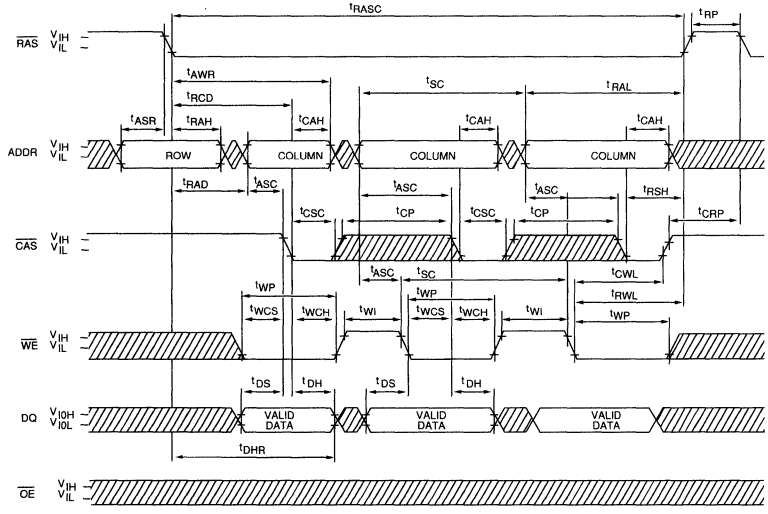
STATIC-COLUMN READ CYCLE



STATIC-COLUMN EARLY-WRITE CYCLE
(CAS Controlled)



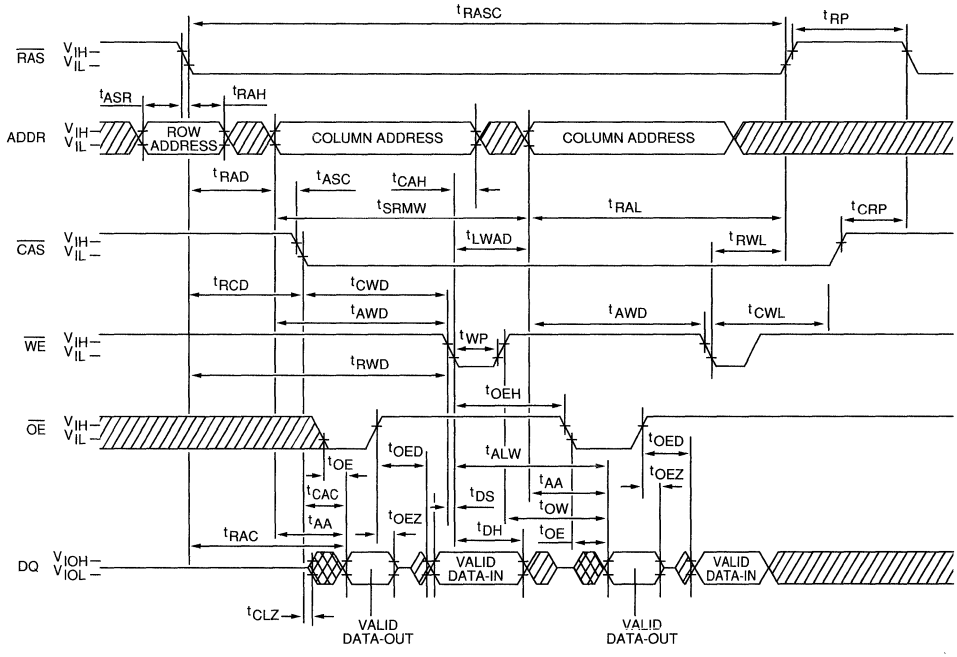
STATIC-COLUMN EARLY-WRITE CYCLE
(WE Controlled)



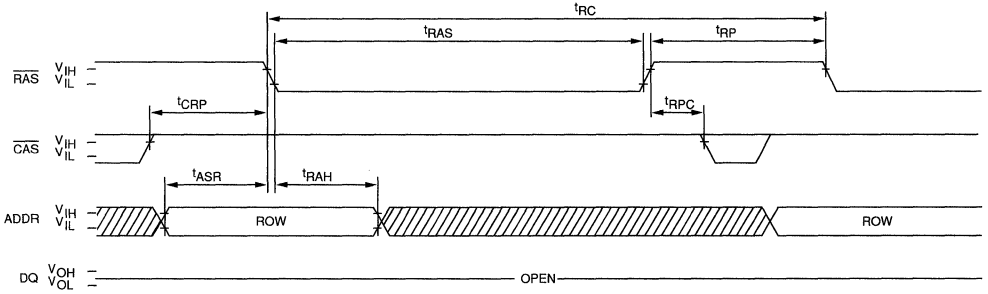
DON'T CARE

UNDEFINED

STATIC-COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



RAS-ONLY REFRESH CYCLE
(ADDR = A_0 - A_9; WE = DON'T CARE)

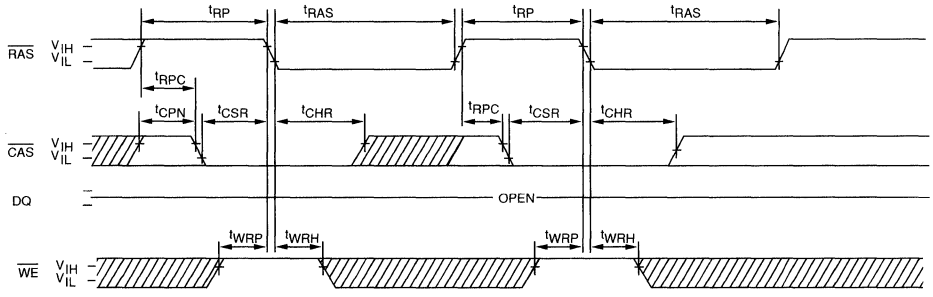


DON'T CARE

UNDEFINED

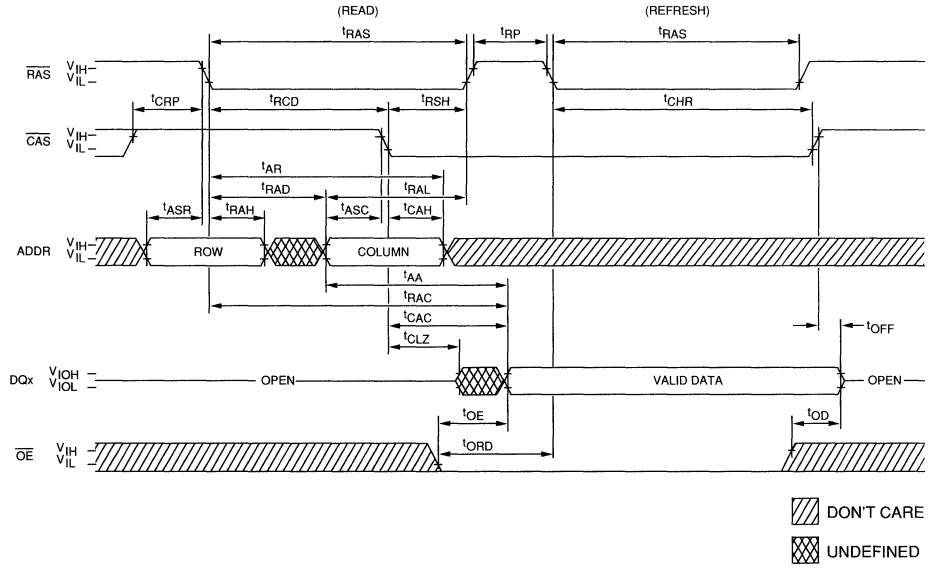
CAS-BEFORE-RAS REFRESH CYCLE

(A_0 - A_9, and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW) [24]



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a don't care. The 4 Meg, on the other hand, specifies the CBR REFRESH mode to be a $\overline{W}$CBR, which is CBR with the $\overline{WE}$ pin held at a logical HIGH level.

The reason for $\overline{W}$CBR instead of CBR on the 4 Meg is that a CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode ($\overline{W}$CBR). In contrast, the 1 Meg test mode is entered by applying a HIGH signal to the test pin (pin 4 on DIP, pin 5 on SOJ and pin 8 on ZIP). This HIGH signal is usually a "supervoltage" (V in ≥ 7.5V) so normal TTL or CMOS HIGH levels will not cause the part to enter the test mode.

POWER-UP

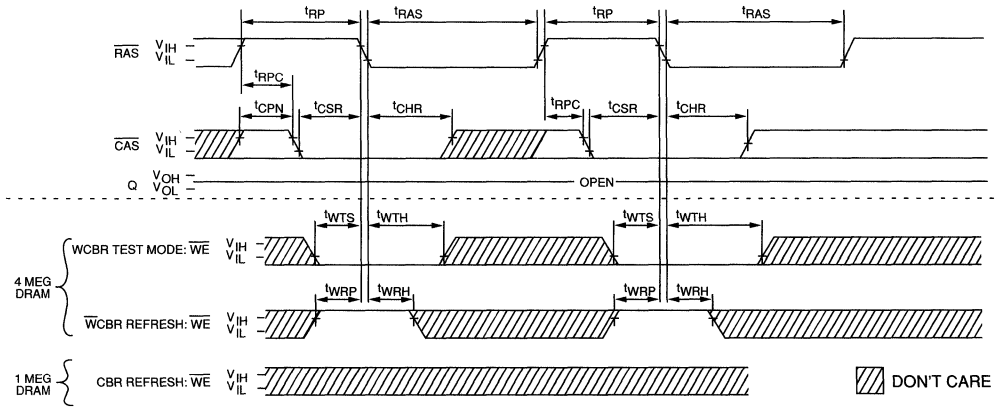
The 4 Meg $\overline{W}$CBR constraint may also introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any 8 $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that 8 $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a $\overline{W}$CBR REFRESH cycle.

SUMMARY

1. The optional 1 Meg test pin is the A10 pin on the 4 Meg .
2. For optional test mode, the 1 Meg requires a valid HIGH on the test pin while the 4 Meg requires a CBR cycle with $\overline{WE}$ LOW.
3. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be don't care while the 4 Meg CBR requires $\overline{WE}$ to be HIGH ($\overline{W}$CBR).
4. The 8 $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or $\overline{W}$CBR REFRESH cycles.

SPECIAL FEATURE

A memory system currently using 1 Meg DRAMs with $\overline{WE}$ as a don't care during CBR REFRESH does not allow for direct upgrading to 4 Meg DRAMs. Micron, realizing some companies will have this situation, provides a special feature on its 4 Meg DRAM, that requires "supervoltage" to access the 4 Meg JEDEC WCBR test function. This allows the Micron 4 Meg DRAM to be refreshed in the same manner as any 1 MEG DRAM. Note that the eight power-up cycles should only be refresh cycles in order to guarantee that any 4 Meg DRAM, including Micron's, does not inadvertently power-up in the test mode.



COMPARISON OF 4 MEG TEST MODE AND $\overline{W}$CBR TO 1 MEG CBR

DRAM

1 MEG x 4 DRAM

QUAD CAS PARITY, FAST PAGE MODE

FEATURES

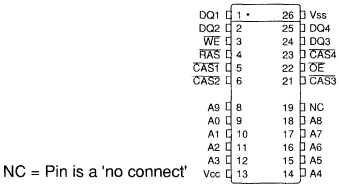
- Four independent $\overline{CAS}$ controls, allowing individual manipulation to each of the four data Input/Output ports (DQ1 through DQ4).
- Offers a single chip solution to byte level parity for 36-bit words when using 1 Meg x 4 DRAMs for memory
- Emulates write-per-bit, at design-in level, with simplified timing constraints
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024-cycle refresh in 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles with $\overline{WE}$ as a don't care

OPTIONS — MARKING

- Timing
  - 70ns access — - 7
  - 80ns access — - 8
  - 100ns access — -10
- Packages
  - Plastic SOJ (300mil) — DJ
  - Plastic SOJ (350mil) — DJW
- Operating Temperature, T_A
  - Commercial (0°C to +70°C) — None

PIN ASSIGNMENT (Top View)

24-Pin SOJ (E-5, E-6)



NC = Pin is a 'no connect'

GENERAL DESCRIPTION

The MT4C4004 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. This 1 Meg x 4 DRAM is unique in that each $\overline{CAS}$ ($\overline{CAS1}$ through $\overline{CAS4}$) controls its corresponding data I/O port in conjunction with $\overline{OE}$ (eg. $\overline{CAS1}$ controls DQ1 I/O port, $\overline{CAS2}$ controls DQ2, $\overline{CAS3}$ controls DQ3 and $\overline{CAS4}$ controls DQ4).

The best way to view the Quad $\overline{CAS}$ function is to imagine the $\overline{CAS}$ inputs going into an AND gate to obtain an internally generated $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on a standard 1 Meg x 4 DRAM device. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$) on the Quad CAS DRAM.

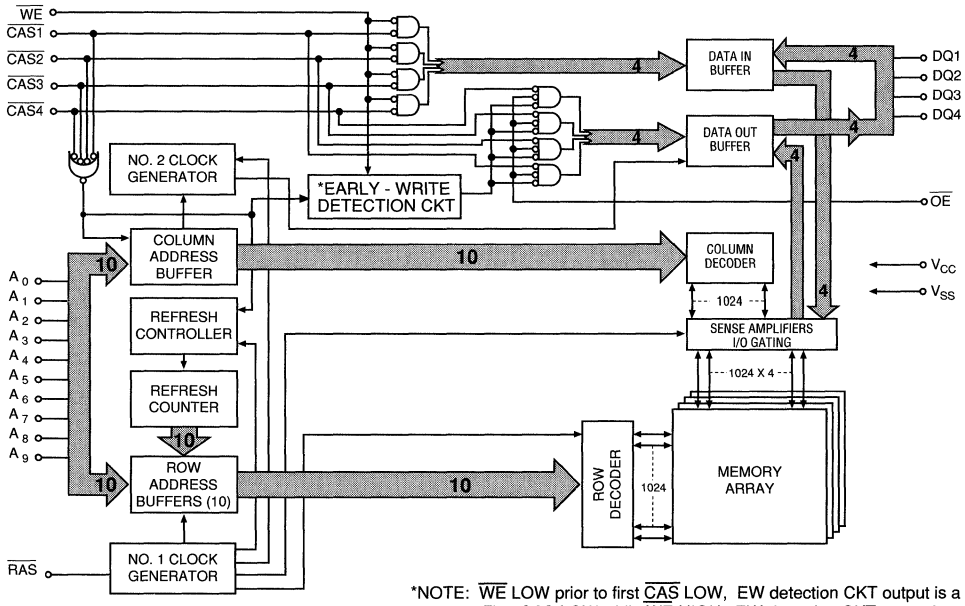
During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits, and the first $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode.

During a WRITE cycle, data-in (Dx) is latched by the falling edge of $\overline{WE}$ or the first $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to the first $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output buffer, data out (Q) is activated and retains the selected cell data until the trailing edge of its corresponding $\overline{CAS}$ occurs (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle ($\overline{OE}$ switching the device from a READ to a WRITE function). The four data inputs and four data outputs are routed through four pins using common I/O, with pin direction controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by the first $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and all four $\overline{CAS}$ controls HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycle will invoke the refresh counter for automatic and sequential row addressing.

FUNCTIONAL BLOCK DIAGRAM
QUAD CAS



*NOTE: $\overline{WE}$ LOW prior to first $\overline{CAS}$ LOW, EW detection CKT output is a 1.
First CAS LOW while $\overline{WE}$ HIGH, EW detection CKT output is a 0,
(OE will now determine I/O).

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CASx}$	$\overline{CASy}$	$\overline{WE}$	$\overline{OE}$	Addresses ^tR	Addresses ^tC	DQx (DQy always High-Z)
Standby		H	X	X	X	X	X	X	High-Z
READ		L	L	H	H	L	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	H	L	X	ROW	COL	Valid Data In
READ-WRITE		L	L	H	H→L	L→H	ROW	COL	Valid Data Out, Data In
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Valid Data Out
PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	H	L	X	ROW	COL	Valid Data In
	2nd Cycle	L	H→L	H	L	X	n/a	COL	Valid Data In
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H	H→L	L→H	ROW	COL	Valid Data Out, Data In
	2nd Cycle	L	H→L	H	H→L	L→H	n/a	COL	Valid Data Out, Data In
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	H	L	X	ROW	COL	Valid Data In
$\overline{RAS}$-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	H	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	26
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC= ^tRC (MIN))	I_{CC3}	100	90	80	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC= ^tPC (MIN))	I_{CC4}	70	60	50	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC= ^tRC (MIN))	I_{CC5}	100	90	80	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC= ^tRC (MIN))	I_{CC6}	100	90	80	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$1-4, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	185		205		220		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		55		ns	31
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		115		ns	31
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	15, 29
Output Enable	^tOE		20		20		25	ns	33
Access time from column address	^tAA		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		50	ns	29
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	27
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	34
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	28
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	16, 32
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	32
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	ns	17, 27
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	28
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	20	50	ns	18
Column address setup time	^tASC	0		0		0		ns	27
Column address hold time	^tCAH	15		15		20		ns	27
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		ns	
Read command setup time	^tRCS	0		0		0		ns	27
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 28
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	29

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

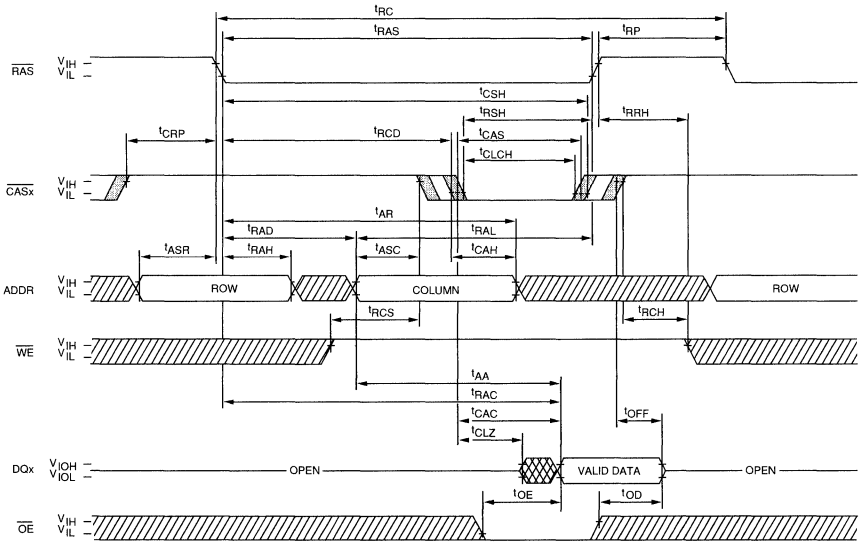
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 29, 38
Output disable	^tOD		20		20		20	ns	34, 38
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21, 27
Write command hold time	^tWCH	15		15		20		ns	36
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	28
Data-in setup time	^tDS	0		0		0		ns	22, 29
Data-in hold time	^tDH	15		15		20		ns	22, 29
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	100		110		130		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		60		ns	21, 27
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5, 27
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5, 28
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		10		ns	30
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		20		ns	37
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN refresh cycle	^tORD	0		0		0		ns	

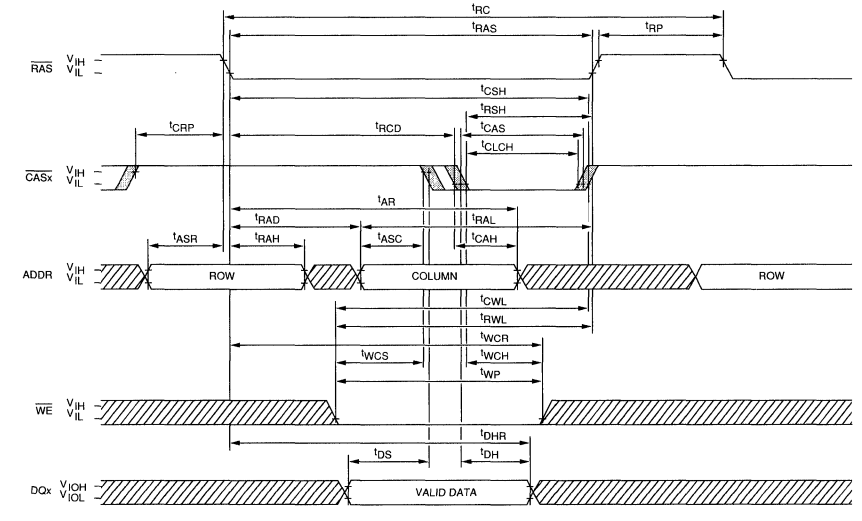
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial 100µs pause is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$x = V_{IH}, data output (Qx) is high impedance.
12. If $\overline{CAS}$x = V_{IL}, Qx may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If at least one $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, all four $\overline{CAS}$ controls must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (max) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in EARLY-WRITE and READ-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-WRITE cycle, and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH})
22. These parameters are referenced to $\overline{CAS}$x leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, READ-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. One to three $\overline{CAS}$ controls may be HIGH throughout any given $\overline{CAS}$ cycle, even though the timing waveforms show all $\overline{CAS}$ controls going LOW. If any one does go LOW, it must meet all the timing requirements listed or the data for that I/O buffer may be invalid. At least one of the four $\overline{CAS}$ controls must be LOW for a valid $\overline{CAS}$ cycle to occur.
26. All other inputs at Vcc -0.2V.
27. The first $\overline{CAS}$x edge to transition LOW.
28. The last $\overline{CAS}$x edge to transition HIGH.
29. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$x input; DQ1 by $\overline{CAS1}$, DQ2 by $\overline{CAS2}$, etc.
30. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
31. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
32. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
33. First DQx controlled by the first $\overline{CAS}$x to go LOW.
34. Last DQx controlled by the last $\overline{CAS}$x to go HIGH.
35. Each $\overline{CAS}$x must meet minimum pulse width.
36. Last $\overline{CAS}$x to go LOW.
37. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If the last $\overline{CAS}$x goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
38. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If the last $\overline{CAS}$x goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$x stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$x remains LOW).

READ CYCLE



EARLY-WRITE CYCLE



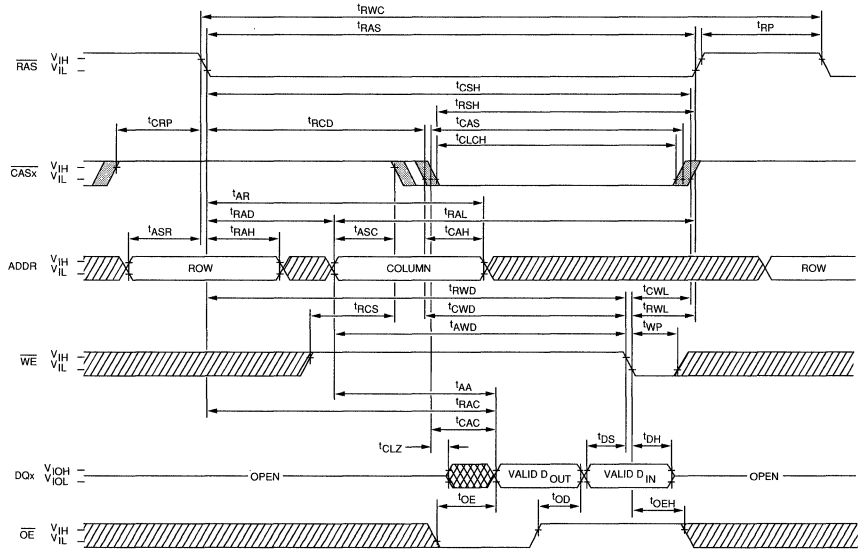
OE = DON'T CARE

DON'T CARE

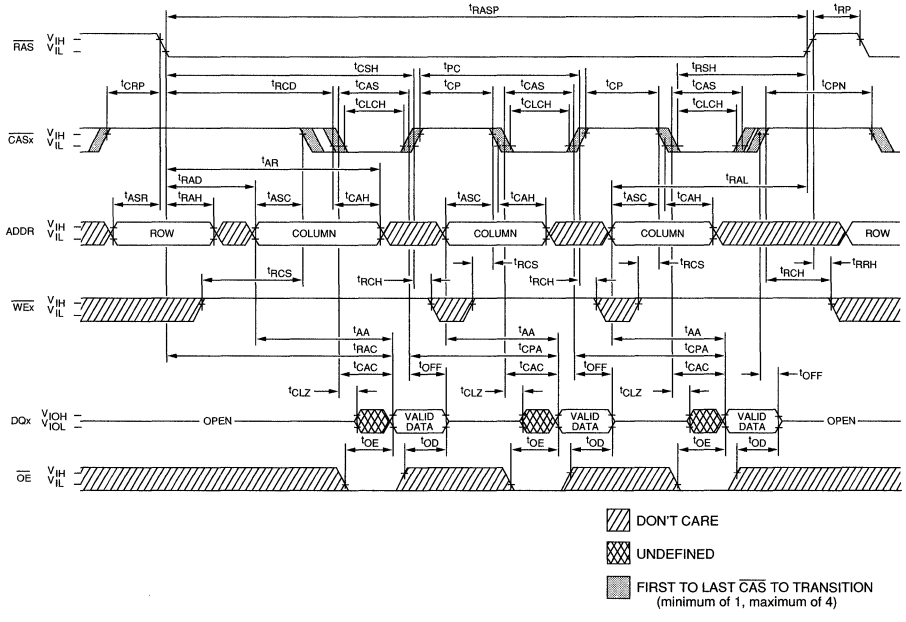
UNDEFINED

FIRST TO LAST $\overline{CAS}$ TO TRANSITION
(minimum of 1, maximum of 4)

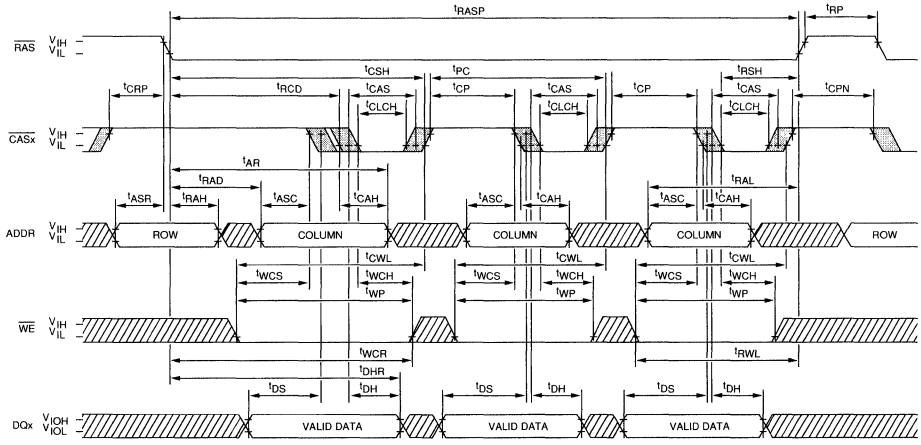
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



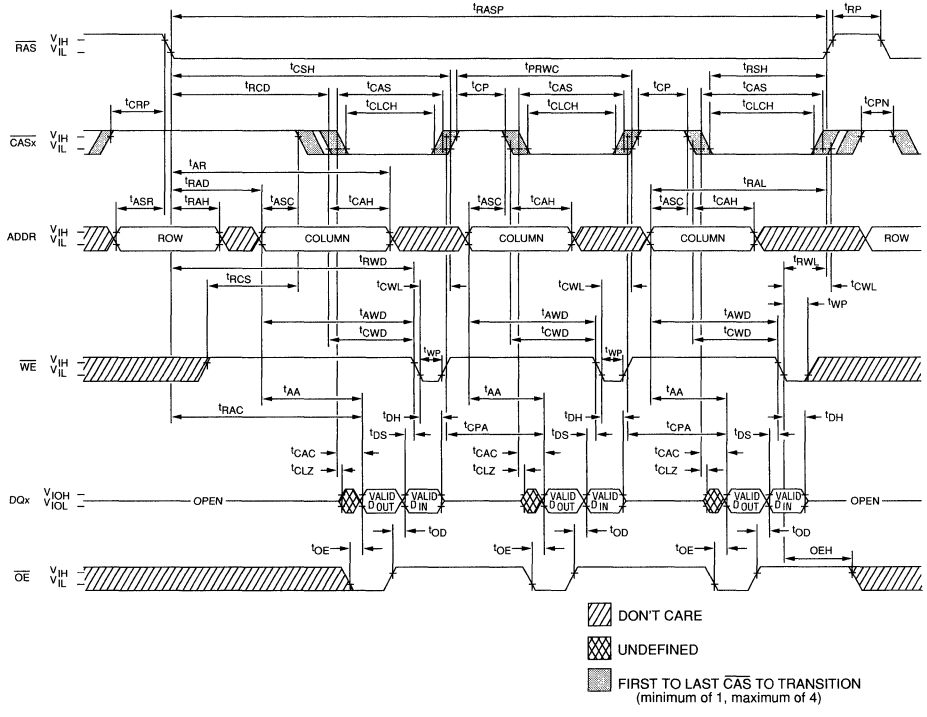
FAST-PAGE-MODE READ CYCLE



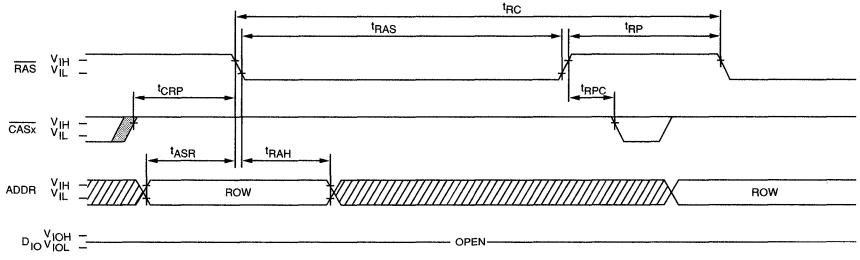
FAST PAGE-MODE EARLY-WRITE CYCLE



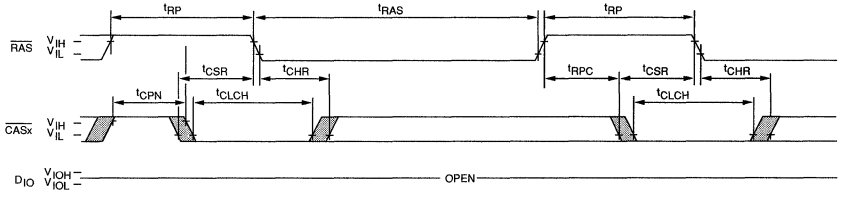
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



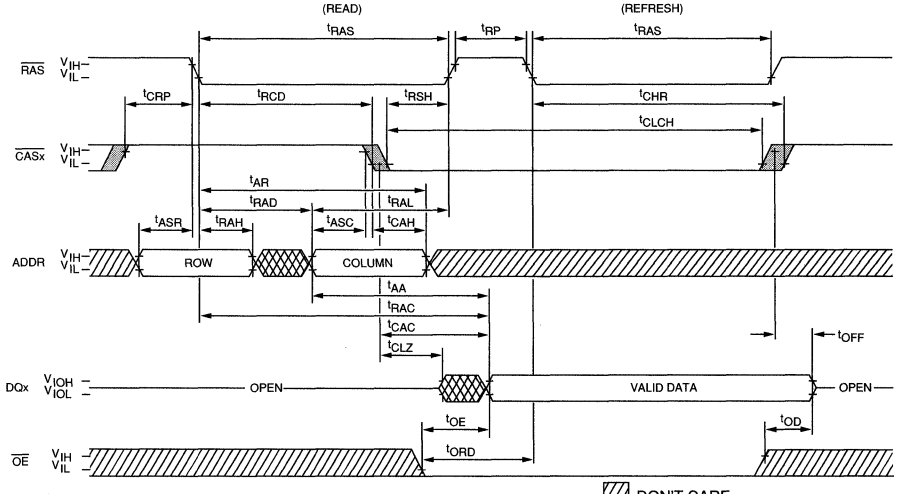
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A_0 - A_8; $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A_0 - A_8, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH, $\overline{OE}$ = LOW) [24]

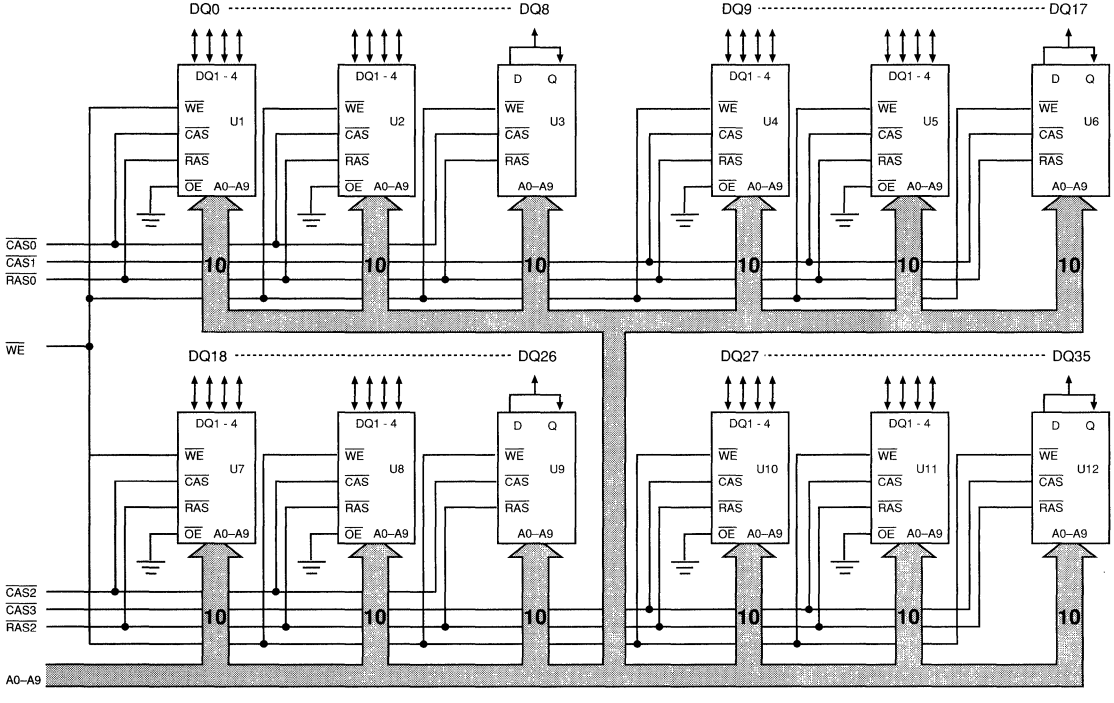


QUAD CAS MODULE UPGRADE

The MT4C4004 (Quad CAS DRAM) was developed to supersede the 1 Meg DRAMs used in the current 1 Meg and 2 Meg x 36 DRAM modules and to add leading-edge CMOS performance. The MT4C4004 is a 1 Meg x 4 CMOS FAST-PAGE-MODE DRAM with four $\overline{CAS}$ input controls. The four individual $\overline{CAS}$ inputs allow each I/O buffer (DQ) to be separately controlled, just as if there were four separate 1 Meg x 1 DRAMs. Most 1 Meg x 1 DRAMs use older CMOS technology and do not have the access speeds of the newer CMOS 4 Meg (1 Meg x 4).

The MT4C4004 will reduce chip count on a x36 module; improving reliability, reducing power consumption and lowering cost. The 1 Meg x 36 will have four 1 Meg x 1 DRAMs replaced by either one or two Quad CAS DRAMs, depending on whether $\overline{RAS0}$ and $\overline{RAS1}$ must be separate or can be connected together. The 2 Meg x 36 will have eight 1 Meg x 1 DRAMs replaced by either two or four Quad CAS DRAMs, depending on whether $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, and $\overline{RAS3}$ must be split or can be connected together.

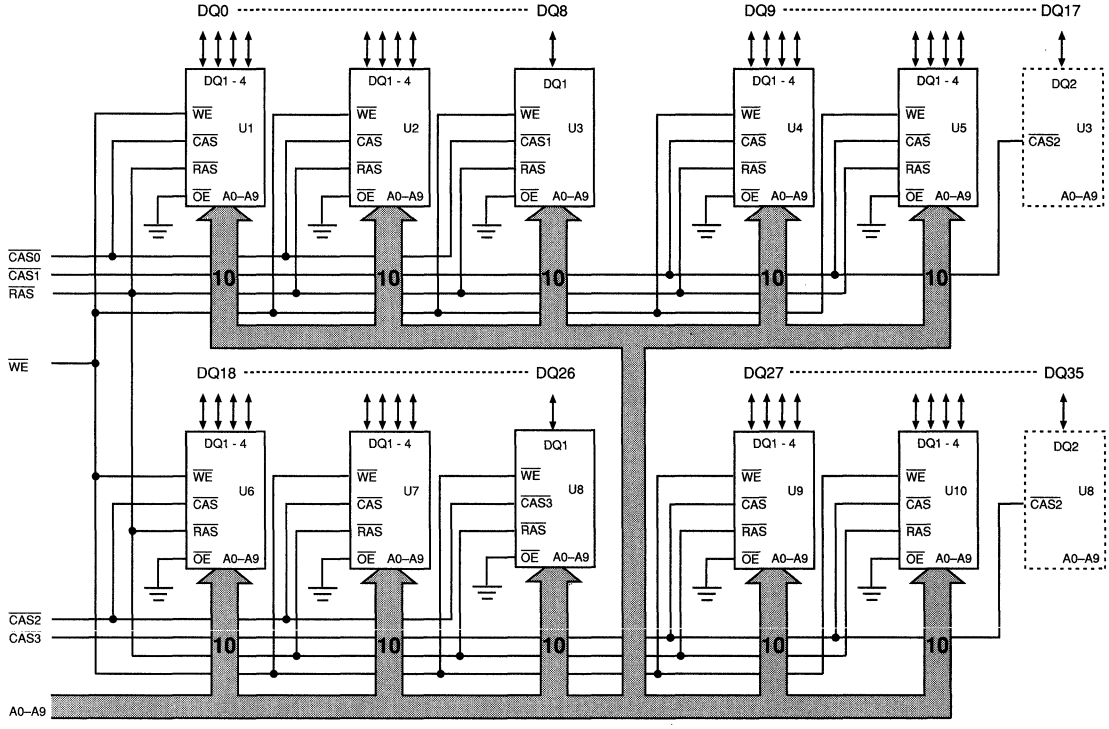
The current 1 Meg x 36 DRAM Module is shown with 256K x 1 DRAMs in Figure 1 below. Figures 2 and 3 show how the same module will be realized with the Quad CAS DRAM for both the split $\overline{RAS}$ (Figure 2) and the common $\overline{RAS}$ (Figure 3) modules.



U1, U2, U4, U5, U7, U8, U10, U11 = MT4C4256DJ
U3, U6, U9, U12 = MT1259EJ

Figure 1
1 MEG x 36 WITH 1 MEG x 1 FOR PARITY BIT

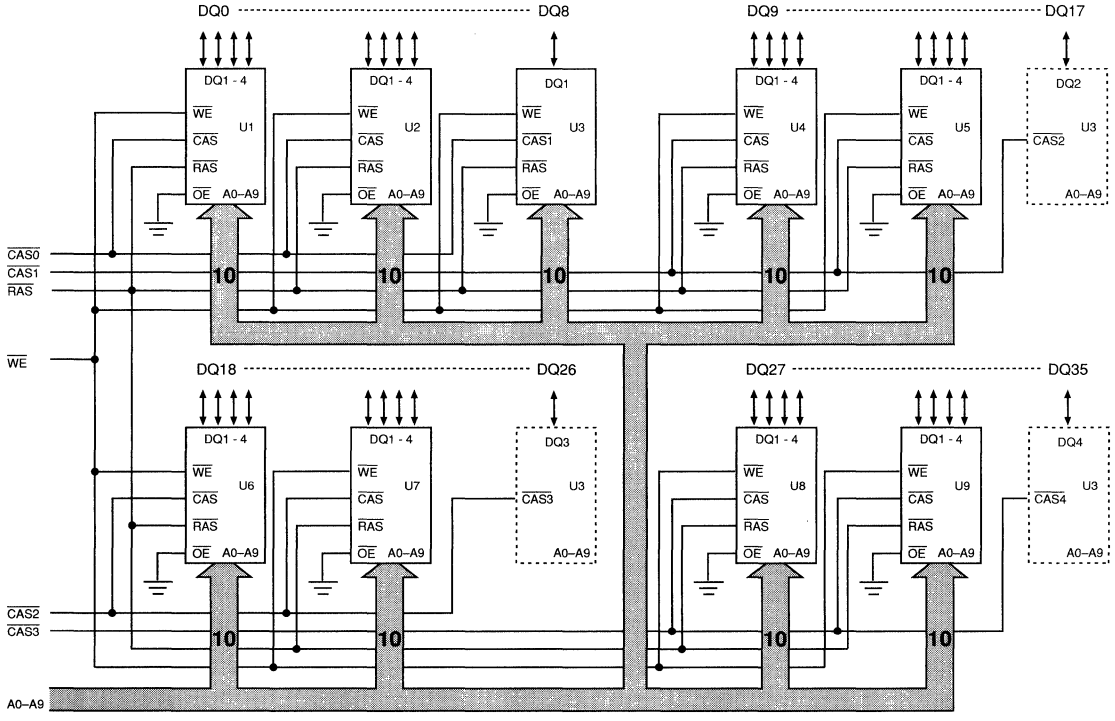
QUAD CAS ENHANCED x36 MODULES



U1, U2, U4, U5, U6, U7, U8, U9 = MT4C4256DJ
U3 = MT4C4259EJ

Figure 2
1 MEG x 36 WITH QUAD $\overline{CAS}$ FOR PARITY BIT AND SPLIT $\overline{RAS}$ CONTROL

QUAD CAS ENHANCED x36 MODULES



U1, U2, U4-U9 = MT4C4256DJ
U3 = MT4C4259EJ

Figure 3
1 MEG x 36 WITH QUAD $\overline{CAS}$ FOR PARITY BIT AND COMMON $\overline{RAS}$ CONTROL

DRAM

1 MEG x 4 DRAM

FAST PAGE MODE, WRITE-PER-BIT

FEATURES

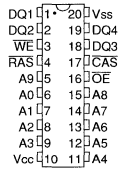
- Industry standard x4 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024-cycle refresh distributed across 16ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), and HIDDEN
- WRITE-PER-BIT access cycle (nonpersistent)
- 300 and 350 mil wide SOJ packages
- Two CBR options: CBR with WE a don't care (1 Meg compatible) and CBR with WE a HIGH (JEDEC test mode capable via WCBR)

OPTIONS / MARKING

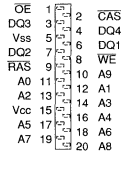
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Ceramic DIP (400mil)	C
Plastic ZIP (350mil)	Z
Plastic SOJ (300mil)	DJ
Plastic SOJ (350mil)	DJW
Plastic TSOP (*)	TG
• CAS-BEFORE-RAS refresh	
CBR with WE a don't care	None
CBR with WE a HIGH	J
• Operating Temperature, TA	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

PIN ASSIGNMENT (Top View)

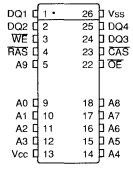
20-Pin CDIP (B-5)



20-Pin ZIP (C-3)



20-Pin SOJ (E-1, E-2)



*Consult factory on availability of TSOP packages

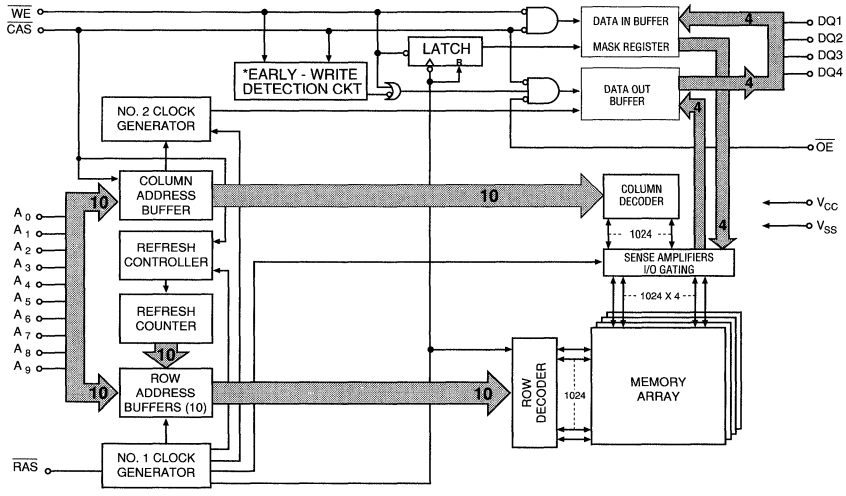
GENERAL DESCRIPTION

The MT4C4005 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin(s), data out (Q) is activated and retains the selected cell data as long as CAS remains low (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE. The WRITE-PER-BIT feature allows the user to define WRITE MASK during a WRITE cycle when RAS goes LOW, depending on the state of WE.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN refresh) so that all 1024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection CKT output is a HIGH (EARLY WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	OE	DATA IN / OUT DQ1-4	NOTES
Standby		H	X	X	X	X	X	High-Z	
READ		L	L	H	ROW	COL	L	Valid Data Out	
EARLY-WRITE		L	L	L	ROW	COL	X	Valid Data In	1
READ-WRITE		L	L	H→L	ROW	COL	L→H	Valid Data Out, Data In	1
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	L	Valid Data Out	
	2nd Cycle	L	H→L	H	n/a	COL	L	Valid Data Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	X	Valid Data In	1
	2nd Cycle	L	H→L	L	n/a	COL	X	Valid Data In	1
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	L→H	Valid Data Out, Data In	1
	2nd Cycle	L	H→L	H→L	n/a	COL	L→H	Valid Data Out, Data In	1
$\overline{RAS}$-ONLY REFRESH		H	X	X	ROW	n/a	X	High-Z	
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	L	Valid Data Out	
	WRITE	L→H→L	L	L	ROW	COL	X	Valid Data In	1
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	Standard	H→L	L	X	X	X	X	High-Z	
	"J" Option	H→L	L	H	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided. Refer to Figure 1.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3, 5

MASKED WRITE ACCESS CYCLE

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ4 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

For nonpersistent MASK WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C4005 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

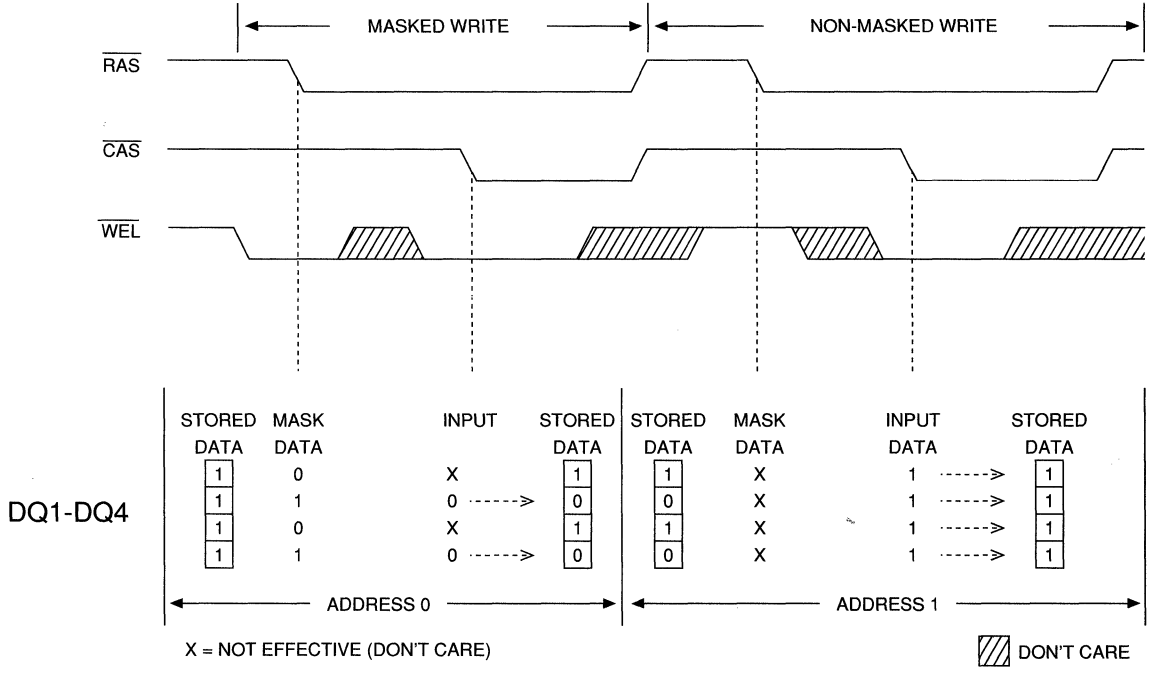


Figure 1
MT4C4005 MASKED WRITE EXAMPLE

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	90		95		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	15
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		40		45	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	21, 27

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

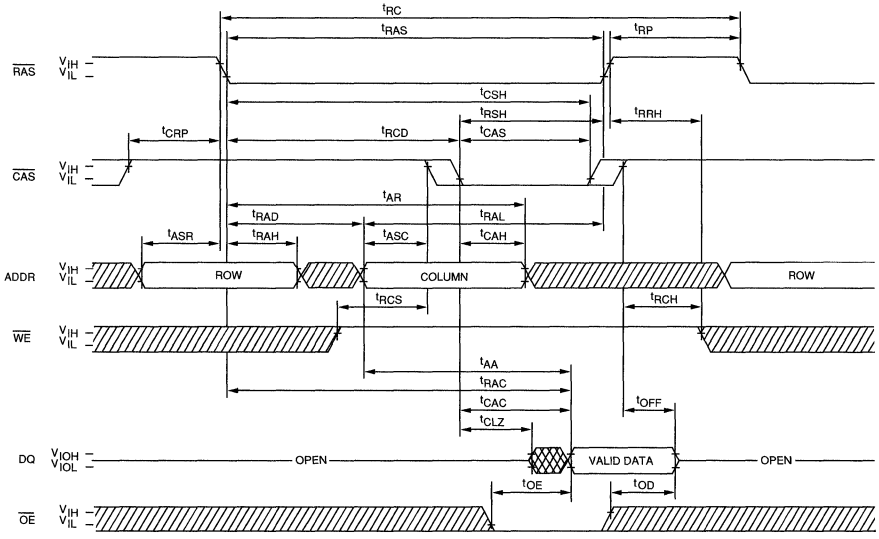
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	90		100		110		ns	21
Column address to $\overline{WE}$ delay time	tAWD	60		65		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	45		50		50		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	5
$\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	10		10		10		ns	25
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	tWTH	10		10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	tWTS	10		10		10		ns	25
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		0		ns	
Output disable	tOD	15		20		20		ns	27
Output enable	tOE	15		20		20		ns	23
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	15		20		20		ns	26
WRITE-PER-BIT setup time	tWBS	0		0		0		ns	
WRITE-PER-BIT hold time	tWBH	10		10		10		ns	
WRITE-PER-BIT mask setup time	tWDS	0		0		0		ns	
WRITE-PER-BIT mask hold time	tWDH	10		10		10		ns	

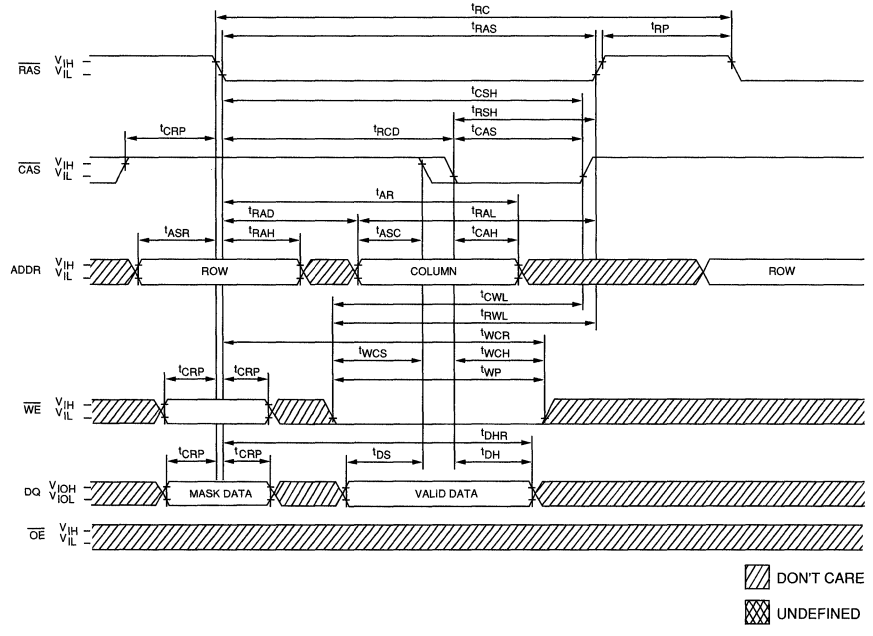
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ${}^{t}T$ = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that ${}^{t}RCD < {}^{t}RCD$ (MAX). If ${}^{t}RCD$ is greater than the maximum recommended value shown in this table, ${}^{t}RAC$ will increase by the amount that ${}^{t}RCD$ exceeds the value shown.
15. Assumes that ${}^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ${}^{t}CPN$.
17. Operation within the ${}^{t}RCD$ (MAX) limit ensures that ${}^{t}RAC$ (MAX) can be met. ${}^{t}RCD$ (MAX) is specified as a reference point only; if ${}^{t}RCD$ is greater than the specified ${}^{t}RCD$ (MAX) limit, then access time is controlled exclusively by ${}^{t}CAC$.
18. Operation within the ${}^{t}RAD$ (MAX) limit ensures that ${}^{t}RCD$ (MAX) can be met. ${}^{t}RAD$ (MAX) is specified as a reference point only; if ${}^{t}RAD$ is greater than the specified ${}^{t}RAD$ (MAX) limit, then access time is controlled exclusively by ${}^{t}AA$.
19. Either ${}^{t}RCH$ or ${}^{t}RRH$ must be satisfied for a READ cycle.
20. ${}^{t}OFF$ (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ${}^{t}WCS$, ${}^{t}RWD$, ${}^{t}AWD$ and ${}^{t}CWD$ are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If ${}^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit through out the entire cycle. If ${}^{t}RWD \geq {}^{t}RWD$ (MIN), ${}^{t}AWD \geq {}^{t}AWD$ (MIN) and ${}^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. ${}^{t}WTS$ and ${}^{t}WTH$ are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ${}^{t}WRP$ and ${}^{t}WRH$ in the CBR refresh cycle.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ${}^{t}OD$ and ${}^{t}OEH$ met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ${}^{t}OEH$ is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once ${}^{t}OD$ or ${}^{t}OFF$ occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

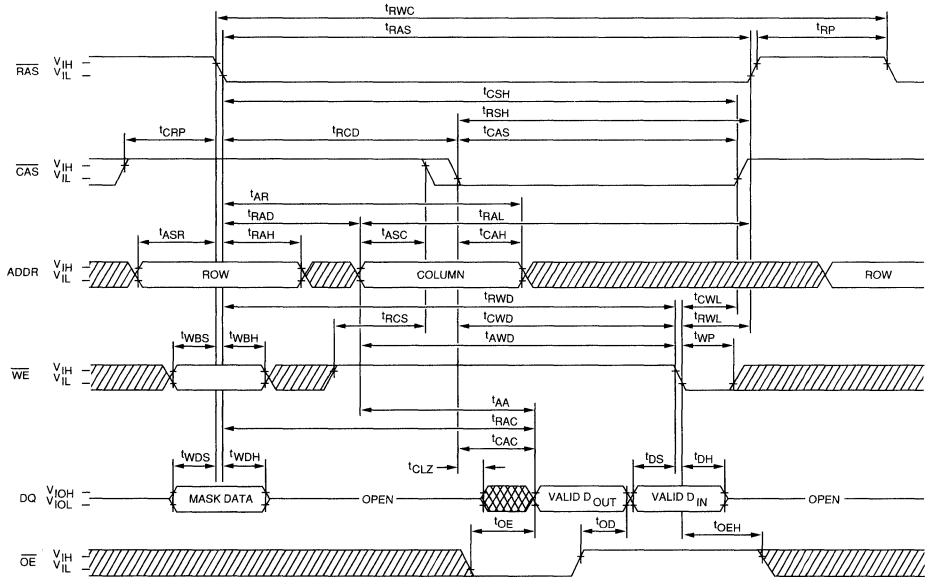
READ CYCLE



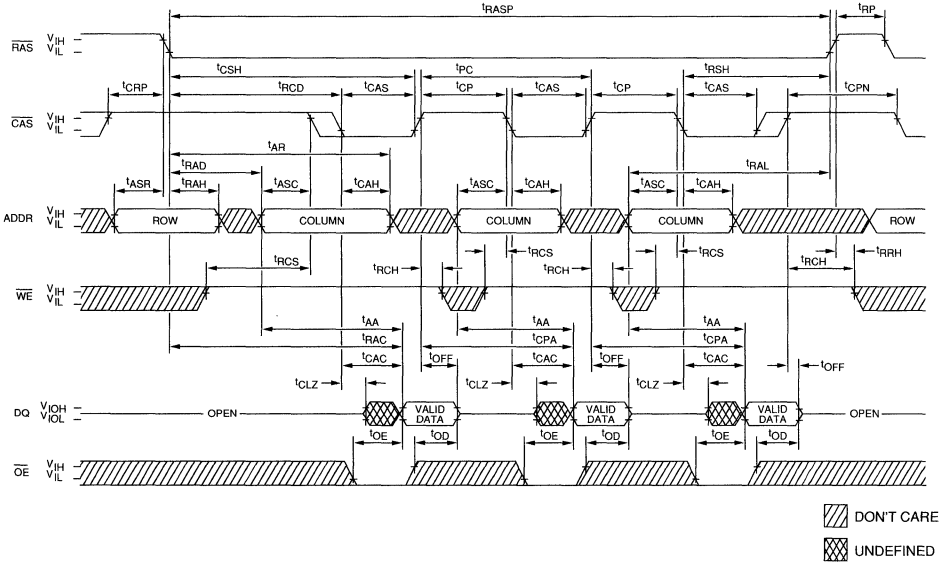
EARLY-WRITE CYCLE



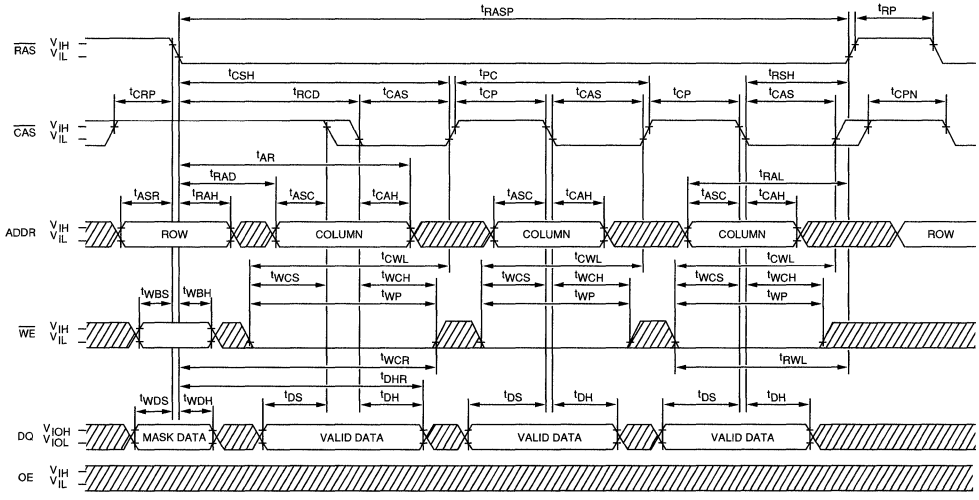
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



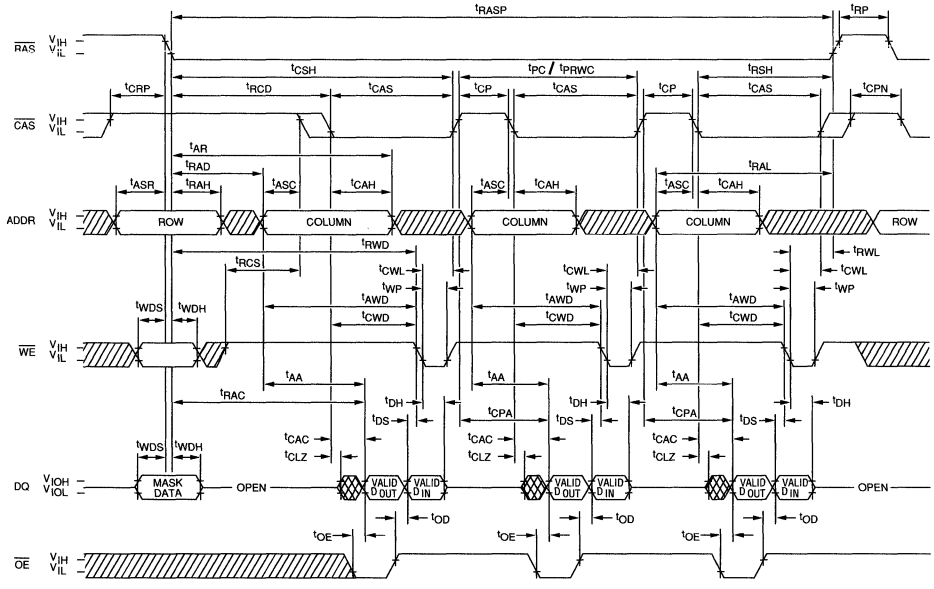
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

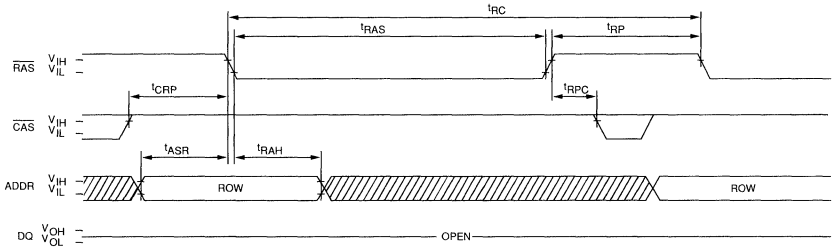


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



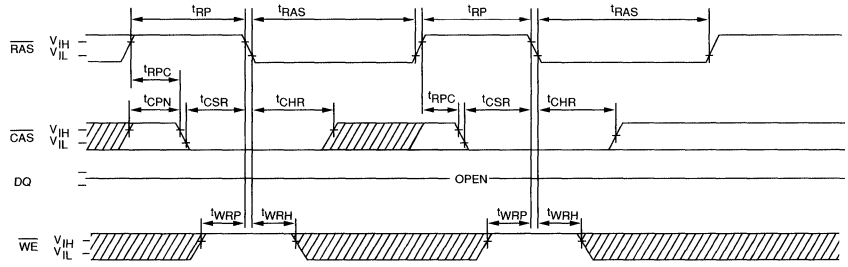
RAS-ONLY REFRESH CYCLE

(ADDR = A_0 - A_9; WE = DON'T CARE)



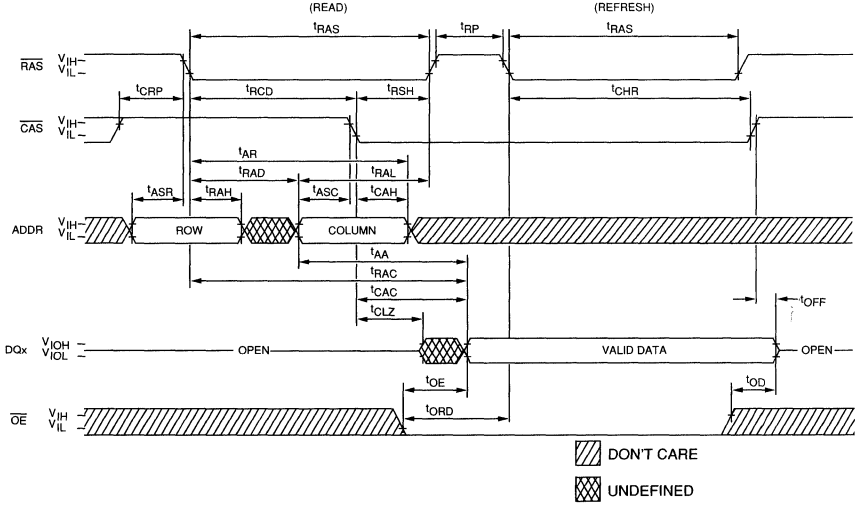
CAS-BEFORE-RAS REFRESH CYCLE

(A_0 - A_9, and OE = DON'T CARE)



HIDDEN REFRESH CYCLE

(WE = HIGH; OE = LOW) [24]



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a don't care. The 4 Meg, on the other hand, specifies the CBR REFRESH mode to be a $\overline{W}$CBR, which is CBR with the $\overline{WE}$ pin held at a logical HIGH level.

The reason for $\overline{W}$CBR instead of CBR on the 4 Meg is that a CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode ($\overline{W}$CBR). In contrast, the 1 Meg test mode is entered by applying a HIGH signal to the test pin (pin 4 on DIP, pin 5 on SOJ and pin 8 on ZIP). This HIGH signal is usually a "supervoltage" (V in ≥ 7.5V) so normal TTL or CMOS HIGH levels will not cause the part to enter the test mode.

POWER-UP

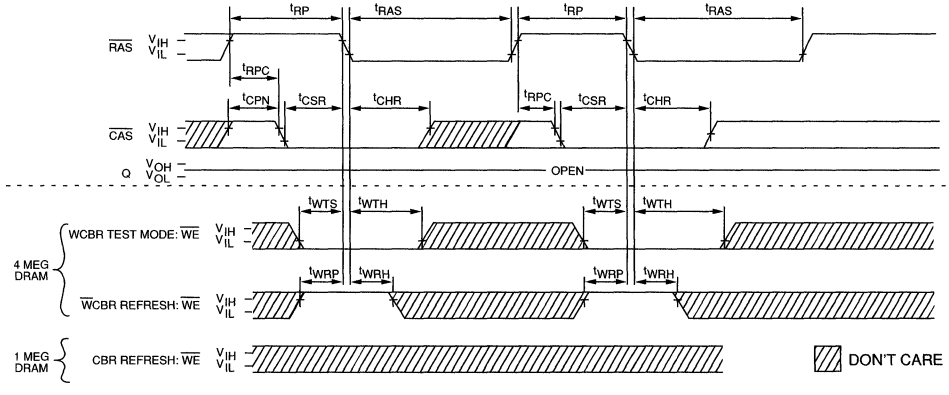
The 4 Meg $\overline{W}$CBR constraint may also introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any 8 $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that 8 $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a $\overline{W}$CBR REFRESH cycle.

SUMMARY

1. The optional 1 Meg test pin is the A10 pin on the 4 Meg (x1 only).
2. For optional test mode, the 1 Meg requires a valid HIGH on the test pin while the 4 Meg requires a CBR cycle with $\overline{WE}$ LOW.
3. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be don't care while the 4 Meg CBR requires $\overline{WE}$ to be HIGH ($\overline{W}$CBR).
4. The 8 $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or $\overline{W}$CBR REFRESH cycles.

SPECIAL FEATURE

A memory system currently using 1 Meg DRAMs with $\overline{WE}$ as a don't care during CBR REFRESH does not allow for direct upgrading to 4 Meg DRAMs. Micron, realizing some companies will have this situation, provides a special feature on its 4 Meg DRAM, that requires "supervoltage" to access the 4 Meg JEDEC WCBR test function. This allows the Micron 4 Meg DRAM to be refreshed in the same manner as any 1 MEG DRAM. Note that the eight power-up cycles should only be refresh cycles in order to guarantee that any 4 Meg DRAM, including Micron's, does not inadvertently power-up in the test mode.



COMPARISON OF 4 MEG TEST MODE AND $\overline{W}$CBR TO 1 MEG CBR

DRAM

4 MEG x 4 DRAM

FAST PAGE MODE: MT4C40004
STATIC COLUMN: MT4C40005

FEATURES

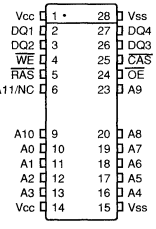
- Industry standard x4 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single power supply : +5V±10% or +3.3V±10%
- Low power, 5mW standby; 250mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), and HIDDEN
- 2048-cycle refresh distributed across 32ms or 4096-cycle refresh distributed across 64ms

OPTIONS MARKING

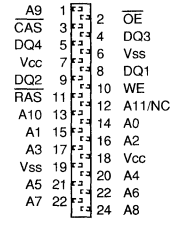
- Timing
  - 50ns access -5
  - 60ns access -6
  - 70ns access -7
  - 80ns access -8
- Packages
  - Plastic ZIP (475mil) Z
  - Plastic SOJ (400mil) DJ
  - Plastic TSOP (*) TG
- Refresh Period
  - 2048 cycles @ 32ms R
  - 4096 cycles @ 64ms None
- Operating Temperature, T_A
  - Commercial (0°C to +70°C) None
  - Industrial (-40°C to +85°C) IT
- Power Supply
  - +5V±10% None
  - +3.3V±10% V

PIN ASSIGNMENT (Top View)

24-Pin SOJ (E-7)



24-Pin ZIP



*Consult factory on availablity of TSOP packages

GENERAL DESCRIPTION

The MT4C40004/5 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 10-12 bits (A0-A11) at a time. $\overline{RAS}$ is used to latch the first 11/12 bits and $\overline{CAS}$ the latter 10/11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pins remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pins, data out (Q), is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A10/11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), or HIDDEN refresh) so that all 2048/4096 combinations of $\overline{RAS}$ addresses (A0-A10/A11) are executed at least every 32ms/64ms, regardless of sequence. The CBR refresh cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

The MT4C40004/5 are available with either 2048 cycles or 4096 cycles of refreshing. If CBR refresh is used, the number of cycles is a "don't care."

DRAM

512K x 8 DRAM

FAST PAGE MODE

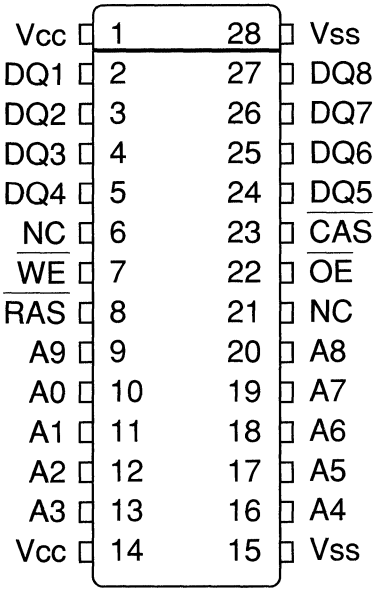
FEATURES

- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 10 row addresses, nine column addresses
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 350mW active, typical
- All device pins are fully TTL and CMOS compatible
- 1024-cycle refresh in 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ and HIDDEN
- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C8513 only)

OPTIONS	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Masked Write	
Not available	MT4C8512
Available	MT4C8513
• Packages	
Plastic SOJ (400mil)	DJ
Plastic TSOP (*)	TG

PIN ASSIGNMENT (Top View)

28-Pin SOJ
(E-9)



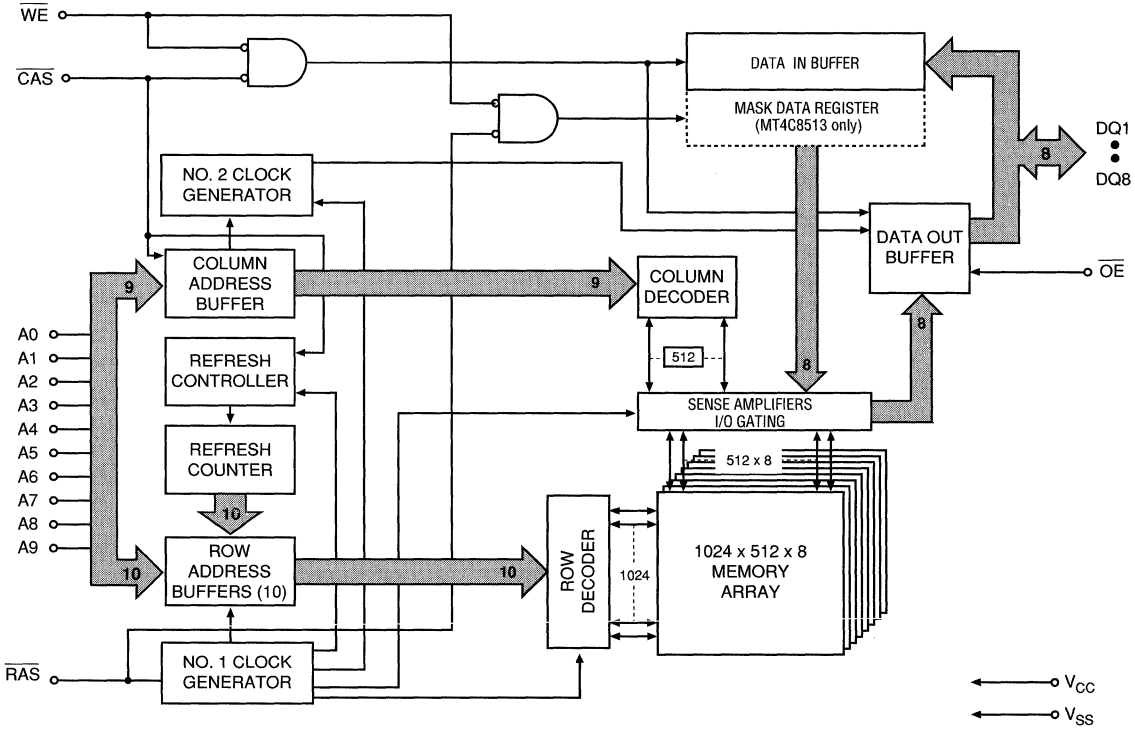
NC = No Connect
*Consult factory for availibilty of TSOP packages

GENERAL DESCRIPTION

The MT4C8512/3 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x8 configuration. Each byte is uniquely addressed through the 19 address bits during READ or WRITE cycles. The address is entered by $\overline{RAS}$ latching the first 10 bits (A0-A9) and $\overline{CAS}$ latching the latter 9 bits (A0-A8).

The MT4C8513 has NONPERSISTENT MASKED WRITE allowing it to perform WRITE-PER-BIT accesses.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits and as a strobe for the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C8513 only).
23	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 9-column address bits, enable the DRAM output buffers, and as a strobe for the data inputs on WRITE cycles.
7	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a Mask Enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED-WRITE cycle (MT4C8513).
22	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a high-impedance state.
10-13, 16-20, 9	A0 to A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 512K available words.
2-5, 24-27	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or high-impedance and/or Output masked data input (for MASKED WRITE cycle only).
6	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	Vcc	Supply	Power Supply: +5V ± 10%
15, 28	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 19 address bits during READ or WRITE cycles. $\overline{RAS}$ is used to latch the first ten bits (A0-A9) and $\overline{CAS}$ the latter nine bits (A0-A8).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

MASKED WRITE ACCESS CYCLE (MT4C8513 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C8513 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

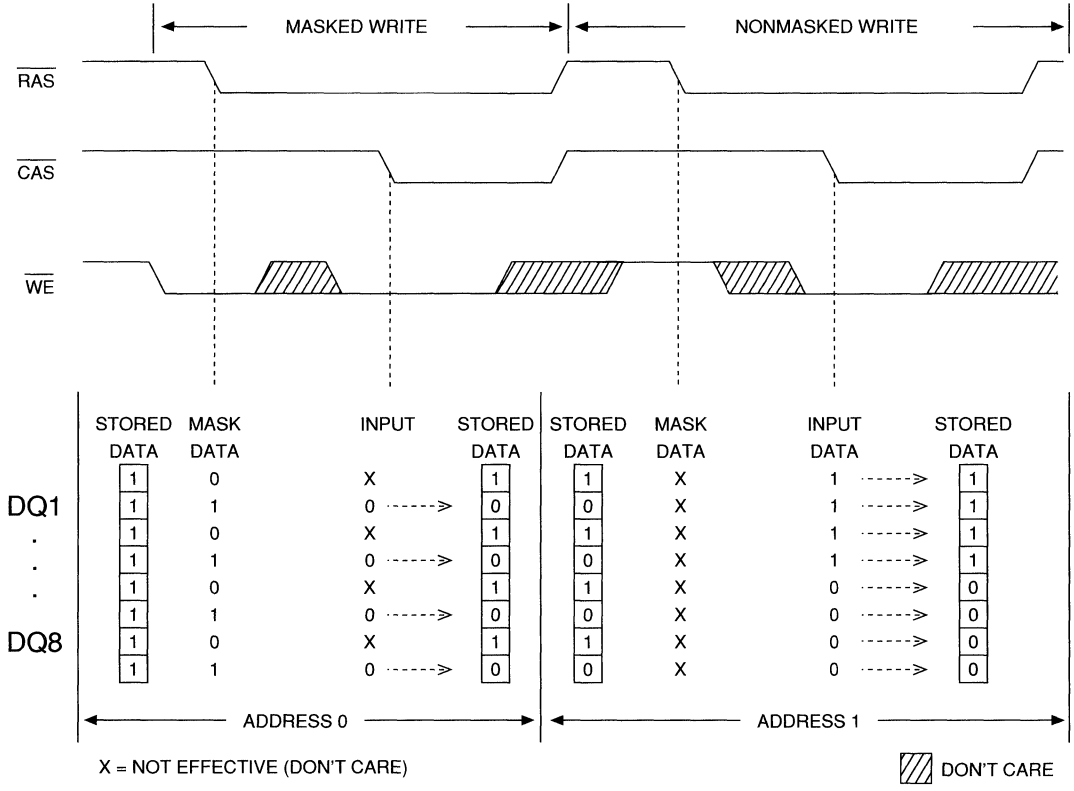


Figure 1
MT4C8513 MASKED WRITE EXAMPLE

TRUTH TABLE

Function		RAS	CAS	WE	OE	Addresses tR	Addresses tC	DQs	NOTES
Standby		H	X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Valid Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Valid Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Valid Data Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Valid Data Out	
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Valid Data In	1
	2nd Cycle	L	H→L	L	X	n/a	COL	Valid Data In	1
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Valid Data Out, Data In	1
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Valid Data Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Valid Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data In will be dependent on the mask provided (MT4C8513 only). Refer to Figure 1.
2. EARLY WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ Vcc, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$,$\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		145		170		ns	
READ-WRITE cycle time	t_{RWC}	175		185		220		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		45		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	95		100		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Output Enable time	t_{OE}		20		20		25	ns	
Access time from column address	t_{AA}		35		40		45	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		55		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	25	65	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

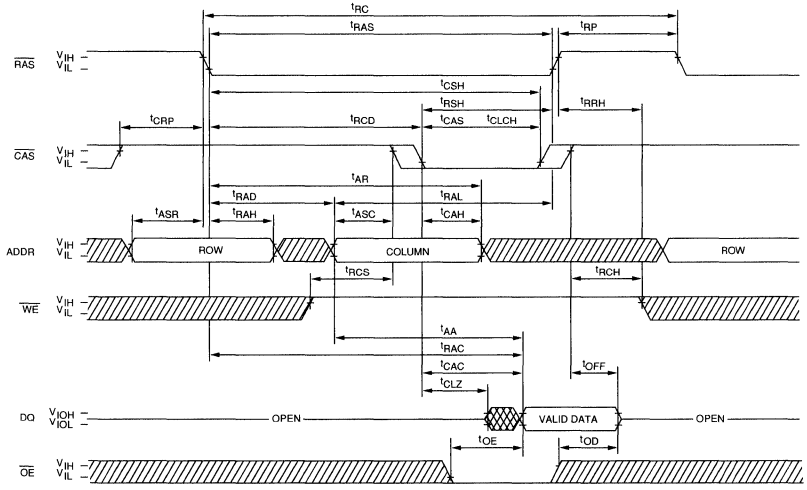
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	15	0	15	0	20	ns	20, 29
Output disable time	^tOD		10		12		20	ns	29
Write command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	15		15		15		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	50		55		65		ns	26
Write command pulse width	^tWP	10		10		15		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	50		55		65		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		125		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	60		65		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		45		60		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	10		10		10		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26, 27
MASKED WRITE command to $\overline{RAS}$ hold time	^tWRH	10		10		15		ns	26, 27
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ hold time	^tMH	10		10		15		ns	26, 27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	10		10		20		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	

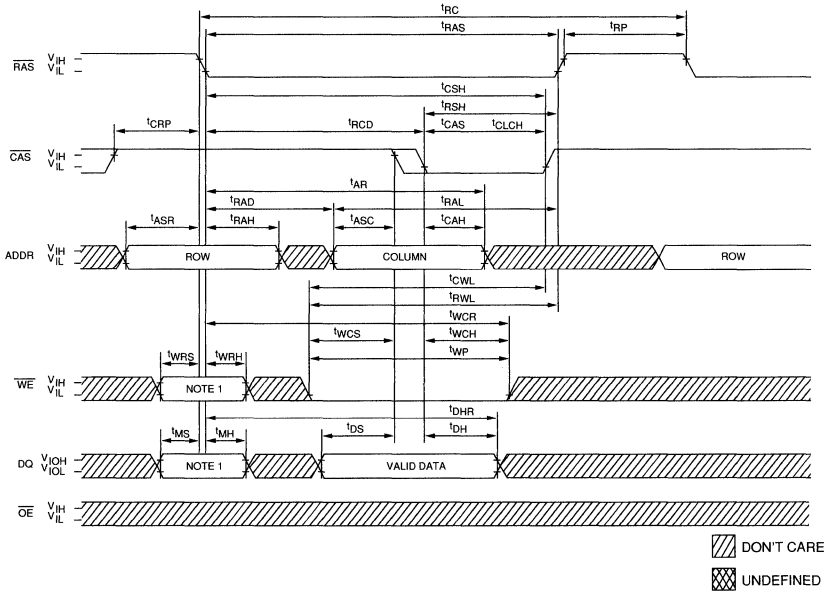
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V; V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ -ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 50pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C8513 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

READ CYCLE

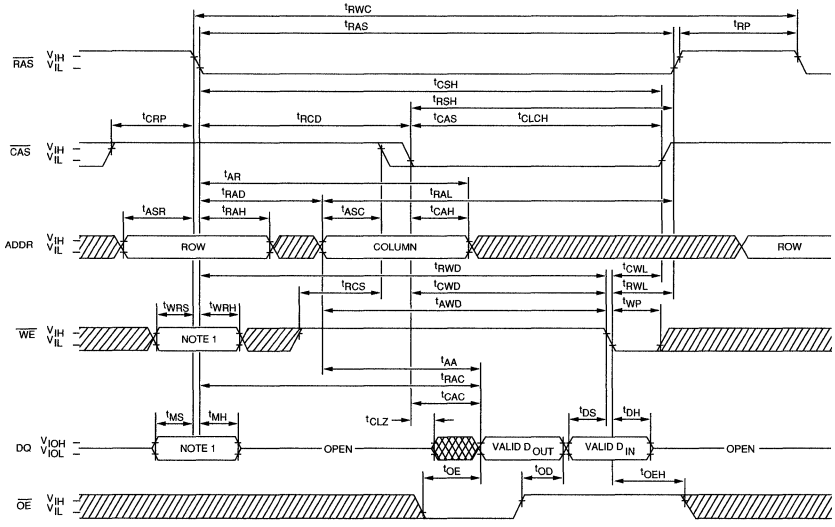


EARLY-WRITE CYCLE

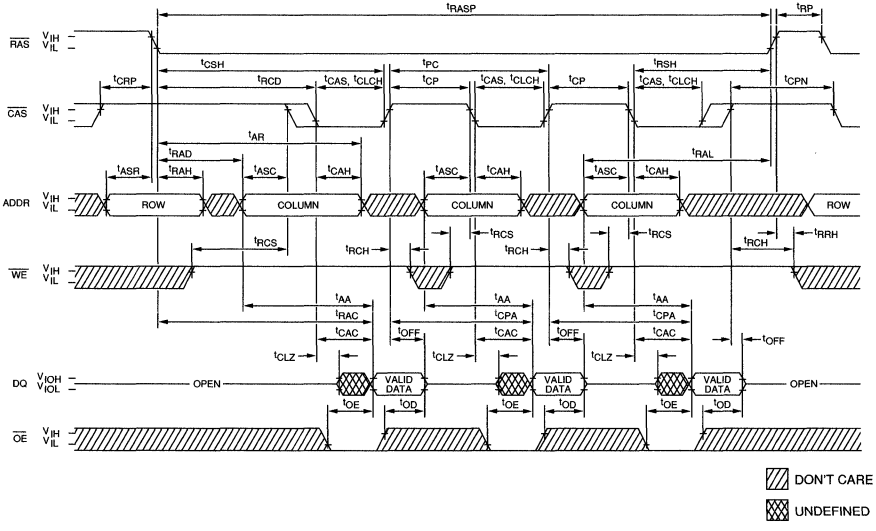


NOTE: 1. Applies to MT4C8513 only; $\overline{WE}$ and DQ inputs on MT4C8512 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

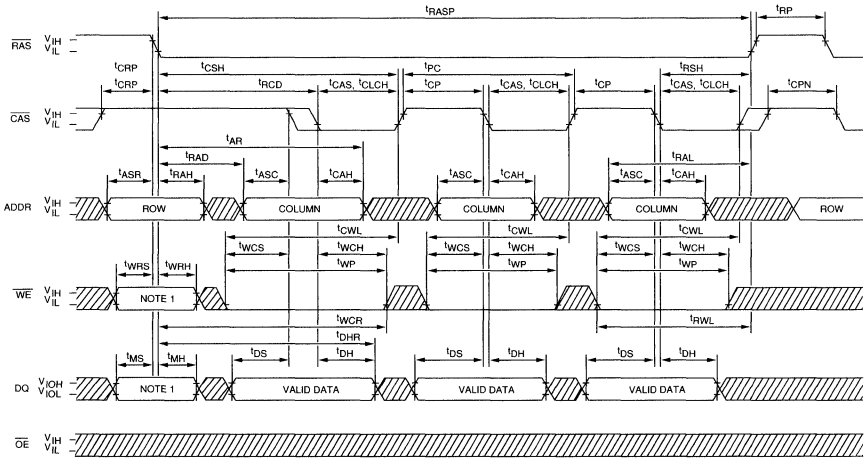


FAST-PAGE-MODE READ CYCLE

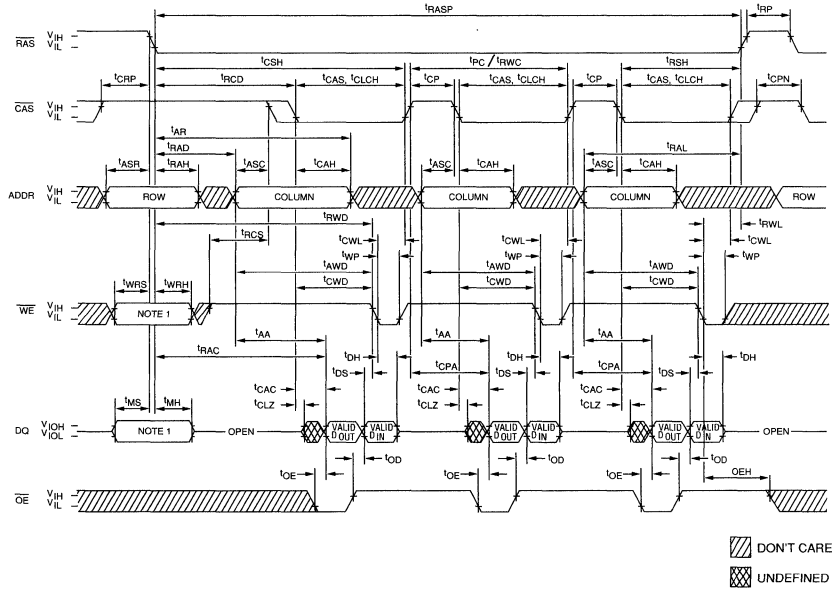


NOTE: 1. Applies to MT4C8513 only; $\overline{WE}$ and DQ inputs on MT4C8512 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

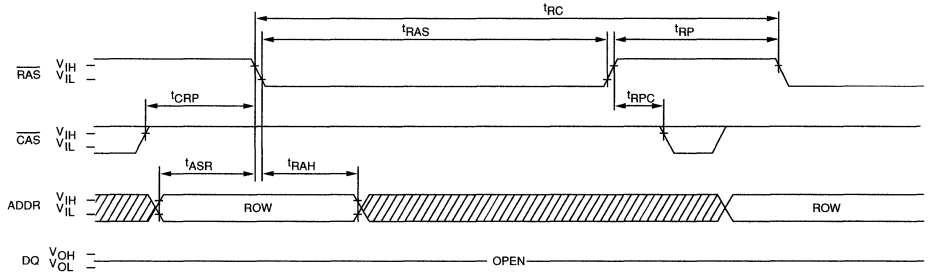


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

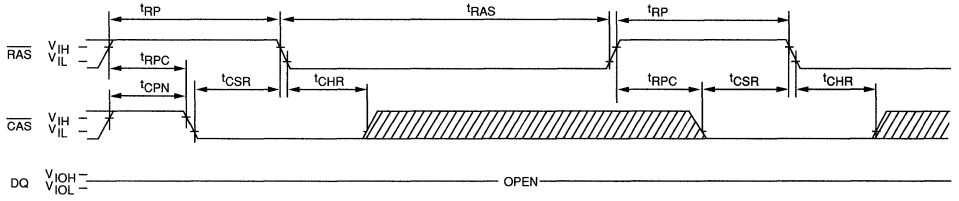


NOTE: 1. Applies to MT4C8513 only; $\overline{WE}$ and DQ inputs on MT4C8512 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

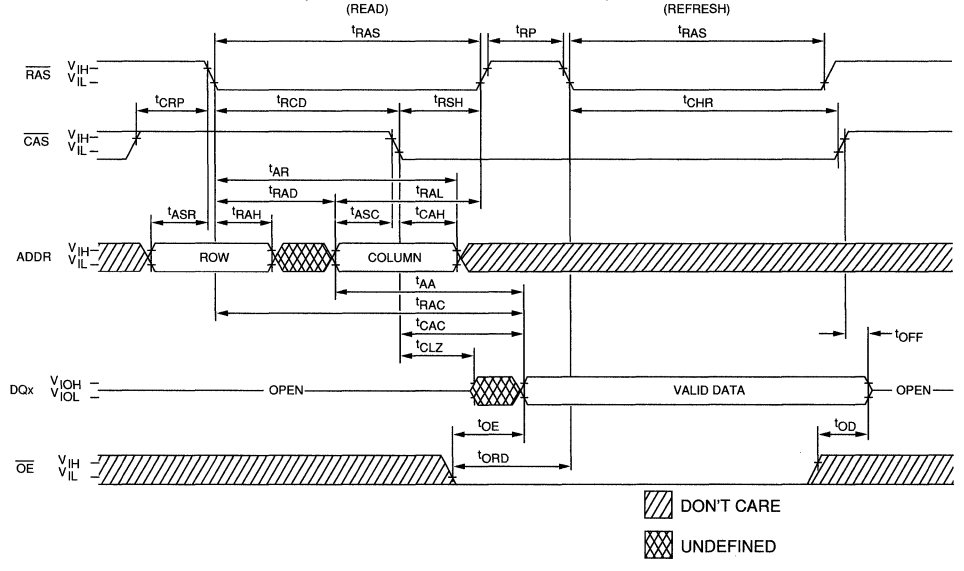
RAS-ONLY REFRESH CYCLE
($\overline{OE}$ and $\overline{WE}$ = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A_0 - A_8; $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW) [24]



DRAM

64K x 16 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All device pins are fully TTL and CMOS compatible
- 256-cycle refresh in 4ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ and HIDDEN
- Optional FAST PAGE MODE access cycle
- 2 TTL Load output drive capability
- BYTE WRITE access cycle (MT4C1664 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1665 only)

OPTIONS / MARKING

• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Write Enable	
Byte or Word	MT4C1664
Word only	MT4C1665
• Mask Enable	
Not Available	MT4C1664
Always Available	MT4C1665
• Packages	
Plastic SOJ (400mil)	DJ
Plastic ZIP (450mil)	Z

PIN ASSIGNMENT (Top View)

40-Pin SOJ (E-12)

Vcc	1	40	Vss
DQ1	2	39	DQ16
DQ2	3	38	DQ15
DQ3	4	37	DQ14
DQ4	5	36	DQ13
DQ5	6	35	DQ12
DQ6	7	34	DQ11
DQ7	8	33	DQ10
DQ8	9	32	DQ9
NC	10	31	NC
Vcc	11	30	Vss
*NC/$\overline{WEH}$	12	29	$\overline{CAS}$
*$\overline{WE}$/$\overline{WEL}$	13	28	$\overline{OE}$
$\overline{RAS}$	14	27	**NC
A0	15	26	NC
A1	16	25	NC
A2	17	24	A7
A3	18	23	A6
A4	19	22	A5
Vcc	20	21	Vss

40-Pin Zip (C-6)

NC	1	2	DQ9
DQ10	3	4	DQ11
DQ12	5	6	DQ13
DQ14	7	8	DQ15
DQ16	9	10	Vss
DQ1	11	12	DQ2
Vcc	13	14	DQ3
DQ4	15	16	DQ5
DQ6	17	18	DQ7
DQ8	19	20	NC
Vcc	21	22	*NC/$\overline{WEH}$
*$\overline{WE}$/$\overline{WEL}$	23	24	$\overline{RAS}$
A0	25	26	A1
A2	27	28	A3
A4	29	30	Vcc
NC	31	32	NC
Vss	33	34	A5
A6	35	36	A7
**NC	37	38	$\overline{OE}$
$\overline{CAS}$	39	40	Vss

* MT4C1665/MT4C1664
** NC = No Connect

GENERAL DESCRIPTION

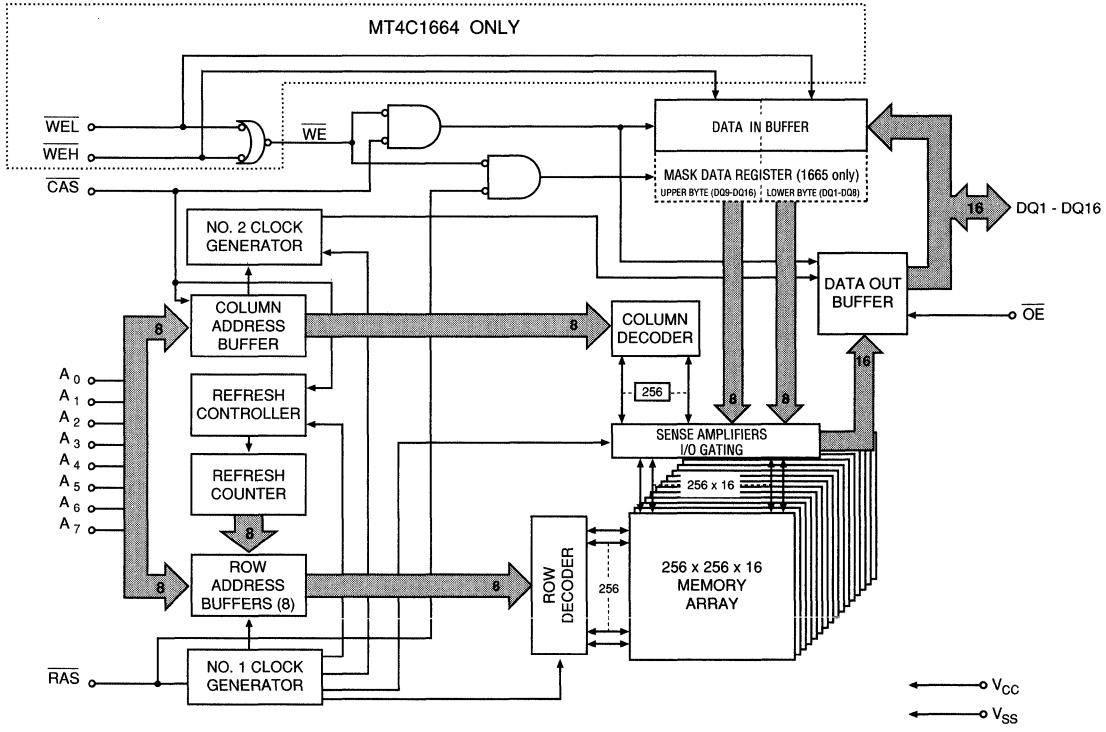
The MT4C1664/5 are randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1664 has both BYTE and WORD WRITE access cycles while the MT4C1665 has only WORD WRITE access cycles.

The MT4C1664 functions in a similar manner to the MT4C1665 except that replacing $\overline{WE}$ with $\overline{WEL}$ and $\overline{WEH}$ allows for BYTE WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an identical manner to $\overline{WE}$: either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$ through an AND gate (Inverted NOR gate).

The MT4C1664 "$\overline{WE}$" function and timing are determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1665 has NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBER(S)	ZIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
14	24	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to clock in the 8 row address bits and as a strobe for the $\overline{WEL}$, $\overline{WEH}$ and DQ inputs for the MASKED WRITE function.
29	39	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 8 column address bits, enable the DRAM output buffers, and as a strobe for the data inputs on WRITE cycles.
28	38	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WEL}$ and $\overline{WEH}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a high impedance state.
13	23	$\overline{WE}$/$\overline{WEL}$*	Input	WRITE Enable Lower Byte: $\overline{WEL}$ on MT4C1664 is $\overline{WE}$ control for the DQ1 through DQ8 inputs. $\overline{WE}$ on MT4C1665 controls DQ1 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a high impedance state (byte WRITE cycle only).
12	22	NC/$\overline{WEH}$*	Input	Write Enable Upper Byte: $\overline{WEH}$ on MT4C1664 is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1665 as it has only WORD WRITE access cycles.
15, 16, 17 18, 19, 22 23, 24	25, 26, 27 28, 29, 34 35, 36	A0 to A7	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 64K available words.
2, 3, 4, 5, 6 7, 8, 9, 32, 33 34, 35, 36 37, 38, 39	11, 12, 14 15, 16, 17 2, 18, 19, 3 4, 5, 6, 7, 8 9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ or $\overline{WEH}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM location. All sixteen I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25, 26 27, 31	1, 20, 31 32, 37	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	Vcc	Supply	Power Supply: +5V ± 10%
21, 30, 40	10, 33, 40	Vss	Supply	Ground

NOTE: *MT4C1665/MT4C1664

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 address bits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. $\overline{RAS}$ is used to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits.

READ or WRITE cycles on the MT4C1665 are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C1664. The MT4C1664 "$\overline{WE}$" function is determined by the first byte WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C1664) or $\overline{WE}$ (MT4C1665).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 256 combinations of $\overline{RAS}$ addresses (A0-A7) are executed at least every 4ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BYTE WRITE DESCRIPTION (MT4C1664 ONLY)

The byte WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$. Enabling $\overline{WEL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{WEH}$ will select an upper BYTE WRITE (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ selects a WIRD WRITE cycle.

The MT4C1664 can be viewed as two 64K x 8 DRAMs which have common input controls, with the exception of the WE input. Figure 1 illustrates the MT4C1664 BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1665 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C1665 is only word selectable when $\overline{WE}$ is LOW at $\overline{RAS}$ time (the MT4C1664 does not have MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1665* MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

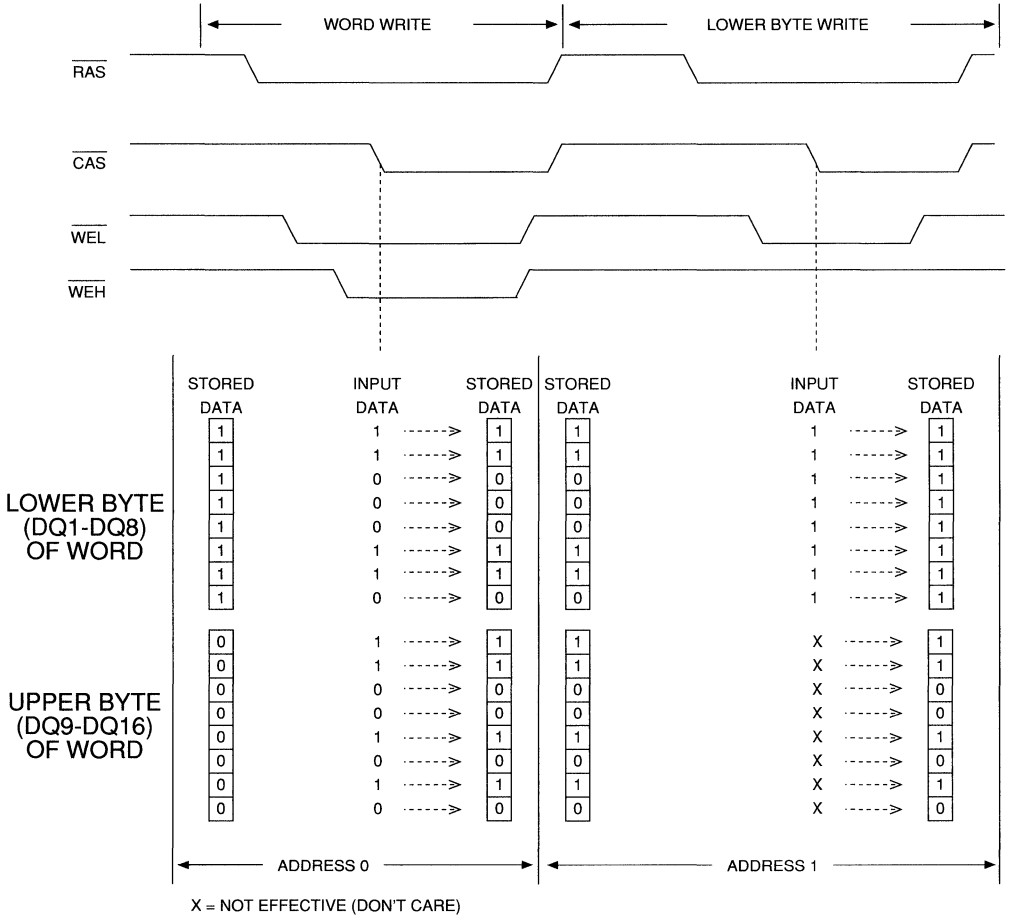


Figure 1
MT4C1664 WORD AND BYTE WRITE EXAMPLE

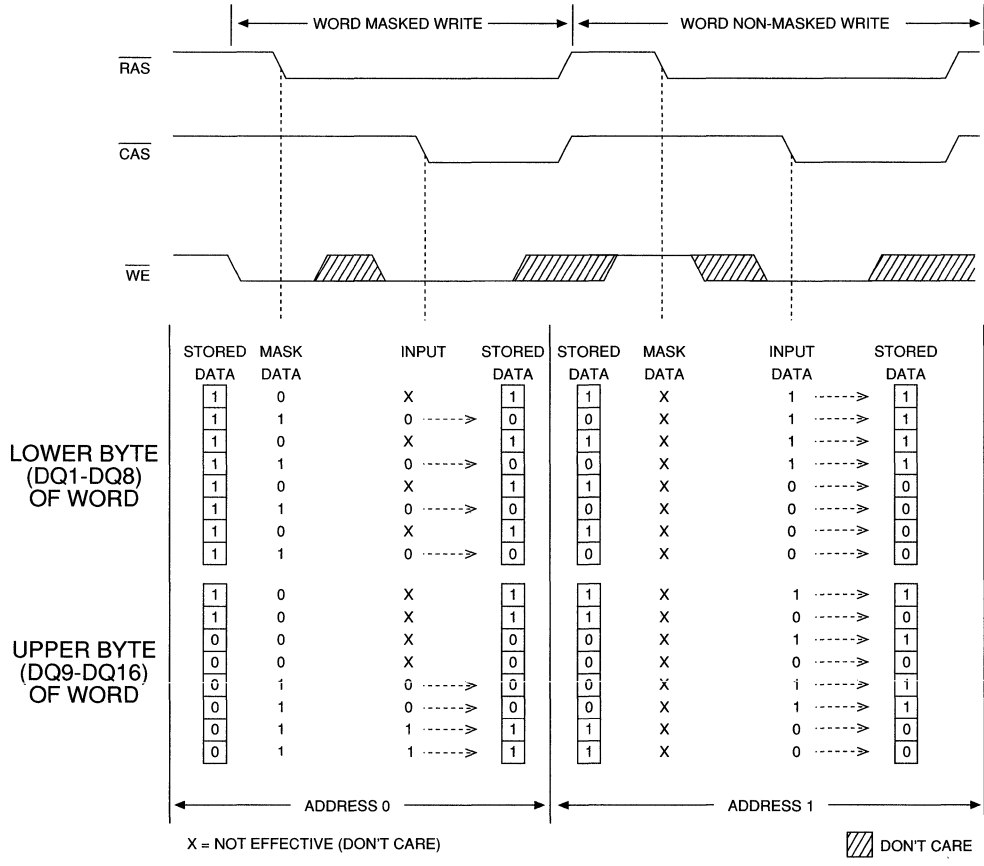


Figure 2
MT4C1665 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1664

Function		RAS	CAS	WEL	WEH	OE	Addresses tR	Addresses tC	DQs	NOTES
Standby		H	X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Valid Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Valid Data In	
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Valid Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Valid Data In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Valid Data Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Valid Data Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Valid Data In	1
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Valid Data In	1
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Valid Data Out, Data In	1
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Valid Data Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Valid Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be byte WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.

TRUTH TABLE: MT4C1665

Function		RAS	CAS	WE	OE	Addresses tR	Addresses tC	DQs	NOTES
Standby		H	X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Valid Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	X	ROW	COL	Valid Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Valid Data Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Valid Data Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Valid Data In	1
	2nd Cycle	L	H→L	L	X	n/a	COL	Valid Data In	1
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Valid Data Out, Data In	1
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Valid Data Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Valid Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data In will be dependent on the mask provided. Refer to Figure 2.
2. EARLY-WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ Vcc, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3, 5

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$,($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($0°C \le T_A \le +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		145		170		ns	
READ-WRITE cycle time	t_{RWC}	175		185		220		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	45		50		60		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	95		100		120		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		25		30	ns	15
Output Enable time	t_{OE}		20		25		30	ns	
Access time from column address	t_{AA}		40		45		50	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		50		55	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		55		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	100,000	30	100,000	30	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	25	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

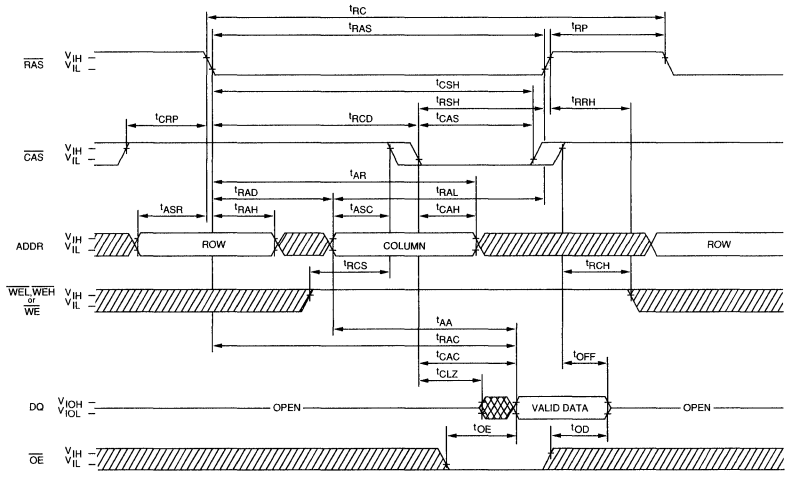
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($0°C \leq T_A \leq +70°C$; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 30
Output disable time	^tOD		10		12		20	ns	30
Write command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	15		15		15		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	50		55		65		ns	26
Write command pulse width	^tWP	15		15		15		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	50		55		65		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		125		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		70		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	^tREF		4		4		4	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26, 27
MASKED WRITE command to $\overline{RAS}$ hold time	^tWRH	15		15		15		ns	26, 27
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	10		10		20		ns	29
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	

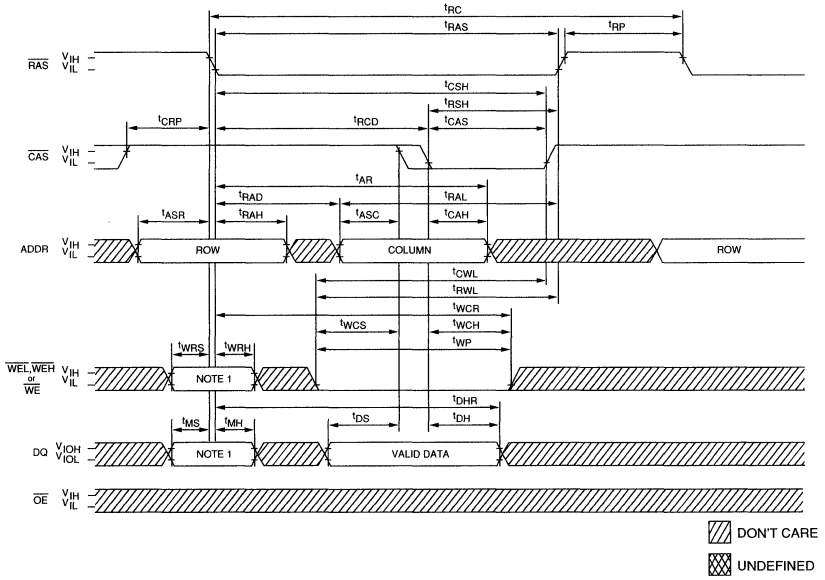
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V; V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ${}^tT$ = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 50pF.
14. Assumes that ${}^tRCD < {}^tRCD$ (MAX). If ${}^tRCD$ is greater than the maximum recommended value shown in this table, ${}^tRAC$ will increase by the amount that ${}^tRCD$ exceeds the value shown.
15. Assumes that ${}^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ${}^tCPN$.
17. Operation within the ${}^tRCD$ (MAX) limit ensures that ${}^tRAC$ (MAX) can be met. ${}^tRCD$ (MAX) is specified as a reference point only; if ${}^tRCD$ is greater than the specified ${}^tRCD$ (MAX) limit, then access time is controlled exclusively by ${}^tCAC$.
18. Operation within the ${}^tRAD$ (MAX) limit ensures that ${}^tRCD$ (MAX) can be met. ${}^tRAD$ (MAX) is specified as a reference point only; if ${}^tRAD$ is greater than the specified ${}^tRAD$ (MAX) limit, then access time is controlled exclusively by ${}^tAA$.
19. Either ${}^tRCH$ or ${}^tRRH$ must be satisfied for a READ cycle.
20. ${}^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ${}^tWCS$, ${}^tRWD$, ${}^tAWD$ and ${}^tCWD$ are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ${}^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^tRWD \ge {}^tRWD$ (MIN), ${}^tAWD \ge {}^tAWD$ (MIN) and ${}^tCWD \ge {}^tCWD$ (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C1664. Write command is defined as $\overline{WE}$ going LOW on the MT4C1665.
27. Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
28. The refresh period may be extended to 8ms without experiencing problems.
29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ${}^tOD$ and ${}^tOEH$ met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ${}^tOEH$ is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
30. The DQs open during READ cycles once ${}^tOD$ or ${}^tOFF$ occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

READ CYCLE

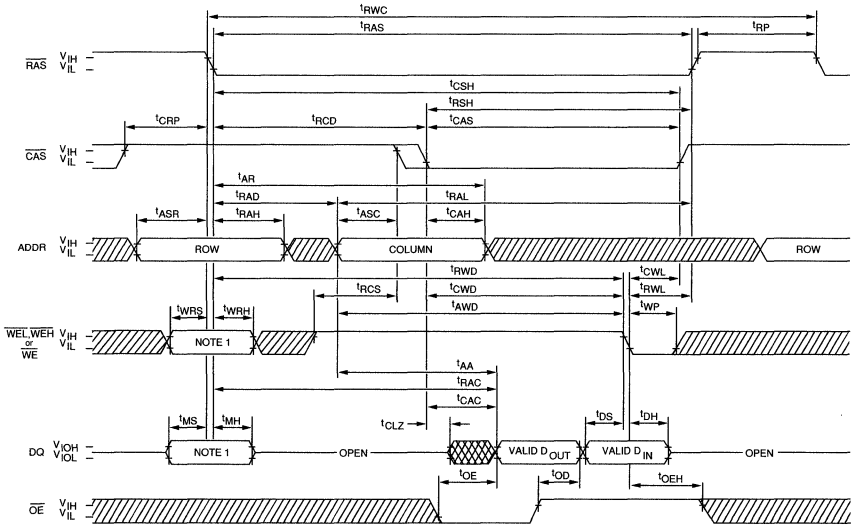


EARLY-WRITE CYCLE

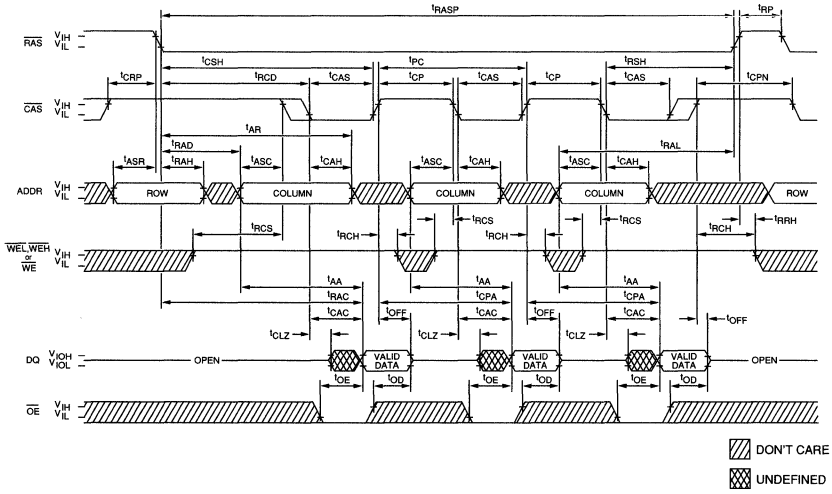


NOTE: 1. Applies to MT4C1665 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1664 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

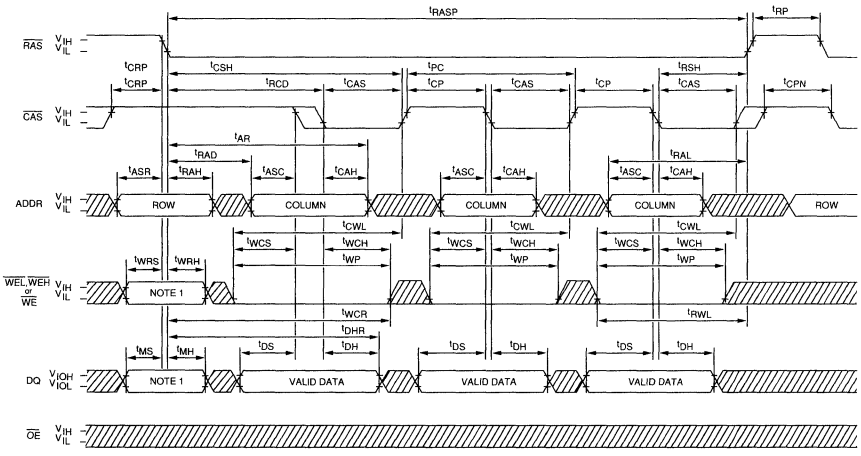


FAST-PAGE-MODE READ CYCLE

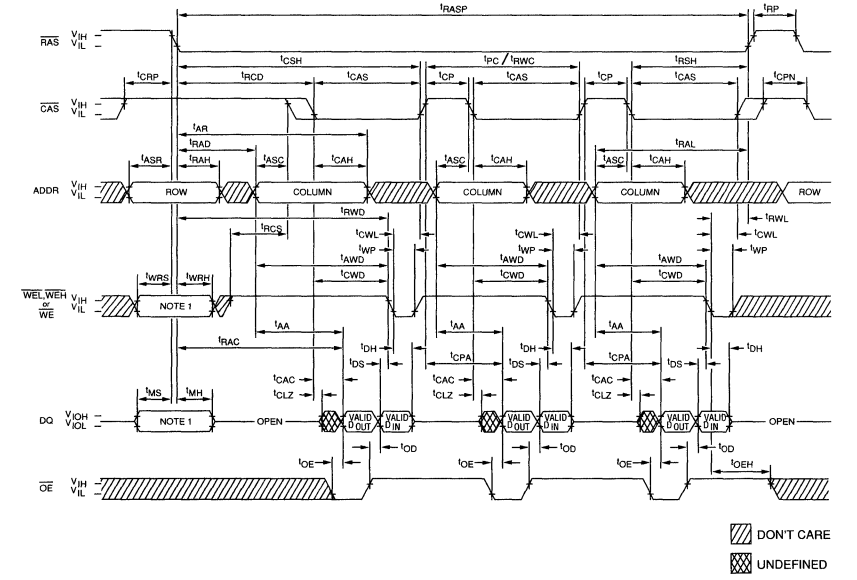


NOTE: 1. Applies to MT4C1665 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1664 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



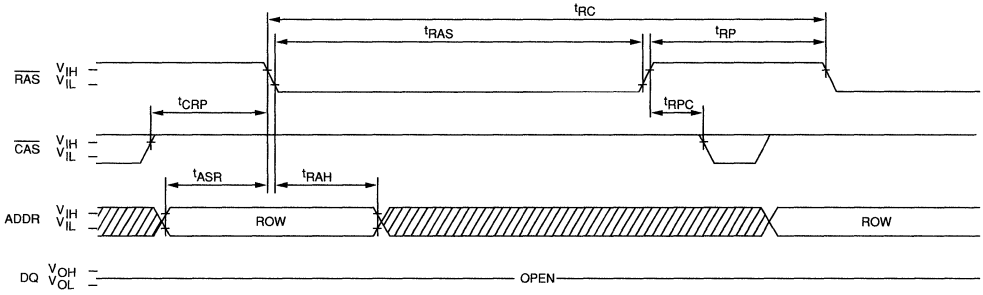
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C1665 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1664 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

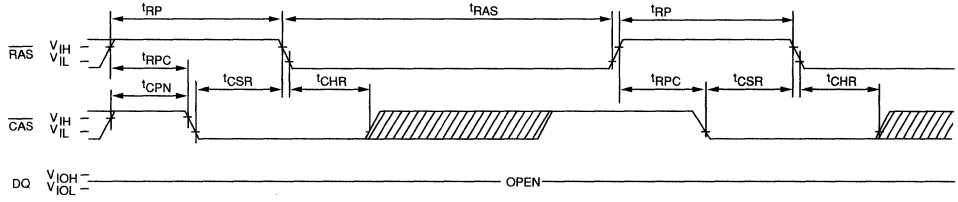
RAS-ONLY REFRESH CYCLE

(ADDR = A_0 - A_7, OE; WEL, WEH or WE = DON'T CARE)



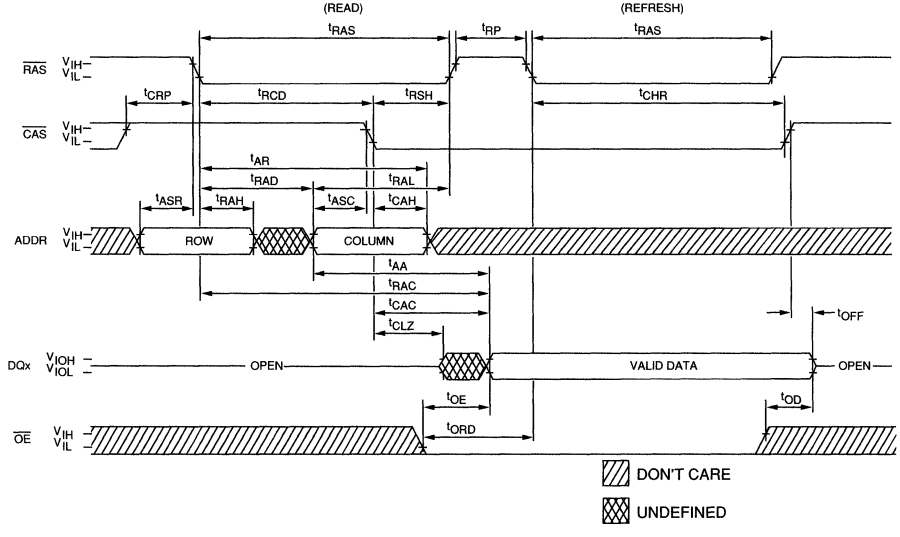
CAS-BEFORE-RAS REFRESH CYCLE

(A_0 - A_7; WEL, WEH or WE, and OE = DON'T CARE)



HIDDEN REFRESH CYCLE

(WEL, WEH or WE = HIGH; OE = LOW) [24]



DRAM

64K x 16 DRAM

LOW POWER, FAST PAGE MODE

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 2mW standby; 200mW active, typical
- All device pins are fully TTL and CMOS compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS and HIDDEN
- Optional FAST PAGE MODE access cycle
- 2 TTL load output drive capability
- BYTE WRITE access cycle (MT4C1668 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1669 only)
- Reduced CMOS STANDBY CURRENT
- Reduced operating and refresh currents
- Extended refresh: 256 cycles over 32ms (125µs cycles)

OPTIONS

OPTIONS	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Write Enable	
Byte or Word	MT4C1668
Word only	MT4C1669
• Mask Enable	
Not available	MT4C1668
Always available	MT4C1669
• Packages	
Plastic SOJ (400mil)	DJ
Plastic ZIP (450mil)	Z

PIN ASSIGNMENT (Top View)

40-Pin SOJ (E-12)

Vcc	1	40	Vss
DQ1	2	39	DQ16
DQ2	3	38	DQ15
DQ3	4	37	DQ14
DQ4	5	36	DQ13
DQ5	6	35	DQ12
DQ6	7	34	DQ11
DQ7	8	33	DQ10
DQ8	9	32	DQ9
NC	10	31	NC
Vcc	11	30	Vss
*NC/WEH	12	29	CAS
*WE/WEL	13	28	OE
RAS	14	27	**NC
A0	15	26	NC
A1	16	25	NC
A2	17	24	A7
A3	18	23	A6
A4	19	22	A5
Vcc	20	21	Vss

40-Pin Zip (C-6)

NC	1	2	DQ9
DQ10	3	4	DQ11
DQ12	5	6	DQ13
DQ14	7	8	DQ15
DQ16	9	10	Vss
DQ1	11	12	DQ2
Vcc	13	14	DQ3
DQ4	15	16	DQ5
DQ6	17	18	DQ7
DQ8	19	20	NC
Vcc	21	22	*NC/WEH
*WE/WEL	23	24	RAS
A0	25	26	A1
A2	27	28	A3
A4	29	30	Vcc
NC	31	32	NC
Vss	33	34	A5
A6	35	36	A7
**NC	37	38	OE
CAS	39	40	Vss

* MT4C1669/MT4C1668
** NC = No Connect

GENERAL DESCRIPTION

The MT4C1668/9 are randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1668 has both BYTE and WORD WRITE access cycles while the MT4C1669 has only WORD WRITE access cycles.

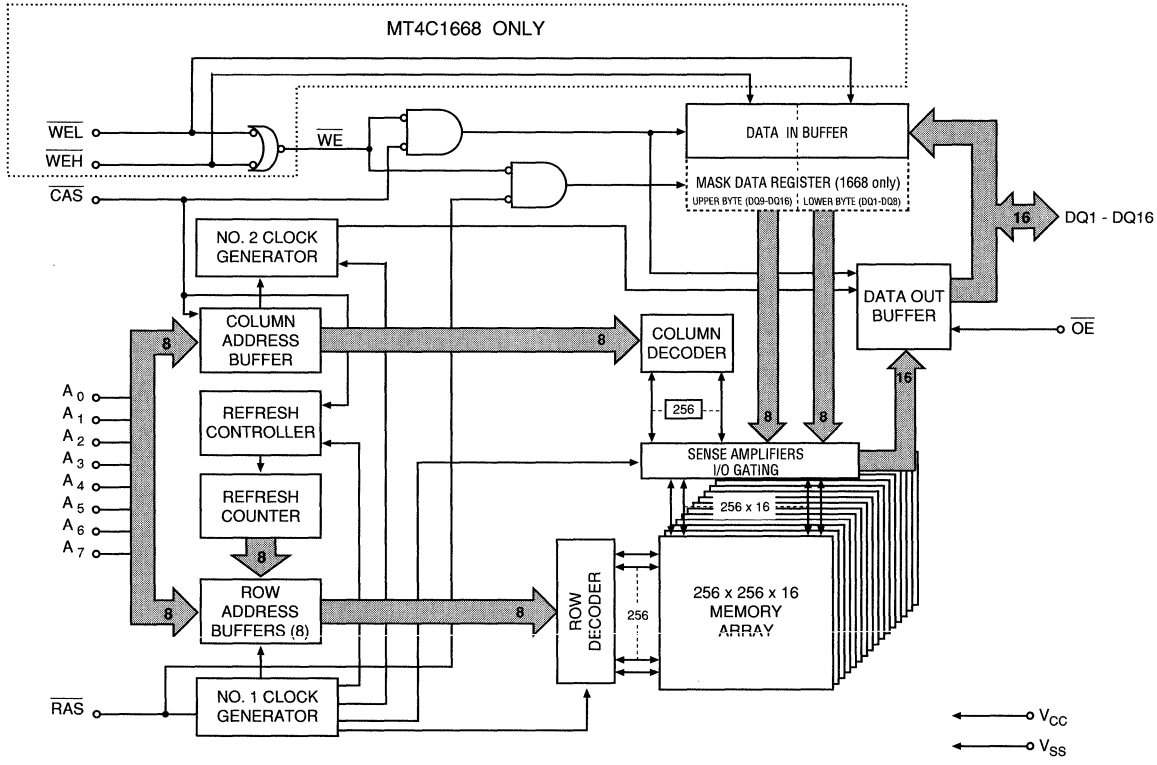
The MT4C1668 functions in a similar manner to the MT4C1669 except that replacing WE with WEL and WEH allows for BYTE WRITE access cycles. WEL and WEH function in an identical manner to WE: either WEL or WEH will generate an internal WE through an AND gate (inverted NOR gate).

The MT4C1668 "WE" function and timing are determined by the first BYTE WRITE (WEL or WEH) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or WEH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1669 has NONPERSISTENT MASKED WRITE capability.

The extended refresh of the MT4C1668/9 provides a factor-of-eight reduction of refresh intervals required, as compared to a standard 64K x 16 DRAM (MT4C1664/5). The MT4C1668/9 offers lower operating power as well as the reduced refresh current and standby current. The MT4C1668/9 are the same devices as the MT4C1664/5, but with the low power capabilites.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBER(S)	ZIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
14	24	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 8 row-address bits and as a strobe for the $\overline{WEL}$, $\overline{WEH}$ and DQ inputs for the MASKED WRITE function.
29	39	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 8 column-address bits, enable the DRAM output buffers, and as a strobe for the data inputs on WRITE cycles.
28	38	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WEL}$ and $\overline{WEH}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a high-impedance state.
13	23	$\overline{WE}$/$\overline{WEL}$*	Input	Write Enable Lower Byte: $\overline{WEL}$ on MT4C1668 is $\overline{WE}$ control for the DQ1 through DQ8 inputs. $\overline{WE}$ on MT4C1669 controls DQ1 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a high impedance state (BYTE WRITE cycle only).
12	22	NC/$\overline{WEH}$*	Input	Write Enable Upper Byte: $\overline{WEH}$ on MT4C1668 is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1669 as it has only WORD WRITE access cycles.
15, 16, 17 18, 19, 22 23, 24	25, 26, 27 28, 29, 34 35, 36	A0 to A7	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 64K available words.
2, 3, 4, 5, 6 7, 8, 9, 32, 33 34, 35, 36 37, 38, 39	11, 12, 14 15, 16, 17 2, 18, 19, 3 4, 5, 6, 7, 8 9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ or $\overline{WEH}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM location. All 16 I/Os are active for READ cycles (there is no Byte READ cycle).
10, 25, 26 27, 31	1, 20, 31 32, 37	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	Vcc	Supply	Power Supply: +5V ± 10%
21, 30, 40	10, 33, 40	Vss	Supply	Ground

NOTE: *MT4C1669/MT4C1668

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 address-bits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. $\overline{RAS}$ is used to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits.

READ or WRITE cycles on the MT4C1669 are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C1668. The MT4C1668 "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C1668) or $\overline{WE}$ (MT4C1669).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 256 combinations of $\overline{RAS}$ addresses (A0-A7) are executed at least every 32ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BYTE WRITE DESCRIPTION (MT4C1668 ONLY)

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$. Enabling $\overline{WEL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{WEH}$ will select an upper BYTE WRITE (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ selects a WORD WRITE cycle.

The MT4C1668 may be viewed as two 64K x 8 DRAMs which have common input controls, with the exception of the WE input. Figure 1 illustrates the MT4C1668 BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1669 ONLY)

Every WRITE access cycle may be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C1669 is only word selectable when $\overline{WE}$ is LOW at $\overline{RAS}$ time (the MT4C1668 does not have a MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1669 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

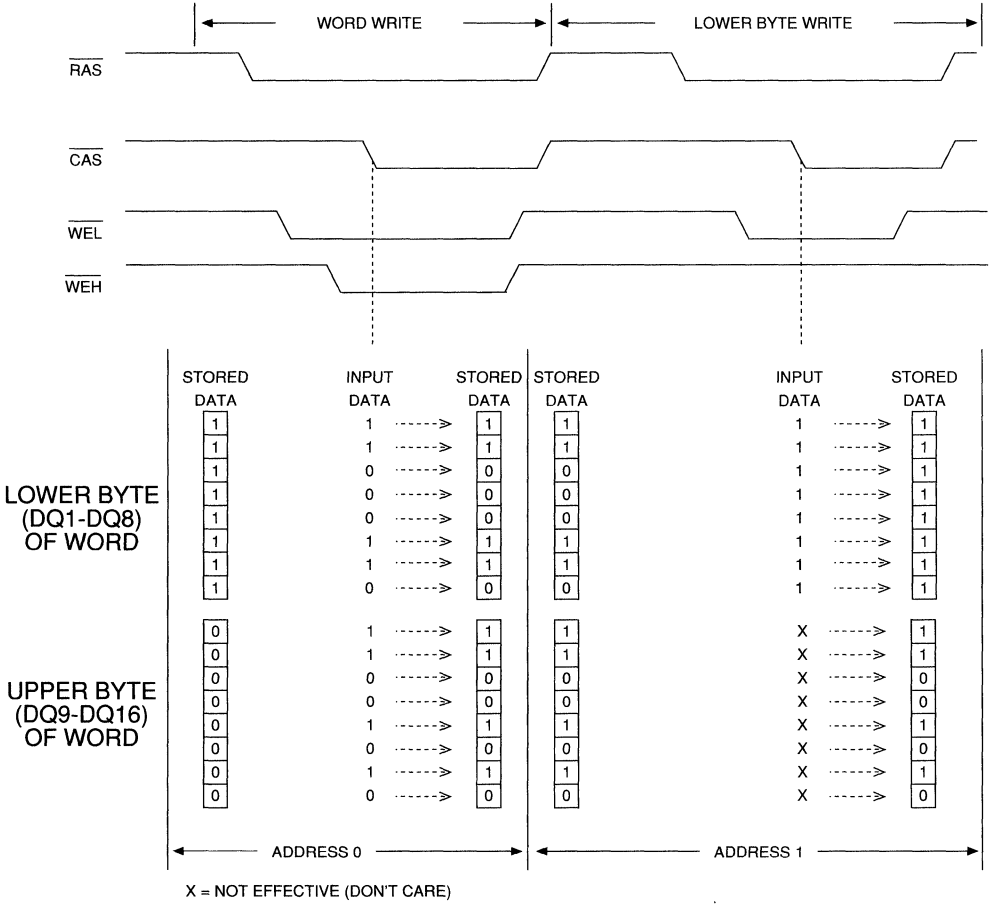


Figure 1
MT4C1668 WORD AND BYTE WRITE EXAMPLE

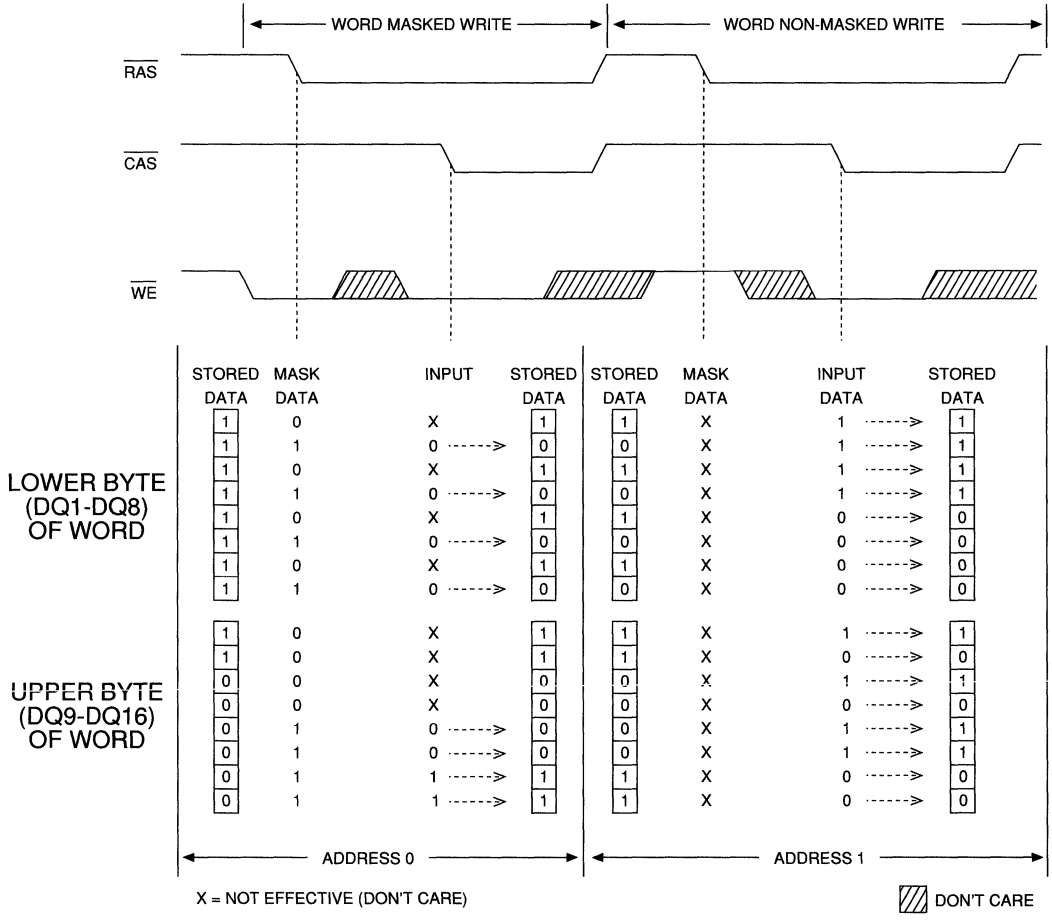


Figure 2
MT4C1669 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1668

Function		RAS	CAS	WEL	WEH	OE	Addresses tR	Addresses tC	DQs	NOTES
Standby		H	X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Valid Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Valid Data In	
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Valid Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Valid Data In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Valid Data Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Valid Data Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Valid Data In	1
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Valid Data In	1
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Valid Data Out, Data In	1
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Valid Data Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Valid Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.

TRUTH TABLE: MT4C1669

Function		RAS	CAS	WE	OE	Addresses tR	Addresses tC	DQs	NOTES
Standby		H	X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Valid Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	X	ROW	COL	Valid Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Valid Data Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Valid Data Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Valid Data In	1
	2nd Cycle	L	H→L	L	X	n/a	COL	Valid Data In	1
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Valid Data Out, Data In	1
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Valid Data Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Valid Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data-In will be dependent on the mask provided. Refer to Figure 2.
2. EARLY-WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ Vcc, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	650	650	650	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	100	90	80	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	75	65	65	mA	3,4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	100	90	80	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	100	90	80	mA	3, 5
REFRESH CURRENT: BATTERY BACK-UP (extended refresh cycles). Average power supply current with $\overline{CAS}$= 0.2V or CBR; $\overline{RAS}$ has minimum ^tRAS of 1µs; A0-A7,$\overline{WE}$,$\overline{OE}$ and DQs = Vcc -0.2V or 0.2V (DQs may float); ^tRC = 125µs	I_{CC7}	800	800	800	µA	3

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$,($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($0°C \le T_A \le +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		145		170		ns	
READ-WRITE cycle time	t_{RWC}	175		185		220		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	45		50		60		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	95		100		120		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		25		30	ns	15
Output Enable time	t_{OE}		20		25		30	ns	
Access time from column address	t_{AA}		40		45		50	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		50		55	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		55		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	100,000	30	100,000	30	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	25	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	15	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

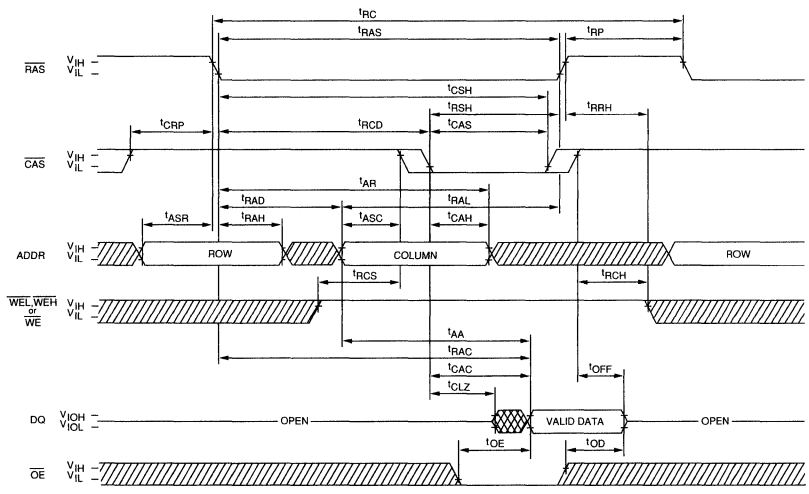
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 30
Output disable time	^tOD		10		12		20	ns	30
Write command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	15		15		15		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	50		55		65		ns	26
Write command pulse width	^tWP	15		15		15		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	50		55		65		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		125		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		70		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	^tREF		32		32		32	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26, 27
MASKED WRITE command to $\overline{RAS}$ hold time	^tWRH	15		15		15		ns	26, 27
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	10		10		20		ns	29
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	

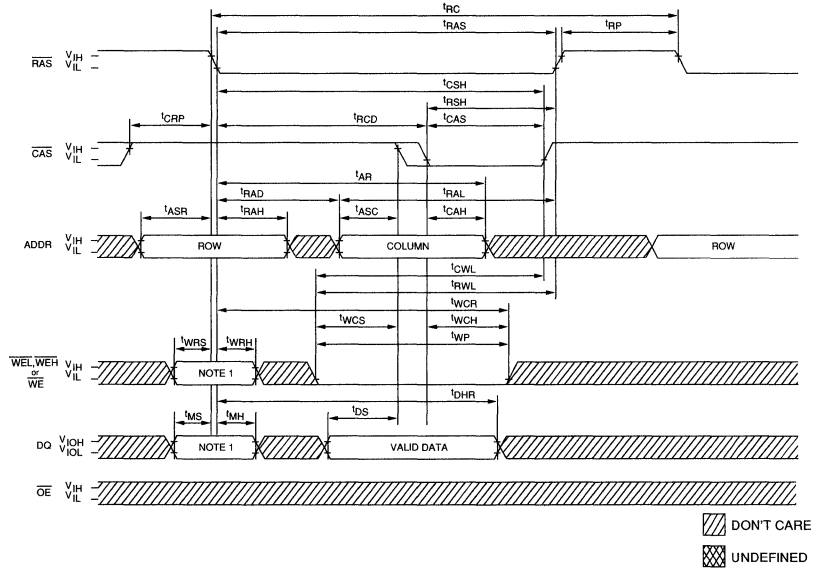
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 32ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 50pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out (Q) will bemaintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. All other inputs at Vcc -0.2V.
26. WRITE command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C1668. WRITE command is defined as $\overline{WE}$ going LOW on the MT4C1669.
27. Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
28. The refresh period may be extended to 8ms without experiencing problems.
29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
30. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

READ CYCLE

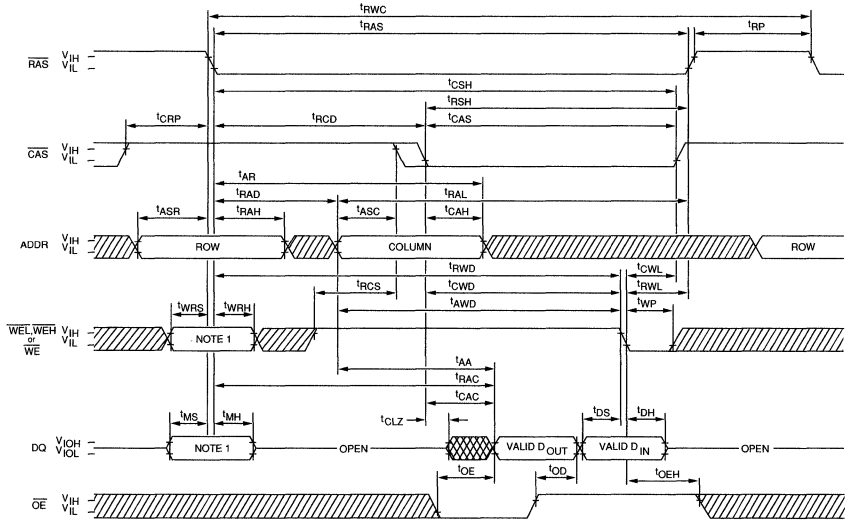


EARLY-WRITE CYCLE

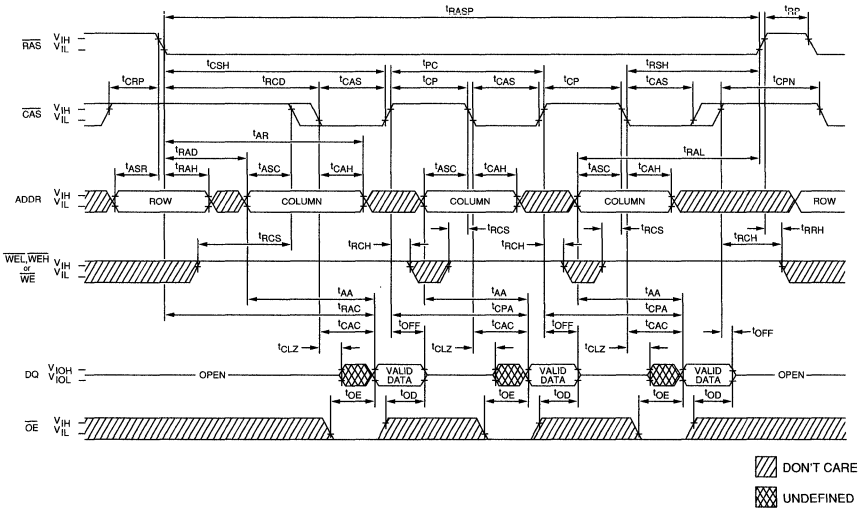


NOTE: 1. Applies to MT4C1669 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1668 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

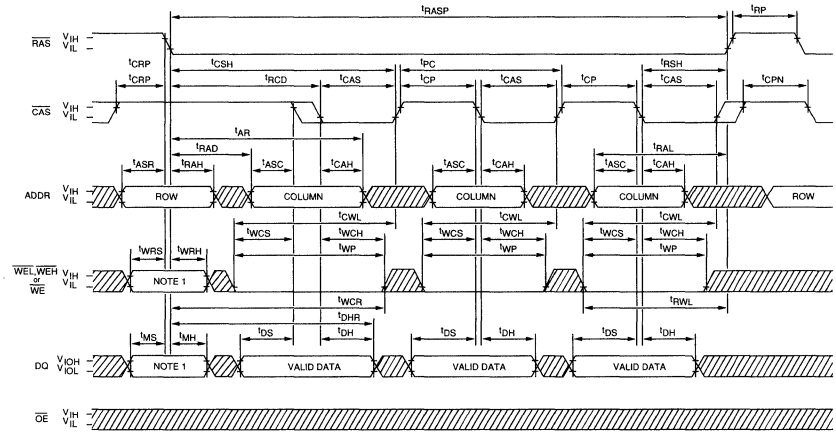


FAST-PAGE-MODE READ CYCLE

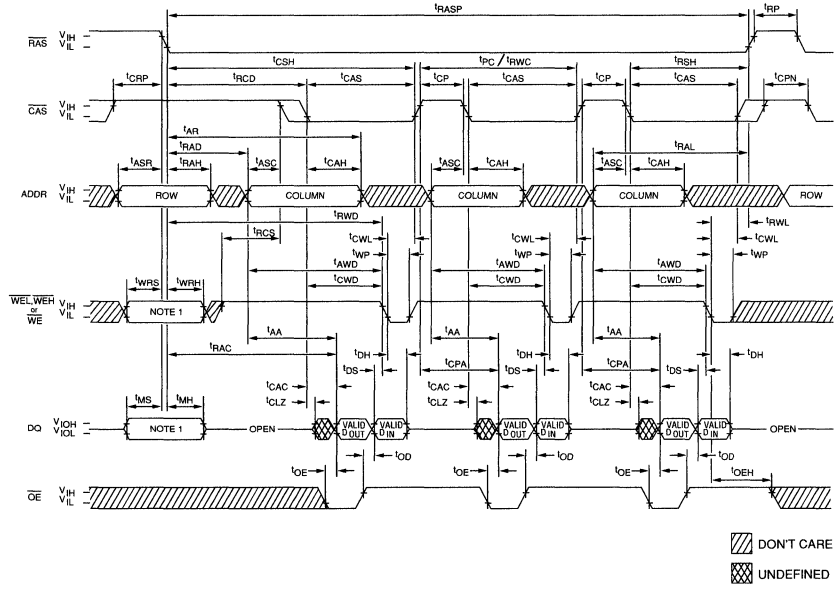


NOTE: 1. Applies to MT4C1669 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1668 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



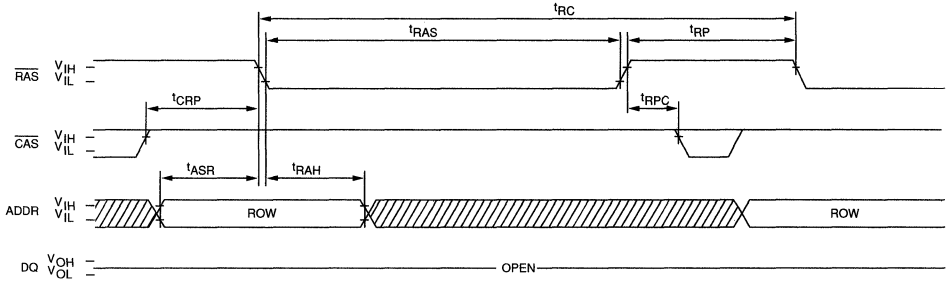
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C1669 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1668 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

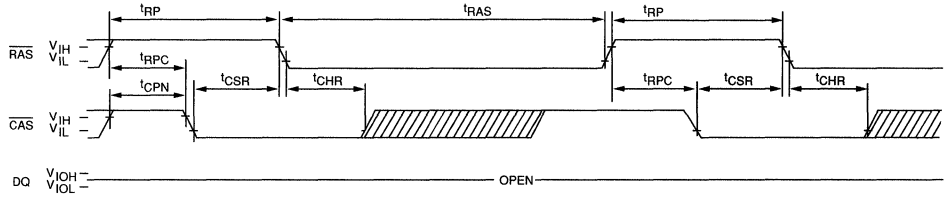
RAS-ONLY REFRESH CYCLE

(ADDR = A_0 - A_7,; OE; WEL, WEH or WE = DON'T CARE)



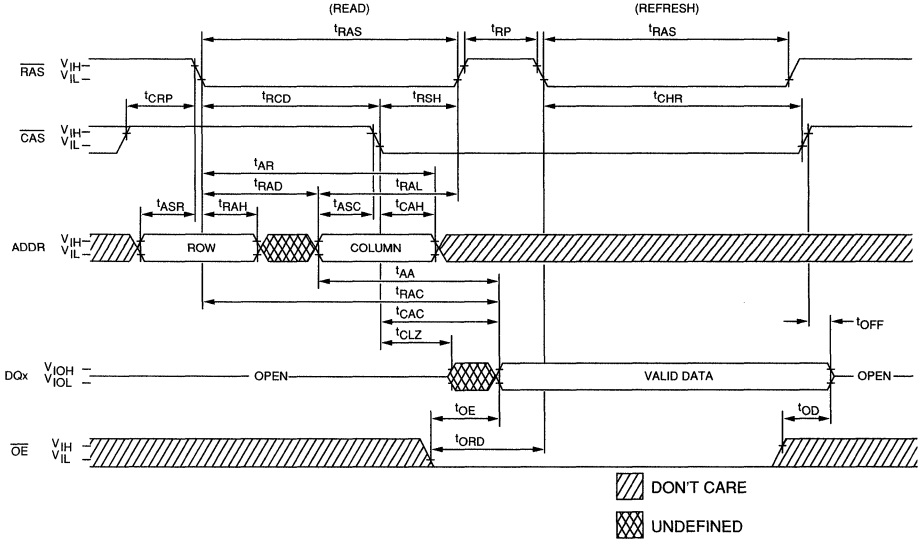
CAS-BEFORE-RAS REFRESH CYCLE

(A_0 - A_7; WEL, WEH or WE,and OE = DON'T CARE)



HIDDEN REFRESH CYCLE

(WEL, WEH or WE = HIGH; OE = LOW) [24]



DRAM

64K x 16 DRAM

STATIC COLUMN MODE

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All device pins are fully TTL and CMOS compatible
- 256 cycle refresh in 4ms
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ and HIDDEN
- Optional STATIC COLUMN MODE access cycle
- 2 TTL Load output drive capability
- BYTE WRITE access cycle (MT4C1670 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1671 only)

OPTIONS

	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Write Enable	
Byte or Word	MT4C1670
Word only	MT4C1671
• Mask Enable	
Not Available	MT4C1670
Always Available	MT4C1671
• Packages	
Plastic SOJ (400mil)	DJ
Plastic ZIP (450mil)	Z

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(E-12)

Vcc	1	40	Vss
DQ1	2	39	DQ16
DQ2	3	38	DQ15
DQ3	4	37	DQ14
DQ4	5	36	DQ13
DQ5	6	35	DQ12
DQ6	7	34	DQ11
DQ7	8	33	DQ10
DQ8	9	32	DQ9
NC	10	31	NC
Vcc	11	30	Vss
*NC/$\overline{\text{WEH}}$	12	29	$\overline{\text{CAS}}$
*$\overline{\text{WE}}$/$\overline{\text{WEL}}$	13	28	$\overline{\text{OE}}$
$\overline{\text{RAS}}$	14	27	**NC
A0	15	26	NC
A1	16	25	NC
A2	17	24	A7
A3	18	23	A6
A4	19	22	A5
Vcc	20	21	Vss

40-Pin Zip
(C-6)

NC	1	2	DQ9
DQ10	3	4	DQ11
DQ12	5	6	DQ13
DQ14	7	8	DQ15
DQ16	9	10	Vss
DQ1	11	12	DQ2
Vcc	13	14	DQ3
DQ4	15	16	DQ5
DQ6	17	18	DQ7
DQ8	19	20	NC
Vcc	21	22	*NC/$\overline{\text{WEH}}$
*$\overline{\text{WE}}$/$\overline{\text{WEL}}$	23	24	$\overline{\text{RAS}}$
A0	25	26	A1
A2	27	28	A3
A4	29	30	Vcc
NC	31	32	NC
Vss	33	34	A5
A6	35	36	A7
**NC	37	38	$\overline{\text{OE}}$
$\overline{\text{CAS}}$	39	40	Vss

* MT4C1671/MT4C1670
** NC = No Connect

GENERAL DESCRIPTION

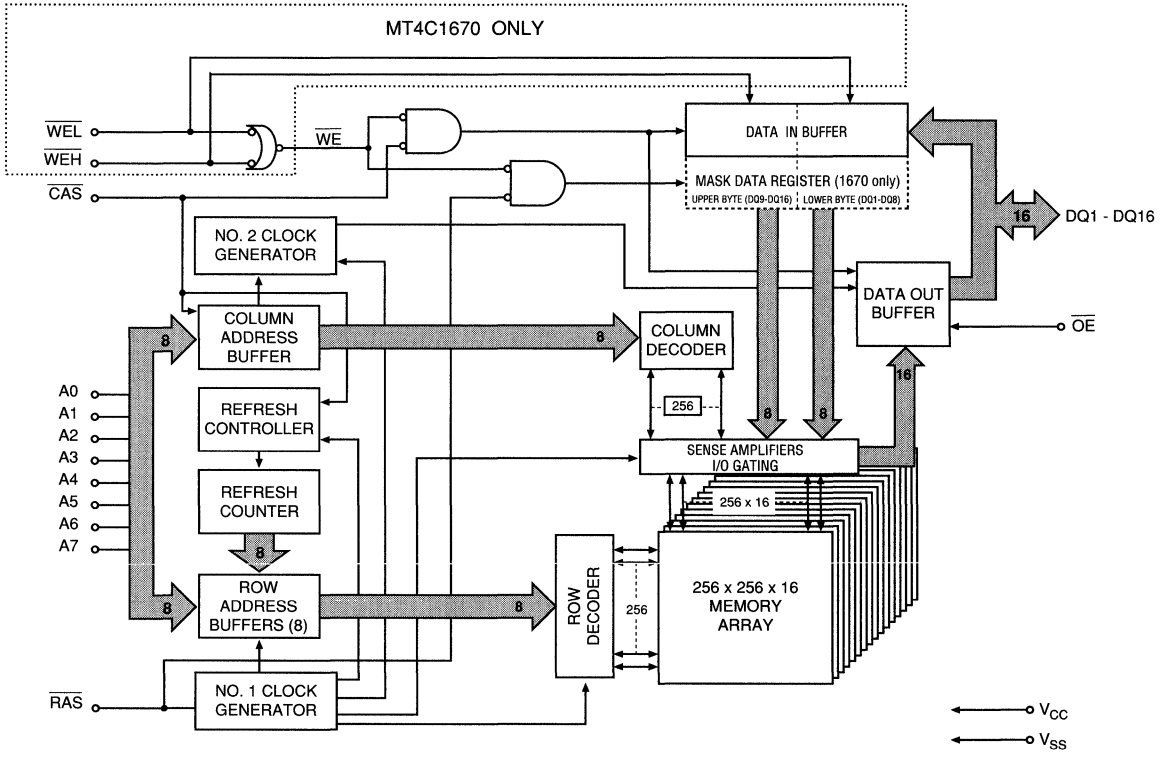
The MT4C1670/1 are randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1670 has both BYTE and WORD WRITE access cycles while the MT4C1671 has only WORD WRITE access cycles.

The MT4C1670 functions in a similar manner to the MT4C1671 except that replacing $\overline{\text{WE}}$ with $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ allows for BYTE WRITE access cycles. $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ function in an identical manner to $\overline{\text{WE}}$: either $\overline{\text{WEL}}$ or $\overline{\text{WEH}}$ will generate an internal $\overline{\text{WE}}$ through an AND gate (Inverted NOR gate).

The MT4C1670 "$\overline{\text{WE}}$" function and timing are determined by the first BYTE WRITE ($\overline{\text{WEL}}$ or $\overline{\text{WEH}}$) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: $\overline{\text{WEL}}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or $\overline{\text{WEH}}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1671 has NONPERSISTENT MASKED WRITE capability.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBER(S)	ZIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
14	24	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock-in the 8 row-address bits and as a strobe for the $\overline{WEL}$, $\overline{WEH}$ and DQ inputs for the MASKED WRITE function.
29	39	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 8 column-address bits, enable the DRAM output buffers, and as a strobe for the data inputs on WRITE cycles.
28	38	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WEL}$ and $\overline{WEH}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a high-impedance state.
13	23	$\overline{WE}$/$\overline{WEL}$*	Input	Write Enable Lower Byte: $\overline{WEL}$ on MT4C1670 is the $\overline{WE}$ control for the DQ1 through DQ8 inputs. $\overline{WE}$ on MT4C1671 controls DQ1 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a high-impedance state (BYTE WRITE cycle only).
12	22	NC/$\overline{WEH}$*	Input	Write Enable Upper Byte: $\overline{WEH}$ on MT4C1670 is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1671 as it has only WORD WRITE access cycles.
15, 16, 17 18, 19, 22 23, 24	25, 26, 27 28, 29, 34 35, 36	A0 to A7	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 64K available words.
2, 3, 4, 5, 6 7, 8, 9, 32, 33 34, 35, 36 37, 38, 39	11, 12, 14 15, 16, 17 2, 18, 19, 3 4, 5, 6, 7, 8	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ or $\overline{WEH}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM location. All 16 I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25, 26 27, 31	1, 20, 31 32, 37	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	Vcc	Supply	Power Supply: +5V ± 10%
21, 30, 40	10, 33, 40	Vss	Supply	Ground

NOTE: *MT4C1671/MT4C1670

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 address-bits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. $\overline{RAS}$ is used to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits.

READ or WRITE cycles on the MT4C1671 are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C1670. The MT4C1670 "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C1670) or $\overline{WE}$ (MT4C1671).

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. By holding $\overline{RAS}$ and $\overline{CAS}$ LOW, different column addresses may be given for executing faster STATIC COLUMN READ cycles. Faster STATIC COLUMN WRITE cycles must have $\overline{CAS}$ or $\overline{WE}$ toggled strobing-in the different column addresses. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 256 combinations of $\overline{RAS}$ addresses (A0-A7) are executed at least every 4ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BYTE WRITE ACCESS CYCLE (MT4C1670 ONLY)

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$. Enabling $\overline{WEL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while Enabling $\overline{WEH}$ will select an upper BYTE WRITE (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ selects a WORD WRITE cycle.

The MT4C1670 may be viewed as two 64K x 8 DRAMS, which have common input controls, with the exception of the WE input. Figure 1 illustrates the MT4C1670 BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1671 ONLY)

Every WRITE access cycle may be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C1671 is only word selectable when $\overline{WE}$ is LOW at $\overline{RAS}$ time (the MT4C1670 does not have a MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1671 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

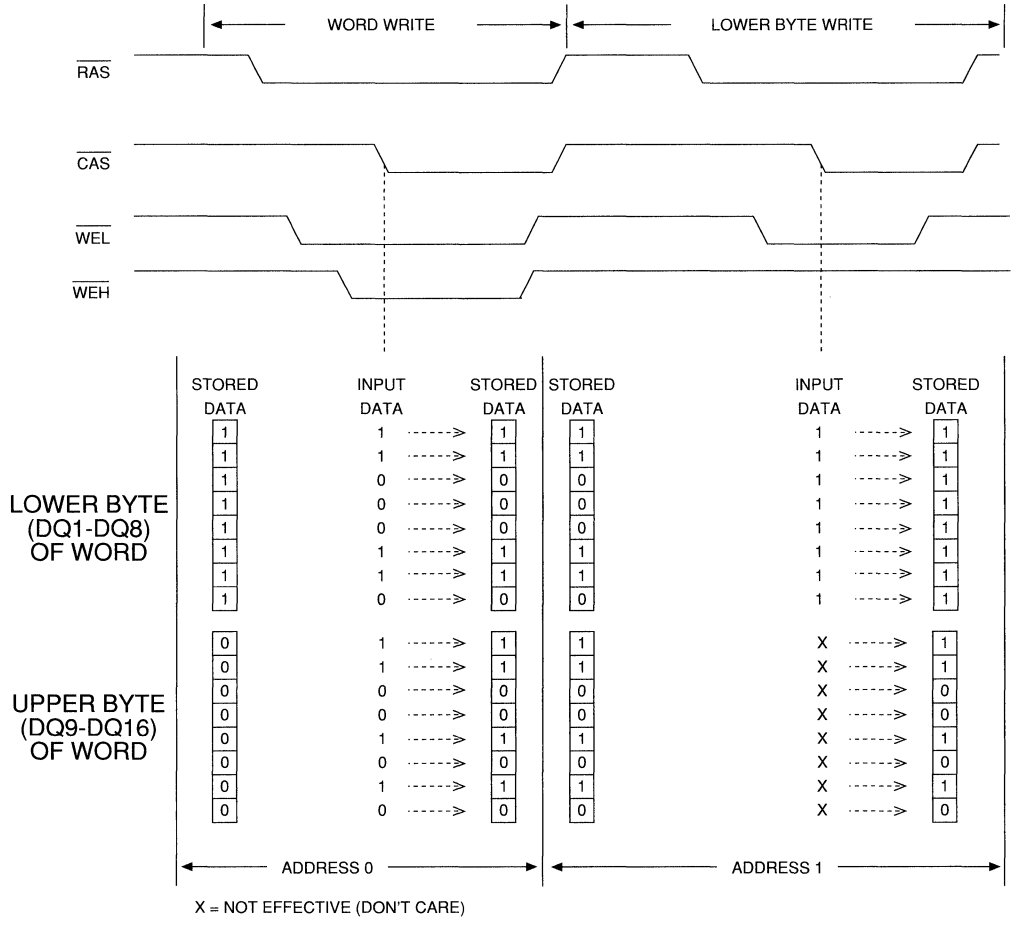


Figure 1
MT4C1670 WORD AND BYTE WRITE EXAMPLE

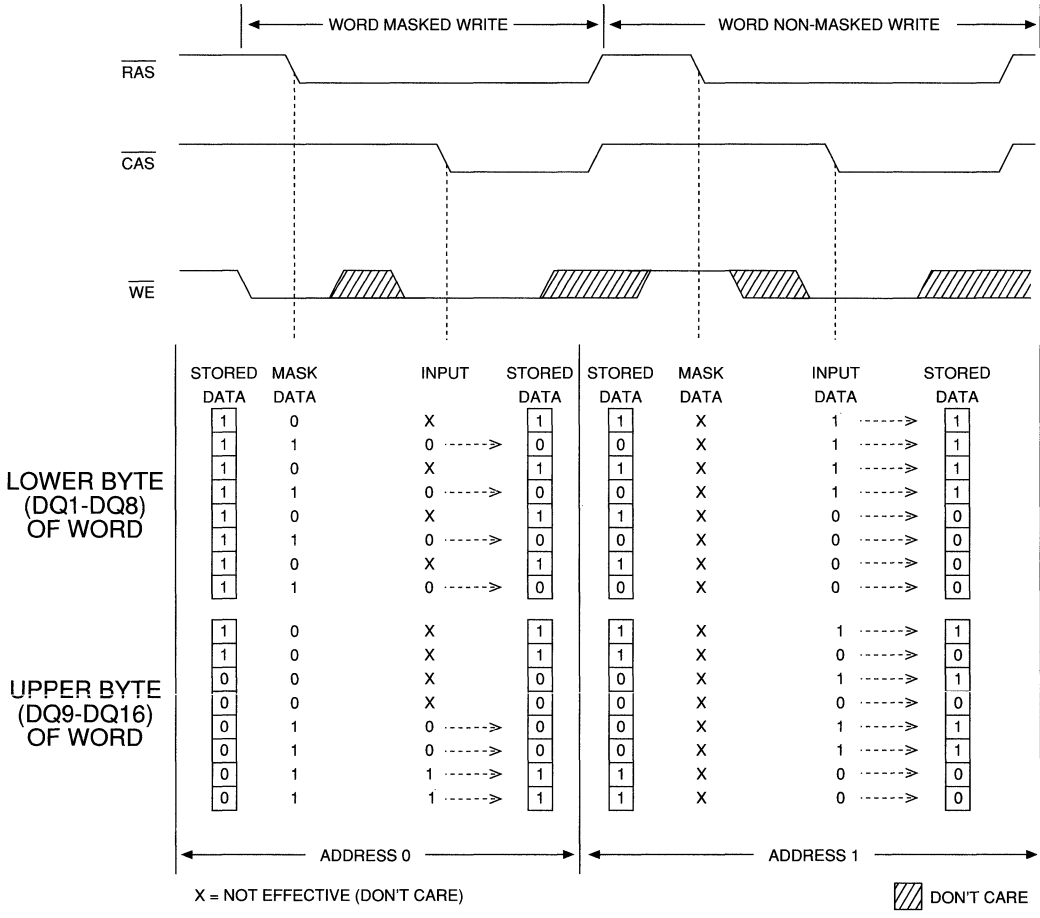


Figure 2
MT4C1671 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1670

Function		RAS	CAS	WEL	WEH	OE	Addresses tR	Addresses tC	DQs	NOTES
Standby		H	X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Valid Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Valid Data In	
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Valid Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Valid Data In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
STATIC COLUMN READ	1st Cycle	L	L	H	H	L	ROW	COL	Valid Data Out	
	2nd Cycle	L	L	H	H	L	n/a	COL	Valid Data Out	
STATIC COLUMN EARLY-WRITE	1st Cycle	L	L	L	L	X	ROW	COL	Valid Data In	1
	2nd Cycle	L	*L	*L	*L	X	n/a	COL	Valid Data In	1, 3
STATIC COLUMN READ-WRITE	1st Cycle	L	L	H→L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
	2nd Cycle	L	L	H→L	H→L	L→H	n/a	COL	Valid Data Out, Data In	1
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Valid Data Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Valid Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Either CAS or WEL / WEH must latch in each additional column address and input data.

TRUTH TABLE: MT4C1671

Function		RAS	CAS	WE	OE	Addresses tR	Addresses tC	DQs	NOTES
Standby		H	X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Valid Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	X	ROW	COL	Valid Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
STATIC COLUMN READ	1st Cycle	L	L	H	L	ROW	COL	Valid Data Out	
	2nd Cycle	L	L	H	L	n/a	COL	Valid Data Out	
STATIC COLUMN EARLY-WRITE	1st Cycle	L	L	L	X	ROW	COL	Valid Data In	1
	2nd Cycle	L	*L	*L	X	n/a	COL	Valid Data In	1, 3
STATIC COLUMN READ-WRITE	1st Cycle	L	L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1
	2nd Cycle	L	L	H→L	L→H	n/a	COL	Valid Data Out, Data In	1
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Valid Data Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Valid Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided. Refer to Figure 2.
2. EARLY-WRITE only.
3. Either CAS or WEL / WEH must latch in each additional column address and input data.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ Vcc, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	110	100	90	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	80	70	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	110	100	90	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	110	100	90	mA	3, 5

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$,($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		145		170		ns	
READ-WRITE cycle time	^tRWC	175		185		220		ns	
STATIC-COLUMN READ or WRITE cycle time	^tSC	45		50		60		ns	
STATIC-COLUMN READ-WRITE cycle time	^tSRMC	95		100		120		ns	
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		25		30		35	ns	15
Output Enable time	^tOE		20		25		30	ns	
Access time from column address	^tAA		40		45		50	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		50		55	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		55		60		ns	
$\overline{CAS}$ pulse width	^tCAS	25	100,000	30	100,000	30	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	25	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		12		12		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	15	50	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		ns	
Read command setup time	^tRCS	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 30

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

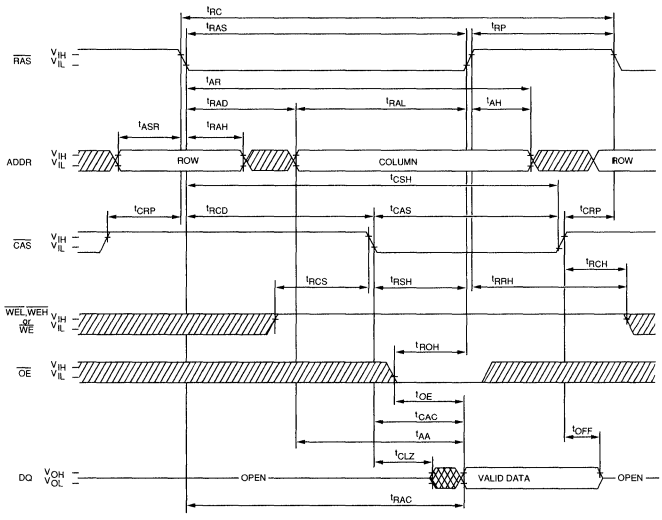
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output Disable time	^tOD		10		12		20	ns	30
Write command setup time	^tWCS	0		0		0		ns	21, 26
Write command hold time	^tWCH	15		15		15		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	50		55		65		ns	26
Write command pulse width	^tWP	15		15		15		ns	26
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	26
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	50		55		65		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	90		100		125		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		70		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	^tREF		4		4		4	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		15		15		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	^tWRS	0		0		0		ns	26, 27
MASKED WRITE command to $\overline{RAS}$ hold time	^tWRH	15		15		15		ns	26, 27
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	26
Mask data to $\overline{RAS}$ hold time	^tMH	15		15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	10		10		20		ns	29
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
Last WRITE to column address delay	^tLWAD	20	30	20	35	25	45	ns	
Last WRITE to column address hold time	^tAHLW	65		75		95		ns	
Access time from last WRITE	^tALW	65		75		95		ns	
Output data enable from WRITE	^tOW	^tAA		^tAA		^tAA		ns	
Output data hold time from column address	^tAOH	5		5		5		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	10		10		10		ns	
Column address hold time referenced to $\overline{RAS}$ HIGH	^tAH	5		5		10		ns	
$\overline{CAS}$ pulse width in STATIC-COLUMN mode	^tCSC	^tCAS		^tCAS		^tCAS		ns	
Write command in active time	^tWI	10		10		10		ns	

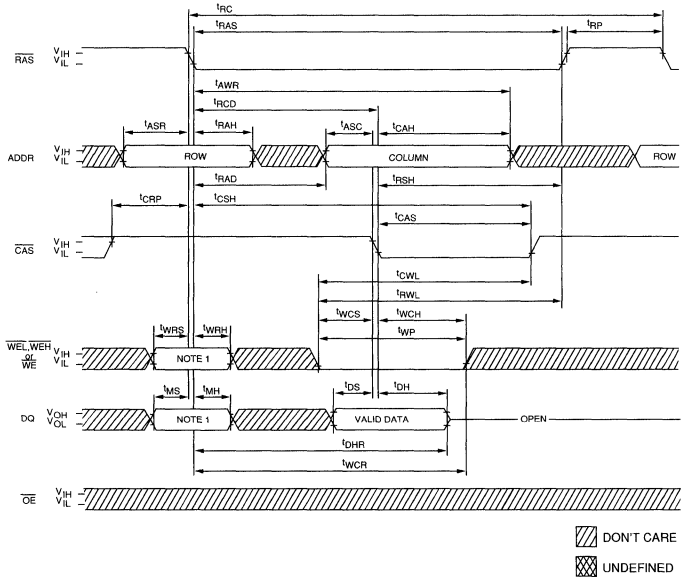
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 50pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out (Q) will bemaintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. All other inputs at Vcc -0.2V.
26. WRITE command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C1670. WRITE command is defined as $\overline{WE}$ going LOW on the MT4C1671.
27. Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
28. The refresh period may be extended to 8ms without experiencing problems.
29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
30. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

READ CYCLE

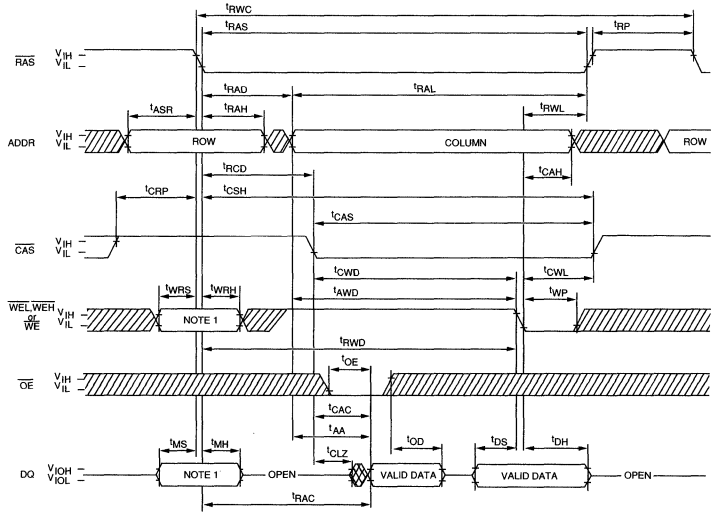


EARLY-WRITE CYCLE

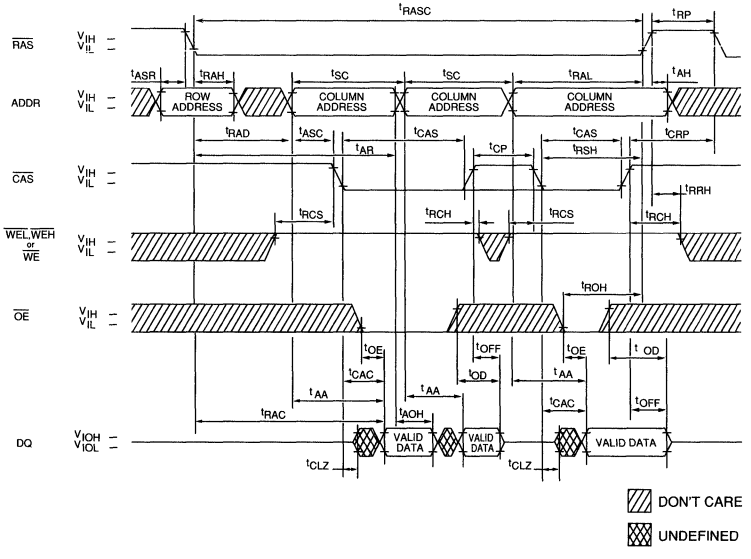


NOTE: 1. Applies to MT4C1671 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

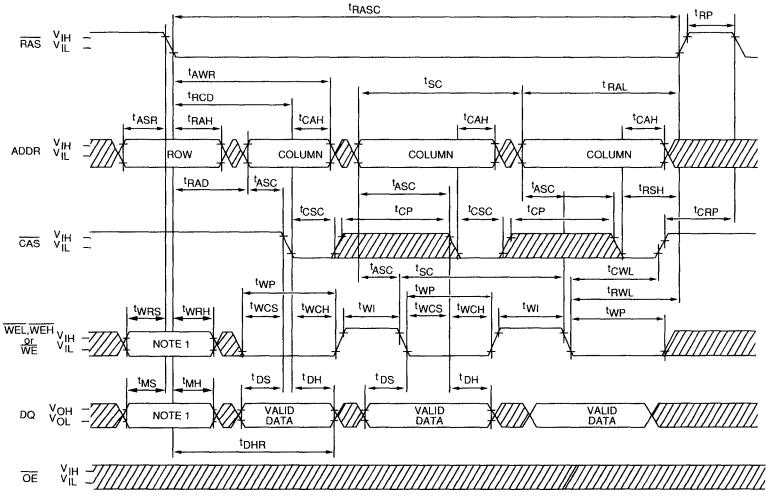


STATIC-COLUMN READ CYCLE

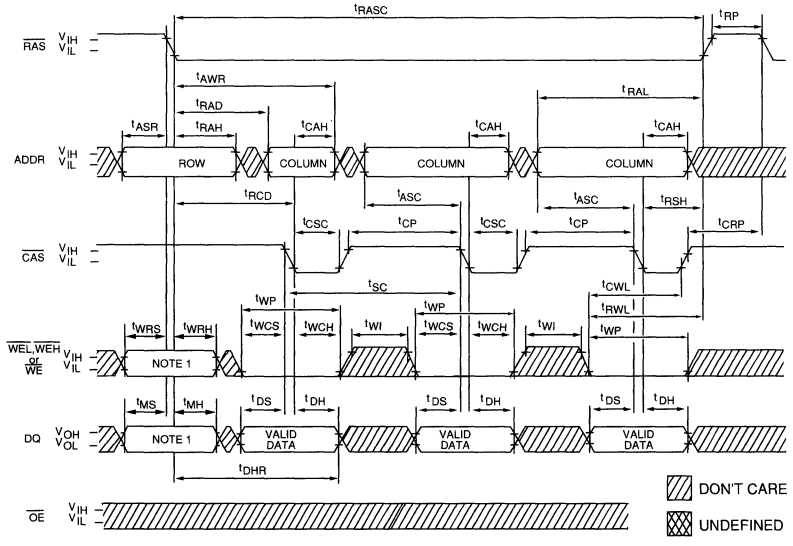


NOTE: 1. Applies to MT4C1671 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

STATIC-COLUMN EARLY-WRITE CYCLE
($\overline{WE}$ CONTROLLED)

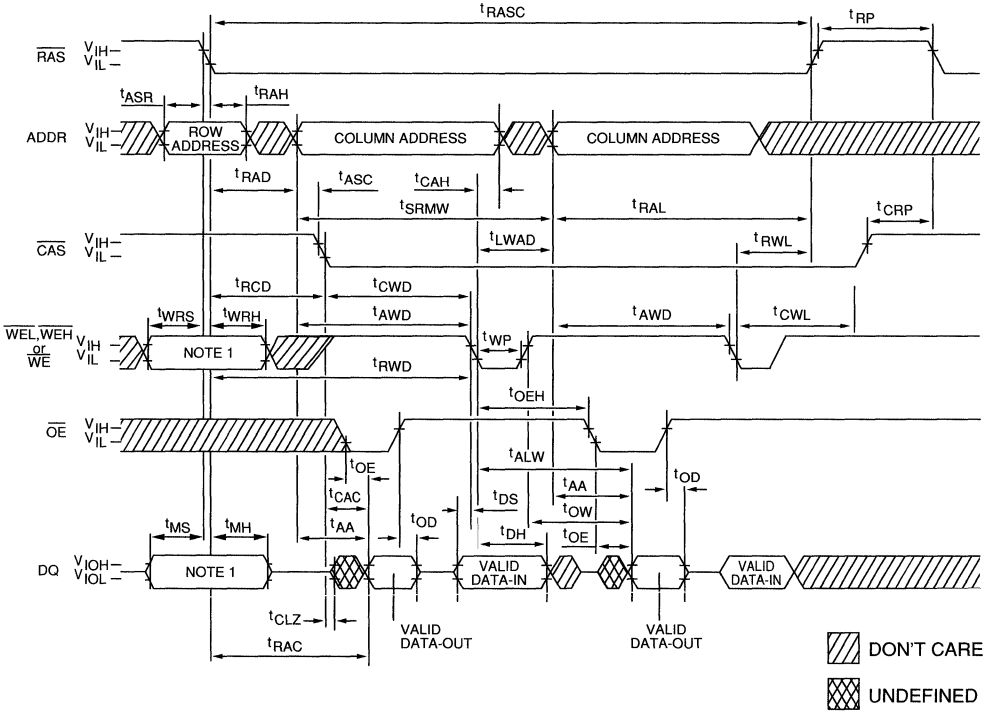


STATIC-COLUMN EARLY-WRITE CYCLE
($\overline{CAS}$ CONTROLLED)



NOTE: 1. Applies to MT4C1671 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

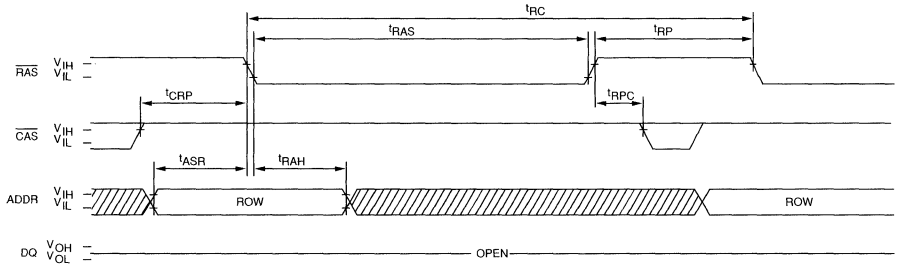
STATIC COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C1671 only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 are don't care at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are don't care for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

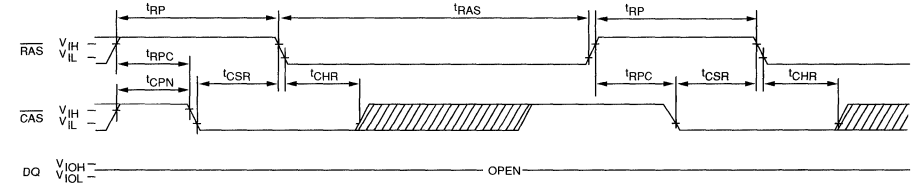
$\overline{RAS}$-ONLY REFRESH CYCLE

(ADDR = A_0 - A_7, $\overline{OE}$; $\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = DON'T CARE)



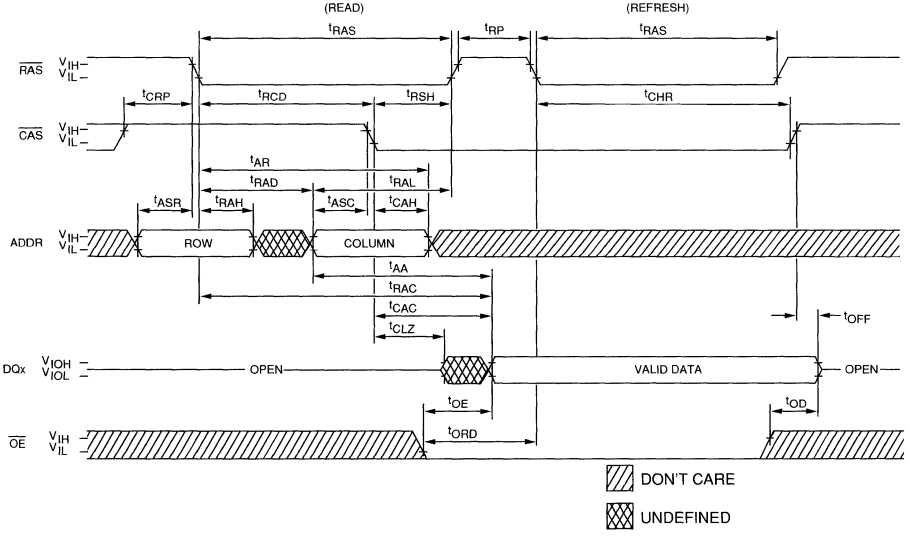
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_7; $\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$,and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = HIGH; $\overline{OE}$ = LOW) [24]



DRAM

64K x 16 DRAM

FAST PAGE MODE, DUAL CAS

FEATURES

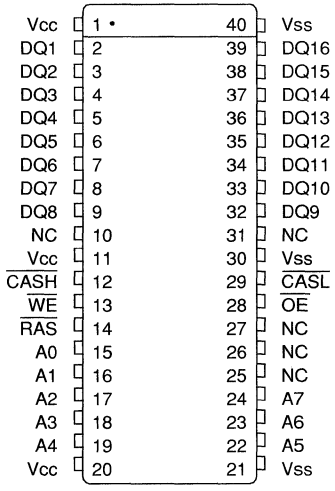
- Industry standard x16 pinouts, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 350mW active, typical
- All device pins are fully TTL and CMOS compatible
- 256-cycle refresh in 4ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS and HIDDEN
- Optional FAST PAGE MODE access cycle
- 2 TTL Load output drive capability
- BYTE WRITE access cycle via two CAS control pins

OPTIONS

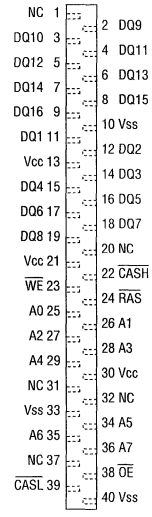
	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Plastic SOJ (400mil)	DJ
Plastic ZIP (475mil)	Z

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(E-12)



40-Pin ZIP
(C-6)



NC = No Connect

GENERAL DESCRIPTION

The MT4C1672 is a randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1672 has both byte and word write access cycles.

The MT4C1672 functions in a similar manner to the MT4C1664 except that the BYTE WRITE cycles are determined by two CAS controls rather than two WE controls.

The MT4C1672 has the same pinout as the MT4C1664 except WEL is replaced by WE, WEH is replaced by CASH and CAS is replaced by CASL. These changes allow for the CAS controlled byte WRITE access cycles.

The MT4C1672 CAS function and timing are determined by the first BYTE WRITE (CASL or CASH) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: CASL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and CASH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1672 does not have BYTE READ cycles. All 16 DQs are active regardless whether CASL or CASH is active. CASL and CASH function in an identical manner to CAS: either CASL or CASH will generate an internal CAS. The first CAS (CASL or CASH) to transition LOW and the last to transition back HIGH determines the CAS timing for all 16 DQs during READ cycles.

The MT4C1672 specifications are exactly the same as the MT4C1664 specifications. Referrence to the MT4C1664 data sheet will provide all the specifications needed for the MT4C1672.

DRAM

256K x 16 DRAM

FAST PAGE MODE

FEATURES

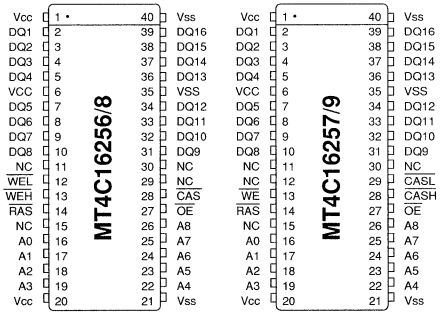
- Industry standard x16 pinouts, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 350mW active, typical
- All device pins are fully TTL and CMOS compatible
- 512 cycle refresh in 8ms (9 rows and 9 columns)
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ and HIDDEN
- Optional FAST PAGE MODE access cycle, 512 locations wide
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C16257/9 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C16258/9 only)

OPTIONS

	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Write Cycle Access	
Byte or Word via $\overline{WE}$	MT4C16256, MT4C16258
Byte or Word via $\overline{CAS}$	MT4C16257, MT4C16259
• Masked Write	
Not Available	MT4C16256, MT4C16257
Available	MT4C16258, MT4C16259
• Packages	
Plastic SOJ	DJ
Plastic TSOP (*)	TG

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(E-12)



NC = No Connect
*Consult factory for availibilty of TSOP packages

GENERAL DESCRIPTION

The MT4C16256/7/8/9 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. The MT4C16256 and MT4C16258 have both byte and word write access cycles via two write enable pins. The MT4C16257 and MT4C16259 have both byte and word write access cycles via two $\overline{CAS}$ pins. The MT4C16258 and MT4C16259 are also able to perform WRITE-PER-BIT accesses.

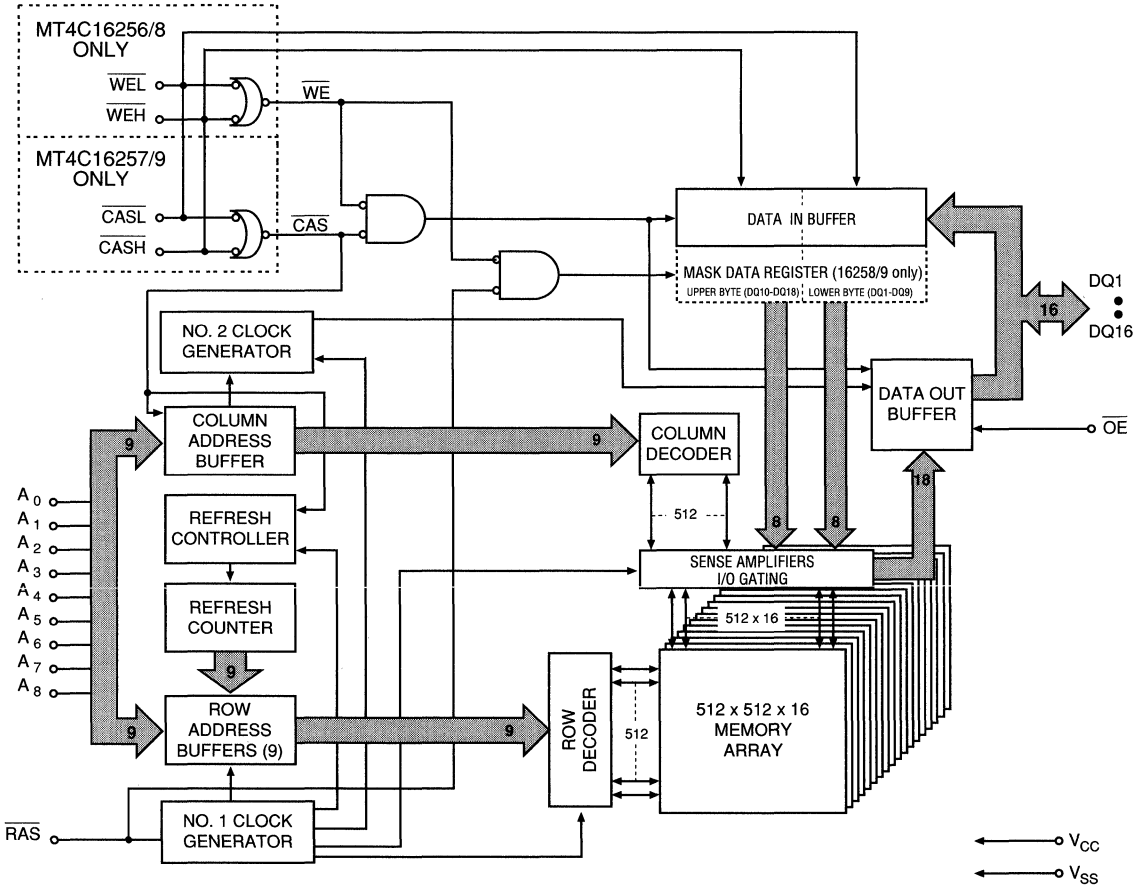
The MT4C16256 and MT4C16257 function in the same manner except that $\overline{WEL}$ and $\overline{WEH}$ on MT4C16256 and $\overline{CASL}$ and $\overline{CASH}$ on MT4C16257 control the selection of byte WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an identical manner to $\overline{WE}$ in that either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$. $\overline{CASL}$ and $\overline{CASH}$ function in an identical manner to $\overline{CAS}$ in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$.

The MT4C16256 "$\overline{WE}$" function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16257 "$\overline{CAS}$" function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$)to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4C16257.

The MT4C16258 and MT4C16259 function in the same manner as MT4C16256 and MT4C16257, respectively; and they have NONPERSISTENT, MASKED WRITE cycles capabilities. This option allows the MT4C16258 and MT4C16259 to operate with either normal WRITE cycles or with NONPERSISTENT, MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
14	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to latch in the 9 row address bits and as a strobe for the $\overline{WE}$ and DQ's on the MASKED WRITE option (MT4C16258 and MT4C16259 only).
28	$\overline{CAS}$/ $\overline{CASH}$	Input	Column Address Strobe: $\overline{CAS}$ (MT4C16256/8) is used to latch in the 9 column address bits, enable the DRAM output buffers, and as a strobe for the data inputs on WRITE cycles. $\overline{CAS}$ controls DQ1 through DQ16.Column Address Strobe Upper Byte: $\overline{CASH}$ (MT4C16257/9) is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
27	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ (MT4C16256/8) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/9) must be LOW and $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8) or $\overline{WE}$ (MT4C16257/9) must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a high impedance state.
13	$\overline{WEH}$/$\overline{WE}$	Input	Write Enable Upper Byte: $\overline{WEH}$ (MT4C16256/8) is $\overline{WE}$ control forthe DQ9 through DQ16 inputs. If $\overline{WEL}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. The DQs for the byte not being written will remain in a high impedance state (byte WRITE cycle only). Write Enable: $\overline{WE}$ (MT4C16257/9) controls DQ1 through DQ16 inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C16258/9 also use $\overline{WE}$ to enable the MASK register during $\overline{RAS}$ time.
12	$\overline{WEL}$/NC	Input	Write Enable Lower Byte: $\overline{WEL}$ (MT4C16256/8) is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. The DQs for the byte not being written will remain in a high impedance state (byte WRITE cycle only).
29	NC/$\overline{CASL}$	Input	Column Address Strobe Low Byte: $\overline{CASL}$ (MT4C16257/9) is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a high impedance state during either a READ or a WRITE access cycle.
16-19 22-26	A0 to A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CASL}$ / $\overline{CASH}$) to select one 16-bit word (or 8-bit byte) out of the 256K available words.
2-5, 7-10 31-34, 36-39	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. Byte writes can be performed by using $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/8) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. All sixteen I/O's are active for READ cycles (MT4C16256/8). The MT4C16257/9 allow for Byte READ cycles.
11, 15, 30	NC		No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	Vcc	Supply	Power Supply: +5V ± 10%
21, 35, 40	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered nine bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first nine bits and $\overline{CAS}$ the latter nine bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes low. The MT4C16256 and MT4C16258 each have one $\overline{CAS}$ control while the MT4C16257 and MT4C16259 have two: $\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 256K x 16 DRAMs. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8 and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C16257 and MT4C16259 "$\overline{CAS}$" function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C16257 and MT4C16259 both byte READ and byte WRITE cycle capabilities.

A READ or WRITE cycle on the MT4C16257 or MT4C16259 is selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C16256 or MT4C16258. The MT4C16256 and MT4C16258 "$\overline{WE}$" function is determined by the first byte WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C16256 and MT4C16258) or $\overline{WE}$ (MT4C16257 and MT4C16259).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled strobing in different column addresses and executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for ROW address control.

BYTE ACCESS CYCLE

The byte WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{WEL}$/$\overline{CASL}$ will select a lower byte WRITE cycle (DQ1-DQ8) while Enabling $\overline{WEH}$ or $\overline{CASH}$ will select an upper byte WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$ selects a word WRITE cycle.

The MT4C16256, MT4C16257, MT4C16258 and MT4C16259 can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the $\overline{WE}$ or the $\overline{CAS}$ inputs. Figure 1 illustrates the MT4C16256 byte and word WRITE cycles and Figure 2 illustrates the MT4C16257 byte and word WRITE cycles.

The MT4C16257 also has byte and word READ cycles since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 3 illustrates the MT4C16257 byte and word READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C16258/9 Only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C16256 and MT4C16257 do not have the MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated (non-persistent), even if the previous cycle's mask was the same mask.

Figure 4 illustrates the MT4C16258 and MT4C16259 MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

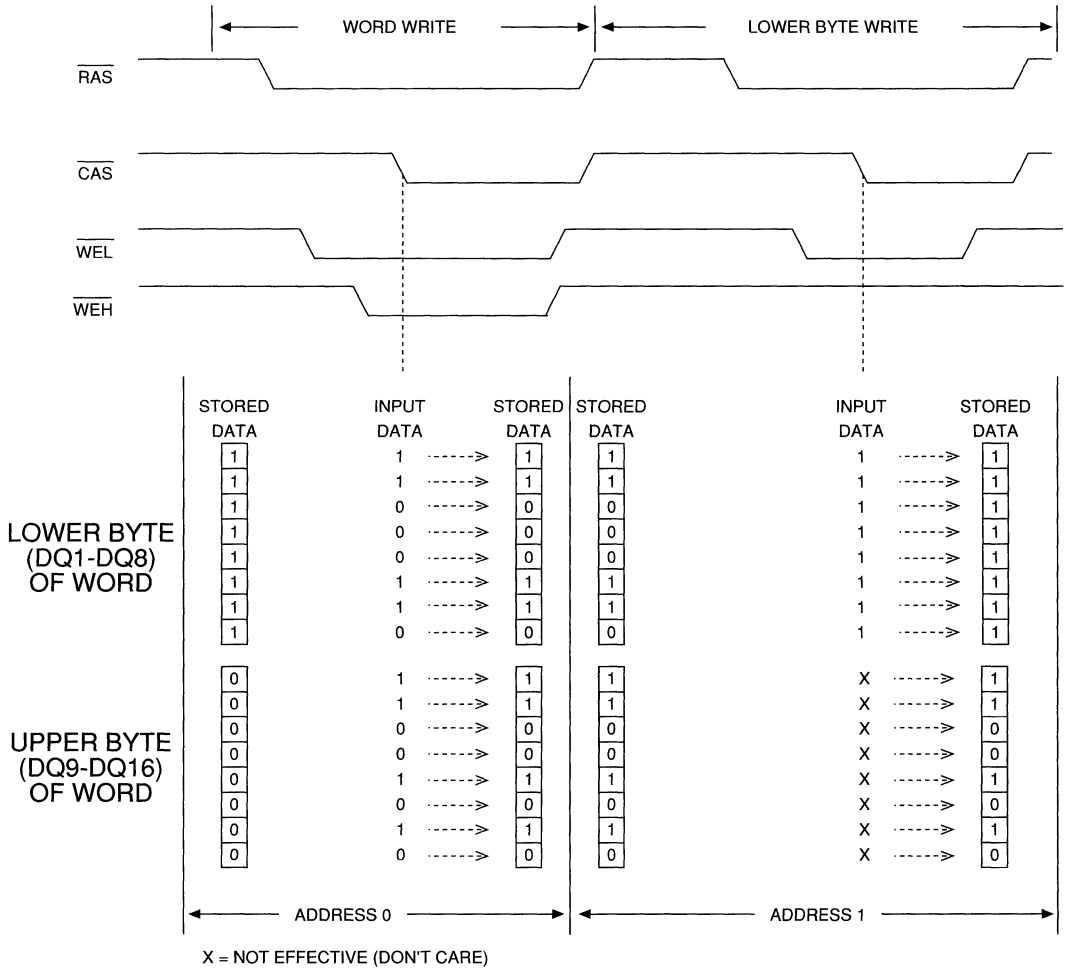


Figure 1
MT4C16256/8 WORD AND BYTE WRITE EXAMPLE

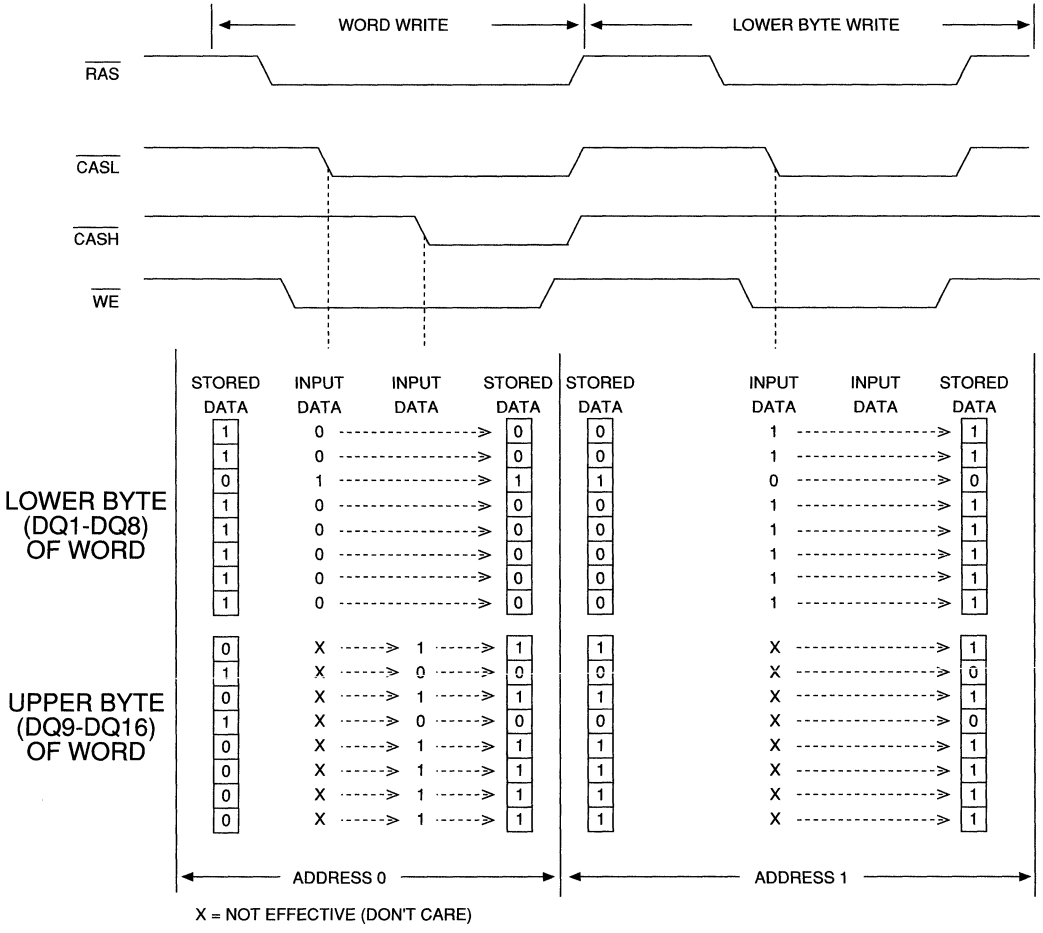


Figure 2
MT4C16257/9 WORD AND BYTE WRITE EXAMPLE

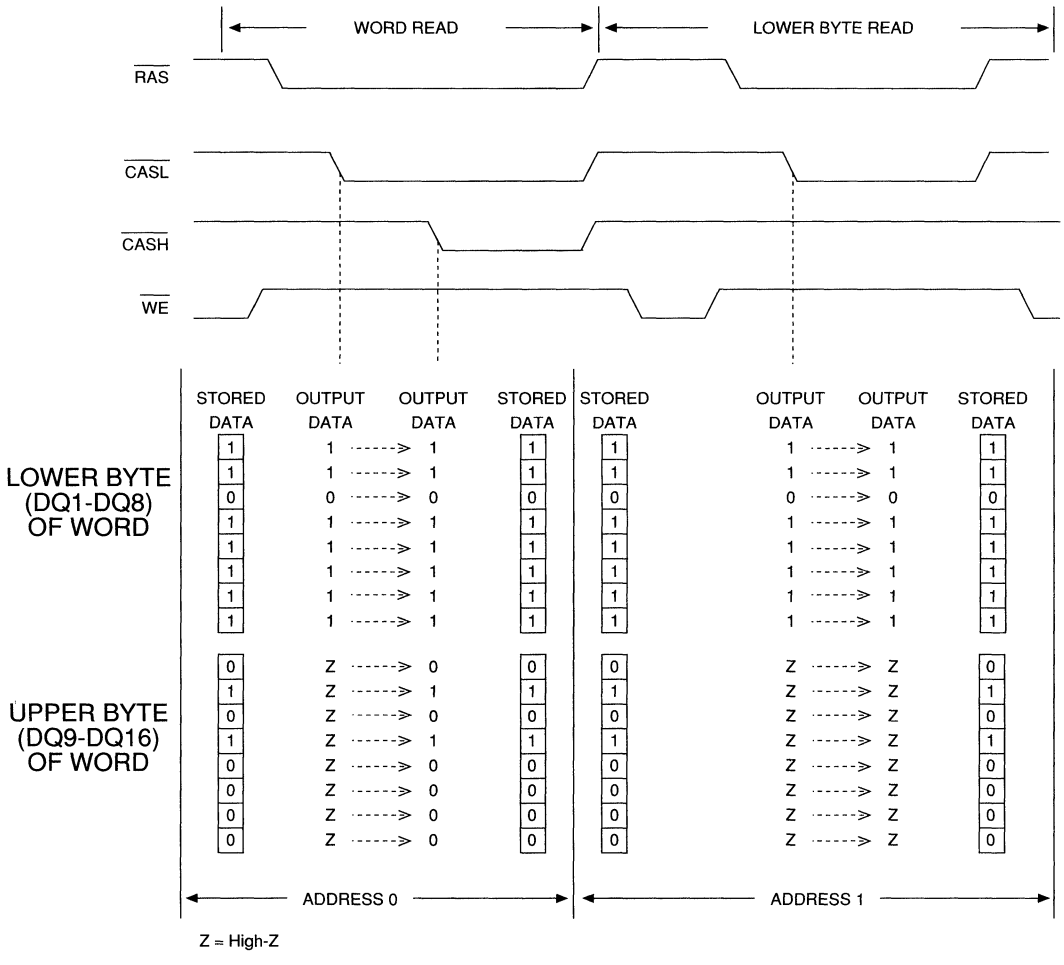


Figure 3
MT4C16257/9 WORD AND BYTE READ EXAMPLE

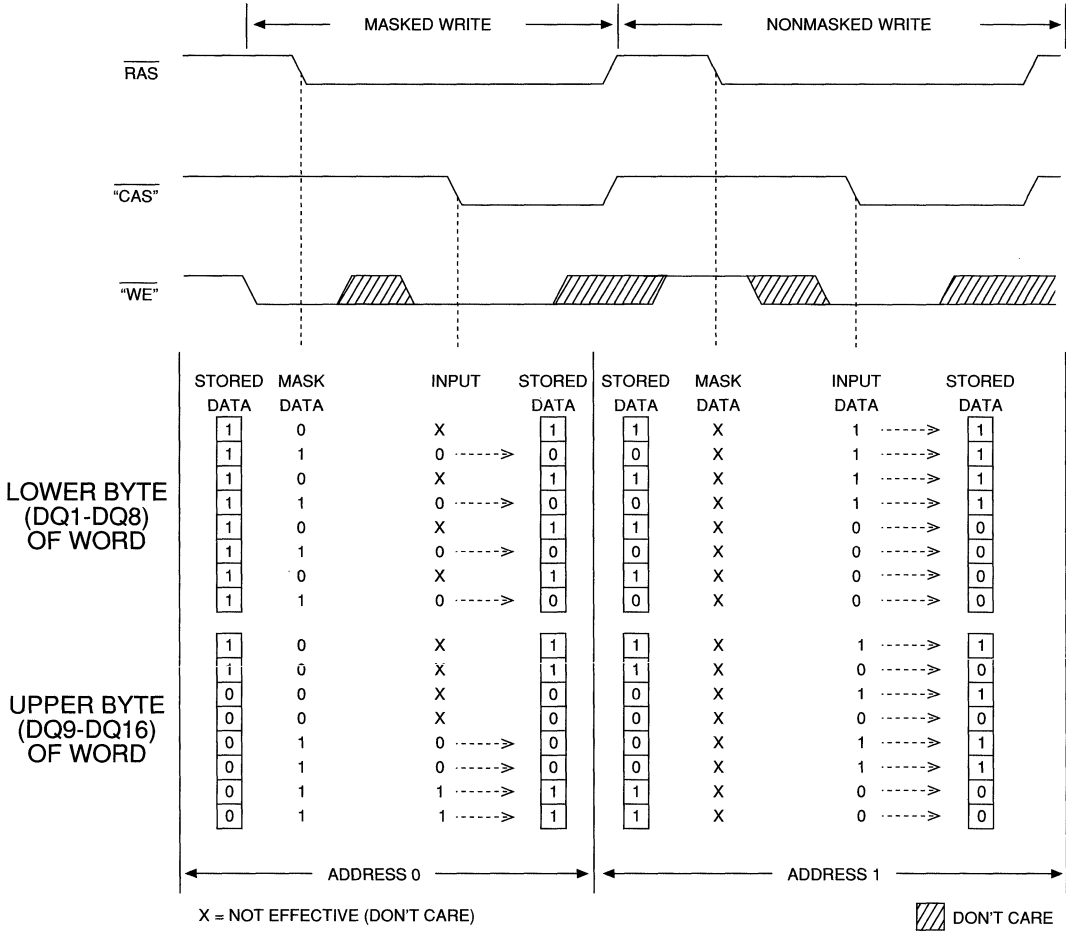


Figure 4
MT4C16258/9 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C16256/8

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WEL}$	$\overline{WEH}$	$\overline{OE}$	Addresses ^tR	Addresses ^tC	DQs	NOTES
Standby		H	X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Valid Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Valid Data In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Valid Data In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Valid Data In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1, 3
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Valid Data Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Valid Data Out	
PAGE-MODE WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Valid Data In	1, 3
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Valid Data In	1, 3
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1, 3
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Valid Data Out, Data In	1, 3
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Valid Data Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Valid Data In	1, 2, 3
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE:
1. These cycles may also be byte WRITE cycles (either $\overline{WEL}$ or $\overline{WEH}$ active).
2. EARLY-WRITE only.
3. Data in will be dependent on the mask provided (MT4C16258 only). Refer to Figure 4.

TRUTH TABLE: MT4C16257/9

Function		RAS	CASL	CASH	WE	OE	Addresses tR	Addresses tC	DQs	NOTES
Standby		H	X	X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Valid Data Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte,Valid Data Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte,Valid Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Valid Data In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Valid Data In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Valid Data In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1, 2, 5
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Valid Data Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Valid Data Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Valid Data In	1, 5
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Valid Data In	1, 5
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Valid Data Out, Data In	1, 2, 5
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Valid Data Out, Data In	1, 2, 5
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Valid Data Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Valid Data In	1, 3, 5
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be byte WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be byte READ cycles (either CASL or CASH active).
3. EARLY-WRITE only.
4. Only one of the two CAS must be active (CASL or CASH).
3. Data in will be dependent on the mask provided (MT4C16259 only). Refer to Figure 4.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, Ta (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	$V_{CC}+1$	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input ($0V \le V_{IN} \le V_{CC}$, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le V_{OUT} \le 5.5V$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	120	110	100	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	90	80	70	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	120	110	100	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	120	110	100	mA	3

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$/($\overline{CASL}$,$\overline{CASH}$), ($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		145		170		ns	
READ-WRITE cycle time	^tRWC	175		185		220		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		55		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		120		ns	35
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		30	ns	15, 33
Output enable time	^tOE		20		20		30	ns	33
Access time from column address	^tAA		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		50	ns	33
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	40
$\overline{RAS}$ precharge time	^tRP	50		55		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	30	100,000	ns	39
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	32
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 36
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		10		10		ns	36
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	25	60	ns	17, 31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	32
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	15	50	ns	18
Column address set-up time	^tASC	0		0		0		ns	31
Column address hold time	^tCAH	15		15		15		ns	31
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		ns	
Read command set-up time	^tRCS	0		0		0		ns	26, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26 ,32
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	33

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	tOFF	0	15	0	15	0	20	ns	20, 29, 33
Output disable time	tOD		10		12		20	ns	29, 41
Write command setup time	tWCS	0		0		0		ns	21, 26, 31
Write command hold time	tWCH	15		15		15		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	tWCR	50		55		65		ns	26
Write command pulse width	tWP	10		10		15		ns	26
Write command to $\overline{RAS}$ lead time	tRWL	20		20		20		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		20		20		ns	26, 32
Data-in setup time	tDS	0		0		0		ns	22, 33
Data-in hold time	tDH	15		15		20		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	50		55		65		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	90		100		125		ns	21
Column address to $\overline{WE}$ delay time	tAWD	60		65		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	45		45		60		ns	21, 31
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	tREF		8		8		8	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	5, 31
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	5, 32
MASKED WRITE command to $\overline{RAS}$ setup time	tWRS	0		0		0		ns	26, 27
MASKED WRITE command to $\overline{RAS}$ hold time	tWRH	15		15		15		ns	26, 27
Mask data to $\overline{RAS}$ setup time	tMS	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ hold time	tMH	15		15		15		ns	26, 27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	10		10		20		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during hidden refresh cycle	tORD	0		0		0		ns	
Last $\overline{CAS}$ going low to first $\overline{CAS}$ to return high	tCLCH	10		10		10		ns	34

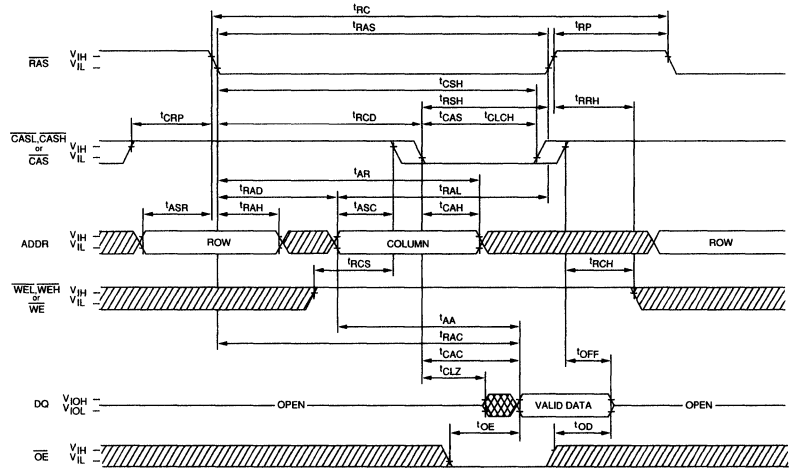
NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and Vcc = 5V.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.

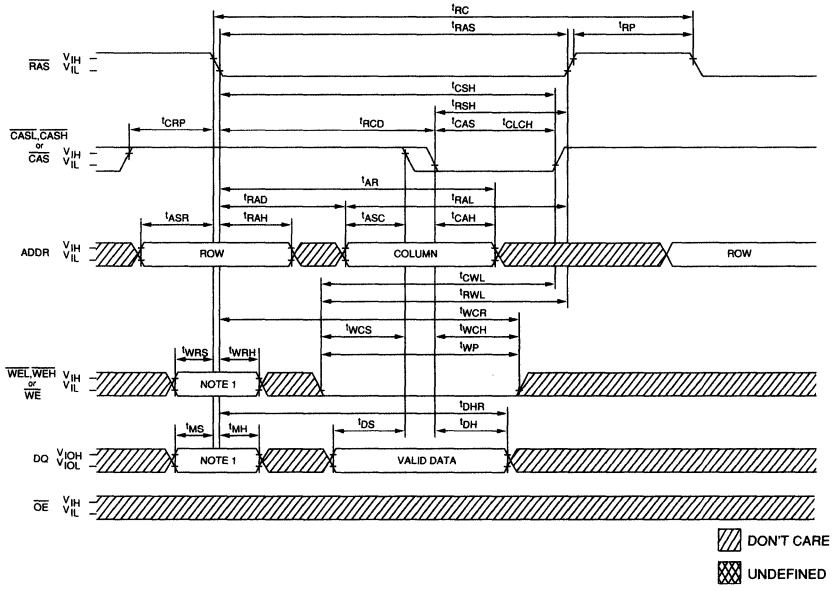
NOTES

7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 50pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ Controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C16256/8. Write command is defined as $\overline{WE}$ going LOW on the MT4C16257/9.
27. MT4C16258/9 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a don't care. If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a don't care; and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
30. Notes 31 through 41 apply to MT4C16257/9 only (*):
31. *The first $\overline{CASx}$ edge to transition low.
32. *The last $\overline{CASx}$ edge to transition high.
33. *Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ1-DQ8 by $\overline{CASH}$.
34. *Last falling $\overline{CASx}$ edge to first rising $\overline{CASx}$ edge.
35. *Last rising $\overline{CASx}$ edge to next cycle's last rising $\overline{CASx}$ edge.
36. *Last rising $\overline{CASx}$ edge to first falling $\overline{CASx}$ edge.
37. *First DQs controlled by the first $\overline{CASx}$ to go LOW.
38. *Last DQs controlled by the last $\overline{CASx}$ to go HIGH.
39. *Each $\overline{CASx}$ must meet minimum pulse width.
40. *Last $\overline{CASx}$ to go LOW.
41. *All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$

READ CYCLE

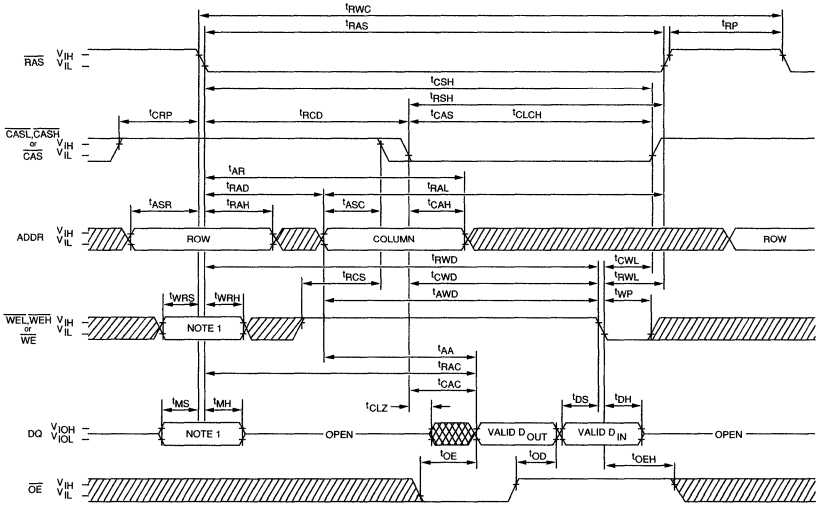


EARLY-WRITE CYCLE

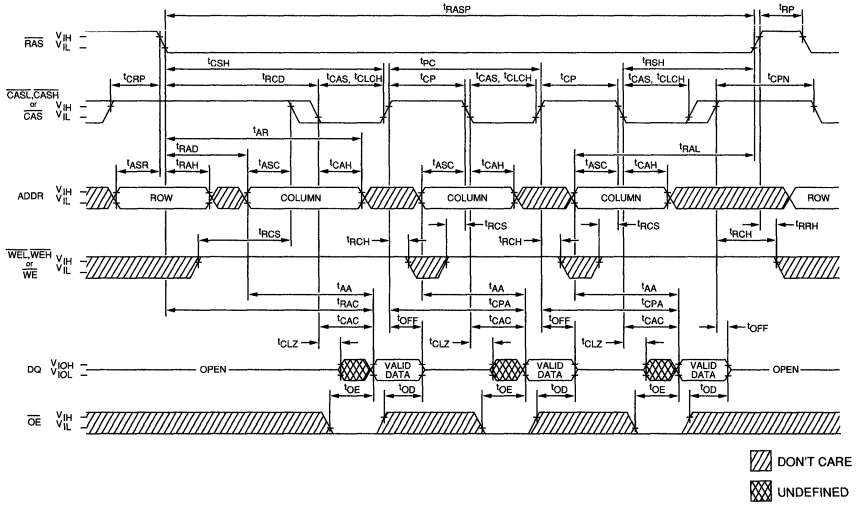


NOTE: 1. Applies to MT4C16258 and MT4C16259 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE: $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE: $\overline{WE}$ LOW at $\overline{RAS}$ time. $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

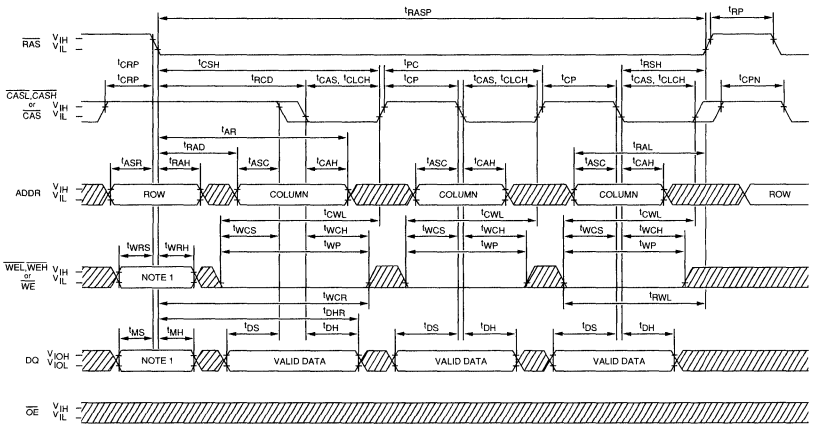


FAST PAGE-MODE READ CYCLE

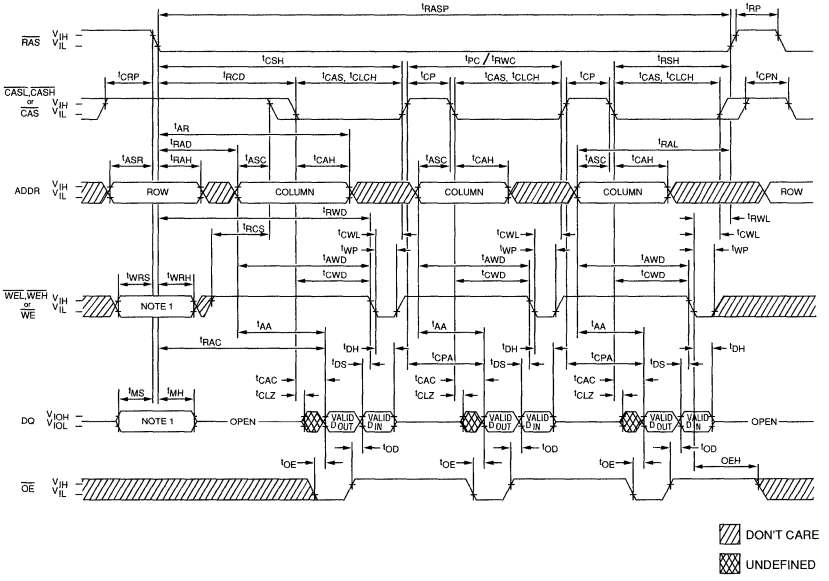


NOTE: 1. Applies to MT4C16258 and MT4C16259 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE: $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE: $\overline{WE}$ LOW at $\overline{RAS}$ time. $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at $\overline{RAS}$ time.

FAST PAGE-MODE EARLY-WRITE CYCLE



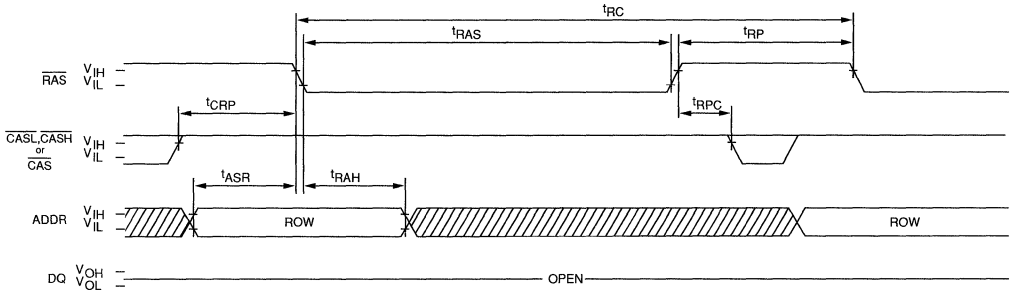
FAST PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C16258 and MT4C16259 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE: $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE: $\overline{WE}$ LOW at $\overline{RAS}$ time. $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at $\overline{RAS}$ time.

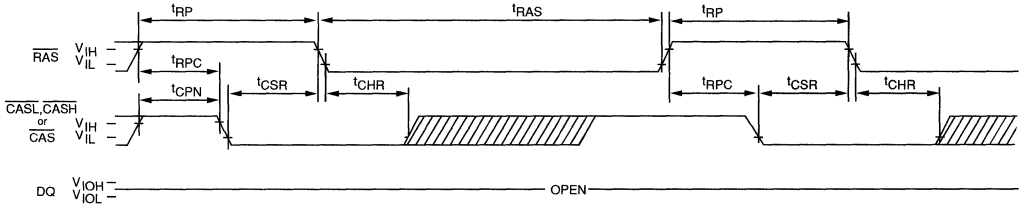
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7, $\overline{OE}$; $\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = DON'T CARE)



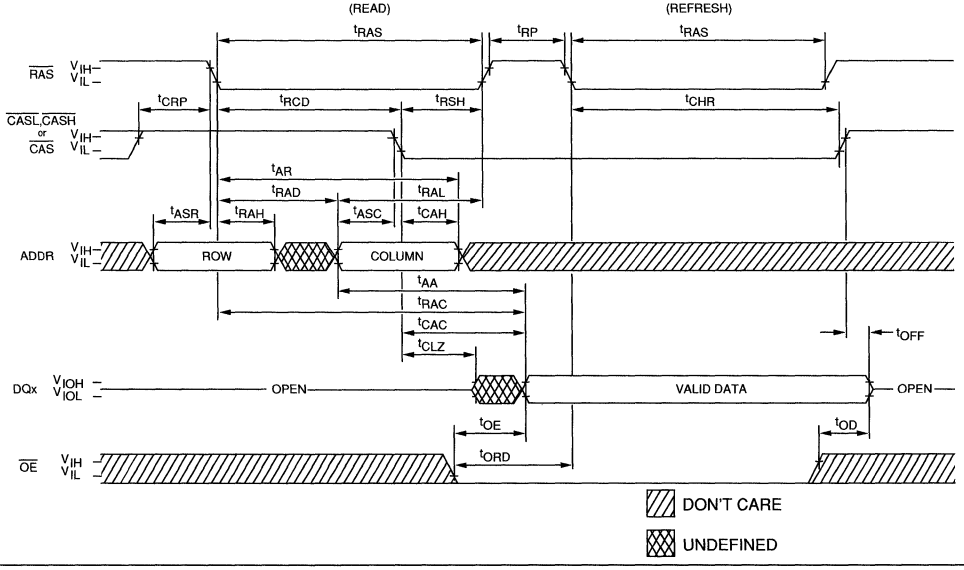
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_7; $\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$,and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = HIGH; $\overline{OE}$ = LOW) [24]



MICRON TECHNOLOGY, INC.

DRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package			Process	Page
				Standby	Active	SIP	SIMM	ZIP		
256K x 8	Fast Page Mode	MT2D2568	70, 80,100,120	6mW	350mW	30	30	-	CMOS	2-1
1 Meg x 8	Fast Page Mode	MT8D18	70, 80, 100	24mW	1,400mW	30	30	-	CMOS	2-11
1 Meg x 8	Fast Page Mode	MT2D18	60, 70, 80, 100	5mW	450mW	30	30	-	CMOS	2-21
4 Meg x 8	Fast Page Mode	MT8D48	60, 70, 80	24mW	1,800mW	30	30	-	CMOS	2-31
256K x 9	Fast Page/Page Mode	MT3D2569	70, 80, 100,120	9mW	625mW	30	30	-	C/NMOS	2-41
1 Meg x 9	Fast Page Mode	MT9D19	70, 80, 100	27mW	1,575mW	30	30	-	CMOS	2-51
1 Meg x 9	Fast Page Mode	MT3D19	70, 80, 100	9mW	625mW	30	30	-	CMOS	2-61
4 Meg x 9	Fast Page Mode	MT9D49	60, 70, 80	27mW	2,025mW	30	30	-	CMOS	2-71
256K x 32	Fast Page Mode	MT8D25632	70, 80, 85,100	24mW	1,400mW	-	72	72	CMOS	2-81
512K x 32	Fast Page Mode	MT16D51232	70, 80, 85, 100	48mW	2,800mW	-	72	72	CMOS	2-91
1 Meg x 32	Fast Page Mode	MT8D132	70, 80, 100	24mW	1,800mW	-	72	72	CMOS	2-101
2 Meg x 32	Fast Page Mode	MT16D232	70, 80, 100	48mW	3,600mW	-	72	72	CMOS	2-111
256K x 36	Fast Page Mode	MT9D25636	70, 80, 85,100	27mW	1,515mW	-	72	72	CMOS	2-121
256K x 36	Fast Page Mode	MT10D25636	70, 80, 85,100	30mW	1,750mW	-	72	72	CMOS	2-131
512K x 36	Fast Page Mode	MT18D51236	70, 80, 85,100	54mW	3,150mW	-	72	72	CMOS	2-141
512K x 36	Fast Page Mode	MT20D51236	70, 80, 85,100	60mW	1,780mW	-	72	72	CMOS	2-151
1 Meg x 36	Fast Page Mode	MT9D136	70, 80, 100	27mW	2,175mW	-	72	72	CMOS	2-161
2 Meg x 36	Fast Page Mode	MT18D236	70, 80, 100	54mW	4,500mW	-	72	72	CMOS	2-171

DRAM MODULE

256K x 8 DRAM

FAST PAGE MODE

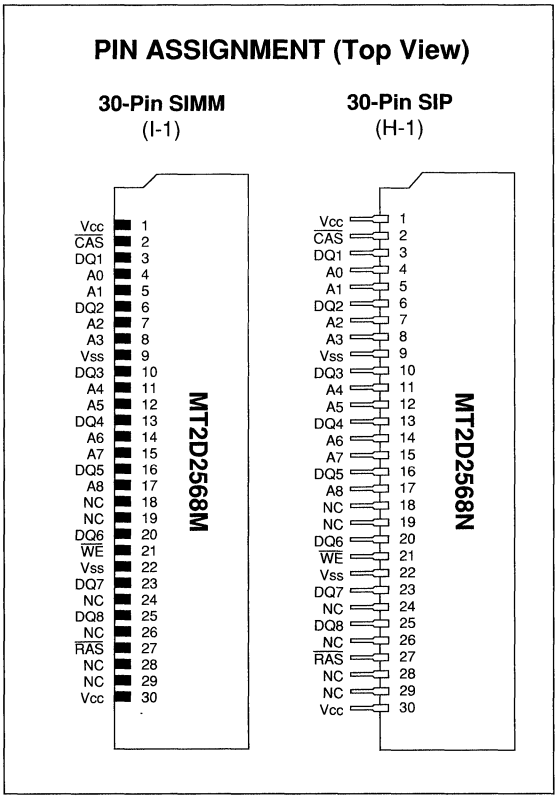
FEATURES

- Industry standard pinout in a 30-pin single-in-line memory module
- High-performance, CMOS silicon gate process
- Single 5V ±10% power supply
- Low power, 6mW standby; 350mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Optional FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh distributed across 8ms

OPTIONS

	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N

PIN ASSIGNMENT (Top View)



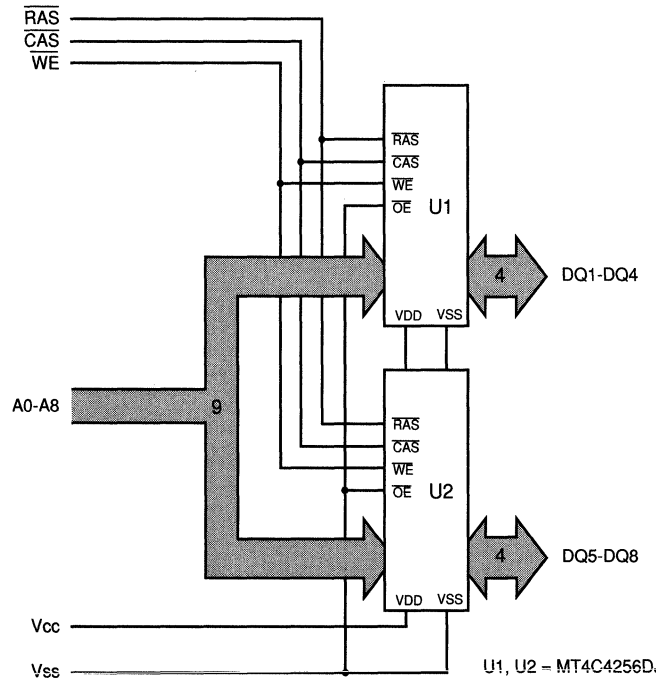
GENERAL DESCRIPTION

The MT2D2568 is a randomly accessed solid-state memory containing 262,144 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY-WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	DQ1-8
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Valid Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Valid Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN	READ	L→H→L	L	H	ROW	COL	Valid Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-2.0	0.8	V	1, 22
INPUT LEAKAGE Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	A0-A8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	I_I	-4	4	µA	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	DQ1-8	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	1
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	-12	UNITS	NOTES
STANDBY CURRENT: TTL Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	4	4	4	4	mA	
STANDBY CURRENT: CMOS Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	2	2	2	2	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC3}	160	140	120	100	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC4}	120	100	80	60	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH}; ^tRC = ^tRC (MIN))	I_{CC5}	160	140	120	100	mA	3, 4
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$	I_{CC6}	160	140	120	100	mA	3, 4

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		10	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		14	pF	18
Input/Output Capacitance: DQ	C_{IO}		14	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	135		150		180		220		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		55		70		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a		n/a	21
Access time from $\overline{RAS}$	^tRAC		70		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		25		30	ns	15
Output Enable	^tOE		20		20		25		30	ns	
Access time from column address	^tAA		35		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		50		65	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	30	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		20		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		10		ns	
Row address setup time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	10		10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	20	50	20	60	ns	18
Column address setup time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		60		ns	
Read command setup time	^tRCS	0		0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

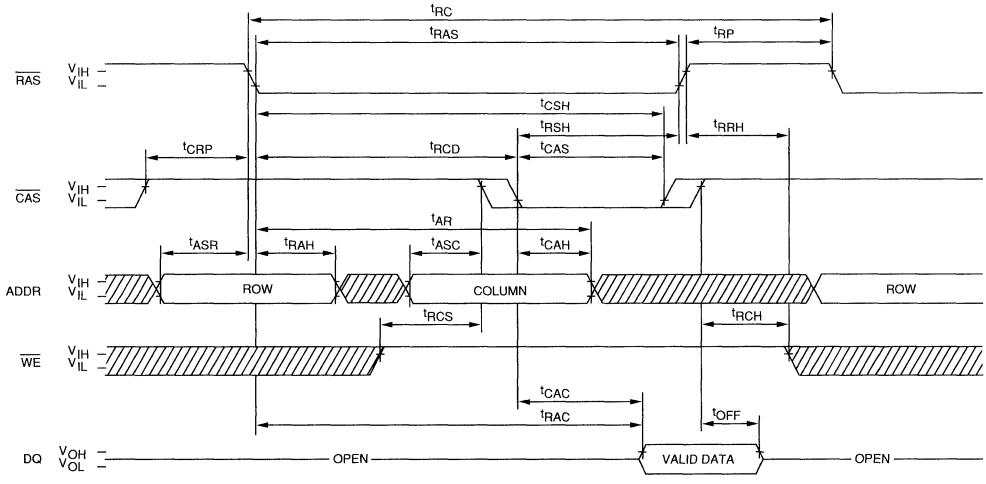
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	0	35	ns	20
Output Disable	^tOD		20		20		20		20	ns	
$\overline{WE}$ command setup time	^tWCS	0		0		0		0		ns	
Write command hold time	^tWCH	15		15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		85		ns	
Write command pulse width	^tWP	15		15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		30		ns	
Data-in setup time	^tDS	0		0		0		0		ns	
Data-in hold time	^tDH	15		15		20		25		ns	
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	n/a		n/a		n/a		n/a		n/a	21
Column address to $\overline{WE}$ delay time	^tAWD	n/a		n/a		n/a		n/a		n/a	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	n/a		n/a		na		n/a		n/a	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		8		8		8		8	ms	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	15		15		15		15		ns	19
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	n/a		n/a		n/a		n/a		n/a	21

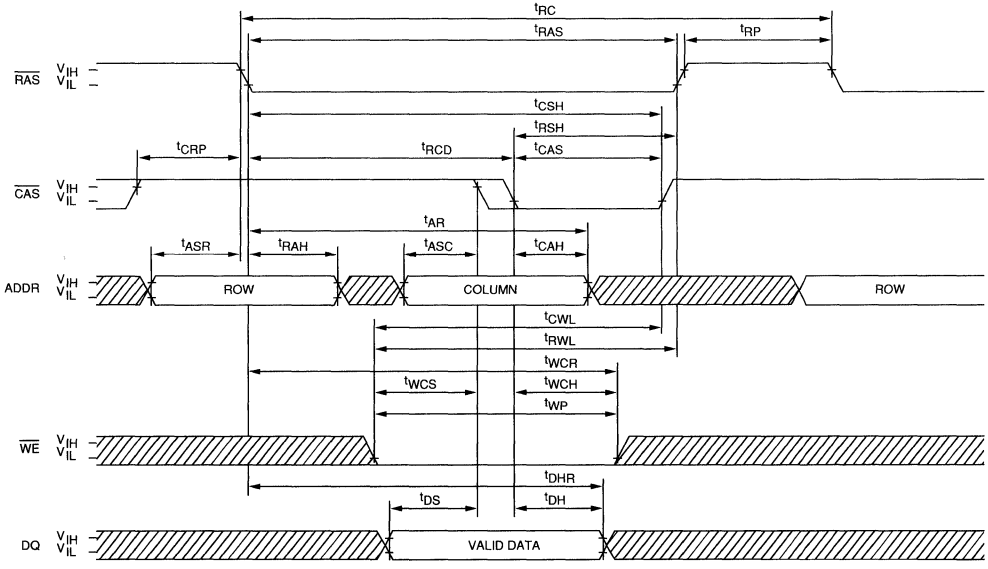
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\,^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1 and U2.
22. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

READ CYCLE



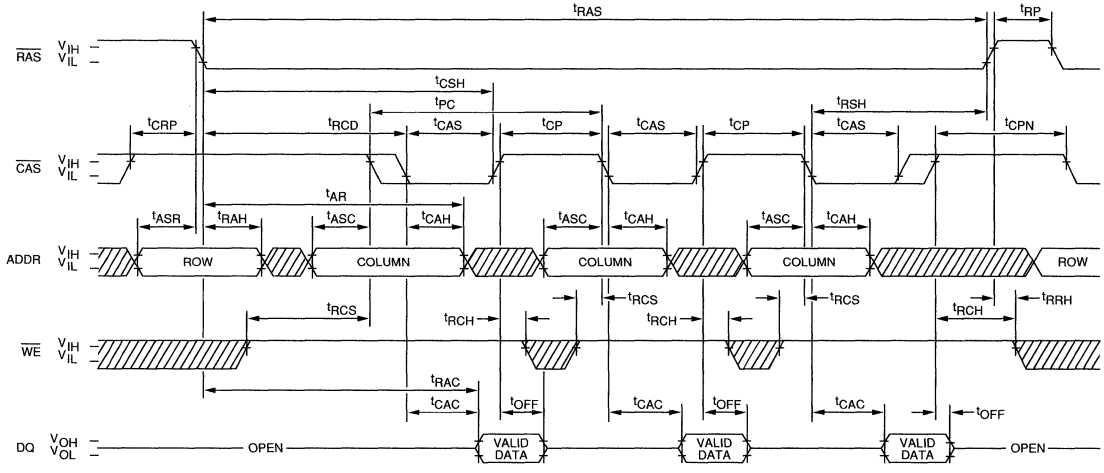
EARLY-WRITE CYCLE



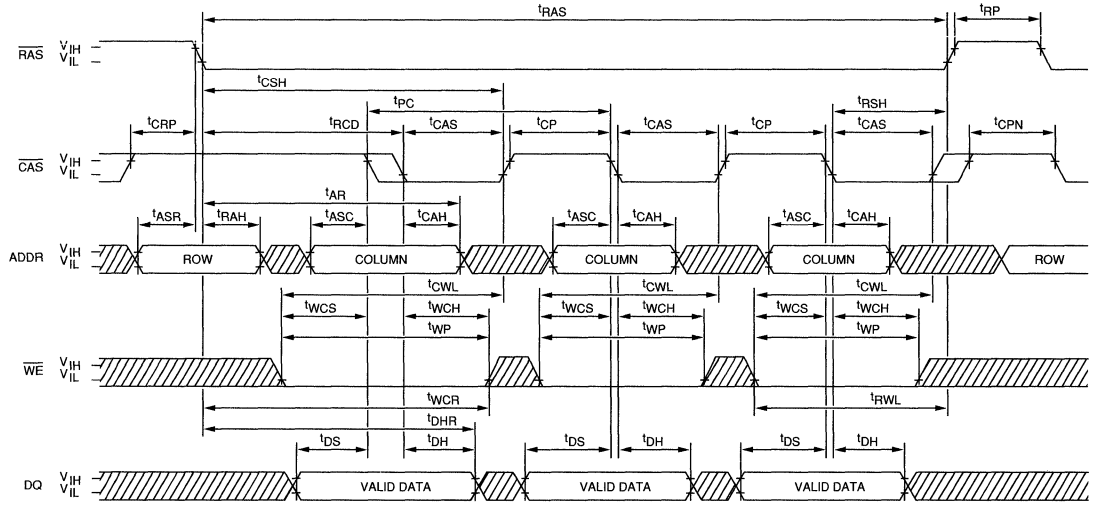
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



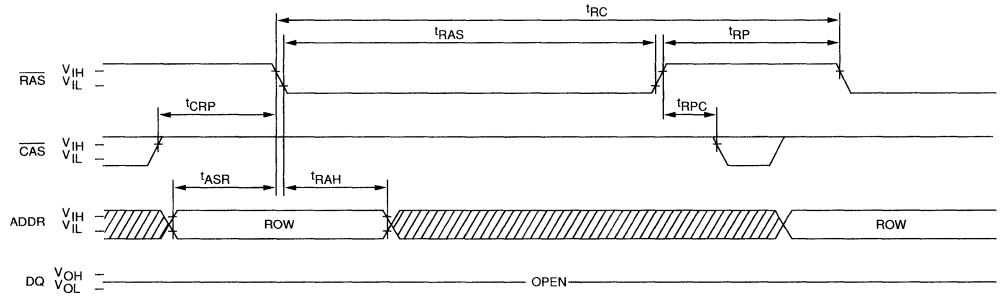
FAST-PAGE-MODE EARLY-WRITE CYCLE



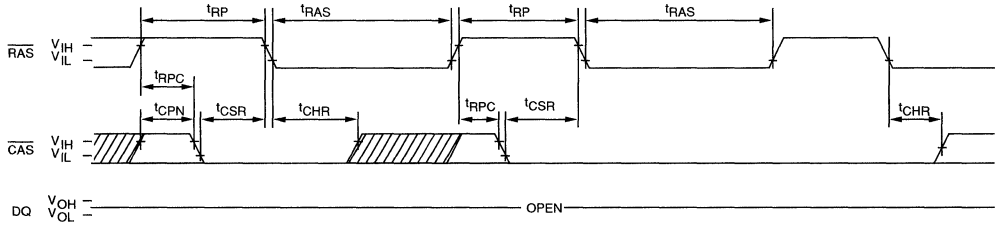
DON'T CARE

UNDEFINED

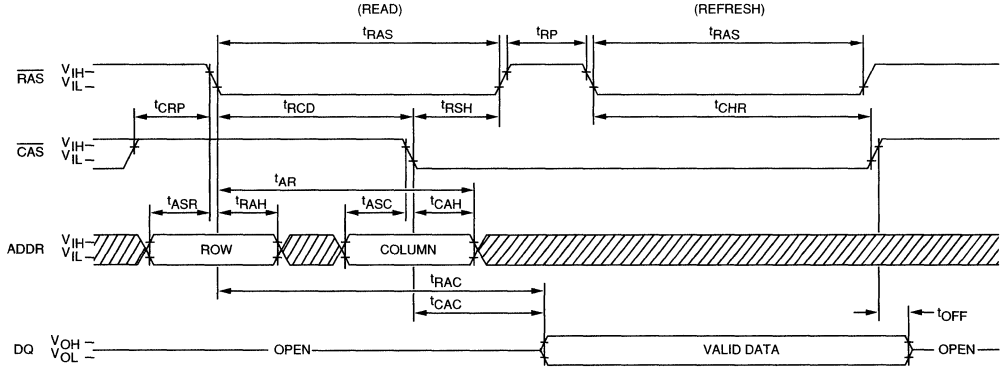
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A_0 - A_8 ; and $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A_0 - A_8 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH) [20]



DRAM MODULE

1 MEG x 8 DRAM

FAST PAGE MODE

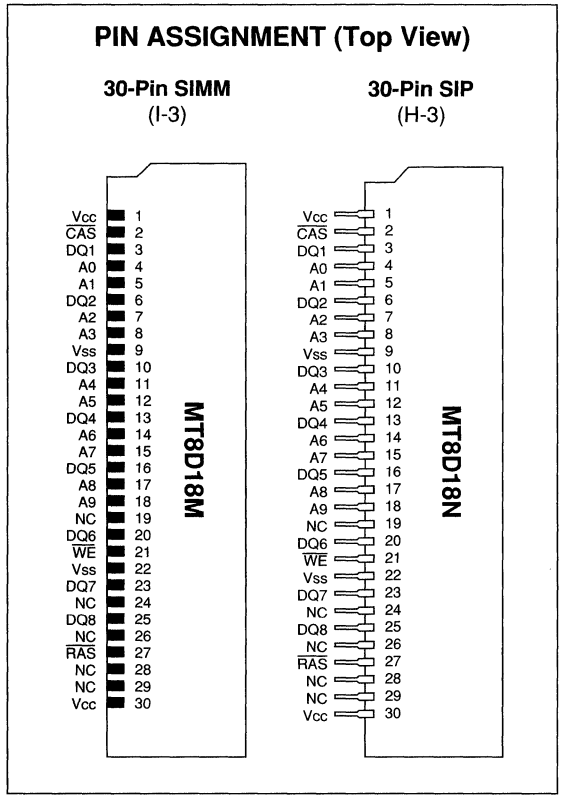
FEATURES

- Industry standard pinout in a 30-pin single-in-line package
- High-performance CMOS silicon gate process
- Single 5V ±10% power supply
- Low power, 24mW standby; 1400mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh distributed across 8ms
- Optional FAST PAGE MODE access cycle

OPTIONS

	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N

PIN ASSIGNMENT (Top View)



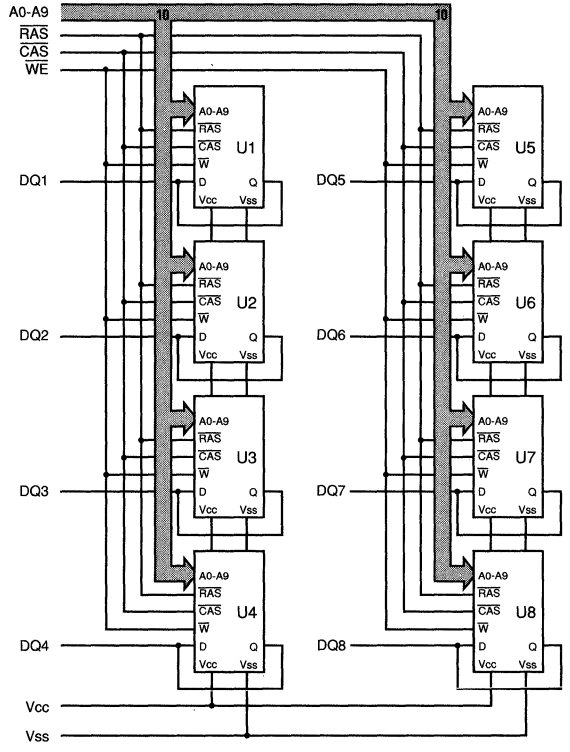
GENERAL DESCRIPTION

The MT8D18 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Early WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycles (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1 - U8 = MT4C1024DJ

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tA	DQ1-8
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-2.0	0.8	V	1, 25
INPUT LEAKAGE: Any Input 0V ≤ V_{IN} ≤ V_{CC}, (All other pins not under test = 0V)	D9, $\overline{CAS9}$	I_I	-2	2	µA	
	A0-A9, $\overline{RAS}$, $\overline{WE}$	I_I	-16	16	µA	
OUTPUT LEAKAGE: (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	Q9	I_{OZ}	-10	10	µA	
	DQ1-8	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output HighVoltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	MAX -10	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	16	mA	
STANDBY CURRENT: CMOS Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	8	8	8	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC3}	640	560	480	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC4}	480	400	320	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH}; ^tRC = ^tRC (MIN))	I_{CC5}	640	560	480	mA	3, 4
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC6}	640	560	480	mA	3, 4

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		45	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		63	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	24
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a	24
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	15
Access time from column address	^tAA		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		50	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	40	15	40	20	50	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

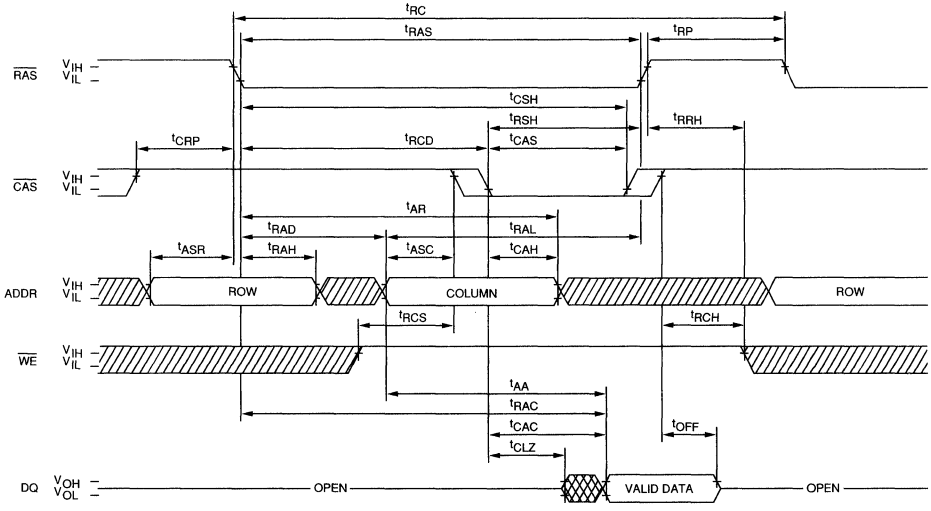
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq 75°C$; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	15		15		20		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	n/a		n/a		n/a		n/a	25
Column address to $\overline{WE}$ delay time	^tAWD	n/a		n/a		n/a		n/a	25
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	n/a		n/a		n/a		n/a	25
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	15		15		15		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	n/a		n/a		n/a		n/a	25

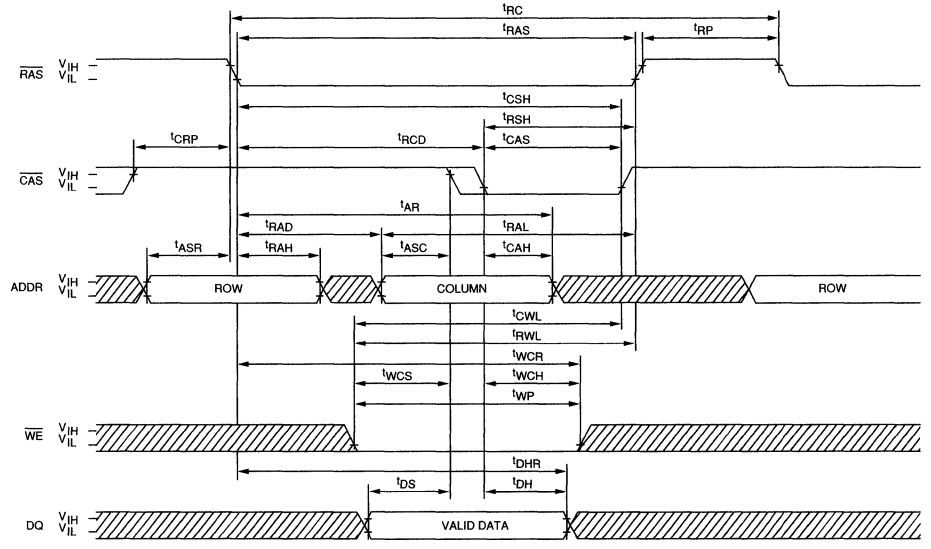
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ${}^{t}T$ = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ${}^{t}RCD < {}^{t}RCD$ (MAX). If ${}^{t}RCD$ is greater than the maximum recommended value shown in this table, ${}^{t}RAC$ will increase by the amount that ${}^{t}RCD$ exceeds the value shown.
15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ${}^{t}CPN$.
17. Operation within the ${}^{t}RCD$ (MAX) limit ensures that ${}^{t}RAC$ (MAX) can be met. ${}^{t}RCD$ (MAX) is specified as a reference point only; if ${}^{t}RCD$ is greater than the specified ${}^{t}RCD$ (MAX) limit, then access time is controlled exclusively by ${}^{t}CAC$.
18. Operation within the ${}^{t}RAD$ (MAX) limit ensures that ${}^{t}RCD$ (MAX) can be met. ${}^{t}RAD$ (MAX) is specified as a reference point only; if ${}^{t}RAD$ is greater than the specified ${}^{t}RAD$ (MAX) limit, then access time is controlled exclusively by ${}^{t}AA$.
19. Either ${}^{t}RCH$ or ${}^{t}RRH$ must be satisfied for a READ cycle.
20. ${}^{t}OFF$ (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. All other inputs equal Vcc -0.2V.
24. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
25. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

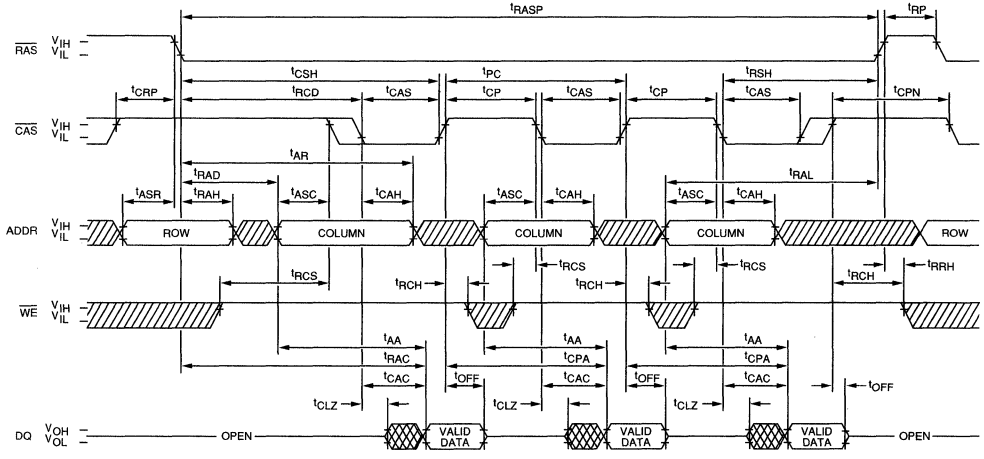
READ CYCLE



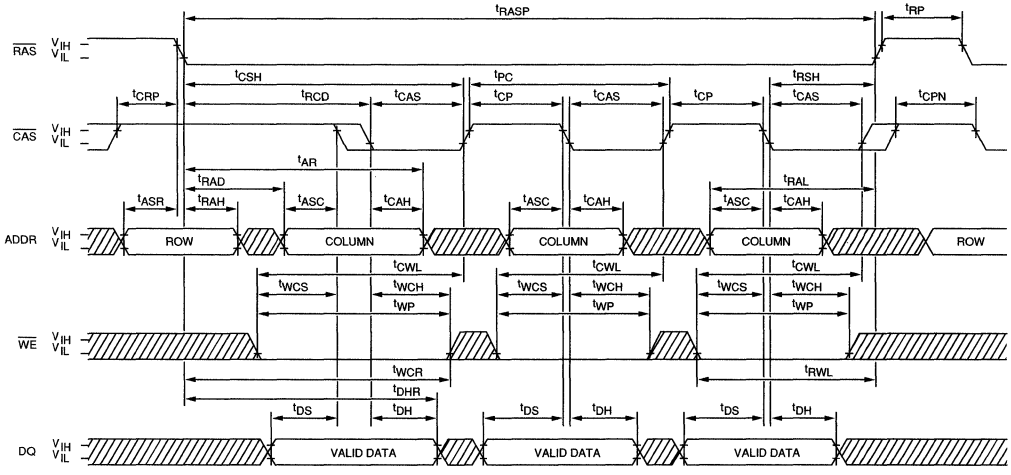
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE



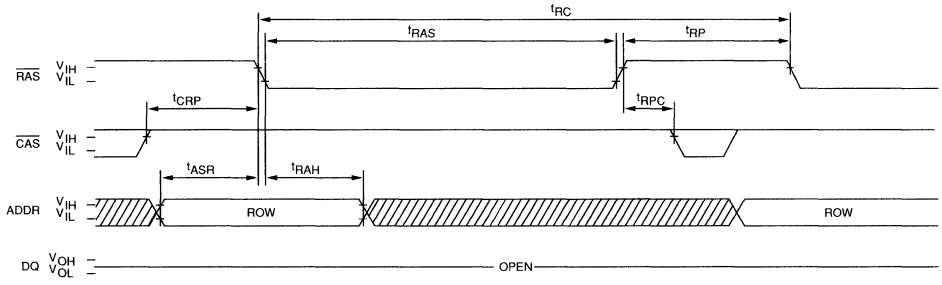
FAST-PAGE-MODE EARLY-WRITE CYCLE



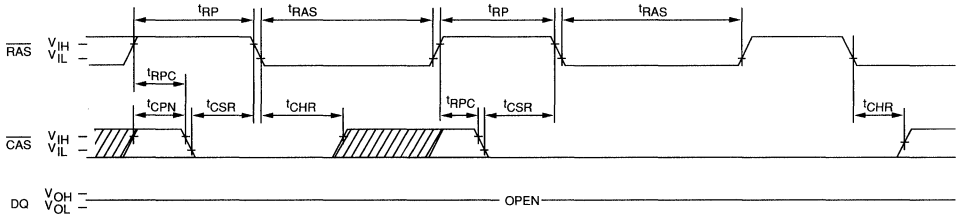
DON'T CARE

UNDEFINED

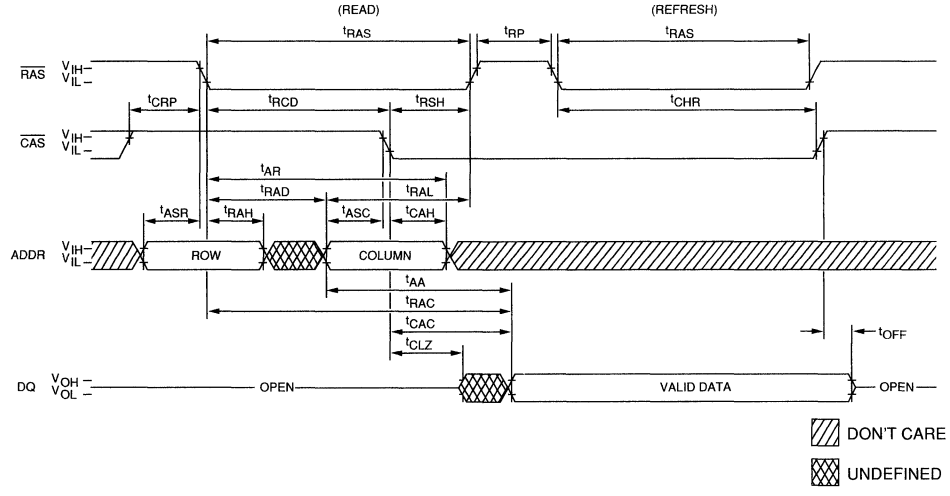
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH) [22]



DRAM MODULE

1 MEG x 8 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pinout in a 30-pin, single-in-line memory module
- High-performance, CMOS silicon gate process
- Single 5V ±10% power supply
- Low power, 5mW standby; 450mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Optional FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 1,024-cycle refresh distributed across 16ms

OPTIONS MARKING

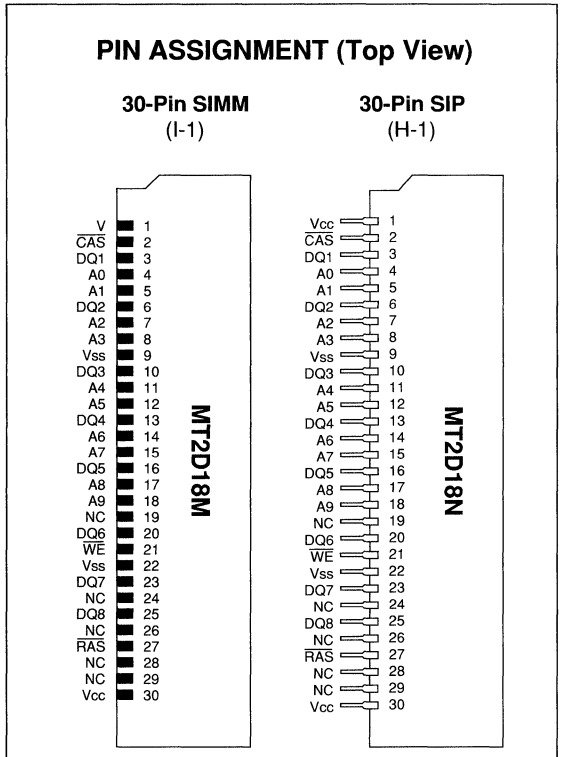
- Timing

60ns access	- 6
70ns access	- 7
80ns access	- 8
100ns access	-10

- Packages

Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N

PIN ASSIGNMENT (Top View)



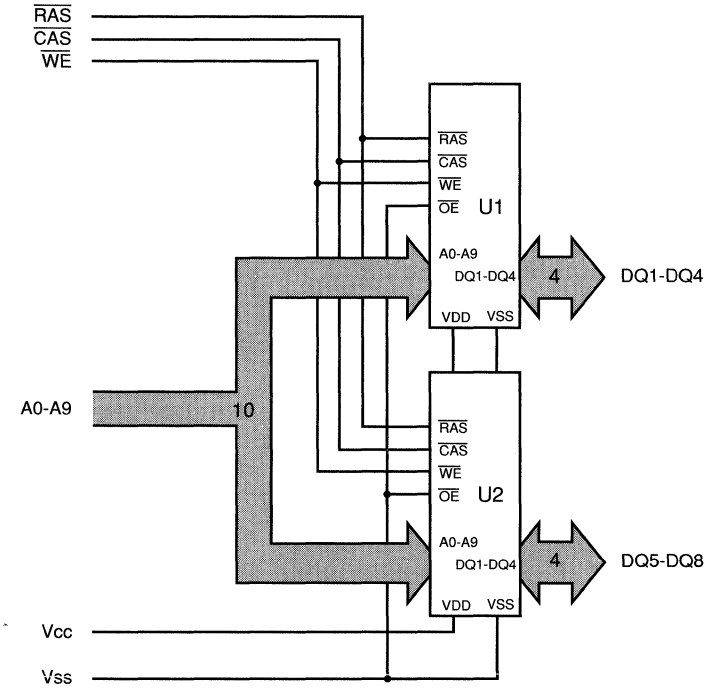
GENERAL DESCRIPTION

The MT2D18 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Early WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1, U2 = MT4C4001DJ

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	DQ1-8
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Valid Data Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Valid Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN	READ	L→H→L	L	H	ROW	COL	Valid Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Any Input $0V \le V_{IN} \le V_{CC}$ (All other pins not under test = 0V)	A0-A9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	I_I	-4	4	µA	
OUTPUT LEAKAGE (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	DQ1-DQ8	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	1
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: TTL Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	4	4	4	4	mA	
STANDBY CURRENT: CMOS Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	2	2	2	2	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC3}	220	200	180	160	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC4}	160	140	120	100	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH}; ^tRC = ^tRC (MIN))	I_{CC5}	220	200	180	160	mA	3, 4
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$	I_{CC6}	220	200	180	160	mA	3, 4

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		10	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		14	pF	18
Input/Output Capacitance: DQ	C_{IO}		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	110		130		150		180		ns	
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE cycle time	tPC	40		40		45		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	n/a		n/a		n/a		n/a		n/a	21
Access time from $\overline{RAS}$	tRAC		60		70		80		100	ns	14
Access time from $\overline{CAS}$	tCAC		15		20		20		25	ns	15
Access time from column address	tAA		30		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		40		45		50	ns	
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		25		ns	
$\overline{RAS}$ precharge time	tRP	45		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	15	100,000	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		100		ns	
$\overline{CAS}$ precharge time	tCPN	10		10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	15	45	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address setup time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		15		ns	
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	20	50	ns	18
Column address setup time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	tAR	50		55		60		70		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		50		ns	
Read command setup time	tRCS	0		0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

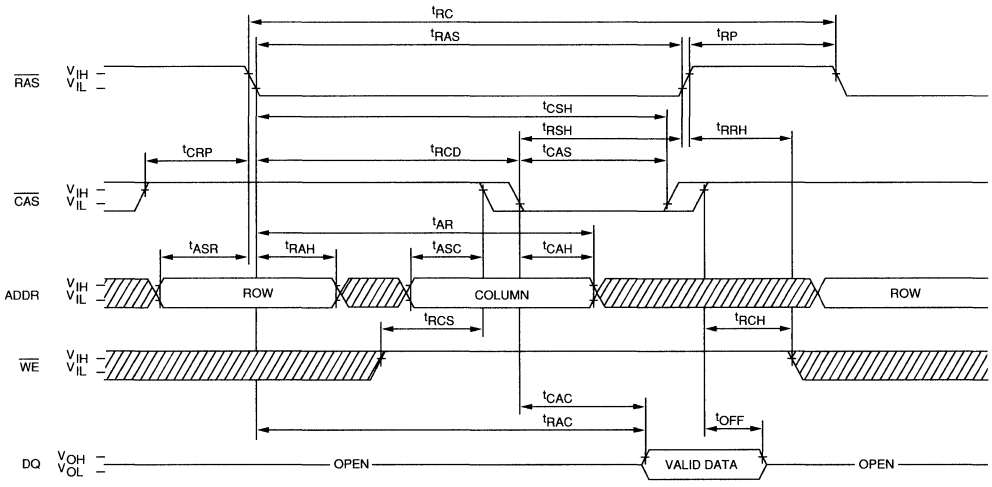
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-6		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		0		ns	
Write command hold time	^tWCH	10		15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		70		ns	
Write command pulse width	^tWP	10		15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		25		ns	
Data-in setup time	^tDS	0		0		0		0		ns	
Data-in hold time	^tDH	10		15		15		20		ns	
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		70		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	n/a		n/a		n/a		n/a		n/a	21
Column address to $\overline{WE}$ delay time	^tAWD	n/a		n/a		n/a		n/a		n/a	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	n/a		n/a		n/a		n/a		n/a	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		16		16		16		16	ms	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	15		15		15		15		ns	19
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	n/a		n/a		n/a		n/a		n/a	21

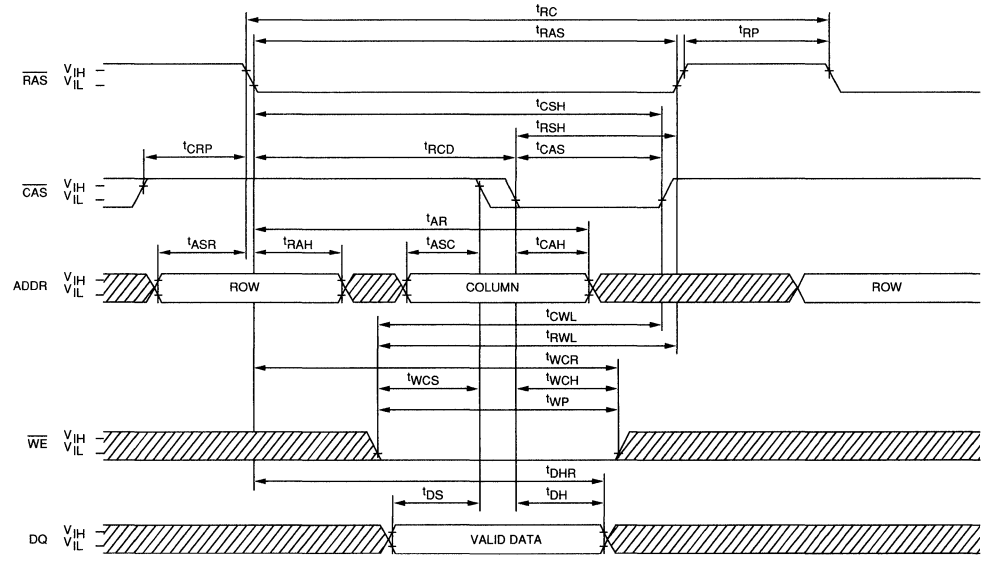
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\,^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1 and U2.

READ CYCLE



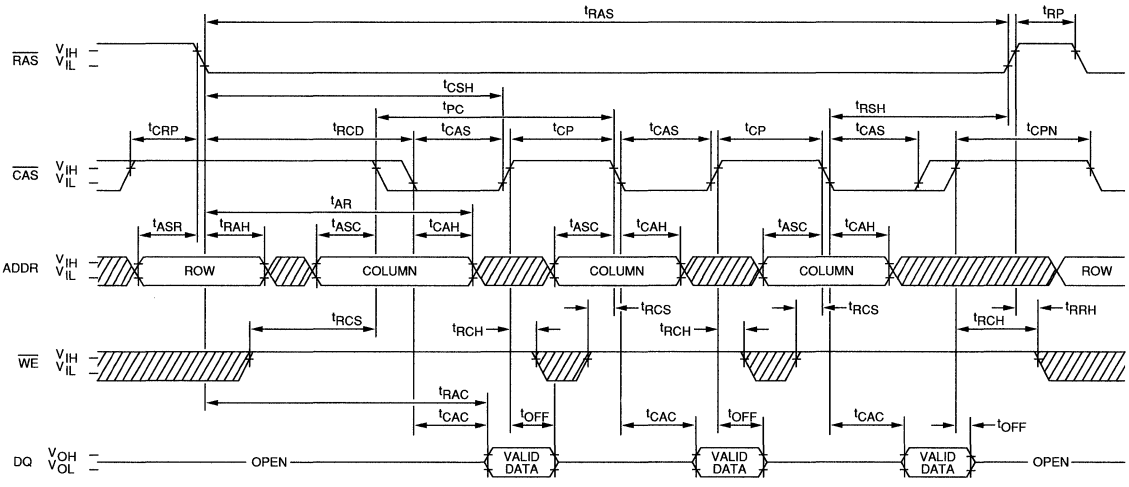
EARLY-WRITE CYCLE



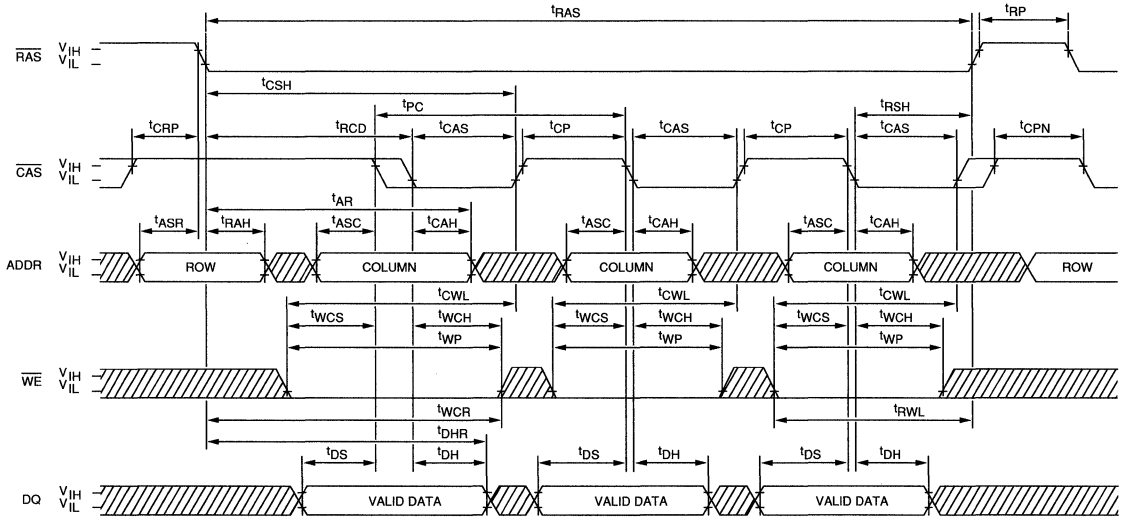
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



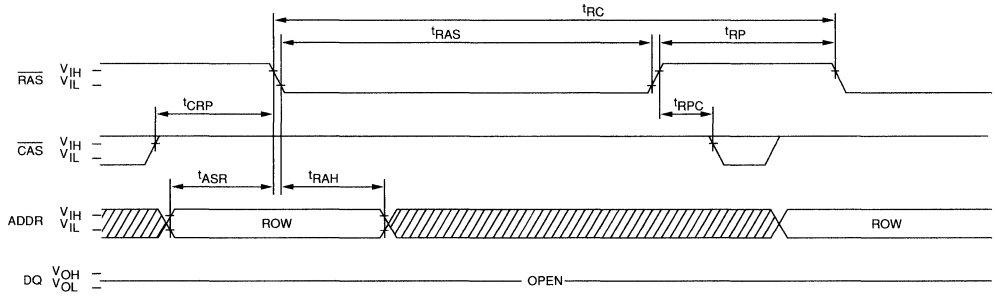
FAST-PAGE-MODE EARLY-WRITE CYCLE



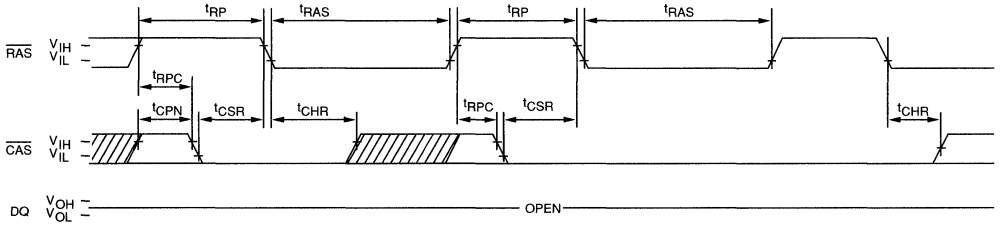
DON'T CARE

UNDEFINED

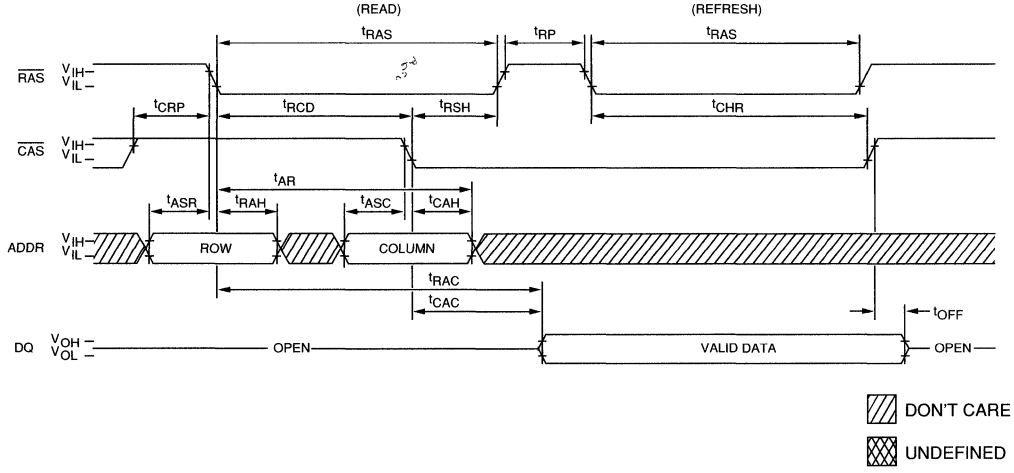
$\overline{RAS}$-ONLY REFRESH CYCLE
($ADDR = A_0 - A_9$; $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
($A_0 - A_9$ and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH) [20]



DRAM MODULE

4 MEG x 8 DRAM

FAST PAGE MODE

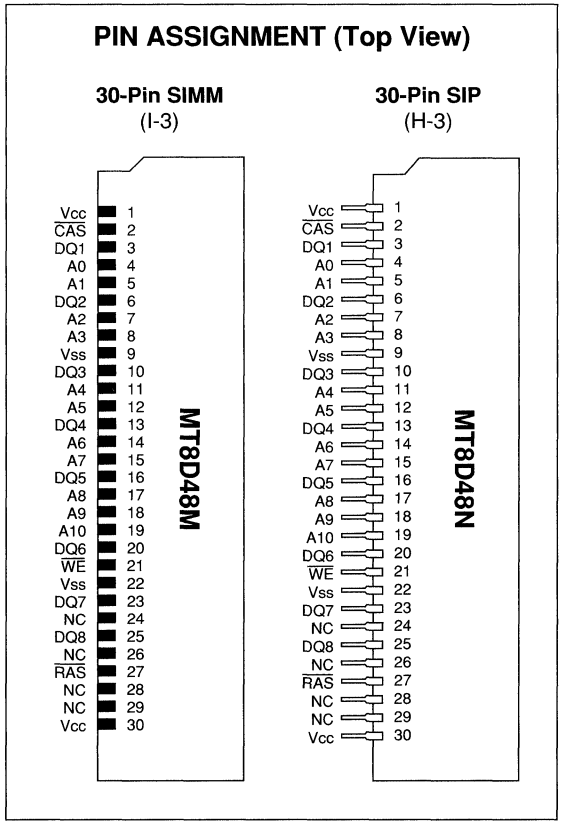
FEATURES

- Industry standard pinout in a 30-pin single-in-line package
- High-performance CMOS silicon gate process
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 24mW standby; 1,800mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

• Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
• Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N

PIN ASSIGNMENT (Top View)



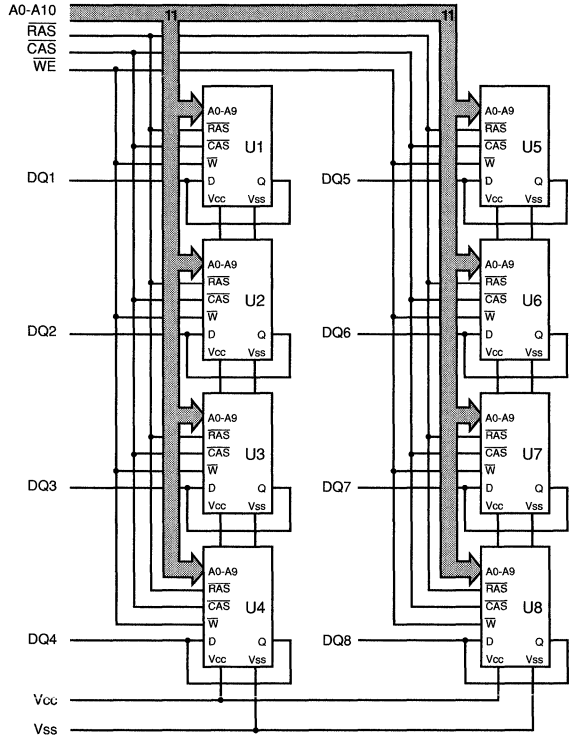
GENERAL DESCRIPTION

The MT8D48 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x8 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode, while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. EARLY-WRITE occurs when WE goes LOW prior to CAS going LOW, and the ouput remains open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A10) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C1004DJ

TRUTH TABLE

Function		RAS	CAS	CAS9	WE	Addresses tR	Addresses tA	DQ1-8
Standby		H	X	X	X	X	X	High Impedance
READ		L	L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H	ROW	COL	Valid Data Out
READ	2nd Cycle	L	H→L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Valid Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High Impedance
HIDDEN	READ	L→H→L	L	L	H	ROW	COL	Valid Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH	Standard	H→L	L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input: 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	A0-A10, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$	I_I	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	DQ1-DQ8	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	16	mA	
STANDBY CURRENT (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	8	8	8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	880	800	720	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	640	560	480	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	880	800	720	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	880	800	720	mA	3

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		45	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{WE}$	C_{I2}		63	pF	2
Output Capacitance: Q	C_O		7	pF	2
Input Capacitance: D	C_{I3}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
READ-WRITE cycle time	t_{RWC}	n/a		n/a		n/a		n/a	24
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	n/a		n/a		n/a		n/a	24
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	15
Access time from column address	t_{AA}		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		40		45	ns	25
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

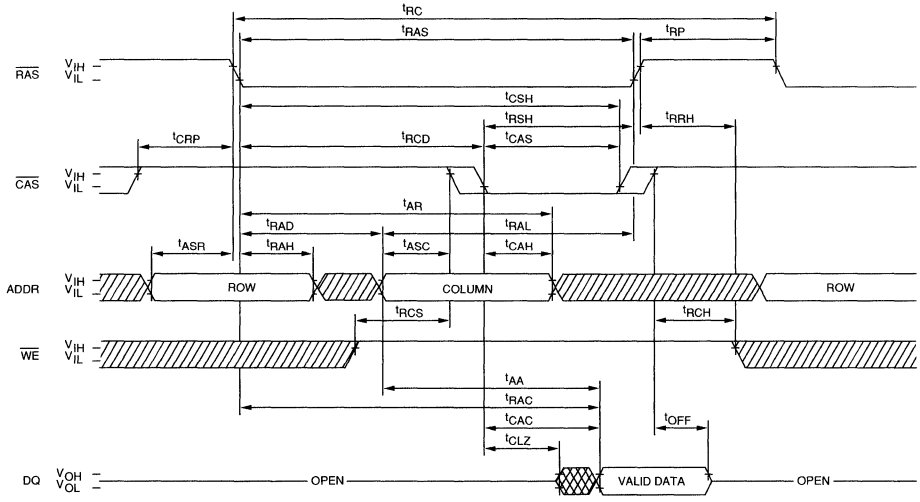
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	20		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	21
Data-in hold time	tDH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	n/a		n/a		n/a		n/a	24
Column address to $\overline{WE}$ delay time	tAWD	n/a		n/a		n/a		n/a	24
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	n/a		n/a		n/a		n/a	24
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCHR	15		15		15		ns	5

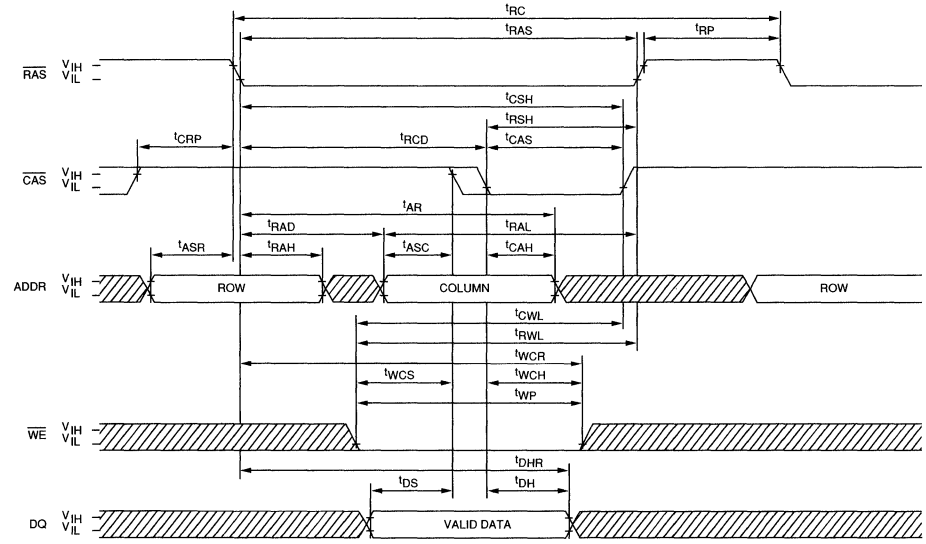
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. All other inputs equal Vcc -0.2V.
24. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.

READ CYCLE



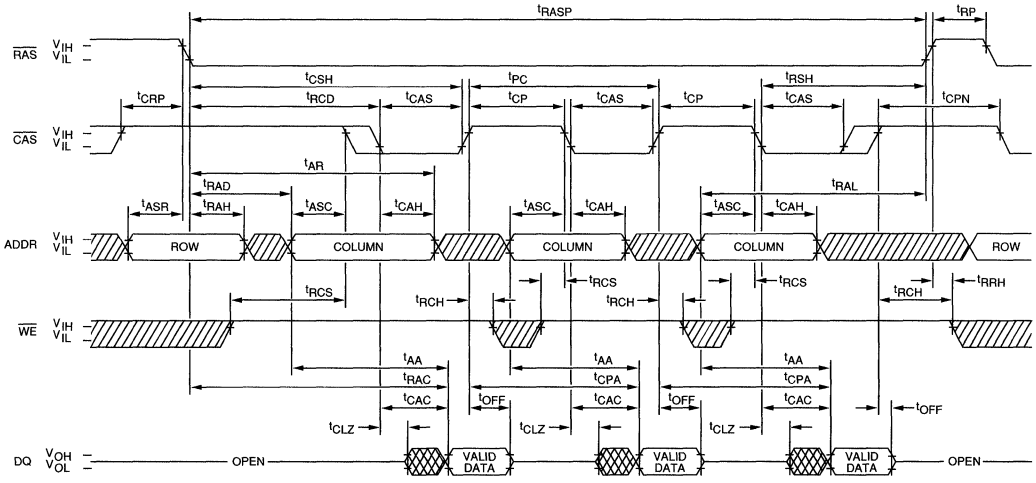
EARLY-WRITE CYCLE



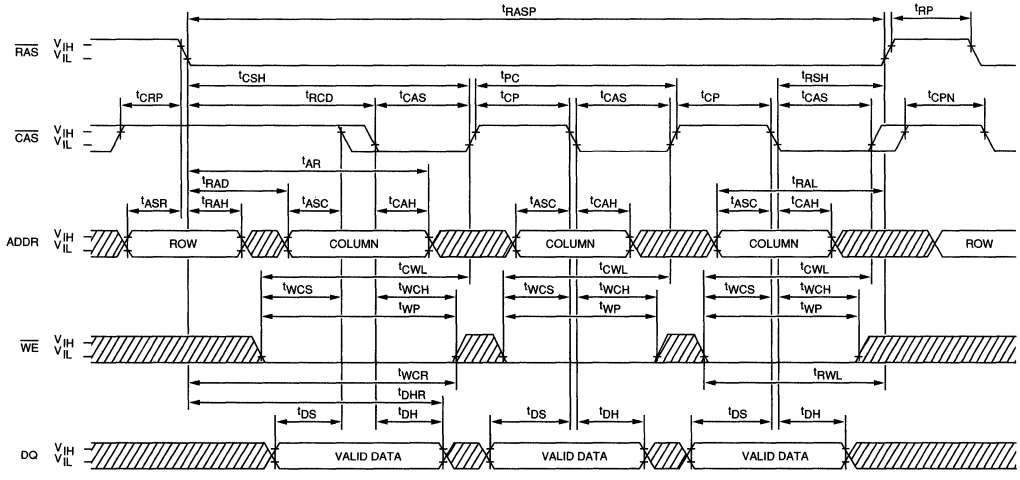
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

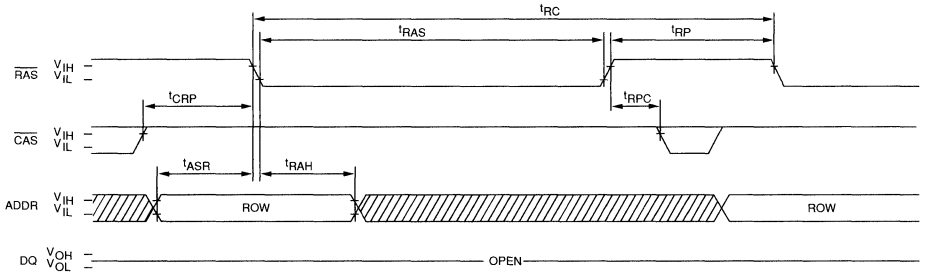


DON'T CARE

UNDEFINED

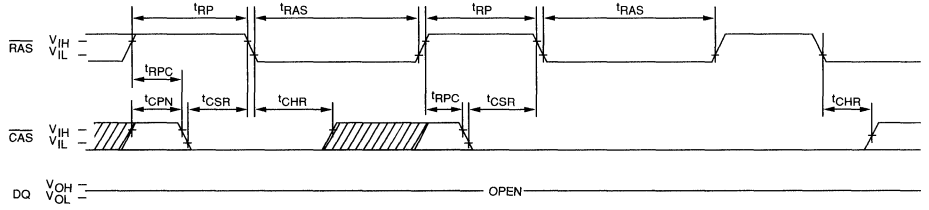
$\overline{RAS}$-ONLY REFRESH CYCLE

(ADDR = A_0 - A_9; A_{10} and $\overline{WE}$ = DON'T CARE)



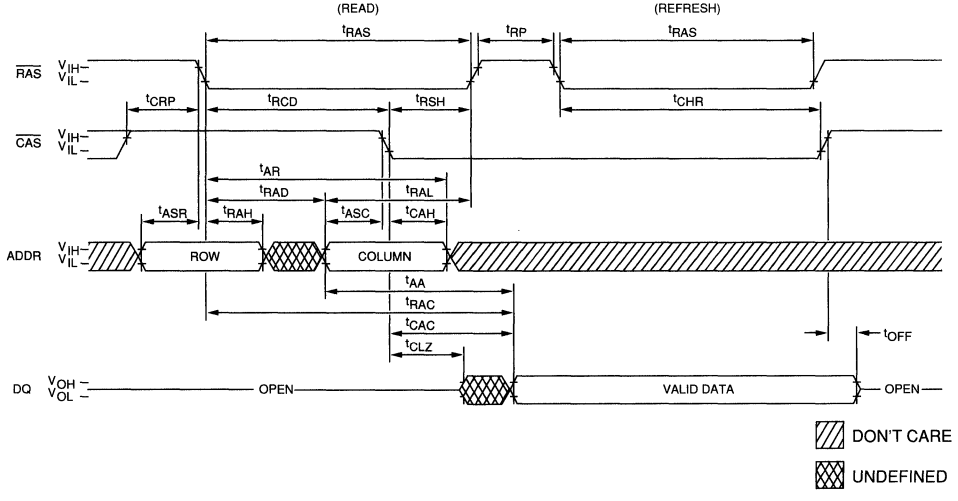
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_{10} and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DRAM MODULE

256K x 9 DRAM

FAST PAGE MODE/PAGE MODE

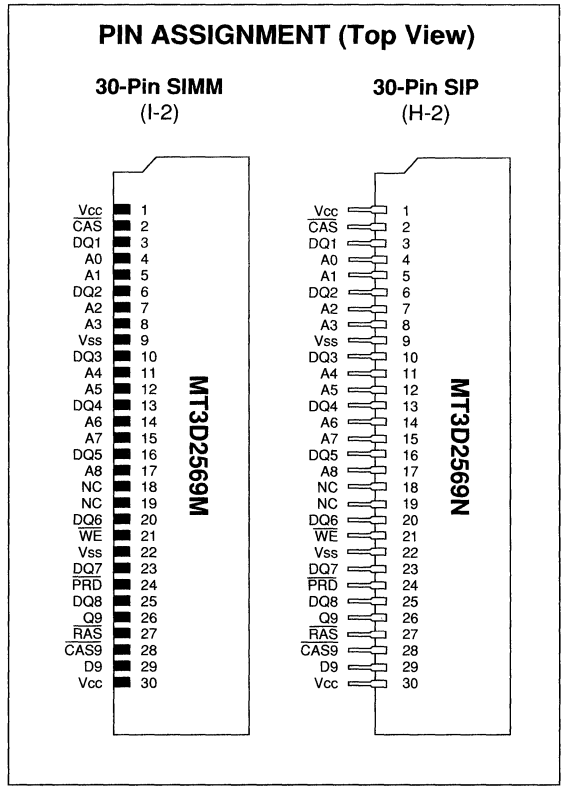
FEATURES

- Industry standard pinout in a 30-pin single-in-line memory module
- High-performance, CMOS silicon gate process
- Single 5V ±10% power supply
- Low power, 9mW standby; 625mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Optional FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh distributed across 8ms

OPTIONS

	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
120ns access	-12
• Access Mode	
FAST PAGE MODE	P
PAGE MODE	NONE
• Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N

PIN ASSIGNMENT (Top View)



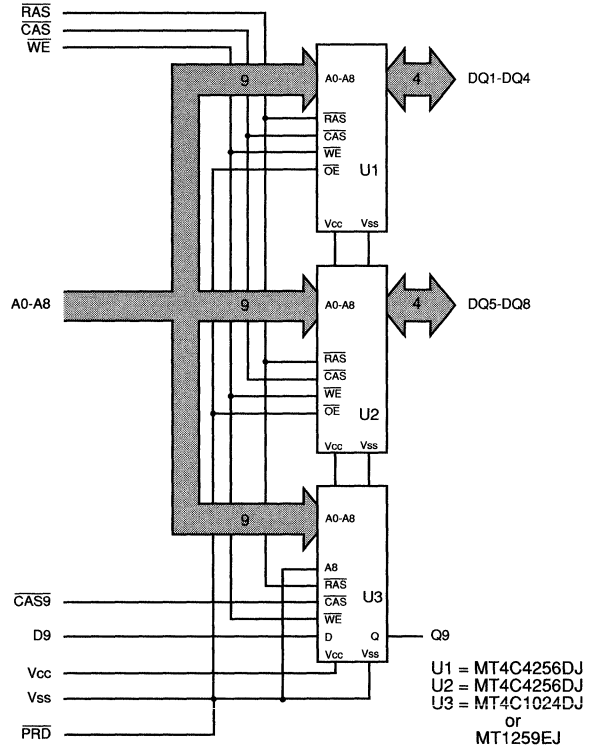
GENERAL DESCRIPTION

The MT3D2569 is a randomly accessed solid-state memory containing 262,144 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 18 address bits, which are entered nine bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first nine bits and $\overline{CAS}$ the latter nine bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY-WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Function		RAS	CAS	CAS9	WE	Addresses tR	Addresses tC	DQ1-8, D9, Q9
Standby		H	X	X	X	X	X	High Impedance
READ		L	L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Valid Data In
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L	H→L	H	n/a	COL	Valid Data Out
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation 3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-2.0	0.8	V	1, 22
INPUT LEAKAGE Any Input 0V ≤ V_{IN} ≤ V_{CC}, (All other pins not under test = 0V)	D9, $\overline{CAS9}$	I_I	-2	2	µA	
	A0-A8, $\overline{RAS}$, $\overline{WE}$	I_I	-6	6	µA	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	Q9	I_{OZ}	-10	10	µA	
	DQ1-DQ8	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	1
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	-12	UNITS	NOTES
STANDBY CURRENT: TTL Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	6	6	6	6	mA	
STANDBY CURRENT: CMOS Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	3	3	3	3	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC3}	240	210	180	150	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC4}	180	150	120	90	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH}; ^tRC = ^tRC (MIN))	I_{CC5}	240	210	180	150	mA	3, 4
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC6}	240	210	180	150	mA	3, 4

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		15	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		27	pF	18
Input Capacitance: D	C_{I3}		7	pF	18
Input/Output Capacitance: DQ	C_{IO}		12	pF	18
Output Capacitance: Q	C_O		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	135		150		180		220		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		55		70		ns	
PAGE-MODE READ or WRITE cycle time	^tPC	n/a		n/a		90		100		ns	
Access time from $\overline{RAS}$	^tRAC		70		80		100		120	ns	14
Access time from $\overline{CAS}$ (FAST PAGE MODE)	^tCAC		20		20		25		30	ns	15
Access time from $\overline{CAS}$ (PAGE MODE)	^tCAC		n/a		n/a		50		60	ns	
Output Enable	^tOE		20		20		25		30	ns	
Access time from column address	^tAA		35		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		50		65	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	30	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		20		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		15		ns	
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	n/a		n/a		30		30		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		10		ns	
Row address setup time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	10		10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	20	50	20	60	ns	18
Column address setup time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		60		ns	
Read command setup time	^tRCS	0		0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

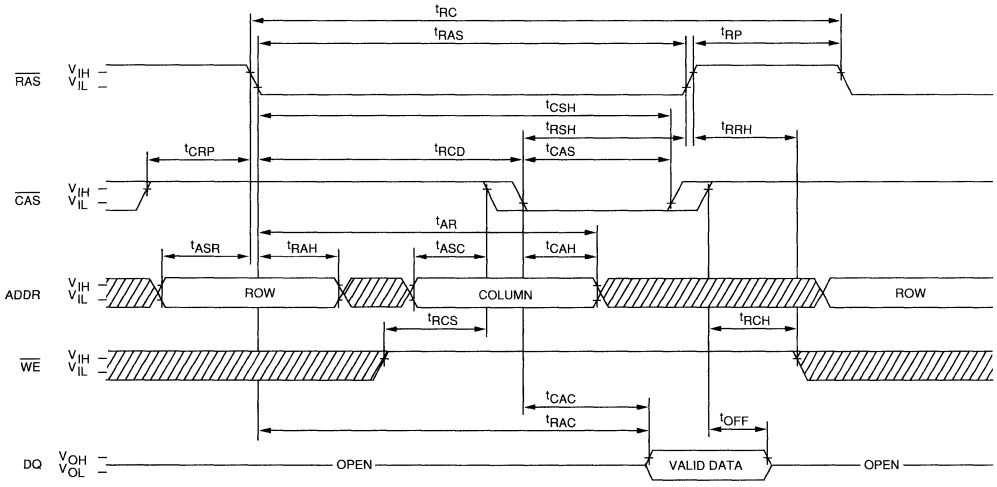
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	0	35	ns	20
Output Disable	^tOD		20		20		20		20	ns	
$\overline{WE}$ command setup time	^tWCS	0		0		0		0		ns	
Write command hold time	^tWCH	15		15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		85		ns	
Write command pulse width	^tWP	15		15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		30		ns	
Data-in setup time	^tDS	0		0		0		0		ns	
Data-in hold time	^tDH	15		15		20		25		ns	
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	n/a		n/a		n/a		n/a		n/a	21
Column address to $\overline{WE}$ delay time	^tAWD	n/a		n/a		n/a		n/a		n/a	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	n/a		n/a		n/a		n/a		n/a	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		8		8		8		8	ms	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	15		15		15		15		ns	19
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	n/a		n/a		n/a		n/a		n/a	21

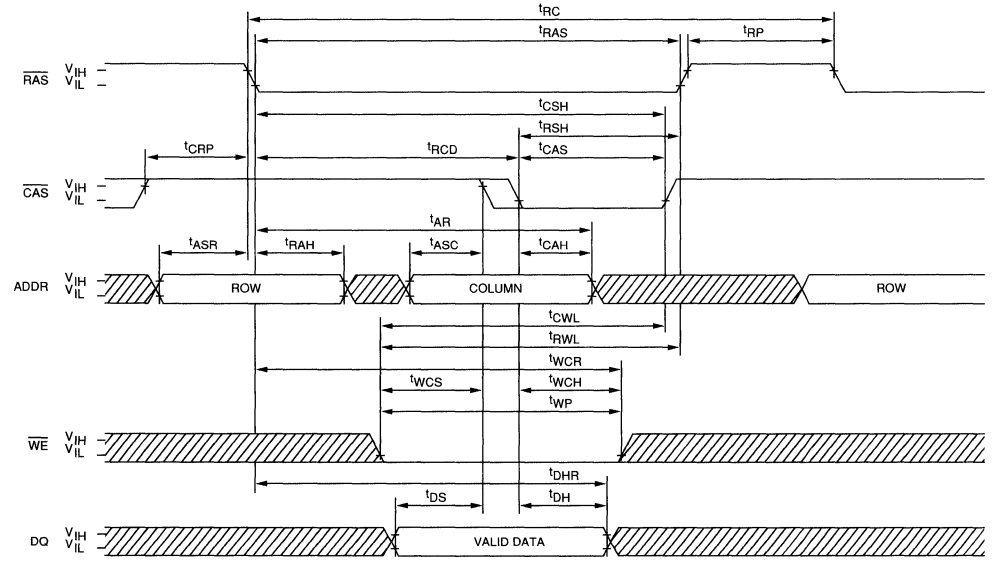
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge {}^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. ^{t}RCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1 andU2.
22. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

READ CYCLE



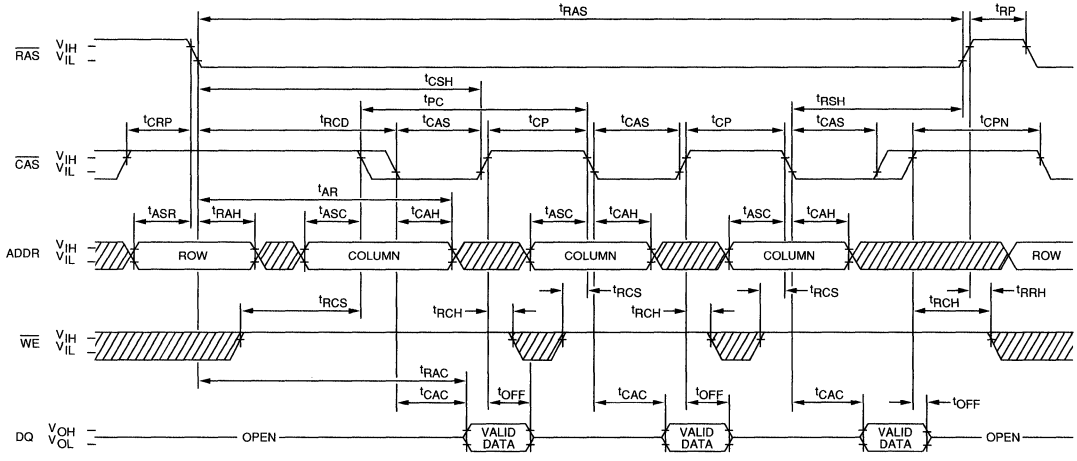
EARLY-WRITE CYCLE



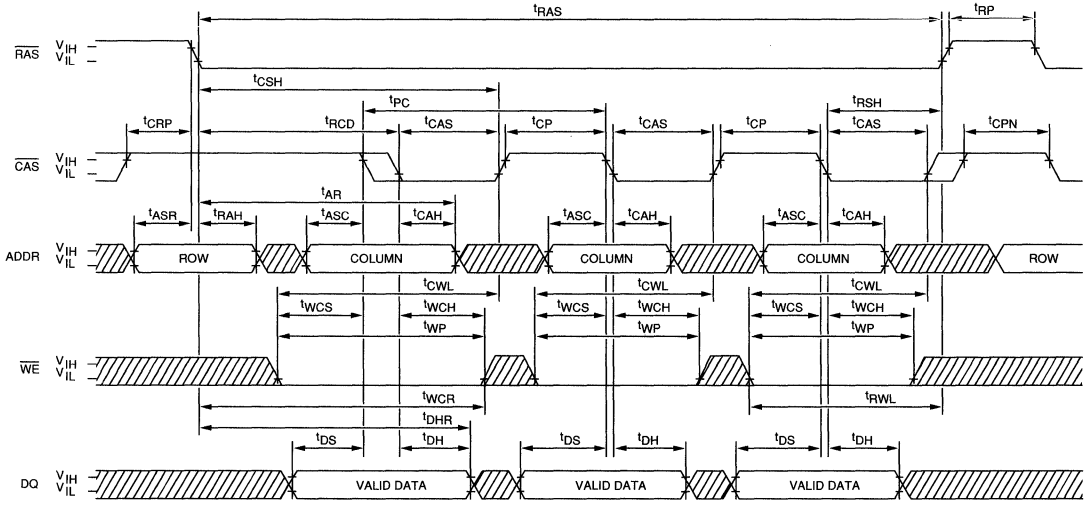
DON'T CARE

UNDEFINED

PAGE/FAST-PAGE-MODE READ CYCLE



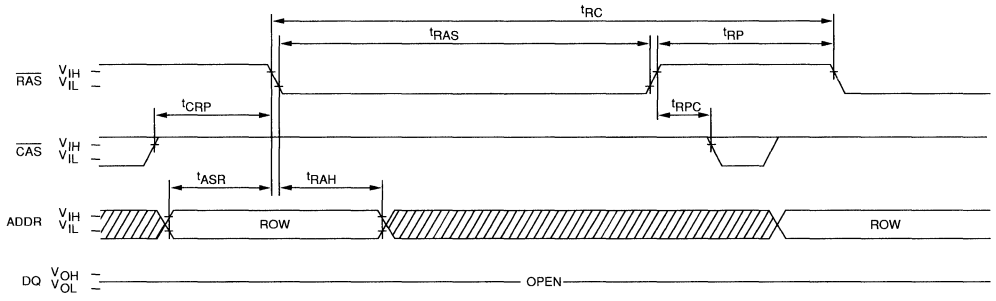
PAGE/FAST-PAGE-MODE EARLY-WRITE CYCLE



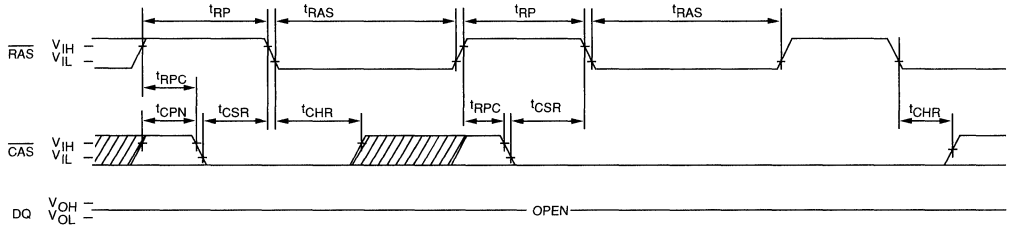
DON'T CARE

UNDEFINED

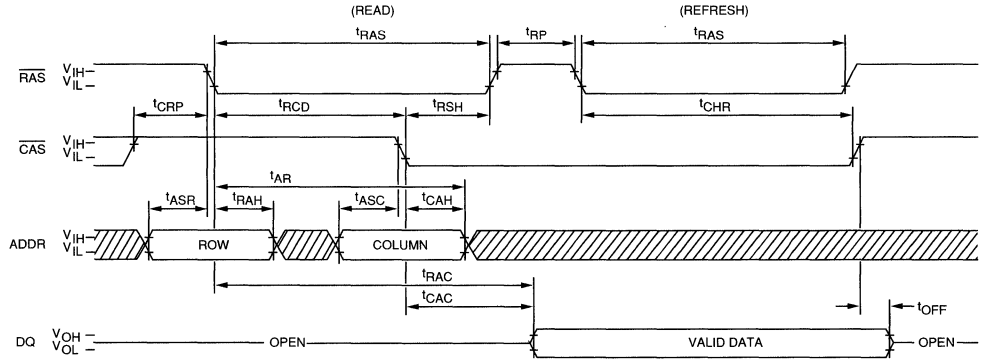
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A_0 - A_8 ; $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A_0 - A_8 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH) [20]



DON'T CARE

UNDEFINED

DRAM MODULE

1 MEG x 9 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pinout in a 30-pin single-in-line package
- High-performance, CMOS silicon gate process
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 27mW standby; 1,575mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, and HIDDEN
- 512-cycle refresh distributed across 8ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

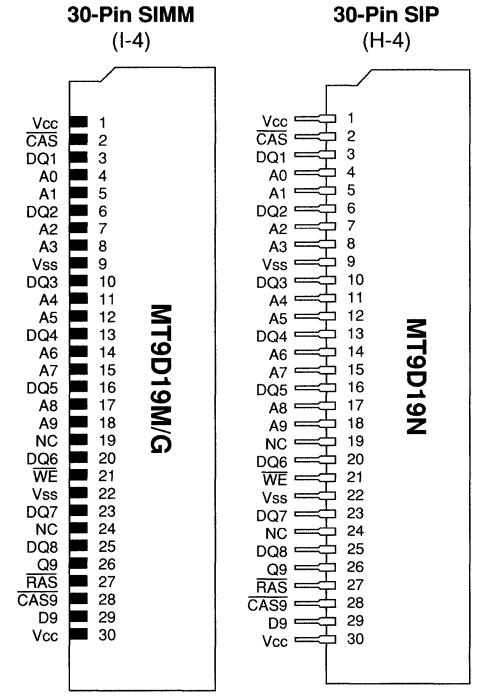
- Timing

70ns access	- 7
80ns access	- 8
100ns access	-10

- Packages

Leadless 30-pin SIMM	M
Leadless 30-pin SIMM (Gold)	G
Leaded 30-pin SIP	N

PIN ASSIGNMENT (Top View)



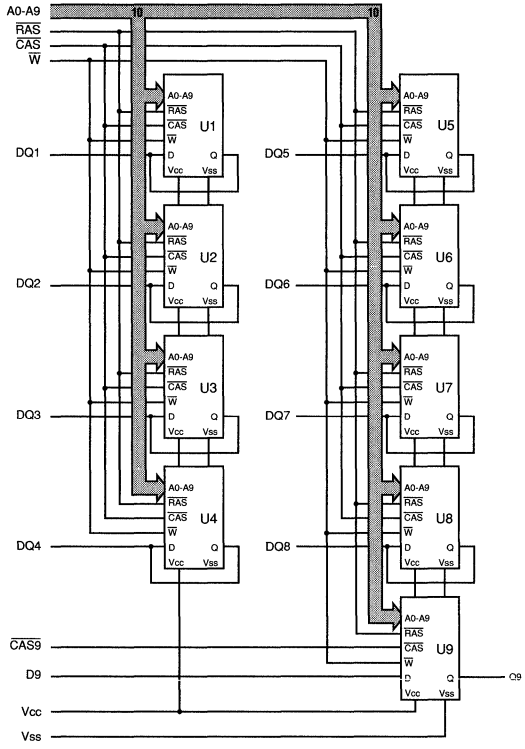
GENERAL DESCRIPTION

The MT9D19 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY-WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pins remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A9) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U9 = MT4C1024DJ

TRUTH TABLE

Function		RAS	CAS	CAS9	WE	Addresses tR	Addresses tA	DQ1-8, D9, Q9
Standby		H	X	X	X	X	X	High Impedance
READ		L	L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H	ROW	COL	Valid Data Out
READ	2nd Cycle	L	H→L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Valid Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High Impedance
HIDDEN	READ	L→H→L	L	L	H	ROW	COL	Valid Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-2.0	0.8	V	1, 25
INPUT LEAKAGE: Any Input $0V \le V_{IN} \le V_{CC}$ (All other pins not under test = 0V)	D9, $\overline{CAS9}$	I_I	-2	2	µA	
	A0-A9, $\overline{RAS}$, $\overline{WE}$	I_I	-18	18	µA	
OUTPUT LEAKAGE: (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	Q9	I_{OZ}	-10	10	µA	
	DQ1-8	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: TTL Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	18	18	18	mA	
STANDBY CURRENT: CMOS Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	9	9	9	mA	
OPERATING CURRENT: ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC3}	720	630	540	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC4}	540	450	360	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH}; ^tRC = ^tRC (MIN))	I_{CC5}	720	630	540	mA	3, 4
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC6}	720	630	540	mA	3, 4

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		45	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		63	pF	2
Input Capacitance: D	C_{I3}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤70°C; V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	n/a		n/a		n/a		n/a	25
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		40		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	n/a		n/a		n/a		n/a	25
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Access time from column address	t_{AA}		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		50	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	15	40	20	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

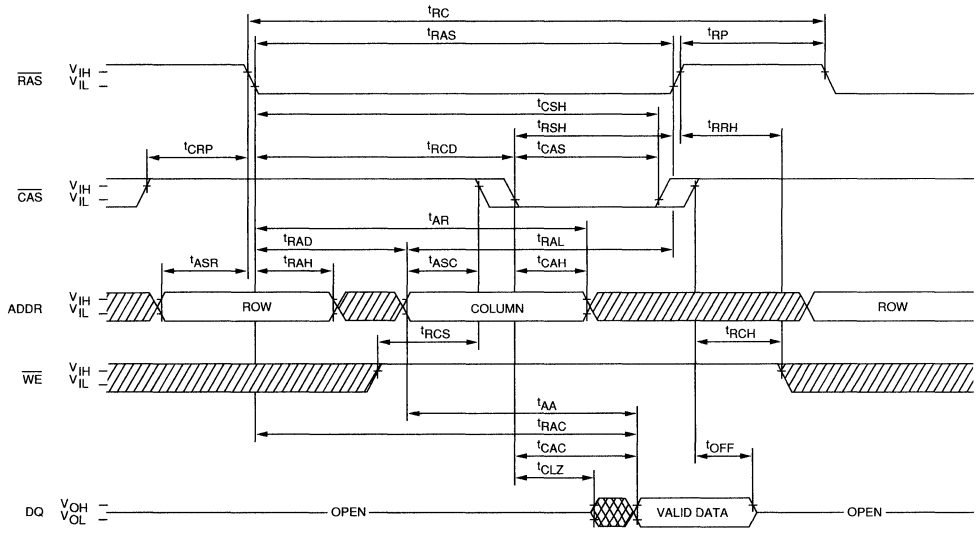
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 75°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Data-in hold time	^tDH	15		15		20		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	n/a		n/a		n/a		n/a	24
Column address to $\overline{WE}$ delay time	^tAWD	n/a		n/a		n/a		n/a	24
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	n/a		n/a		n/a		n/a	24
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	15		15		15		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	n/a		n/a		n/a		n/a	24

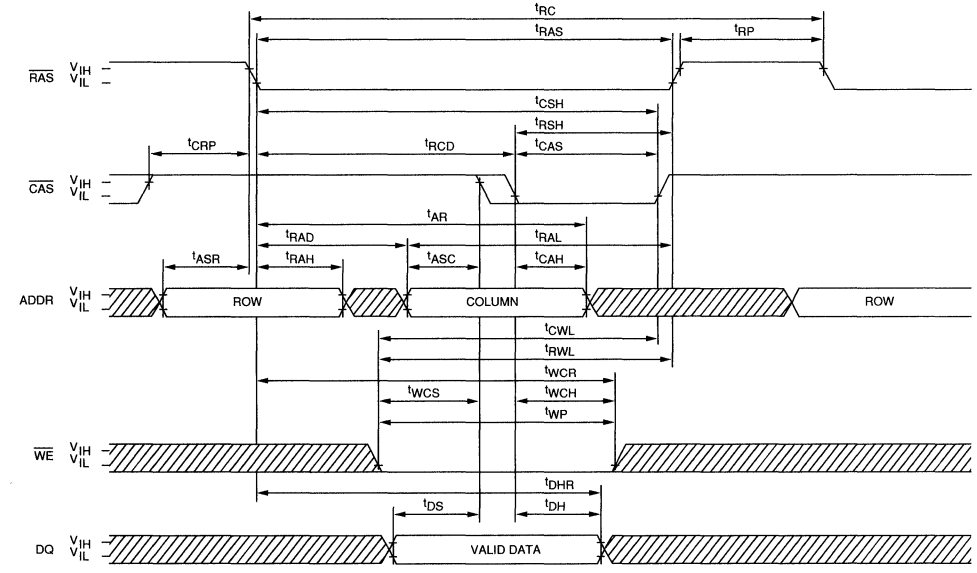
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ${}^tT$ = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ${}^tRCD < {}^tRCD$ (MAX). If ${}^tRCD$ is greater than the maximum recommended value shown in this table, ${}^tRAC$ will increase by the amount that ${}^tRCD$ exceeds the value shown.
15. Assumes that ${}^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ${}^tCPN$.
17. Operation within the ${}^tRCD$ (MAX) limit ensures that ${}^tRAC$ (MAX) can be met. ${}^tRCD$ (MAX) is specified as a reference point only; if ${}^tRCD$ is greater than the specified ${}^tRCD$ (MAX) limit, then access time is controlled exclusively by ${}^tCAC$.
18. Operation within the ${}^tRAD$ (MAX) limit ensures that ${}^tRCD$ (MAX) can be met. ${}^tRAD$ (MAX) is specified as a reference point only; if ${}^tRAD$ is greater than the specified ${}^tRAD$ (MAX) limit, then access time is controlled exclusively by ${}^tAA$.
19. Either ${}^tRCH$ or ${}^tRRH$ must be satisfied for a READ cycle.
20. ${}^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. All other inputs equal Vcc -0.2V.
24. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
25. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

READ CYCLE



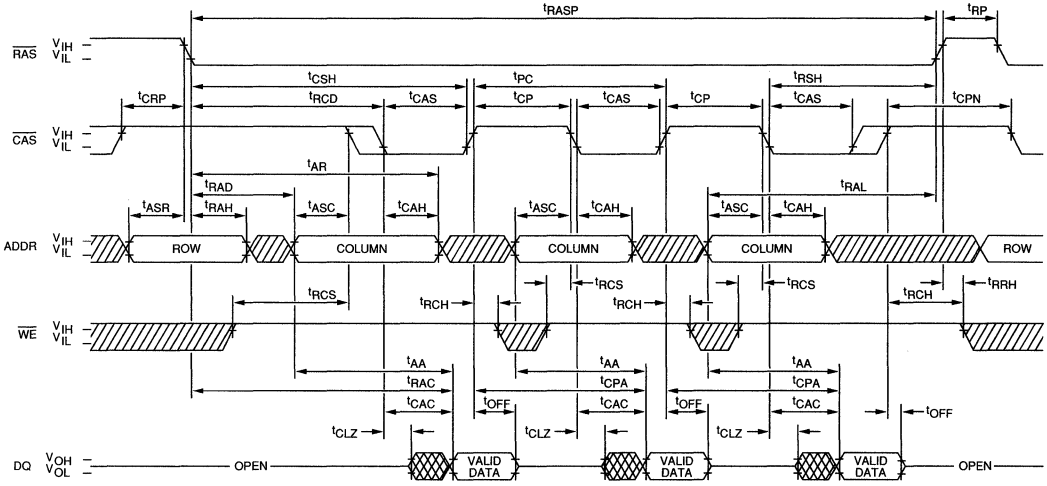
EARLY-WRITE CYCLE



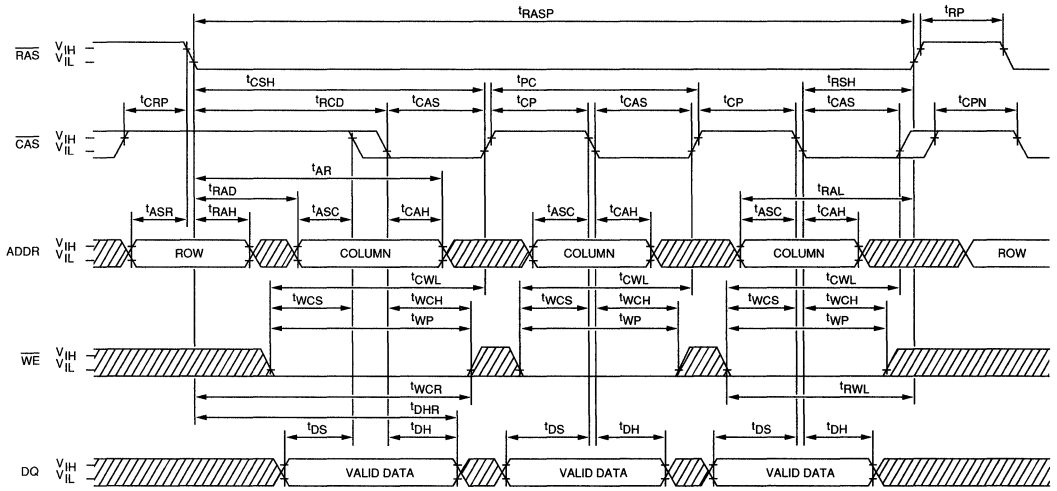
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

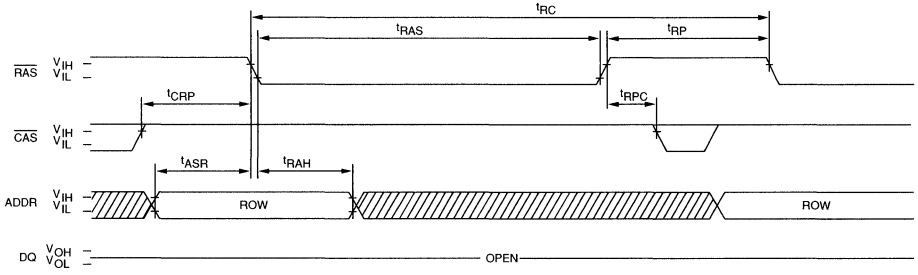


DON'T CARE

UNDEFINED

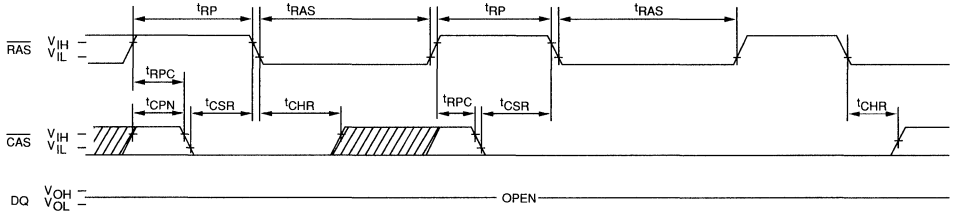
$\overline{RAS}$-ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE)



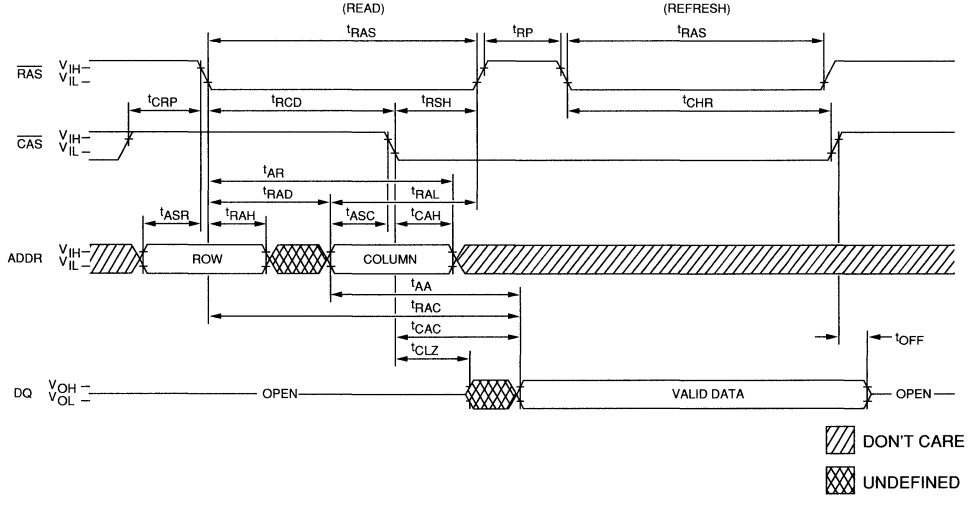
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH) [22]



DRAM MODULE

1 MEG x 9 DRAM

FAST PAGE MODE

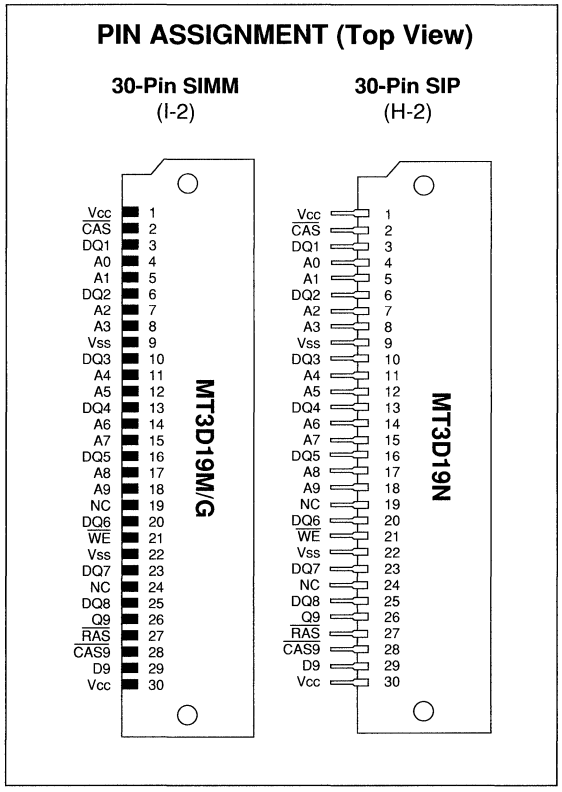
FEATURES

- Industry standard pinout in a 30-pin single-in-line memory module
- High-performance, CMOS silicon gate process
- Single 5V ±10% power supply
- Low power, 9mW standby; 625mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Optional FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 1,024-cycle refresh distributed across 16ms

OPTIONS

	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Leadless 30-pin SIMM	M
Leadless 30-pin SIMM (Gold)	G
Leaded 30-pin SIP	N

PIN ASSIGNMENT (Top View)



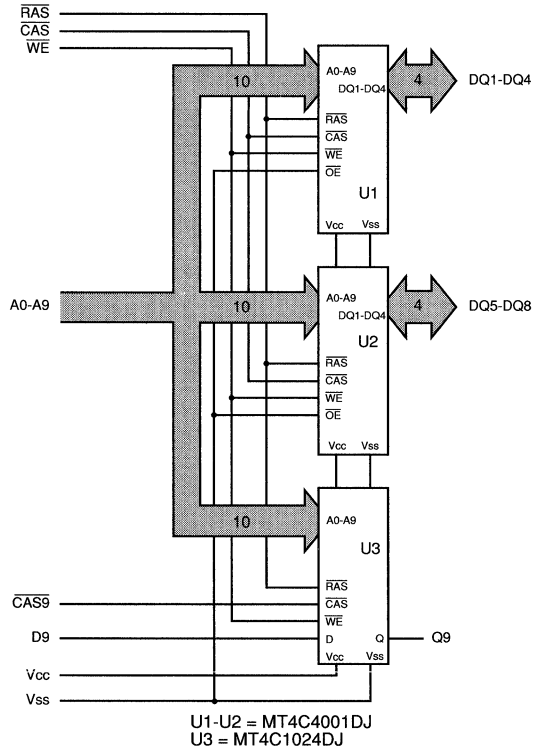
GENERAL DESCRIPTION

The MT3D19 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U2 = MT4C4001DJ
U3 = MT4C1024DJ

TRUTH TABLE

Function		RAS	CAS	CAS9	WE	Addresses tR	Addresses tC	DQ1-8, D9, Q9
Standby		H	X	X	X	X	X	High Impedance
READ		L	L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation 3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Any Input $0V \le V_{IN} \le V_{CC}$ (All other pins not under test = 0V)	D9, $\overline{CAS9}$	I_I	-2	2	µA	
	A0-A9, $\overline{RAS}$, $\overline{WE}$	I_I	-6	6	µA	
OUTPUT LEAKAGE (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	Q9	I_{OZ}	-10	10	µA	
	DQ1-DQ8	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	1
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: TTL Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	6	6	6	mA	
STANDBY CURRENT: CMOS Input Levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	3	3	3	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC3}	280	250	220	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC4}	200	170	140	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH}; ^tRC = ^tRC (MIN))	I_{CC5}	280	250	220	mA	3, 4
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC6}	280	250	220	mA	3, 4

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		15	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		21	pF	18
Input Capacitance: D	C_{I3}		7	pF	18
Input/Output Capacitance: DQ	$C_{I/O}$		7	pF	18
Output Capacitance: Q	C_O		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		45		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a	21
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	15
Access time from column address	^tAA		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		50	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	20	50	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		50		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

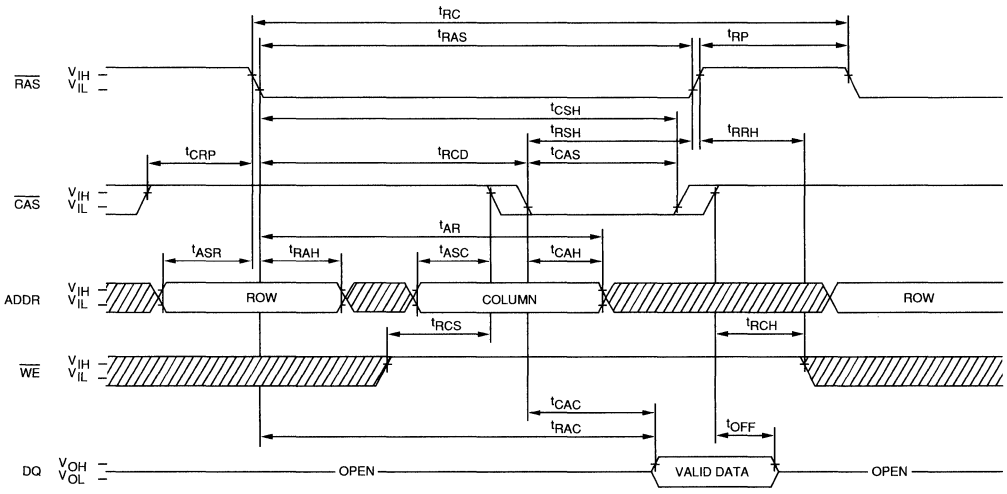
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		70		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	
Data-in hold time	^tDH	15		15		20		ns	
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		70		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	n/a		n/a		n/a		n/a	21
Column address to $\overline{WE}$ delay time	^tAWD	n/a		n/a		n/a		n/a	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	n/a		n/a		n/a		n/a	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	15		15		15		ns	19
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	n/a		n/a		n/a		n/a	21

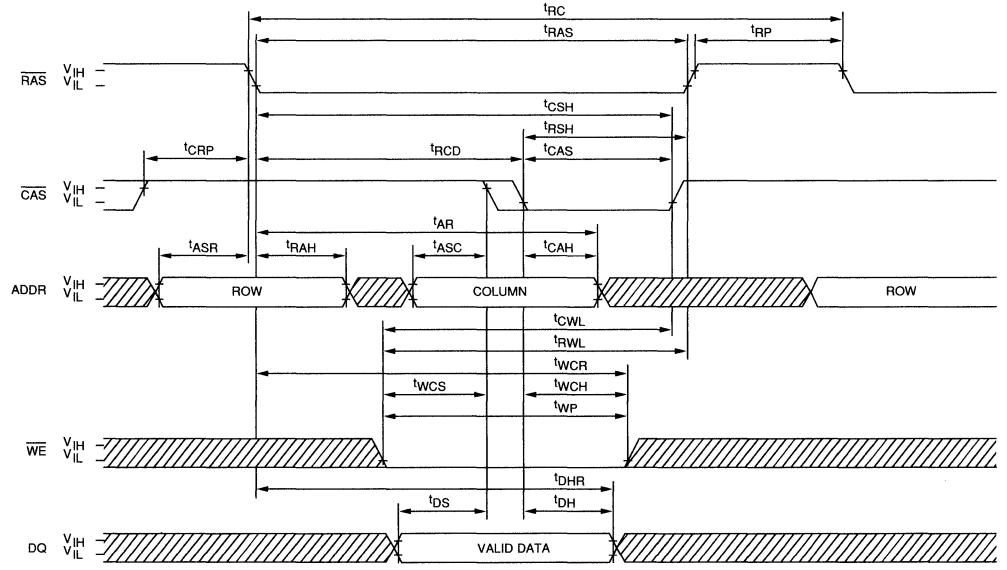
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge {}^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. ^{t}RCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1 and U2.

READ CYCLE



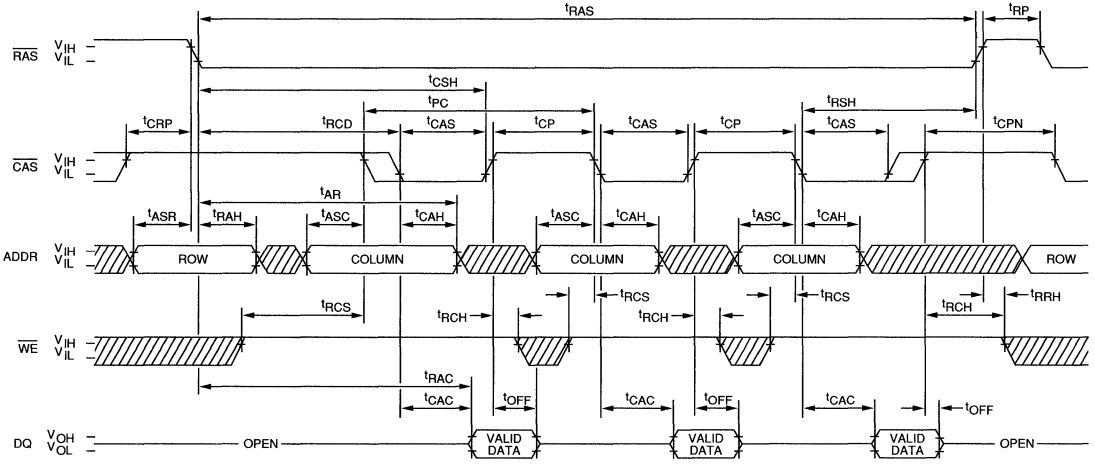
EARLY-WRITE CYCLE



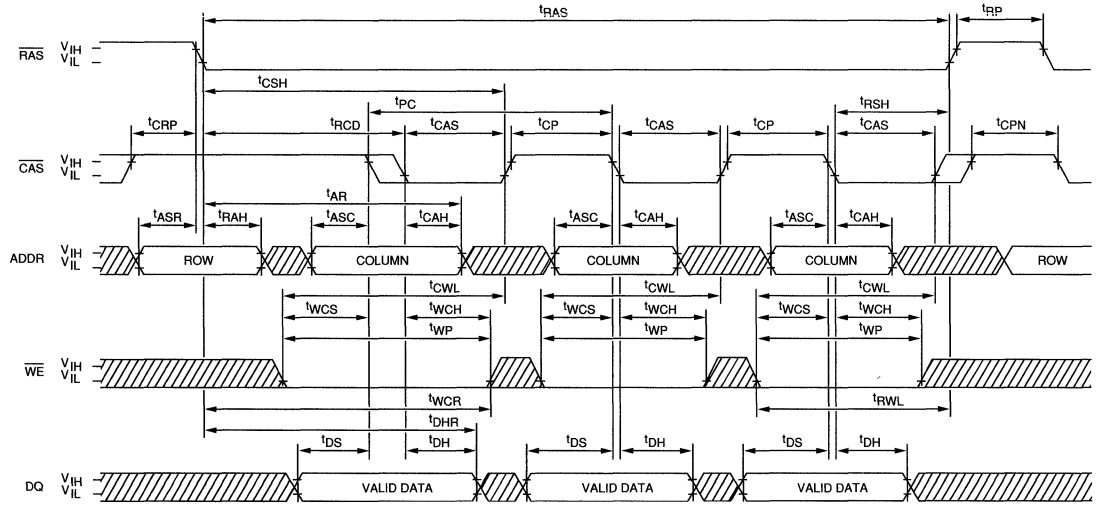
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

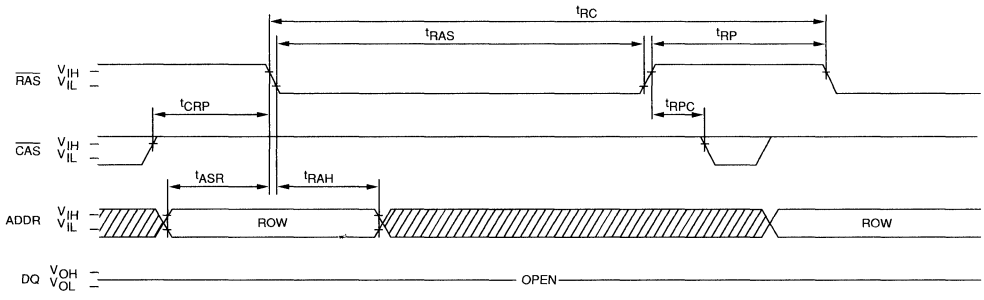


DON'T CARE

UNDEFINED

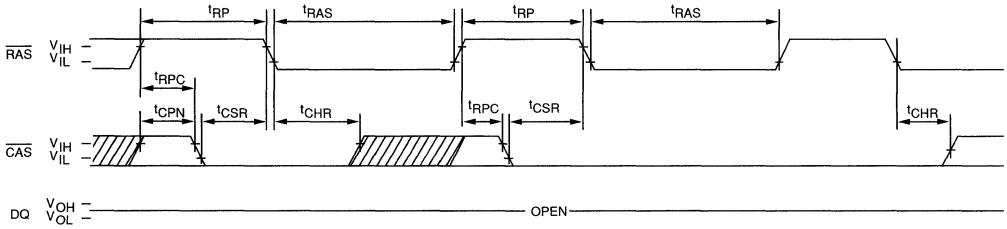
$\overline{RAS}$-ONLY REFRESH CYCLE

(ADDR = A_0 - A_9 ; $\overline{WE}$ = DON'T CARE)



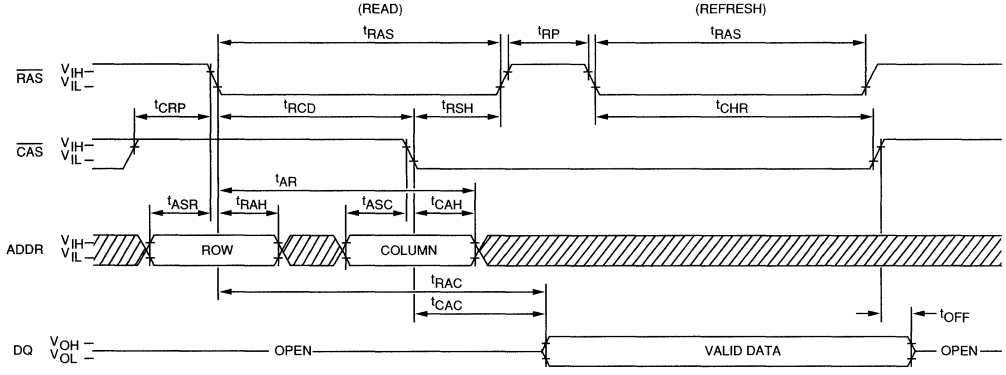
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH) [20]



DON'T CARE

UNDEFINED

DRAM MODULE

4 MEG x 9 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pinout in a 30-pin single-in-line package
- High-performance, CMOS silicon gate process
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 27mW standby; 2,025mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

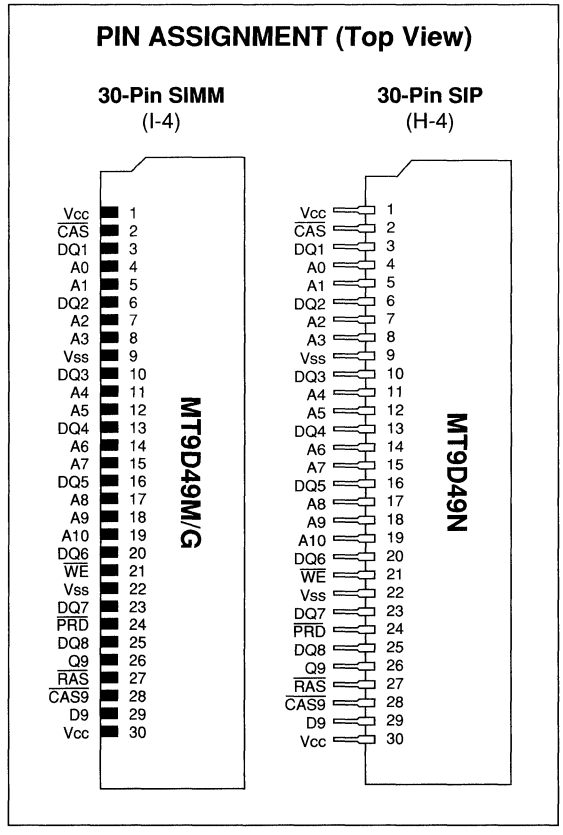
- Timing

60ns access	-6
70ns access	-7
80ns access	-8

- Packages

Leadless 30-pin SIMM	M
Leadless 30-pin SIMM (Gold)	G
Leaded 30-pin SIP	N

PIN ASSIGNMENT (Top View)



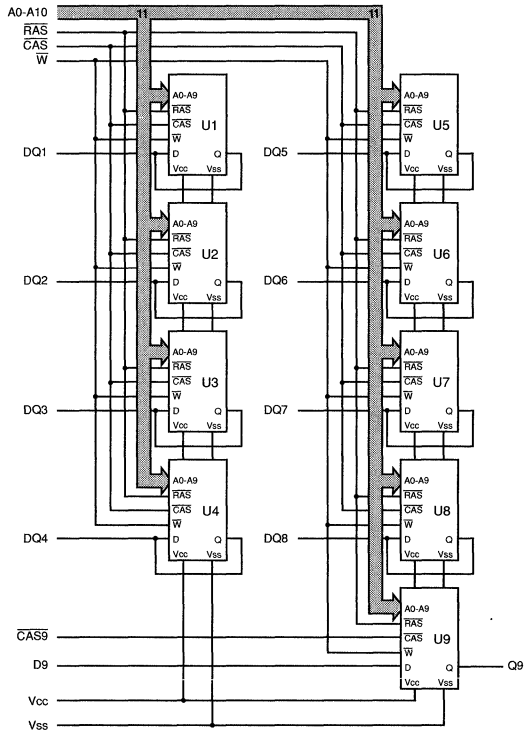
GENERAL DESCRIPTION

The MT9D49 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x9 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, and the ouput remains open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A10) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U9 = MT4C1004DJ

TRUTH TABLE

Function		RAS	CAS	CAS9	WE	Addresses tR	Addresses tA	DQ1-8, D9, Q9
Standby		H	X	X	X	X	X	High Impedance
READ		L	L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH	Standard	H→L	L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input: 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	A9, $\overline{CAS9}$	I_I	-2	2	µA	
	A0-A10, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$	I_I	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	Q9	I_{OZ}	-10	10	µA	
	DQ1-DQ8	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	18	18	18	mA	
STANDBY CURRENT (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	9	9	9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	990	900	810	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	720	630	540	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	990	900	810	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	990	900	810	mA	3

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		45	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{WE}$	C_{I2}		63	pF	2
Input Capacitance: D9	C_{I3}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2
Output Capacitance: Q9	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	24
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		n/a	24
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		40		45	ns	25
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	45		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	10		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

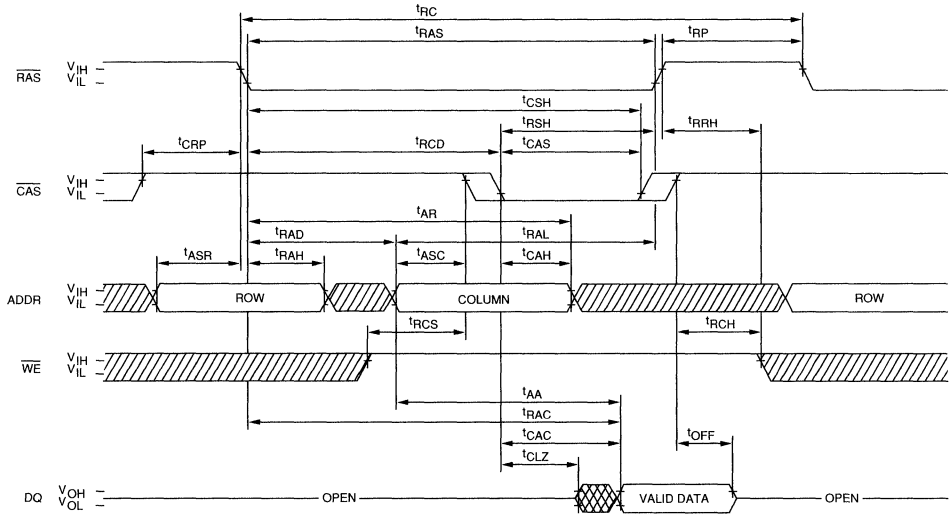
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^{t}WCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		60		ns	
Write command pulse width	^{t}WP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		20		ns	
Data-in setup time	^{t}DS	0		0		0		ns	21
Data-in hold time	^{t}DH	10		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	n/a		n/a		n/a		n/a	24
Column address to $\overline{WE}$ delay time	^{t}AWD	n/a		n/a		n/a		n/a	24
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	n/a		n/a		n/a		n/a	24
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^{t}REF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^{t}CSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^{t}CHR	15		15		15		ns	5

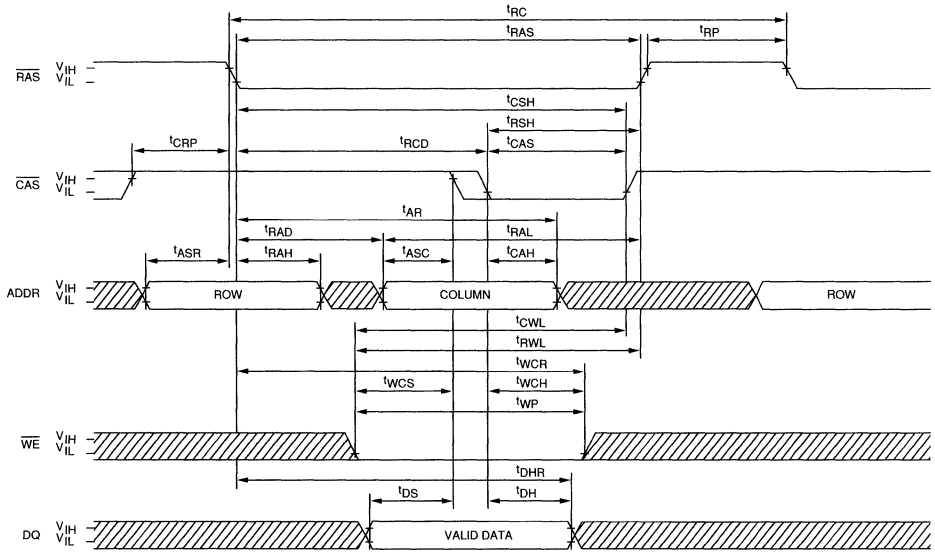
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. All other inputs equal V_{CC} -0.2V.
24. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.

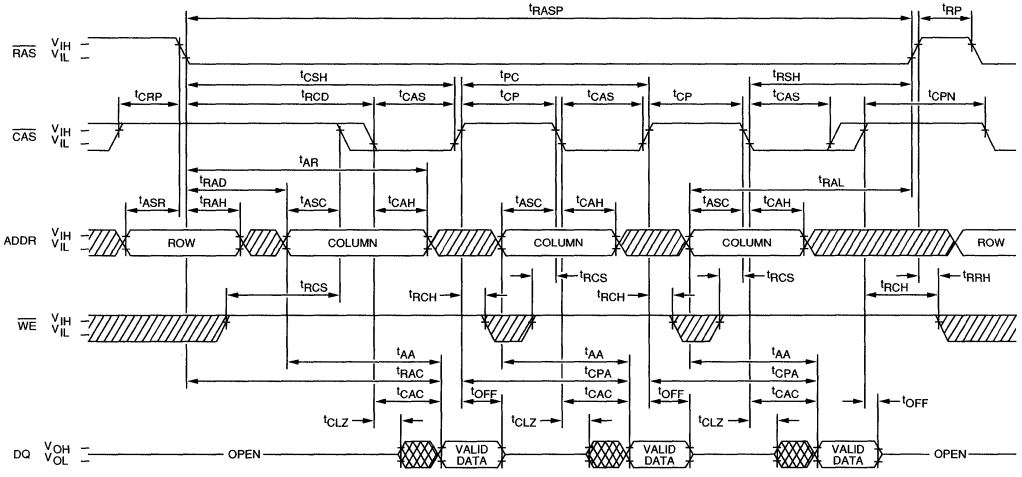
READ CYCLE



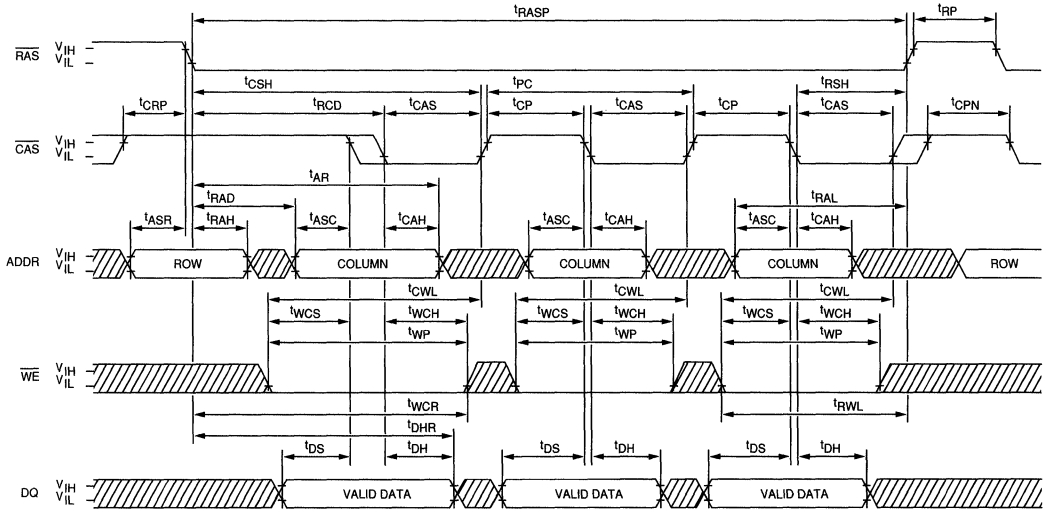
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

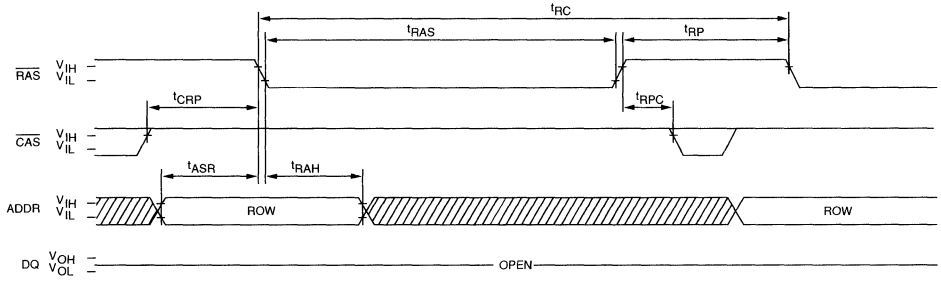


DON'T CARE

UNDEFINED

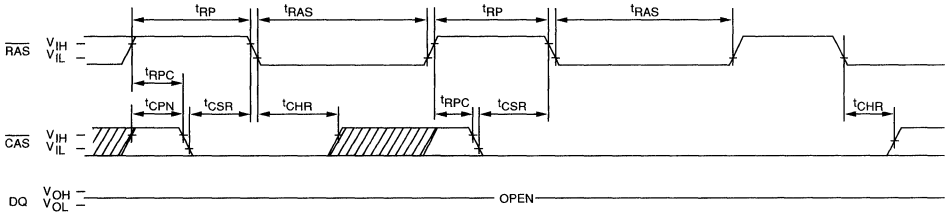
$\overline{RAS}$-ONLY REFRESH CYCLE

(ADDR = A_0 - A_9; A_{10} and $\overline{WE}$ = DON'T CARE)



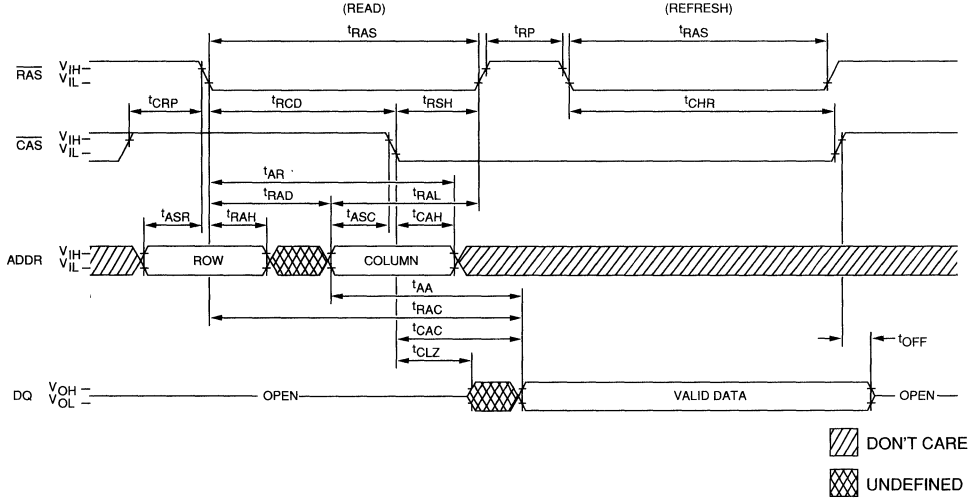
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_{10} and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH) [23]



DRAM MODULE

256K x 32 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon gate process.
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 24mW standby; 1,400mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh distributed across 8ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

- Timing

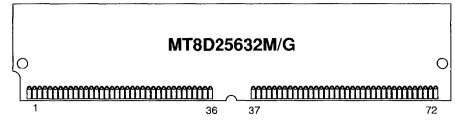
70ns access	- 7
80ns access	- 8
85ns access	-85
100ns access	-10

- Packages

Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (Gold)	G
Leaded 72-pin ZIP	Z

PIN ASSIGNMENT (Top View)

72-Pin SIMM (I-5)



72-Pin ZIP (J-4)

PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PRD1
14	A2	32	NC	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

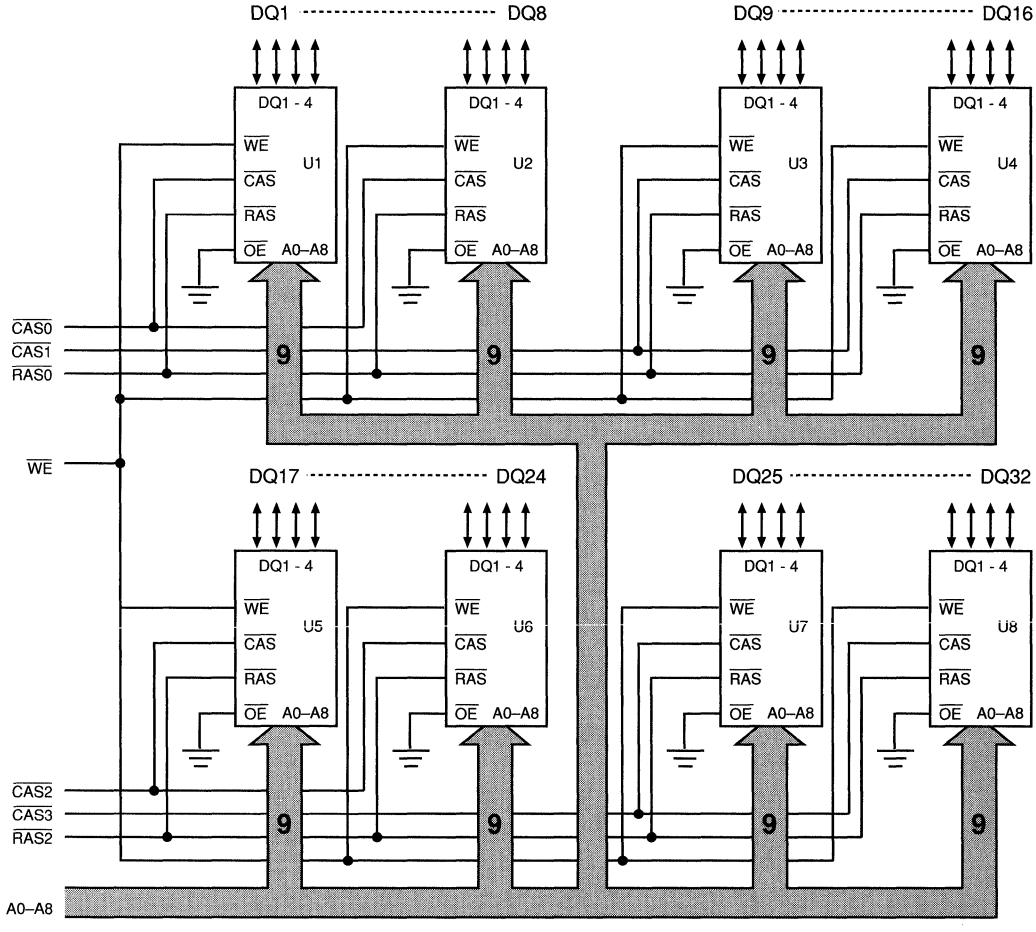
GENERAL DESCRIPTION

The MT8D25632 is a randomly accessed solid-state memory containing 262,144 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4256DJ

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	DQ1-32
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L→H	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L→H	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L→H	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L→H	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

PRESENCE DETECT

SYMBOL	-7	-8	-85	-10
PRD1	NC	VSS	VSS	VSS
PRD2	NC	NC	NC	NC
PRD3	VSS	VSS	NC	VSS
PRD4	VSS	NC	VSS	VSS

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-2.0	0.8	V	1, 22
INPUT LEAKAGE CURRENT Any input: 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V) For each package input	A0-A8, $\overline{WE}$	I_I	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) For each package input	DQ1-DQ32	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8, -85	-10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	640	560	480	mA	2
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	480	400	320	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles (MIN))	I_{CC3}	16	16	16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles (MIN)). (All other inputs at V_{CC} -0.2V or V_{SS} +0.2V)	I_{CC4}	8	8	8	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}	640	560	480	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	640	560	480	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		40	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		56	pF	17
Input Capacitance: $\overline{RAS0}$	C_{I3}		28	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$	C_{I4}		14	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}		7	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

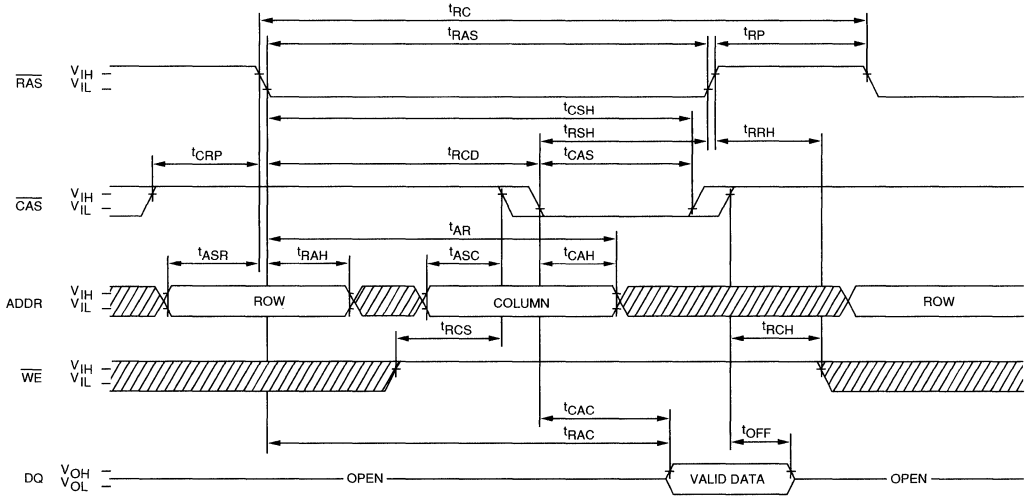
(Notes: 3, 4, 5, 10, 11, 16, 17) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8, -85		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	135		150		180		ns	6, 7
FAST-PAGE-MODE cycle time	^tPC	40		45		55		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	55		60		70		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		ns	14
Read command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		20		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	55		60		75		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	16
Refresh period (256 cycles)	^tREF		8		8		8	ms	20
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ REFRESH)	^tCHR	15		15		15		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	19

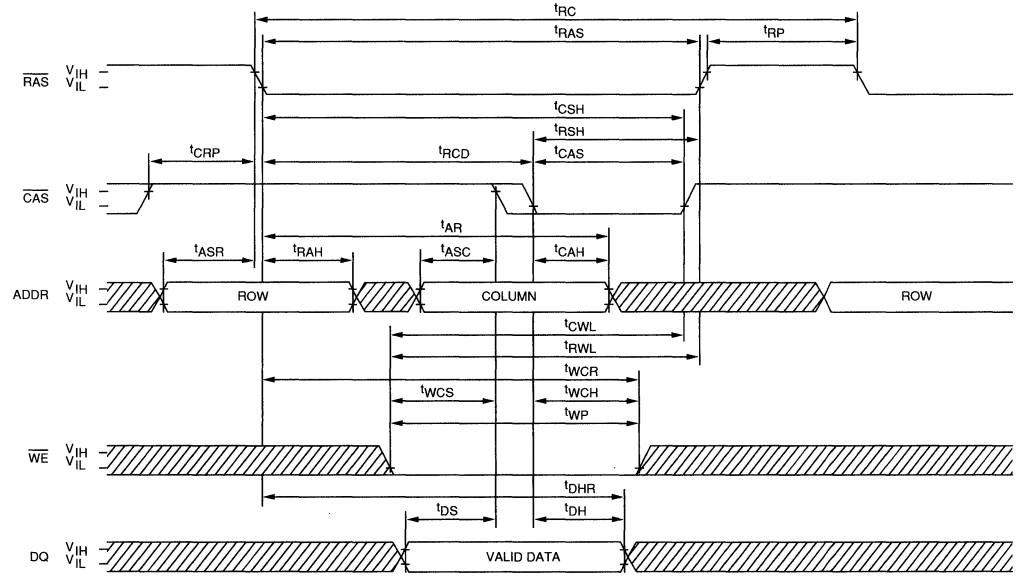
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. ^{t}RCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U8.
22. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

READ CYCLE



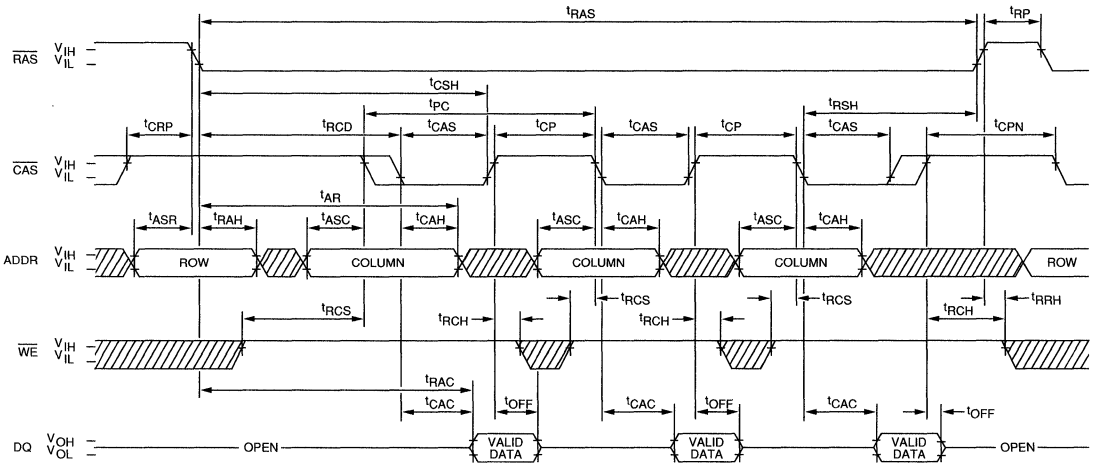
EARLY-WRITE CYCLE



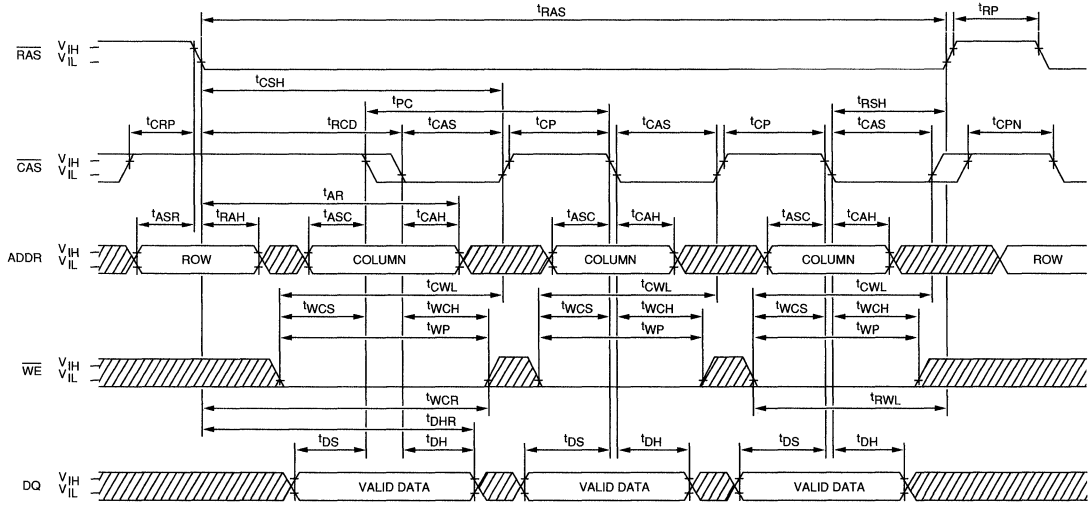
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

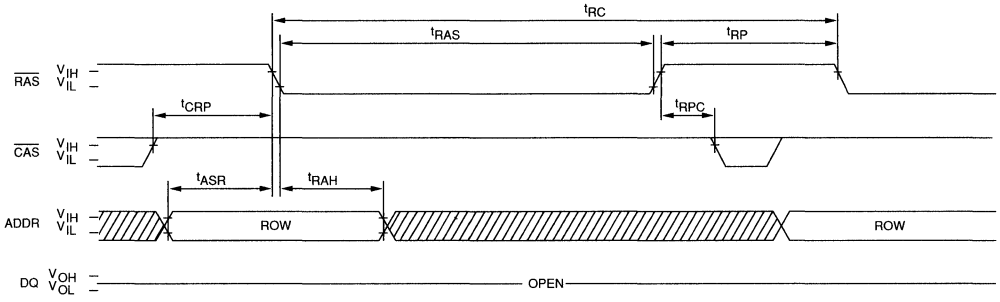


DON'T CARE

UNDEFINED

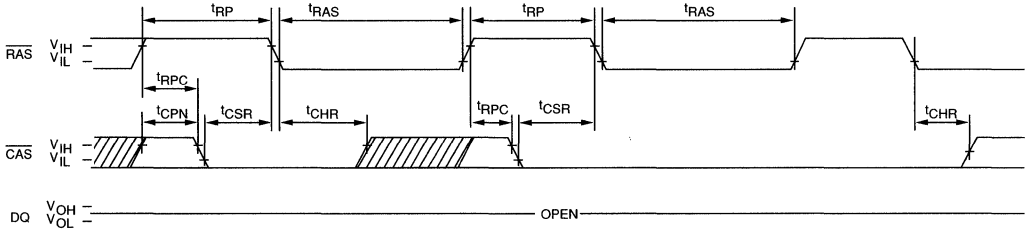
$\overline{RAS}$-ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE)



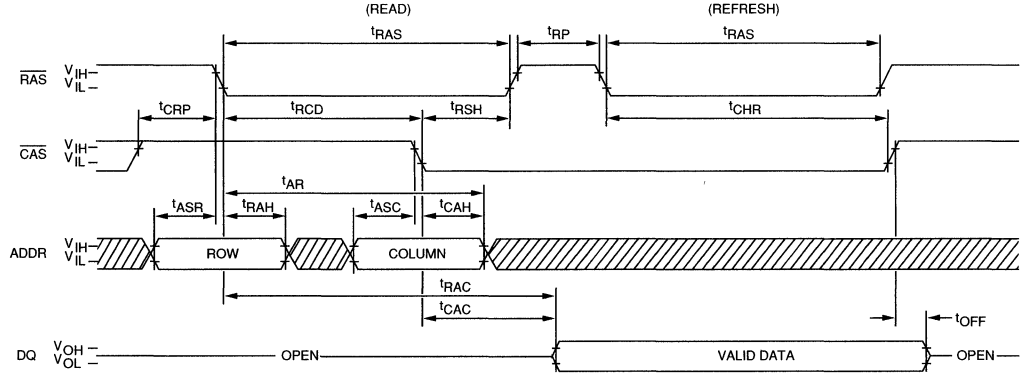
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH) [20]



DON'T CARE

UNDEFINED

DRAM MODULE

512K x 32 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon gate process.
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 48mW standby; 2,800mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh distributed across 8ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

- Timing

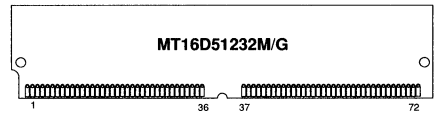
70ns access	- 7
80ns access	- 8
85ns access	-85
100ns access	-10

- Packages

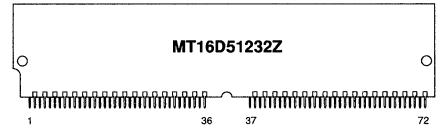
Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (Gold)	G
Leaded 72-pin ZIP	Z

PIN ASSIGNMENT (Top View)

72-Pin SIMM (I-6)



72-Pin ZIP (J-5)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ25	68	PRD2
15	A3	33	$\overline{RAS3}$	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

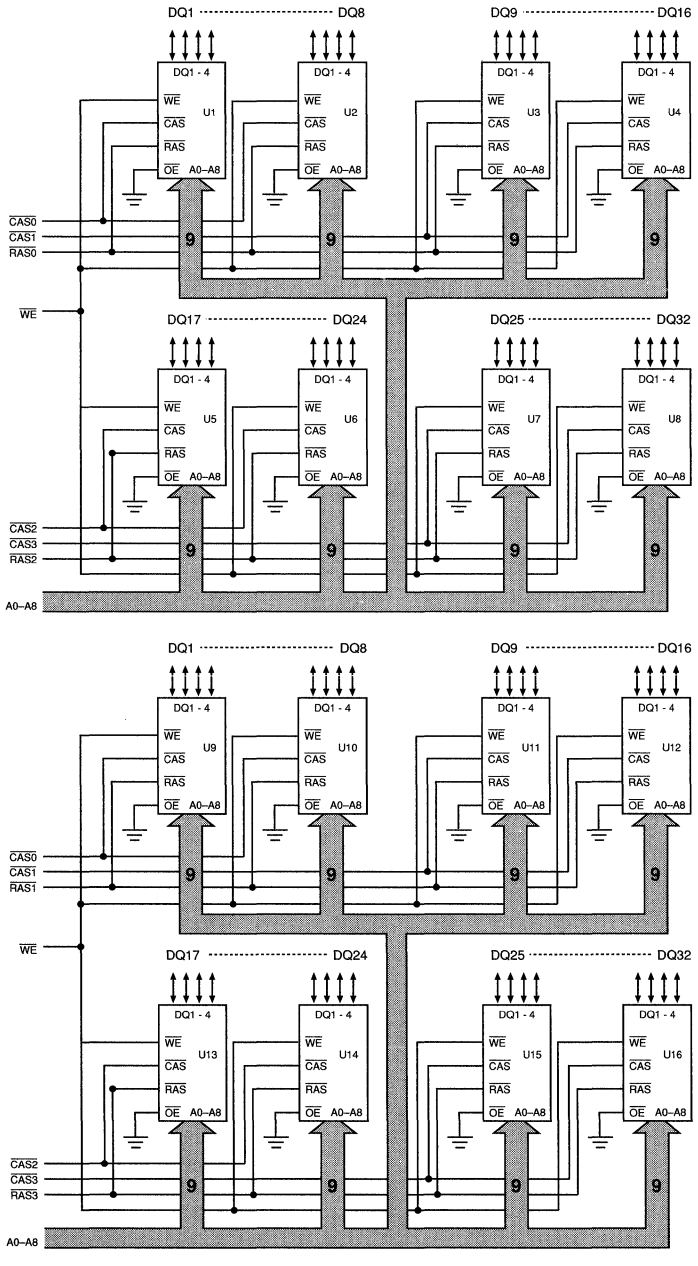
GENERAL DESCRIPTION

The MT16D51232 is a randomly accessed solid-state memory containing 524,288 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4256DJ

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	DQ1-32
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L→H	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L→H	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L→H	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L→H	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

PRESENCE DETECT

SYMBOL	-7	-8	-85	-10
PRD1	VSS	NC	NC	NC
PRD2	VSS	VSS	VSS	VSS
PRD3	NC	VSS	NC	VSS
PRD4	NC	NC	VSS	VSS

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-2.0	0.8	V	1, 22
INPUT LEAKAGE CURRENT Any Input: 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V) For each package input	A0-A8, $\overline{WE}$	II	-32	32	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ Vcc) For each package input	DQ1-32	IOZ	-24	24	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	1
Output Low Voltage (IOUT = 5mA)		VOL		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8, -85	-10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	ICC1	656	576	496	mA	2
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = VIL, $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	ICC2	496	416	336	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = VIH after 8 $\overline{RAS}$ cycles (MIN))	ICC3	32	32	32	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V after 8 $\overline{RAS}$ cycles (MIN)). (All other inputs at Vcc -0.2V or Vss +0.2V)	ICC4	16	16	16	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = VIH)	ICC5	656	576	496	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	ICC6	656	576	496	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	CI1		80	pF	17
Input Capacitance: $\overline{WE}$	CI2		112	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$, $\overline{RAS0}$-$\overline{RAS3}$	CI4		28	pF	17
Input/Output Capacitance: DQ1-DQ32	CIO		14	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

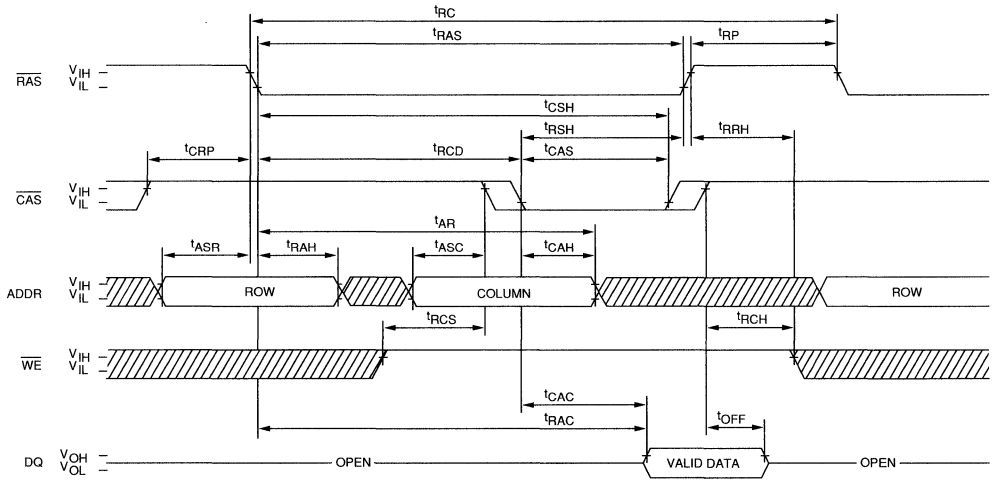
(Notes: 3, 4, 5, 10, 11, 16, 17) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8, 85		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	135		150		180		ns	6, 7
FAST-PAGE-MODE cycle time	^tPC	40		45		55		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	55		60		70		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		ns	14
Read command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		20		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	55		60		75		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	16
Refresh period (256 cycles)	^tREF		8		8		8	ms	20
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ REFRESH)	^tCHR	15		15		15		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	19

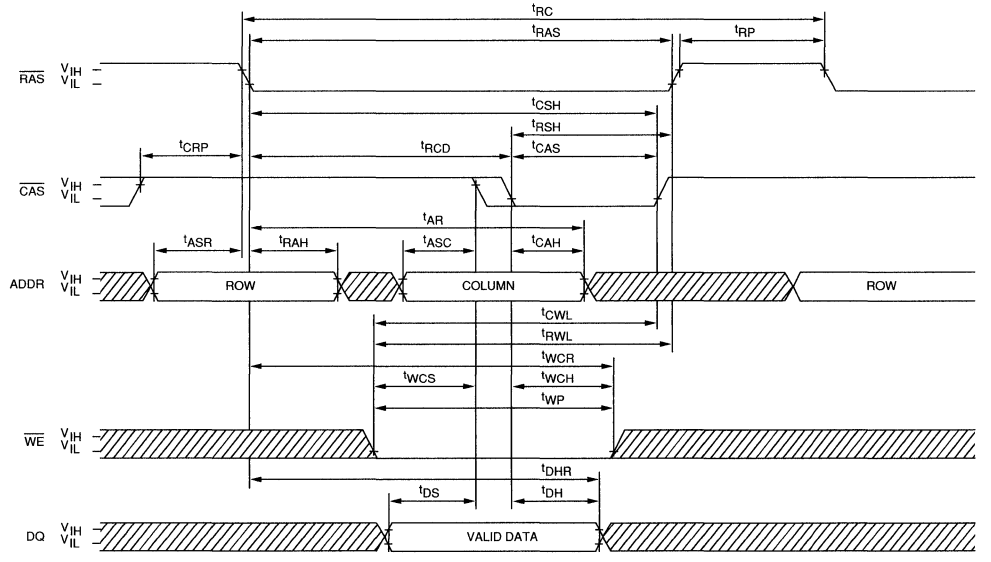
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\ ^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U16.
22. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

READ CYCLE



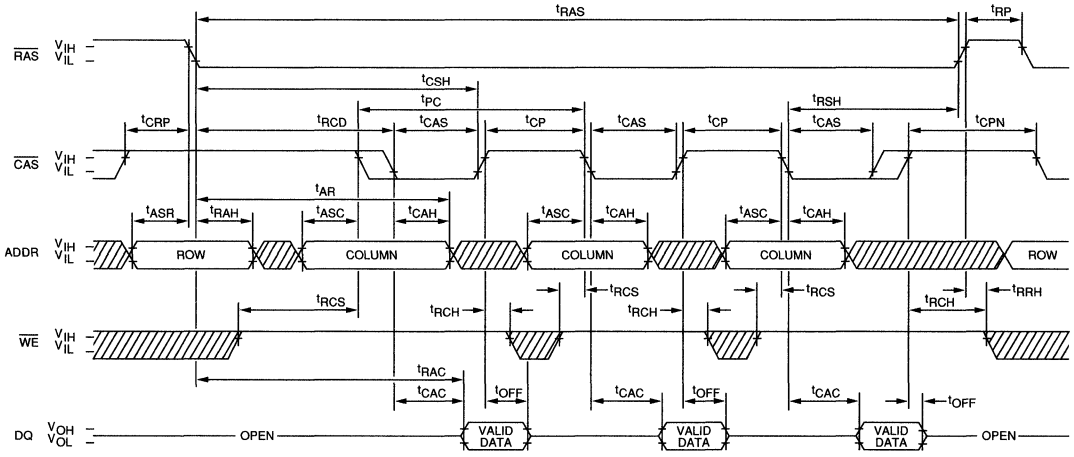
EARLY-WRITE CYCLE



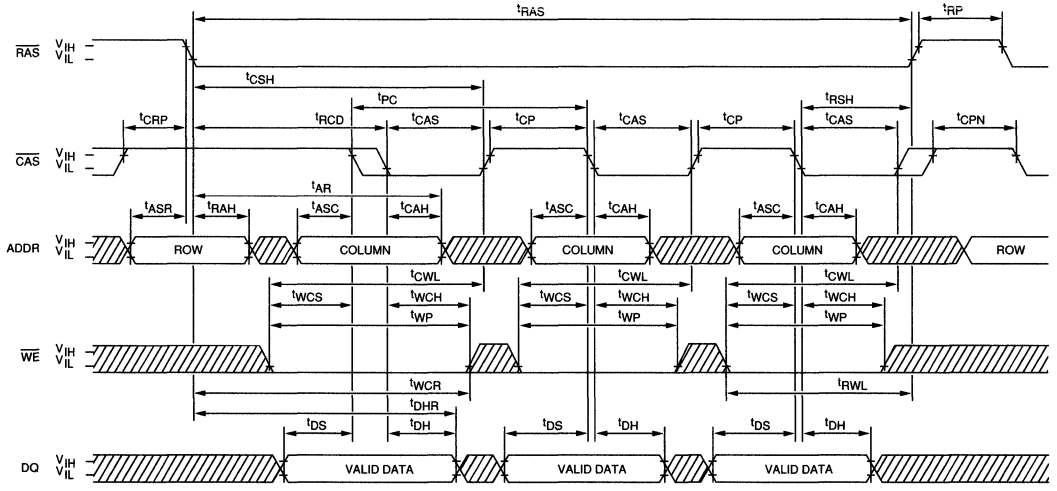
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



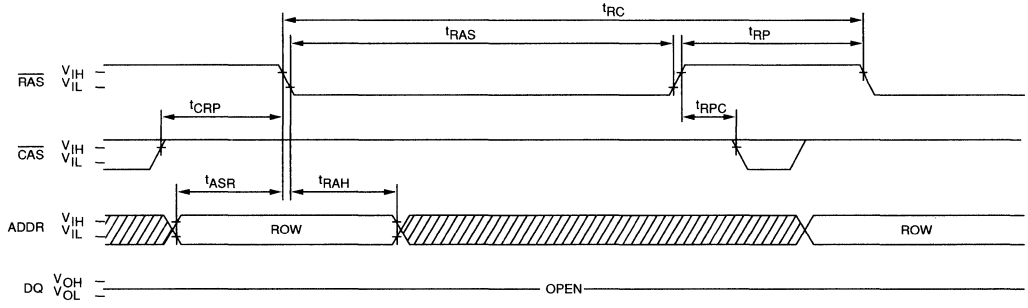
FAST-PAGE-MODE EARLY-WRITE CYCLE



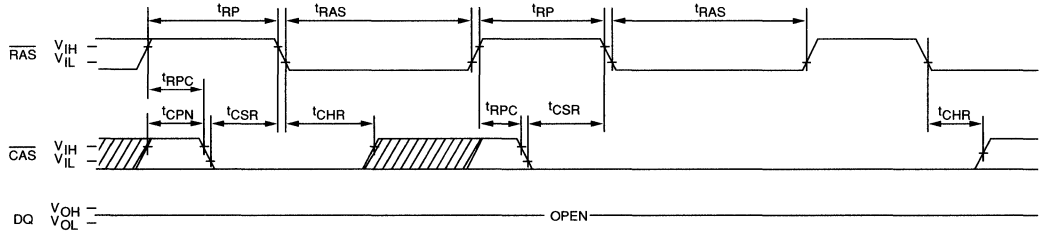
DON'T CARE

UNDEFINED

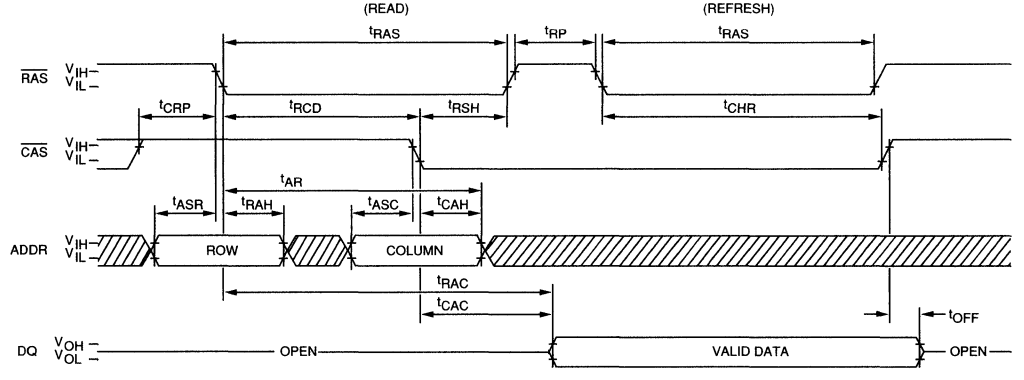
$\overline{RAS}$-ONLY REFRESH CYCLE
($ADDR = A_0 - A_7$; A_8 and $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
($A_0 - A_8$, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH) [20]



DRAM MODULE

1 MEG x 32 DRAM

FAST PAGE MODE

FEATURES

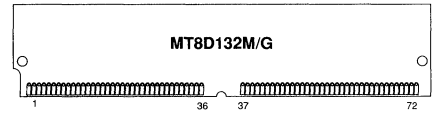
- Industry standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon gate process.
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 24mW standby; 1,800mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

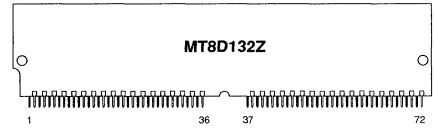
- Timing
  - 70ns access - 7
  - 80ns access - 8
  - 100ns access -10
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
  - Leaded 72-pin ZIP Z

PIN ASSIGNMENT (Top View)

72-Pin SIMM (I-5)



72-Pin ZIP (J-4)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

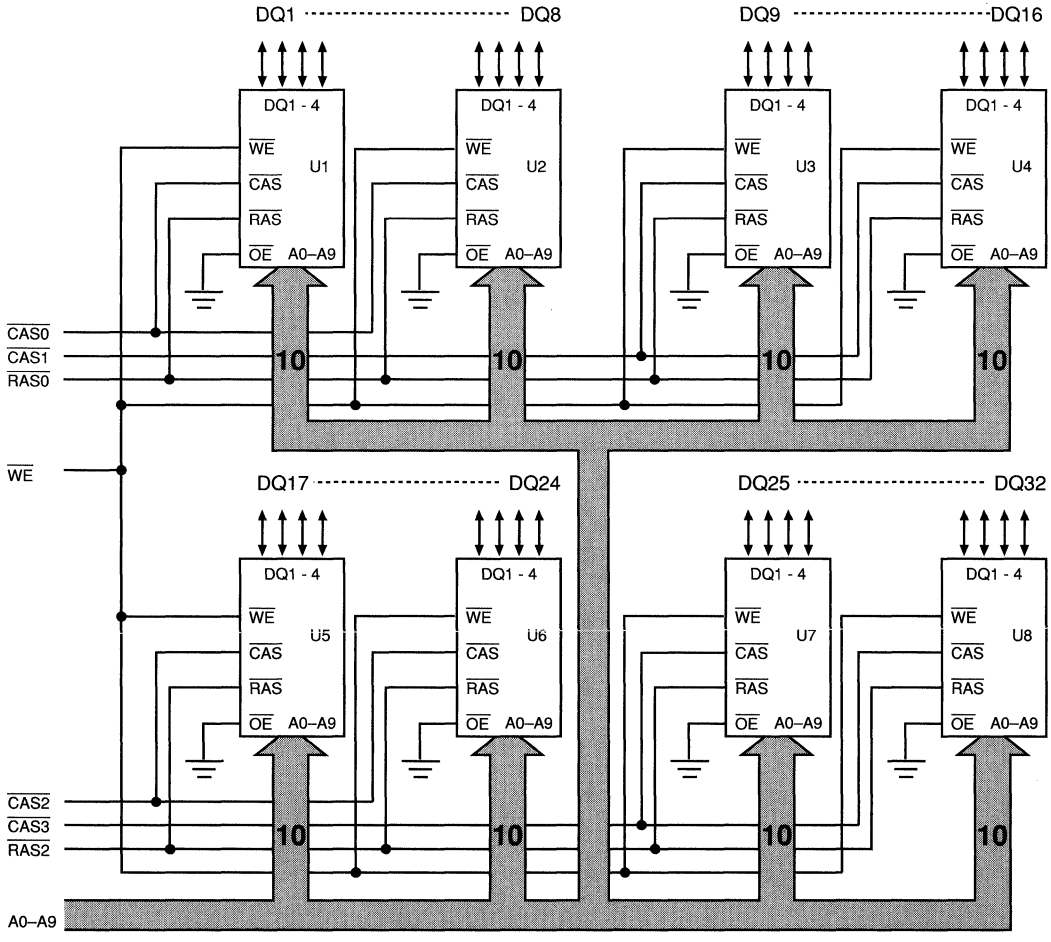
GENERAL DESCRIPTION

The MT8D132 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4001DJ

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	DQ1-32
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

PRESENCE DETECT

SYMBOL	-7	-8	-10
PRD1	NC	VSS	NC
PRD2	VSS	VSS	NC
PRD3	VSS	NC	NC
PRD4	NC	VSS	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input: $0V \le V_{IN} \le V_{CC}$ (All other pins not under test = 0V) For each package input	A0-A8, $\overline{WE}$	I_I	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le V_{OUT} \le V_{CC}$) For each package input	DQ1-DQ32	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $^tRC = {}^tRC$ (MIN))	I_{CC1}	800	720	640	mA	2
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ = Cycling: $^tPC = {}^tPC$ (MIN))	I_{CC2}	560	480	400	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles MIN)	I_{CC3}	16	16	16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{CC}$ -0.2V after 8 $\overline{RAS}$ cycles MIN All other inputs at Vcc -0.2V or Vss +0.2V)	I_{CC4}	8	8	8	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS} = V_{IH}$)	I_{CC5}	800	720	640	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	800	720	640	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		40	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		56	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		28	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS0}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		14	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}		7	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

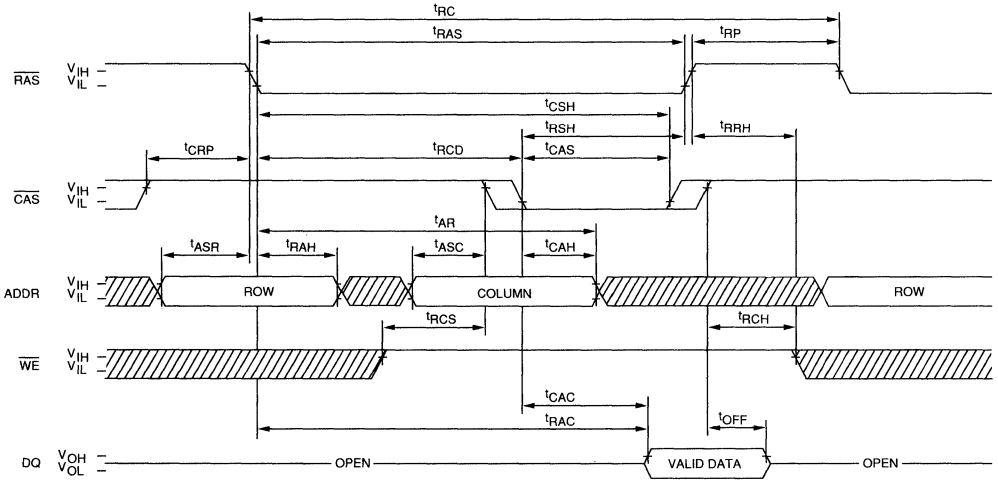
(Notes: 3, 4, 5, 10, 11, 16, 17) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	6, 7
FAST-PAGE-MODE cycle time	t_{PC}	40		45		55		ns	6, 7
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	7, 8
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	7, 9
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	50	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	t_{CRP}	5		5		20		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		70		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	15
Data-in hold time	t_{DH}	15		15		20		ns	15
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	
Transition time (rise or fall)	t_T	3	50	3	50	3	50	ns	16
Refresh period (256 cycles)	t_{REF}		16		16		16	ms	20
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	t_{CHR}	15		15		15		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	t_{CSR}	10		10		10		ns	19
$\overline{RAS}$-to-$\overline{CAS}$ precharge time	t_{RPC}	0		0		0		ns	19

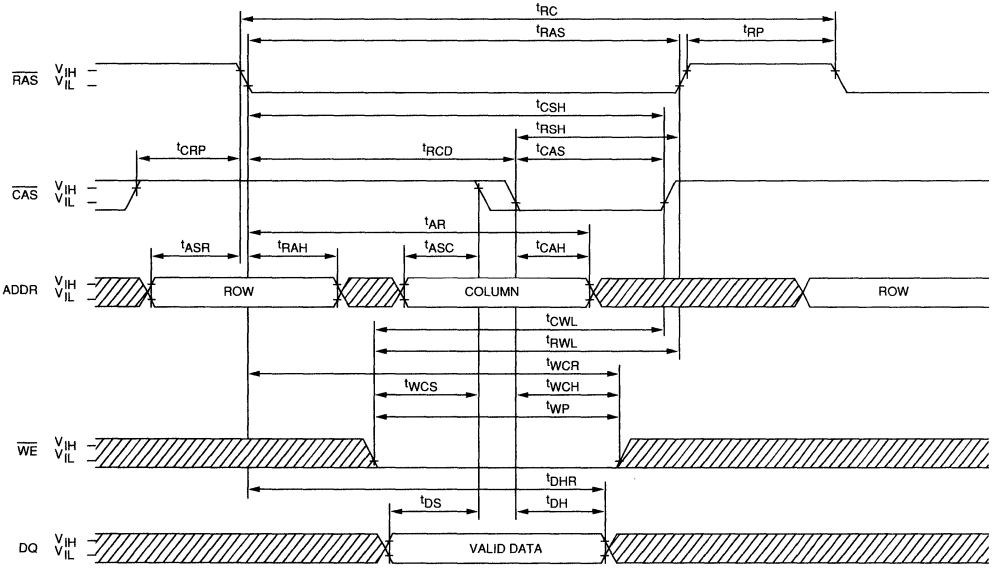
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\,^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U8.

READ CYCLE



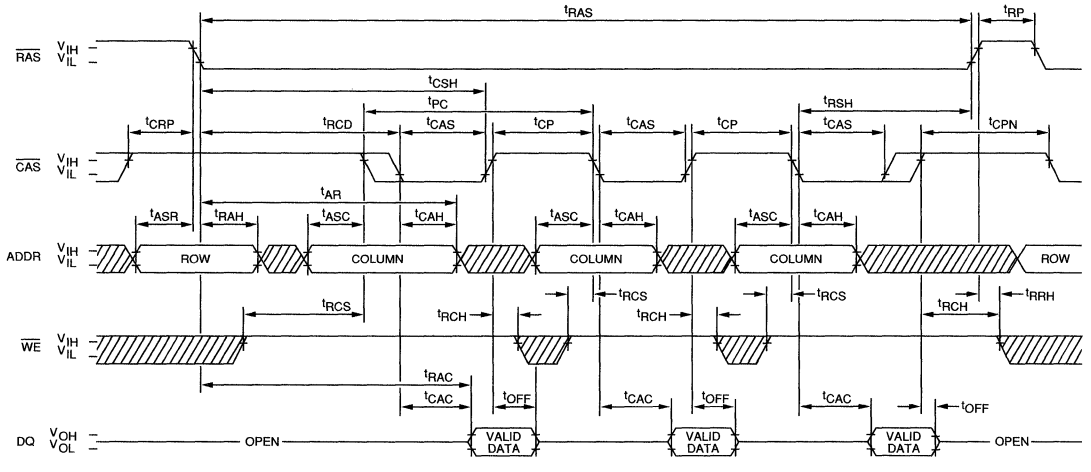
EARLY-WRITE CYCLE



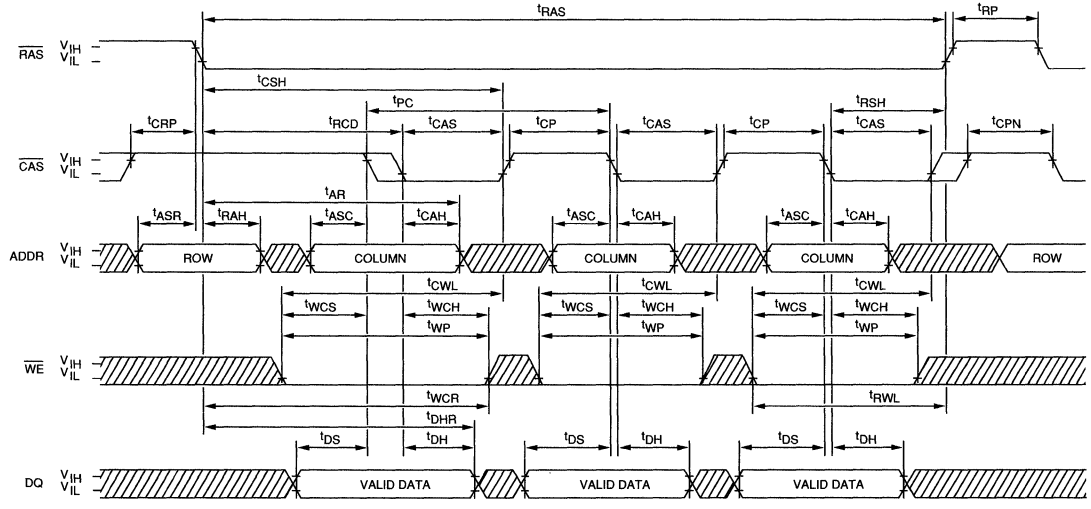
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



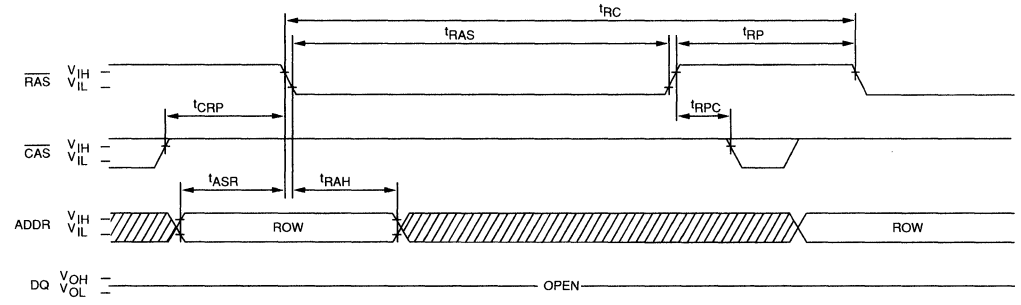
FAST-PAGE-MODE EARLY-WRITE CYCLE



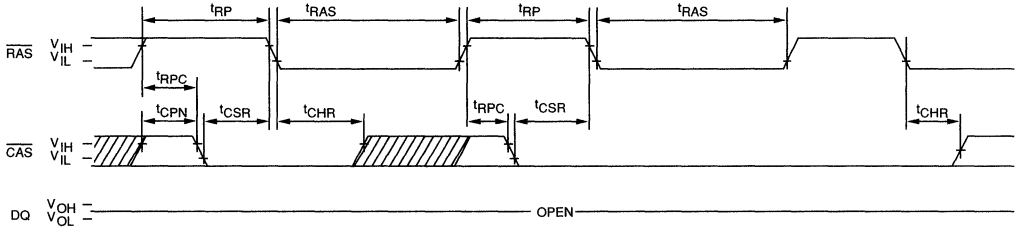
DON'T CARE

UNDEFINED

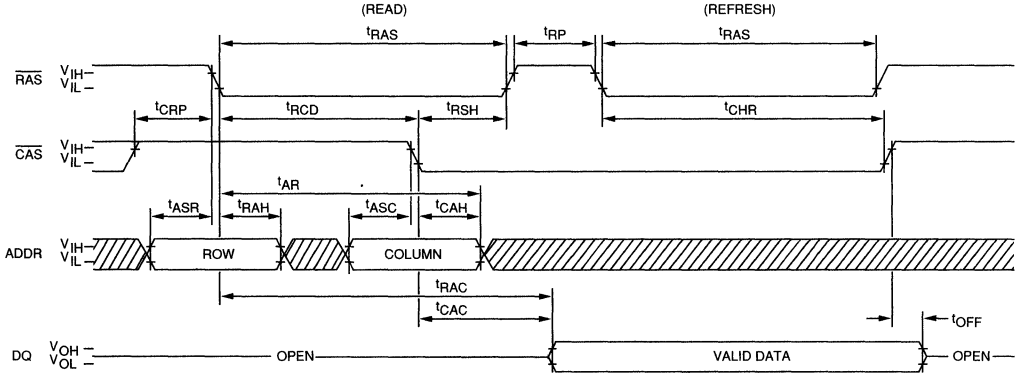
RAS-ONLY REFRESH CYCLE
(ADDR = A_0 - A_9; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A_0 - A_9, WE = DON'T CARE)



HIDDEN REFRESH CYCLE
(WE = HIGH) [20]



DON'T CARE

UNDEFINED

DRAM MODULE

2 MEG x 32 DRAM

FAST PAGE MODE

FEATURES

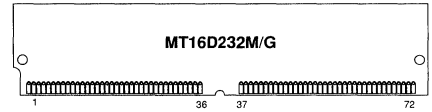
- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon gate process.
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 48mW standby; 3600mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

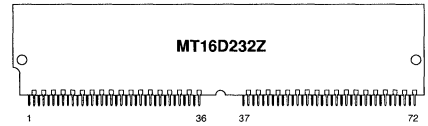
- Timing
  - 70ns access - 7
  - 80ns access - 8
  - 100ns access -10
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
  - Leaded 72-pin ZIP Z

PIN ASSIGNMENT (Top View)

72-Pin SIMM (I-6)



72-Pin ZIP (J-5)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	$\overline{RAS3}$	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

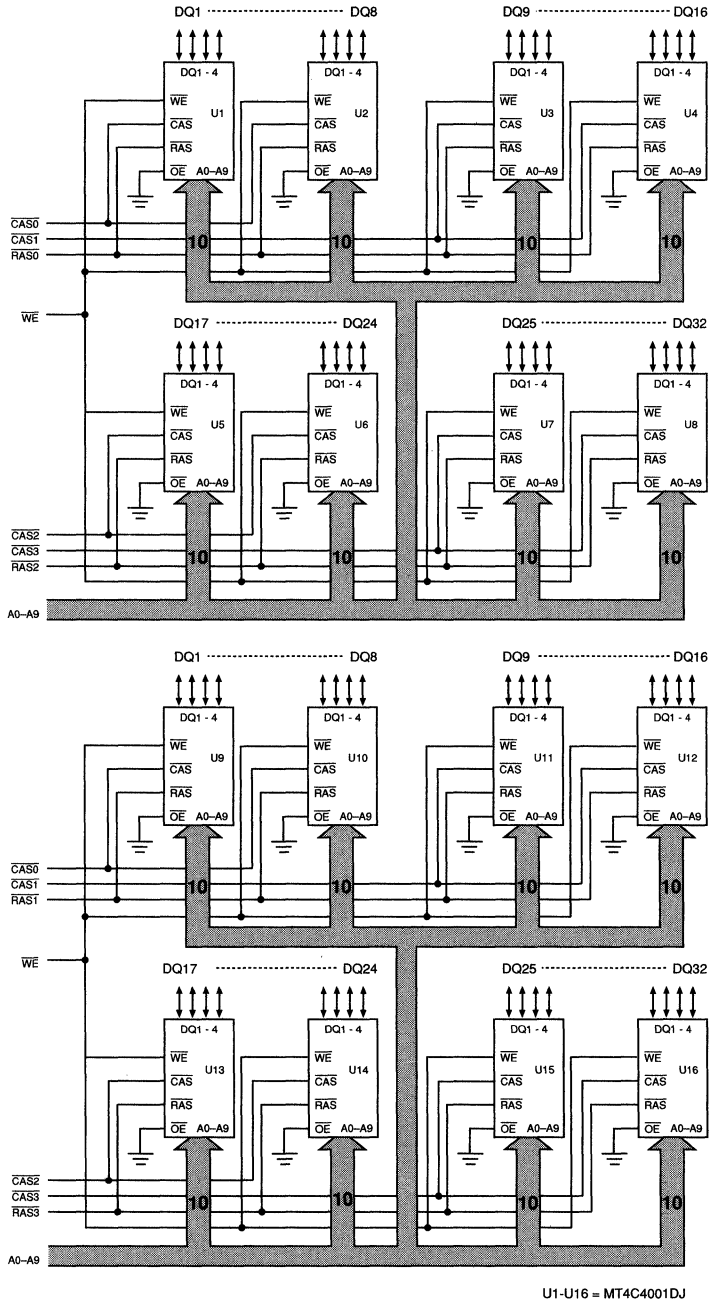
GENERAL DESCRIPTION

The MT16D232 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x32 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY-WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 1,024 combination of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4001DJ

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	DQ1-32
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-	1st Cycle	L	H→L	H	ROW	COL	Valid Data Out
MODE READ	2nd Cycle	L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-	1st Cycle	L	H→L	L	ROW	COL	Valid Data In
MODE WRITE	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN	READ	L→H→L	L	H	ROW	COL	Valid Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

PRESENCE DETECT

SYMBOL	-7	-8	-10
PRD1	NC	VSS	NC
PRD2	NC	VSS	NC
PRD3	VSS	VSS	NC
PRD4	NC	NC	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	$V_{CC}+1$	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input $0V \le V_{IN} \le V_{CC}$ (All other pins not under test = 0V) For each package input	A0-A9, $\overline{WE}$	I_I	-32	32	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le V_{OUT} \le V_{CC}$) For each package input	DQ1-DQ32	I_{OZ}	-24	24	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $^tRC = {}^tRC$ (MIN))	I_{CC1}	816	736	656	mA	2
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ = Cycling: $^tPC = {}^tPC$ (MIN))	I_{CC2}	576	496	416	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles (MIN))	I_{CC3}	32	32	32	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{CC}$ -0.2V after 8 $\overline{RAS}$ cycles (MIN)). (All other inputs at V_{CC} -0.2V or V_{SS} +0.2V)	I_{CC4}	16	16	16	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS} = V_{IH}$)	I_{CC5}	816	736	656	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	816	736	656	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		80	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		112	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$, $\overline{RAS0}$-$\overline{RAS3}$	C_{I4}		28	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}		14	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

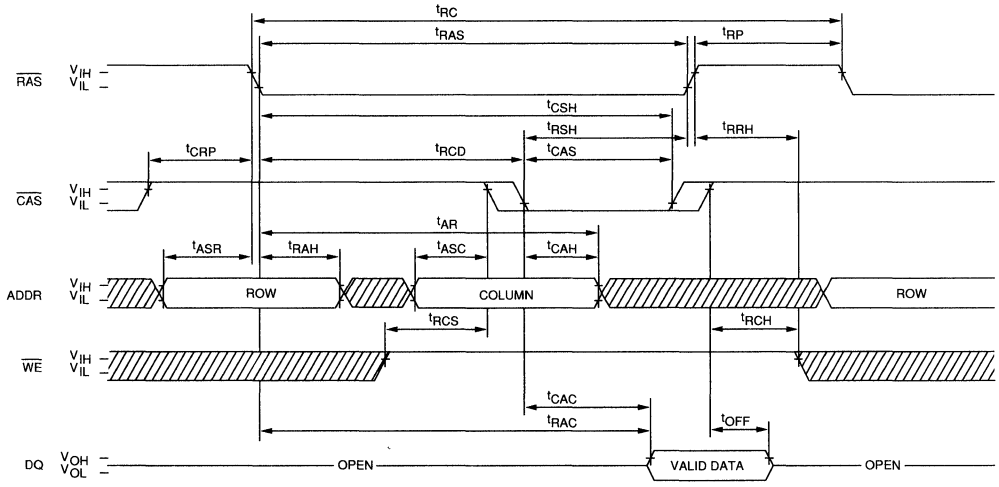
(Notes: 3, 4, 5, 10, 11, 16, 17) ($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	130		150		180		ns	6, 7
FAST-PAGE-MODE cycle time	^tPC	40		45		55		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	^tCRP	5		5		20		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	55		60		70		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		ns	14
Read command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		20		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	55		60		75		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	16
Refresh period (256 cycles)	^tREF		16		16		16	ms	20
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	15		15		15		ns	19
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	19

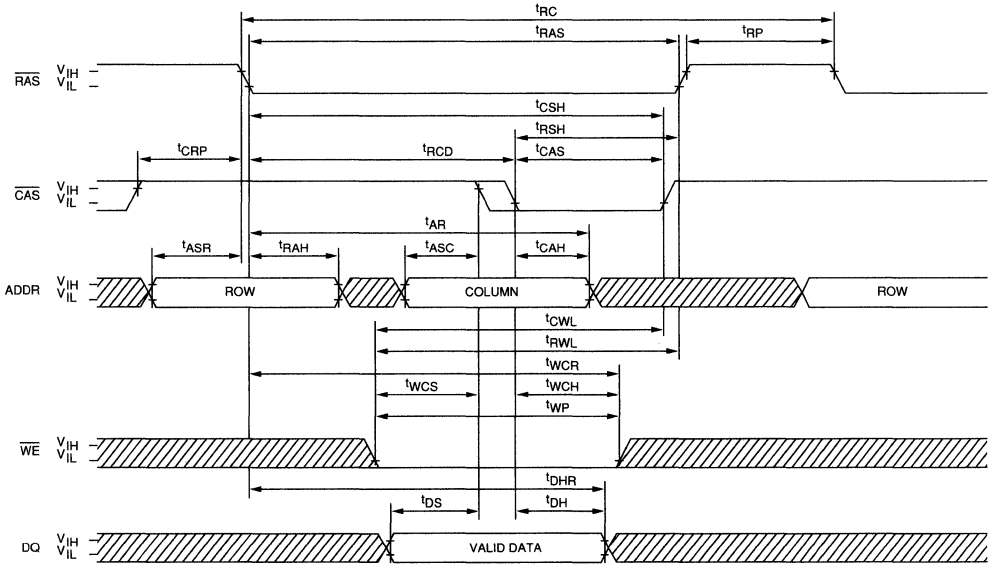
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U16.

READ CYCLE



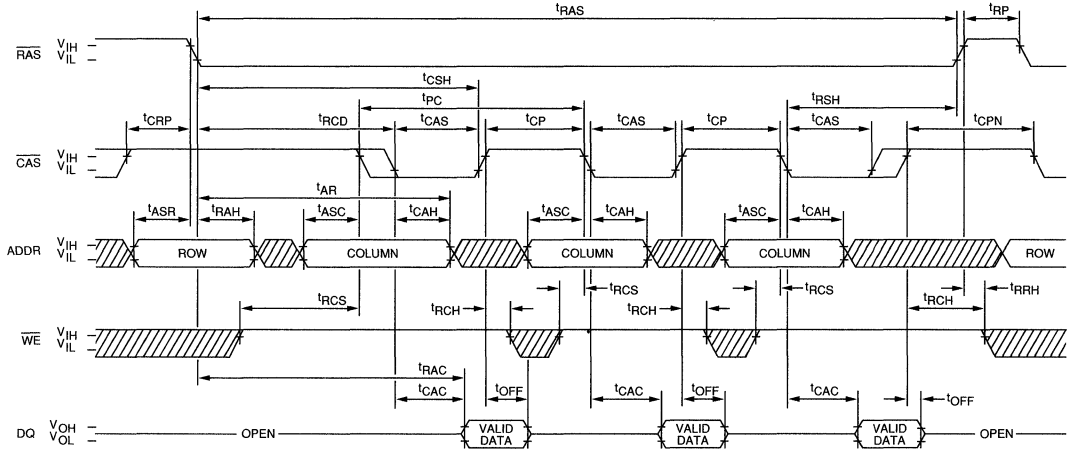
EARLY-WRITE CYCLE



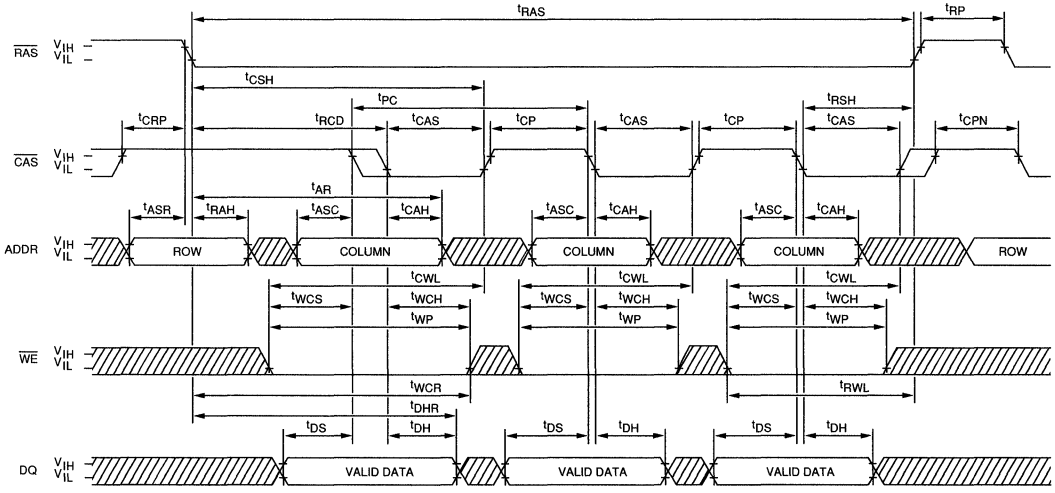
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



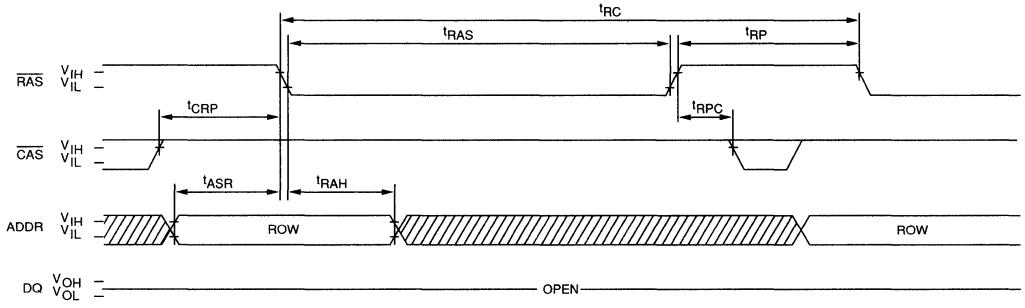
FAST-PAGE-MODE EARLY-WRITE CYCLE



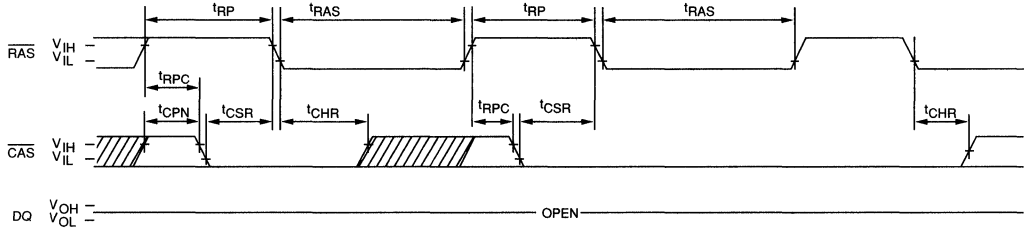
DON'T CARE

UNDEFINED

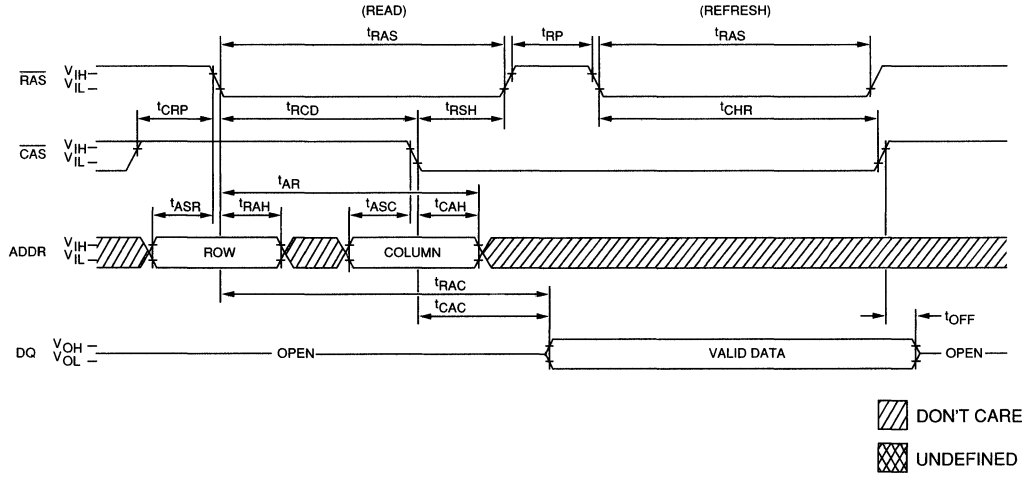
$\overline{RAS}$-ONLY REFRESH CYCLE
($ADDR = A_0 - A_9$; $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
($A_0 - A_9$, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH) [20]



DRAM MODULE

256K x 36 DRAM

FAST PAGE MODE

FEATURES

- Common $\overline{RAS}$ control pinout in a 72-pin single-in-line package
- High-performance CMOS silicon gate process.
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 27mW standby; 1,515mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh distributed across 8ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

- Timing

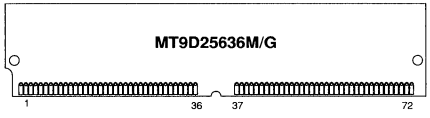
70ns access	- 7
80ns access	- 8
85ns access	-85
100ns access	-10

- Packages

Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (Gold)	G
Leaded 72-pin ZIP	Z

PIN ASSIGNMENT (Top View)

72-Pin SIMM (I-7)



72-Pin ZIP (J-6)

PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	NC	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS0}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

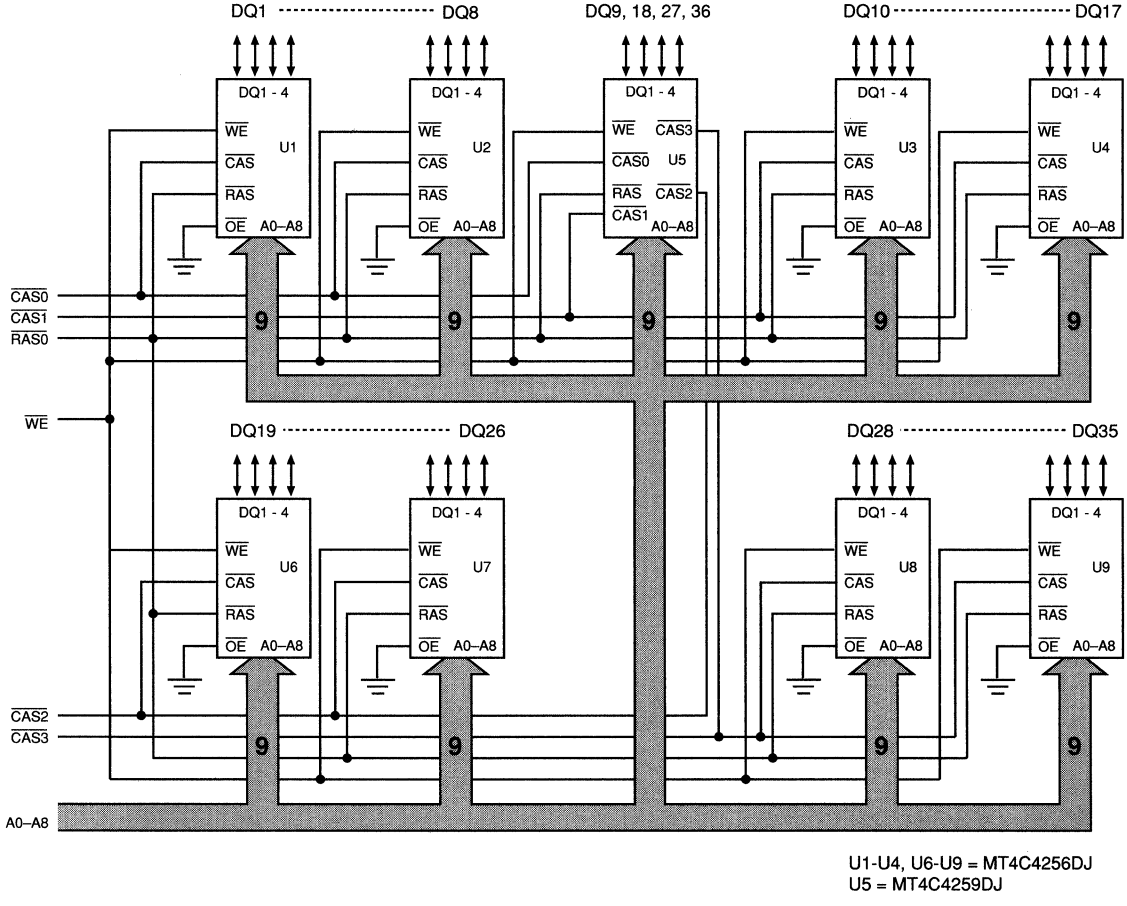
GENERAL DESCRIPTION

The MT9D25636 is a randomly accessed solid-state memory containing 262,144 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U4, U6-U9 = MT4C4256DJ
U5 = MT4C4259DJ

NOTE: Due to the use of a Quad $\overline{CAS}$ parity DRAM, $\overline{RAS0}$ is common to all devices.

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	DQ1-36
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L→H	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L→H	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L→H	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L→H	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

PRESENCE DETECT

SYMBOL	-7	-8	-85	-10
PRD1	NC	VSS	VSS	VSS
PRD2	NC	NC	NC	NC
PRD3	VSS	VSS	NC	VSS
PRD4	VSS	NC	VSS	VSS

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-2.0	0.8	V	1, 22
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V) For each package input	A0-A8, $\overline{WE}$	II	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ Vcc) For each package input	DQ1-DQ36	IOZ	-12	12	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	1
Output Low Voltage (IOUT = 5mA)		VOL		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8, -85	-10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	ICC1	720	630	540	mA	2
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = VIL, $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	ICC2	540	450	360	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = VIH after 8 $\overline{RAS}$ cycles (MIN))	ICC3	18	18	18	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V after 8 $\overline{RAS}$ cycles (MIN)). (All other inputs at Vcc -0.2V or Vss +0.2V)	ICC4	9	9	9	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = VIH)	ICC5	720	630	540	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	ICC6	720	630	540	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	CI1		45	pF	17
Input Capacitance: $\overline{WE}$	CI2		63	pF	17
Input Capacitance: $\overline{RAS0}$	CI3		63	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	CI4		21	pF	17
Input/Output Capacitance: DQ1-DQ36	CIO		7	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

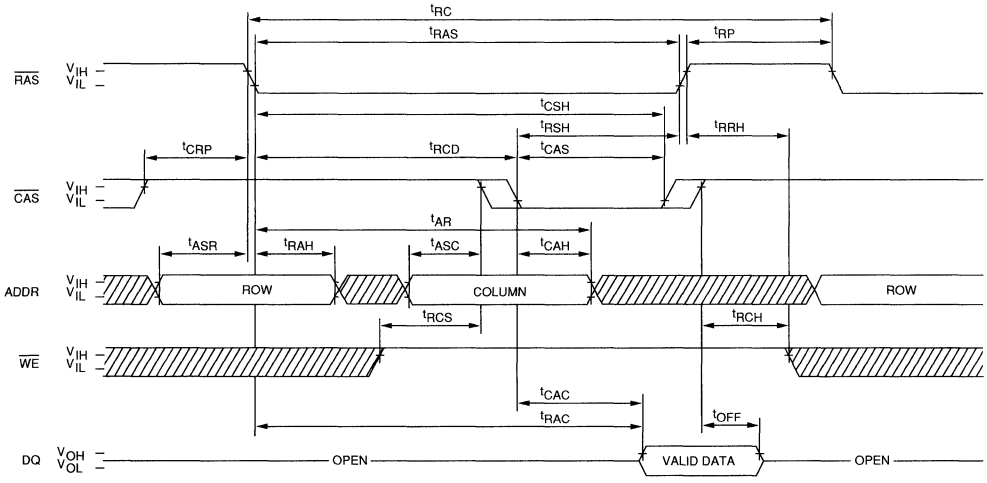
(Notes: 3, 4, 5, 10, 11, 16, 17) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8, -85		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	135		150		180		ns	6, 7
FAST-PAGE-MODE cycle time	^tPC	40		45		55		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	55		60		70		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		ns	14
Read command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	^tWCR	55		60		75		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		20		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	55		60		75		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	16
Refresh period (256 cycles)	^tREF		8		8		8	ms	20
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	15		15		15		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	19

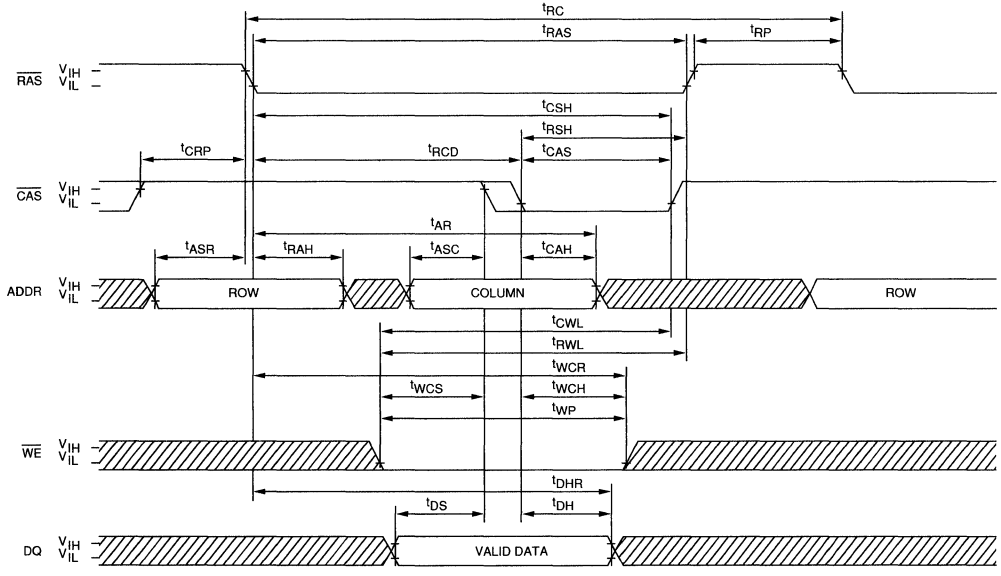
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. ^{t}RCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U9.
22. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

READ CYCLE



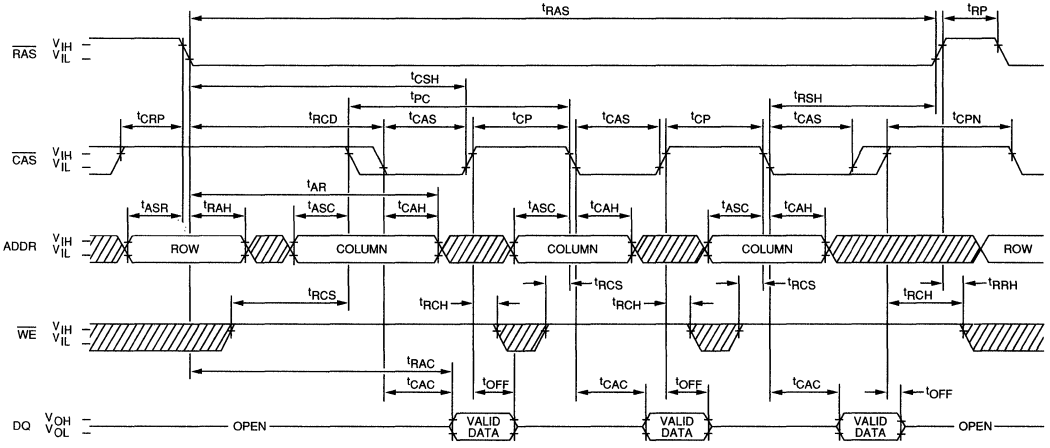
EARLY-WRITE CYCLE



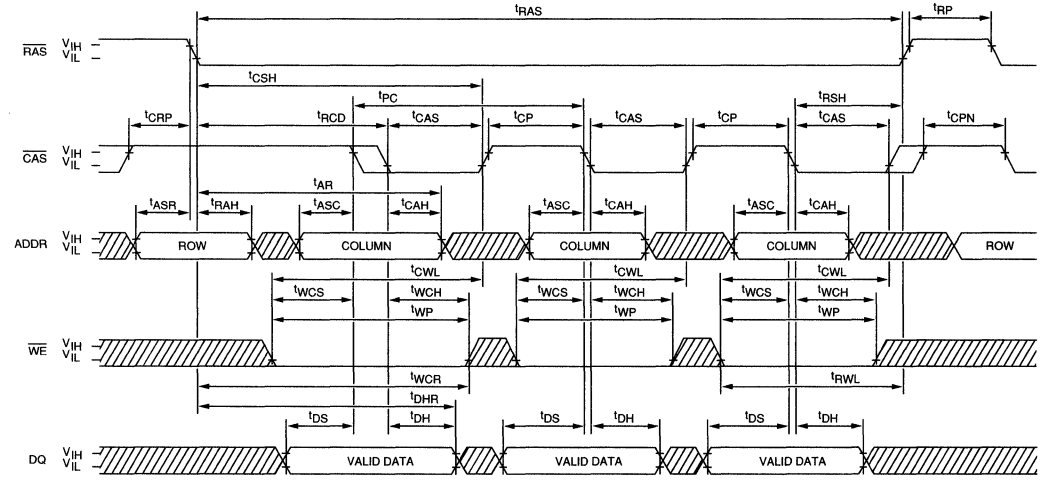
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

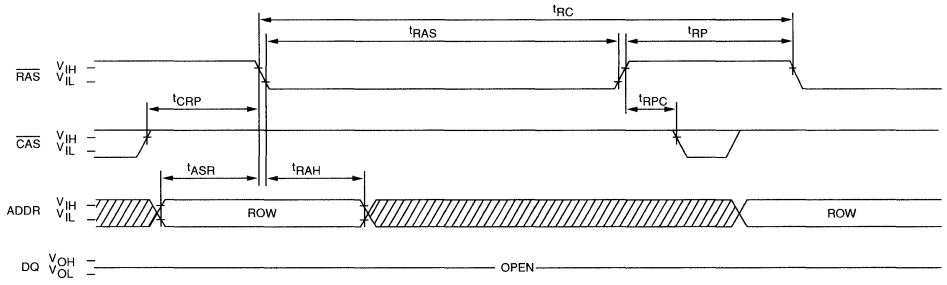


DON'T CARE

UNDEFINED

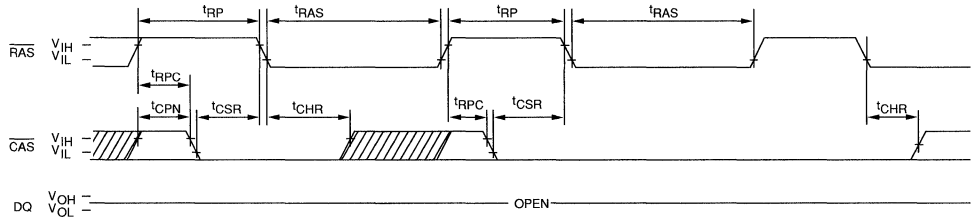
$\overline{RAS}$-ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE)



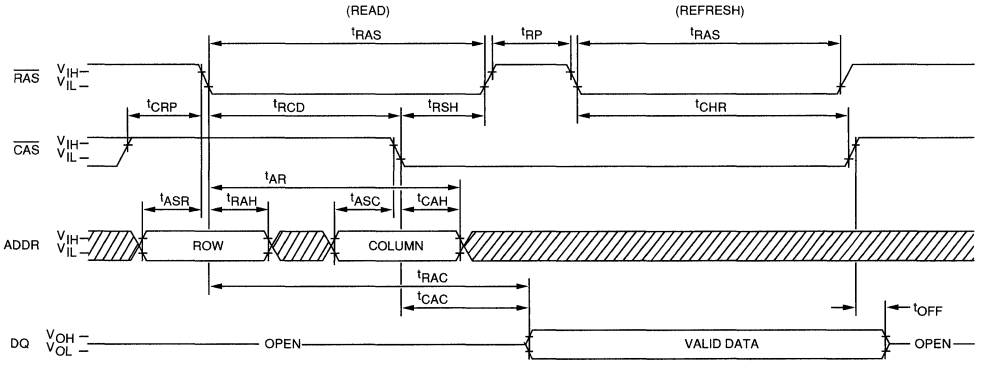
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH) [20]



DRAM MODULE

256K x 36 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon gate process.
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 30mW standby; 1,750mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, and HIDDEN
- 512-cycle refresh distributed across 8ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

- Timing

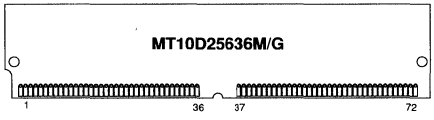
70ns access	- 7
80ns access	- 8
85ns access	-85
100ns access	-10

- Packages

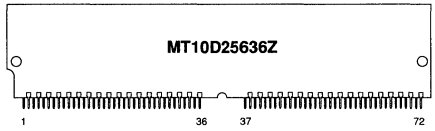
Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (Gold)	G
Leaded 72-pin ZIP	Z

PIN ASSIGNMENT (Top View)

72-Pin SIMM (I-9)



72-Pin ZIP (J-8)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	NC	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

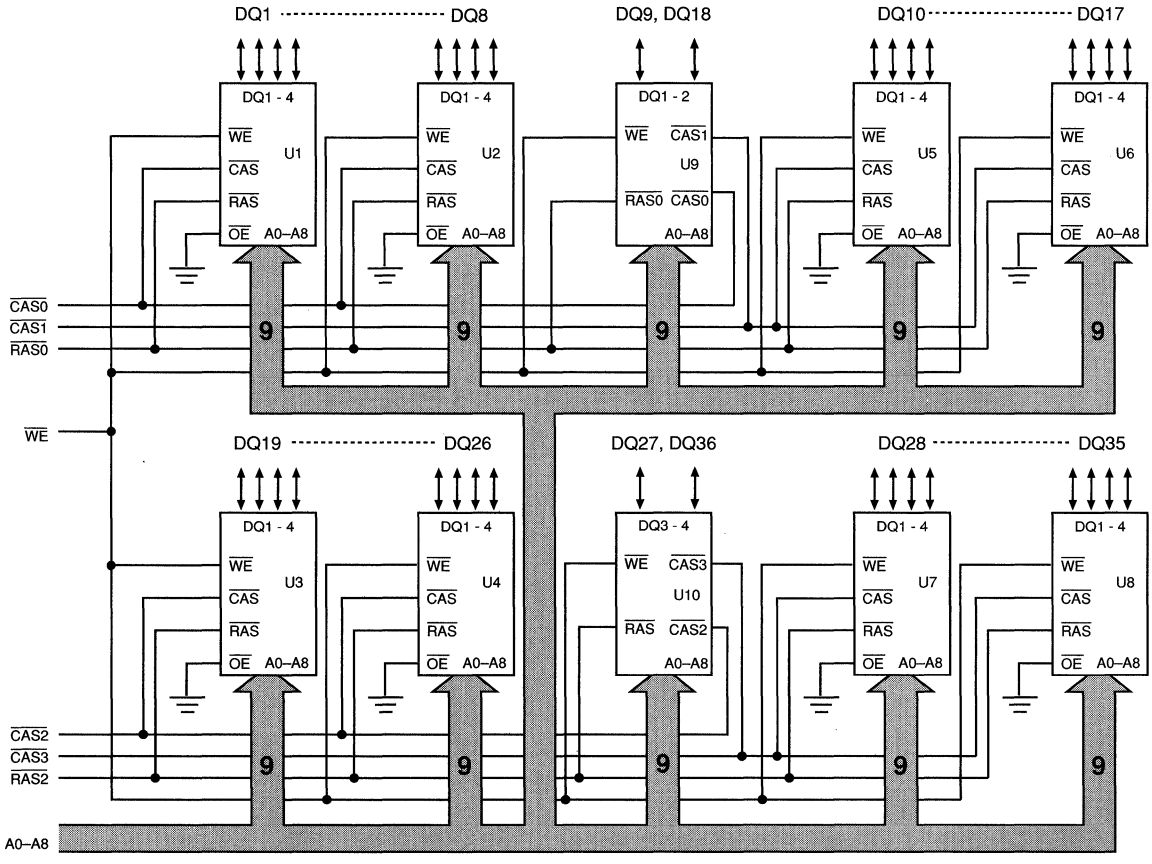
GENERAL DESCRIPTION

The MT10D25636 is a randomly accessed solid-state memory containing 262,144 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4256DJ
U9 & U10 = MT4C4259DJ

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	DQ1-36
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L→H	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L→H	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L→H	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L→H	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

PRESENCE DETECT

SYMBOL	-7	-8	-85	-10
PRD1	NC	VSS	VSS	VSS
PRD2	NC	NC	NC	NC
PRD3	VSS	VSS	NC	VSS
PRD4	VSS	NC	VSS	VSS

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 10W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-2.0	0.8	V	1, 22
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V) for each package input	A0-A8, $\overline{WE}$	I_I	-20	20	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ Vcc) for each package input	DQ1-DQ36	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8, -85	-10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	800	700	600	mA	2
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	600	500	400	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles (MIN))	I_{CC3}	20	20	20	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V after 8 $\overline{RAS}$ cycles (MIN)). (All other inputs at Vcc -0.2V or Vss +0.2V)	I_{CC4}	10	10	10	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}	800	700	600	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	800	700	600	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		50	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		70	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		35	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		21	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		7	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

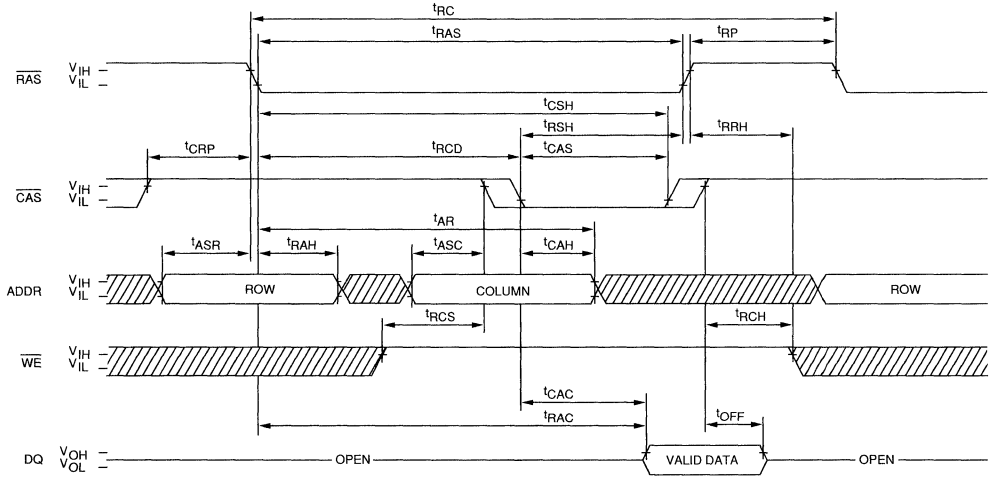
(Notes: 3, 4, 5, 10, 11, 16, 17) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8, -85		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	135		150		180		ns	6, 7
FAST-PAGE-MODE cycle time	tPC	40		45		55		ns	6, 7
Access time from $\overline{RAS}$	tRAC		70		80		100	ns	7, 8
Access time from $\overline{CAS}$	tCAC		20		20		25	ns	7, 9
$\overline{RAS}$ pulse width	tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	tCPN	10		10		15		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	50	20	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	tCRP	5		5		5		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		15		ns	
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	55		60		70		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	14
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	55		60		75		ns	
Write command pulse width	tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	tCWL	20		20		25		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	15		15		20		ns	15
Data-in hold time referenced to $\overline{RAS}$	tDHR	55		60		75		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	16
Refresh period (256 cycles)	tREF		8		8		8	ms	20
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCHR	15		15		15		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCSR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	19

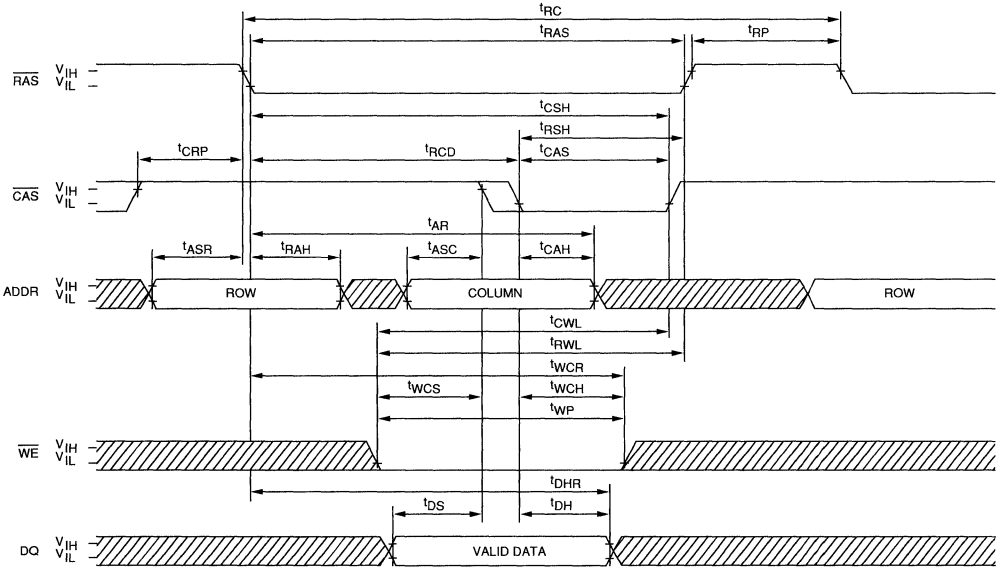
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\ ^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U9.
22. The module shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

READ CYCLE



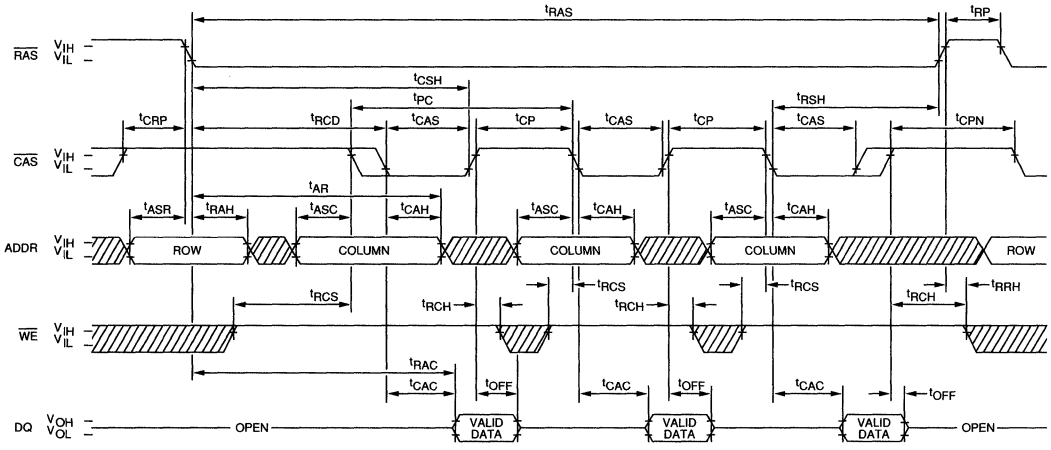
EARLY-WRITE CYCLE



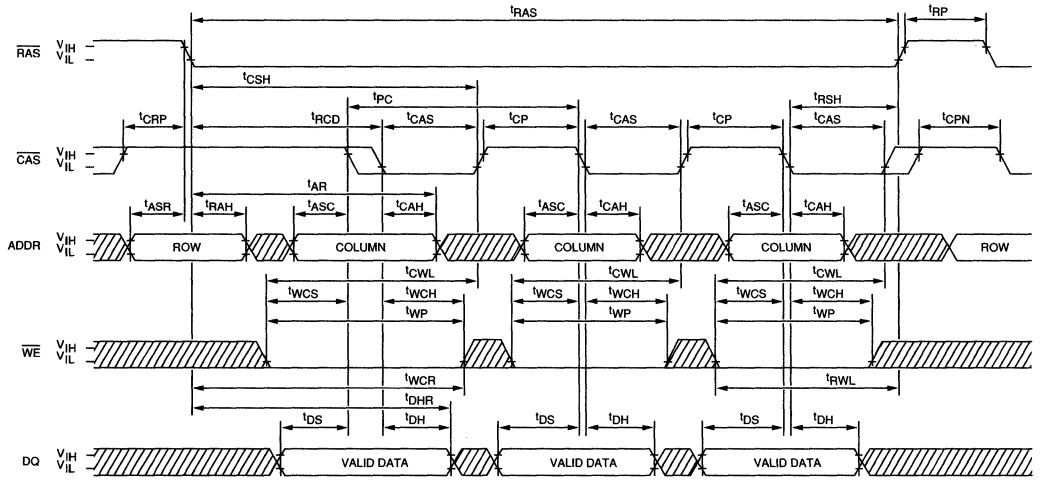
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

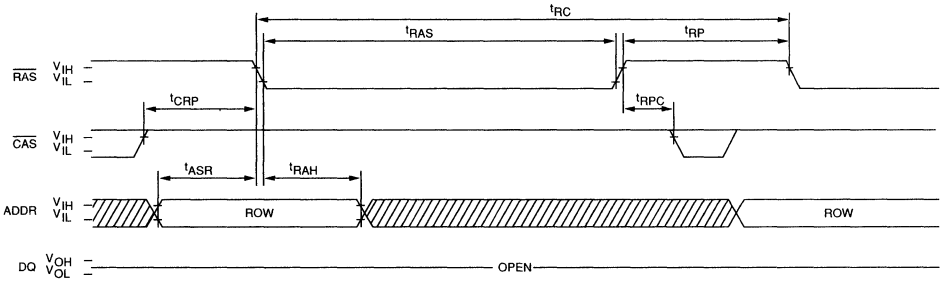


DON'T CARE

UNDEFINED

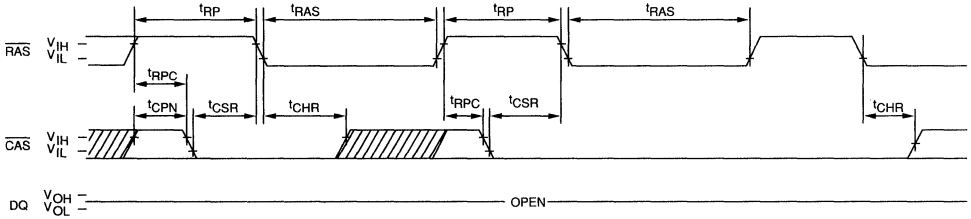
$\overline{RAS}$-ONLY REFRESH CYCLE

($ADDR = A_0 - A_7$; A_8 and $\overline{WE}$ = DON'T CARE)



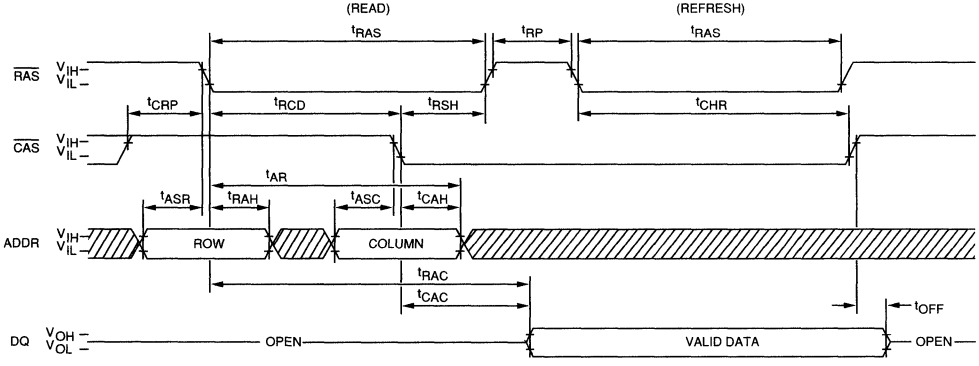
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

($A_0 - A_8$, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH) [20]



DON'T CARE

UNDEFINED

DRAM MODULE

512K x 36 DRAM

FAST PAGE MODE

FEATURES

- Common $\overline{RAS}$ control per side pinout in a 72-pin single-in-line package
- High performance CMOS silicon gate process.
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 54mW standby; 3,150mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh distributed across 8ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

- Timing

70ns access	- 7
80ns access	- 8
85ns access	-85
100ns access	-10

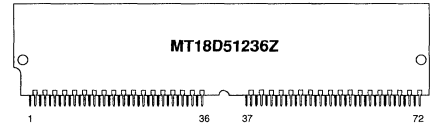
- Packages

Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (Gold)	G
Leaded 72-pin ZIP	Z

PIN ASSIGNMENT (Top View)

72-Pin SIMM (I-8)

72-Pin ZIP (J-7)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	$\overline{RAS1}$	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	NC	50	DQ28	68	PRD2
15	A3	33	$\overline{RAS1}$	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS0}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

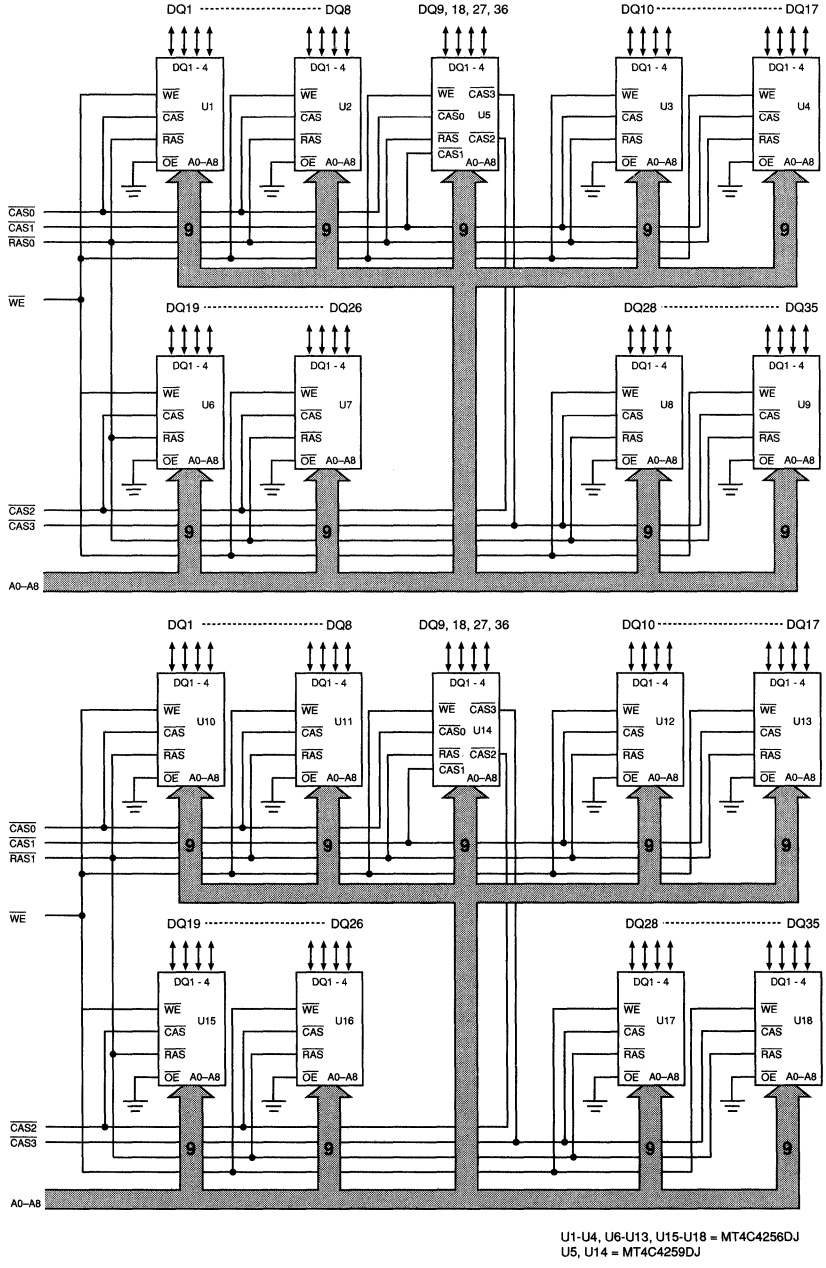
GENERAL DESCRIPTION

The MT18D51236 is a randomly accessed solid-state memory containing 524,288 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U4, U6-U13, U15-U18 = MT4C4256DJ
U5, U14 = MT4C4259DJ

NOTE: Due to the use of a Quad $\overline{CAS}$ parity DRAM, $\overline{RAS0}$ is common to side 1 and $\overline{RAS1}$ is common to side 2.

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	DQ1-36
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L→H	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L→H	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L→H	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L→H	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

PRESENCE DETECT

SYMBOL	-7	-8	-85	-10
PRD1	VSS	NC	NC	NC
PRD2	VSS	VSS	VSS	VSS
PRD3	NC	VSS	NC	VSS
PRD4	NC	NC	VSS	VSS

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 18W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-2.0	0.8	V	1, 22
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V) For each package input	A0-A8, $\overline{WE}$	I_I	-36	36	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ Vcc) For each package input	DQ1-DQ36	I_{OZ}	-24	24	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8, -85	-10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	738	648	558	mA	2
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	558	468	378	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles (MIN))	I_{CC3}	36	36	36	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V after 8 $\overline{RAS}$ cycles (MIN)). (All other inputs at Vcc -0.2V or Vss +0.2V)	I_{CC4}	18	18	18	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}	738	648	558	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	738	648	558	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		90	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		126	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$	C_{I3}		63	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		42	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		14	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

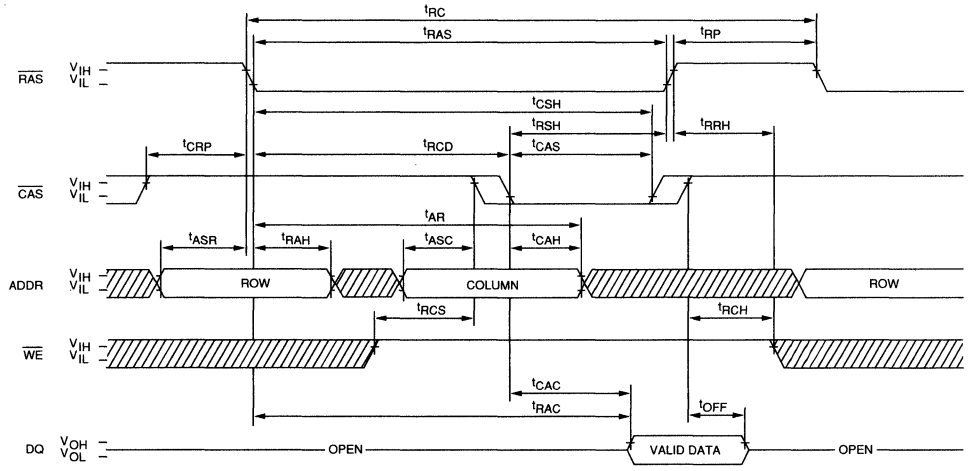
(Notes: 3, 4, 5, 10, 11, 16, 17) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5.0V \pm 10\ \%$)

A.C. CHARACTERISTICS		-7		-8, -85		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	135		150		180		ns	6, 7
FAST-PAGE-MODE cycle time	tPC	40		45		55		ns	6, 7
Access time from $\overline{RAS}$	tRAC		70		80		100	ns	7, 8
Access time from $\overline{CAS}$	tCAC		20		20		25	ns	7, 9
$\overline{RAS}$ pulse width	tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	tCPN	10		10		15		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	40	20	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	tCRP	5		5		5		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		15		ns	
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	55		60		70		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	14
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	55		60		75		ns	
Write command pulse width	tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	tCWL	20		20		25		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	15		15		20		ns	15
Data-in hold time referenced to $\overline{RAS}$	tDHR	55		60		75		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	16
Refresh period (256 cycles)	tREF		8		8		8	ms	20
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCHR	15		15		15		ns	19
$\overline{CAS}$ setup time $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCSR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	19

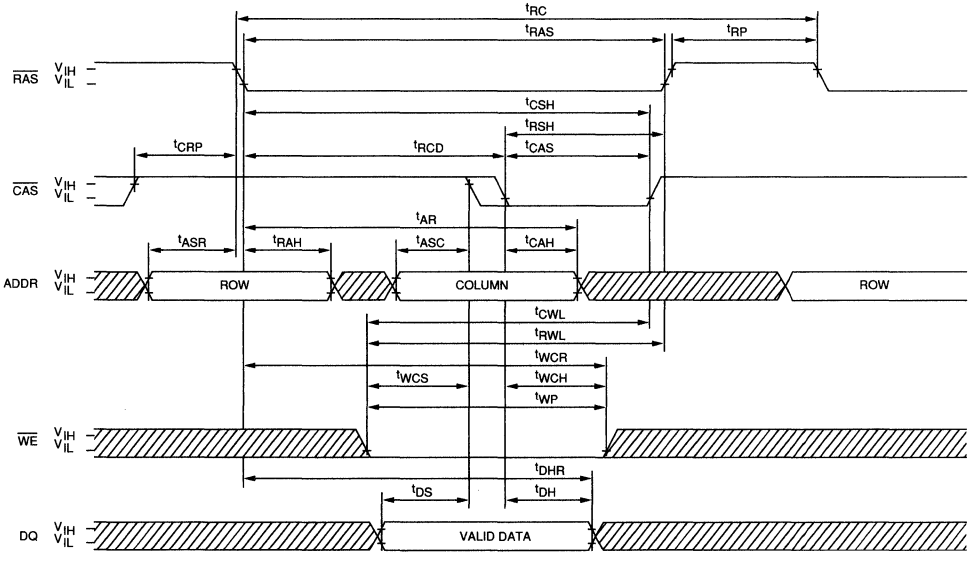
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\,^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U18.
22. The module shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

READ CYCLE



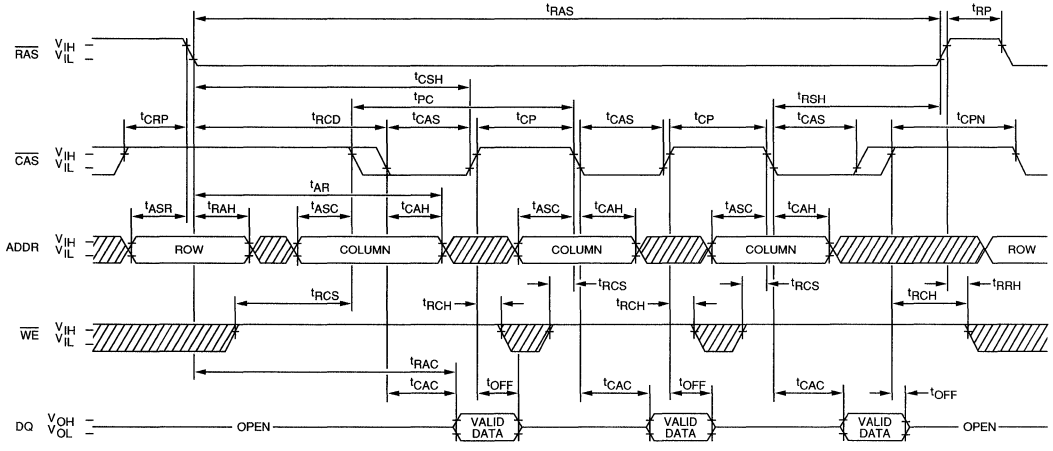
EARLY-WRITE CYCLE



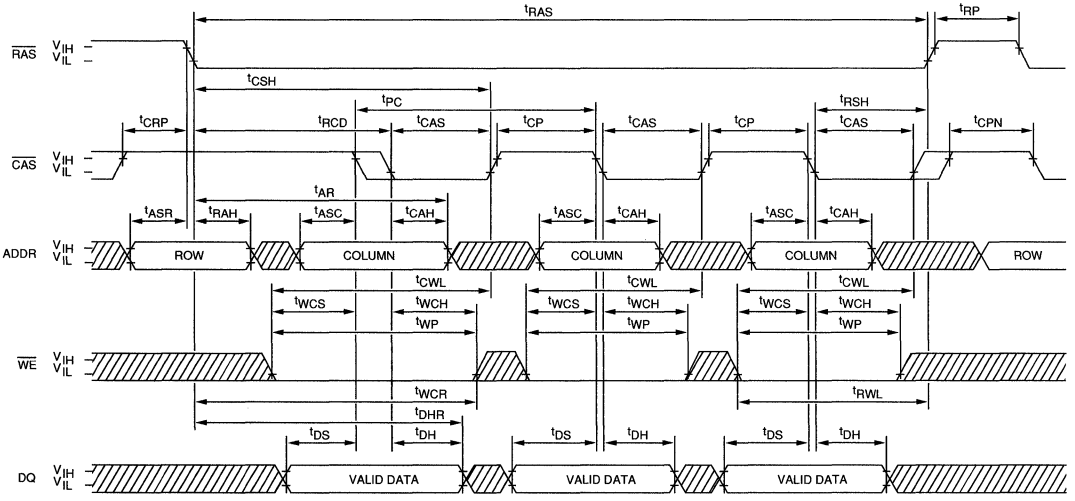
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

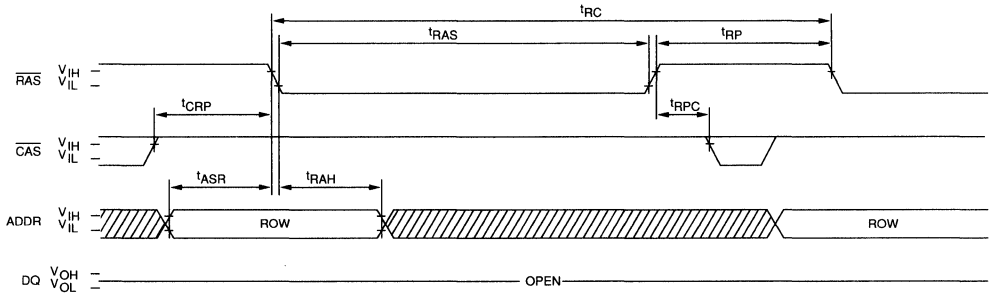


DON'T CARE

UNDEFINED

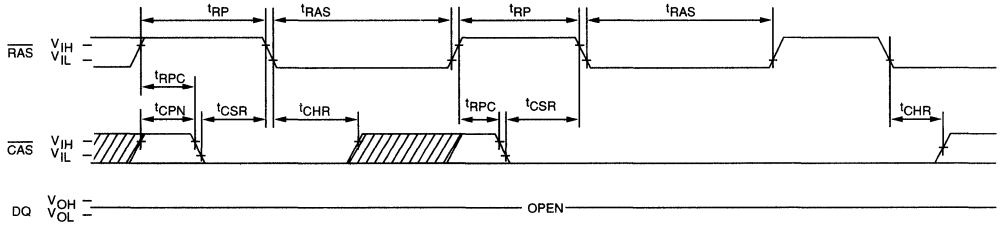
$\overline{RAS}$-ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE)



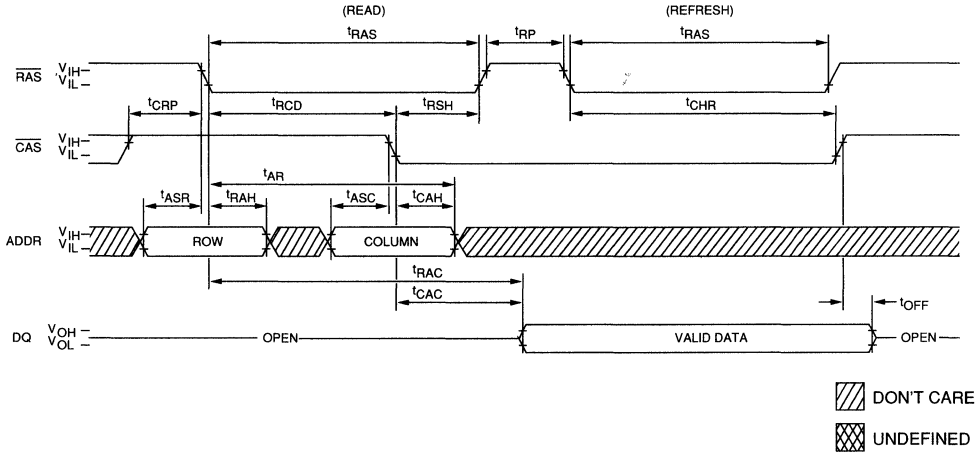
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH) [20]



DRAM MODULE

512K x 36 DRAM

FAST PAGE MODE

FEATURES

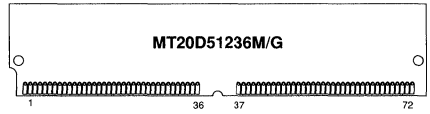
- Industry standard pinout in a 72-pin single-in-line package
- High performance CMOS silicon gate process.
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 60mW standby; 1,780mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh distributed across 8ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

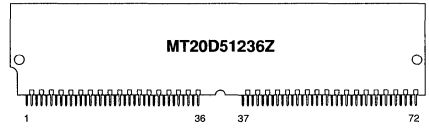
- Timing
  - 70ns access - 7
  - 80ns access - 8
  - 85ns access -85
  - 100ns access -10
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
  - Leaded 72-pin ZIP Z

PIN ASSIGNMENT (Top View)

72-Pin SIMM (I-10)



72-Pin ZIP (J-9)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	$\overline{RAS1}$	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	NC	50	DQ28	68	PRD2
15	A3	33	$\overline{RAS3}$	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

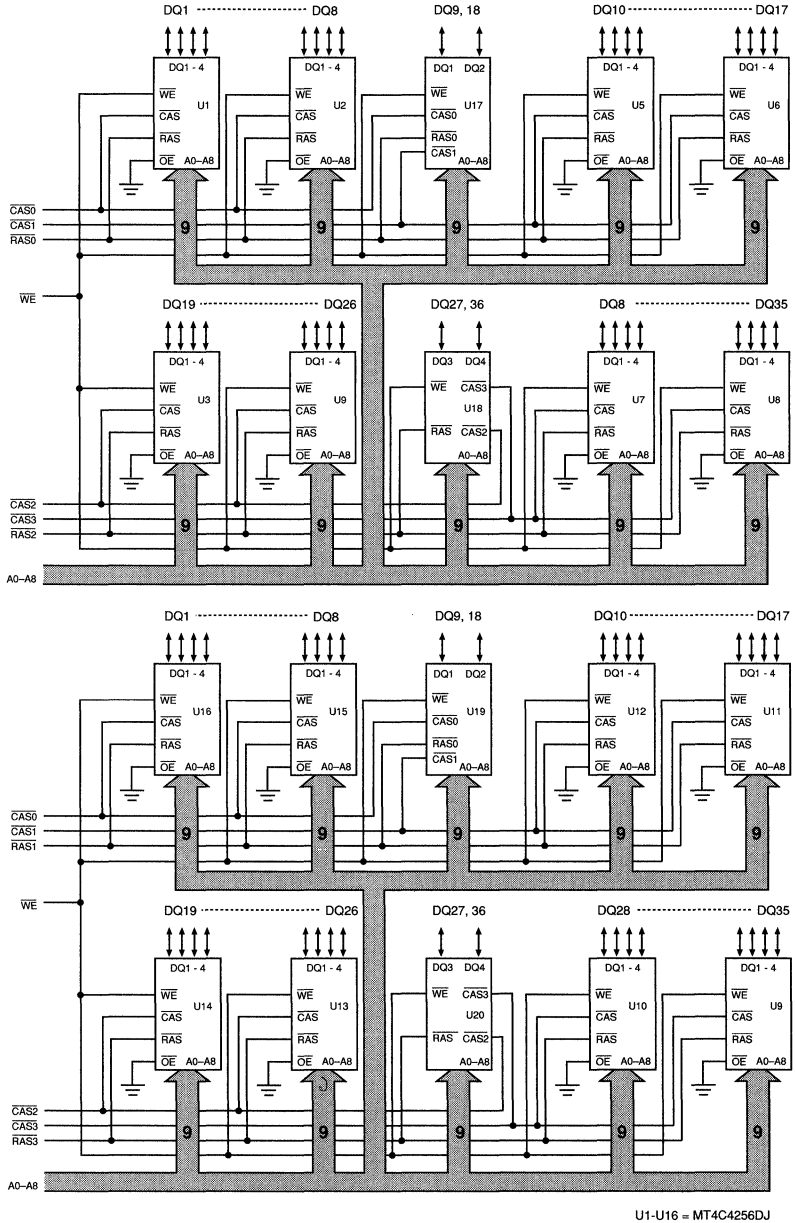
GENERAL DESCRIPTION

The MT20D51236 is a randomly accessed solid-state memory containing 524,288 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4256DJ
U17- 20 = MT4C4259DJ

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	DQ1-36
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L→H	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L→H	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L→H	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L→H	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

PRESENCE DETECT

SYMBOL	-7	-8	-85	-10
PRD1	VSS	NC	NC	NC
PRD2	VSS	VSS	VSS	VSS
PRD3	NC	VSS	NC	VSS
PRD4	NC	NC	VSS	VSS

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 20W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-2.0	0.8	V	1, 22
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V) for each package input	A0-A8, $\overline{WE}$	II	-40	40	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ Vcc) for each package input	DQ1-DQ36	IOZ	-24	24	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	1
Output Low Voltage (IOUT = 5mA)		VOL		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8, -85	-10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	ICC1	820	720	620	mA	2
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = VIL, $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	ICC2	620	520	420	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = VIH after 8 $\overline{RAS}$ cycles (MIN))	ICC3	40	40	40	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V after 8 $\overline{RAS}$ cycles (MIN)). (All other inputs at Vcc -0.2V or Vss +0.2V)	ICC4	20	20	20	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = VIH)	ICC5	820	720	620	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	ICC6	820	720	620	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	CI1		100	pF	17
Input Capacitance: $\overline{WE}$	CI2		140	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	CI3		35	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	CI4		42	pF	17
Input/Output Capacitance: DQ1-DQ36	CIO		14	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

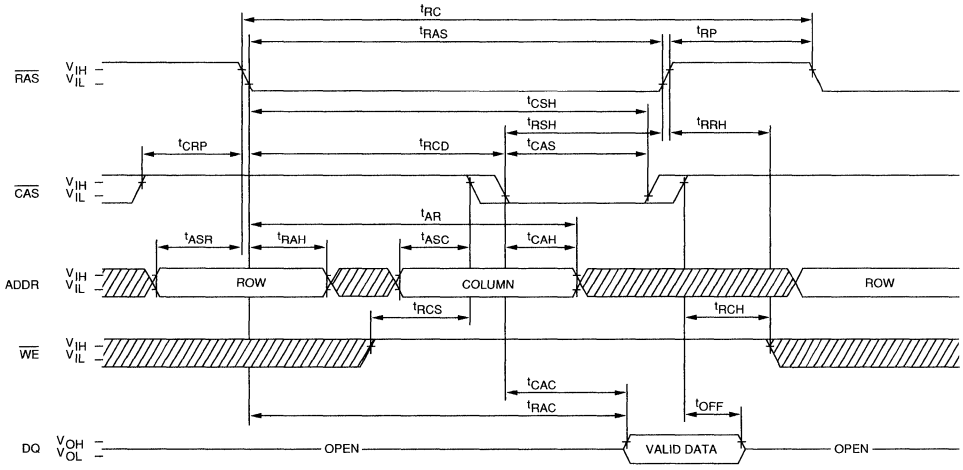
(Notes: 3, 4, 5, 10, 11, 16, 17) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10 %)

A.C. CHARACTERISTICS		-7		-8, -85		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	135		150		180		ns	6, 7
FAST PAGE MODE cycle time	tPC	40		45		55		ns	6, 7
Access time from $\overline{RAS}$	tRAC		70		80		100	ns	7, 8
Access time from $\overline{CAS}$	tCAC		20		20		25	ns	7, 9
$\overline{RAS}$ pulse width	tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	tCPN	10		10		15		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	50	20	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	tCRP	5		5		5		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		15		ns	
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	55		60		70		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	14
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	55		60		75		ns	
Write command pulse width	tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	tCWL	20		20		25		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	15		15		20		ns	15
Data-in hold time referenced to $\overline{RAS}$	tDHR	55		60		75		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	16
Refresh period (256 cycles)	tREF		8		8		8	ms	20
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCHR	15		15		15		ns	19
$\overline{CAS}$ setup time $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCSR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	19

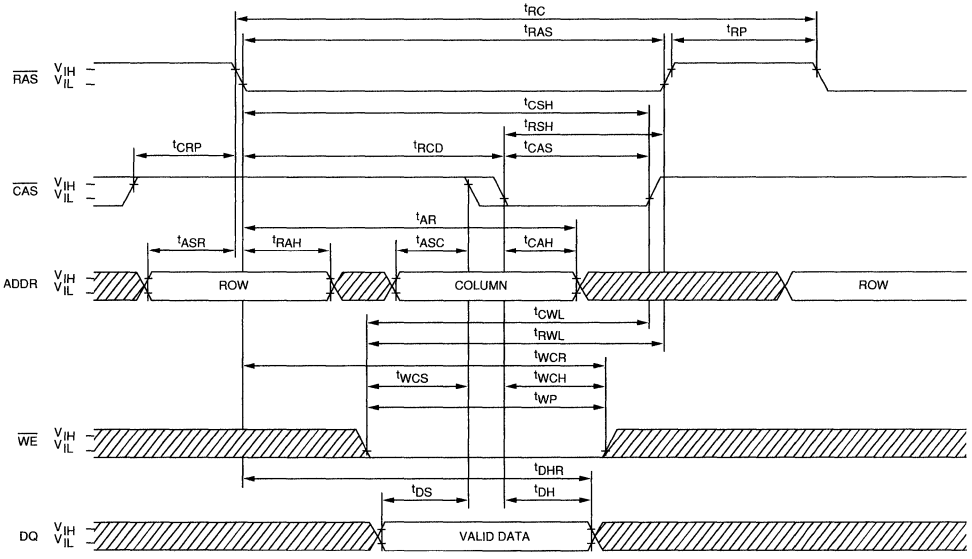
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U18.
22. The module shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

READ CYCLE



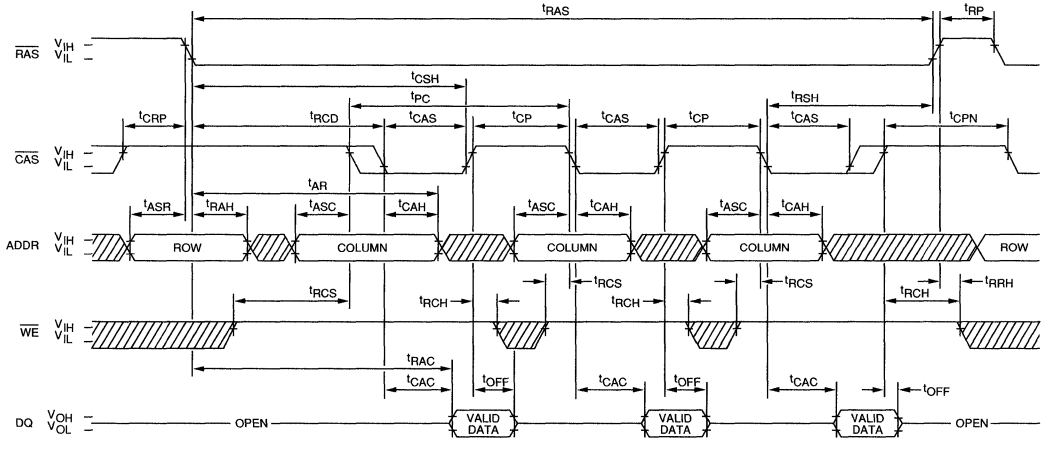
EARLY-WRITE CYCLE



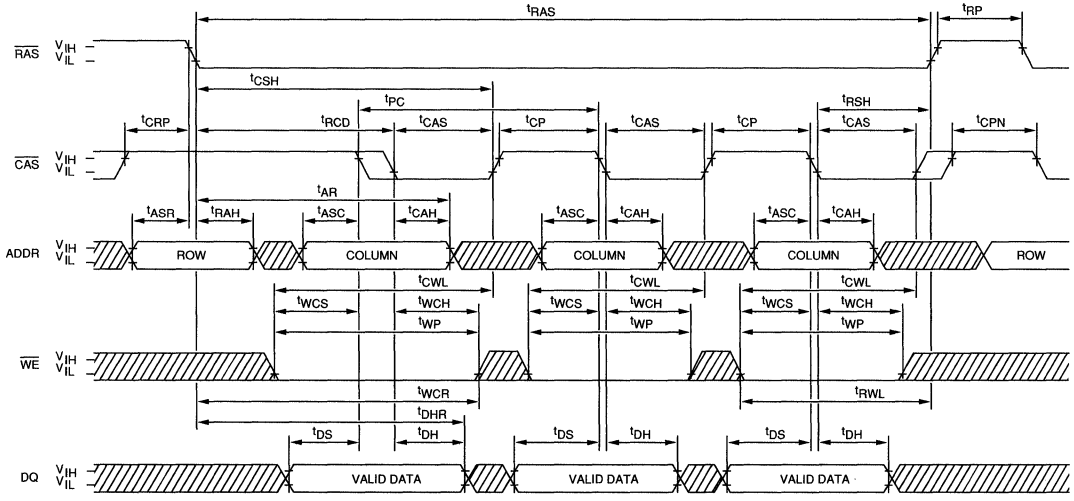
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

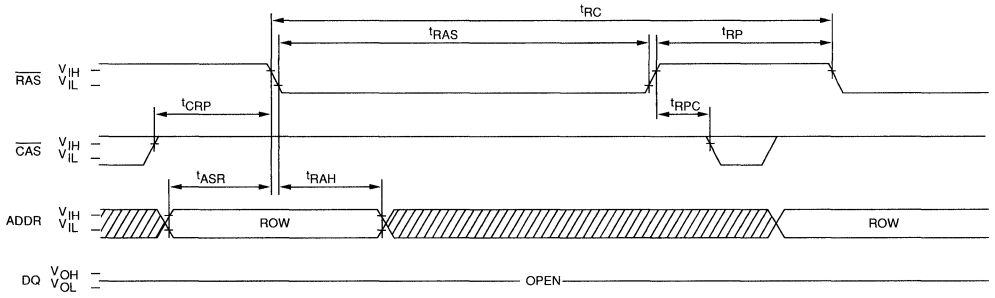


DON'T CARE

UNDEFINED

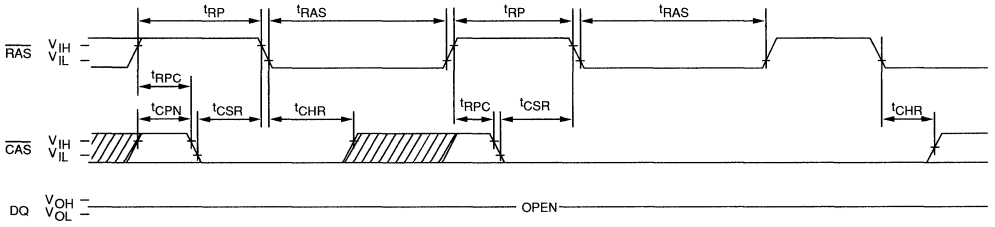
$\overline{RAS}$-ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE)



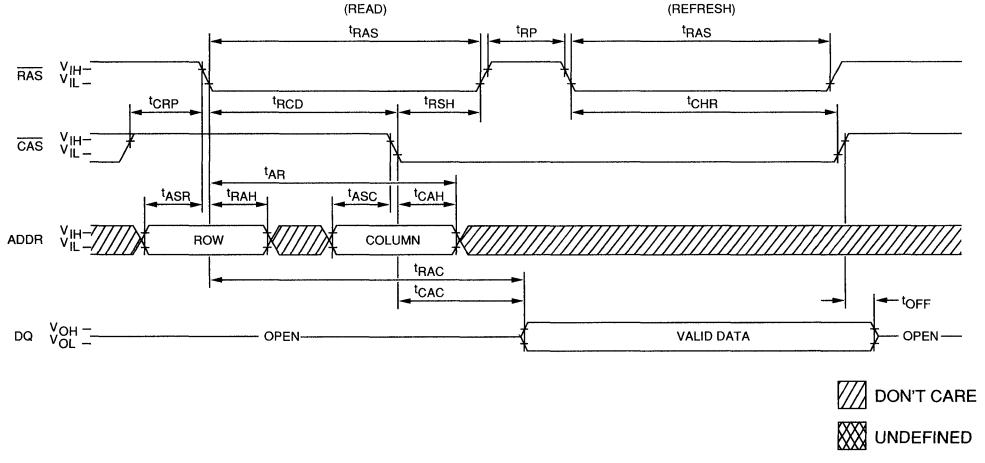
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH) [20]



DRAM MODULE

1 MEG x 36 DRAM

FAST PAGE MODE

FEATURES

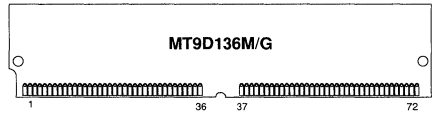
- Common $\overline{RAS}$ control pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon gate process.
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 27mW standby; 2,175mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

- Timing
  - 70ns access - 7
  - 80ns access - 8
  - 100ns access -10
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
  - Leaded 72-pin ZIP Z

PIN ASSIGNMENT (Top View)

72-Pin SIMM (I-7)



72-Pin ZIP (J-6)

PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS0}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

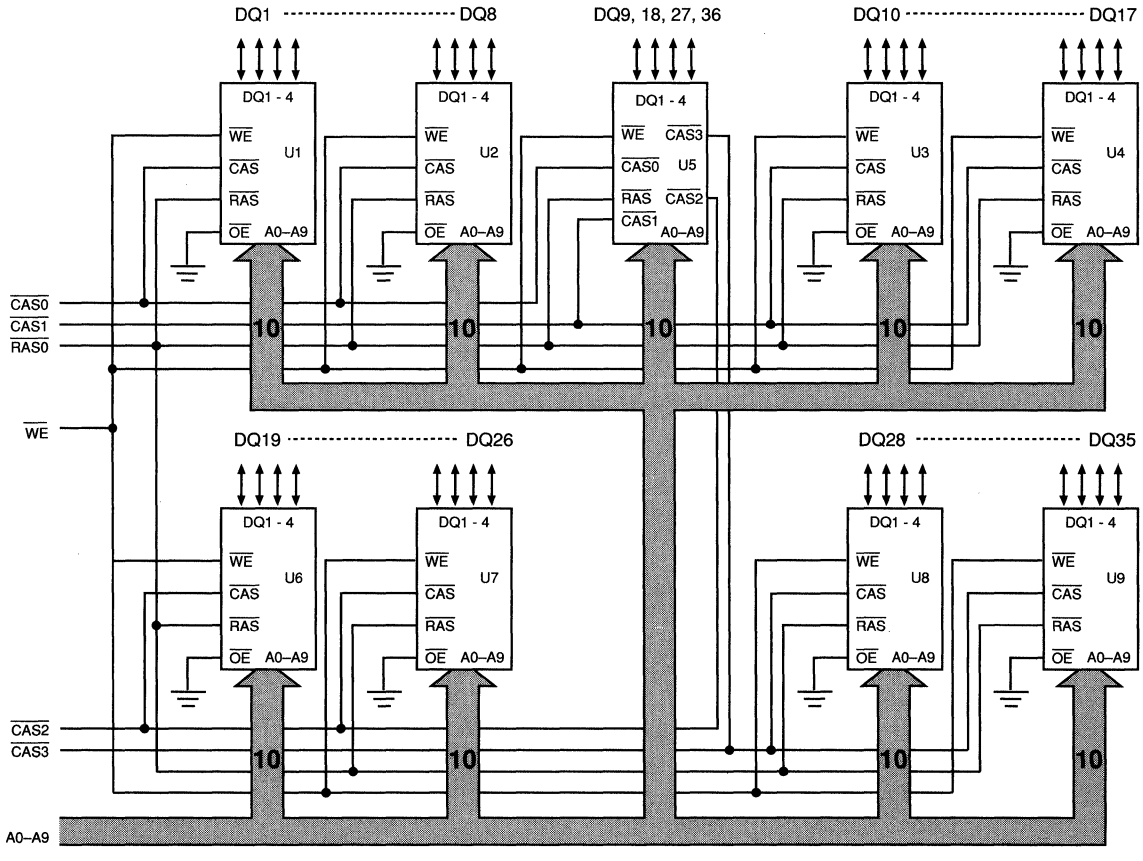
GENERAL DESCRIPTION

The MT9D136 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U4, U6-U9 = MT4C4001DJ
U5 = MT4C4004DJ

NOTE: Due to the use of a Quad $\overline{CAS}$ DRAM, $\overline{RAS0}$ is common to all devices.

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses		DQ1-36
					^tR	^tC	
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-	1st Cycle	L	H→L	H	ROW	COL	Valid Data Out
MODE READ	2nd Cycle	L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-	1st Cycle	L	H→L	L	ROW	COL	Valid Data In
MODE WRITE	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN	READ	L→H→L	L	H	ROW	COL	Valid Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	High Impedance

PRESENCE DETECT

SYMBOL	-7	-8	-10
PRD1	NC	VSS	NC
PRD2	VSS	VSS	NC
PRD3	VSS	NC	NC
PRD4	NC	VSS	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V) For each package input	A0-A8, $\overline{WE}$	I_I	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ Vcc) For each package input	DQ1-DQ36	I_{OZ}	-12	12	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	1
Output Low Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	900	810	720	mA	2
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	630	540	450	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles (MIN))	I_{CC3}	18	18	18	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V after 8 $\overline{RAS}$ cycles (MIN)). (All other inputs at Vcc -0.2V or Vss +0.2V)	I_{CC4}	9	9	9	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}	900	810	720	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	900	810	720	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		45	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		63	pF	17
Input Capacitance: $\overline{RAS0}$	C_{I3}		63	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		21	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		7	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

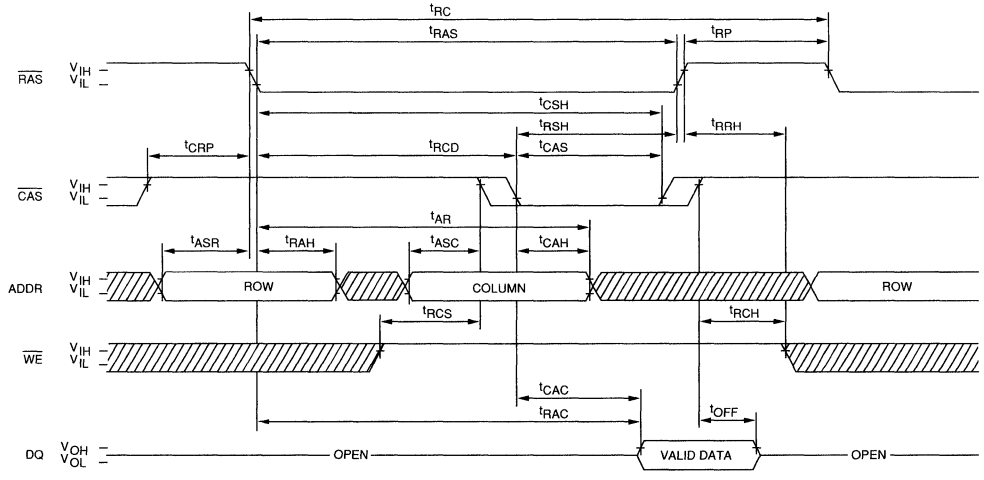
(Notes: 3, 4, 5, 10, 11, 16, 17) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	130		150		180		ns	6, 7
FAST-PAGE-MODE cycle time	tPC	40		45		55		ns	6, 7
Access time from $\overline{RAS}$	tRAC		70		80		100	ns	7, 8
Access time from $\overline{CAS}$	tCAC		20		20		25	ns	7, 9
$\overline{RAS}$ pulse width	tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	tCPN	10		10		15		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	50	20	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	tCRP	5		5		20		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		15		ns	
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	55		60		70		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	14
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	55		60		75		ns	
Write command pulse width	tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	tCWL	20		20		25		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	15		15		20		ns	15
Data-in hold time referenced to $\overline{RAS}$	tDHR	55		60		75		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	16
Refresh period (256 cycles)	tREF		16		16		16	ms	20
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCHR	15		15		15		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCSR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	19

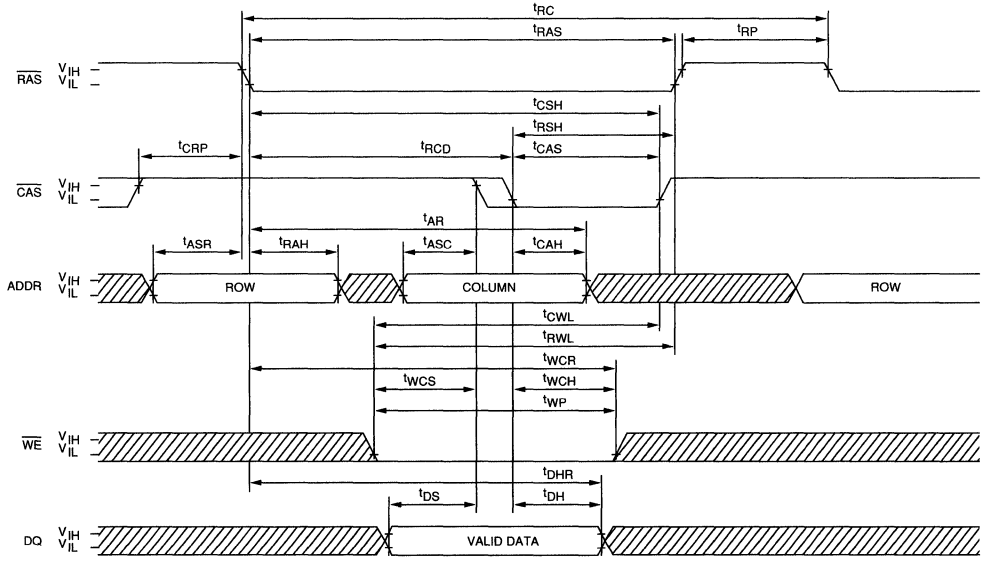
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
10. If $\overline{CAS} = V_{IH}$, data output is high impedance.
11. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\,^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U9.

READ CYCLE



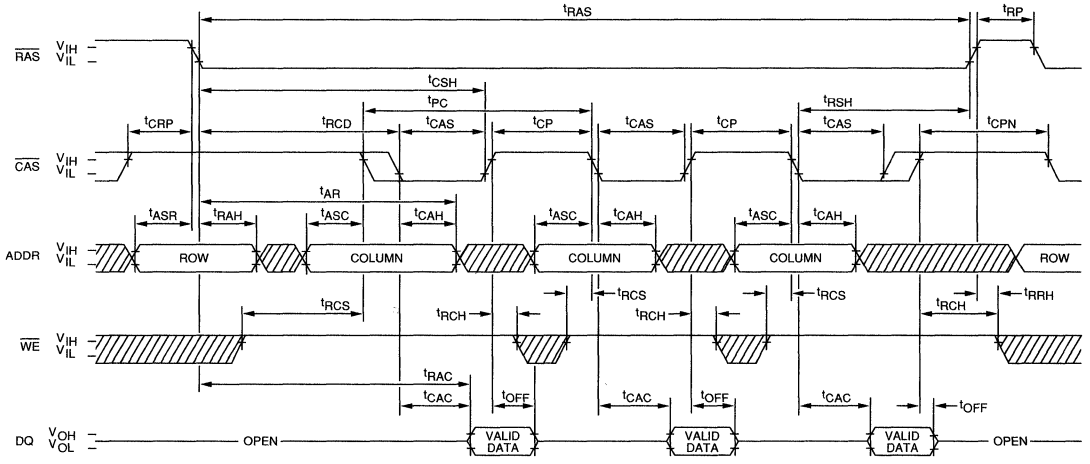
EARLY-WRITE CYCLE



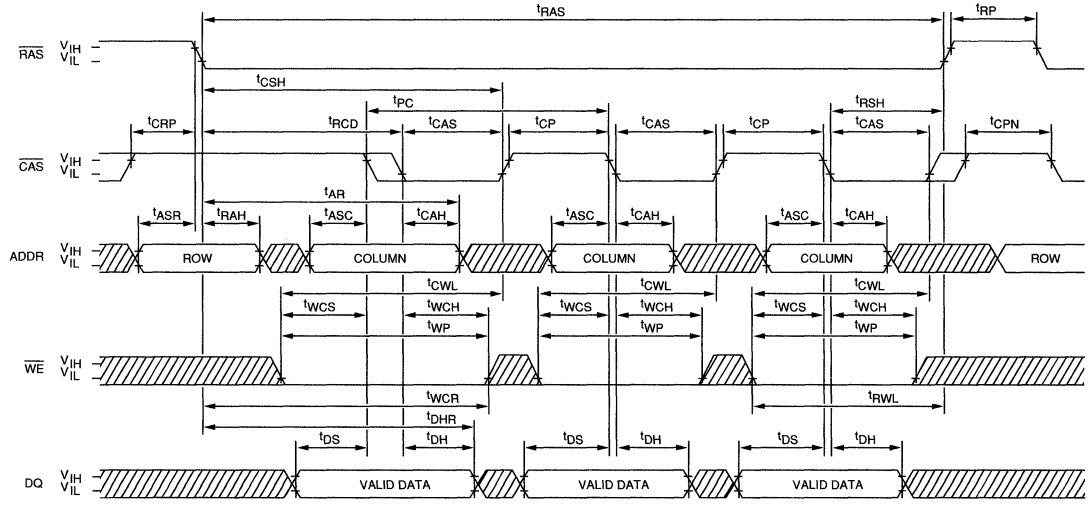
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



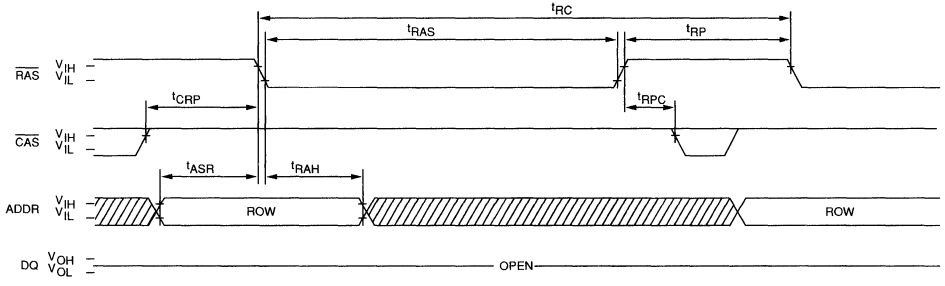
FAST-PAGE-MODE EARLY-WRITE CYCLE



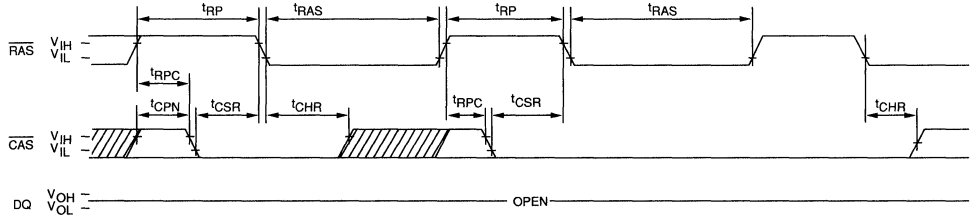
DON'T CARE

UNDEFINED

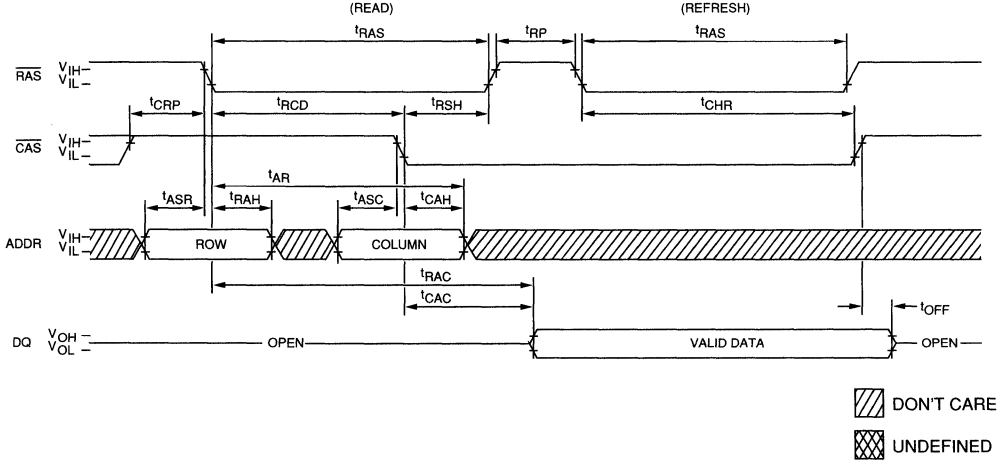
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A_0 - A_9; $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A_0 - A_9, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH) [20]



DRAM MODULE

2 MEG x 36 DRAM

FAST PAGE MODE

FEATURES

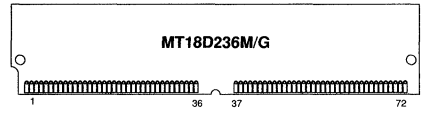
- Common $\overline{RAS}$ control per side pinout in a 72-pin single-in-line package
- High-performance CMOS silicon gate process.
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 54mW standby; 4,500mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

- Timing
  - 70ns access - 7
  - 80ns access - 8
  - 100ns access -10
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
  - Leaded 72-pin ZIP Z

PIN ASSIGNMENT (Top View)

72-Pin SIMM (I-8)



72-Pin ZIP (J-7)

PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	$\overline{RAS1}$	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	$\overline{RAS1}$	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS0}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

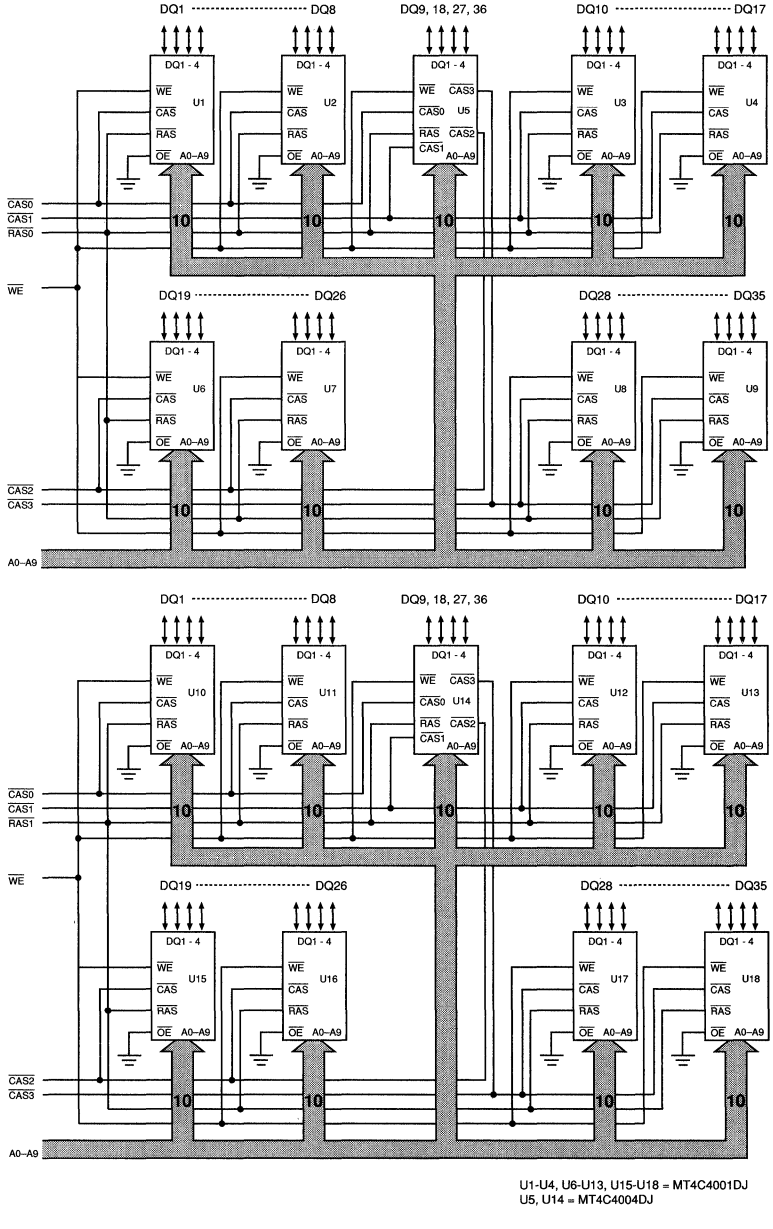
GENERAL DESCRIPTION

The MT18D236 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U4, U6-U13, U15-U18 = MT4C4001DJ
U5, U14 = MT4C4004DJ

NOTE: Due to the use of a Quad $\overline{\text{CAS}}$ parity DRAM, $\overline{\text{RAS0}}$ is common to side 1 and $\overline{\text{RAS1}}$ is common to side 2.

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	DQ1-36
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-	1st Cycle	L	H→L	H	ROW	COL	Valid Data Out
MODE READ	2nd Cycle	L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-	1st Cycle	L	H→L	L	ROW	COL	Valid Data In
MODE WRITE	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN	READ	L→H→L	L	H	ROW	COL	Valid Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

PRESENCE DETECT

SYMBOL	-7	-8	-10
PRD1	NC	VSS	NC
PRD2	NC	VSS	NC
PRD3	VSS	VSS	NC
PRD4	NC	NC	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 18W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input: 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V) For each package input	A0-A9, $\overline{WE}$	II	-36	36	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ Vcc) For each package input	DQ1-DQ36	IOZ	-24	24	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	1
Output Low Voltage (IOUT = 5mA)		VOL		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: tRC = tRC (MIN))	ICC1	918	828	738	mA	2
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = VIL, $\overline{CAS}$ = Cycling: tPC = tPC (MIN))	ICC2	648	558	468	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = VIH after 8 $\overline{RAS}$ cycles (MIN))	ICC3	36	36	36	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V after 8 $\overline{RAS}$ cycles (MIN)). (All other inputs at Vcc -0.2V or Vss +0.2V)	ICC4	18	18	18	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = VIH)	ICC5	918	828	738	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	ICC6	918	828	738	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	CI1		90	pF	17
Input Capacitance: $\overline{WE}$	CI2		126	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$	CI3		63	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	CI4		42	pF	17
Input/Output Capacitance: DQ1-DQ36	CIO		14	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

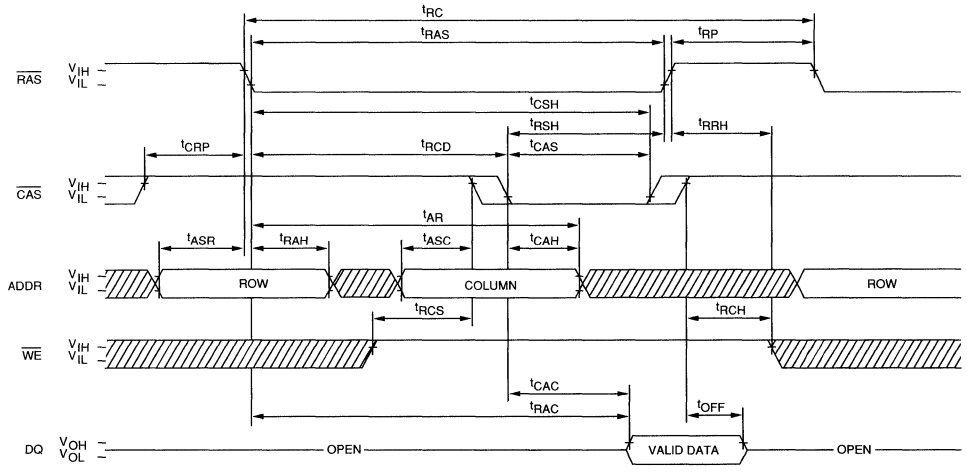
(Notes: 3, 4, 5, 10, 11, 16, 17) ($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	130		150		180		ns	6, 7
FAST-PAGE-MODE cycle time	tPC	40		45		55		ns	6, 7
Access time from $\overline{RAS}$	tRAC		70		80		100	ns	7, 8
Access time from $\overline{CAS}$	tCAC		20		20		25	ns	7, 9
$\overline{RAS}$ pulse width	tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	tCPN	10		10		15		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	50	20	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	tCRP	5		5		20		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		15		ns	
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	55		60		70		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	14
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	55		60		75		ns	
Write command pulse width	tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		25		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		25		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	15		15		20		ns	15
Data-in hold time referenced to $\overline{RAS}$	tDHR	55		60		75		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	16
Refresh period (256 cycles)	tREF		16		16		16	ms	20
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCHR	15		15		15		ns	19
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCSR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	19

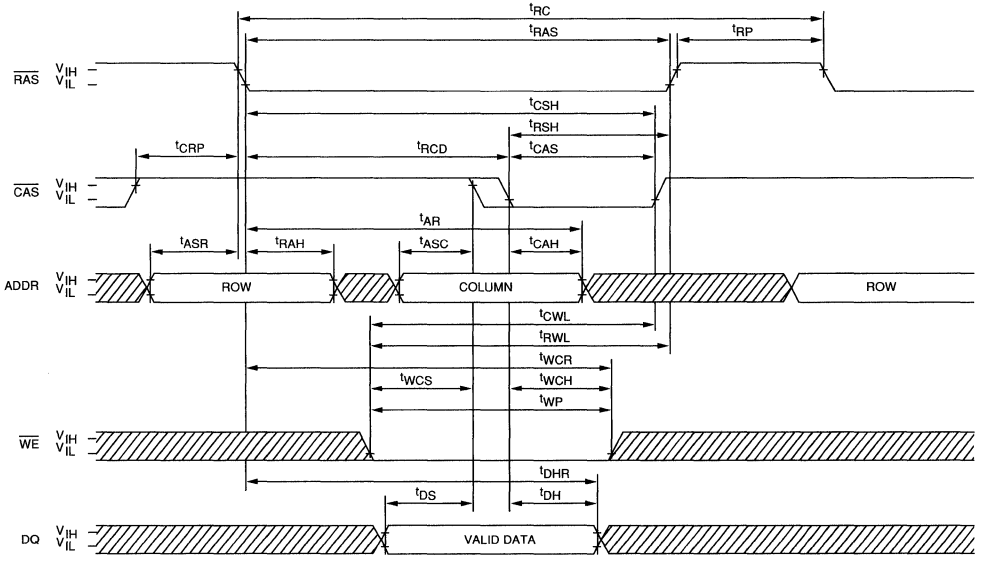
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I\,^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U18.

READ CYCLE



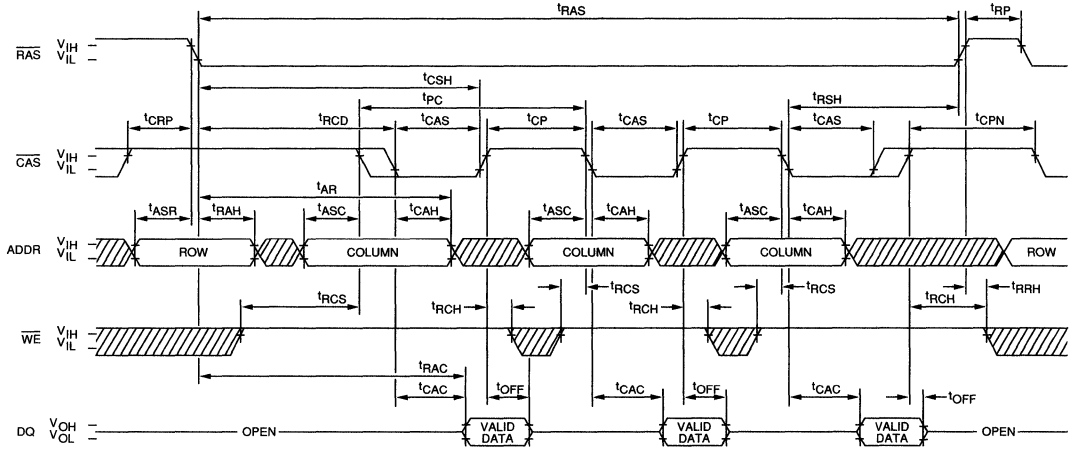
EARLY-WRITE CYCLE



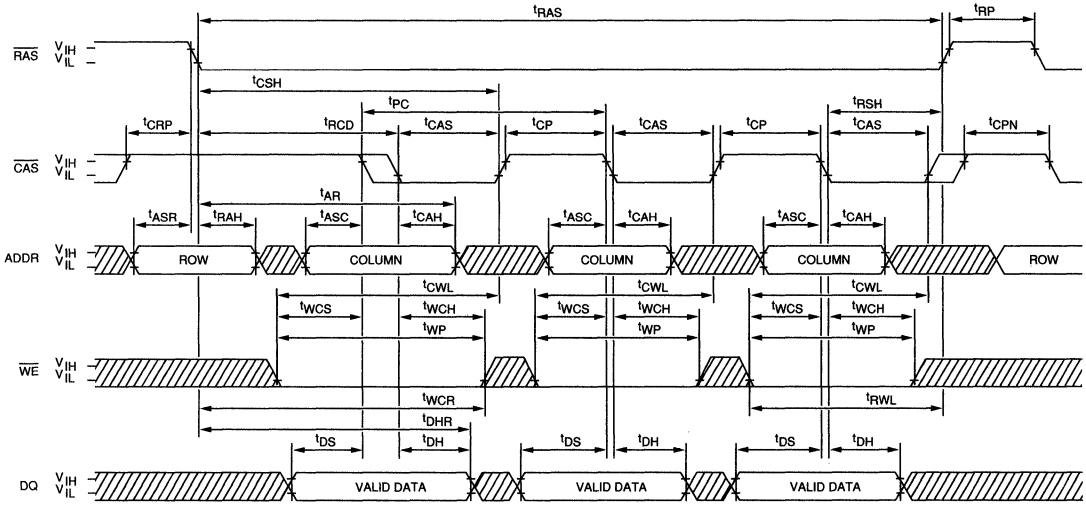
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



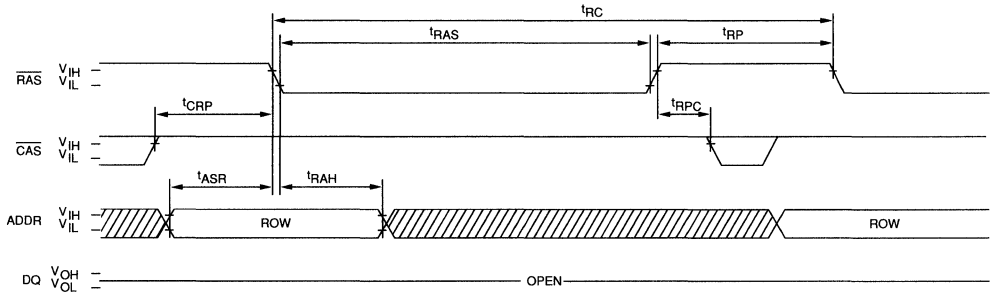
FAST-PAGE-MODE EARLY-WRITE CYCLE



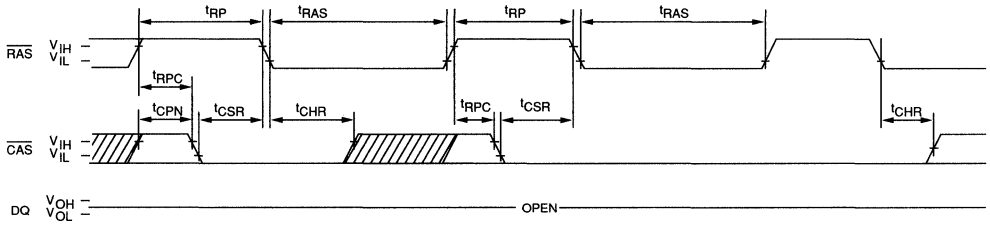
DON'T CARE

UNDEFINED

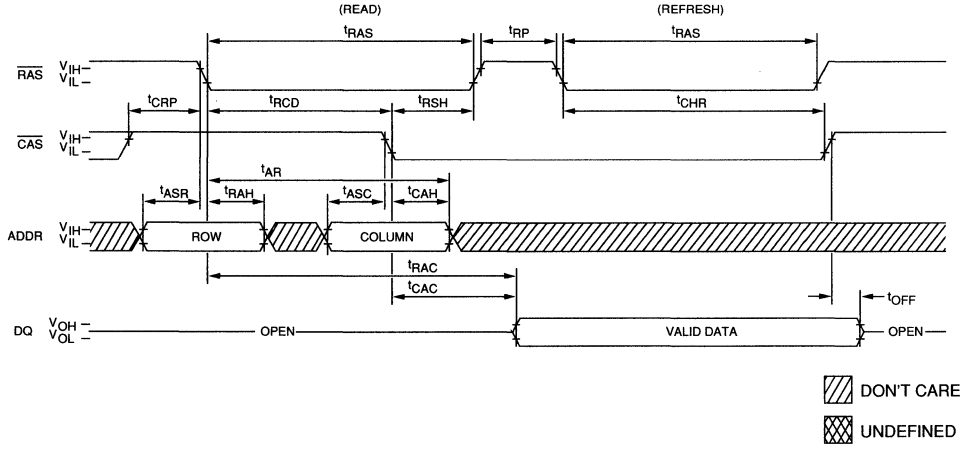
$\overline{RAS}$-ONLY REFRESH CYCLE
($ADDR = A_0 - A_9$; $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
($A_0 - A_9$, $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH) [20]



MICRON TECHNOLOGY, INC.

DUAL PORT DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package and Number of Pins				Process	Page
				Standby	Active	PDIP	ZIP	SOJ	CDIP		
64K x 4	PM	MT42C4064	100,120,150	15mW	250mW	24	24	-	24	CMOS	3-1
256K x 4	FPM	MT42C4255	80,100,120	15mW	200mW	-	28	28	-	CMOS	3-27
256K x 4	FPM, BW	MT42C4256	80,100,120	15mW	200mW	-	28	28	-	CMOS	3-61
128K x 8	FPM	MT42C8127	100,120	15mW	200mW	-	-	40	-	CMOS	3-97
128K x 8	FPM, BW	MT42C8128	80,100,120	15mW	275mW	-	40	40	-	CMOS	3-131
256K x 8	FPM, BW	MT42C8256	70, 80,100	20mW	300mW	-	-	40	-	CMOS	3-167

PM = Page Mode, FPM = Fast Page Mode, BW = Block Write

TRIPLE PORT DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package and Number of Pins			Process	Page
				Standby	Active	ZIP	SOJ	PLCC		
256K x 4	FPM, BW, QSF pin	MT43C4257	80,100,120	15mW	450mW	-	40	-	CMOS	3-169
256K x 4	FPM, BW, SSF pin	MT43C4258	80,100,120	15mW	450mW	-	40	-	CMOS	3-169
128K x 8	FPM, BW, QSF pin	MT43C8128	80,100,120	15mW	450mW	-	-	52	CMOS	3-215
128K x 8	FPM, BW, SSF pin	MT43C8129	80,100,120	15mW	450mW	-	-	52	CMOS	3-215

PM = Page Mode, FPM = Fast Page Mode, BW = Block Write

VRAM

64K x 4 DRAM WITH 256 x 4 SAM

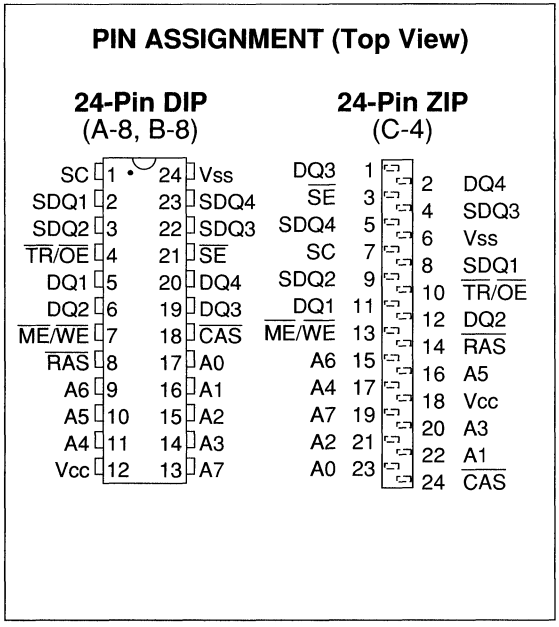
FEATURES

- Industry standard pinout, timing and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256-cycle refresh within 4ms
- Optional PAGE MODE access cycles
- Dual port organization: 64K x 4 DRAM port
  256 x 4 SAM port
- Bit MASKED WRITE mode capability on DRAM port
- No refresh required for Serial Access Memory
- Low power: 15mW standby; 250mW active, typical
- Fast access times – 100ns parallel, 33ns serial

OPTIONS

	MARKING
• Timing (DRAM, SAM)	
100ns, 33ns	-10
120ns, 40ns	-12
150ns, 60ns	-15
• Packages	
Plastic DIP (400 mil)	None
Ceramic DIP (400 mil)	C
Plastic ZIP	Z

PIN ASSIGNMENT (Top View)



GENERAL DESCRIPTION

The MT42C4064 is a high speed, dual port CMOS dynamic random access memory, or video RAM (VRAM) containing 262,144 bits. They may be accessed by a four bit wide DRAM port or by a 256 x 4 bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4067 (64K x 4) bit DRAM. Four 256-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 4-bit random access I/O port, the four internal 256 bit wide paths between the DRAM and the SAM, and the 4-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address-decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

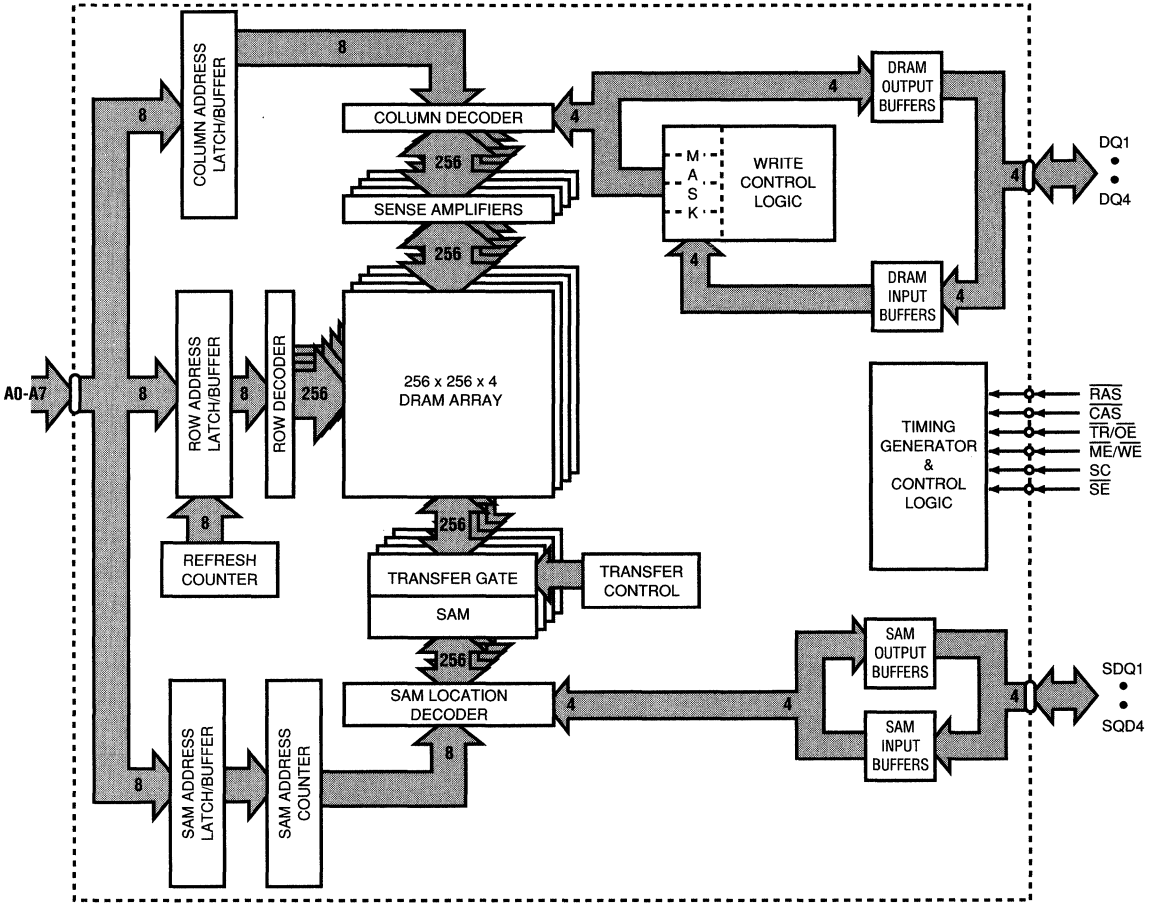


Figure 1
MT42C4064 BLOCK DIAGRAM

PIN DESCRIPTIONS

DIP PIN NUMBER(S)	ZIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
1	7	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
4	8, 9, 4, 5	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW); otherwise, the output buffers are in a High-Z.
7	13	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASKED WRITE cycle is performed, or Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = H) or WRITE ($\overline{WE}$ = L) cycle when accessing the DRAM. This includes a DRAM-TO-SAM TRANSFER ($\overline{WE}$ = H) or SAM- TO-DRAM TRANSFER ($\overline{WE}$ = L).
8	14	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 8 row-address bits and as a strobe for the MASK ENABLE and TRANSFER functions.
9, 10, 11, 13, 14, 15, 16, 17	23, 22, 21, 20 17, 16, 15, 19	A0 to A7	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select 4 bits out of the 64K available. During TRANSFER operations, A0 to A7 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW).
18	24	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 8 column-address bits and enable the DRAM output buffers ($\overline{TR/OE}$ must also be LOW).
21	3	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state.$\overline{SE}$ is also used during a TRANSFER operation to indicate whether a SAM-TO-DRAM TRANSFER or a SERIAL-INPUT-MODE ENABLE cycle is performed.
5, 6, 19, 20	11,12,1,2	DQ1 - DQ4	Input/ Output	DRAM Data I/O: Inputs, Outputs, or High-Z, and/or Mask Data Inputs: For MASKED WRITE cycle only.
2, 3, 22, 23	8,9,4,5	SDQ1 - SDQ4	Input/ Output	Serial Data I/O: Input, Output, or High-Z.
12	18	Vcc	Supply	Power Supply: +5V ±10%
24	6	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The VRAM can be divided into three functional blocks (see Figure 1); the DRAM, the transfer control circuitry, and the serial access memory (SAM). All of the operations described below are also shown in the AC Timing Diagrams section of this data sheet, and are summarized in the Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

DRAM OPERATION

The DRAM portion of the VRAM is functionally identical to standard 64K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion.

READ/WRITE Cycles

The 16 address bits that are used to select a 4-bit word from the 65,536 available are latched into the chip using the A0 -A7, $\overline{RAS}$, and $\overline{CAS}$ inputs. First, the 8 row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 8 column-address bits are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH to LOW.

For single port DRAMs the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $(\overline{TR})/\overline{OE}$ is used, when $\overline{RAS}$ goes LOW, to select between an internal transfer operation and a DRAM operation. $(\overline{TR})/\overline{OE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition for a DRAM port READ or WRITE operation.

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1 - DQ4 port. The $(\overline{TR})/\overline{OE}$ input must be LOW to enable the DRAM output port.

For single port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $(\overline{ME})/\overline{WE}$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $(\overline{ME})/\overline{WE}$ is LOW at the $\overline{RAS}$ HIGH to LOW transition, a MASKED WRITE operation is selected. For a normal DRAM WRITE operation, $(\overline{ME})/\overline{WE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition. $(\overline{ME})/\overline{WE}$ is a "don't care" at the $\overline{RAS}$ HIGH to LOW transition for a DRAM READ cycle.

If $(\overline{ME})/\overline{WE}$ is LOW when $\overline{CAS}$ goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1 - DQ4 port will be written into the selected memory cells. If $\overline{ME}/(\overline{WE})$ is LOW when $\overline{RAS}$ goes LOW, the input data will be "masked" before being stored in the DRAM.

The VRAM can perform all the normal DRAM cycles including EARLY-WRITE, LATE-WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE-MODE READ, PAGE-MODE WRITE, and PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in this data sheet for more details on these operations.

REFRESH

The MT42C4064 supports $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN types of refresh cycles. All 256 row-address combinations must be accessed within 4ms. For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh mode, the row addresses are generated internally and the user need not supply them as he must in $\overline{RAS}$ ONLY refresh. $\overline{TR}/(\overline{OE})$ must be HIGH when $\overline{RAS}$ goes LOW for the $\overline{RAS}$ ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ types of refresh cycles. Any READ, WRITE, or TRANSFER operation also refreshes the DRAM row that is being accessed.

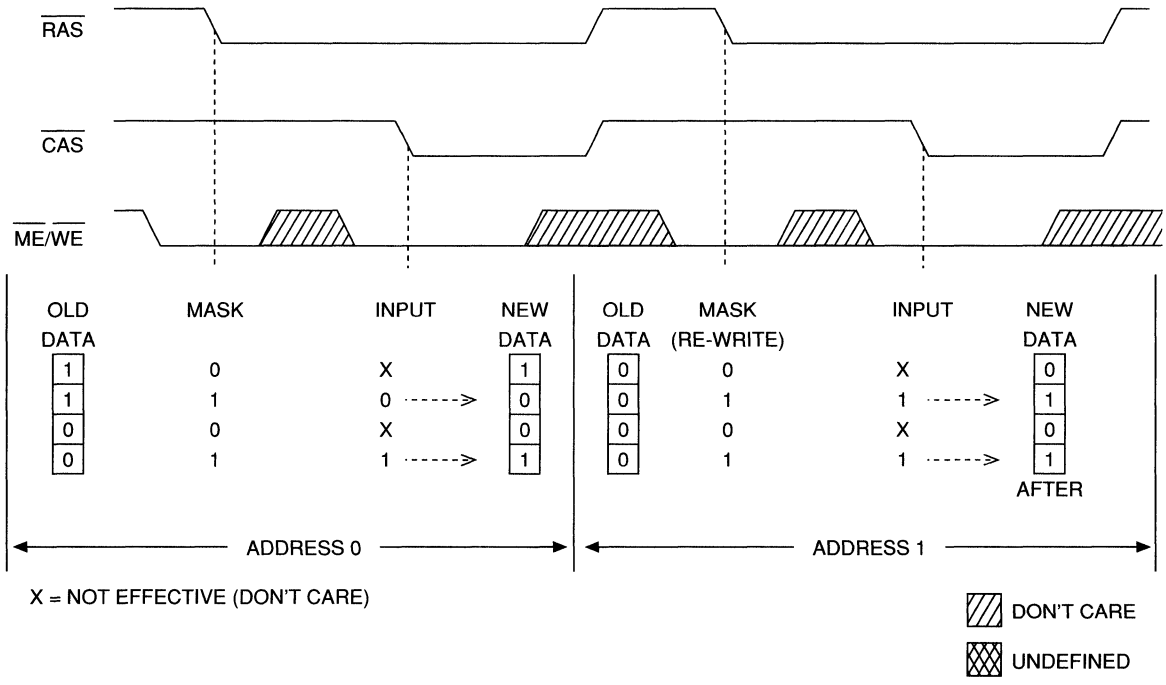


Figure 2
MT42C4064 MASKED WRITE

MASKED WRITE

If $\overline{ME}$/($\overline{WE}$) is LOW at the $\overline{RAS}$ HIGH to LOW transition, the data (mask data) present on the DQ1 - DQ4 inputs will be written into the bit mask data register. The mask data acts as an individual write enable for each of the four DQ1 - DQ4 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1 - DQ4 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. Since the mask data register is reset (to all 1's) at the end of every MASKED WRITE cycle, new mask data must be supplied at the beginning of each MASKED WRITE cycle. An example of a typical MASKED WRITE cycle is shown in Figure 2.

TRANSFER OPERATION

DRAM-TO-SAM TRANSFER (READ TRANSFER)

A TRANSFER operation is initiated when $\overline{TR}/(\overline{OE})$ is LOW at $\overline{RAS}$ (HIGH to LOW) time. $(\overline{ME})/\overline{WE}$ indicates the direction of the transfer and must be HIGH as $\overline{RAS}$ goes LOW for a DRAM-TO-SAM TRANSFER. In this case, the row address bits indicate the four 256-bit DRAM rows that are to be transferred to the four SAM data registers, and the column address bits indicate the start address, or Tap, of the next SERIAL OUTPUT cycle from the SAM data registers. $\overline{RAS}$ and $\overline{CAS}$ are used to strobe the address bits into the part. To complete the TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are still LOW. The 1024 bits of DRAM data are then written into the SAM data registers and the serial shift start address is stored in an internal 8-bit register. There must be no rising edges on the serial clock (SC) input while a normal READ TRANSFER is taking place (refer to the AC timing diagrams for READ TRANSFER). A REAL-TIME READ-TRANSFER cycle is the only time when SC must be synchronized with the DRAM $\overline{RAS}$ and $\overline{CAS}$ timing (by using $\overline{TR}/(\overline{OE})$ is to fire the TRANSFER, LOW to HIGH transition). See the REAL-TIME READ-TRANSFER AC timing waveforms. If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation.

SAM-TO-DRAM TRANSFER (WRITE TRANSFER)

The SAM-TO-DRAM TRANSFER operation is identical to the DRAM-TO-SAM TRANSFER described above except that $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row that the SAM data registers will be written to and the column address indicates the Tap address of the next SERIAL INPUT cycle for the SAM data registers. If $\overline{SE}$ is HIGH when $\overline{RAS}$ goes LOW, a SERIAL-INPUT-MODE ENABLE cycle is performed.

SAM OPERATION

SERIAL INPUT/OUTPUT MODE CONTROL

The SAM port is automatically placed in the serial output mode after a DRAM-TO-SAM TRANSFER operation. Conversely, after a SAM-TO-DRAM TRANSFER, the SAM port will be in the serial input mode.

SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER)

It is possible to change the direction of the SAM port from output to input without performing a SAM-TO-DRAM TRANSFER. This operation, called a SERIAL-INPUT-MODE ENABLE cycle, is simply a SAM-TO-DRAM TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the data registers will be ready to accept input data.

The only way to put the SAM port in the serial output mode is to do a DRAM-TO-SAM TRANSFER.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM data register contents will start at the tap start address that was loaded during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 4-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW to HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW, and will wrap around to location 0 after reaching its maximum count of 255.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the serial address register contents, which was loaded when the serial input mode were enabled, will determine the serial address to which the first bit will be written. $\overline{SE}$ acts as an enable for serial data input and must be LOW for normal serial input. If $\overline{SE}$ is HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address register is incremented with every L → H transition of SC, regardless of the logic level on the $\overline{SE}$ input.

TRUTH TABLE

DRAM Operations (SC, $\overline{SE}$, and SDQ1 — SDQ4 are "don't care")

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$		$\overline{TR}/\overline{OE}$		Addresses		DQ1 to DQ4	Notes
			tR*	tC*	tR*	tC*	tR*	tC*		
Standby	H	H	X	X	X	X	X	X	High-Z	
READ	L	L	X	H	H	H→L	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	H	L	H	X	ROW	COL	Data In	1
MASKED WRITE	H→L	L	L	L	H	X	ROW	COL	Mask Data In, Valid Data In	
READ-WRITE	L	L	H	H→L	H	L→H	ROW	COL	Valid Data Out	1
PAGE-MODE READ	L	H→L→H, H→L→H	H	H	H	H→L	ROW	COL	Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	H	L	H	X	ROW	COL	Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H, H→L→H	H	H→L	H	L→H	ROW	COL	Valid Data Out, Valid Data In	1
$\overline{RAS}$-ONLY REFRESH	L	H	X	n/a	H	n/a	ROW	n/a	High-Z	
HIDDEN REFRESH	L→H→L	L	X	H	X	L	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	X	X	X	X	X	X	High-Z	

TRANSFER Operations (DQ1 — DQ4 are "don't care")

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$		$\overline{TR}/\overline{OE}$		Addresses		SC	$\overline{SE}$	SDQ1 to SDQ4	Notes
			tR*	tC*	tR*	tC*	tR*	tC*				
DRAM-TO-SAM TRANSFER	L	L	H	X	L	L	ROW	TAP**	X	X	X	2
SAM-TO-DRAM TRANSFER	L	L	L	X	L	X	ROW	TAP**	X	L	X	3
SERIAL-INPUT-MODE ENABLE	L	L	L	X	L	X	ROW	TAP**	X	H	X	4

* tR = when $\overline{RAS}$ goes from HIGH to LOW
tC = when $\overline{CAS}$ goes from HIGH to LOW
** TAP = Tap Address, the serial address to which the next serial input or output cycle will start.

Notes: 1. Any type of WRITE cycle may also be a MASKED WRITE cycle.
2. The SAM will be in a SERIAL OUTPUT mode after a DRAM-TO- SAM TRANSFER.
3. The SAM will be in a SERIAL INPUT mode after a SAM-TO-DRAM TRANSFER.
4. The SAM will be put in the SERIAL INPUT mode but the SAM-TO-DRAM TRANSFER will not occur.

TRUTH TABLE

Serial I/O Operations ($\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, and DQ1 - DQ4 are "don't care")

Function	SC	$\overline{SE}$	SDQ1 — SDQ4	Notes
SERIAL OUTPUT	L→H	L	Valid Data Out	5
SERIAL INPUT	L→H	L	Valid Data In	6

Notes: 5. The SAM must be in the SERIAL OUTPUT mode.
6. The SAM must be in the SERIAL INPUT mode.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Operating Temperature, Ta(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input (0V≤VIN≤Vcc), all other pins not under test = 0V).	IL	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V≤VOUT≤Vcc).	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 5mA)	VOL		0.4	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_7	C_{I1}		5	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, SC, $\overline{SE}$	C_{I2}		7	pF	18
Output Capacitance: DQ, SDQ	C_O		7	pF	18

CURRENT DRAIN, SAM IN STANDBY

(Notes 2, 3) ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION OF DRAM	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; $^tRC = {}^tRC$ (MIN)).	I_{CC1}		40	mA	
OPERATING CURRENT: PAGE MODE ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ = Cycling; $^tPC = {}^tPC$ (MIN)).	I_{CC2}		40	mA	
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles MIN).	I_{CC3}		10	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{CC}$-0.2V after 8 $\overline{RAS}$ cycles MIN. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V).	I_{CC4}		4	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS} = V_{IH}$).	I_{CC5}		30	mA	
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling).	I_{CC6}		30	mA	22
SAM/DRAM DATA TRANSFER	I_{CC7}		60	mA	

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(Notes 2, 3) ($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION OF DRAM	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; $^tRC = {}^tRC$ (MIN)).	I_{CC8}		60	mA	
OPERATING CURRENT: PAGE MODE ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ = Cycling; $^tPC = {}^tPC$ (MIN)).	I_{CC9}		60	mA	
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles MIN).	I_{CC10}		30	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{CC}$-0.2V after 8 $\overline{RAS}$ cycles MIN. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V).	I_{CC11}		25	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS} = V_{IH}$).	I_{CC12}		50	mA	
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling).	I_{CC13}		50	mA	22
SAM/DRAM DATA TRANSFER	I_{CC14}		90	mA	

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 6, 10, 11, 17) ($0°C \leq T_A \leq +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	190		220		260		ns	
READ-MODIFY-WRITE cycle time	^tRWC	250		295		345		ns	20, 21
PAGE-MODE READ or WRITE cycle time	^tPC	75		90		110		ns	6
PAGE-MODE READ-MODIFY-WRITE cycle time	^tPRWC	125		150		175		ns	20, 21
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	15		20		25		ns	
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	15		20		25		ns	19
$\overline{RAS}$ to $\overline{CAS}$ delay	^tRCD	15	50	15	60	15	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	15		15		15		ns	
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	20		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		70		80		ns	
READ command setup time	^tRCS	0		0		0		ns	
READ command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
READ command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	16
WRITE command hold time	^tWCH	20		25		30		ns	
WRITE command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	
WRITE command pulse width	^tWP	20		25		30		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		20		25		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	65		80		95		ns	16, 20
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	120		150		185		ns	16, 20
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 6, 10, 11, 17) ($0°C \leq T_A \leq +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Hold Time	^tRWH	10		10		15	ns		
Mask Data (DQ_) to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask Data (DQ_) to $\overline{RAS}$ hold time	^tMH	20		20		25		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	
Refresh period (256 cycles)	^tREF		4		4		4	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC		0		0		0	ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	20		25		30		ns	22
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	25	0	25	0	30	ns	7, 12
Access time from ($\overline{TR}$)/$\overline{OE}$	^tOE		25		25		30	ns	
Output Disable	^tOD	0	25	0	25	0	30	ns	
Output Disable hold time from start of WRITE	^tOEH		25		25		30	ns	
Output Enable to $\overline{RAS}$ delay	^tORD		0		0		0	ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 6, 17) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER command to $\overline{RAS}$ setup time	^tTS	0		0		0		ns	23
TRANSFER command to $\overline{RAS}$ hold time	^tRTH	80		90		100		ns	23
TRANSFER command to $\overline{CAS}$ hold time	^tCTH	30		30		35		ns	23
TRANSFER command to SC lead time	^tTSL	5		5		10		ns	23
TRANSFER command to $\overline{RAS}$ lead time	^tTRL	10		10		10		ns	23
TRANSFER command to $\overline{RAS}$ delay time	^tTRD	15		15		20		ns	23
TRANSFER command to $\overline{CAS}$ time	^tTCL	10		10		10		ns	23
TRANSFER command to $\overline{CAS}$ delay time	^tTCD	15		15		20		ns	23
First SC edge to TRANSFER command delay time	^tTSD	10		10		20		ns	23
$\overline{CAS}$ to first SC delay	^tRSD		95		105		115	ns	
RAS to first SC delay	^tCSD		25		35		45	ns	
SAM-TO-DRAM (WRITE) transfer command to $\overline{RAS}$ hold time	^tRTHW	15		15		15		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	10	40	10	50	10	60	ns	
SC to $\overline{RAS}$ setup time	^tSRS	35		40		45		ns	
$\overline{RAS}$ to SC delay time	^tSRD	25		30		35		ns	
Serial data input to SE delay time	^tSZE	0		0		0		ns	
$\overline{RAS}$ to SD buffer turn-on time	^tSRO	0		0		0		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	50		55		60		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		0		ns	
SERIAL INPUT MODE ENABLE ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		0		ns	
SERIAL INPUT MODE ENABLE ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	15		15		15		ns	
NONTRANSFER command to $\overline{RAS}$ setup time	^tYS	0		0		0		ns	24
NONTRANSFER command to $\overline{RAS}$ hold time	^tYH	15		15		20		ns	24

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

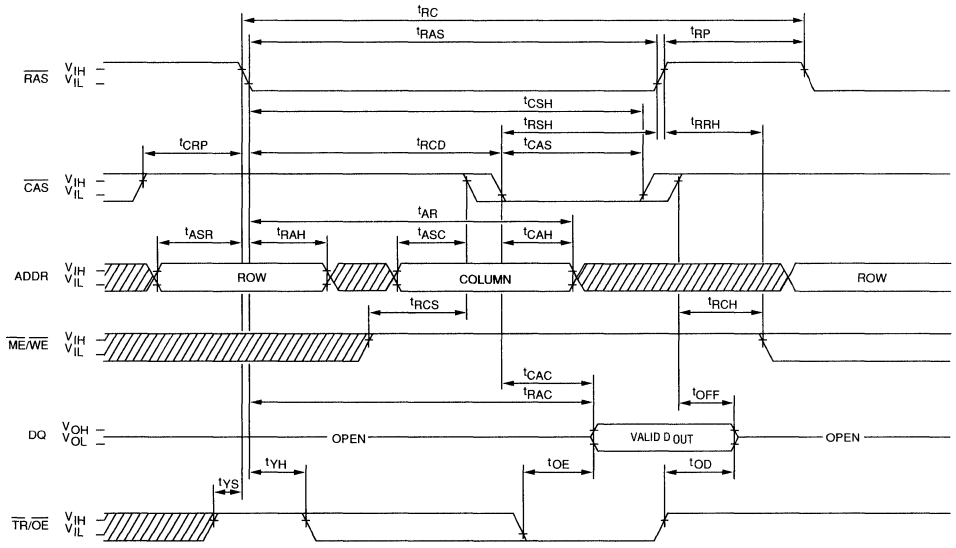
(Notes 3, 4, 5, 17, 25) (0° C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	33	50000	40	50000	60	50000	ns	
Access time from SC	^tSAC		33		40		60	ns	25
SC precharge time	^tSP	10		10		20		ns	
SC pulse width	^tSAS	10		10		20		ns	
Access time from $\overline{SE}$	^tSEA		25		30		40	ns	25
$\overline{SE}$ precharge time	^tSEP	10		15		20		ns	
$\overline{SE}$ pulse width	^tSE	15		15		20		ns	
Serial data out hold time after SC high	^tSOH	10		10		10		ns	25
Serial output buffer turn off delay from $\overline{SE}$	^tSEZ	0	15	0	25	0	30	ns	25
Serial data in setup time	^tSDS	0		0		0		ns	
Serial data in hold time	^tSDH	15		20		25			
SERIAL INPUT (Write) Enable setup time	^tSWS	0		0		0		ns	
SERIAL INPUT (Write) Enable hold time	^tSWH	20		35		45		ns	
SERIAL INPUT (Write) Disable setup time	^tSWIS	0		0		0		ns	
SERIAL INPUT (Write) Disable hold time	^tSWIH	20		35		45		ns	

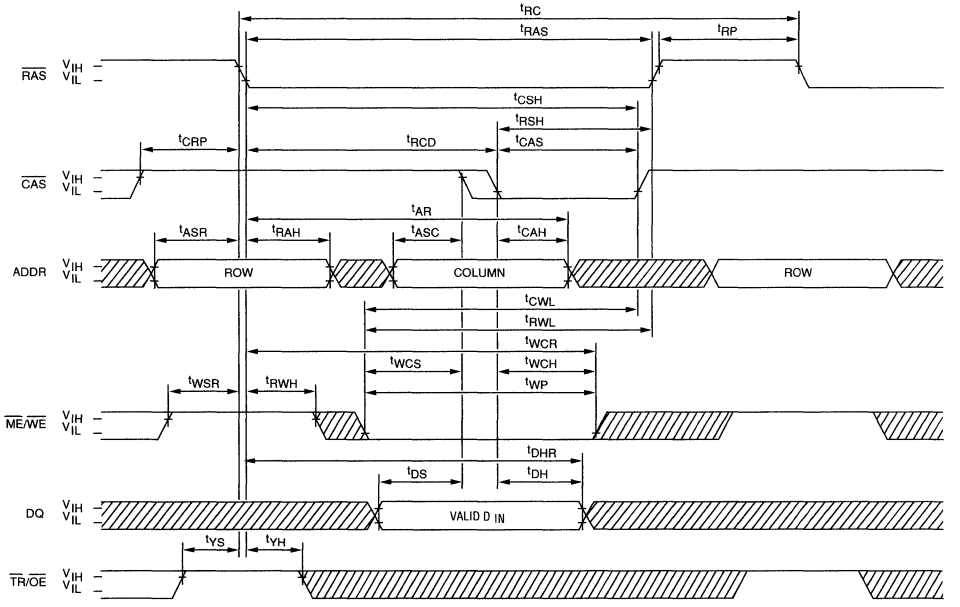
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles and 1 SC cycle, before proper device operation is assured. The $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms static refresh require-ment is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, DRAM data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, DRAM data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and to $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $^tCWD \ge {}^tCWD$ (MIN) and $^tRWD \ge {}^tRWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back toV_{IH}) is indeterminate. If $^tWCS \le {}^tWCS$, the cycle is a LATE WRITE [($\overline{ME}$)/$\overline{WE}$ falls after CAS] ^tWCS, ^tCWD and ^tRWD do not apply.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. Includes the $\overline{OE}$ delay time (30ns for the -10, 40ns for the -12, and 50ns for the -15).
21. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH (V_{IH}) DQ goes open. If $\overline{OE}$ is tied permanently LOW a READ-MODIFY-WRITE operation is not possible.
22. Enables on-chip refresh and address counters.
23. TRANSFER command means that $\overline{TR}$/($\overline{OE}$) is LOW when $\overline{RAS}$ goes LOW.
24. NONTRANSFER command means that $\overline{TR}$/($\overline{OE}$) is HIGH when $\overline{RAS}$ goes LOW.
25. Measured with a load equivalent to 2 TTL gates and 50pF.

DRAM READ CYCLE



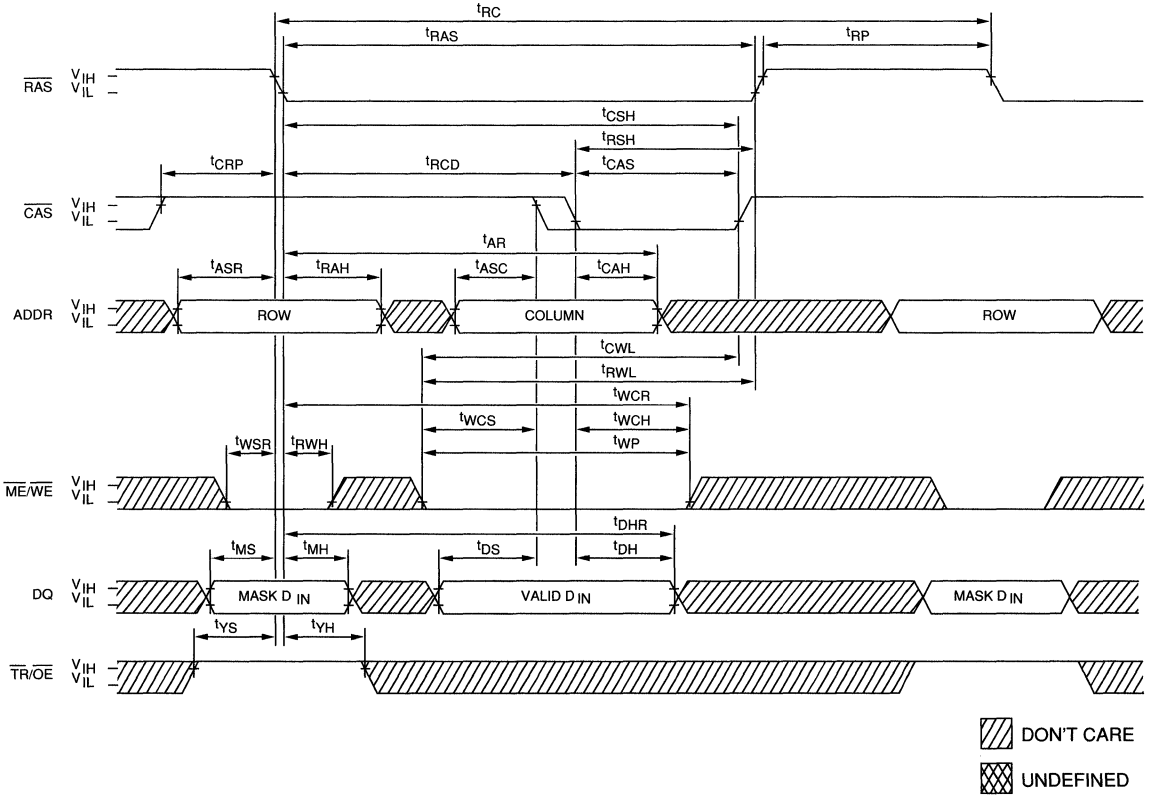
DRAM EARLY-WRITE CYCLE



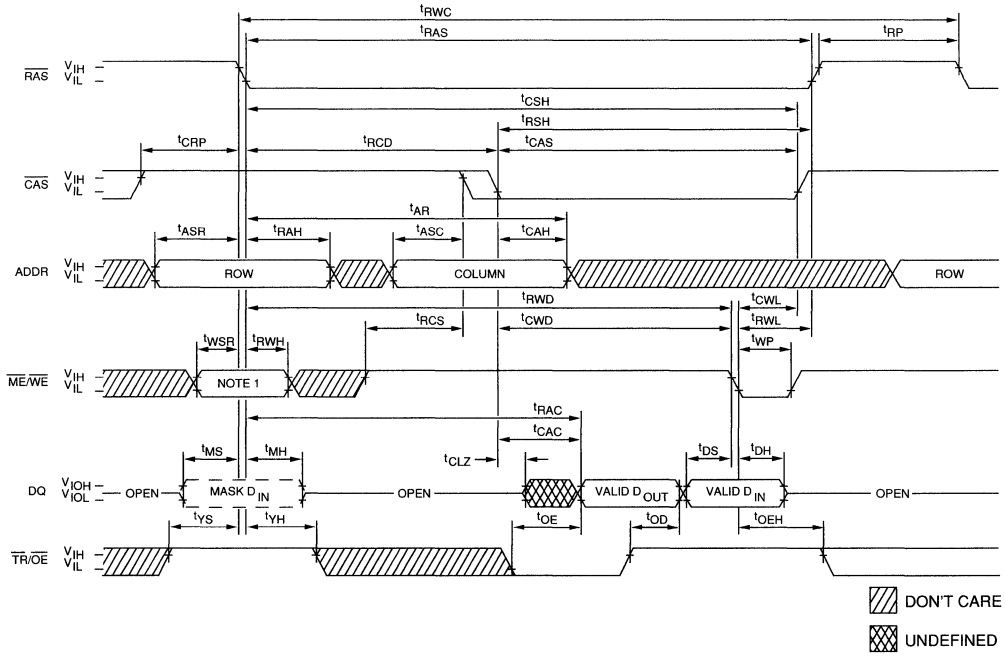
DON'T CARE

UNDEFINED

DRAM MASKED WRITE CYCLE

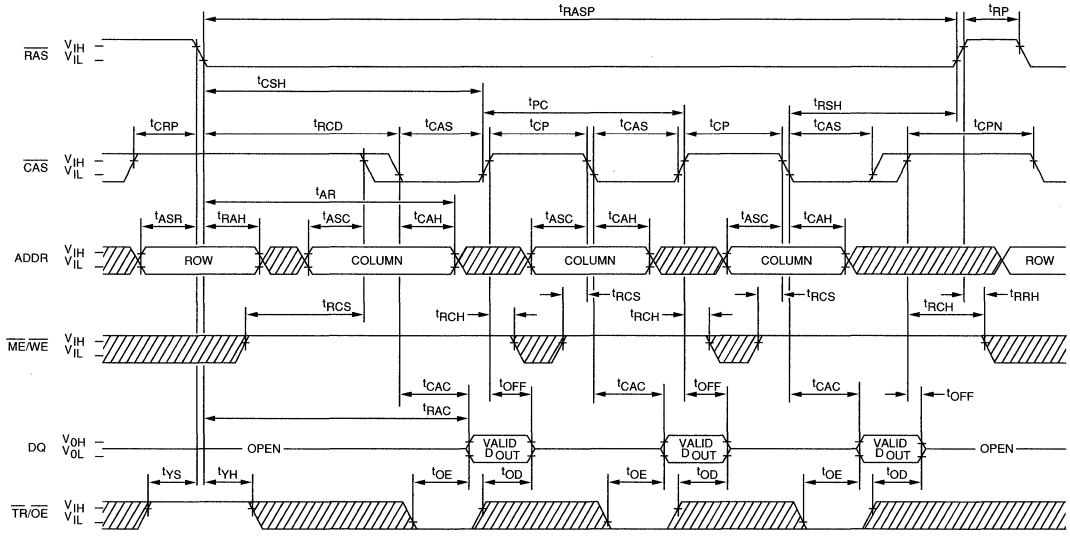


DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE and LATE-WRITE CYCLE)

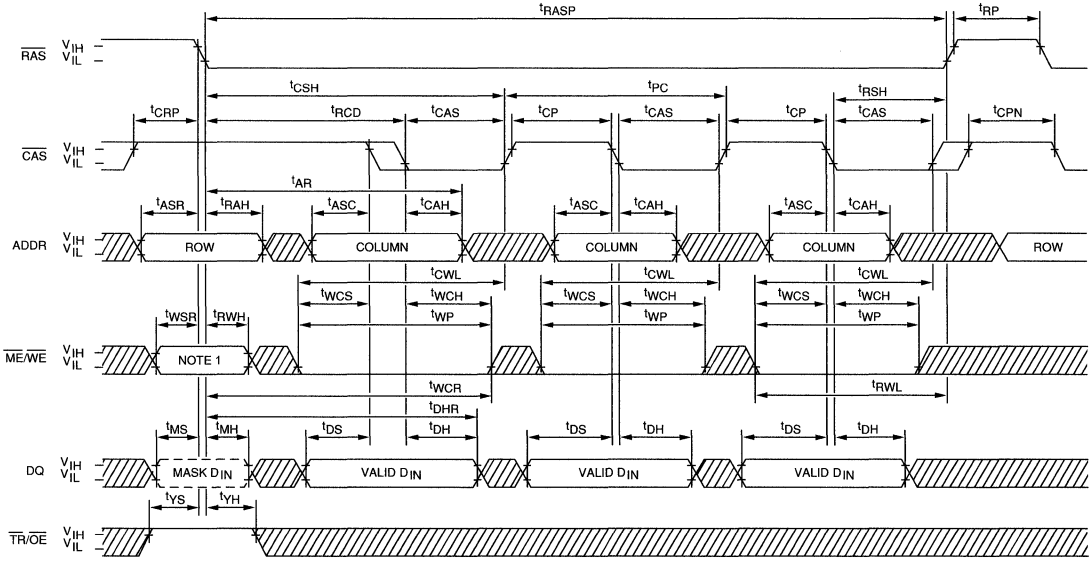


NOTE: If $\overline{ME}/\overline{WE}$ is LOW, a MASKED WRITE cycle will be performed.

DRAM PAGE-MODE READ CYCLE



DRAM PAGE-MODE EARLY-WRITE CYCLE

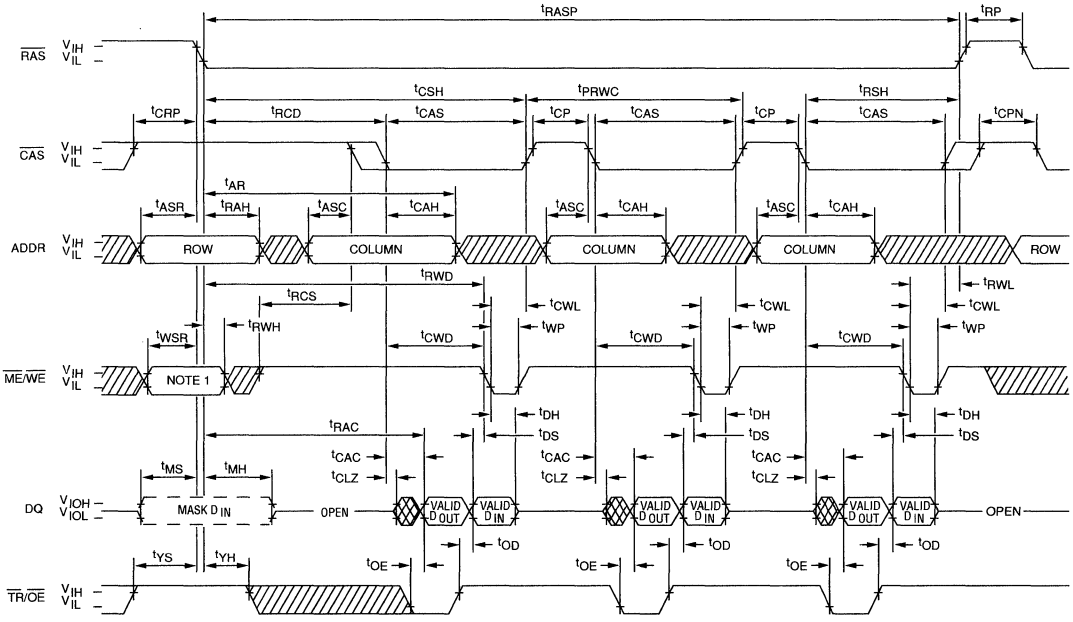


DON'T CARE

UNDEFINED

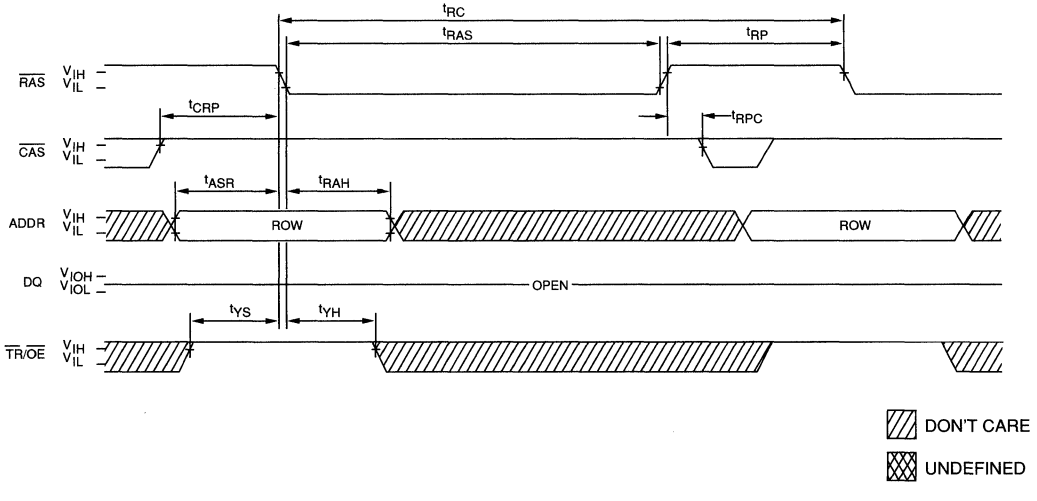
NOTE: If $\overline{ME}/\overline{WE}$ is LOW, a MASKED WRITE cycle will be performed.

DRAM PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



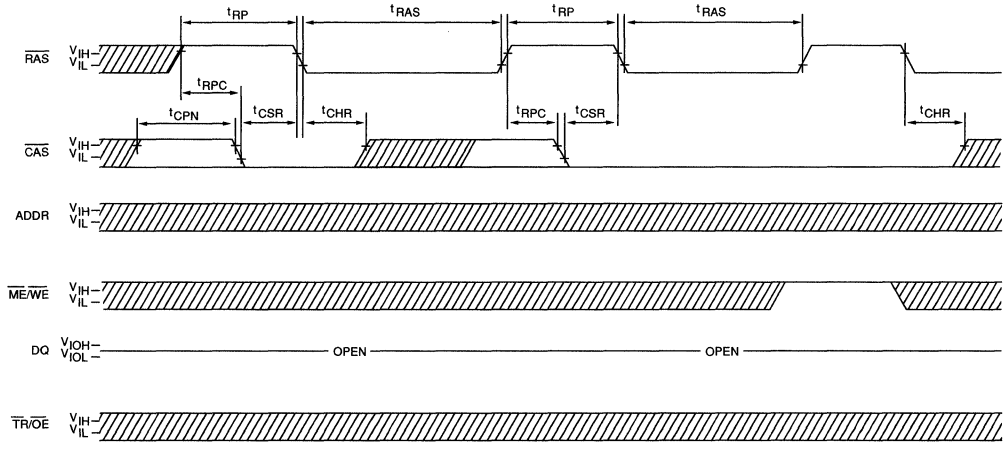
NOTE: 1. If $\overline{ME}/\overline{WE}$ is LOW, a MASKED WRITE cycle will be performed.

$\overline{RAS}$-ONLY REFRESH CYCLE
($\overline{ME}/\overline{WE}$ = Don't Care)

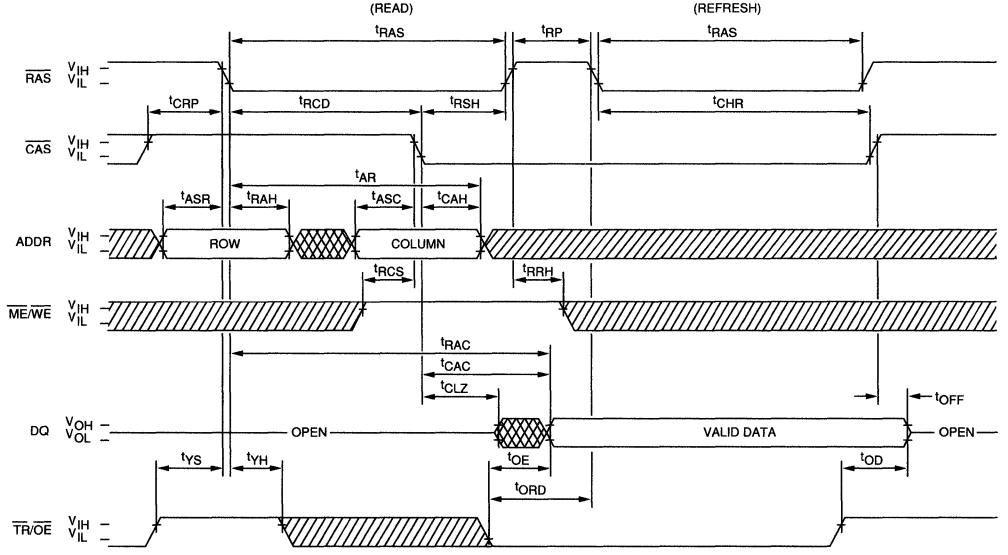


CAS-BEFORE-RAS REFRESH CYCLE

(A_0 - A_7 and ME/WE are Don't Care.)



HIDDEN REFRESH CYCLE



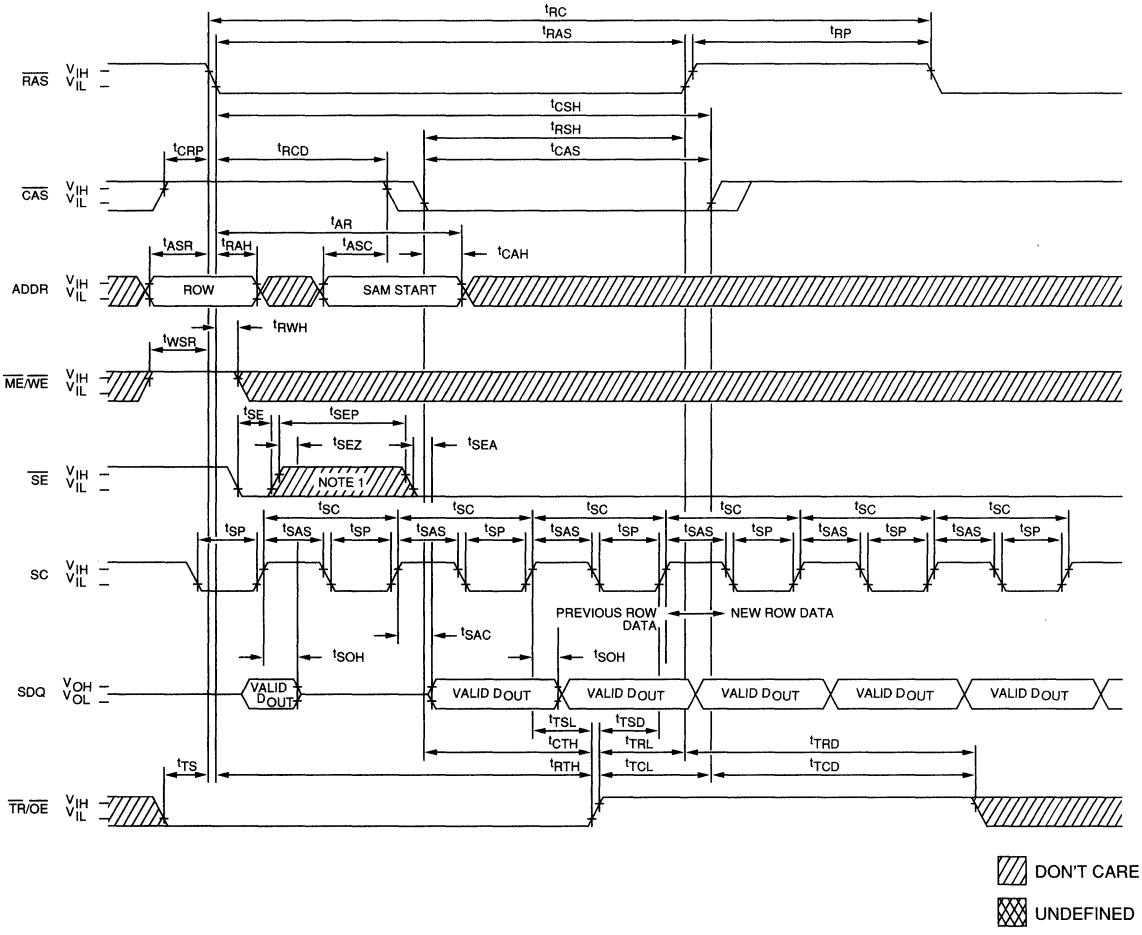
DON'T CARE

UNDEFINED

NOTE: A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case ME/WE = LOW (when CAS goes LOW) and TR/OE = HIGH.

DRAM-TO-SAM TRANSFER
(READ TRANSFER)

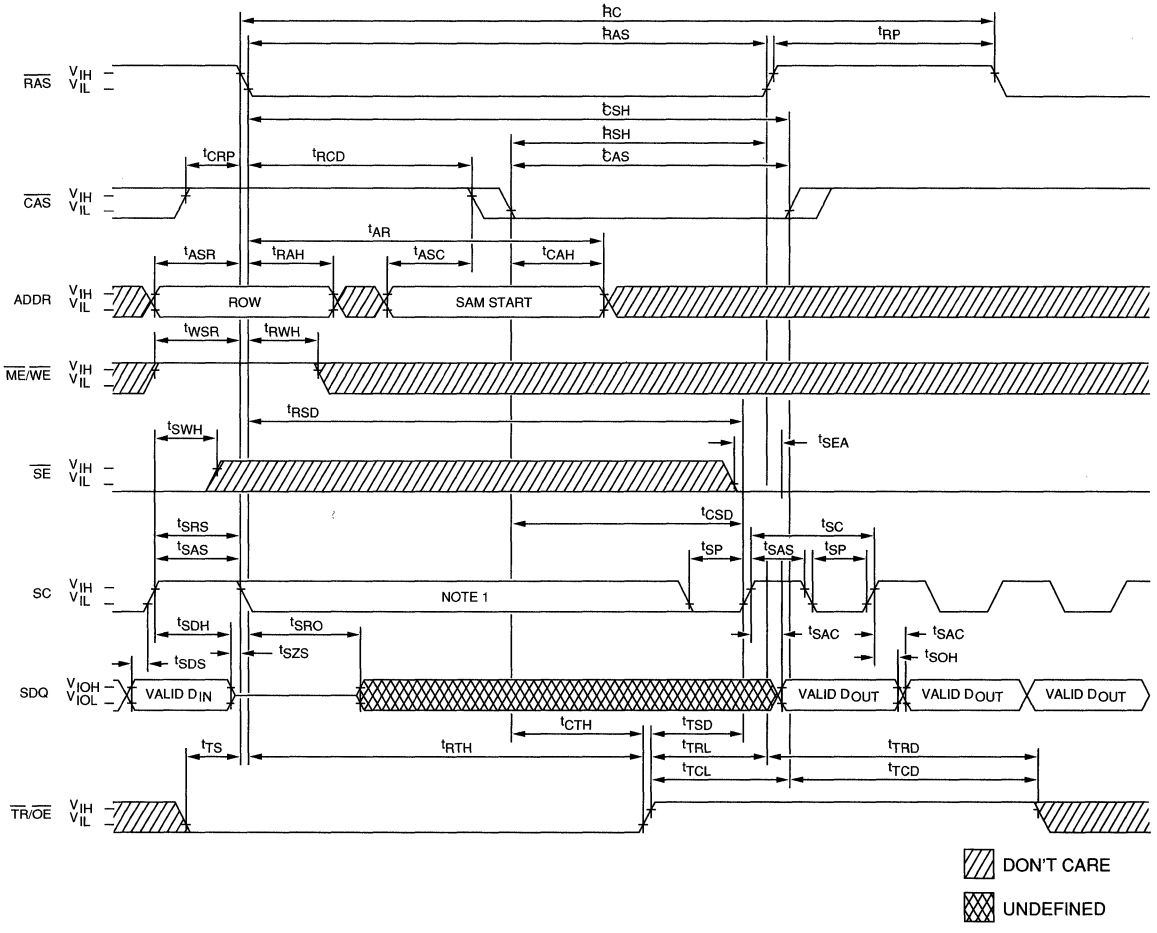
(When part was previously in the SERIAL OUTPUT mode.)



NOTE: This $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

DRAM-TO-SAM TRANSFER
(READ TRANSFER)

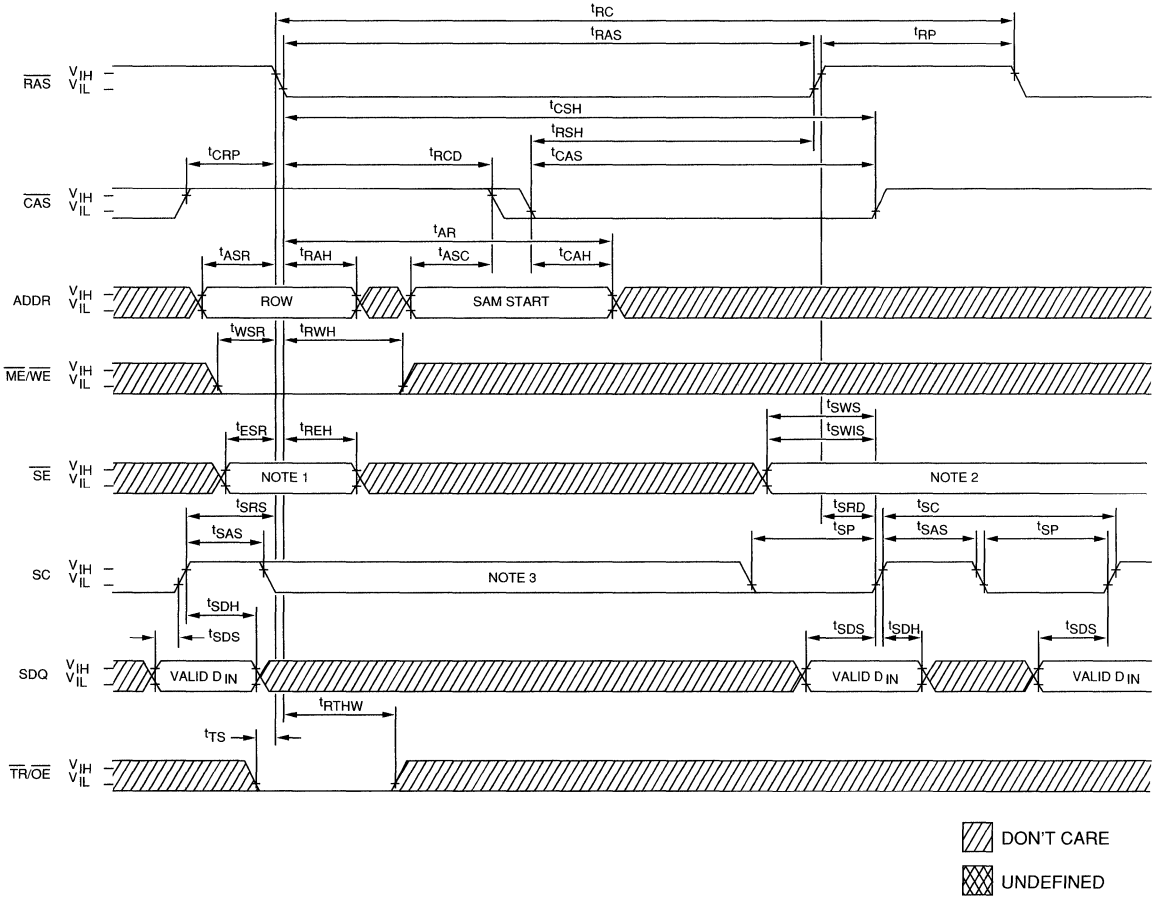
(When part was previously in the SERIAL INPUT mode.)



NOTE: There must be no rising edges on the SC input during this time.

SAM-TO-DRAM TRANSFER
(WRITE TRANSFER)

(When part was previously in the SERIAL INPUT mode.)

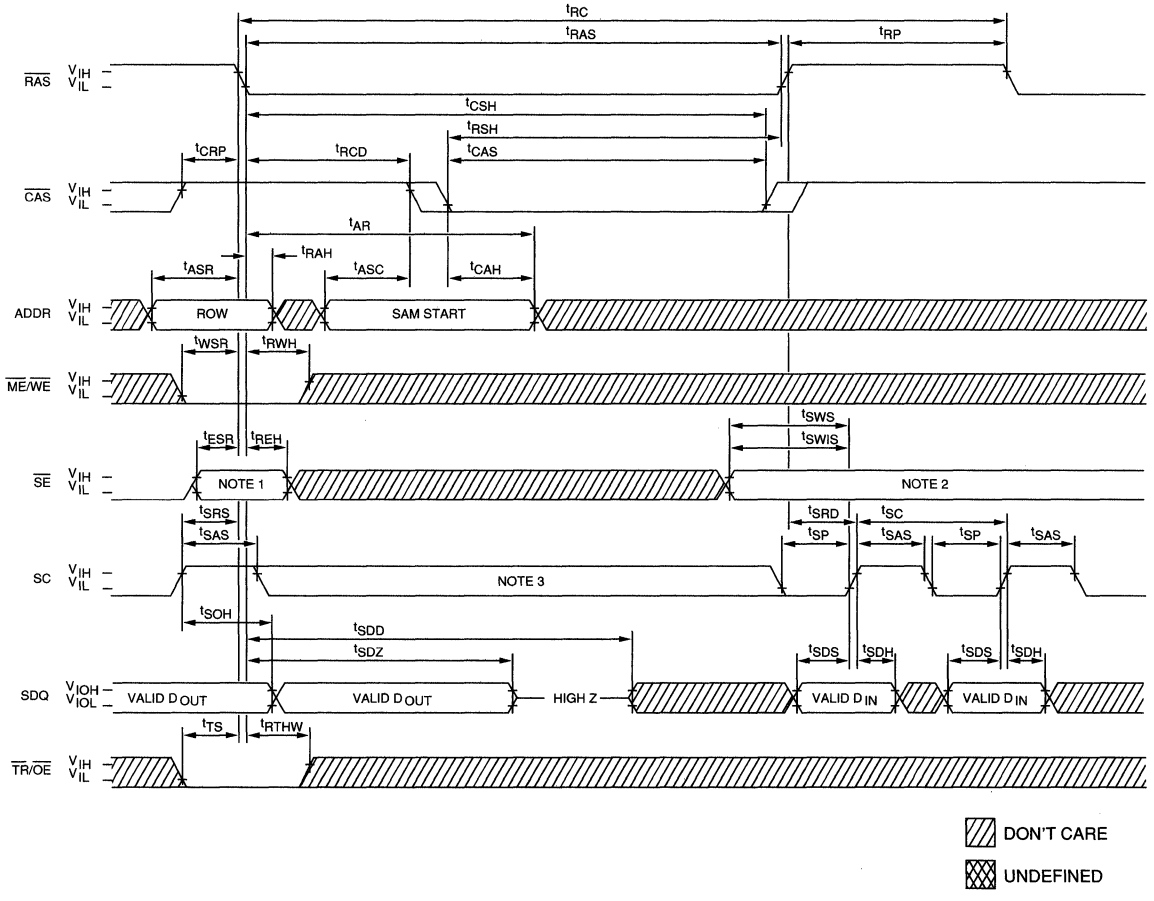


NOTE: 1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

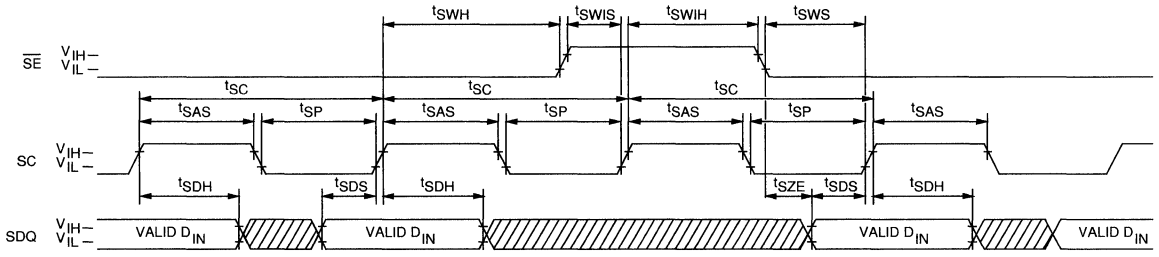
3. There must be no rising edges on the SC input during this time.

SAM-TO-DRAM TRANSFER
(WRITE TRANSFER or PSEUDO WRITE TRANSFER)
(When part was previously in the SERIAL OUTPUT mode.)

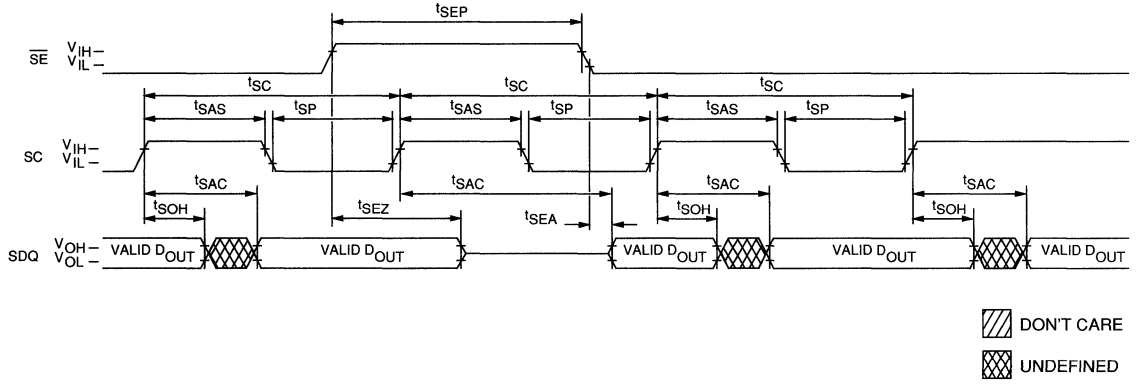


NOTE: 1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



VRAM

256K x 4 DRAM WITH 512 x 4 SAM

FEATURES

- Industry standard pinout, timing and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 256K x 4 DRAM port
  512 x 4 SAM port
- No refresh required for Serial Access Memory
- Low power: 15mW standby; 275mW active, typical
- Fast access times – 80ns random, 25ns serial

SPECIAL FUNCTIONS

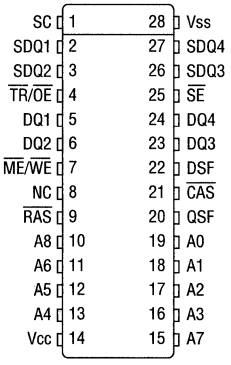
- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER

OPTIONS / MARKING

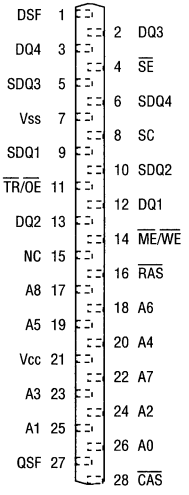
• Timing (DRAM, SAM)	
80ns, 25ns	- 8
100ns, 30ns	-10
120ns, 35ns	-12
• Packages	
Plastic SOJ	DJ
Plastic ZIP	Z

PIN ASSIGNMENT (Top View)

28-Pin SOJ (E-9)



28-Pin ZIP (C-5)



GENERAL DESCRIPTION

The MT42C4255 is a high speed, dual port CMOS dynamic random access memory or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed either by a 4-bit wide DRAM port or by a 512 x 4-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4-bit DRAM). Four 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 4-bit random access I/O port, the four internal 512 bit wide paths between the DRAM and the SAM, and the 4-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C4255 is compatible with (and can be identical to) the operation of the MT42C4064 (64K x 4 VRAM). However, the MT42C4255 offers several additional functions that may be used to increase system performance or ease critical timing requirements. These "special functions" are described in detail in the following section.

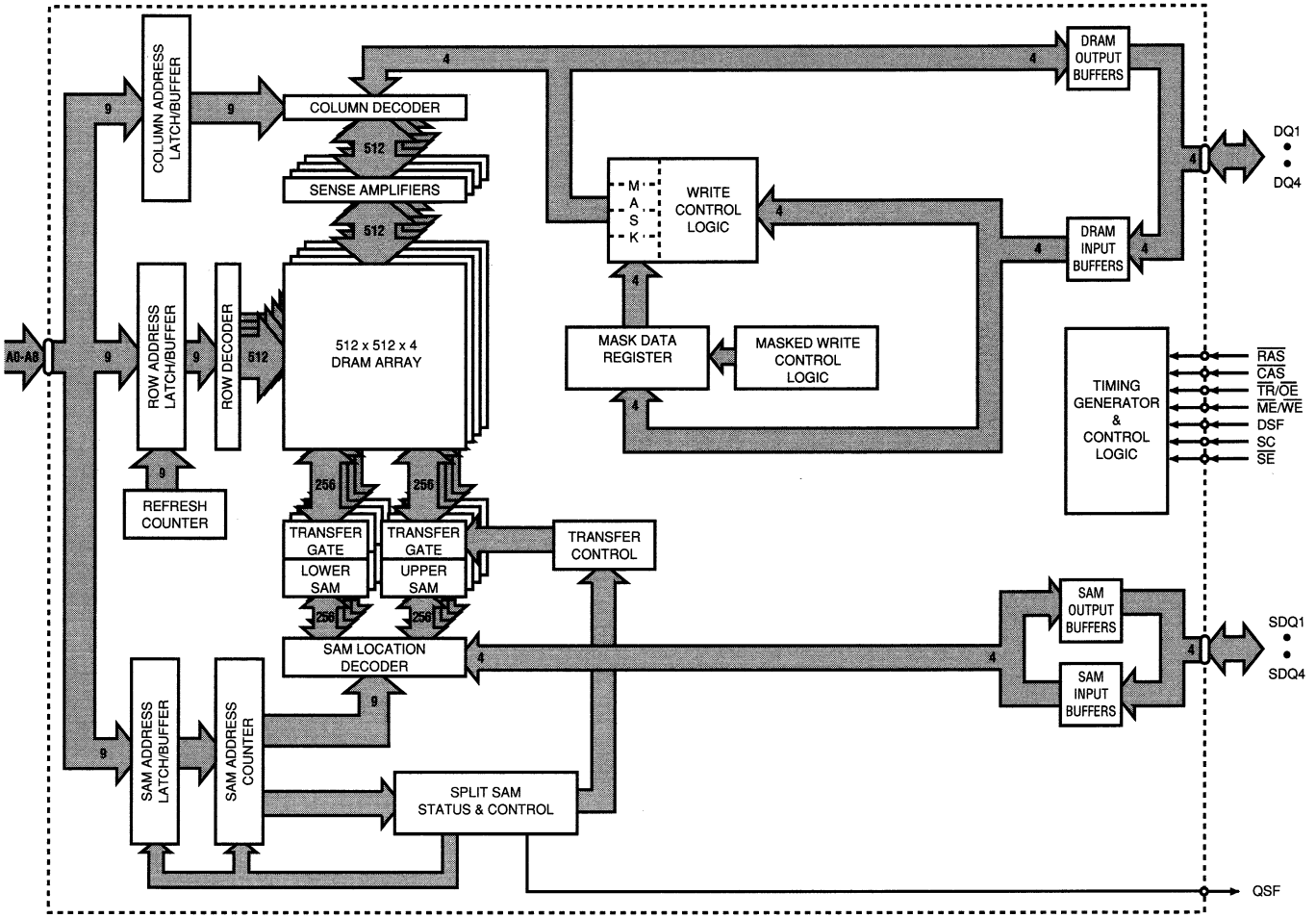


Figure 1
MT42C4255 BLOCK DIAGRAM

PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	8	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
4	11	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in the High-Z state.
7	14	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
25	4	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in the High-Z state. $\overline{SE}$ is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a PSEUDO WRITE TRANSFER cycle is performed.
22	1	DSF	Input	Special Function Select: DSF is used to indicate which special functions (MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used on a particular access cycle.
9	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and as a strobe for the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, and DQ inputs.
21	28	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 9 column-address bits and enable the DRAM output buffers (DQs) (along with $\overline{TR/OE}$).
19, 18, 17, 16, 13, 12, 11, 15, 10	26, 25, 24, 23, 20, 19, 18, 22, 17	A0 to A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select 4 bits out of the 262,144 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW). A8 = "don't care" for the start address when doing SPLIT TRANSFERS.
5, 6, 23, 24	12, 13, 2, 3	DQ1 - DQ4	Input/ Output	DRAM Data I/O: Data Input/Output for DRAM cycles; inputs for the LOAD MASK REGISTER cycles.
2, 3, 26, 27	9, 10, 5, 6	SDQ1 - SDQ4	Input/ Output	Serial Data I/O: Input/Output for SAM access cycles or High-Z, when $\overline{SE}$ = HIGH.
20	27	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address 0 to 255, HIGH if address 256 to 511.
8	15	NC	–	No Connect: This pin should be left either unconnected or tied to ground.
14	21	V_{CC}	Supply	Power Supply: +5V ±10%
28	7	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C4255 may be divided into three functional blocks (see Figure 1): the DRAM, the transfer circuitry, and the serial access memory (SAM). All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C4255 VRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 8ms. The MT42C4255 supports $\overline{CAS}$-BEFORE-$\overline{RAS}$, $\overline{RAS}$-ONLY and HIDDEN types of refresh cycles.

For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for $\overline{RAS}$-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the $\overline{RAS}$-ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles.

HIDDEN REFRESH cycles are performed by toggling $\overline{RAS}$ (and keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C4255 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has several special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select a 4-bit word from the 262,144 available are latched into the chip using the A0-A8, $\overline{RAS}$ and $\overline{CAS}$ inputs. First, the 9 row-address bits are set-up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 9 column-address bits are set-up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH to LOW.

For single port DRAMS, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. However, for the VRAM, when $\overline{RAS}$ goes LOW, $(\overline{TR})/\overline{OE}$ selects between DRAM access or TRANSFER cycles. $(\overline{TR})/\overline{OE}$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations (except $\overline{CAS}$-BEFORE-$\overline{RAS}$).

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH to LOW sometime after $\overline{RAS}$ falls to enable the DRAM output port.

For single port normal DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $\overline{ME}/(\overline{WE})$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW before $\overline{CAS}$ goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells. If $(\overline{ME})/\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

NONPERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only specific bits within a 4-bit word. The MT42C4255 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual WRITE ENABLE for each of the four DQ1-DQ4 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is non-persistent (must be re-entered at every $\overline{RAS}$ cycle) if DSF is LOW when $\overline{RAS}$ goes LOW. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle. An example NONPERSISTENT MASKED WRITE cycle is shown in Figure 2.

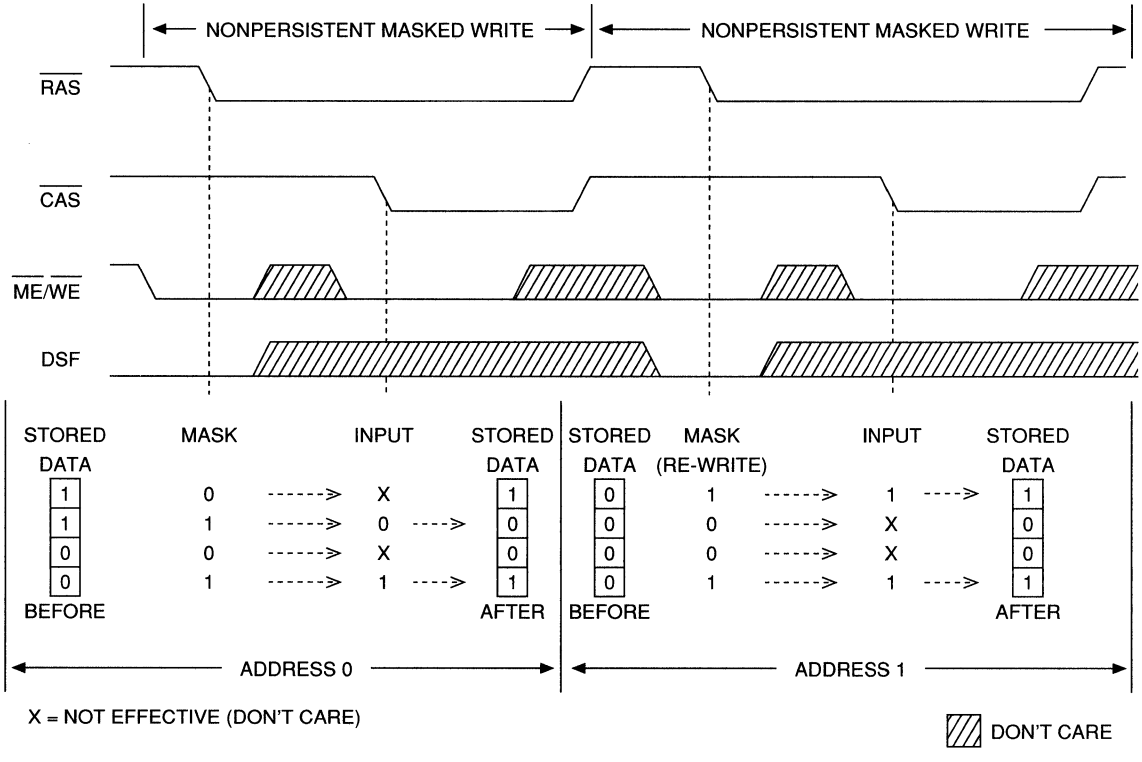


Figure 2
NONPERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW. Mask data may also be loaded into the mask register by performing a NONPERSISTENT MASKED WRITE before the PERSISTENT MASKED WRITE.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls, and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITE cycles, to any address, may be performed without having to reload the mask data register. Figure 3 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot provide mask data to the DQ pins at $\overline{RAS}$ time to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations can be performed during FAST PAGE MODE and the same mask will apply to all addressed columns in the addressed row.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a REGISTER load cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless NONPERSISTENT MASKED WRITE or LOAD MASK REGISTER cycles are performed.

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE cycles to selectively enable writes to the four DQ planes.

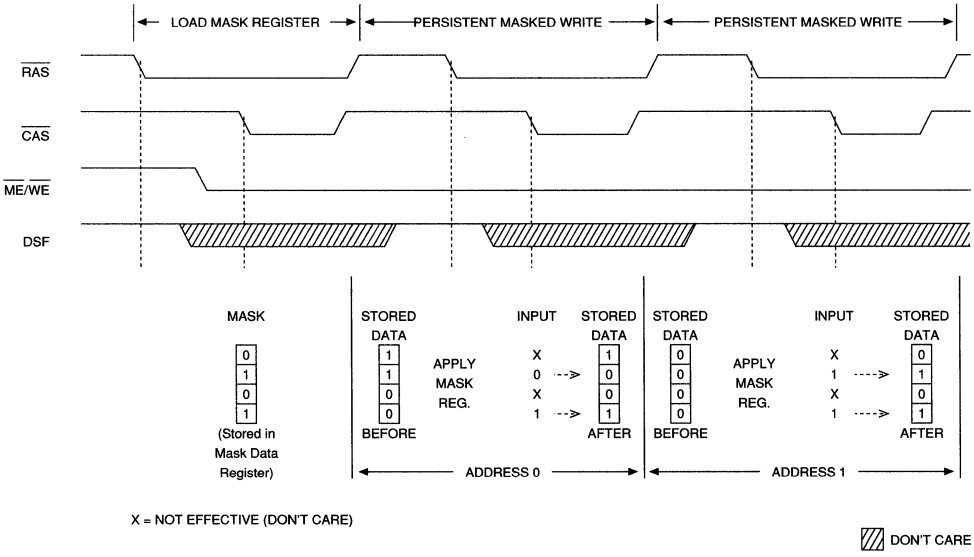


Figure 3
PERSISTENT MASKED WRITE EXAMPLE

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the four 512-bit DRAM row planes that are to be transferred to the four SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished two ways. If the transfer is to be synchronized with SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW (refer to the AC Timing Diagrams). The 2048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 9-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 255), and HIGH if access is from the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

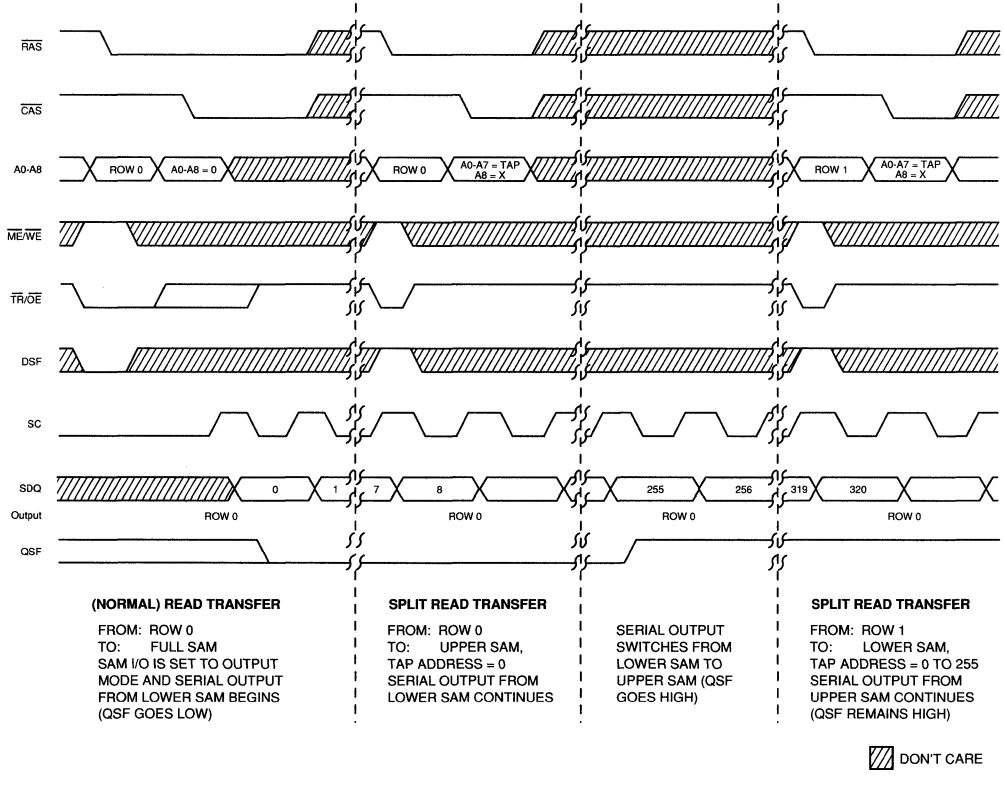


Figure 5
TYPICAL SPLIT READ TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data can be transferred to the other half. The transfer can occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles.

A normal, non-split READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles to provide a reference to which half of the SAM the access will begin. Then SPLIT READ TRANSFERS may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH to LOW transition of $\overline{CAS}$. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 5 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The purpose of the SPLIT TRANSFER of the same data is to initiate the split SAM operating mode and load the Tap address. Serial access continues, and when the SAM address counter reaches 255 ("A8"=0, A0-A7=1) the new Tap address is loaded for the next half ("A8"=1, A0-A7=Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 5 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transfer the upper half of row 1 to the upper SAM.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously, except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QFS is LOW if access is to the lower half of the SAM, and HIGH if access is to the upper half.

PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER is a WRITE TRANSFER with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and $(\overline{ME})/\overline{WE}$ is LOW when $\overline{RAS}$ goes LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle.

POWER UP AND INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 8ms, the MT42C4255 must be initialized.

After Vcc is at specified operating conditions, for 100µs minimum, 8 $\overline{RAS}$ cycles and 1 SC cycle must be executed to initialize the memory array. When the device is initialized, the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of $(\overline{TR})/\overline{OE}$. The DRAM array will contain random data.

The SAM portion of the MT42C4255 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQ's) will be High- Z, regardless of the state of $\overline{SE}$a,b. The mask register will contain random data after power-up.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					A0 - A8[1]		DQ1 - DQ4[2]		
		CAS	TR / OE	ME / WE	DSF	SE	RAS	CAS A8=X	RAS	CAS[3]	MASK REGISTER
	DRAM OPERATIONS										
CBR	CAS-BEFORE-RAS REFRESH	0	X	X	X	X	—	X	—	X	X
ROR	RAS-ONLY REFRESH	1	1	X	X	X	ROW	—	X	—	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	ROW	COLUMN	X	VALID DATA	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	ROW	COLUMN	X	VALID DATA	USE
	REGISTER OPERATIONS										
LMR	LOAD MASK REGISTER	1	1	1	1	X	ROW[4]	X	X	WRITE MASK	LOAD
	TRANSFER OPERATIONS										
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	ROW	TAP[5]	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	ROW	TAP[5]	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	ROW	TAP[5]	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)	1	0	0	0	1	ROW[4]	TAP[5]	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	ROW	TAP[5]	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ4 inputs when RAS falls and when CAS falls.
3. On WRITE cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is latched at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. This is the first SAM address location that the first SC cycle will access. For Split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for lower half, 511 for upper half).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Operating Temperature, Ta(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input ($0V \leq V_{IN} \leq V_{CC}$), all other pins not under test = 0V)	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		8	pF	2
Input/Output Capacitance: DQ, SDQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	90	80	70	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	70	60	50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min)	I_{CC3}	10	10	10	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH})	I_{CC4}	90	80	70	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling)	I_{CC5}	80	70	60	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	95	85	75	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC7}	130	120	110	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC8}	110	100	90	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min)	I_{CC9}	50	45	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH})	I_{CC10}	130	120	110	mA	3, 4
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling)	I_{CC11}	120	110	100	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	135	125	115	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		180		210		ns	
READ-MODIFY-WRITE cycle time	^tRWC	205		235		280		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		55		65		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	100		110		140		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		25		30		35	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	^tOE		20		25		30	ns	
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		30		35		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		80		ns	
$\overline{CAS}$ pulse width	^tCAS	25	10,000	30	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	55	20	70	25	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	12		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	20	60	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	20		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	30	ns	20, 23
Output Disable	^tOD	0	20	0	20	0	30	ns	23
Output Disable hold time from start of write	^tOEH		15		15		20	ns	27
Output Enable to $\overline{RAS}$ delay	^tORD		0		0		0	ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		70		85		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		130		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		80		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	55		60		65		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	30		30		30		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	12		15		15		ns	
Mask Data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask Data to $\overline{RAS}$ hold time	^tMH	12		15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER command to $\overline{RAS}$ setup time	^tTLS	0		0		0		ns	25
TRANSFER command to $\overline{RAS}$ hold time	^tTLH	12	10,000	15	10,000	15	10,000	ns	25
TRANSFER command to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	^tRTH	70	10,000	80	10,000	90	10,000	ns	25
TRANSFER command to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	^tCTH	20		25		30		ns	25
TRANSFER command to column address hold time (for REAL TIME READ TRANSFER only)	^tATH	25		30		35		ns	25
TRANSFER command to SC lead time	^tTSL	5		5		5		ns	25
TRANSFER command to $\overline{RAS}$ lead time	^tTRL	0		0		0		ns	25
TRANSFER command to $\overline{RAS}$ delay time	^tTRD	15		15		15		ns	25
TRANSFER command to $\overline{CAS}$ time	^tTCL	0		0		0		ns	25
TRANSFER command to $\overline{CAS}$ delay time	^tTCD	15		15		15		ns	25
First SC edge to TRANSFER command delay time	^tTSD	10		10		10		ns	25
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	10	35	10	40	10	50	ns	
SC to $\overline{RAS}$ setup time	^tSRS	30		30		40		ns	
$\overline{RAS}$ to SC delay time	^tSRD	20		25		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		0		ns	
$\overline{RAS}$ to SD buffer turn-on time	^tSRO	10		15		15		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	45		50		55		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	12		15		15		ns	
NONTRANSFER command to $\overline{RAS}$ setup time	^tYS	0		0		0		ns	26
NONTRANSFER command to $\overline{RAS}$ hold time	^tYH	12		15		15		ns	26
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	12		15		15		ns	
SC to QSF delay time	^tSQD		25		30		35	ns	
SPLIT TRANSFER setup time	^tSTS	30		35		40		ns	
SPLIT TRANSFER hold time	^tSTH	30		35		40		ns	
$\overline{RAS}$ to QSF delay time	^tRQD		65		85		105	ns	
$\overline{TR/OE}$ to QSF delay time	^tTQD		25		30		35	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		35		40		45	ns	
$\overline{RAS}$ to first SC delay	^tRSD	80		95		105		ns	
$\overline{CAS}$ to first SC delay	^tCSD	20		25		35		ns	
Column address valid to first SC delay	^tASD	45		55		65		ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

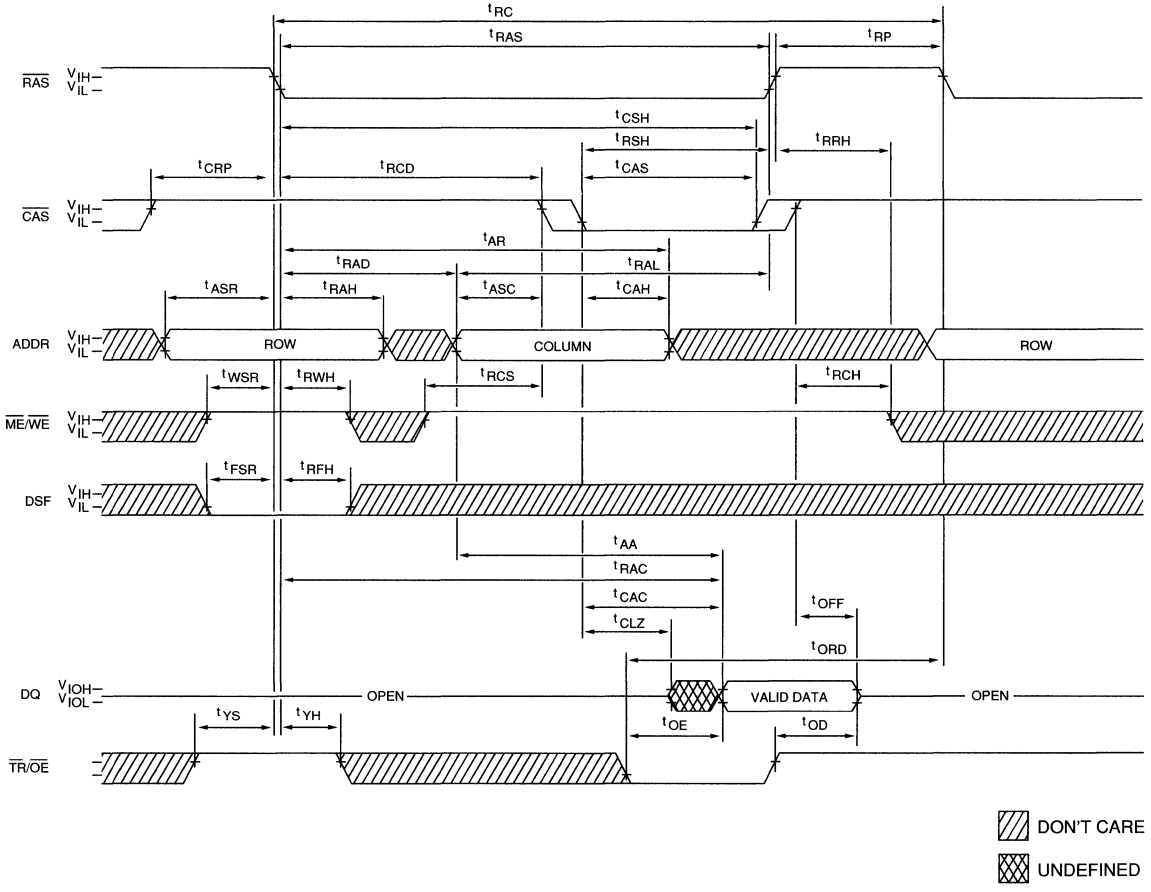
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	25		30		35		ns	
Access time from SC	^tSAC		25		30		35	ns	24
SC precharge time (SC LOW time)	^tSP	10		10		12		ns	
SC pulse width (SC HIGH time)	^tSAS	10		10		12		ns	
Access time from $\overline{SE}$	^tSEA		15		20		30	ns	24
$\overline{SE}$ precharge time	^tSEP	10		15		15		ns	
$\overline{SE}$ pulse width	^tSE	10		15		15		ns	
Serial data-out hold time after SC high	^tSOH	5		5		5		ns	24
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	0	12	0	15	0	25	ns	24
Serial data-in setup time	^tSDS	0		0		0		ns	24
Serial data-in hold time	^tSDH	10		15		20		ns	24
SERIAL INPUT (Write) Enable setup time	^tSWS	0		0		0		ns	
SERIAL INPUT (Write) Enable hold time	^tSWH	10		15		20		ns	
SERIAL INPUT (Write) Disable setup time	^tSWIS	0		0		0		ns	
SERIAL INPUT (Write) Disable hold time	^tSWIH	10		15		20		ns	

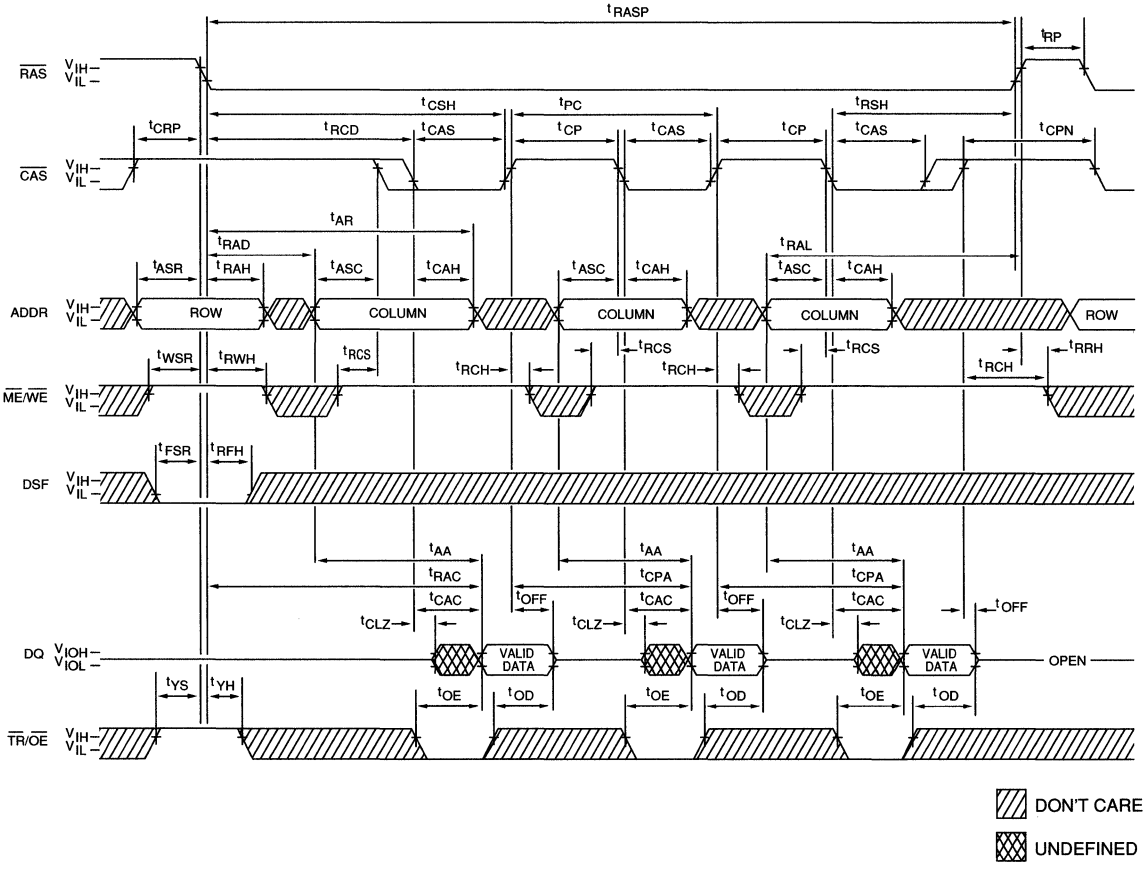
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles and 1 SC cycle before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, DRAM data output (DQ1-DQ4) is high impedance.
12. If $\overline{CAS} = V_{IL}$, DRAM data output (DQ1-DQ4) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF. Output reference levels: $V_{OH} = 2.4V$; $V_{OL} = 0.4V$.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \leq ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 2 TTL gate and 50pF. Output reference levels: $V_{OH} = 2.0V$; $V_{OL} = 0.8V$.
25. TRANSFER command means that $\overline{TR}/\overline{OE}$ is LOW when $\overline{RAS}$ goes LOW.
26. NONTRANSFER command means that $\overline{TR}/\overline{OE}$ is HIGH when $\overline{RAS}$ goes LOW.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



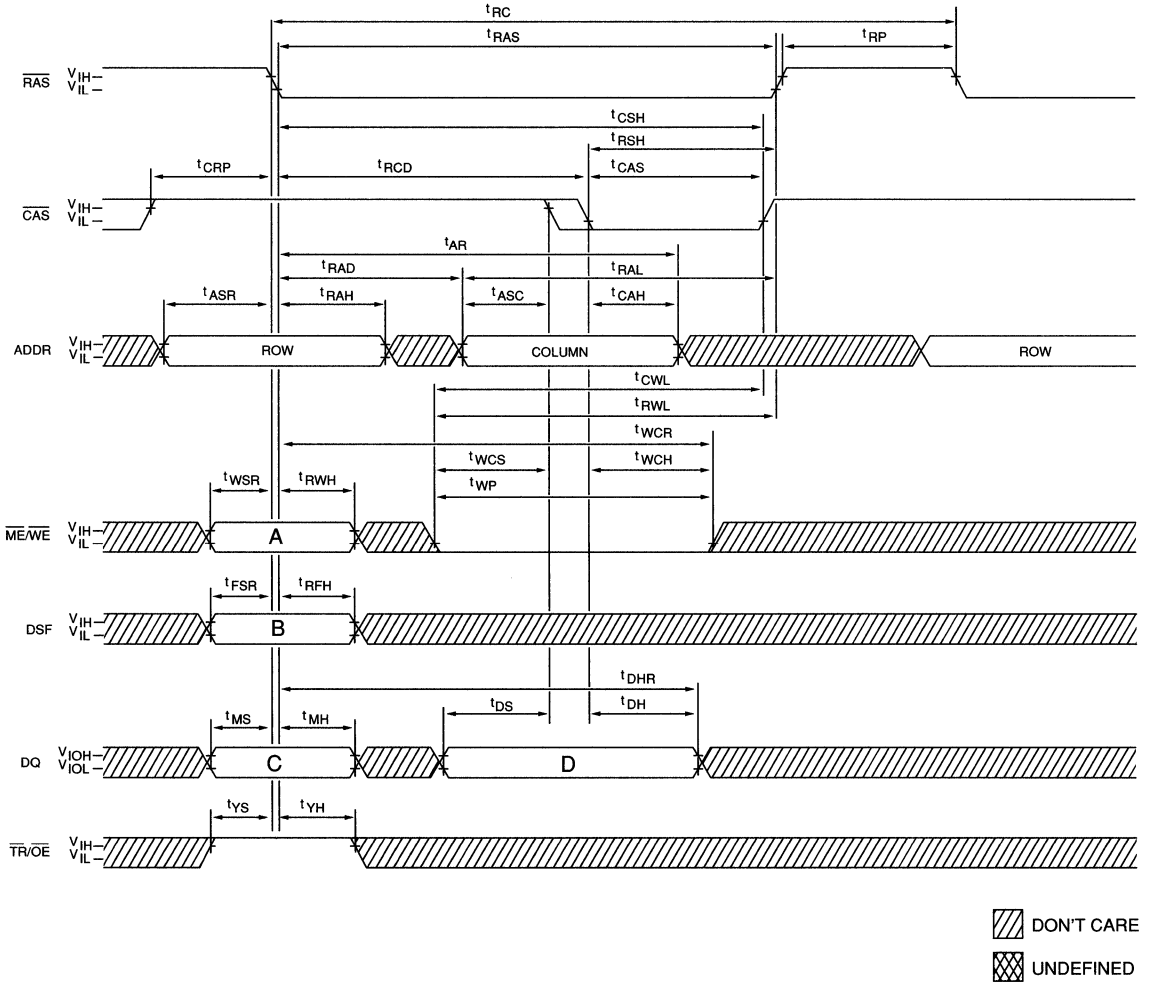
NOTE: WRITE or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

WRITE CYCLE FUNCTION TABLE

LOGIC STATES				FUNCTION
$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DQ (Input)	
1	0	X	DRAM Data	Normal DRAM WRITE
0	0	Write Mask	DRAM Data (Masked)	NONPERSISTENT (Load and Use Register) MASKED WRITE to DRAM
0	1	X	DRAM Data (Masked)	PERSISTENT (Use Register) MASKED WRITE to DRAM
1	1	X	Write Mask	Load Mask Register

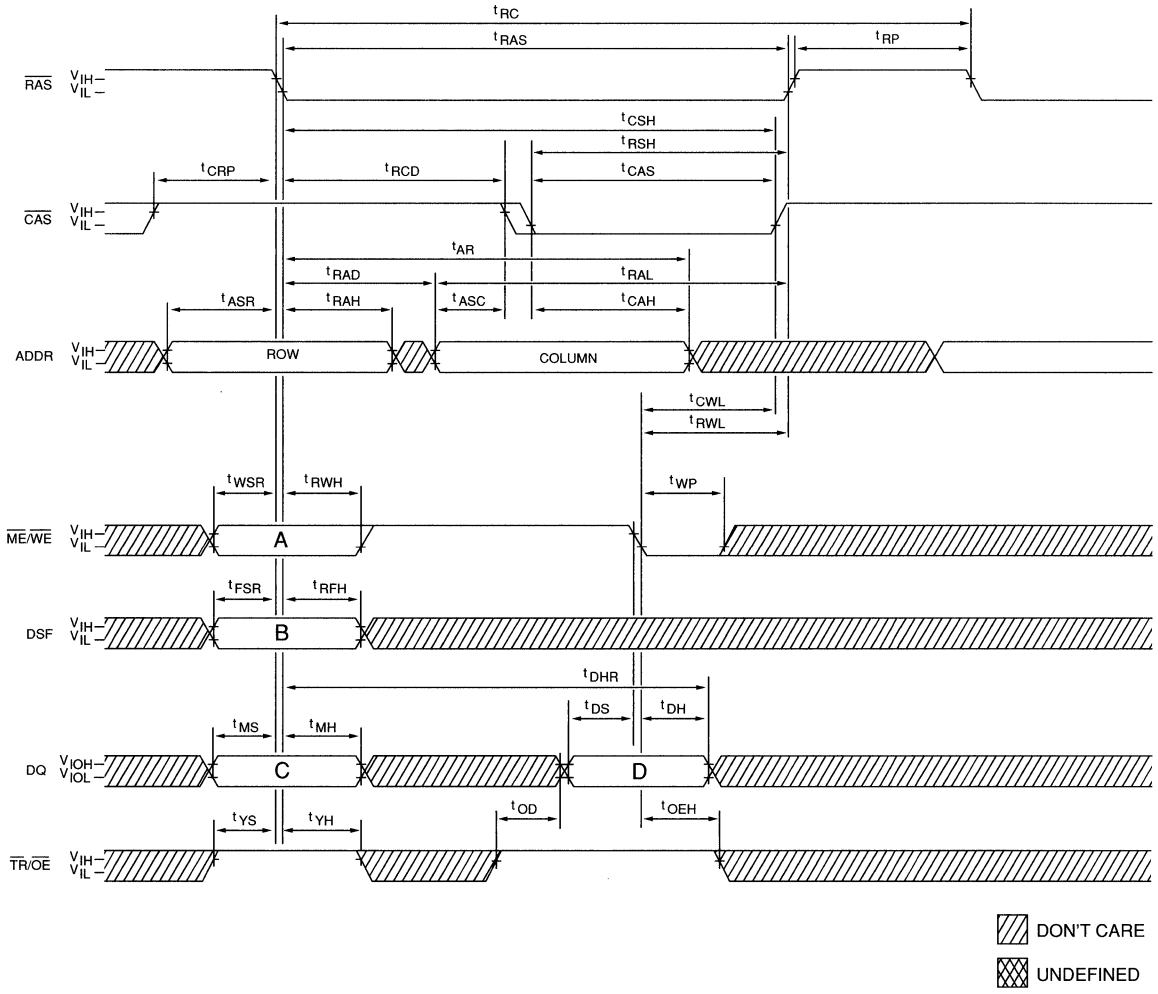
NOTE: Refer to this function table to determine the logic states of "A", "B", "C", and "D" for the WRITE cycle timing diagrams on the following pages.

DRAM EARLY-WRITE CYCLE



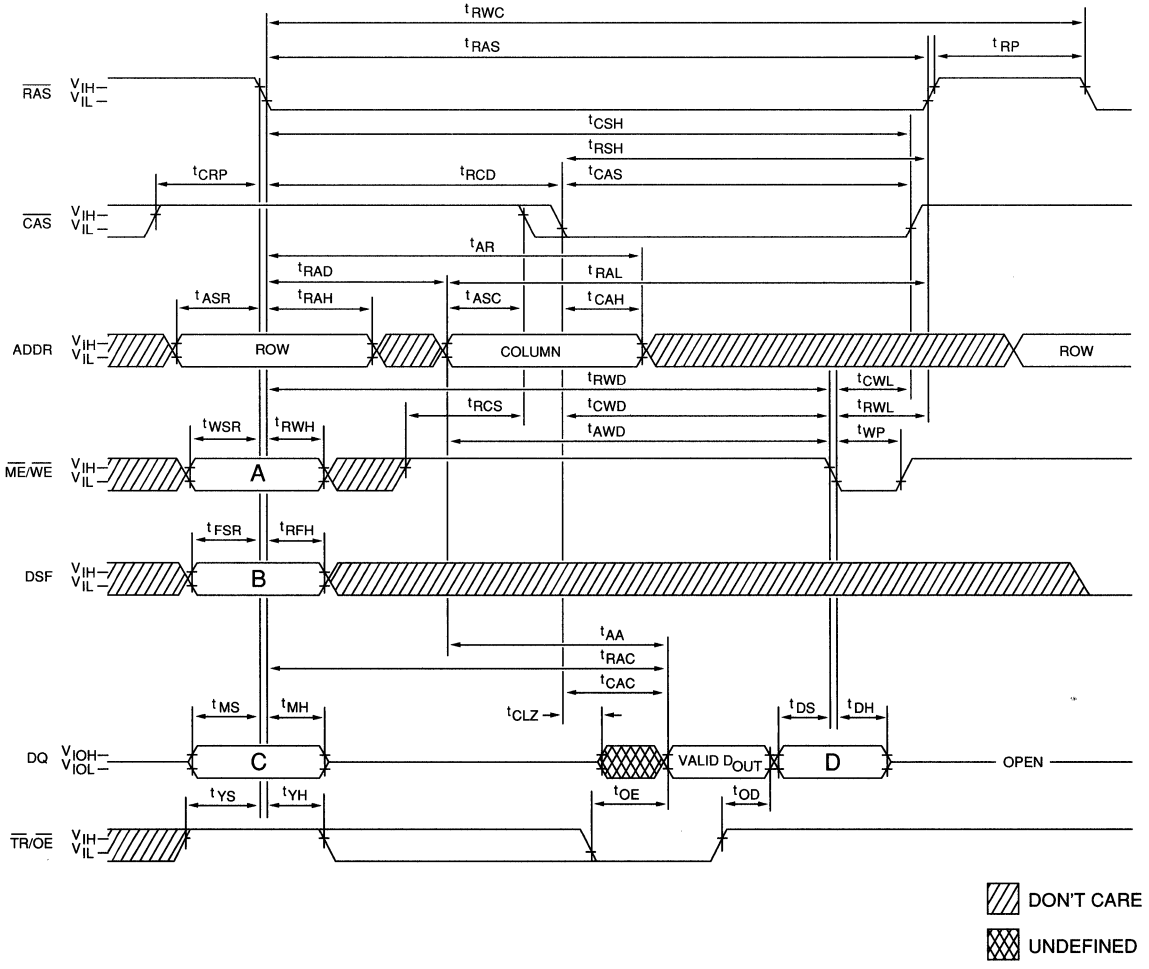
NOTE: The logic states of "A", "B", "C", and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE



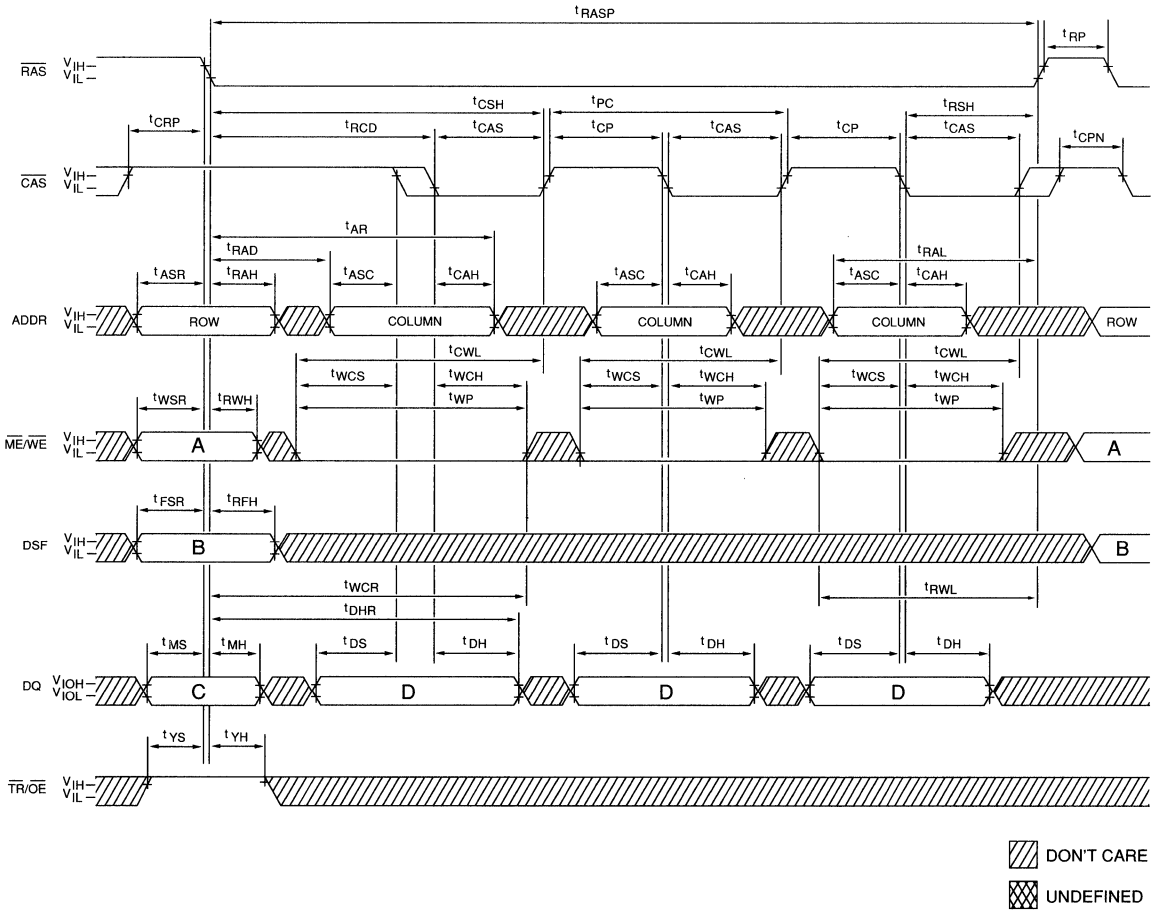
NOTE: The logic states of "A", "B", "C", and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



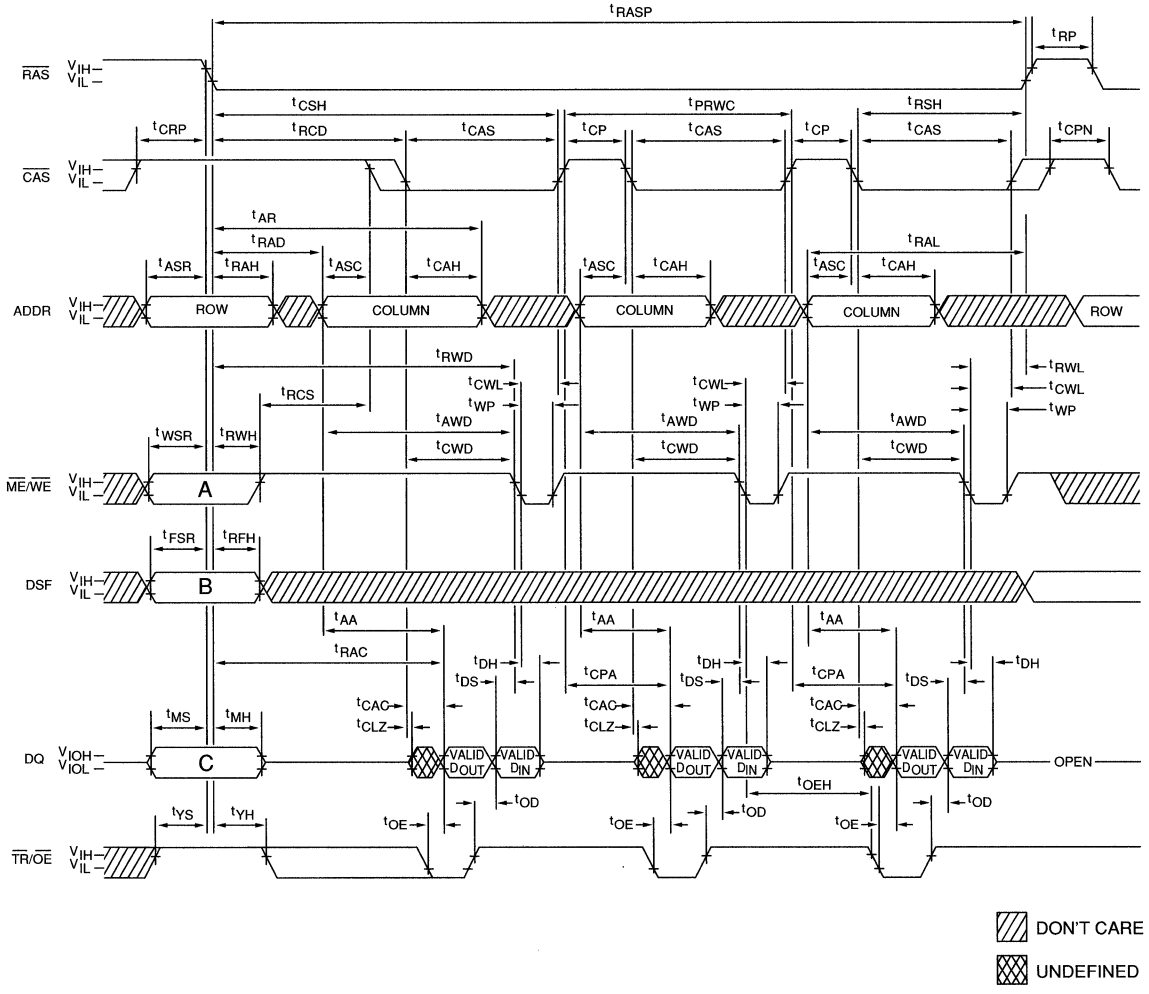
NOTE: The logic states of "A", "B", "C", and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
2. The logic states of "A", "B", "C", and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

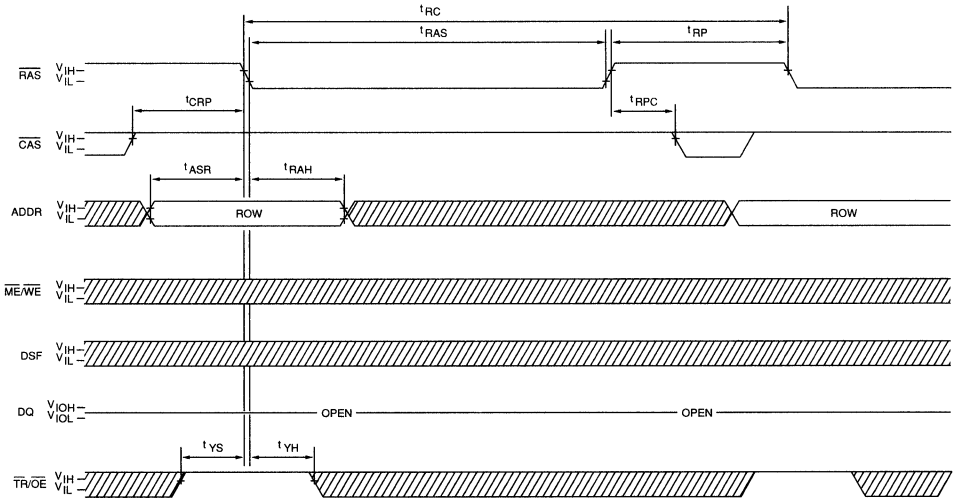
DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE or LATE-WRITE CYCLES)



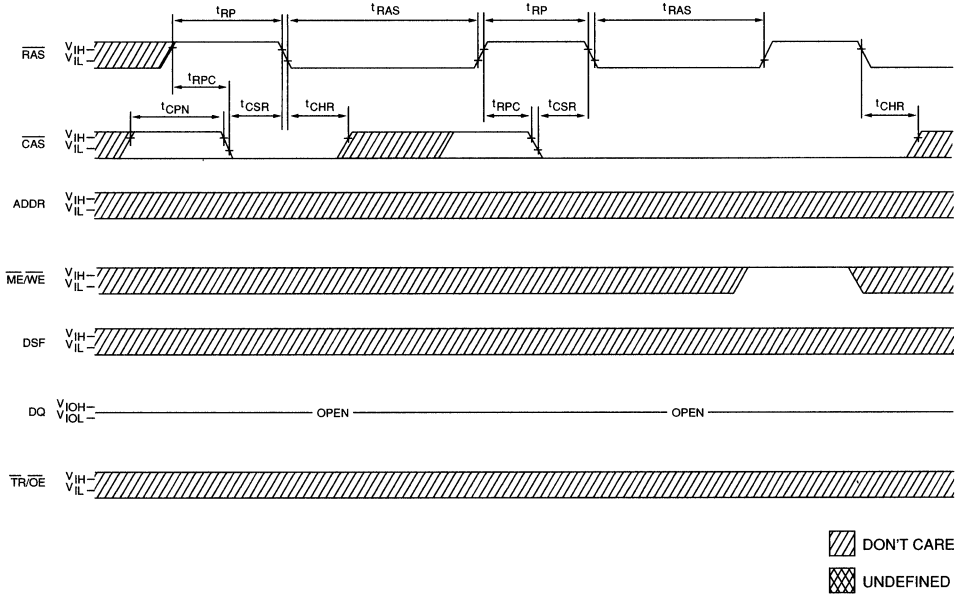
NOTE: 1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE

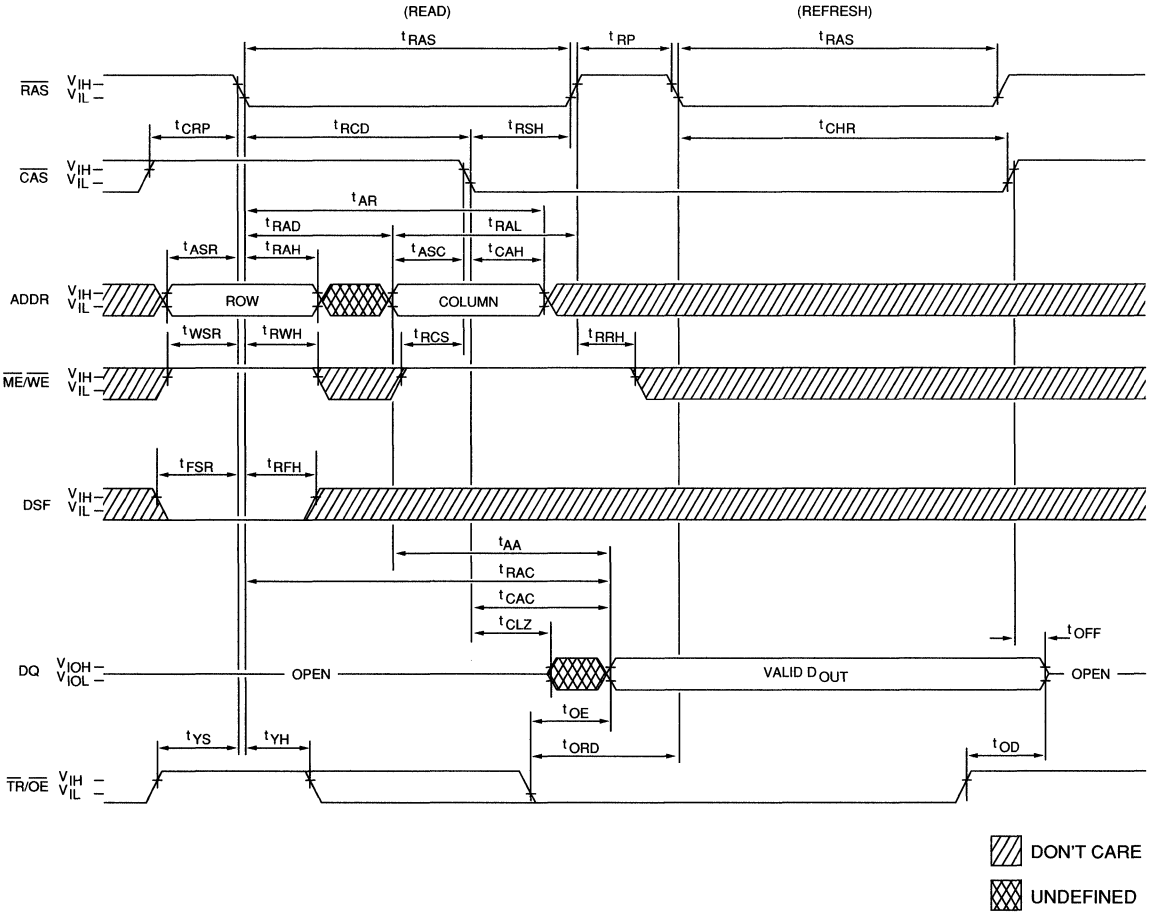
(ADDR = A0-A8)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

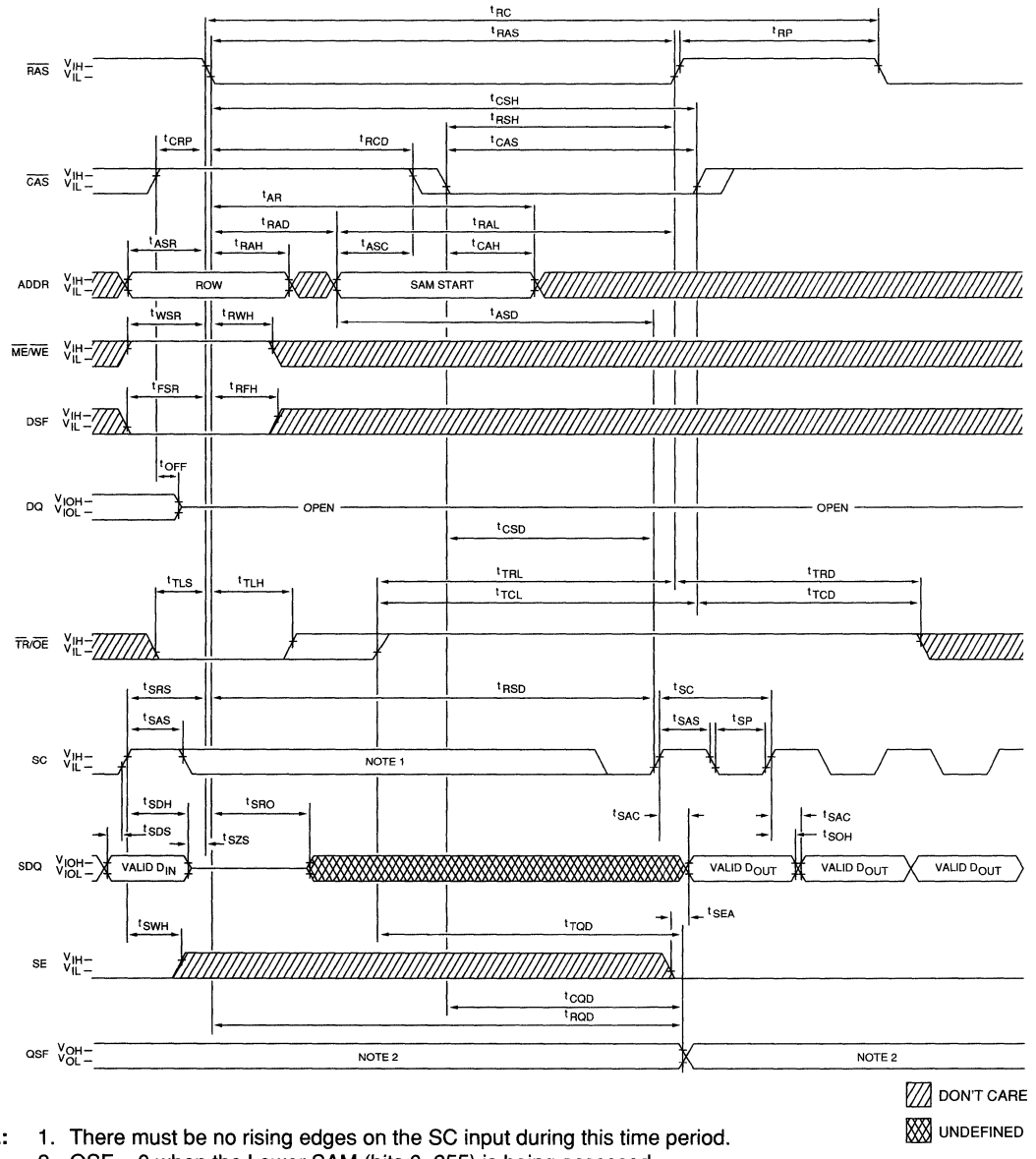


DRAM HIDDEN-REFRESH CYCLE



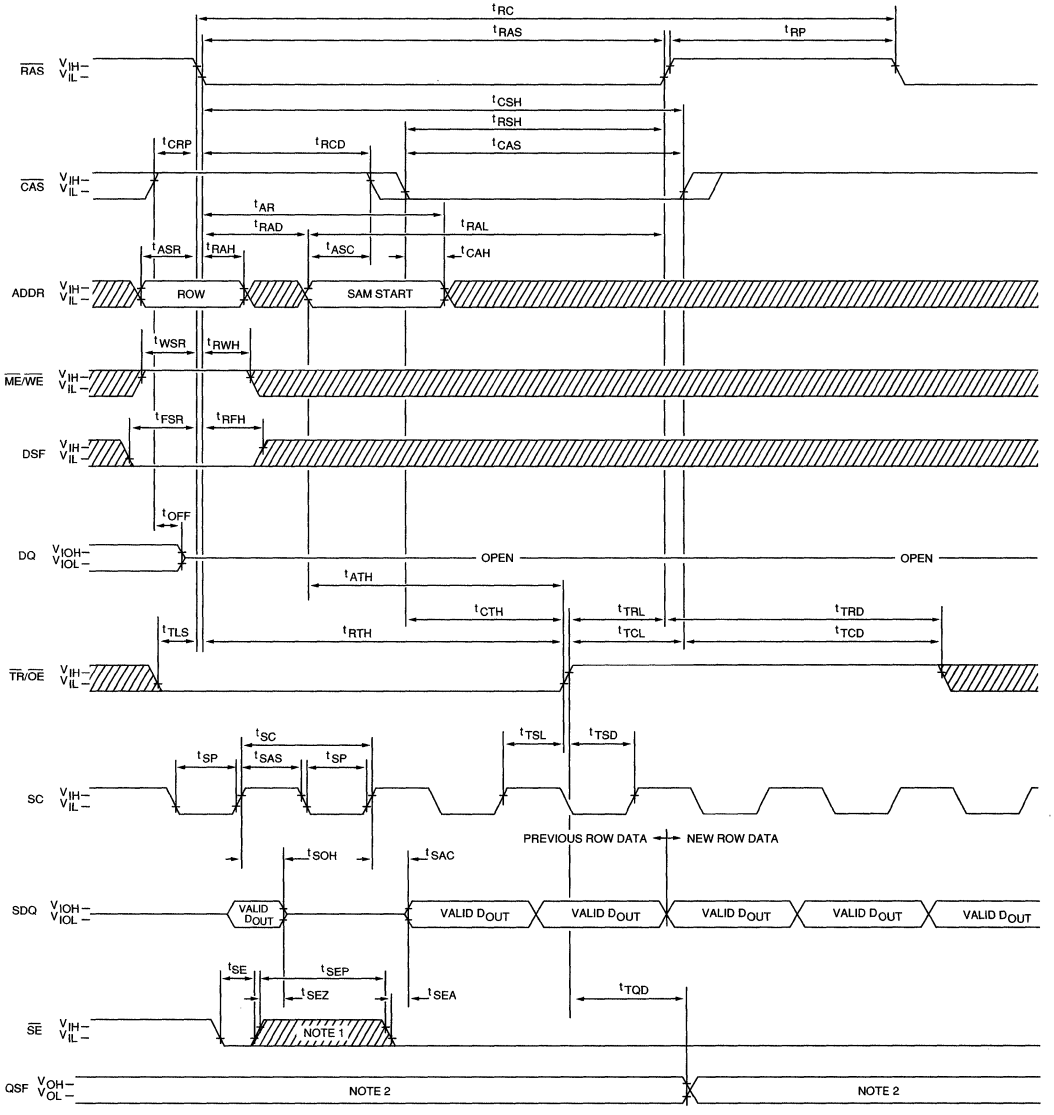
NOTE: A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



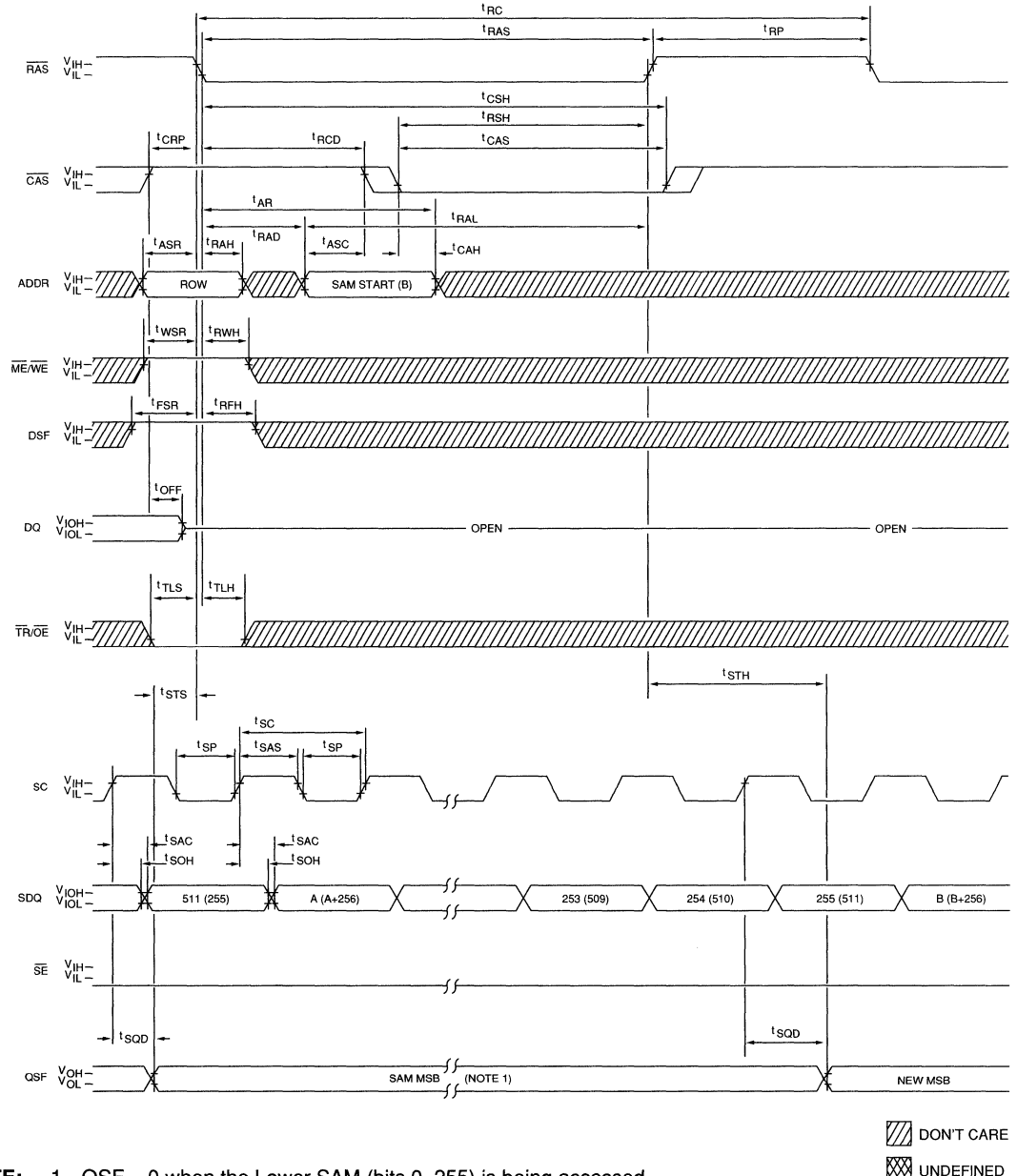
NOTE: 1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

REAL-TIME READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

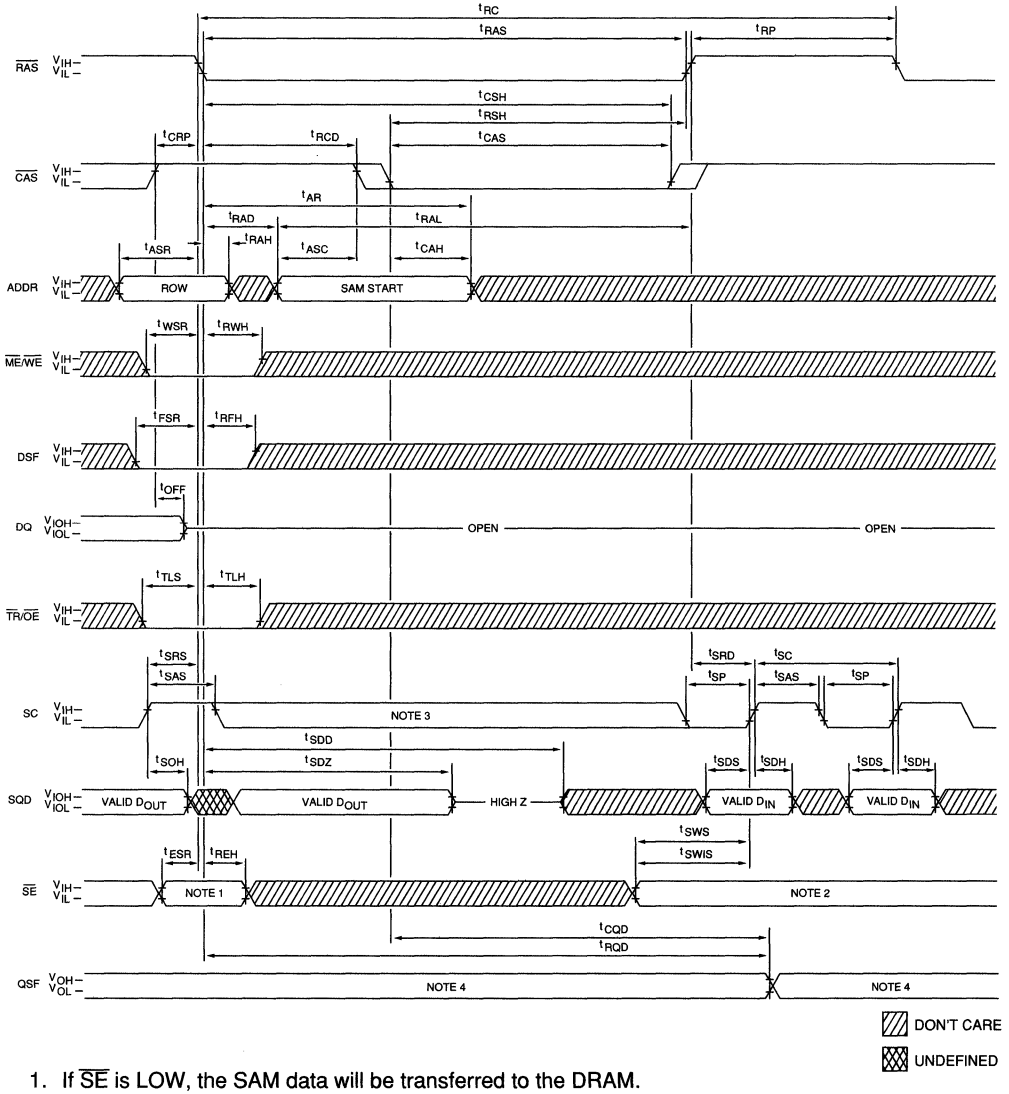
SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

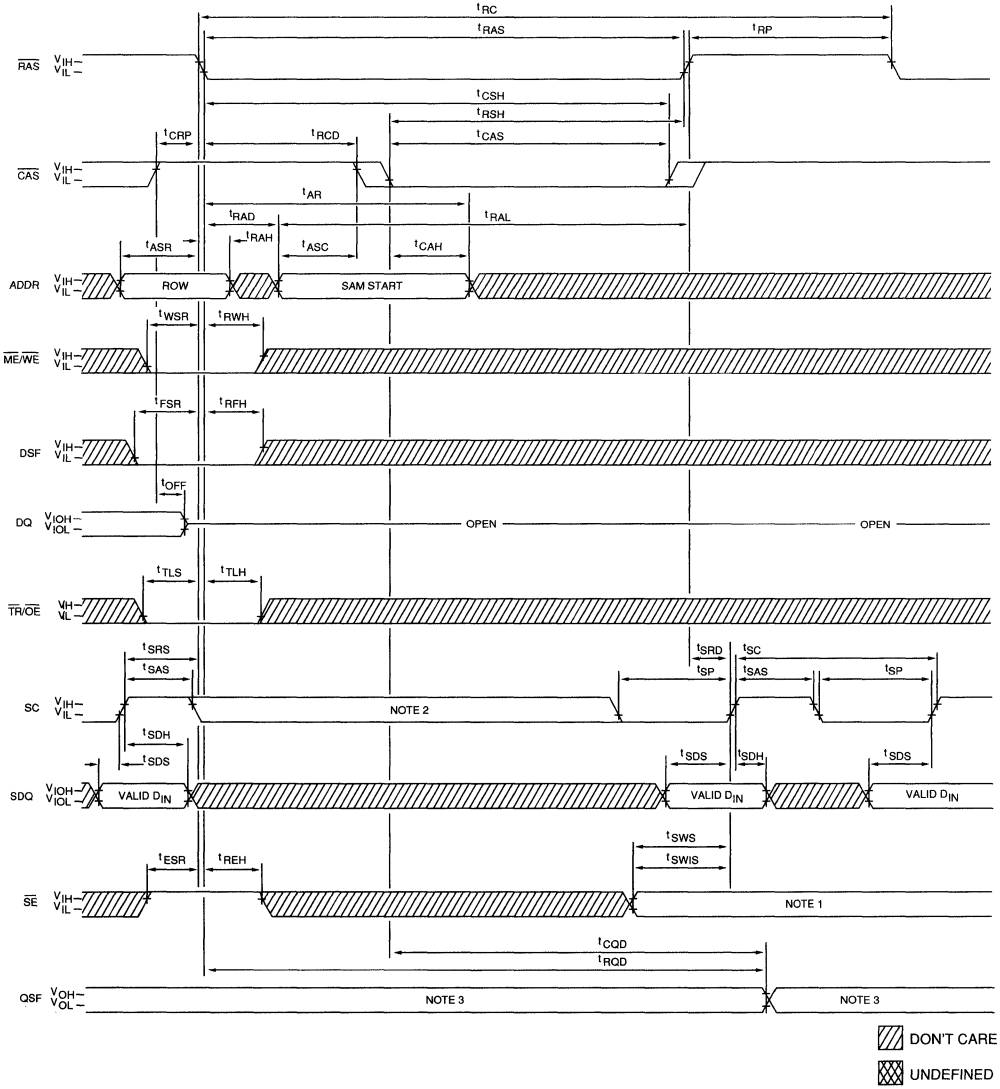
(When part was previously in the SERIAL OUTPUT mode)



NOTE:

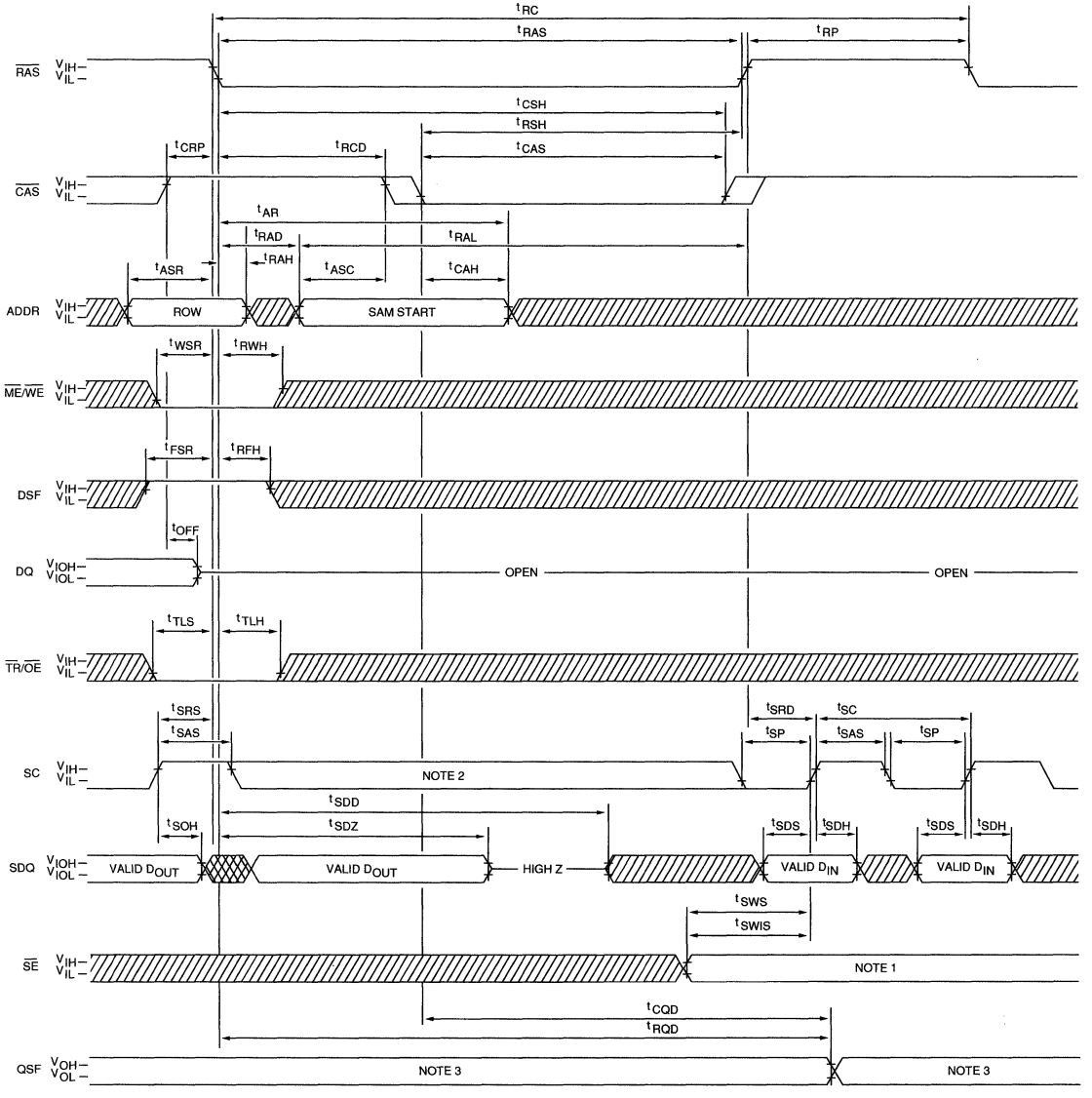
1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
   If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL-INPUT-MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of the state of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



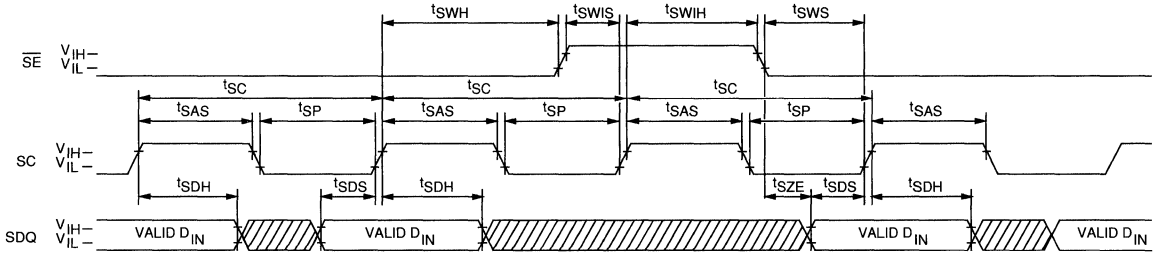
NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

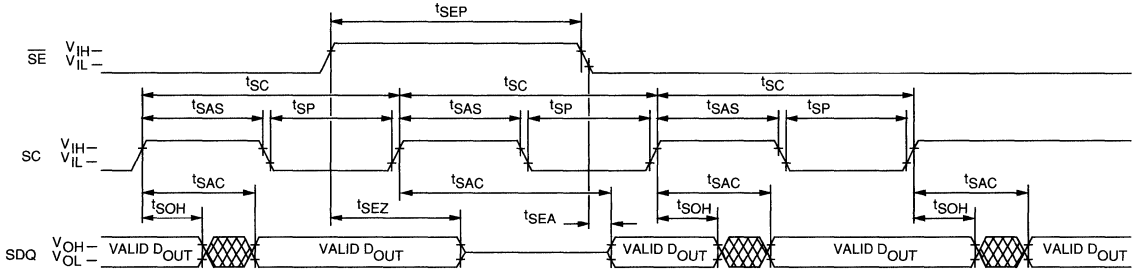


NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of the state of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



DON'T CARE

UNDEFINED

VRAM

256K x 4 DRAM WITH 512 x 4 SAM

FEATURES

- Industry standard pinout, timing and functions
- High-performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 256K x 4 DRAM port
  512 x 4 SAM port
- No refresh required for Serial Access Memory
- Low power: 15mW standby; 275mW active, typical
- Fast access times – 80ns random, 25ns serial

SPECIAL FUNCTIONS

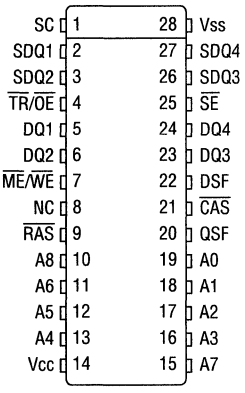
- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER
- BLOCK WRITE

OPTIONS / MARKING

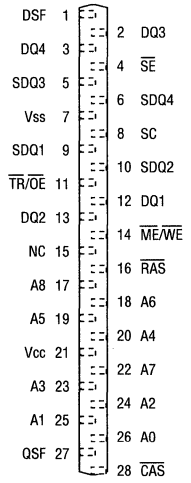
• Timing (DRAM, SAM)	
80ns, 25ns	- 8
100ns, 30ns	-10
120ns, 35ns	-12
• Packages	
Plastic SOJ	DJ
Plastic ZIP	Z

PIN ASSIGNMENT (Top View)

28-Pin SOJ
(E-9)



28-Pin ZIP
(C-5)



GENERAL DESCRIPTION

The MT42C4256 is a high-speed, dual port CMOS dynamic random access memory or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed by a 4-bit wide DRAM port or by a 512 x 4-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4 DRAM). Four 512-bit data registers make up the SAM portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths; the 4-bit random access I/O port, the four internal 512 bit wide paths between the DRAM and the SAM, and the 4-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C4256 is compatible with (and can be identical to) the operation of the MT42C4064 (64K x 4 VRAM). However, the MT42C4256 offers several additional functions that may be used to increase system performance or ease critical timing requirements. These "special functions" are described in detail in the following sections.

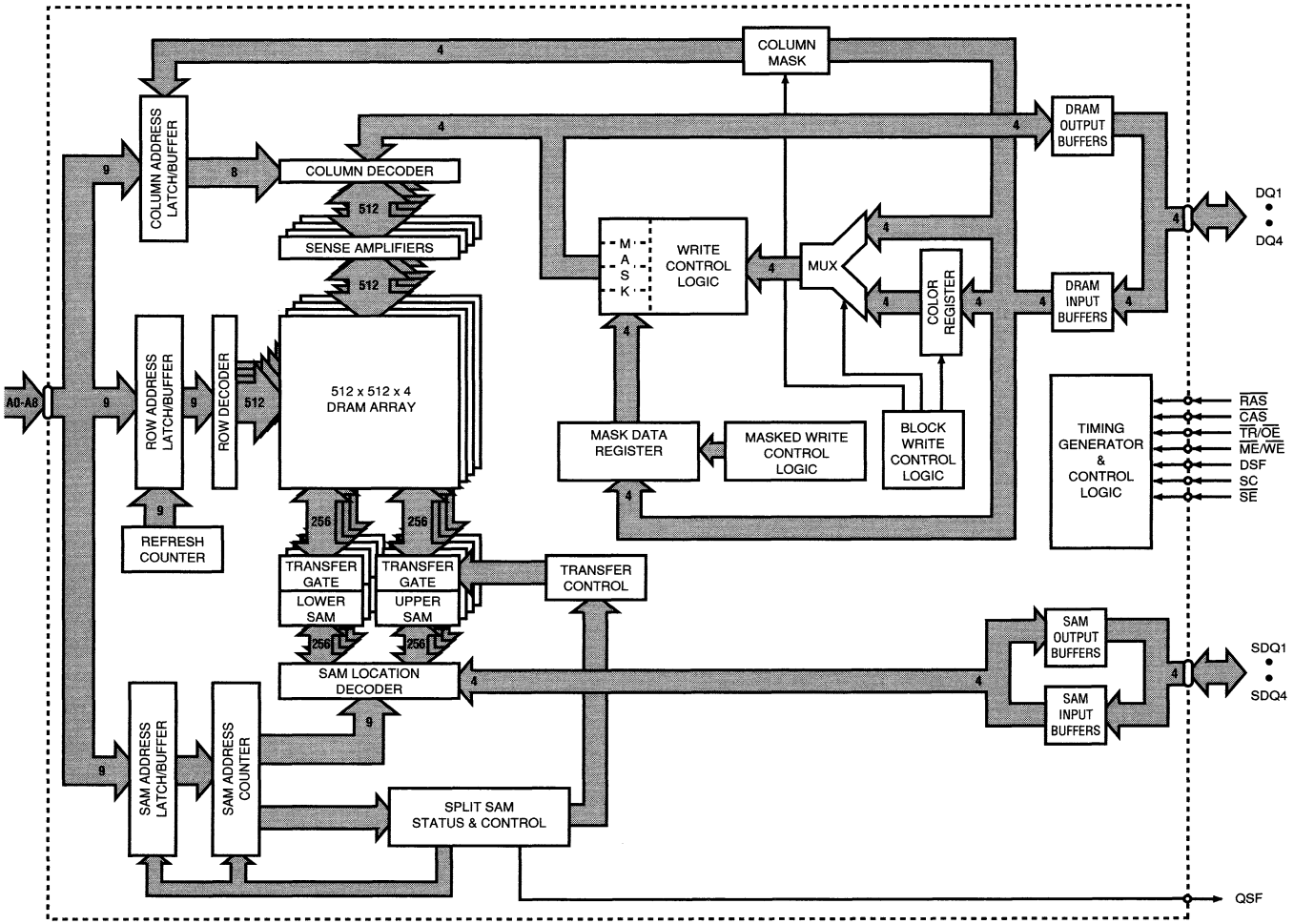


Figure 1
MT42C4256 BLOCK DIAGRAM

PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	8	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
4	11	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a High-Z state.
7	14	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
25	4	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state. $\overline{SE}$ is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
22	1	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used on a particular access cycle.
9	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and as a strobe for the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs.
21	28	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 9 column-address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and as a strobe for the DSF input.
19, 18, 17, 16, 13, 12, 11, 15, 10	26, 25, 24, 23, 20, 19, 18, 22, 17	A0 to A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 4-bit word out of the 256K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW).
5, 6, 23, 24	12, 13, 2, 3	DQ1 - DQ4	Input/ Output	DRAM Data I/O: DRAM input/Output for DRAM cycles; inputs for Mask Data Register and Color Register load cycles, and Bit and Column Mask inputs for BLOCK WRITE.
2, 3, 26, 27	9, 10, 5, 6	SDQ1 - SDQ4	Input/ Output	Serial Data I/O: Input, output, or High-Z.
20	27	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
8	15	NC	–	No Connect: This pin should be left either unconnected or tied to ground.
14	21	V_{CC}	Supply	Power Supply: +5V ±10%
28	7	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C4256 may be divided into three functional blocks (see Figure 1): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C4256 VRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C4256 supports $\overline{CAS}$-BEFORE-$\overline{RAS}$, $\overline{RAS}$-ONLY and HIDDEN types of refresh cycles.

For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for $\overline{RAS}$-ONLY refresh cycles. The DQ pins remain in a High-Z state for both the $\overline{RAS}$-ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycles.

HIDDEN REFRESH cycles are performed by toggling $\overline{RAS}$ (and keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C4256 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has several special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select a 4-bit word from the 262,144 available are latched into the chip using the A0-A8, $\overline{RAS}$ and $\overline{CAS}$ inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 9 column address bits are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH to LOW.

For single port DRAMS, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. However, for the VRAM, when $\overline{RAS}$ goes LOW, $(\overline{TR})/\overline{OE}$ selects between DRAM access or TRANSFER cycles. $(\overline{TR})/\overline{OE}$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition for all DRAM operations (except $\overline{CAS}$-BEFORE-$\overline{RAS}$).

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH to LOW sometime after $\overline{RAS}$ falls to enable the DRAM output port.

For single port normal DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $\overline{ME}/(\overline{WE})$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW before $\overline{CAS}$ goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells. If $(\overline{ME})/\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

NON PERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only specific bits within a 4-bit word. The MT42C4256 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH to LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is nonpersistent (must be re-entered at every $\overline{RAS}$ cycle) if DSF is LOW when $\overline{RAS}$ goes LOW. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle. An example NON PERSISTENT MASKED WRITE cycle is shown in Figure 2.

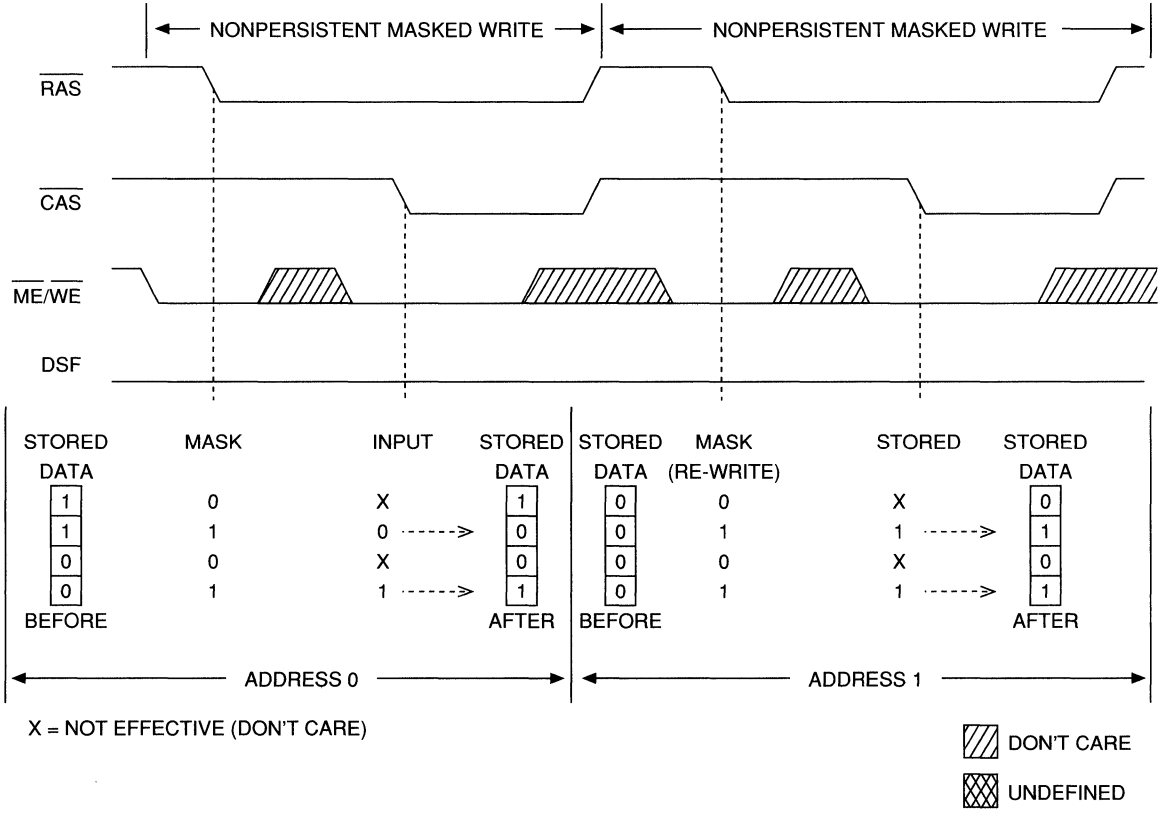


Figure 2
NONPERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW. Mask data may also be loaded into the mask register by performing a NONPERSISTENT MASKED WRITE cycle before the PERSISTENT MASKED WRITE cycles.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls, and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITE cycles, to any address, may be performed without having to reload the mask data register. Figure 3 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot provide mask data to the DQ pins at $\overline{RAS}$ time to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations may be performed during FAST PAGE MODE cycles and the same mask will apply to all addressed columns in the addressed row.

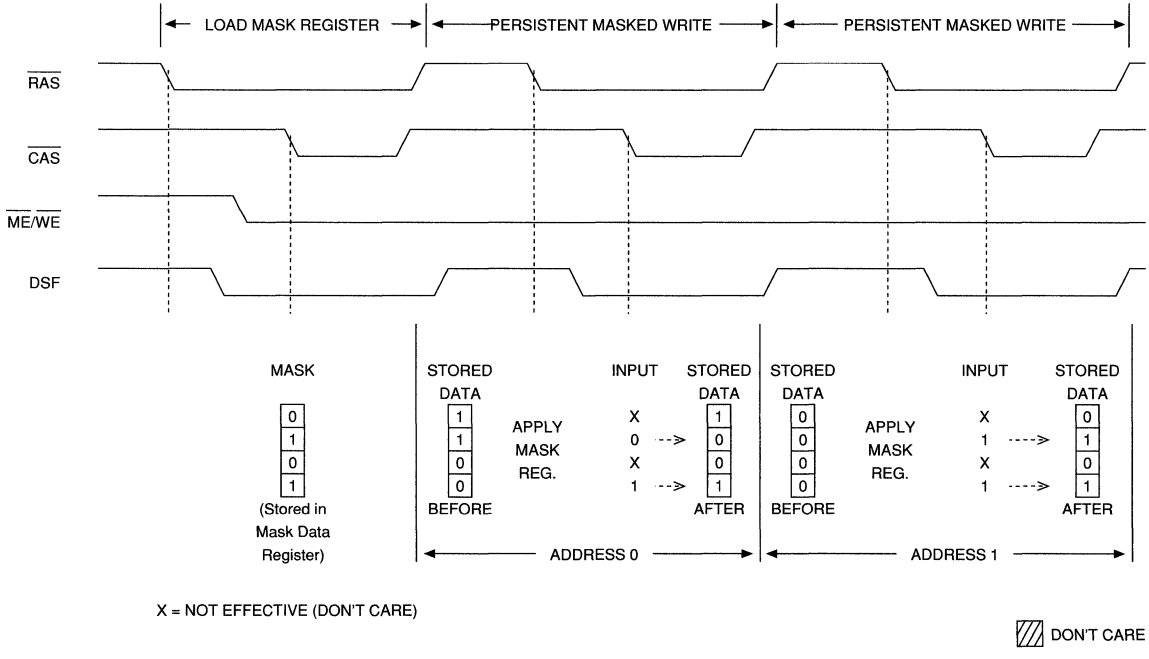


Figure 3
PERSISTENT MASKED WRITE EXAMPLE

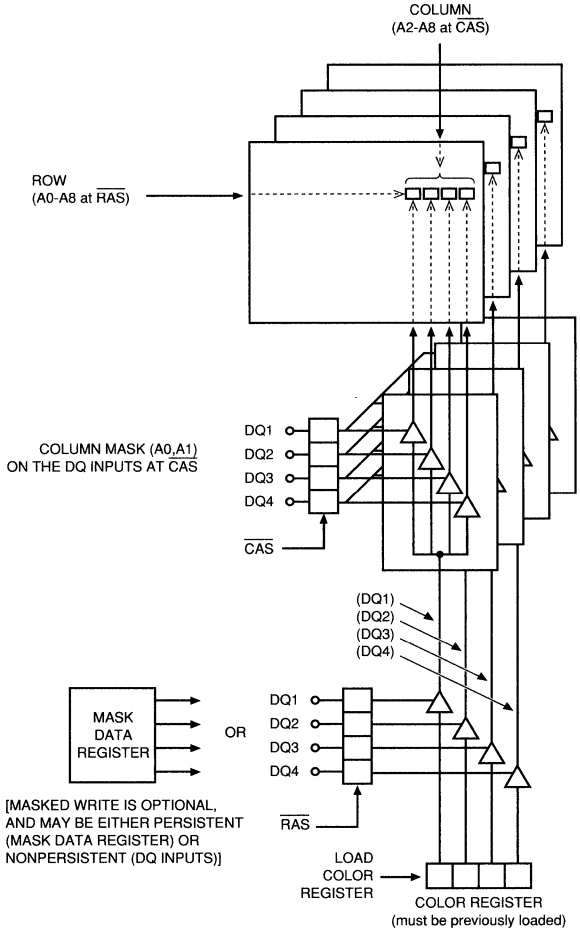


Figure 4
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C4256 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 4). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle, however when $\overline{CAS}$ goes LOW only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs are then used to determine what combination of the four column locations will be changed. DQ1 acts as a write enable for column location A0=0, A1=0; DQ2 controls column location A0=1, A1=0; DQ3 controls A0=0, A1=1; and DQ4 controls A0=1, A1=1. The write enable controls are active HIGH; a logic 1 enables and a logic 0 disables the WRITE function.

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

NONPERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a NONPERSISTENT MASKED cycle. The DSF pin must be driven HIGH when $\overline{CAS}$ goes LOW, to perform the NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes may be masked and any combination of the four column locations may be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}$/($\overline{OE}$), $\overline{ME}$/($\overline{WE}$), and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NONPERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed.

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the four DQ planes.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the four 512-bit DRAM row planes that are to be transferred to the four SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished two ways. If the transfer is to be synchronized with SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW (refer to the AC Timing Diagrams). The 2048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 9-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 255), and HIGH if access is from the upper half (256 through 511). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

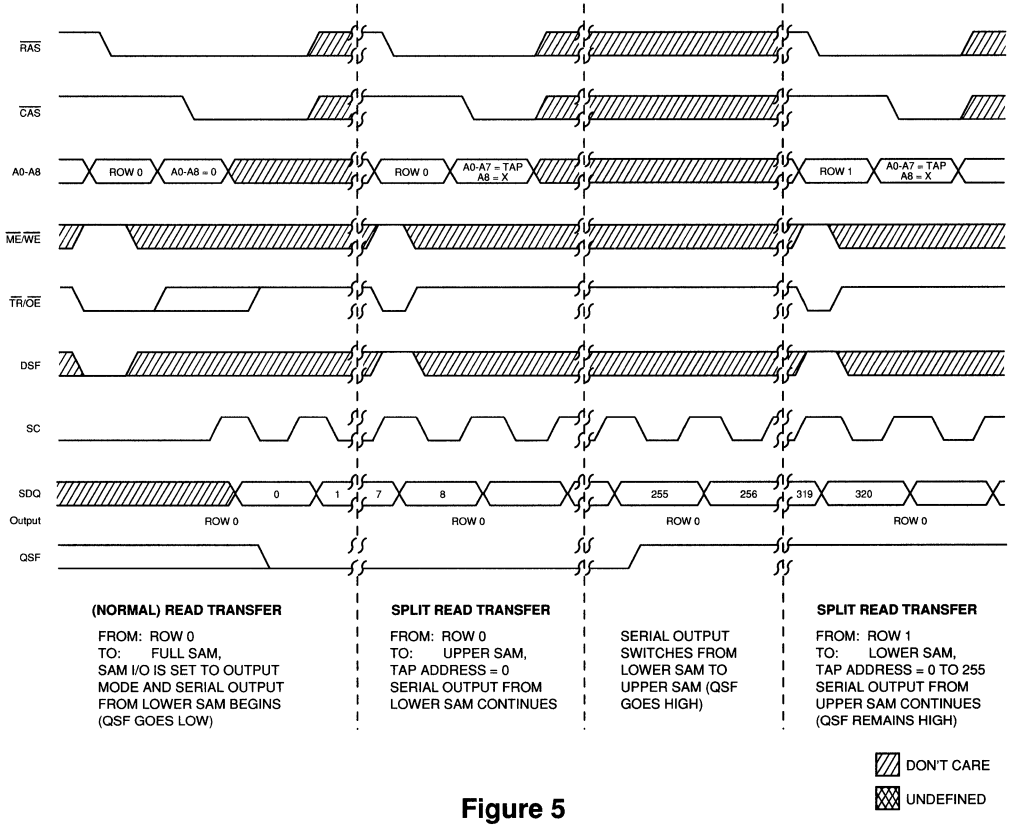


Figure 5
TYPICAL SPLIT READ TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data can be transferred to the other half. The transfer can occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles. A SPLIT READ TRANSFER does not change the direction of the SAM port.

A normal, non-split READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles to provide a reference to which half of the SAM the access will begin and set SAM I/O direction. Then SPLIT READ TRANSFERS may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in non split transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH to LOW transition of $\overline{CAS}$. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 5 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The purpose of the SPLIT TRANSFER of the same data is to initiate the split SAM operating mode and load the Tap address. Serial access continues, and when the SAM address counter reaches 255 ("A8"=0, A0-A7=1) the new Tap address is loaded for the next half ("A8"=1, A0-A7=Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 5 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transfer the upper half of row 1 to the upper SAM. If the half boundry is reached, before a SRT is done for the next half, a Tap address of "0" will be used. Access will start at 0 if going to the lower half, 256 if going to the upper. See Figure 6.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QFS is LOW if access is to the lower half of the SAM, and HIGH if access isto the upper half.

PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and $(\overline{ME})/\overline{WE}$ is LOW when $\overline{RAS}$ goes LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle.

POWER-UP AND INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 8ms, the MT42C4256 must be initialized.

After Vcc is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. When the device is initialized the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of $(\overline{TR})/\overline{OE}$. The DRAM array will contain random data. QSF will be drawing data.

The SAM portion of the MT42C4256 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQs) will be High-Z, regardless of the state of $\overline{SE}$a,b. The mask and color register will contain random data after power-up.

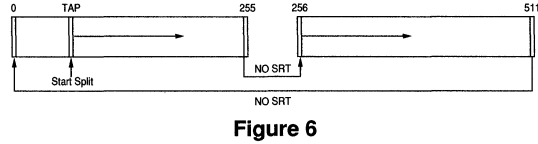


Figure 6
SPLIT SAM TRANSFER

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					CAS FALL	A0 - A8[1]		DQ1 - DQ4[2]		REGISTERS	
		CAS	TR / OE	ME / WE	DSF	SE	DSF	RAS	CAS	RAS	CAS[3] WE	MASK	COLOR
	DRAM OPERATIONS												
CBR	CAS-BEFORE-RAS REFRESH	0	X	1	X	X	X	—	X	—	X	X	X
ROR	RAS-ONLY REFRESH	1	1	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	0	ROW	COLUMN	X	VALID	X	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	X	1	ROW	COLUMN (A2 - A8)	X	COLUMN MASK	X	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	X	1	ROW	COLUMN	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASKED REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	X	1	ROW	COLUMN (A2 - A8)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	1	X	0	ROW[4]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	X	1	ROW[4]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS												
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	X	ROW	TAP[5]	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	X	ROW	TAP[5]	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	X	ROW	TAP[5]	X	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)	1	0	0	0	1	X	ROW[4]	TAP[5]	X	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	X	ROW	TAP[5]	X	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ4 inputs when RAS falls and when CAS falls.
3. On WRITE cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is latched at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. This is the SAM location that the first SC cycle will access. For Split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for lower half, 511 for upper half).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Operating Temperature, Ta(Ambient) .....0°C to +70°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0V)	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		8	pF	2
Input/Output Capacitance: DQ, SDQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $^tRC = {}^tRC$ (MIN))	I_{CC1}	90	80	70	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS} = V_{IL}$; $\overline{CAS}$ = Cycling: $^tPC = {}^tPC$ (MIN))	I_{CC2}	70	60	50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min)	I_{CC3}	10	10	10	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH})	I_{CC4}	90	80	70	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling)	I_{CC5}	80	70	60	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	95	85	75	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $^tRC = {}^tRC$ (MIN))	I_{CC7}	130	120	110	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS} = V_{IL}$; $\overline{CAS}$ = Cycling: $^tPC = {}^tPC$ (MIN))	I_{CC8}	110	100	90	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min)	I_{CC9}	50	45	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH})	I_{CC10}	130	120	110	mA	3, 4
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling)	I_{CC11}	120	110	100	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	135	125	115	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		180		210		ns	
READ-MODIFY-WRITE cycle time	^tRWC	205		235		280		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		55		65		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	100		110		140		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	^tOE		20		25		30	ns	
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		80		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	55	20	70	25	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	12		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	20	60	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	20		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	30	ns	20, 23
Output Disable	^tOD	0	20	0	20	0	30	ns	23
Output Disable hold time from start of write	^tOEH		15		15		20	ns	27
Output Enable to $\overline{RAS}$ delay	^tORD		0		0		0	ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		70		85		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		130		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		80		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		70		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	30		30		30		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	12		15		15		ns	
Mask Data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask Data to $\overline{RAS}$ hold time	^tMH	12		15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER command to $\overline{RAS}$ setup time	^tTLS	0		0		0		ns	25
TRANSFER command to $\overline{RAS}$ hold time	^tTLH	12	10,000	15	10,000	15	10,000	ns	25
TRANSFER command to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	^tRTH	70	10,000	80	10,000	90	10,000	ns	25
TRANSFER command to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	^tCTH	20		25		30		ns	25
TRANSFER command to column address hold time (for REAL-TIME READ TRANSFER only)	^tATH	25		30		35		ns	25
TRANSFER command to SC lead time	^tTSL	5		5		5		ns	25
TRANSFER command to $\overline{RAS}$ lead time	^tTRL	0		0		0		ns	25
TRANSFER command to $\overline{RAS}$ delay time	^tTRD	15		15		15		ns	25
TRANSFER command to $\overline{CAS}$ time	^tTCL	0		0		0		ns	25
TRANSFER command to $\overline{CAS}$ delay time	^tTCD	15		15		15		ns	25
First SC edge to Transfer command delay time	^tTSD	10		10		10		ns	25
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	10	35	10	40	10	50	ns	
SC to $\overline{RAS}$ setup time	^tSRS	30		30		40		ns	
$\overline{RAS}$ to SC delay time	^tSRD	20		25		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		0		ns	
$\overline{RAS}$ to SD buffer turn-on time	^tSRO	10		15		15		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	45		50		55		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	10		15		15		ns	
NONTRANSFER command to $\overline{RAS}$ setup time	^tYS	0		0		0		ns	26
NONTRANSFER command to $\overline{RAS}$ hold time	^tYH	12		15		15		ns	26
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	12		15		15		ns	
SC to QSF delay time	^tSQD		25		30		35	ns	
SPLIT TRANSFER setup time	^tSTS	30		35		40		ns	
SPLIT TRANSFER hold time	^tSTH	30		35		40		ns	
$\overline{RAS}$ to QSF delay time	^tRQD		65		85		105	ns	
DSF to $\overline{RAS}$ hold time	^tFHR	60		65				ns	
DSF to $\overline{CAS}$ Set up time	^tFSC	0		0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		20				ns	
$\overline{TR/OE}$ to QSF delay time	^tTQD		25		30		35	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		35		40		45	ns	
$\overline{RAS}$ to first SC delay	^tRSD	80		95		105		ns	
$\overline{CAS}$ to first SC delay	^tCSD	20		25		35		ns	
Column address valid to first SC delay	^tASD	45		55		65		ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

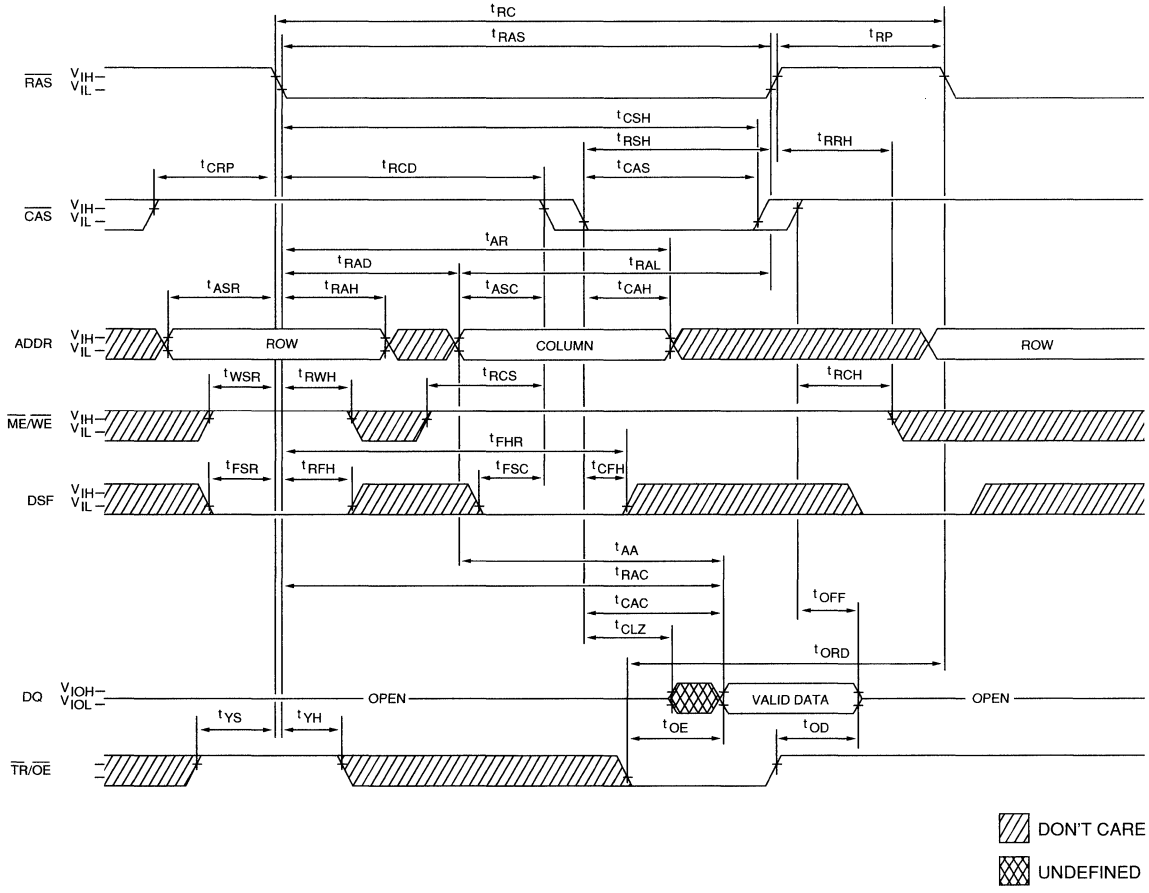
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock-cycle time	^tSC	25		30		35		ns	
Access time from SC	^tSAC		25		25		35	ns	24
SC precharge time (SC LOW time)	^tSP	10		10		12		ns	
SC pulse width (SC HIGH time)	^tSAS	10		10		12		ns	
Access time from $\overline{SE}$	^tSEA		15		20		30	ns	24
$\overline{SE}$ precharge time	^tSEP	10		15		15		ns	
$\overline{SE}$ pulse width	^tSE	10		15		15		ns	
Serial data-out hold time after SC high	^tSOH	5		5		5		ns	24
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	0	12	0	15	0	25	ns	24
Serial data-in setup time	^tSDS	0		0		0		ns	24
Serial data-in hold time	^tSDH	10		15		20		ns	24
Serial input (Write) Enable setup time	^tSWS	0		0		0		ns	
Serial input (Write) Enable hold time	^tSWH	10		15		20		ns	
Serial input (Write) Disable setup time	^tSWIS	0		0		0		ns	
Serial input (Write) Disable hold time	^tSWIH	10		15		20		ns	

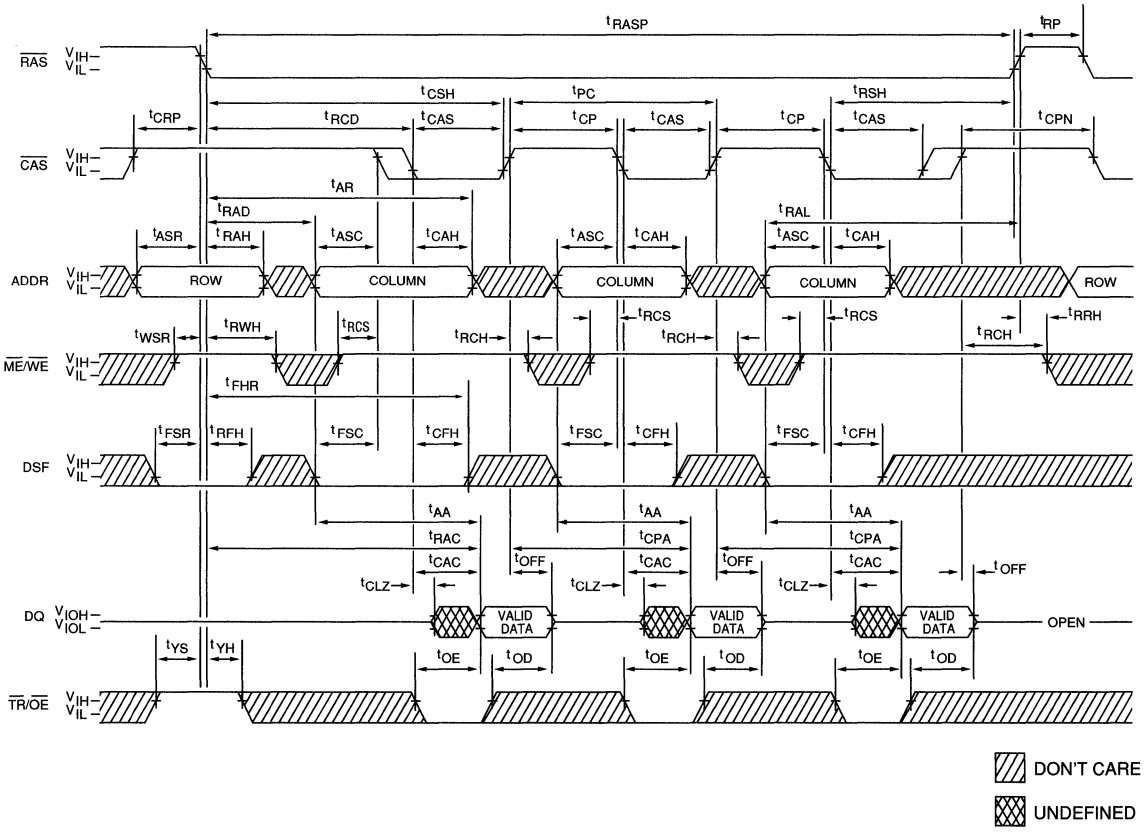
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, DRAM data output (DQ1-DQ4) is high impedance.
12. If $\overline{CAS} = V_{IL}$, DRAM data output (DQ1-DQ4) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF. Output reference levels: $V_{OH} = 2.4V$; $V_{OL} = 0.4V$.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \leq ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 2 TTL gate and 50pF. Output reference levels: $V_{OH} = 2.0V$; $V_{OL} = 0.8V$.
25. Transfer command means that $\overline{TR}/\overline{OE}$ is LOW when $\overline{RAS}$ goes LOW.
26. Non transfer command means that $\overline{TR}/\overline{OE}$ is HIGH when $\overline{RAS}$ goes LOW.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



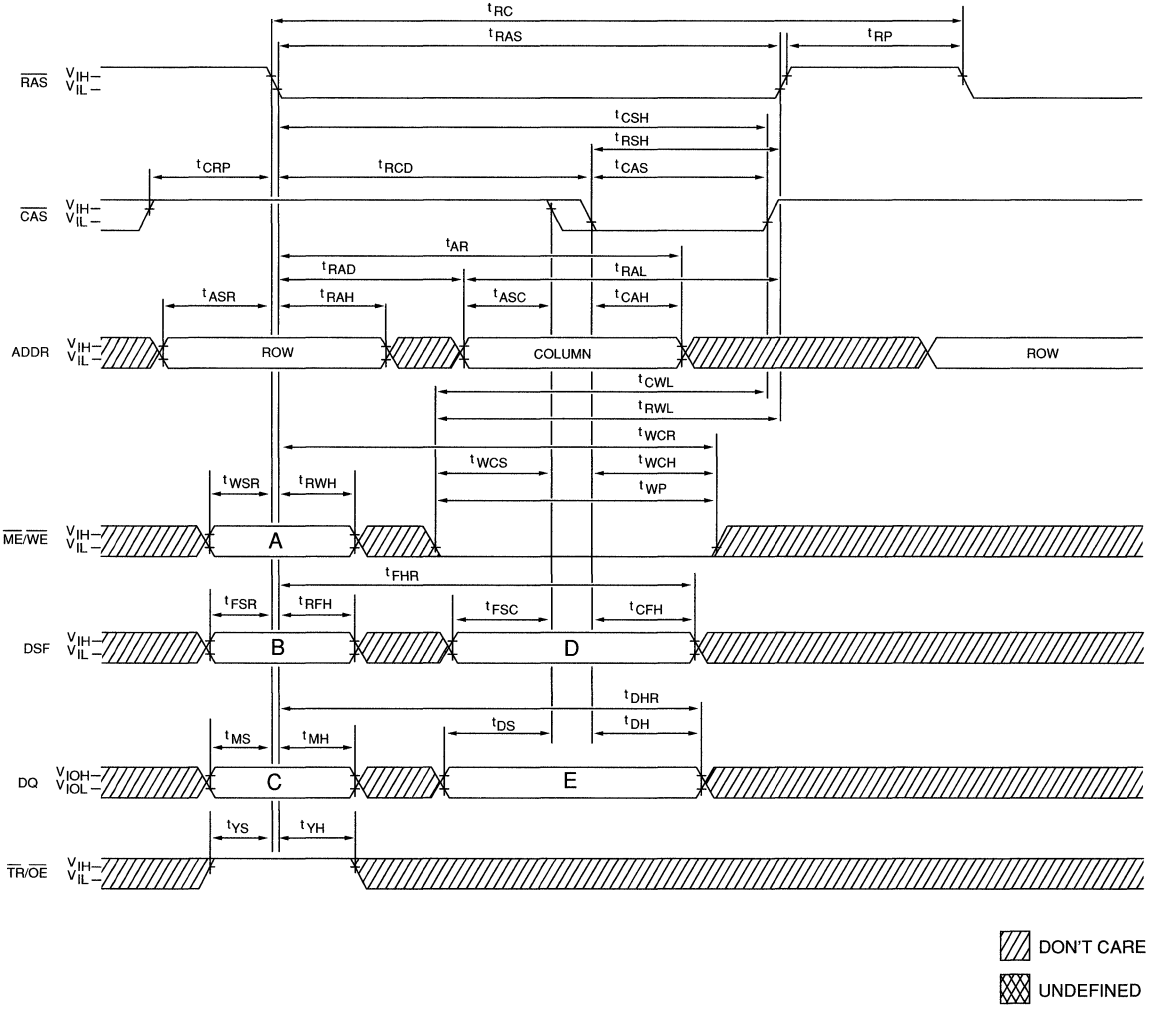
NOTE: 1. WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

WRITE CYCLE FUNCTION TABLE[1]

LOGIC STATES					FUNCTION
$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge		
A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)	
1	0	X	0	DRAM Data	Normal DRAM WRITE (or READ)
0	0	Write Mask	0	DRAM Data (Masked)	NONPERSISTENT (Load and Use) MASKED WRITE to DRAM
0	1	X	0	DRAM Data (Masked)	PERSISTENT (Use Register) MASKED WRITE to DRAM
1	0	X	1	Column Mask	BLOCK WRITE to DRAM (No Data Mask)
0	0	Write Mask	1	Column Mask	NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM
0	1	X	1	Column Mask	PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM
1	1	X	0	Write Mask	Load Mask Register
1	1	X	1	Color Data	Load Color Register

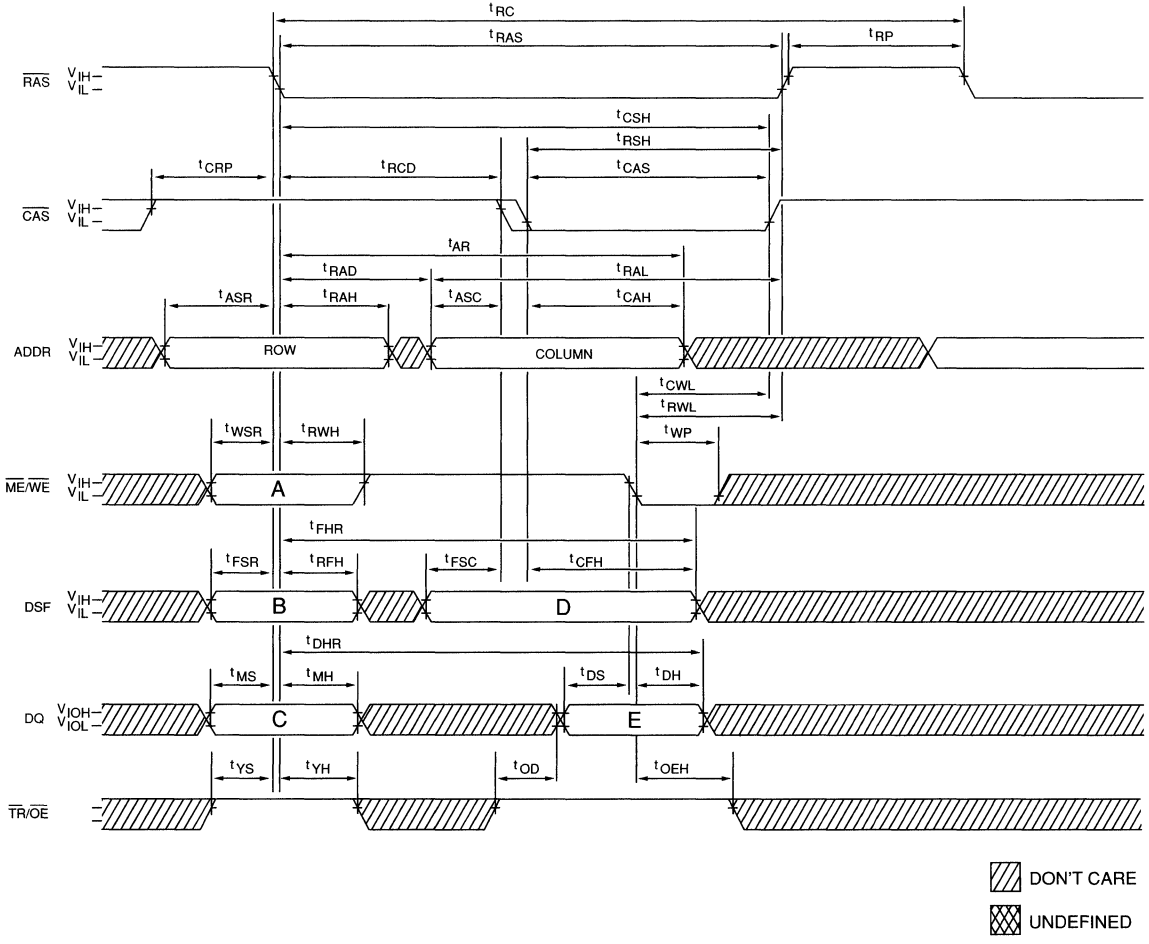
NOTE: 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$, whichever occurs later.

DRAM EARLY-WRITE CYCLE [1]



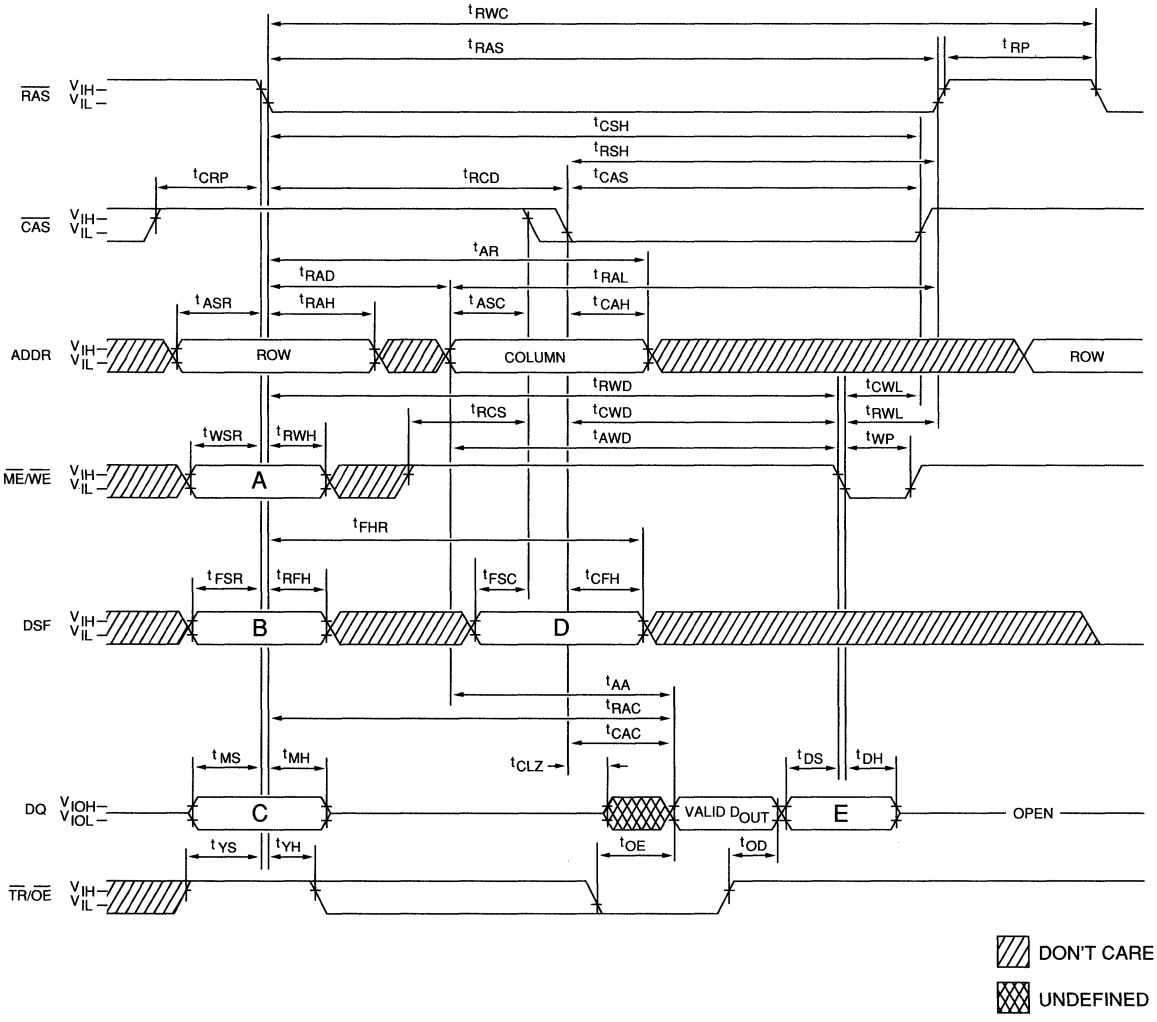
NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE[1]



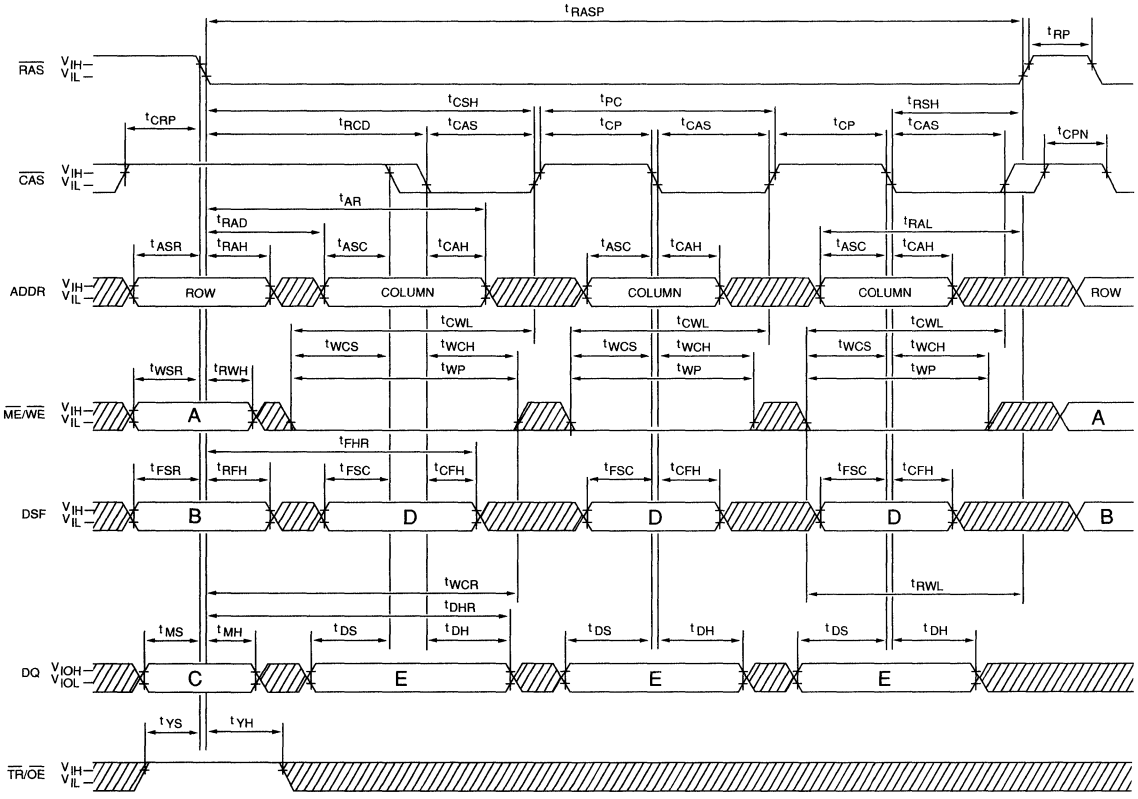
NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



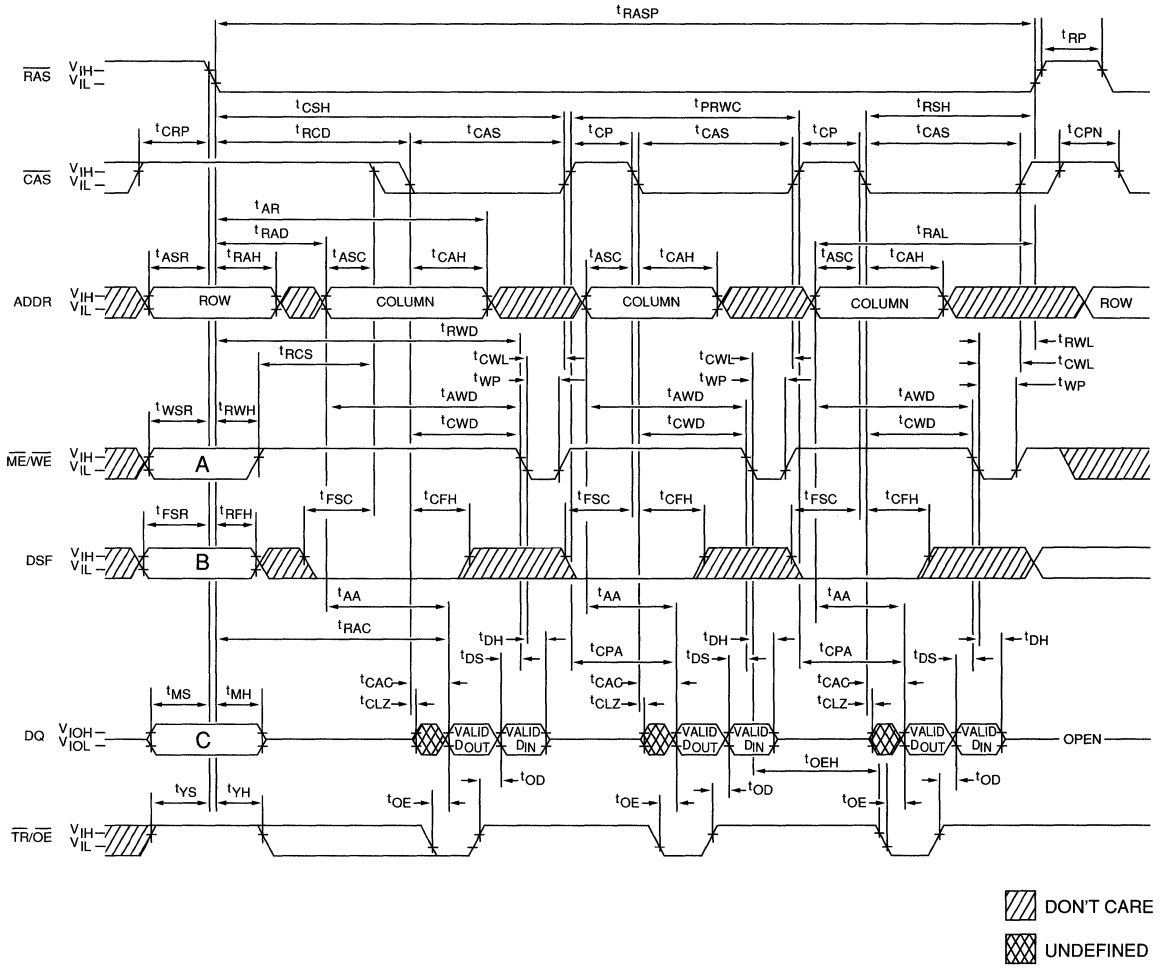
NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

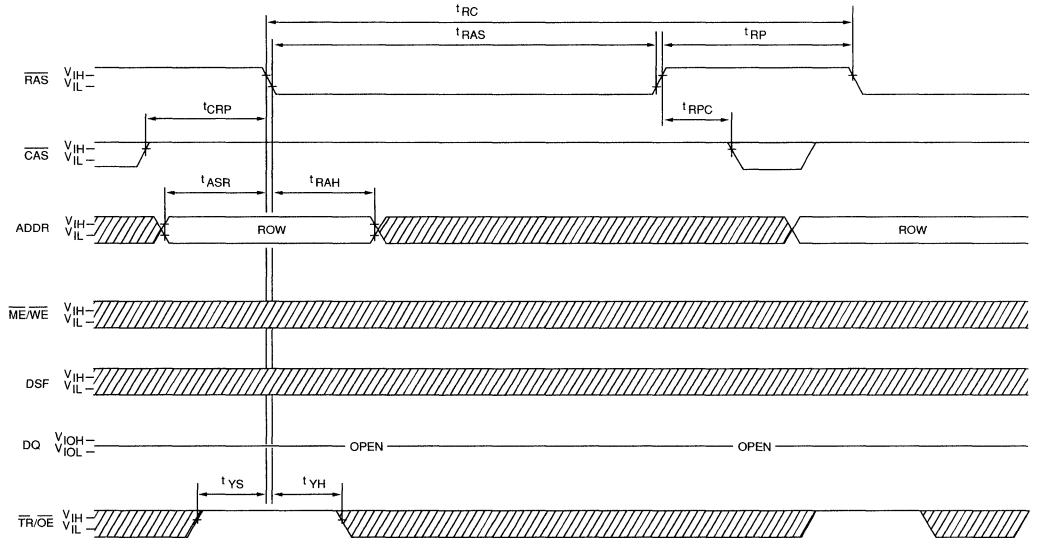
DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



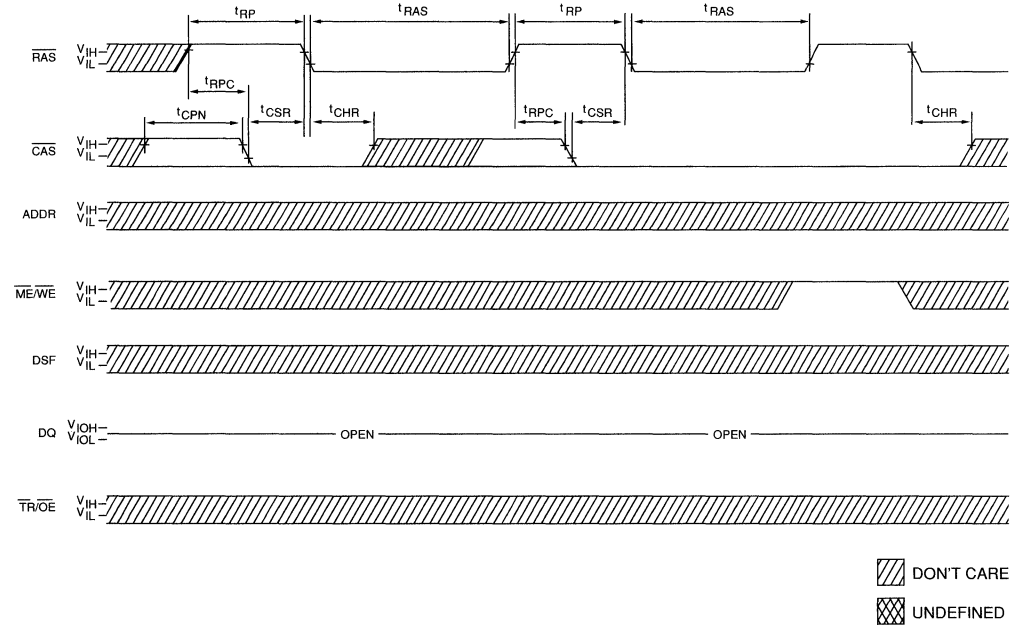
NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE

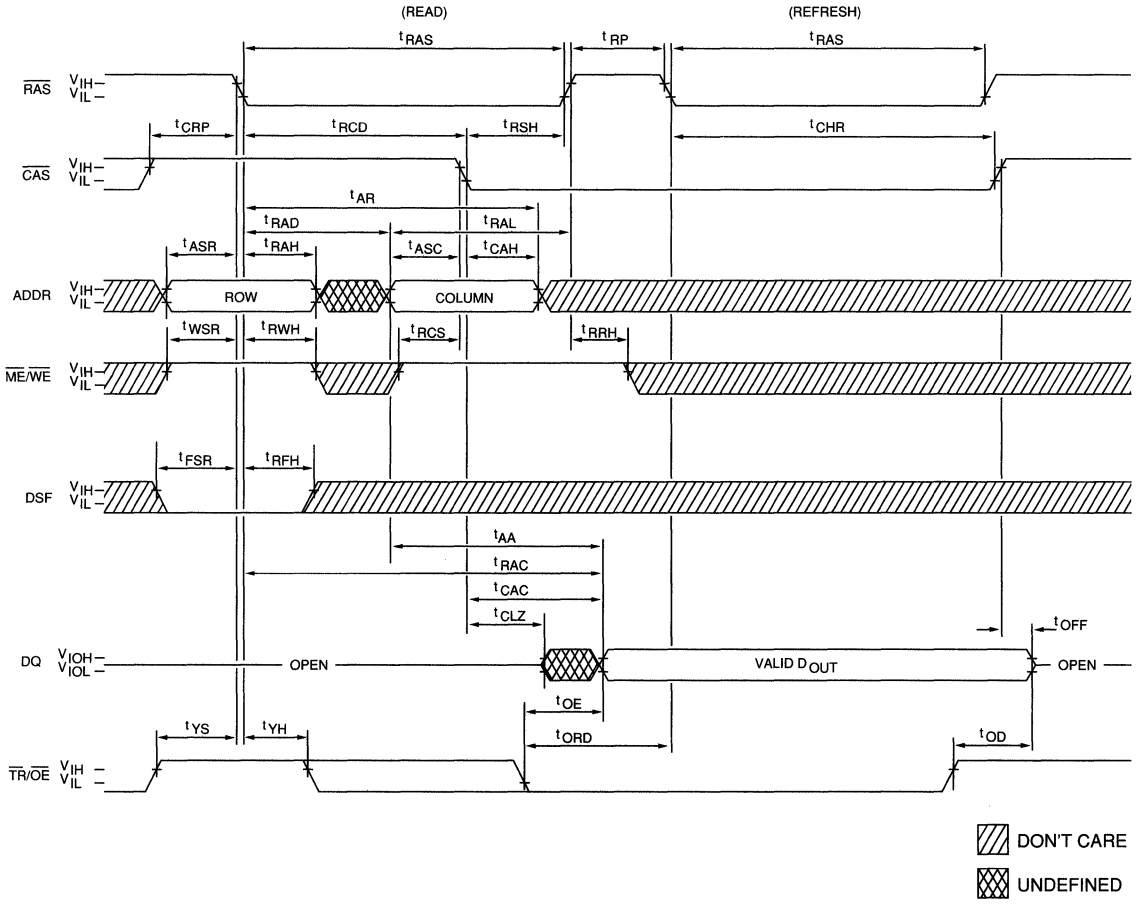
(ADDR = A0-A8)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



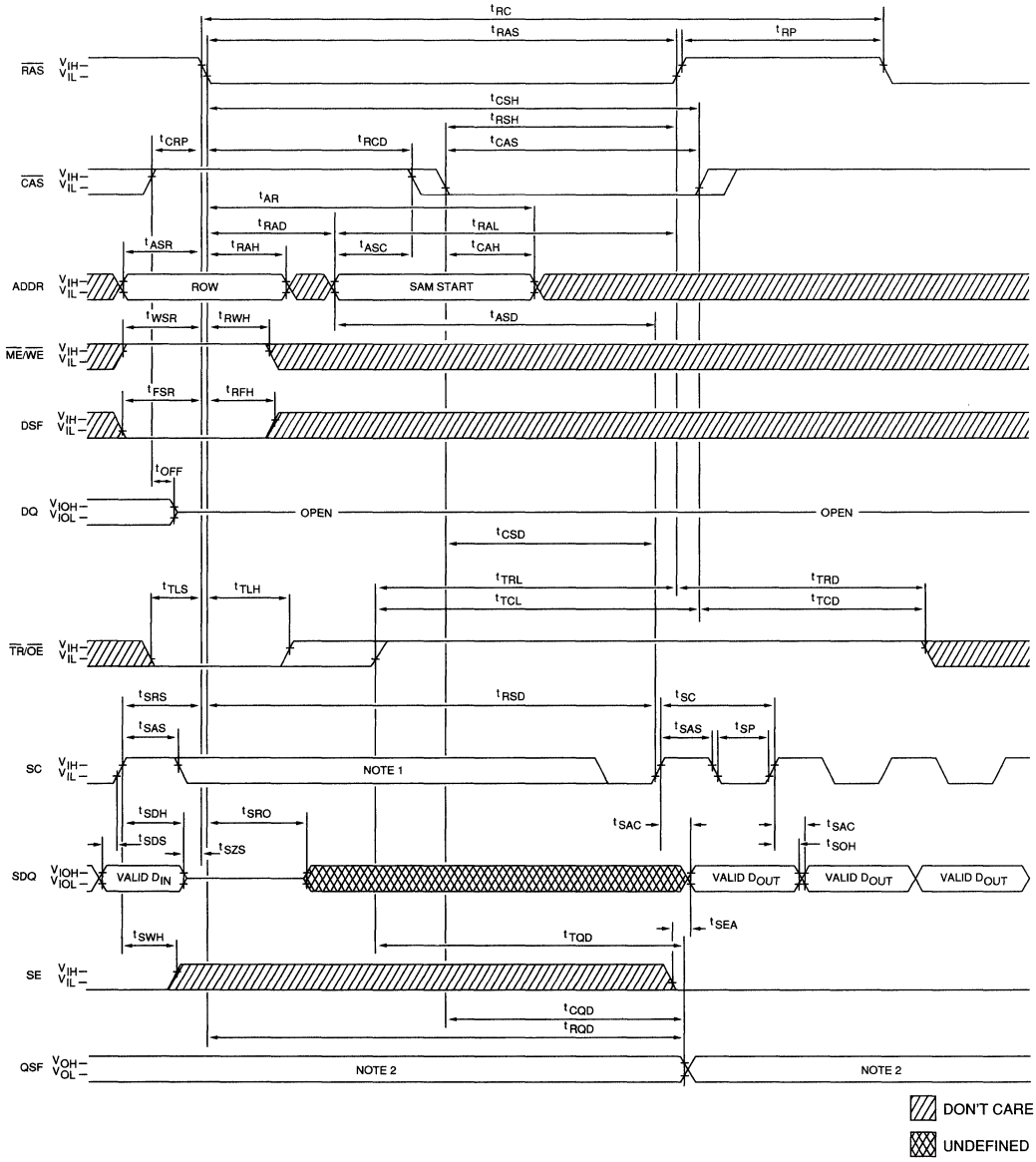
DRAM HIDDEN-REFRESH CYCLE



NOTE: 1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

READ TRANSFER
(DRAM-TO-SAM TRANSFER)

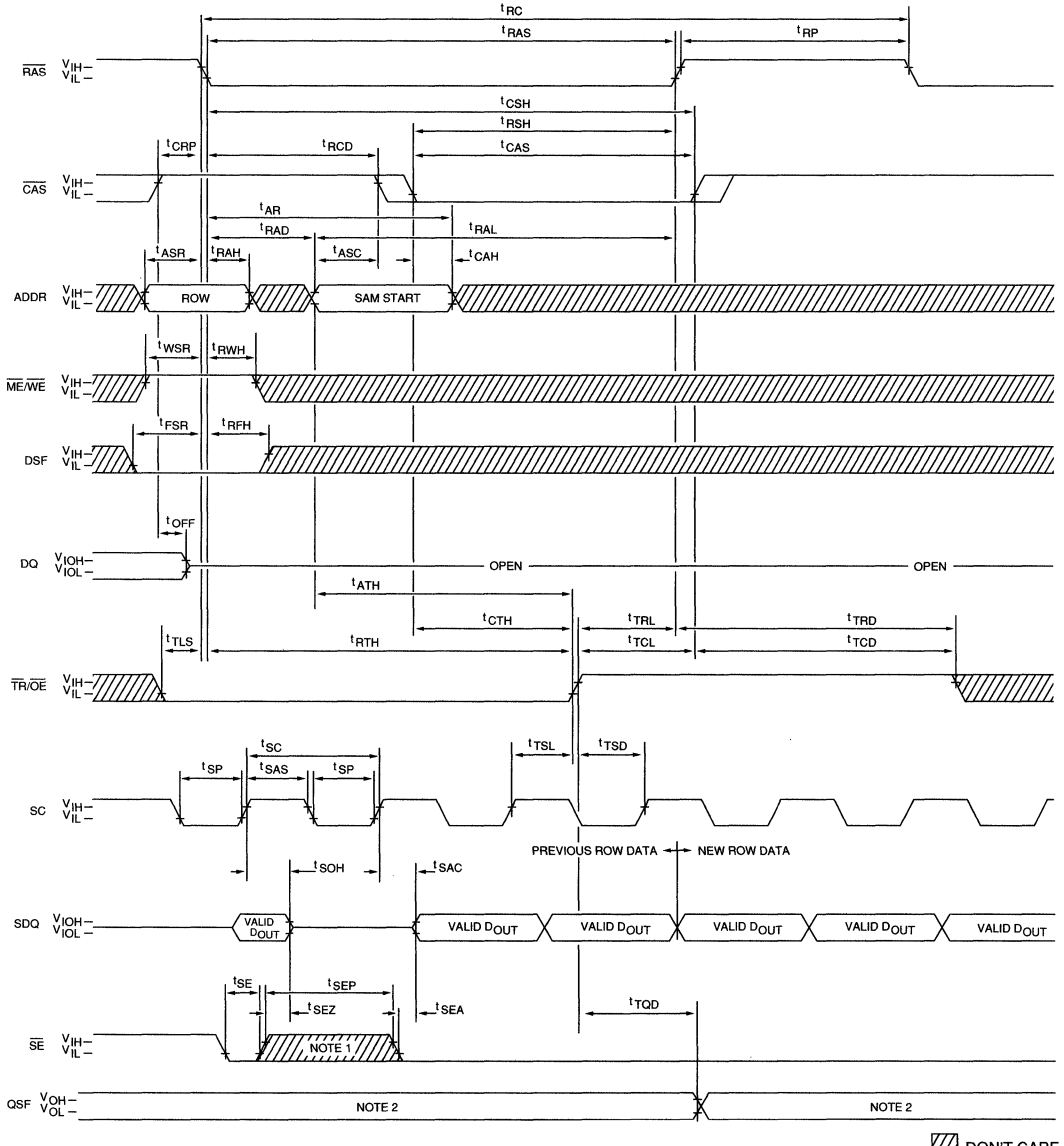
(When part was previously in the SERIAL INPUT mode.)



NOTE: 1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

REAL-TIME READ-TRANSFER (DRAM-TO-SAM TRANSFER)

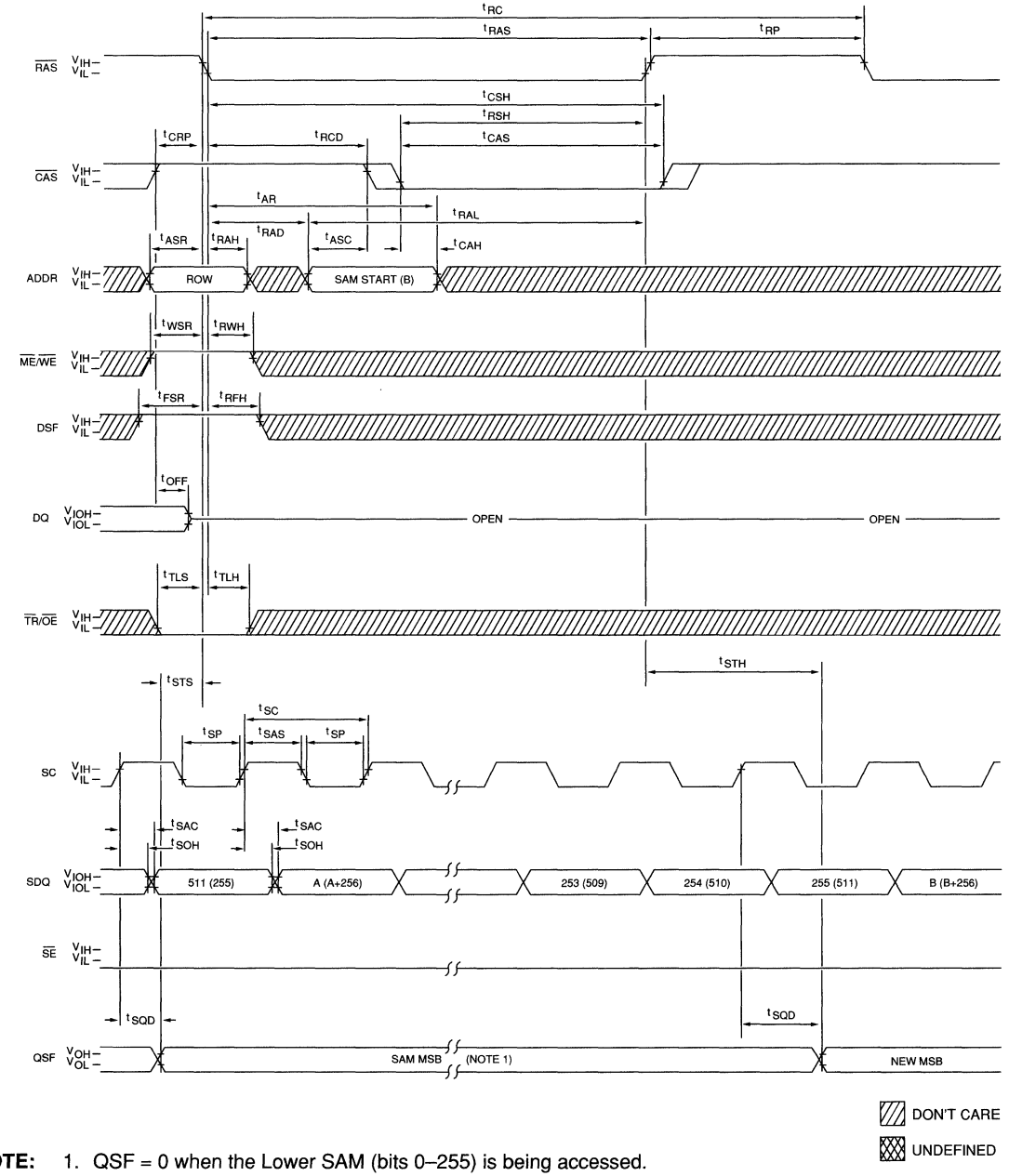
(When part was previously in the SERIAL OUTPUT mode)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

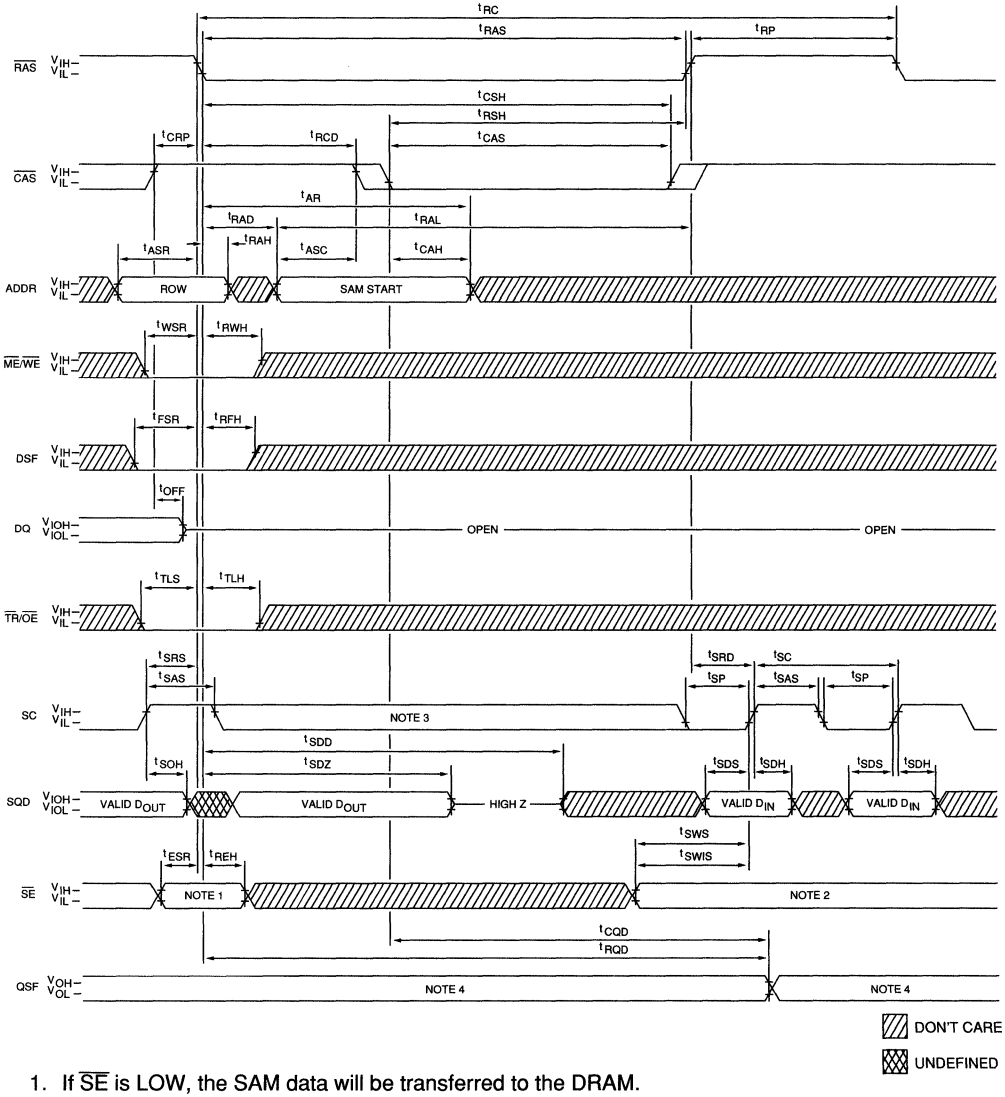
SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

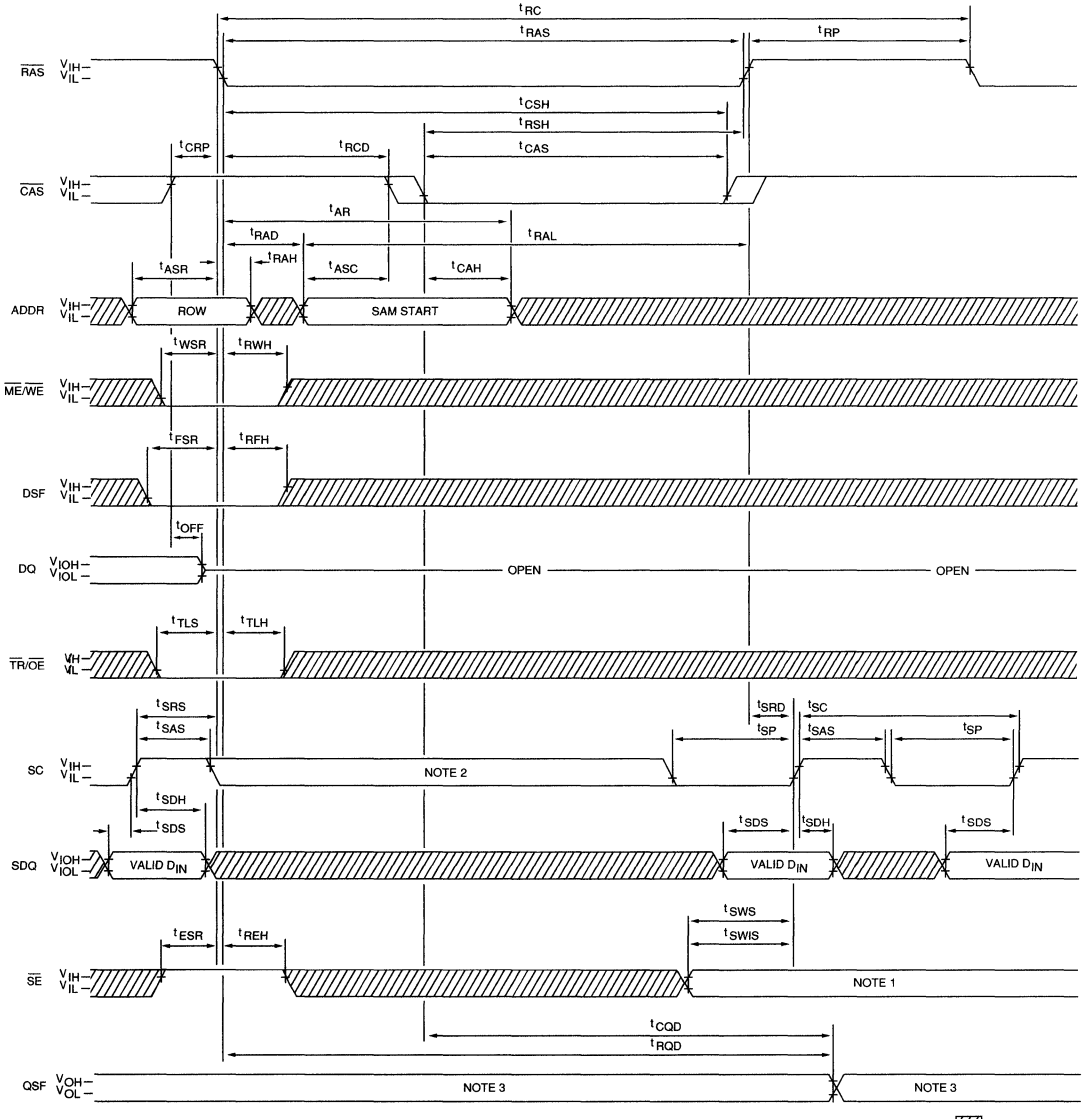
(When part was previously in the SERIAL OUTPUT mode)



NOTE:

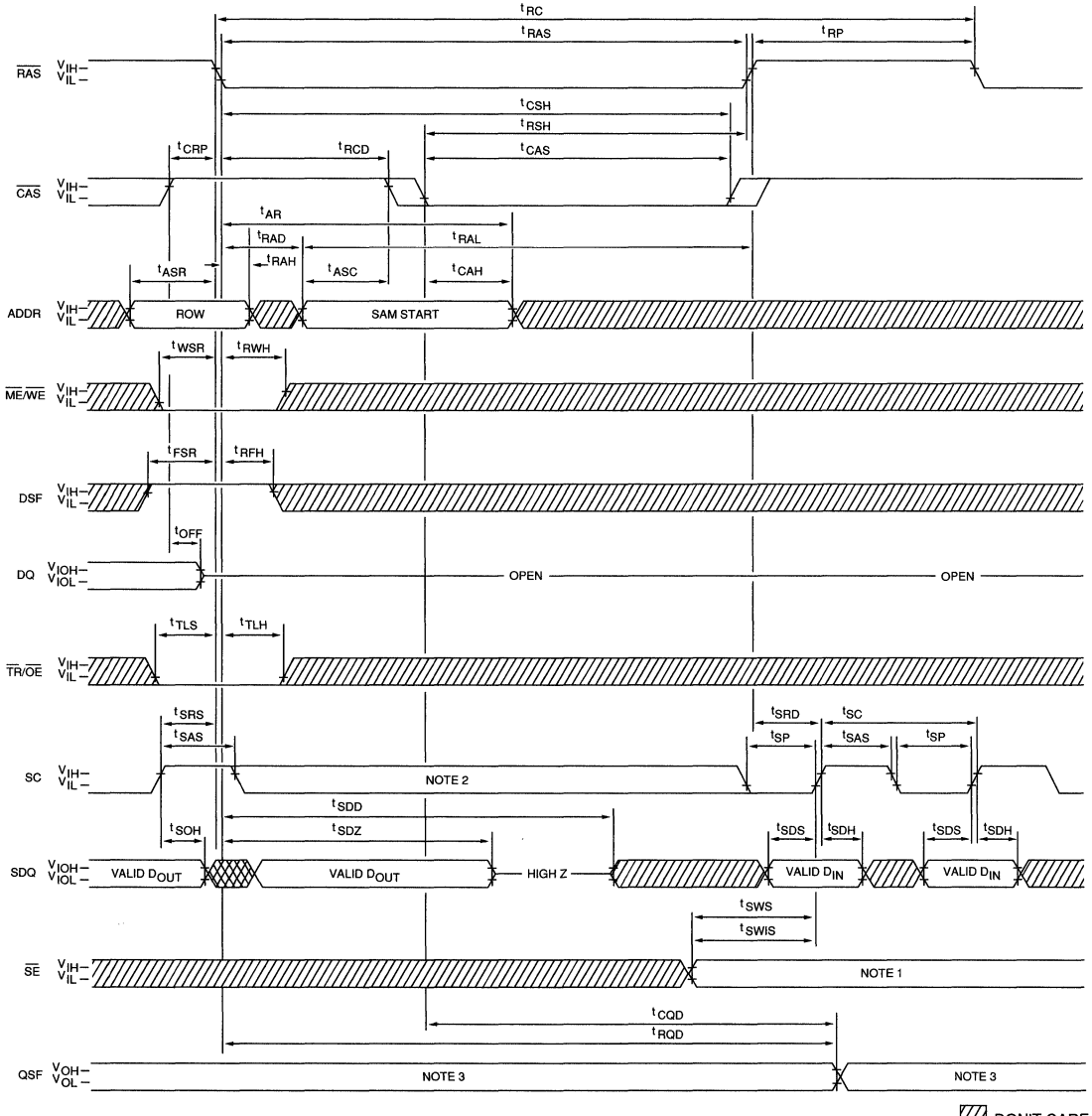
1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
   If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL-INPUT-MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. STS is LOW to select SAMa or HIGH to select SAMb
5. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



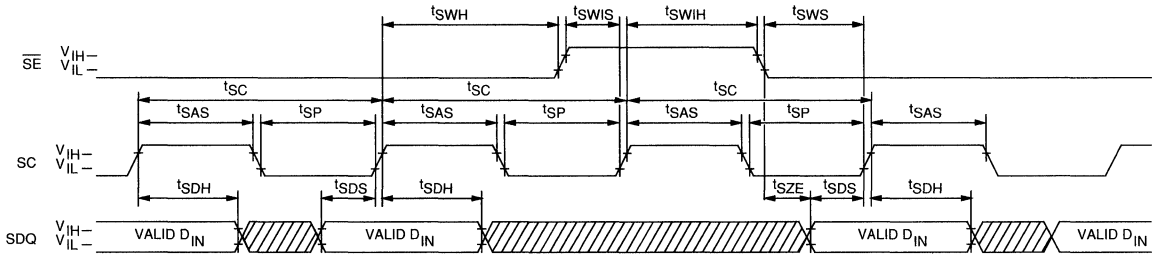
NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

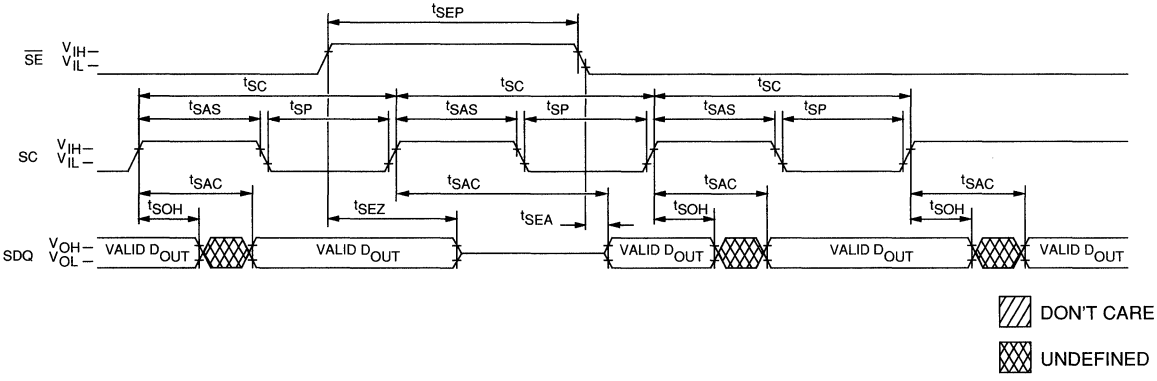


NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



VRAM

128K x 8 DRAM WITH 256 x 8 SAM

FEATURES

- Industry standard pinout, timing and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$, and HIDDEN
- 512-cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 128K x 8 DRAM port
  256 x 8 SAM port
- No refresh required for Serial Access Memory
- Low power: 15mW standby; 275mW active, typical
- Fast access times – 100ns random, 30ns serial

SPECIAL FUNCTIONS

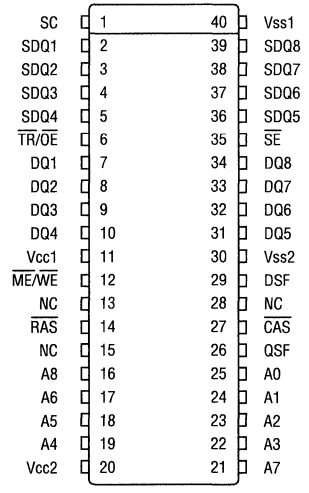
- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER

OPTIONS — MARKING

- Timing (DRAM, SAM)
  100ns, 30ns — -10
  120ns, 35ns — -12
- Packages
  Plastic SOJ — DJ

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(E-12)



GENERAL DESCRIPTION

The MT42C8127 is a high speed, dual port CMOS dynamic random access memory, or Video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed either by an 8-bit wide DRAM port or by a 256 x 8-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4-bit DRAM). Eight 256-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 256 bit wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{\text{RAS}}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C8127 is compatible with (and can be identical to) the operation of the MT42C4064 (64K x 4 VRAM). However, the MT42C8127 offers several additional functions that may be used to increase system performance or ease critical timing requirements. These "special functions" are described in detail in the following sections.

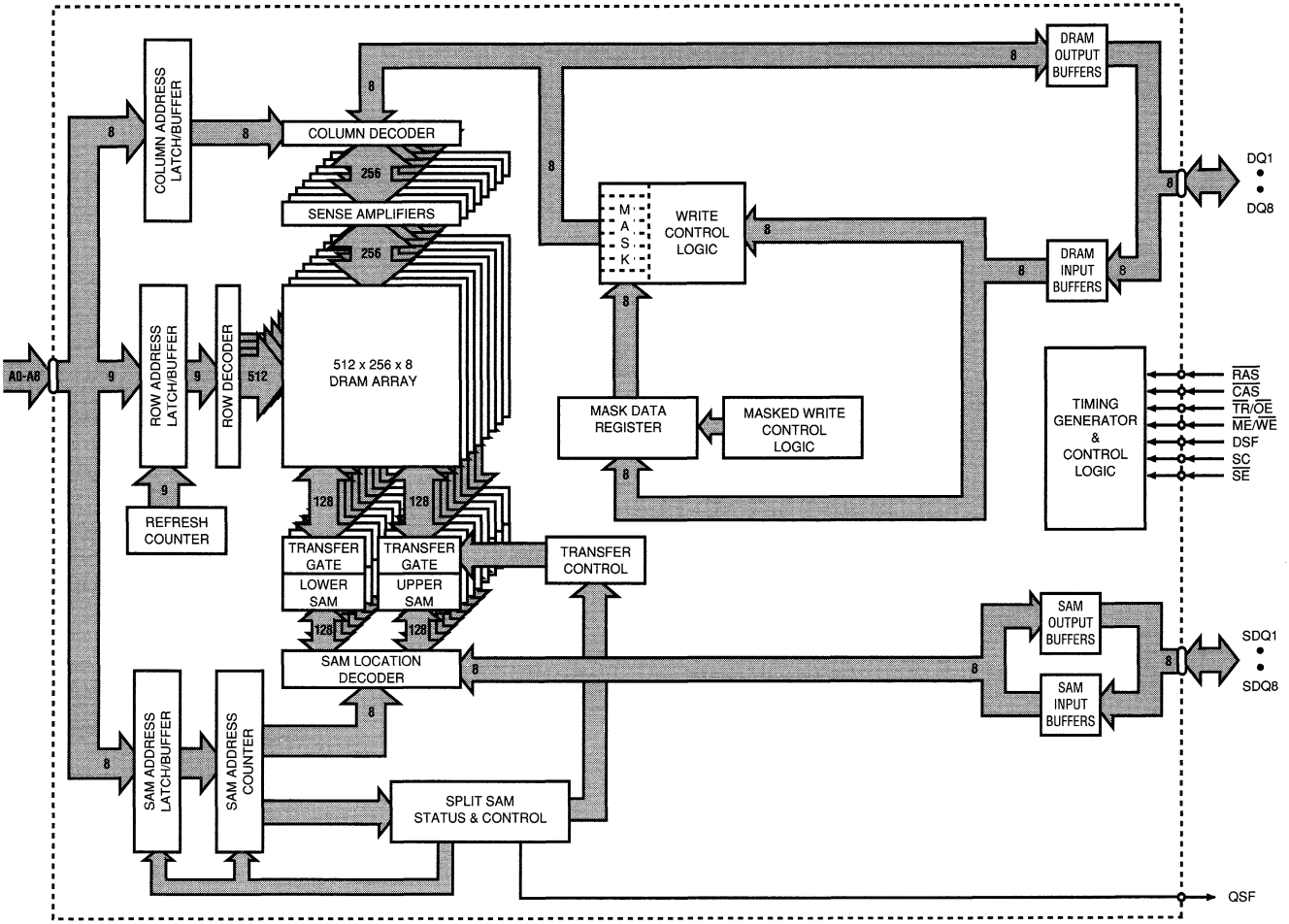


Figure 1
MT42C8127 BLOCK DIAGRAM

PIN DESCRIPTIONS

SOJ PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
6	16	$\overline{TR/OE}$	Input Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in the High-Z state.
12	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
35	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in the High-Z state. $\overline{SE}$ is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a PSEUDO WRITE TRANSFER cycle is performed.
29	DSF	Input	Special Function Select: DSF is used to indicate which special functions (MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used for a particular access cycle.
14	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and as a strobe for the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, and DQ inputs.
27	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 8 column-address bits and enable the DRAM output buffers (DQ's) (along with $\overline{TR/OE}$).
25, 24, 23, 22, 19, 18, 17, 21, 16	A0 to A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 131,072 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A7 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A7, A8 = "don't care" for the start address when doing SPLIT TRANSFERS.
7, 8, 9, 10, 31, 32, 33, 34	DQ1 - DQ8	Input/ Output	DRAM Data I/O: Data Input/Output for DRAM cycles; inputs for the LOAD MASK REGISTER cycles.
2, 3, 4, 5, 36 37, 38, 39	SDQ1 - SDQ8	Input/ Output	Serial Data I/O: Input/Output for SAM access cycles or High-Z, when $\overline{SE}$ = HIGH.
26	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address 0 to 127, HIGH if address 128 to 255.
13, 15, 28	NC	–	No Connect: This pin should be either left unconnected or tied to ground.
11, 20	V_{CC}	Supply	Power Supply: +5V ±10%
30, 40	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8127 can be divided into three functional blocks (see Figure 1): the DRAM, the transfer circuitry, and the serial access memory (SAM). All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations, the TR/OE pin will be shown as TR/(OE).*

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C8127 VRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 8ms. The MT42C8127 supports CAS-BEFORE-RAS, RAS-ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the RAS ONLY and CAS-BEFORE-RAS cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C8127 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has several special functions that can be used when writing to the DRAM.

The 17 address bits that are used to select an 8-bit word from the 131,072 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the 9 row-address bits are set-up on the address inputs and clocked into the part when RAS transitions from HIGH to LOW. Next, the 8 column-address bits are set-up on the address inputs and clocked-in when CAS goes from HIGH to LOW.

For single port DRAMS, the OE pin is a "don't care" when RAS goes LOW. However, for the VRAM, when RAS goes LOW, (TR)/OE selects between DRAM access or TRANSFER cycles. (TR)/OE must be HIGH at the RAS HIGH-to-LOW transition for all DRAM operations (except CAS-BEFORE-RAS).

If (ME)/WE is HIGH when CAS goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ8 port. The (TR)/OE input must transition from HIGH to LOW sometime after RAS falls to enable the DRAM output port.

For single port normal DRAMs, WE is a "don't care" when RAS goes LOW. For the VRAM, ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH to LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells. If (ME)/WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

NONPERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only specific bits within an 8-bit word. The MT42C8127 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register. The mask data acts as an individual WRITE ENABLE for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is non-persistent (must be re-entered at every $\overline{RAS}$ cycle) if DSF is LOW when $\overline{RAS}$ goes LOW. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle. An example NONPERSISTENT MASKED WRITE cycle is shown in Figure 2.

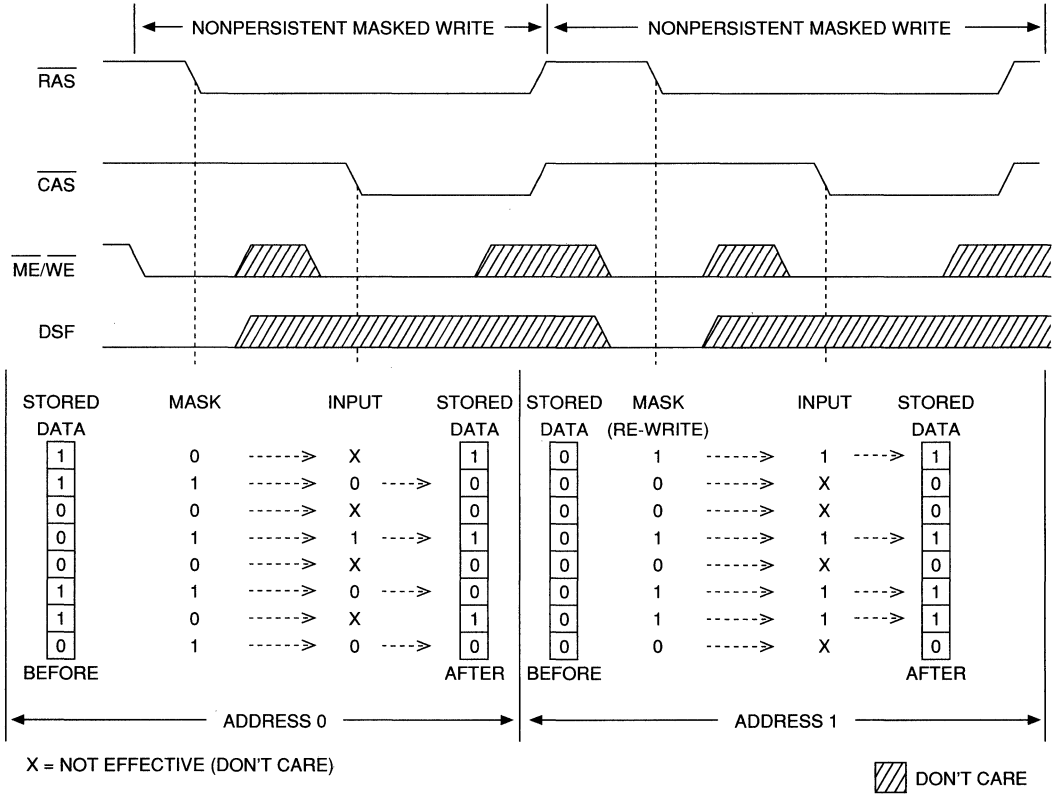


Figure 2
NONPERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW. Mask data may also be loaded into the mask register by performing a NONPERSISTENT MASKED WRITE cycle before the PERSISTENT MASKED WRITE cycles.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITEs, to any address, may be performed without having to reload the mask data register. Figure 3 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers, that cannot provide mask data to the DQ pins at $\overline{RAS}$ time, to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations can be performed during FAST PAGE MODE and the same mask will apply to all addressed columns in the addressed row.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE except that DSF is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a REGISTER load cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NONPERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed.*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE cycles to selectively enable writes to the eight DQ planes.

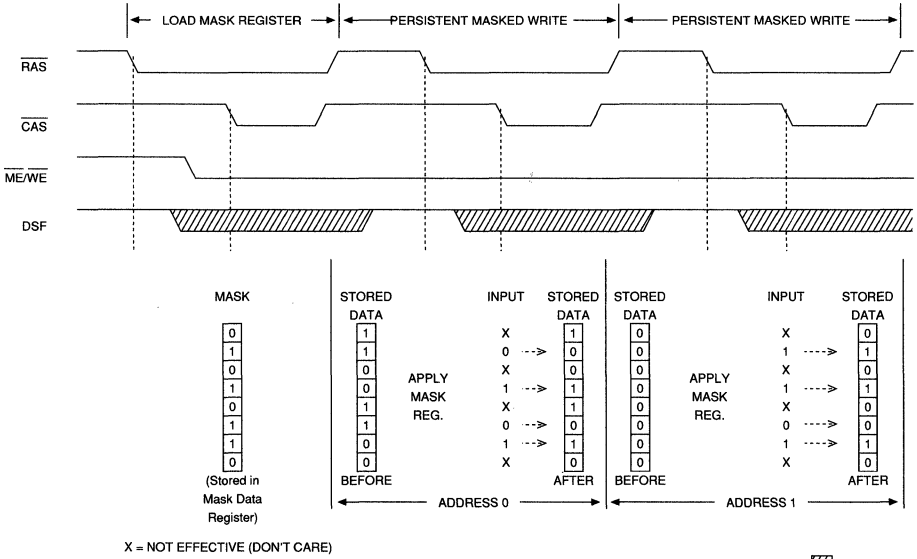


Figure 3
PERSISTENT MASKED WRITE EXAMPLE

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the eight 256-bit DRAM row planes that are to be transferred to the eight SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished two ways. If the transfer is to be synchronized with SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW (refer to the AC Timing Diagrams). The 2048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 8-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 127), and HIGH if access is from the upper half (128 through 255). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW to HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

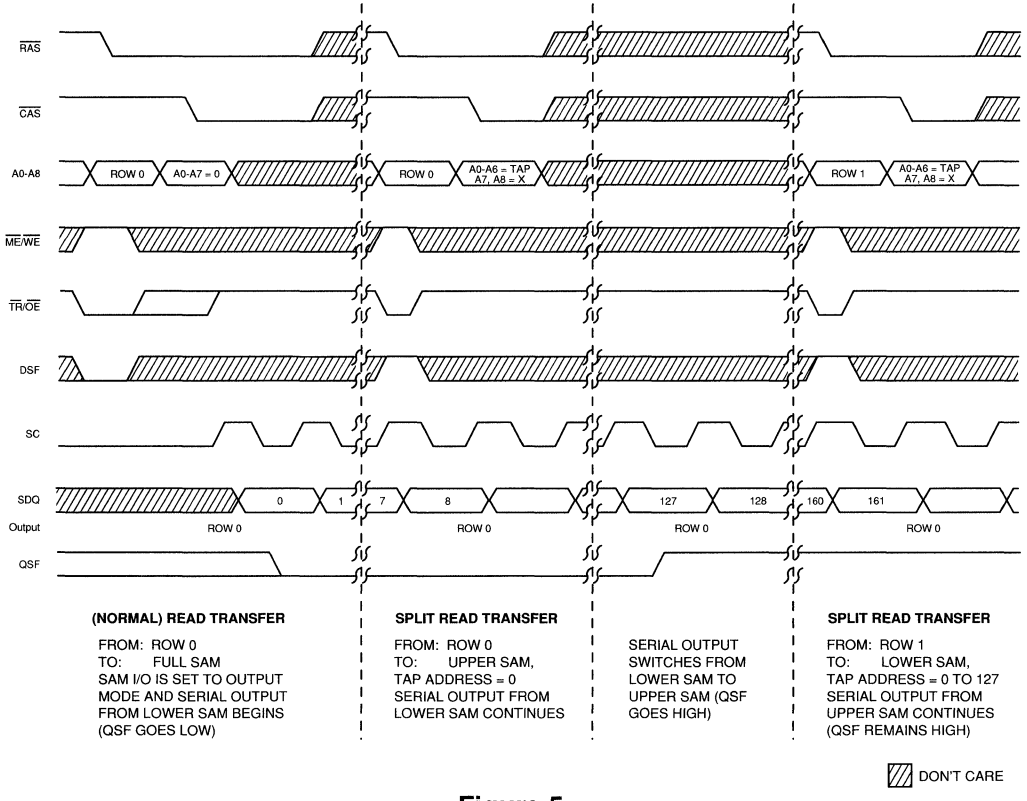


Figure 5
TYPICAL SPLIT READ TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data can be transferred to the other half. The transfer can occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles.

A normal, non-split READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles to provide a reference to which half of the SAM the access will begin. Then SPLIT READ TRANSFERS may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A6, is used to input the SAM Tap address. Address pins A7 and A8 are "don't care" when the Tap address is loaded at the HIGH to LOW transition of $\overline{CAS}$. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 5 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The purpose of the SPLIT TRANSFER of the same data is to initiate the split SAM operating mode and load the Tap address. Serial access continues, and when the SAM address counter reaches 127 ("A7"=0, A0-A6=1) the new Tap address is loaded for the next half ("A7"=1, A0-A6=Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 5 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transfer the upper half of row 1 to the upper SAM.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QSF will indicate the SAM half accessed.

PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of SAM port from output to input without performing a WRITE TRANSFER. A PSEUDO WRITE TRANSFER is a WRITE TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and $(\overline{ME})/\overline{WE}$ is LOW when $\overline{RAS}$ goes LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle.

POWER UP AND INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 8ms, the MT42C8127 must be initialized.

After Vcc is at specified operating conditions, for 100µs minimum, 8 $\overline{RAS}$ cycles and 1 SC cycle must be executed to initialize the memory array. When the device is initialized the DRAM I/O pins (DQ's) are in a High-Z state, regardless of the state of $(\overline{TR})/\overline{OE}$. The DRAM array will contain random data.

The SAM portion of the MT42C8127 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQ's) will be High-Z, regardless of the state of $\overline{SE}$a,b. The mask register will contain random data after power-up.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					A0 - A8[1]		DQ1 - DQ8[2]		MASK REGISTER
		CAS	TR / OE	ME / WE	DSF	SE	RAS	CAS A8=X	RAS	CAS[3]	
	DRAM OPERATIONS										
CBR	CAS-BEFORE-RAS REFRESH	0	X	X	X	X	—	X	—	X	X
ROR	RAS-ONLY REFRESH	1	1	X	X	X	ROW	—	X	—	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	ROW	COLUMN	X	VALID DATA	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	ROW	COLUMN	X	VALID DATA	USE
	REGISTER OPERATIONS										
LMR	LOAD MASK REGISTER	1	1	1	1	X	ROW[4]	X	X	WRITE MASK	LOAD
	TRANSFER OPERATIONS										
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	ROW	TAP[5]	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	ROW	TAP[5]	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	ROW	TAP[5]	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)	1	0	0	0	1	ROW[4]	TAP[5]	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	ROW	TAP[5]	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and A0-A7 when CAS falls.
2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
3. On WRITE cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is latched at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. This is the first SAM address location that the first SC cycle will access. For Split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (127 for lower half, 255 for upper half).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Operating Temperature, Ta(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0V)	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		8	pF	2
Input/Output Capacitance: DQ, SDQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MAX -10	MAX -12	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: T_{RC} = $T_{RC(MIN)}$)	I_{CC1}	80	70	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: T_{PC} = $T_{PC(MIN)}$)	I_{CC2}	60	70	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min)	I_{CC3}	10	10	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH})	I_{CC4}	80	70	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling)	I_{CC5}	70	60	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	85	75	mA	3

CURRENT DRAIN, SAM ACTIVE (tsc = MIN)

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MAX -10	MAX -12	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: T_{RC} = $T_{RC(MIN)}$)	I_{CC7}	120	110	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: T_{PC} = $T_{PC(MIN)}$)	I_{CC8}	100	90	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min)	I_{CC9}	45	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH})	I_{CC10}	120	110	mA	3, 4
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling)	I_{CC11}	110	100	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	125	115	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	180		210		ns	
READ-MODIFY-WRITE cycle time	^tRWC	235		280		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	55		65		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	110		140		ns	
Access time from $\overline{RAS}$	^tRAC		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		30		35	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	^tOE		25		30	ns	
Access time from column address	^tAA		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	30		35		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		ns	
$\overline{CAS}$ pulse width	^tCAS	30	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		20		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	70	25	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		10		ns	
Row address setup time	^tASR	0		0		ns	
Row address hold time	^tRAH	15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	20	50	20	60	ns	18
Column address setup time	^tASC	0		0		ns	
Column address hold time	^tCAH	20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	50		60		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	30	ns	20, 23
Output Disable	^tOD	0	20	0	30	ns	23
Output Disable hold time from start of write	^tOEH		15		20	ns	27
Output Enable to $\overline{RAS}$ delay	^tORD		0		0	ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	70		85		ns	
Write command pulse width	^tWP	15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	130		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	80		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	60		75		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	30		30		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	15		15		ns	
Mask Data to $\overline{RAS}$ setup time	^tMS	0		0		ns	
Mask Data to $\overline{RAS}$ hold time	^tMH	15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER command to $\overline{RAS}$ setup time	^tTLS	0		0		ns	25
TRANSFER command to $\overline{RAS}$ hold time	^tTLH	15	10,000	15	10,000	ns	25
TRANSFER command to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	^tRTH	80	10,000	90	10,000	ns	25
TRANSFER command to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	^tCTH	25		30		ns	25
TRANSFER command to column address hold time (for REAL-TIME READ TRANSFER only)	^tATH	30		35		ns	25
TRANSFER command to SC lead time	^tTSL	5		5		ns	25
TRANSFER command to $\overline{RAS}$ lead time	^tTRL	0		0		ns	25
TRANSFER command to $\overline{RAS}$ delay time	^tTRD	15		15		ns	25
TRANSFER command to $\overline{CAS}$ time	^tTCL	0		0		ns	25
TRANSFER command to $\overline{CAS}$ delay time	^tTCD	15		15		ns	25
First SC edge to TRANSFER command delay time	^tTSD	10		10		ns	25
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	10	40	10	50	ns	
SC to $\overline{RAS}$ setup time	^tSRS	30		40		ns	
$\overline{RAS}$ to SC delay time	^tSRD	25		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		ns	
$\overline{RAS}$ to SD buffer turn-on time	^tSRO	15		15		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	50		55		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	15		15		ns	
NONTRANSFER command to $\overline{RAS}$ setup time	^tYS	0		0		ns	26
NONTRANSFER command to $\overline{RAS}$ hold time	^tYH	15		15		ns	26
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	15		15		ns	
SC to QSF delay time	^tSQD		30		35	ns	
SPLIT TRANSFER setup time	^tSTS	35		40		ns	
SPLIT TRANSFER hold time	^tSTH	35		40		ns	
$\overline{RAS}$ to first SC delay	^tRSD	95		105		ns	
$\overline{CAS}$ to first SC delay	^tCSD	25		35		ns	
Column address valid to first SC delay	^tASD	55		65		ns	
$\overline{TR/OE}$ to QSF Delay Time	^tTQD		35		40	ns	
$\overline{CAS}$ to QSF Delay Time	^tCQD		45		50	ns	
$\overline{RAS}$ to QSF delay time	^tRQD		85		105	ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

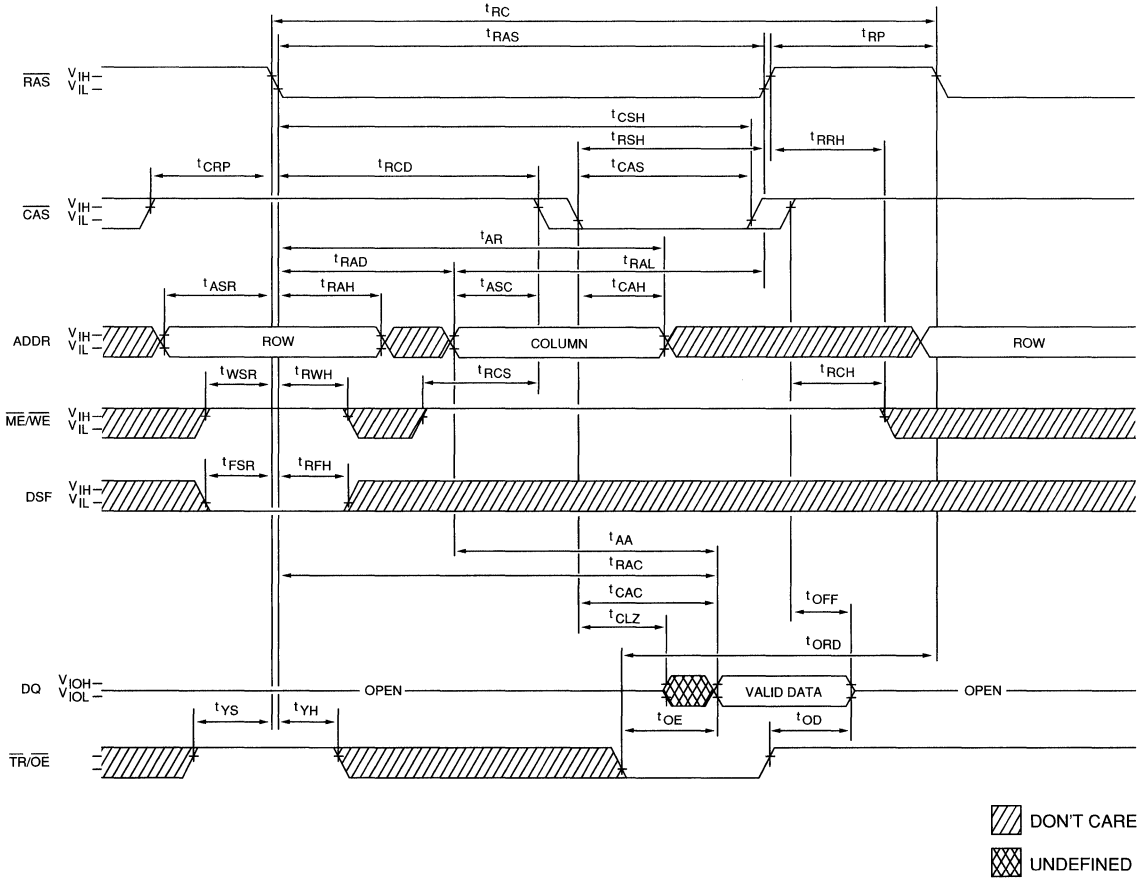
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**		
Serial clock cycle time	^tSC	30		35		ns	
Access time from SC	^tSAC		30		35	ns	24
SC precharge time (SC LOW time)	^tSP	10		12		ns	
SC pulse width (SC HIGH time)	^tSAS	10		12		ns	
Access time from $\overline{SE}$	^tSEA		20		30	ns	24
$\overline{SE}$ precharge time	^tSEP	15		15		ns	
$\overline{SE}$ pulse width	^tSE	15		15		ns	
Serial data-out hold time after SC high	^tSOH	5		5		ns	24
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	0	15	0	25	ns	24
Serial data-in setup time	^tSDS	0		0		ns	24
Serial data-in hold time	^tSDH	15		20		ns	24
SERIAL INPUT (Write) Enable setup time	^tSWS	0		0		ns	
SERIAL INPUT (Write) Enable hold time	^tSWH	15		20		ns	
SERIAL INPUT (Write) Disable setup time	^tSWIS	0		0		ns	
SERIAL INPUT (Write) Disable hold time	^tSWIH	15		20		ns	

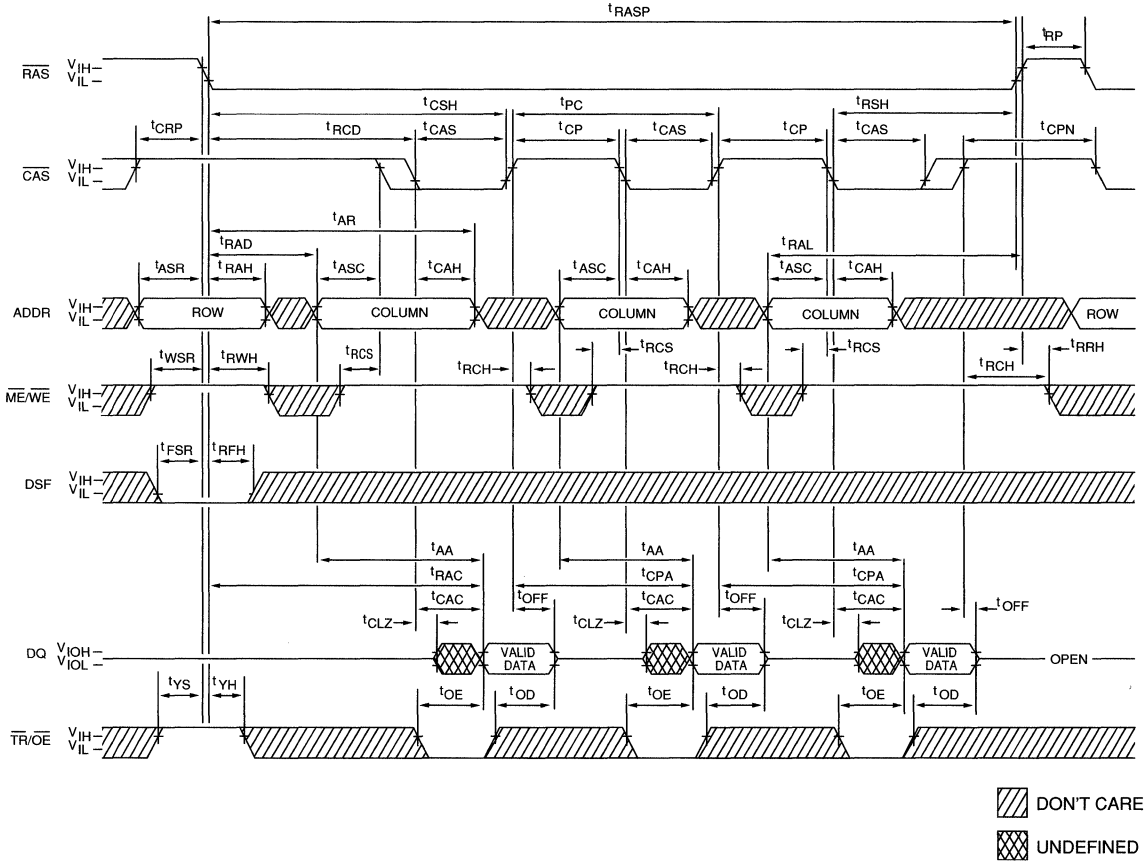
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycle and 1 SC cycle before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, DRAM data output (DQ1-DQ8) is high impedance.
12. If $\overline{CAS} = V_{IL}$, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gate and 100pF. Output reference levels: $V_{OH} = 2.0V$; $V_{OL} = 0.8V$.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \le ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: $V_{OH} = 2.0V$; $V_{OL} = 0.8V$.
25. TRANSFER command means that $\overline{TR}/\overline{OE}$ is LOW when $\overline{RAS}$ goes LOW.
26. NONTRANSFER command means that $\overline{TR}/\overline{OE}$ is HIGH when $\overline{RAS}$ goes LOW.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



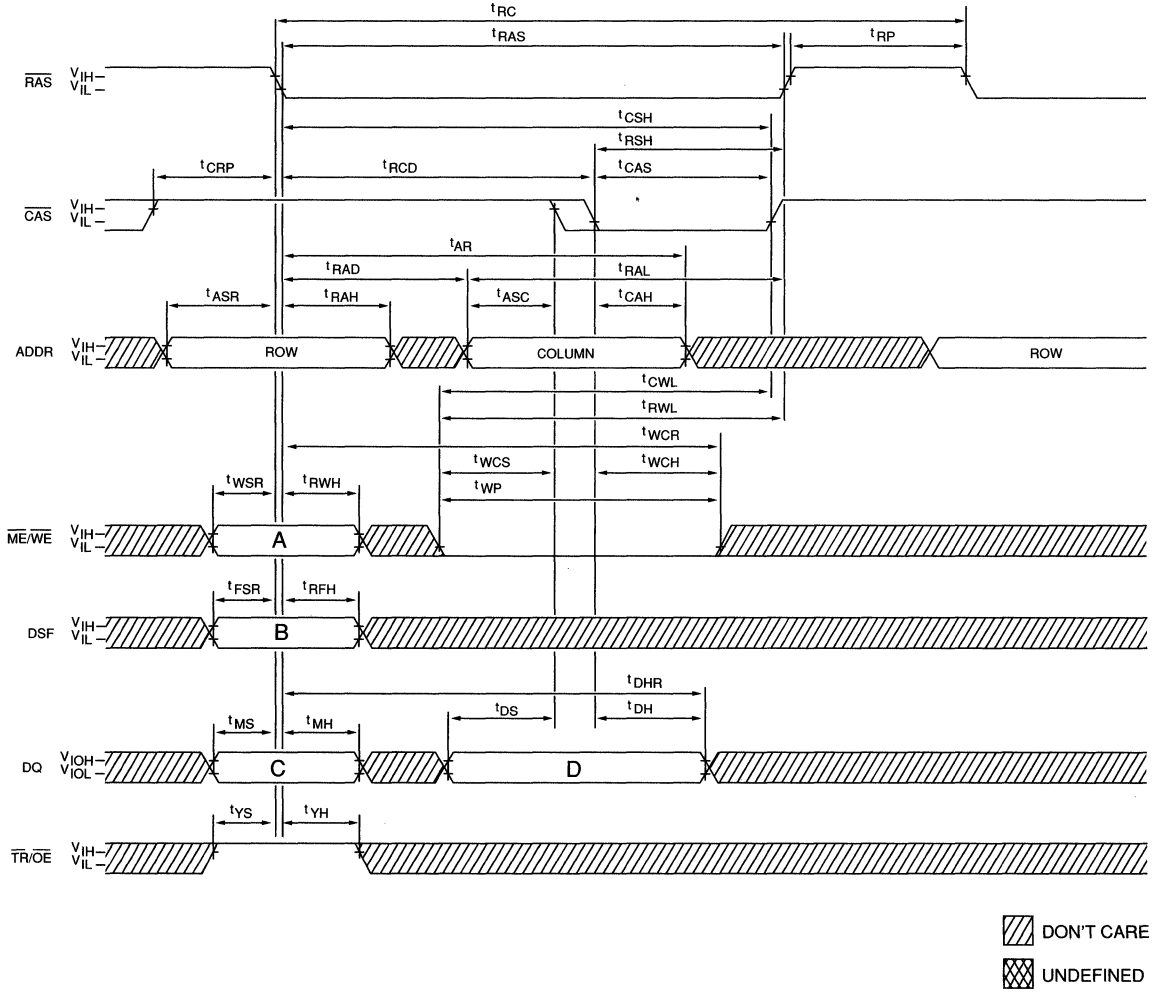
NOTE: WRITE or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

WRITE CYCLE FUNCTION TABLE

LOGIC STATES				FUNCTION
$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DQ (Input)	
1	0	X	DRAM Data	Normal DRAM WRITE
0	0	Write Mask	DRAM Data (Masked)	NONPERSISTENT (Load and Use Register) MASKED WRITE to DRAM
0	1	X	DRAM Data (Masked)	PERSISTENT (Use Register) MASKED WRITE to DRAM
1	1	X	Write Mask	Load Mask Register

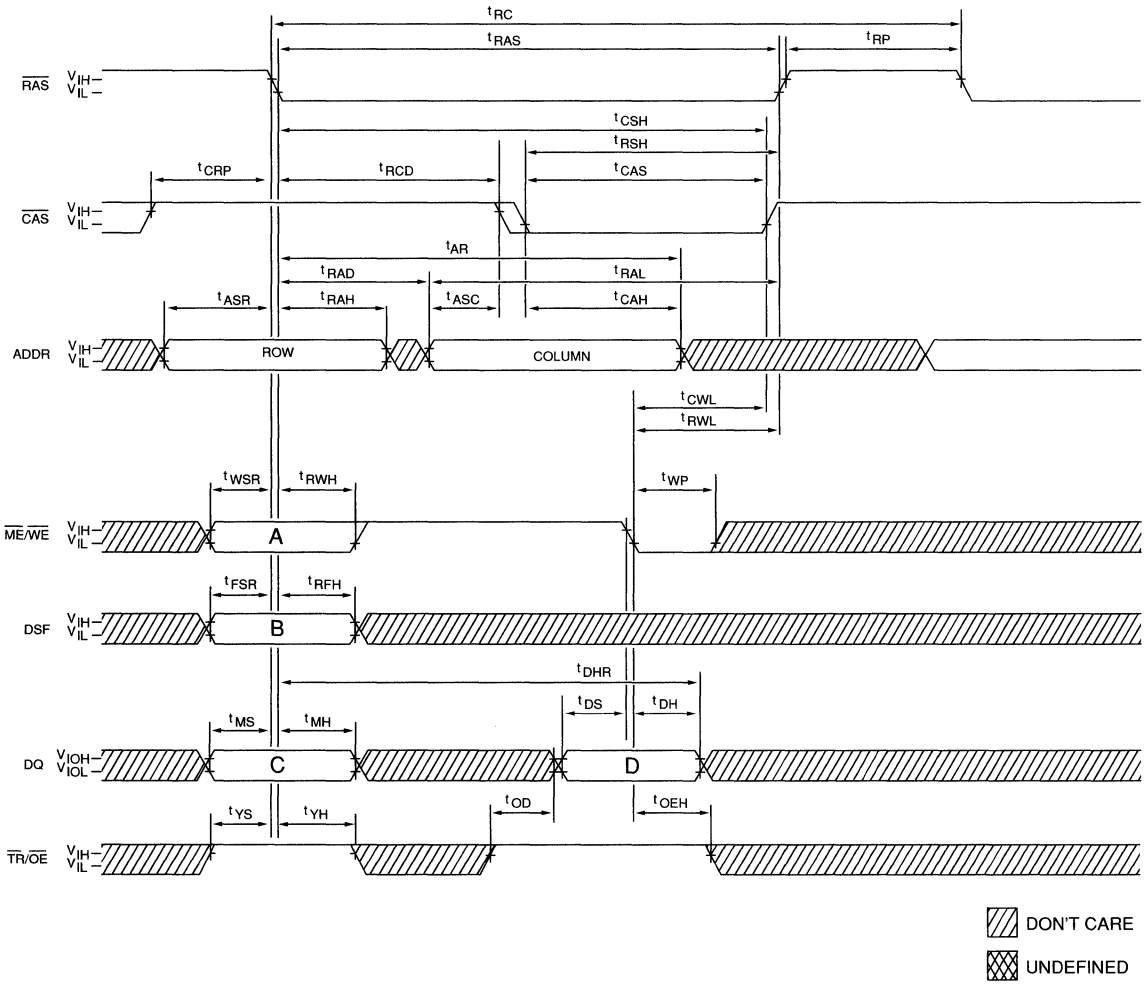
NOTE: Refer to this function table to determine the logic states of "A", "B", "C", and "D" for the WRITE cycle timing diagrams on the following pages.

DRAM EARLY-WRITE CYCLE



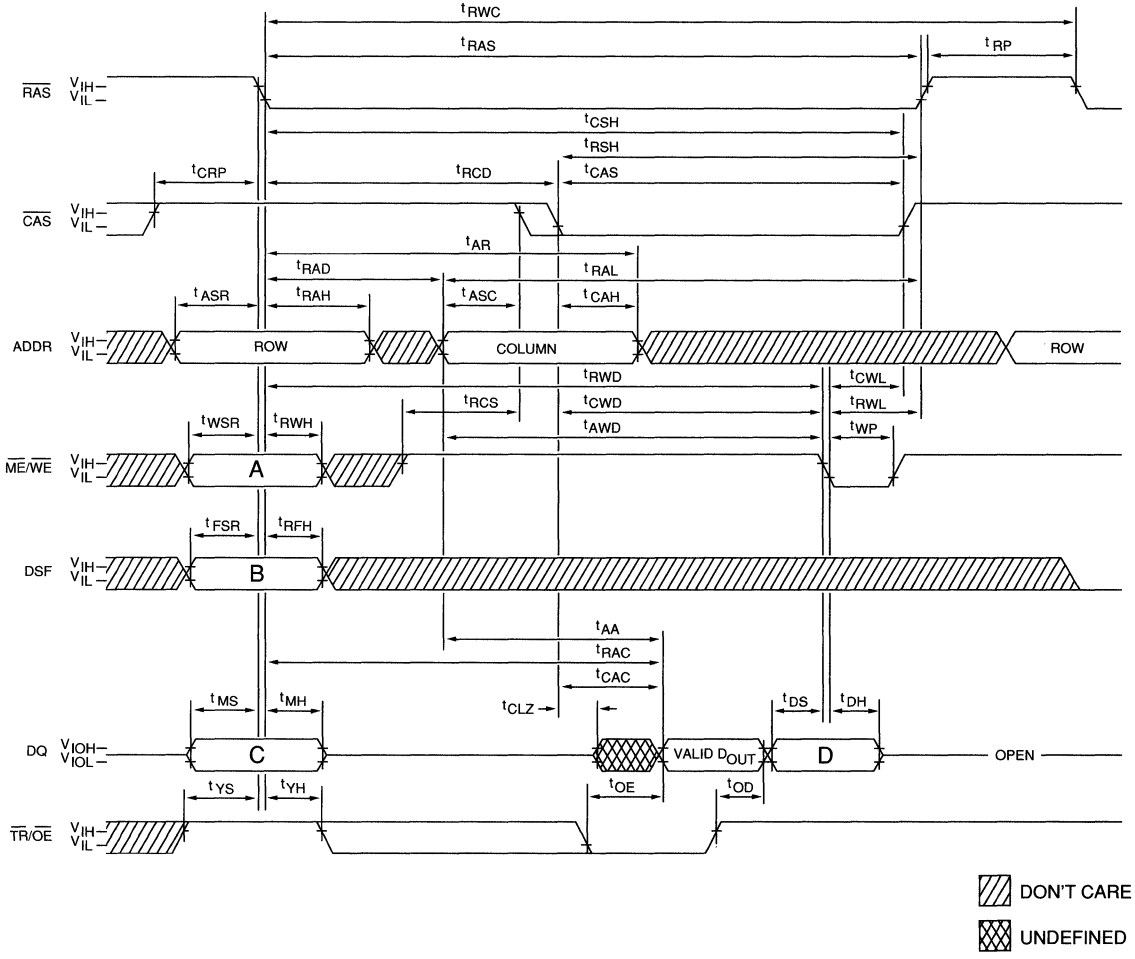
NOTE: The logic states of "A", "B", "C", and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE



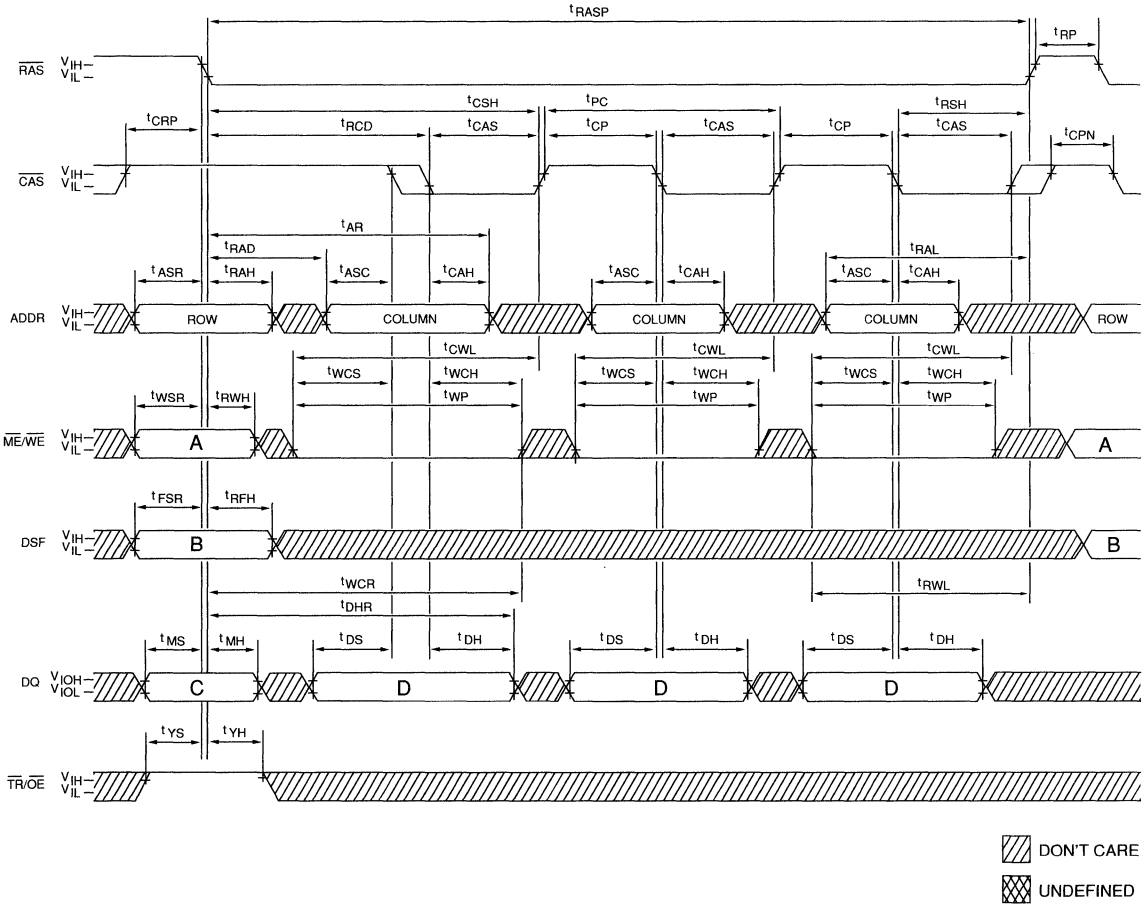
NOTE: The logic states of "A", "B", "C", and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



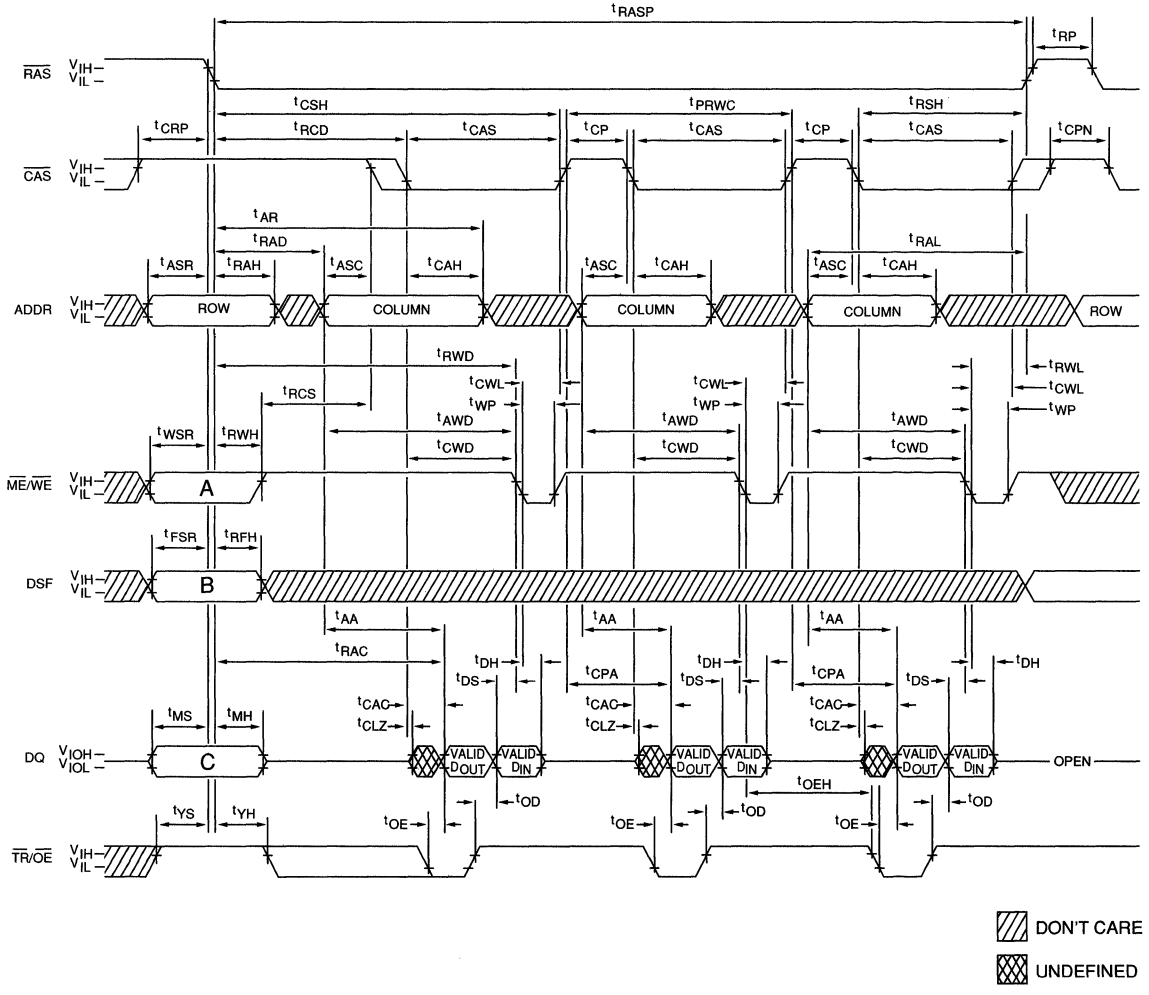
NOTE: The logic states of "A", "B", "C", and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



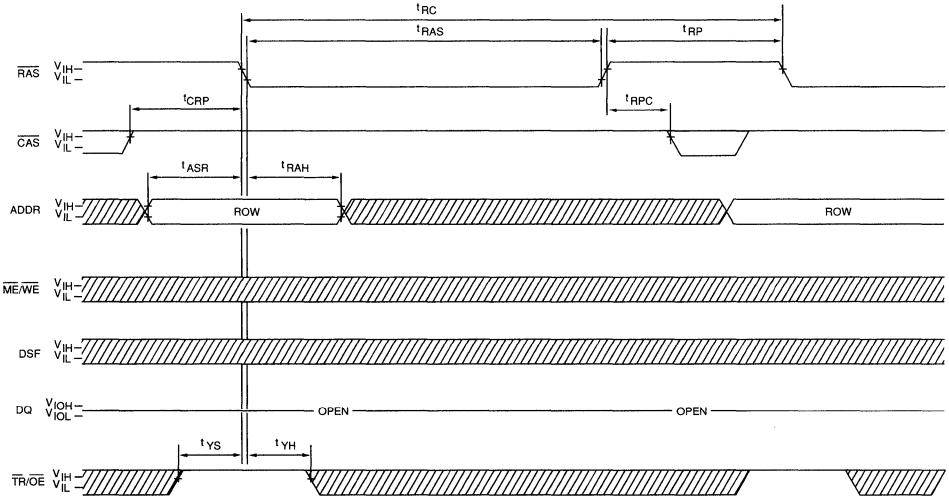
NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
2. The logic states of "A", "B", "C", and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE or LATE-WRITE CYCLES)

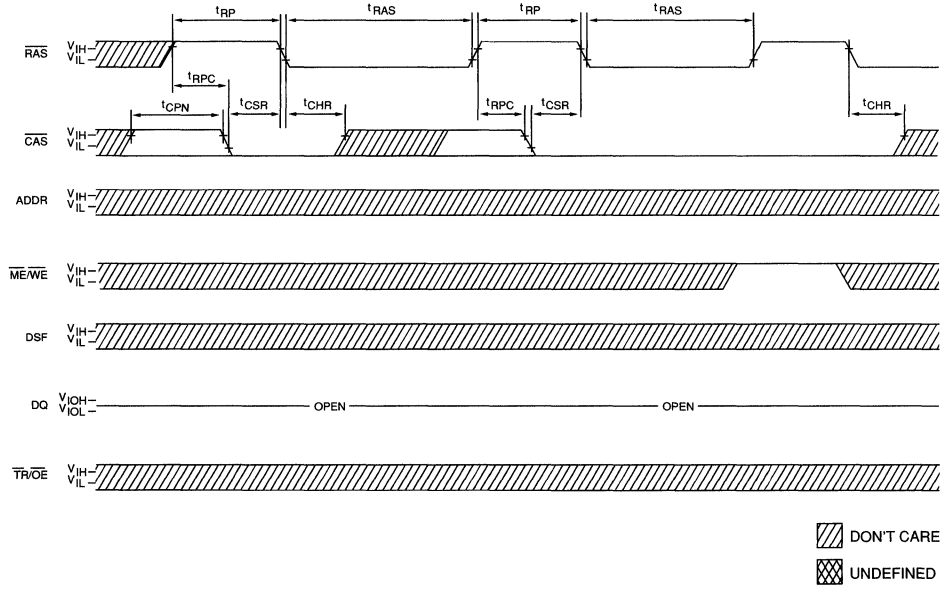


NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

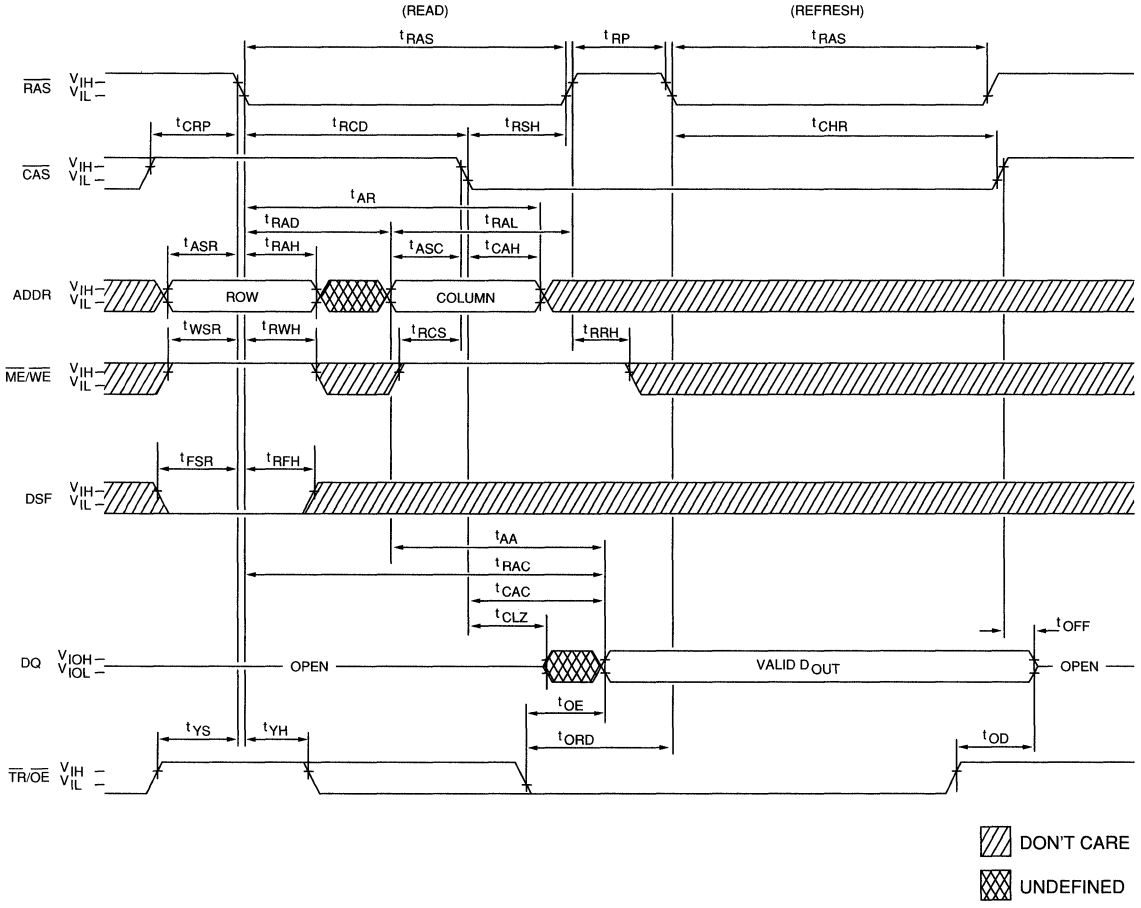
DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

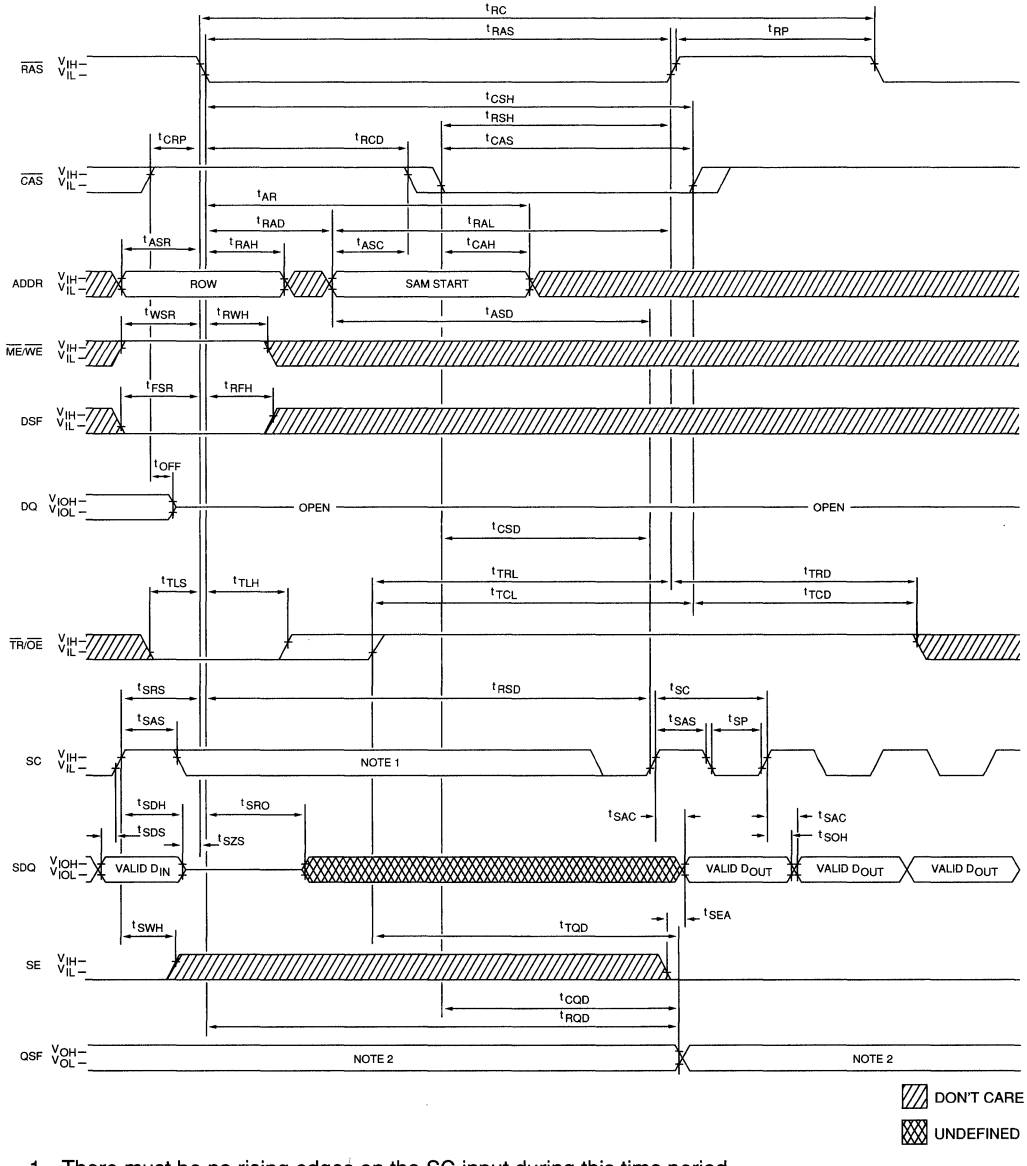


DRAM HIDDEN-REFRESH CYCLE



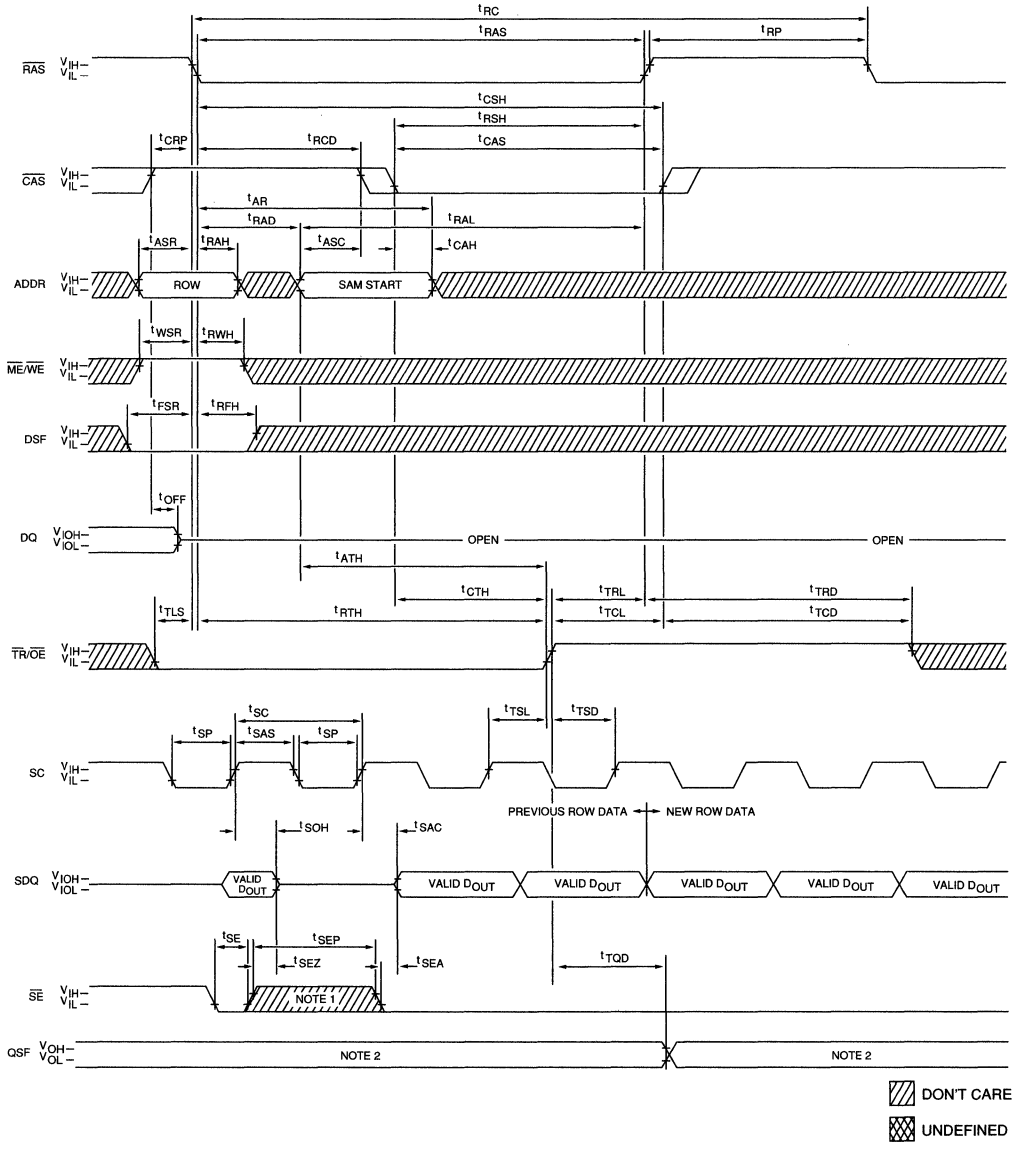
NOTE: A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



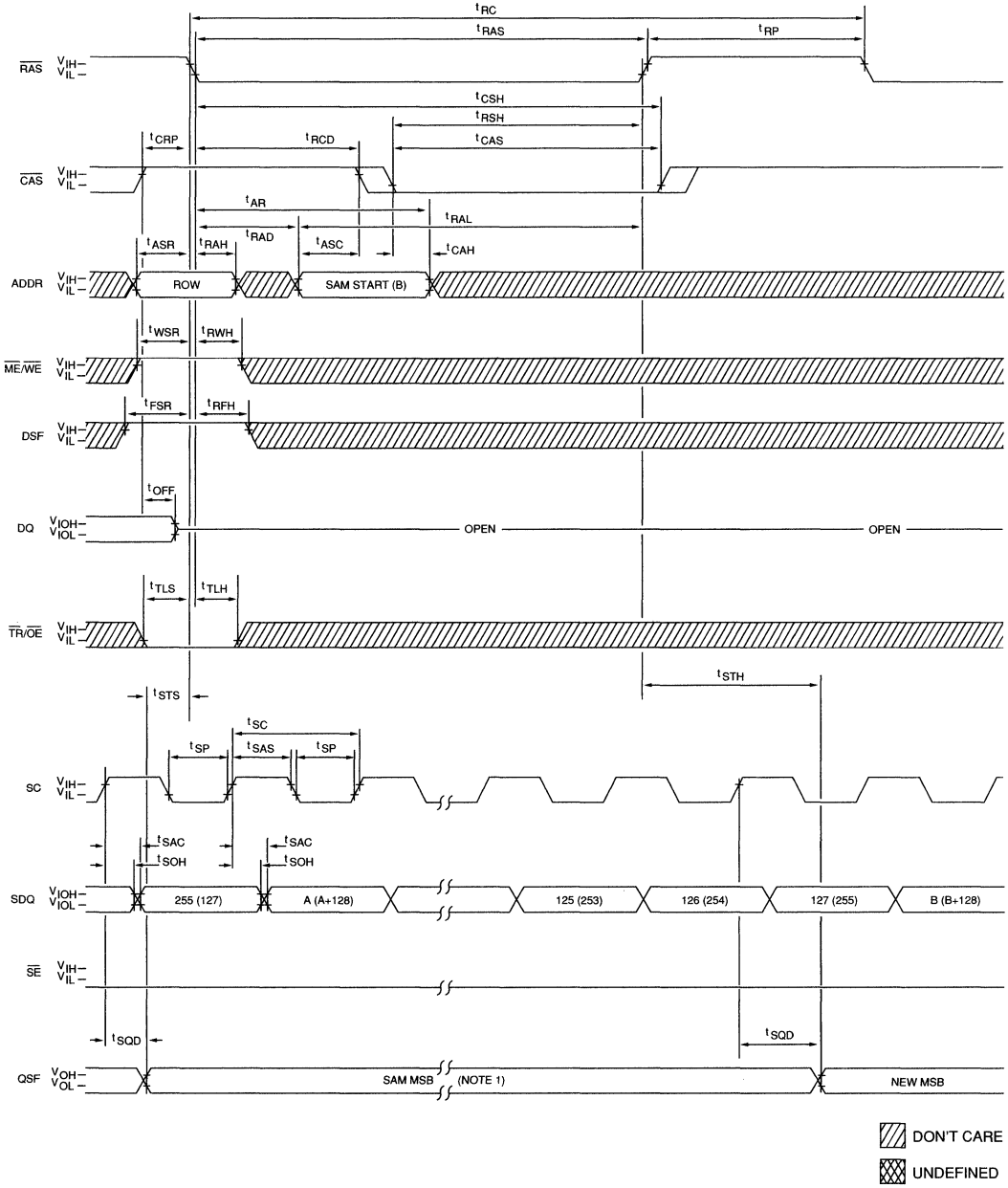
NOTE: 1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

REAL-TIME READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

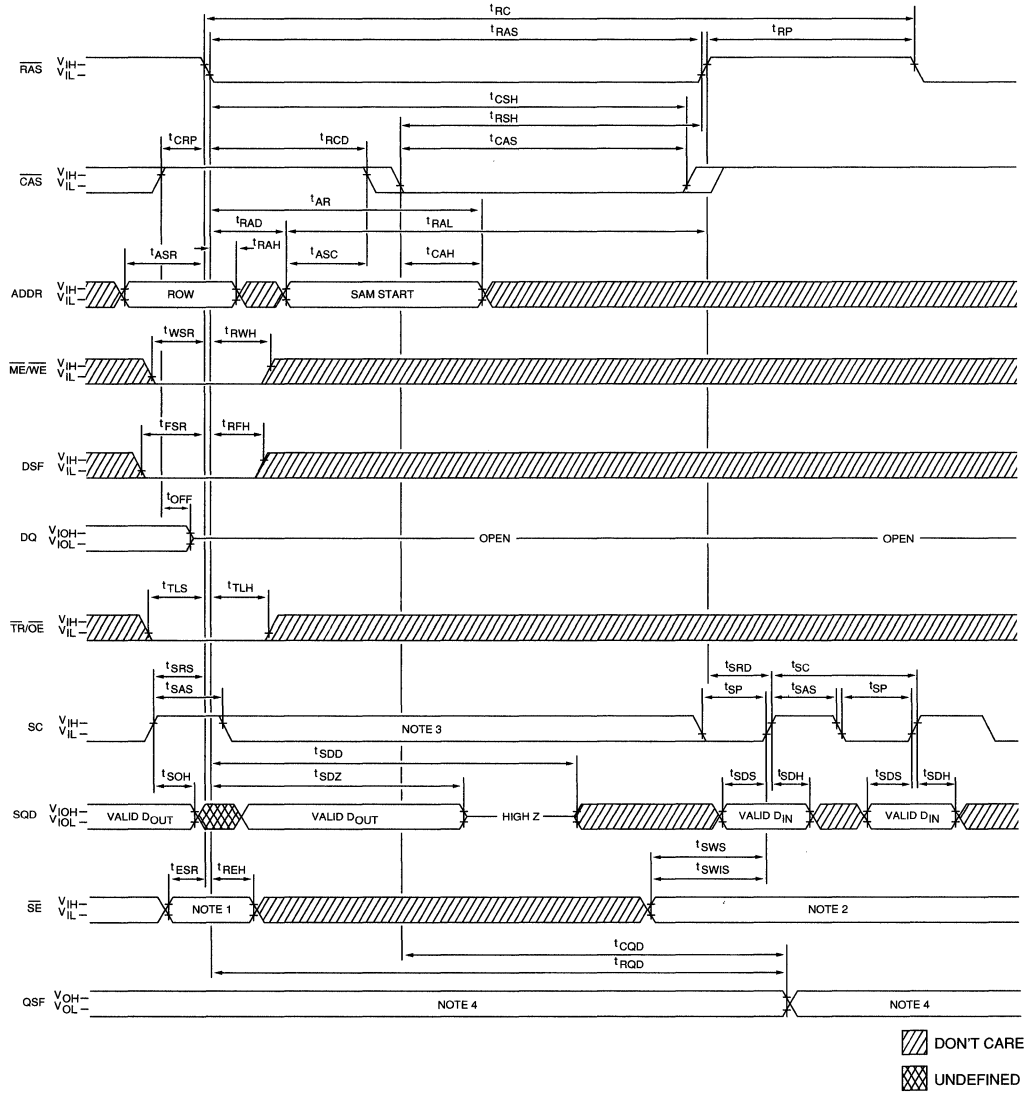
SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

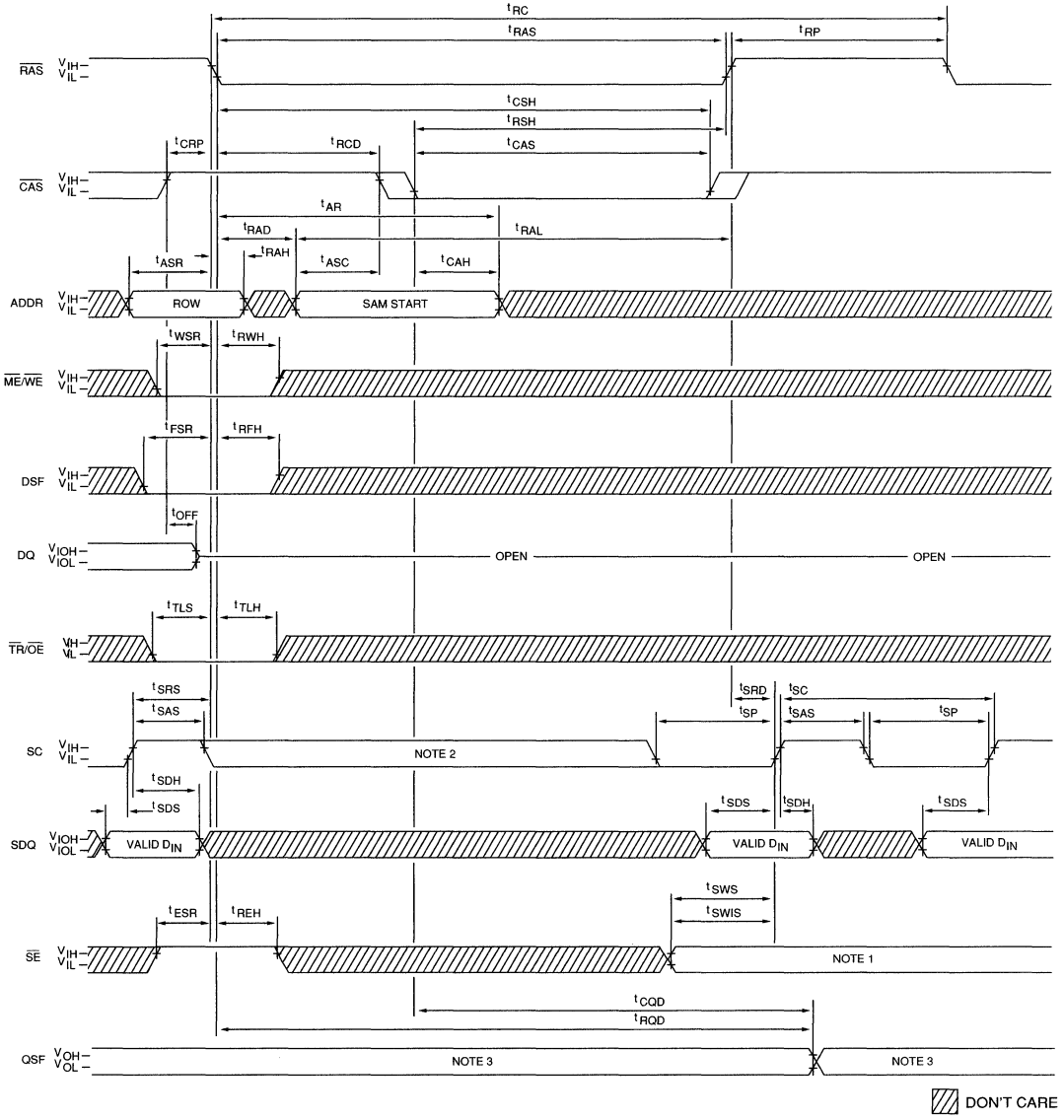
WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



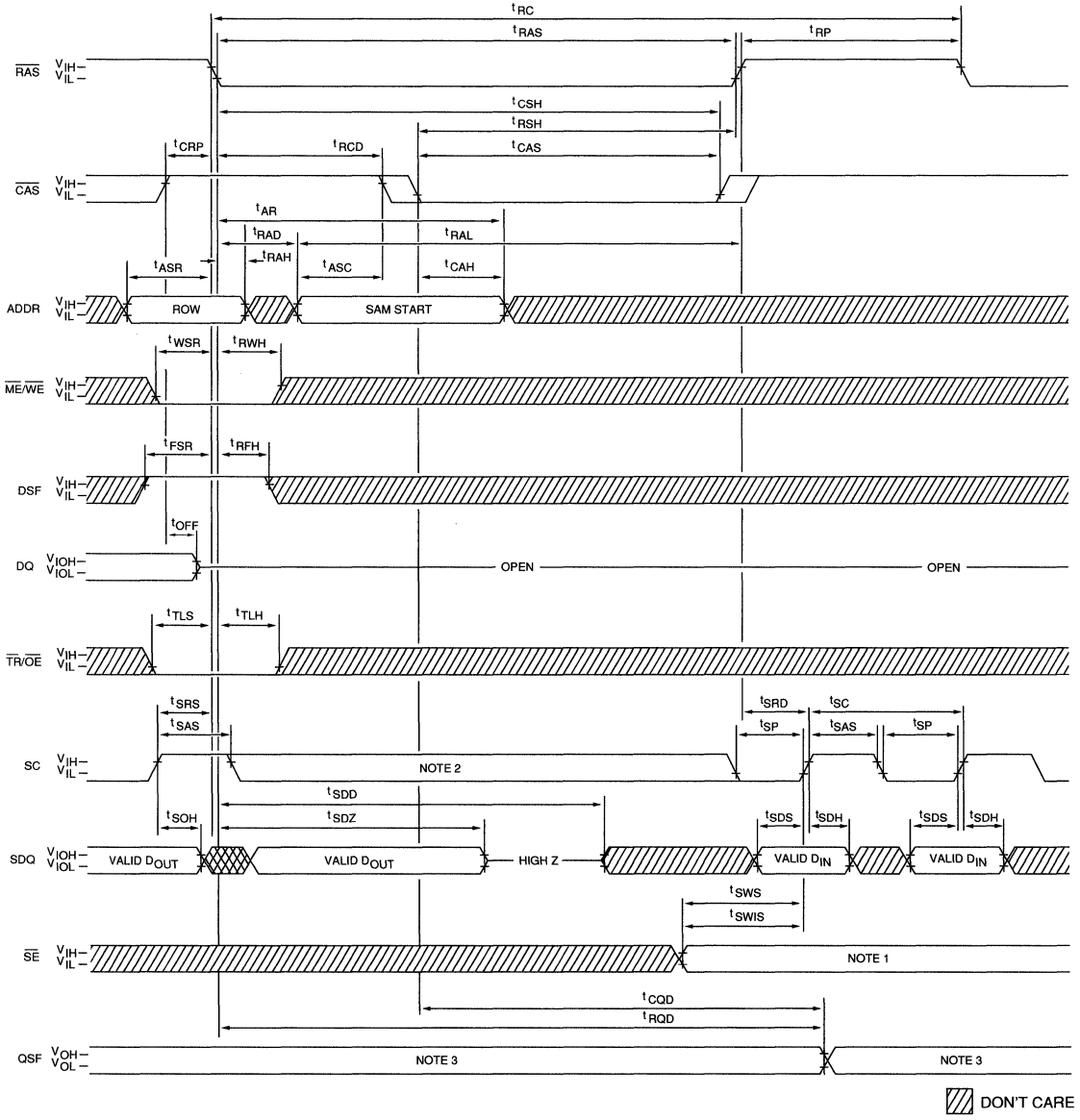
NOTE:
1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
   If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



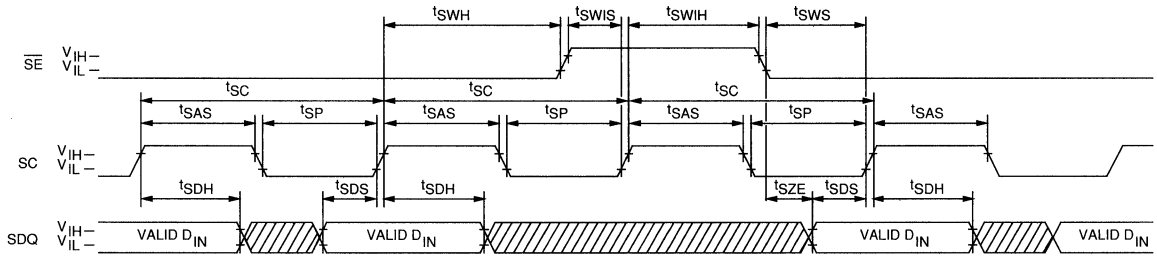
NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

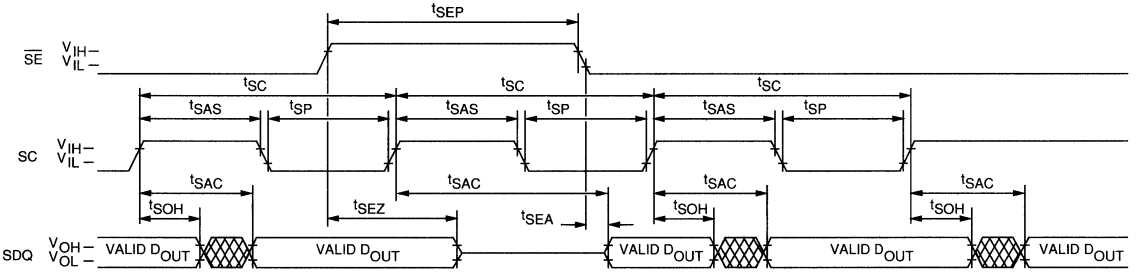


NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



DON'T CARE

UNDEFINED

VRAM

128K x 8 DRAM WITH 256 x 8 SAM

FEATURES

- Industry standard pinout, timing and functions
- High-performance CMOS silicon gate process
- Single +5V ±10% power supply
- Low power: 15mW standby; 275mW active, typical
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh within 8ms
- No refresh required for Serial Access Memory
- Optional FAST PAGE MODE access cycles
- Dual port organization: 256K x 4 DRAM port
  512 x 4 SAM port
- Fast access times – 80ns random, 25ns serial

SPECIAL FUNCTIONS

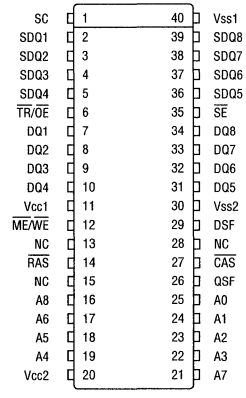
- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER
- BLOCK WRITE

OPTIONS / MARKING

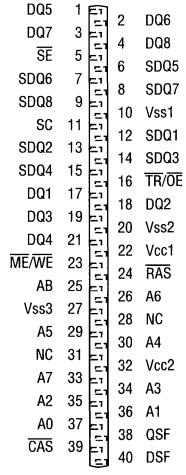
• Timing (DRAM, SAM)	
80ns, 25ns	- 8
100ns, 30ns	-10
120ns, 35ns	-12
• Packages	
Plastic SOJ	DJ
Plastic ZIP	Z

PIN ASSIGNMENT (Top View)

40-Pin SOJ (E-12)



40-Pin ZIP (C-6)



GENERAL DESCRIPTION

The MT42C8128 is a high-speed, dual port CMOS dynamic random access memory or Video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed either by an 8-bit wide DRAM port or by a 256 x 8-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4 DRAM). Eight 256-bit data registers make up the SAM portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 256 bit wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C8128 is compatible with (and can be identical to) the operation of the MT42C4064 (64K x 4 VRAM). However, the MT42C8128 offers several additional functions that may be used to increase system performance or ease critical timing requirements. These "special functions" are described in detail in the following sections.

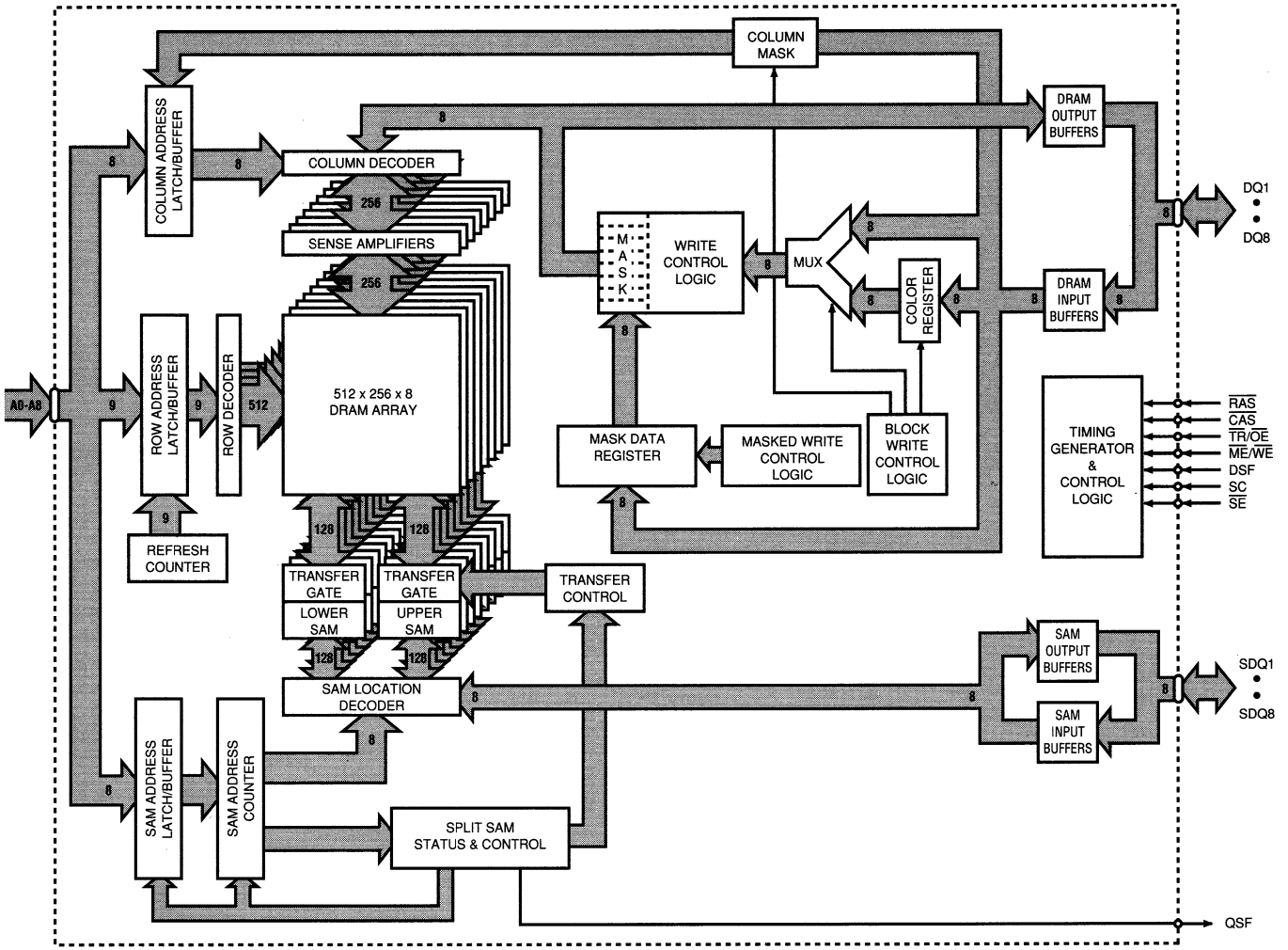


Figure 1
MT42C8128 BLOCK DIAGRAM

PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	11	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
6	16	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a High-Z state.
12	23	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
35	5	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state. $\overline{SE}$ is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
29	40	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used for a particular access cycle.
14	24	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and as a strobe for the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, $\overline{SE}$, $\overline{CAS}$ and DQ inputs.
27	39	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 8 column-address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and as a strobe for the DSF input.
16, 17, 18 19, 21, 22 23, 24, 25	37, 36, 35 34, 30, 29 26, 33, 25	A0 to A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 128K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A7 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A7, A8 = "don't care" for the start address when doing SPLIT TRANSFER.
7, 8, 9, 10, 31 32, 33, 34	17, 18, 19, 21 1, 2, 3, 4	DQ1 - DQ8	Input/ Output	DRAM Data I/O: DRAM input/Output for DRAM cycles; inputs for Mask Data Register and Color Register load cycles, and Bit and Column Mask inputs for BLOCK WRITE.
2, 3, 4, 5, 36 37, 38, 39	12, 13, 14, 15 6, 7, 8, 9	SDQ1 - SDQ8	Input/ Output	Serial Data I/O: Input, output, or High-Z.
26	38	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-127, HIGH if address is 128-255.
28	28, 31	NC	–	No Connect: This pin should be either left unconnected or tied to ground.
11, 20	22, 32	V_{CC}	Supply	Power Supply: +5V ±10%
30, 40	10, 20, 27	V_{SS}	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8128 can be divided into three functional blocks (see Figure 1): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations, the TR/OE pin will be shown as TR/(OE).*

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C8128 VRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C8128 supports CAS-BEFORE-RAS, RAS ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the RAS-ONLY and CAS-BEFORE-RAS cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C8128 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has several special functions that can be used when writing to the DRAM.

The 17 address bits that are used to select a 8-bit word from the 131,072 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the nine row-address bits are set up on the address inputs and clocked into the part when RAS transitions from HIGH to LOW. Next, the 8 column address bits are set up on the address inputs and clocked-in when CAS goes from HIGH to LOW.

For single port DRAMS, the OE pin is a "don't care" when RAS goes LOW. However, for the VRAM, when RAS goes LOW, (TR)/OE selects between DRAM access or TRANSFER cycles. (TR)/OE must be HIGH at the RAS HIGH-to-LOW transition for all DRAM operations (except CAS-BEFORE-RAS).

If (ME)/WE is HIGH when CAS goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ8 port. The (TR)/OE input must transition from HIGH to LOW sometime after RAS falls to enable the DRAM output port.

For single port normal DRAMs, WE is a "don't care" when RAS goes LOW. For the VRAM, ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH to LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells. If (ME)/WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

NON PERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only specific bits within a 8-bit word. The MT42C8128 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$) and DSF are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is non persistent (must be re-entered at every $\overline{RAS}$ cycle) if DSF is LOW when $\overline{RAS}$ goes LOW. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE $\overline{RAS}$ cycle. An example NONPERSISTENT MASKED WRITE cycle is shown in Figure 2.

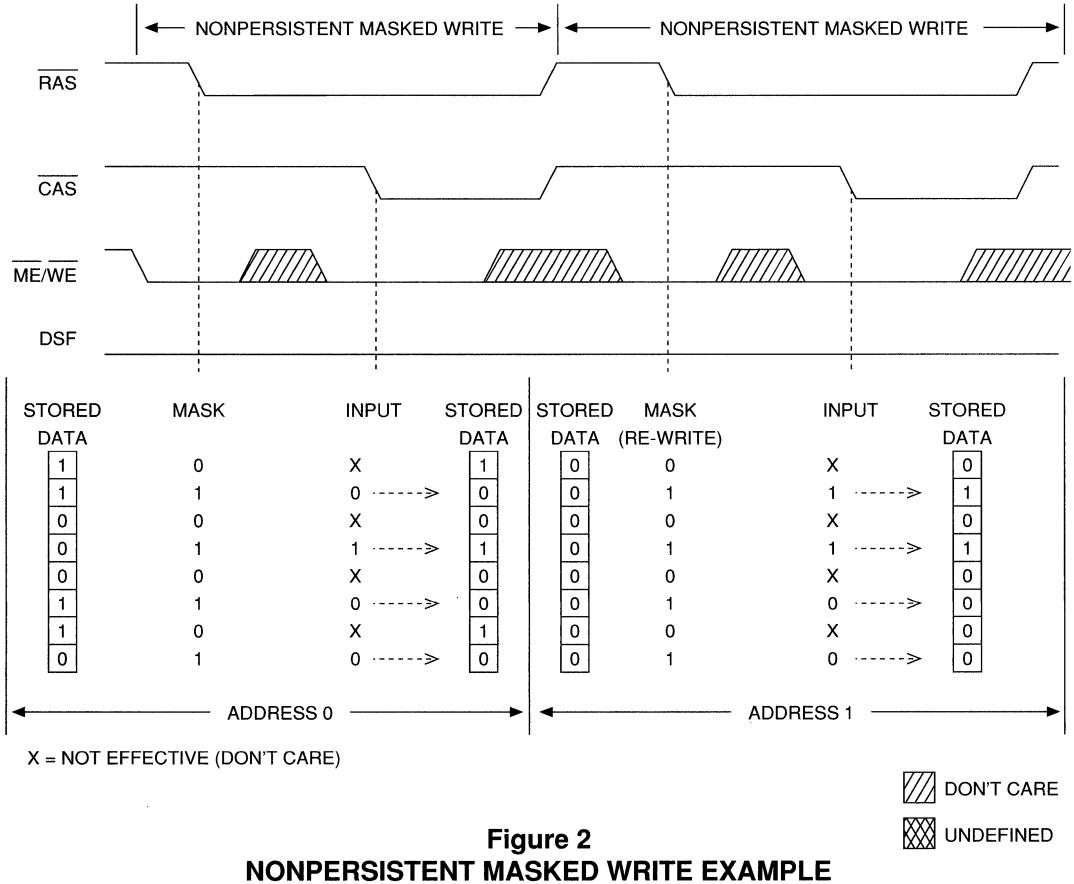


Figure 2
NONPERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW. Mask data may also be loaded into the mask register by performing a NONPERSISTENT MASKED WRITE cycle before the PERSISTENT MASKED WRITE cycles.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITE cycles, to any address, may be performed without having to reload the mask data register. Figure 3 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers, that cannot provide mask data to the DQ pins at $\overline{RAS}$ time, to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations can be performed during FAST PAGE MODE cycles and the same mask will apply to all addressed columns in the addressed row.

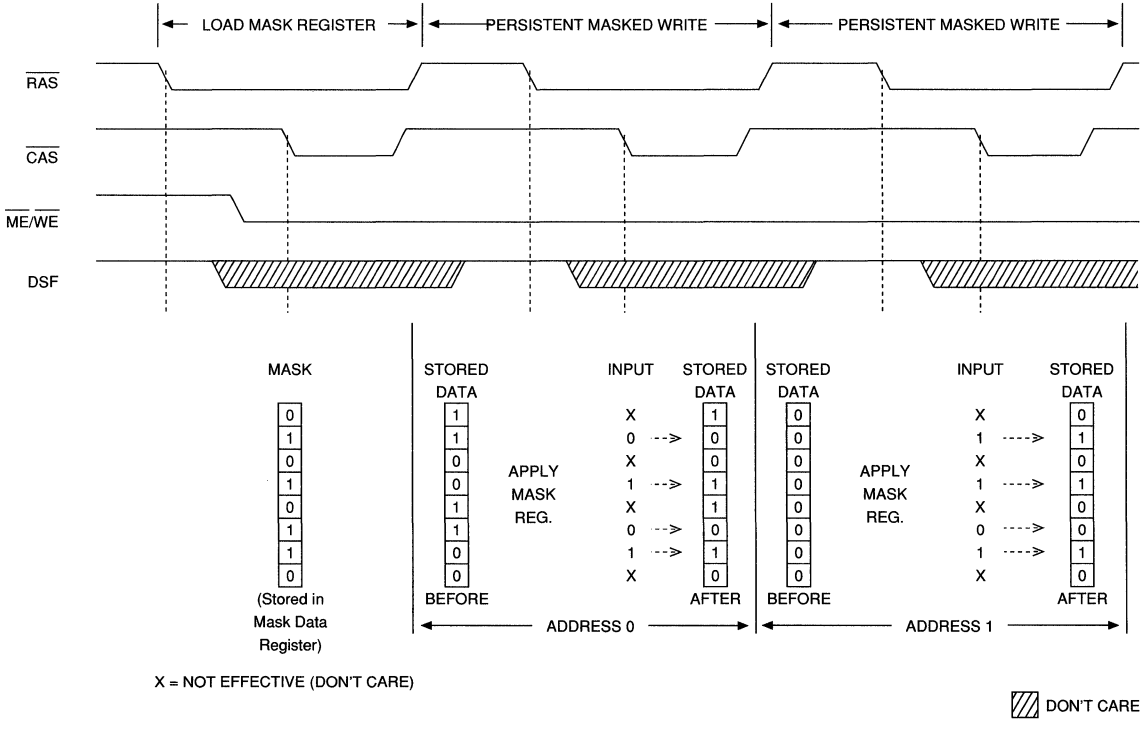


Figure 3
PERSISTENT MASKED WRITE EXAMPLE

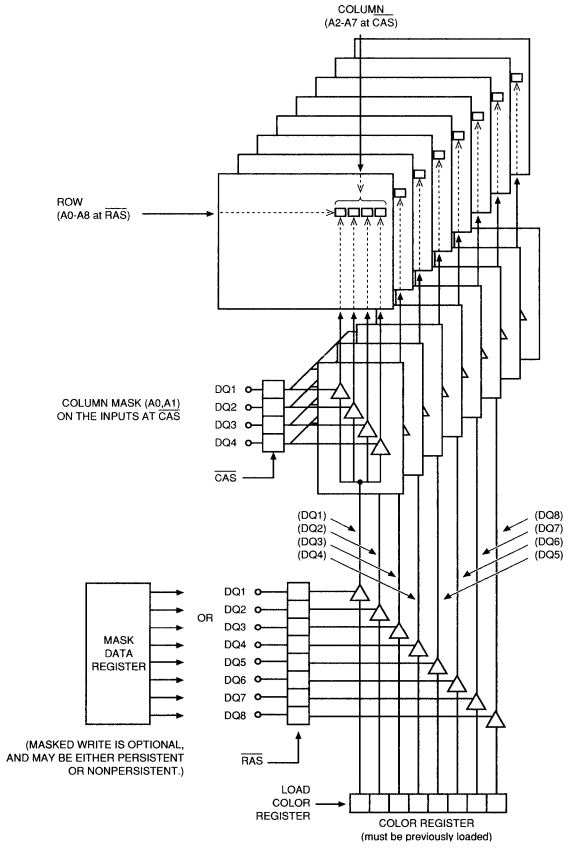


Figure 4
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is HIGH when $\overline{CAS}$ goes LOW, the MT42C8128 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 4). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The ROW is addressed as in a normal DRAM WRITE cycle. However when $\overline{CAS}$ goes LOW, only the A2-A7 inputs are used. A2-A7 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3, and 4) are then used to determine what combination of the four column locations will be changed. The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The Write Enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

INPUTS	Address Controlled	
	A0	A1
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

NONPERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF LOW when $\overline{RAS}$ goes LOW initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH when $\overline{CAS}$ goes LOW, to perform a NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the eight bit planes can be masked and any combination of the four column locations can be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}$/($\overline{OE}$), $\overline{ME}$/($\overline{WE}$), and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NONPERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed.

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the eight 256-bit DRAM row planes that are to be transferred to the eight SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. $\overline{CAS}$ must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished two ways. If the transfer is to be synchronized with SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after $\overline{CAS}$ goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before $\overline{CAS}$ goes LOW (refer to the AC Timing Diagrams). The 2048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 8-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 127), and HIGH if access is from the upper half (128 through 255). If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW to HIGH transition, regardless of the state of $\overline{SE}$. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

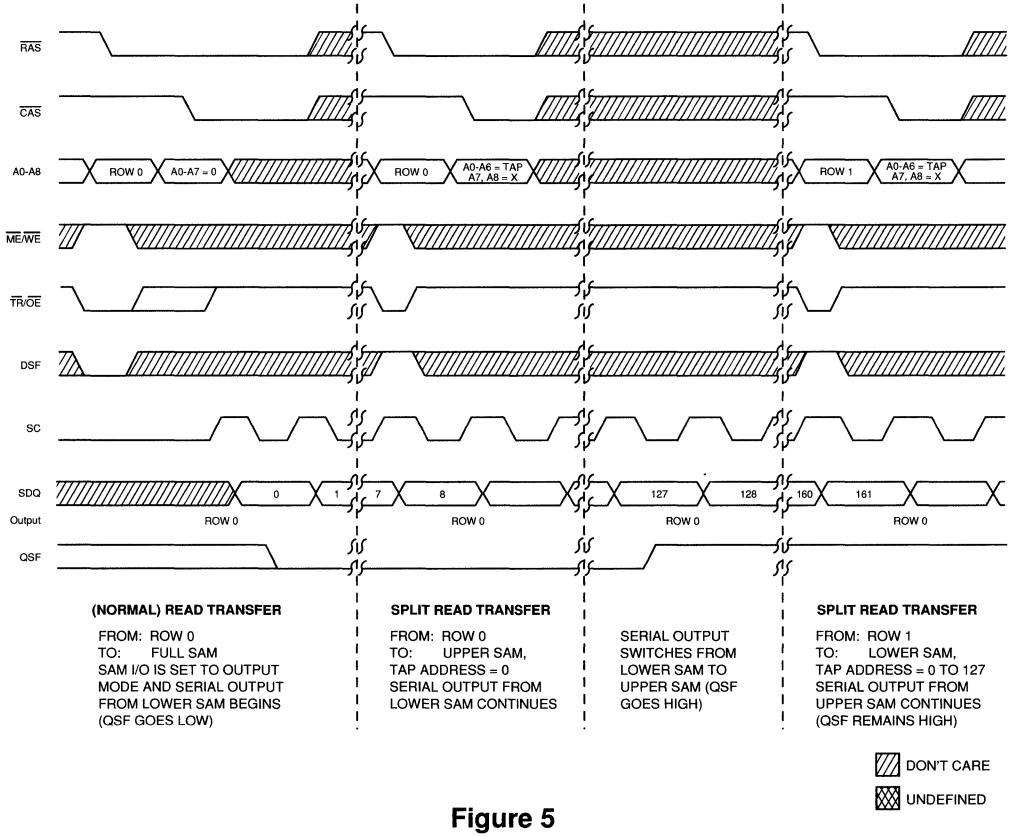


Figure 5
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data can be transferred to the other half. The transfer can occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles. A SPLIT READ TRANSFER does not change the direction of the SAM port.

A normal, non-split READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles to provide a reference to which half of the SAM the access will begin and set SAM I/O direction. Then SPLIT READ TRANSFERS may be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A6, is used to input the SAM Tap address. Address pin A7 is a "don't care" when the Tap address is loaded at the HIGH to LOW transition of $\overline{CAS}$. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 5 shows a typical SPLIT-READ-TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The purpose of the SPLIT TRANSFER of the same data is to initiate the split SAM operating mode and load the Tap address. Serial access continues, and when the SAM address counter reaches 127 ("A7"=0, A0-A6=1) the new Tap address is loaded for the next half ("A7"=1, A0-A6=Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 5 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transfer the upper half of row 1 to the upper SAM. if the half boundry is reached, before a SRT is done for the half, a Tap address of "0" will be used. Access will start at 0 if going to the lower half, 128 if going to the upper. See Figure 6.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to that of the READ TRANSFER described previously except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QFS is LOW if access is to the lower half of the SAM, HIGH if to the upper.

PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and $(\overline{ME})/\overline{WE}$ is LOW when $\overline{RAS}$ goes LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle.

POWER-UP AND INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 8ms, the MT42C8128 must be initialized.

After Vcc is at specified operating conditions, for 100µs minimum, eight $\overline{RAS}$ cycles must be executed to initialize the dynamic memory array. When the device is initialized the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of $(\overline{TR})/\overline{OE}$. The DRAM array will contain random data. QSF will be drawing data.

The SAM portion of the MT42C8128 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQs) will be High-Z, regardless of the state of $\overline{SE}$a,b. The mask and color register will contain random data after power-up.

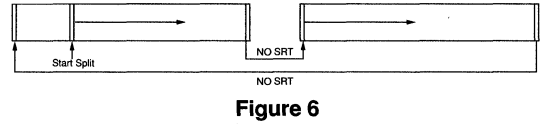


Figure 6
SPLIT SAM TRANSFER

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					CAS FALL	A0 - A8[1]		DQ1 - DQ8[2]		REGISTERS	
		CAS	TR / OE	ME / WE	DSF	SE	DSF	RAS	CAS A8 = X	RAS	CAS[3] WE	MASK	COLOR
	DRAM OPERATIONS												
CBR	CAS-BEFORE-RAS REFRESH	0	X	1	X	X	X	—	X	—	X	X	X
ROR	RAS-ONLY REFRESH	1	1	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	0	ROW	COLUMN	X	VALID	X	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	X	1	ROW	COLUMN (A2 - A7)	X	COLUMN MASK	X	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	X	1	ROW	COLUMN	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASKED REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	X	1	ROW	COLUMN (A2 - A7)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	1	X	0	ROW[4]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	X	1	ROW[4]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS												
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	X	ROW	TAP[5]	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	X	ROW	TAP[5]	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	X	ROW	TAP[5]	X	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT- MODE ENABLE)	1	0	0	0	1	X	ROW[4]	TAP[5]	X	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	X	ROW	TAP[5]	X	X	X	X

NOTE:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and A0-A7 when CAS falls.
2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
3. On WRITE cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is latched at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. This is the SAM location that the first SC cycle will access. For Split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (127 for lower half, 255 for upper half).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Operating Temperature, Ta(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input ($0V \leq V_{IN} \leq V_{CC}$), all other pins not under test = 0V)	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SC, $\overline{SE}$, DSF	C_{I2}		8	pF	2
Input/Output Capacitance: DQ, SDQ	$C_{I/O}$		9	pF	2
Output Capacitance: QSF	C_O		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC1}	90	80	70	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC2}	70	60	50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min)	I_{CC3}	10	10	10	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH})	I_{CC4}	90	80	70	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling)	I_{CC5}	80	70	60	mA	3, 5
SAM/DRAM DATA TRANSFER	I_{CC6}	95	85	75	mA	3

CURRENT DRAIN, SAM ACTIVE (^tSC = MIN)

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: ^tRC = ^tRC (MIN))	I_{CC7}	130	120	110	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC8}	110	100	90	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min)	I_{CC9}	50	45	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH})	I_{CC10}	130	120	110	mA	3, 4
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling)	I_{CC11}	120	110	100	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	I_{CC12}	135	125	115	mA	3, 4

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		180		210		ns	
READ-MODIFY-WRITE cycle time	^tRWC	205		235		280		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		55		65		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	tPRWC	100		110		140		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Access time from ($\overline{TR}$)/$\overline{OE}$	^tOE		20		25		30	ns	
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		80		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	55	20	70	25	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	12		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	20	60	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	20		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	30	ns	20, 23
Output Disable	^tOD	0	20	0	20	0	30	ns	23
Output Disable hold time from start of write	^tOEH		15		15		20	ns	27
Output Enable to $\overline{RAS}$ delay	^tORD		0		0		0	ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		70		85		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		130		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		80		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		70		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	30		30		30		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	10		15		15		ns	
Mask Data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask Data to $\overline{RAS}$ hold time	^tMH	10		15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER command to $\overline{RAS}$ setup time	^tTLS	0		0		0		ns	25
TRANSFER command to $\overline{RAS}$ hold time	^tTLH	12	10,000	15	10,000	15	10,000	ns	25
TRANSFER command to $\overline{RAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tRTH	70	10,000	80	10,000	90	10,000	ns	25
TRANSFER command to $\overline{CAS}$ hold time (REAL-TIME READ-TRANSFER only)	^tCTH	20		25		30		ns	25
TRANSFER command to column address hold time (for REAL TIME READ TRANSFER only)	^tATH	25		30		35		ns	25
TRANSFER command to SC lead time	^tTSL	5		5		5		ns	25
TRANSFER command to $\overline{RAS}$ lead time	^tTRL	0		0		0		ns	25
TRANSFER command to $\overline{RAS}$ delay time	^tTRD	15		15		15		ns	25
TRANSFER command to $\overline{CAS}$ time	^tTCL	0		0		0		ns	25
TRANSFER command to $\overline{CAS}$ delay time	^tTCD	15		15		15		ns	25
First SC edge to Transfer command delay time	^tTSD	10		10		10		ns	25
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	10	35	10	40	10	50	ns	
SC to $\overline{RAS}$ setup time	^tSRS	30		30		40		ns	
$\overline{RAS}$ to SC delay time	^tSRD	20		25		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		0		ns	
$\overline{RAS}$ to SD buffer turn-on time	^tSRO	10		15		15		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	45		50		55		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		0		ns	
Serial-input-mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	12		15		15		ns	
NONTRANSFER command to $\overline{RAS}$ setup time	^tYS	0		0		0		ns	26
NONTRANSFER command to $\overline{RAS}$ hold time	^tYH	12		15		15		ns	26
DSF to $\overline{RAS}$ setup time	^tFSR	0		0		0		ns	
DSF to $\overline{RAS}$ hold time	^tRFH	12		15		15		ns	
SC to QSF delay time	^tSQD		25		30		35	ns	
SPLIT TRANSFER setup time	^tSTS	30		35		40		ns	
SPLIT TRANSFER hold time	^tSTH	30		35		40		ns	
$\overline{RAS}$ to QSF delay time	^tRQD		65		85		105	ns	
DSF to $\overline{RAS}$ hold time	^tFHR	60		65				ns	
DSF to $\overline{CAS}$ Set up time	^tFSC	0		0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		20				ns	
$\overline{TR/OE}$ to QSF delay time	^tTQD		25		30		35	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		35		40		45	ns	
$\overline{RAS}$ to first SC delay	^tRSD	80		95		105		ns	
$\overline{CAS}$ to first SC delay	^tCSD	20		25		35		ns	
Column address valid to first SC delay	^tASD	45		55		65		ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

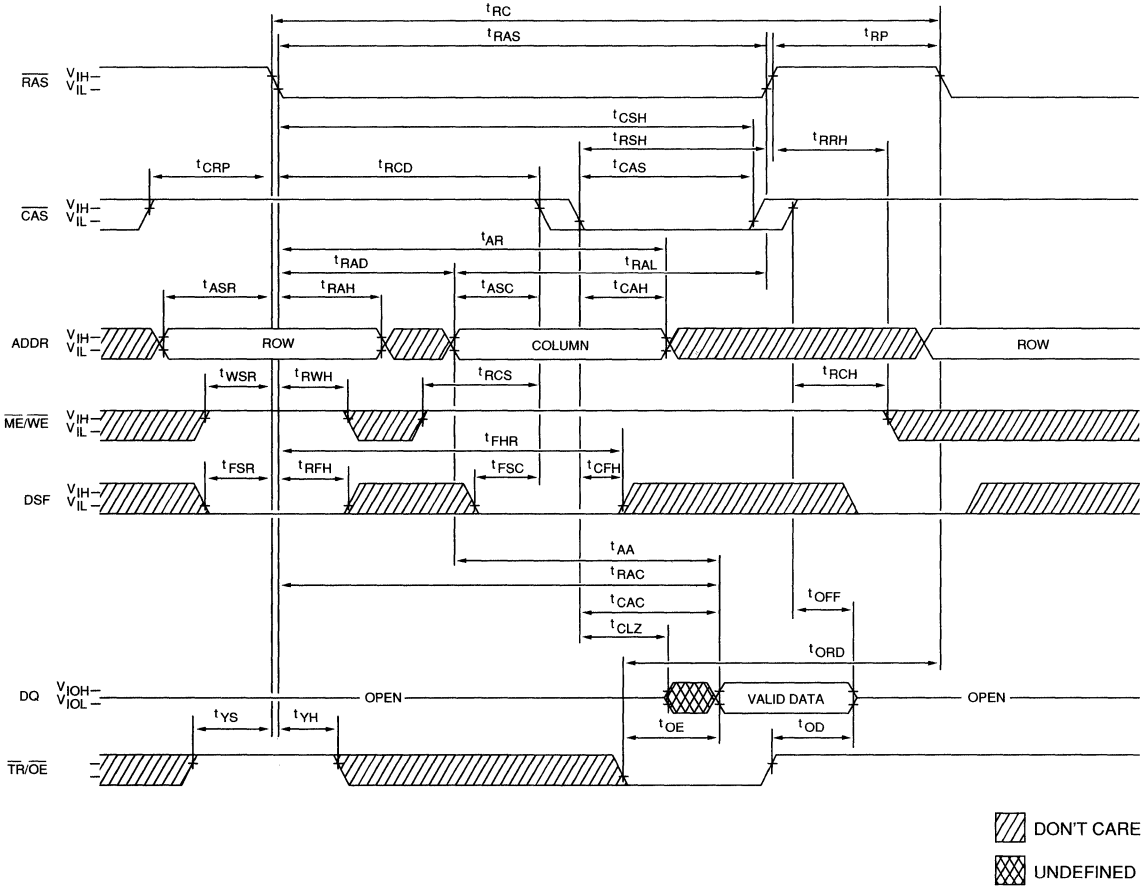
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock-cycle time	^tSC	25		30		35		ns	
Access time from SC	^tSAC		25		25		35	ns	24
SC precharge time (SC LOW time)	^tSP	10		10		12		ns	
SC pulse width (SC HIGH time)	^tSAS	10		10		12		ns	
Access time from $\overline{SE}$	^tSEA		15		20		30	ns	24
$\overline{SE}$ precharge time	^tSEP	10		15		15		ns	
$\overline{SE}$ pulse width	^tSE	10		15		15		ns	
Serial data-out hold time after SC high	^tSOH	5		5		5		ns	24
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	0	12	0	15	0	25	ns	24
Serial data-in setup time	^tSDS	0		0		0		ns	24
Serial data-in hold time	^tSDH	10		15		20		ns	24
Serial input (Write) Enable setup time	^tSWS	0		0		0		ns	
Serial input (Write) Enable hold time	^tSWH	10		15		20		ns	
Serial input (Write) Disable setup time	^tSWIS	0		0		0		ns	
Serial input (Write) Disable hold time	^tSWIH	10		15		20		ns	

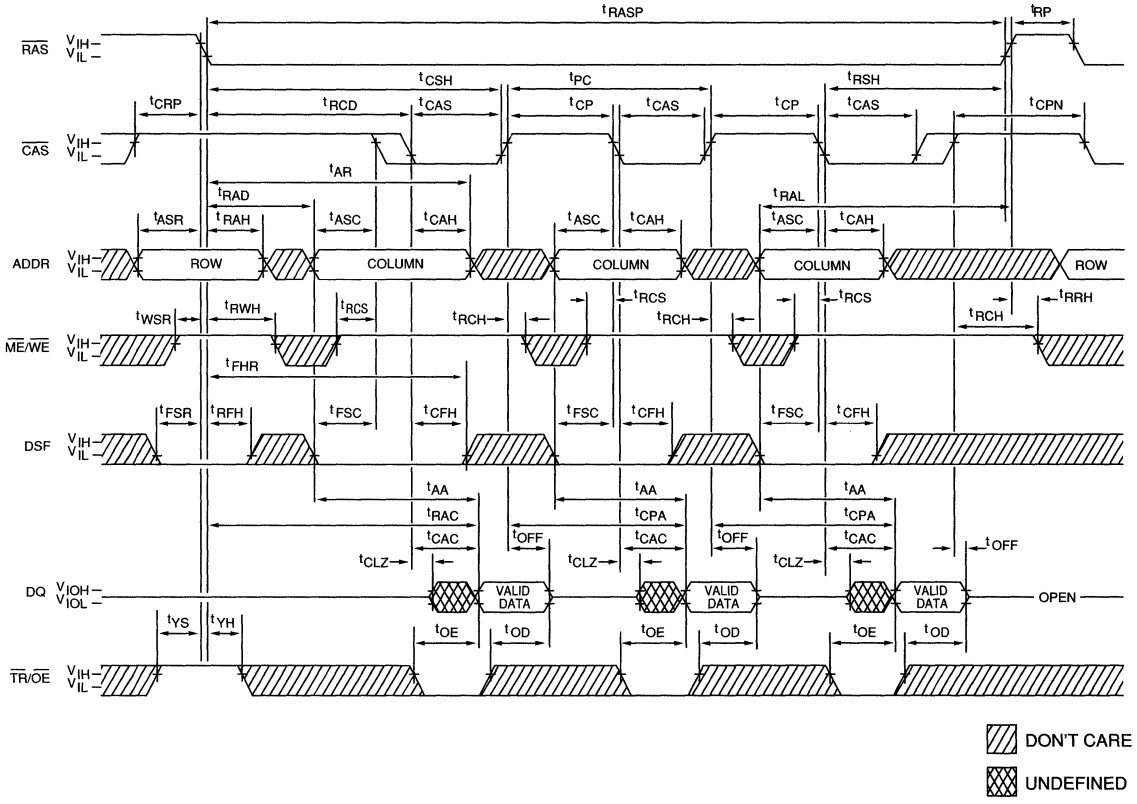
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, DRAM data output (DQ1-DQ8) is high impedance.
12. If $\overline{CAS} = V_{IL}$, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gates and 100pF. Output reference levels: $V_{OH} = 2.0V$; $V_{OL} = 0.8V$.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \le ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: $V_{OH} = 2.0V$; $V_{OL} = 0.8V$.
25. Transfer command means that $\overline{TR}/\overline{OE}$ is LOW when $\overline{RAS}$ goes LOW.
26. Non transfer command means that $\overline{TR}/\overline{OE}$ is HIGH when $\overline{RAS}$ goes LOW.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE



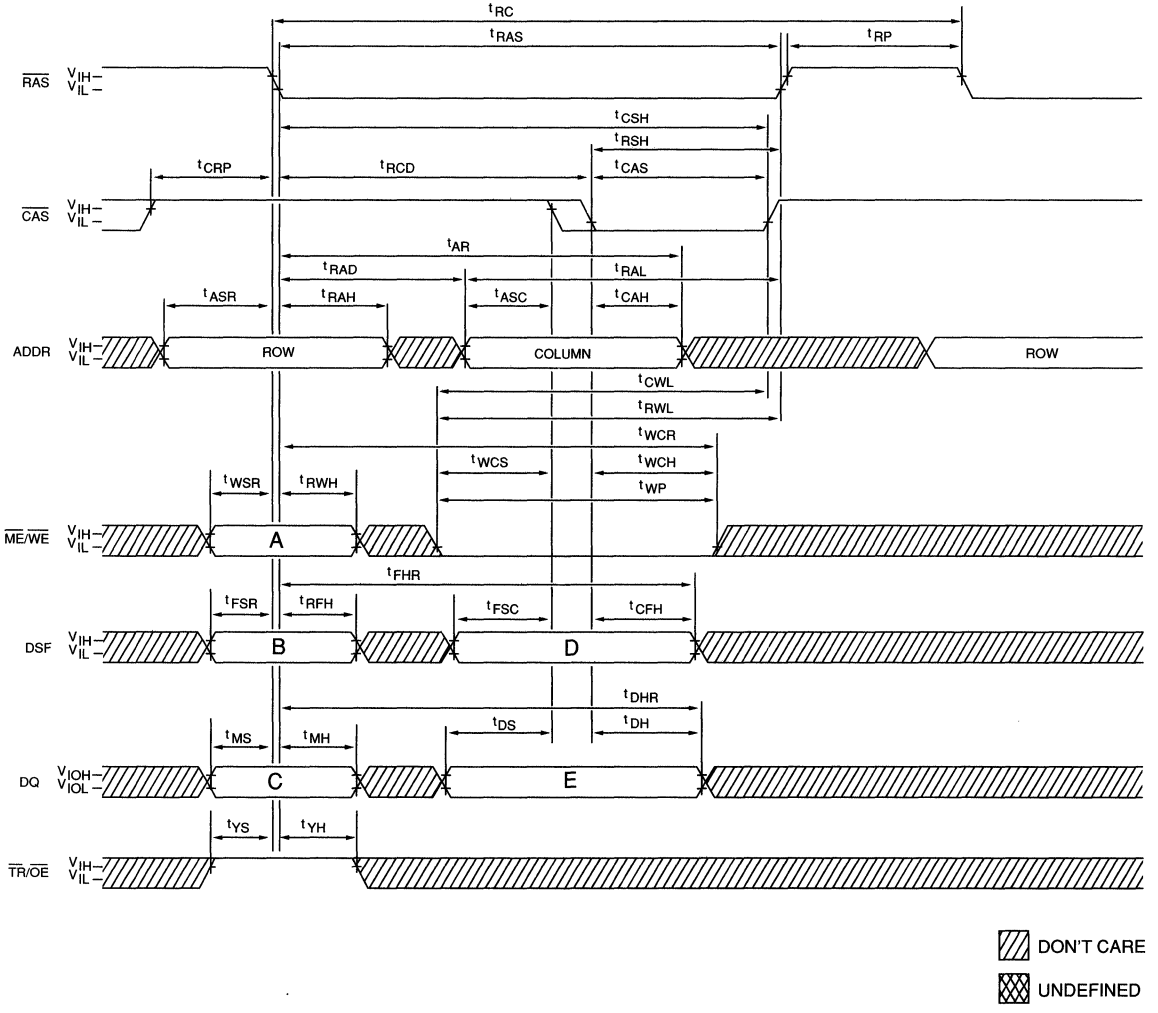
NOTE: 1. WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

WRITE CYCLE FUNCTION TABLE[1]

LOGIC STATES					FUNCTION
$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge		
A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E[2] DQ (Input)	
1	0	X	0	DRAM Data	Normal DRAM WRITE (or READ)
0	0	Write Mask	0	DRAM Data (Masked)	NONPERSISTENT (Load and Use) MASKED WRITE to DRAM
0	1	X	0	DRAM Data (Masked)	PERSISTENT (Use Register) MASKED WRITE to DRAM
1	0	X	1	Column Mask	BLOCK WRITE to DRAM (No Data Mask)
0	0	Write Mask	1	Column Mask	NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM
0	1	X	1	Column Mask	PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM
1	1	X	0	Write Mask	Load Mask Data Register
1	1	X	1	Color Data	Load Color Register

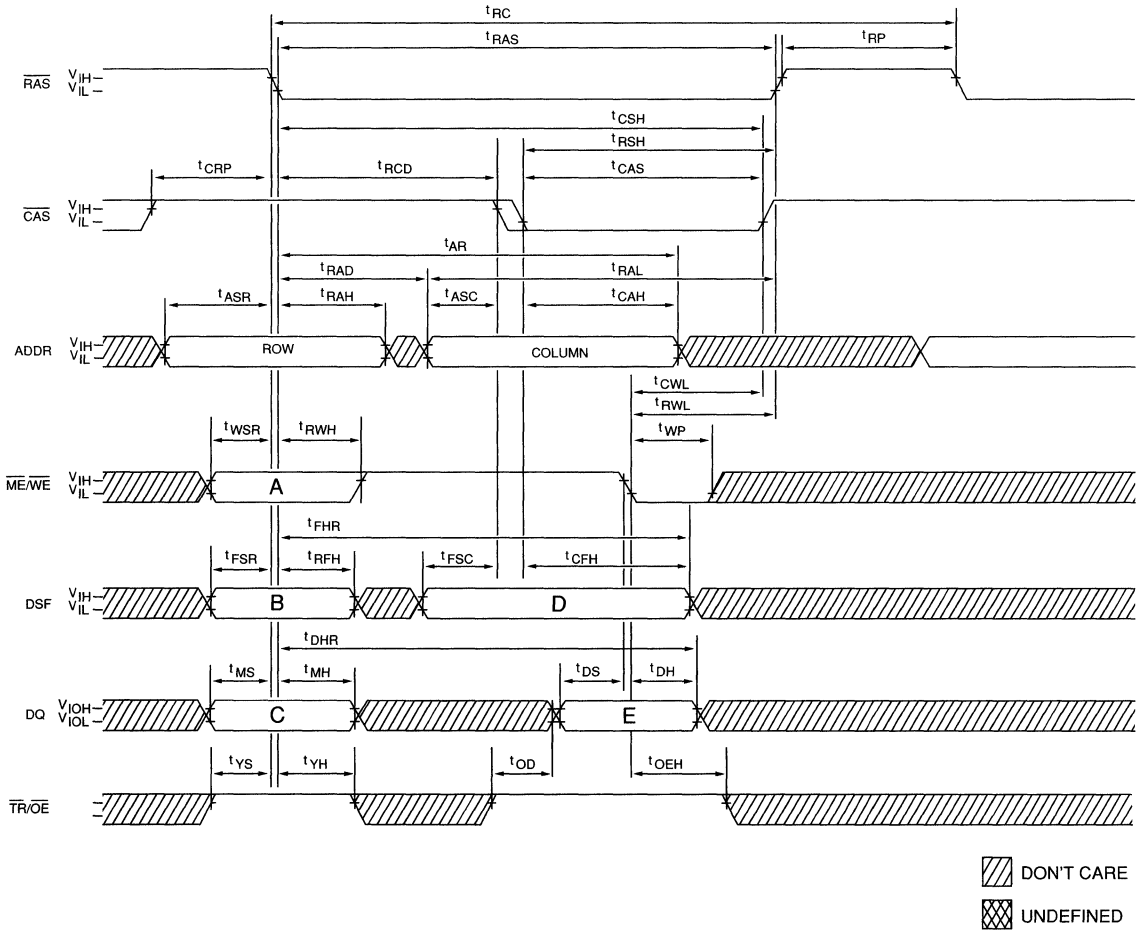
NOTE: 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
2. $\overline{CAS}$ or $\overline{ME}/\overline{WE}$, whichever occurs later.

DRAM EARLY-WRITE CYCLE[1]



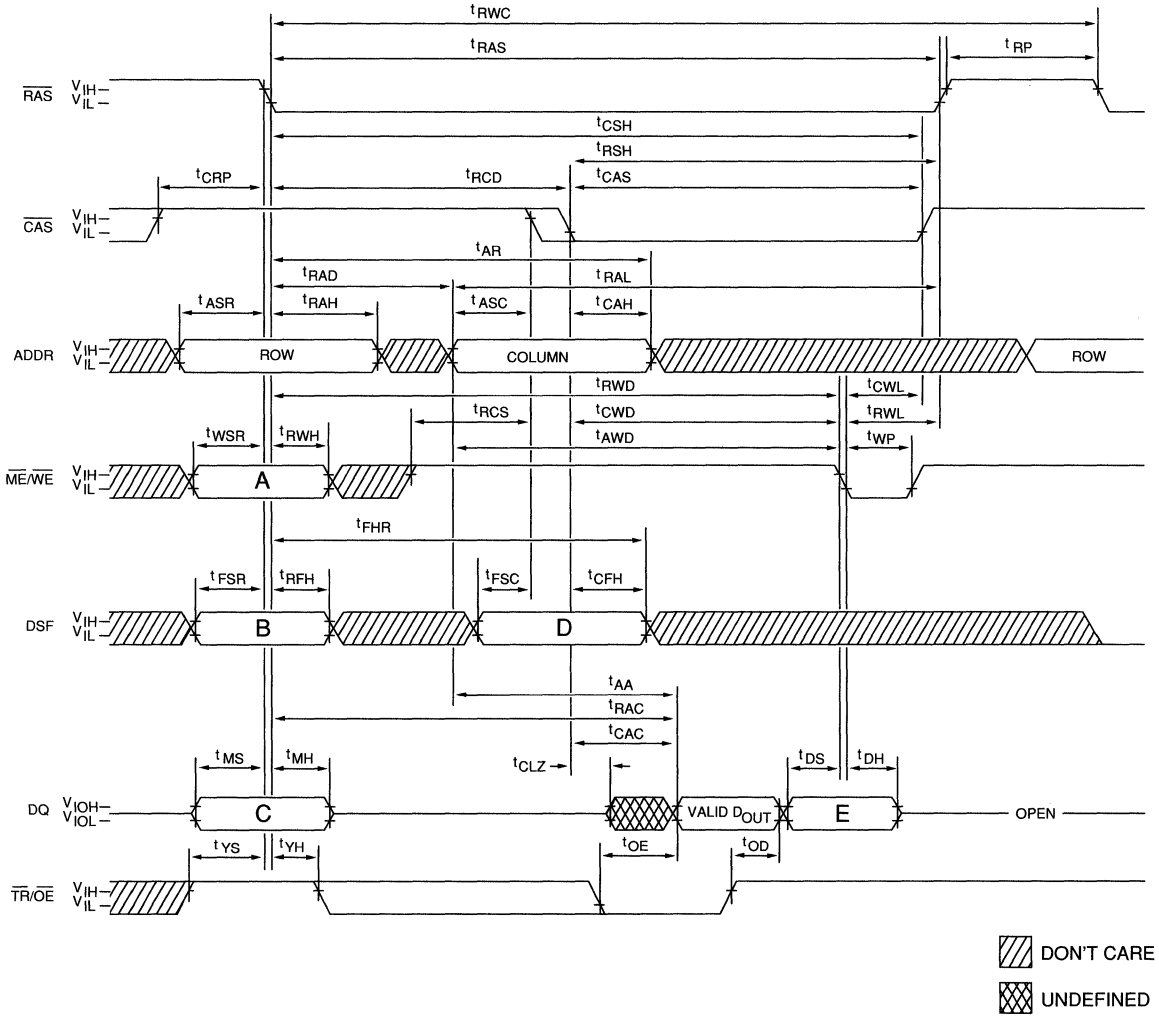
NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE



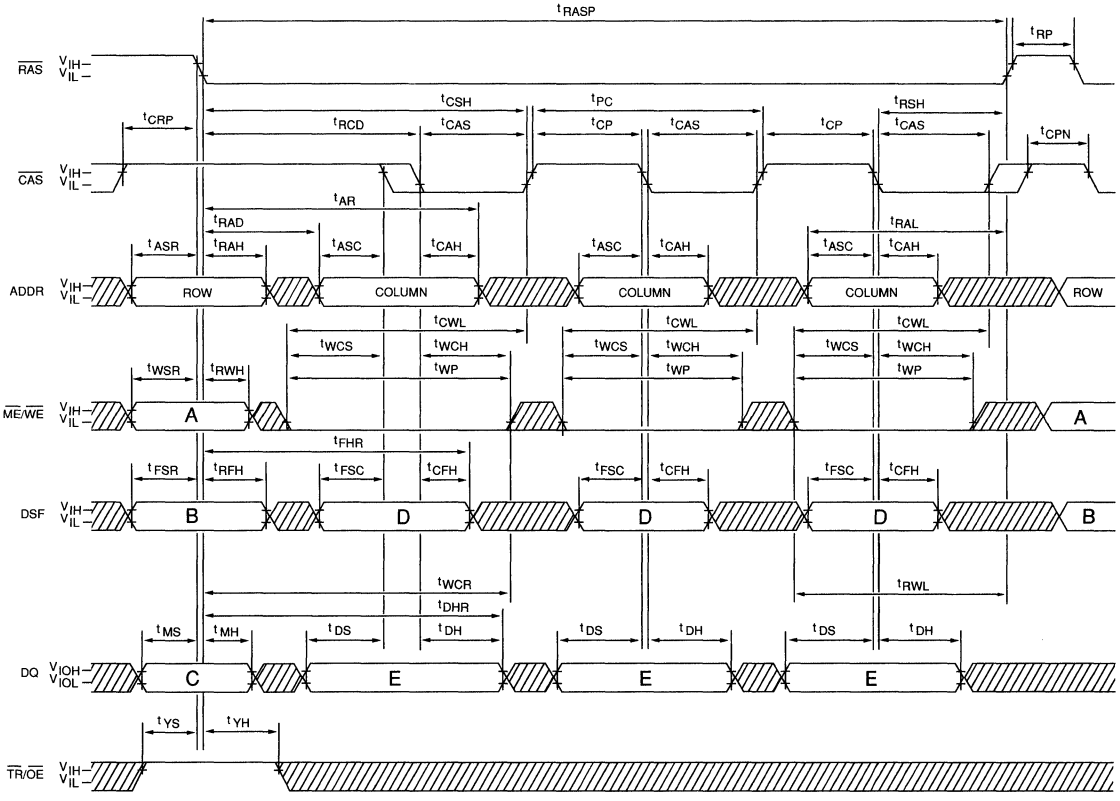
NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



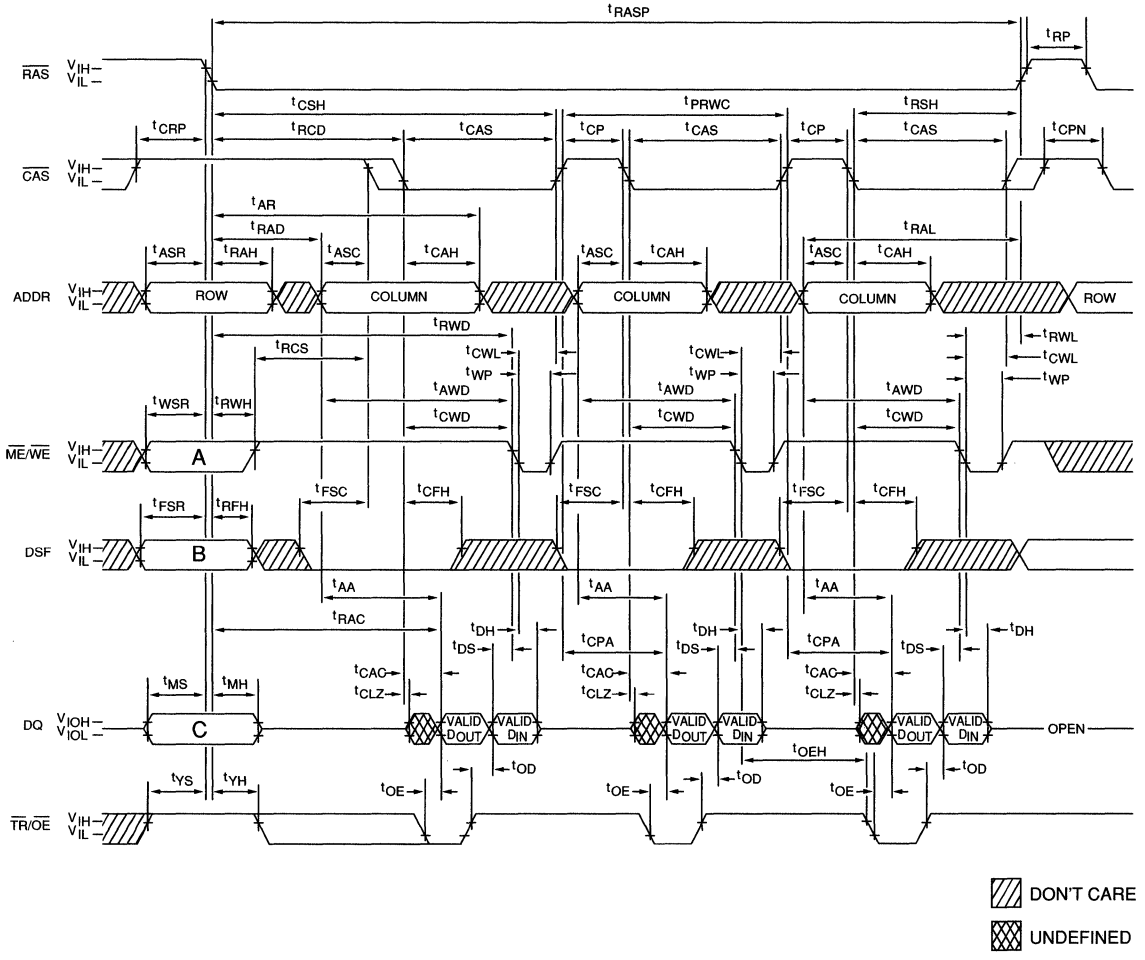
NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



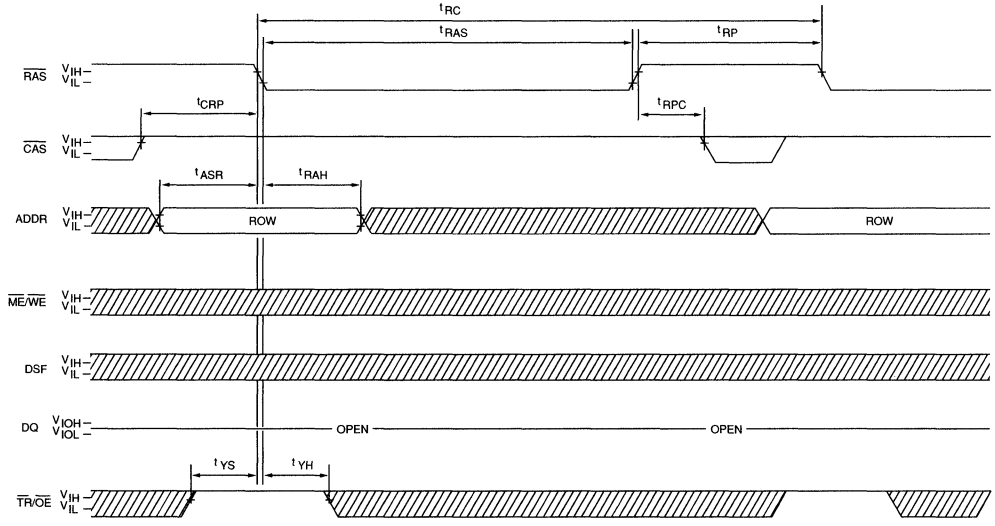
NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE OR LATE-WRITE CYCLES)

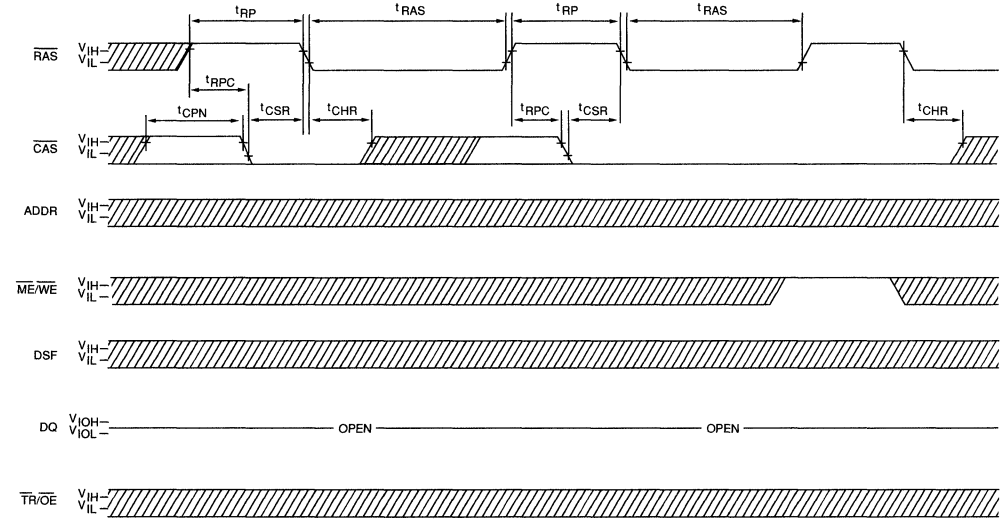


NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

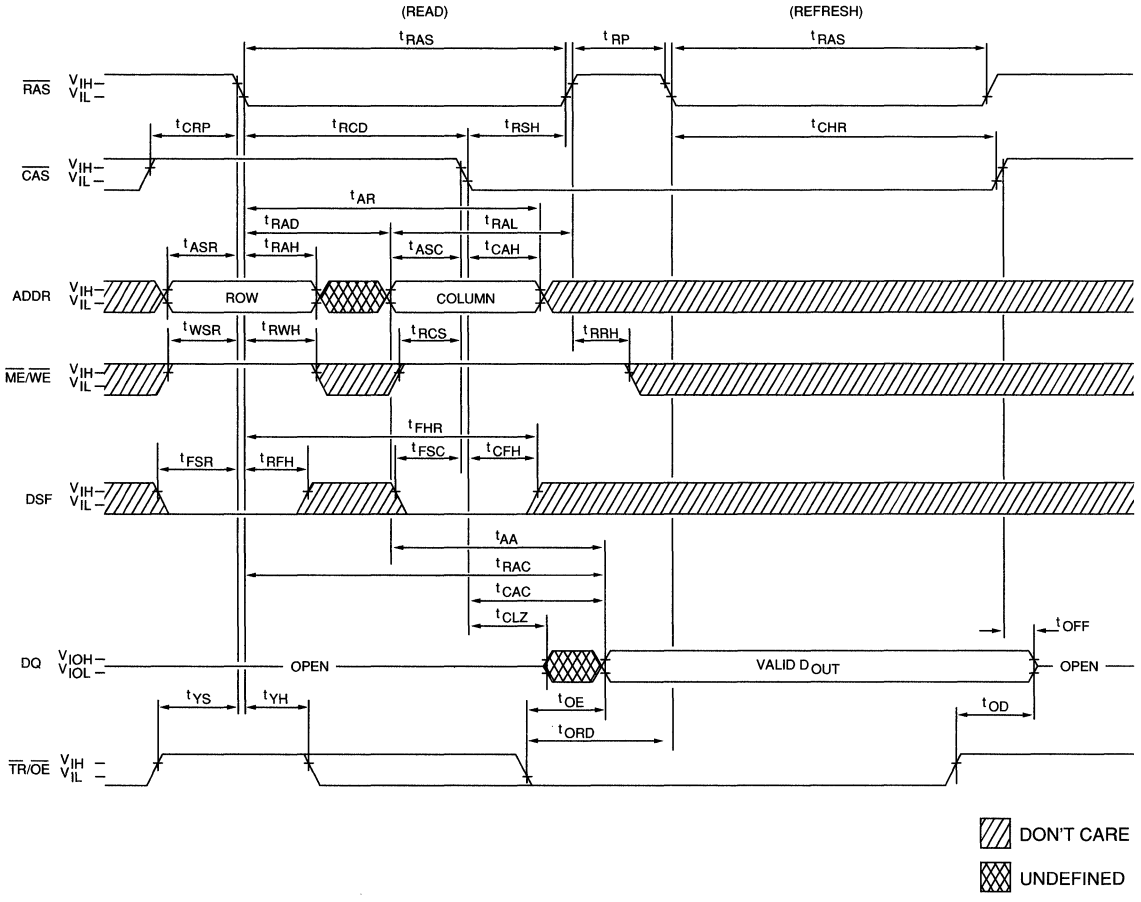
DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

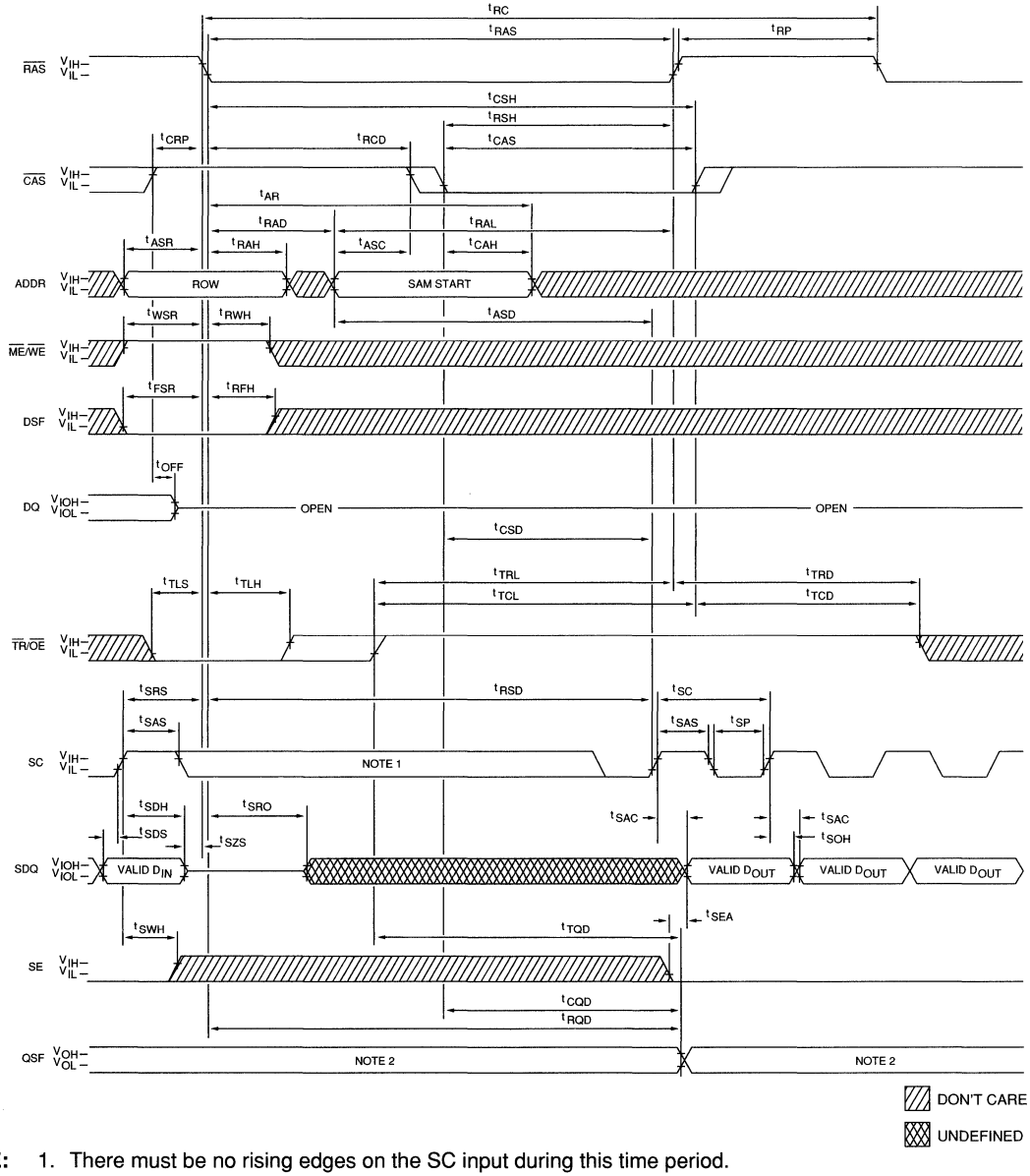


DRAM HIDDEN-REFRESH CYCLE



NOTE: 1. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH.

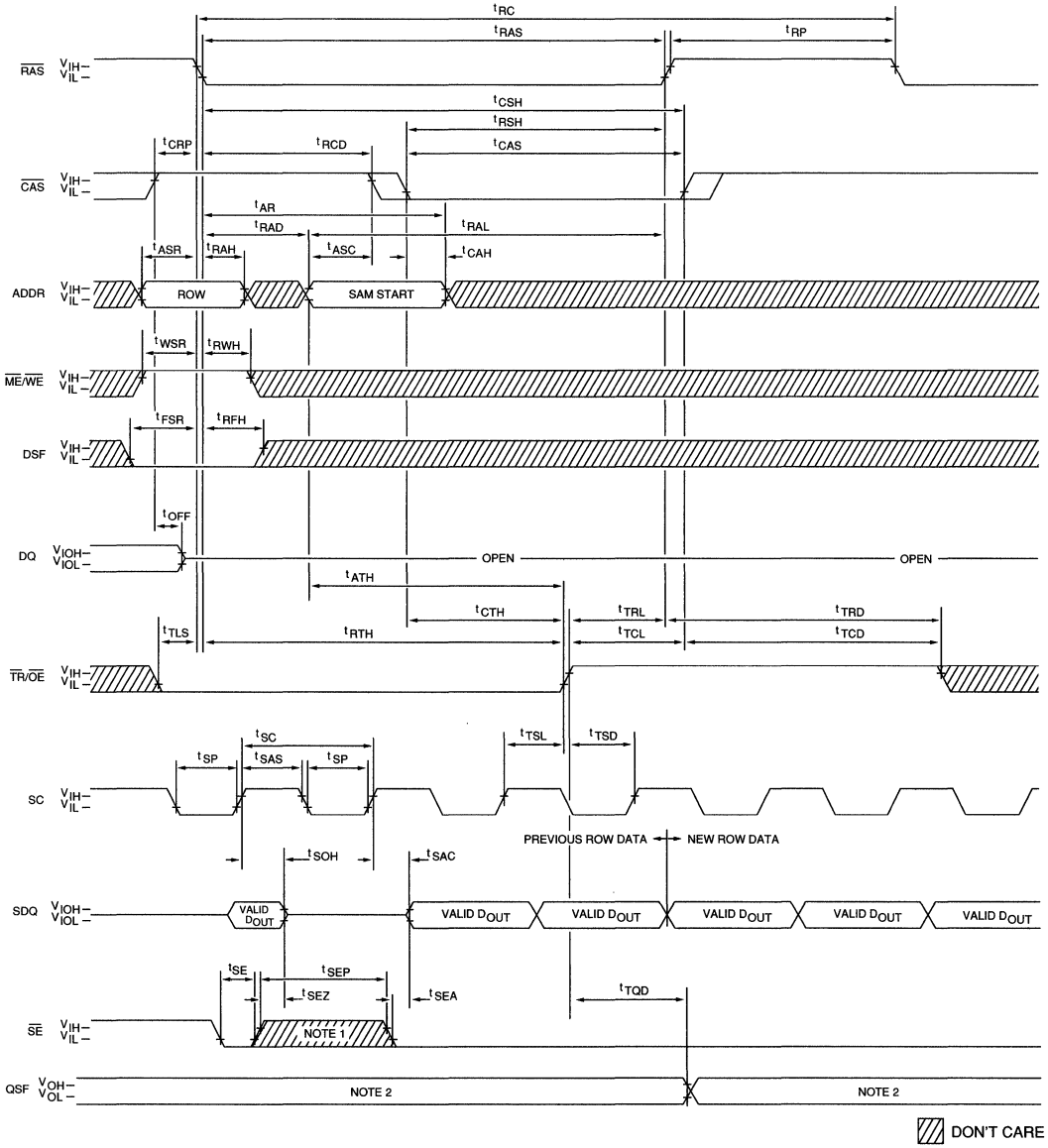
READ TRANSFER
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



NOTE: 1. There must be no rising edges on the SC input during this time period.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)

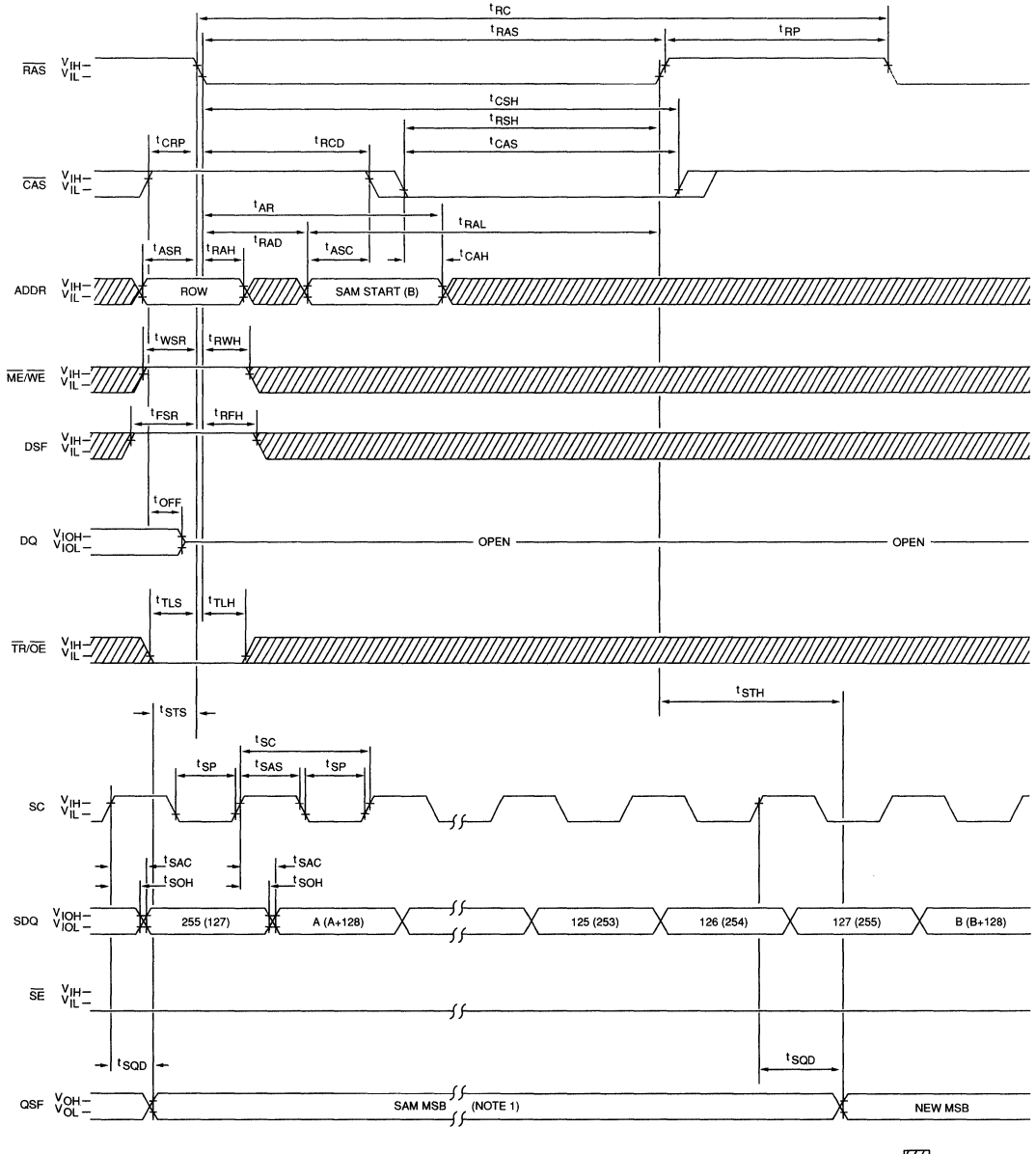
(When part was previously in the SERIAL OUTPUT mode)



NOTE: 1. The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

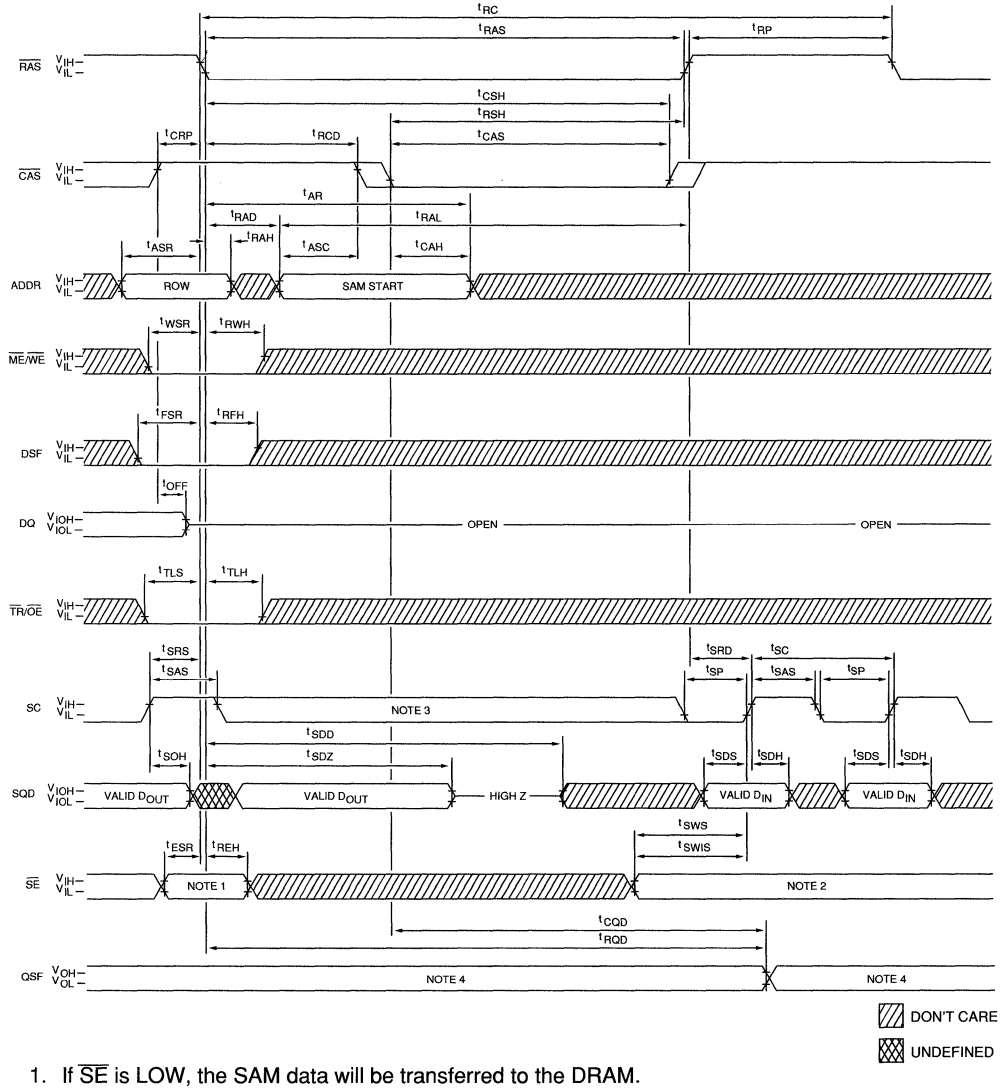
SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

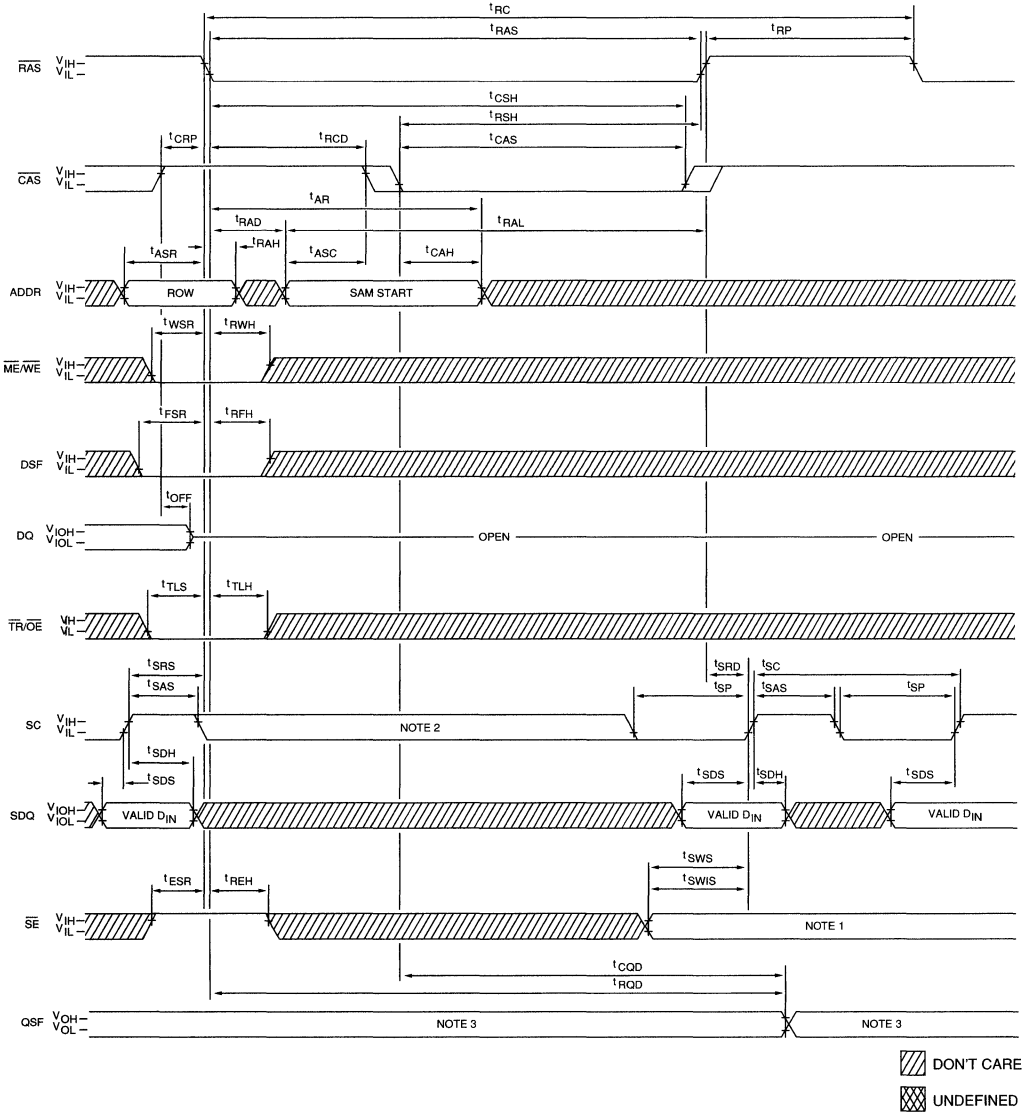
(When part was previously in the SERIAL OUTPUT mode)



NOTE:

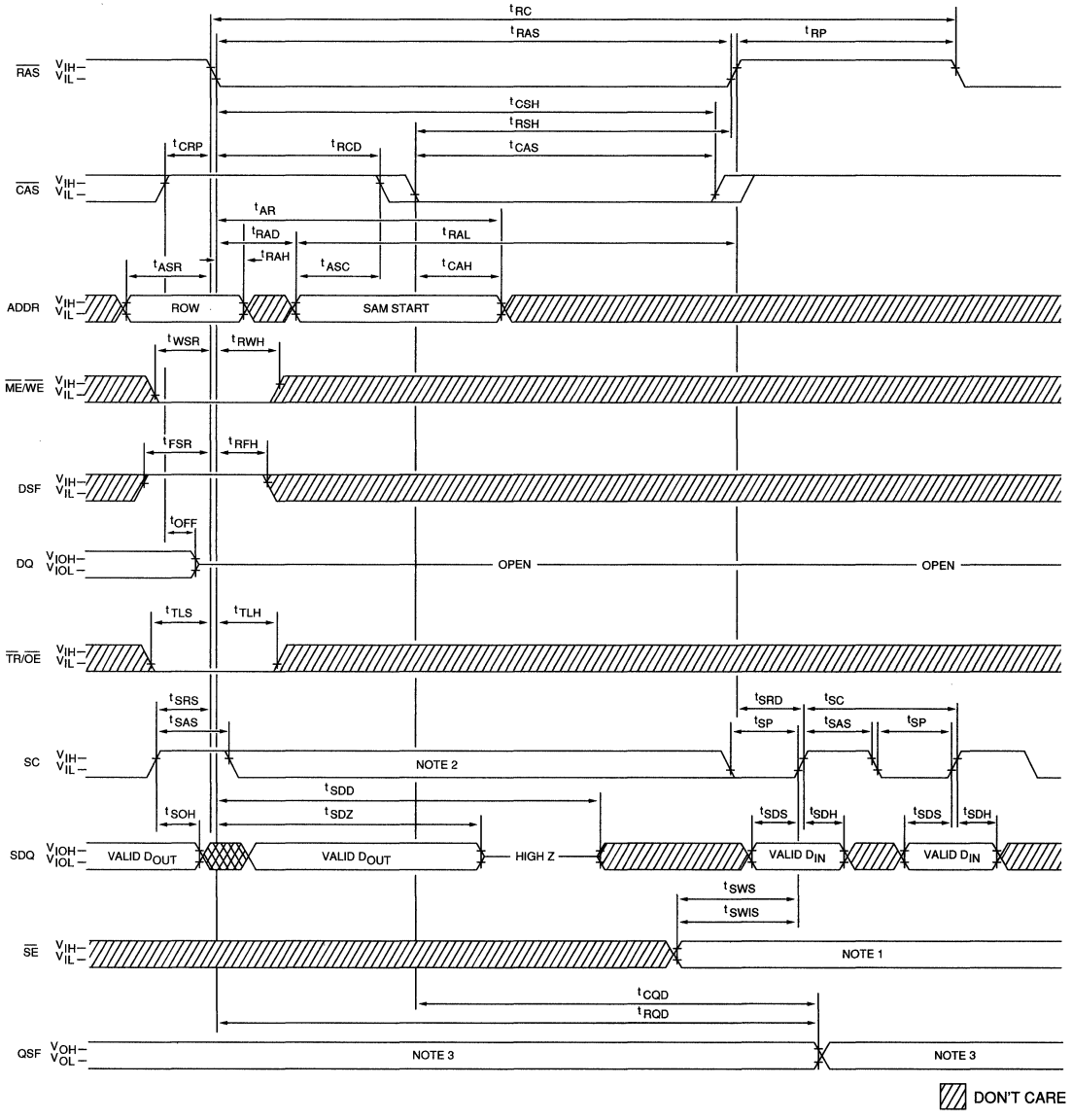
1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
   If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL-INPUT-MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. STS is LOW to select SAMa or HIGH to select SAMb
5. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



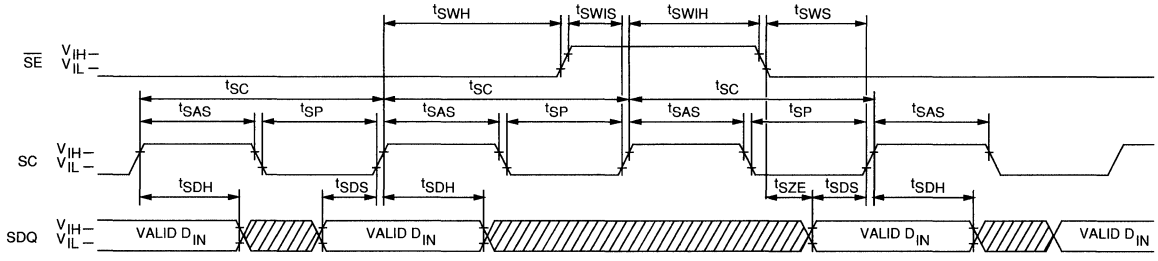
NOTE: 1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

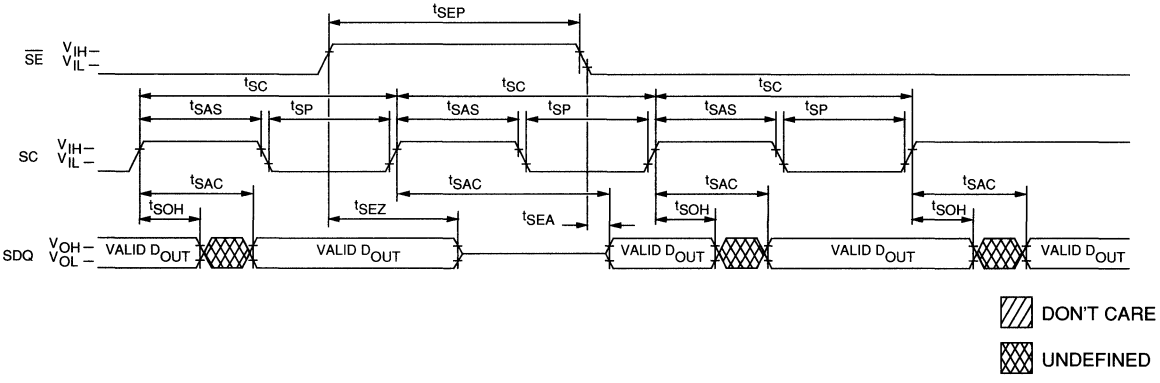


NOTE:
1. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
2. There must be no rising edges on the SC input during this time period.
3. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



DON'T CARE

UNDEFINED

VRAM

256K x 8 DRAM WITH 512 x 8 SAM

FEATURES

- Industry standard pin-out timing, and functions
- High-performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512-cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 256K x 8 DRAM port
  512 x 8 SAM port
- No refresh required for Serial Access Memory
- Low power: 20mW standby; 300mW active, typical
- Fast access times – 70ns random, 20ns serial

SPECIAL FUNCTIONS

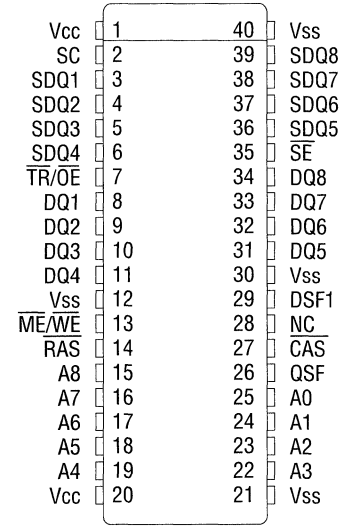
- JEDEC Standard Manditory Function set
- PERSISTENT MASKED WRITE
- MASKED WRITE TRANSFER/SERIAL INPUT
- MASKED SPLIT WRITE TRANSFER
- BLOCK WRITE (MASK)
- MASKED FLASH WRITE

OPTIONS

OPTIONS	MARKING
• Timing (DRAM, SAM)	
70ns, 20ns	- 7
80ns, 25ns	- 8
100ns, 30ns	-10
• Packages	
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(E-12)



GENERAL DESCRIPTION

The MT42C8256 is a high speed, dual port CMOS dynamic random access memory, or video RAM (VRAM) containing 2,097,152 bits. These bits may be accessed by an 8-bit wide DRAM port or by a 512 x 8 bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 8-bit DRAM), with the addition of MASKED WRITE, BLOCK WRITE and FLASH WRITE. Eight 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 512 bit wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the DPDRAM is fully static and does not require any refresh.

The operation and control of the MT42C8256 is similar to with the operation of the MT42C8128 (128K x 8 VRAM).

TRIPLE PORT DRAM

256K x 4 DRAM WITH DUAL 512 x 4 SAMS

FEATURES

- Three asynchronous, independent, data access ports
- Fast access times – 80ns random, 25ns serial
- Operation and control compatible with 1 Meg VRAMS
- High performance CMOS silicon gate process
- Low power: 15mW standby; 450mW active, typical
- 512-cycle refresh within 8ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, and HIDDEN
- FAST PAGE MODE access cycles
- Two, bidirectional Serial Access Memories (SAMs)
- Fully static SAM and Mask Register, no refresh required
- 2048-bit Transfer Mask Register
- SERIAL MASK DATA INPUT mode

SPECIAL FUNCTIONS

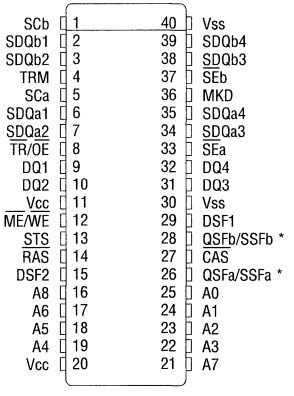
- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ and WRITE TRANSFERs
- BLOCK WRITE
- BIT MASKED TRANSFERs

OPTIONS / MARKING

- Timing (DRAM, SAMs)
  - 80ns, 25ns — -8
  - 100ns, 30ns — -10
  - 120ns, 35ns — -12
- Packages
  - Plastic SOJ (400 mil) — DJ
- Functionality
  - QSF output (indicates SAM-half accessed) — 43C4257
  - SSF input (Split SAM special function, stop count) — 43C4258

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(E-12)



* MT43C4257/MT43C4258

GENERAL DESCRIPTION

The MT43C4257/8 are high speed, triple port CMOS dynamic random access memories (TPDRAMs) containing 1,048,576 bits. Data may be accessed by a 4 bit wide DRAM port or by either of two independently clocked 512 x 4-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and either SAM.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4 DRAM). Eight 512-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 4-bit random access I/O port, the pair of internal 2048 bit wide paths between the DRAM and the SAMs, and the pair of 4-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing and address decoding logic.

All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 2048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 512 x 4-bit Bit Mask Data register can be parallel loaded from the DRAM, from either SAM, or serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of RAS addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require refresh.

The operation and control of the MT43C4257/8 are compatible with the operation of the MT42C4256 (256K x 4 Video RAM). However, the MT43C4257/8 offer an additional SAM and special features that may be used to enhance system performance.

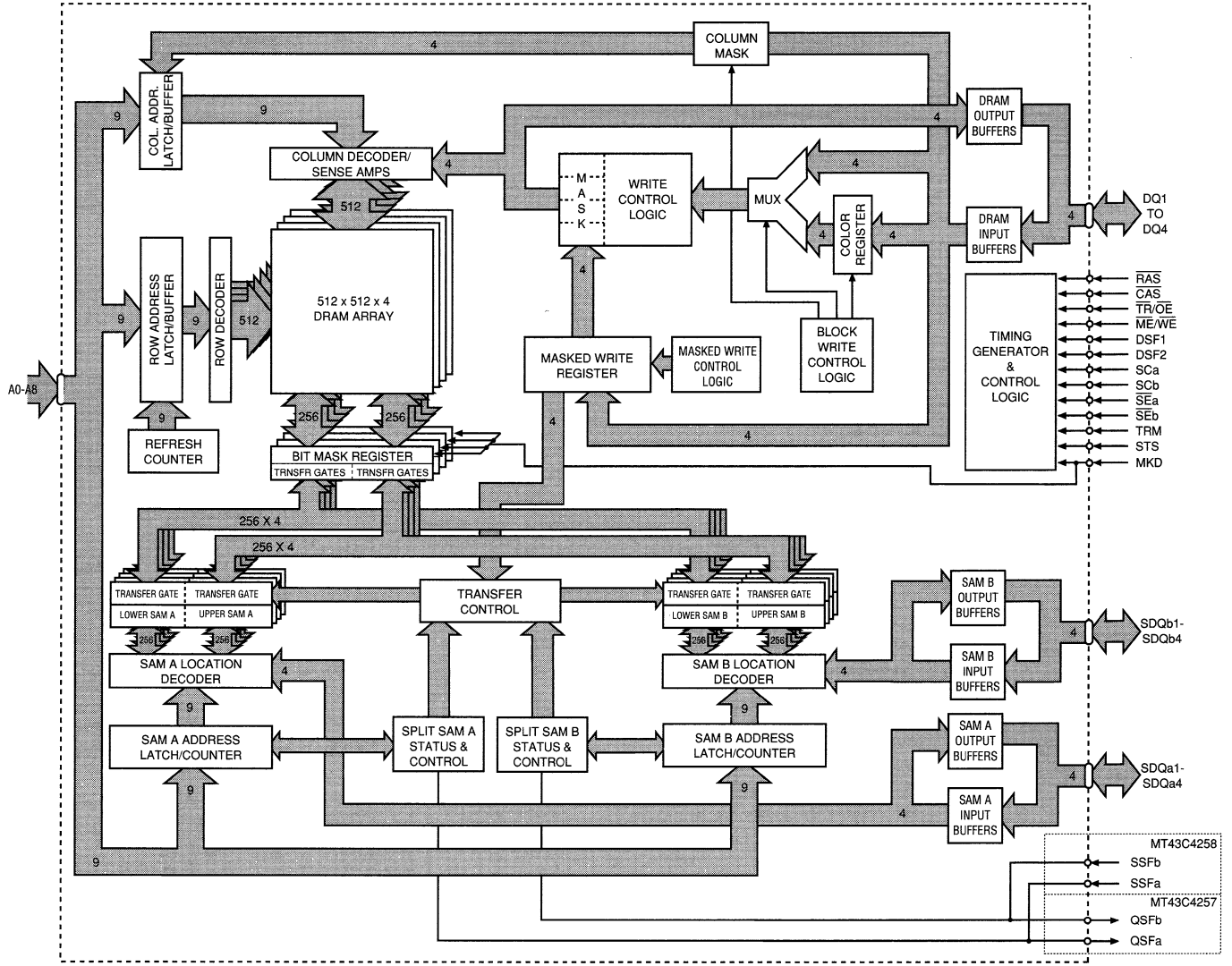


Figure 1
MT43C4257/8 BLOCK DIAGRAM

MULTIPORT DRAM

PIN DESCRIPTIONS

SOJ PIN NUMBER(S)	FUTURE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
5		SCa	Input	Serial Clock, SAMa: Clock input to the serial address counter for the SAMa registers and strobe for SAMa control and data inputs.
1		SCb	Input	Serial Clock, SAMb: Clock input to the serial address counter for the SAMb registers and strobe for SAMb control and data inputs.
8		$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at the falling edge of $\overline{RAS}$, or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a high impedance state.
12		$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
33		$\overline{SE}$a	Input	Serial Port Enable SAMa: $\overline{SE}$a enables Port A serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$a is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
37		$\overline{SE}$b	Input	Serial Port Enable, SAMb: $\overline{SE}$b enables Port B serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$b is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
29		DSF1	Input	Special Function (Control) 1: DSF1 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
15		DSF2	Input	Special Function (Control) 2: DSF2 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
14		$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and as a strobe for control and data inputs.
27		$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 9 column-address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and as a strobe for control and data inputs.

PIN DESCRIPTIONS (Continued)

SOJ PIN NUMBER(S)	FUTURE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25, 24, 23 22, 19, 18 17, 21, 16		A0 - A8	Input	Address Inputs: For DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 4-bit word out of the 256K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW).
13		STS	Input	SAM Transfer Select: The state of STS at $\overline{RAS}$ time determines which SAM is involved in a transfer (SAMa=LOW, SAMb=HIGH).
36		MKD	Input	Mask Data Input: MKD is used during BIT MASK REGISTER LOAD cycles to enable or disable the serial mask input mode (SMI). If SMI is enabled (MKD=HIGH at $\overline{RAS}$), then MKD is used as mask data input and is clocked by SCb into the mask data register.
4		TRM	Input	Transfer Mask Select: TRM is used to select between NORMAL TRANSFER cycles and BIT MASKED TRANSFER or BIT MASK REGISTER LOAD cycles.
9, 10, 31, 32		DQ1 - DQ4	Input/ Output	DRAM Data I/O: Data inputs and outputs for the DRAM memory array; inputs for the MASK and COLOR REGISTER load cycles; address mask inputs for BLOCK WRITE cycles.
6, 7, 34, 35		SDQa1-SDQa4	Input/ Output	Serial Data I/O, SAMa: Input, Output, or High-Z.
2, 3, 38, 39		SDQb1-SDQb4	Input/ Output	Serial Data I/O, SAMb: Input, Output, or High-Z.
26		QSFa/SSFa	Output Input	Split SAM Status, SAMa (MT43C4257): QSFa indicates which half of SAMa is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMa (MT43C4258): SSFa=HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFa is synchronized with SCa.
28		QSFb/SSFb	Output Input	Split SAM Status, SAMb (MT43C4257): QSFb indicates which half of SAMb is being accessed. (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMb (MT43C4258): SSFb=HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFb is synchronized with SCb.
11, 20		Vcc	Supply	Power Supply: +5V ±10%
30, 40		Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT43C4257/8 can be divided into four functional blocks (see Figure 1): the DRAM and its special functions, the Bit Mask Register (BMR), the two Serial Access Memories (SAMs), and the DRAM/SAM/BMR transfer circuitry. All the operations described below are also shown in the AC Timing Diagrams section of this data sheet and are summarized in the Functional Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

DRAM OPERATION

This section describes the operation of the random access port and the special functions associated with the DRAM.

DRAM REFRESH (ROR, CBR, and HR)

Like any DRAM-based memory, the MT43C4257/8 TPDRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT43C4257/8 supports $\overline{CAS}$-BEFORE-$\overline{RAS}$, $\overline{RAS}$ ONLY and HIDDEN types of refresh cycles.

For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH cycle, the row-addresses are generated and stored in an internal address counter. The user need not supply any address data and simply must perform 512 $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles within the 8ms time period.

For $\overline{RAS}$-ONLY REFRESH cycles, the refresh address must be generated externally and applied to the A0-A8 inputs . The DQ pins remain in a High-Z state for both the $\overline{RAS}$-ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles.

HIDDEN REFRESH (HR) cycles are performed by toggling $\overline{RAS}$ (while keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM and Bit Mask Register portions of the MT43C4257/8 are fully static and do not require any refreshing.

DRAM READ AND WRITE CYCLES (RW)

The DRAM portion of the TPDRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this device, several conditions that were undefined or "don't care" states for the DRAM are specified for the TPDRAM. These conditions are highlighted in the following discussion. In addition, the TPDRAM has several special functions that may be used when writing to the DRAM.

The 18 address bits used to select a 4-bit word from the 262,144 available are latched into the chip using the A0-A8, $\overline{RAS}$, and $\overline{CAS}$ inputs. First, the 9 row-address bits are setup on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 9 column-address bits are setup on the address inputs and clocked in when $\overline{CAS}$ goes from HIGH to LOW.

For single port DRAMS, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. For the TPDRAM, $(\overline{TR})/\overline{OE}$ is used when $\overline{RAS}$ goes LOW, to select between DRAM and TRANSFER cycles. $(\overline{TR})/\overline{OE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition for all DRAM operations.

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH to LOW sometime after $\overline{RAS}$ falls to enable the DRAM output port.

For single port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the TPDRAM, $\overline{ME}/(\overline{WE})$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle or a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH to LOW transition, a MASKED WRITE operation is selected. For any TPDRAM non-masked access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW when $\overline{CAS}$ goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells.

The TPDRAM can perform all the normal DRAM cycles: READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE, and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

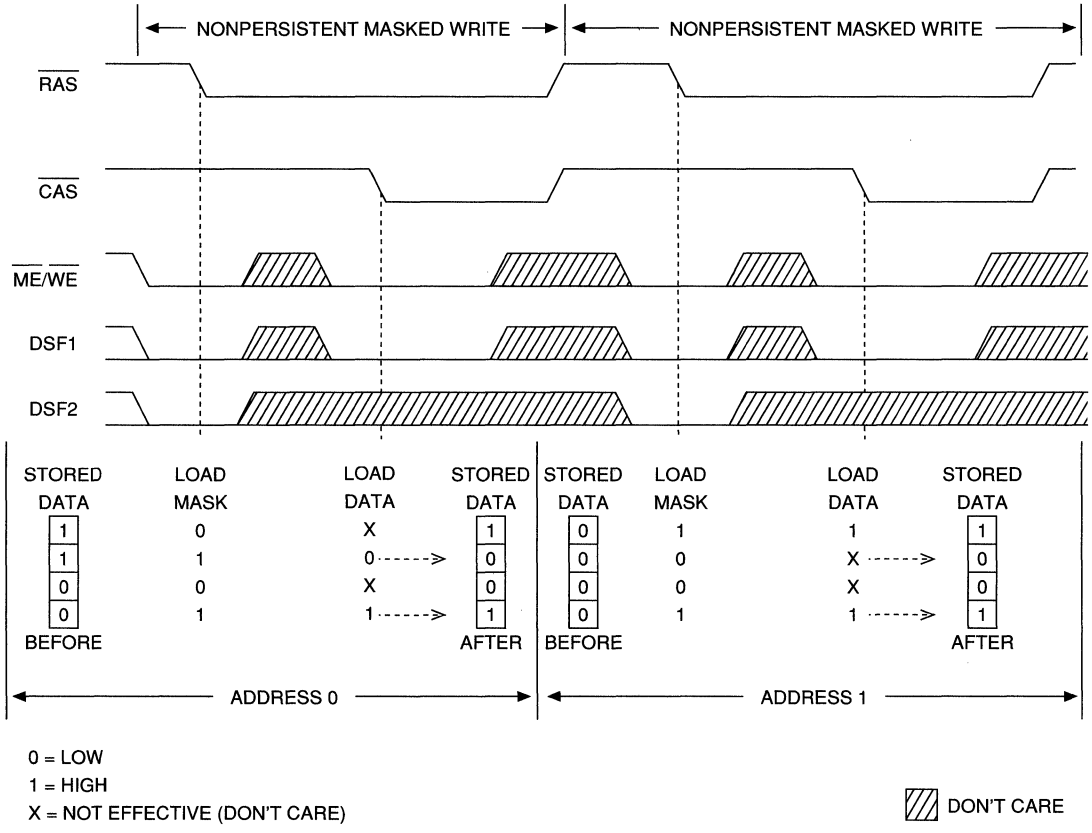


Figure 2
NONPERSISTENT MASKED WRITE EXAMPLE

NONPERSISTENT MASKED WRITE (RWNM)

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within a 4-bit word. The MT43C4257/8 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$), DSF1 and DSF2 are LOW at the $\overline{RAS}$ HIGH to LOW transition, the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. This convention is used for all masks on the MT43C4257/8. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. When using NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is loaded into the mask data register at every falling edge of $\overline{RAS}$. FAST PAGE MODE can be used in tandem with NONPERSISTENT MASKED WRITE to write several column locations using the same mask during one $\overline{RAS}$ cycle. An example of NONPERSISTENT MASKED WRITE cycle is shown in Figure 2.

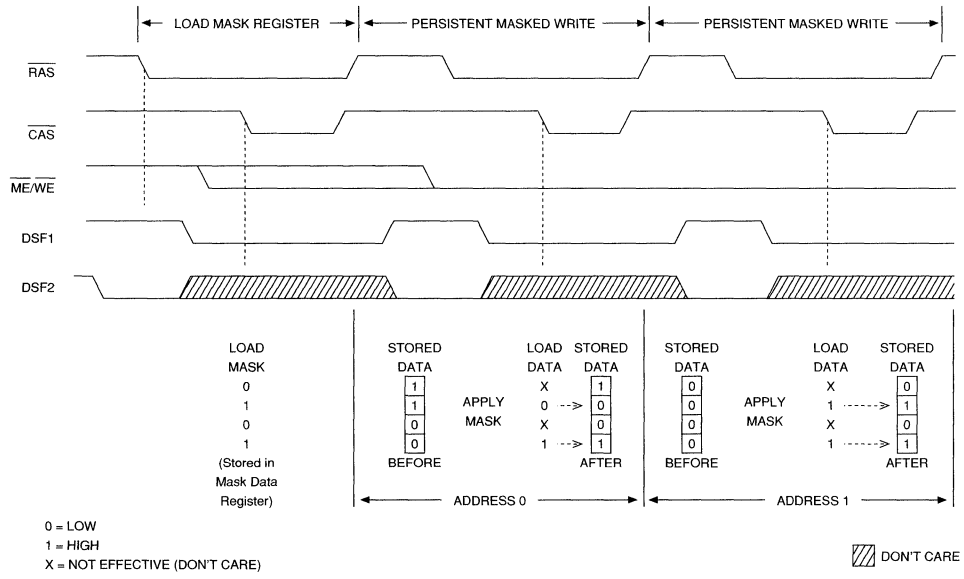


Figure 3
PERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE (RWOM)

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}$/($\overline{WE}$) and DSF1 HIGH, and DSF2 LOW when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW, provided DSF1 is LOW (see the LOAD MASK REGISTER description).

Mask data may also be loaded into the mask register by simply performing a NONPERSISTENT MASKED WRITE before the PERSISTENT MASKED WRITE cycles.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}$/($\overline{WE}$) and DSF2 LOW and DSF1 HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present at the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls. Another PERSISTENT MASKED WRITE cycle may be performed without reloading the register. Figure 3 shows the LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycle operations. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow systems that cannot output data at $\overline{RAS}$ time to perform MASKED WRITE cycles. PERSISTENT MASKED WRITE can also operate in FAST PAGE MODE.

BLOCK WRITE (BW)

If DSF1 is HIGH when $\overline{CAS}$ goes LOW, the MT43C4257/8 will perform a BLOCK WRITE cycle ($\overline{WE}$ = "don't care") instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register (instead of the DQ inputs) are directly written to four adjacent column locations (see Figure 4). A total of 16 bits will be written simultaneously, improving the normal DRAM fill rate by four times. The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" (out of the 128 possible) of four adjacent column locations that will be accessed. When $\overline{CAS}$ goes LOW, the DQ inputs are then used to determine which combination of the four column locations will be changed. DQ1 acts as a write enable for column location A0=0, A1=0; DQ2 controls column location A0=1, A1=0; DQ3 controls A0=0, A1=1; and DQ4 controls A0=1, A1=1. The write enable controls are active HIGH; a logic 1 enables and a logic 0 disables the WRITE function.

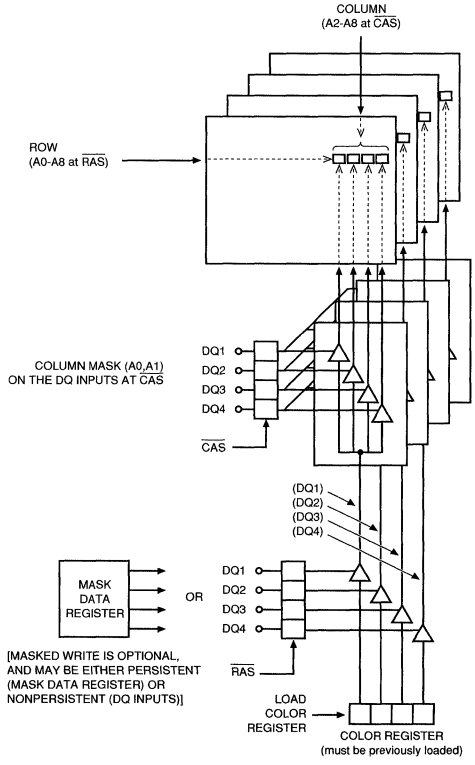


Figure 4
BLOCK WRITE EXAMPLE

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane. The DQ mask is not used in this mode.

Note: *When performing a BLOCK WRITE, $\overline{WE}$ is a "don't care". This means LATE-WRITEs in the BW mode are not allowed.*

NONPERSISTENT MASKED BLOCK WRITE (BWNM)

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}/(\overline{WE})$ LOW and DSF1 LOW when $\overline{RAS}$ goes LOW, initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH, when $\overline{CAS}$ goes LOW to perform a NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes may be masked and any combination of the four column locations may be masked.

PERSISTENT MASKED BLOCK WRITE (BWOM)

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF1 is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

DRAM REGISTER OPERATIONS

The MT43C4257/8 contains two 4-bit registers that are used as data registers for special functions. This section describes how to load these registers.

LOAD MASK REGISTER (LMR)

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF1 is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF1 being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a REGISTER load cycle. DSF1 is used when $\overline{CAS}$ goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NONPERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the four DQ planes.

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF1 is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

This section describes transfer operations between the DRAM and either SAM. The direction of the transfer is specified with respect the DRAM portion of the device. A write is referenced to the DRAM array and a read is referenced from the array.

Note: *The three ports of the TPDRAM are independent and asynchronous to one another. Any or all of the ports may be accessed simultaneously at the maximum allowable frequencies. The only time the ports are synchronized is during transfers to or from the DRAM and SAM portions of the device. A transfer involving a SAM does not affect access from the other SAM port. Both SAMs may be accessed during a DRAM/BMR transfer operation or any other DRAM access cycle other than a SAM transfer.*

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of STS when $\overline{RAS}$ goes LOW indicates which SAM the TRANSFER will address. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER. At the same time, DSF1 is used to select between normal TRANSFER cycles and SPLIT TRANSFER cycles and DSF2 is used to select between normal TRANSFER cycles and MASKED TRANSFER cycles. A TRANSFER cycle can be performed without dropping $\overline{CAS}$. In this case, the previously loaded Tap address will be used.

The MT43C4257/8 include a feature called BIT MASKED TRANSFER, which uses a third, 2048-bit data register to individually mask every bit involved in a transfer operation. The BIT MASKED TRANSFER may be applied to either READ or WRITE TRANSFERS. The TRM pin is used to select between NORMAL and BIT MASKED TRANSFER (or BIT MASK REGISTER LOAD) cycles. The type of transfer operation is always selected on the falling edge of $\overline{RAS}$.

NORMAL TRANSFERS

The MT43C4257/8 support all of the popular transfer cycles available on the 1 Meg Video RAMs. Each of these is described in the following section.

READ TRANSFER (RT)

A READ TRANSFER cycle is selected if $\overline{ME}/(\overline{WE})$ is HIGH, and DSF1 and $\overline{TR}/(\overline{OE})$ are LOW when $\overline{RAS}$ goes LOW. When $\overline{RAS}$ goes LOW, the READ TRANSFER is to SAMa if STS = LOW, or to SAMb if STS = HIGH. The row address bits indicate the four 512-bit DRAM rows that are to be transferred to the four SAM data registers. The column address bits indicate the start address (or Tap point) of the next serial output cycle from the designated SAM data registers. QSF indicates the SAM half being accessed; LOW if the lower half, HIGH if the upper. Performing a READ TRANSFER cycle sets the direction of the selected SAM's I/O buffers to the output mode.

To complete a REAL-TIME READ-TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are LOW. In order to synchronize the REAL-TIME READ TRANSFER to the serial clock, the rising edge of $\overline{TR}/(\overline{OE})$ must occur between the rising edges of successive clocks on the SC input (refer to the AC timing diagrams). A "regular" READ TRANSFER is not sychronized with the SC pin of the addressed SAM. This type of RT is performed when $\overline{TR}/(\overline{OE})$ is taken HIGH "early," without regard to the falling edge of $\overline{CAS}$. The transfer will be completed internally by the device. The first serial clock must meet the tRSD, tCSD and tASD delays. (see READ TRANSFER AC timing diagram). The 2048 bits of DRAM data are then written into the SAM data registers and the selected SAM's Tap address that was stored in the internal, 9-bit Tap address register is loaded into the address counter. If $\overline{SE}$ for the SAM selected ($\overline{SE}$a for SAMa) is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. $\overline{SE}$ enables the serial outputs, and may be either HIGH or LOW during this operation.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream (the "full" READ TRANSFER cycle has to occur immediately after the final bit of "old data," and before the first bit of "new data" is clocked out the SAM port).

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data can be transferred to the other half. The transfer can occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is relaxed for SRT cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ and $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles.

SPLIT TRANSFERs do not change the SAM I/O direction. A normal (non-split) READ TRANSFER cycle must precede any sequence of SRT cycles to put the SAM I/O in the output mode and provide the initial SAM Tap address (which half). Then an SRT can be initiated by taking DSF1 HIGH and selecting the desired SAM (using STS) when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. When an SRT cycle is initiated, the half of the SAM not actively being accessed will be the half

that receives the transfer. When $\overline{CAS}$ falls, address pins A0-A7 determine the Tap address for the SAM-half selected; A8 = "don't care." If $\overline{CAS}$ does not fall, the previously loaded Tap address will be reused and the TRANSFER will be to the idle half.

Figure 5 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The purpose of the SRT from the same row is to initiate the split SAM operating mode and load the Tap address for the upper half of the SAM. For the MT43C4257, serial access continues and when the SAM address counter reaches 255 ("A8"=1, A0-A7=0), the QSF output for that SAM goes HIGH and the Tap address for the upper half is automatically loaded. Since the serial access has now switched to the upper half of the SAM, new data may now be transferred to the lower half. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed may now be repeated. For example, the next step in Figure 5 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transferring the upper half of row 1 to the upper SAM. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address load for the addressed SAM will be reused.

The split SAM operation is slightly different for the MT43C4258. Instead of having a QSF, this device has a Split SAM Special Function (SSF) input. With this input the serial access may be switched at will from one half of the SAM to the other. In other words, the address count may be stopped on the current half and the Tap address of the next half may be loaded, without waiting for the maximum address count of the current half (255; lower, 511; upper). If no SSF pulse is applied, the Tap address of the next half will be automatically loaded when the maximum count of the current SAM-half is reached. QSF = 0 when the Lower SAM (bits 0–255) is being accessed. QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

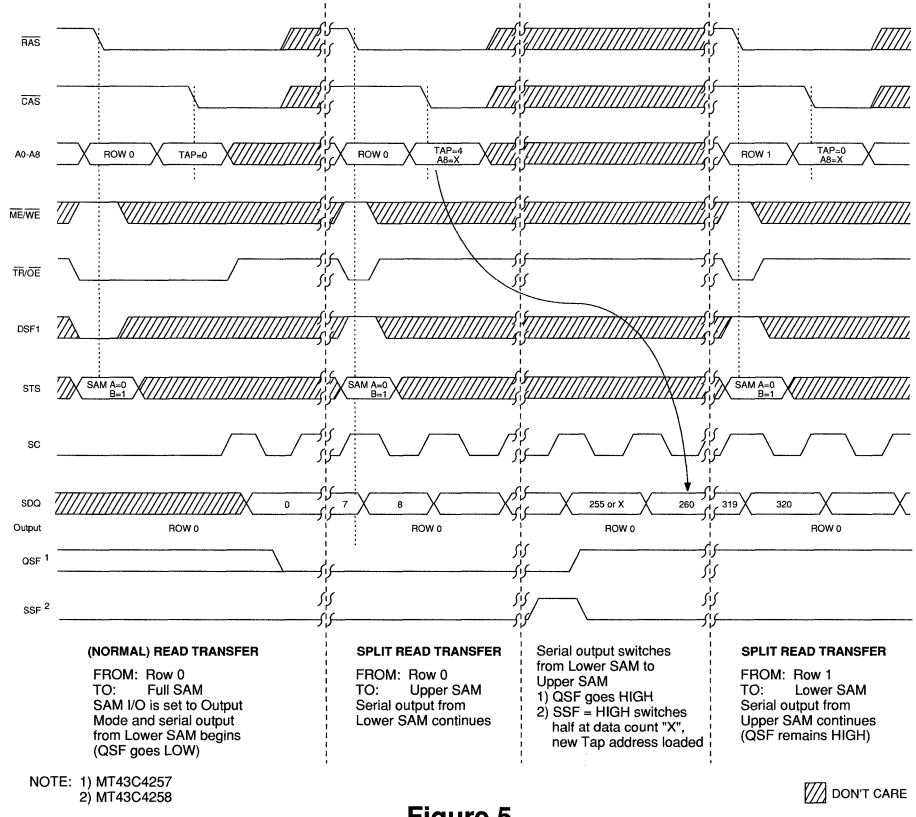


Figure 5
TYPICAL SPLIT READ TRANSFER INITIATION SEQUENCE

WRITE TRANSFER (WT)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously, except ($\overline{ME}$)/$\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The DSF2 input is used to select between the WT and DQ MASKED WRITE TRANSFER cycles, and must be LOW for the WT cycle. The STS pin is also taken LOW or HIGH to select SAMa or SAMb, respectively, when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data register will be written, and the Tap address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. QSF indicates the SAM half being accessed; LOW if the lower half, HIGH if the upper. Performing a WT sets the direction of the SAM I/O buffers to the input mode.

PSEUDO WRITE TRANSFER (PWT)

The PSEUDO WRITE TRANSFER cycle can be used to change the direction of a SAM port from output to input without disturbing the DRAM data in the selected row. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with the $\overline{SE}$ of the appropriate SAM held HIGH instead of LOW. The addressed row will be refreshed. A DQ MASKED WRITE TRANSFER (with all bits masked) is an alternate method for changing the direction of the SAM port without disturbing the addressed row data.

DQ MASKED WRITE TRANSFER (DMWT)

The data being transferred from either SAM to the DRAM may be masked by performing a DQ MASKED WRITE TRANSFER cycle. The transfer of data may be selectively enabled for each of the four DQ planes (see Figure 6). The DMWT cycle is identical to the WRITE TRANSFER cycle except DSF2 is HIGH and mask data must be on the DQ inputs at the falling edge of $\overline{RAS}$.

The complete SAM register will be transferred to the selected row in each DQ plane if the mask data input is HIGH, and the SAM register will not be transferred if the mask data input for that DQ plane is LOW. DRAM data is not disturbed in masked DQ planes.

SPLIT WRITE TRANSFER (SWT)

The SPLIT WRITE TRANSFER feature makes it possible to input and transfer uninterrupted bit streams. Figure 7 shows a typical initiation sequence for SWT cycles.

Like the SRT, the SPLIT WRITE TRANSFER cycle does not change the state of the SAM I/O buffers. A normal, DQ MASKED or PSEUDO WRITE TRANSFER cycle is required to set the Tap address and set the SAM I/O direction to input mode.

After the WT, a SWT is performed to enter the split SAM operating mode. This sets the Tap for the next half of the SAM. The addressed half of the SAM is immediately transferred to the first destination row. This half of the SAM may not yet contain valid data. However, another SWT to the same row will normally occur after this is loaded, so the initial invalid data will be overwritten. Another approach would be to initiate an SWT addressed to any DRAM row, but mask (disable) all four of the DQ planes. This method can be used to initiate the SWT sequence without disturbing any DRAM data.

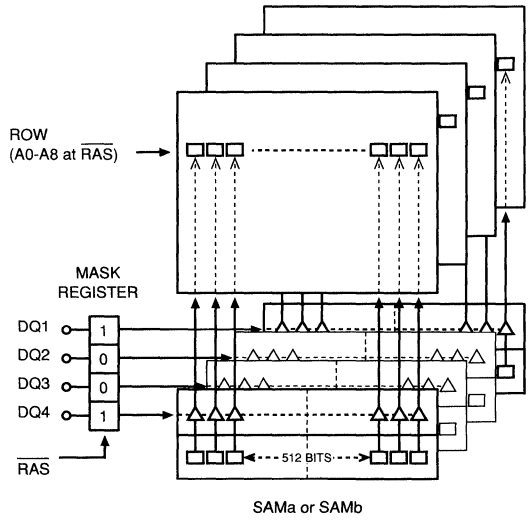


Figure 6
DQ MASKED WRITE TRANSFER

Write mask data must be supplied to the DQ inputs during every SWT cycle at $\overline{RAS}$ time. The mask data acts as an individual write enable for each of the four DRAM DQ planes. For example, the DQ1 MASKED WRITE bit enables or disables the transfer of the SAM SDQ1 register to the DQ1 plane of the DRAM row selected (see the DQ MASKED WRITE TRANSFER description). As in all other MASKED WRITE operations, a HIGH enables the WRITE TRANSFER and a LOW disables the WRITE TRANSFER. As with SPLIT READ TRANSFER, the half of the SAM not receiving data will be the half transferred and the Tap address (A0-A7) for the other half is loaded when $\overline{CAS}$ falls (A8 is a "don't care"). If $\overline{CAS}$ does not fall, the previously loaded Tap address, A0-A7, will be reused. The TRANSFER will be to the idle half. When the serial clock crosses the half-SAM boundary, the new Tap address for that half is automatically loaded.

The QSFa and QSFb output (MT43C4257) indicate which half of SAMa or SAMb, respectively, is currently accepting data. After QSF goes HIGH, indicating that serial input has now switched to the upper SAM, the contents of the lower half of the SAM may be transferred to any DRAM row. The

cycle of checking for a change in QSF and then transferring the half of the SAM just filled may now be repeated. The next step on Figure 7 is to wait for QSF to go LOW and then SWT the contents of the upper half of the SAM to row 0. If the terminal count of the SAM half is reached before an SWT is performed for the next half, the access will be repeated from the same half and previously loaded address (access will not move to the next half).

When operating the MT43C4258 in the SWT mode, the address pointer may be changed, at will, to the new Tap address of the next half when the final desired input data is clocked in. When the final data is input, the SSF input is taken HIGH at the corresponding rising edge of SC. The next SC rising edge will input data into the Tap location of the next half of the SAM. If SSF is not applied, the Tap address will be automatically loaded when the maximum Tap address count is reached for the current half (255 or 511). If SSF is HIGH at SC, before an SWT is performed for the next half, the access will jump to the old Tap address of the same half. Access will not preceed to the next half. If terminal count is reached before an SWT, the access will proceed as it does for the MT43C4257.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SCa,b, $\overline{SE}$a,b and SSFa,b (MT43C4258). The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 4-bit port. $\overline{SE}$ is used as an output enable during the

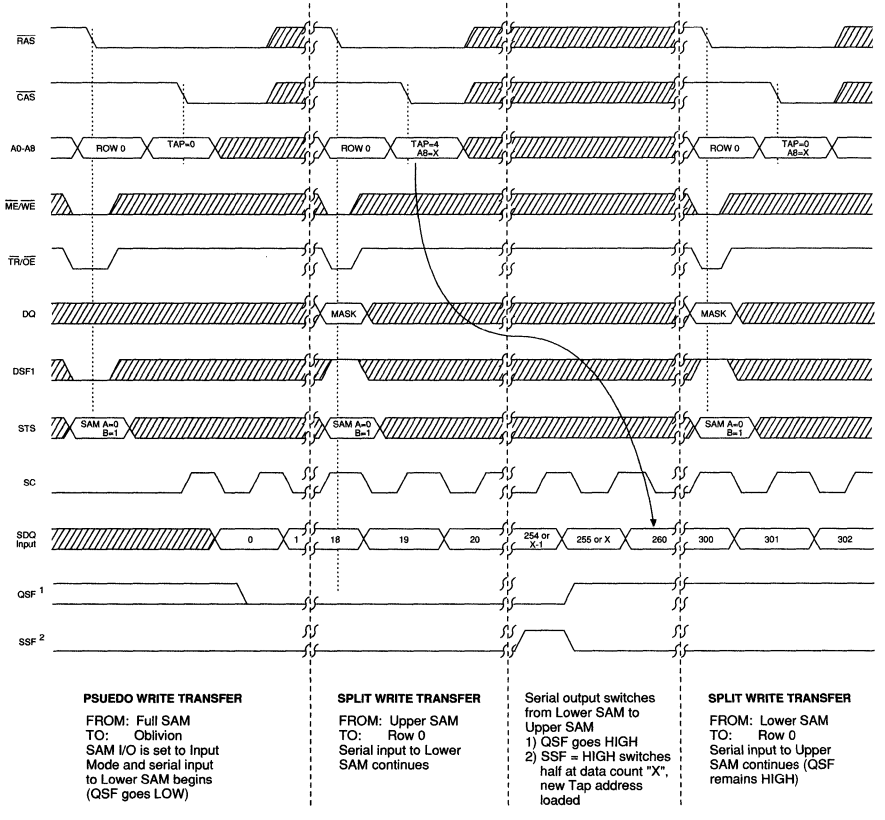


Figure 7
TYPICAL SPLIT WRITE TRANSFER INITIATION SEQUENCE

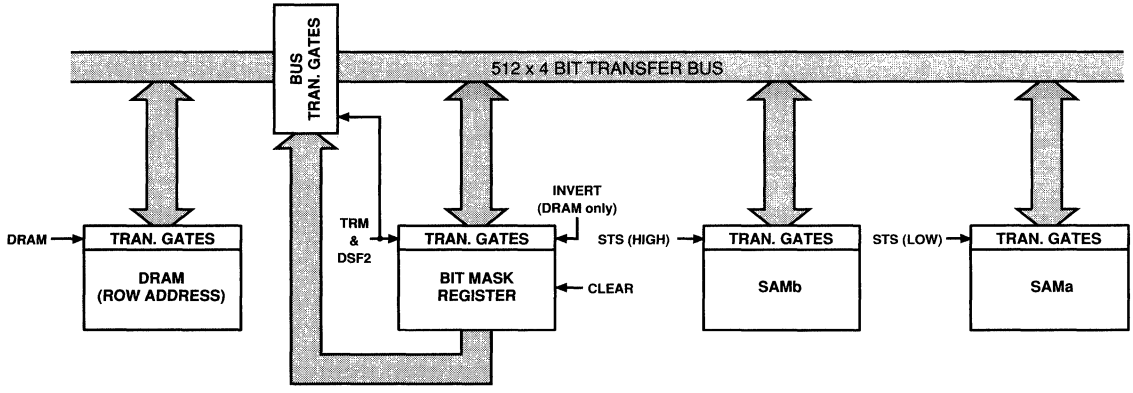


Figure 8
BIT MASKED TRANSFER BLOCK DIAGRAM

SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. For the MT43C4257, the address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half, for split modes. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes. For the 43C4258, the address count will wrap as it does for the MT43C4257 or it may be triggered, at will, to the next half by the SSF input (split SAM modes). If SSF is HIGH at a LOW-to-HIGH transition of SC, the Tap address of the next half will be loaded into the address pointer. The following LOW to HIGH transition of SC will clock data from the Tap address of the new half.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address register (loaded when the serial input mode was enabled) will determine the serial address of the first 4-bit word written. $\overline{SE}$ acts as a WRITE ENABLE for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW to HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input.

BIT MASKED TRANSFERS

This section describes transfers between the DRAM and either of the two SAMs using the BIT MASKED TRANSFER capability. Before performing these BIT MASKED TRANSFERS, the bit mask register must first be loaded with the mask data. See the next section, BIT MASK REGISTER OPERATIONS, for instructions on how to load the Bit Mask Register (BMR).

The BMR is a 2048-bit register that individually controls each of the 2048 transfer gates on the internal 512 x 4 transfer bus (see Figure 8). These bus transfer gates reside between the DRAM array and the three data registers and are set to the "pass-thru" mode for nonmasked transfers. For BIT MASKED TRANSFERs, the data in the BMR is coupled to the control inputs of the bus transfer gates. A logic "1" in the BMR will select the pass-thru (unmasked) mode for the corresponding SAM data bit, while a logic "0" will select the masked mode for that bit.

BIT MASKED TRANSFERs may be incorporated when doing READ, WRITE, SPLIT READ and SPLIT WRITE TRANSFERs. The timing and control required for any particular BIT MASKED TRANSFER cycle is identical to the corresponding normal TRANSFER cycle, except that TRM and DSF2 are HIGH instead of LOW. BIT MASKED TRANSFERs between the DRAM and either of the two SAM registers are possible. Figure 9 illustrates the BIT MASKED TRANSFER functions.

BIT MASKED READ TRANSFER (BMRT)

BIT MASKED READ TRANSFER can be used to transfer any combination of the 2048 bits contained in any DRAM row address to either of the two SAMs. The logic conditions and timing for the BMRT function are identical to the normal READ TRANSFER function except to select the BIT MASKED feature, TRM and DSF2 are HIGH. If a bit in the BMR is a logic "1", the bus connection between the corresponding DRAM bit and the selected SAM bit is enabled and the data at the destination (one of the SAMs for BMRT) will be changed to the source data (the DRAM row for BMRT).

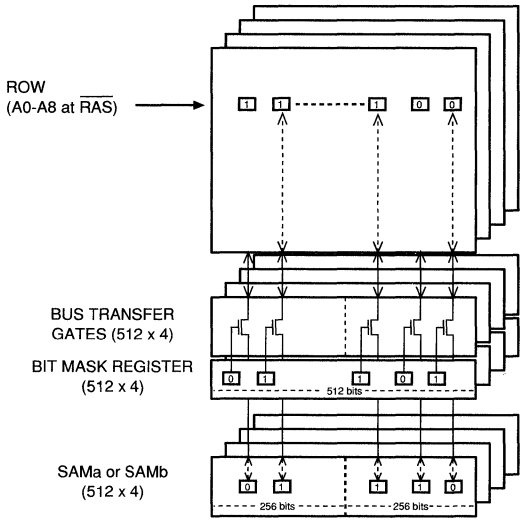


Figure 9
BIT MASK TRANSFER BLOCK DIAGRAM

BIT MASKED SPLIT READ TRANSFER (BMSRT)

The BIT MASKED SPLIT READ TRANSFER operation is identical to the normal SPLIT READ TRANSFER except that the bit mask (stored in the bit mask register) is applied to the transfer data by taking TRM and DSF2 HIGH when $\overline{RAS}$ falls. The remaining control timing is identical to the requirements for a normal SPLIT READ TRANSFER.

BIT MASKED WRITE TRANSFER (BMWT)

Like WRITE TRANSFER, the BIT MASKED WRITE TRANSFER function may be used to transfer data to any DRAM row address from either of the two SAM registers. In this case, the SAM data will be masked by the contents of the Bit Mask Register before the data is written to the DRAM.

BIT MASKED SPLIT WRITE TRANSFER (BMSWT)

Like the other BIT MASKED TRANSFER cycles, the BMSWT is nearly identical to the SPLIT WRITE TRANSFER, except TRM and DSF2 are HIGH when $\overline{RAS}$ falls. Two masks are applied during a BMSWT operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at $\overline{RAS}$ time. If a DQ input is LOW at $\overline{RAS}$ time, none of the 256 SAM bits for that DQ plane will be transferred to the DRAM row-half selected. If a DQ input is HIGH, the 256 SAM bits for that row half will be masked by the corresponding 256 mask register bits when written to the selected DRAM row-half. The remaining control timing is identical to the requirements for a normal SPLIT WRITE TRANSFER.

BIT MASK REGISTER OPERATIONS

This section describes how to transfer data to or from the Bit Mask Register (BMR) and how to clear the BMRs contents. Data may also be inverted when being transferred between the BMR and DRAM.

BMR READ TRANSFER (BMR-RT)

Any DRAM row may be transferred to the BMR by using the BMR READ TRANSFER function. When $\overline{RAS}$ falls, $\overline{TR}$/$\overline{OE}$ is LOW to select a transfer cycle. TRM is HIGH to indicate that the BMR is involved in the TRANSFER cycle, and DSF2 is LOW to indicate that the data is to be transferred to the BMR (as opposed to using the contents of the BMR as bit mask data). The remainder of the timing and control required is identical to a normal READ TRANSFER cycle. No Tap address is loaded in this TRANSFER.

Note that the SAM transfer select (STS) pin is used to select whether non-inverted (STS=LOW) or inverted (STS=HIGH) data is transferred to the bit mask register. For all transfers to or from the bit mask register, the state of the MKD pin when $\overline{RAS}$ falls selects whether the Serial Mask Input (SMI) feature is enabled (see the Functional Truth Table). SMI is a special serial input mode that allows mask information to be clocked into the BMR at the same address location as the data clocked into SAMb (see the SMI mode description). MKD is LOW when $\overline{RAS}$ falls to disable SMI or HIGH to enable SMI. After the transfer is completed, the MKD pin then acts either as a mask data input to the BMR (SMI enabled) or is "don't care" (SMI disabled). The MKD input is tied to the 4 bit-planes, the data on the MKD pin is written to each bit plane simultaneously.

BMR INVERTED READ TRANSFER (BMR-IRT)

If the STS pin is HIGH at $\overline{RAS}$ time the DRAM data will be inverted before being written to the BMR. All 2048 bits involved in the transfer will be complemented. The functionality and logic levels for the other control inputs are identical to the BMR READ TRANSFER cycle. Note that MKD is still used to enable or disable the SMI mode. There is no added cycle time delay for either the BMR INVERTED READ or BMR INVERTED WRITE TRANSFER cycles.

BMR WRITE TRANSFER (BMR-WT)

The contents of the BMR may also be transferred to any DRAM row by using the BMR WRITE TRANSFER cycle. ($\overline{ME}$)/$\overline{WE}$ and DSF2 are LOW and TRM is HIGH when $\overline{RAS}$ falls, to select a write transfer from the BMR. The DQ inputs are used to input a DQ bit-plane mask when $\overline{RAS}$ falls. This allows each of the four DQ planes to be write enabled or disabled during the BMR-WT. The MKD input is used to enable or disable the SMI mode. STS must be LOW at $\overline{RAS}$ time to transfer non-inverted BMR data to the DRAM row selected.

BMR INVERTED WRITE TRANSFER (BMR-IWT)

As with the BMR INVERTED READ TRANSFER, the 2048 bits involved in the transfer may be inverted while being transferred. Taking STS HIGH at $\overline{RAS}$ time will cause the BMR data to be inverted before it is stored in the selected DRAM row. The other control and DQ (mask) inputs are the same as the BMR-WT.

SAM-TO-BMR TRANSFER (SAM-BMR)

The contents of either SAM may be transferred to the BMR in the same manner that a DRAM row is transferred. In this case, DSF1 is HIGH to indicate that the SAM is the source of the data instead of the DRAM. ($\overline{ME}$)/$\overline{WE}$ is used to indicate the direction of the transfer and must be LOW, when $\overline{RAS}$ falls, for a SAM-TO-BMR TRANSFER. STS is no longer used to select between normal and inverted data, it now indicates which SAM is involved in the transfer. Since a SAM-TO-BMR TRANSFER "reads" data from the SAM, the SAM will be placed into input mode by this transfer cycle. The MKD input is still used to determine if the SMI mode will be enabled after the transfer is completed. Since no DRAM access is involved, it is not necessary to provide any particular ROW address at $\overline{RAS}$ time. However, whichever ROW address is present at $\overline{RAS}$ time will be used as the address for a $\overline{RAS}$-ONLY REFRESH. Since a SAM is involved in the transfer, a new SAM starting Address (or Tap) will be loaded at $\overline{CAS}$ time. This address will be loaded into the serial address counter of the SAM selected by STS at $\overline{RAS}$ time.

Note: *Any SAM/BMR TRANSFER will take the device out of the split SAM mode, if it was in that mode before the transfer.*

BMR-TO-SAM TRANSFER (BMR-SAM)

The contents of the BMR may also be transferred to one of the SAM registers. The ($\overline{ME}$)/$\overline{WE}$ input is used to indicate the direction of the transfer and must be HIGH for a BMR-TO-SAM TRANSFER. STS is LOW to select SAMa or HIGH to select SAMb as the destination for the BMR data. The remaining inputs and functionality are identical to the SAM-TO-BMR TRANSFER. Since a BMR-TO-SAM TRANSFER writes new data to the selected SAM register, the I/O for the SAM involved will be placed in the output mode and a new Tap address will be loaded when $\overline{CAS}$ falls.

CLEAR BIT MASK REGISTER (CLR-BMR)

The entire contents of the BMR can be cleared (set all bit LOW) within a single transfer cycle by performing a CLEAR BMR cycle. Unlike the other cycles that access the BMR, TRM is LOW at $\overline{RAS}$ time for the CLEAR BIT MASK REGISTER function. $\overline{TR}$/($\overline{OE}$) is LOW to indicate that the cycle is a transfer cycle (although there is really no data transfer involved). The CLR-BMR function is selected when $\overline{ME}$/($\overline{WE}$), DSF1 and DSF2 are HIGH when RAS falls.

When the BMR is cleared, all data will be masked when a BIT MASKED TRANSFER cycle is performed.

The BMR INVERTED WRITE and BMR WRITE TRANSFERS can be used with the CLR-BMR function to set or clear, respectively, any DRAM row. The CLR-BMR function is used to clear the BMR then the BMR TRANSFERS are performed to the addressed DRAM row.

The CLEAR BIT MASK REGISTER function is useful when using the SERIAL MASK INPUT mode. It is automatically performed (when in the SMI mode) when data is transferred from SAMb to the DRAM (see SERIAL MASK INPUT section).

SERIAL MASK INPUT (SMI)

Whenever the BMR is accessed, the MKD input is sensed and latched into the BMR control logic. If the MKD pin is LOW at $\overline{RAS}$ time the Serial Mask Input (SMI) mode is disabled and the BMR may only be loaded via internal transfer cycles. If MKD is HIGH when $\overline{RAS}$ falls, during a BMR access, then the BMR control logic enables the SMI mode and the BMR may be serially loaded via the MKD input.

When SMI is enabled, the MKD input is coupled to all four of the bit mask register's DQ planes (see Figure 10). The SCb clock input and SAMb's address counter are used to input data to SAMb and the BMR. SEb will enable (LOW) or disable (HIGH) input data to SAMb and the BMR, the address count will increment regardless of the state of SEb.

The most common application of the SMI mode is to automatically load a transfer mask with the new data written to SAMb. To initialize the sequence, the BMR is cleared (CLR-BMR) with MKD=HIGH at $\overline{RAS}$ time to enable the SMI mode. Then SAMb is prepared to accept input data by performing PSEUDO WRITE TRANSFER. The SAM starting address loaded will also apply to the BMR. For every address location that data is written to in SAMb, the corresponding address location in the BMR will be written to the value present on MKD (all four planes of the

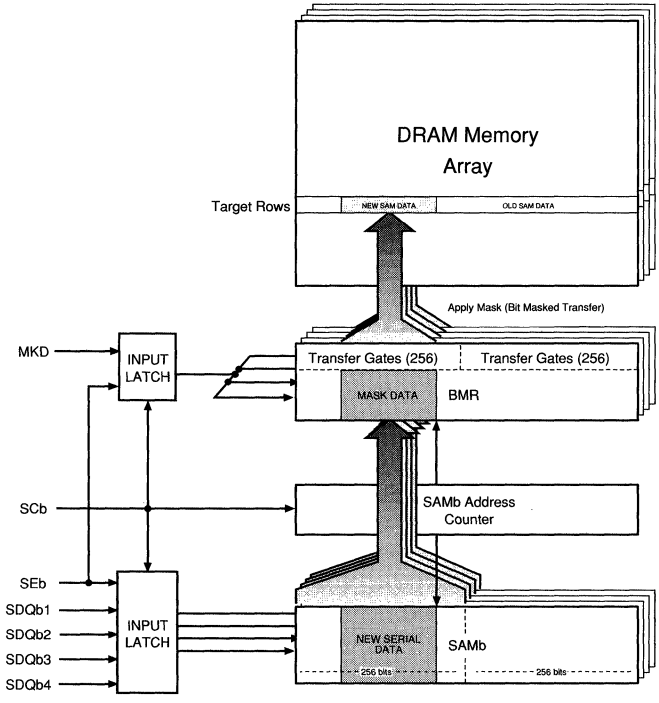


Figure 10
SERIAL-MASK-INPUT MODE BLOCK DIAGRAM

BMR will be written). After the input of data to SAMb is complete, a BIT MASKED WRITE TRANSFER may be done and only the unmasked data from SAMb will be transferred to the DRAM. The BMR will be cleared automatically after a BIT MASKED WRITE TRANSFER from SAMb, if the device is in the SMI mode. A BMSWT from SAMb will clear only half of the BMR. This allows a new mask to be loaded during the next fill of SAMb, without performing a CLR-BMR cycle. If data is to be masked during the BMWT then MKD is held LOW when the corresponding SAMb data is written. If the data is to be written (unmasked) to the DRAM during the BMWT, then MKD is held HIGH when the corresponding SAMb location is written. The function of the MKD pin is dependent on the I/O direction of SAMb. MKD is an input only, if SMI is enabled and SAMb is in input mode. If SMI is enabled and SAMb is in output mode, the MKD input is a "don't care," no new data may be written to the BMR via MKD. MKD is also "don't care" if the SMI mode is disabled. Note that the mask data loaded via SAMb may also be applied to a SAMa TRANSFER cycle, if the mask hasn't been cleared by a SAMb TRANSFER or a CLR-BMR cycle. The BMR will not be cleared after a TRANSFER involving SAMa.

POWER UP INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 8ms, the device must be initialized.

After Vcc is at specified operating conditions, for 100µs (minimum), eight $\overline{RAS}$ cycles must be executed to initalize the dynamic memory array. When the device is initialized the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of ($\overline{TR}$)/$\overline{OE}$. The DRAM array will contain random data.

The SAM portion of the device is completely static and does not require an initialization cycle. Both SAM ports will power-up in the serial input mode (WRITE TRANSFERs) and the SAM I/O pins (SDQs) are in a High-Z state, regardless of the state of $\overline{SE}$ ab. Also, SPLIT TRANSFER and SMI modes are disabled. Both QSF (MT43C4257) outputs are in the High-Z state. Both SAMs, bit mask, color, and DRAM mask registers all contain random data after power-up.

TRUTH TABLE [1]

CODE	FUNCTION	RAS FALLING EDGE									CAS FALL	A0 - A8[2]		DQ1 - DQ4[3]		REGISTERS	
		CAS	TR / OE	ME / WE[10]	DSF1	DSF2	SEa, SEb	TRM	MKD	STS	DSF1	RAS	CAS	RAS	CAS[4]	MASK	COLOR
	DRAM OPERATIONS																
CBR	CAS-BEFORE-RAS REFRESH	0	1[11]	1[11]	X	X	X	X	X	X	X	X	X	X	X	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	X	X	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0[11]	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	X	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	0[11]	X	X	X	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	0[11]	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	0[11]	X	X	X	X	1	ROW	COLUMN (A2 - A8)	X	COLUMN MASK	X	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	0[11]	X	X	X	X	1	ROW	COLUMN (A2 - A8)	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	0[11]	X	X	X	X	1	ROW	COLUMN (A2 - A8)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS																
LMR	LOAD MASK REGISTER	1	1	1	1	0[11]	X	X	X	X	0	X[5]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	0[11]	X	X	X	X	1	X[5]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS																
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	X	X
SRT[9]	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	0	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)	1	0	0	0	0	1	0	X	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	X	X
SWT[9]	SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER WITH MASK)	1	0	0	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	LOAD & USE	X
DMWT	DQ MASKED WRITE TRANSFER	1	0	0	0	1	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	LOAD & USE	X

TRUTH TABLE[1]

CODE	FUNCTION	RAS FALLING EDGE									CAS FALL	A0 - A8[2]		DQ1 - DQ4[3]		REGISTERS	
		CAS	TR / OE	ME / WE[10]	DSF1	DSF2	SEa, SEb	TRM	MKD	STS	DSF1	RAS	CAS	RAS	CAS[4]	MASK	COLOR
	BIT MASK REGISTER OPERATIONS																
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	0	X	ROW	X	X	X	X	X
BMR-IRT	BMR READ TRANSFER (DRAM→INVERT→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	1	X	ROW	X	X	X	X	X
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	0	X	ROW	X	DQ MASK	X	X	X
BMR-IWT	BMR WRITE TRANSFER (BMR→INVERT→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	1	X	ROW	X	DQ MASK	X	X	X
SAM-BMR	SAM→BMR TRANSFER	1	0	0	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	X	X
BMR-SAM	BMR→SAM TRANSFER	1	0	1	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	X	X
CLR-BMR	CLEAR BIT MASK REGISTER (SETS BMR TO ALL "0's")	1	0	1	1	1	X	0	0/1[7]	X	X	X[5]	X	X	X	X	X
	BIT MASKED TRANSFER OPERATIONS																
BMRT	BIT MASKED READ TRANSFER (BM DRAM→SAM TRANSFER)	1	0	1	0	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	X	X
BMSRT[9]	BIT MASKED SPLIT READ TRANSFER (BM SPLIT DRAM→SAM TRANSFER)	1	0	1	1	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	X	X
BMWT	BIT MASKED WRITE TRANSFER (BM SAM→DRAM TRANSFER)	1	0	0	0	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	X	X
BMSWT[9]	BIT MASKED SPLIT WRITE TRANSFER (BM SPLIT SAM→DRAM TRANSFER)	1	0	0	1	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	LOAD & USE	X

NOTE:
1. 0 = LOW (V_{IL}), 1 = HIGH (V_{IH}), X = "don't care", - = "not applicable"
2. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
3. These columns show what must be present on the DQ1-DQ4 inputs when RAS falls and when CAS falls.
4. On WRITE cycles (except BLOCK WRITE), the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is enabled on the falling edge of CAS or TR/OE, whichever is later.
5. The ROW that is addressed will be refreshed, but no particular ROW address is required.
6. Tap Address; this is the SAM location that the first SC cycle will access. For SPLIT TRANSFERS the half receiving the transfer is determined by the MSB of the internal address counter. The SAM half not currently being accessed will be the half receiving the transfer. Column address A8 is a "don't care" for SPLIT TRANSFERS.
7. The Serial Mask Input mode (SMI) is enabled ("1") or disabled ("0") when the BMR is accessed (see BMR OPERATIONS). If SMI is enabled (MKD = "1"), mask data is serially clocked into the BMR with SCb and the BMR is automatically cleared after a BIT MASKED WRITE or BIT MASKED SPLIT WRITE TRANSFER cycle from SAMb. For BIT MASKED READ TRANSFERs to any SAM and BIT MASKED WRITE TRANSFERs from SAMa, the BMR is not cleared automatically.
8. If the SMI mode is enabled, mask data is clocked into the BMR with SCb. A HIGH will allow data from the SAM address location to be written to the DRAM, a LOW will mask data to the DRAM during a BIT MASKED WRITE or BIT MASKED SPLIT WRITE TRANSFER.
9. SPLIT TRANSFERs do not change SAM I/O direction.
10. SAM I/O direction is a function of the state of ME/WE at RAS time. If ME/WE is LOW, then the selected SAM is an input; if ME/WE is HIGH then the SAM is an output.
11. The MT43C4257/8 operates properly if this state is "X", but to allow for future functional enhancements it is recommended that they are driven as shown in the Truth Table.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Operating Temperature, Ta(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$, all other pins not under test = 0V).	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled, $0V \le V_{OUT} \le V_{CC}$).	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA, SDQs; -5mA all other outputs)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.5mA, SDQs; 5mA all other outputs)	V_{OL}		0.4	V	1

CAPACITANCE

(T_A = 25°C; V_{CC} = 5.0V; f = 1MHz)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8, TRM, MKD	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SCa,b, $\overline{SE}$a,b, DSF1,2, STS SSFa,b	C_{I2}		7	pF	2
Input/Output Capacitance: DQ, SDQa,b	$C_{I/O}$		9	pF	2
Output Capacitance: QSFa,b	C_O		9	pF	2

CURRENT DRAIN, SAMa and SAMb IN STANDBY

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MAX -8	MAX -10	MAX -12	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC1}	100	90	80	mA	3, 4
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL} $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC2}	90	80	70	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, after 8 $\overline{RAS}$ cycles min)	I_{CC3}	7	7	7	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V, after 8 $\overline{RAS}$ cycles min). All other inputs at V_{CC} -0.2V or V_{SS} +0.2V	I_{CC4}	1	1	1	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC5}	100	90	80	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	90	80	70	mA	3, 5
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	I_{CC7}	110	100	90	mA	3

CURRENT DRAIN, SAMa and SAMb ACTIVE

(Notes 3, 4) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MAX -8	MAX -10	MAX -12	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC8}	180	170	160	mA	
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL} $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC9}	160	150	140	mA	
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, after 8 $\overline{RAS}$ cycles min)	I_{CC10}	85	85	85	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V, after 8 $\overline{RAS}$ cycles min). All other inputs at V_{CC} -0.2V or V_{SS} +0.2V	I_{CC11}	75	75	75	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH})	I_{CC12}	180	170	160	mA	
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC13}	170	160	150	mA	5
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	I_{CC14}	180	170	160	mA	

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		180		210		ns	
READ-MODIFY-WRITE cycle time	^tRWC	205		235		280		ns	
FAST PAGE MODE READ or WRITE cycle time	^tPC	45		55		65		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	^tPRWC	100		110		140		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14, 17
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Access time from ($\overline{TR}$)/OE	^tOE		20		25		30	ns	
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		80		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	20	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	12		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	25	60	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	30	ns	20
Output disable	^tOD	0	20	0	20	0	30	ns	
Output disable hold time from start of write	^tOEH		15		15		20	ns	
Output enable to $\overline{RAS}$ delay	^tORD		0		0		0	ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		85		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		130		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		80		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		55		70		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	12		15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	12		15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER command to $\overline{RAS}$ setup time	^tTLS	0		0		0		ns	25
TRANSFER command to $\overline{RAS}$ hold time	^tTLH	12	10,000	15	10,000	15	10,000	ns	25
TRANSFER command to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	^tRTH	70	10,000	80	10,000	90	10,000	ns	25
TRANSFER command to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	^tCTH	20		25		30		ns	25
TRANSFER command to column address hold time (For REAL-TIME READ TRANSFER only)	^tATH	25		30		35		ns	25
TRANSFER command to SC lead time	^tTSL	5		5		5		ns	25
TRANSFER command to $\overline{RAS}$ HIGH lead time	^tTRL	0		0		0		ns	25
TRANSFER command to $\overline{RAS}$ delay time	^tTRD	15		15		15		ns	25
TRANSFER command to $\overline{CAS}$ HIGH lead time	^tTCL	0		0		0		ns	25
TRANSFER command to $\overline{CAS}$ delay time	^tTCD	15		15		15		ns	25
First SC edge to TRANSFER command delay time	^tTSD	10		10		10		ns	25
$\overline{RAS}$ to first SC edge delay time	^tRSD	80		95		105		ns	
$\overline{CAS}$ to first SC edge delay time	^tCSD	25		30		35		ns	
Column address to first SC edge delay time	^tASD	50		60		65		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	10	35	10	40	10	45	ns	
SC to $\overline{RAS}$ setup time	^tSRS	30		30		40		ns	
$\overline{RAS}$ to SC delay time	^tSRD	20		25		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		0		ns	
$\overline{RAS}$ to SD buffer turn on time	^tSRO	10		15		15		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	45		50		55		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		0		ns	
Serial-Input-Mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		0		ns	
Serial-Input-Mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	12		15		15		ns	
NONTRANSFER command to $\overline{RAS}$ setup time	^tYS	0		0		0		ns	26
NONTRANSFER command to RAS hold time	^tYH	12		15		15		ns	26
DSF, TRM, STS, MKD to $\overline{RAS}$ setup time	^tFSR	0		0		0		ns	
DSF, TRM, STS, MKD to $\overline{RAS}$ hold time	^tRFH	12		15		15		ns	
DSF to $\overline{RAS}$ hold time	^tFHR	60		65		70		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		20		20		ns	
SC to QSF delay time	^tSQD		35		40		45	ns	
$\overline{RAS}$ to QSF delay time	^tRQD		65		85		105	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		35		40		45	ns	
$\overline{TR/OE}$ to QSF delay time	^tTQD		25		30		35	ns	
SPLIT TRANSFER setup time	^tSTS	30		35		40		ns	
SPLIT TRANSFER hold time	^tSTH	30		35		40		ns	
Split SAM setup time to $\overline{RAS}$ from last SC	^tSCR	30		35		40		ns	29
Split SAM hold time to $\overline{RAS}$ from first SC	^tRSC	30		35		40		ns	29

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

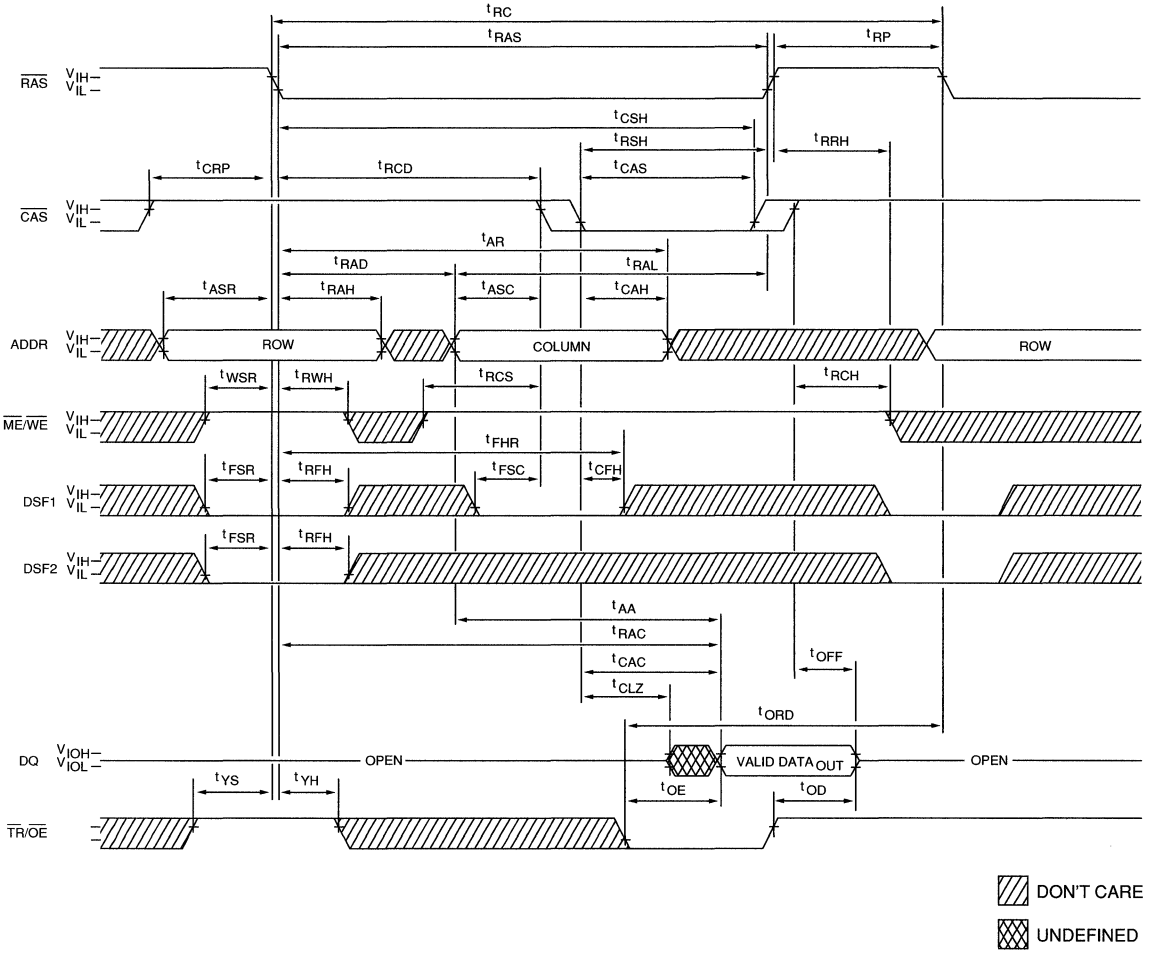
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	25		30		35		ns	
Access time from SC	^tSAC		25		30		35	ns	24
SC precharge time (SC LOW time)	^tSP	10		10		12		ns	
SC pulse width (SC HIGH time)	^tSAS	5		10		12		ns	
Access time from $\overline{SE}$	^tSEA		15		20		30	ns	24
$\overline{SE}$ precharge time	^tSEP	10		15		15		ns	
$\overline{SE}$ pulse width	^tSE	10		15		15		ns	
Serial data out hold time after SC HIGH	^tSOH	5		5		5		ns	24
Serial output buffer turn off delay from $\overline{SE}$	^tSEZ	0	12	0	15	0	25	ns	24
Serial data in setup time	^tSDS	0		0		0		ns	24
Serial data in hold time	^tSDH	10		15		20		ns	24
SERIAL INPUT (Write) Enable setup time	^tSWS	0		0		0		ns	
SERIAL INPUT (Write) Enable hold time	^tSWH	15		15		25		ns	
SERIAL INPUT (Write) Disable setup time	^tSWIS	0		0		0		ns	
SERIAL INPUT (Write) Disable hold time	^tSWIH	15		15		25		ns	
SSF to SC setup time	^tSFS	0		0		0		ns	29
SSF to SC hold time	^tSFH	15		20		20		ns	29
SSF LOW to SC HIGH delay	^tSFD	0		0		0		ns	29

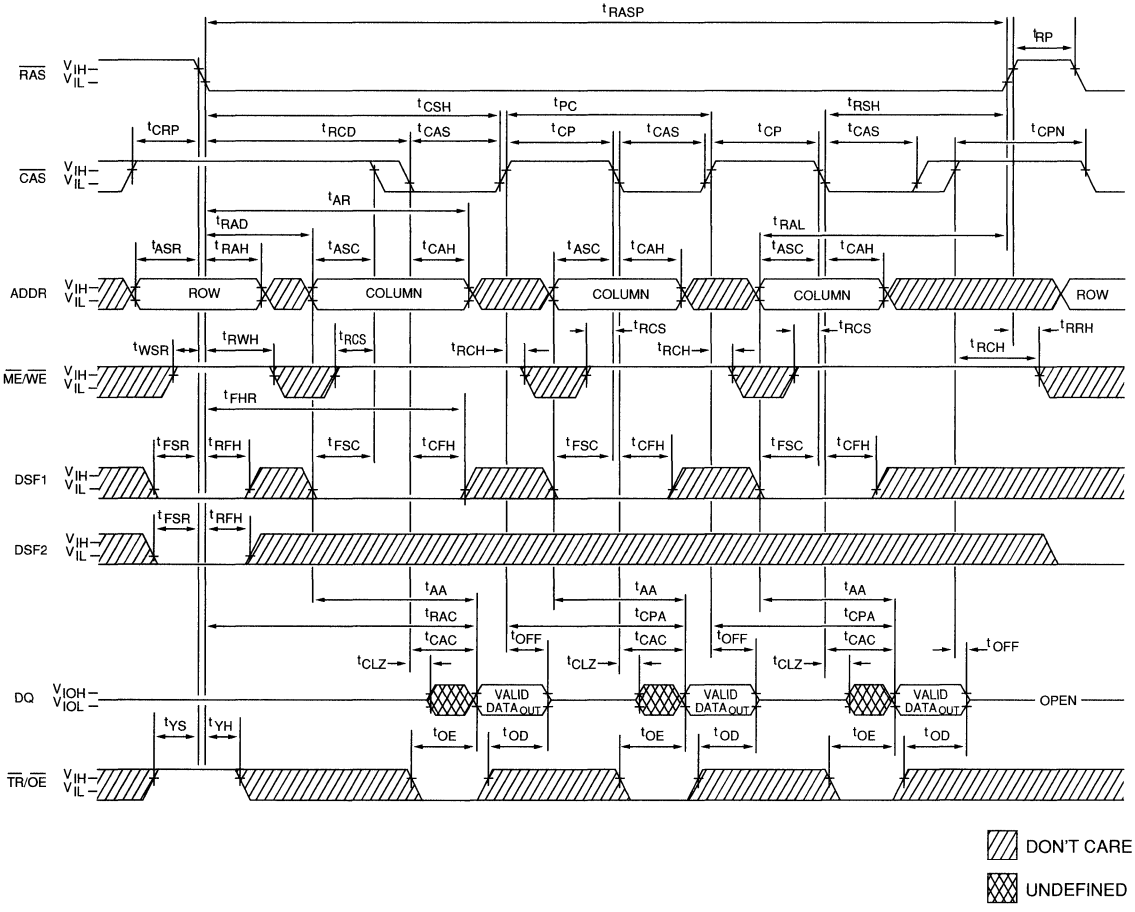
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, DRAM data outputs (DQ1-DQ4) is high impedance.
12. If $\overline{CAS} = V_{IL}$, DRAM data outputs (DQ1-DQ4) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF. Output reference levels: $V_{OH} = 2.0V$; $V_{OL} = 0.8V$.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \leq ^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 2 TTL gates and 50pF. Output reference levels: $V_{OH} = 2.0V$; $V_{OL} = 0.8V$.
25. TRANSFER command means that $\overline{TR}/\overline{OE}$ is LOW when $\overline{RAS}$ goes LOW.
26. NONTRANSFER command means that $\overline{TR}/\overline{OE}$ is HIGH when $\overline{RAS}$ goes LOW.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. Applies to the MT43C4257 only.
29. Applies to the MT43C4258 only.

DRAM READ CYCLE



DRAM FAST-PAGE-MODE READ CYCLE

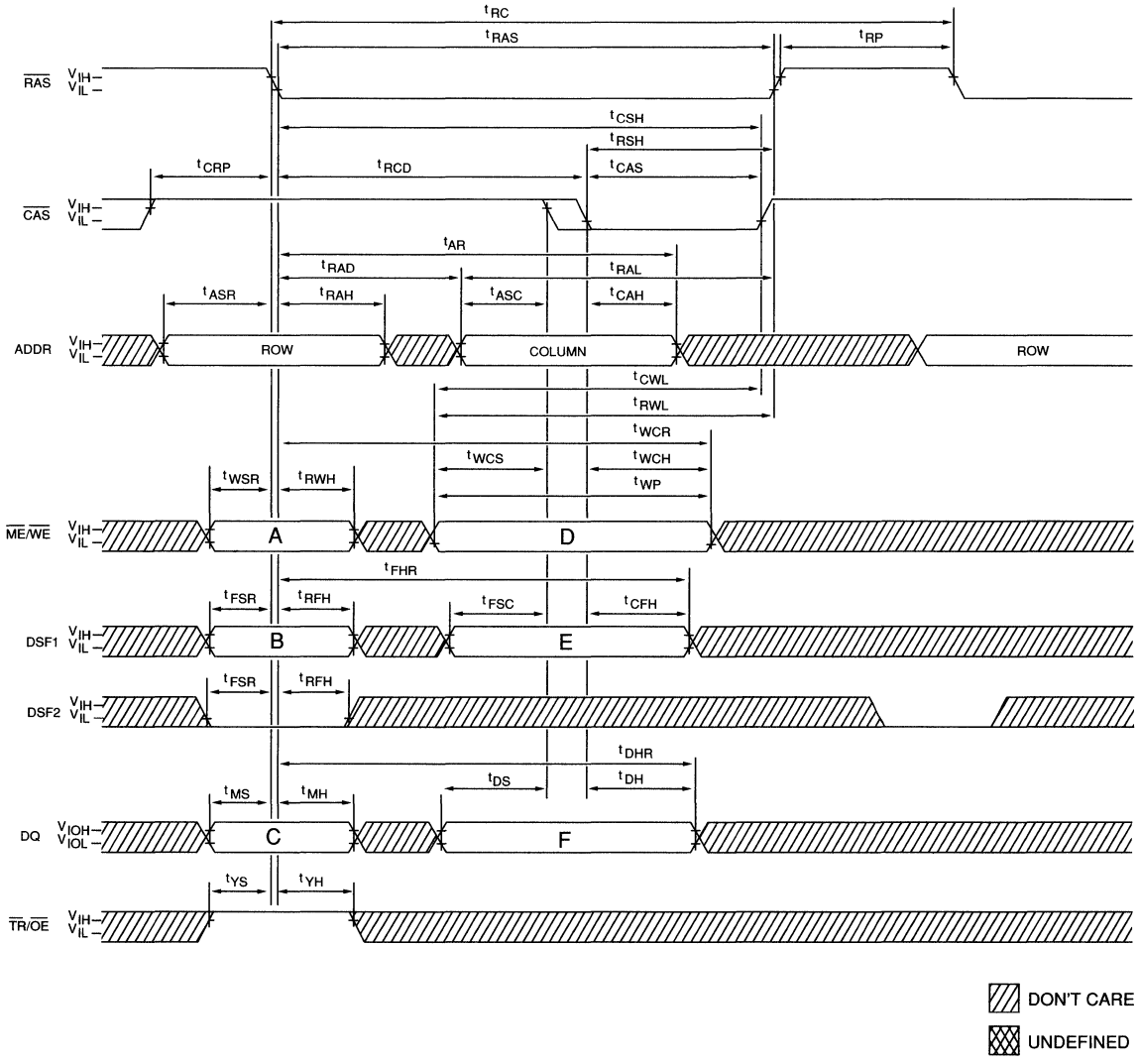


WRITE CYCLE FUNCTION TABLE [1]

LOGIC STATES[2]						FUNCTION	CODE
RAS Falling Edge			CAS Falling Edge				
A ME/WE	B DSF1	C DQ (Input)	D ME/WE	E DSF1	F DQ (Input)		
1	0	X	0/I[5]	0	DRAM	Normal DRAM WRITE	RW
0	0	Write Mask	0/I[5]	0	DRAM (Masked)	NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	RWNM
0	1	X	0/I[5]	0	DRAM (Masked)	PERSISTENT (Use Register) MASKED WRITE to DRAM	RWOM
1	0	X	X[3]	1	Column Mask	BLOCK WRITE to DRAM (No Data Mask)	BW
0	0	Write Mask	X[3]	1	Column Mask	NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	BWNM
0	1	X	X[3]	1	Column Mask	PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	BWOM
1	1	X	X[4]	0	Write Mask	LOAD MASK REGISTER	LMR
1	1	X	X[4]	1	Color Data	LOAD COLOR REGISTER	LCR

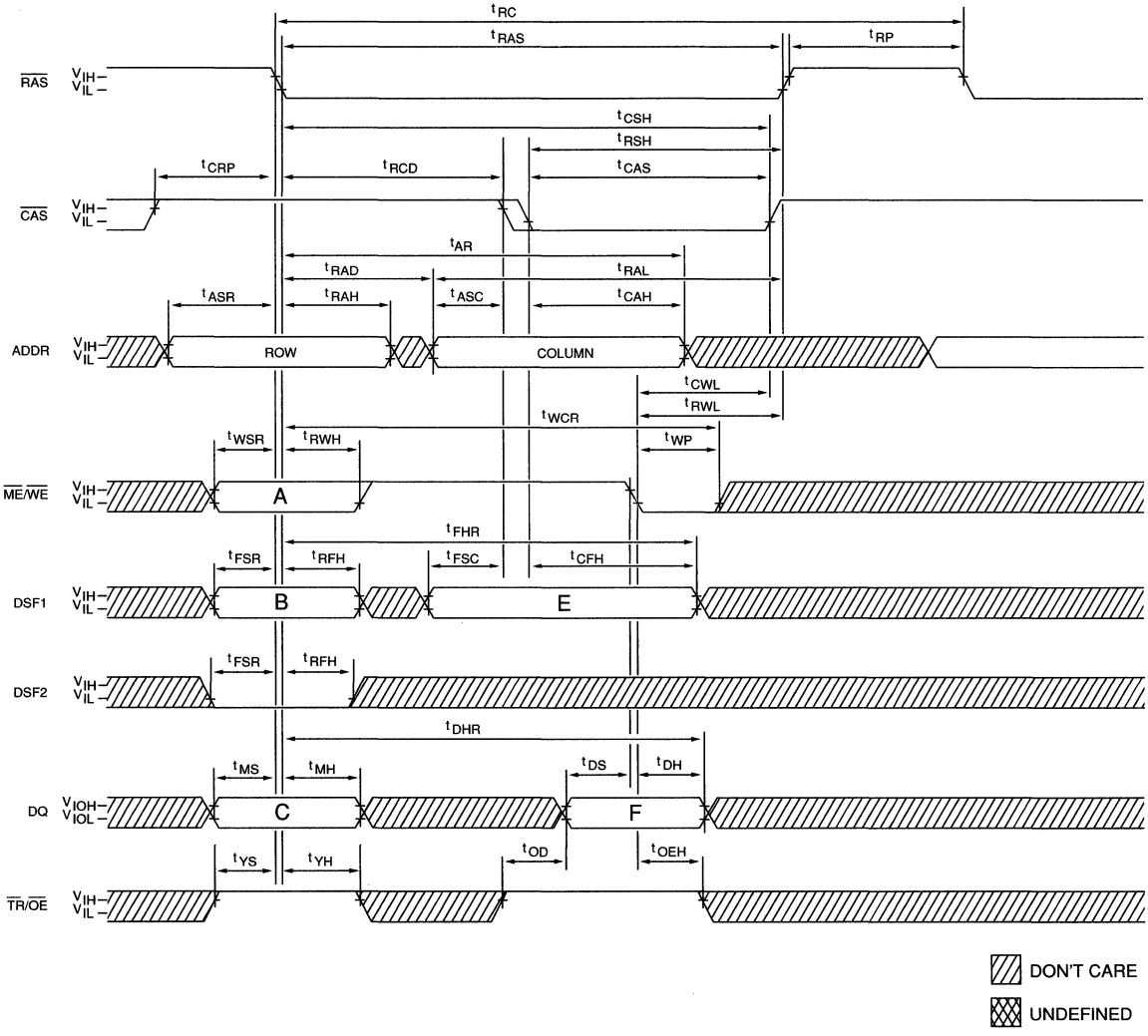
NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" and "F" for the WRITE cycle timing diagrams on the following pages.
2. TRM, MKD and STS are "don't care" for all WRITE cycles.
3. $\overline{WE}$ is a "don't care" for BLOCK WRITE cycles. It occurs on the falling edge of $\overline{CAS}$.
4. Register load cycles can be either EARLY or LATE-WRITE cycles.
5. If $\overline{ME/WE}$ is LOW, an EARLY-WRITE is performed; if it is HIGH, a LATE-WRITE is performed if $\overline{ME/WE}$ falls after $\overline{CAS}$.

DRAM EARLY-WRITE CYCLE



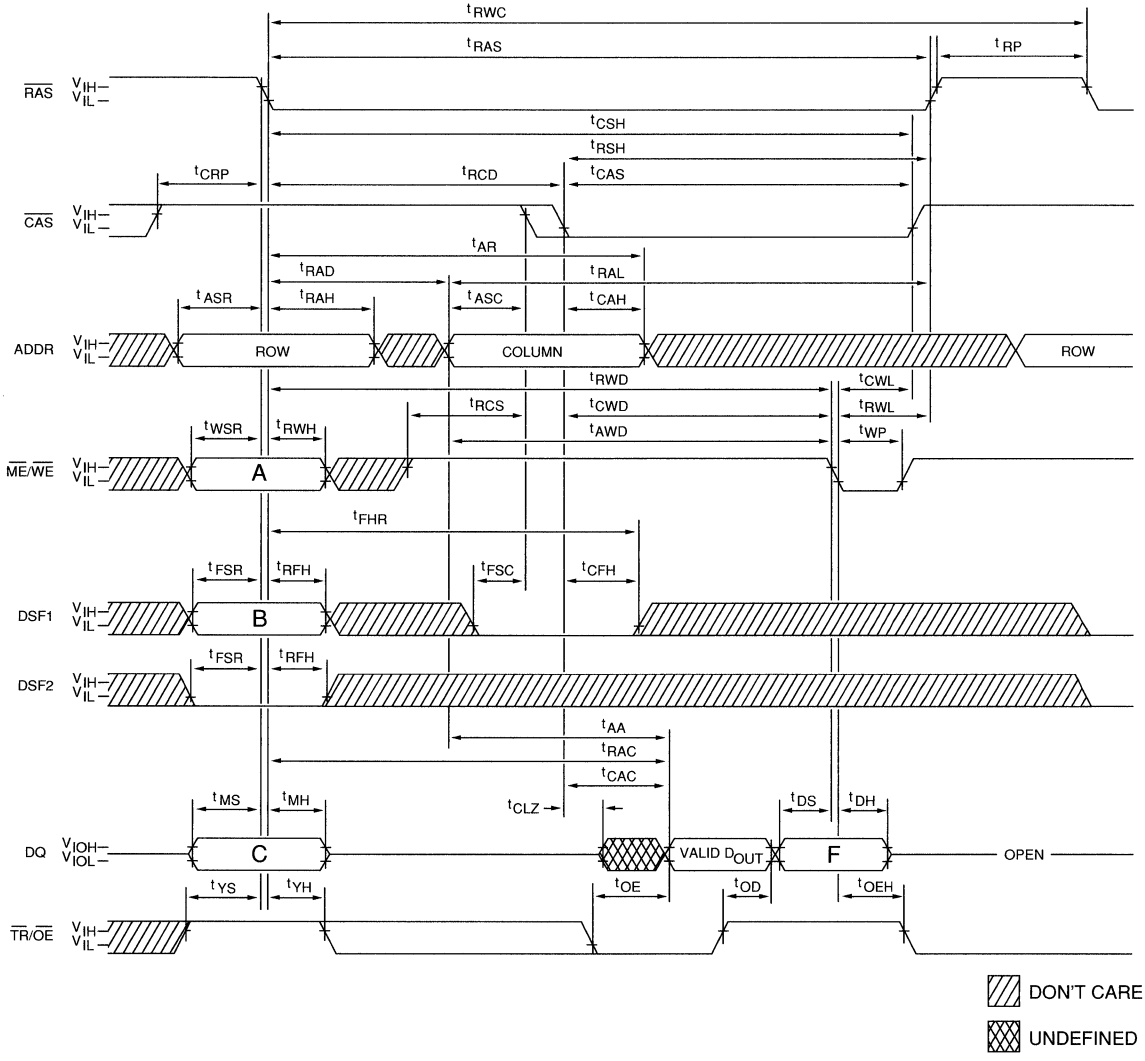
NOTE: 1. The logic states of "A", "B", "C", "E", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE [1, 2]



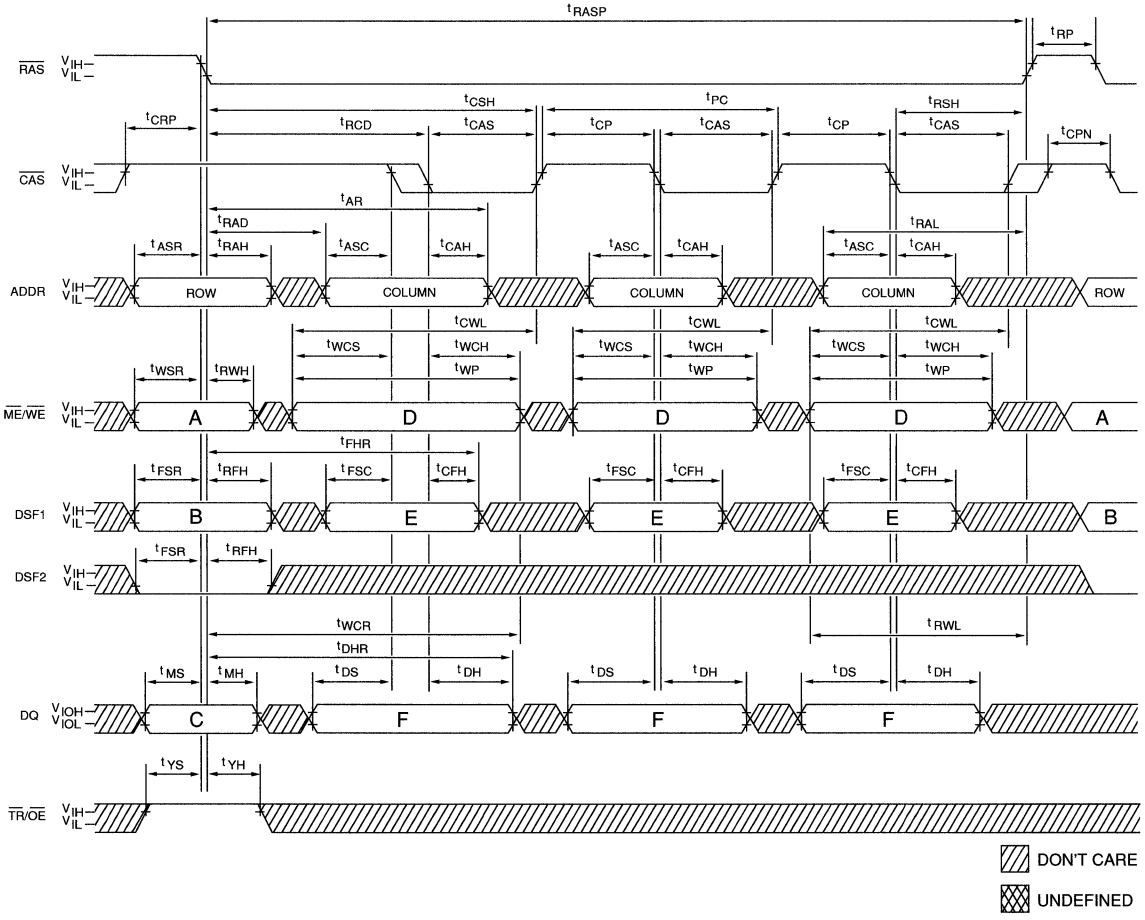
NOTE: 1. The logic states of "A", "B", "C", "E", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. LATE-WRITE cycles are not valid for BLOCK WRITEs. ($\overline{ME}$)/$\overline{WE}$ = "don't care" at the falling edge of $\overline{CAS}$.

DRAM READ-WRITE CYCLE [1]
(READ-MODIFY-WRITE CYCLE)



NOTE: 1. The logic states of "A", "B", "C", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

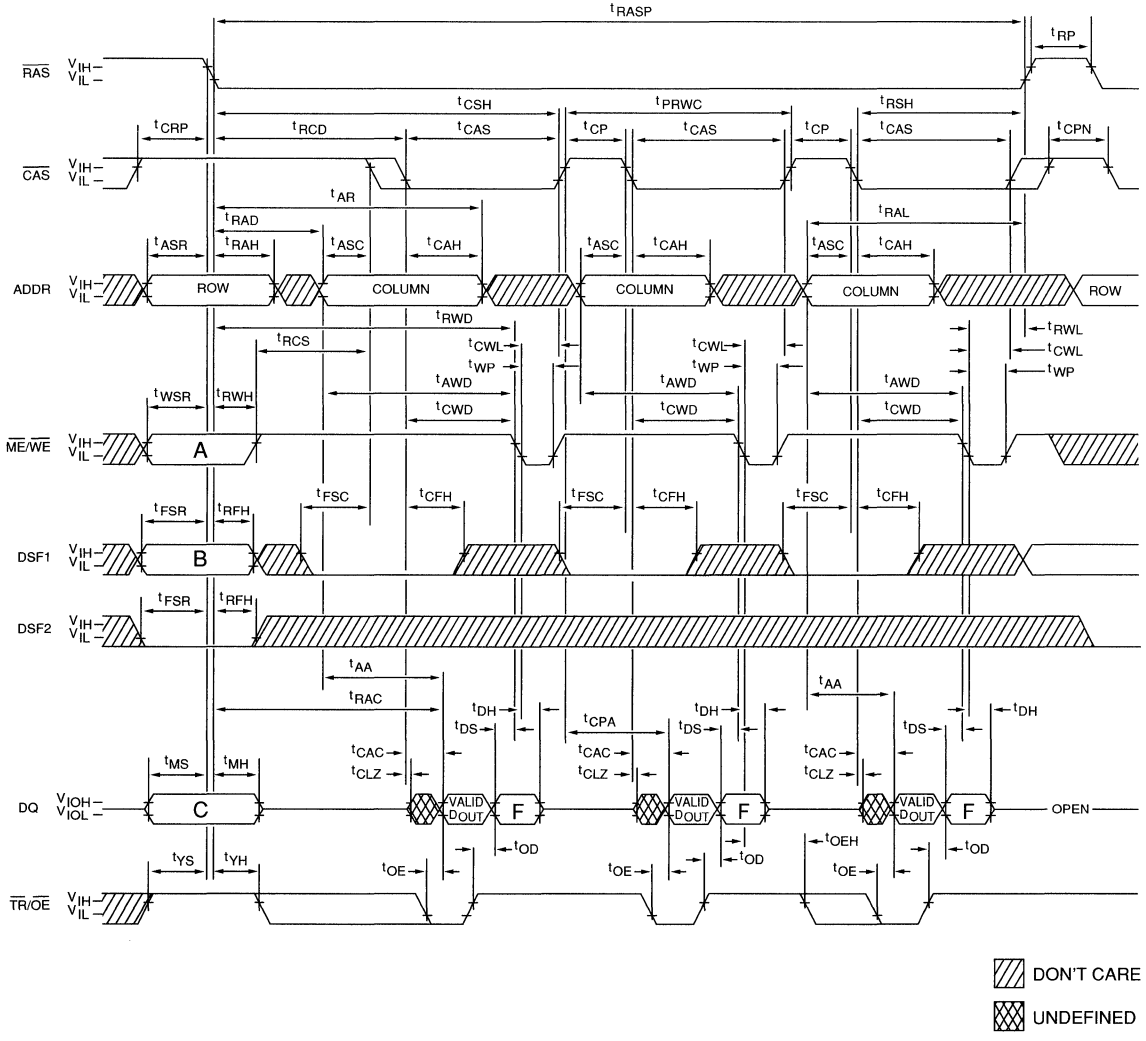
DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE [1, 2]



NOTE: 1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.

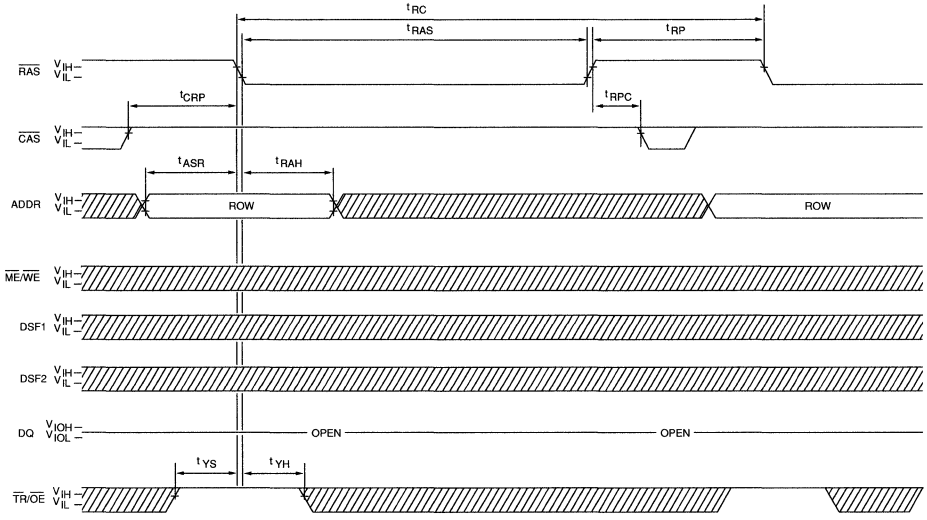
2. The logic states of "A", "B", "C", "D", "E", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE or LATE-WRITE CYCLES)

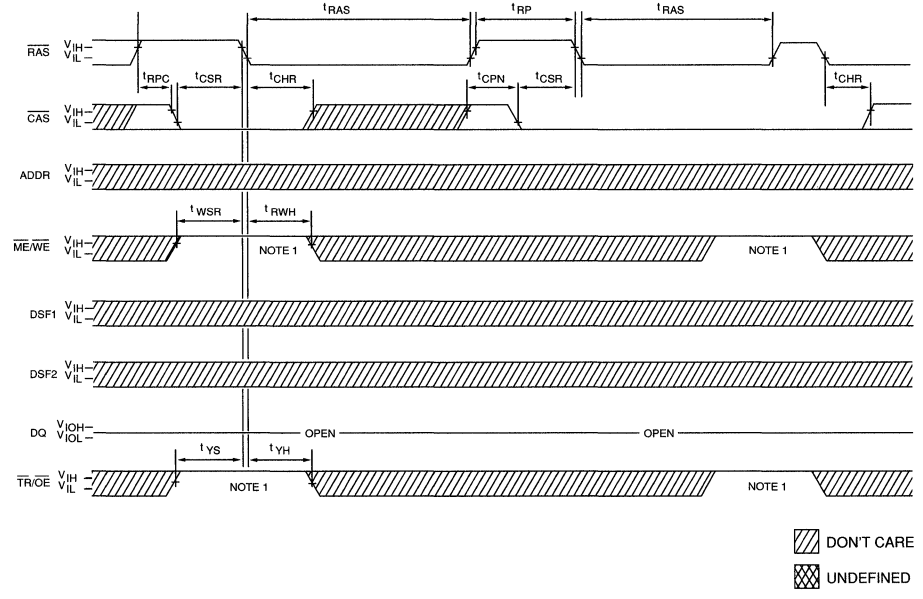


NOTE:
1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF1 state for the desired WRITE operation.
2. The logic states of "A", "B", "C", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)

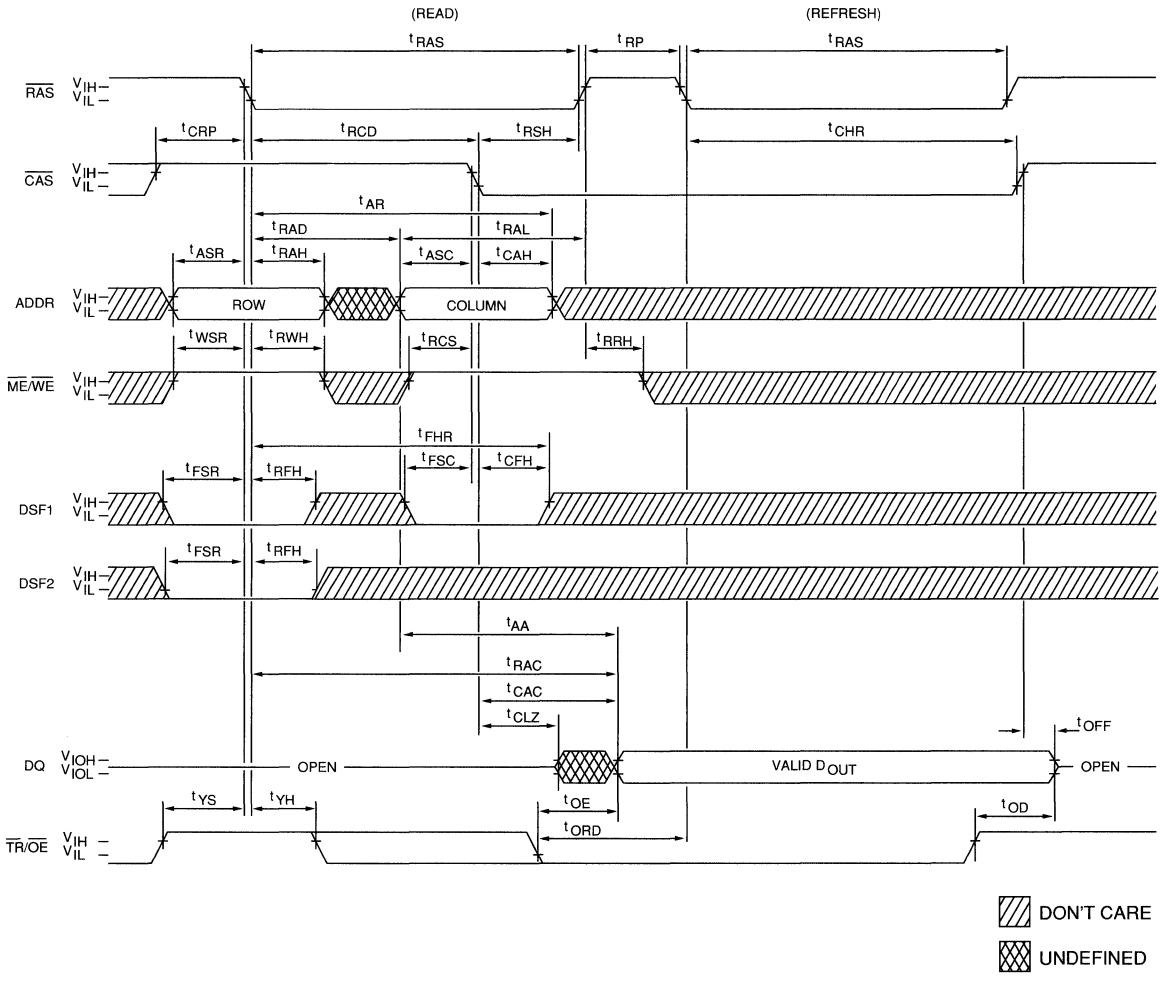


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



NOTE: 1. The MT43C4257/8 operates with this state as "don't care", but to allow for future functional enhancements, it is recommended that they be driven as illustrated for system upgradability.

DRAM HIDDEN-REFRESH CYCLE

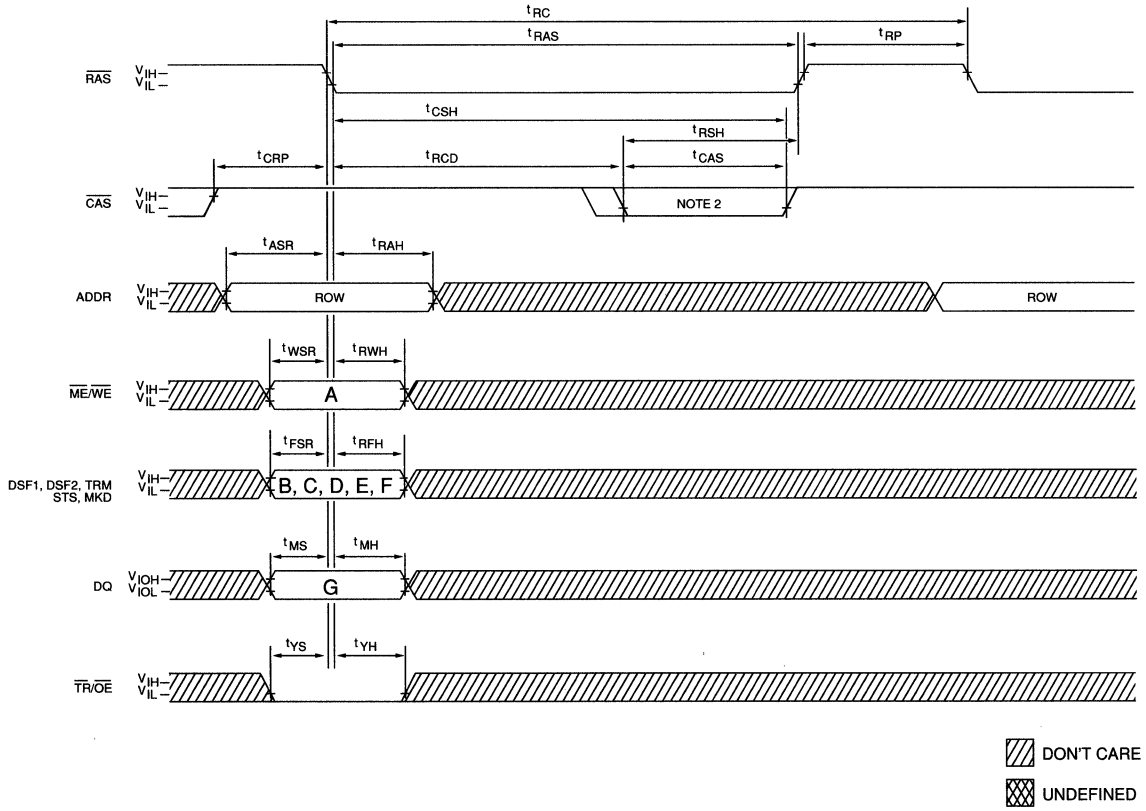


NOTE: 1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}$/$\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}$/$\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}$/$\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}$/$\overline{OE}$.

DRAM/BMR TRANSFER CYCLE FUNCTION TABLE

LOGIC STATES (RAS Falling Edge)							FUNCTION	CODE
A ME/WE	B DSF1	C DSF2	D TRM	E STS	F MKD	G DQ (input)		
1	0	0	1	0	X[1]	X	BMR READ TRANSFER (DRAM→BMR TRANSFER)	BMR-RT
1	0	0	1	1	X[1]	X	BMR READ TRANSFER (DRAM→invert→BMR TRANSFER)	BMR-IRT
0	0	0	1	0	X[1]	MASK	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	BMR-WT
0	0	0	1	1	X[1]	MASK	BMR WRITE TRANSFER (BMR→invert→DRAM TRANSFER)	BMR-IWT
1	1	1	0	X	X[1]	X	CLEAR BMR (CLR-BMR)	CLR- BMR

DRAM/BMR TRANSFERS



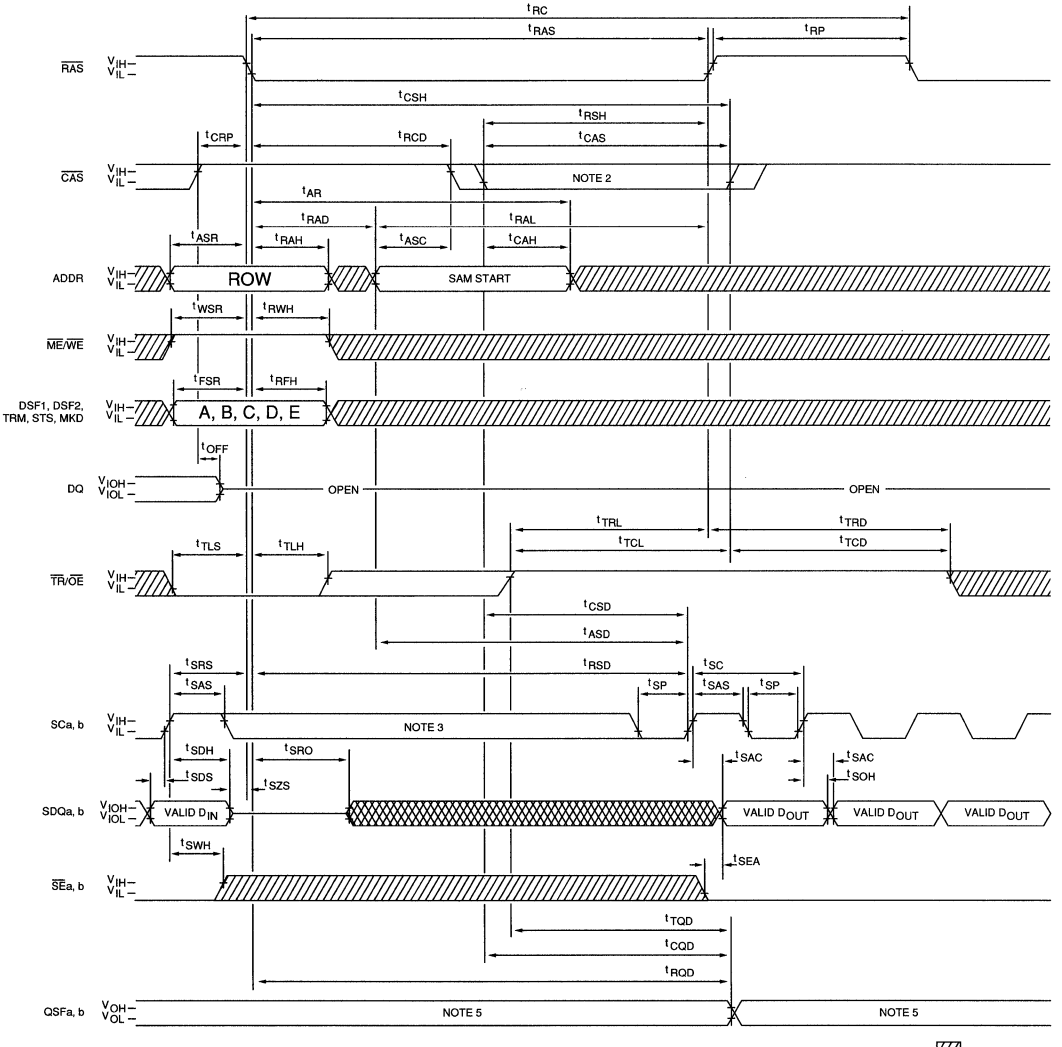
NOTE: 1. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.
2. It is not necessary to drop CAS during a DRAM/BMR TRANSFER.

READ TRANSFER CYCLE FUNCTION TABLE[1]

LOGIC STATES[2] (RAS Falling Edge)					FUNCTION	CODE
A DSF1	B DSF2	C TRM	D STS	E MKD		
0	0	0	0/1[2]	X	READ TRANSFER (DRAM→SAM)	RW
1	0	0	0/1[2]	X	SPLIT READ TRANSFER (DRAM→SAM)	SRT
0	1	1	0/1[2]	X	BIT MASKED READ TRANSFER	BMRT
1	1	1	0/1[2]	X	BIT MASKED SPLIT READ TRANSFER	BMSRT
1	0	1	0/1[2]	0/1[3]	BMR→SAM TRANSFER	BMR-SAM

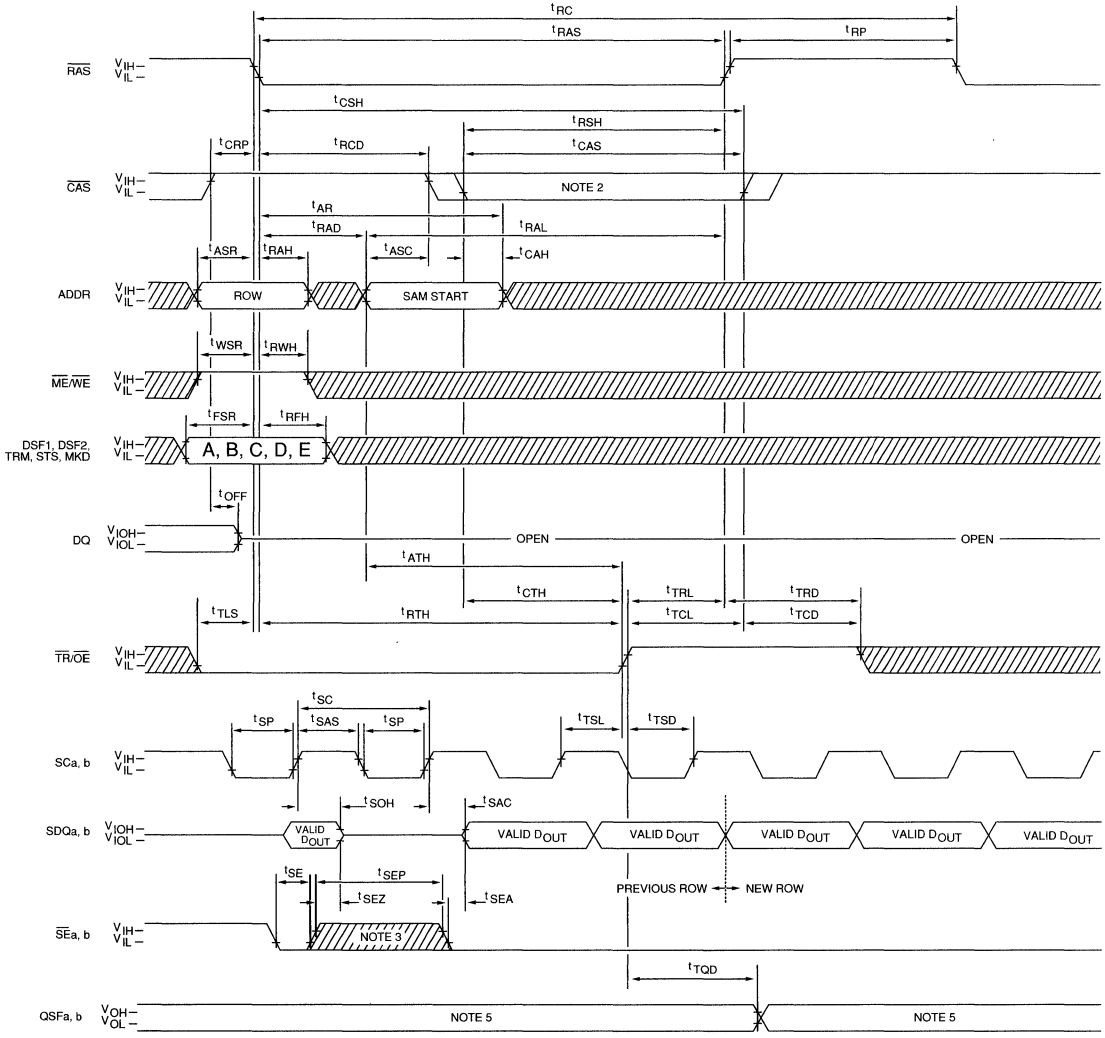
NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for READ TRANSFER cycle timing diagrams on the following pages.
2. The state of STS at the falling edge of $\overline{RAS}$ determines the SAM involved in the transfer. When STS = LOW the transfer is to SAMa; when STS = HIGH the transfer is to SAMb.
3. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.

READ TRANSFER[1,4]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



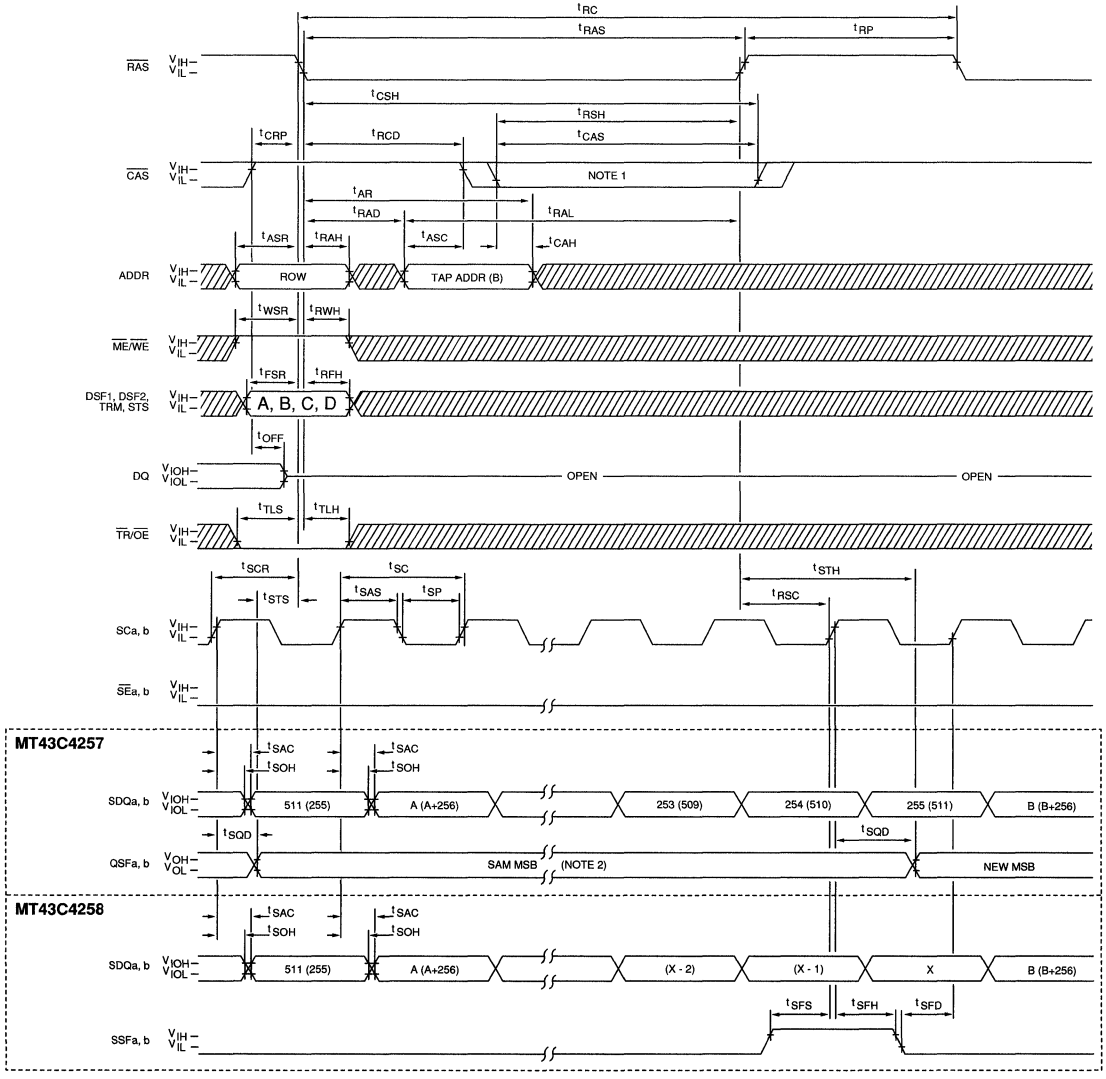
NOTE:
1. QSF = "OPEN"; SSF = "Don't Care"
2. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
3. There must be no rising edges on the SC input during this time period.
4. The logic states of "A", "B", "C", and "D" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

REAL-TIME READ TRANSFER[1,4]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL OUTPUT mode)



NOTE:
1. QSF = "OPEN"; SSF = "Don't Care"
2. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed
3. The $\overline{SE}$ pulse is shown to illustrate the serial output enable and disable timing. It is not required.
4. The logic states of "A", "B", "C", and "D" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
   QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SPLIT READ TRANSFER[3]
(SPLIT DRAM-TO-SAM TRANSFER)



DON'T CARE

UNDEFINED

NOTE:
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused for the idle half.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
3. The logic states of "A", "B", "C", and "D" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.

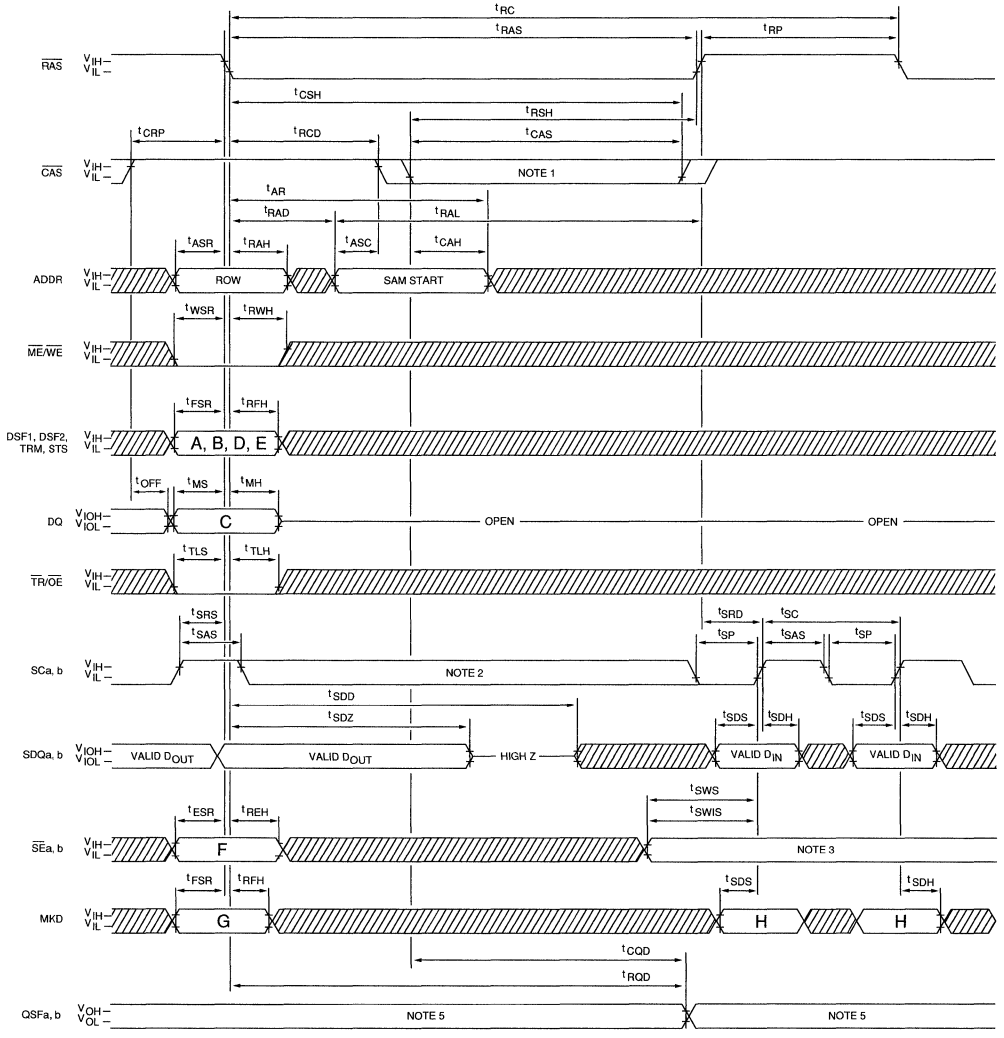
WRITE TRANSFER CYCLE FUNCTION TABLE[1]

LOGIC STATES								FUNCTION	CODE
RAS Falling Edge							SC		
A DSF1	B DSF2	C DQ	D TRM	E STS	F $\overline{SE}$	G MKD	H MKD		
0	0	X	0	0/1[2]	0	X	-	WRITE TRANSFER (SAM→DRAM)	WT
0	0	X	0	0/1[2]	1	X	-	PSEUDO WRITE TRANSFER	PWT
1	0	mask	0	0/1[2]	X	X	-	SPLIT WRITE TRANSFER (SAM→DRAM)	SWT
0	1	mask	0	0/1[2]	X	X	-	DQ MASKED WRITE TRANSFER (SAM→DRAM)	DMWT
0	1	X	1	0/1[2]	X	X	0/1[4]	BIT MASKED WRITE TRANSFER (SAM→DRAM)	BMWT
1	1	mask	1	0/1[2]	X	X	0/1[4]	BIT MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	BMSWT
1	0	X	1	0/1[2]	X	0/1[3]	-	SAM→BMR TRANSFER	SAM-BMR

NOTE:
1. QSF = "OPEN"; SSF = "Don't Care."
   Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" , "F", "G", and "H" for WRITE TRANSFER cycle timing diagrams on the following pages.
2. The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW the transfer is to SAMa; when SAM = HIGH the transfer is to SAMb.
3. Serial Mask Input (SMI) mode is enabled if MKD = HIGH and disabled if MKD = LOW.
4. When in the SMI mode (see BMR transfer waveforms) MKD is the SMI data input. MKD data is clocked into all bit planes of the bit mask register with SCb. A logic "1" on MKD will allow data to pass through the mask; a logic "0" will mask the corresponding location of the SAM during a BIT MASKED TRANSFER. BIT MASKED TRANSFERs to or from SAMa must not take place while mask data is being serially input via SCb and MKD.

WRITE TRANSFER[4]

(When part was previously in the SERIAL OUTPUT mode)

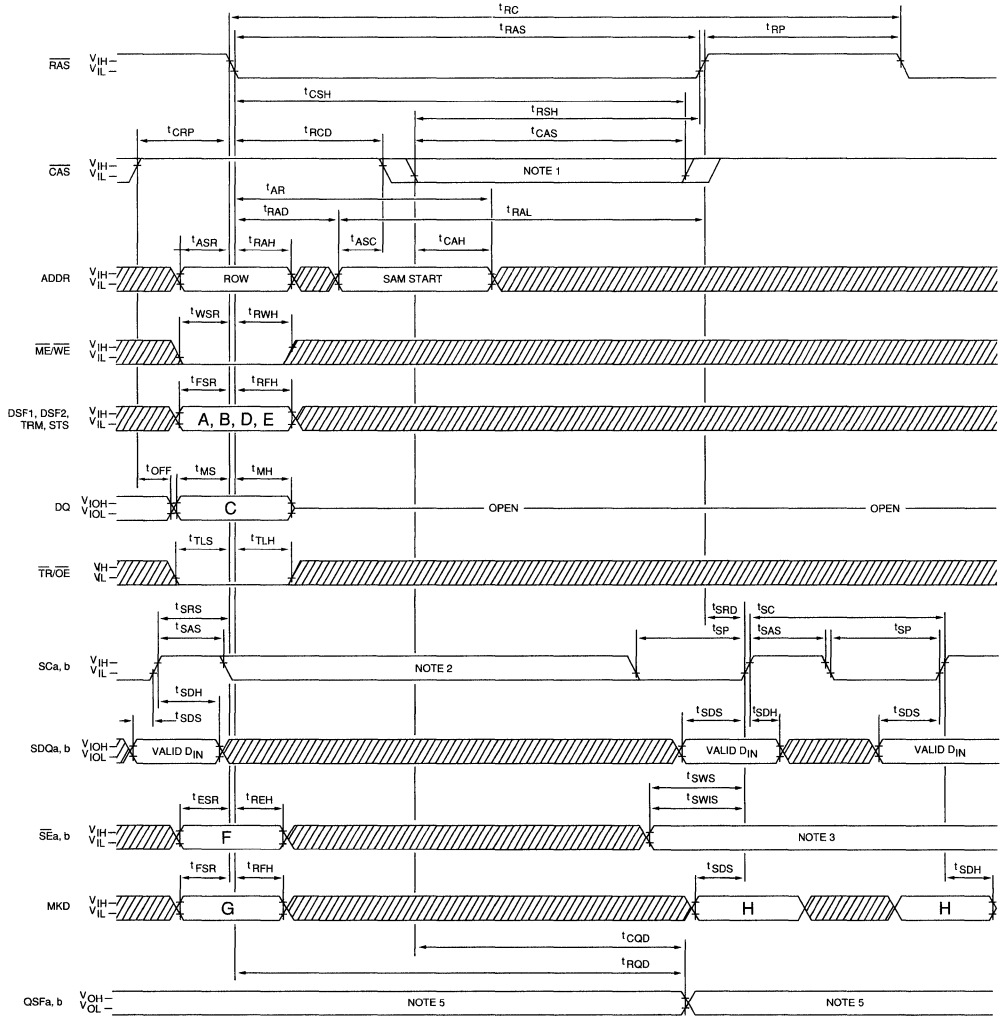


NOTE:

1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. There must be no rising edges on the SC input during this time period.
3. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed. SSFa,b = "don't care" (MT43C4258).

WRITE TRANSFER[4]

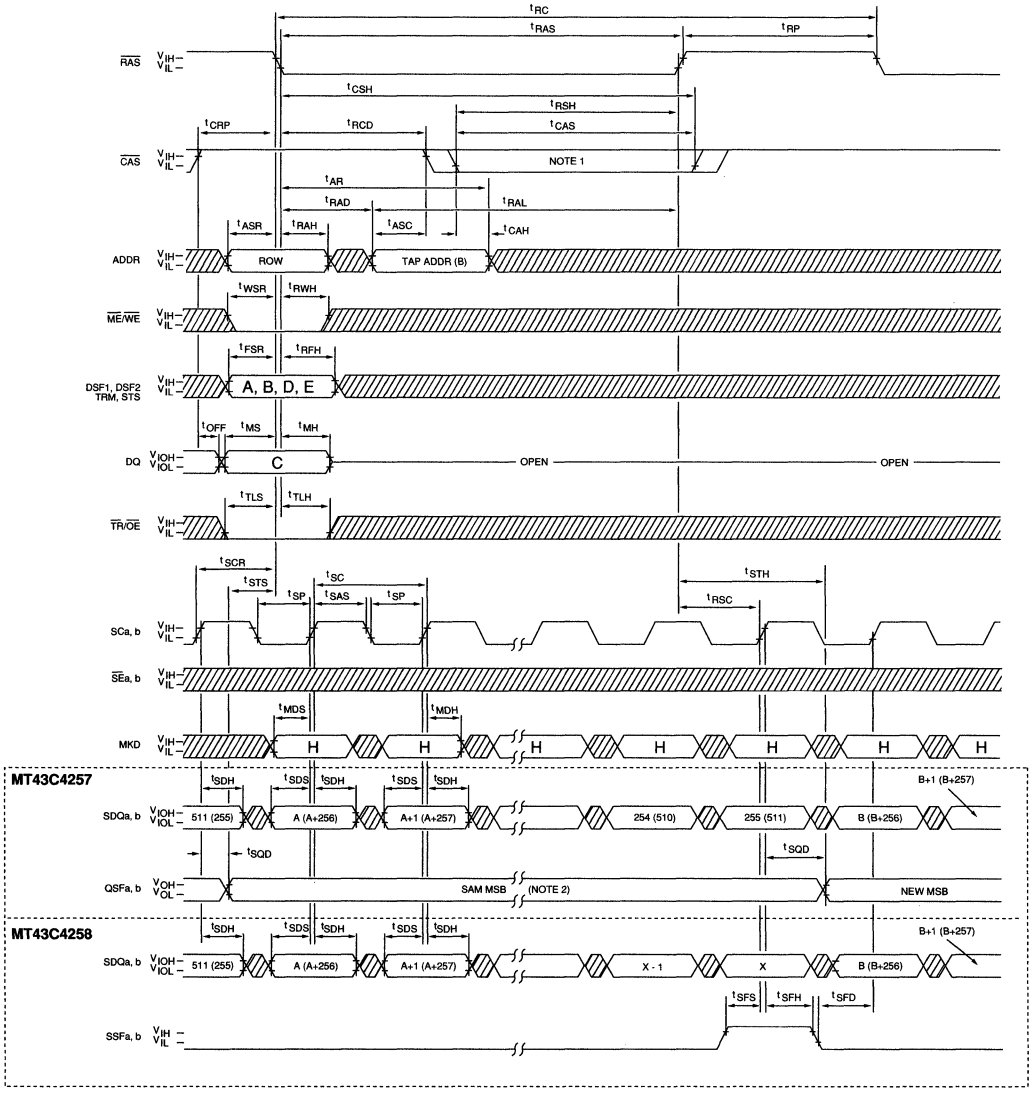
(When part was previously in the SERIAL INPUT mode)



NOTE:

1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed. SSFa,b = "don't care" (MT43C4258).

SPLIT WRITE TRANSFER[3]
(SPLIT SAM-TO-DRAM TRANSFER)

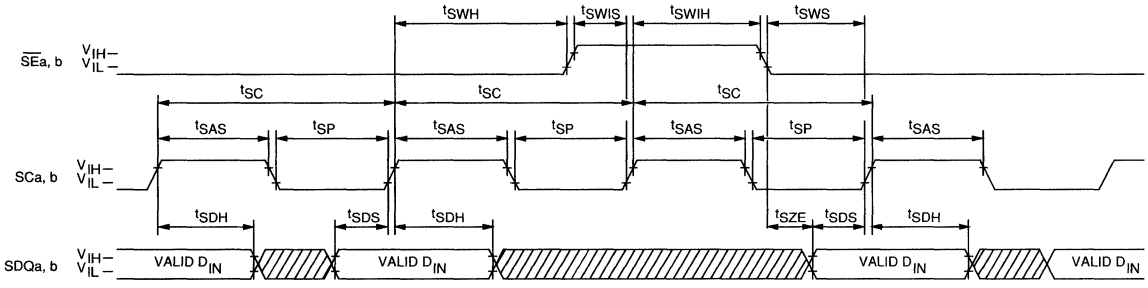


DON'T CARE

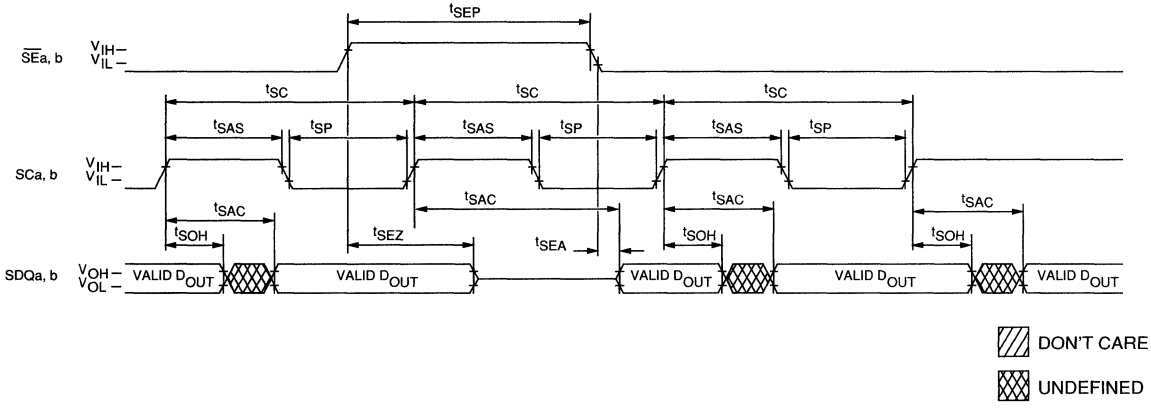
UNDEFINED

NOTE:
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address load for the addressed SAM will be reused.
2. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
   QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
3. The logic states of "A", "B", "C", "D", "E", and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.

SAMa or SAMb SERIAL INPUT



SAMa or SAMb SERIAL OUTPUT



NOTE : $\overline{SE}$a, SCa and SDQa are used when accessing SAMa and $\overline{SE}$b; SCb and SDQb are used when access in SAMb.

TRIPLE PORT DRAM

128K x 8 DRAM WITH DUAL 256 x 8 SAMS

FEATURES

- Three asynchronous, independent, data access ports
- Fast access times – 80ns random, 25ns serial
- Operation and control compatible with 1 Meg VRAMS
- High performance CMOS silicon gate process
- Low power: 15mW standby; 450mW active, typical
- 512-cycle refresh within 8ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- FAST PAGE MODE access cycles
- Two bidirectional Serial Access Memories (SAMs)
- Fully static SAMs and Mask Register, no refresh required
- 2048-bit Transfer Mask Register
- SERIAL MASK DATA INPUT mode

SPECIAL FUNCTIONS

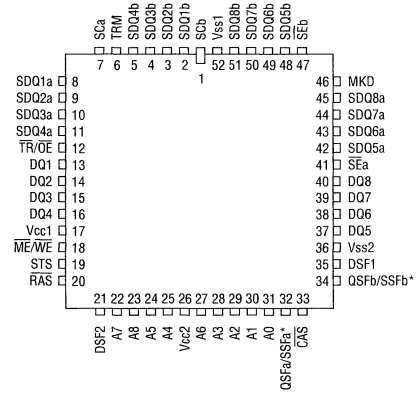
- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ AND WRITE TRANSFERS
- BLOCK WRITE
- BIT MASKED TRANSFERS

OPTIONS — MARKING

- Timing (DRAM, SAMs)
  - 80ns, 25ns — -8
  - 100ns, 30ns — -10
  - 120ns, 35ns — -12
- Packages
  - Plastic LCC (750 mil) — EJ
- Functionality
  - QSF output (indicates SAM half accessed) — 43C8128
  - SSF input (Split SAM special function, stop count) — 43C8129

PIN ASSIGNMENT (Top View)

52-PIN PLCC (D-3)



* MT43C8128/MT43C8129

GENERAL DESCRIPTION

The MT43C8128/9 are high speed, triple port CMOS dynamic random access memories (TPDRAM) containing 1,048,576 bits. Data may be accessed by an 8 bit wide DRAM port or by either of two independently-clocked 256 x 8-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and the SAMs.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4) DRAM. Sixteen 256-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 8-bit random access I/O port, a pair of internal 2048 bit wide paths between the DRAM and the SAMs, and the pair of 8-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing, and address decoding logic.

All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 2048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 256 x 8-bit, Bit Mask Data Register can be parallel loaded from the DRAM or, either SAM, or it may be serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require any refresh.

The operation and control of the MT43C8128/9 are compatible with the operation of the MT42C8128 (128K x 8 Video RAM). However, the MT43C8128/9 offer an additional SAM and special features that may be used to enhance system performance.

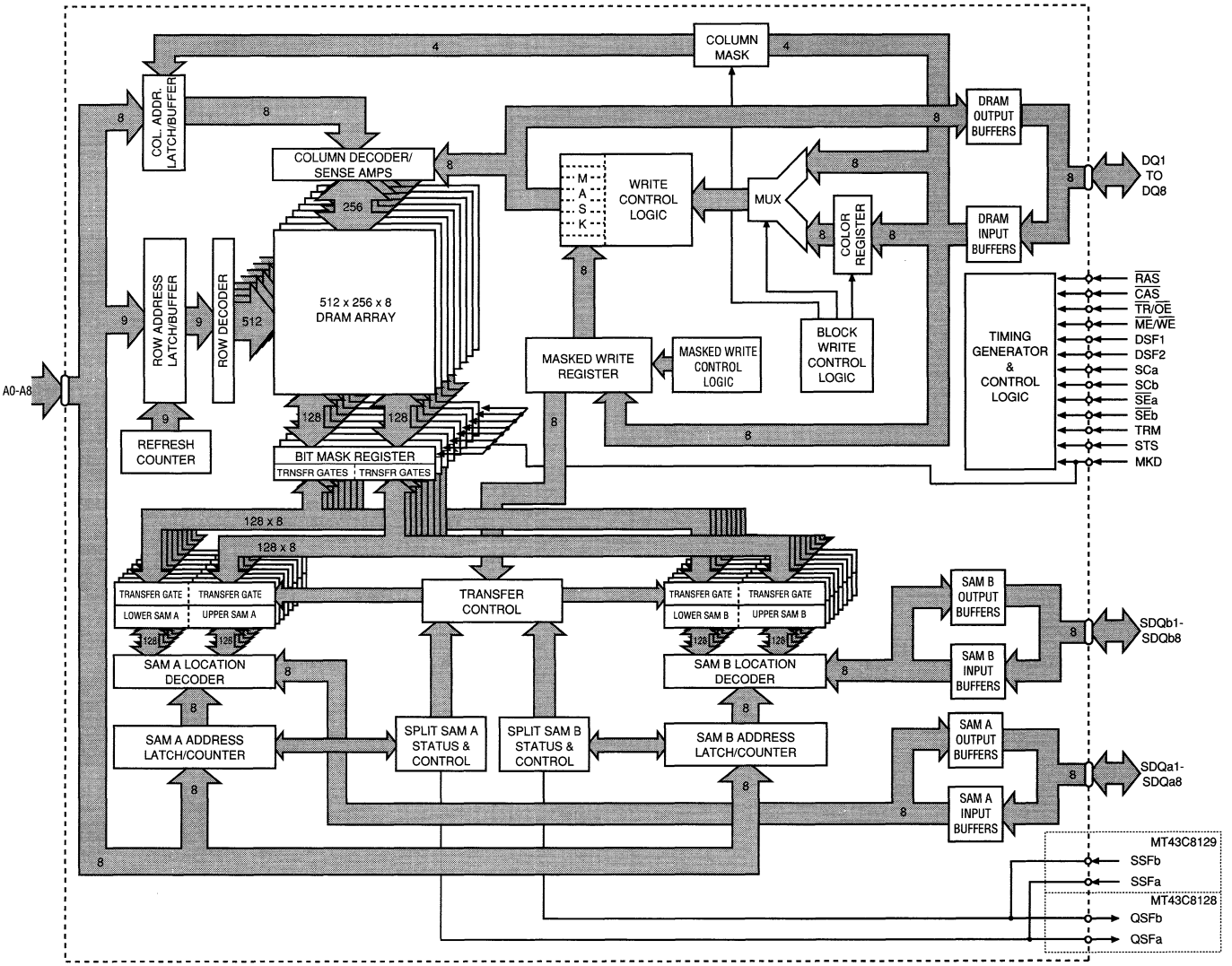


Figure 1
MT43C8128/9 BLOCK DIAGRAM

PIN DESCRIPTIONS

PLCC PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7	SCa	Input	Serial Clock, SAMa: Clock input to the serial address counter for the SAMa registers and strobe for SAMa control and data inputs.
1	SCb	Input	Serial Clock, SAMb: Clock input to the serial address counter for the SAMb registers and strobe for SAMb control and data inputs.
12	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at the falling edge of $\overline{RAS}$, or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a high impedance state.
18	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
41	$\overline{SE}$a	Input	Serial Port Enable SAMa: $\overline{SE}$a enables Port A serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$a is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
47	$\overline{SE}$b	Input	Serial Port Enable, SAMb: $\overline{SE}$b enables Port B serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. $\overline{SE}$b is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
35	DSF1	Input	Special Function (Control) 1: DSF1 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
21	DSF2	Input	Special Function (Control) 2: DSF2 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
20	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row-address bits and as a strobe for control and data inputs.
33	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 8 column-address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and as a strobe for control and data inputs.

PIN DESCRIPTIONS (Continued)

PLCC PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
31, 30, 29, 28 25, 24, 27, 22 23	A0 - A8	Input	Address Inputs: For DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 8-bit word out of the 128K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and A0-A7 indicate the SAM start address (when $\overline{CAS}$ goes LOW). A7, A8 = "don't care" for the start address when doing SPLIT TRANSFER.
19	STS	Input	SAM Transfer Select: The state of STS at $\overline{RAS}$ time determines which SAM is involved in a transfer (SAMa=LOW, SAMb=HIGH).
46	MKD	Input	Mask Data Input: MKD is used during BIT MASK REGISTER LOAD cycles to enable or disable the serial mask input mode (SMI). If SMI is enabled (MKD=HIGH at $\overline{RAS}$), then MKD is used as mask data input and is clocked by SCb into the mask data register.
6	TRM	Input	Transfer Mask Select: TRM is used to select between NORMAL TRANSFER cycles and BIT MASKED TRANSFER or BIT MASK REGISTER LOAD cycles.
13, 14, 15, 16 37, 38, 39, 40	DQ1 - DQ8	Input/ Output	DRAM Data I/O: Data inputs and outputs for the DRAM memory array; inputs for the MASK and COLOR REGISTER load cycles; address mask inputs for BLOCK WRITE cycles.
8, 9, 10, 11 42, 43, 44, 45	SDQa1-SDQa8	Input/ Output	Serial Data I/O, SAMa: Input, Output, or High-Z.
2, 3, 4, 5 48, 49, 50, 51	SDQb1-SDQb8	Input/ Output	Serial Data I/O, SAMb: Input, Output, or High-Z.
32	QSFa/SSFa	Output Input	Split SAM Status, SAMa (MT43C8128): QSFa indicates which half of SAMa is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMa (MT43C8129): SSFa=HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFa is synchronized with SCa.
34	QSFb/SSFb	Output Input	Split SAM Status, SAMb (MT43C8128): QSFb indicates which half of SAMb is being accessed (Lower = LOW, Upper = HIGH). Split SAM Special Function, SAMb (MT43C8129): SSFb=HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFb is synchronized with SCb.
17, 26	Vcc	Supply	Power Supply: +5V ±10%
52, 36	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT43C8128/9 may be divided into four functional blocks (see Figure 1): the DRAM and its special functions, the Bit Mask Register (BMR), the two Serial Access Memories (SAMs), and the DRAM/SAM/BMR transfer circuitry. All the operations described below are also shown in the AC Timing Diagrams section of this data sheet and are summarized in the Functional Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the TR/OE pin will be shown as TR/(OE).*

DRAM OPERATION

This section describes the operation of the random access port and the special functions associated with the DRAM.

DRAM REFRESH (ROR, CBR, and HR)

Like any DRAM-based memory, the MT43C8128/9 TPDRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 8ms. The MT43C8128/9 supports CAS-BEFORE-RAS, RAS-ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

For RAS-ONLY REFRESH cycles, the refresh address must be generated externally and applied to the A0-A8 inputs . The DQ pins remain in a High-Z state for both the RAS ONLY and CAS-BEFORE-RAS cycles.

HIDDEN REFRESH (HR) cycles are performed by toggling RAS (while keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM and Bit Mask Register portions of the MT43C8128/9 are fully static and do not require any refreshing.

DRAM READ AND WRITE CYCLES (RW)

The DRAM portion of the TPDRAM is nearly identical to standard 128K x 8 DRAMs. However, because several of the DRAM control pins are used for additional functions on this device, several conditions that were undefined or "don't care" states for the DRAM are specified for the TPDRAM. These conditions are highlighted in the following discussion. In addition, the TPDRAM has several special functions that may be used when writing to the DRAM.

The 17 address bits used to select an 8-bit word from the 131,072 available are latched into the chip using the A0-A8, RAS, and CAS inputs. First, the 9 row-address bits are setup on the address inputs and clocked into the part when RAS transitions from HIGH to LOW. Next, the 8 column-address bits (A0 - A7) are setup on the address inputs and clocked in when CAS goes from HIGH to LOW.

For single port DRAMS, the OE pin is a "don't care" when RAS goes LOW. For the TPDRAM, (TR)/OE is used when RAS goes LOW, to select between DRAM and TRANSFER cycles. (TR)/OE must be HIGH at the RAS HIGH-to-LOW transition for all DRAM operations.

If (ME)/WE is HIGH when CAS goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ8 port. The (TR)/OE input must transition from HIGH-to-LOW sometime after RAS falls to enable the DRAM output port.

For single port DRAMs, WE is a "don't care" when RAS goes LOW. For the TPDRAM, ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle or a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any TPDRAM non-masked access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH to LOW transition. If (ME)/WE is LOW when CAS goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells.

The TPDRAM can perform all the normal DRAM cycles: READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE, and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

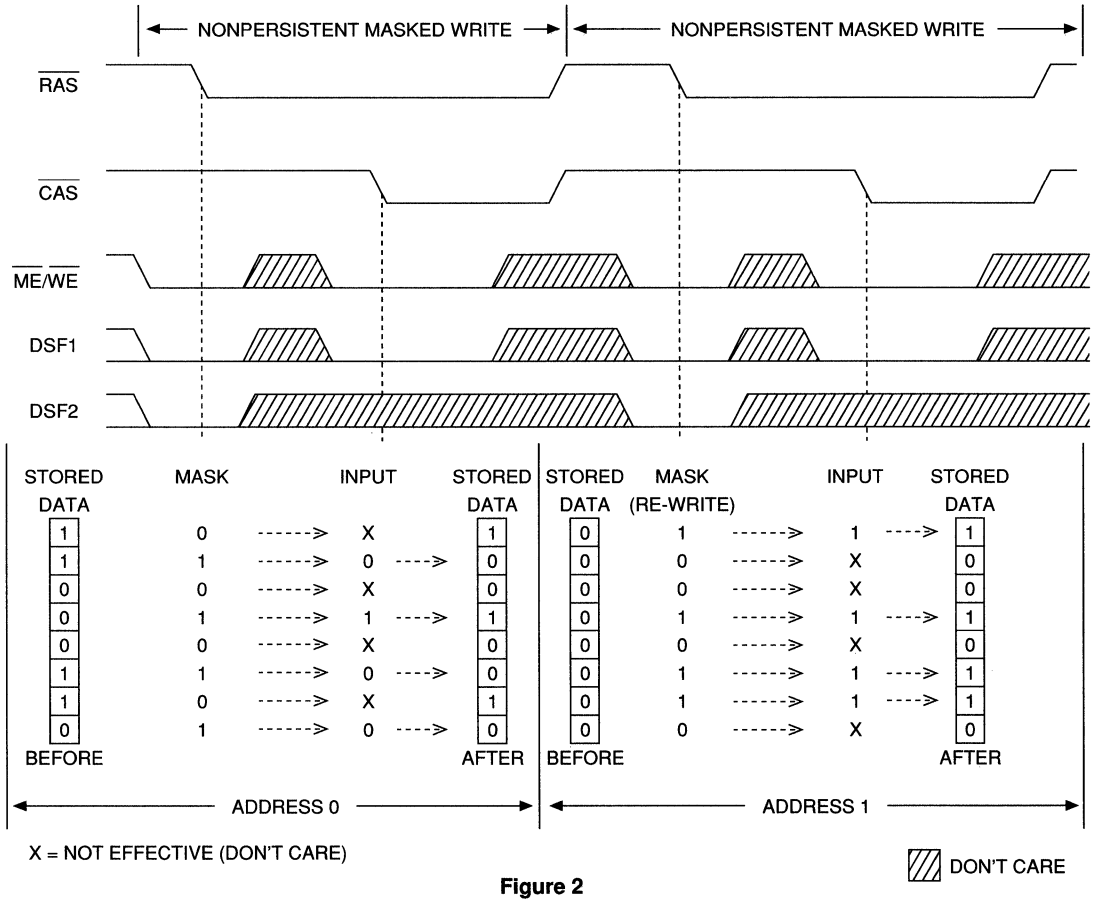


Figure 2
NONPERSISTENT MASKED WRITE EXAMPLE

NONPERSISTENT MASKED WRITE (RWNM)

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within an 8-bit word. The MT43C8128/9 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$), DSF1 and DSF2 are LOW at the $\overline{RAS}$ HIGH-to-LOW transition, the data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. This convention is used for all masks on the MT43C8128/9. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. When using NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is loaded into the mask data register at every falling edge of $\overline{RAS}$. FAST PAGE MODE may be used in tandem with NONPERSISTENT MASKED WRITE to write several column locations using the same mask during one $\overline{RAS}$ cycle. An example of NONPERSISTENT MASKED WRITE cycle is shown in Figure 2.

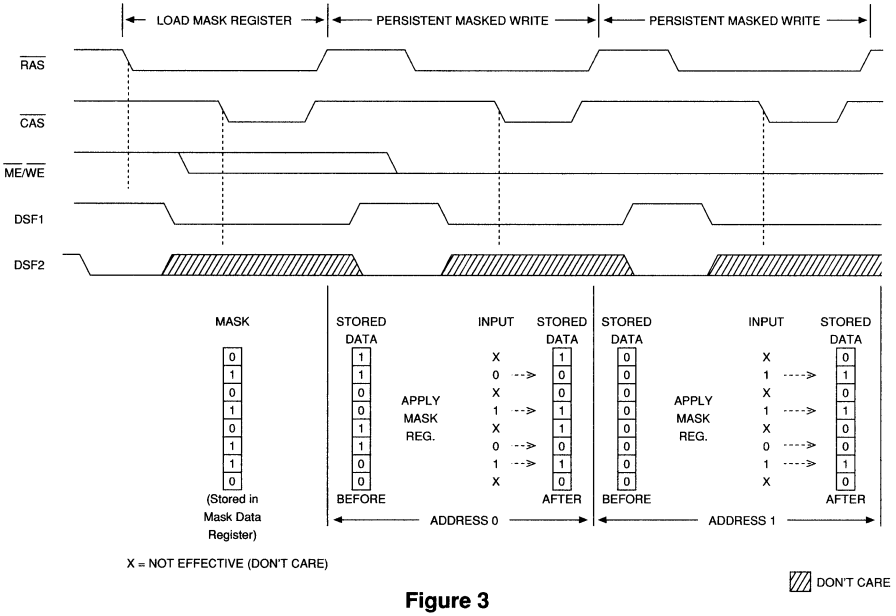


Figure 3
PERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE (RWOM)

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/(\overline{WE})$ and DSF1 HIGH, and DSF2 LOW when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW, provided DSF1 is LOW (see the LOAD MASK REGISTER description).

Mask data may also be loaded into the mask register by simply performing a NONPERSISTENT MASKED WRITE before the PERSISTENT MASKED WRITE cycles.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{ME}/(\overline{WE})$ and DSF2 LOW and DSF1 HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present at the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls. Another PERSISTENT MASKED WRITE cycle may be performed without reloading the register. Figure 3 shows the LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycle operations. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow systems that cannot output data at $\overline{RAS}$ time to perform MASKED WRITE cycles. PERSISTENT MASKED WRITE can also operate in FAST PAGE MODE.

BLOCK WRITE (BW)

If DSF1 is HIGH when $\overline{CAS}$ goes LOW, the MT43C8128/9 will perform a BLOCK WRITE cycle ($\overline{WE}$ = "don't care") instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register (instead of the DQ inputs) are directly written to four adjacent column locations (see Figure 4). A total of 32 bits will be written simultaneously, improving the normal DRAM fill rate by four times. The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However, when $\overline{CAS}$ goes LOW, only the A2-A7 inputs are used. A2-A7 specify the "block" (out of the 64 possible) of four adjacent column locations that will be accessed. When $\overline{CAS}$ goes LOW, the DQ inputs are then used to determine which combination of the four column locations will be changed. DQ1 acts as a write enable for column location A0=0, A1=0; DQ2 controls column location A0=1, A1=0; DQ3 controls A0=0, A1=1; and DQ4 controls A0=1, A1=1. The write enable controls are active HIGH; a logic 1 enables and a logic 0 disables the WRITE function.

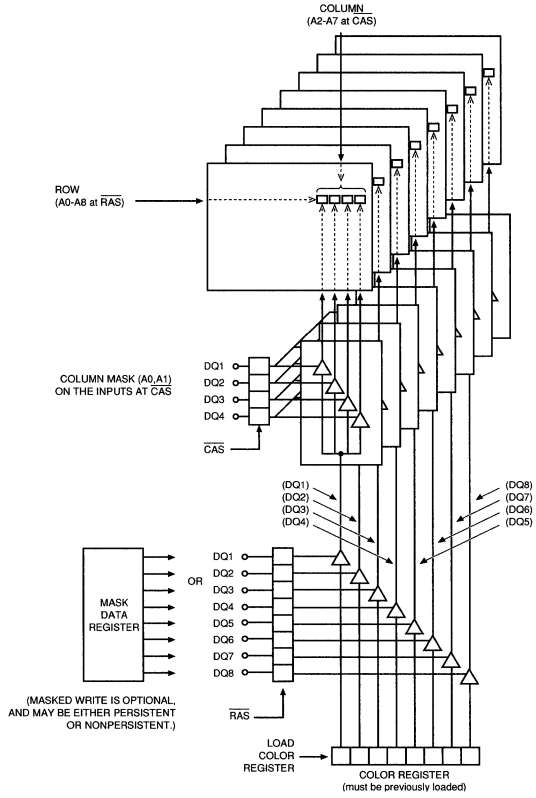


Figure 4
BLOCK WRITE EXAMPLE

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane. The DQ mask is not used in this mode.

Note: *When performing a BLOCK WRITE, $\overline{WE}$ is a "don't care". This means LATE-WRITEs in the BW mode are not allowed.*

NONPERSISTENT MASKED BLOCK WRITE (BWNM)

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{ME}$/($\overline{WE}$) LOW and DSF1 LOW when $\overline{RAS}$ goes LOW, initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH, when $\overline{CAS}$ goes LOW, to perform a NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes may be masked and any combination of the eight column locations may be masked.

PERSISTENT MASKED BLOCK WRITE (BWOM)

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF1 is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

DRAM REGISTER OPERATIONS

The MT43C8128/9 contains two 8-bit registers that are used as data registers for special functions. This section describes how to load these registers.

LOAD MASK REGISTER (LMR)

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF1 is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}$/($\overline{OE}$), $\overline{ME}$/($\overline{WE}$), and DSF1 being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a REGISTER load cycle. DSF1 is used when $\overline{CAS}$ goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: *For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NONPERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed*

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF1 is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

This section describes transfer operations between the DRAM and either SAM. The direction of the transfer is specified with respect the DRAM portion of the device. A write is referenced to the DRAM array and a read is referenced from the array.

Note: *The three ports of the TPDRAM are independent and asynchronous to one another. Any or all of the ports may be accessed simultaneously at the maximum allowable frequencies. The only time the ports are synchronized is during transfers to or from the DRAM and SAM portions of the device. A transfer involving a SAM does not affect access from the other SAM port. Both SAMs may be accessed during a DRAM/BMR transfer operation or any other DRAM access cycle other than a SAM transfer.*

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of $\overline{RAS}$. The state of STS when $\overline{RAS}$ goes LOW indicates which SAM the TRANSFER will address. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER. At the same time, DSF1 is used to select between normal TRANSFER cycles and SPLIT TRANSFER cycles and DSF2 is used to select between normal TRANSFER cycles and MASKED TRANSFER cycles. A TRANSFER cycle can be performed without dropping $\overline{CAS}$. In this case, the previously loaded Tap address will be used.

The MT43C8128/9 include a feature called BIT MASKED TRANSFER, which uses a third, 2048-bit data register to individually mask every bit involved in a TRANSFER operation. The BIT MASKED TRANSFER may be applied to either READ or WRITE TRANSFERS. The TRM pin is used to select between NORMAL and BIT MASKED TRANSFER (or BIT MASK REGISTER LOAD) cycles. The type of transfer operation is always selected on the falling edge of $\overline{RAS}$.

NORMAL TRANSFERS

The MT43C8128/9 support all of the popular transfer cycles available on the 1 Meg video RAMs. Each of these is described in the following section.

READ TRANSFER (RT)

A READ TRANSFER cycle is selected if $\overline{ME}/(\overline{WE})$ is HIGH, and DSF1 and $\overline{TR}/(\overline{OE})$ are LOW when $\overline{RAS}$ goes LOW. When $\overline{RAS}$ goes LOW, the READ TRANSFER is to SAMa if STS = LOW, or to SAMb if STS = HIGH. The row address bits indicate the eight 256-bit DRAM rows that are to be transferred to the eight SAM data registers. The column address bits indicate the start address (or Tap point) of the next serial output cycle from the designated SAM data registers. QSF indicates the SAM half being accessed: LOW if the lower half; HIGH if the upper. Performing a READ TRANSFER cycle sets the direction of the selected SAMs I/O buffers to the output mode.

To complete a REAL-TIME READ-TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are LOW. In order to synchronize the REAL-TIME READ-TRANSFER to the serial clock, the rising edge of $\overline{TR}/(\overline{OE})$ must occur between the rising edges of successive clocks on the SC input (refer to the AC timing diagrams). A "regular" READ TRANSFER is not sychronized with the SC pin of the addressed SAM. This type of RT is performed when $\overline{TR}/(\overline{OE})$ is taken HIGH "early," without regard to the falling edge of $\overline{CAS}$. The transfer will be completed internally by the device. The first serial clock must meet the tRSD, tCSD and tASD delays. (see READ TRANSFER AC timing diagram). The 2048 bits of DRAM data are then written into the SAM data registers, and the selected SAM's Tap address that was stored in the internal, 8-bit Tap address register is loaded into the address counter. If $\overline{SE}$ for the SAM selected ($\overline{SE}$a for SAMa) is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. $\overline{SE}$ enables the serial outputs, and may be either HIGH or LOW during this operation.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream (the "full" READ TRANSFER cycle has to occur immediately after the final bit of "old data," and before the first bit of "new data" is clocked out of the SAM port).

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer can occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is relaxed for SRT cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ and $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles.

SPLIT TRANSFERs do not change the SAM I/O direction. A normal (nonsplit) READ TRANSFER cycle must precede any sequence of SRT cycles to put the SAM I/O in the output mode and provide the initial SAM Tap address (which half). Then an SRT may be initiated by taking DSF1 HIGH and selecting the desired SAM (using STS) when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. When an SRT cycle is initiated, the half of

the SAM not actively being accessed will be the half that receives the transfer. When $\overline{CAS}$ falls, address pins A0-A6 determine the Tap address for the SAM-half selected; A7 = "don't care." If $\overline{CAS}$ does not fall, the previously loaded Tap address will be reused and the TRANSFER will be to the idle half.

Figure 5 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The purpose of the SRT from the same row is to initiate the split SAM operating mode and load the Tap address for the upper half of the SAM. For the MT43C8128, serial access continues and when the SAM address counter reaches 127 ("A7"=1, A0-A6=0), the QSF output for that SAM goes HIGH and the Tap address for the upper half is automatically loaded. Since the serial access has now switched to the upper half of the SAM, new data may now be transferred to the lower half. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed may now be repeated. For example, the next step in Figure 5 would be to wait until QSF went LOW (indicating that row-1 data is shifting out the lower SAM) and then transferring the upper half of row 1 to the upper SAM. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address load for the addressed SAM will be reused.

The split SAM operation is slightly different for the MT43C8129. Instead of having a QSF, this device has a Split SAM Special Function (SSF) input. With this input the serial access may be switched at will from one half of the SAM to the other. In other words, the address count may be stopped on the current half and the Tap address of the next half may be loaded, without waiting for the maximum address count of the current half (127; lower, 255; upper). If no SSF pulse is applied, the Tap address of the next half will be automatically loaded when the maximum count of the current SAM-half is reached. QSF = 0 when the Lower SAM (bits 0–255) is being accessed. QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

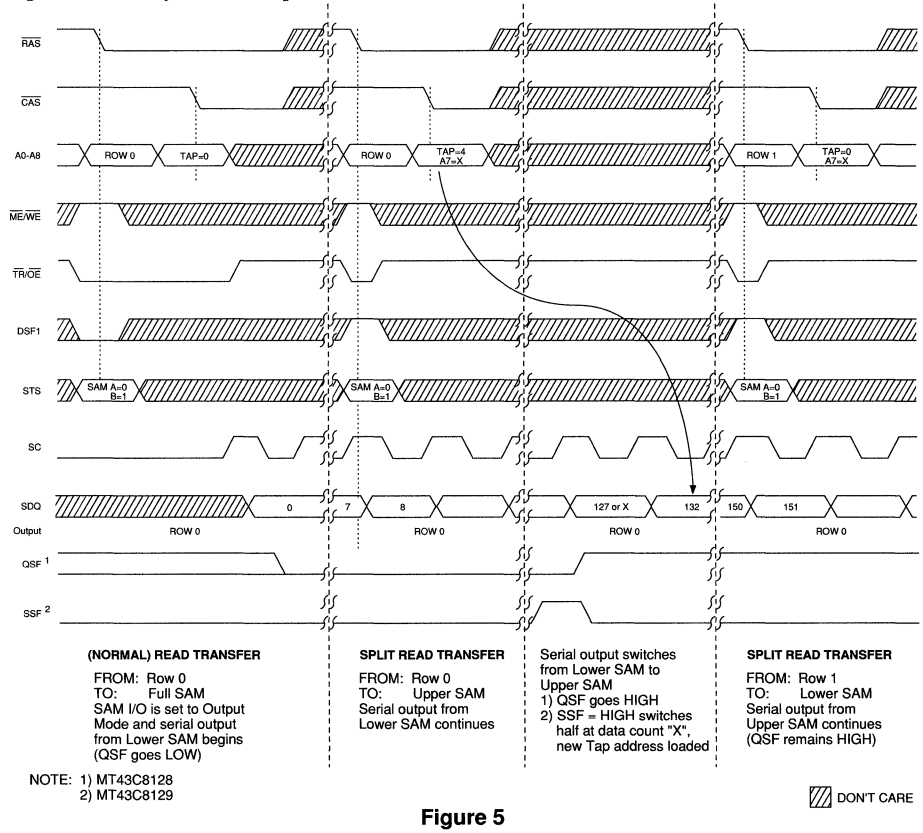


Figure 5

TYPICAL SPLIT READ TRANSFER INITIATION SEQUENCE

WRITE TRANSFER (WT)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously, except ($\overline{ME}$)/$\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The DSF2 input is used to select between the WT and DQ MASKED WRITE TRANSFER cycles, and must be LOW for the WT cycle. The STS pin is also taken LOW or HIGH to select SAMa or SAMb, respectively, when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row to which the SAM data register will be written, and the Tap address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. QSF indicates the SAM half being accessed; LOW if the lower half, HIGH if the upper. Performing a WT sets the direction of the SAM I/O buffers to the input mode.

PSEUDO WRITE TRANSFER (PWT)

The PSEUDO WRITE TRANSFER cycle can be used to change the direction of a SAM port from output to input without disturbing the DRAM data in the selected row. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with the $\overline{SE}$ of the appropriate SAM held HIGH instead of LOW. The addressed row will be refreshed. A DQ MASKED WRITE TRANSFER (with all bits masked) is an alternate method for changing the direction of the SAM port without disturbing the addressed row data.

DQ MASKED WRITE TRANSFER (DMWT)

The data being transferred from either SAM to the DRAM may be masked by performing a DQ MASKED WRITE TRANSFER cycle. The transfer of data may be selectively enabled for each of the eight DQ planes (see Figure 6). The DMWT cycle is identical to the WRITE TRANSFER cycle except DSF2 is HIGH and mask data must be on the DQ inputs at the falling edge of $\overline{RAS}$.

The complete SAM register will be transferred to the selected row in each DQ plane if the mask data input is HIGH, and the SAM register will not be transferred if the mask data input for that DQ plane is LOW. DRAM data is not disturbed in masked DQ planes.

SPLIT WRITE TRANSFER (SWT)

The SPLIT WRITE TRANSFER feature makes it possible to input and transfer uninterrupted bit streams. Figure 7 shows a typical initiation sequence for SWT cycles.

Like the SRT, the SPLIT WRITE TRANSFER cycle does not change the state of the SAM I/O buffers. A normal, DQ MASKED or PSEUDO WRITE TRANSFER cycle is required to set the Tap address and set the SAM I/O direction to input mode.

After the WT, a SWT is performed to enter the split SAM operating mode. This sets the Tap for the next half of the SAM. The addressed half of the SAM is immediately transferred to the first destination row. This half of the SAM may not yet contain valid data. However, another SWT to the same row will normally occur after this is loaded, so the initial invalid data will be overwritten. Another approach would be to initiate an SWT addressed to any DRAM row, but mask (disable) all eight of the DQ planes. This method can be used to initiate the SWT sequence without disturbing any DRAM data.

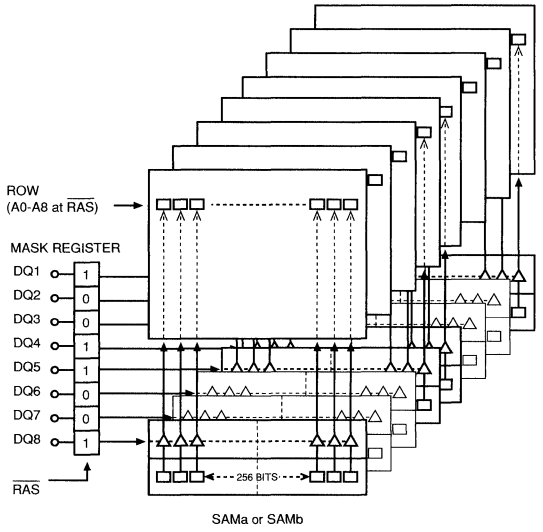


Figure 6
DQ MASKED WRITE TRANSFER

Write mask data must be supplied to the DQ inputs during every SWT cycle at $\overline{RAS}$ time. The mask data acts as an individual write enable for each of the eight DRAM DQ planes. For example, the DQ1 MASKED WRITE bit enables or disables the transfer of the SAM SDQ1 register to the DQ1 plane of the DRAM row selected (see the DQ MASKED WRITE TRANSFER description). As in all other MASKED WRITE operations, a HIGH enables the WRITE TRANSFER and a LOW disables the WRITE TRANSFER. As with SPLIT READ TRANSFER, the half of the SAM not receiving data will be the half transferred and the Tap address (A0-A6) for the other half is loaded when $\overline{CAS}$ falls (A7 is a "don't care"). If $\overline{CAS}$ does not fall, the previously loaded Tap address, A0-A6, will be reused. The TRANSFER will be to the idle half. When the serial clock crosses the half-SAM boundary, the new Tap address for that half is automatically loaded.

The QSFa and QSFb outputs (MT43C8128) indicate which half of SAMa or SAMb, respectively, is currently accepting data. After QSF goes HIGH, indicating that serial input has now switched to the upper SAM, the contents of the lower

half of the SAM may be transferred to any DRAM row. The cycle of checking for a change in QSF and then transferring the half of the SAM just filled may now be repeated. The next step on Figure 7 is to wait for QSF to go LOW and then SWT the contents of the upper half of the SAM to row 0. If the terminal count of the SAM half is reached before an SWT is performed for the next half, the access will be repeated from the same half and previously loaded address (access will not move to the next half).

When operating the MT43C8129 in the SWT mode, the address pointer may be changed, at will, to the new Tap address of the next half when the final desired input data is clocked-in. When the final data is input, the SSF input is taken HIGH at the corresponding rising edge of SC. The next SC rising edge will input data into the Tap location of the next half of the SAM. If SSF is not applied, the Tap address will be automatically loaded when the maximum Tap address count is reached for the current half (127 or 255). If SSF is HIGH at SC, before an SWT is performed for the next half, the access will jump to the old Tap address of the same half. Access will not preceed to the next half. If terminal count is reached before an SWT, the access will proceed as it does for the MT43C4257.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SCa,b and $\overline{SE}$a,b. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded during the DRAM-TO-SAM

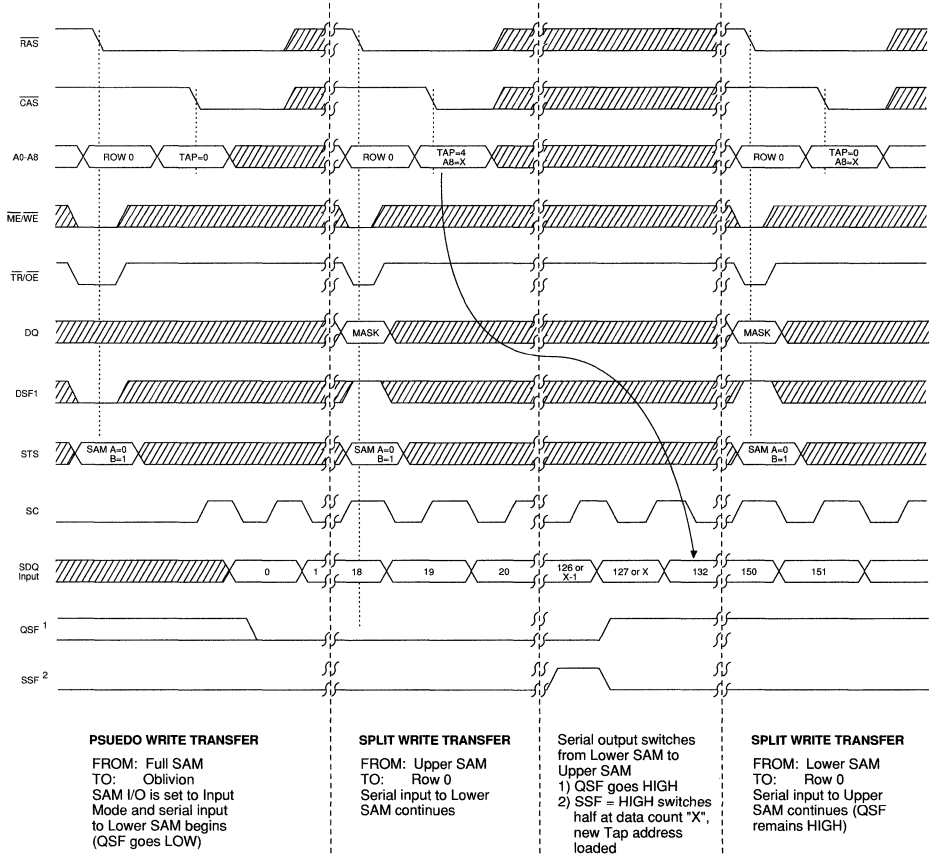


Figure 7

TYPICAL SPLIT WRITE TRANSFER INITIATION SEQUENCE

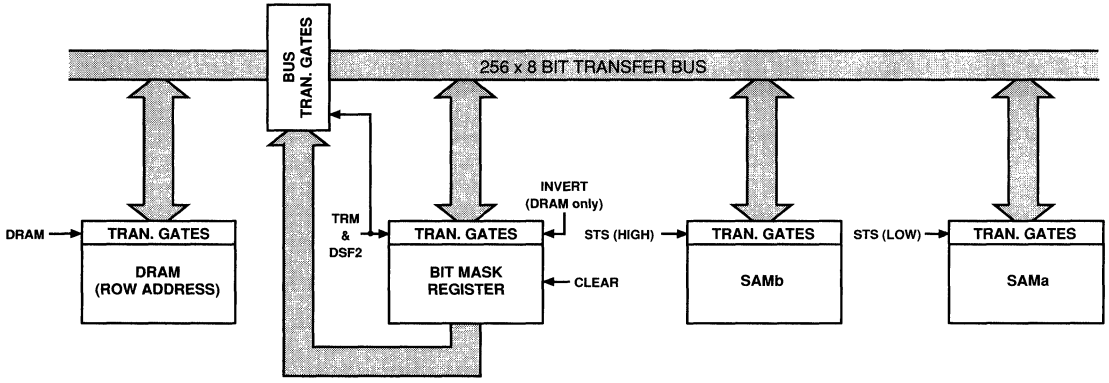


Figure 8
BIT MASKED TRANSFER BLOCK DIAGRAM

TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW. For the MT43C8128, the address progresses through the SAM and will wrap around (after count 127 or 255) to the Tap address of the next half, for split modes. Address count will wrap around (after count 255) to Tap address 0 if in the "full" SAM modes. For the MT43C8129, the address count will wrap as it does for the MT43C8128 or it may be triggered, at will, to the next half by the SSF input (split SAM modes). If SSF is HIGH at a LOW-to-HIGH transition of SC, the Tap address of the next half will be loaded into the address pointer. The following LOW-to-HIGH transition of SC will clock data from the Tap address of the new half.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address register (loaded when the serial input mode was enabled) will determine the serial address of the first 8-bit word written. $\overline{SE}$ acts as a WRITE ENABLE for serial input data and must be LOW for valid serial input. If $\overline{SE}$ = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{SE}$ input.

BIT MASKED TRANSFERS

This section describes transfers between the DRAM and either of the two SAMs using the BIT MASKED TRANSFER capability. Before performing these BIT MASKED TRANSFERS, the bit mask register must first be loaded with the mask data. See the next section, BIT MASK REGISTER OPERATIONS, for instructions on how to load the Bit Mask Register (BMR).

The BMR is a 2048-bit register that individually controls each of the 2048 transfer gates on the internal 256 x 8 transfer bus (see Figure 8). These bus transfer gates reside between the DRAM array and the three data registers and are set to the "pass-thru" mode for nonmasked transfers. For BIT MASKED TRANSFERs, the data in the BMR is coupled to the control inputs of the bus transfer gates. A logic "1" in the BMR will select the pass-thru (unmasked) mode for the corresponding SAM data bit, while a logic "0" will select the masked mode for that bit.

BIT MASKED TRANSFERs may be incorporated when doing READ, WRITE, SPLIT READ and SPLIT WRITE TRANSFERs. The timing and control required for any particular BIT MASKED TRANSFER cycle is identical to the corresponding normal TRANSFER cycle, except that TRM and DSF2 are HIGH instead of LOW. BIT MASKED TRANSFERs between the DRAM and either of the two SAM registers are possible. Figure 9 illustrates the BIT MASKED TRANSFER functions.

BIT MASKED READ TRANSFER (BMRT)

BIT MASKED READ TRANSFER can be used to transfer any combination of the 2048 bits contained in any DRAM row address to either of the two SAMs. The logic conditions and timing for the BMRT function are identical to the normal READ TRANSFER function except to select the BIT MASKED feature, TRM and DSF2 are HIGH. If a bit in the BMR is a logic "1", the bus connection between the corresponding DRAM bit and the selected SAM bit is enabled and the data at the destination (one of the SAMs for BMRT) will be changed to the source data (the DRAM row for BMRT).

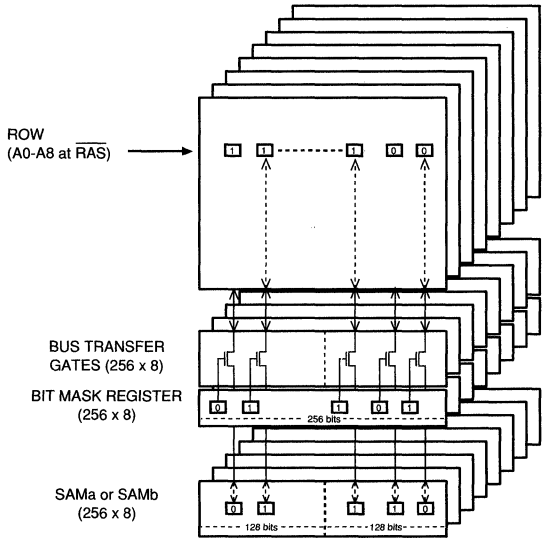


Figure 9
BIT MASK TRANSFER BLOCK DIAGRAM

BIT MASKED SPLIT READ TRANSFER (BMSRT)

The BIT MASKED SPLIT READ TRANSFER operation is identical to the normal SPLIT READ TRANSFER except that the bit mask (stored in the bit mask register) is applied to the transfer data by taking TRM and DSF2 HIGH when $\overline{RAS}$ falls. The remaining control timing is identical to the requirements for a normal SPLIT READ TRANSFER.

BIT MASKED WRITE TRANSFER (BMWT)

Like WRITE TRANSFER, the BIT MASKED WRITE TRANSFER function may be used to transfer data to any DRAM row address from either of the two SAM registers. In this case, the SAM data will be masked by the contents of the bit mask register before the data is written to the DRAM.

BIT MASKED SPLIT WRITE TRANSFER (BMSWT)

Like the other BIT MASKED TRANSFER cycles, the BMSWT is nearly identical to the SPLIT WRITE TRANSFER, except TRM and DSF2 are HIGH when $\overline{RAS}$ falls. Two masks are applied during a BMSWT operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at $\overline{RAS}$ time. If a DQ input is LOW at $\overline{RAS}$ time, none of the 128 SAM bits for that DQ plane will be transferred to the DRAM row-half selected. If a DQ input is HIGH, the 128 SAM bits for that row-half will be masked by the corresponding 128 mask register bits when written to the selected DRAM row-half. The remaining control timing is identical to the requirements for a normal SPLIT WRITE TRANSFER.

BIT MASK REGISTER OPERATIONS

This section describes how to transfer data to or from the Bit Mask Register (BMR) and how to clear the BMR's contents. Data may also be inverted when being transferred between the BMR and DRAM.

BMR READ TRANSFER (BMR-RT)

Any DRAM row may be transferred to the bit mask register by using the BMR READ TRANSFER function. When $\overline{RAS}$ falls, $\overline{TR}/(\overline{OE})$ is LOW to select a transfer cycle. TRM is HIGH to indicate that the BMR is involved in the TRANSFER cycle, and DSF2 is LOW to indicate that the data is to be transferred to the BMR (as opposed to using the contents of the BMR as bit mask data). The remainder of the timing and control required is identical to a normal READ TRANSFER cycle. No Tap address is loaded in this TRANSFER.

Note that the SAM transfer select (STS) pin is used to select whether non-inverted (STS=LOW) or inverted (STS=HIGH) data is transferred to the bit mask register. For all transfers to or from the bit mask register, the state of the MKD pin when $\overline{RAS}$ falls selects whether the Serial Mask Input (SMI) feature is enabled (see the Functional Truth Table). SMI is a special serial input mode that allows mask information to be clocked into the BMR at the same address location as the data clocked into SAMb (see the SMI mode description). MKD is LOW when $\overline{RAS}$ falls to disable SMI or HIGH to enable SMI. After the transfer is completed the MKD pin then acts either as a mask data input to the BMR (SMI enabled) or is "don't care" (SMI disabled). The MKD input is tied to the 8 bit-planes, the data on the MKD pin is written to each bit-plane simultaneously.

BMR INVERTED READ TRANSFER (BMR-IRT)

If the STS pin is HIGH at $\overline{RAS}$ time the DRAM data will be inverted before being written to the BMR. All 2048 bits involved in the transfer will be complemented. The functionality and logic levels for the other control inputs are identical to the BMR READ TRANSFER cycle. Note that MKD is still used to enable or disable the SMI mode. There is no added cycle time delay for either the BMR INVERTED READ or BMR INVERTED WRITE TRANSFER cycles.

BMR WRITE TRANSFER (BMR-WT)

The contents of the BMR may also be transferred to any DRAM row by using the BMR WRITE TRANSFER cycle. ($\overline{ME}$)/$\overline{WE}$ and DSF2 are LOW and TRM is HIGH when $\overline{RAS}$ falls, to select a write transfer from the BMR. The DQ inputs are used to input a DQ bit-plane mask when $\overline{RAS}$ falls. This allows each of the four DQ planes to be write enabled or disabled during the BMR-WT. The MKD input is used to enable or disable the SMI mode. STS must be LOW at $\overline{RAS}$ time to transfer non-inverted BMR data to the DRAM row selected.

BMR INVERTED WRITE TRANSFER (BMR-IWT)

As with the BMR INVERTED READ TRANSFER, the 2048 bits involved in the transfer may be inverted while being transferred. Taking STS HIGH at $\overline{RAS}$ time will cause the BMR data to be inverted before it is stored in the selected DRAM row. The other control and DQ (mask) inputs are the same as the BMR-WT.

SAM-TO-BMR TRANSFER (SAM-BMR)

The contents of either SAM may be transferred to the BMR in the same manner that a DRAM row is transferred. In this case, DSF1 is HIGH to indicate that the SAM is the source of the data instead of the DRAM. ($\overline{ME}$)/$\overline{WE}$ is used to indicate the direction of the transfer and must be LOW, when $\overline{RAS}$ falls, for a SAM-TO-BMR TRANSFER. STS is no longer used to select between normal and inverted data, it now indicates which SAM is involved in the transfer. Since a SAM-TO-BMR TRANSFER "reads" data from the SAM, the SAM will be placed into input mode by this transfer cycle. The MKD input is still used to determine if the SMI mode will be enabled after the transfer is completed. Since no DRAM access is involved, it is not necessary to provide any particular ROW address at $\overline{RAS}$ time. However, whichever ROW address is present at $\overline{RAS}$ time will be used as the address for a $\overline{RAS}$-ONLY REFRESH. Since a SAM is involved in the transfer, a new SAM starting Address (or Tap) will be loaded at $\overline{CAS}$ time. This address will be loaded into the serial address counter of the SAM selected by STS at $\overline{RAS}$ time.

Note: *Any SAM/BMR TRANSFER will take the device out of the split SAM mode, if it was in that mode before the transfer.*

BMR-TO-SAM TRANSFER (BMR-SAM)

The contents of the BMR may also be transferred to one of the SAM registers. The ($\overline{ME}$)/$\overline{WE}$ input is used to indicate the direction of the transfer and must be HIGH for a BMR-TO-SAM TRANSFER. STS is LOW to select SAMa or HIGH to select SAMb as the destination for the BMR data. The remaining inputs and functionality are identical to the SAM-TO-BMR TRANSFER. Since a BMR-TO-SAM TRANSFER writes new data to the selected SAM register, the I/O for the SAM involved will be placed in the output mode and a new Tap address will be loaded when $\overline{CAS}$ falls.

CLEAR BIT MASK REGISTER (CLR-BMR)

The entire contents of the BMR can be cleared (set all bit LOW) within a single transfer cycle by performing a CLEAR BMR cycle. Unlike the other cycles that access the BMR, TRM is LOW at $\overline{RAS}$ time for the CLEAR BIT MASK REGISTER function. $\overline{TR}$/($\overline{OE}$) is LOW to indicate that the cycle is a transfer cycle (although there is really no data transfer involved). The CLR-BMR function is selected when $\overline{ME}$/($\overline{WE}$), DSF1 and DSF2 are HIGH when RAS falls.

When the BMR is cleared, all data will be masked when a BIT MASKED TRANSFER cycle is performed.

The BMR INVERTED WRITE and BMR WRITE TRANSFERS can be used with the CLR-BMR function to set or clear, respectively, any DRAM row. The CLR-BMR function is used to clear the BMR then the BMR TRANSFERS are performed to the addressed DRAM row.

The CLEAR BIT MASK REGISTER function is useful when using the SERIAL MASK INPUT mode. It is automatically performed (when in the SMI mode) when data is transferred from SAMb to the DRAM (see SERIAL MASK INPUT section).

SERIAL MASK INPUT (SMI)

Whenever the BMR is accessed, the MKD input is sensed and latched into the BMR control logic. If the MKD pin is LOW at $\overline{RAS}$ time the Serial Mask Input (SMI) mode is disabled and the BMR may only be loaded via internal transfer cycles. If MKD is HIGH when $\overline{RAS}$ falls, during a BMR access, then the BMR control logic enables the SMI mode and the BMR may be serially loaded via the MKD input.

When SMI is enabled, the MKD input is coupled to all eight of the bit mask register's DQ planes (see Figure 10). The SCb clock input and SAMb's address counter are used to input data to SAMb and the BMR. SEb will enable (LOW) or disable (HIGH) input data to SAMb and the BMR, the address count will increment regardless of the state of SEb.

The most common application of the SMI mode is to automatically load a transfer mask with the new data written to SAMb. To initialize the sequence, the BMR is cleared (CLR-BMR) with MKD=HIGH at $\overline{RAS}$ time to enable the SMI mode. Then SAMb is prepared to accept input data by performing PSEUDO WRITE TRANSFER. The SAM starting address loaded will also apply to the BMR. For every address location that to which data is written in SAMb, the corresponding address location in the BMR will be written to the value present on MKD (all eight planes of the BMR will be written). After the input of data to SAMb

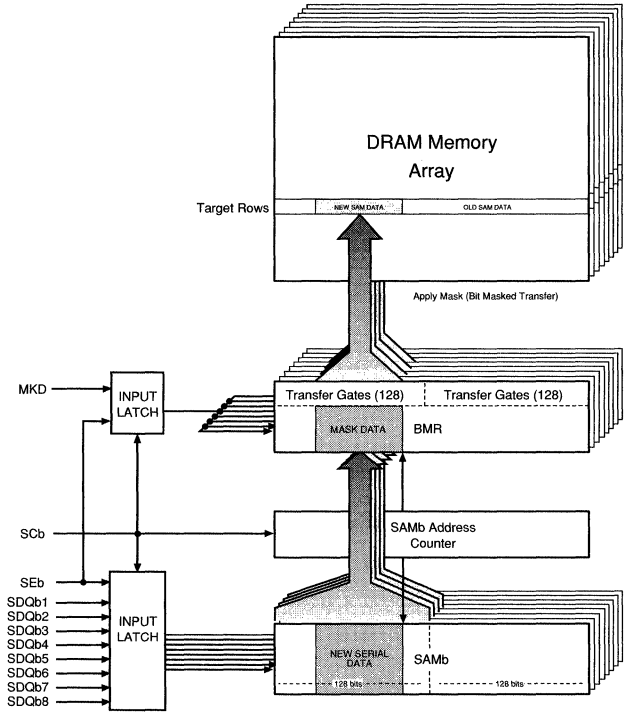


Figure 10
SERIAL-MASK-INPUT MODE BLOCK DIAGRAM

is complete, a BIT MASKED WRITE TRANSFER may be done and only the unmasked data from SAMb will be transferred to the DRAM. The BMR will be cleared automatically after a BIT MASKED WRITE TRANSFER from SAMb, if the device is in the SMI mode. A BMSWT from SAMb will clear on half of the BMR. This allows a new mask to be loaded during the next fill of SAMb, without performing a CLR-BMR cycle. If data is to be masked during the BMWT, then MKD is held LOW when the corresponding SAMb data is written. If the data is to be written (unmasked) to the DRAM during the BMWT, then MKD is held HIGH when the corresponding SAMb location is written. The function of the MKD pin is dependent on the I/O direction of SAMb. MKD is an input only, if SMI is enabled and SAMb is in input mode. If SMI is enabled and SAMb is in output mode, the MKD input is a "don't care," no new data may be written to the BMR via MKD. MKD is also "don't care" if the SMI mode is disabled. Note that the mask data loaded via SAMb may also be applied to a SAMa TRANSFER cycle, if the mask hasn't been cleared by a SAMb TRANSFER or a CLR-BMR cycle. The BMR will not be cleared after a TRANSFER involving SAMa.

POWER UP INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 8ms the device must be initialized.

After Vcc is at specified operating conditions, for 100µs (minimum), eight $\overline{RAS}$ cycles must be executed to initalize the dynamic memory array. When the device is initialized the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of $(\overline{TR})/\overline{OE}$. The DRAM array will contain random data.

The SAM portion of the device is completely static and does not require an initialization cycle. Both SAM ports will power up in the serial input mode (WRITE TRANSFERs) and the SAM I/O pins (SDQ's) are in a High-Z state, regardless of the state of $\overline{SE}$ ab. Also, SPLIT TRANSFER and SMI modes are disabled. Both QSF (MT43C8128) outputs are in the High-Z state. Both SAMs as well as bit mask, color, and DRAM mask registers all contain random data after power-up.

TRUTH TABLE [1]

CODE	FUNCTION	RAS FALLING EDGE									CAS FALL	A0 - A8[2]		DQ1 - DQ8[3]		REGISTERS	
		CAS	TR / OE	ME / WE[10]	DSF1	DSF2	SEa, SEb	TRM	MKD	STS	DSF1	RAS	CAS A8=X	RAS	CAS[4]	MASK	COLOR
	DRAM OPERATIONS																
CBR	CAS-BEFORE-RAS REFRESH	0	1[11]	1[11]	X	X	X	X	X	X	X	X	X	X	X	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	X	X	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0[11]	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	X	X
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	0[11]	X	X	X	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	0[11]	X	X	X	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	0[11]	X	X	X	X	1	ROW	COLUMN (A2 - A7)	X	COLUMN MASK	X	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	0[11]	X	X	X	X	1	ROW	COLUMN (A2 - A7)	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	0[11]	X	X	X	X	1	ROW	COLUMN (A2 - A7)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS																
LMR	LOAD MASK REGISTER	1	1	1	1	0[11]	X	X	X	X	0	X[5]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	0[11]	X	X	X	X	1	X[5]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS																
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	X	X
SRT[9]	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	0	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)	1	0	0	0	0	1	0	X	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	X	X
SWT[9]	SPLIT WRITE TRANSFER (SPLIT SAM-TO-DRAM TRANSFER WITH MASK)	1	0	0	1	0	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	LOAD & USE	X
DMWT	DQ MASKED WRITE TRANSFER	1	0	0	0	1	X	0	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	LOAD & USE	X

TRUTH TABLE[1]

CODE	FUNCTION	RAS FALLING EDGE									CAS FALL	A0 - A8[2]		DQ1 - DQ4[3]		REGISTERS	
		CAS	TR / OE	ME / WE[10]	DSF1	DSF2	SEa, SEb	TRM	MKD	STS	DSF1	RAS	CAS A8=X	RAS	CAS[4]	MASK	COLOR
	BIT MASK REGISTER OPERATIONS																
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	0	X	ROW	X	X	X	X	X
BMR-IRT	BMR READ TRANSFER (DRAM→INVERT→BMR TRANSFER)	1	0	1	0	0	X	1	0/1[7]	1	X	ROW	X	X	X	X	X
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	0	X	ROW	X	DQ MASK	X	X	X
BMR-IWT	BMR WRITE TRANSFER (BMR→INVERT→DRAM TRANSFER)	1	0	0	0	0	X	1	0/1[7]	1	X	ROW	X	DQ MASK	X	X	X
SAM-BMR	SAM→BMR TRANSFER	1	0	0	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	X	X
BMR-SAM	BMR→SAM TRANSFER	1	0	1	1	0	X	1	0/1[7]	0=SAMa 1=SAMb	X	X[5]	TAP[6]	X	X	X	X
CLR-BMR	CLEAR BIT MASK REGISTER (SETS BMR TO ALL "0's")	1	0	1	1	1	X	0	0/1[7]	X	X	X[5]	X	X	X	X	X
	BIT MASKED TRANSFER OPERATIONS																
BMRT	BIT MASKED READ TRANSFER (BM DRAM→SAM TRANSFER)	1	0	1	0	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	X	X
BMSRT[9]	BIT MASKED SPLIT READ TRANSFER (BM SPLIT DRAM→SAM TRANSFER)	1	0	1	1	1	X	1	X	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	X	X
BMWT	BIT MASKED WRITE TRANSFER (BM SAM→DRAM TRANSFER)	1	0	0	0	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	X	X	X	X
BMSWT[9]	BIT MASKED SPLIT WRITE TRANSFER (BM SPLIT SAM→DRAM TRANSFER)	1	0	0	1	1	X	1	X[8]	0=SAMa 1=SAMb	X	ROW	TAP[6]	DQ MASK	X	LOAD & USE	X

NOTES:
1. 0 = LOW (V_{IL}), 1 = HIGH (V_{IH}), X = "don't care", - = "not applicable"
2. These columns show what must be present on the A0-A8 inputs when RAS falls and A0-A7 when CAS falls.
3. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
4. On WRITE cycles (except BLOCK WRITE), the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is enabled on the falling edge of CAS or TR/OE, whichever is later.
5. The ROW that is addressed will be refreshed, but no particular ROW address is required.
6. Tap Address; this is the SAM location that the first SC cycle will access. For SPLIT TRANSFERs the half receiving the transfer is determined by the MSB of the internal address counter. The SAM half not currently being accessed will be the half receiving the transfer. Column address A7 is a "don't care" for SPLIT TRANSFERS.
7. The Serial Mask Input mode (SMI) is enabled ("1") or disabled ("0") when the BMR is accessed (see BMR OPERATIONS). If SMI is enabled (MKD = "1"), mask data is serially clocked into the BMR with SCb and the BMR is automatically cleared after a BIT MASKED WRITE or BIT MASKED SPLIT WRITE TRANSFER cycle from SAMb. For BIT MASKED READ TRANSFERs to any SAM and BIT MASKED WRITE TRANSFERs from SAMa, the BMR is not cleared automatically.
8. If the SMI mode is enabled, mask data is clocked into the BMR with SCb. A HIGH will allow data from the SAM address location to be written to the DRAM, a LOW will mask data to the DRAM during a BIT MASKED WRITE or BIT MASKED SPLIT WRITE TRANSFER.
9. SPLIT TRANSFERs do not change SAM I/O direction.
10. SAM I/O direction is a function of the state of ME/WE at RAS time. If ME/WE is LOW, then the selected SAM is an input; if ME/WE is HIGH then the SAM is an output.
11. The MT43C8128/9 operates properly if this state is "X", but to allow for future functional enhancements it is recommended that they are driven as shown in the Truth Table.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Operating Temperature, Ta(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$, all other pins not under test = 0V).	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled, $0V \le V_{OUT} \le V_{CC}$).	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	1

CAPACITANCE

(T_A = 25°C; V_{CC} = 5.0V; f = 1MHz)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8, TRM, MKD	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, SCa,b, $\overline{SE}$a,b, DSF1,2, STS SSFa,b	C_{I2}		7	pF	2
Input/Output Capacitance: DQ, SDQa,b	$C_{I/O}$		9	pF	2
Output Capacitance: QSFa,b	C_O		9	pF	2

CURRENT DRAIN, SAMa and SAMb IN STANDBY

(0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC1}	100	90	80	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL} $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC2}	90	80	70	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH}, after 8 $\overline{RAS}$ cycles min)	I_{CC3}	7	7	7	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=Vcc-0.2V, after 8 $\overline{RAS}$ cycles min). All other inputs at Vcc-0.2V or Vss+0.2V	I_{CC4}	1	1	1	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH})	I_{CC5}	100	90	80	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling)	I_{CC6}	90	80	70	mA	3,5
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	I_{CC7}	110	100	90	mA	3

CURRENT DRAIN, SAMa and SAMb ACTIVE

(Notes 3, 4) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC8}	180	170	160	mA	
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL} $\overline{CAS}$ = Cycling; ^tPC = ^tPC (MIN))	I_{CC9}	160	150	140	mA	
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH}, after 8 $\overline{RAS}$ cycles min)	I_{CC10}	85	85	85	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=Vcc-0.2V, after 8 $\overline{RAS}$ cycles min). All other inputs at Vcc-0.2V or Vss+0.2V	I_{CC11}	75	75	75	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH})	I_{CC12}	180	170	160	mA	
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling)	I_{CC13}	170	160	150	mA	5
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	I_{CC14}	180	170	160	mA	

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		180		210		ns	
READ-MODIFY-WRITE cycle time	^tRWC	205		235		280		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		55		65		ns	
FAST-PAGE-MODE READ-MODIFY-WRITE cycle time	^tPRWC	100		110		140		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14, 17
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Access time from ($\overline{TR}$)/OE	^tOE		20		25		30	ns	
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		80		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	20	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	12		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	25	60	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	30	ns	20
Output Disable	^tOD	0	20	0	20	0	30	ns	
Output Disable hold time from start of write	^tOEH		15		15		20	ns	
Output Enable to $\overline{RAS}$ delay	^tORD		0		0		0	ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		85		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		25		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		130		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		80		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		60		70		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ setup time	^tWSR	0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	12		15		15		ns	
Mask data to $\overline{RAS}$ setup time	^tMS	0		0		0		ns	
Mask data to $\overline{RAS}$ hold time	^tMH	12		15		15		ns	

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER command to $\overline{RAS}$ setup time	^tTLS	0		0		0		ns	25
TRANSFER command to $\overline{RAS}$ hold time	^tTLH	12	10,000	15	10,000	15	10,000	ns	25
TRANSFER command to $\overline{RAS}$ hold time (REAL-TIME READ TRANSFER only)	^tRTH	70	10,000	80	10,000	90	10,000	ns	25
TRANSFER command to $\overline{CAS}$ hold time (REAL-TIME READ TRANSFER only)	^tCTH	20		25		30		ns	25
TRANSFER command to column address hold time (For REAL-TIME READ TRANSFER only)	^tATH	25		30		35		ns	25
TRANSFER command to SC lead time	^tTSL	5		5		5		ns	25
TRANSFER command to $\overline{RAS}$ HIGH lead time	^tTRL	0		0		0		ns	25
TRANSFER command to $\overline{RAS}$ delay time	^tTRD	15		15		15		ns	25
TRANSFER command to $\overline{CAS}$ HIGH lead time	^tTCL	0		0		0		ns	25
TRANSFER command to $\overline{CAS}$ delay time	^tTCD	15		15		15		ns	25
First SC edge to TRANSFER command delay time	^tTSD	10		10		10		ns	25
$\overline{RAS}$ to first SC edge delay time	^tRSD	80		95		105		ns	
$\overline{CAS}$ to first SC edge delay time	^tCSD	25		30		35		ns	
Column address to first SC edge delay time	^tASD	50		60		65		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	^tSDZ	10	35	10	40	10	45	ns	
SC to $\overline{RAS}$ setup time	^tSRS	30		30		40		ns	
$\overline{RAS}$ to SC delay time	^tSRD	20		25		30		ns	
Serial data input to $\overline{SE}$ delay time	^tSZE	0		0		0		ns	
$\overline{RAS}$ to SD buffer turn-on time	^tSRO	10		15		15		ns	
Serial data input delay from $\overline{RAS}$	^tSDD	45		50		55		ns	
Serial data input to $\overline{RAS}$ delay time	^tSZS	0		0		0		ns	
Serial Input Mode enable ($\overline{SE}$) to $\overline{RAS}$ setup time	^tESR	0		0		0		ns	
Serial Input Mode enable ($\overline{SE}$) to $\overline{RAS}$ hold time	^tREH	12		15		15		ns	
NONTRANSFER command to $\overline{RAS}$ setup time	^tYS	0		0		0		ns	26
NONTRANSFER command to RAS hold time	^tYH	12		15		15		ns	26
DSF, TRM, STS, MKD to $\overline{RAS}$ setup time	^tFSR	0		0		0		ns	
DSF, TRM, STS, MKD to $\overline{RAS}$ hold time	^tRFH	12		15		15		ns	
DSF to $\overline{RAS}$ hold time	^tFHR	60		65		70		ns	
DSF to $\overline{CAS}$ setup time	^tFSC	0		0		0		ns	
DSF to $\overline{CAS}$ hold time	^tCFH	15		20		20		ns	
SC to QSF delay time	^tSQD		35		40		45	ns	
$\overline{RAS}$ to QSF delay time	^tRQD		65		85		105	ns	
$\overline{CAS}$ to QSF delay time	^tCQD		35		40		45	ns	
$\overline{TR/OE}$ to QSF delay time	^tTQD		25		30		35	ns	
SPLIT TRANSFER setup time	^tSTS	30		35		40		ns	
SPLIT TRANSFER hold time	^tSTH	30		35		40		ns	
Split SAM setup time to $\overline{RAS}$ from last SC	^tSCR	30		35		40		ns	29
Split SAM hold time to $\overline{RAS}$ from first SC	^tRSC	30		35		40		ns	29

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

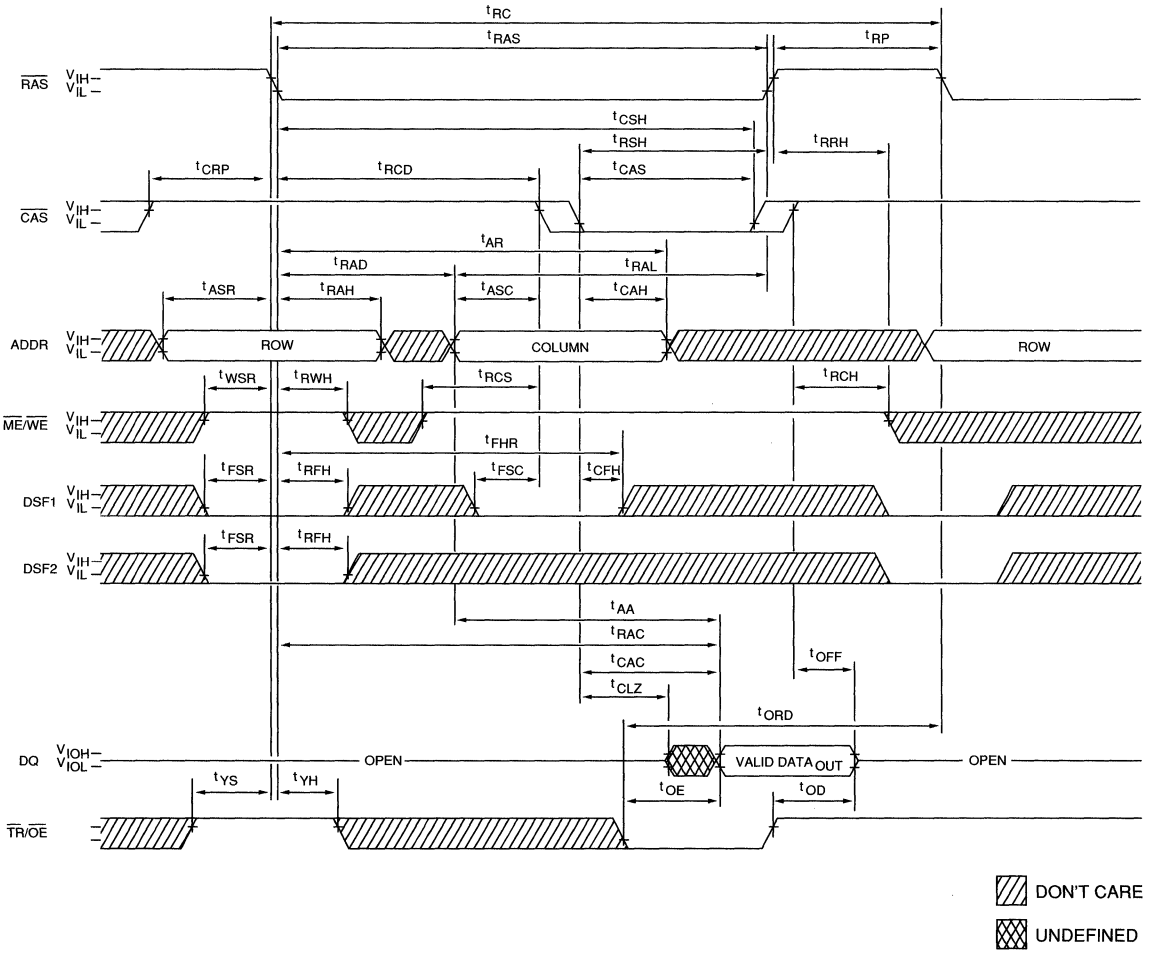
(Notes 6, 7, 8, 9, 10) (0° C ≤ T_A ≤ + 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial clock cycle time	^tSC	25		30		35		ns	
Access time from SC	^tSAC		25		30		35	ns	24
SC precharge time (SC LOW time)	^tSP	10		10		12		ns	
SC pulse width (SC HIGH time)	^tSAS	5		10		12		ns	
Access time from $\overline{SE}$	^tSEA		15		20		30	ns	24
$\overline{SE}$ precharge time	^tSEP	10		15		15		ns	
$\overline{SE}$ pulse width	^tSE	10		15		15		ns	
Serial data out hold time after SC HIGH	^tSOH	5		5		5		ns	24
Serial output buffer turn-off delay from $\overline{SE}$	^tSEZ	0	12	0	15	0	25	ns	24
Serial data in setup time	^tSDS	0		0		0		ns	24
Serial data in hold time	^tSDH	10		15		20		ns	24
SERIAL INPUT (Write) Enable setup time	^tSWS	0		0		0		ns	
SERIAL INPUT (Write) Enable hold time	^tSWH	15		15		25		ns	
SERIAL INPUT (Write) Disable setup time	^tSWIS	0		0		0		ns	
SERIAL INPUT (Write) Disable hold time	^tSWIH	15		15		25		ns	
SSF to SC setup time	^tSFS	0		0		0		ns	29
SSF to SC hold time	^tSFH	15		20		20		ns	29
SSF LOW to SC HIGH delay	^tSFD	0		0		0		ns	29

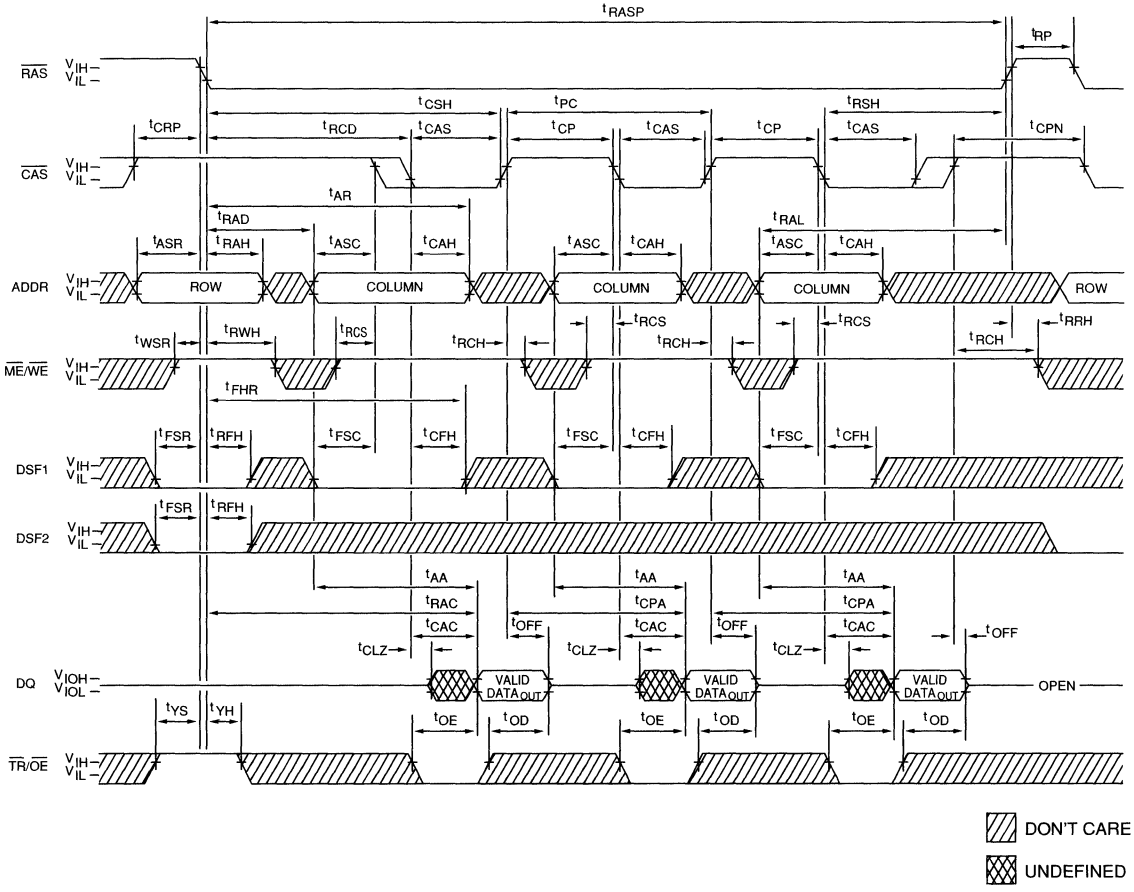
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} MIN and V_{IL} MAX are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data outputs (DQ1-DQ8) is high impedance.
12. If $\overline{CAS}$ = V_{IL}, DRAM data outputs (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the speci fied ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If $^tWCS \leq {}^tWCS$ (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of the output buffers (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate but the WRITE will be valid, if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{ME}/\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open. The DQs will go open with $\overline{OE}$ or $\overline{CAS}$, whichever goes HIGH first.
24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: V_{OH} = 2.0V; V_{OL} = 0.8V.
25. TRANSFER command means that $\overline{TR}/\overline{OE}$ is LOW when $\overline{RAS}$ goes LOW.
26. NON-TRANSFER command means that $\overline{TR}/\overline{OE}$ is HIGH when $\overline{RAS}$ goes LOW.
27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. Applies to the MT43C8128 only.
29. Applies to the MT43C8129 only.

DRAM READ CYCLE



DRAM FAST PAGE MODE READ CYCLE

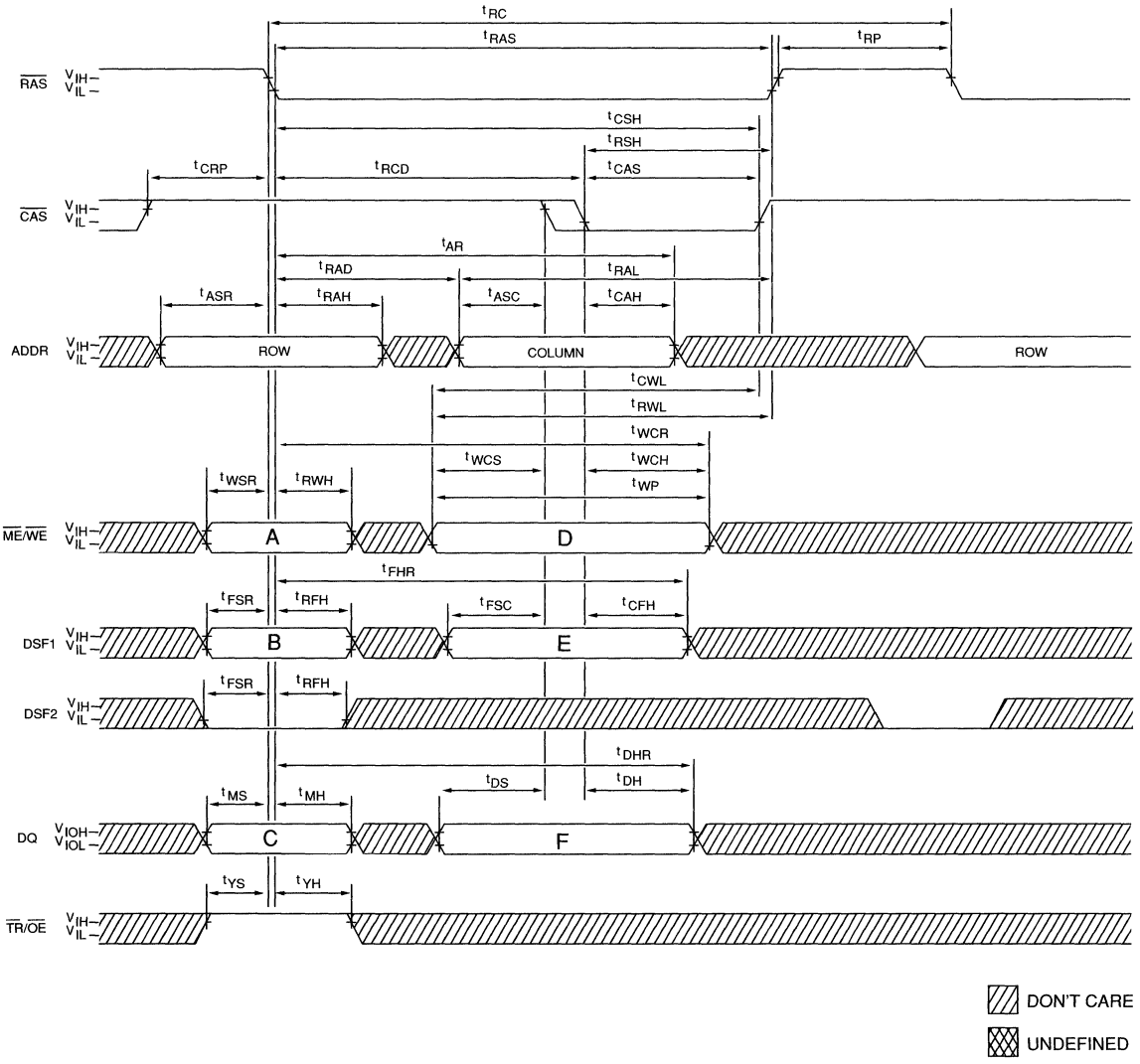


WRITE CYCLE FUNCTION TABLE [1]

LOGIC STATES[2]						FUNCTION	CODE
RAS Falling Edge			CAS Falling Edge				
A ME/WE	B DSF1	C DQ (Input)	D ME/WE	E DSF1	F DQ (Input)		
1	0	X	0/I[5]	0	DRAM	Normal DRAM WRITE	RW
0	0	Write Mask	0/I[5]	0	DRAM (Masked)	NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	RWNM
0	1	X	0/I[5]	0	DRAM (Masked)	PERSISTENT (Use Register) MASKED WRITE to DRAM	RWOM
1	0	X	X[3]	1	Column Mask	BLOCK WRITE to DRAM (No Data Mask)	BW
0	0	Write Mask	X[3]	1	Column Mask	NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	BWNM
0	1	X	X[3]	1	Column Mask	PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	BWOM
1	1	X	X[4]	0	Write Mask	LOAD MASK REGISTER	LMR
1	1	X	X[4]	1	Color Data	LOAD COLOR REGISTER	LCR

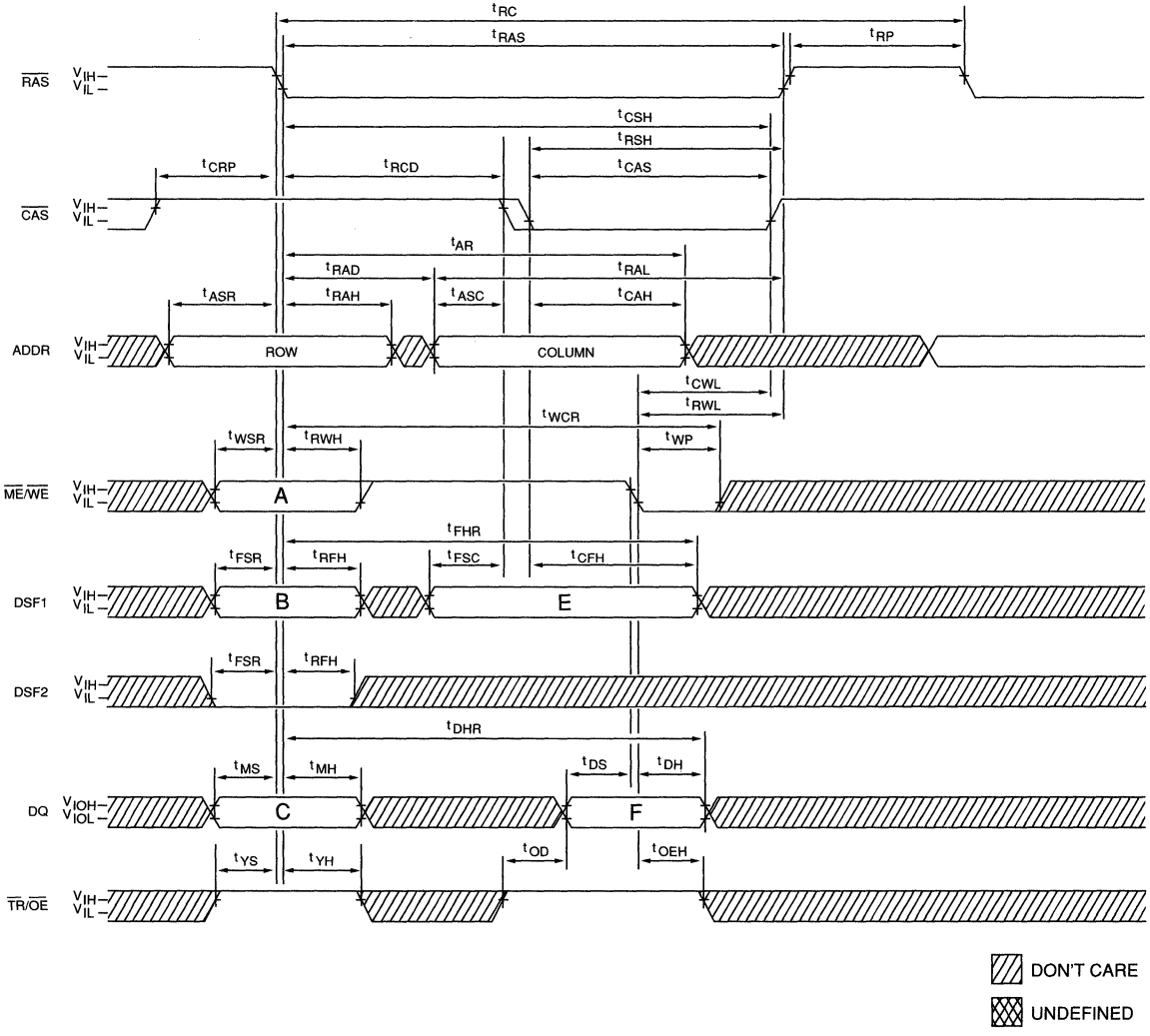
NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" and "F" for the WRITE cycle timing diagrams on the following pages.
2: TRM, MKD and STS are "don't care" for all WRITE cycles.
3. $\overline{WE}$ is a "don't care" for BLOCK WRITE cycles. It occurs on the falling edge of $\overline{CAS}$.
4. Register load cycles can be either EARLY or LATE-WRITE cycles.
5. If $\overline{ME/WE}$ is LOW, an EARLY-WRITE is performed; if it is HIGH, a LATE-WRITE is performed if $\overline{ME/WE}$ falls after $\overline{CAS}$.

DRAM EARLY-WRITE CYCLE



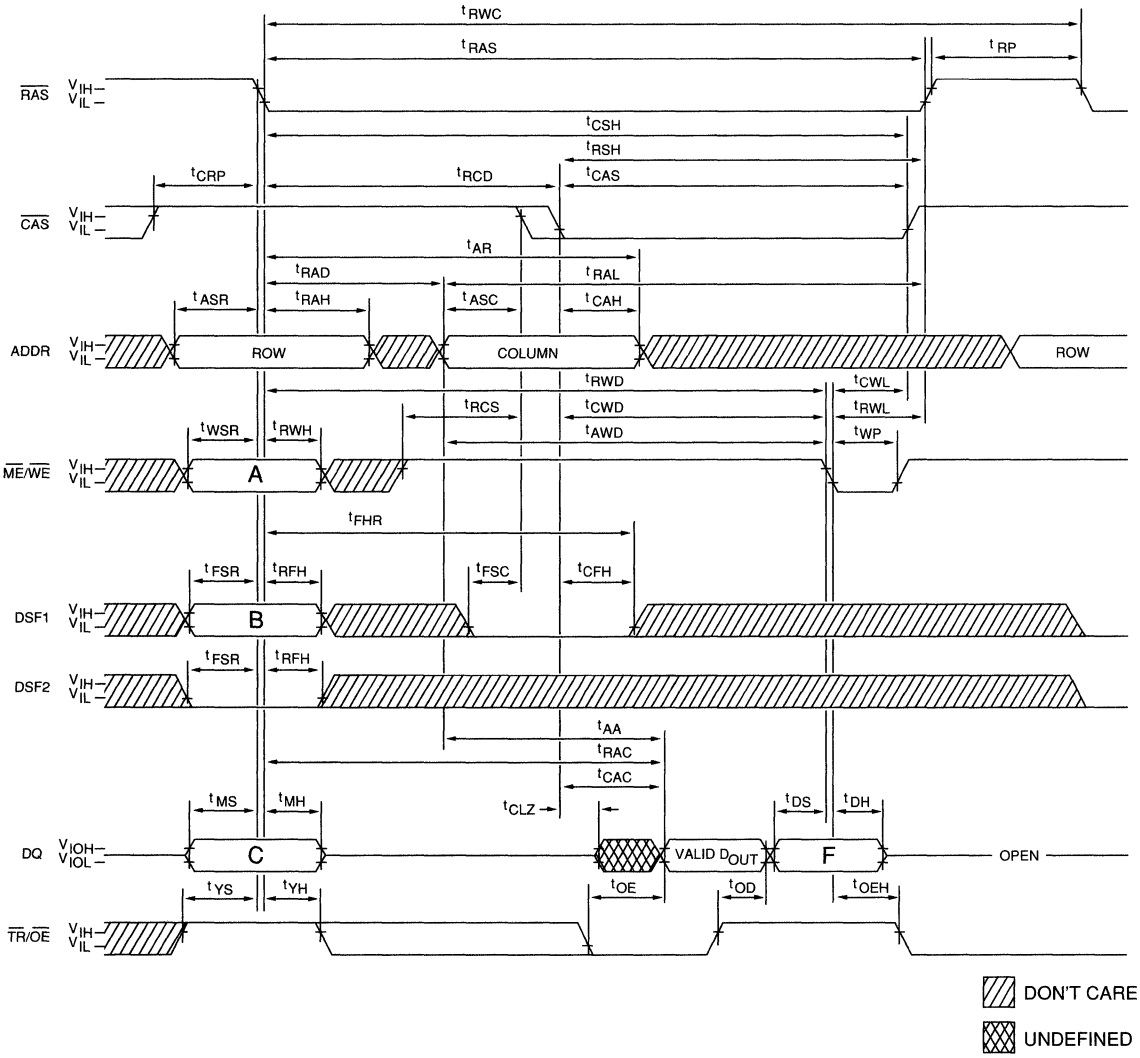
NOTE: The logic states of "A", "B", "C", "D", "E" and "F" determine the type of WRITE operation performed. See the WRITE Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE



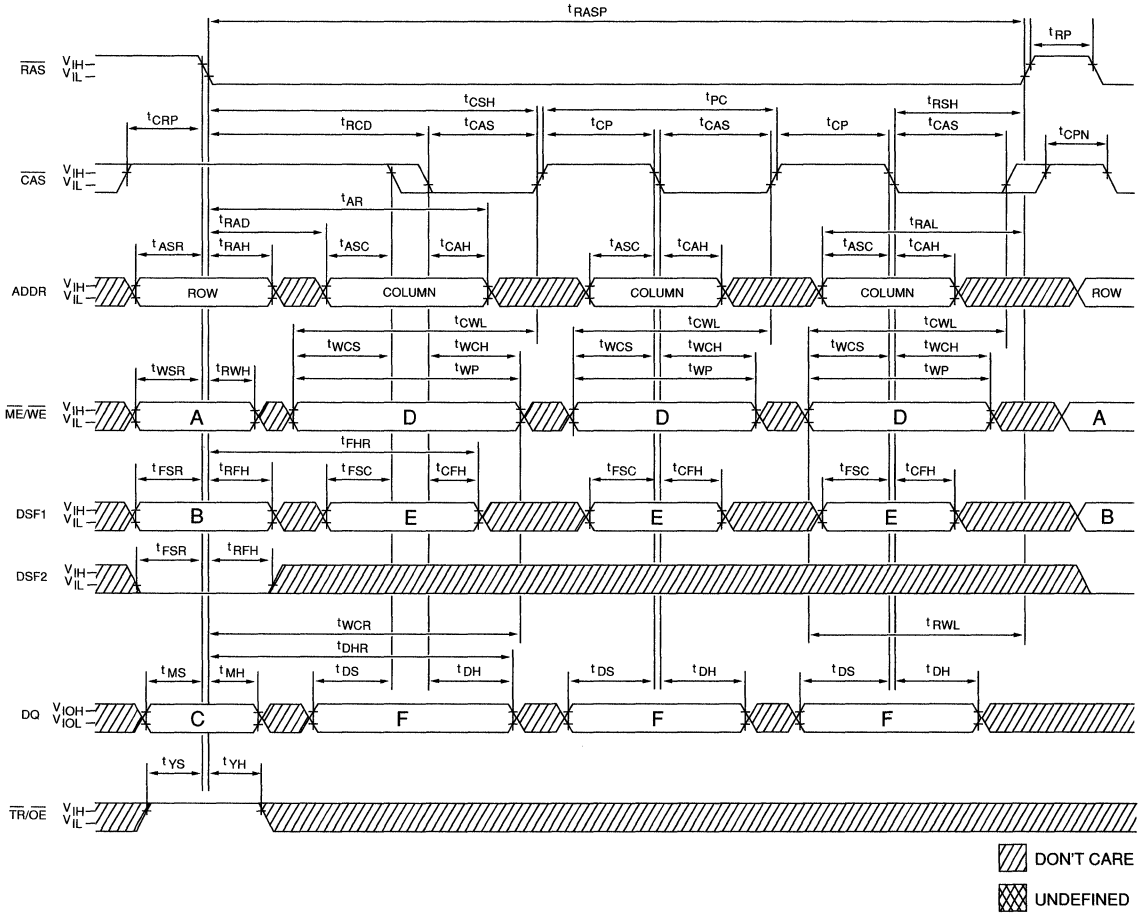
NOTE: 1. The logic states of "A", "B", "C", "E", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
2. LATE-WRITE cycles are not valid for BLOCK WRITEs. ($\overline{ME}$)/$\overline{WE}$ = "don't care" at the falling edge of $\overline{CAS}$.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



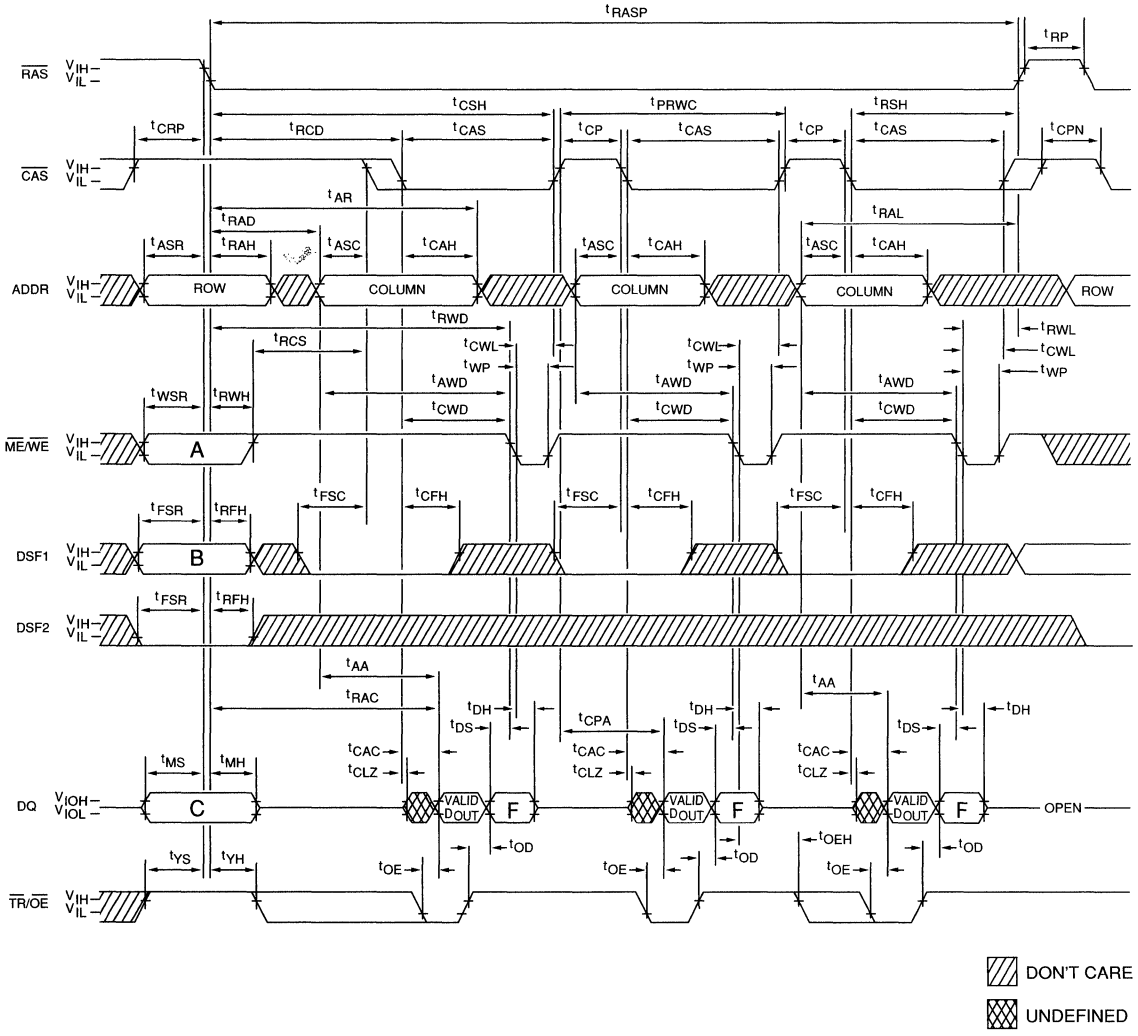
NOTE: The logic states of "A", "B", "C", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE [1,2]



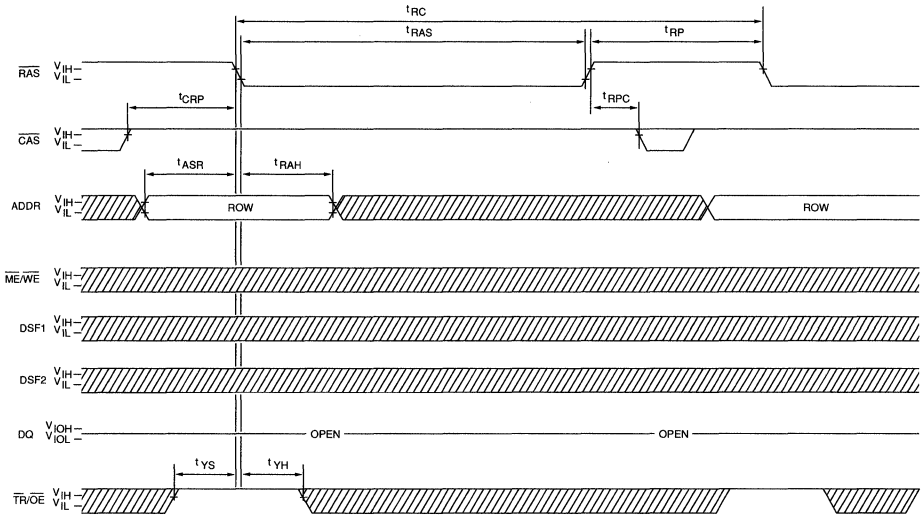
NOTE:
1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
2. The logic states of "A", "B", "C", "D", "E", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE or LATE-WRITE CYCLES)

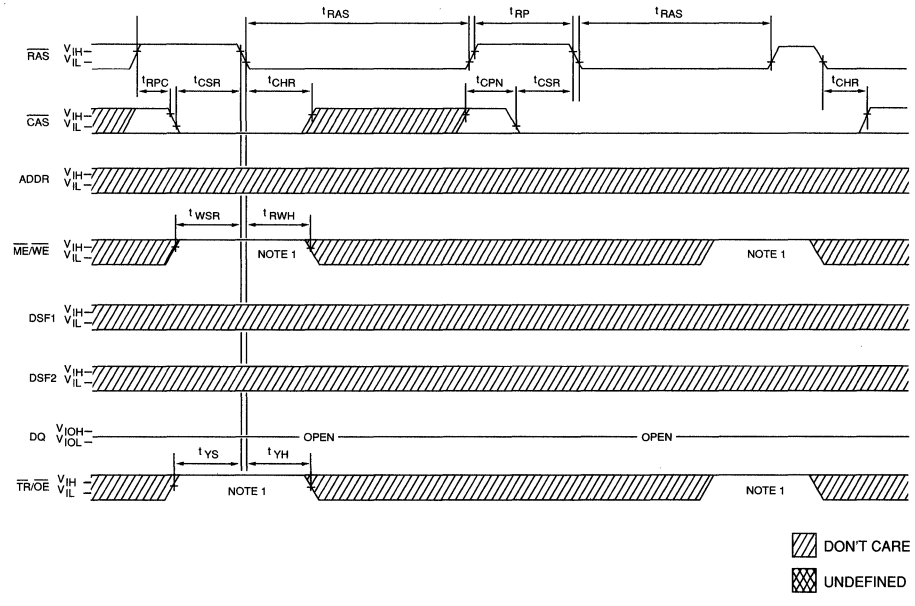


NOTE: 1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF1 state for the desired WRITE operation.
2: The logic states of "A", "B", "C", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8)

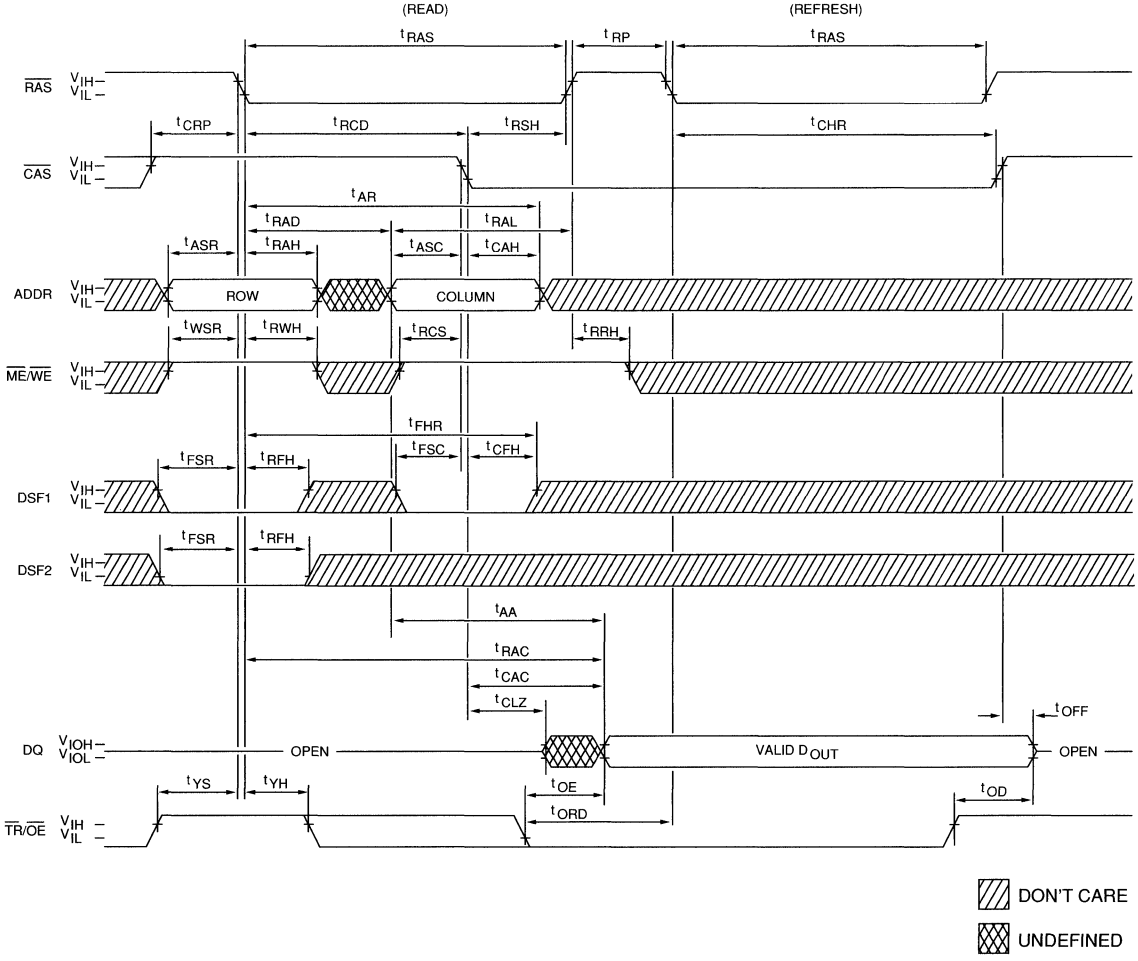


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



NOTE: 1. The MT43C8128/9 operates with this state as "don't care", but to allow for future functional enhancements it is recommended that they be driven as illustrated for system upgradability.

DRAM HIDDEN-REFRESH CYCLE

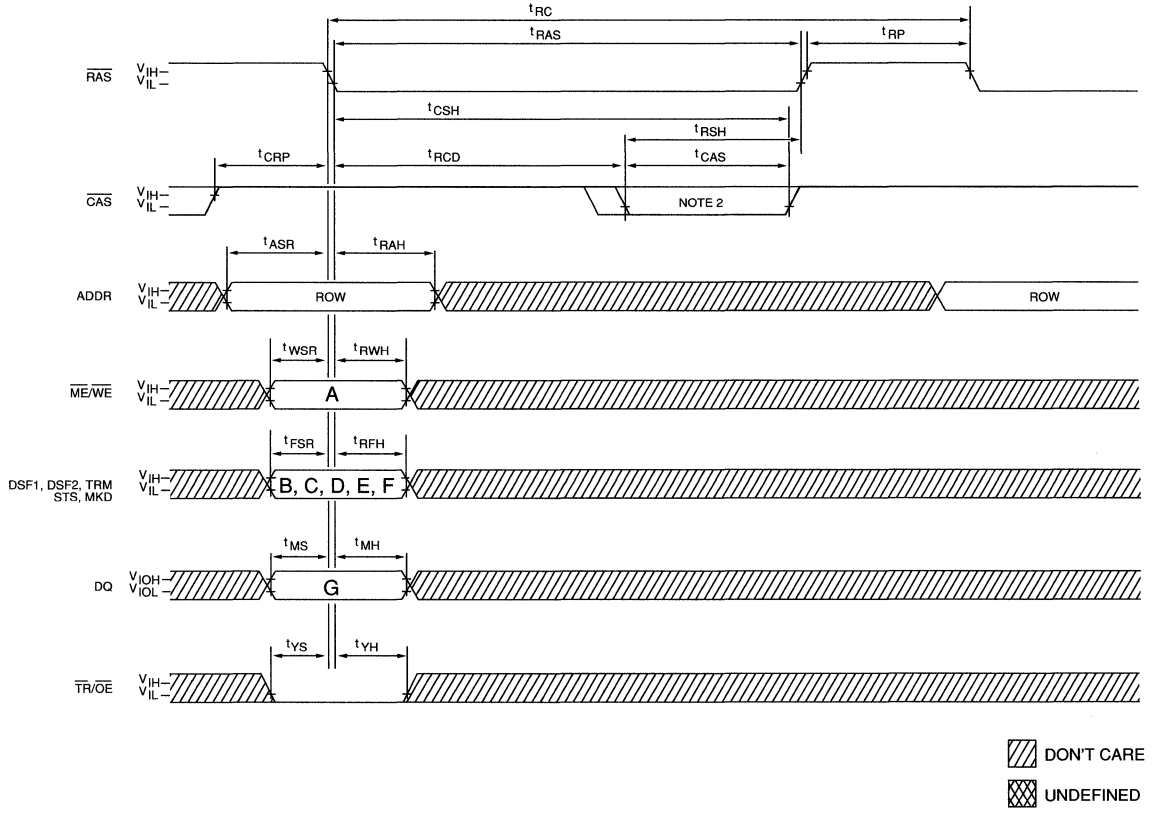


NOTE: A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH. In the TRANSFER case, $\overline{TR}/\overline{OE}$ = LOW (when $\overline{RAS}$ goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of $\overline{TR}/\overline{OE}$.

DRAM/BMR TRANSFER CYCLE FUNCTION TABLE

LOGIC STATES ($\overline{RAS}$ Falling Edge)							FUNCTION	CODE
A $\overline{ME/WE}$	B DSF1	C DSF2	D TRM	E STS	F MKD	G DQ (input)		
1	0	0	1	0	X[1]	X	BMR READ TRANSFER (DRAM→BMR TRANSFER)	BMR-RT
1	0	0	1	1	X[1]	X	BMR $\overline{READ}$ TRANSFER (DRAM→invert→BMR TRANSFER)	BMR-IRT
0	0	0	1	0	X[1]	MASK	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	BMR-WT
0	0	0	1	1	X[1]	MASK	BMR $\overline{WRITE}$ TRANSFER (BMR→invert→DRAM TRANSFER)	BMR-IWT
1	1	1	0	X	X[1]	X	CLEAR BMR (CLR-BMR)	CLR- BMR

DRAM/BMR TRANSFERS



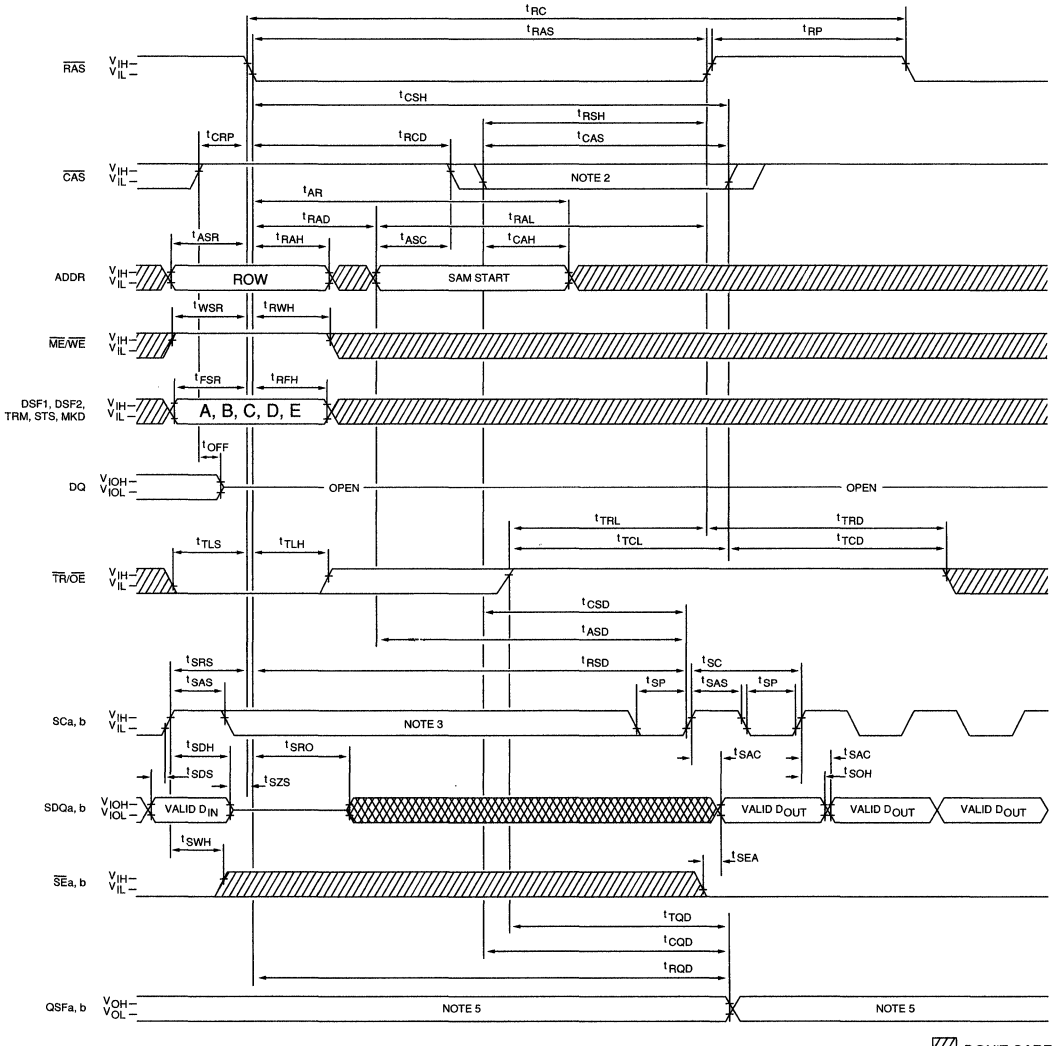
NOTE: 1. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.
2. It is not necessary to drop $\overline{CAS}$ during a DRAM/BMR TRANSFER.

READ TRANSFER CYCLE FUNCTION TABLE[1]

LOGIC STATES[2]					FUNCTION	CODE
$\overline{RAS}$ Falling Edge						
A DSF1	B DSF2	C TRM	D STS	E MKD		
0	0	0	0/1[2]	X	READ TRANSFER (DRAM→SAM)	RW
1	0	0	0/1[2]	X	SPLIT READ TRANSFER (DRAM→SAM)	SRT
0	1	1	0/1[2]	X	BIT MASKED READ TRANSFER	BMRT
1	1	1	0/1[2]	X	BIT MASKED SPLIT READ TRANSFER	BMSRT
1	0	1	0/1[2]	0/1[3]	BMR→SAM TRANSFER	BMR-SAM

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for READ TRANSFER cycle timing diagrams on the following pages.
2. The state of STS at the falling edge of $\overline{RAS}$ determines the SAM involved in the transfer. When STS = LOW the transfer is to SAMa; when STS = HIGH the transfer is to SAMb.
3. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.

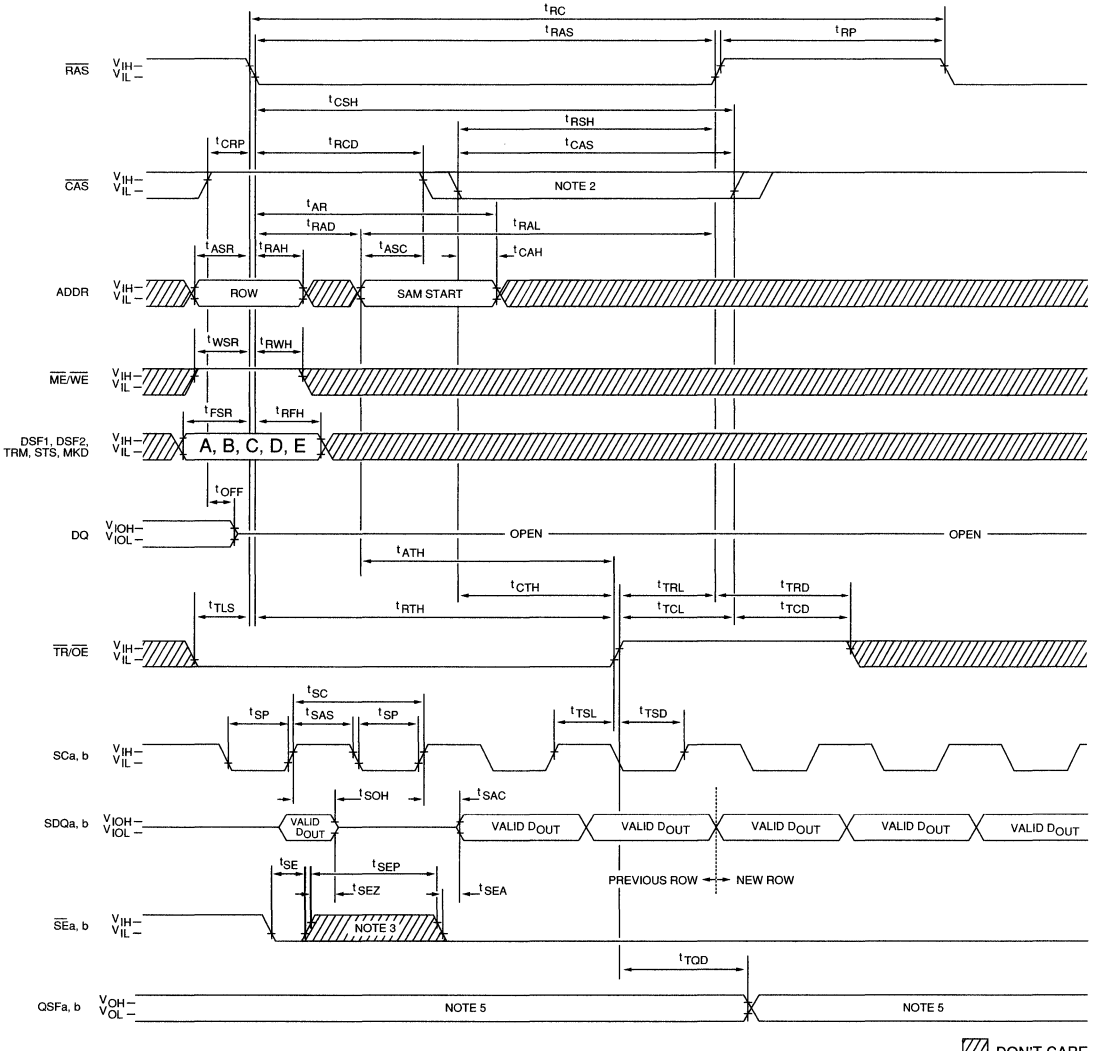
READ TRANSFER[1,4]
(DRAM-TO-SAM TRANSFER)
(When part was previously in the SERIAL INPUT mode)



NOTE:
1. SSF = "Don't Care"
2. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
3. There must be no rising edges on the SC input during this time period.
4. The logic states of "A", "B", "C", and "D" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

REAL-TIME READ TRANSFER[1,4]
(DRAM-TO-SAM TRANSFER)

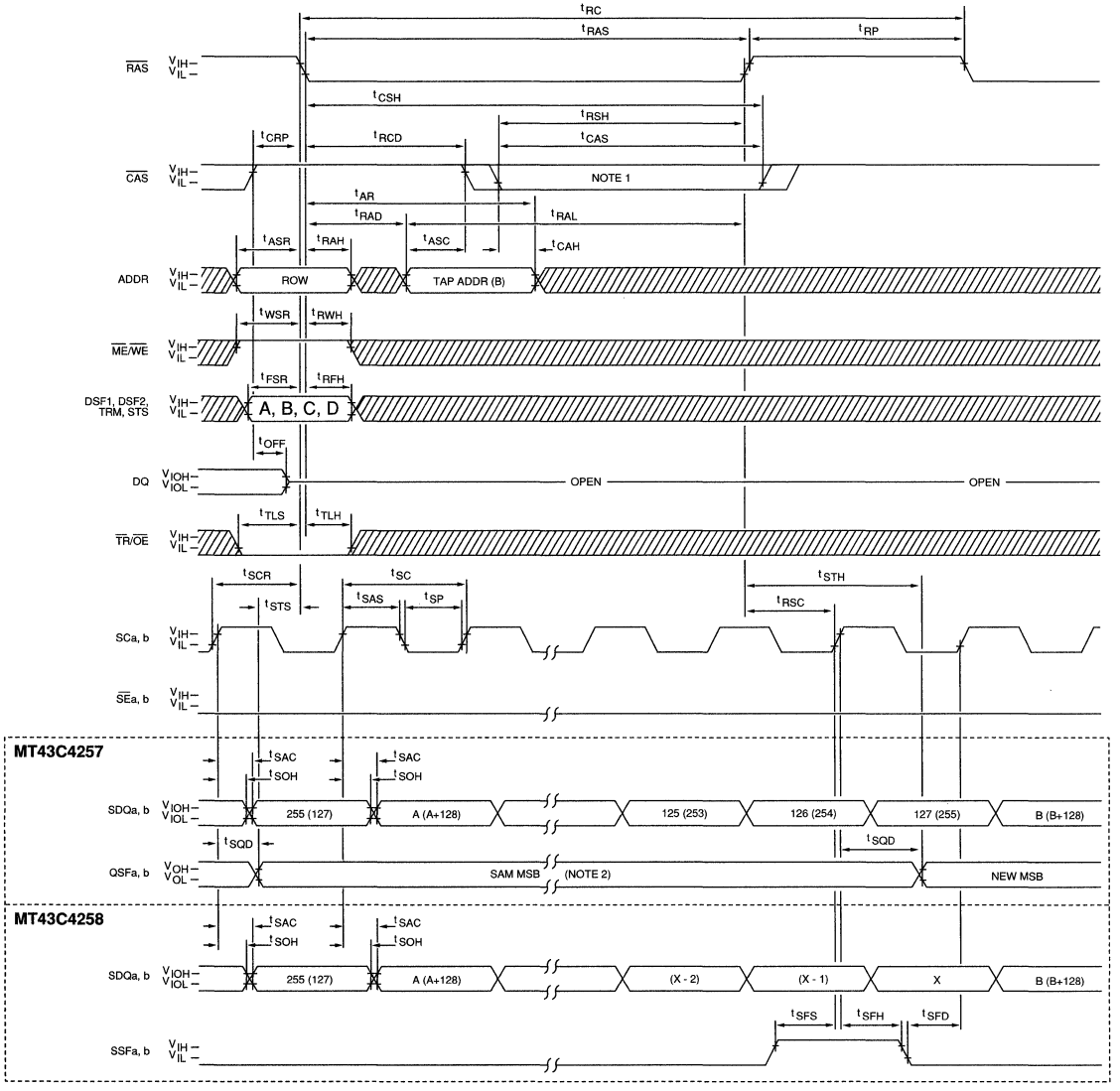
(When part was previously in the SERIAL OUTPUT mode)



NOTE:

1. SSF = "Don't Care"
2. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed
3. The $\overline{SE}$ pulse is shown to illustrate the serial output enable and disable timing. It is not required.
4. The logic states of "A", "B", "C", and "D" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

SPLIT READ TRANSFER[3]
(SPLIT DRAM-TO-SAM TRANSFER)



DON'T CARE

UNDEFINED

NOTE:
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused for the idle half.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.
3. The logic states of "A", "B", "C", and "D" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.

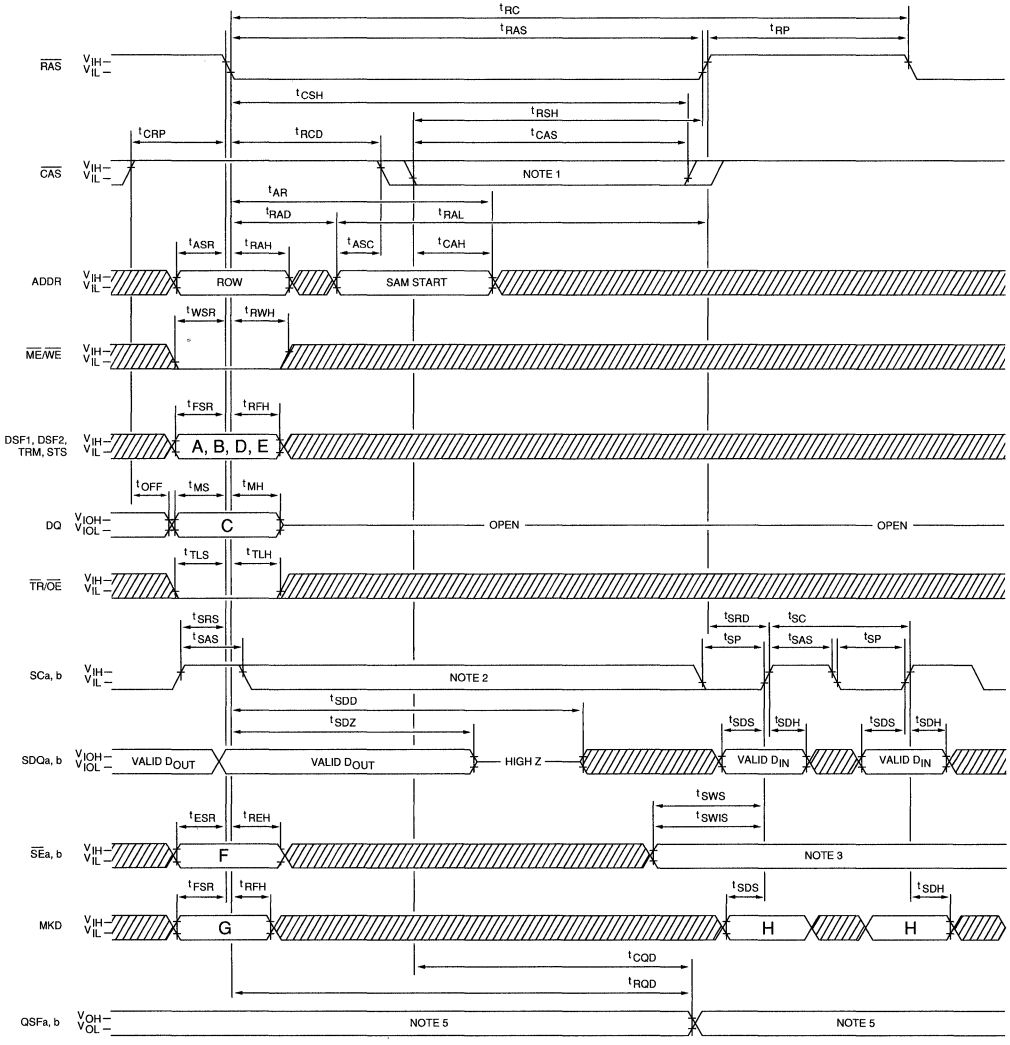
WRITE TRANSFER CYCLE FUNCTION TABLE[1]

LOGIC STATES								FUNCTION	CODE
$\overline{RAS}$ Falling Edge							SC		
A DSF1	B DSF2	C DQ	D TRM	E STS	F $\overline{SE}$	G MKD	H MKD		
0	0	X	0	0/1[2]	0	X	-	WRITE TRANSFER (SAM→DRAM)	WT
0	0	X	0	0/1[2]	1	X	-	PSEUDO WRITE TRANSFER	PWT
1	0	mask	0	0/1[2]	X	X	-	SPLIT WRITE TRANSFER (SAM→DRAM)	SWT
0	1	mask	0	0/1[2]	X	X	-	DQ MASKED WRITE TRANSFER (SAM→DRAM)	DMWT
0	1	X	1	0/1[2]	X	X	0/1[4]	BIT MASKED WRITE TRANSFER (SAM→DRAM)	BMWT
1	1	mask	1	0/1[2]	X	X	0/1[4]	BIT MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	BMSWT
1	0	X	1	0/1[2]	X	0/1[3]	-	SAM→BMR TRANSFER	SAM-BMR

NOTE:
1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E", "F", "G", and "H" for WRITE TRANSFER cycle timing diagrams on the following pages.
2. The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW the transfer is to SAMa; when SAM = HIGH the transfer is to SAMb.
3. Serial Mask Input (SMI) mode is enabled if MKD = HIGH and disabled if MKD = LOW.
4. When in the SMI mode (see BMR transfer waveforms) MKD is the SMI data input. MKD data is clocked into all bit planes of the bit mask register with SCb. A logic "1" on MKD will allow data to pass through all the mask; a logic "0" will mask the corresponding location of the SAM during a BIT MASKED TRANSFER. BIT MASKED TRANSFERs to or from SAMa must not take place while mask data is being serially input via SCb and MKD.

WRITE TRANSFER[4]

(When part was previously in the SERIAL OUTPUT mode)

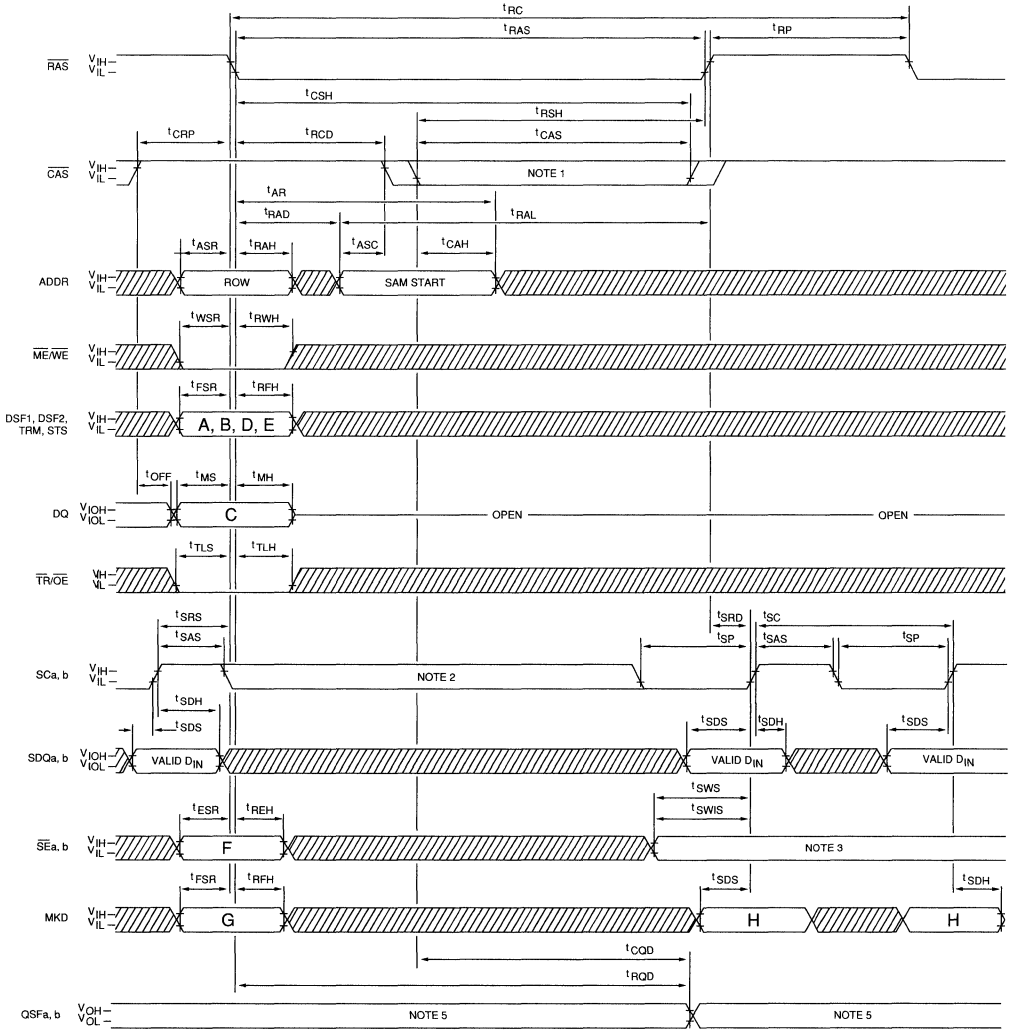


NOTE:

1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. There must be no rising edges on the SC input during this time period.
3. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed. SSFa,b = "don't care" (MT43C8129).

WRITE TRANSFER[4]

(When part was previously in the SERIAL INPUT mode)



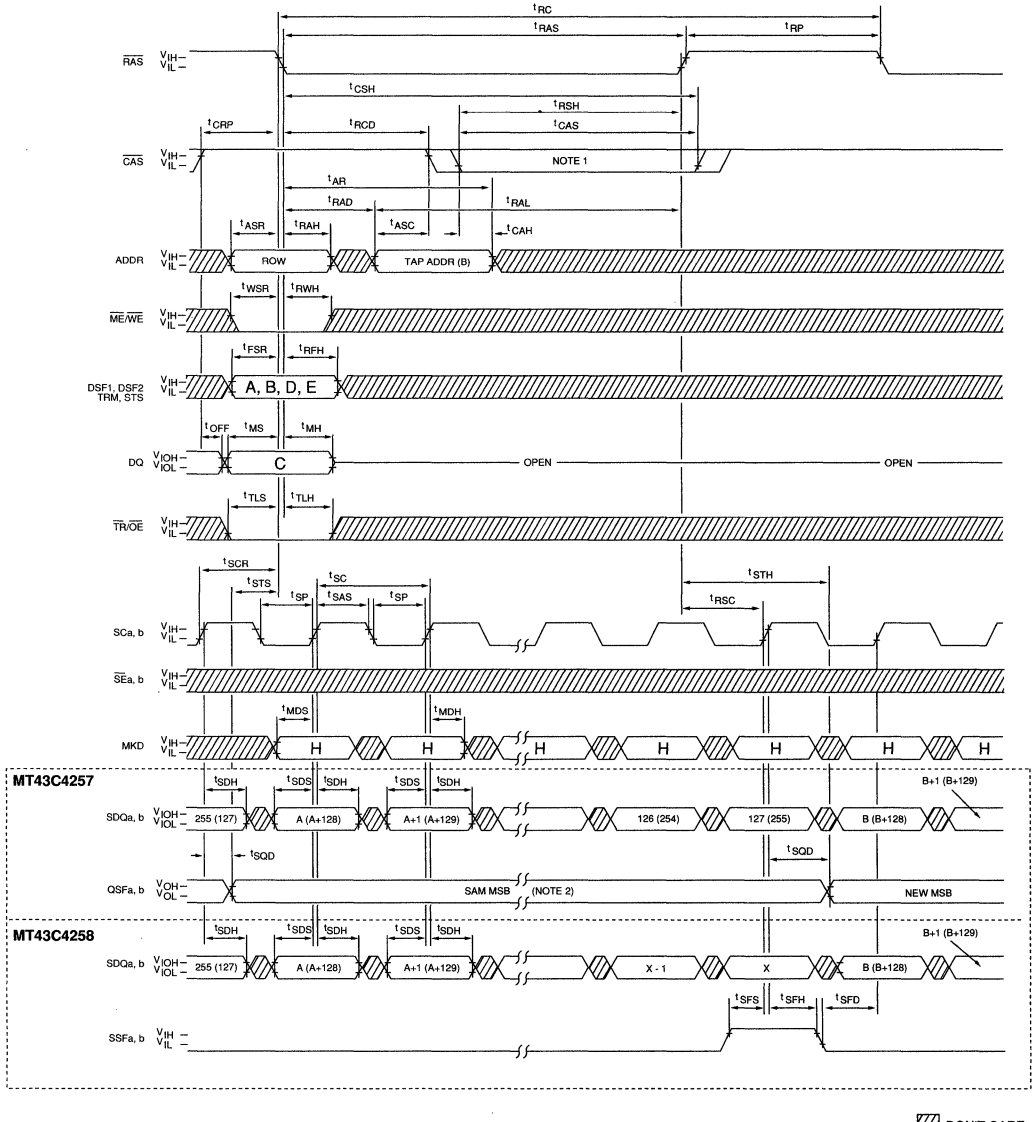
DON'T CARE

UNDEFINED

NOTE:

1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time period.
4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
5. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed. SSFa,b = "don't care" (MT43C8129).

SPLIT WRITE TRANSFER[3]
(SPLIT SAM-TO-DRAM TRANSFER)

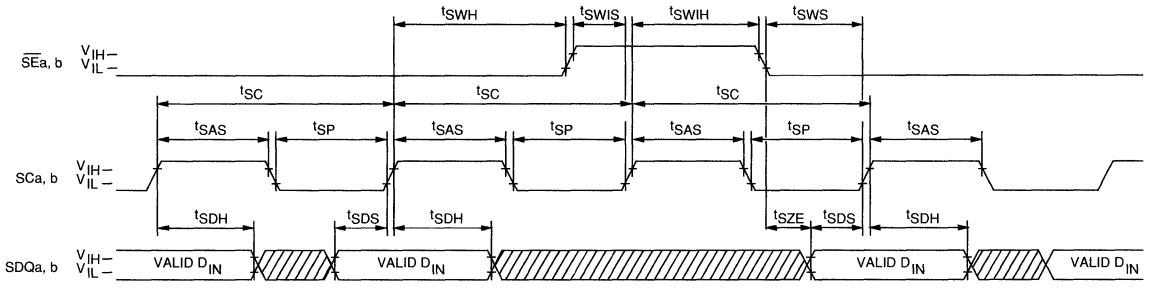


DON'T CARE

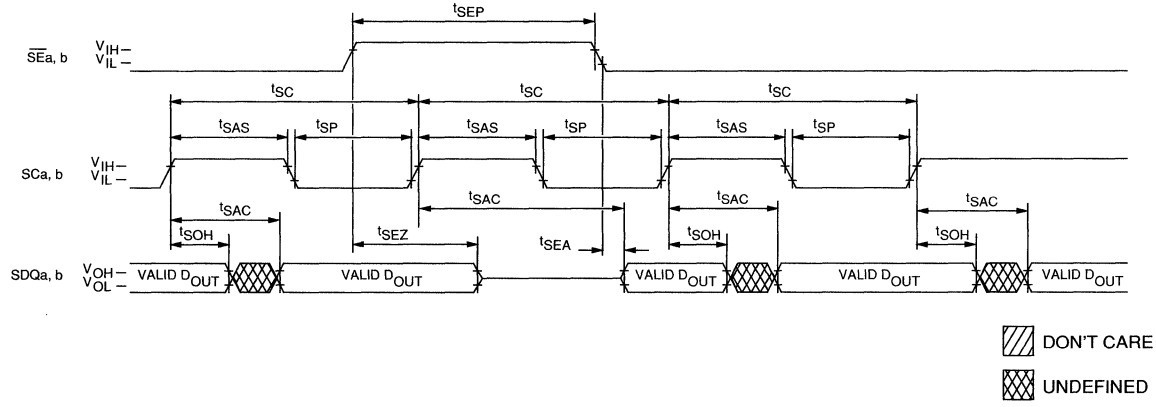
UNDEFINED

NOTE:
1. $\overline{CAS}$ is used to load the Tap address. If $\overline{CAS}$ does not fall, the last Tap address loaded for the addressed SAM will be reused.
2. QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
   QSF = 1 when the Upper SAM (bits 128–255) is being accessed.
3. The logic states of "A", "B", "C", "D", "E", and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.

SAMa or SAMb SERIAL INPUT



SAMa or SAMb SERIAL OUTPUT



NOTE : $\overline{SE}$a, SCa and SDQa are used when accessing SAMa and $\overline{SE}$b; SCb and SDQb are used when access in SAMb.

MICRON TECHNOLOGY, INC.

SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins						Process	Page
				PDIP	SOJ	CDIP	LCC	ZIP	TSOP		
16K x 1	CE only	MT5C1601	12 to 35	20	24	20	20	-	-	CMOS	4-1
64K x 1	CE only	MT5C6401	12 to 35	22	24	22	-	-	-	CMOS	4-9
256K x 1	CE only	MT5C2561	20 to 45	24	24	24	28	-	-	CMOS	4-17
1 Meg x 1	CE only	MT5C1001	25 to 45	28	28	28	32	*	28	CMOS	4-25
4K x 4	CE only	MT5C1604	12 to 35	20	24	20	20	-	-	CMOS	4-33
4K x 4	CE & OE	MT5C1605	12 to 35	22	24	22	-	-	-	CMOS	4-41
4K x 4	Separate I/O	MT5C1606	12 to 35	24	24	24	28	-	-	CMOS	4-49
4K x 4	Separate I/O High-Z	MT5C1607	12 to 35	24	24	24	28	-	-	CMOS	4-49
16K x 4	CE only	MT5C6404	12 to 35	22	24	22	-	-	-	CMOS	4-57
16K x 4	CE & OE	MT5C6405	12 to 35	24	24	24	28	-	-	CMOS	4-65
16K x 4	Separate I/O, CE1, CE2	MT5C6406	12 to 35	28	28	28	28	-	-	CMOS	4-73
16K x 4	Separate I/O High-Z	MT5C6407	12 to 35	28	28	28	28	-	-	CMOS	4-73
64K x 4	CE only	MT5C2564	20 to 45	24	24	24	28	-	-	CMOS	4-81
64K x 4	CE & OE	MT5C2565	20 to 45	28	28	28	28	-	-	CMOS	4-89
256K x 4	CE & OE	MT5C1005	25 to 45	28	28	28	32	*	28	CMOS	4-97
2K x 8	CE & OE	MT5C1608	12 to 35	24	24	24	24	-	-	CMOS	4-105
8K x 8	CE1, CE2 & OE	MT5C6408	12 to 35	28	28	28	32	-	-	CMOS	4-113
32K x 8	CE & OE	MT5C2568	20 to 45	28	28	28	32	28	-	CMOS	4-121
128K x 8	OE, CE1 & CE2	MT5C1008	25 to 45	32	32	32	32	*	32	CMOS	4-129
16K x 16	Latched Address/Data	MT5C2516	15 to 25	-	-	-	-	-	-	CMOS	4-137
16K x 18	Latched Address/Data	MT5C2818	15 to 25	-	-	-	-	-	-	CMOS	4-151

* ZIP introduced in Q191

SRAM

16K x 1 SRAM

FEATURES

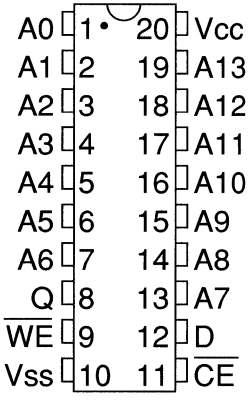
- High speed: 12, 15, 20, 25, 30 and 35ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

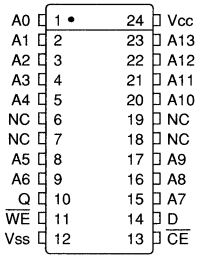
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

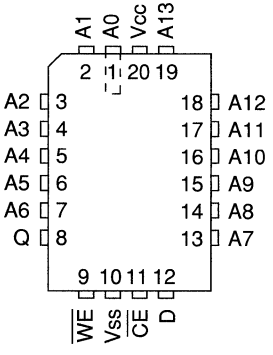
20L/300 DIP
(A-4, B-4)



24L/300 SOJ
(E-4)



20L/LCC
(F-3)



GENERAL DESCRIPTION

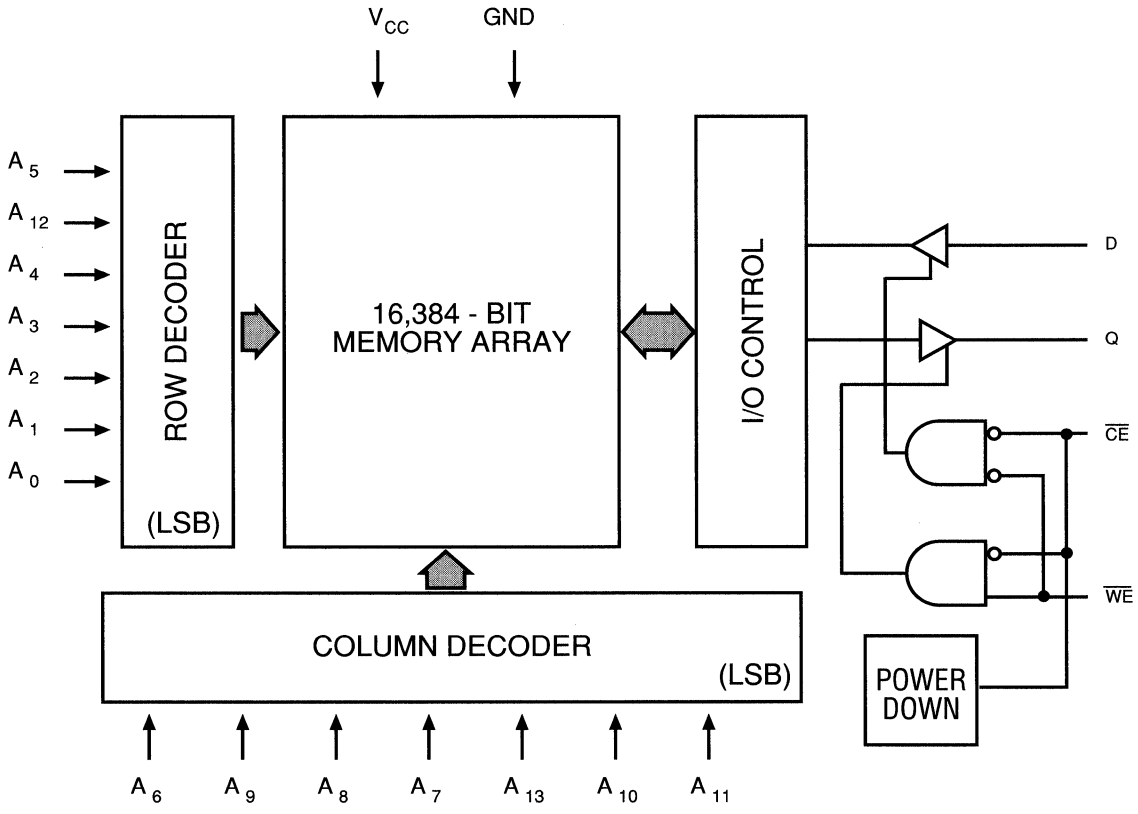
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	140	125	110	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	50	45	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	3	3	3	3	3	3	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip Enable access time	^tACE		11		12		15		20		25		30	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	^tHZCE		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip Disable to power-down time	^tPD		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip Enable to end of write	^tCW	10		12		15		20		25		25		ns	
Address valid to end of write	^tAW	12		12		15		20		25		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data setup time	^tDS	7		8		10		10		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^tHZWE		6		6		8		10		12		15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

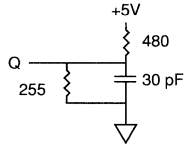


Fig. 1 OUTPUT LOAD EQUIVALENT

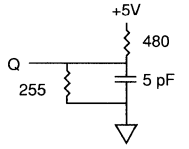


Fig. 2 OUTPUT LOAD EQUIVALENT

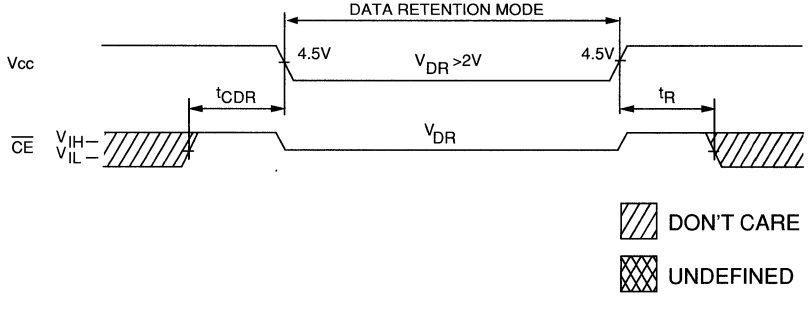
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-165.

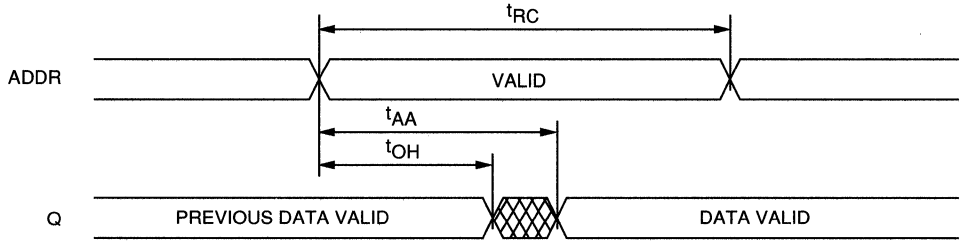
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	I_{CCDR}		95	250	µA	
		Vcc = 3v			300	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

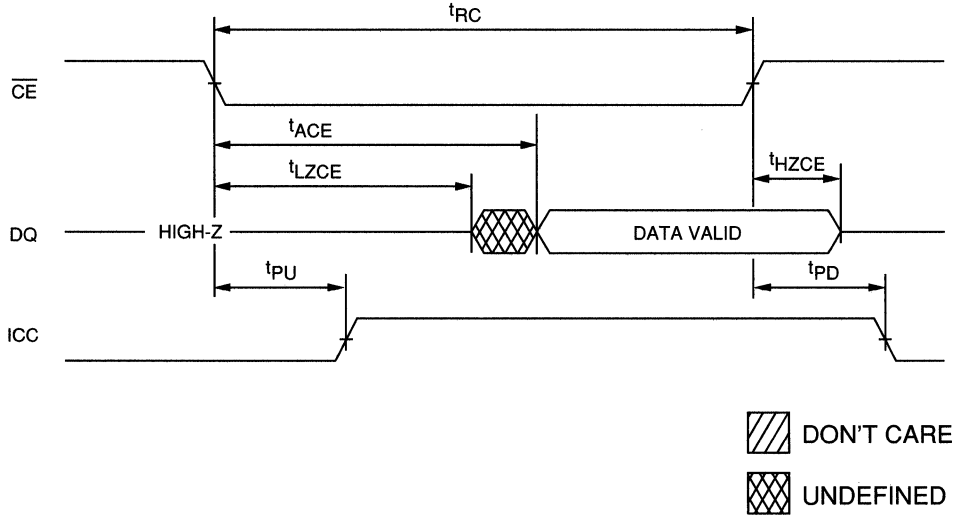
LOW Vcc DATA RETENTION WAVEFORM



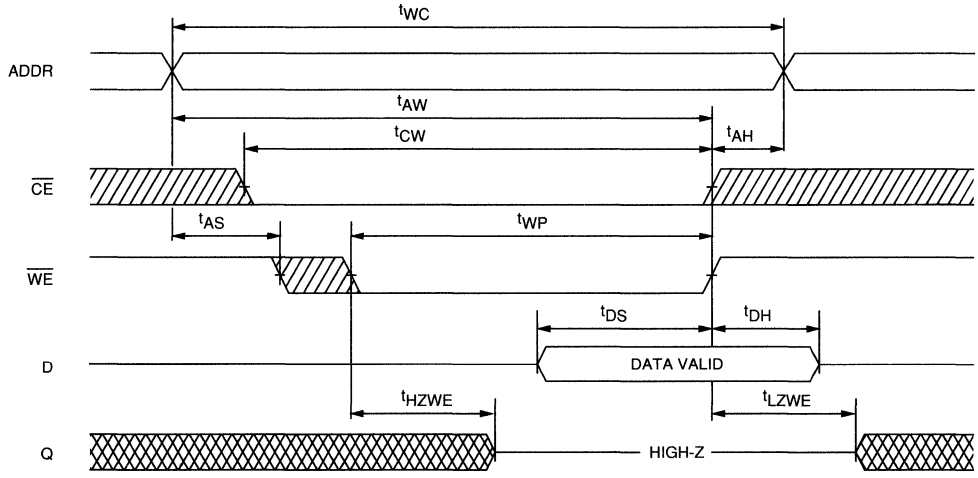
READ CYCLE NO. 1 [8, 9]



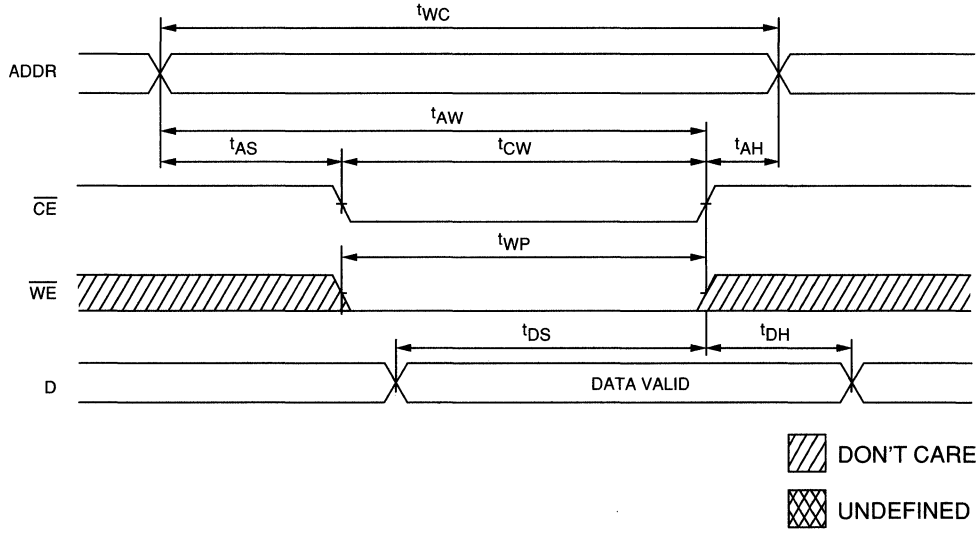
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [12]



SRAM

64K x 1 SRAM

FEATURES

- High speed: 12, 15, 20, 25, 30 and 35ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

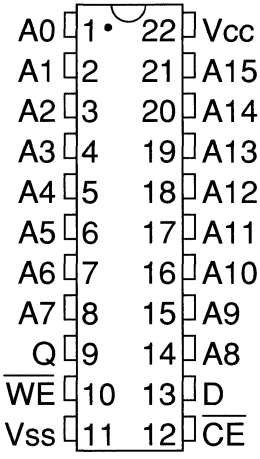
For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

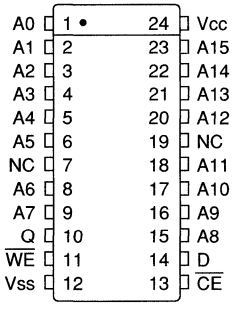
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

PIN ASSIGNMENT (Top View)

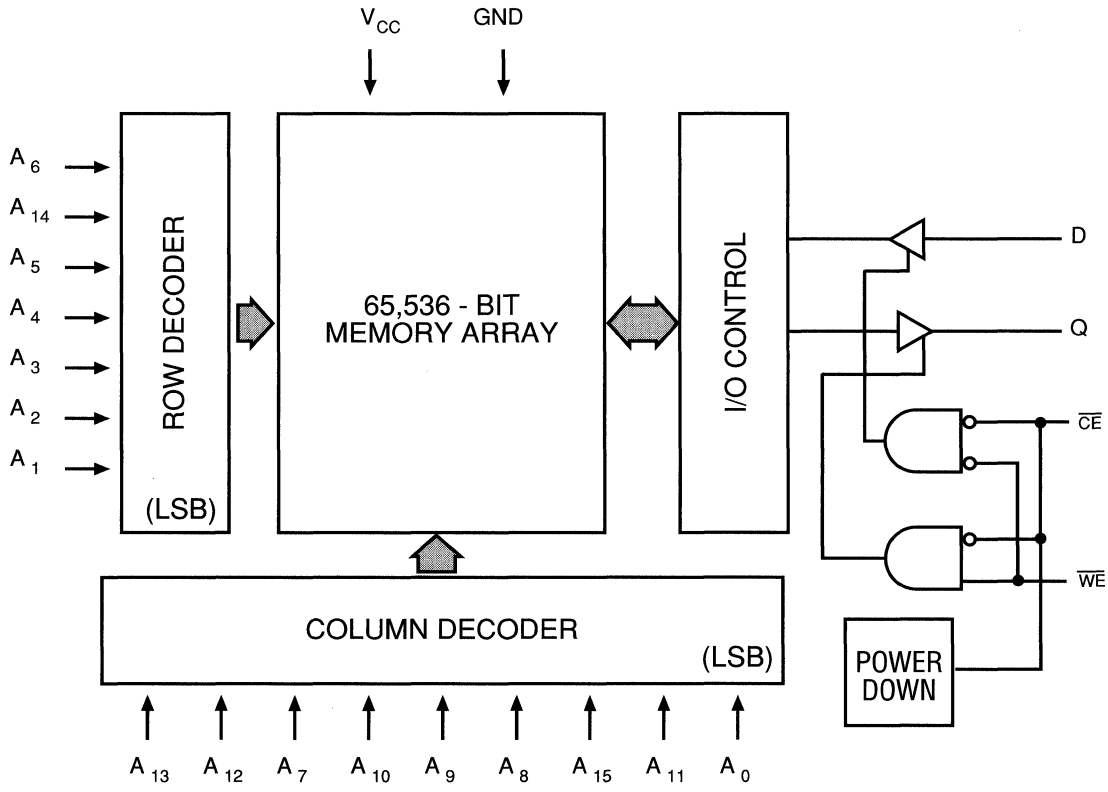
22L/300 DIP
(A-6, B-6)



24L/300 SOJ
(E-4)



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	60	50	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip Enable access time	t_{ACE}		12		12		15		20		25		30	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	t_{HZCE}		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		0		ns	
Chip Disable to power-down time	t_{PD}		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip Enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address setup time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data setup time	t_{DS}	8		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	t_{HZWE}		6		6		8		10		12		15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

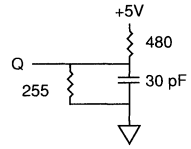


Fig. 1 OUTPUT LOAD EQUIVALENT

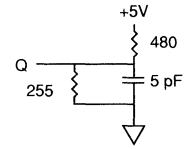


Fig. 2 OUTPUT LOAD EQUIVALENT

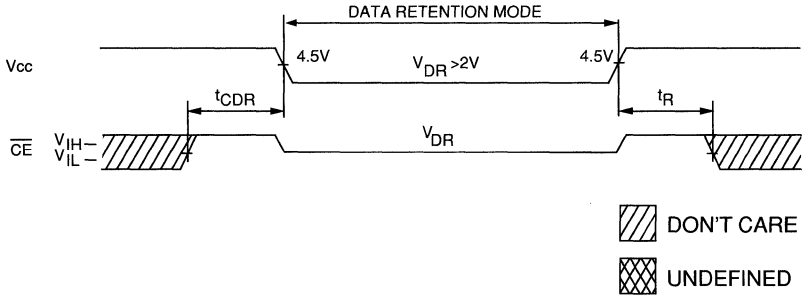
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-167.

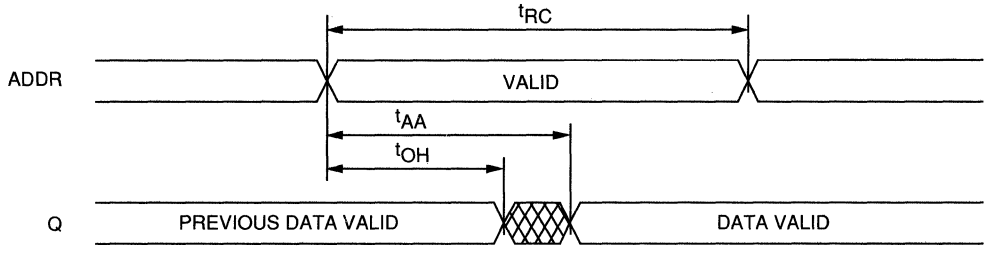
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	I_{CCDR}		95	250	µA	
		Vcc = 3v			300	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

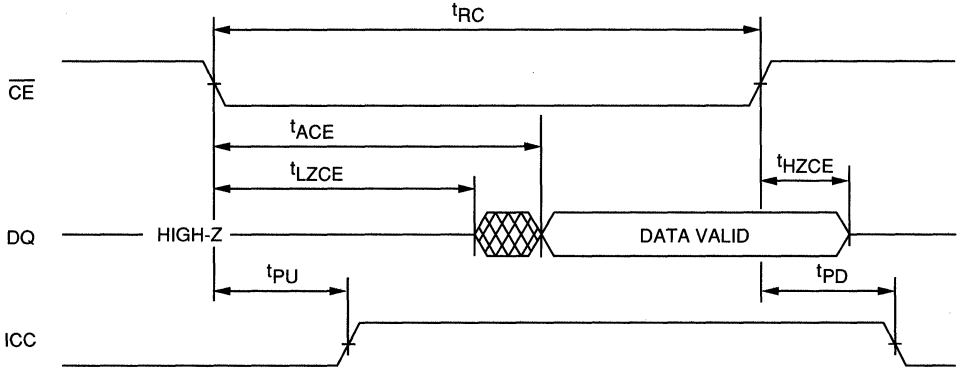
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10]

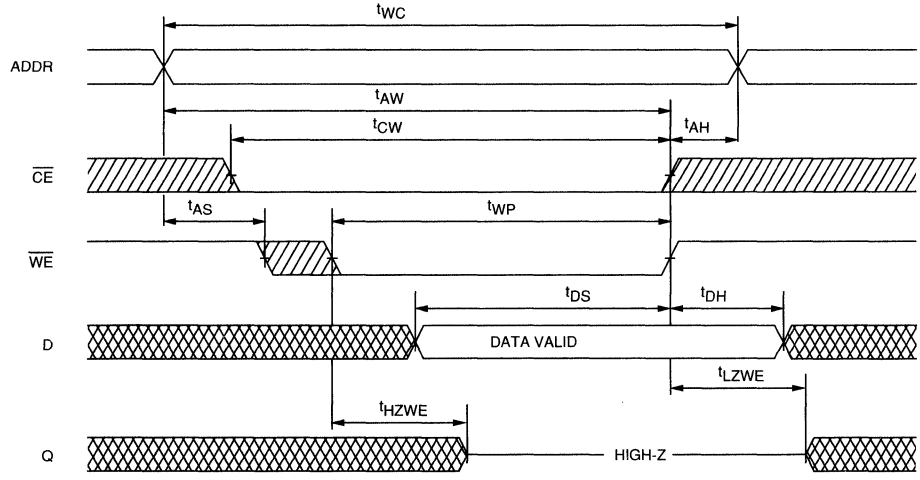


DON'T CARE

UNDEFINED

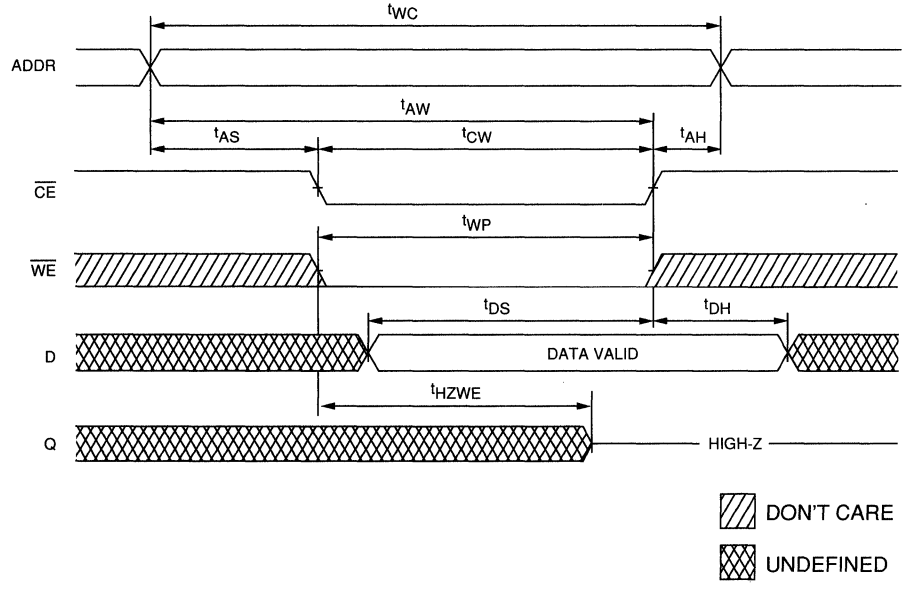
WRITE CYCLE NO. 1

(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2

(Chip Enable Controlled) [12]



SRAM

256K x 1 SRAM

FEATURES

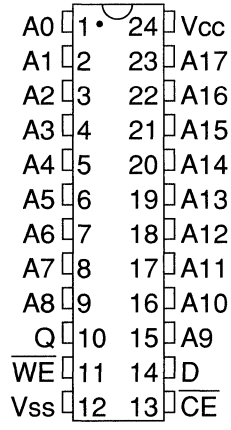
- High speed: 20, 25, 30, 35, and 45ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

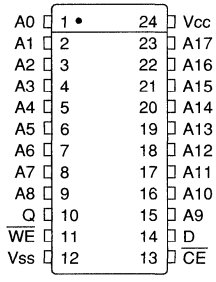
	MARKING
• Timing	
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

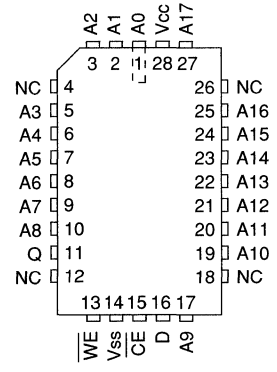
24L/300 DIP
(A-7, B-7)



24L/300 SOJ
(E-4)



28L/LCC
(F-4)



GENERAL DESCRIPTION

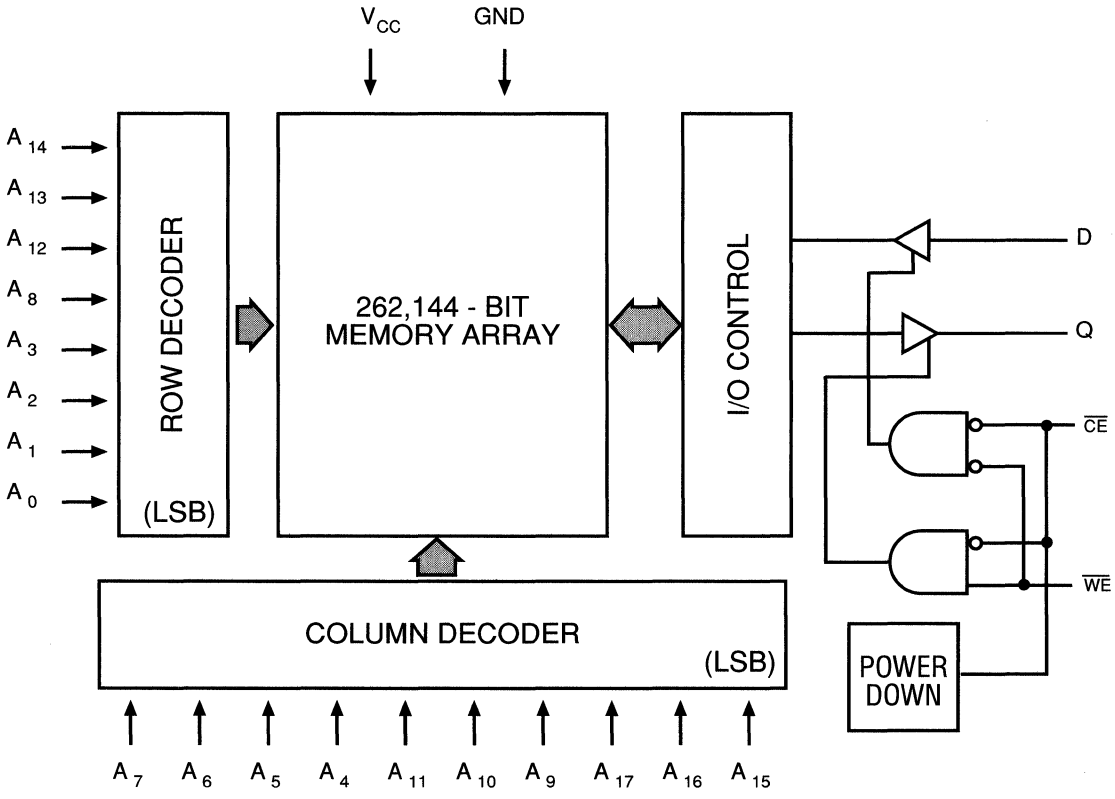
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-30	-35	-40	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	105	95	95	90	90	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	30	25	25	25	25	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	5	5	7	7	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	20		25		30		35		45		ns	
Address access time	^tAA		20		25		30		35		45	ns	
Chip Enable access time	^tACE		20		25		30		35		45	ns	
Output hold from address change	^tOH	3		5		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	6		6		6		6		6		ns	
Chip Disable to output in High-Z	^tHZCE		9		9		12		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip Disable to power-down time	^tPD		20		25		30		35		45	ns	
WRITE Cycle													
WRITE cycle time	^tWC	20		20		25		30		35		ns	
Chip Enable to end of write	^tCW	15		15		18		20		25		ns	
Address valid to end of write	^tAW	15		15		18		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
Write pulse width	^tWP	15		15		18		20		25		ns	
Data setup time	^tDS	10		10		12		15		20		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	5		5		5		5		5		ns	
Write Enable to output in High-Z	^tHZWE		10		10		12		15		18	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

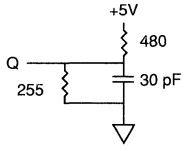


Fig. 1 OUTPUT LOAD EQUIVALENT

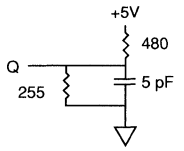


Fig. 2 OUTPUT LOAD EQUIVALENT

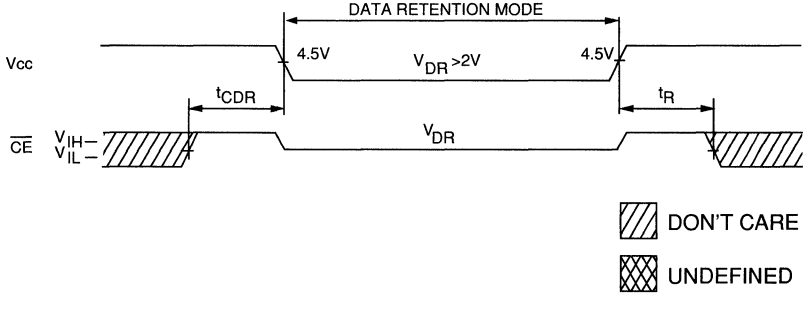
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-169.

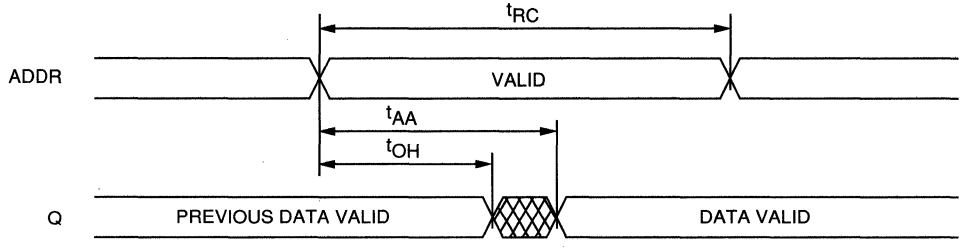
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	300	µA	
		Vcc = 3v			350	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

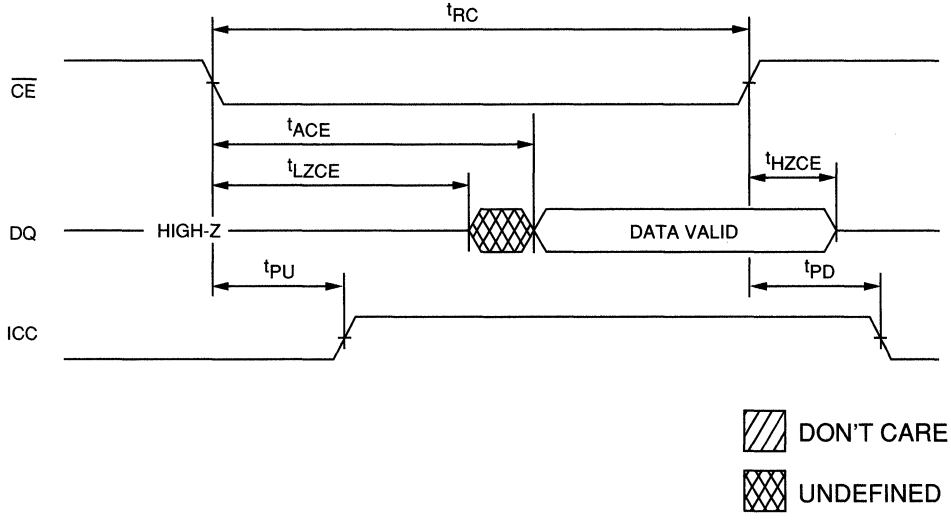
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]

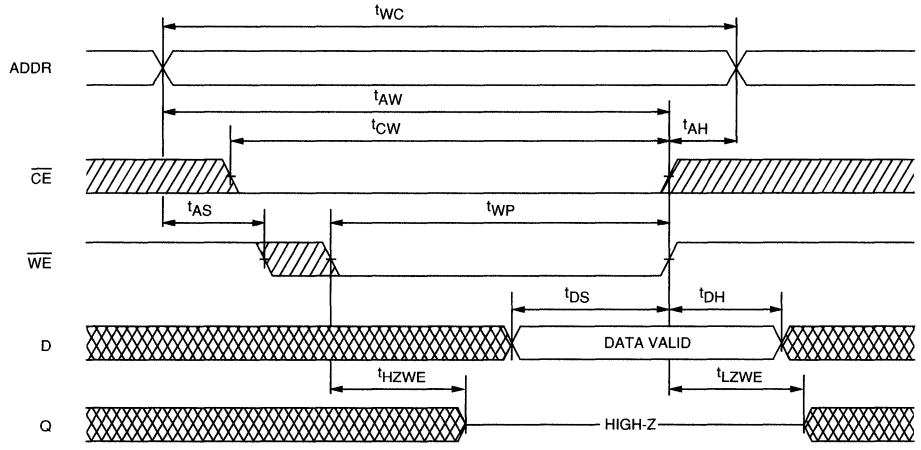


READ CYCLE NO. 2 [7, 8, 10]



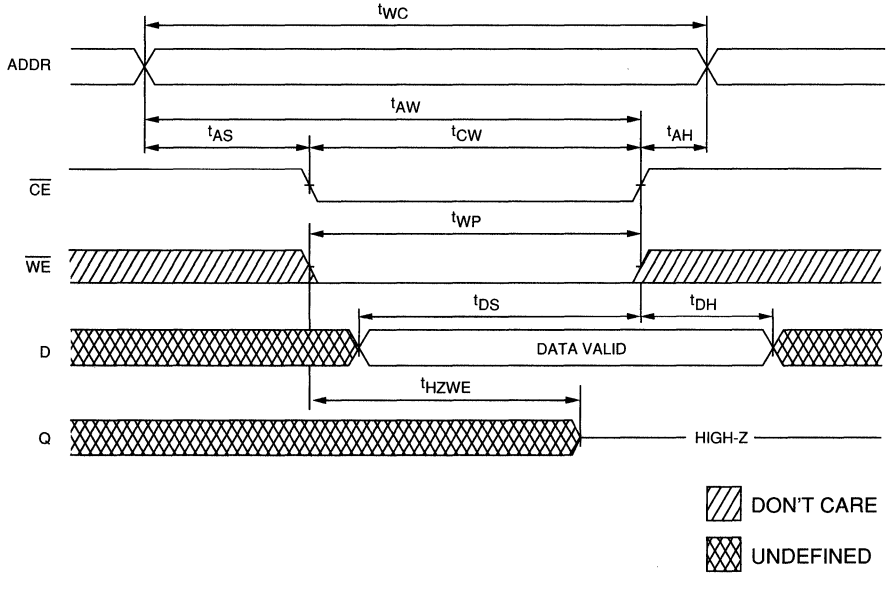
WRITE CYCLE NO. 1

(Write Enable Controlled) [12]



WRITE CYCLE NO. 2

(Chip Enable Controlled) [12]



SRAM

1 MEG x 1 SRAM

FEATURES

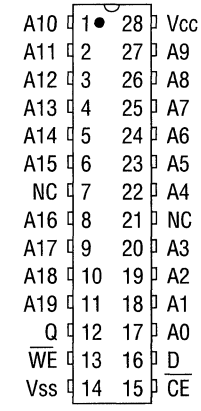
- High speed: 25, 35, and 45ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

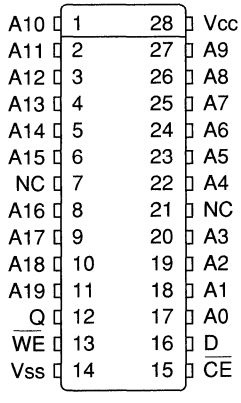
	MARKING
• Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (400 mil)	None
Ceramic DIP (400mil)	C
Plastic SOJ (400 mil)	DJ
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

28L/400 DIP
(A-10)



28L/400 SOJ
(E-9)



GENERAL DESCRIPTION

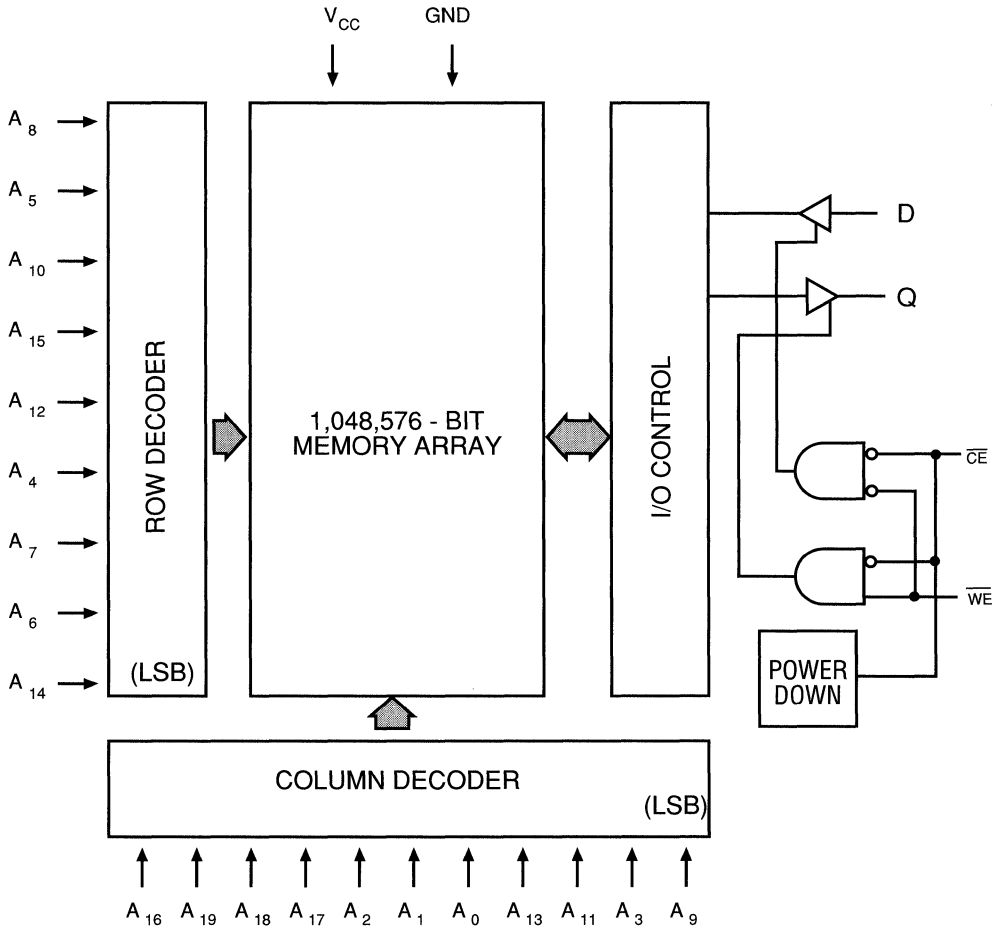
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A6 and A14) are encoded using a gray code.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5.0V ± 10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; Vcc = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}		120	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; Vcc = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}		30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; Vcc = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}		7	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz Vcc = 5V	C_I		8	pF	4
Output Capacitance		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	25		35		45		ns	
Address access time	^tAA		25		35		45	ns	
Chip Enable access time	^tACE		25		35		45	ns	
Output hold from address change	^tOH	5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	
Chip Disable to output in High-Z	^tHZCE		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip Disable to power-down time	^tPD		25		35		45	ns	
WRITE Cycle									
WRITE cycle time	^tWC	25		35		45		ns	
Chip Enable to end of write	^tCW	15		20		25		ns	
Address valid to end of write	^tAW	15		20		25		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
Write pulse width	^tWP	15		20		25		ns	
Data setup time	^tDS	10		15		20		ns	
Data hold time	^tDH	0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	0		0		0		ns	
Write Enable to output in High-Z	^tHZWE	0	10	0	15	0	18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

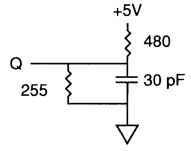


Fig. 1 OUTPUT LOAD EQUIVALENT

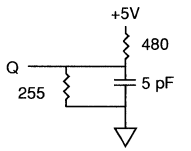


Fig. 2 OUTPUT LOAD EQUIVALENT

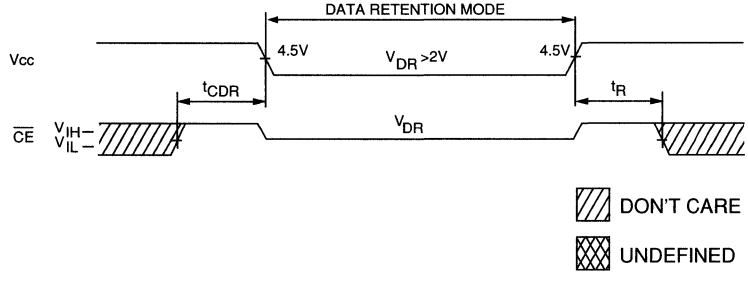
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enable held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-171.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

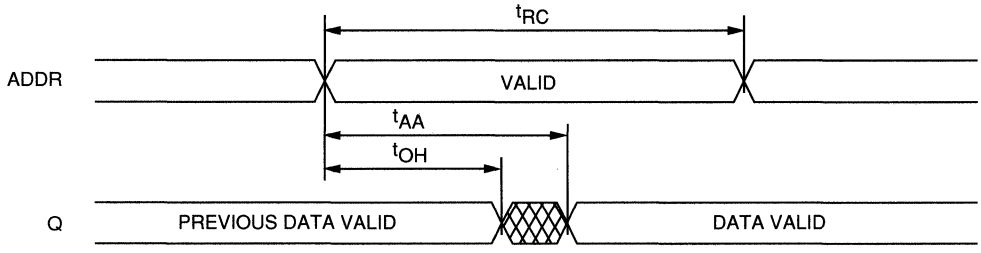
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	500	µA	
		Vcc = 3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

LOW Vcc DATA RETENTION WAVEFORM

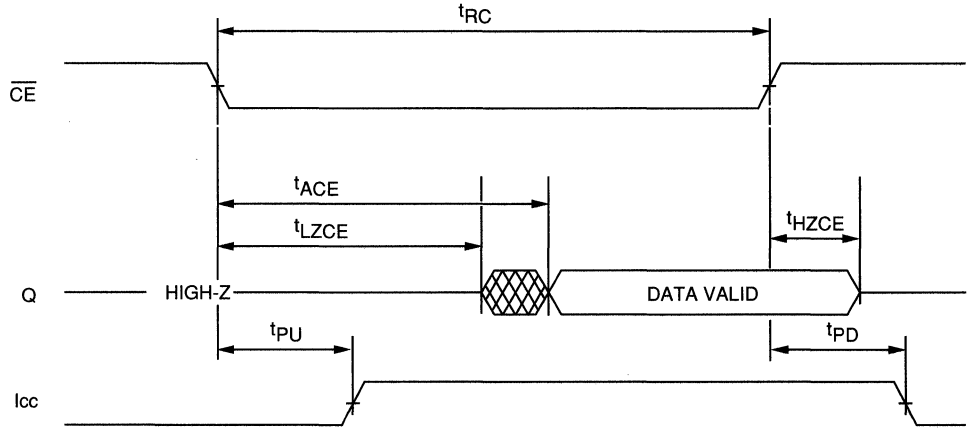


FAST SRAM

READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10]

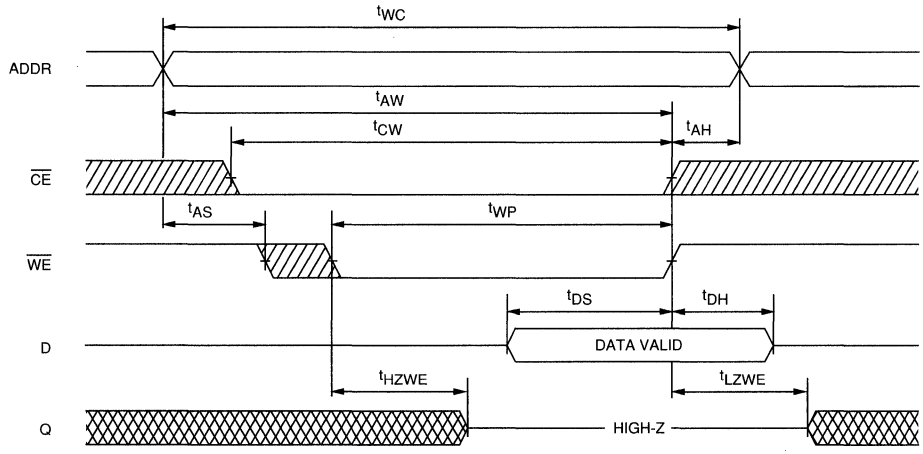


DON'T CARE

UNDEFINED

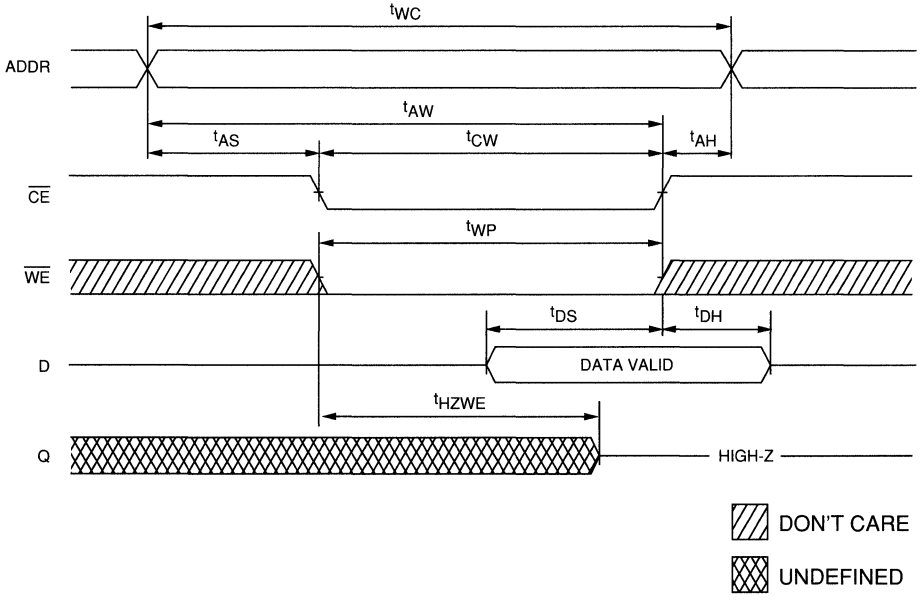
WRITE CYCLE NO. 1

(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2

(Chip Enable Controlled) [12]



SRAM

4K x 4 SRAM

FEATURES

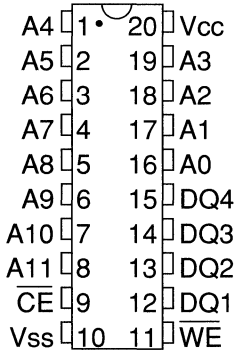
- High speed: 12, 15, 20, 25, 30 and 35ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

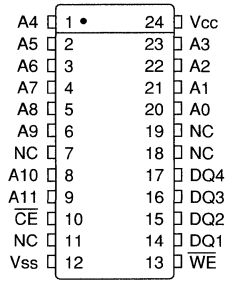
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

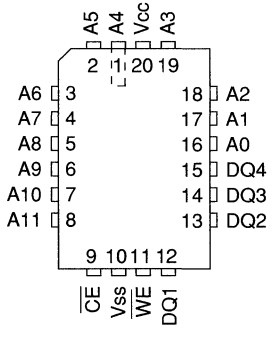
20L/300 DIP
(A-4, B-4)



24L/300 SOJ
(E-4)



20L/LCC
(F-3)



GENERAL DESCRIPTION

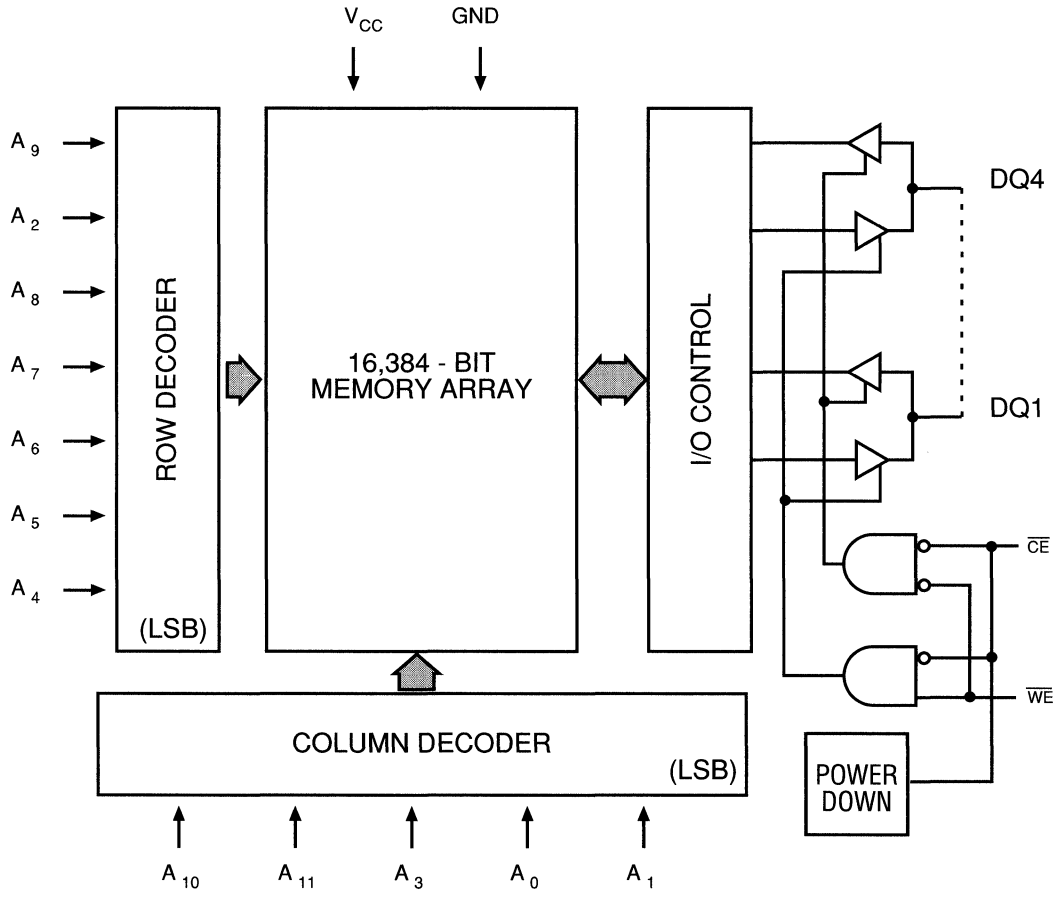
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	140	125	110	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	50	45	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	3	3	3	3	3	3	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip Enable access time	t_{ACE}		11		12		15		20		25		30	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	t_{HZCE}		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		0		ns	
Chip Disable to power-down time	t_{PD}		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip Enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address setup time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data setup time	t_{DS}	7		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	t_{HZWE}		6		6		8		10		12		15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

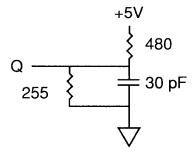


Fig. 1 OUTPUT LOAD EQUIVALENT

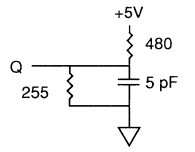


Fig. 2 OUTPUT LOAD EQUIVALENT

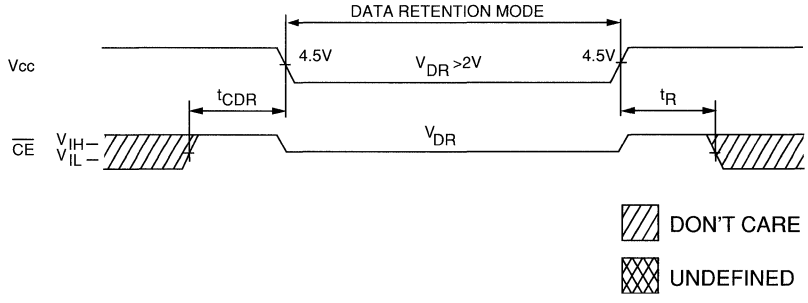
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-165.

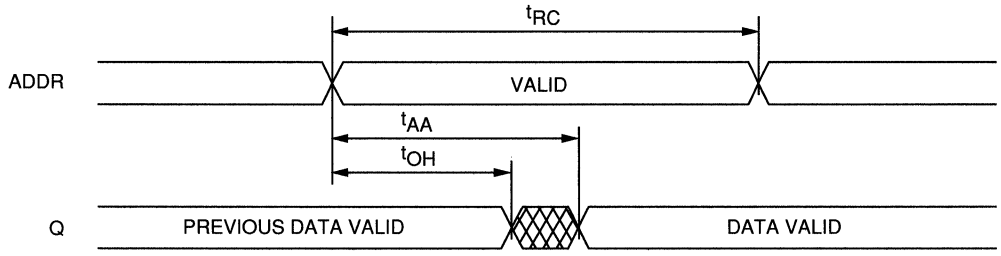
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	250	µA	
		Vcc = 3v			300	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

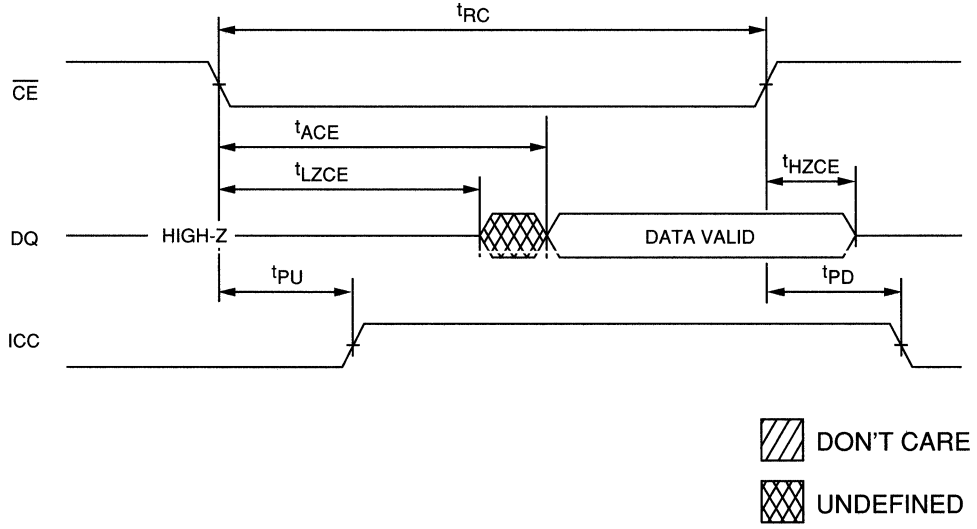
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]

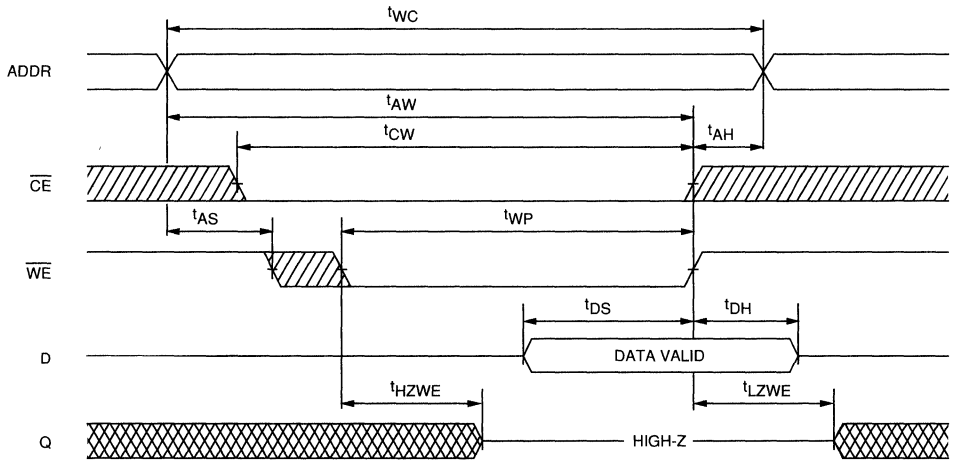


READ CYCLE NO. 2 [7, 8, 10]



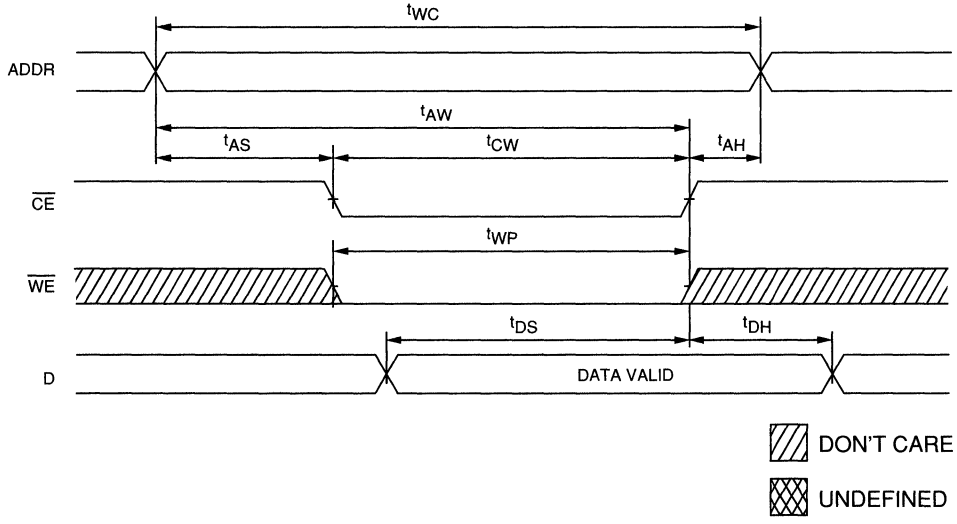
WRITE CYCLE NO. 1

(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2

(Chip Enable Controlled) [12]



SRAM

4K x 4 SRAM
WITH OUTPUT ENABLE

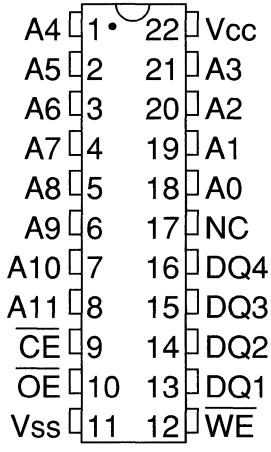
FEATURES
- High speed: 12, 15, 20, 25, 30 and 35ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS — MARKING

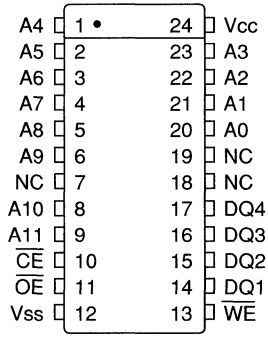
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

22L/300DIP
(A-6, B-6)



24L/300 SOJ
(E-4)



GENERAL DESCRIPTION

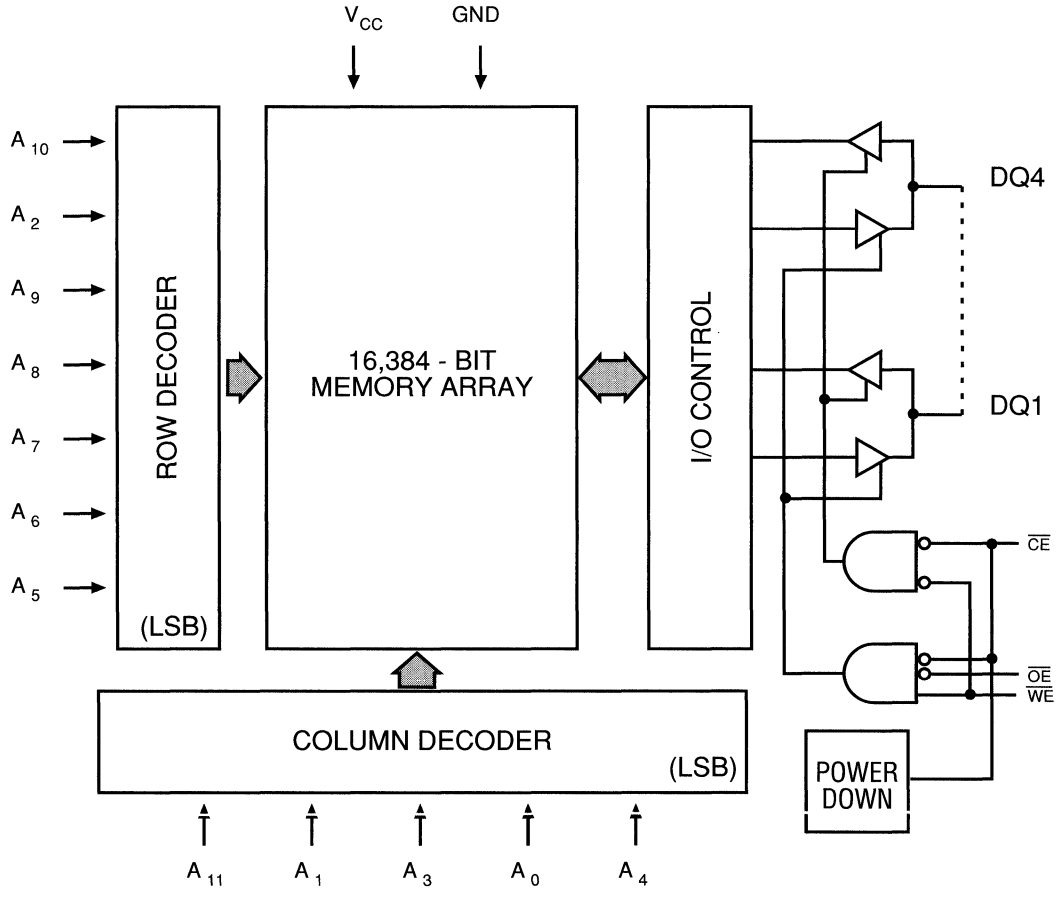
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} .....-1.0V to +7.0V
Storage Temperature (Ceramic) .....-65°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	140	125	110	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	50	45	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	3	3	3	3	3	3	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip Enable access time	^tACE		11		12		15		20		25		30	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	^tHZCE		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip Disable to power-down time	^tPD		12		15		20		25		30		35	ns	
Output enable access time	^tAOE		7		7		9		10		15		20	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output Disable to output in High-Z	^tHZOE		6		6		10		10		15		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip Enable to end of write	^tCW	10		12		15		20		25		25		ns	
Address valid to end of write	^tAW	12		12		15		20		25		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data setup time	^tDS	7		8		10		10		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^tHZWE		6		6		8		10		12		15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

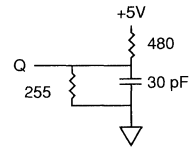


Fig. 1 OUTPUT LOAD EQUIVALENT

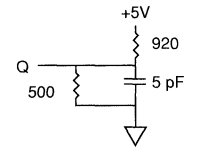


Fig. 2 OUTPUT LOAD EQUIVALENT

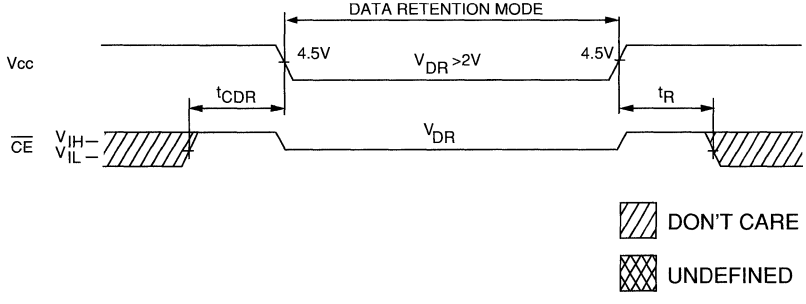
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-165.

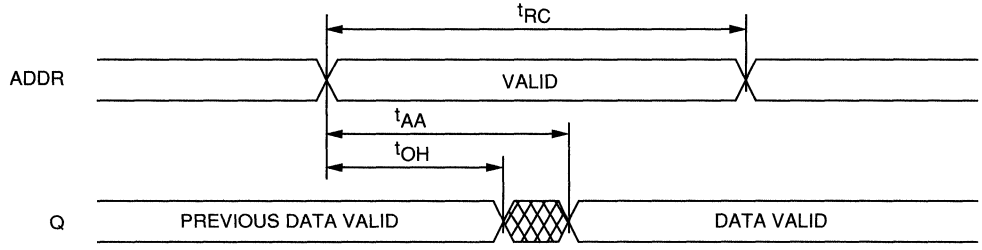
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	250	µA	
		Vcc =3v			300	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

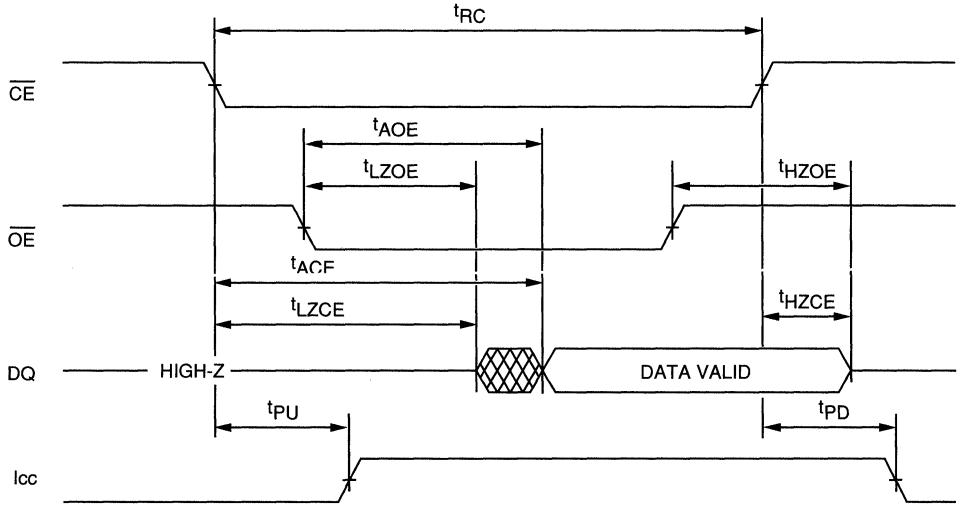
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



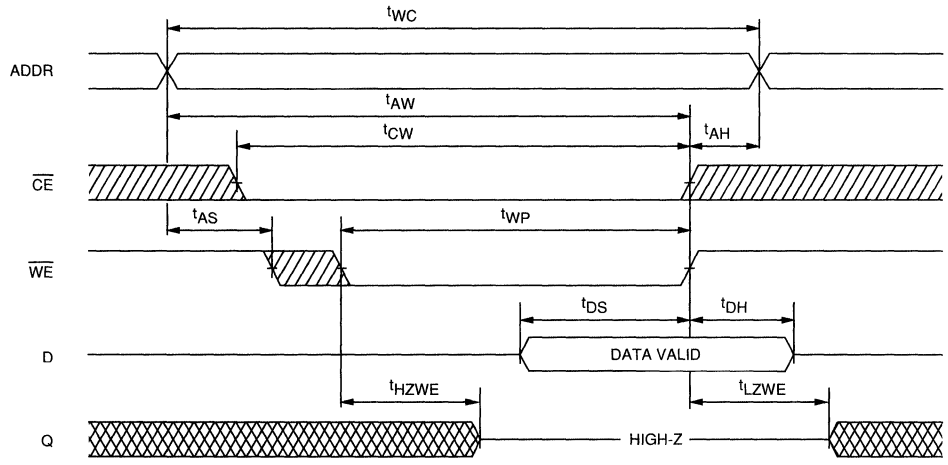
READ CYCLE NO. 2 [7, 8, 10]



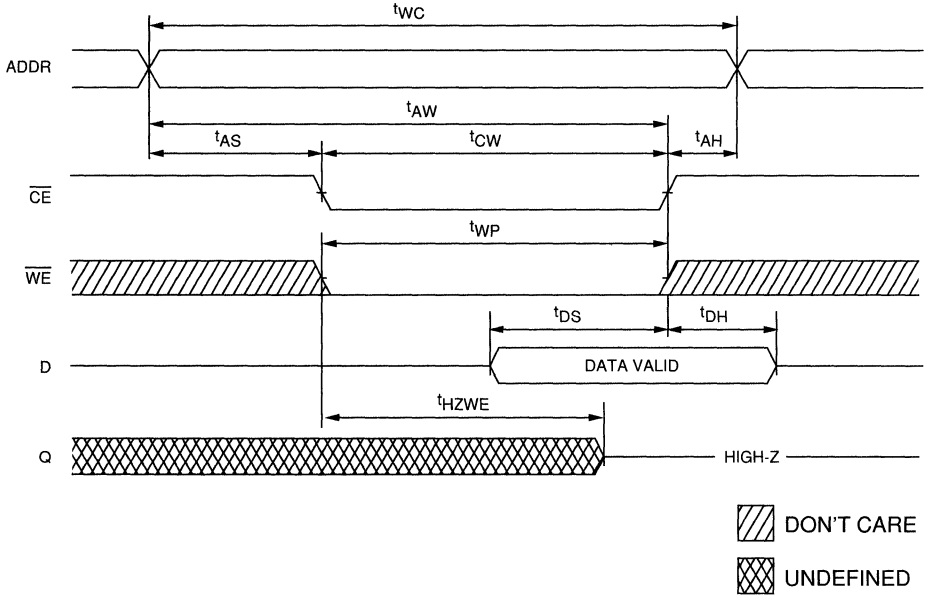
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [12]



SRAM

4K x 4 SRAM

WITH SEPARATE INPUTS AND OUTPUTS

FEATURES

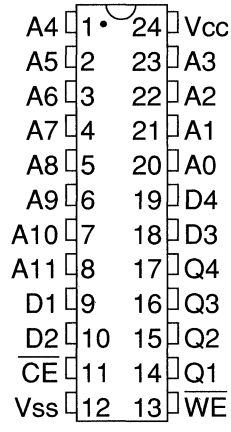
- High speed: 12, 15, 20, 25, 30 and 35ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible
- MT5C1606 – output tracks input during WRITE
- MT5C1607 – output high impedance during WRITE

OPTIONS

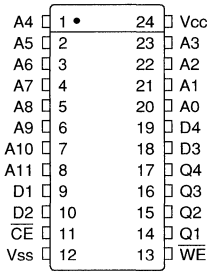
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

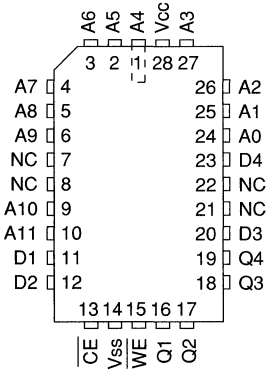
24L/300DIP
(A-7, B-7)



24L/300 SOJ
(E-4)



28L/LCC
(F-4)



GENERAL DESCRIPTION

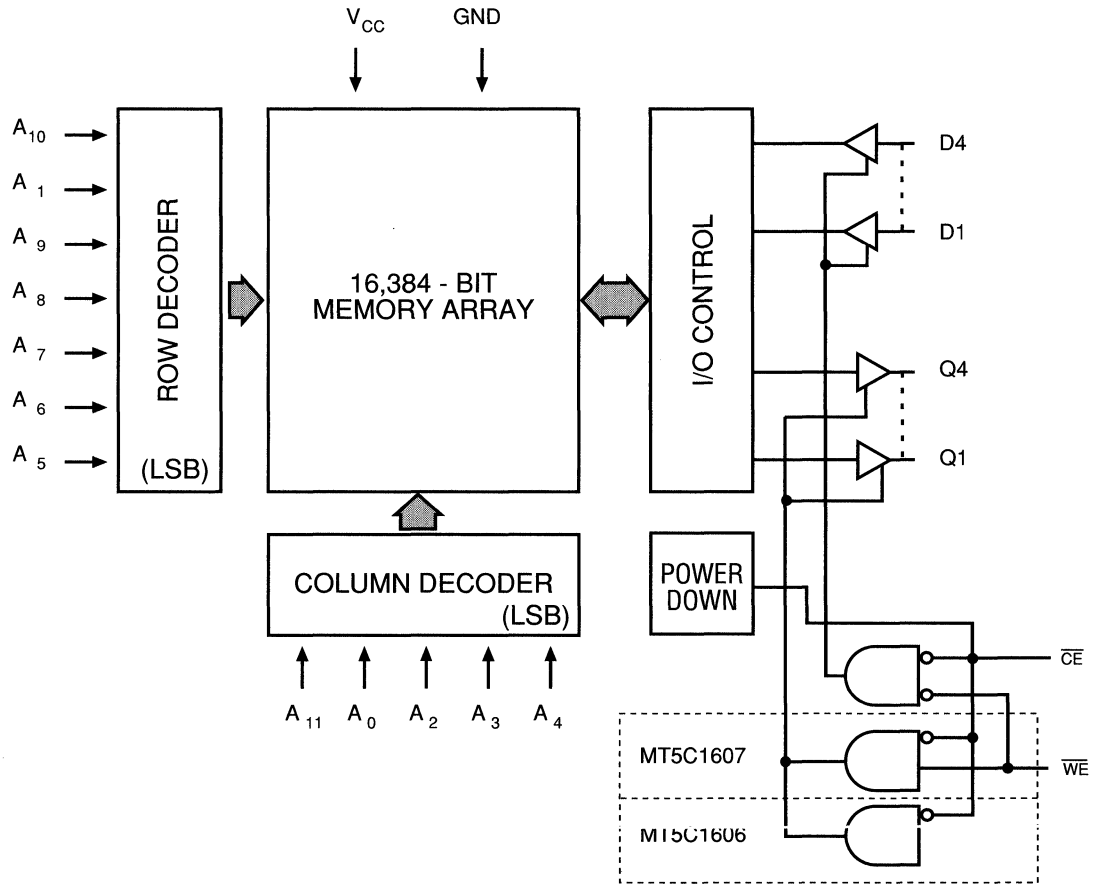
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x4 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE (1)	L	L	HIGH-Z	ACTIVE
WRITE (2)	L	L	D	ACTIVE

NOTE: 1. MT5C1607 ONLY
2. MT5C1606 ONLY

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	140	125	110	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	50	45	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	3	3	3	3	3	3	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip Enable access time	^tACE		11		12		15		20		25		30	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	^tHZCE		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip Disable to power-down time	^tPD		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip Enable to end of write	^tCW	10		12		15		20		25		25		ns	
Address valid to end of write	^tAW	12		12		15		20		25		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data setup time	^tDS	7		8		10		10		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^tHZWE		6		6		8		10		12		15	ns	
Write Enable to output valid	^tAWE		12		15		20		25		30		35	ns	
Data valid to output valid	^tADV		12		15		20		25		30		35	ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

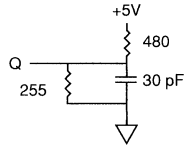


Fig. 1 OUTPUT LOAD EQUIVALENT

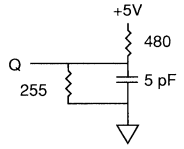


Fig. 2 OUTPUT LOAD EQUIVALENT

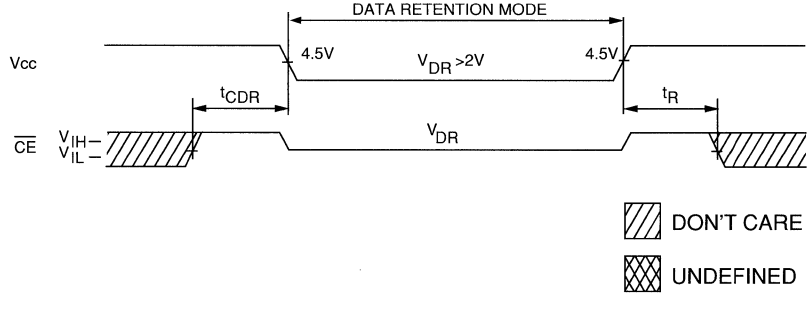
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-165.

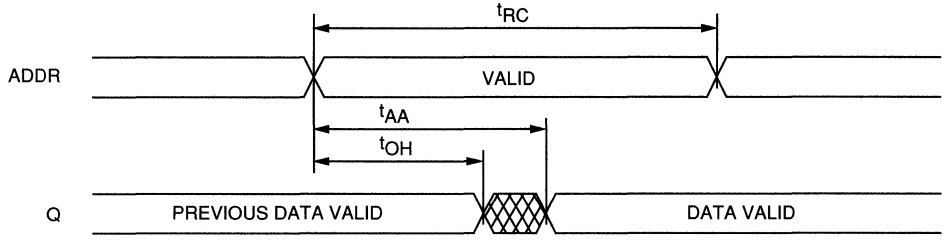
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	I_{CCDR}		95	250	µA	
		Vcc = 3v			300	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

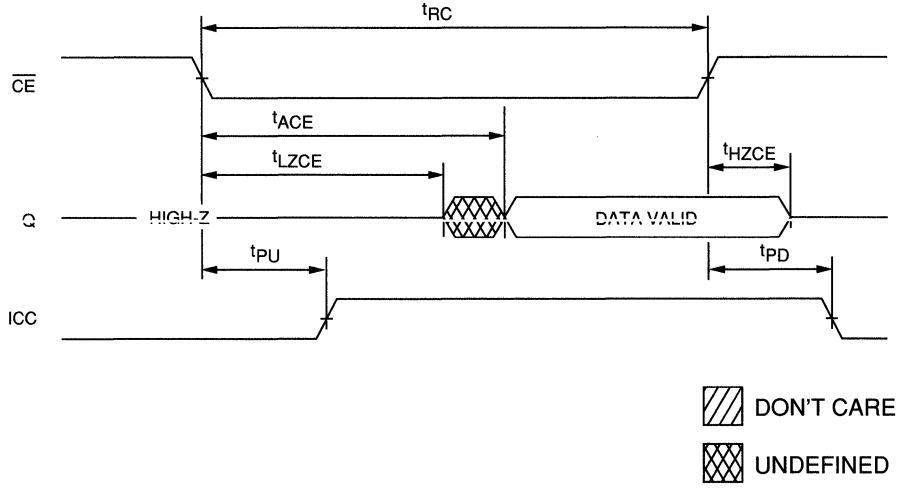
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]

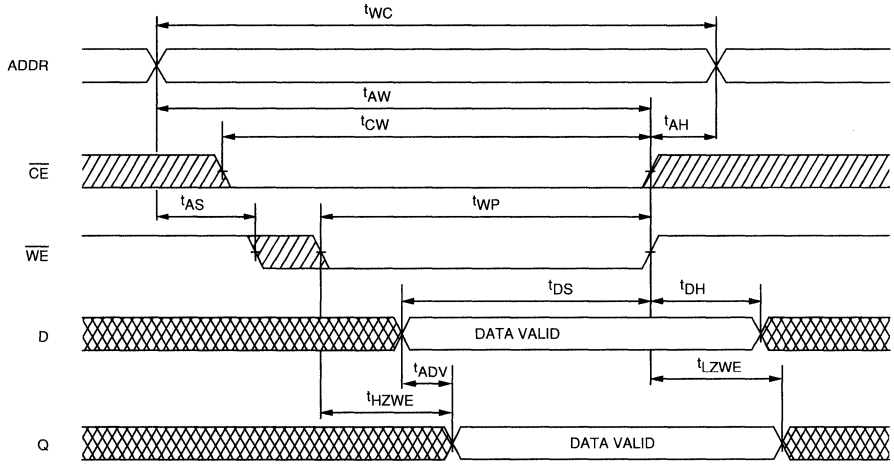


READ CYCLE NO. 2 [7, 8, 10]



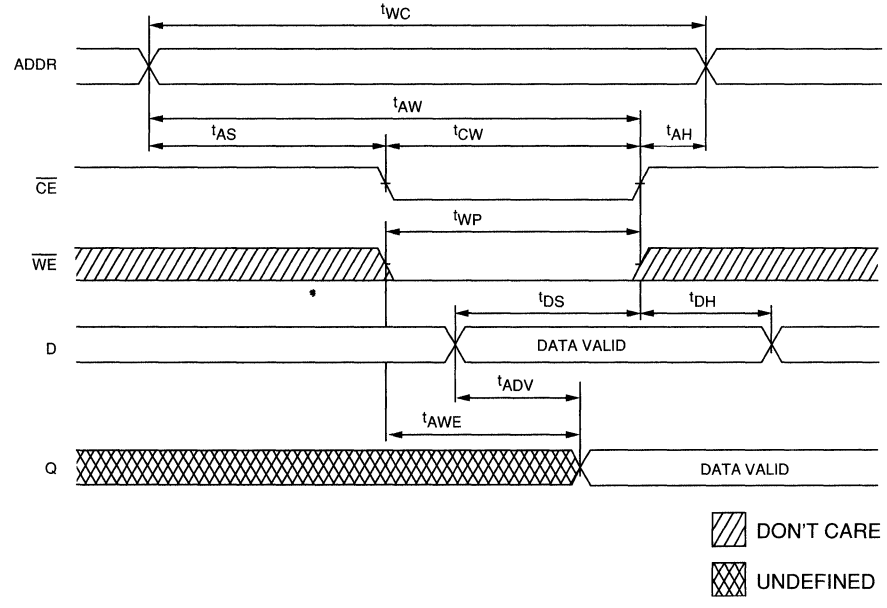
WRITE CYCLE NO. 1

(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2

(Chip Enable Controlled) [12]



SRAM

16K x 4 SRAM

FEATURES

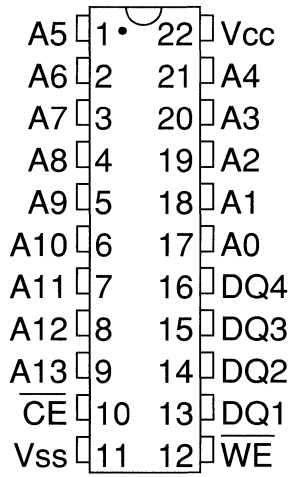
- High speed: 12, 15, 20, 25, 30 and 35ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

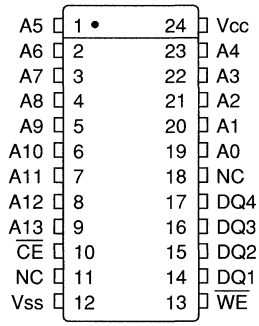
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

22L/300 DIP
(A-6, B-6)



24L/300 SOJ
(E-4)



GENERAL DESCRIPTION

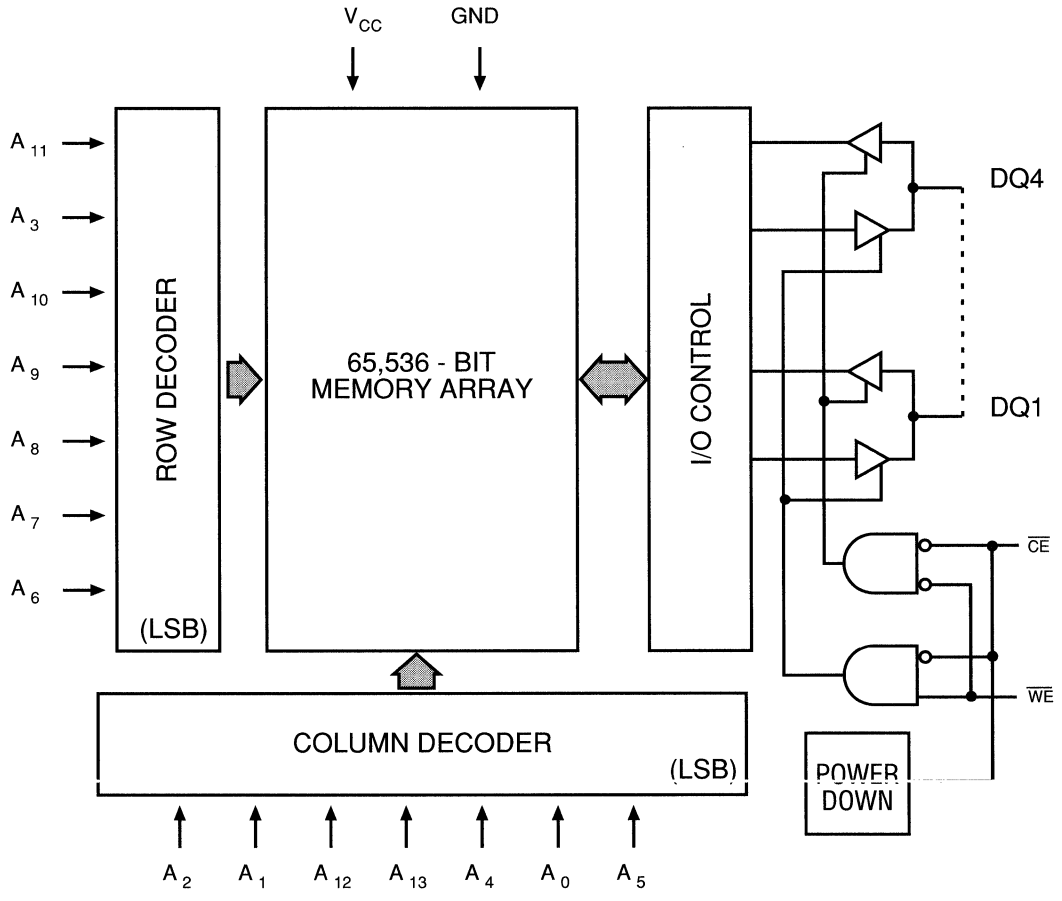
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	60	50	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip Enable access time	t_{ACE}		12		12		15		20		25		30	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	t_{HZCE}		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		0		ns	
Chip Disable to power-down time	t_{PD}		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip Enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address setup time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data setup time	t_{DS}	8		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	t_{HZWE}		6		6		8		10		12		15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

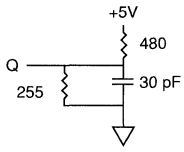


Fig. 1 OUTPUT LOAD EQUIVALENT

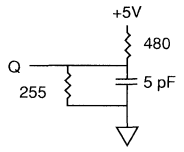


Fig. 2 OUTPUT LOAD EQUIVALENT

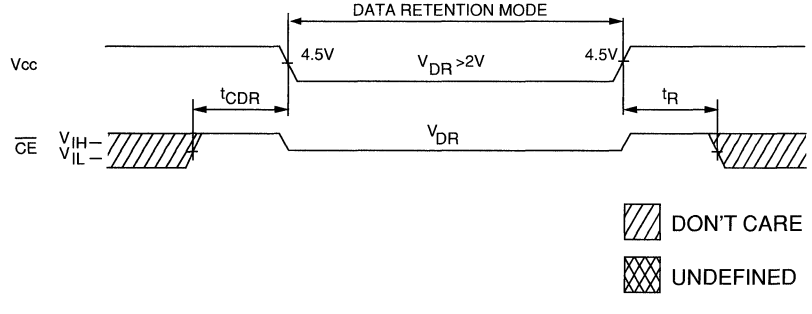
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-167.

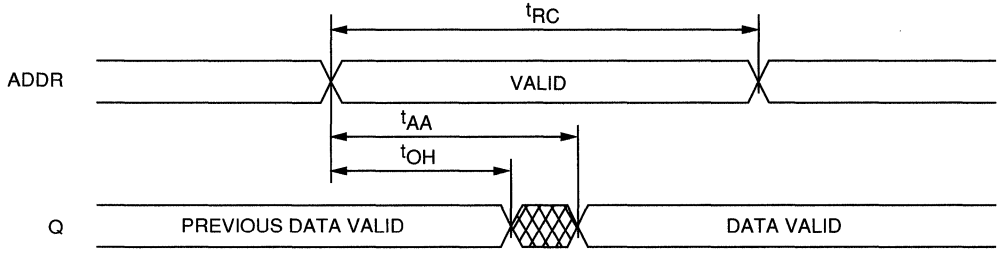
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	I_{CCDR}		95	250	µA	
		Vcc = 3v			300	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

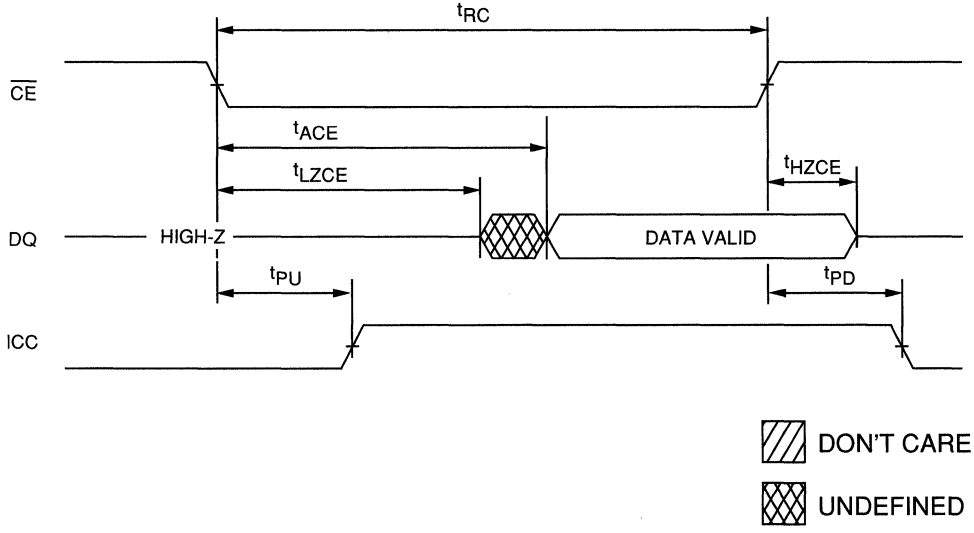
LOW Vcc DATA RETENTION WAVEFORM



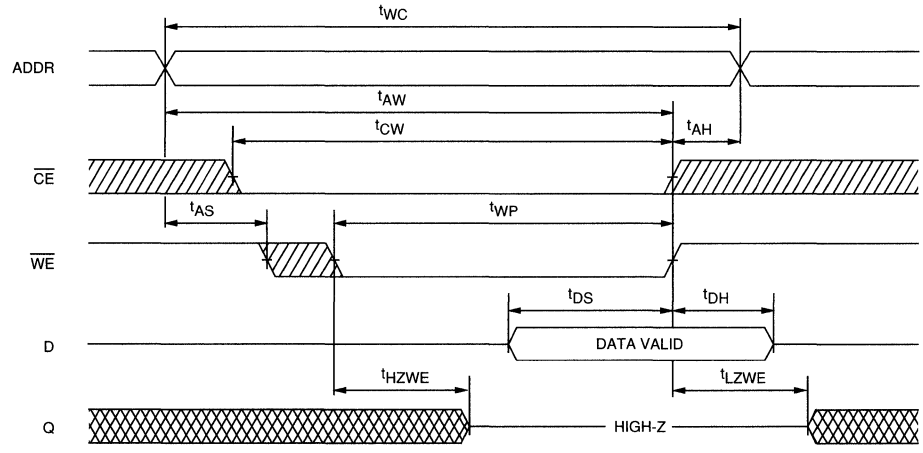
READ CYCLE NO. 1 [8, 9]



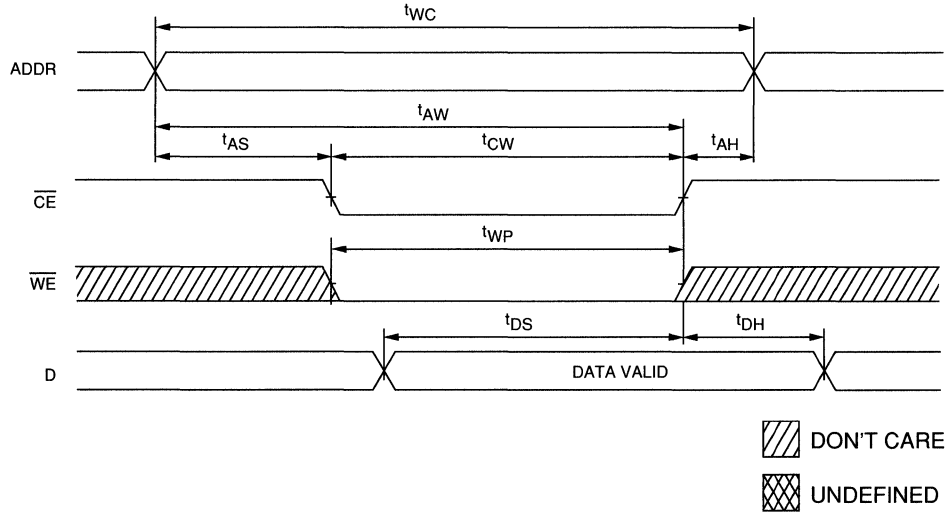
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled)[12]



SRAM

16K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

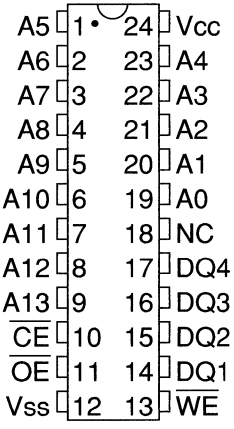
- High speed: 12, 15, 20, 25, 30 and 35ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

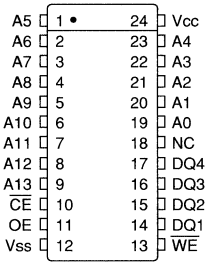
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

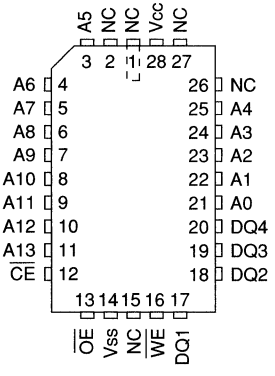
24L/300 DIP
(A-7, B-7)



24L/300 SOJ
(E-4)



28L/LCC
(F-4)



GENERAL DESCRIPTION

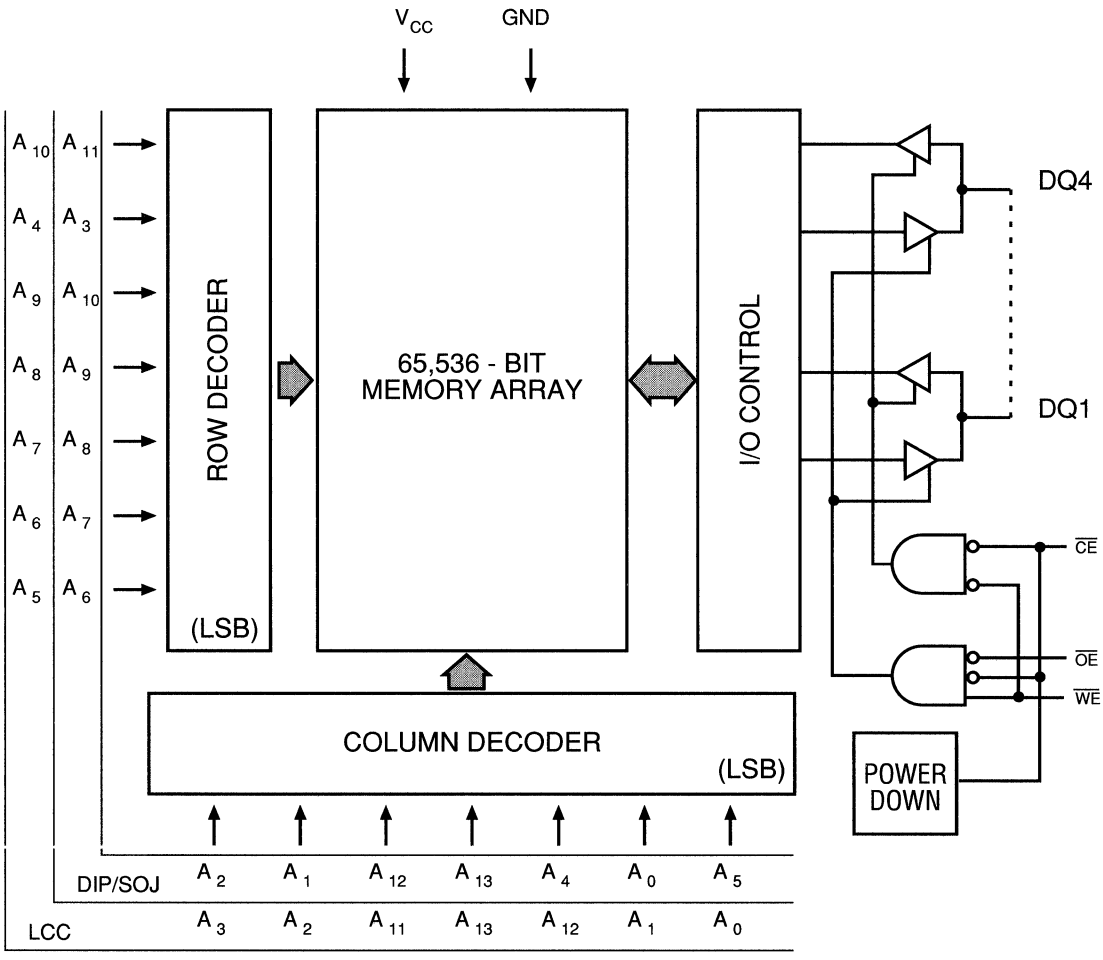
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	60	50	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \leq T_A \leq 70°C$; Vcc = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	tRC	12		15		20		25		30		35		ns	
Address access time	tAA		12		15		20		25		30		35	ns	
Chip Enable access time	tACE		12		12		15		20		25		30	ns	
Output hold from address change	tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	tLZCE	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	tHZCE		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		0		ns	
Chip Disable to power-down time	tPD		12		15		20		25		30		35	ns	
Output Enable access time	tAOE		7		7		9		10		15		20	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		0		0		ns	
Output Disable to output in High-Z	tHZOE		6		6		10		10		15		20	ns	6
WRITE Cycle															
WRITE cycle time	tWC	12		15		20		25		30		35		ns	
Chip Enable to end of write	tCW	10		12		15		20		25		25		ns	
Address valid to end of write	tAW	12		12		15		20		25		25		ns	
Address setup time	tAS	0		0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		0		ns	
Write pulse width	tWP	10		12		15		20		25		25		ns	
Data setup time	tDS	8		8		10		10		15		15		ns	
Data hold time	tDH	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	tLZWE	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	tHZWE		6		6		8		10		12		15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

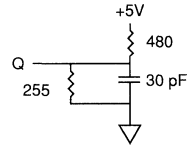


Fig. 1 OUTPUT LOAD EQUIVALENT

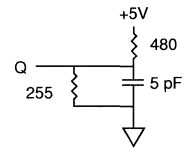


Fig. 2 OUTPUT LOAD EQUIVALENT

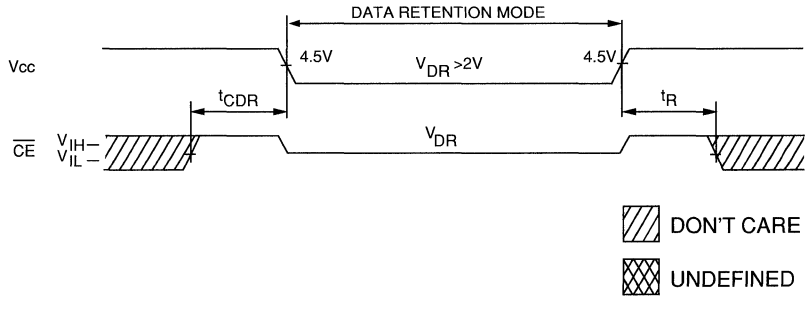
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-167.

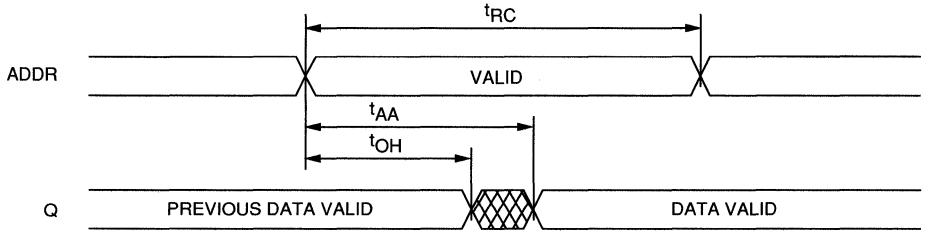
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	250	µA	
		Vcc = 3v			300	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

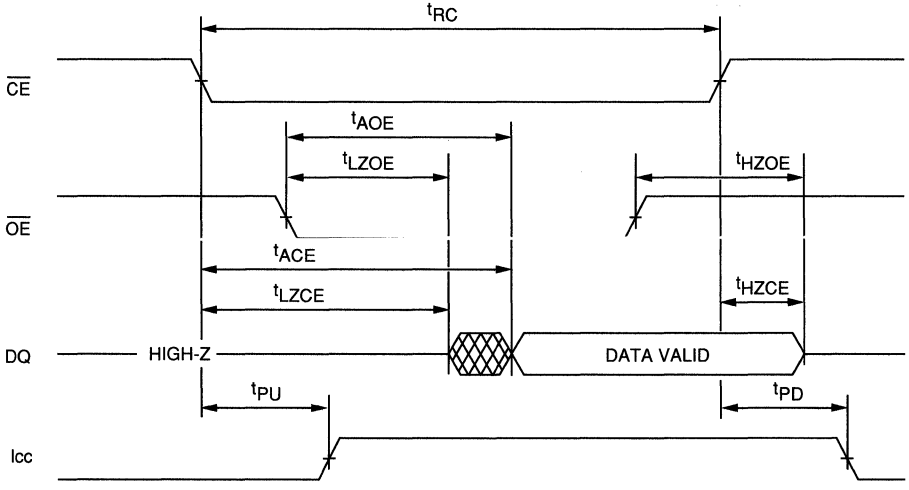
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



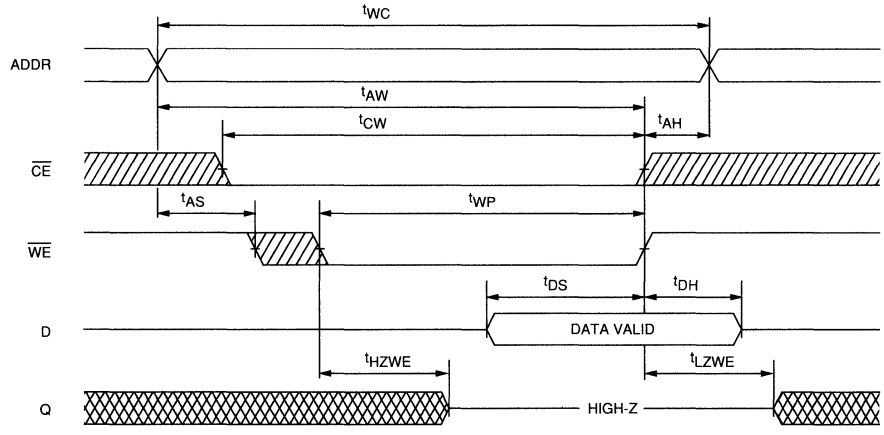
READ CYCLE NO. 2 [7, 8, 10]



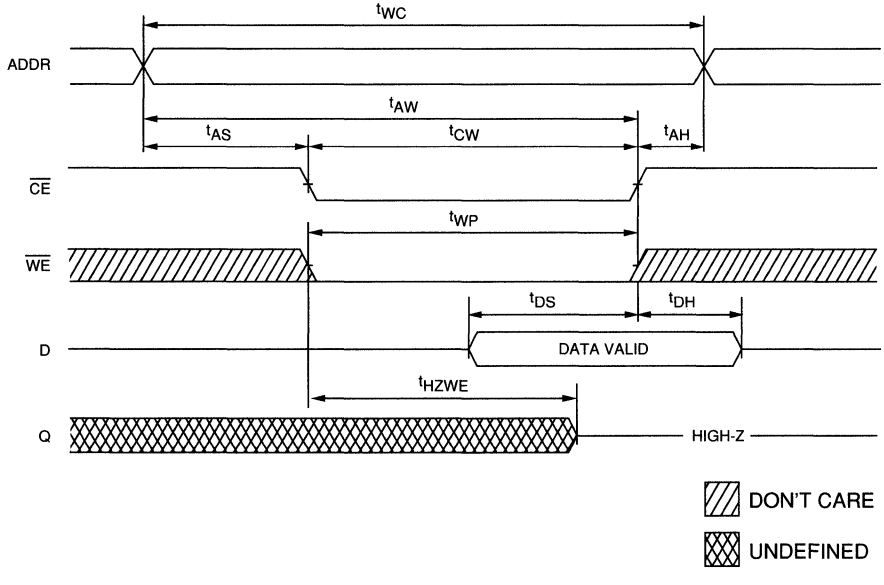
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [12]



SRAM

16K x 4 SRAM

WITH SEPARATE INPUTS AND OUTPUTS

FEATURES

- High speed: 12, 15, 20, 25, 30 and 35ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE1}$, $\overline{CE2}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- MT5C6406 – output tracks input during WRITE
- MT5C6407 – output high impedance during WRITE

OPTIONS

	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

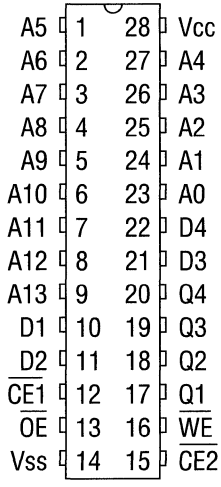
For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x4 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

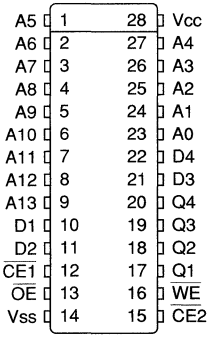
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

PIN ASSIGNMENT (Top View)

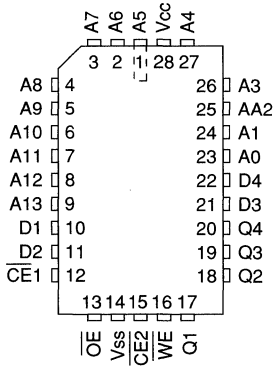
28L/300 DIP
(A-9, B-9)



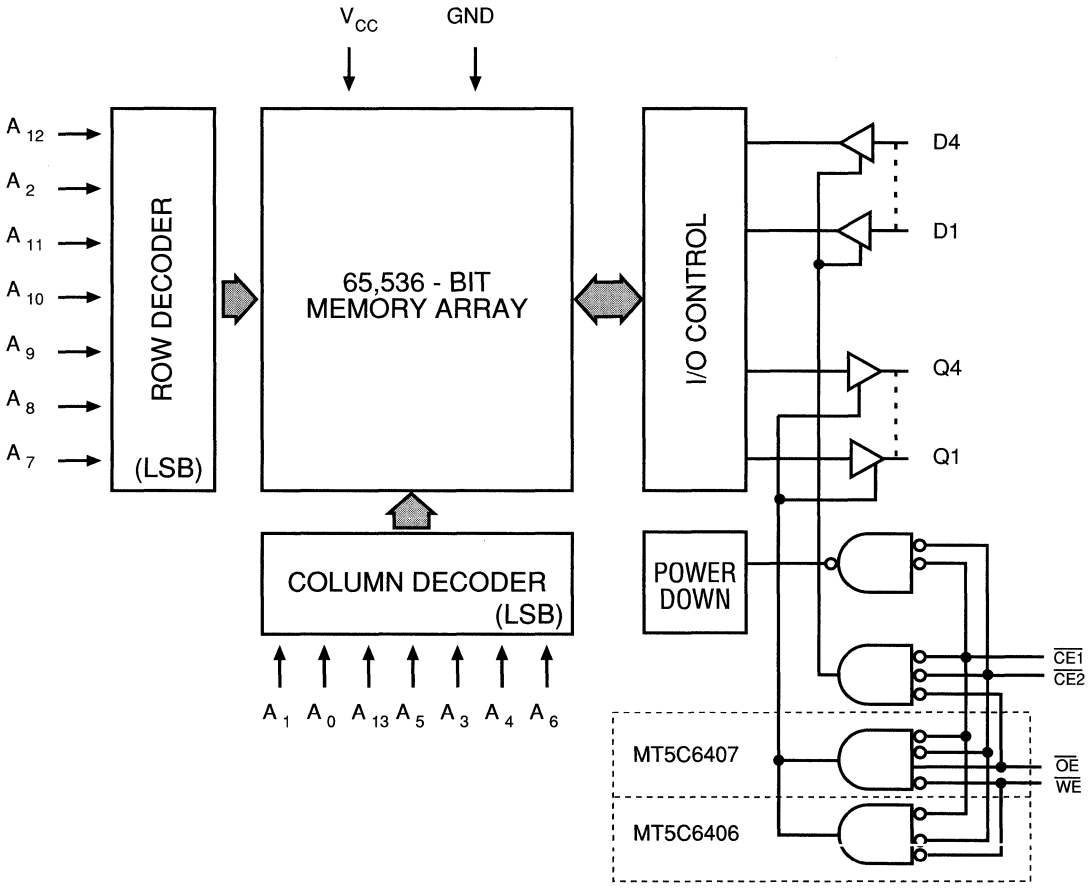
28L/300 SOJ
(E-8)



28L/LCC
(F-4)



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	$\overline{CE2}$	$\overline{OE}$	$\overline{WE}$	OUTPUTS	POWER
STANDBY	H	X	X	X	HIGH-Z	STANDBY
STANDBY	X	H	X	X	HIGH-Z	STANDBY
READ	L	L	L	H	Q	ACTIVE
READ	L	L	H	H	HIGH-Z	ACTIVE
WRITE (1)	L	L	X	L	HIGH-Z	ACTIVE
WRITE (2)	L	L	L	L	D	ACTIVE
WRITE (2)	L	L	H	L	HIGH-Z	ACTIVE

NOTE: 1. MT5C6407 ONLY
2. MT5C6406 ONLY

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	60	50	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; Vcc = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip Enable access time	^tACE		12		12		15		20		25		30	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	^tHZCE		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip Disable to power-down time	^tPD		12		15		20		25		30		35	ns	
Output Enable access time	^tAOE		7		7		9		10		15		20	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output Disable to output in High-Z	^tHZOE		6		6		10		10		15		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip Enable to end of write	^tCW	10		12		15		20		25		25		ns	
Address valid to end of write	^tAW	12		12		15		20		25		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data setup time	^tDS	8		8		10		10		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^tHZWE		6		6		8		10		12		15	ns	6
Write Enable to output valid	^tAWE		12		15		20		25		30		35	ns	
Data valid to output valid	^tADV		12		15		20		25		30		35	ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

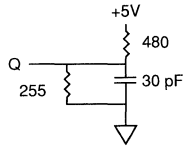


Fig. 1 OUTPUT LOAD EQUIVALENT

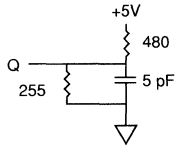


Fig. 2 OUTPUT LOAD EQUIVALENT

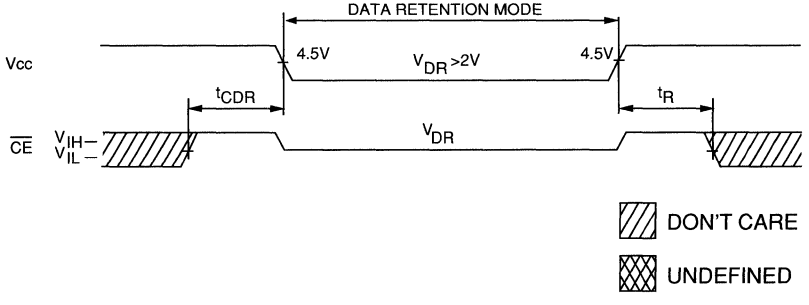
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-167.

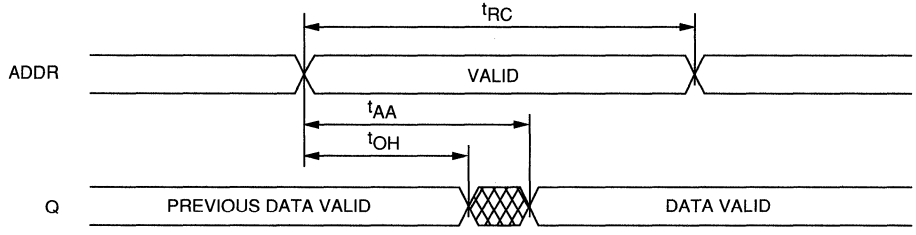
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	250	µA	
		Vcc = 3v			300	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

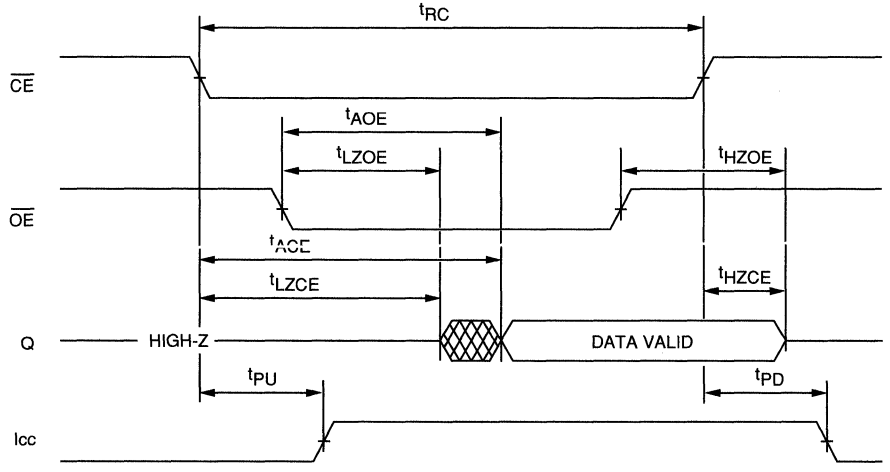
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



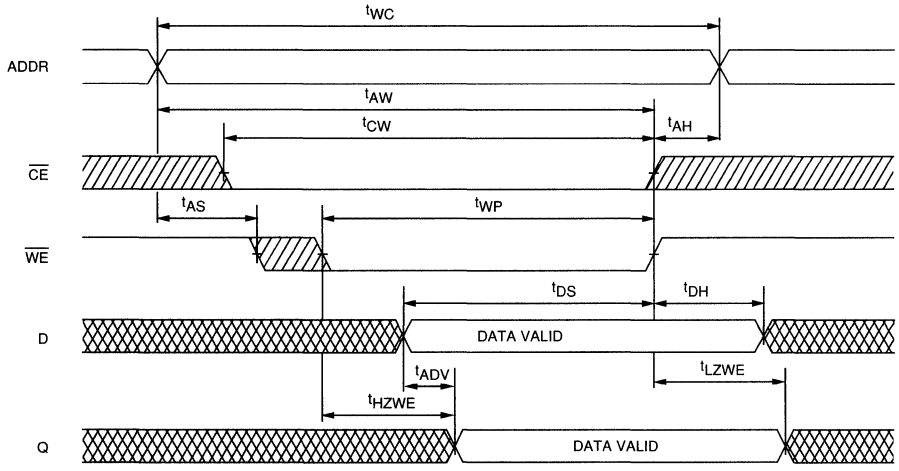
READ CYCLE NO. 2 [7, 8, 10]



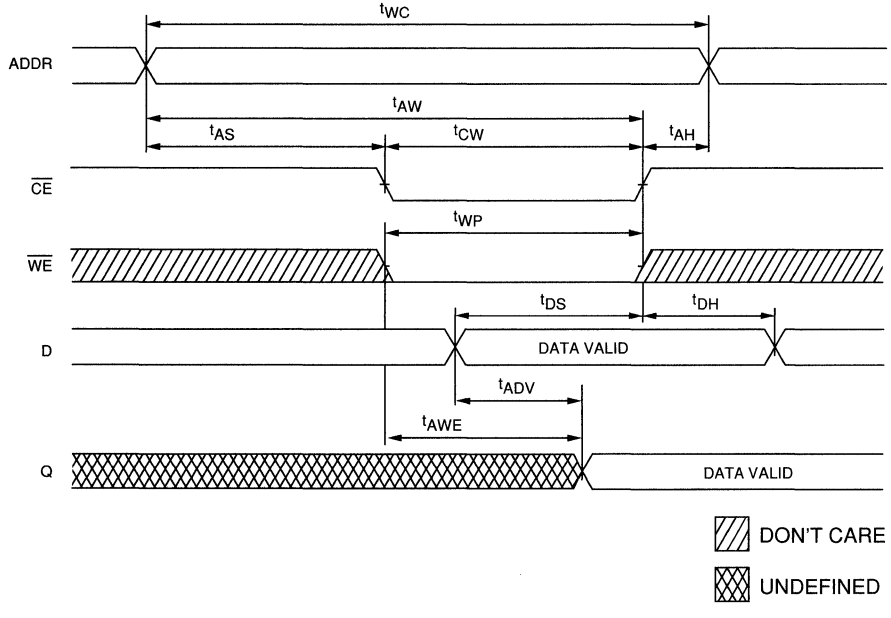
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [12]



SRAM

64K x 4 SRAM

FEATURES

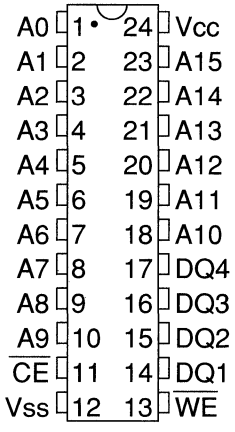
- High speed: 20, 25, 30, 35, and 45ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

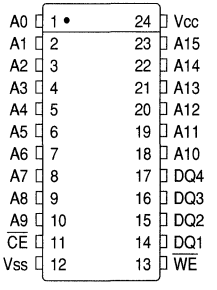
	MARKING
• Timing	
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

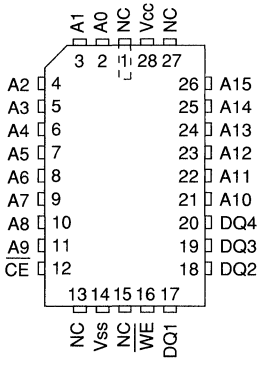
24L/300 DIP
(A-7, B-7)



24L/300 SOJ
(E-4)



28L/LCC
(F-4)



GENERAL DESCRIPTION

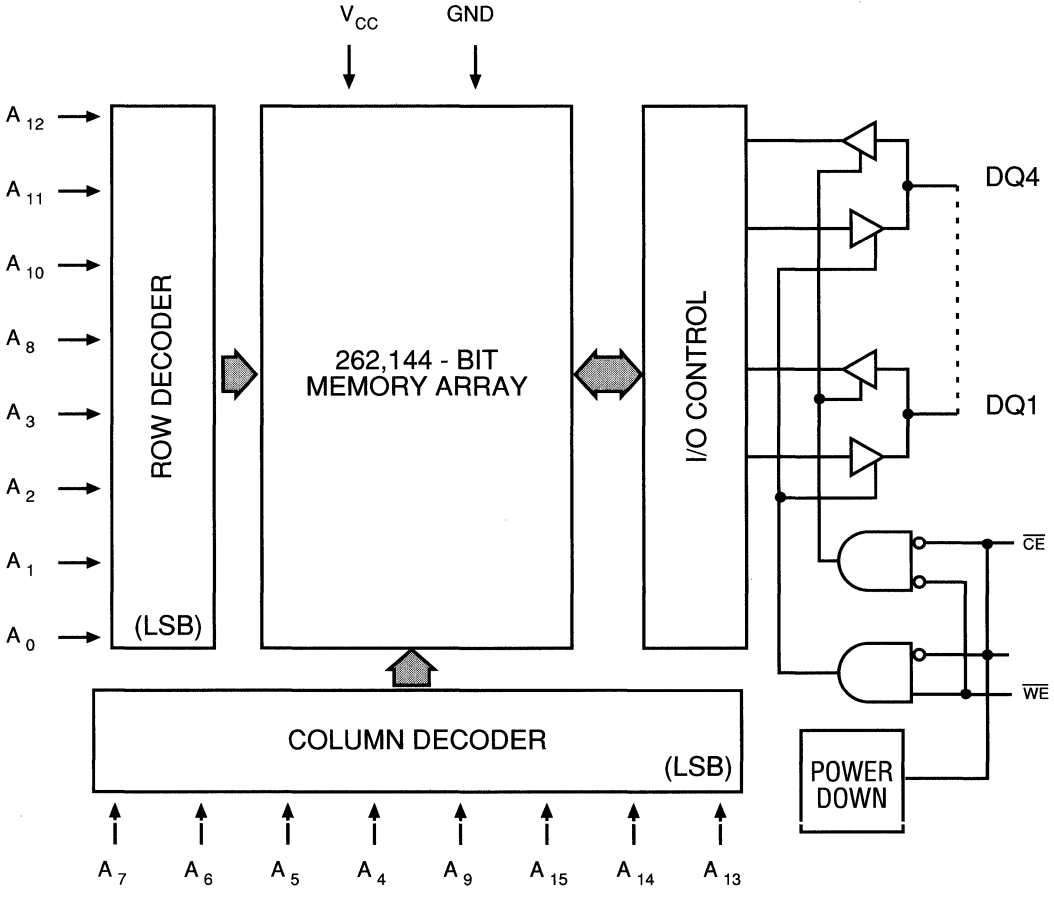
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-30	-35	-40	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	105	95	95	90	90	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	30	25	25	25	25	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	5	5	7	7	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	20		25		30		35		45		ns	
Address access time	^tAA		20		25		30		35		45	ns	
Chip Enable access time	^tACE		20		25		30		35		45	ns	
Output hold from address change	^tOH	3		5		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	6		6		6		6		6		ns	
Chip Disable to output in High-Z	^tHZCE		9		9		12		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip Disable to power-down time	^tPD		20		25		30		35		45	ns	
WRITE Cycle													
WRITE cycle time	^tWC	20		20		25		30		35		ns	
Chip Enable to end of write	^tCW	15		15		18		20		25		ns	
Address valid to end of write	^tAW	15		15		18		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
Write pulse width	^tWP	15		15		18		20		25		ns	
Data setup time	^tDS	10		10		12		15		20		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	5		5		5		5		5		ns	
Write Enable to output in High-Z	^tHZWE		10		10		12		15		18	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

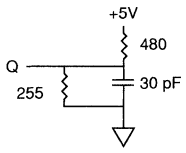


Fig. 1 OUTPUT LOAD EQUIVALENT

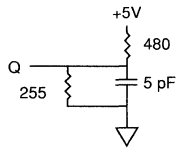


Fig. 2 OUTPUT LOAD EQUIVALENT

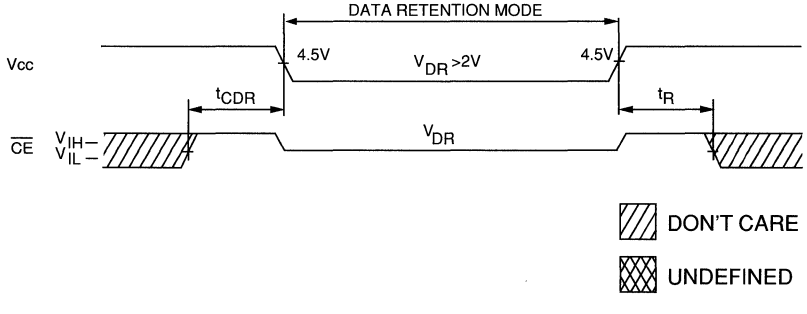
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-169.

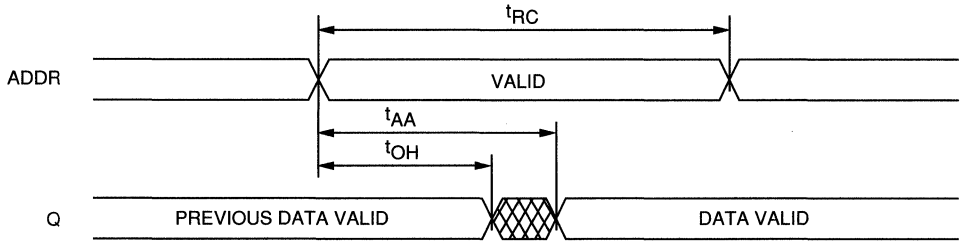
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	I_{CCDR}		95	300	µA	
		Vcc = 3v			350	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

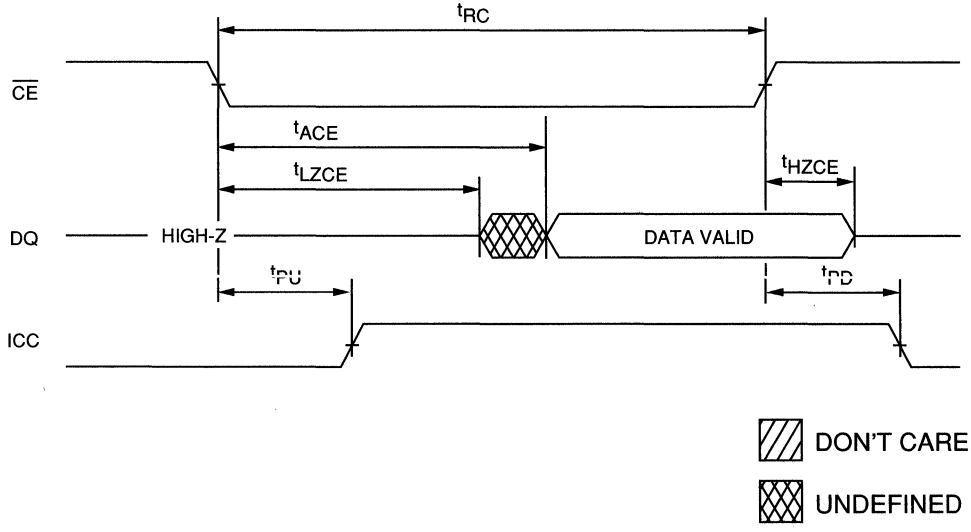
LOW Vcc DATA RETENTION WAVEFORM



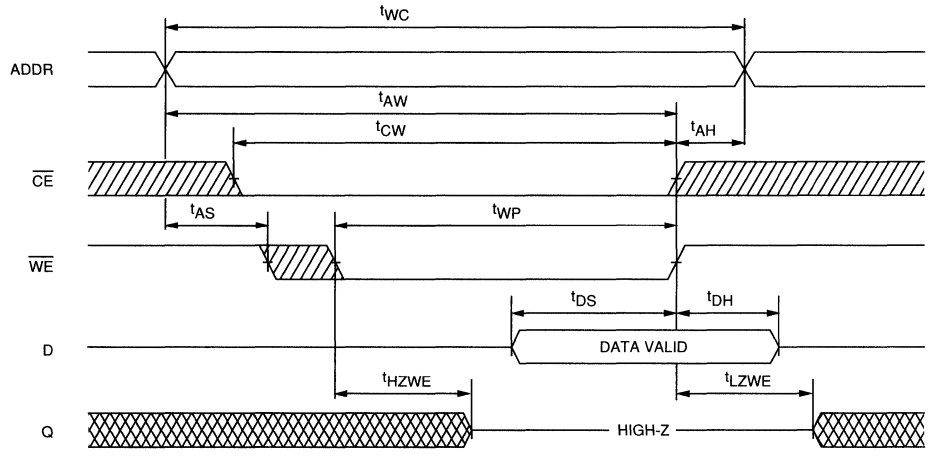
READ CYCLE NO. 1 [8, 9]



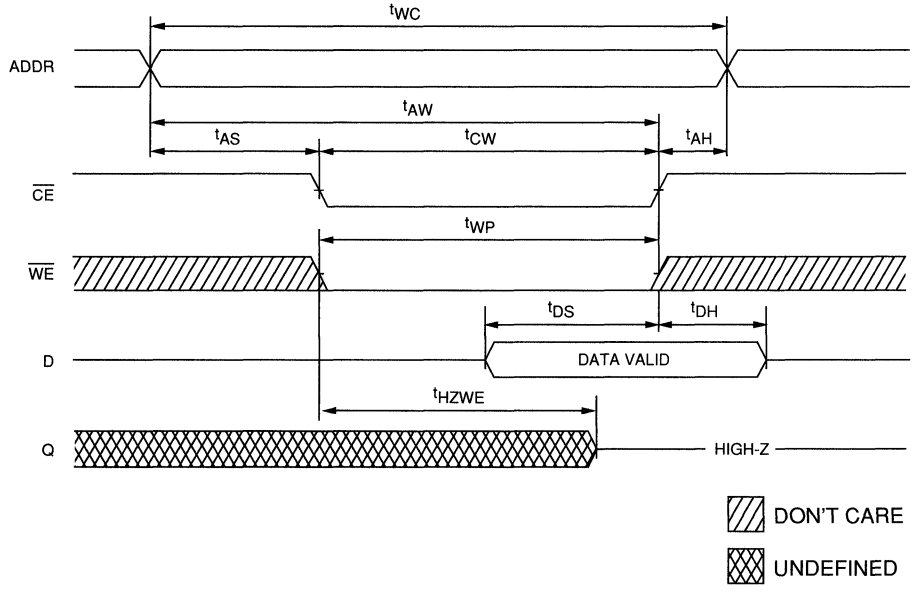
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [12]



SRAM

64K x 4 SRAM

WITH OUTPUT ENABLE

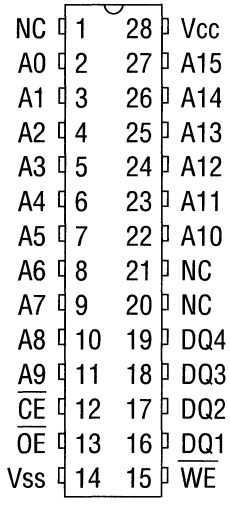
FEATURES

- High speed: 20, 25, 30, 35, and 45ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

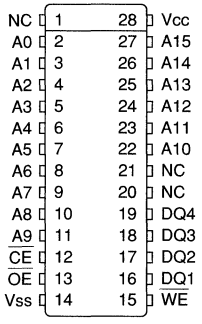
OPTIONS	MARKING
• Timing	
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

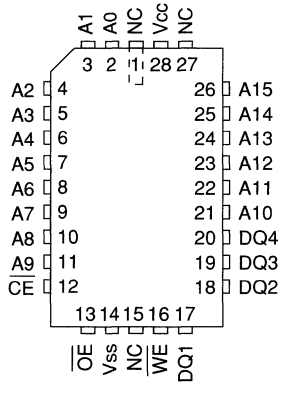
28L/300 DIP
(A-9, B-9)



28L/300 SOJ
(E-8)



28L/LCC
(F-4)



GENERAL DESCRIPTION

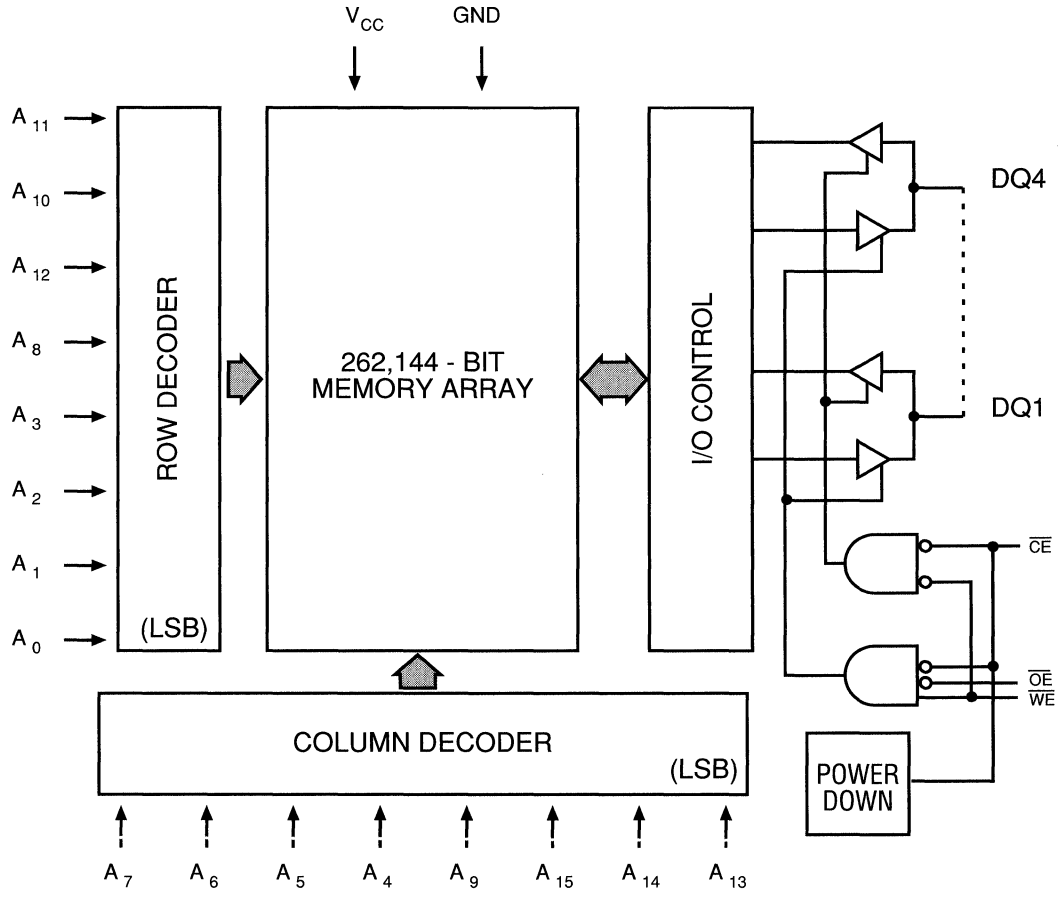
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) on this organization. These enhancements can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-30	-35	-40	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	105	95	95	90	90	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	30	25	25	25	25	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	5	5	7	7	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	tRC	20		25		30		35		45		ns	
Address access time	tAA		20		25		30		35		45	ns	
Chip Enable access time	tACE		20		25		30		35		45	ns	
Output hold from address change	tOH	3		5		5		5		5		ns	
Chip Enable to output in Low-Z	tLZCE	6		6		6		6		6		ns	
Chip Disable to output in High-Z	tHZCE		9		9		12		15		18	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		ns	
Chip Disable to power-down time	tPD		20		25		30		35		45	ns	
Output Enable access time	tAOE		8		8		10		12		15	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		0		ns	
Output Disable to out put in High-Z	tHZOE		7		7		10		12		15	ns	
WRITE Cycle													
WRITE cycle time	tWC	20		20		25		30		35		ns	
Chip Enable to end of write	tCW	15		15		18		20		25		ns	
Address valid to end of write	tAW	15		15		18		20		25		ns	
Address setup time	tAS	0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		ns	
Write pulse width	tWP	15		15		18		20		25		ns	
Data setup time	tDS	10		10		12		15		20		ns	
Data hold time	tDH	0		0		0		0		0		ns	
Write Disable to output in Low-Z	tLZWE	5		5		5		5		5		ns	
Write Enable to output in High-Z	tHZWE		10		10		12		15		18	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

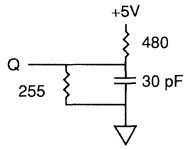


Fig. 1 OUTPUT LOAD EQUIVALENT

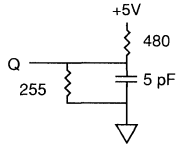


Fig. 2 OUTPUT LOAD EQUIVALENT

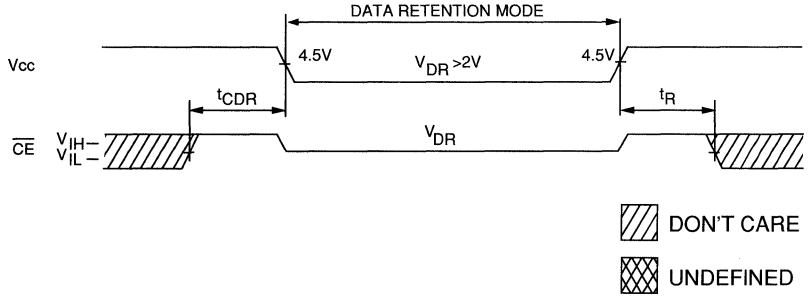
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-169.

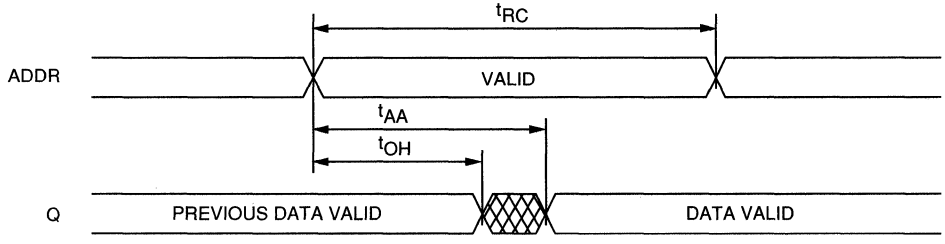
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	300	µA	
		Vcc = 3v			350	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

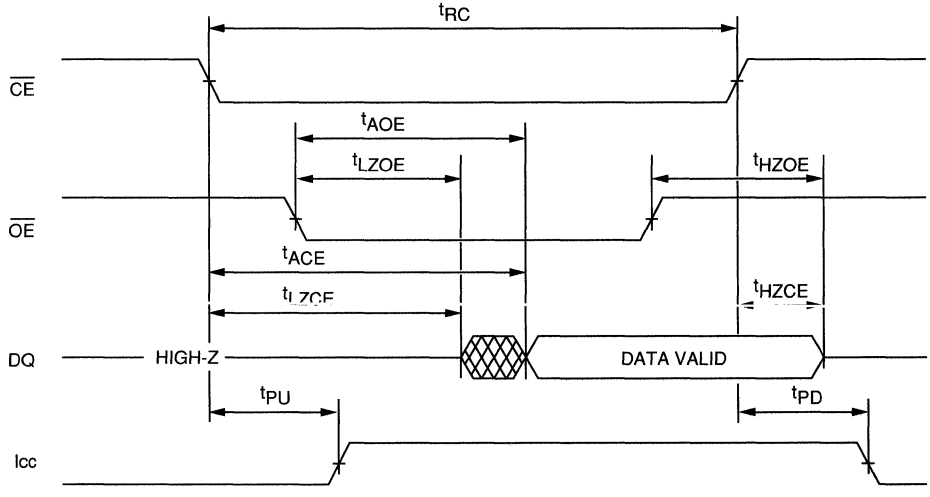
LOW Vcc DATA RETENTION WAVEFORM



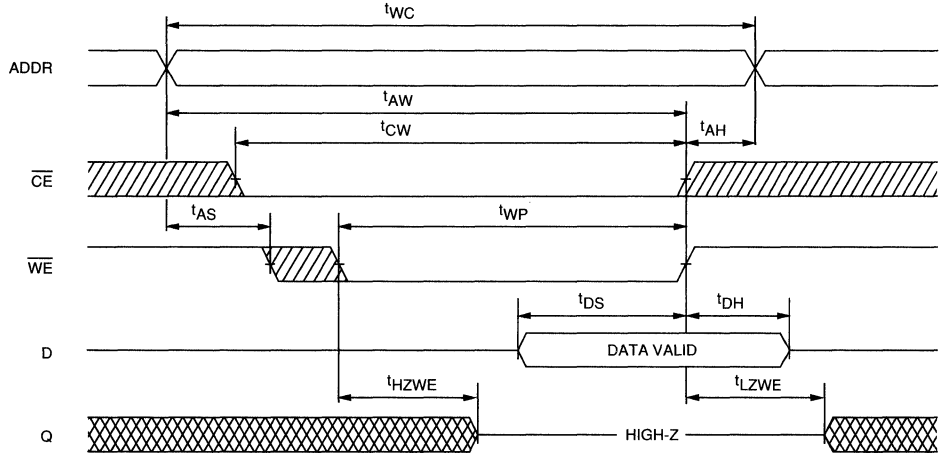
READ CYCLE NO. 1 [8, 9]



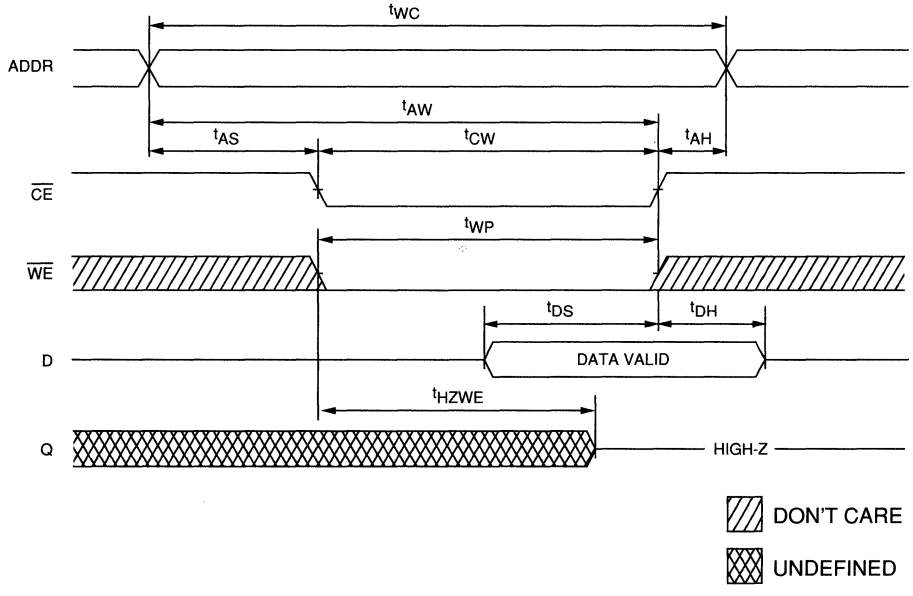
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [12]



SRAM

256K x 4 SRAM
WITH OUTPUT ENABLE

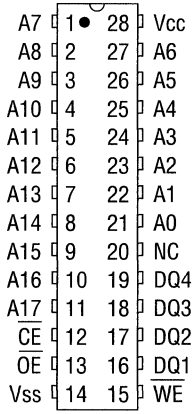
FEATURES
- High speed: 25, 35, and 45ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast Output Enable access time: 8ns

OPTIONS — MARKING

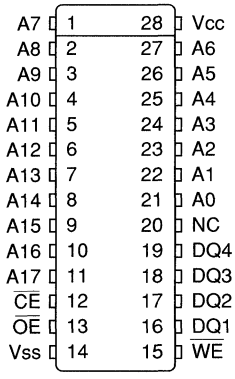
• Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (400 mil)	None
Ceramic DIP (400mil)	C
Plastic SOJ (400 mil)	DJ
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

28L/400 DIP
(A-10)



28L/400 SOJ
(E-9)



GENERAL DESCRIPTION

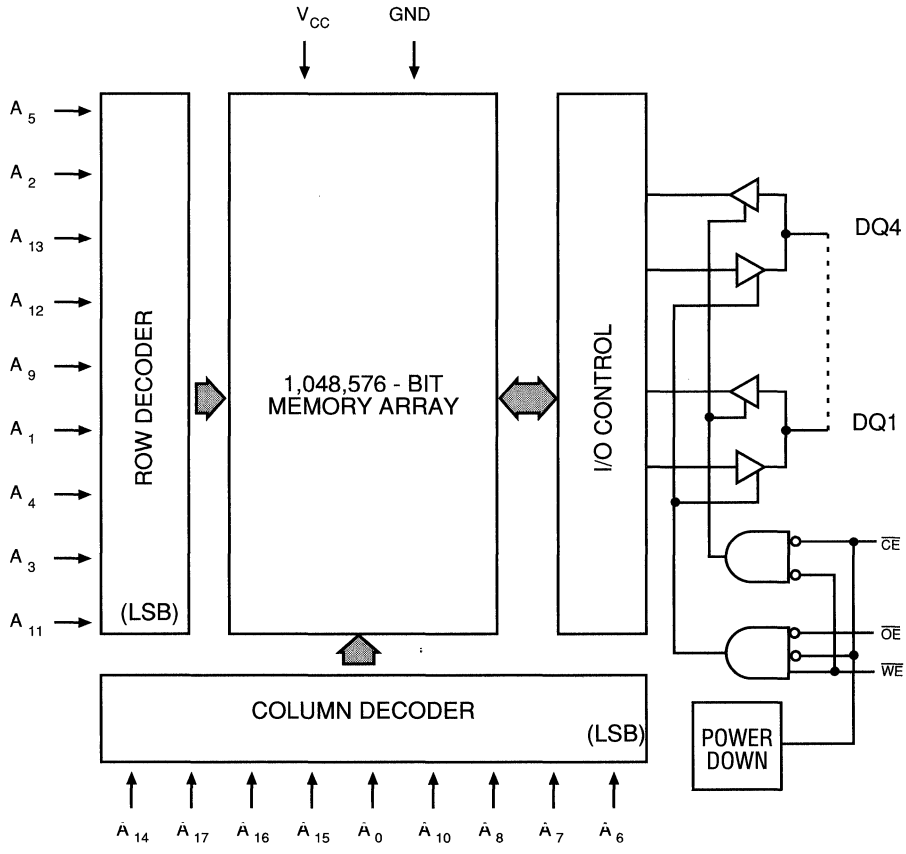
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A11 and A3) are encoded using a gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}		120	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}		30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}		7	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	25		35		45		ns	
Address access time	^tAA		25		35		45	ns	
Chip Enable access time	^tACE		25		35		45	ns	
Output hold from address change	^tOH	5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	
Chip Disable to output in High-Z	^tHZCE		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip Disable to power-down time	^tPD		25		35		45	ns	
Output Enable access time	^tAOE		8		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output Disable to output in High-Z	^tHZOE		10		12		15	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	25		35		45		ns	
Chip Enable to end of write	^tCW	15		20		25		ns	
Address valid to end of write	^tAW	15		20		25		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
Write pulse width	^tWP	15		20		25		ns	
Data setup time	^tDS	10		15		20		ns	
Data hold time	^tDH	0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	0		0		0		ns	
Write Enable to output in High-Z	^tHZWE	0	10	0	15	0	18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

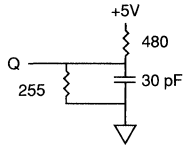


Fig. 1 OUTPUT LOAD EQUIVALENT

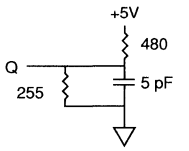


Fig. 2 OUTPUT LOAD EQUIVALENT

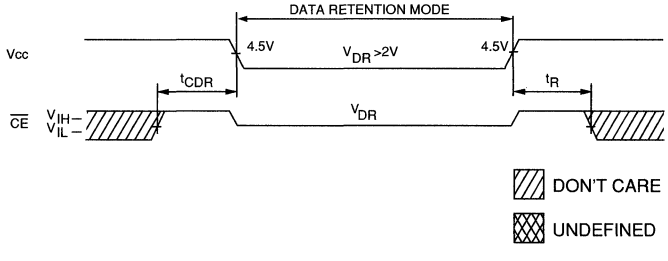
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enable held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-171.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

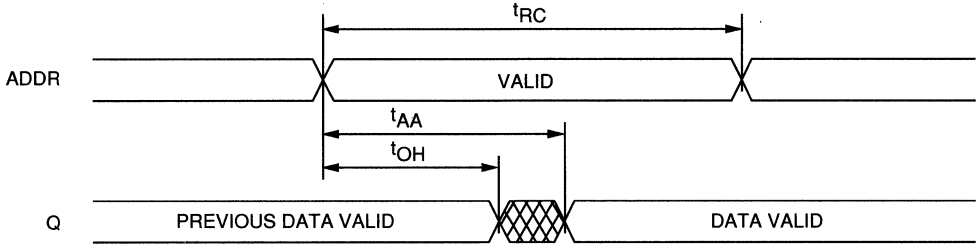
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	500	µA	
		Vcc = 3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

LOW Vcc DATA RETENTION WAVEFORM

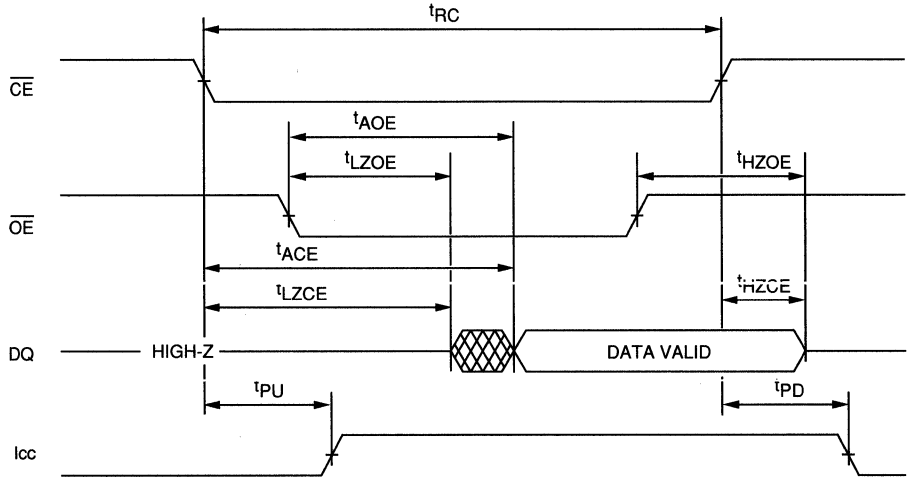


FAST SRAM

READ CYCLE NO. 1 [8, 9]



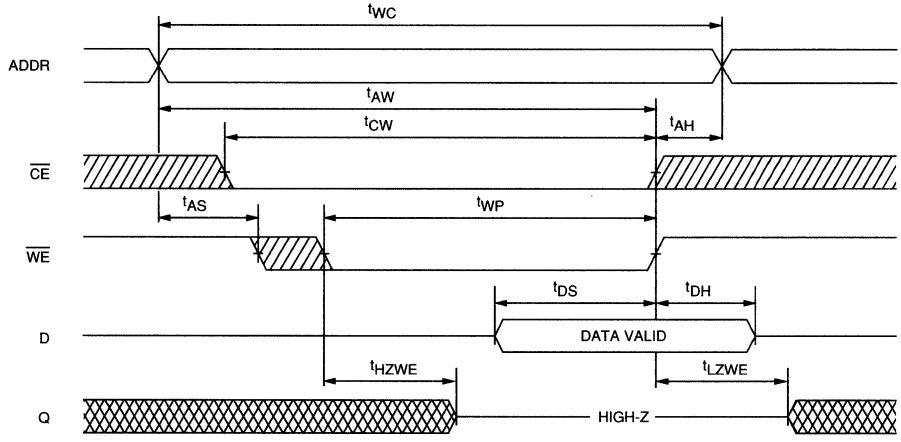
READ CYCLE NO. 2 [7, 8, 10]



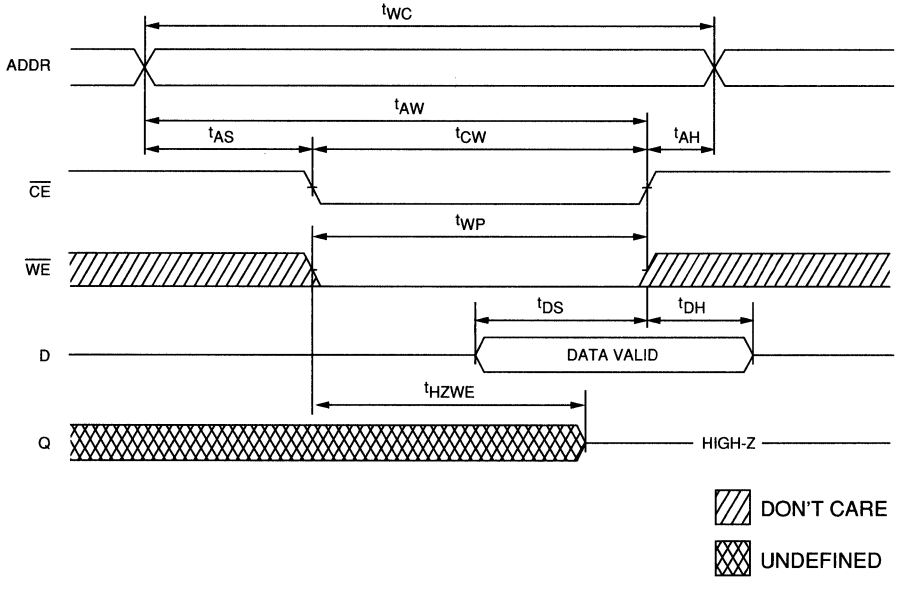
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled) [12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [12]



SRAM

2K x 8 SRAM

FEATURES

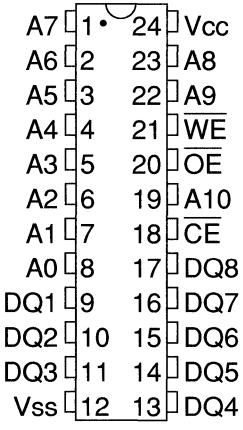
- High speed: 12, 15, 20, 25, 30 and 35ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

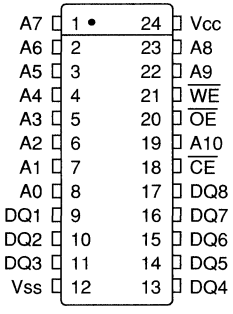
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

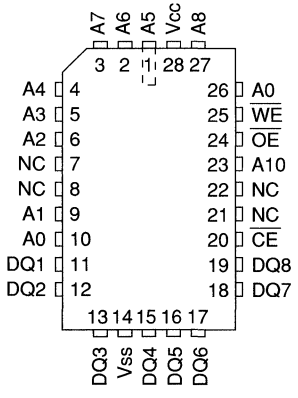
24L/300DIP
(A-7, B-7)



24L/300 SOJ
(E-4)



28L/LCC
(F-4)



GENERAL DESCRIPTION

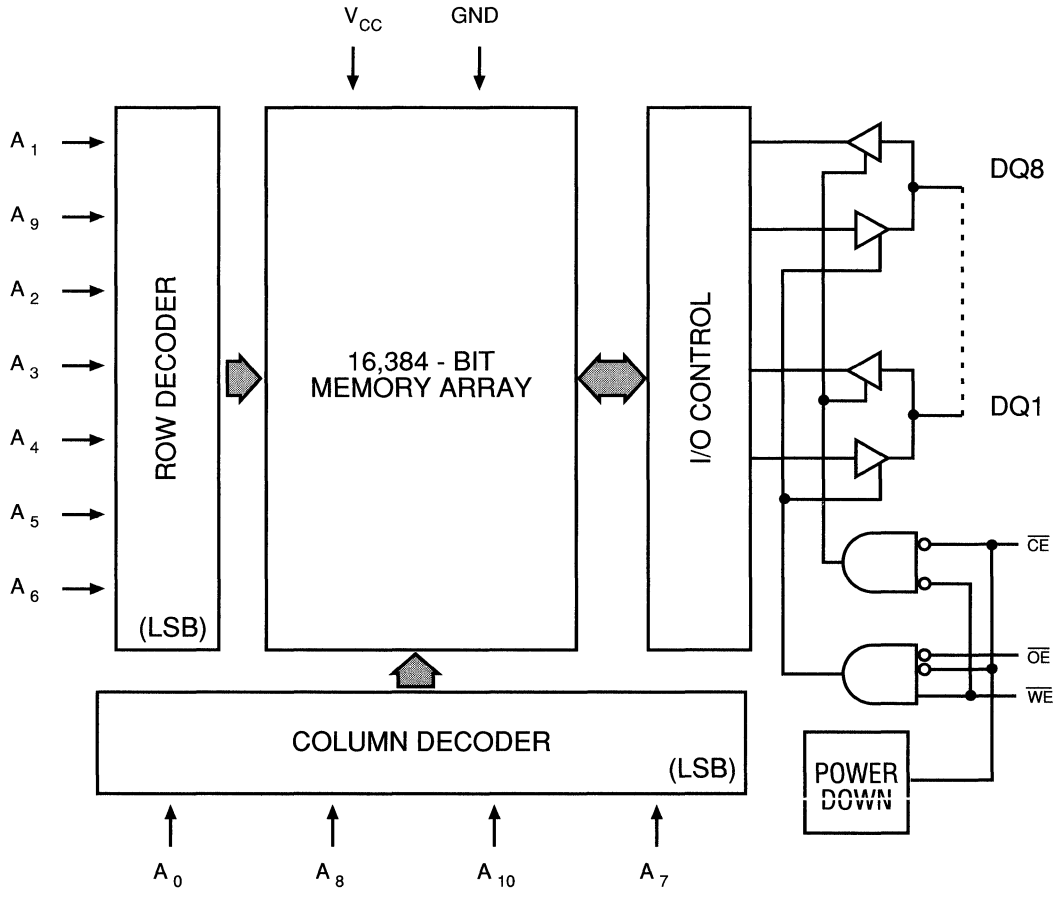
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} .....-1.0V to +7.0V
Storage Temperature (Ceramic) .....-65°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	140	125	110	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	50	45	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	3	3	3	3	3	3	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip Enable access time	t_{ACE}		11		12		15		20		25		30	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	t_{HZCE}		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		0		ns	
Chip Disable to power-down time	t_{PD}		12		15		20		25		30		35	ns	
Output Enable access time	t_{AOE}		7		7		9		10		15		20	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		0		0		ns	
Output Disable to output in High-Z	t_{HZOE}		6		6		10		10		15		20	ns	6
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip Enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address setup time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data setup time	t_{DS}	7		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	t_{HZWE}		6		6		8		10		12		15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

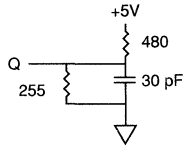


Fig. 1 OUTPUT LOAD EQUIVALENT

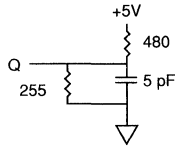


Fig. 2 OUTPUT LOAD EQUIVALENT

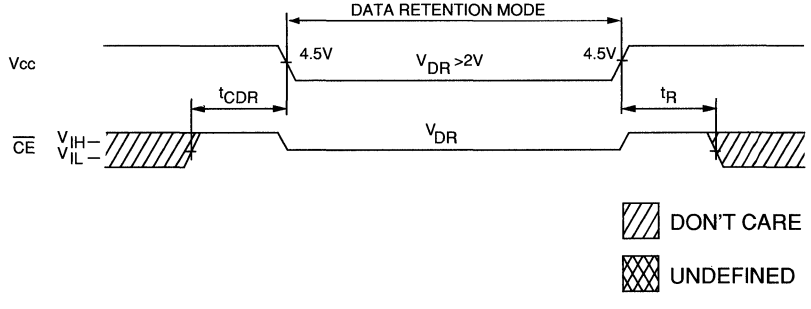
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-165.

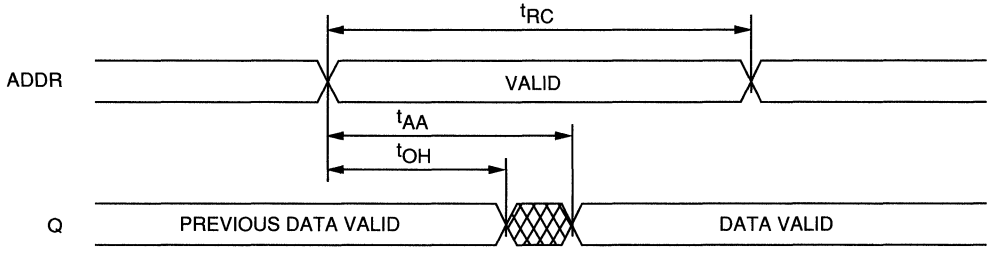
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	250	µA	
		Vcc = 3v			300	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

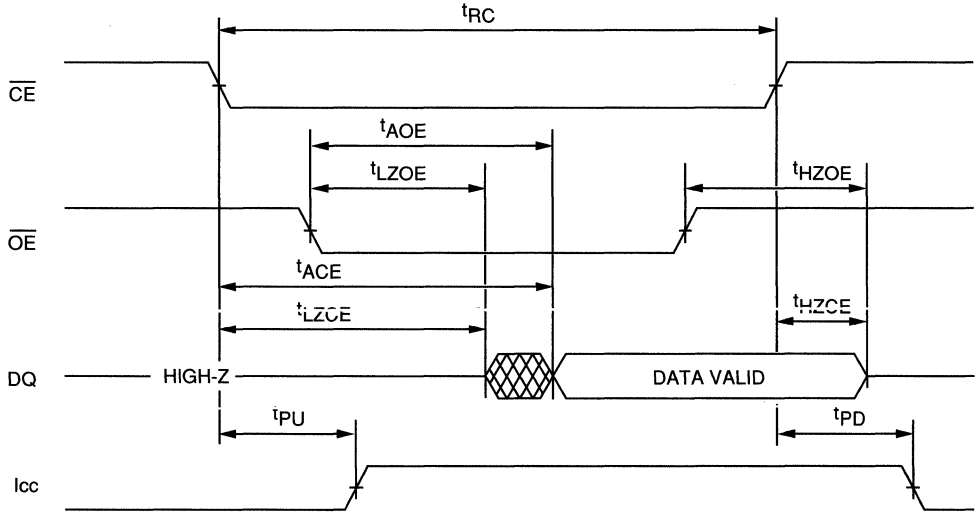
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10]

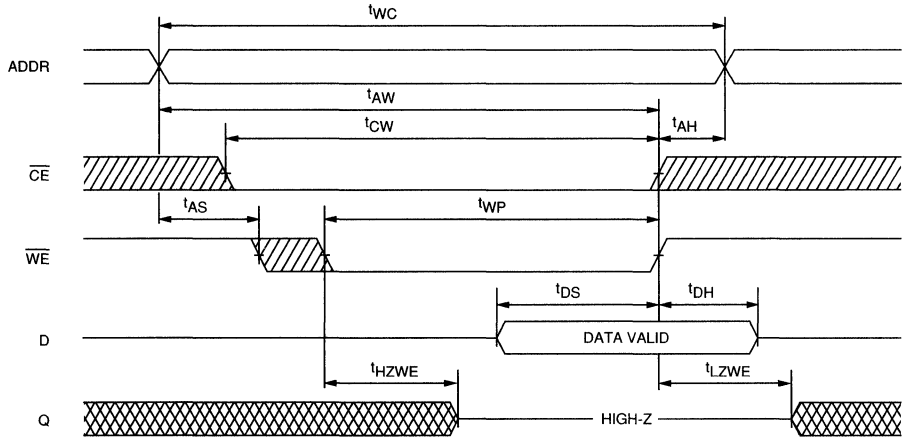


DON'T CARE

UNDEFINED

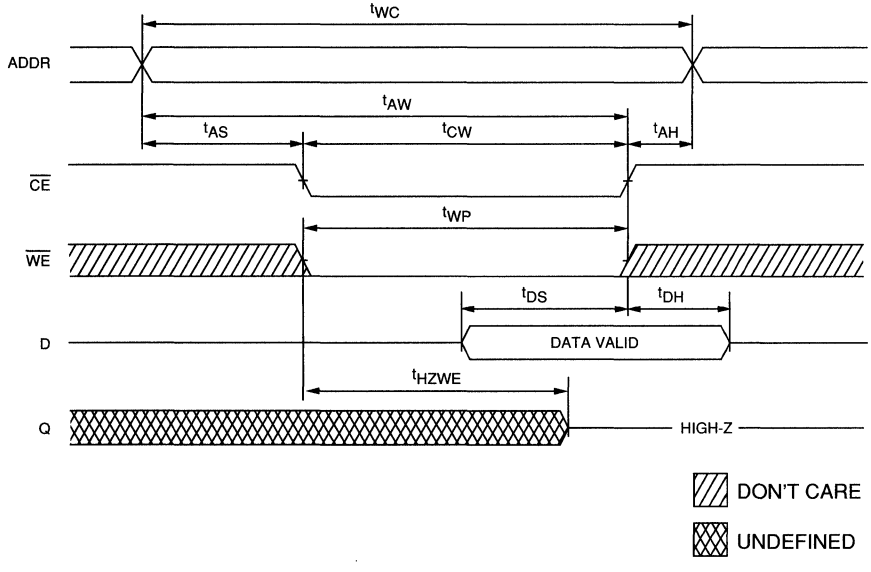
WRITE CYCLE NO. 1

(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2

(Chip Enable Controlled) [12]



SRAM

8K x 8 SRAM

FEATURES

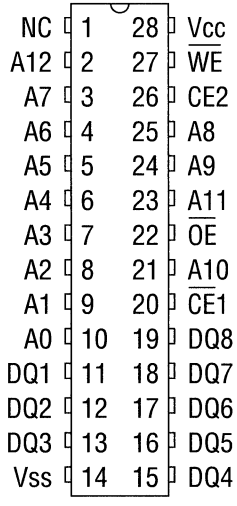
- High speed: 12, 15, 20, 25, 30 and 35ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$1, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

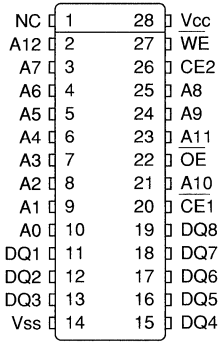
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
Ceramic LCC (32 pin)	ECW
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

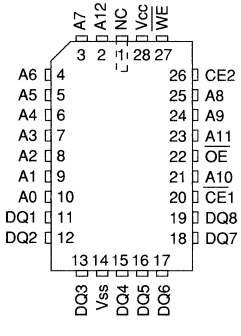
28L/300 DIP
(A-9, B-9)



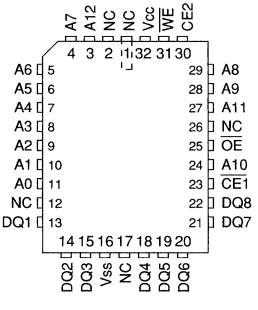
28L/300 SOJ
(E-8)



28L/LCC
(F-4)



32L/LCC
(F-6)



GENERAL DESCRIPTION

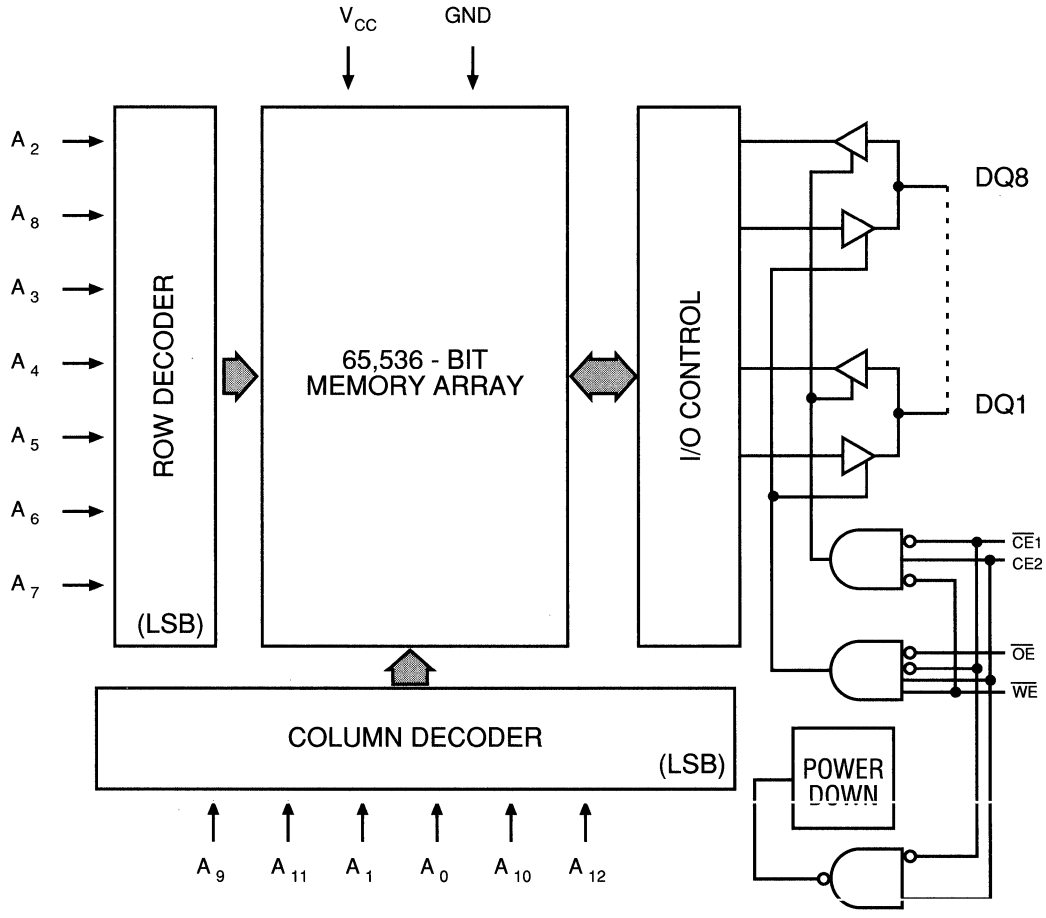
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers two chip enables on the x8 organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	DQ OPERATION	POWER
STANDBY	H	X	X	X	HIGH-Z	STANDBY
STANDBY	X	L	X	X	HIGH-Z	STANDBY
READ	L	H	H	L	Q	ACTIVE
READ	L	H	H	H	HIGH-Z	ACTIVE
WRITE	L	H	L	X	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	60	50	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip Enable access time	^tACE		12		12		15		20		25		30	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	^tHZCE		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip Disable to power-down time	^tPD		12		15		20		25		30		35	ns	
Output Enable access time	^tAOE		7		7		9		10		15		20	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output Disable to output in High-Z	^tHZOE		6		6		10		10		15		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip Enable to end of write	^tCW	10		12		15		20		25		25		ns	
Address valid to end of write	^tAW	12		12		15		20		25		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data setup time	^tDS	8		8		10		10		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^tHZWE		6		6		8		10		12		15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

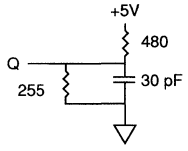


Fig. 1 OUTPUT LOAD EQUIVALENT

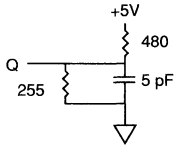


Fig. 2 OUTPUT LOAD EQUIVALENT

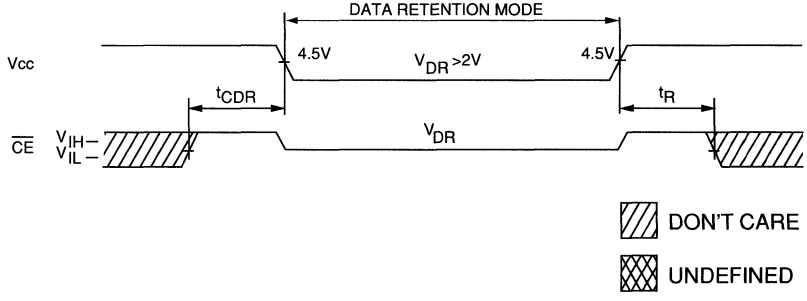
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-167.

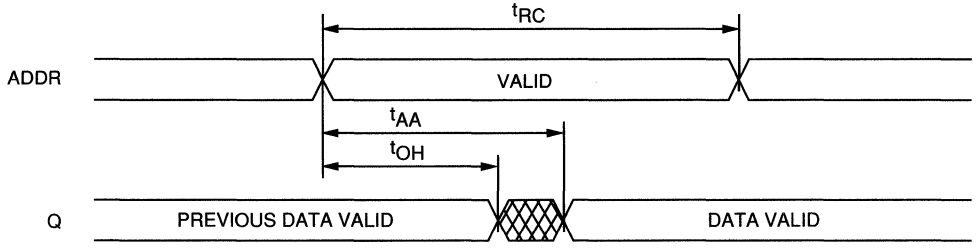
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	250	µA	
		Vcc = 3v			300	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

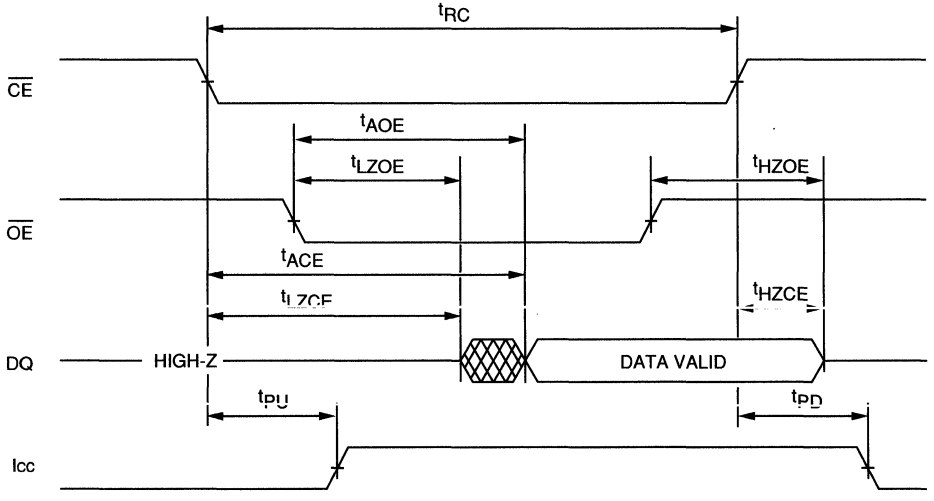
LOW Vcc DATA RETENTION WAVEFORM



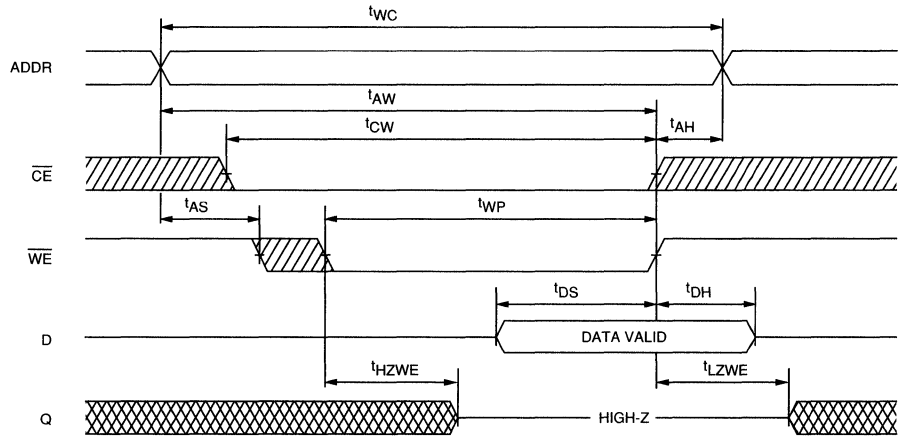
READ CYCLE NO. 1 [8, 9]



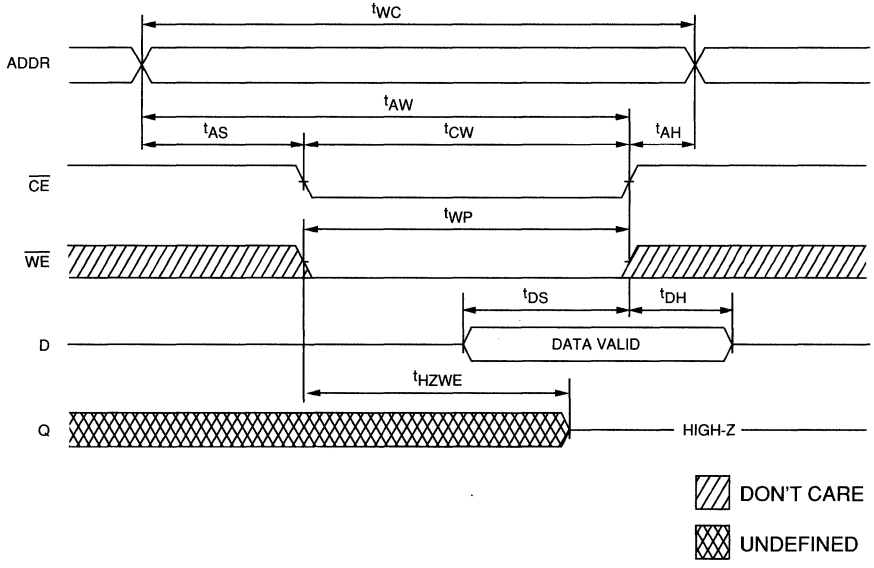
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [12]



SRAM

32K x 8 SRAM

FEATURES

- High speed: 20, 25, 30, 35, and 45ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Ceramic DIP (300 mil)	C
Ceramic DIP (600 mil)	CW
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
Ceramic LCC (32 pin)	ECW
• Two Volt Data Retention	L
• Temperature	
Industrial (-40°C to +85°C)	IT

GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

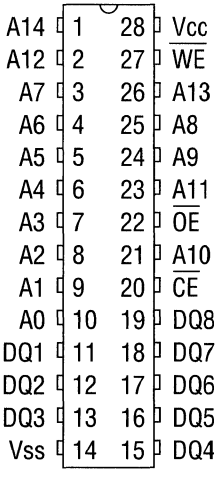
For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) on this organization. These enhancements can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

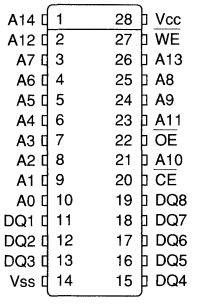
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

PIN ASSIGNMENT (Top View)

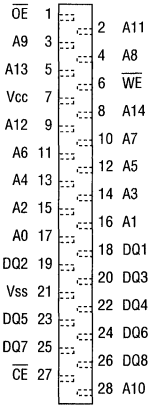
28L/300/600 DIP (A-9, A-11, B-9, B-11)



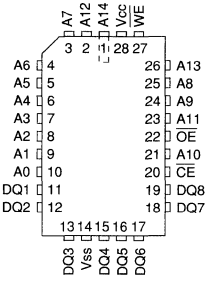
28L/300 SOJ (E-8)



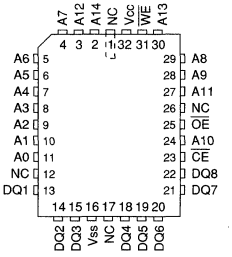
28L ZIP (C-5)



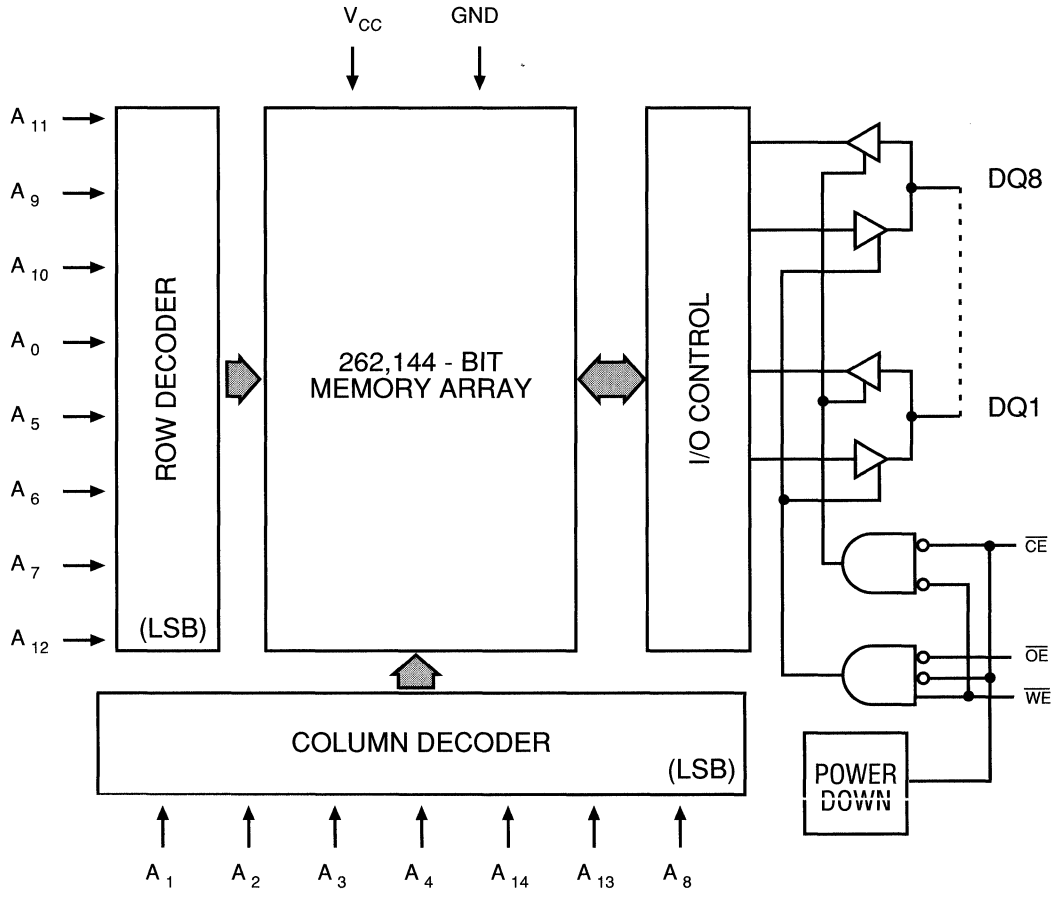
28L/LCC (F-4)



32L/LCC (F-6)



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-30	-35	-40	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	105	95	95	90	90	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	30	25	25	25	25	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	5	5	7	7	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	20		25		30		35		45		ns	
Address access time	t_{AA}		20		25		30		35		45	ns	
Chip Enable access time	t_{ACE}		20		25		30		35		45	ns	
Output hold from address change	t_{OH}	3		5		5		5		5		ns	
Chip Enable to output in Low-Z	t_{LZCE}	6		6		6		6		6		ns	
Chip Disable to output in High-Z	t_{HZCE}		9		9		12		15		18	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		ns	
Chip Disable to power-down time	t_{PD}		20		25		30		35		45	ns	
Output Enable access time	t_{AOE}		8		8		10		12		15	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		0		ns	
Output Disable to output in High-Z	t_{HZOE}		7		7		10		12		15	ns	
WRITE Cycle													
WRITE cycle time	t_{WC}	20		20		25		30		35		ns	
Chip Enable to end of write	t_{CW}	15		15		18		20		25		ns	
Address valid to end of write	t_{AW}	15		15		18		20		25		ns	
Address setup time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		ns	
Write pulse width	t_{WP}	15		15		18		20		25		ns	
Data setup time	t_{DS}	10		10		12		15		20		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write Disable to output in Low-Z	t_{LZWE}	5		5		5		5		5		ns	
Write Enable to output in High-Z	t_{HZWE}		10		10		12		15		18	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

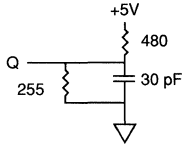


Fig. 1 OUTPUT LOAD EQUIVALENT

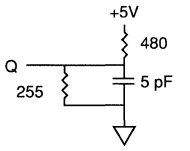


Fig. 2 OUTPUT LOAD EQUIVALENT

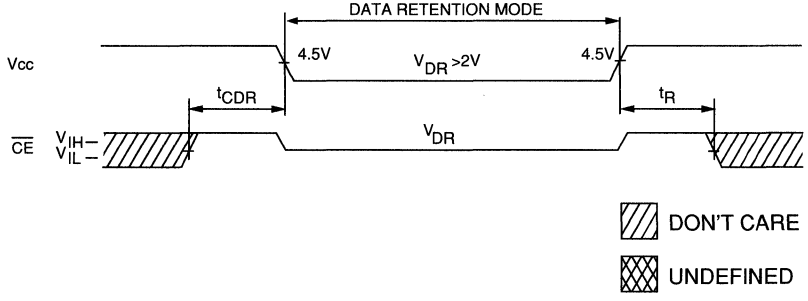
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-169.

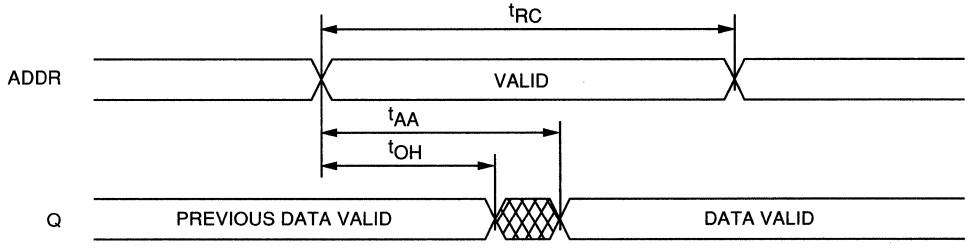
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	300	µA	
		Vcc = 3v			350	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

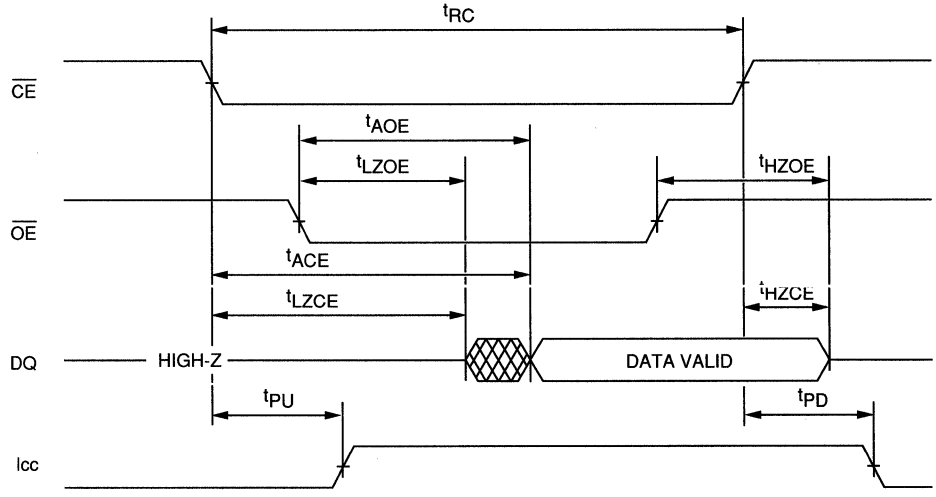
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



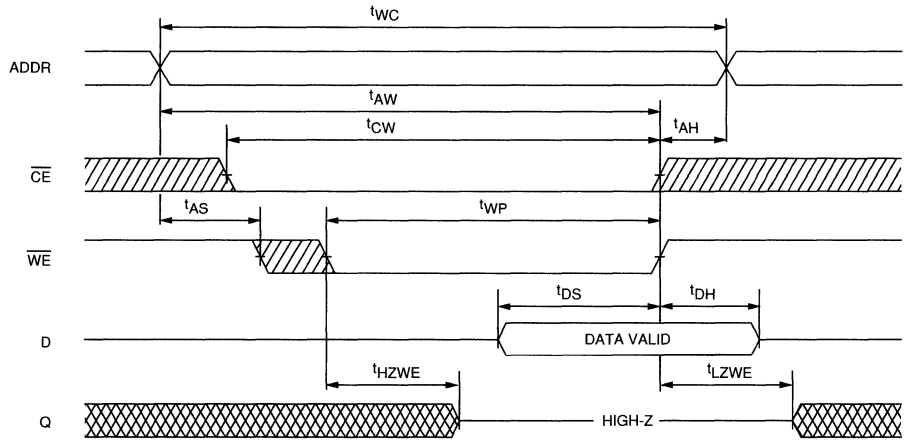
READ CYCLE NO. 2 [7, 8, 10]



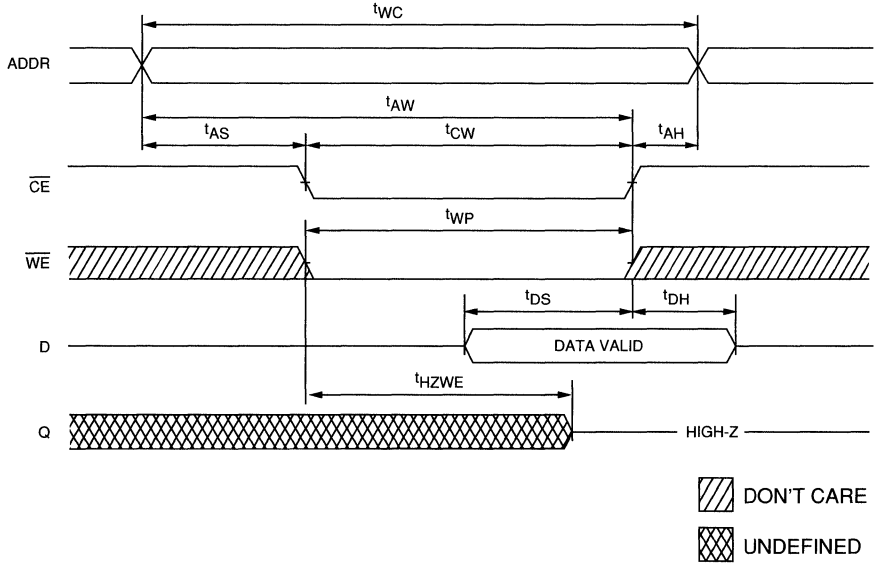
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [12]



SRAM

128K x 8 SRAM

WITH OUTPUT ENABLE

FEATURES

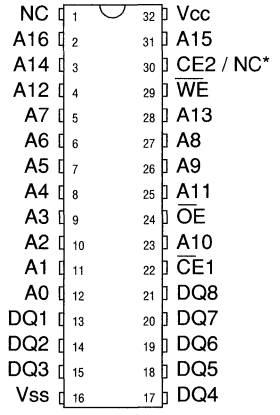
- High speed: 25, 35, and 45ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast Output Enable access time: 8ns

OPTIONS — MARKING

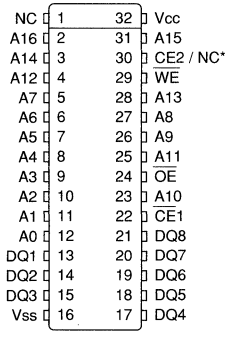
- Timing
  - 25ns access — -25
  - 35ns access — -35
  - 45ns access — -45
- Packages
  - Plastic DIP (400 mil) — None
  - Plastic DIP (600 mil) — W
  - Ceramic DIP (400 mil) — C
  - Ceramic DIP (600 mil) — CW
  - Plastic SOJ (400 mil) — DJ
  - Ceramic LCC (32 pin) — EC
- Two Volt Data Retention — L

PIN ASSIGNMENT (Top View)

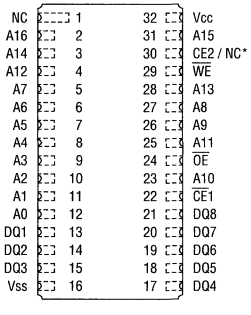
32L/400/600 DIP (A-12, A-13, B-12, B-13)



32L/400 SOJ (E-11)



32L/LCC (F-8)



*Contact factory for no-connect (NC) option on pin 30

GENERAL DESCRIPTION

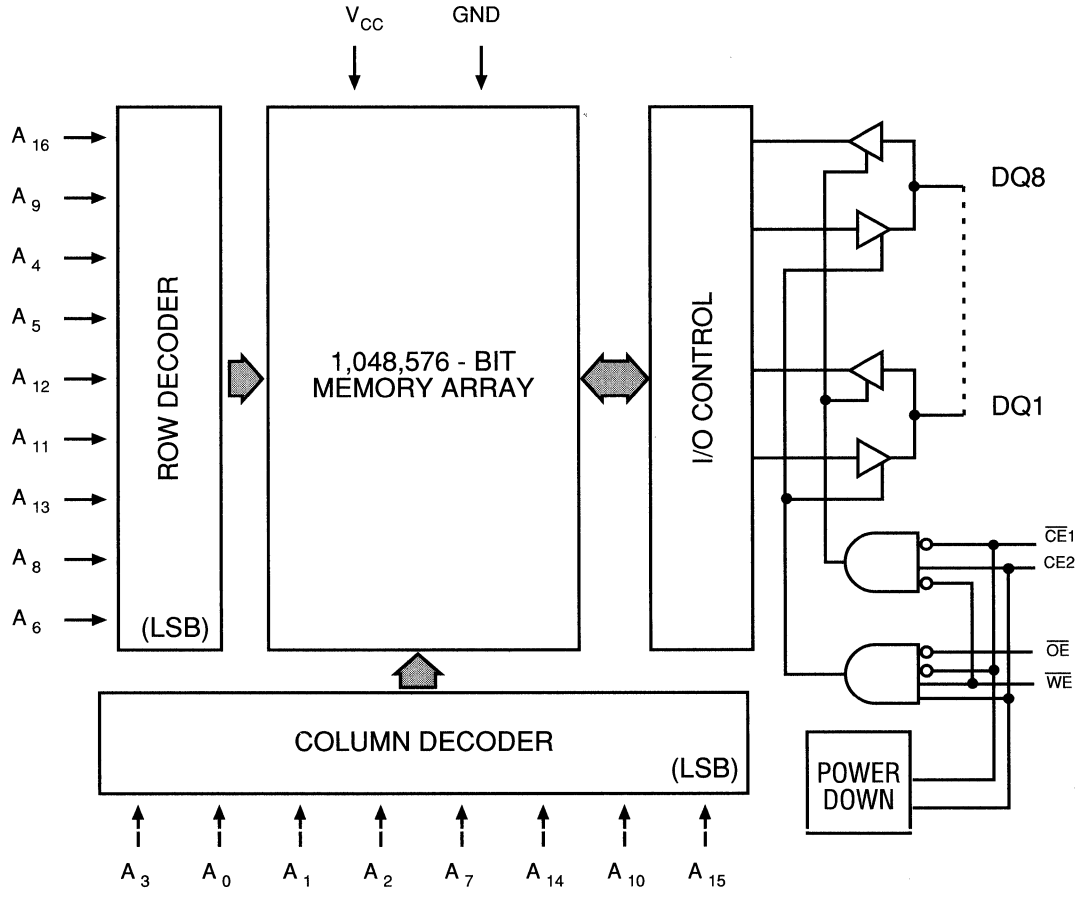
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2). This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A8 and A6) are encoded using a gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
READ	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}		120	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}		30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}		7	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 14) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	25		35		45		ns	
Address access time	^tAA		25		35		45	ns	
Chip Enable access time	^tACE		25		35		45	ns	
Output hold from address change	^tOH	5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	
Chip Disable to output in High-Z	^tHZCE		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip Disable to power-down time	^tPD		25		35		45	ns	
Output Enable access time	^tAOE		8		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output Disable to output in High-Z	^tHZOE		10		12		15	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	25		35		45		ns	
Chip Enable to end of write	^tCW	15		20		25		ns	
Address valid to end of write	^tAW	15		20		25		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
Write pulse width	^tWP	15		20		25		ns	
Data setup time	^tDS	10		15		20		ns	
Data hold time	^tDH	0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	0		0		0		ns	
Write Enable to output in High-Z	^tHZWE	0	10	0	15	0	18	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

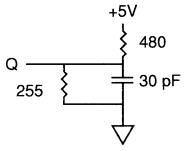


Fig. 1 OUTPUT LOAD EQUIVALENT

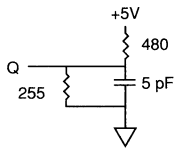


Fig. 2 OUTPUT LOAD EQUIVALENT

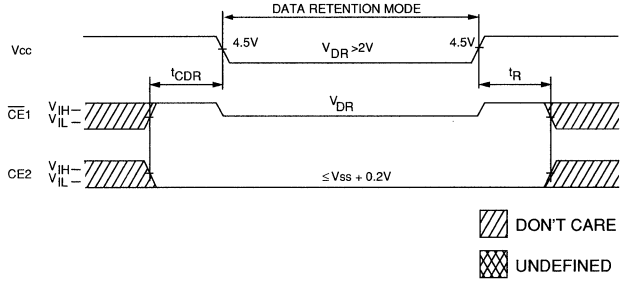
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enable held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 timing is the same as $\overline{CE1}$ timing. The wave form is inverted.
13. Chip enable ($\overline{CE1}$, CE2) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
14. For automotive, industrial and extended temperature specifications refer to page 4-171.

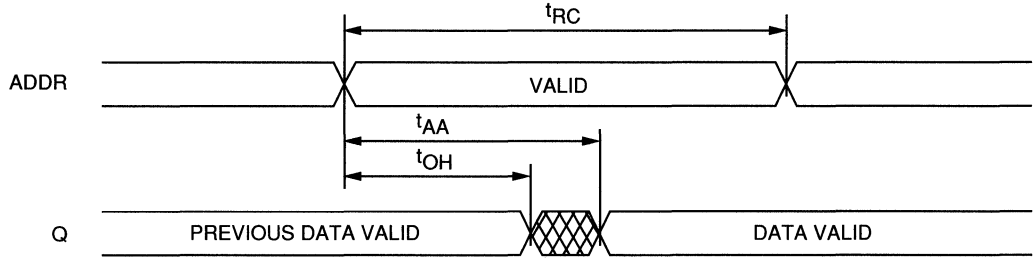
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE1}$ ≥ (Vcc -0.2V) or CE2 ≤ (Vss +0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	500	µA	
		Vcc = 3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

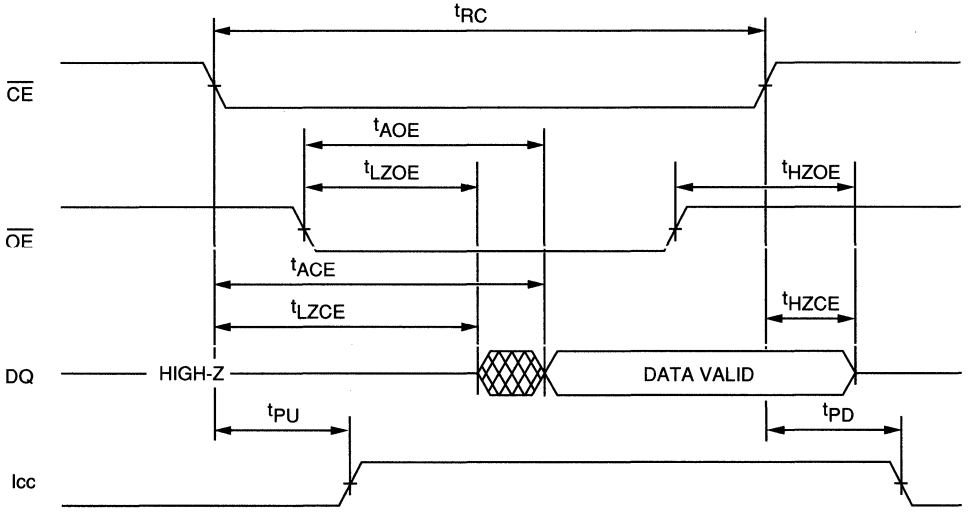
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10, 12]

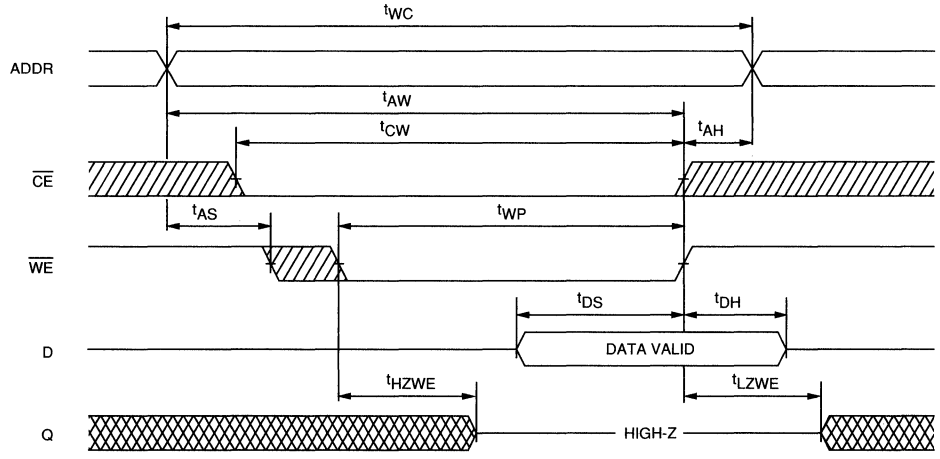


DON'T CARE

UNDEFINED

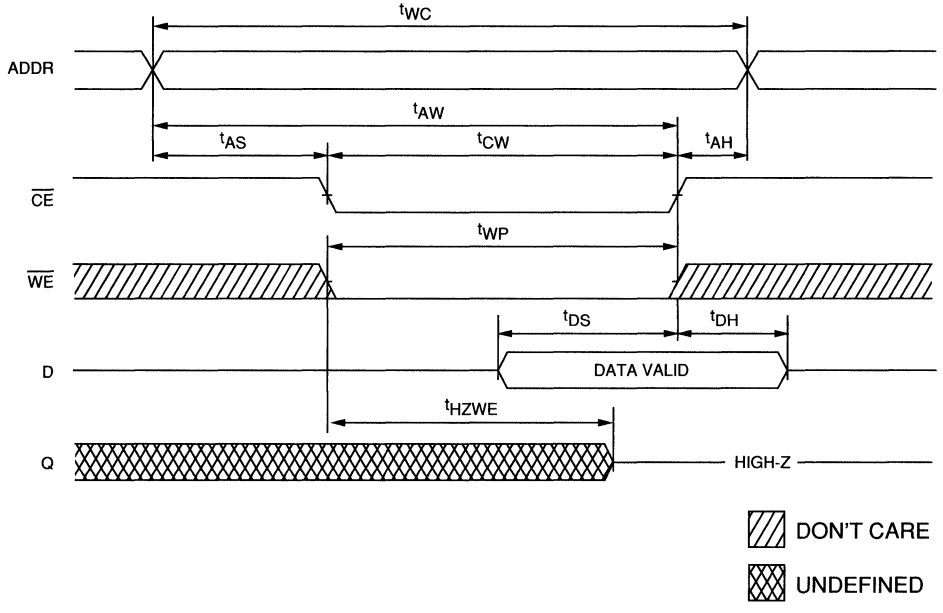
WRITE CYCLE NO. 1

(Write Enable Controlled) [7, 12, 13]



WRITE CYCLE NO. 2

(Chip Enable Controlled) [12, 13]



SRAM

16K x 16 SRAM

WITH ADDRESS / DATA INPUT LATCHES

FEATURES

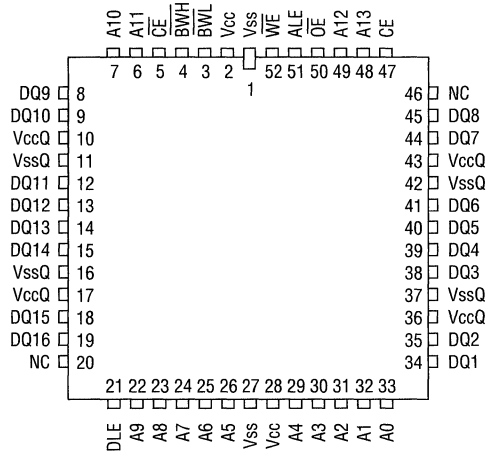
- Fast access times: 15, 17, 20 and 25ns
- Fast output enable: 6, 8 and 10ns
- Single +5V (±10%) power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Optional +3.3V (±10%) output buffer operation
- Separate Data Input Latch
- Common Data Inputs and Data Outputs
- BYTE WRITE capability via Dual Write Strobes
- Address and Chip Enable input latches

OPTIONS

	MARKING
• Timing	
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG
• Density	
16K x 16	MT5C2516

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT5C2516 SRAM integrates a 16K x 16 SRAM core with advanced peripheral circuitry consisting of address and data input latches, latched active HIGH and active LOW chip enables, separate upper and lower byte write strobes and a fast output enable. The device is ideally suited for "pipelined" systems and systems that benefit from a wide data bus.

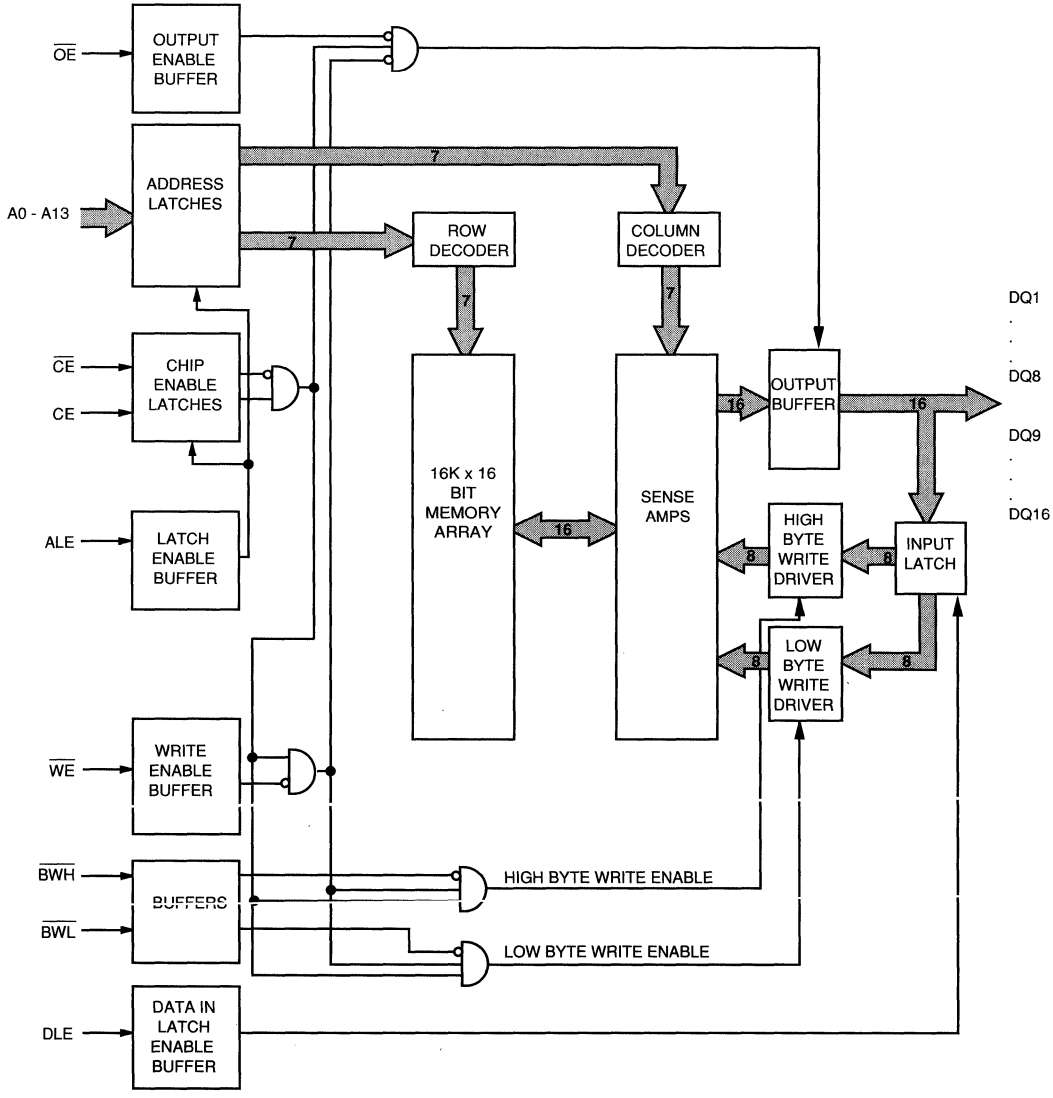
Address and chip enable latches are provided. When address latch enable (ALE) is HIGH, the address and chip enable latches are transparent, allowing the input to flow through the latch. If ALE is LOW, the address and chip enable latch inputs are disabled. This input latch simplifies READ and WRITE cycles by guaranteeing address hold time in a simple fashion.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) allow individual bytes to be written. $\overline{BWL}$ controls DQ1-DQ8 the lower bits. While $\overline{BWH}$ controls DQ9-DQ16 the upper bits.

A data input latch is provided. When data latch enable (DLE) is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, the data latch inputs are disabled. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT5C2516 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided to allow either +3.3V or +5V TTL operation of the output drivers.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC and PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are either latched or unlatched depending on the state of ALE.
52	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
51	ALE	Input	Address Latch Enable: This signal latches the address, CE, and $\overline{CE}$ inputs on its falling edge. When ALE is HIGH, the latch is transparent.
3, 4	$\overline{BWL}$, $\overline{BWH}$	Input	Byte Write Enables: These active LOW inputs allow individual bytes to be written. When $\overline{BWL}$ is LOW, data is written to the lower byte, D1-D8. When $\overline{BWH}$ is LOW, data is written to the upper byte, D9-D16. When both $\overline{BWH}$ and $\overline{BWL}$ are HIGH and meet the required setup time to the falling edge of $\overline{WE}$, then the WRITE cycle is aborted.
5, 47	$\overline{CE}$,CE	Input	Chip Enables: These signals are used to enable the device. Both active HIGH (CE) and active LOW ($\overline{CE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the data latch is transparent. Input data is latched into the on-chip data latch on the falling edge of DLE.
20, 46	NC	Input/ Output	Parity Data I/O: These signals are no connects (NC). No connects are not internally bonded.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. When data is latched, DQ1-DQ16 must meet the required setup and hold times around DLE.
2, 28	Vcc	Supply	Power Supply: +5V ± 10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ± 10% or 3.3V ± 10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1,27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	CE	$\overline{CE}$	$\overline{WE}$	$\overline{BWL}$	$\overline{BWH}$	ALE	DLE	$\overline{OE}$	DQ
Deselected cycle	L	X	X	X	X	X	X	X	High-Z
Deselected	X	H	X	X	X	X	X	X	High-Z
READ	H	L	H	X	X	H	X	H	High-Z
READ	H	L	H	X	X	H	X	L	Q1-Q16
LATCHED READ	H	L	H	X	X	L	X	L	Q1-Q16
WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	H	H	X	D1-D16
LATCHED WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	L	H	X	D1-D16
WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	H	L	X	D1-D16
LATCHED WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	L	L	X	D1-D16
ABORTED WRITE	H	L	L	H	H	X	X	X	High-Z
BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	H	H	X	D1-D8
LATCHED BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	L	H	X	D1-D8
BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	H	H	X	D9-D16
LATCHED BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	L	H	X	D9-D16
BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	H	L	X	D1-D8
LATCHED BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	L	L	X	D1-D8
BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	H	L	X	D9-D16
LATCHED BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	L	L	X	D9-D16

NOTE:
1. Latched inputs (Addresses, CE, and $\overline{CE}$) must satisfy the specified setup and hold times around the falling edge of ALE. Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the ^{t}DLW time.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold times for DLE.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} supply relative to V_{SS}/V_{SSQ} ..... -1.0V to +7.0V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = V_{SSQ}$, Unless Otherwise Noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1
Output Buffer Supply Voltage	5.0V TTL Compatible	V_{CCQ}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, $CE \ge V_{IH}$; V_{CC} = MAX; Outputs Open f = MAX = 1/ ^tRC	I_{CC}	150	250	mA	3
Power Supply Current: Standby	$CE \le V_{IL}$, $\overline{CE} \ge V_{IH}$; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{SB1}	20	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2; $CE \le V_{SS}$ +0.2, V_{CC} = MAX; $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}	8	10	mA	
	$CE \le V_{IL}$; $\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = 0; Outputs Open	I_{SB3}	10	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		6	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 5V	$C_{I/O}$		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = VccQ = 5V ± 10%)

		-15		-17		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
ADDRESS LATCH											
Latch cycle time	^tLC	15		17		20		25		ns	
Latch high time	^tLEH	5		5		5		5		ns	
Address / Chip Enable setup to latch LOW	^tLS	2		2		2		2		ns	
Address / Chip Enable hold from latch LOW	^tLH	3		3		3		3		ns	
Address / Chip Enable setup to latch HIGH	^tLHS	0		0		0		0		ns	
Latch HIGH to output active (Low-Z)	^tLZL	2		2		2		2		ns	6, 7, 4
Latch HIGH to output in High-Z	^tHZL	2	7	2	7	2	7	2	10	ns	6, 7, 4
READ CYCLE											
READ cycle time	^tRC	15		17		20		25		ns	
Address access time	^tAA		15		17		20		25	ns	
Chip Enable access time	^tACE		15		17		20		25	ns	
Output hold from address change	^tOH	4		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	6, 7, 4
Chip Disable to output in High-Z	^tHZCE	2	7	2	7	2	7	2	10	ns	6, 7, 4
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip Disable to power-down time	^tPD		15		17		20		25	ns	
Output Enable access time	^tAOE		6		7		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	2		2		2		2		ns	6, 7, 4
Output Disable to output in High-Z	^tHZOE	2	6	2	7	2	8	2	10	ns	6, 7, 4
WRITE Cycle											
WRITE cycle time	^tWC	15		17		20		25		ns	
Chip Enable to end of write	^tCW	13		14		15		20		ns	
Address valid to end of write	^tAW	13		14		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
Write pulse width	^tWP	13		14		15		20		ns	
Data setup time	^tDS	6		7		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	5		5		5		5		ns	6, 7, 4
Write Enable to output in High-Z	^tHZWE	0	7	0	7	0	7	0	10	ns	6, 7, 4
Byte write enable setup time	^tBWS	6		7		8		10		ns	
Byte write enable hold time	^tBWH	2		2		2		2		ns	
Byte write disable setup time	^tBWDS	0		0		0		0		ns	
Data setup to DLE LOW	^tDLS	1		1		1		1		ns	9
Data hold from DLE LOW	^tDLH	3		3		3		3		ns	9
DLE HIGH to end of write	^tDLW	6		7		8		10		ns	8
End of write to DLE HIGH	^tWDLH	0		0		0		0		ns	9
End of write to ALE HIGH	^tWLH	0		0		0		0		ns	
ALE HIGH setup time to write enable LOW	^tLWS	0		0		0		0		ns	
ALE HIGH to end of write	^tLW	13		14		15		20		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

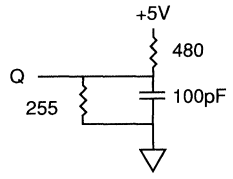


Fig. 1 OUTPUT LOAD EQUIVALENT

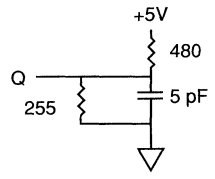
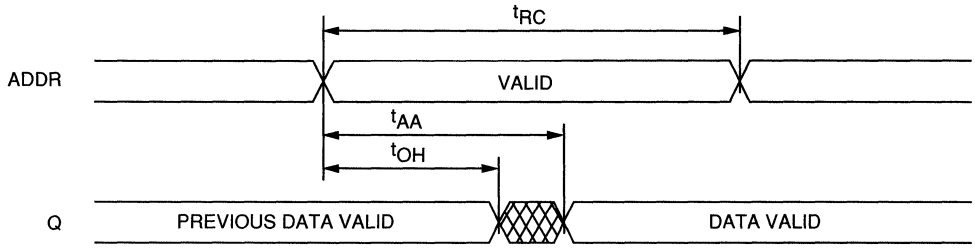


Fig. 2 OUTPUT LOAD EQUIVALENT

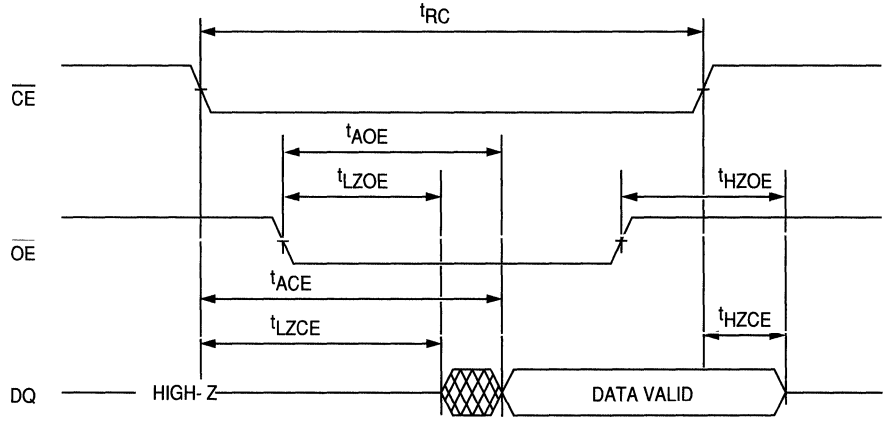
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZOE is less than ^{t}LZOE.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold time with respect to DLE.
10. Any combination of write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) can initiate and terminate a WRITE cycle.
11. $\overline{WE}$ is HIGH for READ cycle.
12. Device is continuously selected. All chip enables held in their active state.
13. Address valid prior to or coincident with the latest occurring chip enable.
14. CE timing is the same as $\overline{CE}$ timing. The wave form is inverted.

READ CYCLE NO. 1 [11, 12]



READ CYCLE NO. 2 [7, 11, 13, 14]

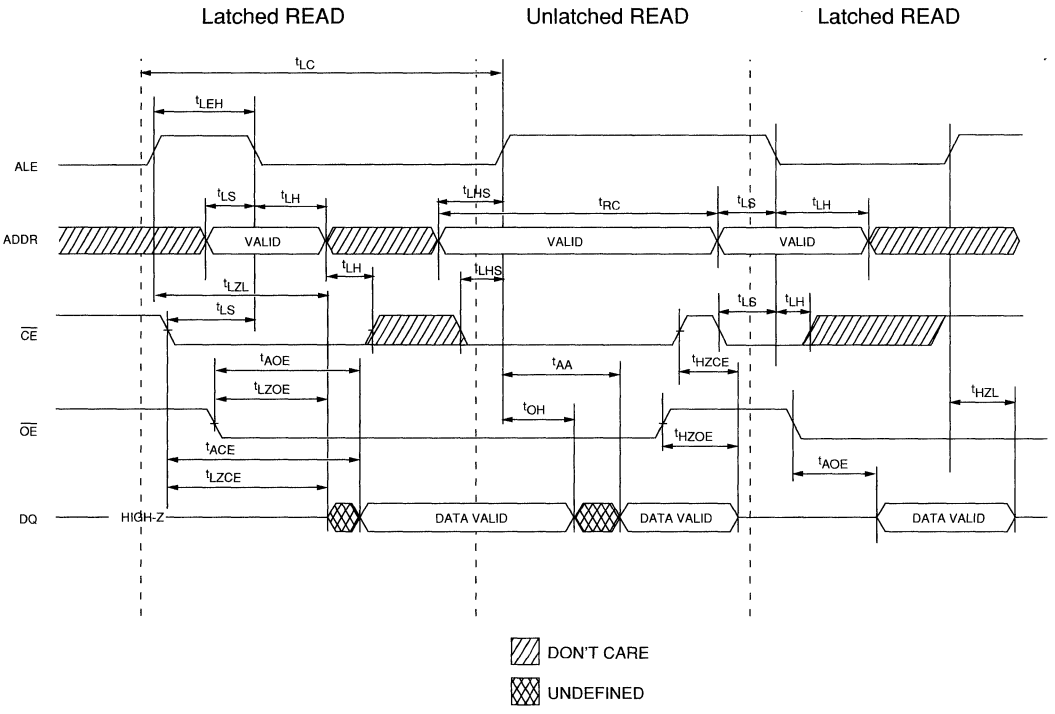


DON'T CARE

UNDEFINED

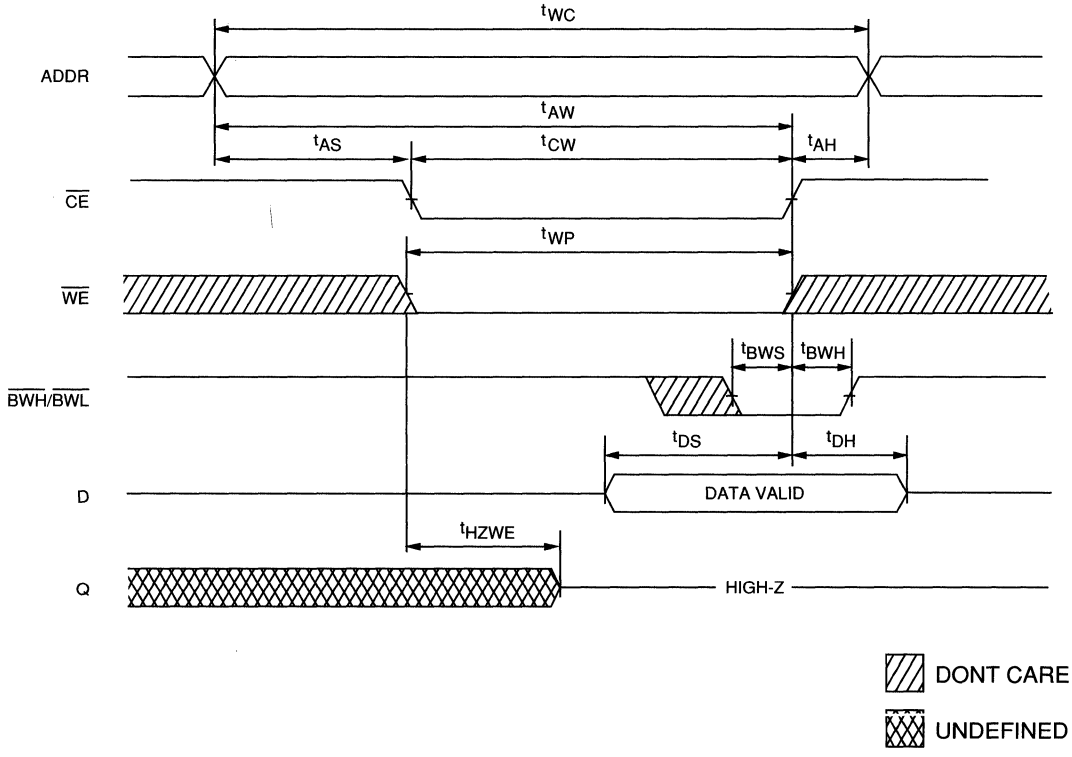
READ CYCLE NO. 3

(ALE=DLE=HIGH) [7, 11, 14]



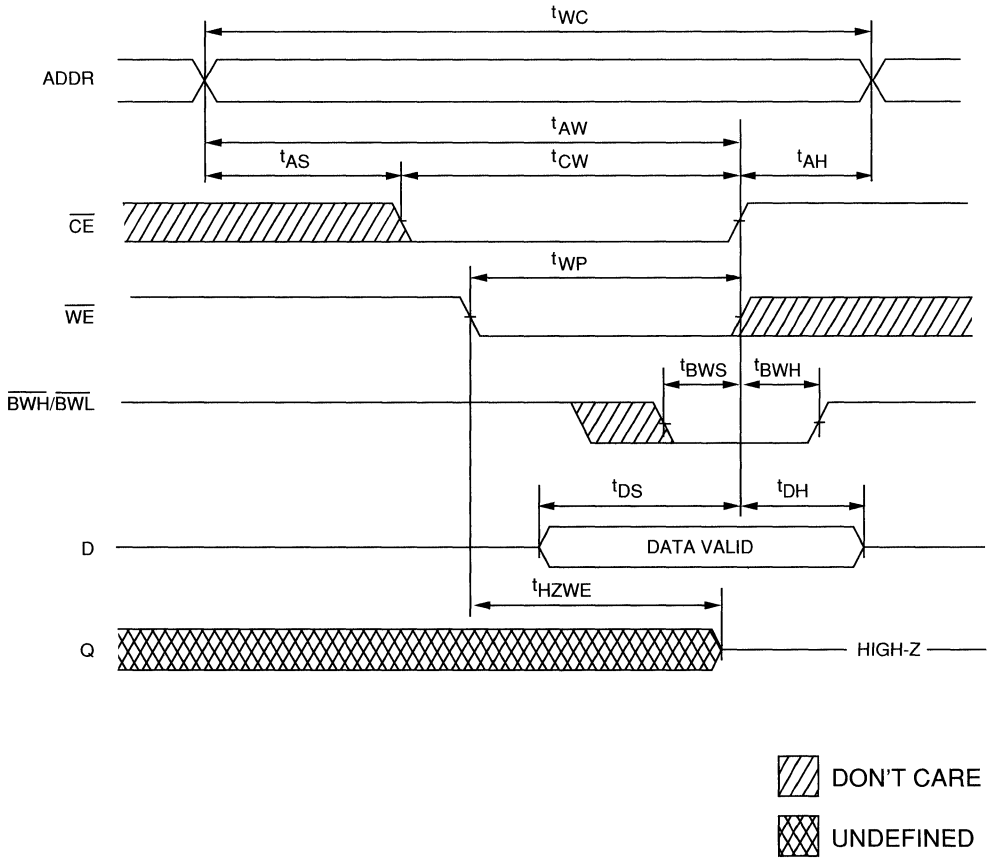
WRITE CYCLE NO. 1

Chip Enable Controlled
(ALE=DLE=HIGH) [10, 14]

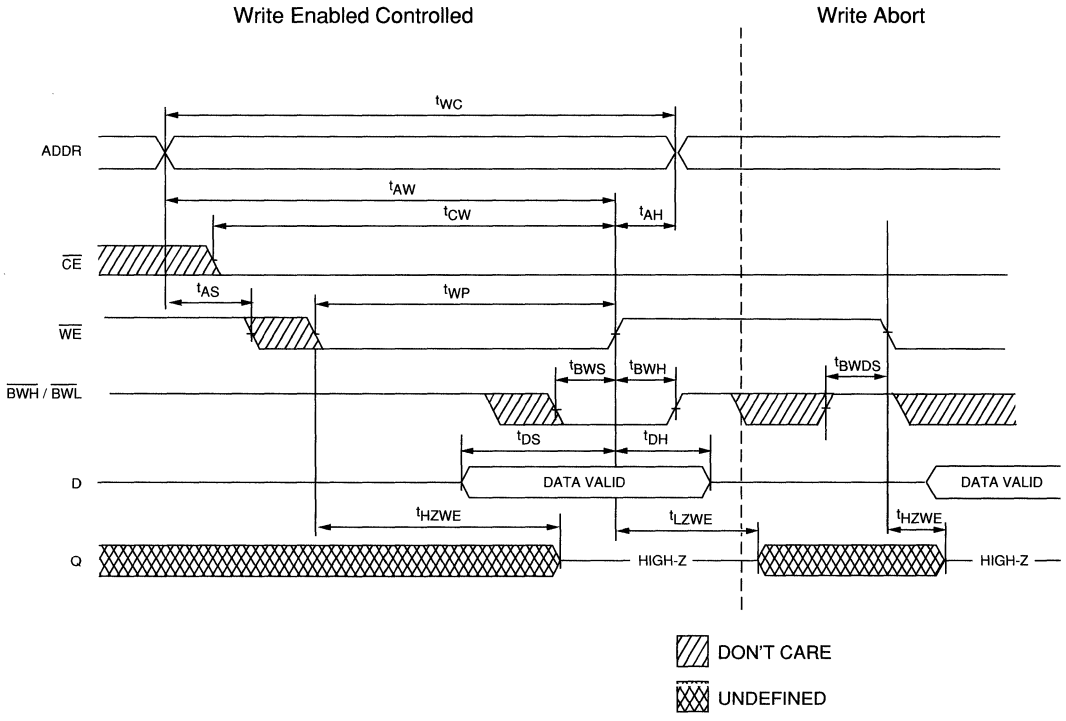


WRITE CYCLE NO. 2

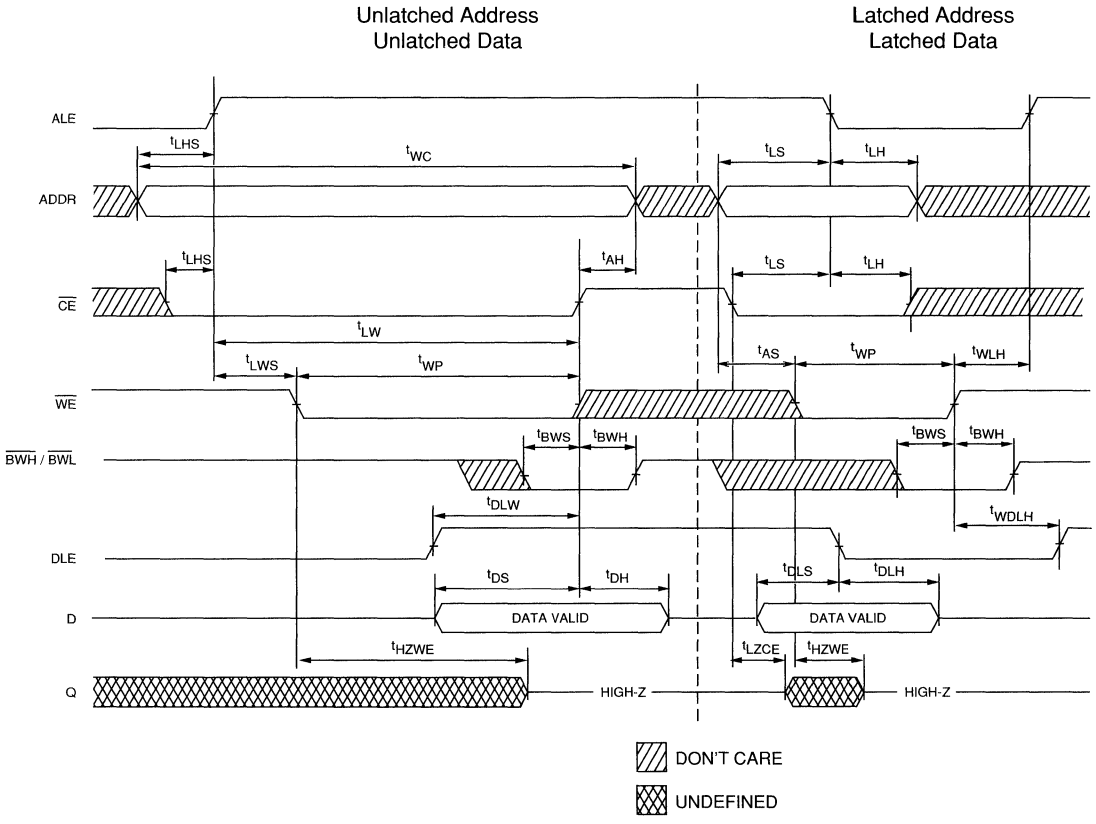
Write Enable Initiated / Chip Enable Terminate
(ALE=DLE=HIGH) [10, 14]



WRITE CYCLE NO. 3
(ALE=DLE=HIGH) [7, 10, 14]



WRITE CYCLE NO. 4 [7, 10, 14]



SRAM

16K x 18 SRAM

WITH ADDRESS / DATA INPUT LATCHES

FEATURES

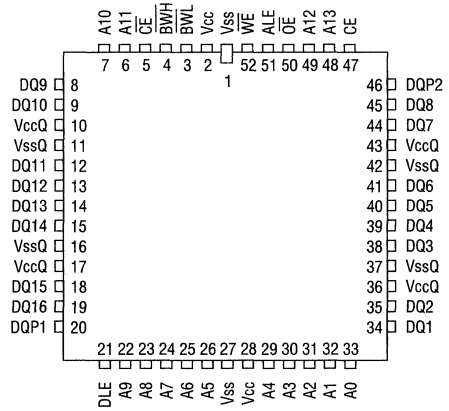
- Fast access times: 15, 17, 20 and 25ns
- Fast output enable: 6, 8 and 10ns
- Single +5V (±10%) power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Optional +3.3V (±10%) output buffer operation
- Separate Data Input Latch
- Common Data Inputs and Data Outputs
- BYTE WRITE capability via Dual Write Strobes
- Parity bits
- Address and Chip Enable input latches

OPTIONS

	MARKING
• Timing	
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG
• Density	
16K x 18	MT5C2818

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT5C2818 SRAM integrates a 16K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, latched active HIGH and active LOW chip enables, separate upper and lower byte write strobes and a fast output enable. The device is ideally suited for "pipelined" systems and systems that benefit from a wide data bus. Parity bits are provided for added data integrity.

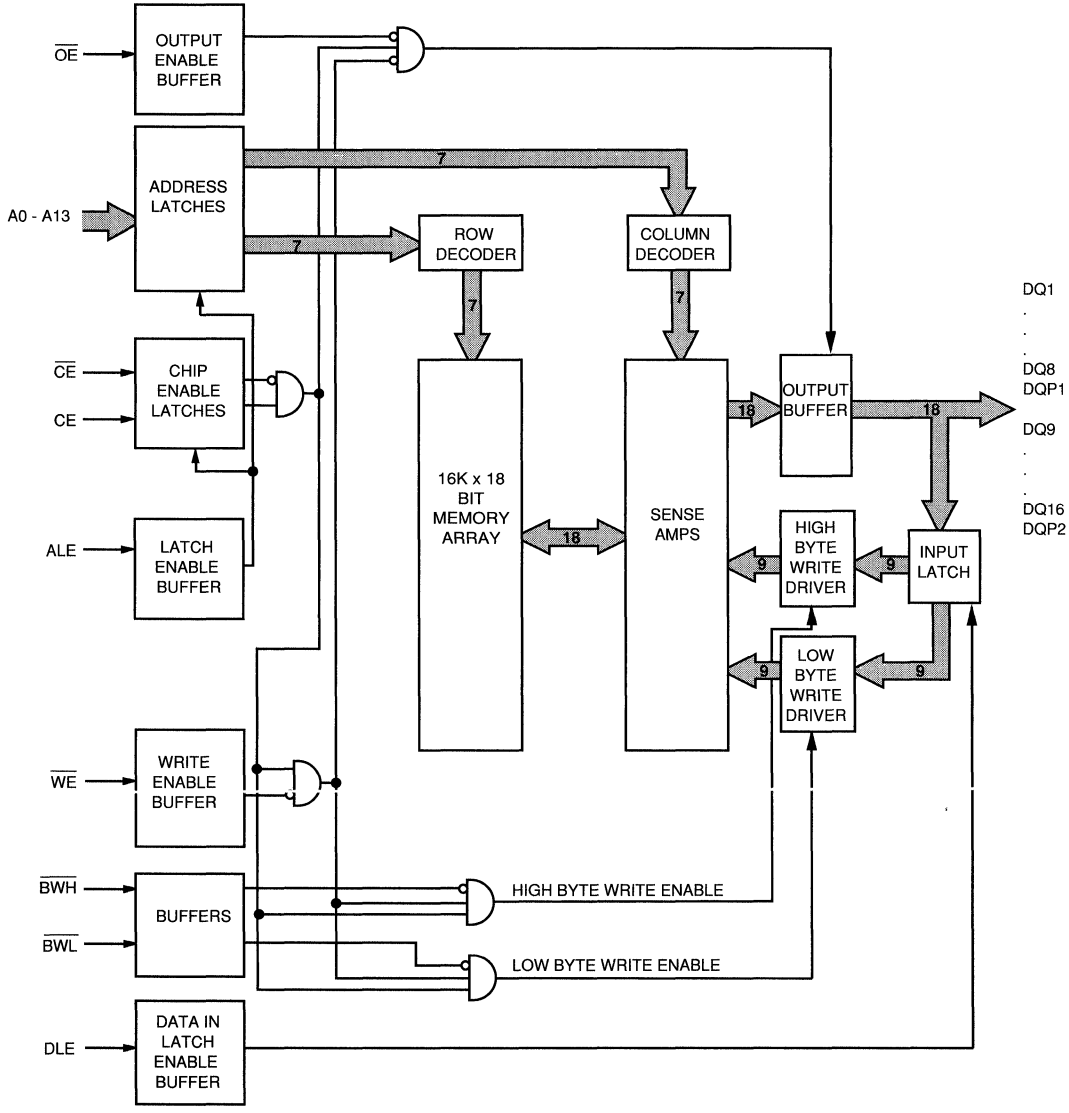
Address and chip enable latches are provided. When address latch enable (ALE) is HIGH, the address and chip enable latches are transparent, allowing the input to flow through the latch. If ALE is LOW, the address and chip enable latch inputs are disabled. This input latch simplifies READ and WRITE cycles by guaranteeing address hold time in a simple fashion.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) allow individual bytes to be written. $\overline{BWL}$ controls DQ1-DQ8 and DQP1, the lower bits. While $\overline{BWH}$ controls DQ9-DQ16 and DQP2, the upper bits.

A data input latch is provided. When data latch enable (DLE) is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, the data latch inputs are disabled. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT5C2818 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided to allow either +3.3V or +5V TTL operation of the output drivers.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC and PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are either latched or unlatched depending on the state of ALE.
52	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
51	ALE	Input	Address Latch Enable: This signal latches the address, CE, and $\overline{CE}$ inputs on its falling edge. When ALE is HIGH, the latch is transparent.
3, 4	$\overline{BWL}$, $\overline{BWH}$	Input	Byte Write Enables: These active LOW inputs allow individual bytes to be written. When $\overline{BWL}$ is LOW, data is written to the lower byte, D1-D8, DQP1. When $\overline{BWH}$ is LOW, data is written to the upper byte, D9-D16, DQP2. When both $\overline{BWH}$ and $\overline{BWL}$ are HIGH and meet the required setup time to the falling edge of $\overline{WE}$, then the WRITE cycle is aborted.
5, 47	$\overline{CE}$,CE	Input	Chip Enables: These signals are used to enable the device. Both active HIGH (CE) and active LOW ($\overline{CE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the data latch is transparent. Input data is latched into the on-chip data latch on the falling edge of DLE.
20, 46	DQP1 DQP2	Input/ Output	Parity Data I/O: These signals are data parity bits. The DQP1 is the parity bit for the lower byte, DQ1-DQ8. DQP2 is the parity bit for the upper byte, DQ9-DQ16.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. When data is latched, DQ1-DQ16 must meet the setup and hold times around DLE.
2, 28	Vcc	Supply	Power Supply: +5V ± 10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ± 10% or 3.3V ± 10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	CE	$\overline{CE}$	$\overline{WE}$	$\overline{BWL}$	$\overline{BWH}$	ALE	DLE	$\overline{OE}$	DQ	DQP
Deselected cycle	L	X	X	X	X	X	X	X	High-Z	High-Z
Deselected	X	H	X	X	X	X	X	X	High-Z	High-Z
READ	H	L	H	X	X	H	X	H	High-Z	High-Z
READ	H	L	H	X	X	H	X	L	Q1-Q16	QP1, QP2
LATCHED READ	H	L	H	X	X	L	X	L	Q1-Q16	QP1, QP2
WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	H	H	X	D1-D16	DP1, DP2
LATCHED WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	L	H	X	D1-D16	DP1, DP2
WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	H	L	X	D1-D16	DP1, DP2
LATCHED WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	L	L	X	D1-D16	DP1, DP2
ABORTED WRITE	H	L	L	H	H	X	X	X	High-Z	High-Z
BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	H	H	X	D1-D8	DP1
LATCHED BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	L	H	X	D1-D8	DP1
BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	H	H	X	D9-D16	DP2
LATCHED BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	L	H	X	D9-D16	DP2
BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	H	L	X	D1-D8	DP1
LATCHED BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	L	L	X	D1-D8	DP1
BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	H	L	X	D9-D16	DP2
LATCHED BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	L	L	X	D9-D16	DP2

NOTE:
1. Latched inputs (Addresses, CE, and $\overline{CE}$) must satisfy the specified setup and hold times around the falling edge of ALE. Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the ^{t}DLW time.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold times for DLE.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} supply relative to V_{SS}/V_{SSQ} ..... -1.0V to +7.0V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%; V_{SS} = V_{SSQ}, Unless Otherwise Noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1
Output Buffer Supply Voltage	5.0V TTL Compatible	V_{CCQ}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, $CE \ge V_{IH}$; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{CC}	150	250	mA	3
Power Supply Current: Standby	$CE \le V_{IL}$, $\overline{CE} \ge V_{IH}$; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{SB1}	20	30	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2V; $CE \le V_{SS}$ +0.2V, V_{CC} = MAX; $V_{IL} \le V_{SS}$ +0.2V, $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	8	10	mA	
	$CE \le V_{IL}$; $\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = 0; Outputs Open	I_{SB3}	10	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz V_{CC} = 5V	C_I		6	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; Vcc = VccQ = 5V ± 10%)

		-15		-17		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
ADDRESS LATCH											
Latch cycle time	^tLC	15		17		20		25		ns	
Latch high time	^tLEH	5		5		5		5		ns	
Address / Chip Enable setup to latch LOW	^tLS	2		2		2		2		ns	
Address / Chip Enable hold from latch LOW	^tLH	3		3		3		3		ns	
Address / Chip Enable setup to latch HIGH	^tLHS	0		0		0		0		ns	
Latch HIGH to output active (Low-Z)	^tLZL	2		2		2		2		ns	6, 7, 4
Latch HIGH to output in High-Z	^tHZL	2	7	2	7	2	7	2	10	ns	6, 7, 4
READ CYCLE											
READ cycle time	^tRC	15		17		20		25		ns	
Address access time	^tAA		15		17		20		25	ns	
Chip Enable access time	^tACE		15		17		20		25	ns	
Output hold from address change	^tOH	4		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	6, 7, 4
Chip Disable to output in High-Z	^tHZCE	2	7	2	7	2	7	2	10	ns	6, 7, 4
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip Disable to power-down time	^tPD		15		17		20		25	ns	
Output Enable access time	^tAOE		6		7		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	2		2		2		2		ns	6, 7, 4
Output Disable to output in High-Z	^tHZOE	2	6	2	7	2	8	2	10	ns	6, 7, 4
WRITE Cycle											
WRITE cycle time	^tWC	15		17		20		25		ns	
Chip Enable to end of write	^tCW	13		14		15		20		ns	
Address valid to end of write	^tAW	13		14		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
Write pulse width	^tWP	13		14		15		20		ns	
Data setup time	^tDS	6		7		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	5		5		5		5		ns	6, 7, 4
Write Enable to output in High-Z	^tHZWE	0	7	0	7	0	7	0	10	ns	6, 7, 4
Byte write enable setup time	^tBWS	6		7		8		10		ns	
Byte write enable hold time	^tBWH	2		2		2		2		ns	
Byte write disable setup time	^tBWDS	0		0		0		0		ns	
Data setup to DLE LOW	^tDLS	1		1		1		1		ns	9
Data hold from DLE LOW	^tDLH	3		3		3		3		ns	9
DLE HIGH to end of write	^tDLW	6		7		8		10		ns	8
End of write to DLE HIGH	^tWDLH	0		0		0		0		ns	9
End of write to ALE HIGH	^tWLH	0		0		0		0		ns	
ALE HIGH setup time to write enable LOW	^tLWS	0		0		0		0		ns	
ALE HIGH to end of write	^tLW	13		14		15		20		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

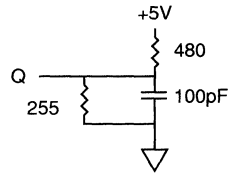


Fig. 1 OUTPUT LOAD EQUIVALENT

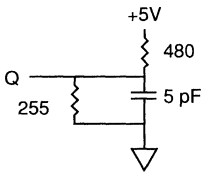
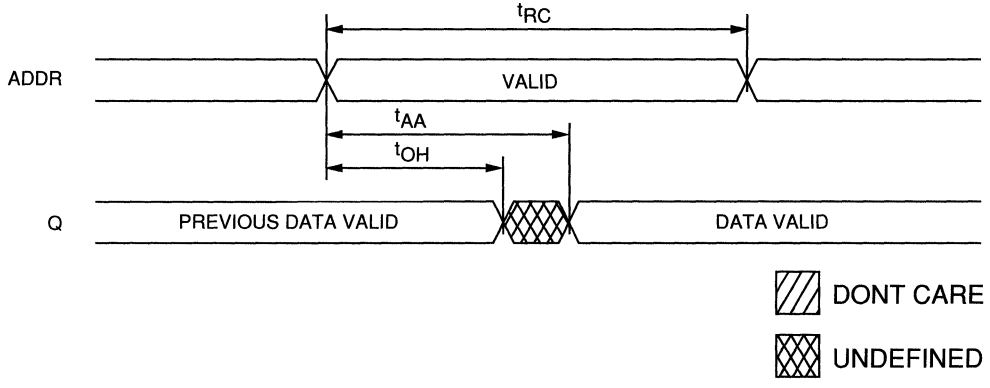


Fig. 2 OUTPUT LOAD EQUIVALENT

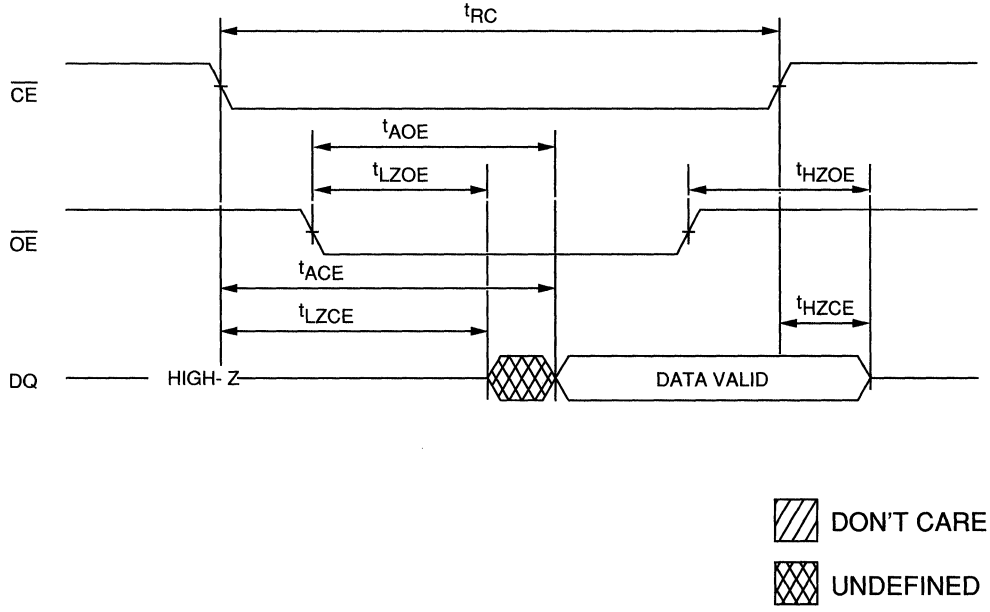
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZOE is less than ^{t}LZOE.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold time with respect to DLE.
10. Any combination of write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) can initiate and terminate a WRITE cycle.
11. $\overline{WE}$ is HIGH for READ cycle.
12. Device is continuously selected. All chip enables held in their active state.
13. Address valid prior to or coincident with the latest occurring chip enable.
14. CE timing is the same as $\overline{CE}$ timing. The wave form is inverted.

READ CYCLE NO. 1 [11, 12]

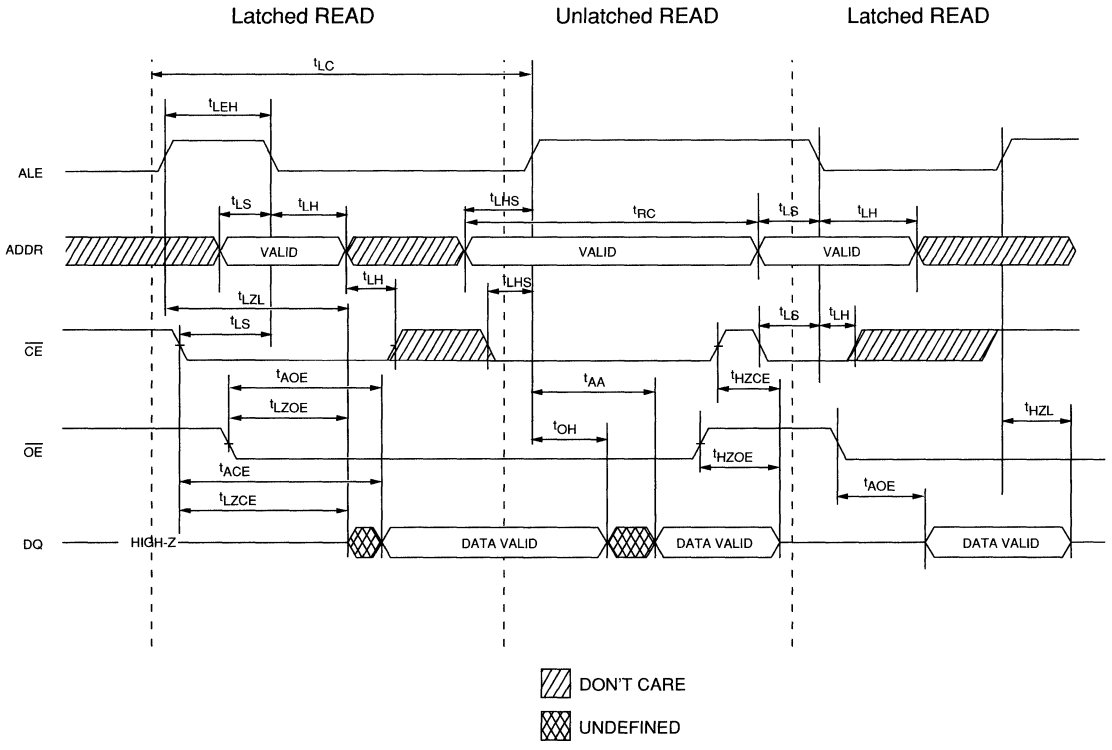


READ CYCLE NO. 2 [7, 11, 13, 14]



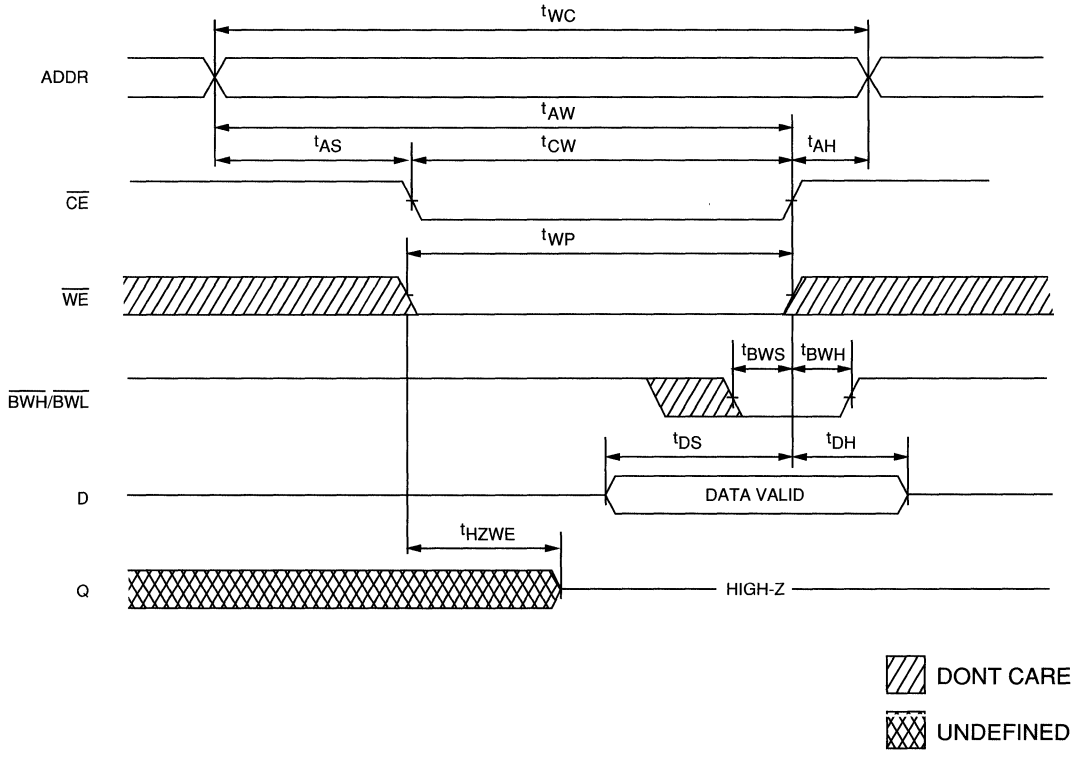
READ CYCLE NO. 3

(ALE=DLE=HIGH) [7, 11, 14]



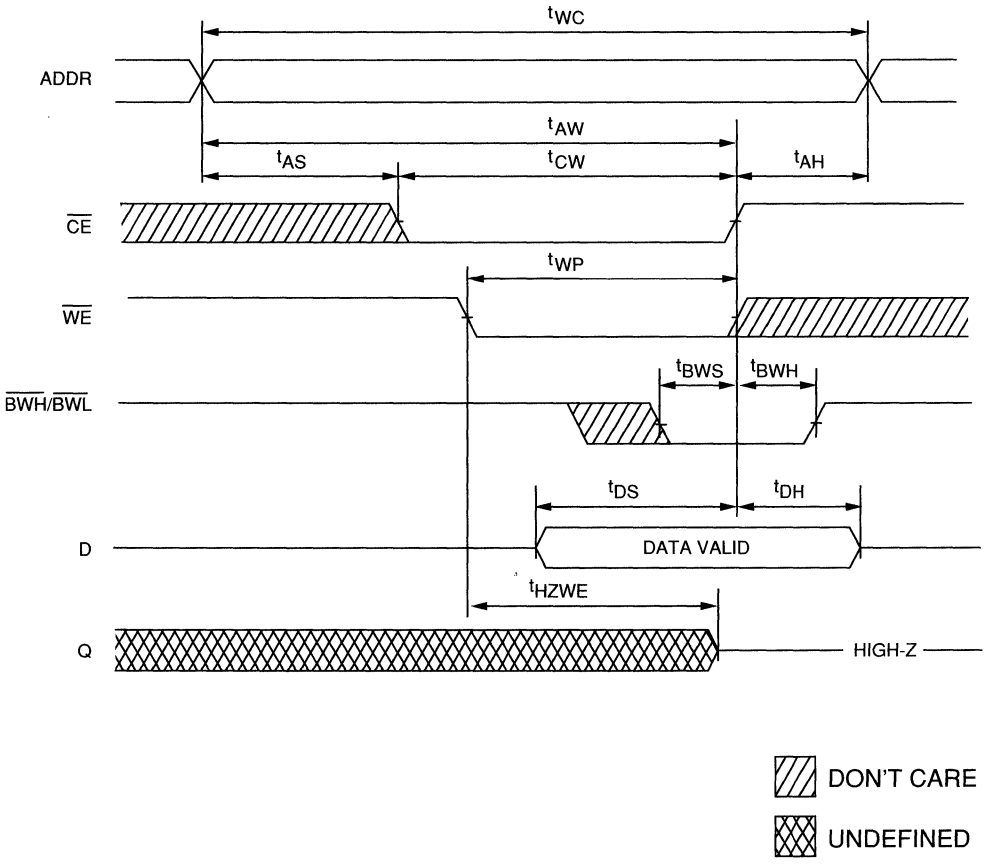
WRITE CYCLE NO. 1

Chip Enable Controlled
(ALE=DLE=HIGH) [10, 14]



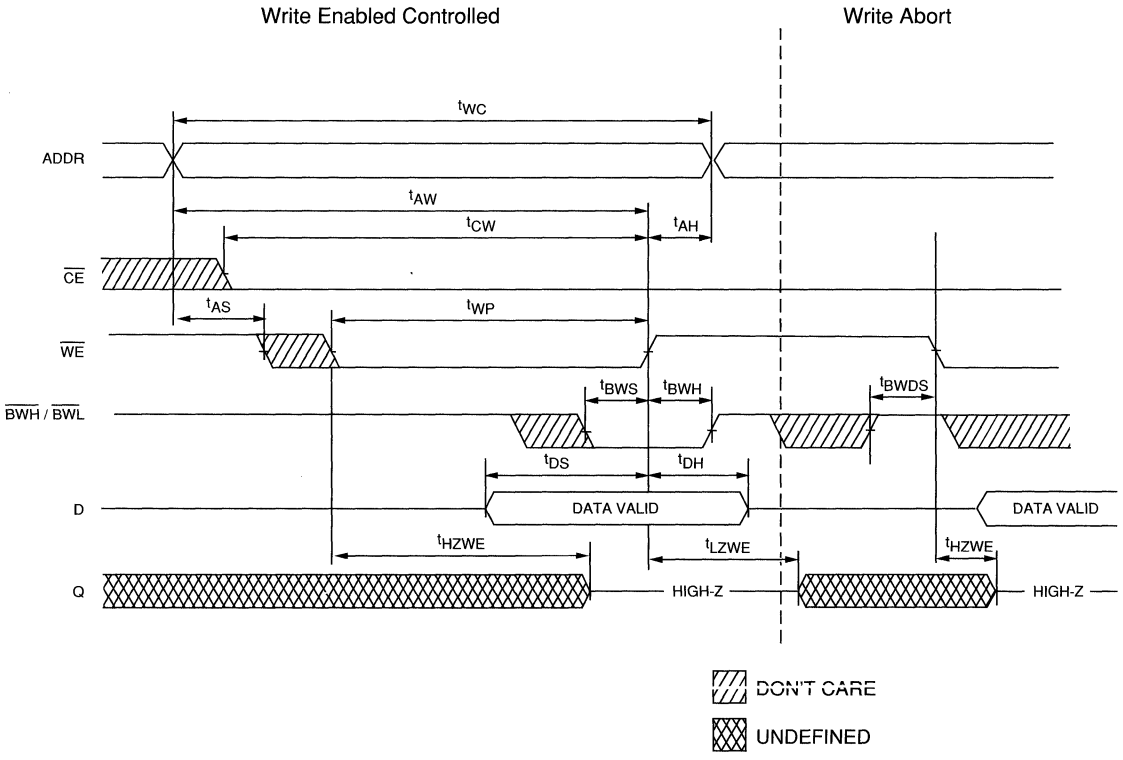
WRITE CYCLE NO. 2

Write Enable Initiated / Chip Enable Terminate
(ALE=DLE=HIGH) [10, 14]

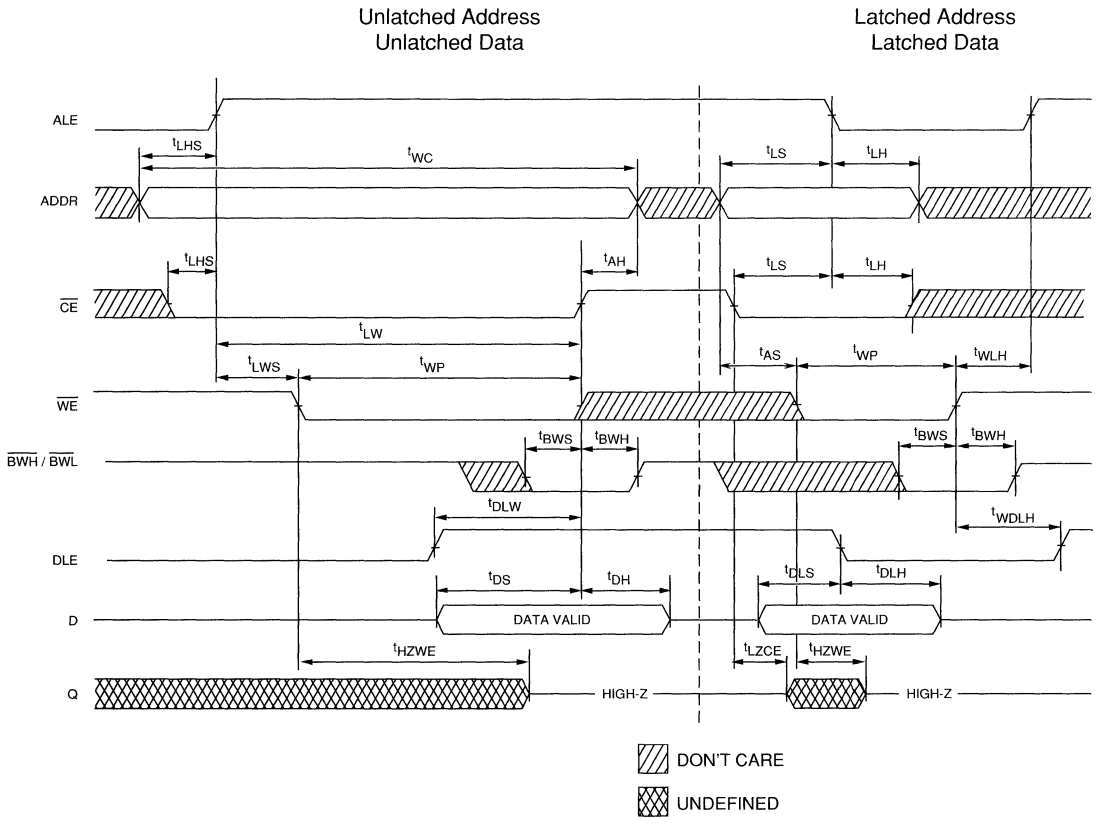


WRITE CYCLE NO. 3

(ALE=DLE=HIGH) [7, 10, 14]



WRITE CYCLE NO. 4 [7, 10, 14]



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**IT- (-40°C to +85°C),
AT- (-40°C to +125°C),
XT- (-55°C to +125°C)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $-55°C \le T_A \le 125°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	150	135	120	110	110	110	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	55	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	3	3	3	3	3	3	mA	

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current: Data Retention	$\overline{CE} \ge (V_{CC}$ -0.2V) $V_{IN} \ge (V_{CC}$ -0.2V) or $\le$ -0.2V	V_{CC} = 2V	I_{CCDR}		150	300	mA	
		V_{CC} = 3V			450	550	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-40°C ≤ T_A ≤ 85°C; -40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; Vcc = 5.0 ± 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip Enable access time	^tACE		11		12		15		20		25		30	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	^tHZCE		7		7		10		10		15		20	ns	6,7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip Disable to power-down time	^tPD		12		15		20		25		30		35	ns	
Output enable access time	^tAOE		7		7		9		10		15		20	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output Disable to output in High-Z	^tHZOE		6		6		10		10		15		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip Enable to end of write	^tCW	10		12		15		20		25		25		ns	
Address valid to end of write	^tAW	12		12		15		20		25		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data setup time	^tDS	9		9		10		12		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^tHZWE		6		6		8		10		12		15	ns	6
Write Enable to output valid	^tAWE		12		15		20		25		30		35	ns	
Data valid to output valid	^tADV		12		15		20		25		30		35	ns	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} .....-1.0V to +7.0V
Storage Temperature (Ceramic) .....-65°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**IT- (-40°C to +85°C),
AT- (-40°C to +125°C),
XT- (-55°C to +125°C)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $-55°C \le T_A \le 125°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/^tRC, Outputs Open	I_{CC}	150	140	130	120	110	110	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/^tRC, Outputs Open	I_{SB1}	60	50	45	40	40	40	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	5	5	5	5	5	5	mA	

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current: Data Retention	$\overline{CE} \ge (V_{CC}$ -0.2V) $V_{IN} \ge (V_{CC}$ -0.2V) or $\le$ -0.2V	V_{CC} = 2V	I_{CCDR}		150	300	mA	
		V_{CC} = 3V			450	550	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-40°C ≤ T_A ≤ 85°C; -40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; Vcc = 5.0 ± 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip Enable access time	^tACE		12		12		15		20		25		30	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	^tHZCE		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip Disable to power-down time	^tPD		12		15		20		25		30		35	ns	
Output Enable access time	^tAOE		7		7		9		10		15		20	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output Disable to output in High-Z	^tHZOE		6		6		10		10		15		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip Enable to end of write	^tCW	10		12		15		20		25		25		ns	
Address valid to end of write	^tAW	12		12		15		20		25		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data setup time	^tDS	9		9		10		12		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^tHZWE		6		6		8		10		12		15	ns	6
Write Enable to output valid	^tAWE		12		15		20		25		30		35	ns	
Data valid to output valid	^tADV		12		15		20		25		30		35	ns	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**IT- (-40°C to +85°C),
AT- (-40°C to +125°C),
XT- (-55°C to +125°C)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $-55°C \le T_A \le 125°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-30	-35	-40	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/^tRC, Outputs Open	I_{CC}	120	110	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/^tRC, Outputs Open	I_{SB1}	30	30	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	8	8	8	8	8	mA	

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current: Data Retention	$\overline{CE} \ge (V_{CC}$ -0.2V) $V_{IN} \ge (V_{CC}$ -0.2V) or $\le$ -0.2V	V_{CC} = 2V	I_{CCDR}		95	500	mA	
		V_{CC} = 3V			300	900	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $-55°C \le T_A \le 125°C$; $V_{CC} = 5.0 \pm 10\%$)

DESCRIPTION		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	20		25		30		35		45		ns	
Address access time	t_{AA}		20		25		30		35		45	ns	
Chip Enable access time	t_{ACE}		20		25		30		35		45	ns	
Output hold from address change	t_{OH}	3		5		5		5		5		ns	
Chip Enable to output in Low-Z	t_{LZCE}	6		6		6		6		6		ns	
Chip Disable to output in High-Z	t_{HZCE}		9		9		12		15		18	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		ns	
Chip Disable to power-down time	t_{PD}		20		25		30		35		45	ns	
Output Enable access time	t_{AOE}		10		10		12		15		15	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		0		ns	
Output Disable to out put in High-Z	t_{HZOE}		7		7		10		12		15	ns	
WRITE Cycle													
WRITE cycle time	t_{WC}	20		20		25		30		35		ns	
Chip Enable to end of write	t_{CW}	15		18		20		20		25		ns	
Address valid to end of write	t_{AW}	15		18		20		20		25		ns	
Address setup time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		ns	
Write pulse width	t_{WP}	15		18		20		20		25		ns	
Data setup time	t_{DS}	10		12		15		15		20		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write Disable to output in Low-Z	t_{LZWE}	5		5		5		5		5		ns	
Write Enable to output in High-Z	t_{HZWE}		10		10		12		15		18	ns	6

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**IT- (-40°C to +85°C),
AT- (-40°C to +125°C),
XT- (-55°C to +125°C)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-40°C \le T_A \le 85°C$; $-40°C \le T_A \le 125°C$; $-55°C \le T_A \le 125°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open		I_{CC}		120	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open		I_{SB1}		30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0		I_{SB2}		7	mA	
Power Supply Current: Data Retention	$\overline{CE} \ge (V_{CC}$ -0.2V) $V_{IN} \ge (V_{CC}$ -0.2V) or $\le$ -0.2V	V_{CC} = 2V	I_{CCDR}		500	mA	
		V_{CC} = 3V			750	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-40°C ≤ T_A ≤ 85°C; -40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; Vcc = 5.0V ± 10%)

DESCRIPTION		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	25		35		45		ns	
Address access time	^tAA		25		35		45	ns	
Chip Enable access time	^tACE		25		35		45	ns	
Output hold from address change	^tOH	5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	
Chip Disable to output in High-Z	^tHZCE		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip Disable to power-down time	^tPD		25		35		45	ns	
Output Enable access time	^tAOE		8		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output Disable to output in High-Z	^tHZOE		10		12		15	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	25		35		45		ns	
Chip Enable to end of write	^tCW	15		20		25		ns	
Address valid to end of write	^tAW	15		20		25		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
Write pulse width	^tWP	15		20		25		ns	
Data setup time	^tDS	10		15		20		ns	
Data hold time	^tDH	0		0		0		ns	
Write Disable to output in Low-Z	^tLZWE	0		0		0		ns	
Write Enable to output in High-Z	^tHZWE	0	10	0	15	0	18	ns	6, 7

MICRON TECHNOLOGY, INC.

SYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package		Process	Page
				PLCC	PQFP		
Dual 16K x 16	Registered Address, Write Control, Dual Chip Enable; Data Input Latch	MT58C1616	15, 17, 20, 25	52	52	CMOS	5-1
Dual 16K x 18	Registered Address, Write Control, Dual Chip Enable; Data Input Latch	MT58C1618	15, 17, 20, 25	52	52	CMOS	5-11

SYNCHRONOUS SRAM

16K x 16 SRAM

WITH CLOCKED, REGISTERED INPUTS

FEATURES

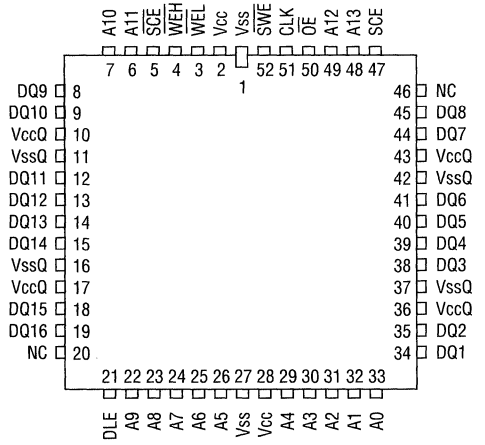
- Fast access times: 15, 17, 20, and 25ns
- Fast Output Enable: 6, 7, 8, and 10ns
- Single +5V (±10%) power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Optional +3.3V (±10%) output buffer operation
- Data Input Latch
- Common Data Inputs and Data Outputs
- BYTE WRITE capability via Dual Write Strobes
- Clock controlled registered address, Write Control and Dual Chip Enables

OPTIONS

	MARKING
• Timing	
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG
• Density	
16K x 16	MT58C1616

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-5)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high speed, low power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

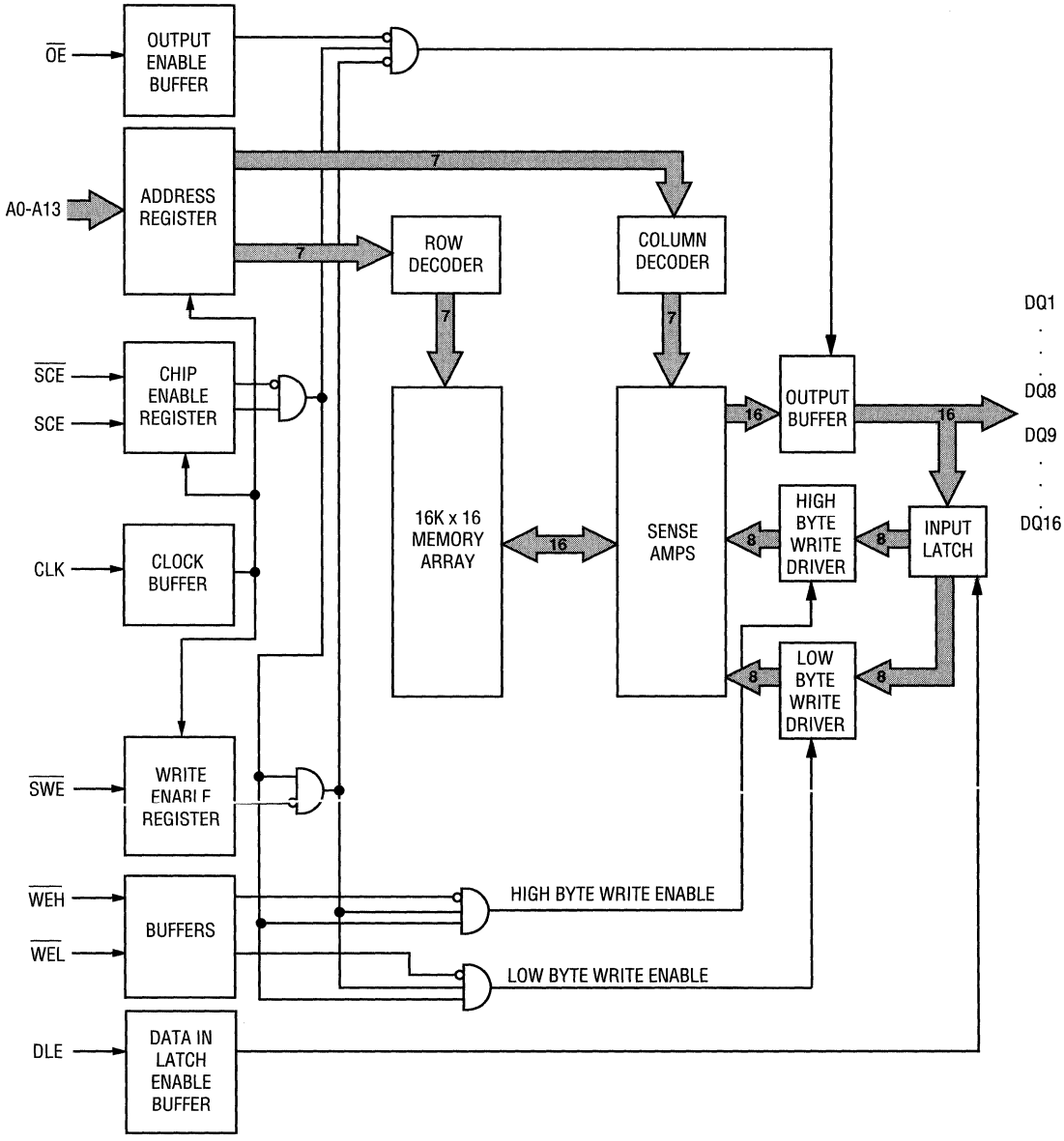
The MT58C1616 SRAM integrates a 16K x 16 SRAM core with advanced synchronous peripheral circuitry. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, the two chip selects ($\overline{SCE}$, SCE) and the synchronous write enable ($\overline{SWE}$). Asynchronous inputs include the byte write enables ($\overline{WEL}$, $\overline{WEH}$), output enable ($\overline{OE}$), data latch enable (DLE) and the clock. Input data can be asynchronously latched by DLE to provide simplified data-in (D) timing during WRITE cycles. Data-out (Q), enabled by $\overline{OE}$ during READ cycles, is asynchronous. The entire data word (DQ1 - DQ16) is output during each READ cycle. The devices are ideally suited for "pipelined" systems and those systems which benefit from a wide data bus.

Address and write control are registered on-chip to simplify WRITE cycles. Dual write enables allow individual bytes to be written. $\overline{WEL}$ controls DQ1-DQ8 while $\overline{WEH}$ controls DQ9-DQ16. $\overline{WEL}$/$\overline{WEH}$ allow late WRITE cycles to be aborted if they are both HIGH during the LOW period of the clock. Dual chip enables (SCE, $\overline{SCE}$) allow on-chip address decoding to be accomplished when the devices are used in a dual bank mode.

A data input latch is provided. When DLE is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, the data latch inputs are disabled. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT58C1616 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided to allow either +3.3V or +5V TTL operation of the output drivers.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC and PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
52	$\overline{SWE}$	Input	Synchronous Write Enable: This input is a synchronous write enable and must meet the setup and hold times around the rising edge of CLK. $\overline{SWE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
51	CLK	Input	Clock: This signal registers the address, SCE, $\overline{SCE}$, and $\overline{SWE}$ inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.
3, 4	$\overline{WEL}$, $\overline{WEH}$	Input	Asynchronous Write Enables: These asynchronous, active LOW inputs allow individual bytes to be written. When $\overline{WEL}$ is LOW, data is written to the lower byte, D1-D8. When $\overline{WEH}$ is LOW, data is written to the upper byte, D9-D16. A late WRITE cycle can be aborted if both $\overline{WEL}$ and $\overline{WEH}$ are HIGH during the LOW period of CLK.
5, 47	$\overline{SCE}$,SCE	Input	Synchronous Chip Selects: These synchronous signals are used to enable the device. Both active HIGH (SCE) and active LOW ($\overline{SCE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH the latch is transparent. Input data is latched asynchronously into the on-chip data latch on the falling edge of DLE. DLE must meet the setup and hold times around CLK if data is latched.
20, 46	NC NC	Input/ Output	These pins are no connects (NC). No connects are not internally bonded.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. Input data must meet the setup and hold time around DLE when being latched.
2, 28	Vcc	Supply	Power Supply: +5V ± 10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ± 10% or 3.3V ± 10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	SCE	$\overline{SCE}$	$\overline{SWE}$	$\overline{WEL}$	$\overline{WEH}$	DLE	$\overline{OE}$	DQ
Deselected Cycle	L	X	X	X	X	X	X	High-Z
Deselected Cycle	X	H	X	X	X	X	X	High-Z
Read Cycle	H	L	H	X	X	X	H	High-Z
Read Cycle	H	L	H	X	X	X	L	Q1-Q16
Word Write Cycle DQ1-DQ16 Transparent data-in	H	L	L	L	L	H	X	D1-D16
Word Write Cycle DQ1-DQ16 Latched data-in	H	L	L	L	L	L	X	D1-D16
Aborted Write Cycle	H	L	L	H	H	X	X	High-Z
Byte Write Cycle DQ1-DQ8 Transparent data-in	H	L	L	L	H	H	X	D1-D8
Byte Write Cycle DQ9-DQ16 Transparent data-in	H	L	L	H	L	H	X	D9-D16
Byte Write Cycle DQ1-DQ8 Latched data-in	H	L	L	L	H	L	X	D1-D8
Byte Write Cycle DQ9-DQ16 Latched data-in	H	L	L	H	L	L	X	D9-D16

NOTE:
1. Registered inputs (Addresses, $\overline{SWE}$, SCE, and $\overline{SCE}$) must satisfy the specified setup and hold times around the rising edge of clock (CLK). Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the WRITE cycle.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold times.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} supply relative to V_{SS}/V_{SSQ} ..... -1.0V to +7.0V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} =5.0V ± 10%; $V_{SS} = V_{SSQ}$, Unless Otherwise Noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1
Output Buffer Supply Voltage	5.0V TTL Compatible	V_{CCQ}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{SCE} \le V_{IL}$; $SCE \ge V_{IH}$; f = MAX, V_{CC} = MAX; Outputs Open	I_{CC}	150	300	mA	3
Power Supply Current: Standby	f = MAX; $SCE \le V_{IL}$; $\overline{SCE} \ge V_{IH}$, V_{CC} = MAX	I_{SB1}	20	50	mA	
	$\overline{SCE} \ge V_{CC}$ -0.2; $SCE \le V_{SS}$ +0.2, V_{CC} = MAX; $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}	8	15	mA	
	f = 0; $SCE \le V_{IL}$; $\overline{SCE} \le V_{IH}$, V_{CC} = MAX	I_{SB3}	10	25	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		6	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; Vcc = VccQ = 5V ± 10%)

		-15		-17		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	tKC	15		17		20		25		ns	
Clock high time	tKH	4		4		4		4		ns	
Clock low time	tKL	8		8		8		8		ns	
Chip Enable											
SCE/$\overline{SCE}$ setup time	tSCES	2		2		2		2		ns	10
SCE/$\overline{SCE}$ hold time	tSCEH	2		2		2		2		ns	10
Address											
Address setup time	tSAS	2		2		2		2		ns	10
Address hold time	tSAH	2		2		2		2		ns	10
READ Cycle											
READ cycle time	tRC	15		17		20		25		ns	11
Clock to output valid	tKQ		15		17		20		25	ns	
Clock to output invalid	tKQX	3		3		3		3		ns	10
Clock to output in Low-Z	tKQLZ	10		10		10		10		ns	6, 7
Clock to output in High-Z	tKQHZ	3	8	3	8	3	8	3	12	ns	6, 7
$\overline{SWE}$ setup time	tSWNS	2		2		2		2		ns	10
$\overline{SWE}$ hold time	tSWNH	2		2		2		2		ns	10
$\overline{OE}$ to output valid	tOEQ		6		7		8		10	ns	
$\overline{OE}$ to output in Low-Z	tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	tOEHZ		8		8		8		8	ns	6, 7
WRITE Cycle											
WRITE cycle time	tWC	15		17		20		25		ns	11
$\overline{SWE}$ setup time	tSWES	2		2		2		2		ns	10
$\overline{SWE}$ hold time	tSWEH	2		2		2		2		ns	10
Data setup time	tDS	5		6		6		7		ns	8, 10
Data hold time	tDH	2		2		2		2		ns	8, 10
Data to DLE not setup time	tDLNS	1		1		1		1		ns	9, 10
Data to DLE not hold time	tDLNH	3		3		3		3		ns	9, 10
DLE setup time	tDLS	6		6		6		7		ns	9, 10
DLE hold time	tDLH	2		2		2		2		ns	9, 10
$\overline{WEL}$ / $\overline{WEH}$ setup time	tWES	6		6		6		7		ns	10
$\overline{WEL}$ / $\overline{WEH}$ hold time	tWEH	2		2		2		2		ns	10
$\overline{WEL}$ / $\overline{WEH}$ not setup time	tWNS		0		0		0		0	ns	10
$\overline{WEL}$ / $\overline{WEH}$ not hold time	tWNH	2		2		2		2		ns	10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

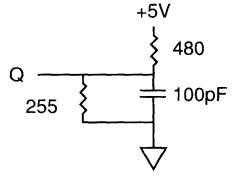


Fig. 1 OUTPUT LOAD EQUIVALENT

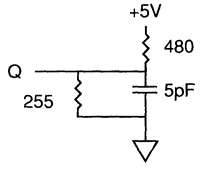
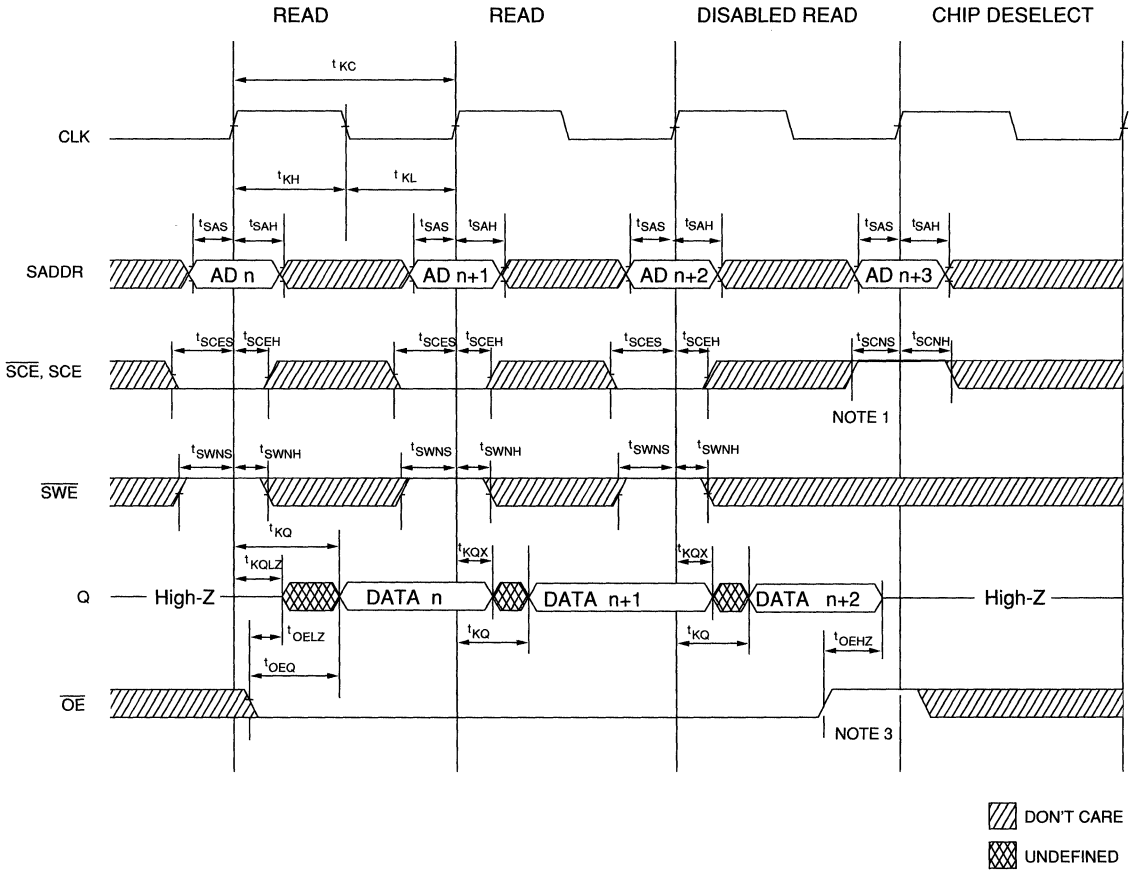


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

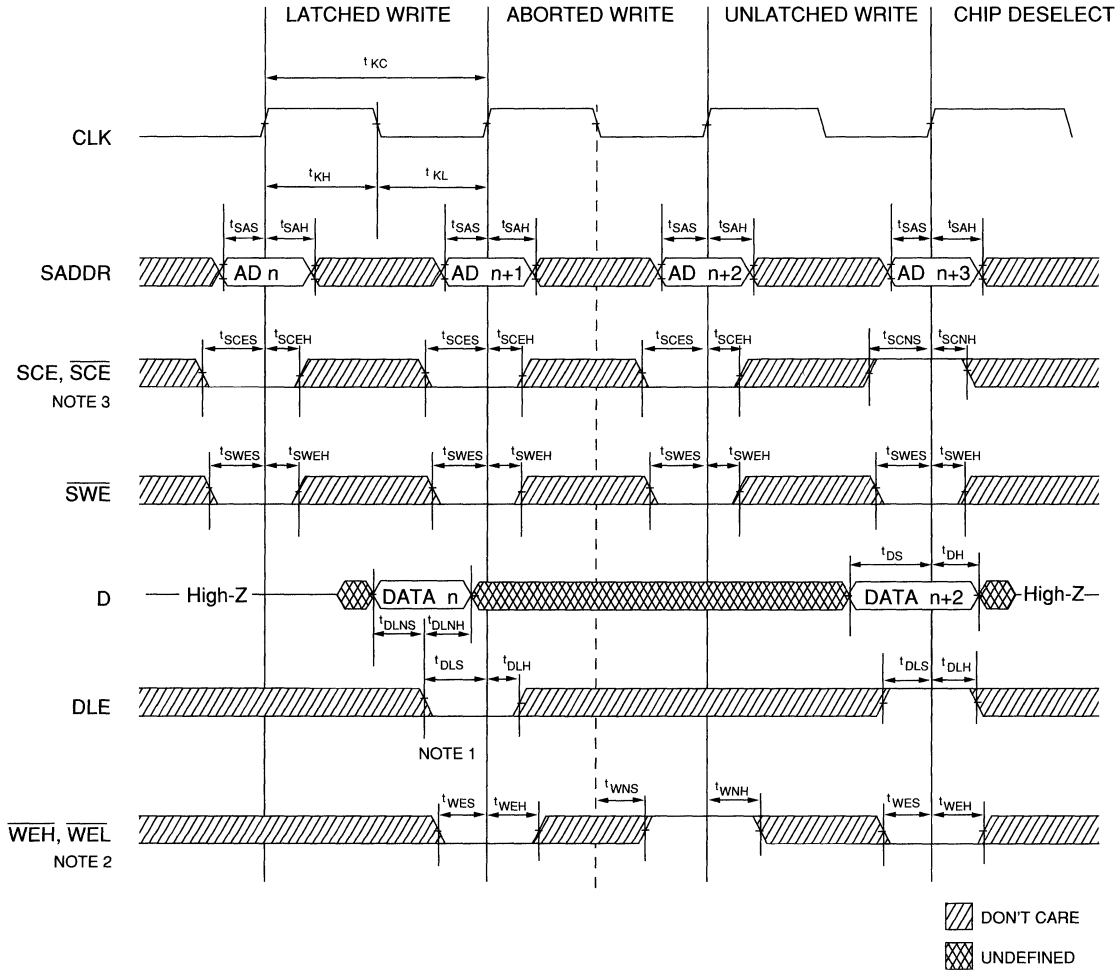
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}KQHZ is less than ^{t}KQLZ and ^{t}OEHZ is less than ^{t}OELZ.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold time with respect to the rising edge of clock (CLK).
10. This is a synchronous device. All synchronous inputs must meet the setup and hold times with stable logic levels for all falling edges of address latch enable (ALE) and data latch enable (DLE).
11. ^{t}RC = ^{t}WC = ^{t}KC

READ TIMING [2]



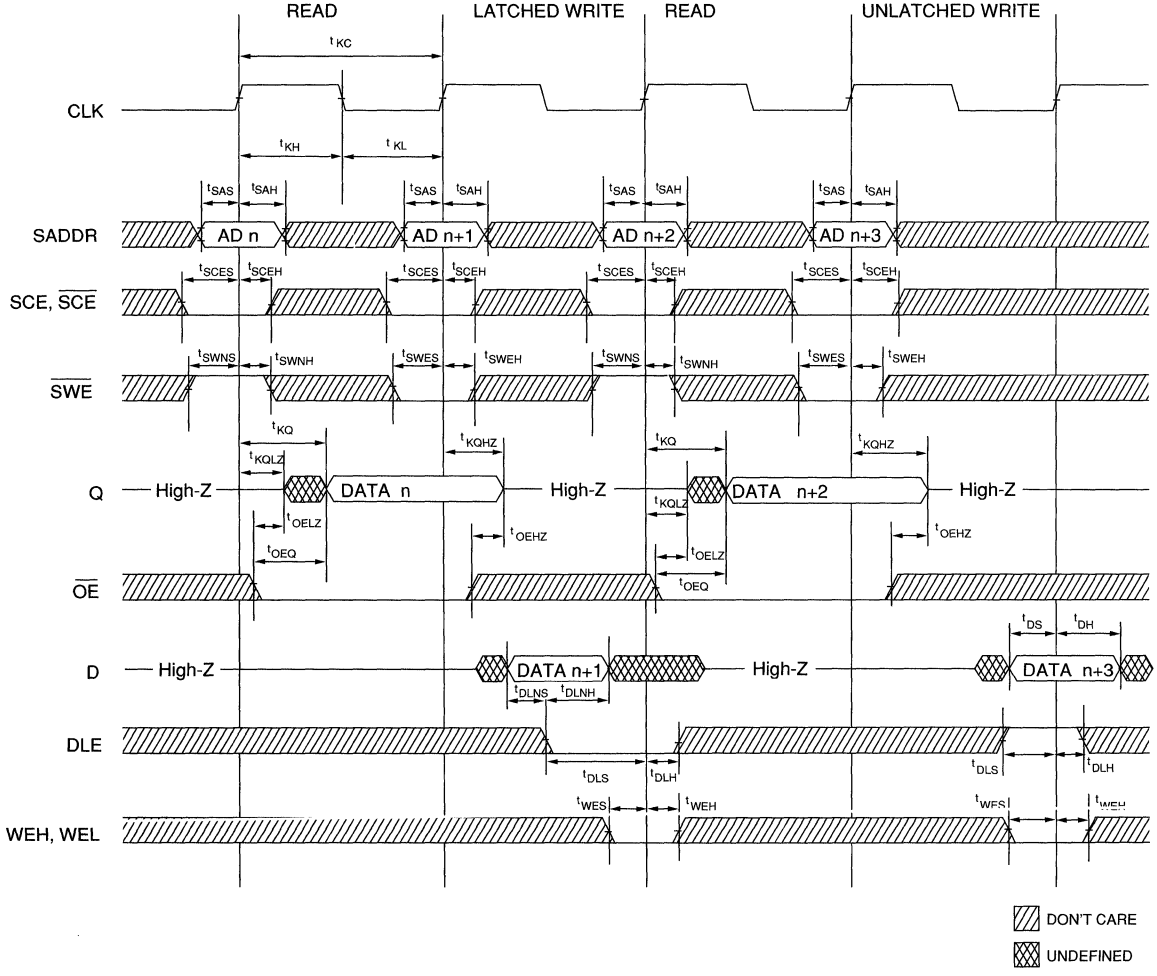
NOTE:
1. When synchronous chip enables (SCE, $\overline{SCE}$) are inactive, the part is deselected.
2. $\overline{WEL}$ / $\overline{WEH}$ are Don't Care signals during a READ cycle.
3. Data out (Q) is disabled whenever asynchronous output enable ($\overline{OE}$) is inactive, during a READ cycle.

WRITE TIMING



NOTE:
1. Data is latched when DLE transitions from HIGH to LOW. When DLE is HIGH, the latch is transparent and data flows through the latch.
2. Asynchronous write enables ($\overline{WEH}$, $\overline{WEL}$) are available for use as byte write enables at the system level. They are also available to perform a late WRITE cycle abort.
3. When synchronous chip enables (SCE, $\overline{SCE}$) are inactive, the part is deselected.

READ/WRITE TIMING



SYNCHRONOUS SRAM

16K x 18 SRAM

WITH CLOCKED, REGISTERED INPUTS

FEATURES

- Fast access times: 15, 17, 20, and 25ns
- Fast Output Enable: 6, 7, 8, and 10ns
- Single +5V (±10%) power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Optional +3.3V (±10%) output buffer operation
- Data Input Latch
- Common Data Inputs and Data Outputs
- BYTE WRITE capability via Dual Write Strobes
- Parity Bits
- Clock controlled registered address, Write Control and Dual Chip Enables

OPTIONS

MARKING

- Timing

15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25

- Packages

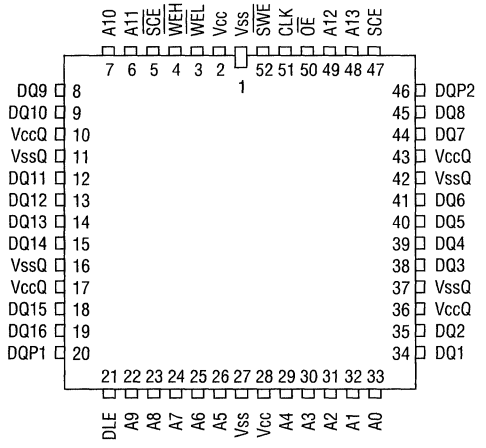
52-pin PLCC	EJ
52-pin PQFP	LG

- Density

16K x 18	MT58C1618

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-5)



GENERAL DESCRIPTION

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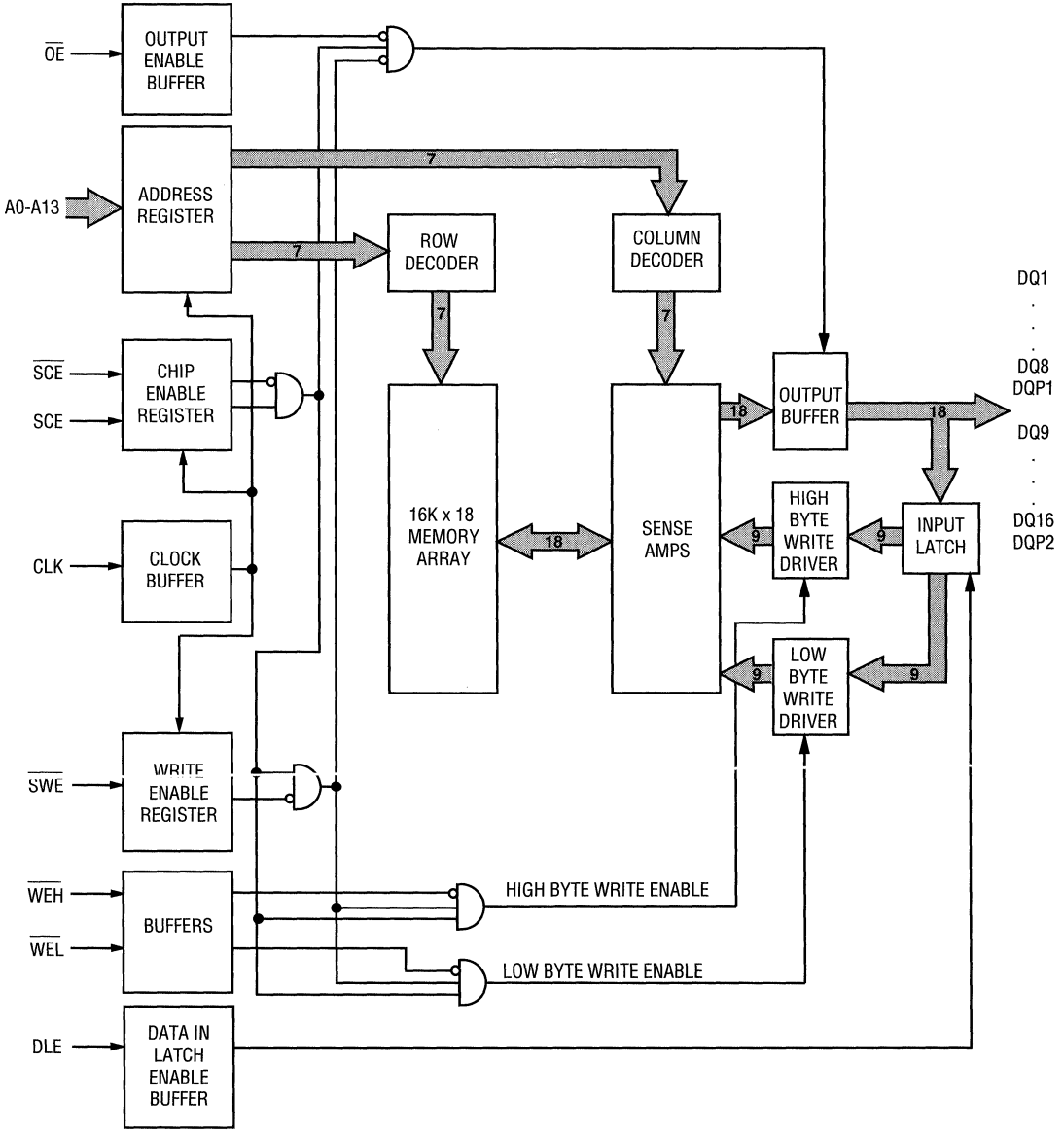
The MT58C1618 SRAM integrates a 16K x 18 SRAM core with advanced synchronous peripheral circuitry. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, the two chip selects ($\overline{SCE}$, SCE) and the synchronous write enable ($\overline{SWE}$). Asynchronous inputs include the byte write enables ($\overline{WEL}$, $\overline{WEH}$), output enable ($\overline{OE}$), data latch enable (DLE) and the clock. Input data can be asynchronously latched by DLE to provide simplified data-in (D) timing during WRITE cycles. Data-out (Q), enabled by $\overline{OE}$ during READ cycles, is asynchronous. The entire data word (DQ1-DQ16, DQP1/2) is output during each READ cycle. The devices are ideally suited for "pipelined" systems and those systems which benefit from a wide data bus.

Address and write control are registered on-chip to simplify WRITE cycles. Dual write enables allow individual bytes to be written. $\overline{WEL}$ controls DQ1-DQ8 and DQP1 while $\overline{WEH}$ controls DQ9-DQ16 and DQP2. $\overline{WEL}$/$\overline{WEH}$ allow late WRITE cycles to be aborted if they are both HIGH during the LOW period of the clock. Dual chip enables (SCE, $\overline{SCE}$) allow on-chip address decoding to be accomplished when the devices are used in a dual bank mode.

A data input latch is provided. When DLE is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, the data latch inputs are disabled. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT58C1618 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided to allow either +3.3V or +5V TTL operation of the output drivers.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC and PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
52	$\overline{SWE}$	Input	Synchronous Write Enable: This input is a synchronous write enable and must meet the setup and hold times around the rising edge of CLK. $\overline{SWE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
51	CLK	Input	Clock: This signal latches the address, SCE, $\overline{SCE}$, and $\overline{SWE}$ inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
3, 4	$\overline{WEL}$, $\overline{WEH}$	Input	Asynchronous Write Enables: These asynchronous, active LOW inputs allow individual bytes to be written. When $\overline{WEL}$ is LOW, data is written to the lower byte, D1-D8, DQP1. When $\overline{WEH}$ is LOW, data is written to the upper byte, D9-D16, DQP2. A late WRITE cycle can be aborted if both $\overline{WEL}$ and $\overline{WEH}$ are HIGH during the LOW period of CLK.
5, 47	$\overline{SCE}$,SCE	Input	Synchronous Chip Selects: These synchronous signals are used to enable the device. Both active HIGH (SCE) and active LOW ($\overline{SCE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH the latch is transparent. Input data is latched asynchronously into the on-chip data latch on the falling edge of DLE. DLE must meet the setup and hold times around DLE if data is latched.
20, 46	DQP1 DQP2	Input/ Output	Parity Data I/O: These signals are data parity bits. The DQP1 is the parity bit for the lower byte, DQ1-DQ8. DQP2 is the parity bit for the upper byte, DQ9-DQ16. Parity data must meet the setup and hold time around DLE when being latched.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. Input data must meet the setup and hold time around DLE when being latched.
2, 28	Vcc	Supply	Power Supply: +5V ± 10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ± 10% or 3.3V ± 10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	SCE	$\overline{SCE}$	$\overline{SWE}$	$\overline{WEL}$	$\overline{WEH}$	DLE	$\overline{OE}$	DQ
Deselected Cycle	L	X	X	X	X	X	X	High-Z
Deselected Cycle	X	H	X	X	X	X	X	High-Z
Read Cycle	H	L	H	X	X	X	H	High-Z
Read Cycle	H	L	H	X	X	X	L	Q1-Q16, QP1, QP2
Word Write Cycle DQ1-DQ16, DQP1, DQP2 Transparent data-in	H	L	L	L	L	H	X	D1-D16, DP1, DP2
Word Write Cycle DQ1-DQ16, DQP1, DQP2 Latched data-in	H	L	L	L	L	L	X	D1-D16, DP1, DP2
Aborted Write Cycle	H	L	L	H	H	X	X	High-Z
Byte Write Cycle DQ1-DQ8, DQP1 Transparent data-in	H	L	L	L	H	H	X	D1-D8, DP1
Byte Write Cycle DQ9-DQ16, DQP2 Transparent data-in	H	L	L	H	L	H	X	D9-D16, DP2
Byte Write Cycle DQ1-DQ8, DQP1 Latched data-in	H	L	L	L	H	L	X	D1-D8, DP1
Byte Write Cycle DQ9-DQ16, DQP2 Latched data-in	H	L	L	H	L	L	X	D9-D16, DP2

NOTE:
1. Registered inputs (Addresses, $\overline{SWE}$, SCE, and $\overline{SCE}$) must satisfy the specified setup and hold times around the rising edge of clock (CLK). Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the WRITE cycle.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold times.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} supply relative to V_{SS}/V_{SSQ} ..... -1.0V to +7.0V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = V_{SSQ}$, Unless Otherwise Noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1
Output Buffer Supply Voltage	5.0V TTL Compatible	V_{CCQ}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{SCE} \le V_{IL}$; $SCE \ge V_{IH}$; f = MAX; V_{CC} = MAX; Outputs Open	I_{CC}	150	300	mA	3
Power Supply Current: Standby	$SCE \le V_{IL}$; $\overline{SCE} \ge V_{IH}$; V_{CC} = MAX; f = MAX	I_{SB1}	20	50	mA	
	$\overline{SCE} \ge V_{CC}$ -0.2; $SCE \le V_{SS}$ +0.2; V_{CC} = MAX; $V_{IL} \le V_{SS}$ +0.2; $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}	8	15	mA	
	f = 0, $\overline{SCE} \le V_{IL}$; $\overline{SCE} \le V_{IH}$; V_{CC} = MAX	I_{SB3}	10	25	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		6	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$; Vcc = VccQ = 5V ± 10%)

		-15		-17		-20		-25			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	tKC	15		17		20		25		ns	
Clock high time	tKH	4		4		4		4		ns	
Clock low time	tKL	8		8		8		8		ns	
Chip Enable											
SCE/$\overline{SCE}$ setup time	tSCES	2		2		2		2		ns	10
SCE/$\overline{SCE}$ hold time	tSCEH	2		2		2		2		ns	10
Address											
Address setup time	tSAS	2		2		2		2		ns	10
Address hold time	tSAH	2		2		2		2		ns	10
READ Cycle											
READ cycle time	tRC	15		17		20		25		ns	11
Clock to output valid	tKQ		15		17		20		25	ns	
Clock to output invalid	tKQX	3		3		3		3		ns	10
Clock to output in Low-Z	tKQLZ	10		10		10		10		ns	6, 7
Clock to output in High-Z	tKQHZ	3	8	3	8	3	8	3	12	ns	6, 7
$\overline{SWE}$ setup time	tSWNS	2		2		2		2		ns	10
$\overline{SWE}$ hold time	tSWNH	2		2		2		2		ns	10
$\overline{OE}$ to output valid	tOEQ		6		7		8		10	ns	
$\overline{OE}$ to output in Low-Z	tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	tOEHZ		8		8		8		8	ns	6, 7
WRITE Cycle											
WRITE cycle time	tWC	15		17		20		25		ns	11
$\overline{SWE}$ setup time	tSWES	2		2		2		2		ns	10
$\overline{SWE}$ hold time	tSWEH	2		2		2		2		ns	10
Data setup time	tDS	5		6		6		7		ns	8, 10
Data hold time	tDH	2		2		2		2		ns	8, 10
Data to DLE not setup time	tDLNS	1		1		1		1		ns	9, 10
Data to DLE not hold time	tDLNH	3		3		3		3		ns	9, 10
DLE setup time	tDLS	6		6		6		7		ns	9, 10
DLE hold time	tDLH	2		2		2		2		ns	9, 10
$\overline{WEL}$ / $\overline{WEH}$ setup time	tWES	6		6		6		7		ns	10
$\overline{WEL}$ / $\overline{WEH}$ hold time	tWEH	2		2		2		2		ns	10
$\overline{WEL}$ / $\overline{WEH}$ not setup time	tWNS		0		0		0		0	ns	10
$\overline{WEL}$ / $\overline{WEH}$ not hold time	tWNH	2		2		2		2		ns	10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

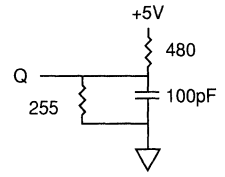


Fig. 1 OUTPUT LOAD EQUIVALENT

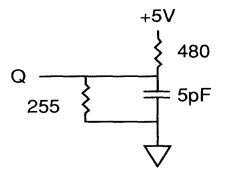
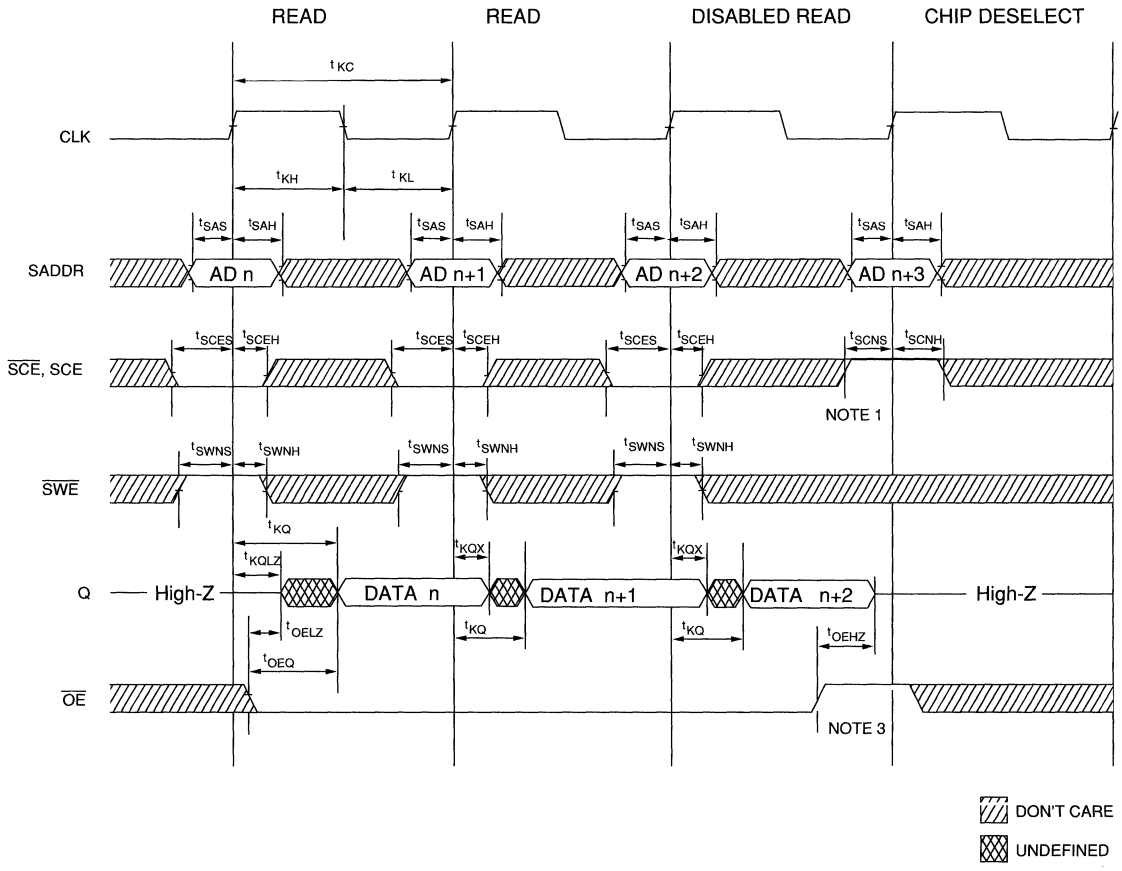


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

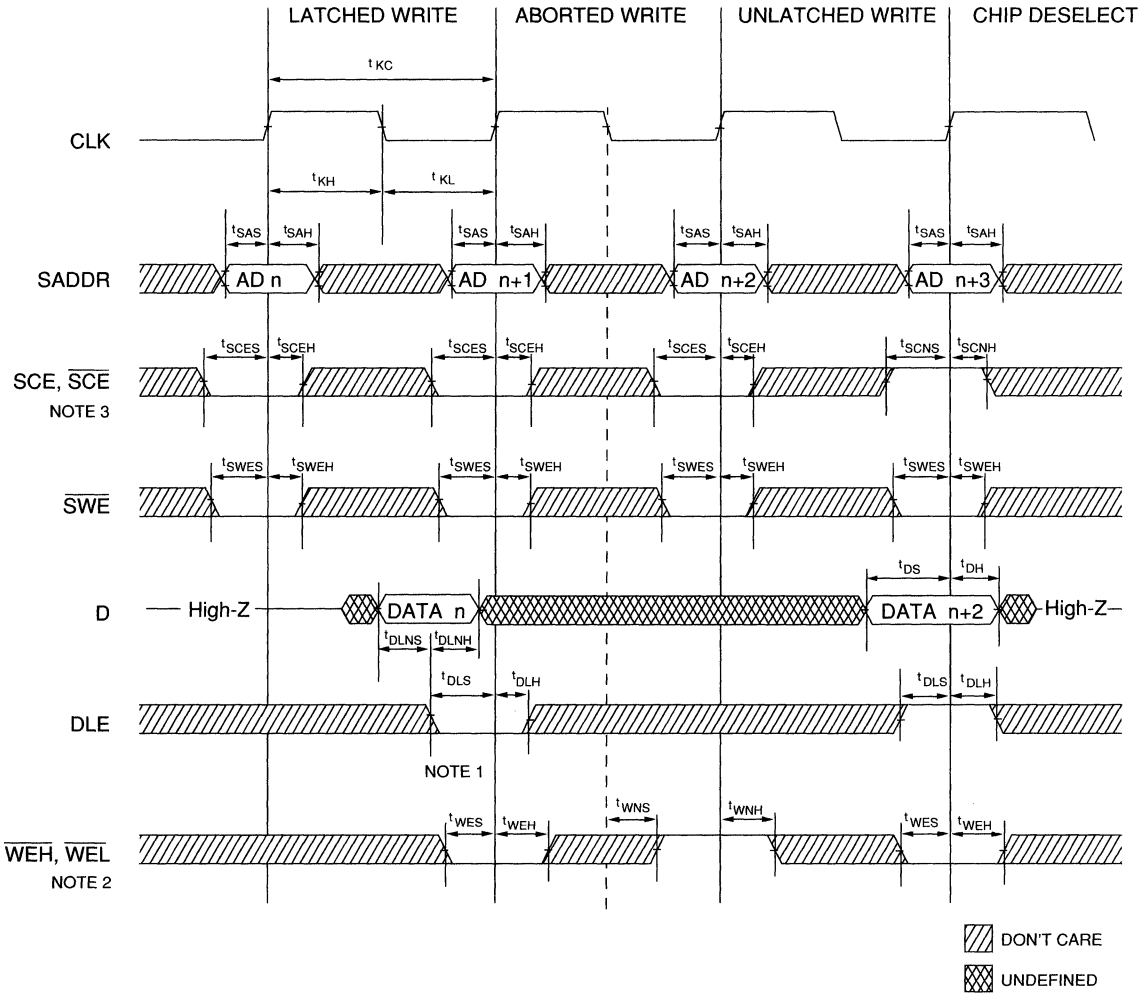
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}KQHZ is less than ^{t}KQLZ and ^{t}OEHZ is less than ^{t}OELZ.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and satisfying the specified setup and hold time with respect to the rising edge of clock (CLK).
10. This is a synchronous device. All synchronous inputs must meet the setup and hold times with stable logic levels for all falling edges of address latch enable (ALE) and data latch enable (DLE).
11. ^{t}RC = ^{t}WC = ^{t}KC

READ TIMING [2]



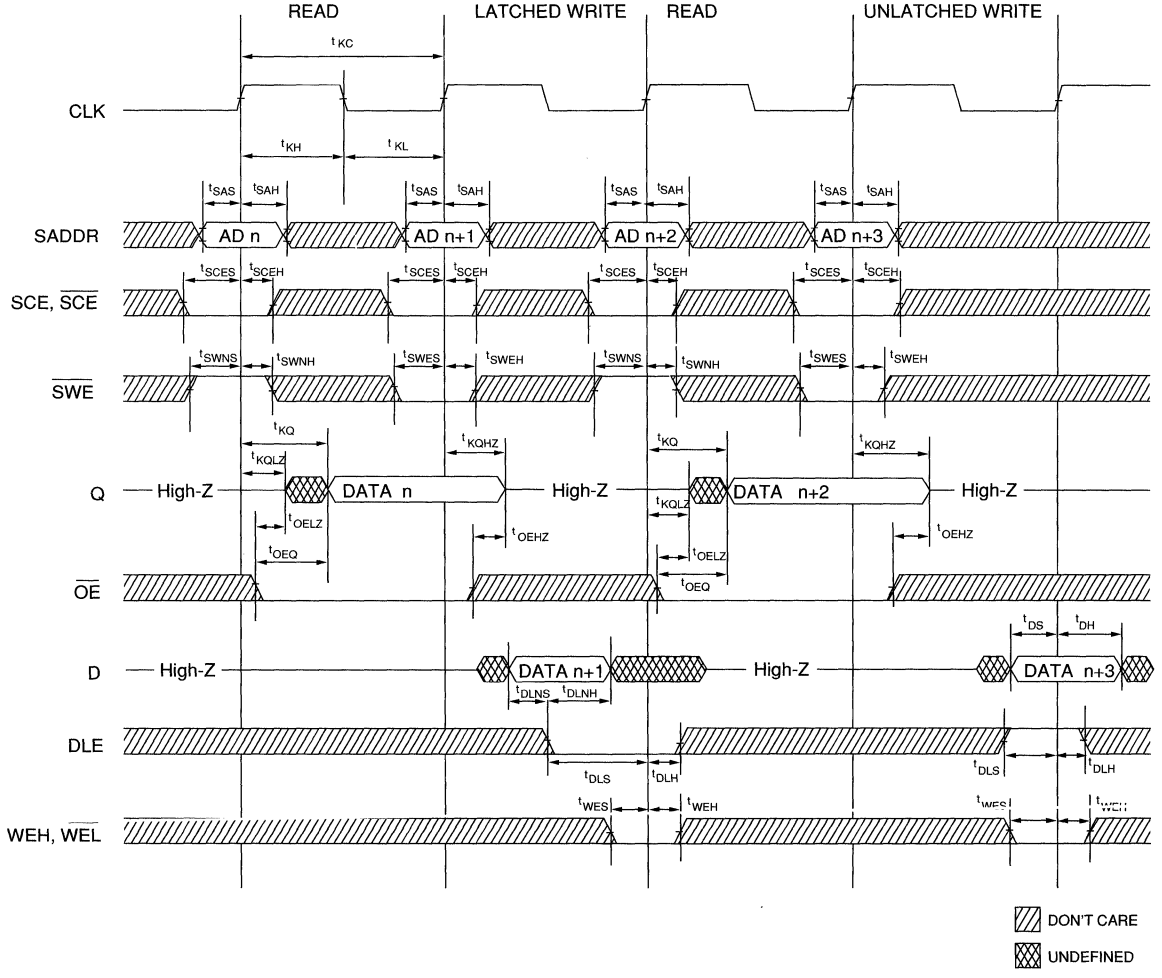
NOTE:
1. When synchronous chip enables (SCE, $\overline{SCE}$) are inactive, the part is deselected.
2. $\overline{WEL}$ / $\overline{WEH}$ are Don't Care signals during a READ cycle.
3. Data out (Q) is disabled whenever asynchronous output enable ($\overline{OE}$) is inactive, during a READ cycle.

WRITE TIMING



NOTE:
1. Data is latched when DLE transitions from HIGH to LOW. When DLE is HIGH, the latch is transparent and data flows through the latch.
2. Asynchronous write enables ($\overline{WEH}$, $\overline{WEL}$) are available for use as byte write enables at the system level. They are also available to perform a late WRITE cycle abort.
3. When synchronous chip enables (SCE, $\overline{SCE}$) are inactive, the part is deselected.

READ/WRITE TIMING



MICRON TECHNOLOGY, INC.

SRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Package and No. of Pins		Process	Page
				DIP	ZIP		
128K x 8	CE & OE	MT4S1288	30, 35, 45	32	-	CMOS	6-1
32K x 16	CE & OE	MT2S3216	30, 35, 45	40	-	CMOS	6-9
64K x 16	CE & OE	MT4S6416	30, 35, 45	40	-	CMOS	6-17
16K x 32	CE & OE	MT8S1632	15, 20, 25, 30, 35, 45	-	64	CMOS	6-25
64K x 32	CE & OE	MT8S6432	20, 25, 30, 35, 45	-	64	CMOS	6-33
128K x 32	CE & OE	MT4S12832	25, 35, 45	-	64	CMOS	6-41
256K x 32	CE & OE	MT8S25632	25, 35, 45	-	64	CMOS	6-49

SRAM MODULE

128K x 8 SRAM

FEATURES

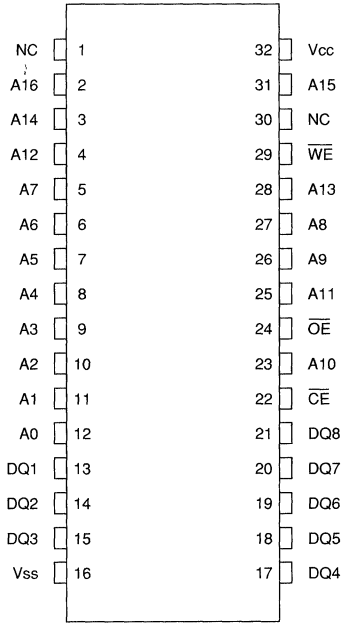
- High speed: 30ns, 35ns, and 45ns
- High-performance, low-power CMOS process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ function
- All inputs and outputs are TTL compatible
- Pin compatible with monolithic 1 Meg SRAM

OPTIONS

	MARKING
• Timing	
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
32-pin DIP (600 mil)	D
• 2V data retention (Available in 45ns, CMOS decoder version only)	L

PIN ASSIGNMENT (Top View)

32-Pin DIP
(K-1)



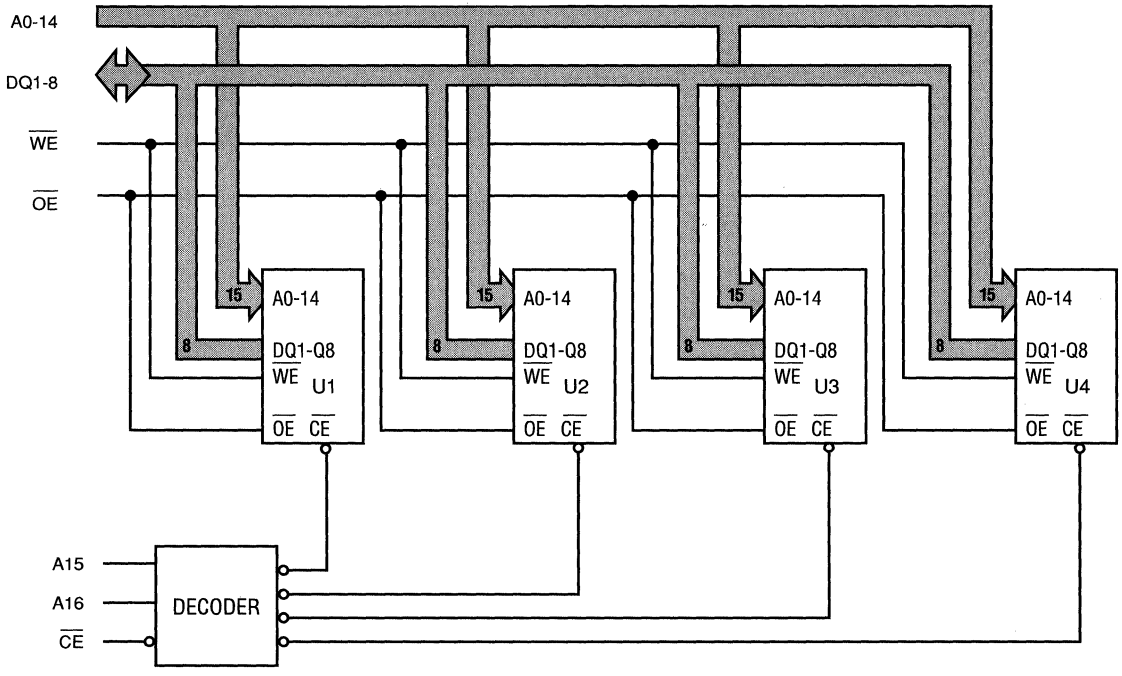
GENERAL DESCRIPTION

The MT4S1288 is a high-speed SRAM memory module containing 131,072 words organized in a x8-bit configuration. The module consists of four 32K x 8 fast static RAMs and a single decoder mounted on a 32-pin DIP, FR4 printed circuit board. Depending upon the speed of the module, the decoder will be either TTL (30ns and 35ns) or CMOS (45ns).

The decoder interprets the higher order address bits (A15 and A16) to select one of the four fast static RAMs. Data is written into the SRAM memory when both write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are LOW. Reading is accomplished when $\overline{WE}$ remains HIGH, and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ sets the output in a high impedance state for additional system design flexibility, and memory expansion may be achieved through use of the $\overline{OE}$ and $\overline{CE}$ functions.

The Micron SRAM family uses high-speed, low-power CMOS designs featuring a four-transistor memory cell and double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V DC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5C2568DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5.0V ± 10%)

					MAX			
DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**-30, -35**	**-45**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage			V_{IH}	2.2	Vcc+1	Vcc+1	V	
Input Low (Logic 0) Voltage			V_{IL}	-0.5	0.8	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	A0-A14, $\overline{WE}$, $\overline{OE}$	I_{LI}	-20	20	20	µA	
		A15, A16, $\overline{CE}$			600	1.0	µA	
Input/Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	DQ1-DQ8	I_{LO}	-20	20	20	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4			V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}	0.4	0.4	0.4	V	1

				MAX			
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**-30, -35**	**-45**	**UNITS**	**NOTES**
Operating Current: TTL Input Levels	$\overline{CE} \le V_{IL}$; Vcc = MAX; f = MAX = 1/ ^tRC, Outputs Open	I_{CC}		190	180	mA	3
Standby Current: TTL Input Levels	$\overline{CE} \ge V_{IH}$, Vcc = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}		120	100	mA	
Standby Current: CMOS Input Levels	$\overline{CE} \ge V_{CC}$ -0.2; Vcc = MAX $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}		40	20	mA	

CAPACITANCE

				MAX			
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**-30, -35**	**-45**	**UNITS**	**NOTES**
Input Capacitance: A0-A14 $\overline{WE}$, & $\overline{OE}$	T_A = 25°C; f = 1MHz Vcc = 5V	C_{I1}		28	28	pF	4
Input Capacitance: A15, A16, & $\overline{CE}$		C_{I2}		5	4.5	pF	4
Input/Output Capacitance: DQ1-DQ8		C_{IO}		28	28	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ± 10%)

DESCRIPTION	SYM	-30		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	^tRC	30		35		45		ns	
Address access time	^tAA		30		35		45	ns	
Chip Enable access time	^tACE		30		35		45	ns	
Output hold from address change	^tOH	5		5		5		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip Enable to output in High-Z	^tHZCE		20		20		25	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		30		35		45	ns	
Output Enable access time	^tAOE		10		12		15	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		10		12		15	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	25		30		35		ns	
Chip Enable to end of write	^tCW	25		30		30		ns	
Address Valid to end of write	^tAW	18		20		25		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
Write pulse width	^tWP	25		25		30		ns	
Data setup time	^tDS	15		15		20		ns	
Data hold time	^tDH	0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	0		0		0		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		12		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

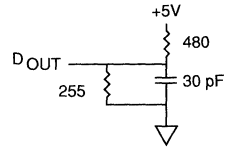


Fig. 1 OUTPUT LOAD EQUIVALENT

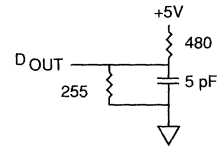


Fig. 2 OUTPUT LOAD EQUIVALENT

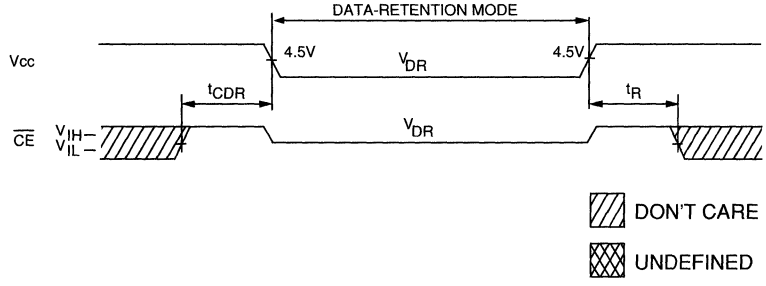
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE, and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All $\overline{CE}$s held in their active state.
10. Address valid prior to or coincident with latest occurring $\overline{CE}$.
11. The ouptut will be in the High-Z state if $\overline{OE}$ is High.
12. The first falling edge of either $\overline{CE}$ or $\overline{WE}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{CE}$ or $\overline{WE}$ will terminate a WRITE cycle.

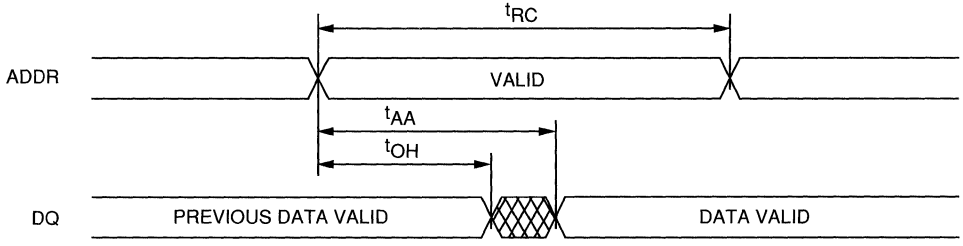
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	I_{CCDR}		0.5	2	mA	
		Vcc = 3v			1.5	3	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

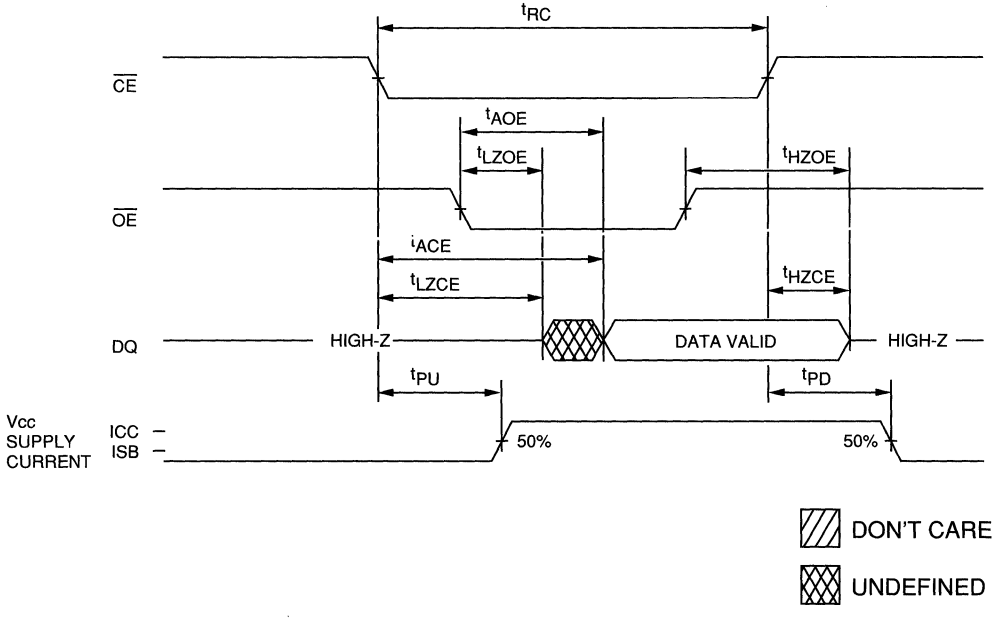
LOW Vcc DATA-RETENTION WAVEFORM



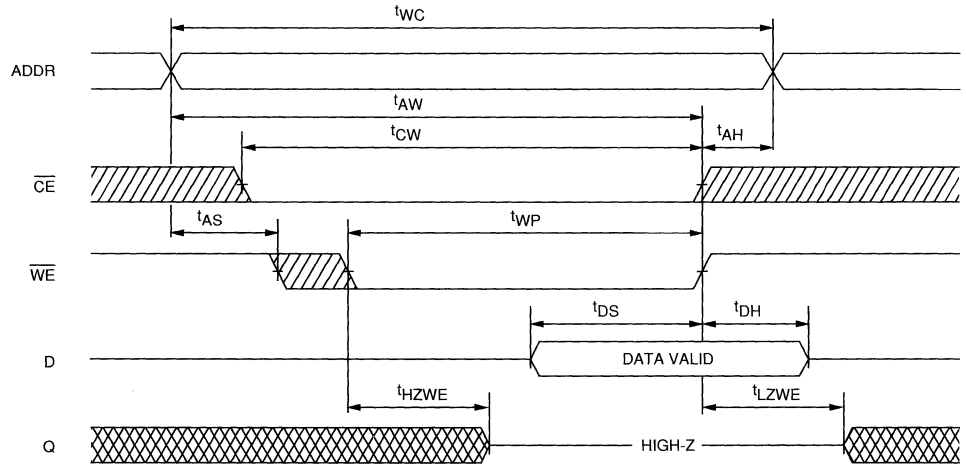
READ CYCLE NO. 1 [8, 9]



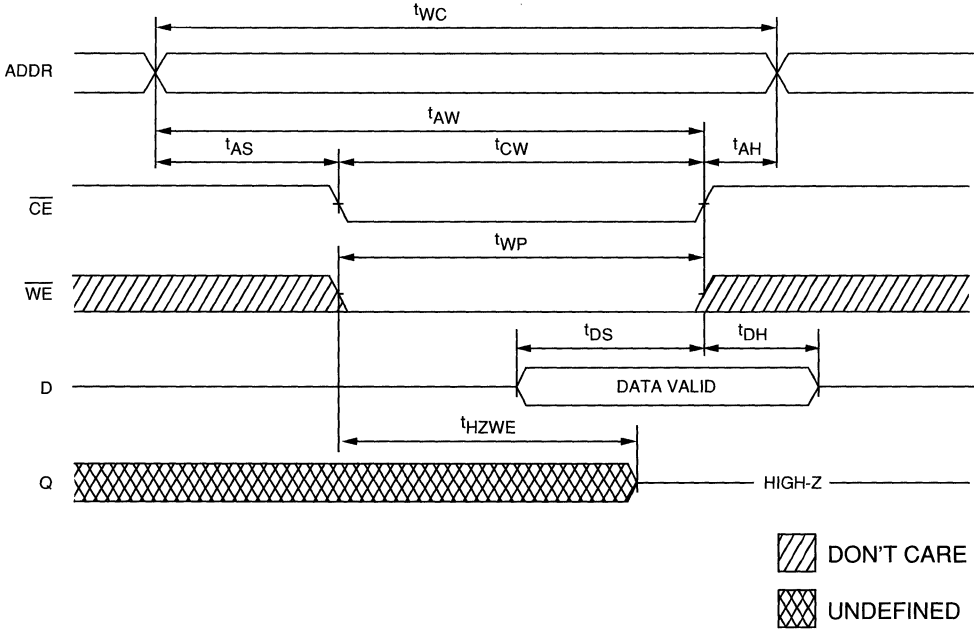
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Write Enable Controlled) [11, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [11, 12]



SRAM MODULE

32K x 16 SRAM

FEATURES

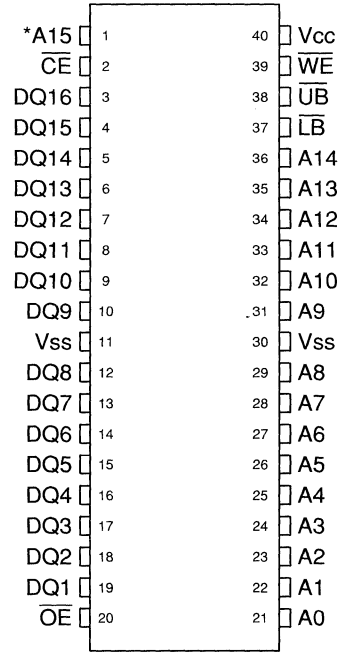
- High speed: 30ns, 35ns and 45ns
- High-performance, low-power CMOS process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ function
- Upper and Lower Byte Select
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
40-pin DIP (600 mil)	D
• 2V data retention	L
(Available in 45ns, CMOS decoder versions only)	

PIN ASSIGNMENT (Top View)

40-Pin DIP
(K-2)



* Address A15 must be connected to Vss

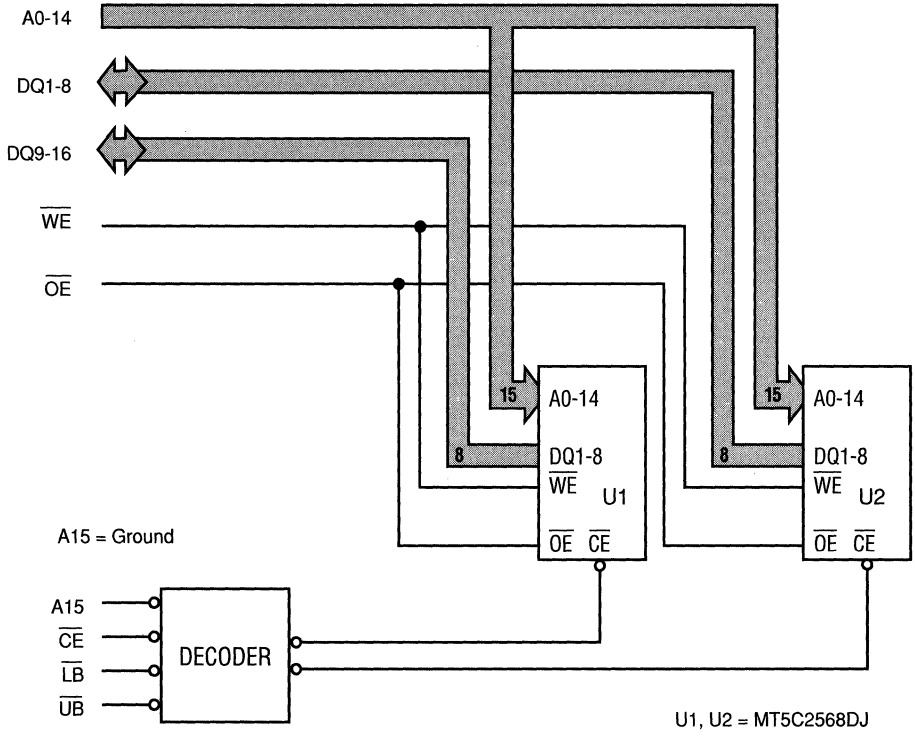
GENERAL DESCRIPTION

The MT2S3216 is a high-speed SRAM memory module containing 32,768 words organized in a x16-bit configuration. The module consists of two 32K x 8 fast static RAMs and a single decoder mounted on a 40-pin DIP, FR4 printed circuit board. Depending upon the speed of the module, the decoder will be either TTL (30ns and 35ns) or CMOS (45ns).

Data is written into the SRAM memory when both write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are LOW. Reading occurs when $\overline{WE}$ remains HIGH, and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{LB}$ and $\overline{UB}$ control the lower and upper byte selection. $\overline{CE}$ sets the output in a high impedance state for additional system design flexibility, and memory expansion may be achieved through use of the $\overline{CE}$ functions.

The Micron SRAM family uses high-speed, low-power CMOS designs featuring a four-transistor memory cell and double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V DC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	A15	DQ OPERATION	POWER
STANDBY	H	X	X	X	X	L	HIGH-Z	STANDBY
STANDBY	L	H	H	X	X	L	HIGH-Z	STANDBY
READ: WORD	L	L	L	L	H	L	Q (1-16)	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	L	H	L	Q (1-8)	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	L	H	L	Q (9-16)	ACTIVE (x8)
READ: WORD	L	L	L	H	H	L	HIGH-Z	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	H	H	L	HIGH-Z	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	H	H	L	HIGH-Z	ACTIVE (x8)
WRITE: WORD	L	L	L	X	L	L	D (1-16)	ACTIVE (x16)
WRITE: LOWER BYTE	L	H	L	X	L	L	D (1-8)	ACTIVE (x8)
WRITE: UPPER BYTE	L	L	H	X	L	L	D (9-16)	ACTIVE (x8)

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} .....-1.0V to +7.0V
Storage Temperature .....-55°C to +150°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX -30, -35	MAX -45	UNITS	NOTES
Input High (Logic 1) Voltage	A0-A14, $\overline{WE}$, $\overline{OE}$		V_{IH}	2.2	Vcc+1	Vcc+1	V	
	A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$		V_{IH}	2.0	Vcc+1	Vcc+1	V	
Input Low (Logic 0) Voltage	A0-A14, $\overline{WE}$, $\overline{OE}$		V_{IL}	-0.5	0.8	0.8	V	1, 2
	A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$		V_{IL}	-0.5	0.8	0.9	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	A0-A14, $\overline{WE}$ $\overline{OE}$	I_{LI}	-10	10	10	µA	
		A15, $\overline{CE}$			1200	2.0	µA	
		$\overline{UB}$, $\overline{LB}$			600	1.0	µA	
Input/Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	DQ1-DQ16	I_{LO}	-5	5	5	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4			V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	0.4	V	1

DESCRIPTION		CONDITIONS	SYMBOL	MIN	MAX -30, -35	MAX -45	UNITS	NOTES
Operating Current: TTL Input Levels	(x16)	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}		210	200	mA	3
	(x8)				140	130		
Standby Current: TTL Input Levels		$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX =1/ ^tRC, Outputs Open	I_{SB1}		70	50	mA	
Standby Current: CMOS Input Levels		$\overline{CE} \ge V_{CC}$ -0.2; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}		35	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX -30, -35	MAX -45	UNITS	NOTES
Input Capacitance: A0-A14, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1MHz Vcc = 5V	C_{I1}		14	14	pF	4
Input Capacitance: A15, $\overline{CE}$		C_{I2}		10	9	pF	4
Input Capacitance: $\overline{UB}$, $\overline{LB}$		C_{I3}		5	4.5	pF	4
Input/Output Capacitance: DQ		C_{IO}		7	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ± 10%)

DESCRIPTION	SYM	-30		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	^tRC	30		35		45		ns	
Address access time	^tAA		30		35		45	ns	
Chip Enable access time	^tACE		30		35		45	ns	
Output hold from address change	^tOH	5		5		5		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip Enable to output in High-Z	^tHZCE		20		20		25	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		30		35		45	ns	
Output Enable access time	^tAOE		10		12		15	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		10		12		15	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	25		30		35		ns	
Chip Enable to end of write	^tCW	25		30		30		ns	
Address valid to end of write	^tAW	18		20		25		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE command pulse width	^tWP	25		25		30		ns	
Data setup time	^tDS	15		15		20		ns	
Data hold time	^tDH	0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	0		0		0		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		12		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

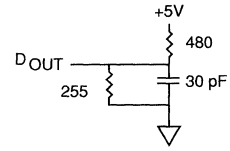


Fig. 1 OUTPUT LOAD EQUIVALENT

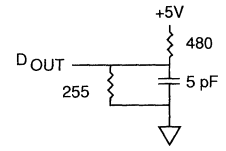


Fig. 2 OUTPUT LOAD EQUIVALENT

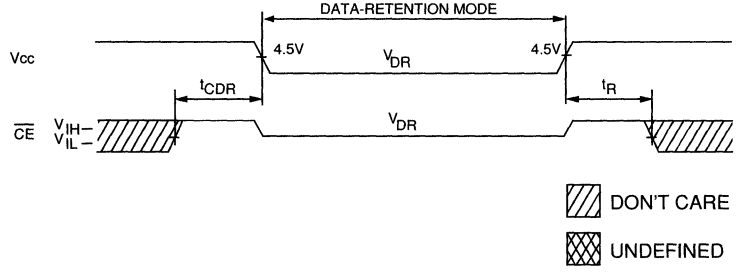
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. The ouptut will be in the High-Z state if $\overline{OE}$ is High.
12. The first falling edge of either $\overline{CE}$ or $\overline{WE}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{CE}$ or $\overline{WE}$ will terminate a WRITE cycle.

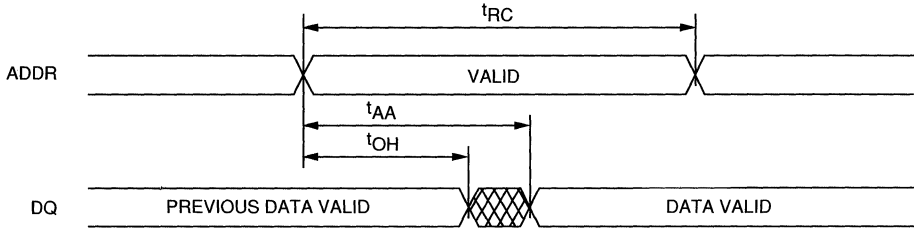
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		0.3	1.0	mA	
		Vcc = 3v			0.8	1.6	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

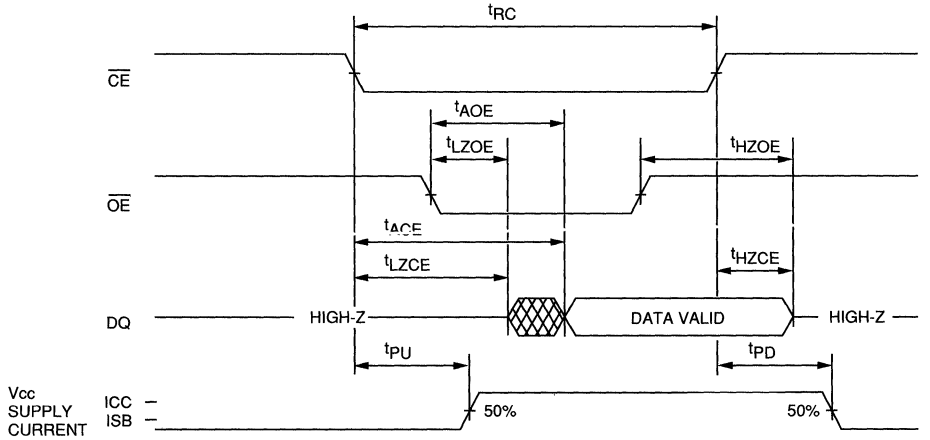
LOW Vcc DATA-RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



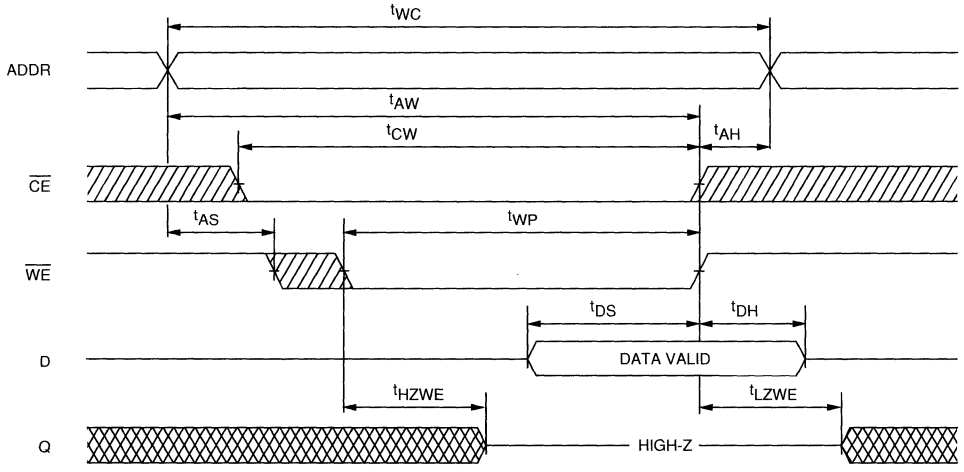
READ CYCLE NO. 2 [7, 8, 10]



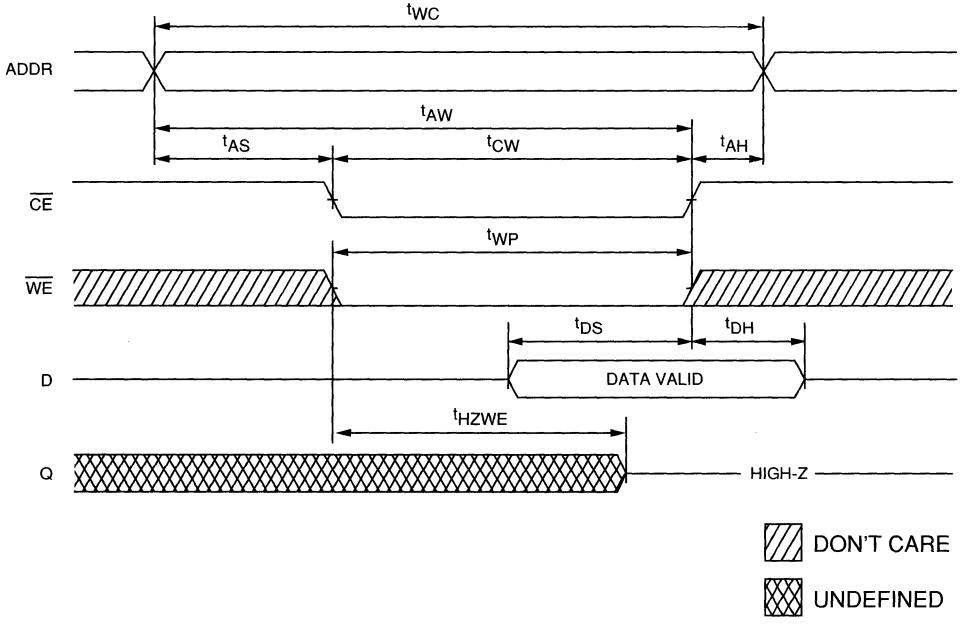
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled) [11, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [11, 12]



(REPLACES: MT85C1664)

SRAM MODULE

64K x 16 SRAM

FEATURES

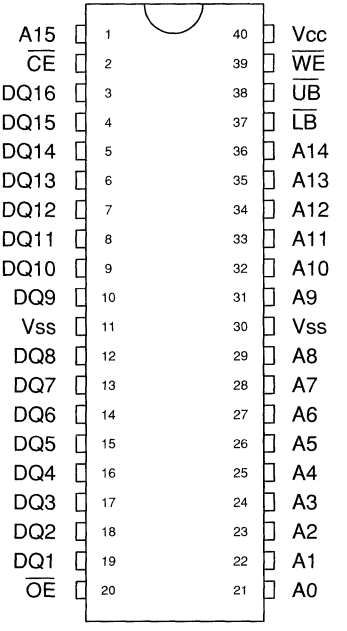
- High speed: 30ns, 35ns and 45ns
- High-performance, low-power, CMOS process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ function
- Upper and Lower Byte Select
- All inputs and outputs are TTL compatible

OPTIONS — MARKING

- Timing
  - 30ns access — -30
  - 35ns access — -35
  - 45ns access — -45
- Packages
  - 40-pin DIP (600 mil) — D
- 2V data retention — L
  (Available in the 45ns, CMOS decoder version only)

PIN ASSIGNMENT (Top View)

40-Pin DIP
(K-3)



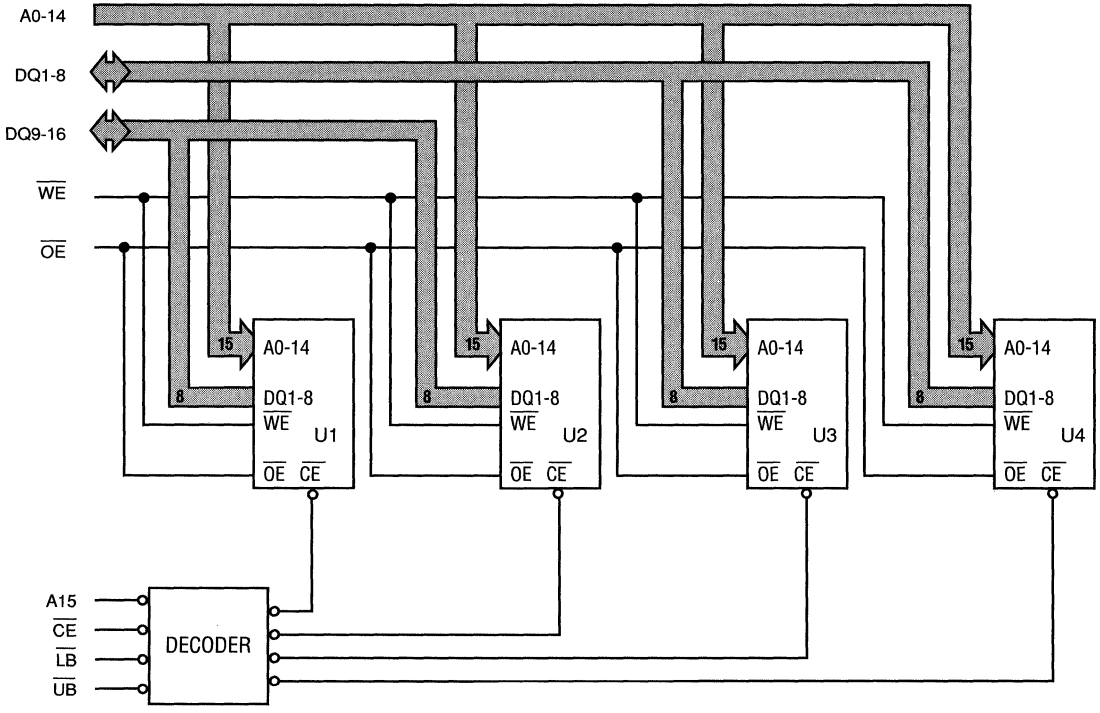
GENERAL DESCRIPTION

The MT4S6416 is a high-speed SRAM memory module containing 65,536 words organized in a x16-bit configuration. The module consists of four 32K x 8 fast static RAMs and a single decoder mounted on a 40-pin DIP, double-sided FR4 printed circuit board. Depending upon the speed of the module, the decoder will be either TTL (30ns and 35ns) or CMOS (45ns).

The decoder interprets the higher order address bit (A15) to select two of the four fast static RAMs. Data is written into the SRAM memory when both write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are LOW. Reading occurs when $\overline{WE}$ remains HIGH, and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{LB}$ and $\overline{UB}$ control the lower and upper byte selection. $\overline{CE}$ sets the output in a high-impedance state for additional system design flexibility, and memory expansion may be achieved through use of the $\overline{OE}$ function.

The Micron SRAM family uses high-speed, low-power CMOS designs featuring a four-transistor memory cell and double-layer metal, double-layer polysilicon technology. All module components can be powered from a single +5V DC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5C2568DJ

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	DQ OPERATION	POWER
STANDBY	H	X	X	X	X	HIGH-Z	STANDBY
STANDBY	L	H	H	X	X	HIGH-Z	STANDBY
READ: WORD	L	L	L	L	H	Q (1-16)	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	L	H	Q (1-8)	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	L	H	Q (9-16)	ACTIVE (x8)
READ: WORD	L	L	L	H	H	HIGH-Z	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	H	H	HIGH-Z	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	H	H	HIGH-Z	ACTIVE (x8)
WRITE: WORD	L	L	L	X	L	D (1-16)	ACTIVE (x16)
WRITE: LOWER BYTE	L	H	L	X	L	D (1-8)	ACTIVE (x8)
WRITE: UPPER BYTE	L	L	H	X	L	D (9-16)	ACTIVE (x8)

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Storage Temperature .....-55°C to +150°C
Power Dissipation 4W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5.0V ± 10%)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX -30, -35	MAX -45	UNITS	NOTES
Input High (Logic 1) Voltage		A0-A14, $\overline{WE}$, $\overline{OE}$	VIH	2.2	Vcc+1	Vcc+1	V	
		A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$	VIH	2.0	Vcc+1	Vcc+1	V	
Input Low (Logic 0) Voltage		A0-A14, $\overline{WE}$, $\overline{OE}$	VIL	-0.5	0.8	0.8	V	1, 2
		A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$	VIL	-0.5	0.8	1.3	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ Vcc	A0-A14	ILI	-40	40	40	µA	
		A15, $\overline{CE}$			1200	1.0	µA	
		$\overline{UB}$, $\overline{LB}$			600	1.0	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ VOUT ≤ Vcc		ILO	-20	20	20	µA	
Output High Voltage	IOH = -4.0mA		VOH	2.4			V	1
Output Low Voltage	IOL = 8.0mA		VOL		0.4	0.4	V	1

DESCRIPTION		CONDITIONS	SYMBOL	MIN	MAX -30, -35	MAX -45	UNITS	NOTES
Operating Current: TTL Input Levels	(x16)	$\overline{CE}$ ≤ VIL, Vcc = MAX f = MAX = 1/ ^tRC, Outputs Open	ICC		210	250	mA	3
	(x8)				105	150		
Standby Current: TTL Input Levels		$\overline{CE}$ ≥ VIH, Vcc = MAX f = MAX = 1/ ^tRC, Outputs Open	ISB1		120	100	mA	
Standby Current: CMOS Input Levels		$\overline{CE}$ ≥ Vcc -0.2, Vcc = MAX VIL ≤ Vss +0.2, VIH ≥ Vcc -0.2, f = 0	ISB2		40	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX -30, -35	MAX -45	UNITS	NOTES
Input Capacitance: A0-A14, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1MHz Vcc=5V	CI1		32	16	pF	4
Input Capacitance: A15, $\overline{CE}$		CI2		10	9	pF	4
Input Capacitance: $\overline{UB}$, $\overline{LB}$		CI3		5	4.5	pF	4
Input/Output Capacitance: DQ		CIO		16	16	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ± 10%)

DESCRIPTION	SYM	-30		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	^tRC	30		35		45		ns	
Address access time	^tAA		30		35		45	ns	
Chip Enable access time	^tACE		30		35		45	ns	
Output hold from address change	^tOH	5		5		5		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip Enable to output in High-Z	^tHZCE		20		20		25	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		30		35		45	ns	
Output Enable access time	^tAOE		20		20		25	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		20		20		30	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	30		35		45		ns	
Chip Enable to end of write	^tCW	25		30		30		ns	
Address valid to end of write	^tAW	25		25		30		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	2		2		2		ns	
Write command pulse width	^tWP	25		25		30		ns	
Data setup time	^tDS	15		15		18		ns	
Data hold time	^tDH	0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	0		0		0		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		20		15		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

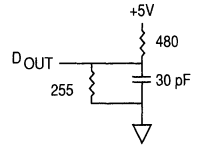


Fig. 1 OUTPUT LOAD EQUIVALENT

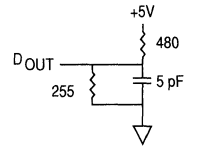


Fig. 2 OUTPUT LOAD EQUIVALENT

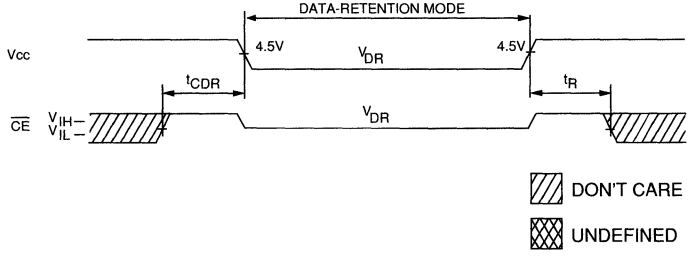
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE and ^{t}HZWE are less than ^{t}LZCE and ^{t}LZWE respectively.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. The ouptut will be in the High-Z state if $\overline{OE}$ is High.
12. The first falling edge of either $\overline{CE}$ or $\overline{WE}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{CE}$ or $\overline{WE}$ will terminate a WRITE cycle.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

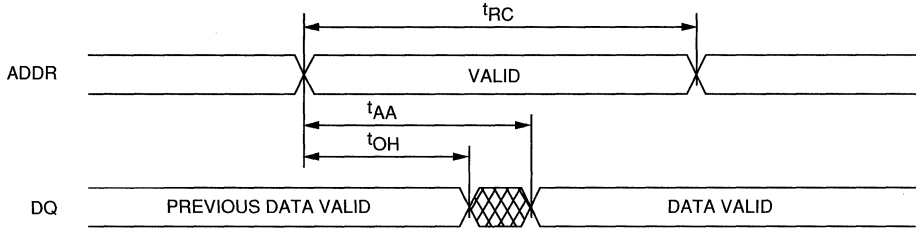
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	CE ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v			0.5	2	mA	
		Vcc = 3v			1.5	3	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

LOW Vcc DATA-RETENTION WAVEFORM

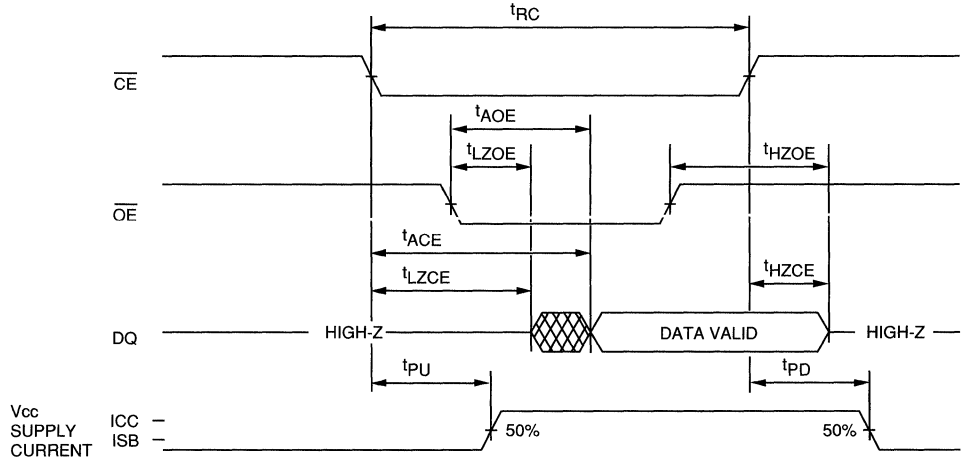


SRAM MODULE

READ CYCLE NO. 1 [8, 9]



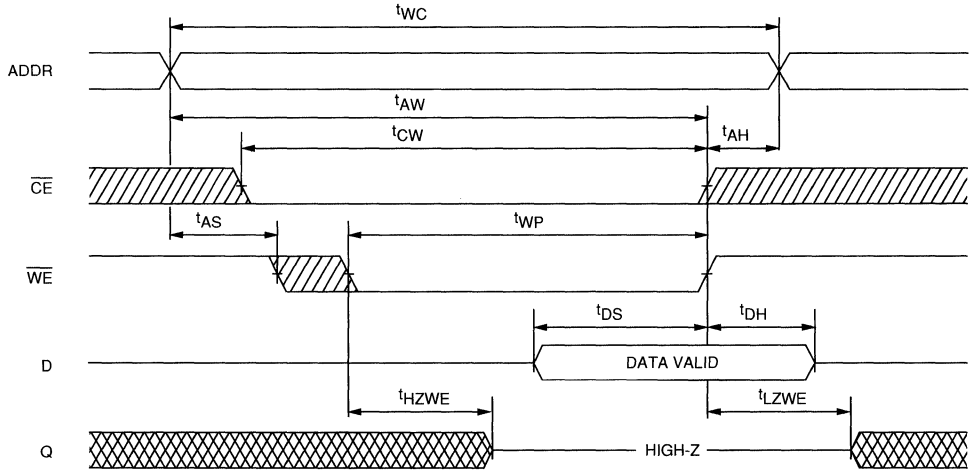
READ CYCLE NO. 2 [7, 8, 10]



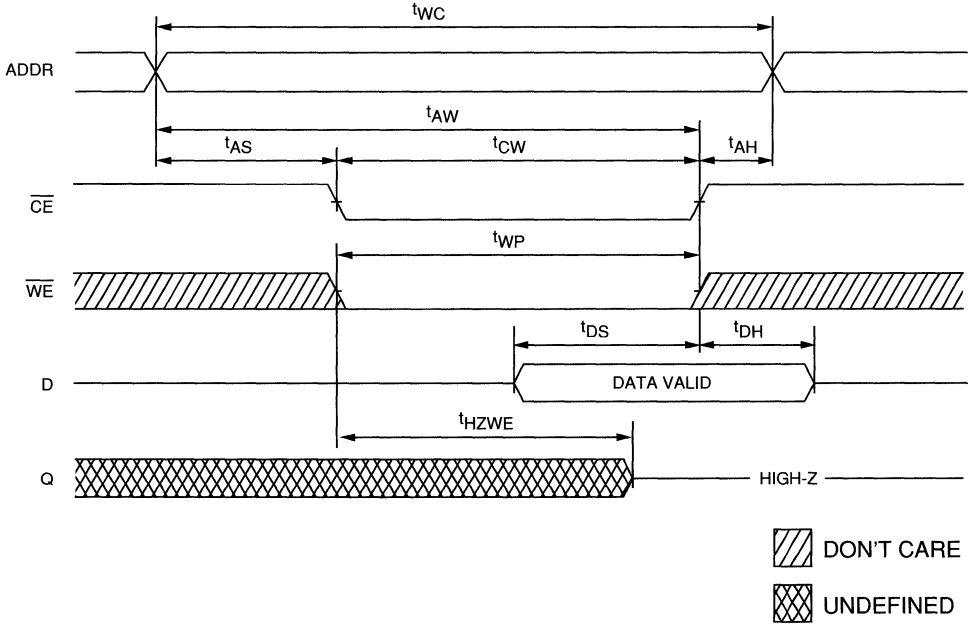
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled) [11, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [11, 12]



SRAM MODULE

16K x 32 SRAM

FEATURES

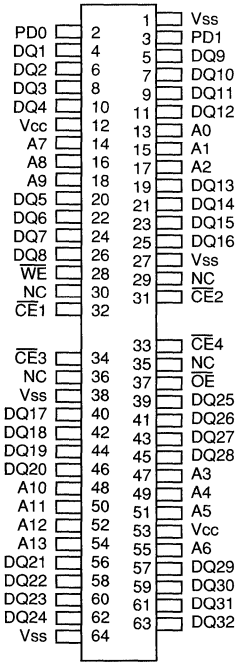
- High speed: 15ns, 20ns, 25ns, 30ns, 35ns and 45ns
- High-performance, low-power, CMOS process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Low profile (.50 inches MAX height)
- All inputs and outputs are TTL compatible
- Industry standard pinout
- Pin compatible with 64K x 32, 128K x 32 and 256K x 32 modules

OPTIONS

OPTIONS	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
64-pin ZIP	Z
• 2V data retention	L

PIN ASSIGNMENT (Top View)

64-Pin ZIP
(J-1)



GENERAL DESCRIPTION

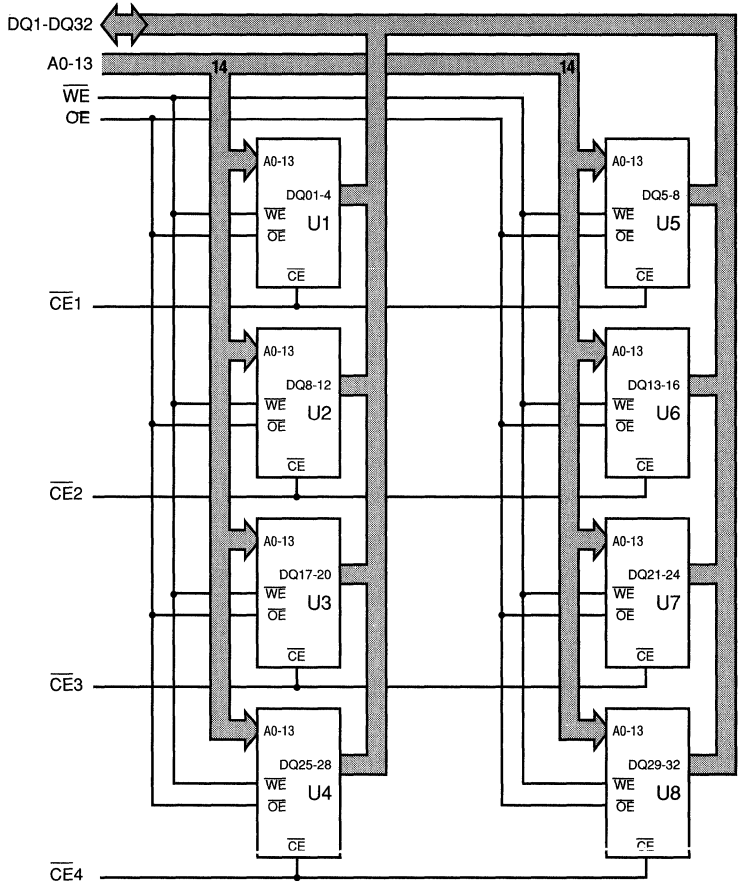
The MT8S1632 is a high-speed SRAM memory module containing 16,384 words organized in a x32-bit configuration. The module consists of eight 16K x 4 fast static RAMs mounted on a 64-pin ZIP, double-sided, FR4 printed circuit board.

Data is written into to the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ can set the output in a high-impedance state for additional flexibility in system design, and memory expansion is accomplished by use of the $\overline{OE}$ function.

PD0 and PD1 identify the module's density, allowing interchangeable use of alternate-density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$), are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5VDC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT5C6405DJ

PRESENCE DETECT
PD0 = Vss
PD1 = No Connect

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature ..... -55°C to +150°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-40	40	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-30, -35, -45	UNITS	NOTES
Operating Current: TTL Input Levels	$\overline{CE} \le V_{IL}$, V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	1040	960	880	800	mA	3
Standby Current: TTL Input Levels	$\overline{CE} \ge V_{IH}$, V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	400	320	240	240	mA	
Power Supply Current: Standby	$\overline{CE} \ge V_{CC}$ -0.2, V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2, f = 0	I_{SB2}	40	40	40	40	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: Ao-A13, $\overline{WE}$, $\overline{CE}$, $\overline{OE}$	T_A = 25°C; f = 1MHz	C_I		70	pF	4
Input/Output Capacitance: DQ1-DQ32	V_{CC} = 5V	$C_{I/O}$		15	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ± 10%)

DESCRIPTION		-15		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	15		20		25		30		35		45		ns	
Address access time	^tAA		15		20		25		30		35		45	ns	
Chip Enable access time	^tACE		12		15		20		25		30		40	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	3		5		5		5		5		5		ns	7
Chip Enable to output in High-Z	^tHZCE		7		10		10		15		20		20	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		15		20		25		30		35		45	ns	
Output Enable access time	^tAOE		7		9		10		15		20		20	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		6		10		10		15		20		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	15		20		25		30		35		45		ns	
Chip Enable to end of write	^tCW	12		15		20		25		25		30		ns	
Address valid to end of write	^tAW	12		15		20		25		25		30		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write command pulse width	^tWP	12		15		20		25		25		30		ns	
Data setup time	^tDS	8		10		10		15		15		20		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		6		8		10		12		15		20	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

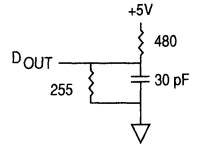


Fig. 1 OUTPUT LOAD EQUIVALENT

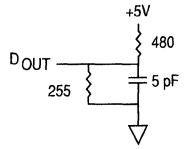


Fig. 2 OUTPUT LOAD EQUIVALENT

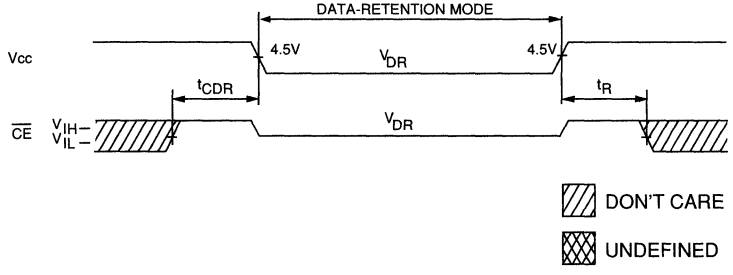
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. The ouptut will be in the High-Z state if $\overline{OE}$ is High.
12. The first falling edge of either $\overline{CE}$ or $\overline{WE}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{CE}$ or $\overline{WE}$ will terminate a WRITE cycle.

DATA RETENTION ELECTRICAL CHARACTERISTICS (-L Version Only)

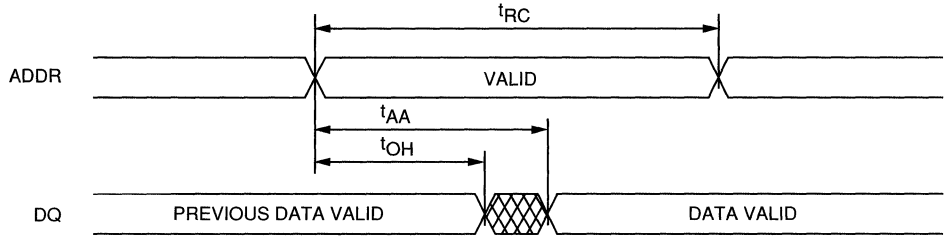
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2	—	V		
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		0.8	4	mA	
		Vcc = 3v			2.8	6	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

LOW Vcc DATA-RETENTION WAVEFORM

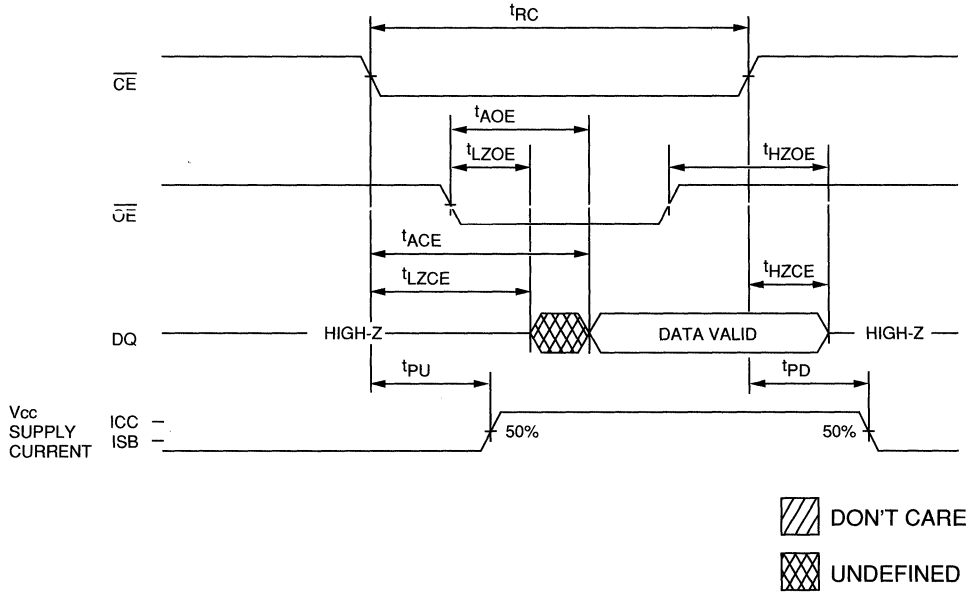


SRAM MODULE

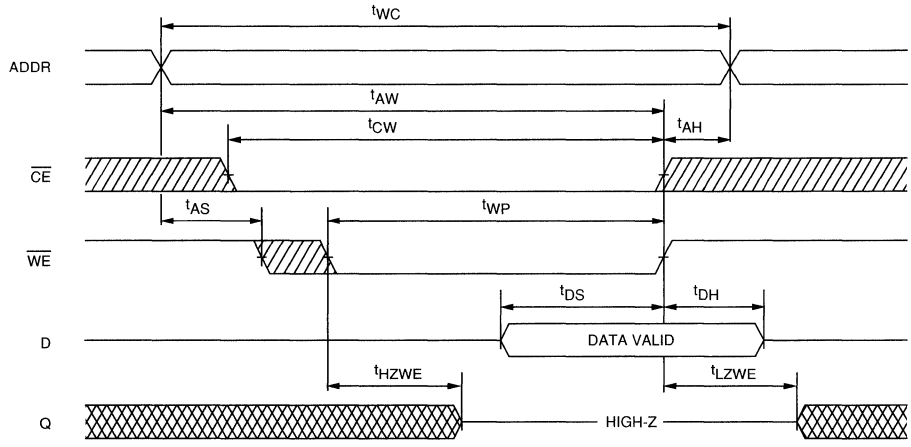
READ CYCLE NO. 1 [8, 9]



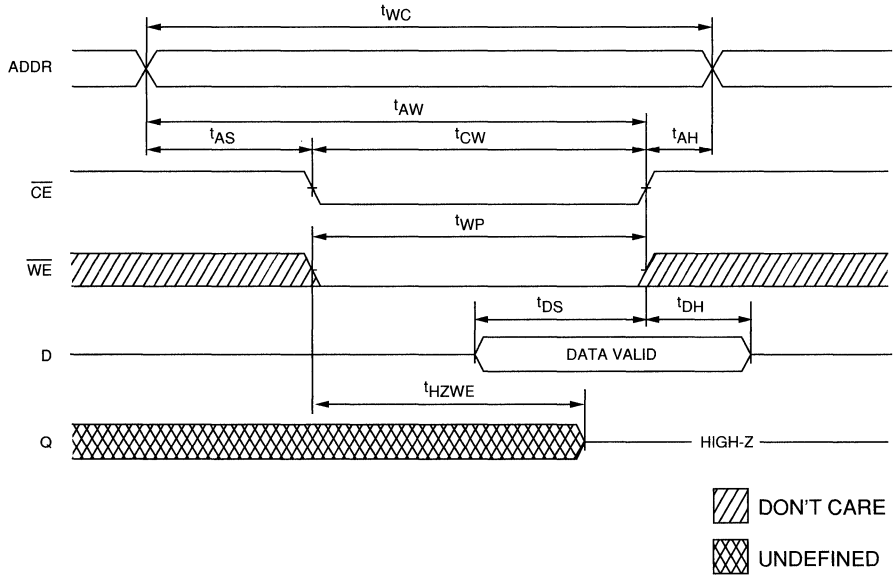
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Write Enable Controlled) [11, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [11, 12]



SRAM MODULE

64K x 32 SRAM

FEATURES

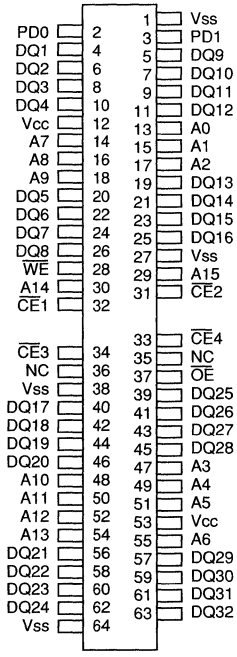
- Industry compatible pinout
- High speed: 20ns, 25ns, 30ns, 35ns and 45ns
- High-performance, low-power, CMOS process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ function
- Low profile (.50 inches MAX height)
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
64-pin ZIP	Z
• 2V data retention	L

PIN ASSIGNMENT (Top View)

64-Pin ZIP
(J-1)



GENERAL DESCRIPTION

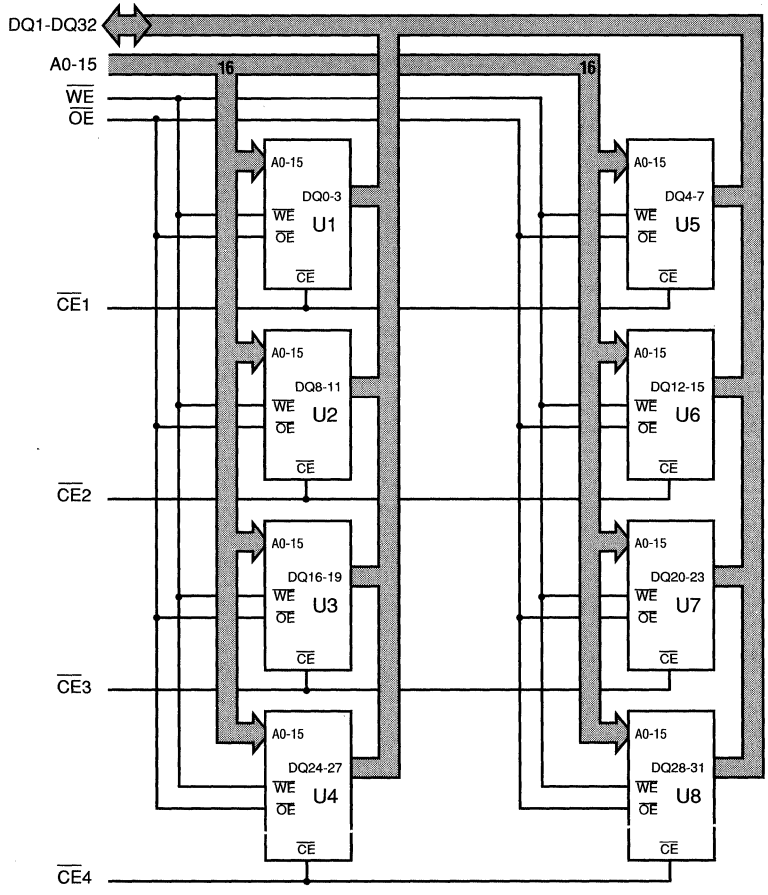
The MT8S6432 is a high-speed SRAM memory module containing 65,536 words organized in a x32-bit configuration. The module consists of eight 64K x 4 fast static RAMs mounted on a 64-pin ZIP, double-sided, FR4 printed circuit board.

Data is written into to the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ can set the output in a high-impedance state for additional flexibility in system design, and memory expansion is accomplished by use of the $\overline{OE}$ function.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5VDC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT5C2565DJ

PRESENCE DETECT
PD0 = No Connect
PD1 = Vss

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature ..... -55°C to +150°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5.0V ± 10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-40	40	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25, -30	-35, -45	UNITS	NOTES
Operating Current: TTL Input Levels	$\overline{CE} \le V_{IL}$, Vc c = MAX f = MAX = 1/ ^tRC, Outputs Open	Icc	840	760	720	mA	3
Standby Current: TTL Input Levels	$\overline{CE} \ge V_{IH}$, Vcc = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	240	200	200	mA	
Power Supply Current: Standby	$\overline{CE} \ge V_{CC}$ -0.2, Vcc = MAX $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2, f = 0	I_{SB2}	40	40	56	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: Ao-A13, $\overline{WE}$, $\overline{CE}$, $\overline{OE}$	T_A = 25°C; f = 1MHz	C_I		72	pF	4
Input/Output Capacitance: DQ1-DQ32	Vcc = 5V	$C_{I/O}$		15	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYM	-20		-25		-30		-40		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle													
READ cycle time	^tRC	20		25		30		35		45		ns	
Address access time	^tAA		20		25		30		35		45	ns	
Chip Enable access time	^tACE		20		25		30		35		45	ns	
Output hold from address change	^tOH	3		5		5		5		5		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	6		6		6		6		6		ns	7
Chip Enable to output in High-Z	^tHZCE		9		9		12		15		18	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		20		25		30		35		45	ns	
Output Enable access time	^tAOE		8		8		10		12		15	ns	
Output Enable LOW to output in Low-Z	^tLZOE	2		2		2		2		2		ns	
Output Enable HIGH to output in High-Z	^tHZOE		7		7		10		12		15	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	20		20		25		30		35		ns	
Chip Enable to end of write	^tCW	15		15		18		20		25		ns	
Address valid to end of write	^tAW	15		15		18		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
Write pulse width	^tWP	15		15		18		20		25		ns	
Data setup time	^tDS	10		10		12		15		20		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	5		5		5		5		5		ns	7
Write Enable HIGH to output in High-Z	^tHZWE	0	10	0	10	0	10	0	12	0	15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

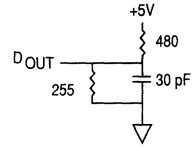


Fig. 1 OUTPUT LOAD EQUIVALENT

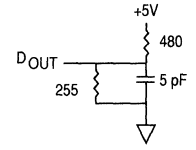


Fig. 2 OUTPUT LOAD EQUIVALENT

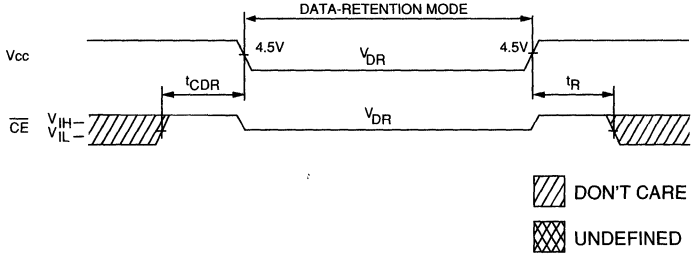
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE and ^{t}HZOE are less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. The ouptut will be in the High-Z state if $\overline{OE}$ is High.
12. The first falling edge of either $\overline{CE}$ or $\overline{WE}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{CE}$ or $\overline{WE}$ will terminate a WRITE cycle.

DATA RETENTION ELECTRICAL CHARACTERISTICS (-L Version Only)

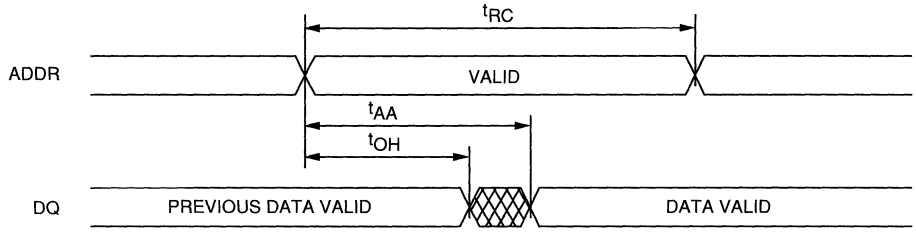
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		0.8	4	mA	
		Vcc = 3v			3	6	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

LOW Vcc DATA-RETENTION WAVEFORM

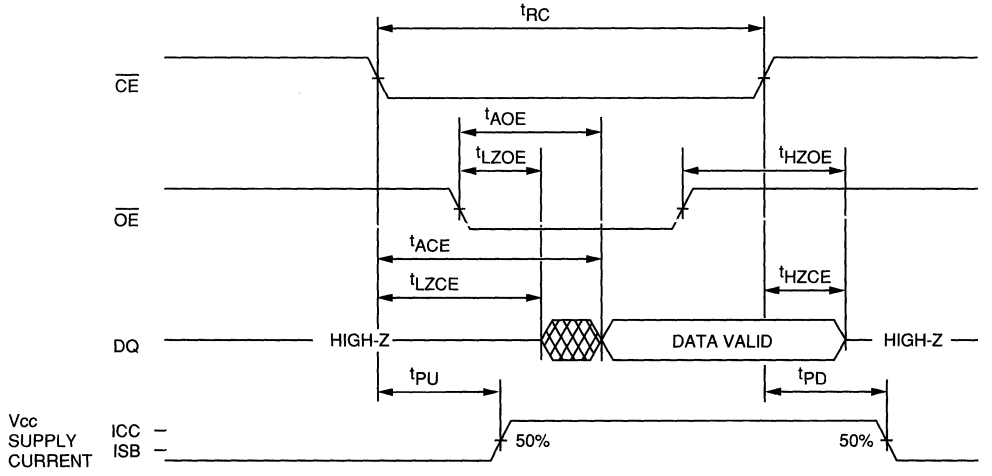


SRAM MODULE

READ CYCLE NO. 1 [8, 9]



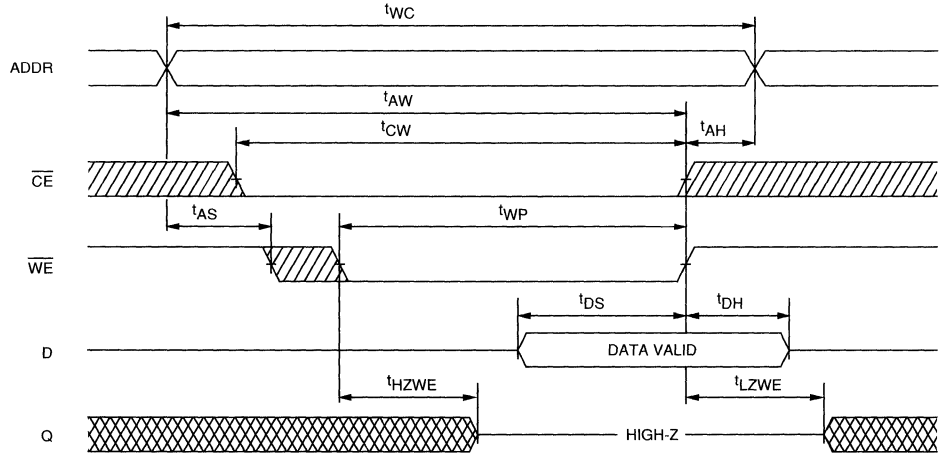
READ CYCLE NO. 2 [7, 8, 10]



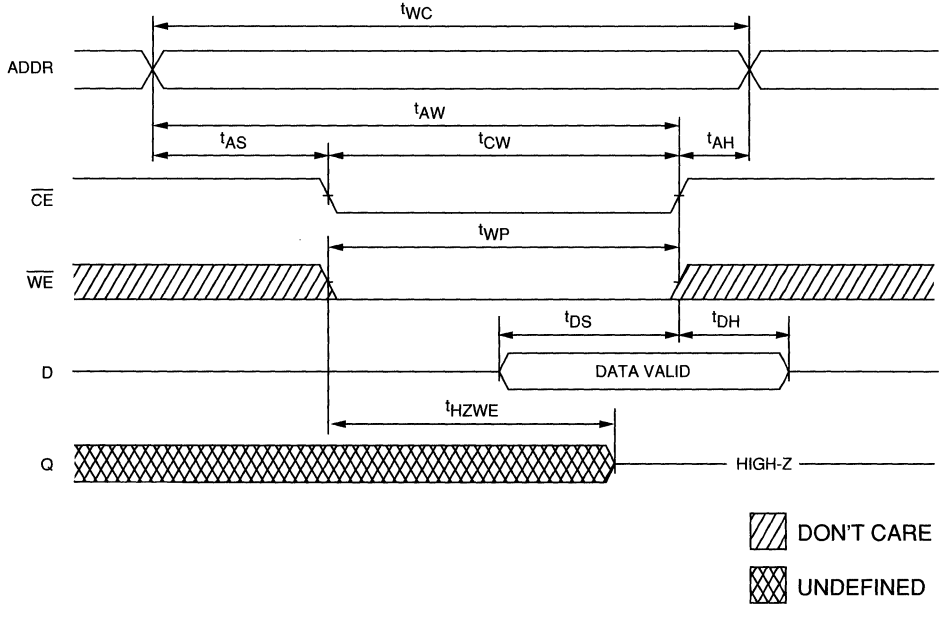
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled) [11, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [11, 12]



SRAM MODULE

128K x 32 SRAM

FEATURES

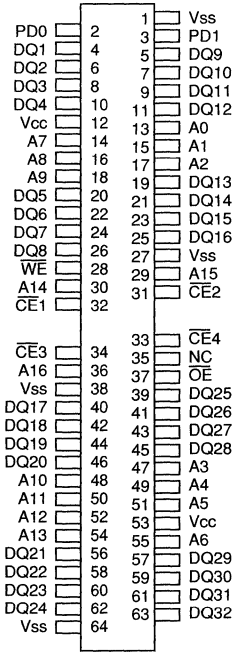
- Industry compatible pinout
- High speed: 25ns, 35ns and 45ns
- High-density 512KB design
- High-performance, low-power, CMOS process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ function
- Low profile (.600 inches MAX height)
- All inputs and outputs are TTL compatible

OPTIONS

OPTIONS	MARKING
• Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
64-pin ZIP	Z
• Optional, 2V data retention	L

PIN ASSIGNMENT (Top View)

64-Pin ZIP
(J-2)



GENERAL DESCRIPTION

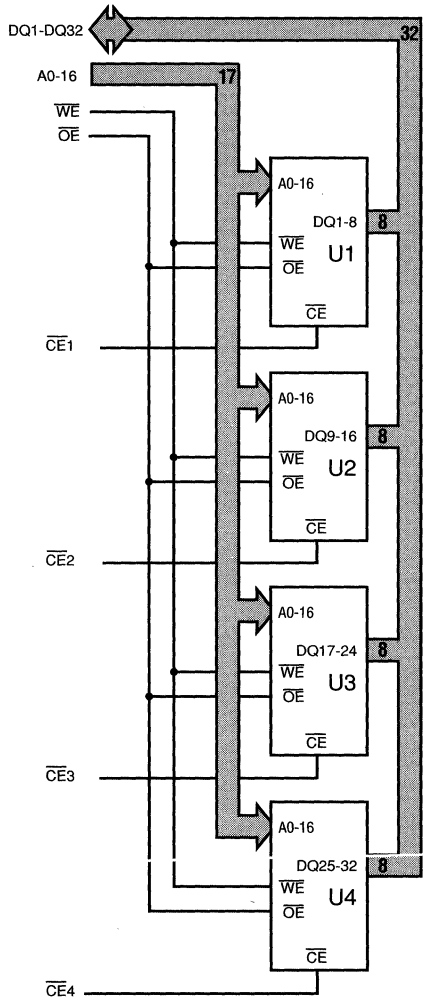
The MT4S12832 is a high-speed SRAM memory module containing 131,072 words organized in a x32-bit configuration. The module consists of four 128K x 8 fast static RAMs mounted on a 64-pin ZIP, double-sided, FR4 printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ can set the output in a high-impedance state for additional flexibility in system design. Memory expansion is accomplished by use of the $\overline{OE}$ function.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5VDC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5C1008

PRESENCE DETECT
PD0 = No Connect
PD1 = No Connect

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} .....-1.0V to +7.0V
Storage Temperature .....-55°C to +150°C
Power Dissipation 4W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-20	20	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-20	20	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-25	- 35	-45	UNITS	NOTES
Operating Current: TTL Input Levels	$\overline{CE} \le V_{IL}$, V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	480	480	480	mA	3
Standby Current: TTL Input Levels	$\overline{CE} \ge V_{IH}$, V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	100	100	100	mA	
Standby Current: CMOS Input Levels	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2, f = 0	I_{SB2}	28	28	28	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: Ao-A13, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1MHz	C_I		32	pF	4
Input/Output Capacitance: DQ1-DQ32	V_{CC} = 5V	$C_{I/O}$		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYM	-25		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	^tRC	25		35		45		ns	
Address access time	^tAA		25		35		45	ns	
Chip Enable access time	^tACE		25		35		45	ns	
Output hold from address change	^tOH	5		5		5		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip Enable to output in High-Z	^tHZCE		10		15		18	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		25		35		45	ns	
Output Enable access time	^tAOE		8		12		15	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		10		12		15	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	25		35		45		ns	
Chip Enable to end of write	^tCW	15		20		25		ns	
Address valid to end of write	^tAW	15		20		25		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
Write command pulse width	^tWP	15		20		25		ns	
Data setup time	^tDS	10		15		20		ns	
Data hold time	^tDH	0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	0		0		0		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		10		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

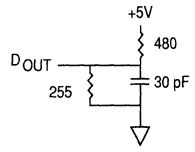


Fig. 1 OUTPUT LOAD EQUIVALENT

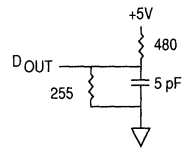


Fig. 2 OUTPUT LOAD EQUIVALENT

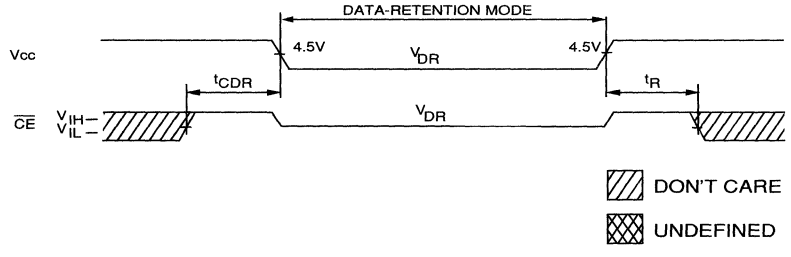
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE and ^{t}HZOE are less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. The ouptut will be in the High-Z state if $\overline{OE}$ is High.
12. The first falling edge of either $\overline{CE}$ or $\overline{WE}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{CE}$ or $\overline{WE}$ will terminate a WRITE cycle.

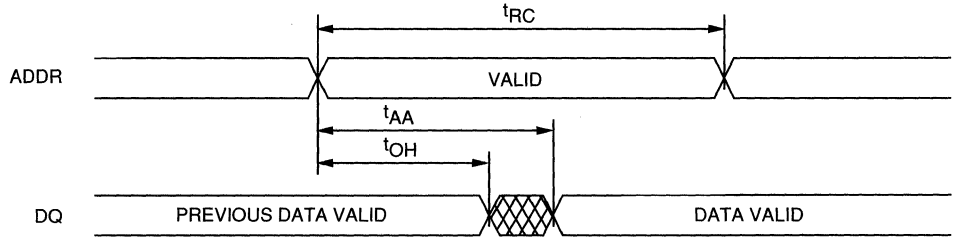
DATA RETENTION ELECTRICAL CHARACTERISTICS (-L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		0.4	2	mA	
		Vcc = 3v			1.4	3	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

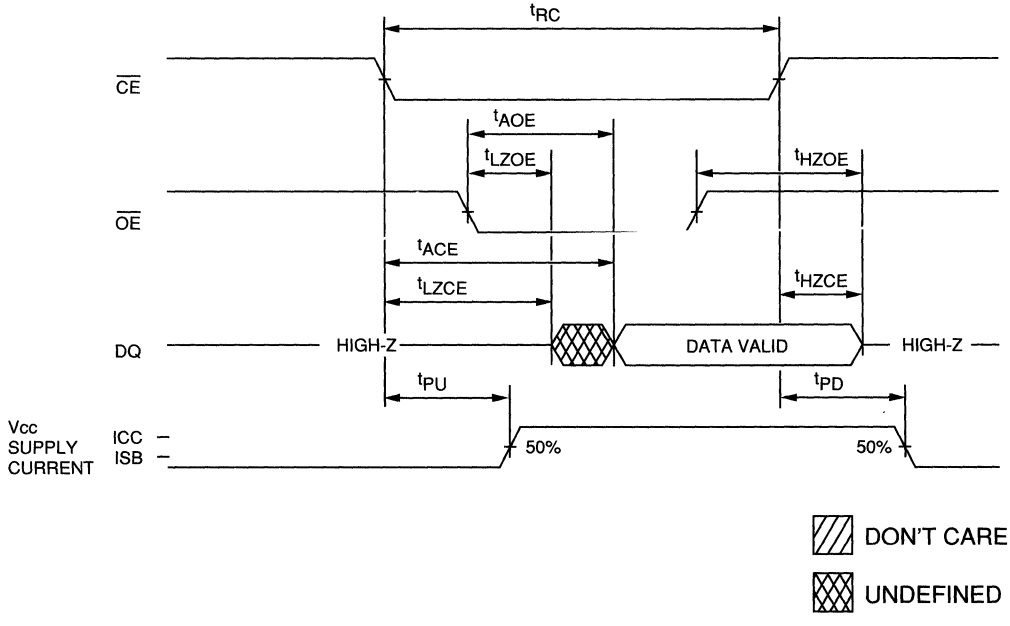
LOW Vcc DATA-RETENTION WAVEFORM



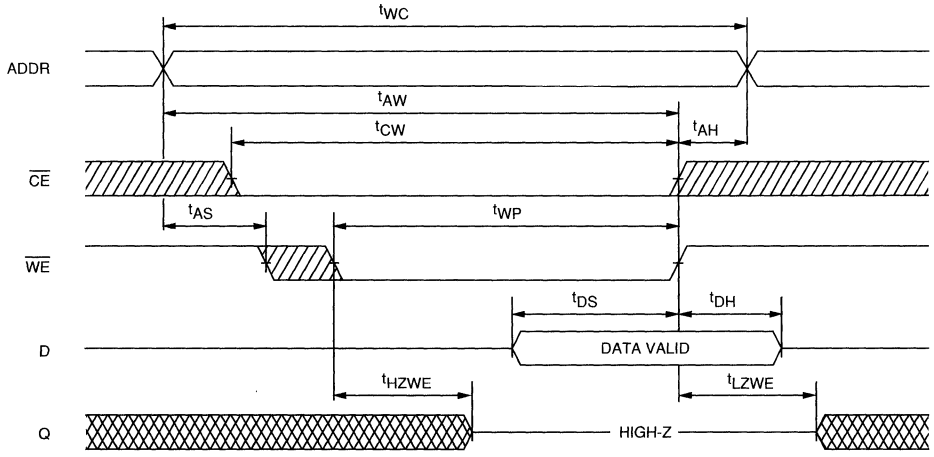
READ CYCLE NO. 1 [8, 9]



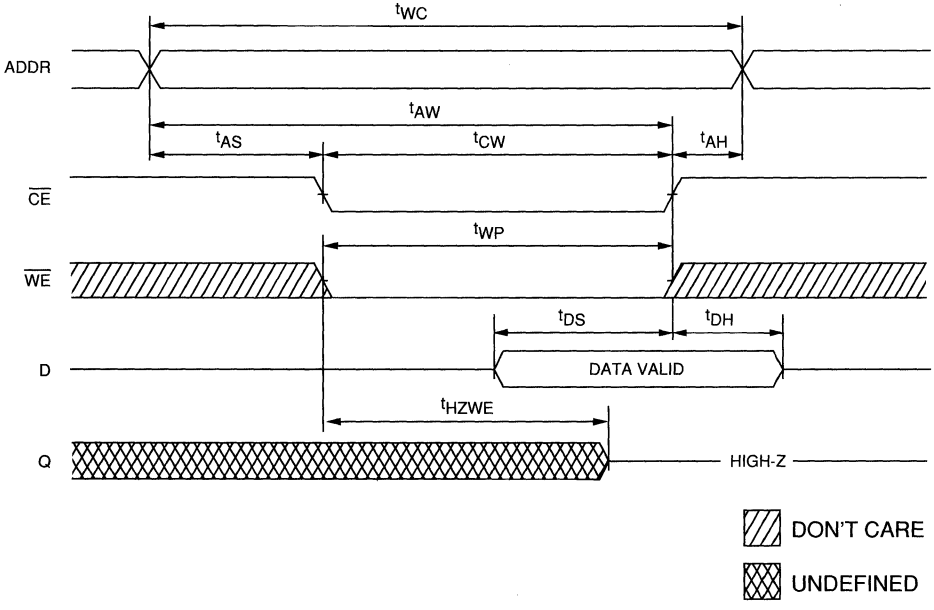
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Write Enable Controlled) [11, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [11, 12]



SRAM MODULE

256K x 32 SRAM

FEATURES

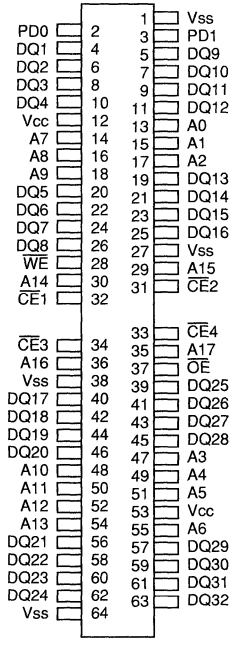
- Industry compatible pinout
- High speed: 25ns, 35ns and 45ns
- High-density 1MB design
- High-performance, low-power, CMOS process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ function
- Low profile (.600 inches MAX height)
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
64-pin ZIP	Z
• Optional, 2V data retention	L

PIN ASSIGNMENT (Top View)

64-Pin ZIP
(J-3)



GENERAL DESCRIPTION

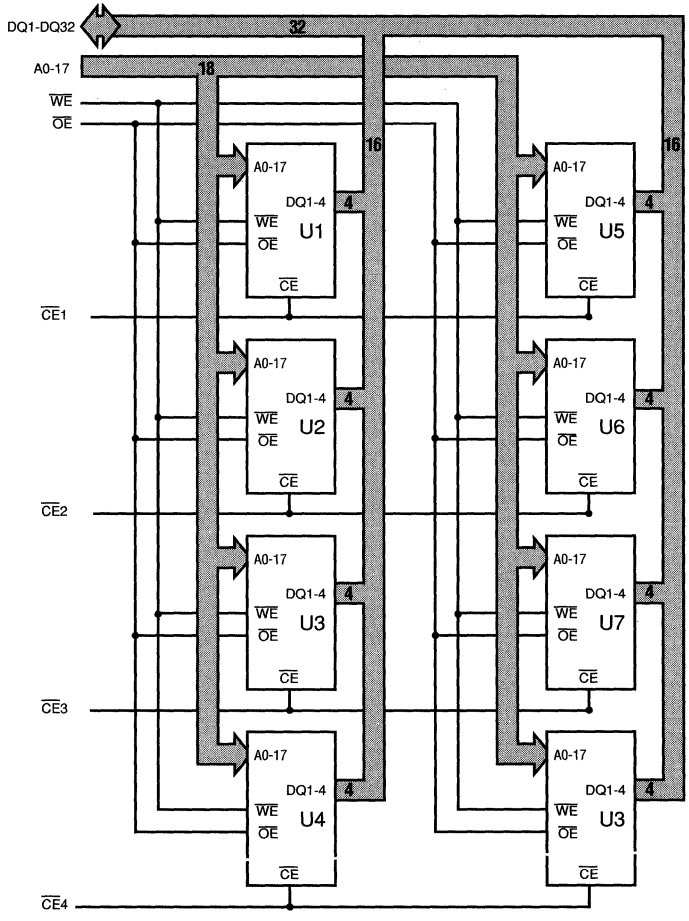
The MT8S25632 is a high-speed SRAM memory module containing 262,144 words organized in a x32-bit configuration. The module consists of eight 256K x 4 fast static RAMs mounted on a 64-pin ZIP, double-sided, FR4 printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ can set the output in a high impedance state for additional flexibility in system design, and memory expansion is accomplished by use of the $\overline{OE}$ and $\overline{CE}$ functions.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5VDC supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT5C1005

PRESENCE DETECT
PD0 = Vss
PD1 = Vss

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature ..... -55°C to +150°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage			V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		I_{LI}	-5	5	µA	
Input/Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	DQ1-DQ32	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-25	-35	-45	UNITS	NOTES
Operating Current: TTL Input Levels	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC; Outputs Open	I_{CC}	960	960	960	mA	3
Standby Current: TTL Input Levels	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC; Outputs Open	I_{SB1}	200	200	200	mA	
Standby Current: CMOS Input Levels	$\overline{CE} \ge V_{CC}$ -0.2; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}	56	56	56	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance; A0-A17, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1MHz	C_{I1}		64	pF	4
Input Capacitance; $\overline{CE}$1-$\overline{CE}$4	V_{CC} = 5V	C_{I2}		16	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYM	-25		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	^tRC	25		35		45		ns	
Address access time	^tAA		25		35		45	ns	
Chip Enable access time	^tACE		25		35		45	ns	
Output hold from address change	^tOH	5		5		5		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip Enable to output in High-Z	^tHZCE		10		15		18	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		25		35		45	ns	
Output Enable access time	^tAOE		8		12		15	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		10		12		15	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	25		35		45		ns	
Chip Enable to end of write	^tCW	15		20		25		ns	
Address valid to end of write	^tAW	15		20		25		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
Write pulse width	^tWP	15		20		25		ns	
Data setup time	^tDS	10		15		20		ns	
Data hold time	^tDH	0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	0		0		0		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		10		15		18	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

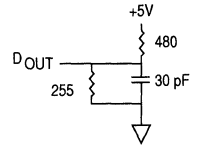


Fig. 1 OUTPUT LOAD EQUIVALENT

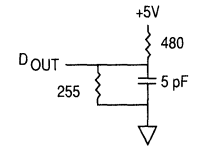


Fig. 2 OUTPUT LOAD EQUIVALENT

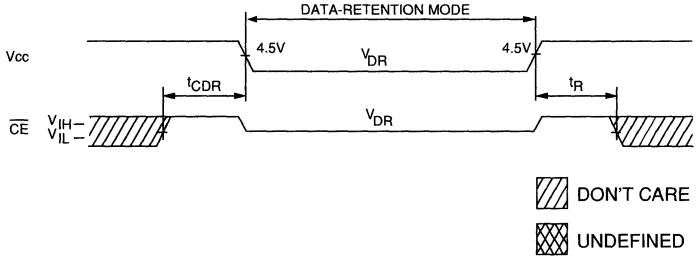
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. The ouptut will be in the High-Z state if $\overline{OE}$ is High.
12. The first falling edge of either $\overline{CE}$ or $\overline{WE}$ will initiate a WRITE cycle, and the first rising edge of either $\overline{CE}$ or $\overline{WE}$ will terminate a WRITE cycle.

DATA RETENTION ELECTRICAL CHARACTERISTICS (-L Version Only)

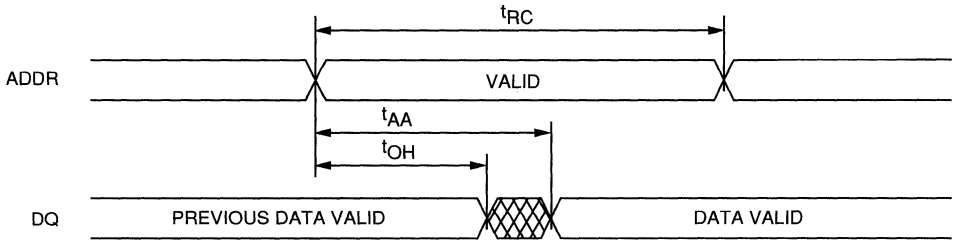
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	I_{CCDR}		0.8	4	mA	
		Vcc = 3v			2.8	6	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

LOW Vcc DATA-RETENTION WAVEFORM

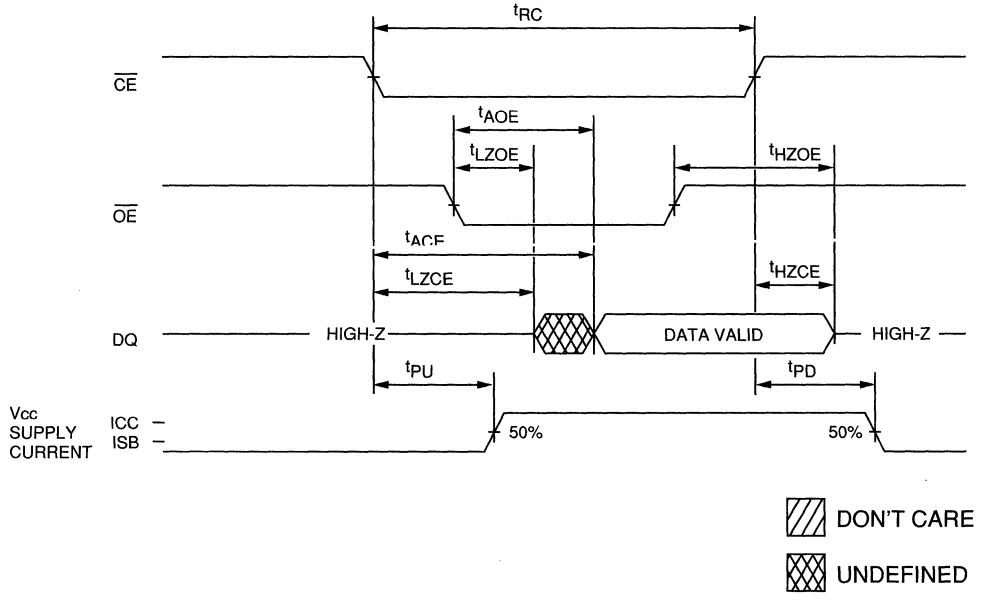


SRAM MODULE

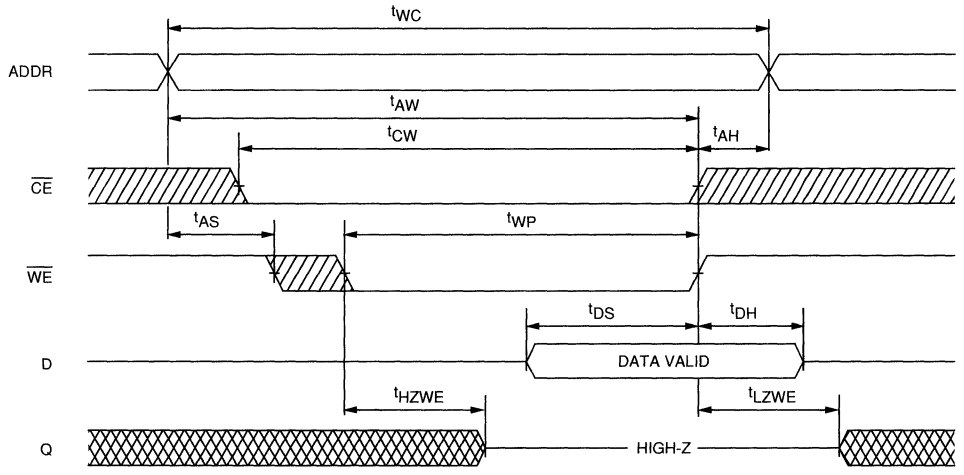
READ CYCLE NO. 1 [8, 9]



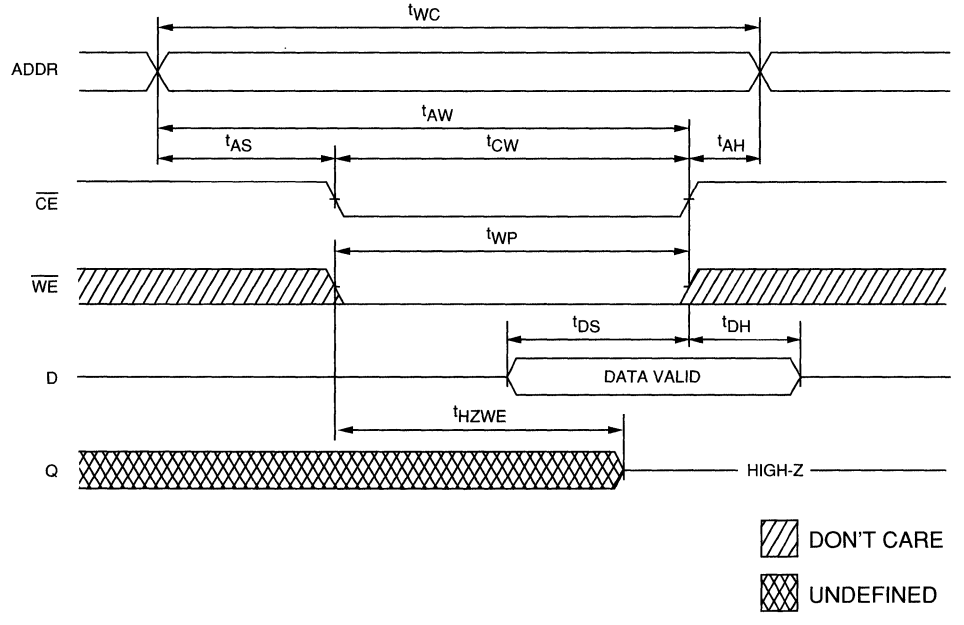
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Write Enable Controlled) [11, 12]



WRITE CYCLE NO. 2
(Chip Enable Controlled) [11, 12]



MICRON TECHNOLOGY, INC.

CACHE DATA SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package		Process	Page
				PLCC	PQFP		
Dual 4K x 16 or Single 8K x 16	Mode, Byte Select CE, OE Address Latch (A0 - A11)	MT56C0816	20, 25, 35	52	52	CMOS	7-1
Dual 4K x 16 or Single 8K x 16	Mode, Byte Select CE, OE Address Latch (A0 - A12)	MT56C3816	20, 25, 35	52	52	CMOS	7-11
Dual 4K x 18 or Single 8K x 18	Mode, Byte Select CE, OE Address Latch (A0 - A11)	MT56C0818	20, 25, 35	52	52	CMOS	7-21
Dual 4K x 18 or Single 8K x 18	Mode, Byte Select CE, OE Synchronous Write Enable	MT56C2818	24, 28	52	52	CMOS	7-31
Dual 4K x 18 or Single 8K x 18	Mode, Byte Select CE, OE Address Latch (A0 - A12)	MT56C3818	20, 25, 35	52	52	CMOS	7-41

CACHE DATA STATIC RAM

DUAL 4K x 16 SRAM, SINGLE 8K x 16 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

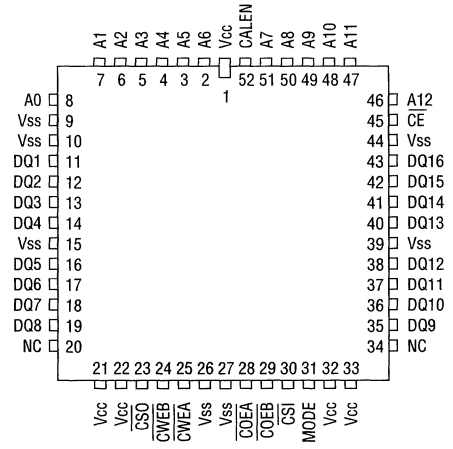
- Operates as two 4K x 16 SRAMs with common addresses and data; also configurable as a single 8K x 16 SRAM
- Built-in input address latches
- Separate upper and lower Byte Select
- Fast access times: 20ns, 25ns and 35ns allow operation with 40, 33 and 25MHz microprocessor systems
- Fast Output Enable: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 cache memory controllers

OPTIONS

	MARKING
• Timing	
20ns access (40 MHz)	-20
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-4)



GENERAL DESCRIPTION

The MT56C0816 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C0816 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either the DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE MODE. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 16-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 16-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

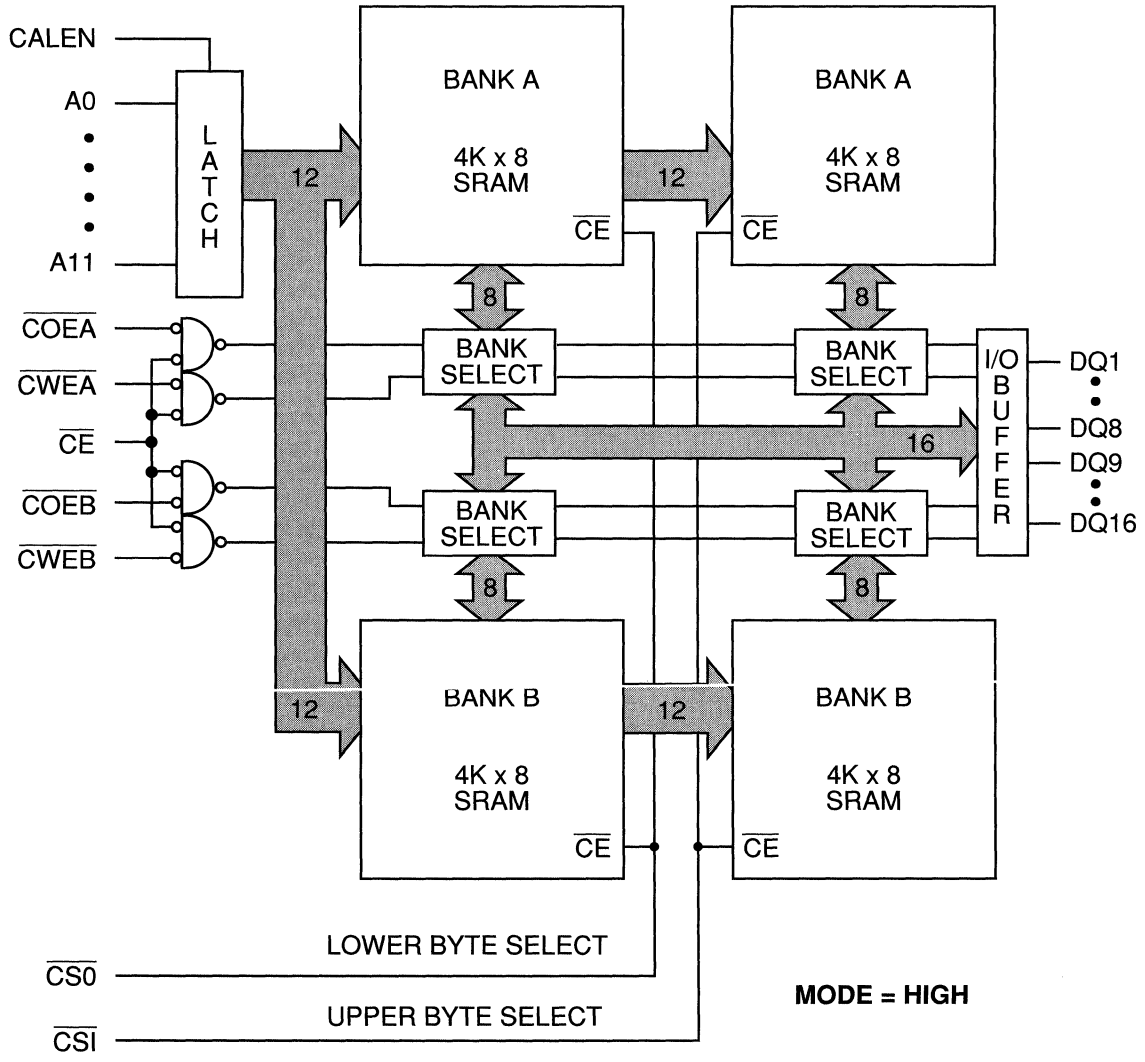
Outputs are enabled on a HIGH to LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH to LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C0816 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

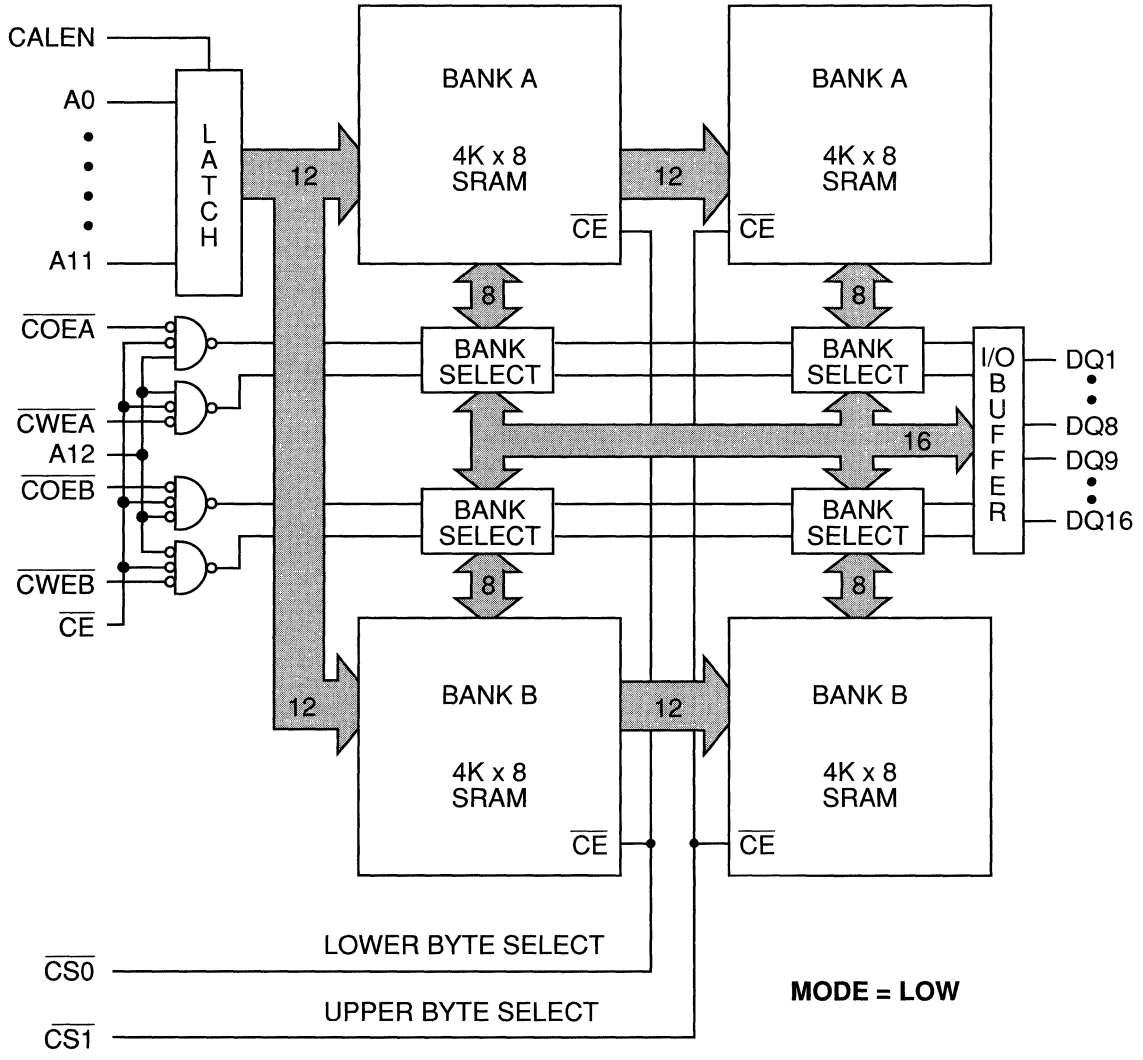
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 16
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM

8K x 16
(DIRECT MAP)



PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K x 16 configuration. It is not used in the dual 4K x 16 configuration.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A11).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 16 configuration. When the pin is tied LOW, the device is configured as an 8K x 16 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 are enabled.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the DIRECT mode, these signals should be externally connected, and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the output.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	Write Enable: In the dual configuration the signal that is LOW enables a data WRITE to the addressed memory location. In the DIRECT mode, these signals should be externally connected, and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ± 5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 16 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1 - DQ8 bank A	L	L	H	L	H	H	H
READ DQ1 - DQ8 bank B	L	L	H	H	L	H	H
READ DQ9 - DQ16 bank A	L	H	L	L	H	H	H
READ DQ9 - DQ16 bank B	L	H	L	H	L	H	H
READ DQ1 - DQ16 bank A	L	L	L	L	H	H	H
READ DQ1 - DQ16 bank B	L	L	L	H	L	H	H
WRITE DQ1 - DQ8 bank A	L	L	H	X	X	L	H
WRITE DQ1 - DQ8 bank B	L	L	H	X	X	H	L
WRITE DQ9 - DQ16 bank A	L	H	L	X	X	L	H
WRITE DQ9 - DQ16 bank B	L	H	L	X	X	H	L
WRITE DQ1 - DQ16 bank A	L	L	L	X	X	L	H
WRITE DQ1 - DQ16 bank B	L	L	L	X	X	H	L
WRITE DQ1 - DQ8 bank A & B	L	L	H	X	X	L	L
WRITE DQ9 - DQ16 bank A & B	L	H	L	X	X	L	L
WRITE DQ1 - DQ16 bank A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE

8K x 16 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1 - DQ8	L	L	H	L	L	H	H
READ DQ9 - DQ16	L	H	L	L	L	H	H
READ DQ1 - DQ16	L	L	L	L	L	H	H
WRITE DQ1 - DQ8	L	L	H	X	X	L	L
WRITE DQ9 - DQ16	L	H	L	X	X	L	L
WRITE DQ1 - DQ16	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ and $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

$\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature ..... -55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 5\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		V_{CC}	4.75	5.25	V	
Input High Voltage		V_{IH}	2.2	V_{CC}+0.3	V	1
Input Low Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	V_{IN} = GND to V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	$V_{I/O}$ = GND to V_{CC} Output(s) Disabled	I_{LO}	-10	10	µA	
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty cycle V_{IN} = GND to V_{CC}	I_{CC1}		220	mA	
Power Supply Current: Average Operating Current	50% Duty cycle V_{IN} = GND to V_{CC}	I_{CC2}		120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0}$ = $\overline{CS1} \ge V_{CC}$ - 0.2V V_{CC} = MAX $V_{IL} \le V_{SS}$ + 0.2V $V_{IH} \ge V_{CC}$ - 0.2V	I_{SB}		20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_{IN}		6	pF	3
Output Capacitance	V_{CC} = 5V	$C_{I/O}$		6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	Θ_{JA}		100	°C/W	
Thermal resistance - Junction to Case		Θ_{JC}		45	°C/W	
Maximum Case Temperature		Tc		110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$; Vcc = 5.0V ±5%)

DESCRIPTION	SYM	-20 MIN	-20 MAX	-25 MIN	-25 MAX	-35 MIN	-35 MAX	UNITS	NOTES
READ Cycle									
READ cycle time	tRC	20		25		35		ns	4, 5
Address access time (A0-A11)	tAA		20		25		35	ns	
A12 address access time	tA12A		15		17		25	ns	
Chip Enable access time	tACE		20		20		25	ns	
Chip Select access time	tACS		20		25		35	ns	
Output Enable access time	tAOE		8		10		13	ns	
Output hold from address change	tOH	3		3		3		ns	
Chip Select to output Low-Z	tLZCS	3		3		3		ns	
Output Enable to output Low-Z	tLZOE	2		2		2		ns	
Chip deselect to output High-Z	tHZCS		15		15		25	ns	6
Output disable to output High-Z	tHZOE		10		10		14	ns	6
Address latch enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	tWC	20		25		35		ns	
Address valid to end of write	tAW	15		18		25		ns	
A12 address valid to end of write	tA12W	15		18		25		ns	
Chip Select to end of write	tCW	15		18		25		ns	
Data valid to end of write	tDW	10		10		10		ns	
Data hold from end of write	tDH	0		0		0		ns	
Write Enable output in High-Z	tHZWE		12		15		15	ns	6
Write disable to output in Low-Z	tLZWE	3		3		3		ns	
Write pulse width	tWP	15		18		25		ns	
$\overline{CE}$ pulse width (during Chip Enable controlled write)	tCP	15		18		25		ns	
Address setup time	tAS	0		0		0		ns	
Write recovery time	tWR	0		0		0		ns	
Address latch enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

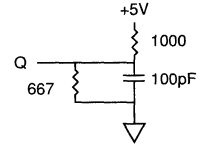


Fig. 1 OUTPUT LOAD EQUIVALENT

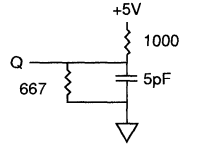


Fig. 2 OUTPUT LOAD EQUIVALENT

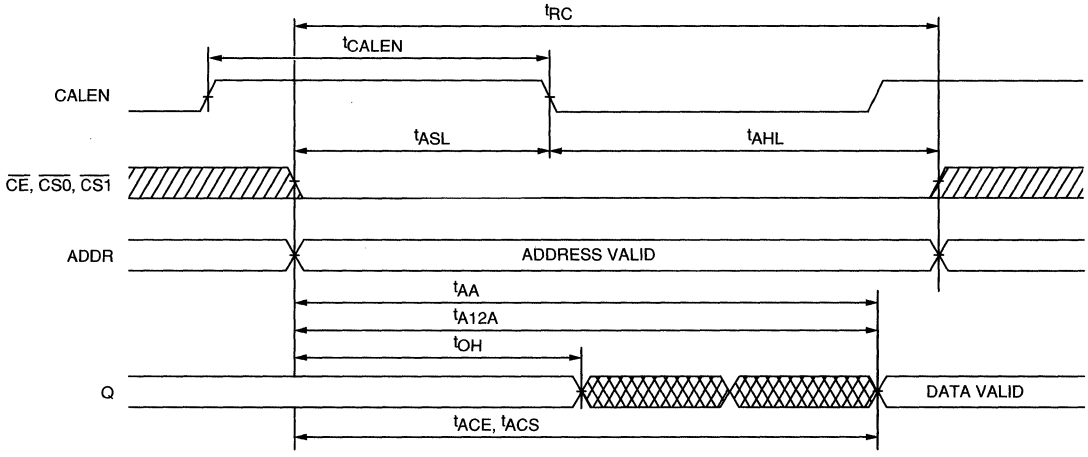
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. tHZCS, tHZOE, and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.

READ CYCLE NO. 1

(Address Controlled)

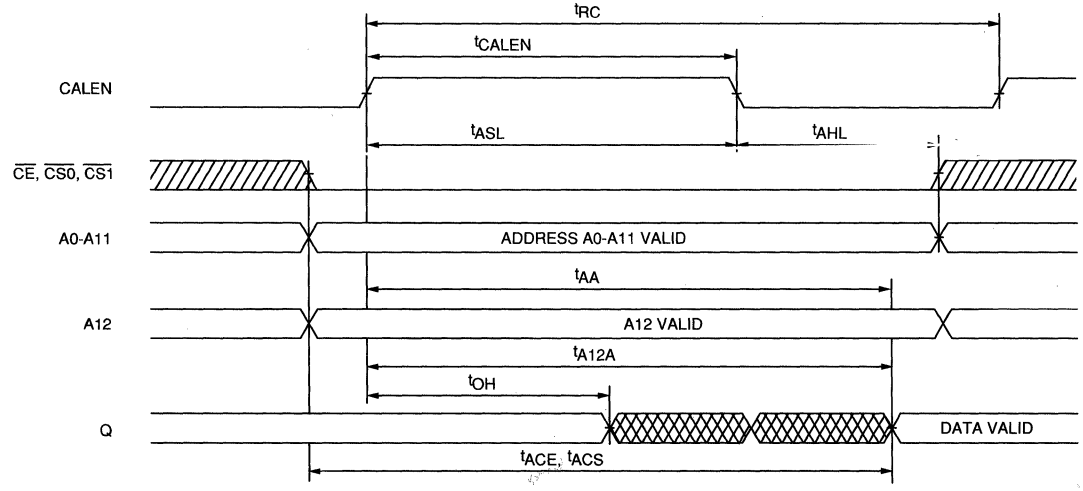
$\overline{CWEA}$ = $\overline{CWEB}$ =V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}



READ CYCLE NO. 2

(CALEN Controlled)

$\overline{CWEA}$ = $\overline{CWEB}$ =V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}

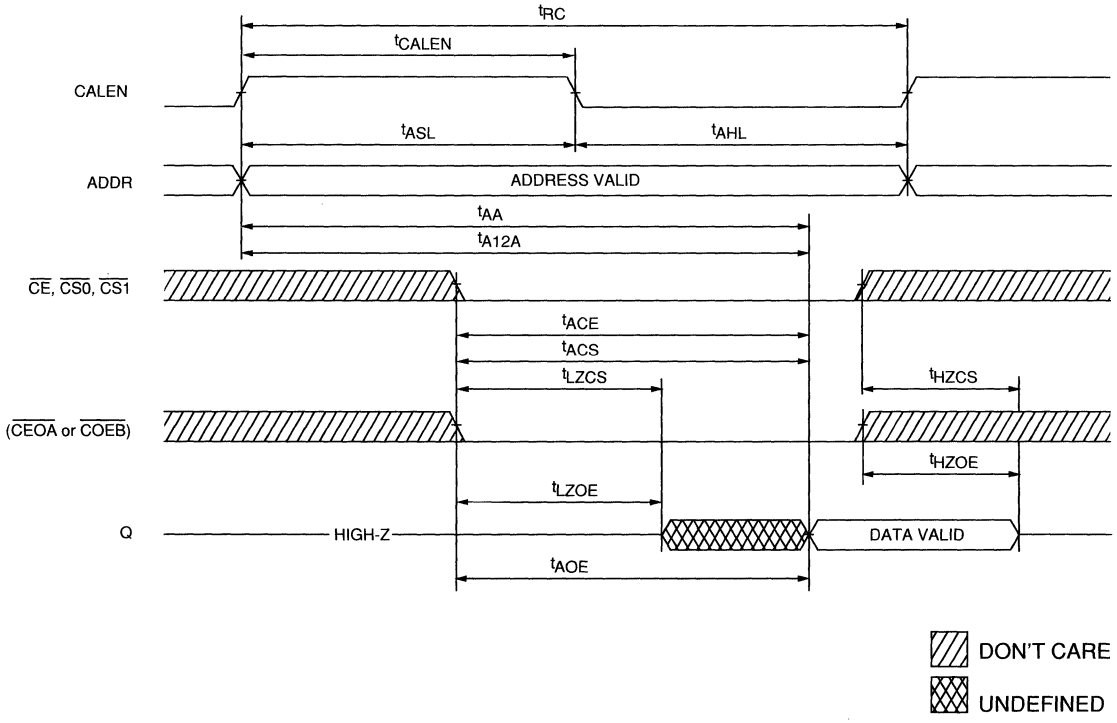


DON'T CARE

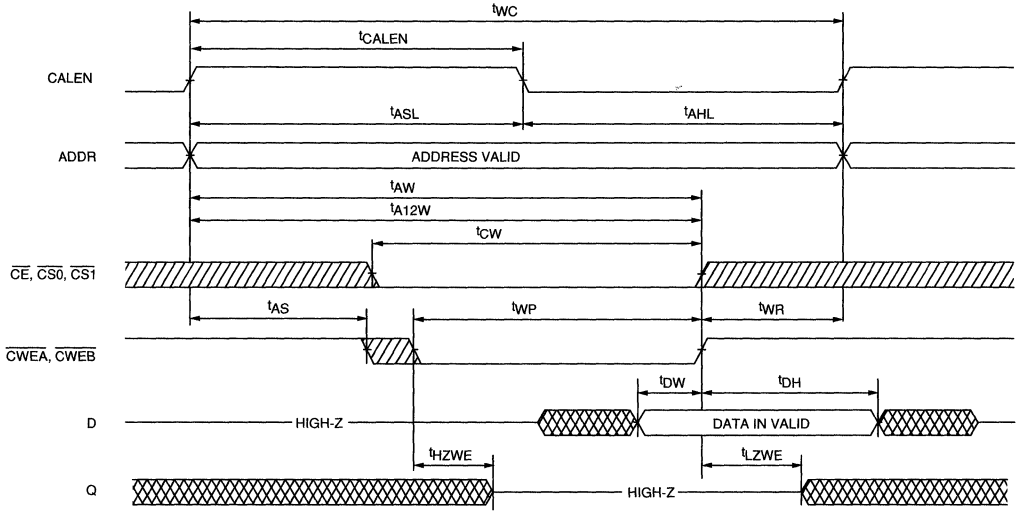
UNDEFINED

READ CYCLE NO. 3

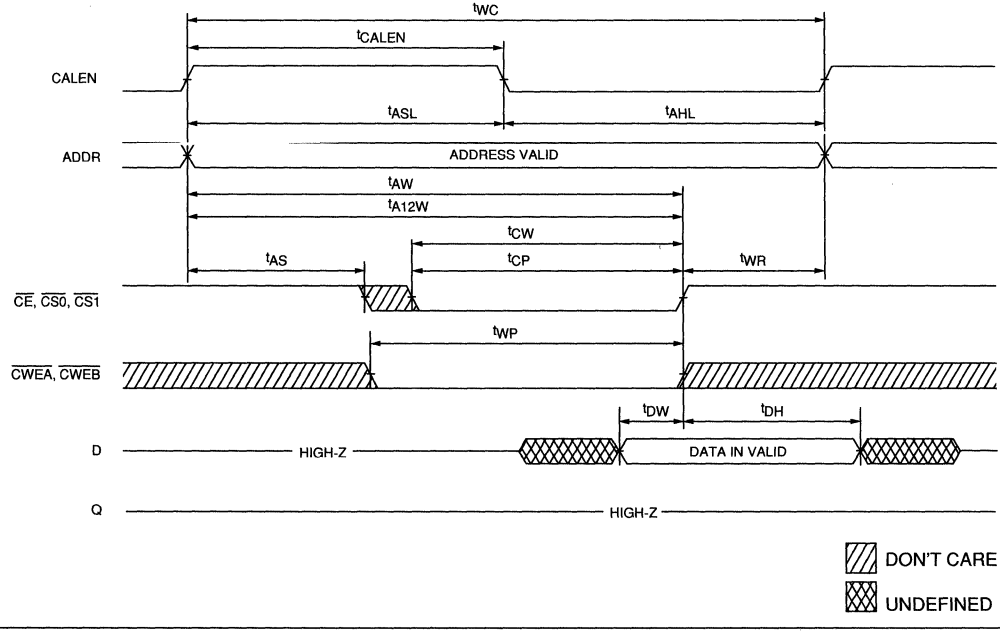
$\overline{CWEA} = \overline{CWEB} = V_{IH}$



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



CACHE DATA STATIC RAM

DUAL 4K x 16 SRAM, SINGLE 8K x 16 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

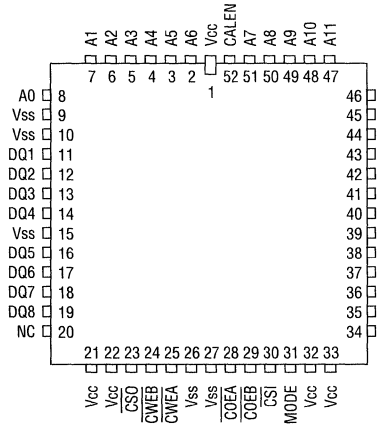
- Operates as two 4K x 16 SRAMs with common addresses and data; also configurable as a single 8K x 16 SRAM
- Built-in input address latches (A0-A12)
- Separate upper and lower Byte Select
- Fast access times: 20ns, 25ns and 35ns allow operation with 40, 33 and 25MHz microprocessor systems
- Fast Output Enable: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 and 80486 cache memory controllers

OPTIONS

	MARKING
• Timing	
20ns access (40 MHz)	-20
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-4)



GENERAL DESCRIPTION

The MT56C3816 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C3816 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either the DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE MODE. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 16-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 16-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

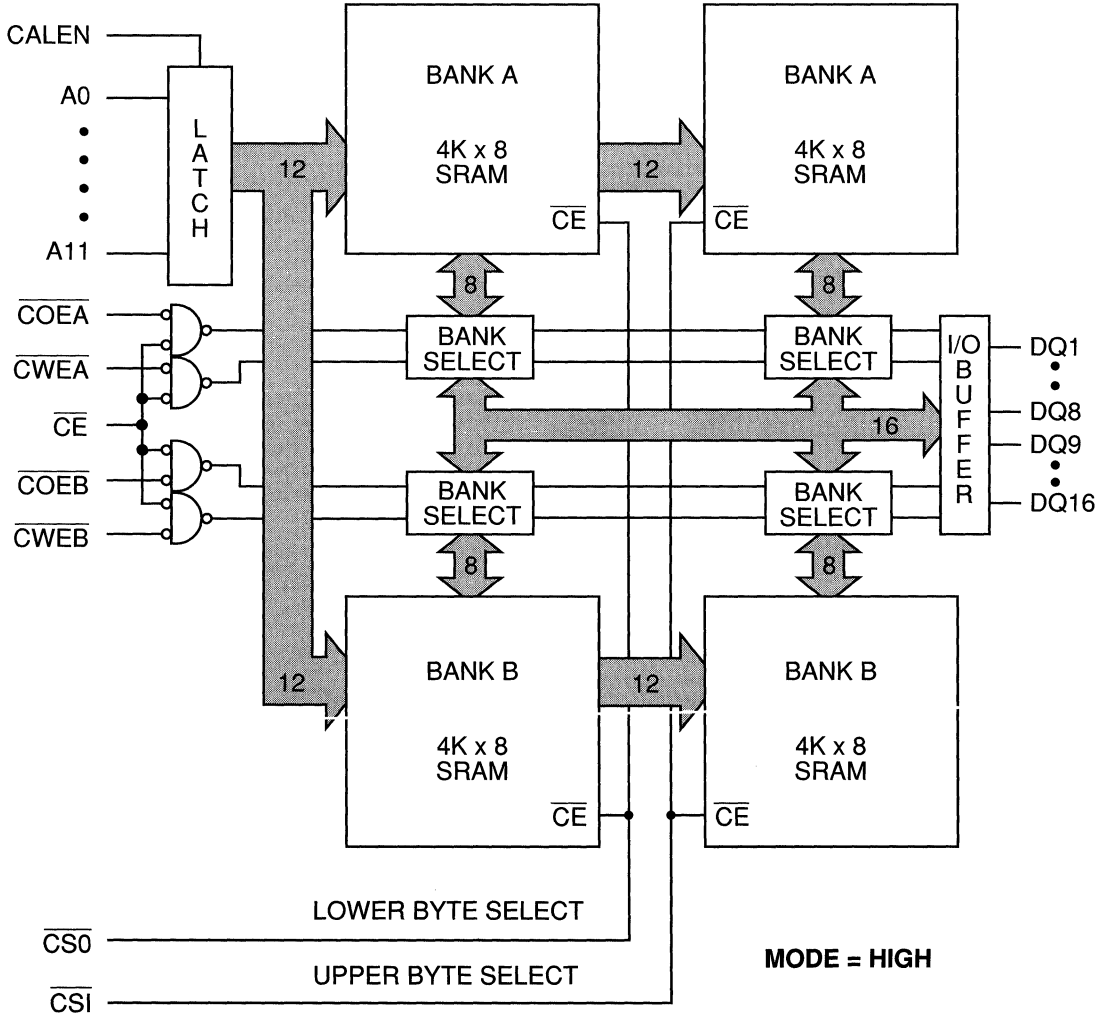
Outputs are enabled on a HIGH to LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH to LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C3816 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

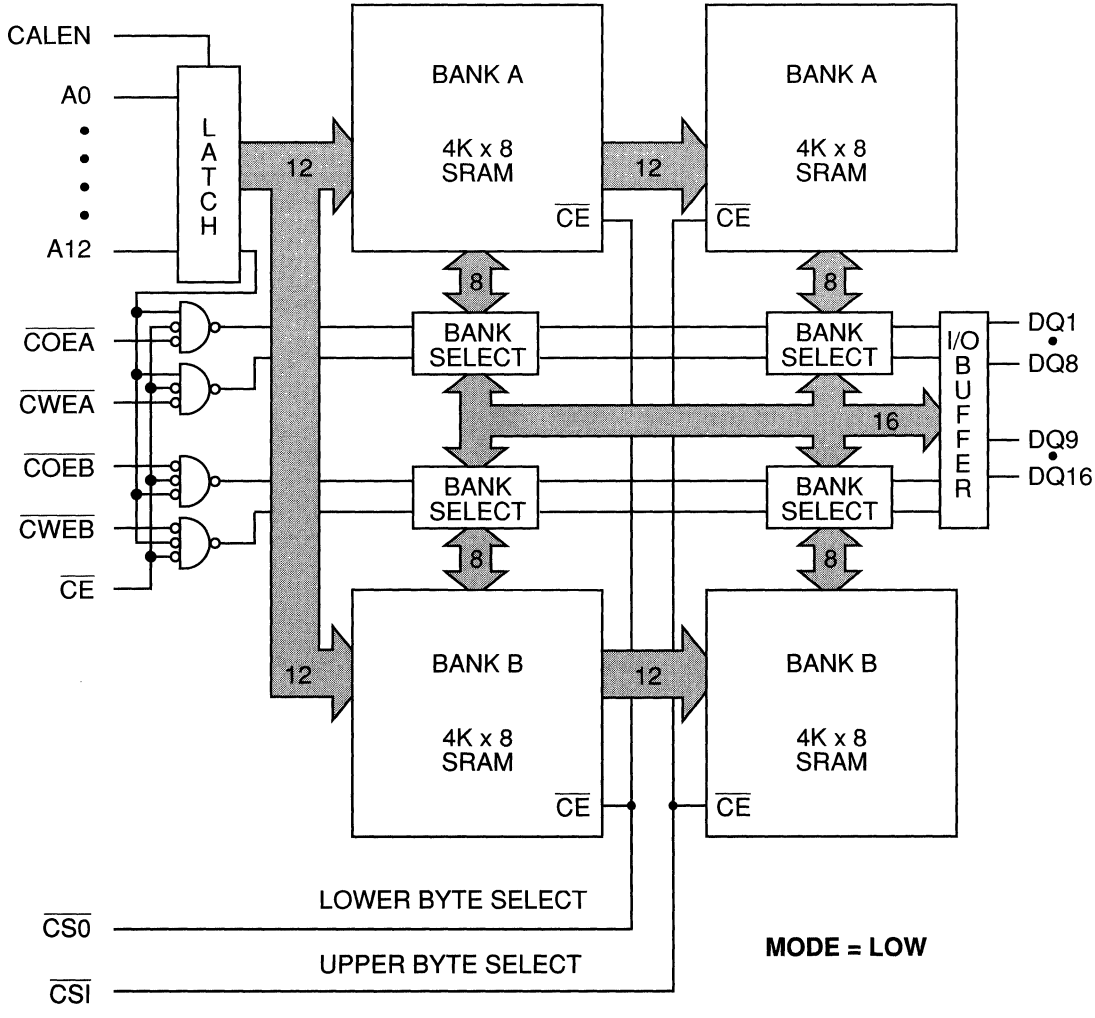
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 16
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM

8K x 16
(DIRECT MAP)



CACHE DATA SRAM

PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K x 16 configuration. It is not used in the dual 4K x 16 configuration. This input is latched by the negative edge of CALEN.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A12).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 16 configuration. When the pin is tied LOW, the device is configured as an 8K x 16 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 are enabled.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the DIRECT mode, these signals should be externally connected, and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	WRITE ENABLE: In the dual configuration, the signal that is LOW enables a data write to the addressed memory location. In the DIRECT mode, these signals should be externally connected, and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ± 5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 16 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1 - DQ8 bank A	L	L	H	L	H	H	H
READ DQ1 - DQ8 bank B	L	L	H	H	L	H	H
READ DQ9 - DQ16 bank A	L	H	L	L	H	H	H
READ DQ9 - DQ16 bank B	L	H	L	H	L	H	H
READ DQ1 - DQ16 bank A	L	L	L	L	H	H	H
READ DQ1 - DQ16 bank B	L	L	L	H	L	H	H
WRITE DQ1 - DQ8 bank A	L	L	H	X	X	L	H
WRITE DQ1 - DQ8 bank B	L	L	H	X	X	H	L
WRITE DQ9 - DQ16 bank A	L	H	L	X	X	L	H
WRITE DQ9 - DQ16 bank B	L	H	L	X	X	H	L
WRITE DQ1 - DQ16 bank A	L	L	L	X	X	L	H
WRITE DQ1 - DQ16 bank B	L	L	L	X	X	H	L
WRITE DQ1 - DQ8 bank A & B	L	L	H	X	X	L	L
WRITE DQ9 - DQ16 bank A & B	L	H	L	X	X	L	L
WRITE DQ1 - DQ16 bank A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE

8K x 16 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1 - DQ8	L	L	H	L	L	H	H
READ DQ9 - DQ16	L	H	L	L	L	H	H
READ DQ1 - DQ16	L	L	L	L	L	H	H
WRITE DQ1 - DQ8	L	L	H	X	X	L	L
WRITE DQ9 - DQ16	L	H	L	X	X	L	L
WRITE DQ1 - DQ16	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ and $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

$\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Storage Temperature .....-55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5.0V ± 5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		VIH	2.2	Vcc+0.3	V	1
Input Low Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	VIN = GND to Vcc	ILI	-10	10	µA	
Output Leakage Current	VI/O = GND to Vcc Output(s) Disabled	ILO	-10	10	µA	
Output Low Voltage	IOL = 4.0mA	VOL		0.4	V	1
Output High Voltage	IOH = -1.0mA	VOH	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty cycle VIN = GND to Vcc	ICC1		220	mA	
Power Supply Current: Average Operating Current	50% Duty cycle VIN = GND to Vcc	ICC2		120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0}$ = $\overline{CS1}$ ≥ Vcc -0.2V Vcc = MAX VIL ≤ Vss +0.2V VIH ≥ Vcc -0.2V	ISB		20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	CIN		6	pF	3
Output Capacitance	Vcc = 5V	CI/O		6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	ØJA		100	°C/W	
Thermal resistance - Junction to Case		ØJC		45	°C/W	
Maximum Case Temperature		Tc		110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$; V_{CC} = 5.0V ±5%)

DESCRIPTION	SYM	-20 MIN	-20 MAX	-25 MIN	-25 MAX	-35 MIN	-35 MAX	UNITS	NOTES
READ Cycle									
READ cycle time	tRC	20		25		35		ns	4, 5
Address access time (A0-A12)	tAA		20		25		35	ns	
Chip Enable access time	tACE		20		20		25	ns	
Chip Select access time	tACS		20		25		35	ns	
Output Enable access time	tAOE		8		10		13	ns	
Output hold from address change	tOH	3		3		3		ns	
Chip Select to output Low-Z	tLZCS	3		3		3		ns	
Output Enable to output Low-Z	tLZOE	2		2		2		ns	
Chip deselect to output High-Z	tHZCS		15		15		25	ns	6
Output disable to output High-Z	tHZOE		10		10		14	ns	6
Address latch enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	tWC	20		25		35		ns	
Address valid to end of write	tAW	15		18		25		ns	
Chip Select to end of write	tCW	15		18		25		ns	
Data valid to end of write	tDW	10		10		10		ns	
Data hold from end of write	tDH	0		0		0		ns	
Write Enable output in High-Z	tHZWE		12		15		15	ns	6
Write disable to output in Low-Z	tLZWE	3		3		3		ns	
Write pulse width	tWP	15		18		25		ns	
$\overline{CE}$ pulse width (during Chip Enable controlled write)	tCP	15		18		25		ns	
Address setup time	tAS	0		0		0		ns	
Write recovery time	tWR	0		0		0		ns	
Address latch enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

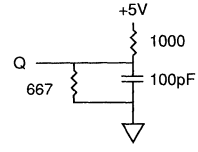


Fig. 1 OUTPUT LOAD EQUIVALENT

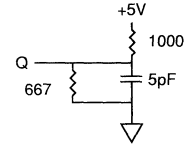


Fig. 2 OUTPUT LOAD EQUIVALENT

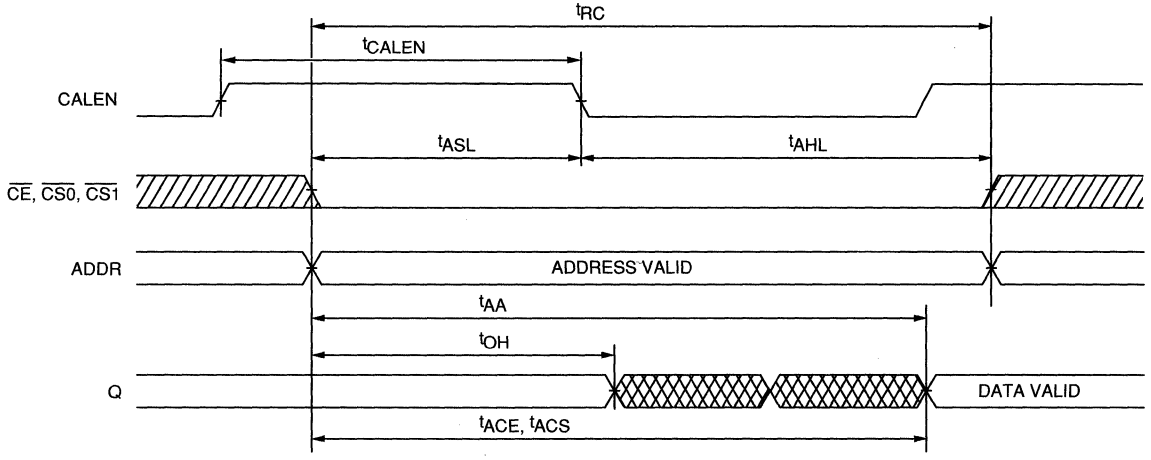
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. tHZCS, tHZOE, and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.

READ CYCLE NO. 1

(Address Controlled)

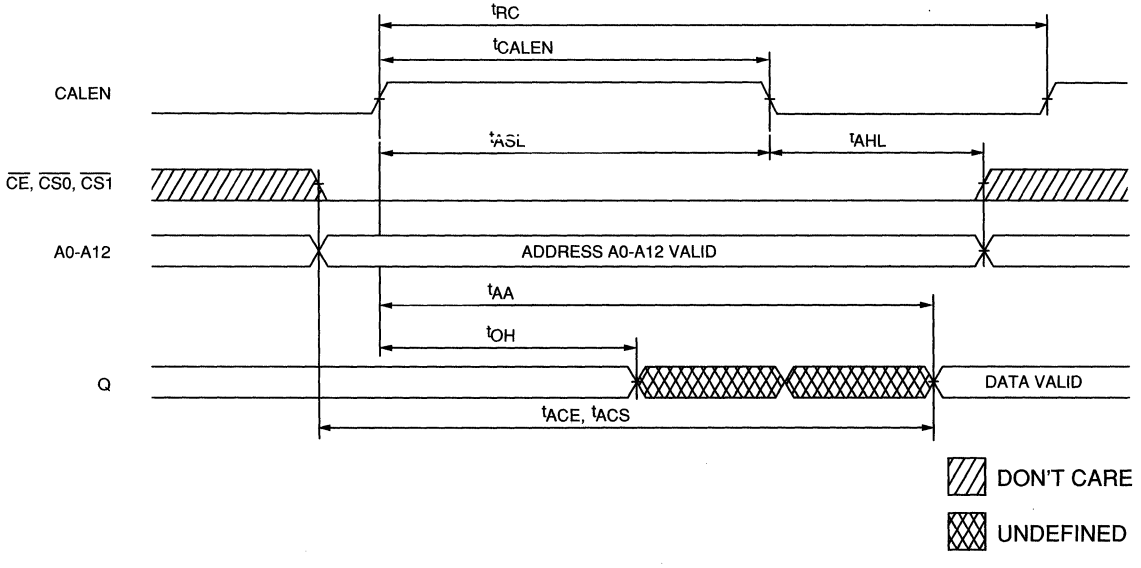
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}



READ CYCLE NO. 2

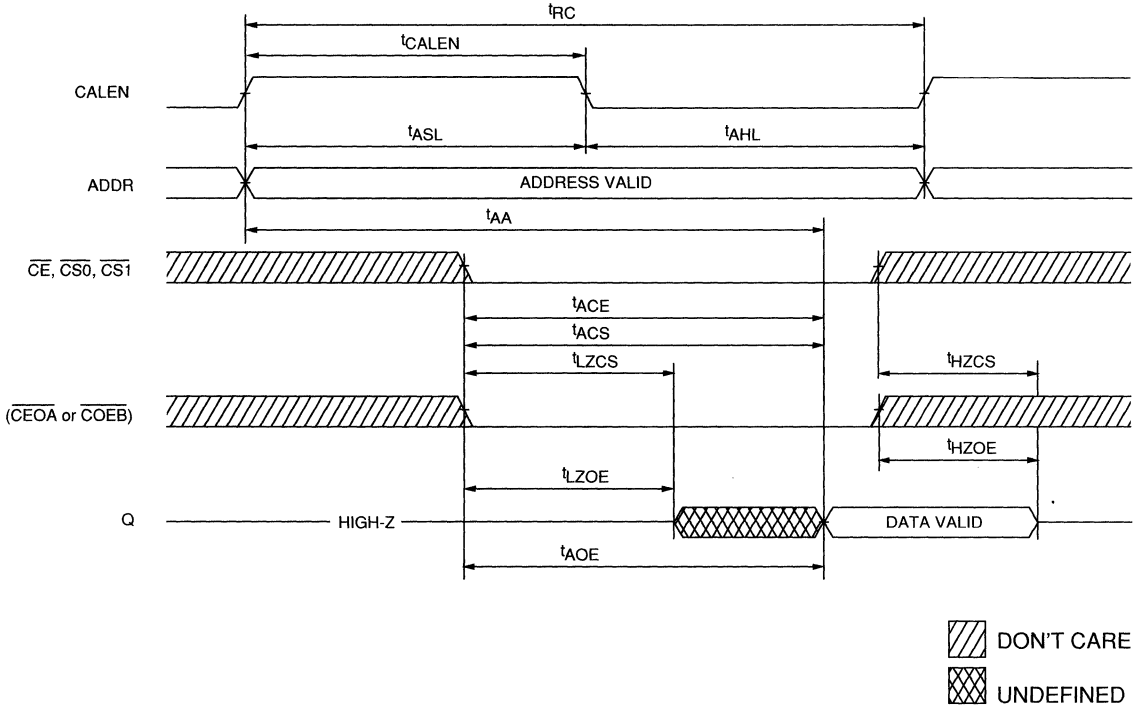
(CALEN Controlled)

$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}

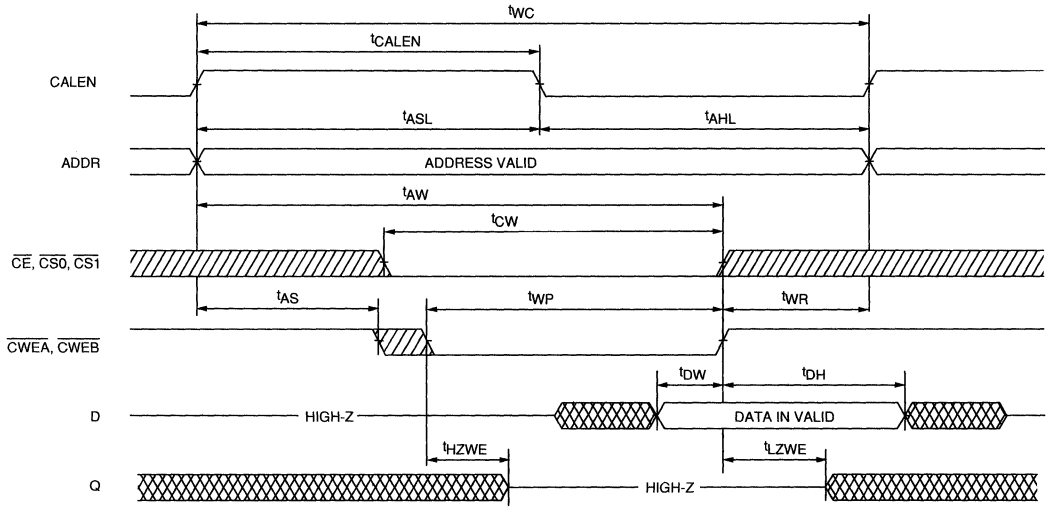


READ CYCLE NO. 3

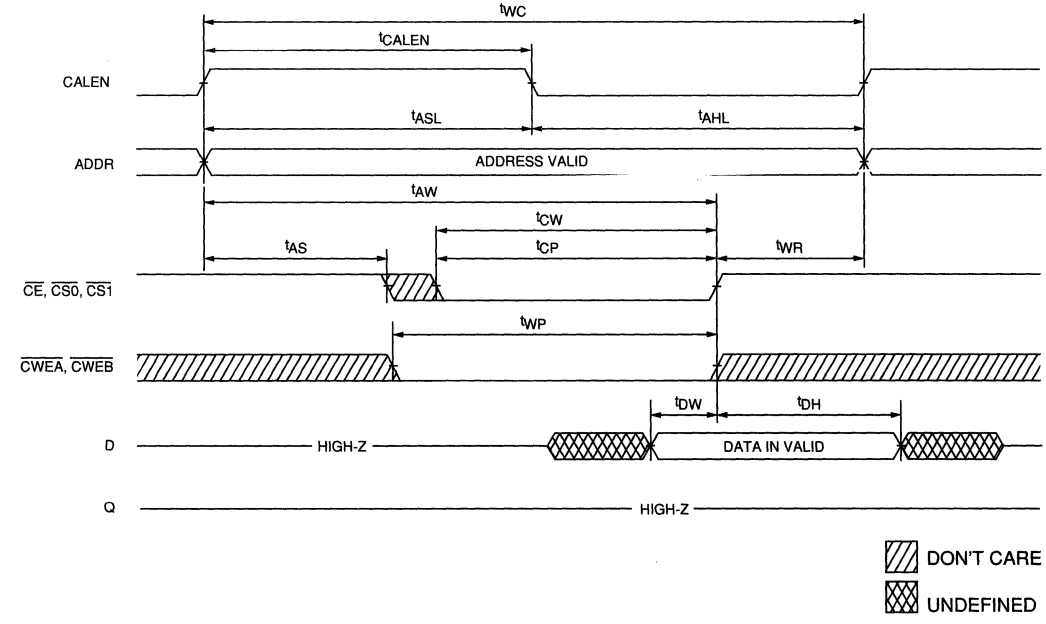
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



CACHE DATA STATIC RAM

DUAL 4K x 18 SRAM, SINGLE 8K x 18 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

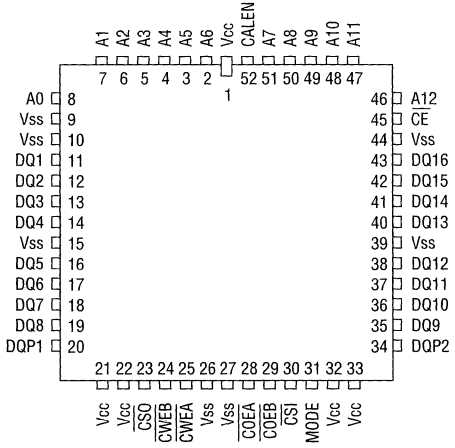
- Operates as two 4K x 18 SRAMs with common addresses and data; also configurable as a single 8K x 18 SRAM
- Built-in input address latches
- Separate upper and lower Byte Select
- Fast access times: 20ns, 25ns and 35ns allow operation with 40, 33 and 25MHz microprocessor systems
- Fast Output Enable: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 cache memory controllers
- Parity bits provided for large cache applications such as secondary cache for the Intel 80486 microprocessors

OPTIONS

	MARKING
• Timing	
20ns access (40 MHz)	-20
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-4)



GENERAL DESCRIPTION

The MT56C0818 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C0818 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either the DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE mode. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 18-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 18-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

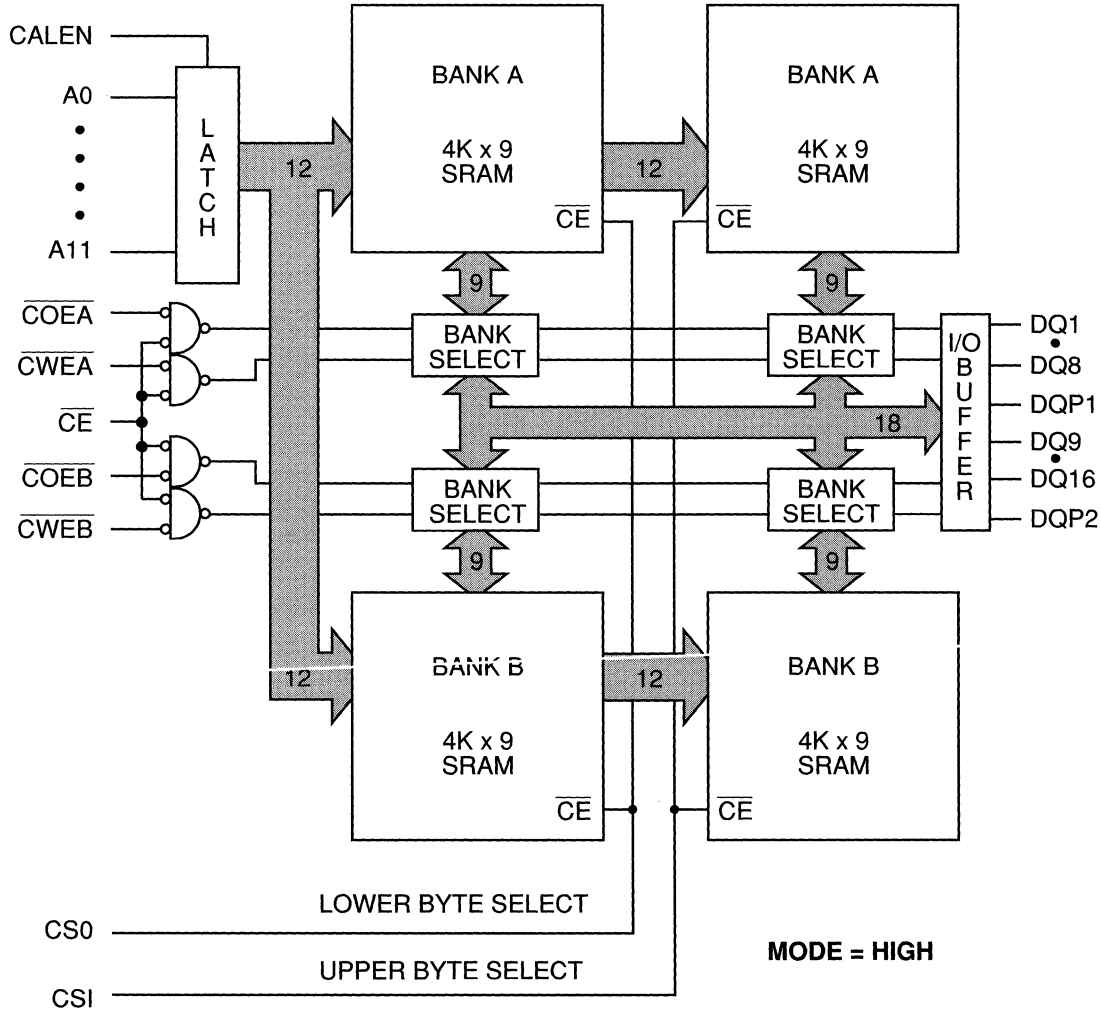
Outputs are enabled on a HIGH to LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH to LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C0818 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

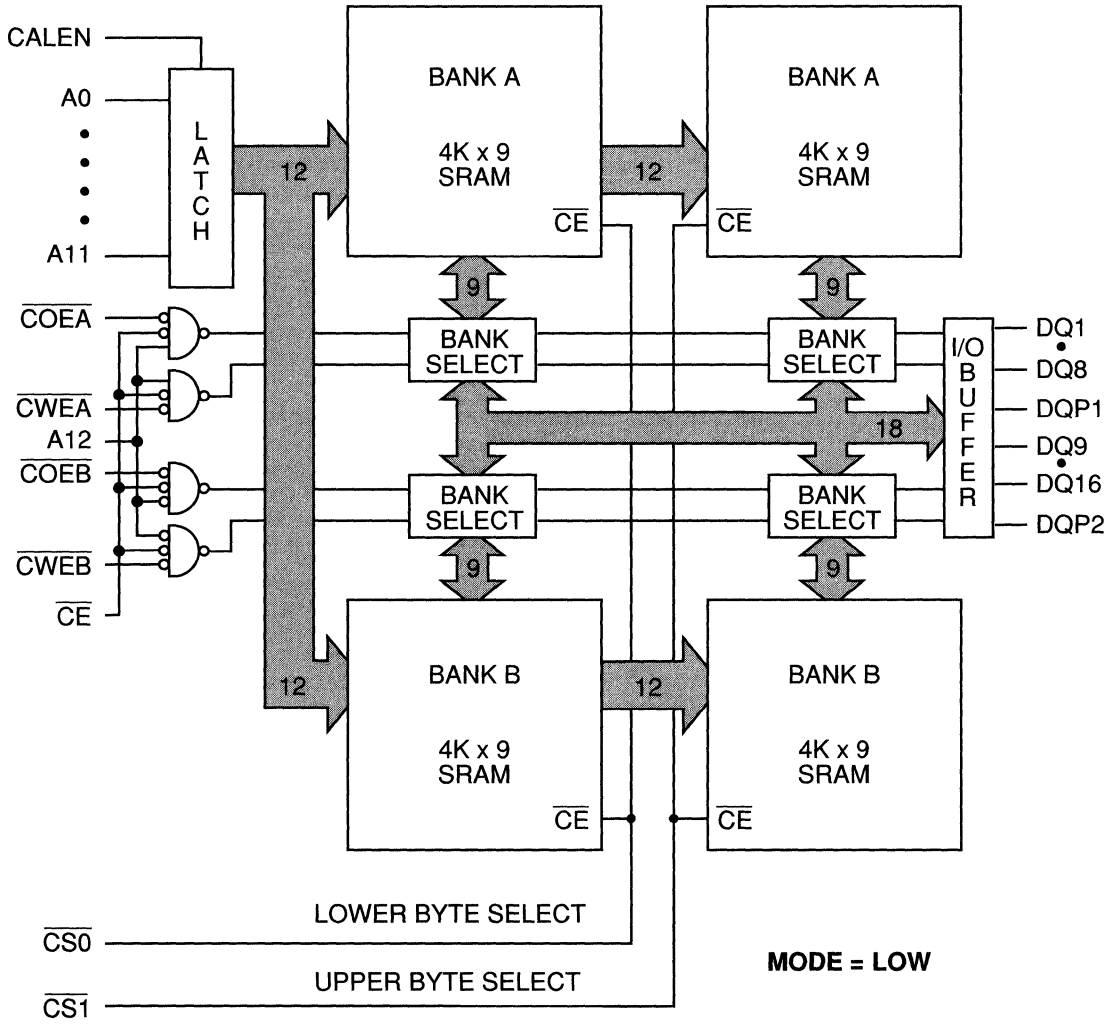
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 18
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM

8K x 18
(DIRECT MAP)



PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K x 18 configuration. It is not used in the dual 4K x 18 configuration.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A11).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 18 configuration. When the pin is tied LOW, the device is configured as an 8K x 18 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 and DQP1 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 and DQP2 are enabled.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected, and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	Write Enable: In the dual configuration the signal that is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected, and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
20,34	DQP1 DQP2	Input/ Output	Parity Data I/O: DQP1 is the parity bit for the lower byte. DQP2 is the parity bit for the upper byte.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ± 5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 18 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1 - DQ8, DQP1 bank A	L	L	H	L	H	H	H
READ DQ1 - DQ8, DQP1 bank B	L	L	H	H	L	H	H
READ DQ9 - DQ16, DQP2 bank A	L	H	L	L	H	H	H
READ DQ9 - DQ16, DQP2 bank B	L	H	L	H	L	H	H
READ DQ1 - DQ16, DQP1, DQP2 bank A	L	L	L	L	H	H	H
READ DQ1 - DQ16, DQP1, DQP2 bank B	L	L	L	H	L	H	H
WRITE DQ1 - DQ8, DQP1 bank A	L	L	H	X	X	L	H
WRITE DQ1 - DQ8, DQP1 bank B	L	L	H	X	X	H	L
WRITE DQ9 - DQ16, DQP2 bank A	L	H	L	X	X	L	H
WRITE DQ9 - DQ16, DQP2 bank B	L	H	L	X	X	H	L
WRITE DQ1 - DQ16, DQP1, DQP2 bank A	L	L	L	X	X	L	H
WRITE DQ1 - DQ16, DQP1, DQP2 bank B	L	L	L	X	X	H	L
WRITE DQ1 - DQ8, DQP1 bank A & B	L	L	H	X	X	L	L
WRITE DQ9 - DQ16, DQP2 bank A & B	L	H	L	X	X	L	L
WRITE DQ1 - DQ16, DQP1, DQP2 bank A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE

8K x 18 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1 - DQ8, DQP1	L	L	H	L	L	H	H
READ DQ9 - DQ16, DQP2	L	H	L	L	L	H	H
READ DQ1 - DQ16, DQP1, DQP2	L	L	L	L	L	H	H
WRITE DQ1 - DQ8, DQP1	L	L	H	X	X	L	L
WRITE DQ9 - DQ16, DQP2	L	H	L	X	X	L	L
WRITE DQ1 - DQ16, DQP1, DQP2	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ and $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

$\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature ..... -55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 5\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		V_{CC}	4.75	5.25	V	
Input High Voltage		V_{IH}	2.2	V_{CC}+0.3	V	1
Input Low Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	V_{IN} = GND to V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	$V_{I/O}$ = GND to V_{CC} Output(s) Disabled	I_{LO}	-10	10	µA	
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty cycle V_{IN} = GND to V_{CC}	I_{CC1}		220	mA	
Power Supply Current: Average Operating Current	50% Duty cycle V_{IN} = GND to V_{CC}	I_{CC2}		120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0}$ = $\overline{CS1}$ ≥ V_{CC} - 0.2V V_{CC} = MAX $V_{IL} \le V_{SS}$ + 0.2V $V_{IH} \ge V_{CC}$ - 0.2V	I_{SB}		20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_{IN}		6	pF	3
Output Capacitance	V_{CC} = 5V	$C_{I/O}$		6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	θ_{JA}		100	°C/W	
Thermal resistance - Junction to Case		θ_{JC}		45	°C/W	
Maximum Case Temperature		Tc		110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 5\%$)

DESCRIPTION		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	tRC	20		25		35		ns	4, 5
Address access time (A0-A11)	tAA		20		25		35	ns	
A12 address access time	tA12A		15		17		25	ns	
Chip Enable access time	tACE		20		20		25	ns	
Chip Select access time	tACS		20		25		35	ns	
Output Enable access time	tAOE		8		10		13	ns	
Output hold from address change	tOH	3		3		3		ns	
Chip Select to output Low-Z	tLZCS	3		3		3		ns	
Output Enable to output Low-Z	tLZOE	2		2		2		ns	
Chip deselect to output High-Z	tHZCS		15		15		25	ns	6
Output disable to output High-Z	tHZOE		10		10		14	ns	6
Address latch enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	tWC	20		25		35		ns	
Address valid to end of write	tAW	15		18		25		ns	
A12 address valid to end of write	tA12W	15		18		25		ns	
Chip Select to end of write	tCW	15		18		25		ns	
Data valid to end of write	tDW	10		10		10		ns	
Data hold from end of write	tDH	0		0		0		ns	
Write enable output in High-Z	tHZWE		12		15		15	ns	6
Write disable to output in Low-Z	tLZWE	3		3		3		ns	
Write pulse width	tWP	15		18		25		ns	
$\overline{CE}$ pulse width (during Chip Enable controlled write)	tCP	15		18		25		ns	
Address setup time	tAS	0		0		0		ns	
Write recovery time	tWR	0		0		0		ns	
Address latch enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

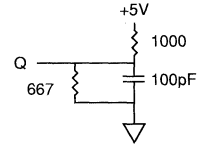


Fig. 1 OUTPUT LOAD EQUIVALENT

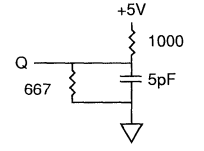


Fig. 2 OUTPUT LOAD EQUIVALENT

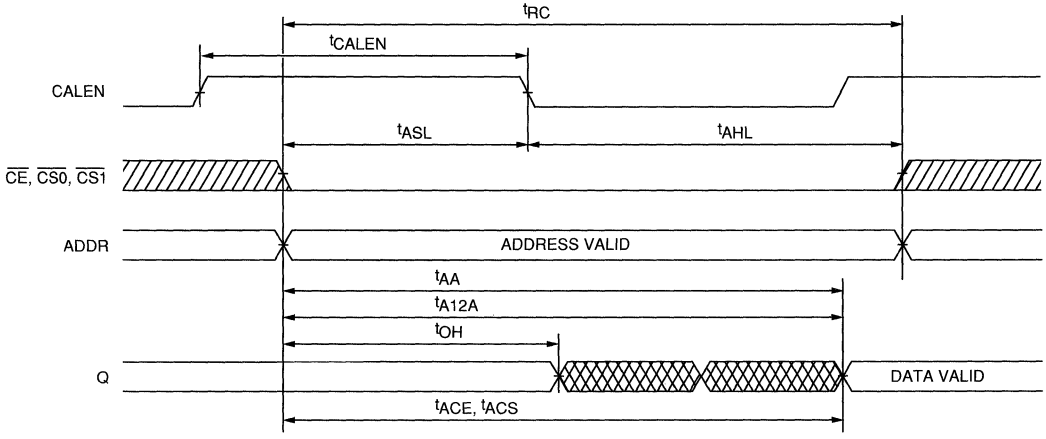
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. tHZCS, tHZOE, and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.

READ CYCLE NO. 1

(Address Controlled)

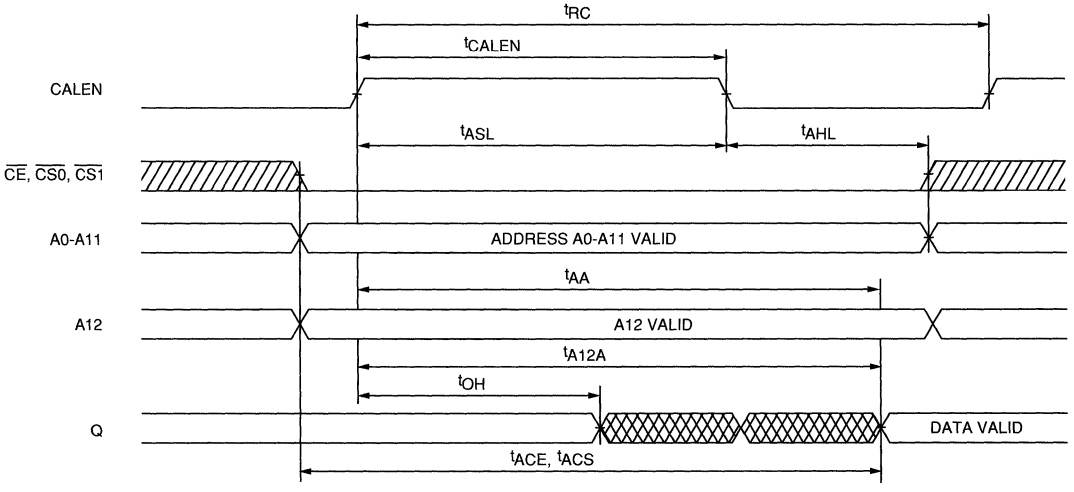
$\overline{CWEA}$ = $\overline{CWEB}$ =V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}



READ CYCLE NO. 2

(CALEN Controlled)

$\overline{CWEA}$ = $\overline{CWEB}$ =V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}

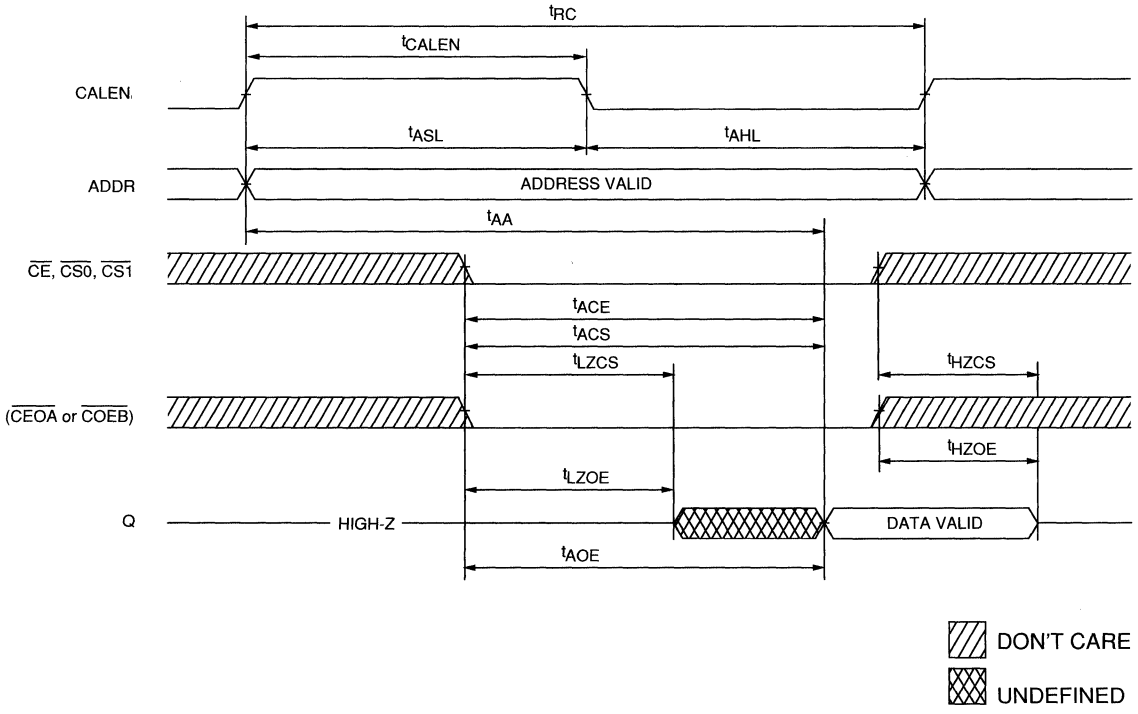


DON'T CARE

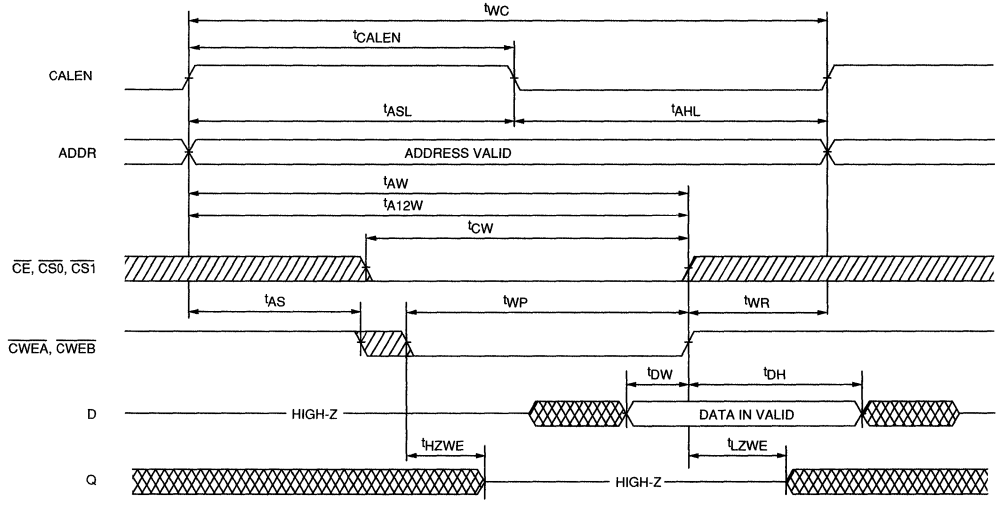
UNDEFINED

READ CYCLE NO. 3

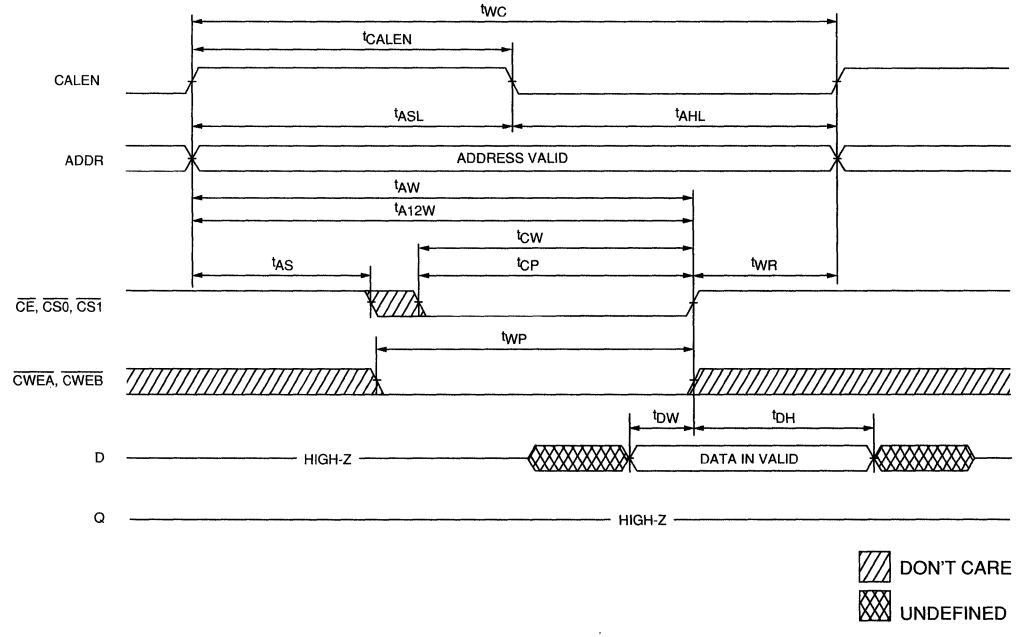
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



CACHE DATA STATIC RAM

DUAL 4K x 18 SRAM, SINGLE 8K x 18 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

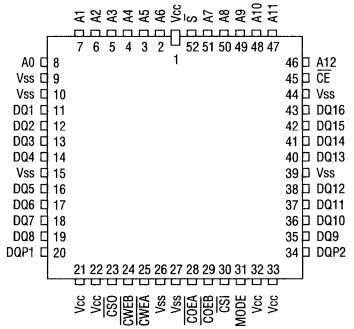
- Automatic WRITE cycle completion
- Operates as two 4K x 18 SRAMs with common addresses and data; also configurable as a single 8K x 18 SRAM
- Automatically controlled input address latches
- Built-in input data latches
- Separate upper and lower Byte Select
- Fast access times: 24ns and 28ns allow operation with 33MHz and 25MHz microprocessor systems
- Fast Output Enable: 8ns
- Parity bits provided for large cache applications such as secondary cache for the Intel 80486 microprocessor
- Directly compatible with the Intel 82485 cache controller

OPTIONS

	MARKING
• Timing	
24ns access (33 MHz)	-24
28ns access (25 MHz)	-28
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-4)



GENERAL DESCRIPTION

The MT56C2818 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C2818 is a highly integrated cache data memory building block. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 18-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 18-bit SRAM.

Strobe ($\overline{S}$)controls the on-chip address and data latches. During READ and WRITE cycles the address latch is always transparent except for the time period ^{t}ALO following the rising edge of $\overline{S}$. The addresses are "locked out" during this time.

$\overline{S}$ has no effect on the data latch during a READ cycle. During a WRITE cycle, data is latched on the rising edge of $\overline{S}$. The rising edge of $\overline{S}$ also initiates the completion of the WRITE cycle.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations. Power consumption may be reduced by keeping either $\overline{CE}$ inactive (HIGH), or $\overline{CS0}$ and $\overline{CS1}$ inactive (HIGH) as much as possible.

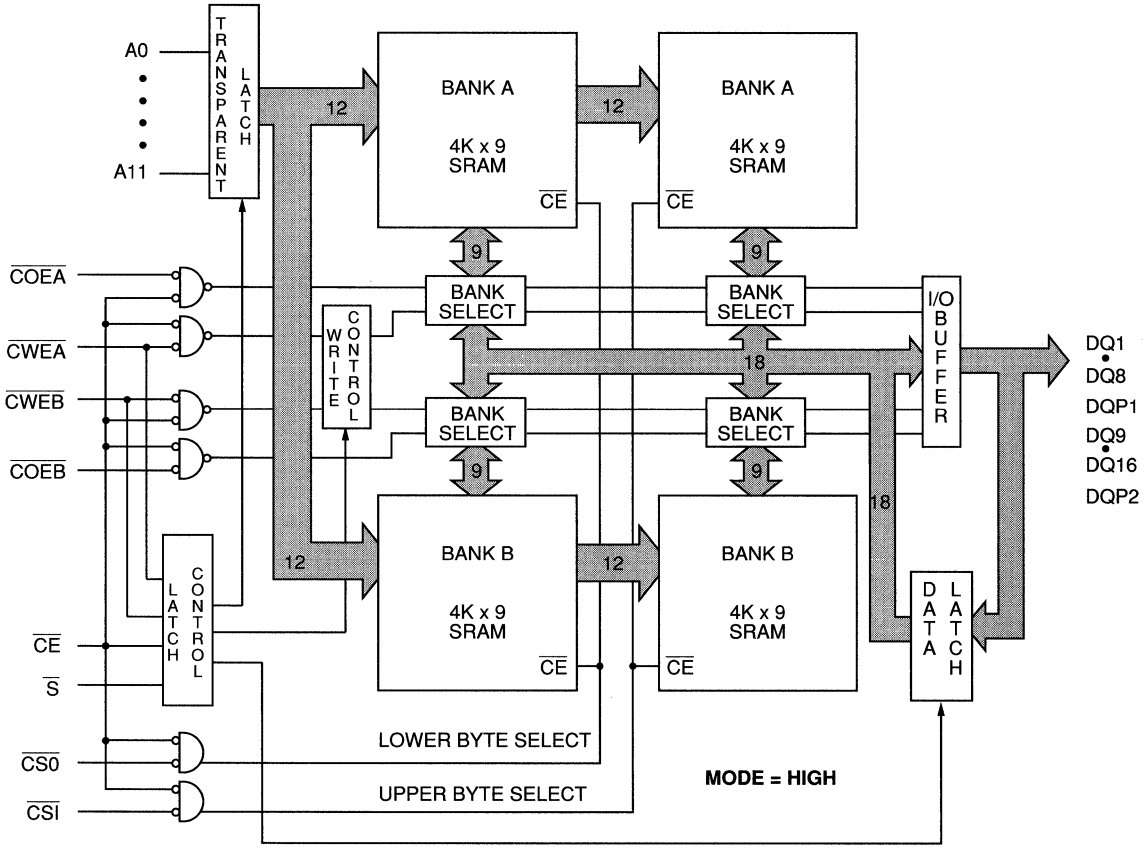
Outputs are enabled on a HIGH to LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH to LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C2818 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

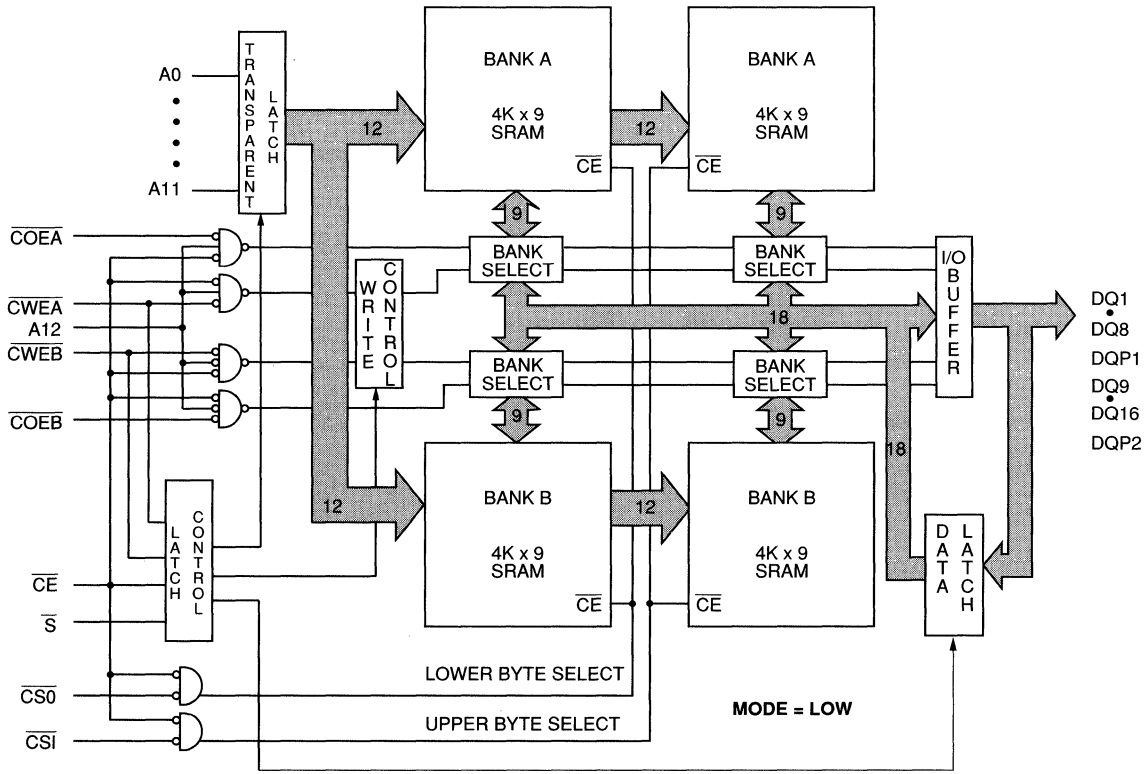
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 18
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM
($\overline{COEA}$ = $\overline{COEB}$; $\overline{CWEA}$ = $\overline{CWEB}$)

8K x 18
(DIRECT MAP)



CACHE DATA SRAM

PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: A0-A11 are always sampled (transparent latch) except for the time ^{t}WAH and ^{t}ALO following the rising edge of $\overline{S}$.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K x 18 configuration. It is not used in the dual 4K x 18 configuration.
52	$\overline{S}$	Input	Strobe: This signal controls the internal data and address latches. The address latch is always transparent except for the time period ^{t}ALO following the rising edge of $\overline{S}$. The addresses are "locked out" during this time period. $\overline{S}$ does not affect the data latch during a READ cycle. During a WRITE cycle the rising edge of $\overline{S}$ latches the data. The rising edge also initiates the termination of the WRITE cycle.
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 18 configuration. When the pin is tied LOW, the device is configured as an 8K x 18 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 and DQP1 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 and DQP2 are enabled. Significant power savings can be achieved by keeping $\overline{CS0}$ and $\overline{CS1}$ inactive as much as possible.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank "A" and bank "B" for READ or WRITE operations. Significant power savings can be achieved by keeping $\overline{CE}$ inactive as much as possible.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration, the signal that is LOW enables bank "A" or "B". Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	Write Enable: In the dual configuration, the signal that is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
20, 34	DQP1, DQP2	Input/ Output	Parity Data I/O: DQP1 is the parity bit for the lower byte. DQP2 is the parity bit for the upper byte.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ± 5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 18 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1 - DQ8, DQP1 bank A	L	L	H	L	H	H	H
READ DQ1 - DQ8, DQP1 bank B	L	L	H	H	L	H	H
READ DQ9 - DQ16, DQP2 bank A	L	H	L	L	H	H	H
READ DQ9 - DQ16, DQP2 bank B	L	H	L	H	L	H	H
READ DQ1 - DQ16, DQP1, DQP2 bank A	L	L	L	L	H	H	H
READ DQ1 - DQ16, DQP1, DQP2 bank B	L	L	L	H	L	H	H
WRITE DQ1 - DQ8, DQP1 bank A	L	L	H	X	X	L	H
WRITE DQ1 - DQ8, DQP1 bank B	L	L	H	X	X	H	L
WRITE DQ9 - DQ16, DQP2 bank A	L	H	L	X	X	L	H
WRITE DQ9 - DQ16, DQP2 bank B	L	H	L	X	X	H	L
WRITE DQ1 - DQ16, DQP1, DQP2 bank A	L	L	L	X	X	L	H
WRITE DQ1 - DQ16, DQP1, DQP2 bank B	L	L	L	X	X	H	L
WRITE DQ1 - DQ8, DQP1 bank A & B	L	L	H	X	X	L	L
WRITE DQ9 - DQ16, DQP2 bank A & B	L	H	L	X	X	L	L
WRITE DQ1 - DQ16, DQP1, DQP2 bank A & B	L	L	L	X	X	L	L

TRUTH TABLE

8K x 18 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1 - DQ8, DQP1	L	L	H	L	L	H	H
READ DQ9 - DQ16, DQP2	L	H	L	L	L	H	H
READ DQ1 - DQ16, DQP1, DQP2	L	L	L	L	L	H	H
WRITE DQ1 - DQ8, DQP1	L	L	H	X	X	L	L
WRITE DQ9 - DQ16, DQP2	L	H	L	X	X	L	L
WRITE DQ1 - DQ16, DQP1, DQP2	L	L	L	X	X	L	L

NOTE: When mode pin is LOW, $\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5.0V ± 5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		VIH	2.2	Vcc +0.3	V	1
Input Low Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	VIN = GND to Vcc	ILI	-10	10	µA	
Output Leakage Current	VI/O = GND to Vcc Output(s) Disabled	ILO	-10	10	µA	
Output Low Voltage	IOL = 4.0mA	VOL		0.4	V	1
Output High Voltage	IOH = -1.0mA	VOH	2.4		V	1

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty cycle VIN = GND to Vcc		ICC1		220	mA	
Power Supply Current: Average Operating Current	50% Duty cycle VIN = GND to Vcc		ICC2		120	mA	
Power Supply Current: CMOS Standby	$\overline{CS1} \ge$ Vcc -0.2V and $\overline{CS0} \ge$ Vcc -0.2V or Vcc = MAX, f = 0, VIL ≤ Vss +0.2V, VIH ≥ Vcc -0.2V	CE≤ Vss +0.2V	ISB1		20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; Vcc = 5V f = 1MHz,	CIN		6	pF	3
Input/Output Capacitance		CI/O		6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	$\emptyset_{JA}$		100	°C/W	
Thermal resistance - Junction to Case		$\emptyset_{JC}$		45	°C/W	
Maximum Case Temperature		Tc		110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 8) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ±5%)

DESCRIPTION	SYM	-24 MIN	-24 MAX	-28 MIN	-28 MAX	UNITS	NOTES
READ Cycle							
READ cycle time	tRC	24		28		ns	4, 5
Address access time (A0-A11)	tAA		24		28	ns	4, 5
A12 address access time	tA12A		17		19	ns	
Chip Enable access time	tACE		23		26	ns	
Chip Select access time	tACS		23		26	ns	
Output Enable access time	tAOE		8		10	ns	
Output hold from address change	tOH	3		3		ns	
Chip select/chip enable to output Low-Z	tLZCS	3		3		ns	
Output Enable to output Low-Z	tLZOE	2		2		ns	
Chip deselect/chip disable to output High-Z	tHZCS		15		15	ns	6
Output disable to output High-Z	tHZOE	2	10	2	10	ns	6
WRITE Cycle							
WRITE cycle time	tWC	24		28		ns	
$\overline{S}$ strobe HIGH level width	tSWH	11		14		ns	7
$\overline{S}$ strobe LOW level width	tSWL	11		14		ns	7
WRITE, Chip Enable/Write Enable to $\overline{S}$ strobe setup	tWSS	10		12		ns	7
WRITE, Chip Enable/Write Enable to $\overline{S}$ strobe hold	tWSH	2		2		ns	7
WRITE, address setup to $\overline{S}$ strobe	tWAS	13		16		ns	7
WRITE, address hold to $\overline{S}$ strobe	tWAH	2		2		ns	7
Address latch closed	tALO		8		8	ns	7
Chip Select to $\overline{S}$ strobe setup	tCSS	13		16		ns	7
Chip Select to $\overline{S}$ strobe hold	tCSH	2		2		ns	7
Data to $\overline{S}$ strobe setup	tDSS	5		5		ns	7
Data to $\overline{S}$ strobe hold	tDSH	3		3		ns	7
Write Enable to output in High-Z	tHZWE		15		15	ns	6
Write Enable to output in Low-Z	tLZWE	8		8		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load (see notes 6 and 8).	Reference Figure 1

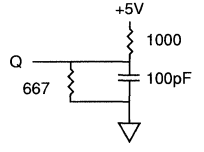


Fig. 1 OUTPUT LOAD EQUIVALENT

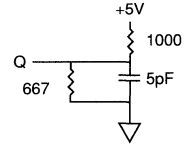
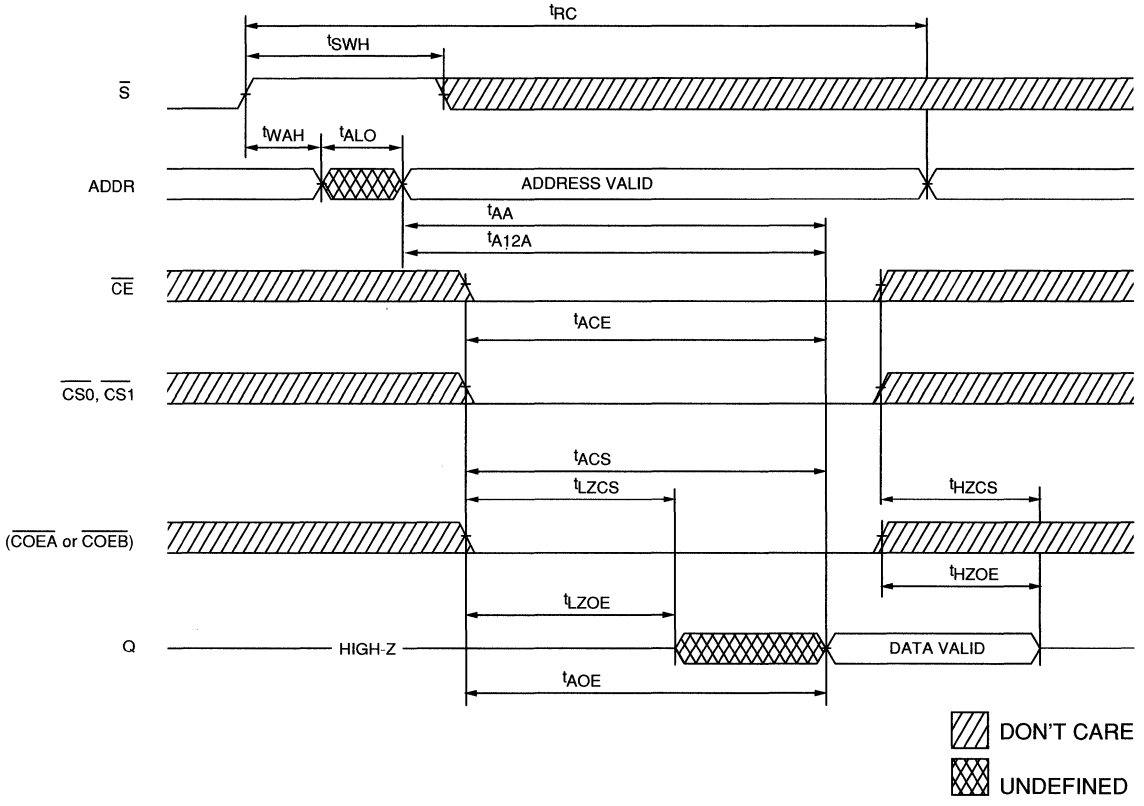


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

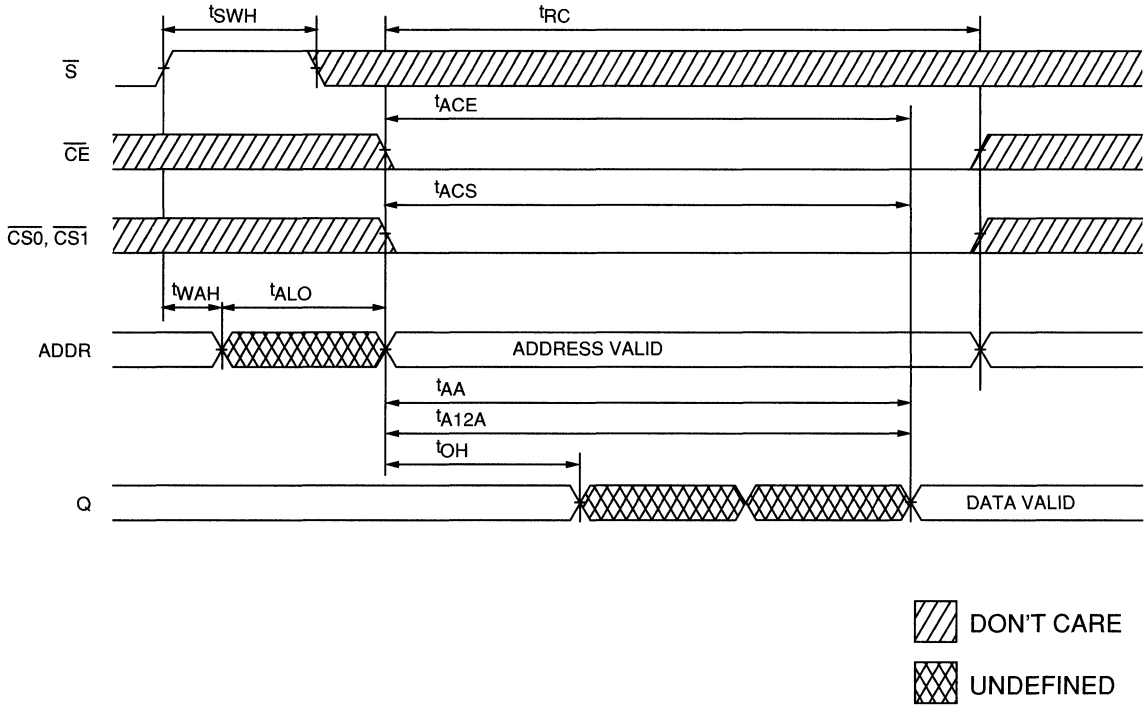
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. tHZCS, tHZOE, and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. Self-timed WRITE parameter.
8. Output timing should be derated by 1ns for each additional 30pf of capacitive loading.

READ CYCLE NO. 1
($\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH})

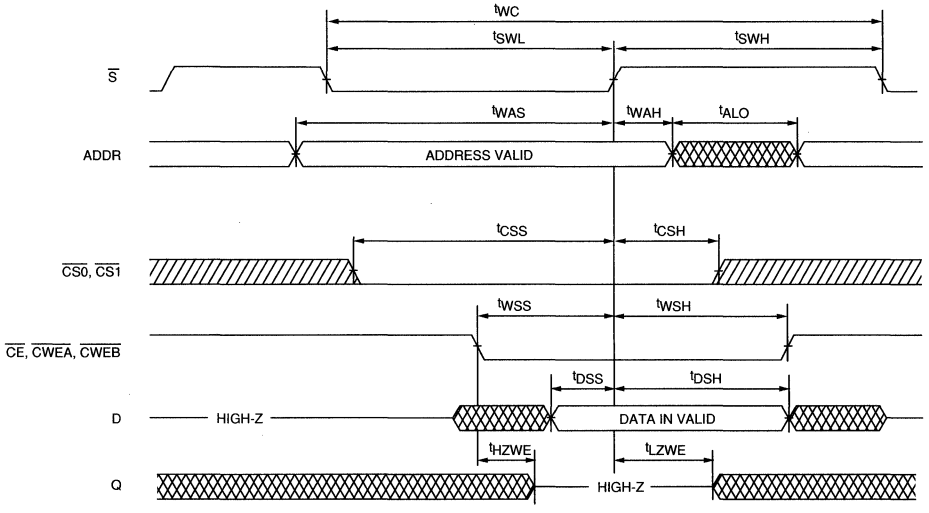


READ CYCLE NO. 2

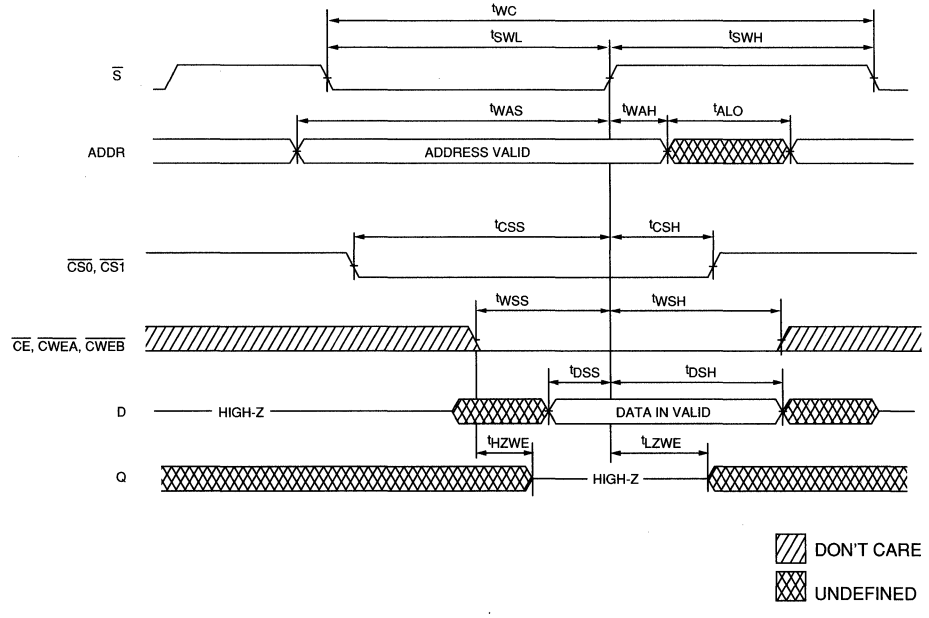
($\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL})
($\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH})



WRITE CYCLE NO. 1
(Write Enable/Chip Enable controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



CACHE DATA STATIC RAM

DUAL 4K x 18 SRAM, SINGLE 8K x 18 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

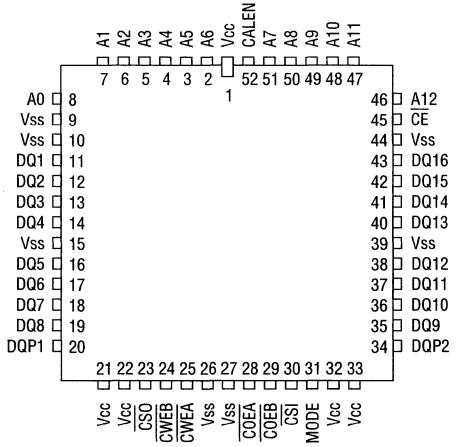
- Operates as two 4K x 18 SRAMs with common addresses and data; also configurable as a single 8K x 18 SRAM
- Built-in input address latches (A0-A12)
- Separate upper and lower Byte Select
- Fast access times: 20ns, 25ns and 35ns allow operation with 40, 33 and 25MHz microprocessor systems
- Fast Output Enable: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 and 80486 cache memory controllers
- Parity bits provided for large cache applications such as secondary cache for the Intel 80486 microprocessors

OPTIONS

	MARKING
• Timing	
20ns access (40 MHz)	-20
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-4)



GENERAL DESCRIPTION

The MT56C3818 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C3818 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either the DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE mode. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 18-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 18-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

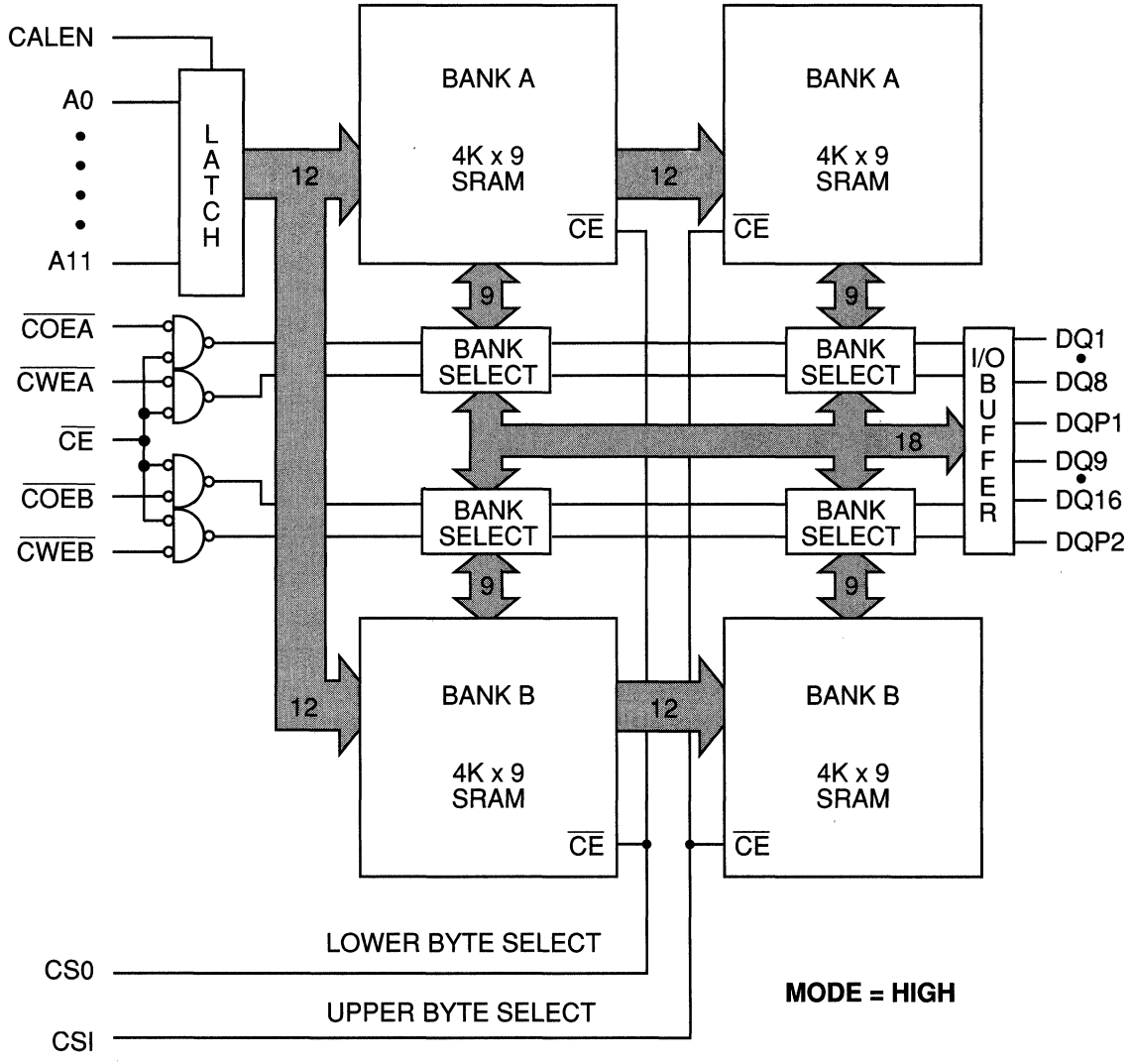
Outputs are enabled on a HIGH to LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH to LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C3818 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

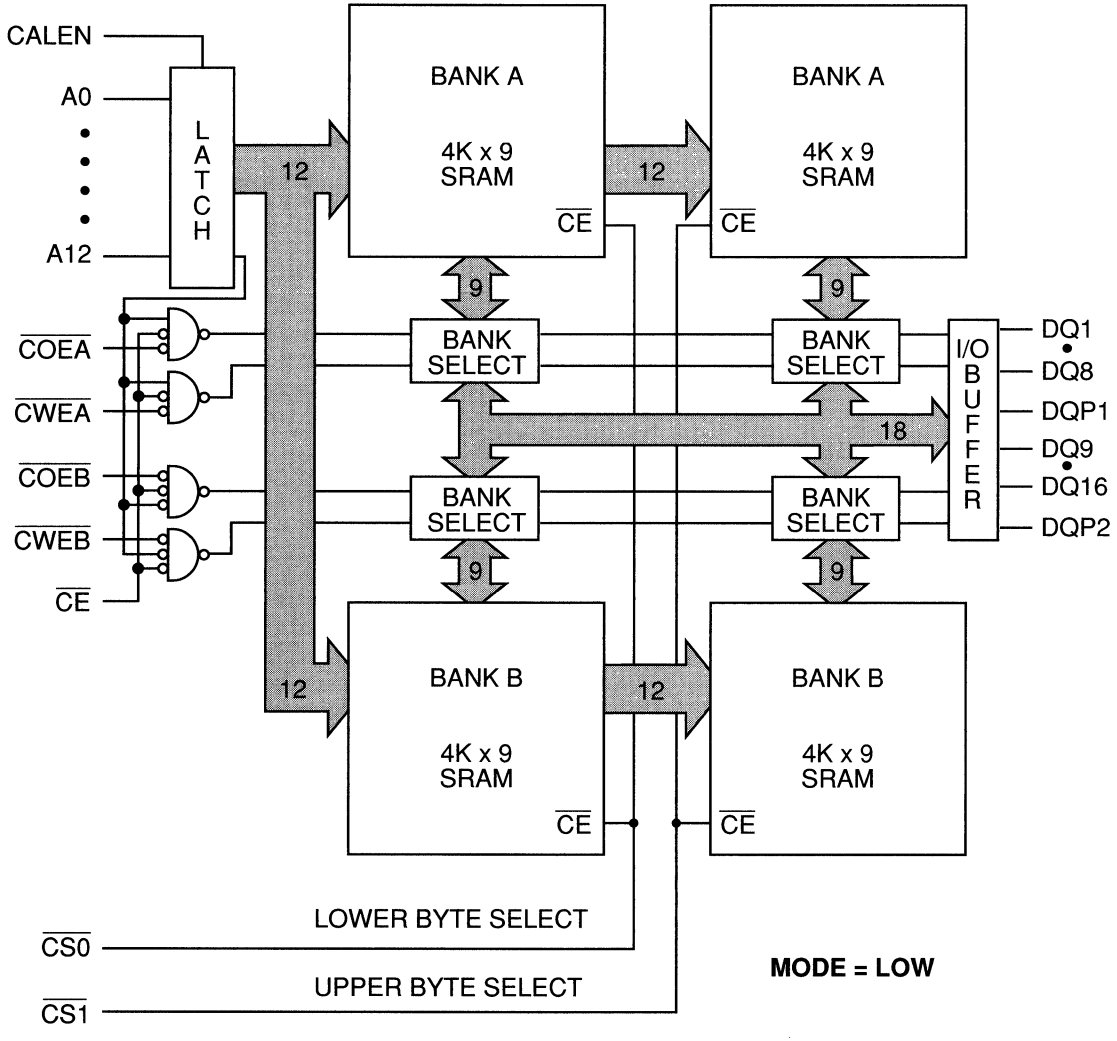
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 18
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM

8K x 18
(DIRECT MAP)



PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K x 18 configuration. It is not used in the dual 4K x 18 configuration. This input is latched by the negative edge of CALEN.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A12).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 18 configuration. When the pin is tied LOW, the device is configured as an 8K x 18 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 and DQP1 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 and DQP2 are enabled.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected, and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	Write Enable: In the dual configuration the signal that is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected, and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
20,34	DQP1 DQP2	Input/ Output	Parity Data I/O: DQP1 is the parity bit for the lower byte. DQP2 is the parity bit for the upper byte.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ± 5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 18 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1 - DQ8,DQP1 bank A	L	L	H	L	H	H	H
READ DQ1 - DQ8, DQP1 bank B	L	L	H	H	L	H	H
READ DQ9 - DQ16, DQP2 bank A	L	H	L	L	H	H	H
READ DQ9 - DQ16, DQP2 bank B	L	H	L	H	L	H	H
READ DQ1 - DQ16, DQP1, DQP2 bank A	L	L	L	L	H	H	H
READ DQ1 - DQ16, DQP1, DQP2 bank B	L	L	L	H	L	H	H
WRITE DQ1 - DQ8, DQP1 bank A	L	L	H	X	X	L	H
WRITE DQ1 - DQ8, DQP1 bank B	L	L	H	X	X	H	L
WRITE DQ9 - DQ16, DQP2 bank A	L	H	L	X	X	L	H
WRITE DQ9 - DQ16, DQP2 bank B	L	H	L	X	X	H	L
WRITE DQ1 - DQ16, DQP1, DQP2 bank A	L	L	L	X	X	L	H
WRITE DQ1 - DQ16, DQP1, DQP2 bank B	L	L	L	X	X	H	L
WRITE DQ1 - DQ8, DQP1 bank A & B	L	L	H	X	X	L	L
WRITE DQ9 - DQ16, DQP2 bank A & B	L	H	L	X	X	L	L
WRITE DQ1 - DQ16, DQP1, DQP2 bank A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE

8K x 18 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1 - DQ8, DQP1	L	L	H	L	L	H	H
READ DQ9 - DQ16, DQP2	L	H	L	L	L	H	H
READ DQ1 - DQ16, DQP1, DQP2	L	L	L	L	L	H	H
WRITE DQ1 - DQ8, DQP1	L	L	H	X	X	L	L
WRITE DQ9 - DQ16, DQP2	L	H	L	X	X	L	L
WRITE DQ1 - DQ16, DQP1, DQP2	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ and $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

$\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature ..... -55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5.0V ± 5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		VIH	2.2	Vcc +0.3	V	1
Input Low Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	VIN = GND to Vcc	ILI	-10	10	µA	
Output Leakage Current	VI/O = GND to Vcc Output(s) Disabled	ILO	-10	10	µA	
Output Low Voltage	IOL = 4.0mA	VOL		0.4	V	1
Output High Voltage	IOH = -1.0mA	VOH	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty cycle VIN = GND to Vcc	ICC1		220	mA	
Power Supply Current: Average Operating Current	50% Duty cycle VIN = GND to Vcc	ICC2		120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0}$ = $\overline{CS1}$ ≥ Vcc -0.2V Vcc = MAX VIL ≤ Vss +0.2V VIH ≥ Vcc -0.2V	ISB		20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	CIN		6	pF	3
Output Capacitance	Vcc = 5V	CI/O		6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	ØJA		100	°C/W	
Thermal resistance - Junction to Case		ØJC		45	°C/W	
Maximum Case Temperature		Tc		110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$, V_{CC} = 5.0V ±5%)

DESCRIPTION	SYM	-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	tRC	20		25		35		ns	4, 5
Address access time (A0-A12)	tAA		20		25		35	ns	
Chip Enable access time	tACE		20		20		25	ns	
Chip Select access time	tACS		20		25		35	ns	
Output Enable access time	tAOE		8		10		13	ns	
Output hold from address change	tOH	3		3		3		ns	
Chip Select to output Low-Z	tLZCS	3		3		3		ns	
Output Enable to output Low-Z	tLZOE	2		2		2		ns	
Chip deselect to output High-Z	tHZCS		15		15		25	ns	6
Output disable to output High-Z	tHZOE		10		10		14	ns	6
Address latch enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	tWC	20		25		35		ns	
Address valid to end of write	tAW	15		18		25		ns	
Chip Select to end of write	tCW	15		18		25		ns	
Data valid to end of write	tDW	10		10		10		ns	
Data hold from end of write	tDH	0		0		0		ns	
Write Enable output in High-Z	tHZWE		12		15		15	ns	6
Write disable to output in Low-Z	tLZWE	3		3		3		ns	
Write pulse width	tWP	15		18		25		ns	
$\overline{CE}$ pulse width (during Chip Enable controlled write)	tCP	15		18		25		ns	
Address setup time	tAS	0		0		0		ns	
Write recovery time	tWR	0		0		0		ns	
Address latch enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

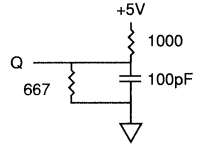


Fig. 1 OUTPUT LOAD EQUIVALENT

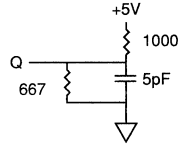


Fig. 2 OUTPUT LOAD EQUIVALENT

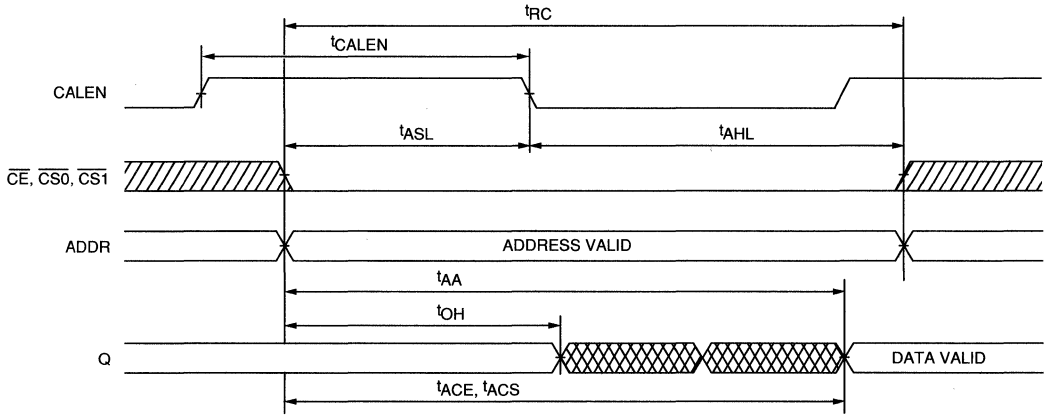
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. tHZCS, tHZOE, and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.

READ CYCLE NO. 1

(Address Controlled)

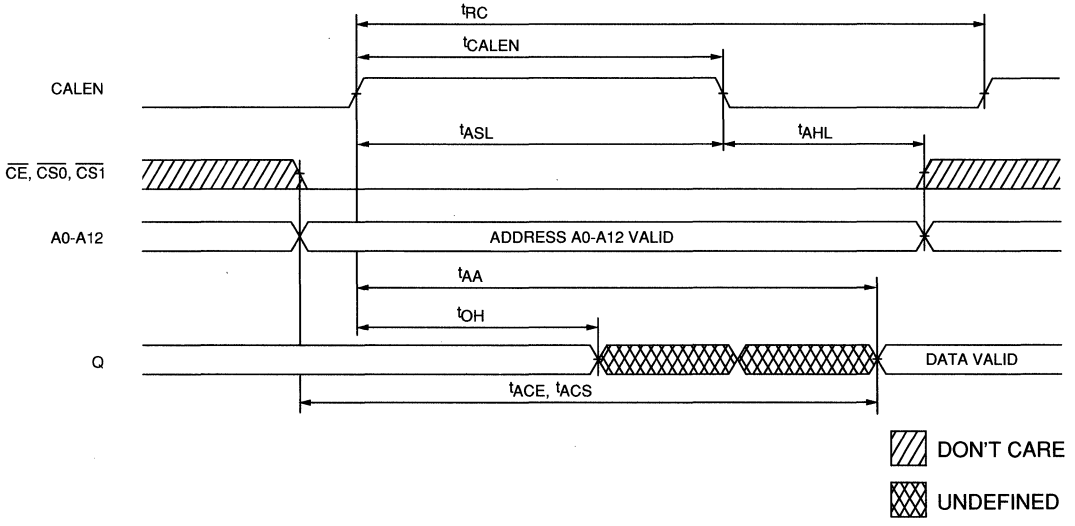
$\overline{CWEA}$ = $\overline{CWEB}$ =V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}



READ CYCLE NO. 2

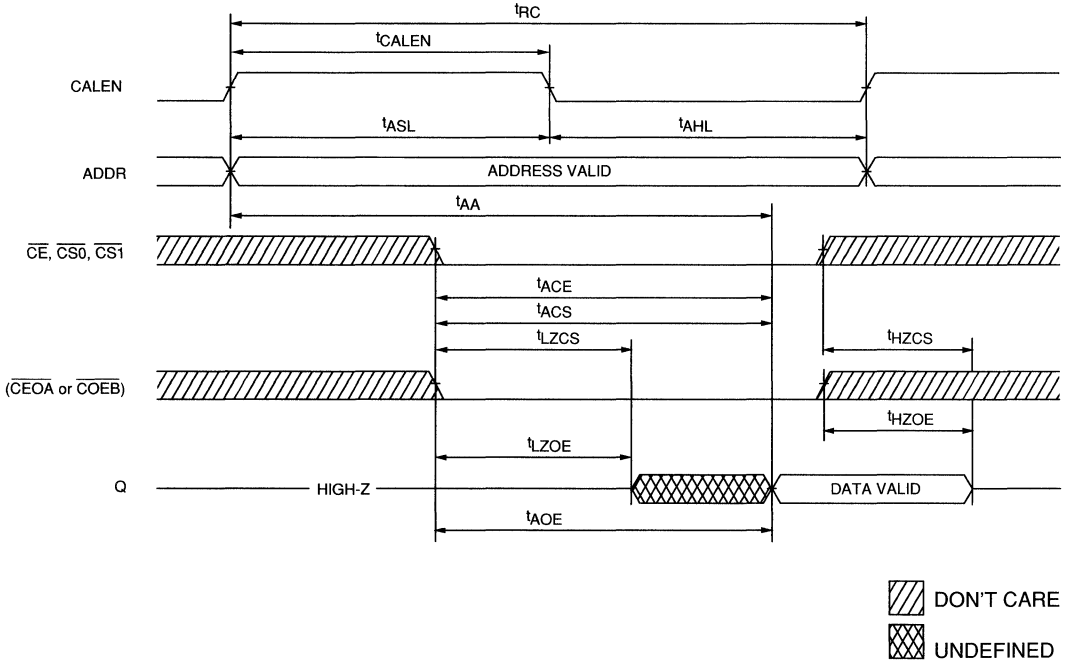
(CALEN Controlled)

$\overline{CWEA}$ = $\overline{CWEB}$ =V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}

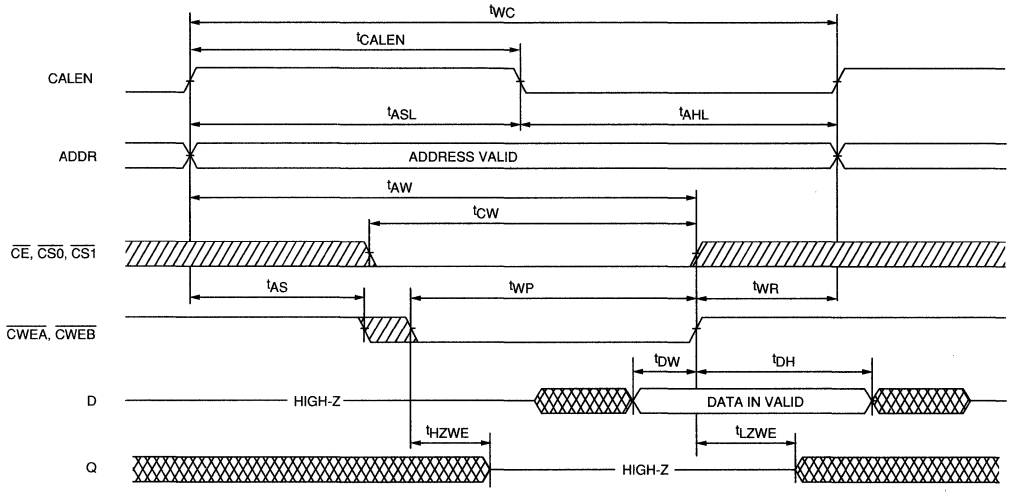


READ CYCLE NO. 3

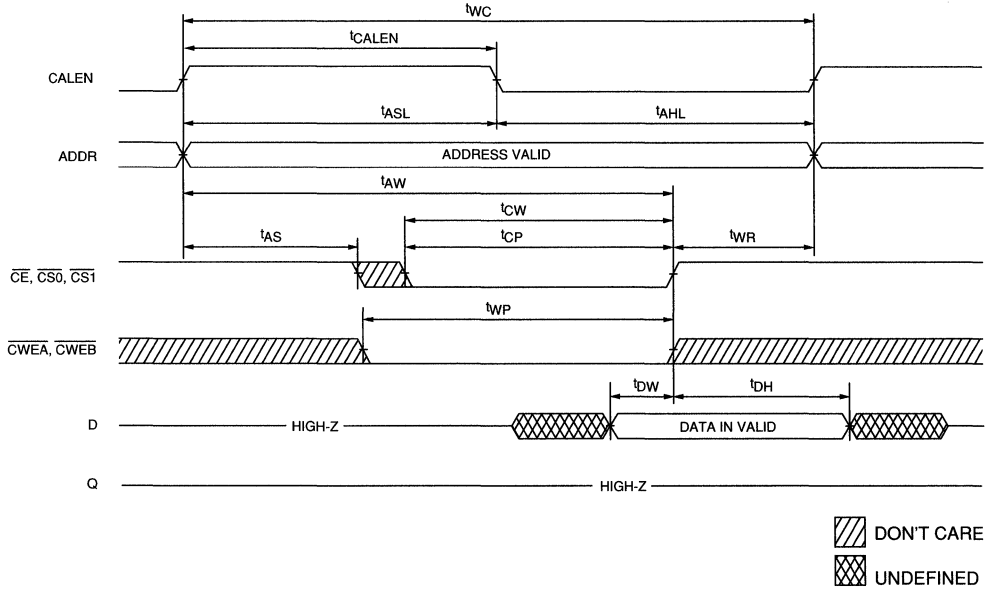
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



MICRON TECHNOLOGY, INC.

FIFO PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Cycle Time (ns)	Package and Number of Pins					Page
				PDIP	CDIP	LCC	PLCC	SOJ	
512 x 9	E	MT52C9005	15, 20, 25, 35	28	28	32	32	28	8-1
512 x 9	PF, E	MT52C9007	15, 20, 25, 35	28	28	32	32	28	8-13
1K x 9	E	MT52C9010	15, 20, 25, 35	28	28	32	32	28	8-29
1K x 9	PF, E	MT52C9012	15, 20, 25, 35	28	28	32	32	28	8-41
2K x 9	E	MT52C9020	15, 20, 25, 35	28	28	32	32	28	8-57
2K x 9	PF, E	MT52C9022	15, 20, 25, 35	28	28	32	32	28	8-69

E = Expandable Depth and Width, PF = Programmable Flag

FIFO

512 x 9 FIFO

FEATURES

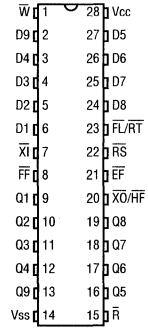
- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Empty, Half-Full and Full Flags
- Half-full flag in STAND ALONE mode
- Auto-retransmit capability
- Fully expandable by width and depth
- Pin and function compatible with higher density standard FIFOs

OPTIONS

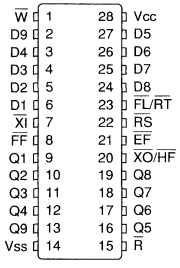
	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Ceramic DIP (600 mil)	C
PLCC	EJ
Ceramic LCC	EC
SOJ (300 mil)	DJ

PIN ASSIGNMENT (Top View)

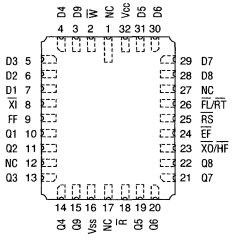
28L DIP (A-9, B-9)



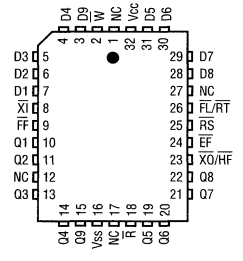
28L SOJ (E-8)



32L LCC (F-4)



32L PLCC (D-2)



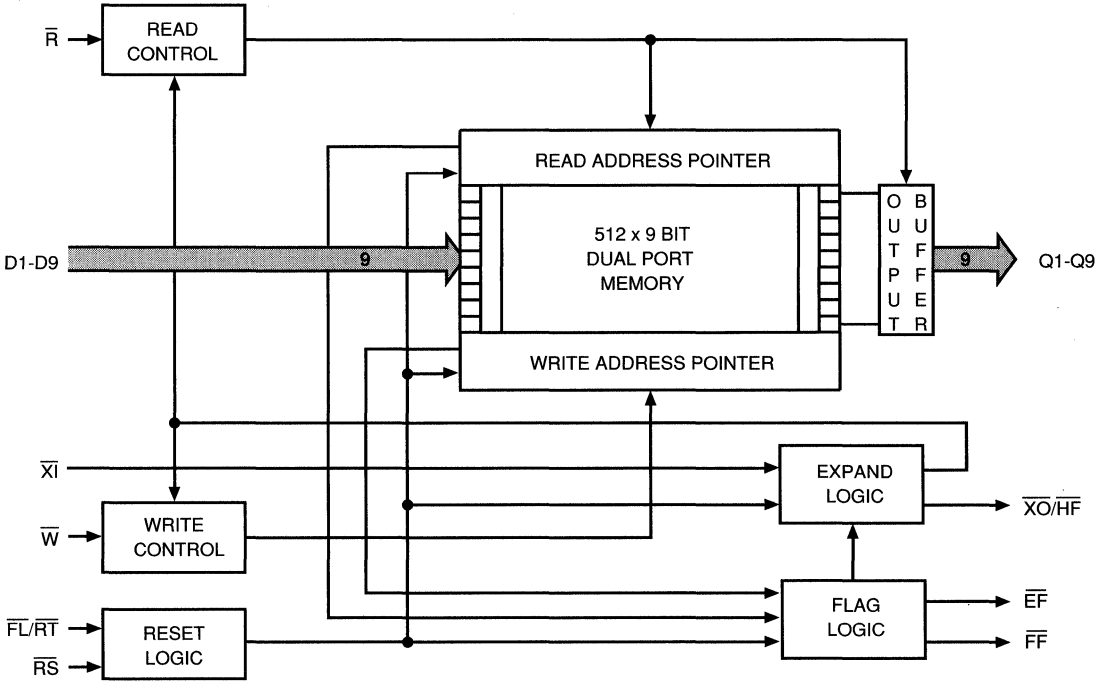
GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual port, six-transistor memory cell with resistor loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain in a high-impedance state. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. Also, the MT52C9005 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with 1K and 2K FIFOs provides a single-chip, depth-expansion solution.

FUNCTIONAL BLOCK DIAGRAM



FIFO

PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1-D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1-Q9).
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$)of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$	Input	First Load: Acts as first load signal in DEPTH EXPANSION mode. $\overline{FL}$, if low, will enable the device as the first to be loaded (enables read and write pointers). $\overline{FL}$ should be tied LOW for the first FIFO in the chain, tied HIGH for all other FIFOs in the chain. Retransmit: Acts as retransmit signal in STAND ALONE mode. $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO}/\overline{HF}$	Output	Expansion Out: Acts as expansion out pin in DEPTH EXPANSION mode. $\overline{XO}$ will pulse LOW on the last physical WRITE or the last physical READ. $\overline{XO}$ should be connected to $\overline{XI}$ of the next FIFO in the daisy chain. Half-full Flag: Acts as Half Full Flag in STAND ALONE mode. $\overline{HF}$ goes LOW when the FIFO becomes more than Half-full; will stay LOW until the FIFO becomes Half-full or less.
10, 11, 13, 14, 19, 20, 21, 22, 15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	Output	Data Output: Output or high impedance.
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9005 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing the half-full flag the $\overline{XO}/\overline{HF}$ pin will be shown as $(\overline{XO})/\overline{HF}$.*

RESET

After Vcc is stable, RESET ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is LOW. If $\overline{XI}$ is connected to $\overline{XO}$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the STAND ALONE mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (512/2 + 1) is written. It will stay asserted until the FIFO becomes half-full or less. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and the FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$ and valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is being used in the SINGLE DEVICE mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ LOW) and a read is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read to a FIFO will cause $\overline{XO}/\overline{HF}$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9005 allows the receiving device to request that the data read earlier from the FIFO to be repeated, when less than 512 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^tRTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. FLOW-THROUGH READs are initiated from the rising edge of $\overline{W}$ and access time is measured from the rising edge of $\overline{EF}$.

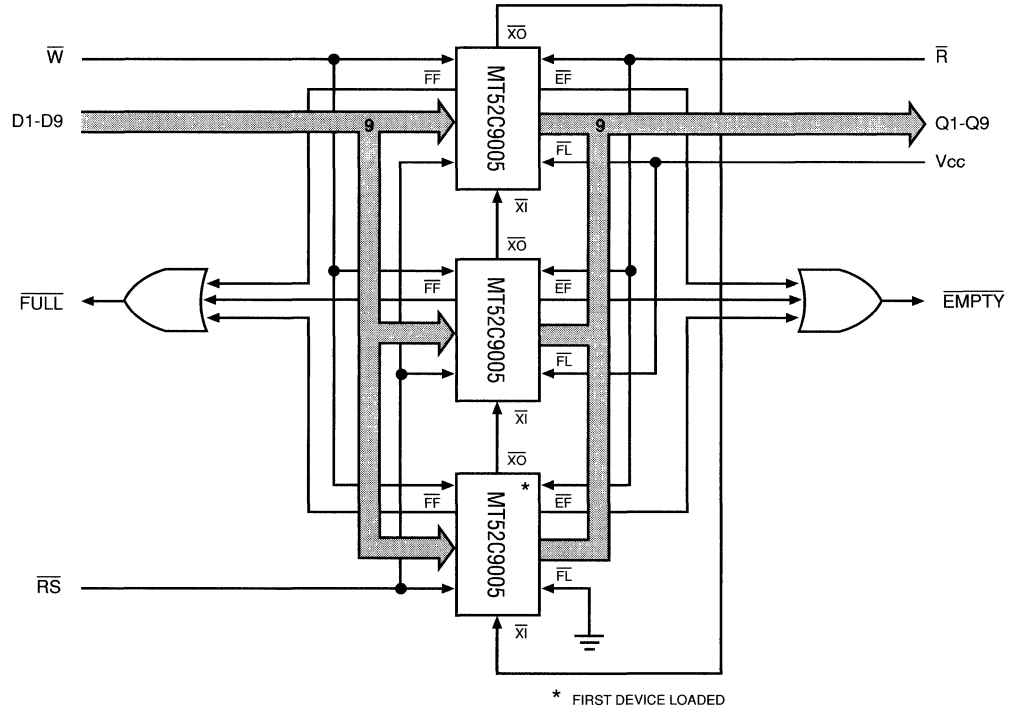


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the stand alone or groups of expanded-depth mode FIFOs. Expanded-width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1) when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9005s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}/(\overline{HF})$ and $\overline{FL}/(\overline{RT})$. Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered during a RESET cycle, by tying the $\overline{XO}/(\overline{HF})$ pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}/(\overline{RT})$ pin grounded. The remaining devices in the chain will have $\overline{FL}/(\overline{RT})$ tied HIGH. During RESET cycle, $\overline{XO}/(\overline{HF})$ of each device is held HIGH, disabling reads and writes to all FIFOs, except the first load device. When the last physical location of the first device is written, the $\overline{XO}/(\overline{HF})$ pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9005. The writes will continue to go to the second device until last location WRITE. Then it will "pass" the write pointer to the third device.

The full condition of the entire FIFO array is signaled by "OR-ing" all the $\overline{FF}$ pins. On the last physical READ of the first device, its $\overline{XO}/(\overline{HF})$ will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. An empty condition is signaled by OR-ing all of the $\overline{EF}$ pins. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$/DIR= First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -0.5V to +7.0V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

FIFO

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}, \overline{R} \le V_{IL}$; V_{CC} = MAX Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$W, \overline{R} \ge V_{IH}$; V_{CC} = MAX	I_{SB1}		15	mA	
	$\overline{W}, \overline{R} \ge V_{CC}$ -0.2; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}		5	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Shift Frequency	Fs		40		33.3		28.5		22.2	MHz	
Access time	^tA		15		20		25		35	ns	
Read cycle time	^tRC	25		30		35		45		ns	
Read command recovery time	^tRR	10		10		10		10		ns	
Read command pulse width	^tRPW	15		20		25		35		ns	6
Read LOW to Low-Z	^tRLZ	5		5		5		5		ns	
Read to HIGH to High-Z	^tRHZ		15		15		18		20	ns	
Data hold from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
Write cycle time	^tWC	25		30		35		45		ns	
Write command pulse width	^tWPW	15		20		25		35		ns	6
Write command recovery time	^tWR	10		10		10		10		ns	
Write HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5
Data setup time	^tDS	10		12		15		20		ns	
Data hold time	^tDH	0		0		0		0		ns	
Reset cycle time	^tRSC	25		30		35		45		ns	
Reset pulse width	^tRSP	15		20		25		35		ns	6
Reset recovery time	^tRSR	10		10		10		10		ns	
Read HIGH to Reset HIGH	^tRRS	15		20		25		35		ns	
Write HIGH to Reset HIGH	^tWRS	15		20		25		35		ns	
Retransmit cycle time	^tRTC	25		30		35		45		ns	
Retransmit pulse width	^tRT	15		20		25		35		ns	
Retransmit recovery time	^tRTR	10		10		10		12		ns	
Retransmit setup time	^tRTS	15		20		25		35		ns	
Reset to $\overline{EF}$ LOW	^tEFL		25		30		35		45	ns	
Reset to $\overline{HF}$ $\overline{FF}$ HIGH	^tHFH, ^tFFH		25		30		35		45	ns	
Read LOW to $\overline{EF}$ LOW	^tREF		20		20		25		35	ns	
Read HIGH to $\overline{FF}$ HIGH	^tRFF		20		20		25		35	ns	
Write LOW to $\overline{FF}$ LOW	^tWFF		20		20		25		35	ns	
Write HIGH to $\overline{EF}$ HIGH	^tWEF		20		20		25		35	ns	
Write LOW to $\overline{HF}$ LOW	^tWHF		25		30		35		45	ns	
Read HIGH to $\overline{HF}$ HIGH	^tRHF		25		30		35		45	ns	
Read pulse after $\overline{EF}$ HIGH	^tRPE	15		20		25		35		ns	5
Write pulse width after $\overline{FF}$ HIGH	^tWPF	15		20		25		35		ns	5
Read/Write to $\overline{XO}$ LOW	^tXOL		20		20		25		35	ns	
Read/Write to $\overline{XO}$ HIGH	^tXOH		20		20		25		35	ns	
$\overline{XI}$ pulse width	^tXIP	15		20		25		35		ns	
$\overline{XI}$ setup Time	^tXIS	10		12		15		15		ns	
$\overline{XI}$ recovery time	^tXIR	10		10		10		10		ns	

FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Flow-through mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

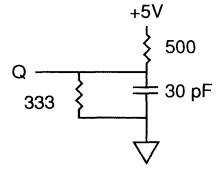
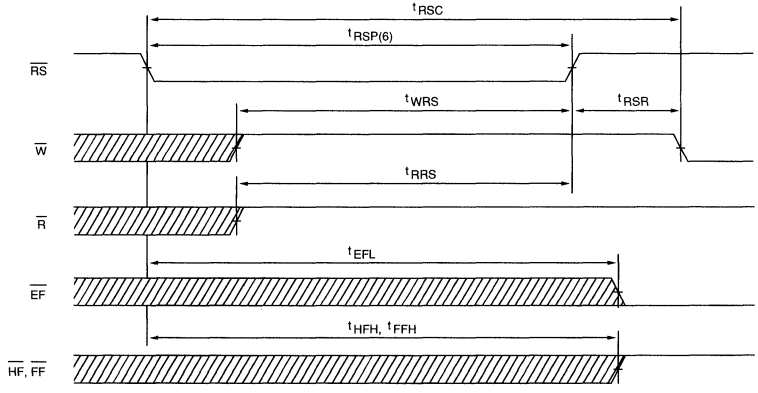
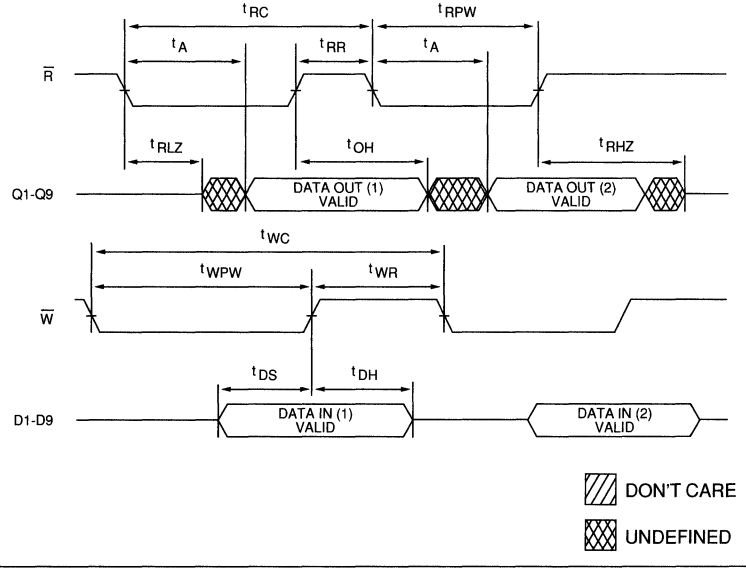


Fig. 2
OUTPUT LOAD EQUIVALENT

RESET

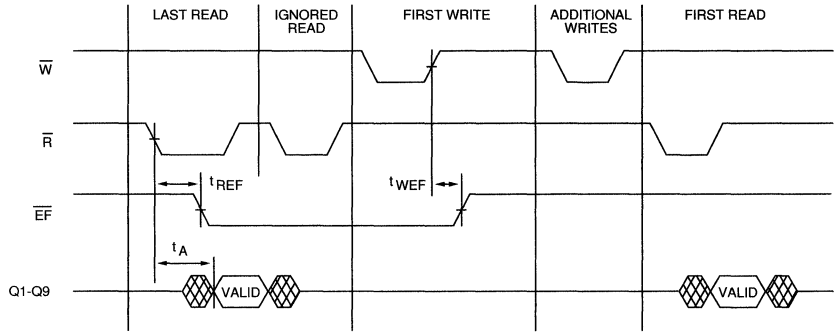


ASYNCHRONOUS READ AND WRITE

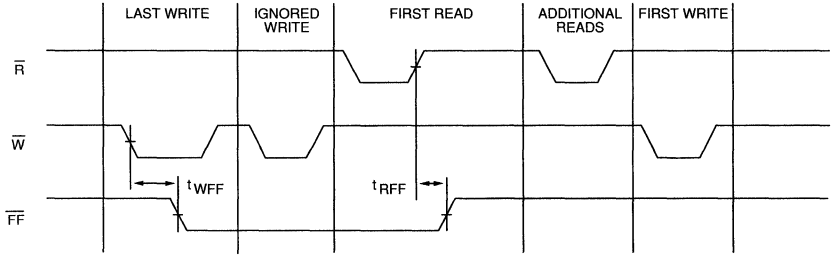


FIFO

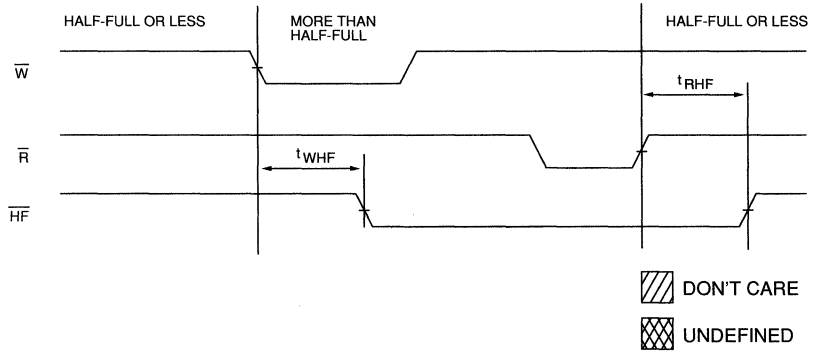
EMPTY FLAG



FULL FLAG

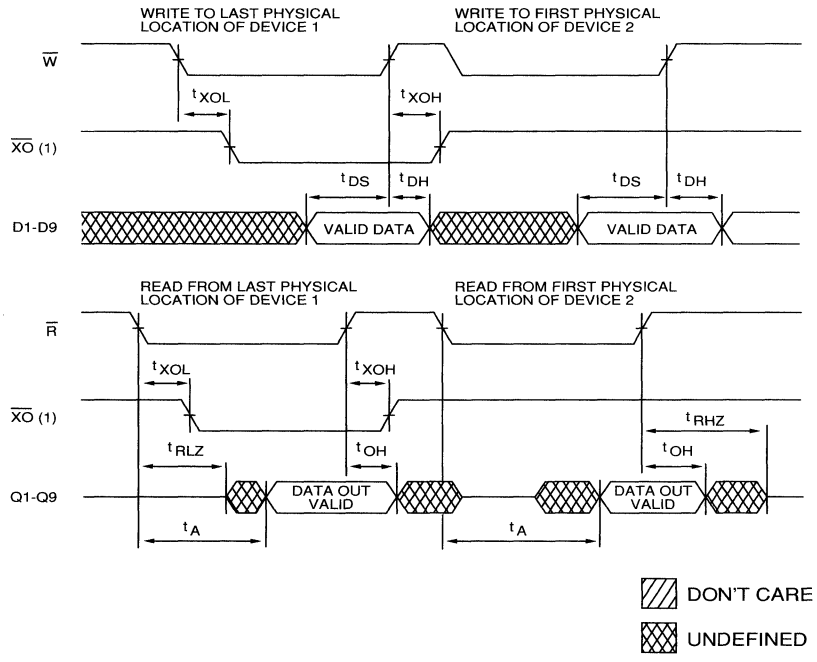


HALF-FULL FLAG



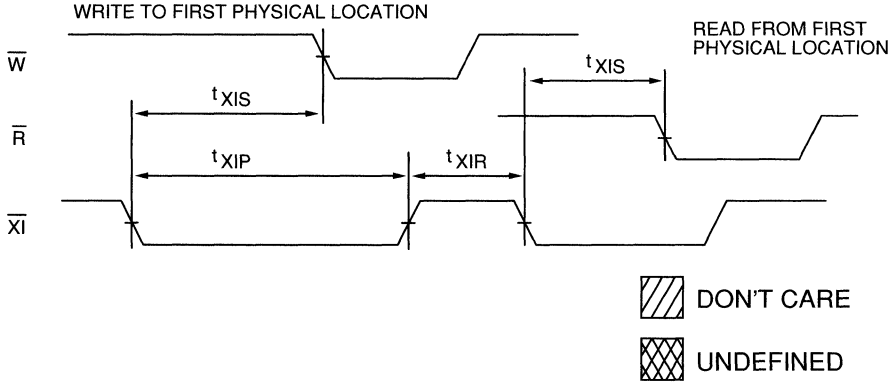
FIFO

EXPANSION MODE ($\overline{XO}$)



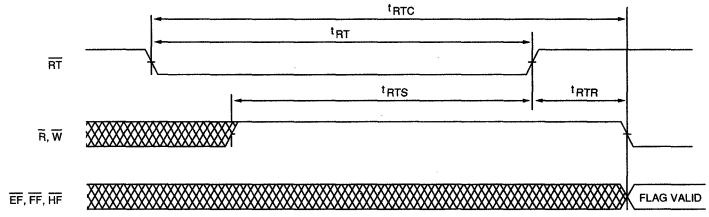
NOTE: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

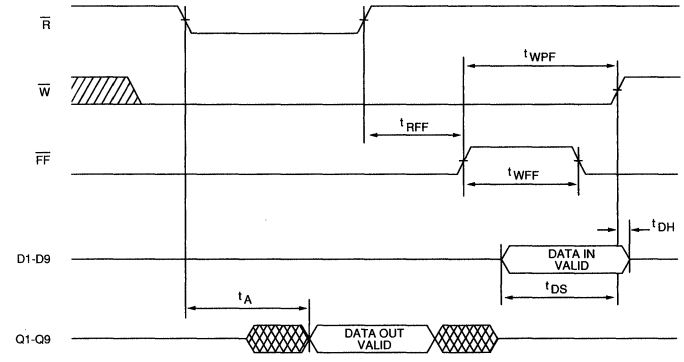


FIFO

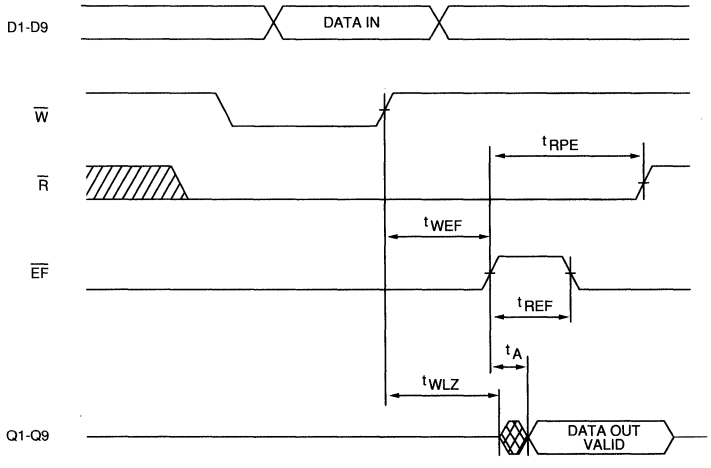
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



DON'T CARE

UNDEFINED

FIFO

512 x 9 FIFO

WITH PROGRAMMABLE FLAGS

FEATURES

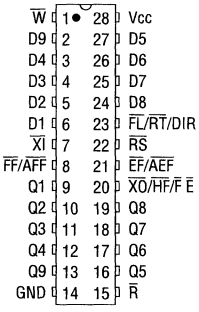
- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typical (standby); 350mW typical (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Two fully configurable Almost Full and Almost Empty Flags
- Programmable Half Full Flag or Full/Empty Flag option eliminates external counter requirement
- Register loading via the input or output pins
- Auto-retransmit capability in single-device mode
- Fully expandable by width and depth
- Pin and function compatible with standard FIFOs

OPTIONS

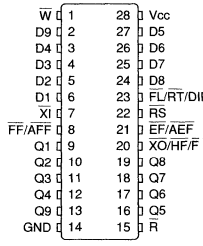
	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Ceramic DIP (600 mil)	C
PLCC	EJ
Ceramic LCC	EC
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

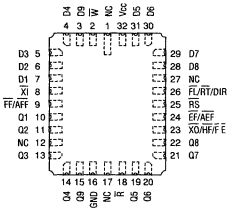
28L/DIP
(A-9, B-9)



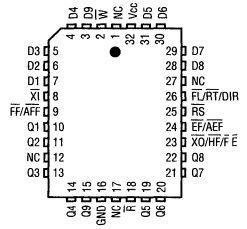
28L/SOJ
(E-8)



32L/LCC
(F-4)



32L/PLCC
(D-2)



GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

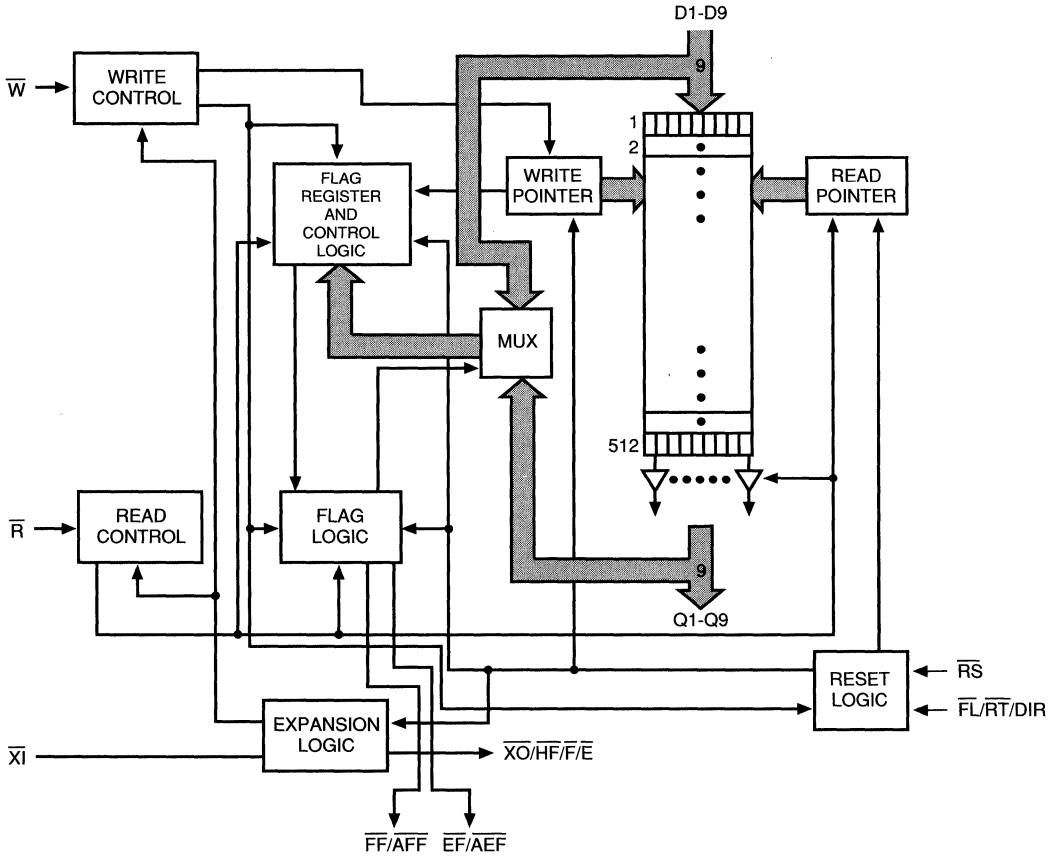
These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates.

When not configured, the MT52C9007 defaults to a standard FIFO with empty ($\overline{EF}$), full ($\overline{FF}$) and half-full ($\overline{HF}$) flag pins. The MT52C9007 can be configured for programmable flags by loading the internal flag registers (as described under "Register Load Mode" on page 8-17). In configured mode, up to three flags are provided. The first two are the almost empty flag ($\overline{AEF}$) and the almost full flag ($\overline{AFF}$) with independently programmable offsets. The third one is either an $\overline{HF}$ or a full and empty ($\overline{FE}$) flag, depending on the bit configuration of the registers. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. Also, the MT52C9007 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with 1K and 2K FIFOs provides a single-chip depth-expansion solution.

FIFO

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: This pin is used to reset the device and load internal flag registers. During device reset, all internal pointers and registers are cleared.
2	1	$\overline{W}$	Input	Write: A LOW on this pin loads data into the device. The internal write pointer is incremented after the rising edge of the write input.
18	15	$\overline{R}$	Input	Read: A LOW on this pin puts the oldest valid data byte in the memory array on the output bus. The internal read pointer is incremented at the rising edge of the read signal. Outputs are High-Z when this pin is HIGH.
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$)of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$/DIR	Input	First Load/Retransmit/Direction: When in single-device mode, this pin can be used to initiate a reread of the previously read data. When in REGISTER LOAD mode, the pin is used for register loading direction. When it is LOW, registers are loaded through the data output pins. When it is HIGH, registers are loaded through the data input pins. In DEPTH EXPANSION mode, this pin should be tied LOW if the device is the first one in the chain and tied HIGH if it is not the first one.
7, 6, 5, 4, 31, 30 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs: Data on these lines are stored in the memory array or flag registers during array WRITE or register programming, respectively.
24	21	$\overline{EF}/\overline{AEF}$	Output	Empty Flag/Almost Empty Flag: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is an Empty Flag output. When in CONFIGURED mode, it is an Almost Empty Flag output. This pin is active LOW.
9	8	$\overline{FF}/\overline{AFF}$	Output	Full Flag/Almost Full Flags: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is a Full Flag output. When in CONFIGURED mode, it is an Almost Full Flag output. This pin is active LOW.
23	20	$\overline{XO}/\overline{HF}/\overline{FE}$	Output	Expansion Out/Half Full/Full/Empty: This pin's function is determined by its operation mode. When in SINGLE DEVICE mode, this pin is either HF Flag or a Full/Empty Flag, depending on the state of the most significant bit of Almost Full Flag Register. The pin is an $\overline{XO}$ output when the part is in DEPTH EXPANSION mode. This pin defaults to $\overline{XO}/\overline{HF}$ in NONCONFIGURED mode.
10, 11, 13, 14 19, 20, 21, 22,15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	I/O	Data Output: These pins may be used for data retrieval. The pins become inputs during register loading with DIR input HIGH. The outputs are disabled (High-Z) during device idle ($\overline{R}$ = HIGH).
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	GND	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9007 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For multiple function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing half-full flags, the $\overline{XO}/\overline{HF}/\overline{F\,E}$ pin will be shown as $(\overline{XO})/\overline{HF}/(\overline{F\,E})$.*

RESET

After Vcc is stable, Reset ($\overline{RS}$) must be taken LOW with both $\overline{R}$ and $\overline{W}$ HIGH to initialize the read and write pointers and flags. This also clears all internal registers. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is tied LOW. If $\overline{XI}$ is connected to $\overline{XO}/(\overline{HF})$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW and the FIFO is not full. The WRITE cycle is initiated by the falling edge of $\overline{W}$. Data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While the $\overline{FF}$ is asserted, all writes are inhibited and previously stored data are unaffected. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and FIFO is not empty ($\overline{EF}$ is High). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$. Valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While the $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is full and a READ is initiated, the $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the expanded mode, the last location read from a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9007 allows the receiving device to request that data just read from the FIFO be repeated, when less than 512 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}$/(DIR) pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may start reading the data from the beginning of the FIFO ^tRTR after $(\overline{FL})/\overline{RT}$/(DIR) is taken HIGH. Some or all flags may be affected depending on the location of the read and write pointers before and after the retransmit.

DATA FLOW-THROUGH

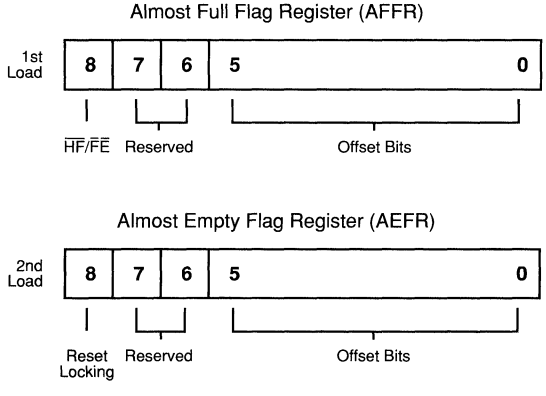
Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a flow-through READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{W}$, and access time is measured from the rising edge of the empty flag.

REGISTER LOAD MODE

This mode of operation is used to reset the device and program the internal flag registers. This yields an almost full and an almost empty flag (DIP package pins 8 and 21 respectively) and a half-full or $\overline{F}/\overline{E}$ flag (DIP package pin 20).

Two 9-bit internal registers have been provided for flag configuration. One is the almost full flag register (AFFR) and the other is the almost empty flag register (AEFR). Bit configurations of the two registers are shown below.

REGISTER SET FOR MT52C9007



Note that bits 0-5 are used for offset setting. The offset value ranges from 1 to 63 words. Each offset value corresponds to a 2-byte increment. This provides a maximum offset of 126 bytes.

Bits 6 and 7 are reserved for future offset expansion. Bit 8 of the AFFR is used for configuration of $\overline{HF}/\overline{F}\,\overline{E}$ pin. When this bit is set LOW, the $HF/\overline{F}\,\overline{E}$ pin is configured as an $\overline{HF}$ flag output. When it is set high, the $HF/\overline{F}\,\overline{E}$ is configured as an $\overline{F}/\overline{E}$ flag output.

Bit 8 of the AEFR is used for reset locking. When this bit is set LOW, subsequent device RESET or REGISTER LOADING cycles reset the device. When the bit is programmed HIGH, subsequent RESET cycles are ignored. In this mode, the flag registers may be reconfigured without device reset. The part may be reset by cycling power to the device or by writing zero (0) into bit 8 of the AEFR register followed by a DEVICE RESET or REGISTER LOAD.

Flag registers are loaded by bringing $\overline{RS}$ LOW followed by the $\overline{R}$ input. The $\overline{R}$ pin should be brought LOW ^{t}RS after the $\overline{RS}$ becomes LOW. The registers may be loaded via the input pins or the output pins depending on the status of the DIR control input. Data is latched into the registers at the rising edge of the $\overline{W}$ control pin. The first WRITE loads the AFFR while the second WRITE loads the AEFR. This loading order is fixed.

BIDIRECTIONAL MODE

Applications requiring data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by using two MT52C9007s. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion may be used in this mode.

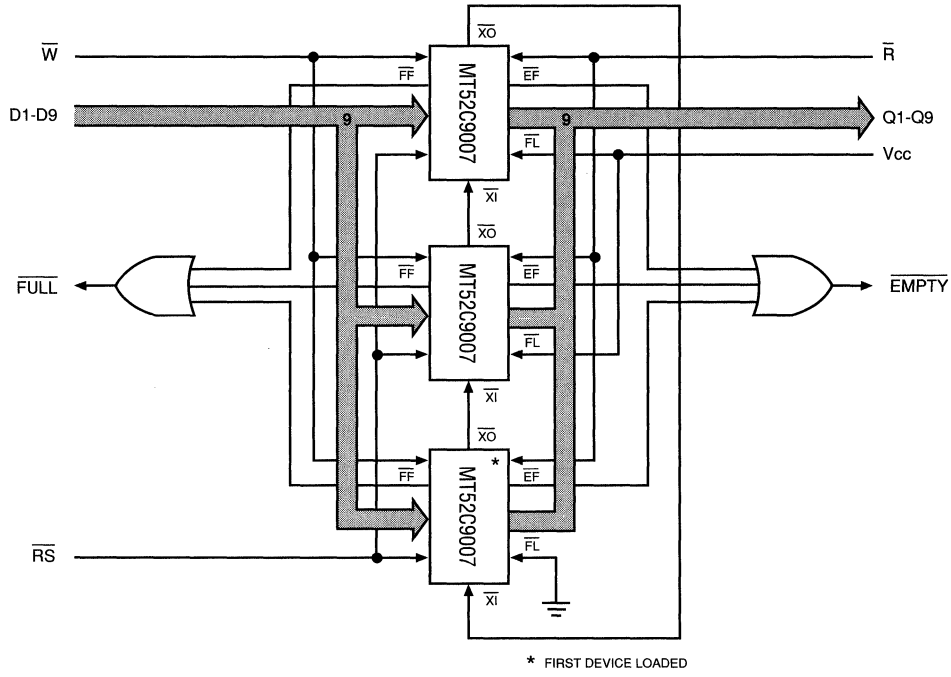
FLAG TIMING

A total of three flag outputs are provided in either CONFIGURED or NONCONFIGURED mode. In the NONCONFIGURED mode, the three flags are $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$. The $\overline{HF}$ flag goes active when more than half the FIFO is full. The flag goes inactive when the FIFO is half full or less.

The full and empty flags are asserted when the last byte is written to or read out of the FIFO, respectively. They are deasserted when the first byte is loaded into an empty FIFO or read out of a full FIFO, respectively. All three flag outputs are active LOW.

When the device is programmed, the $\overline{AFF}$ and $\overline{AEF}$ go active after a READ/WRITE cycle initiation of the location corresponding to the programmed offset value. For example, if the AEFR is programmed with a 10-byte offset (loading a Hex value of 05), the $\overline{AEF}$ flag goes active while reading the 10th location before the FIFO is empty. The flag goes inactive when there are 10 or more bytes left in the FIFO. The assertion timing and deassertion timing of the $\overline{AFF}$ are the same.

The third flag in the PROGRAM mode is either $\overline{HF}$ or $\overline{F}/\overline{E}$ flag depending on the state of the highest bit of the AFFR. If the device is programmed for $\overline{HF}$ flag, it functions like the $\overline{HF}$ flag in NONPROGRAMMED mode. If the device is configured for $\overline{F}/\overline{E}$ flag, the pin will be active (LOW) when the FIFO is either empty or full. The condition of the FIFO is determined by the state of $\overline{F}/\overline{E}$ together with states of $\overline{AFF}$ and $\overline{AEF}$ (example: if $\overline{F}/\overline{E}$ is LOW and $\overline{AFF}$ is LOW but $\overline{AEF}$ is HIGH, the FIFO is full).



* FIRST DEVICE LOADED

Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9007s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) and $\overline{FL}$/($\overline{RT}$/DIR). Figure 1 illustrates a typical three-device expansion. The depth-expansion mode is entered by tying the $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$/DIR) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$/DIR) tied HIGH. Upon a reset, reads and writes to all FIFOs are disabled, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9007. The writes will continue to go to the second device until last location write. Then it will "pass" the write pointer to the third device. The full condition of the entire FIFO array is signaled when all the $\overline{FF}$/($\overline{AFF}$) pins are LOW.

On the last physical READ of the first device, its $\overline{XO}$ ($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. On the last READ, an empty condition is signaled by all of the $\overline{EF}$ pins being LOW. This inhibits further reads. While in the depth-expansion mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1

SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2

DEPTH-EXPANSION/COMPOUND-EXPANSION Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$/DIR= First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -0.5V to +7.0V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	VIH	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-0.5	0.8	V	1, 2

FIFO

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	MIN	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R}$ ≤ VIL; Vcc = MAX f = MAX = 1/ ^{t}RC Outputs Open	ICC		120	115	110	100	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R}$ ≥ VIH; Vcc = MAX f = MAX = 1/ ^{t}RC	ISB1		15	15	15	15	mA	
	$\overline{W}$, $\overline{R}$ ≥ Vcc -0.2; Vcc = MAX VIL ≤ Vss +0.2, VIH ≥ Vcc -0.2; f = 0	ISB2		5	5	5	5	mA	
Input Leakage Current	0V ≤ VIN ≤ Vcc	ILI	-10	10	10	10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ VOUT ≤ Vcc	ILO	-10	10	10	10	10	µA	
Output High Voltage	IOH = -2.0mA	VOH	2.4					V	1
Output Low Voltage	IOL = 8.0mA	VOL					0.4	V	1

CAPACITANCE

(VIN = 0V; VOUT = 0V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz Vcc = 5V	CI		8	pF	4
Output Capacitance		CO		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured and nonconfigured modes) ($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Shift frequency	^tRF		40		33.3		28.5		22.2	MHz	
READ cycle time	^tRC	25		30		35		45		ns	
Access time	^tA		15		20		25		35	ns	6
READ recovery time	^tRR	10		10		10		10		ns	
Read pulse width	^tRPW	15		20		25		35		ns	
Read LOW to Low-Z	^tRLZ	5		5		5		5		ns	7
Read to HIGH to High-Z	^tRHZ		15		15		18		20	ns	7
Data HOLD from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
WRITE Cycle											
WRITE cycle time	^tWC	25		30		35		45		ns	
Write pulse width	^tWPW	15		20		25		35		ns	6
WRITE recovery time	^tWR	10		10		10		10		ns	
Write HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5, 7
Data setup time	^tDS	10		12		15		18		ns	
Data hold time	^tDH	0		0		0		0		ns	
RETRANSMIT Cycle											
Restransmit cycle time	^tRTC	25		30		35		45		ns	
Retransmit pulse width	^tRT	15		20		25		35		ns	
Retransmit recovery time	^tRTR	10		10		10		12		ns	
Retransmit command setup time	^tRTS	15		20		25		35		ns	
RESET Cycle											
RESET cycle time (no register programming)	^tRSC	25		30		35		45		ns	
Reset pulse width	^tRSP	15		20		25		35		ns	6
Reset recovery time	^tRSR	10		10		10		10		ns	
$\overline{RS}$ LOW to $\overline{R}$ LOW	^tRS	15		20		25		35		ns	
Reset and register programming cycle time	^tRSPC	85		100		115		145		ns	
$\overline{R}$ LOW to DIR valid (register load cycle)	^tRDV	5		5		5		5		ns	
$\overline{R}$ LOW to register load	^tRW	10		10		10		10		ns	
$\overline{W}$ HIGH to $\overline{RS}$ LOW	^tWRS	0		0		0		0		ns	
$\overline{R}$ HIGH to $\overline{RS}$ LOW	^tRRS	0		0		0		0		ns	

NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3.0V for pulse width < 20ns.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.
7. Values guaranteed by design, not currently tested.
8. $\overline{R}$ and DIR signals must go inactive (HIGH) coincident with $\overline{RS}$ going inactive (HIGH).
9. DIR must become valid before $\overline{W}$ goes active (LOW).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured mode only) (T_A = 0°C to 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Mode Timing											
$\overline{R}/\overline{W}$ to $\overline{XO}$ LOW	^tXOL		20		20		25		35	ns	
$\overline{R}/\overline{W}$ to $\overline{XO}$ HIGH	^tXOH		20		20		25		35	ns	
$\overline{XI}$ pulse width	^tXIP	15		20		25		35		ns	
$\overline{XI}$ command setup time to $\overline{R}/\overline{W}$	^tXIS	10		12		15		15		ns	
$\overline{XI}$ command recovery time	^tXIR	10		10		10		10		ns	
Flags Timing											
$\overline{W}$ HIGH to Flags Valid	^tWFV		15		15		15		15	ns	
$\overline{RS}$ to $\overline{EF}$ LOW	^tEFL		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{EF}$ LOW	^tREF		20		20		25		35	ns	
$\overline{W}$ HIGH to $\overline{EF}$ HIGH	^tWEF		20		20		25		35	ns	
$\overline{R}$ pulse after $\overline{EF}$ HIGH	^tRPE	15		20		25		35		ns	5
$\overline{RS}$ to $\overline{HF}$, $\overline{FF}$ HIGH	^tHFH, ^tFFH		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{FF}$	^tRFF		15		20		25		30	ns	
$\overline{W}$ LOW to $\overline{FF}$ LOW	^tWFF		20		20		25		35	ns	
$\overline{W}$ pulse width after $\overline{FF}$ HIGH	^tWPF	15		20		25		35		ns	5
$\overline{W}$ LOW to $\overline{HF}$ LOW	^tWHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{HF}$ HIGH	^tRHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{AFF}$	^tRAFF		25		30		35		45	ns	
$\overline{W}$ LOW to $\overline{AFF}$	^tWAFF		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{AEF}$ LOW	^tRAEF		25		30		35		45	ns	
$\overline{W}$ HIGH to $\overline{AEF}$	^tWAEF		25		30		35		45	ns	

FIFO

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

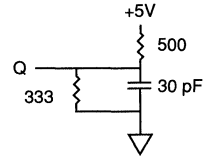
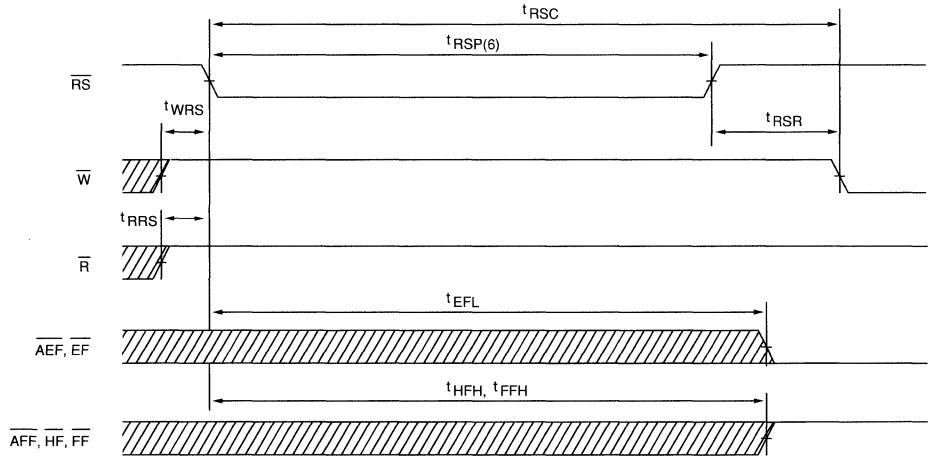
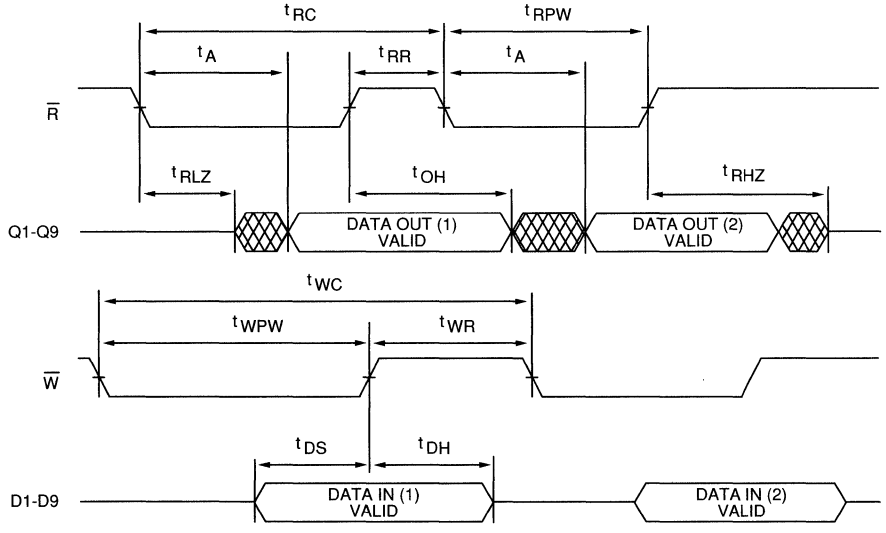


Figure 2
OUTPUT LOAD EQUIVALENT

RESET
(WITH NO REGISTER PROGRAMMING)



ASYNCHRONOUS READ AND WRITE

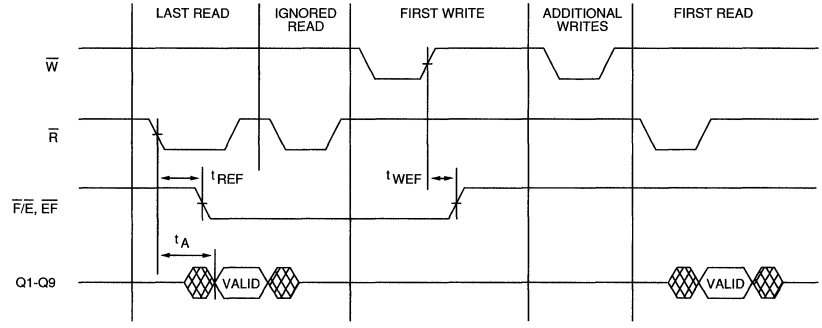


DON'T CARE

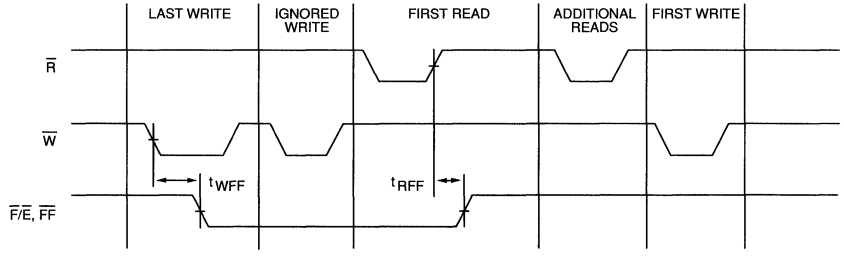
UNDEFINED

FIFO

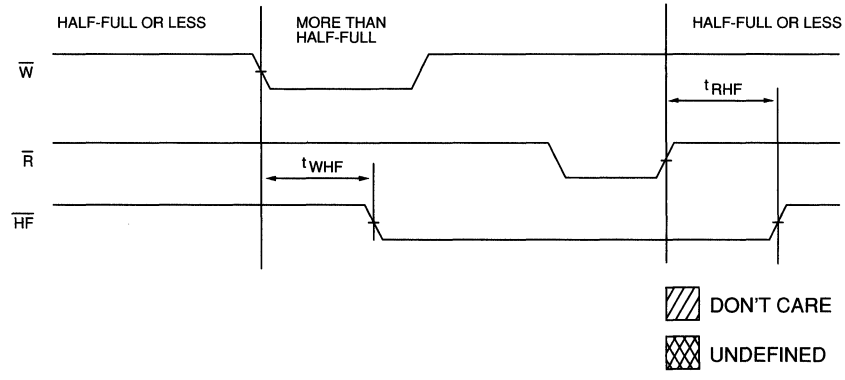
EMPTY FLAG



FULL FLAG

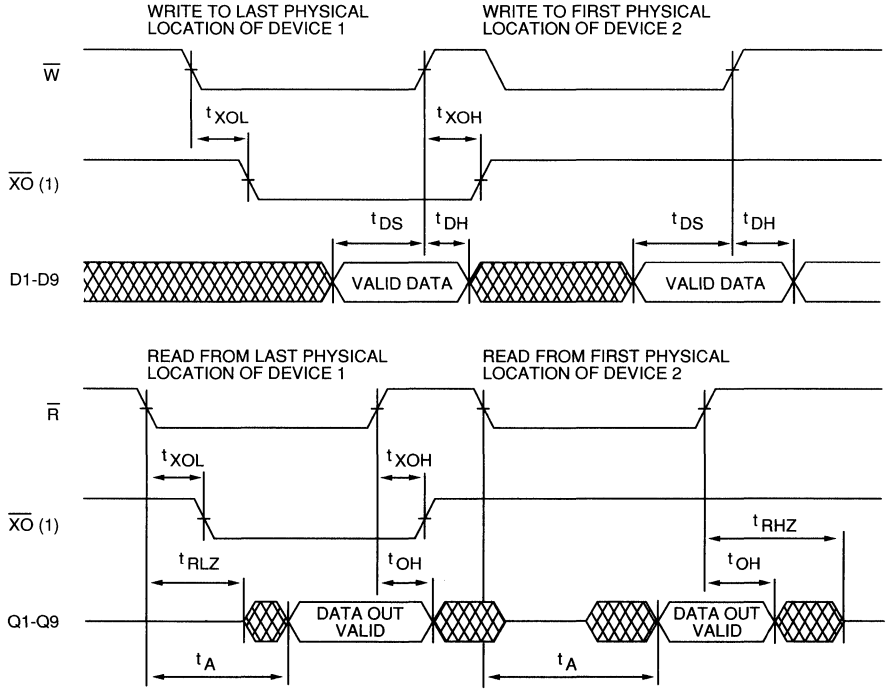


HALF-FULL FLAG
(FOR CONFIGURED AND NONCONFIGURED MODES)



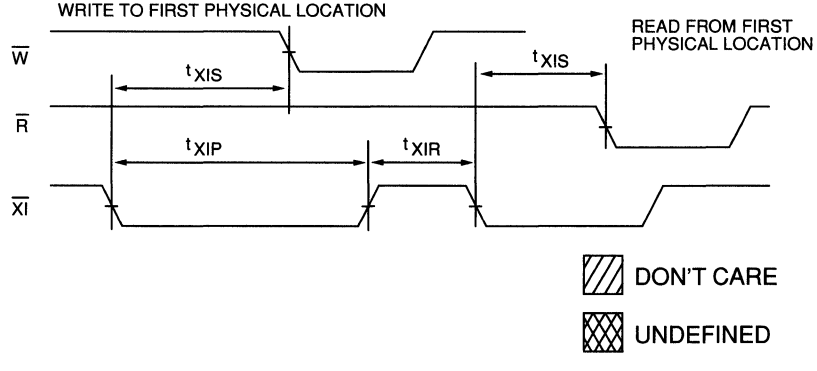
FIFO

EXPANSION MODE ($\overline{XO}$)



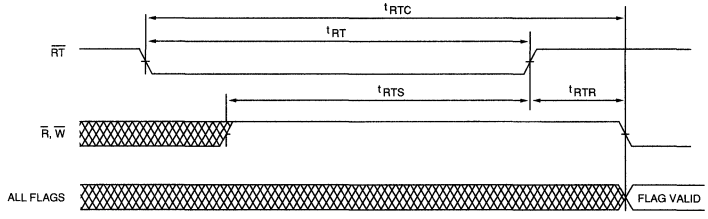
NOTE: 1. $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

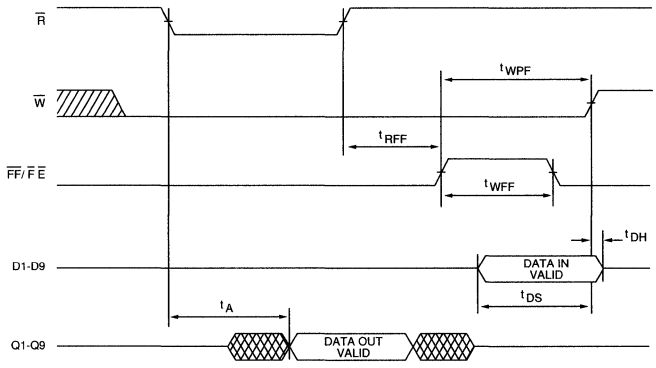


FIFO

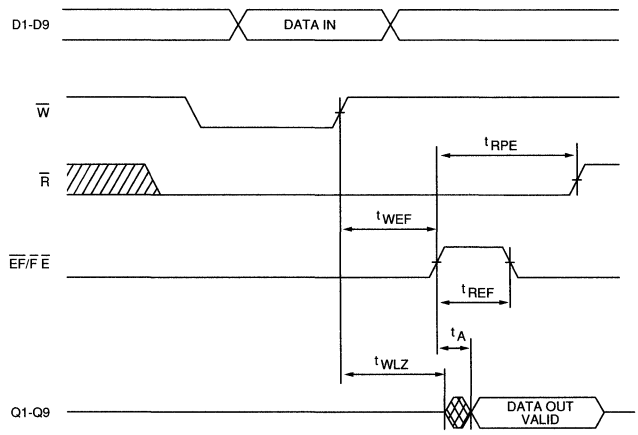
RETRANSMIT



WRITE FLOW-THROUGH

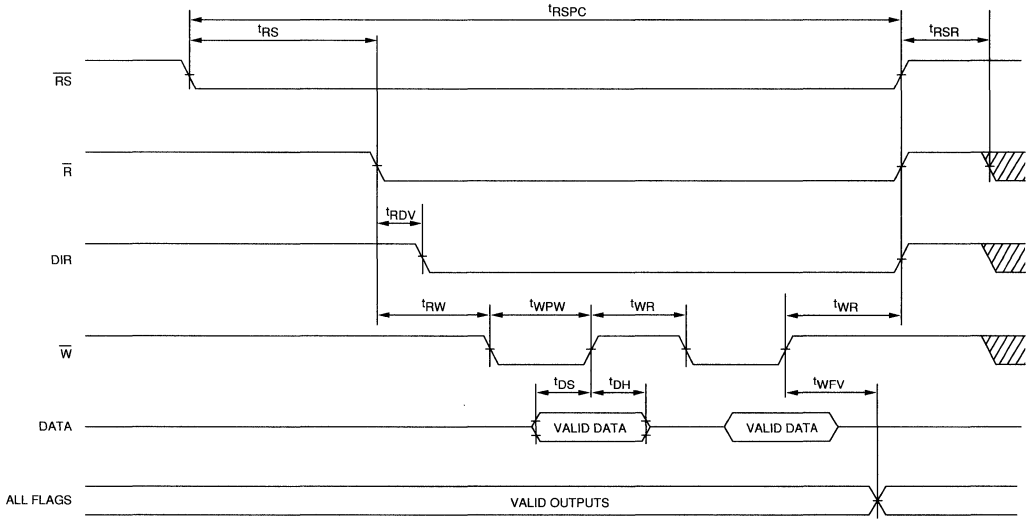


READ FLOW-THROUGH

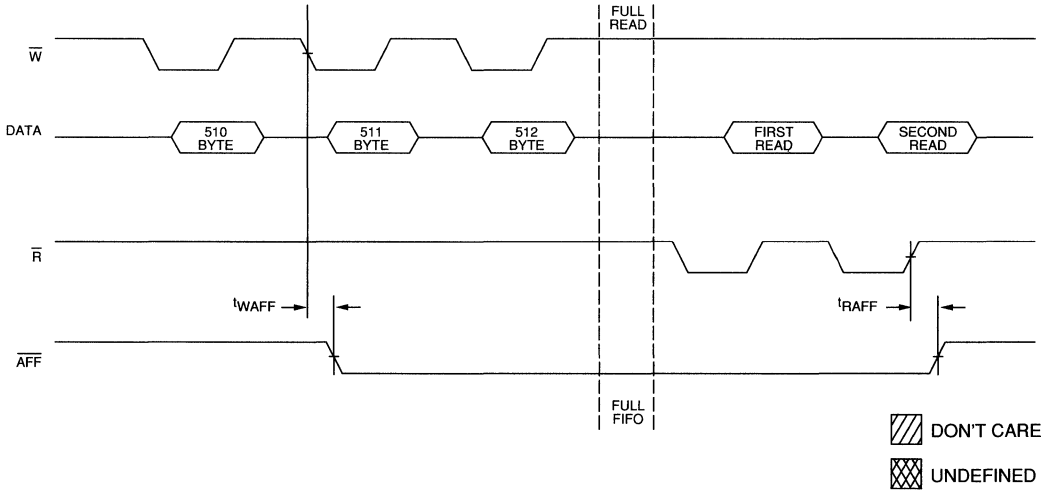


FIFO

RESET/REGISTER PROGRAMMING CYCLE TIME [8, 9]

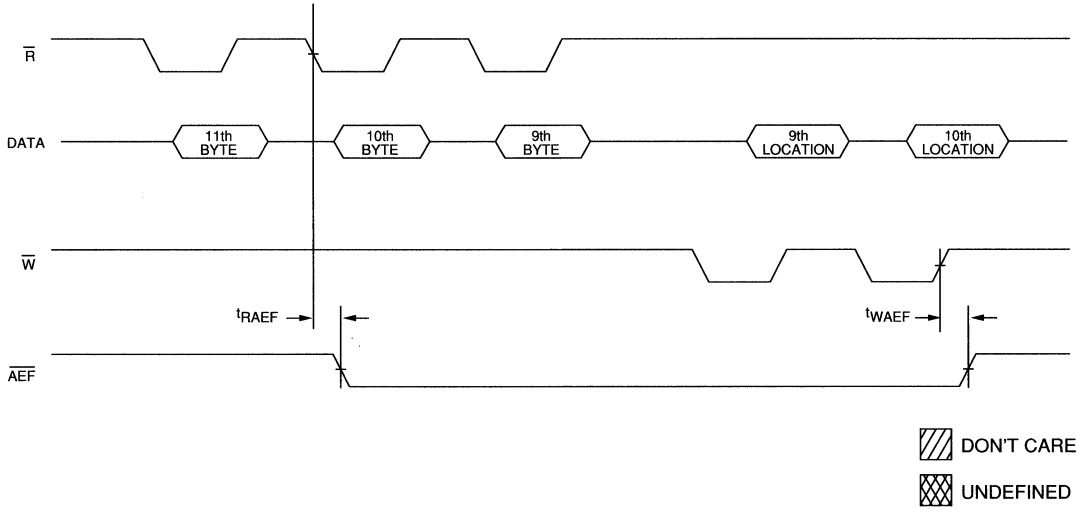


ALMOST FULL FLAG (2-BYTE OFFSET)



FIFO

ALMOST EMPTY FLAG (10-BYTE OFFSET)



FIFO

1K x 9 FIFO

FEATURES

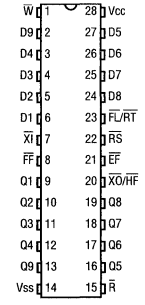
- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Half-Full Flag capability in STAND ALONE mode
- Auto-retransmit capability
- Fully expandable by width and depth
- Pin and function compatible with higher density standard FIFOs

OPTIONS

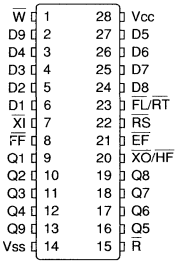
	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Ceramic DIP (600 mil)	C
PLCC	EJ
Ceramic LCC	EC
SOJ (300 mil)	DJ

PIN ASSIGNMENT (Top View)

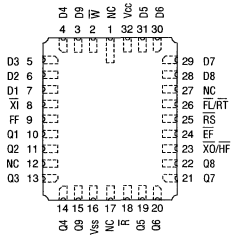
28L DIP (A-9, B-9)



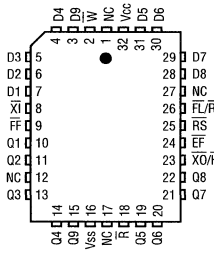
28L SOJ (E-8)



32L LCC (F-4)



32L PLCC (D-2)



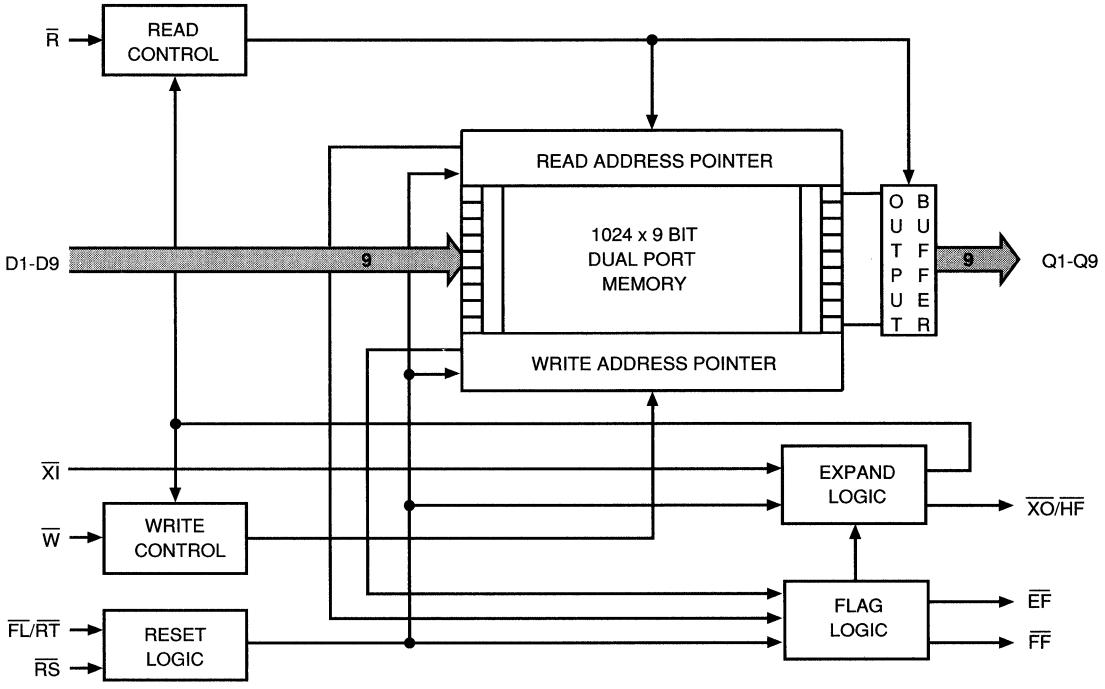
GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual port, six-transistor memory cell with resistor loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain in a high-impedance state. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. Also, the MT52C9010 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with the 2K x 9 FIFO provides a single-chip, depth-expansion solution.

FUNCTIONAL BLOCK DIAGRAM



FIFO

PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1-D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1-Q9).
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$)of the previous device in the daisy chain.
26	23	$\overline{FL/RT}$	Input	First Load: Acts as first load signal in DEPTH EXPANSION mode. $\overline{FL}$ if low, will enable the device as the first to be loaded (enables read and write pointers). $\overline{FL}$ should be tied low for the first FIFO in the chain, tied high for all other FIFOs in the chain Retransmit: Acts as retransmit signal in STAND ALONE mode. $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO/HF}$	Output	Expansion Out: Acts as expansion out pin in DEPTH EXPANSION mode. $\overline{XO}$ will pulse LOW on the last physical WRITE or the last physical read. $\overline{XO}$ should be connected to $\overline{XI}$ of the next FIFO in the daisy chain. Half-Full Flag: Acts as Half Full Flag in STAND ALONE mode. $\overline{HF}$ goes LOW when the FIFO becomes more than half-full; will stay LOW until the FIFO becomes half-full or less.
10, 11, 13, 14, 19, 20, 21, 22, 15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	Output	Data Output: Output or high impedance.
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9010 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing the half-full flags the $\overline{XO}/\overline{HF}$ pin will be shown as $(\overline{XO})/\overline{HF}$.*

RESET

After Vcc is stable, RESET ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is LOW. If $\overline{XI}$ is tied to $\overline{XO}/(\overline{HF})$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the STAND ALONE mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (1024/2 + 1) is written. It will stay asserted until the FIFO becomes half-full or less. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, write to the last location of the FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and the FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^{t}RLZ after the falling edge of $\overline{R}$ and valid data will appear ^{t}A after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is being used in the SINGLE DEVICE mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ LOW) and a read is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9010 allows the receiving device to request that the data read earlier from the FIFO to be repeated, when less than 1024 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^{t}RTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume (useful only in SINGLE mode with no wraparound).

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. FLOW-THROUGH READs are initiated from the rising edge of $\overline{W}$ and access time is measured from the rising edge of $\overline{EF}$.

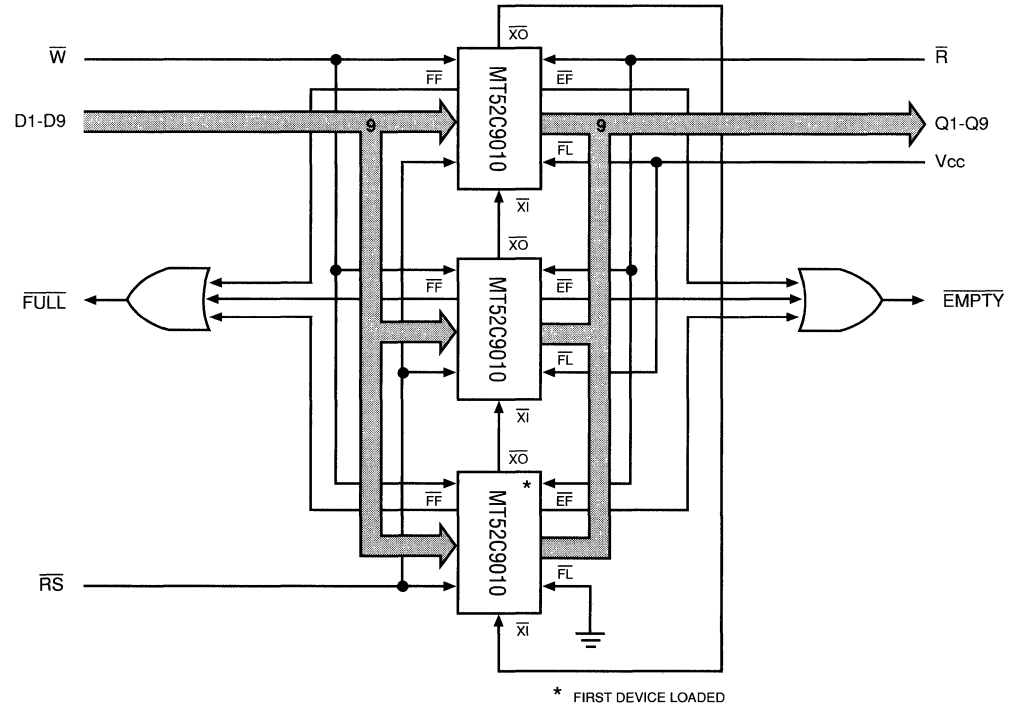


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the stand alone or groups of expanded-depth mode FIFOs. Expanded-width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1) when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9010s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}/(\overline{HF})$ and $\overline{FL}/(\overline{RT})$. Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered during a RESET cycle, by tying the $\overline{XO}/(\overline{HF})$ pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}/(\overline{RT})$ pin grounded. The remaining devices in the chain will have $\overline{FL}/(\overline{RT})$ tied HIGH. During RESET cycle, $\overline{XO}/(\overline{HF})$ of each device is held HIGH, disabling reads and writes to all FIFOs, except the first load device. When the last physical location of the first device is written, the $\overline{XO}/(\overline{HF})$ pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9010. The writes will continue to go to the second device until last location WRITE. Then it will "pass" the write pointer to the third device.

The full condition of the entire FIFO array is signaled by "OR-ing" all the $\overline{FF}$ pins. On the last physical READ of the first device, its $\overline{XO}/(\overline{HF})$ will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. An empty condition is signaled by OR-ing all of the $\overline{EF}$ pins. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$/DIR= First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -0.5V to +7.0V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

FIFO

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}, \overline{R} \le V_{IL}$; V_{CC} = MAX Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$W, \overline{R} \ge V_{IH}$; V_{CC} = MAX	I_{SB1}		15	mA	
	$\overline{W}, \overline{R} \ge V_{CC}$ -0.2; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}		5	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Shift Frequency	Fs		40		33.3		28.5		22.2	MHz	
Access time	tA		15		20		25		35	ns	
Read cycle time	tRC	25		30		35		45		ns	
Read command recovery time	tRR	10		10		10		10		ns	
Read command pulse width	tRPW	15		20		25		35		ns	6
Read LOW to Low-Z	tRLZ	5		5		5		5		ns	
Read to HIGH to High-Z	tRHZ		15		15		18		20	ns	
Data hold from $\overline{R}$ HIGH	tOH	5		5		5		5		ns	
Write cycle time	tWC	25		30		35		45		ns	
Write command pulse width	tWPW	15		20		25		35		ns	6
Write command recovery time	tWR	10		10		10		10		ns	
Write HIGH to Low-Z	tWLZ	5		5		5		5		ns	5
Data setup time	tDS	10		12		15		20		ns	
Data hold time	tDH	0		0		0		0		ns	
Reset cycle time	tRSC	25		30		35		45		ns	
Reset pulse width	tRSP	15		20		25		35		ns	6
Reset recovery time	tRSR	10		10		10		10		ns	
Read HIGH to Reset HIGH	tRRS	15		20		25		35		ns	
Write HIGH to Reset HIGH	tWRS	15		20		25		35		ns	
Retransmit cycle time	tRTC	25		30		35		45		ns	
Retransmit pulse width	tRT	15		20		25		35		ns	
Retransmit recovery time	tRTR	10		10		10		12		ns	
Retransmit setup time	tRTS	15		20		25		35		ns	
Reset to $\overline{EF}$ LOW	tEFL		25		30		35		45	ns	
Reset to $\overline{HF}$ $\overline{FF}$ HIGH	tHFH, tFFH		25		30		35		45	ns	
Read LOW to $\overline{EF}$ LOW	tREF		20		20		25		35	ns	
Read HIGH to $\overline{FF}$ HIGH	tRFF		20		20		25		35	ns	
Write LOW to $\overline{FF}$ LOW	tWFF		20		20		25		35	ns	
Write HIGH to $\overline{EF}$ HIGH	tWEF		20		20		25		35	ns	
Write LOW to $\overline{HF}$ LOW	tWHF		25		30		35		45	ns	
Read HIGH to $\overline{HF}$ HIGH	tRHF		25		30		35		45	ns	
Read pulse after $\overline{EF}$ HIGH	tRPE	15		20		25		35		ns	5
Write pulse width after $\overline{FF}$ HIGH	tWPF	15		20		25		35		ns	5
Read/Write to $\overline{XO}$ LOW	tXOL		20		20		25		35	ns	
Read/Write to $\overline{XO}$ HIGH	tXOH		20		20		25		35	ns	
$\overline{XI}$ pulse width	tXIP	15		20		25		35		ns	
$\overline{XI}$ setup Time	tXIS	10		12		15		15		ns	
$\overline{XI}$ recovery time	tXIR	10		10		10		10		ns	

FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Flow-through mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

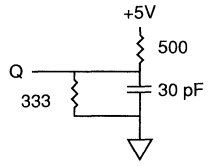
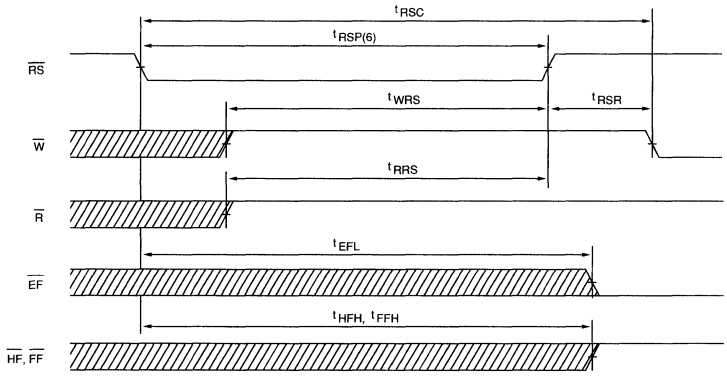
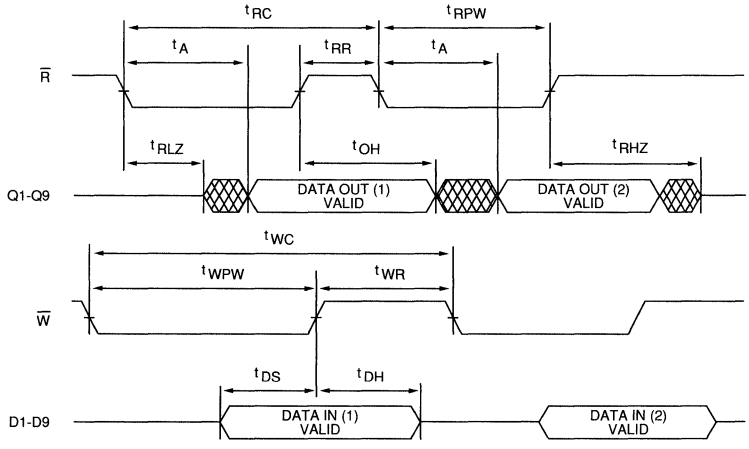


Fig. 2
OUTPUT LOAD EQUIVALENT

RESET



ASYNCHRONOUS READ AND WRITE

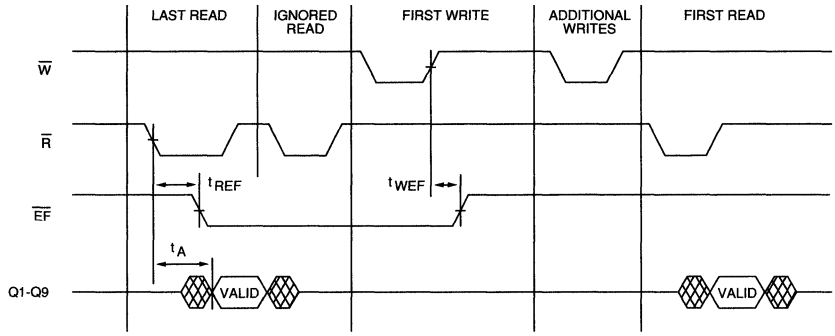


DON'T CARE

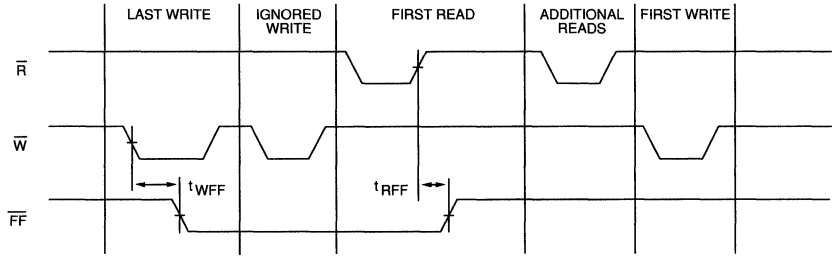
UNDEFINED

FIFO

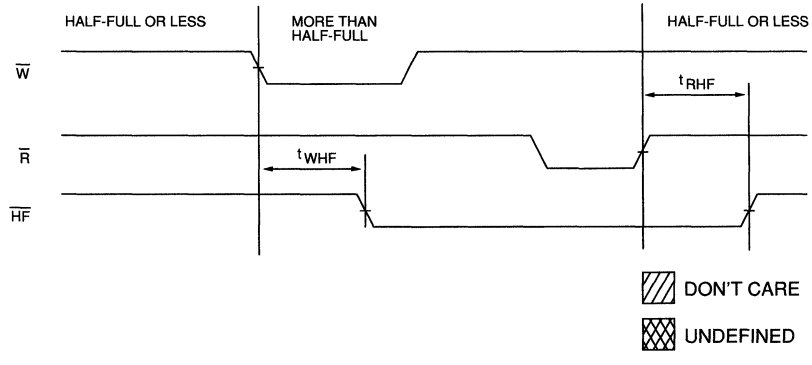
EMPTY FLAG



FULL FLAG

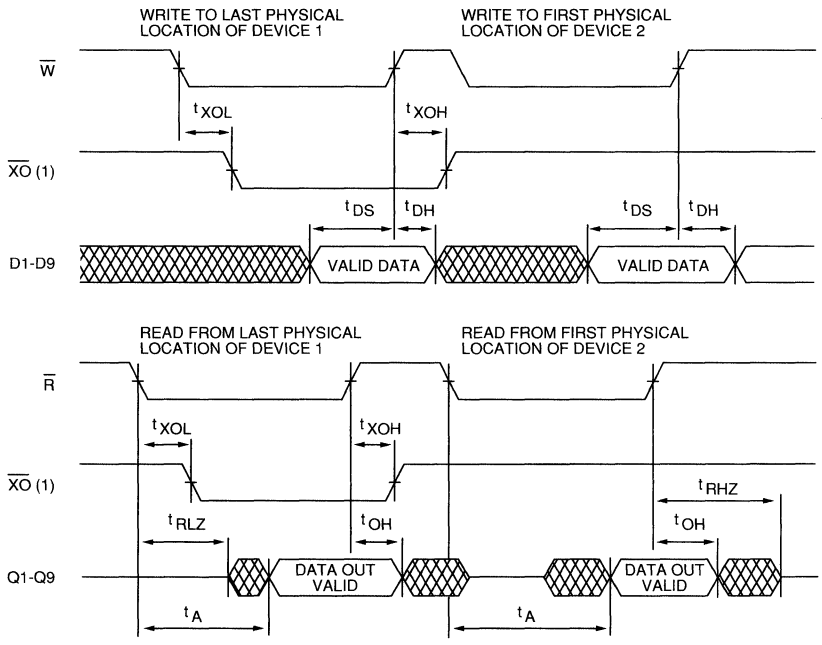


HALF-FULL FLAG



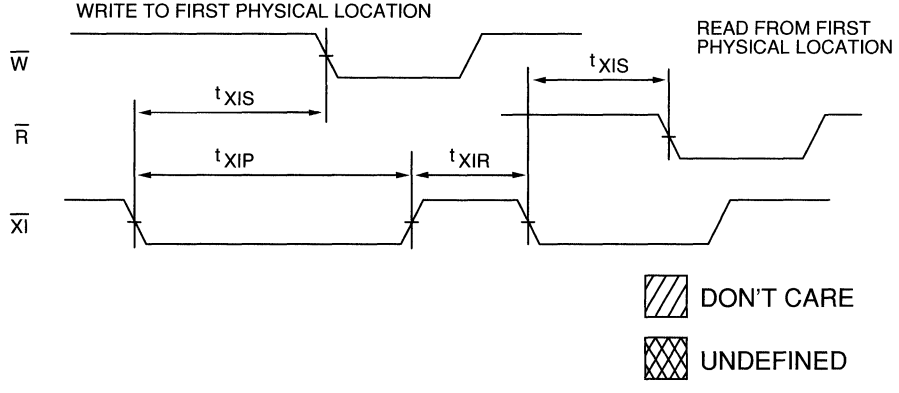
FIFO

EXPANSION MODE ($\overline{XO}$)



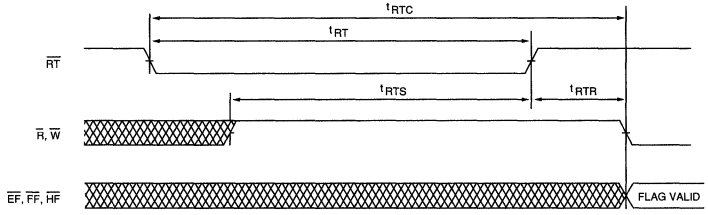
NOTE: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

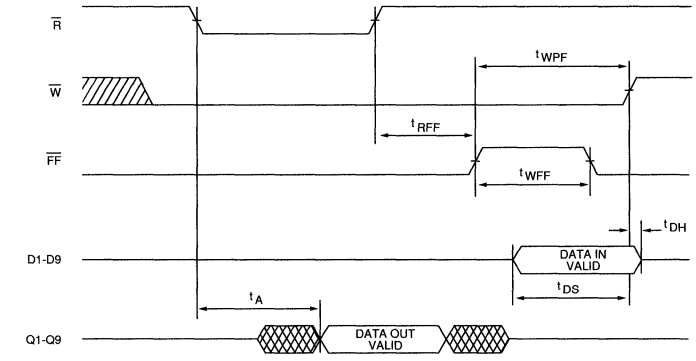


FIFO

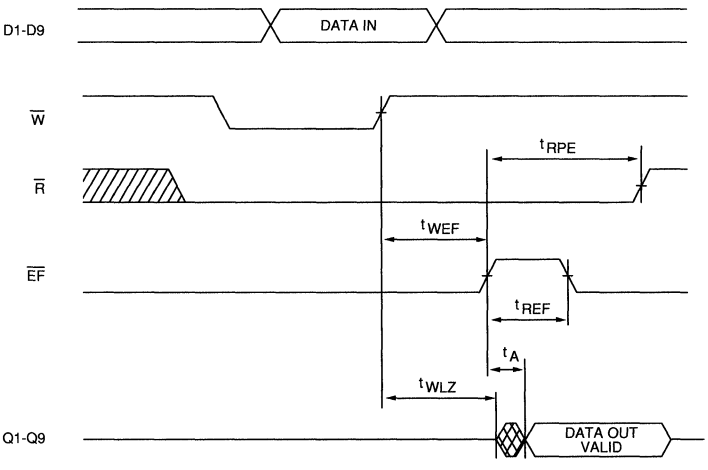
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



DON'T CARE

UNDEFINED

FIFO

FIFO

1K x 9 FIFO

WITH PROGRAMMABLE FLAGS

FEATURES

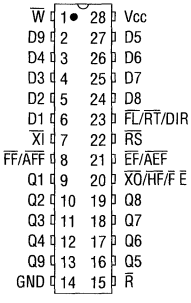
- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typical (standby); 350mW typical (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Two fully configurable Almost Full and Almost Empty Flags
- Programmable Half Full Flag or Full/Empty Flag option eliminates external counter requirement
- Register loading via the input or output pins
- Auto-retransmit capability in single-device mode
- Fully expandable by width and depth
- Pin and function compatible with standard FIFOs

OPTIONS

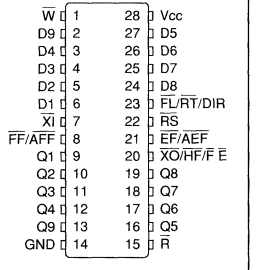
	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Ceramic DIP (600 mil)	C
PLCC	EJ
Ceramic LCC	EC
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

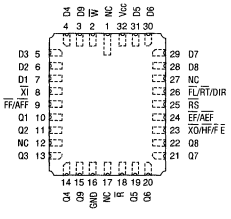
28L/DIP
(A-9, B-9)



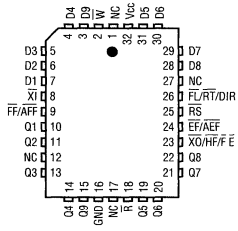
28L/SOJ
(E-8)



32L/LCC
(F-4)



32L/PLCC
(D-2)



GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

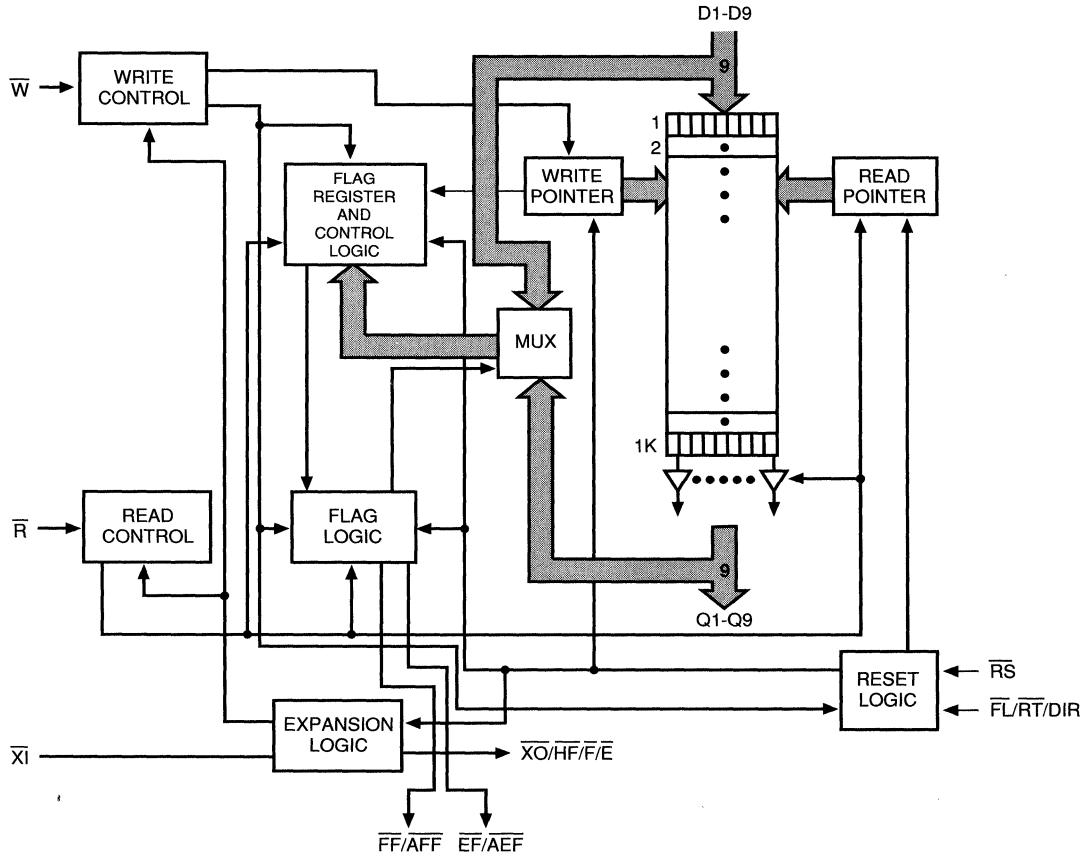
These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates.

When not configured, the MT52C9012 defaults to a standard FIFO with empty ($\overline{EF}$), full ($\overline{FF}$) and half-full ($\overline{HF}$) flag pins. The MT52C9012 can be configured for programmable flags by loading the internal flag registers (as described under "Register Load Mode" on page 8-45). In CONFIGURED mode, up to three flags are provided. The first two are the almost empty flag ($\overline{AEF}$) and the almost full flag ($\overline{AFF}$) with independently programmable offsets. The third one is either an $\overline{HF}$ or a full and empty ($\overline{F\,E}$) flag, depending on the bit configuration of the registers. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the stand-alone mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. Also, the MT52C9012 is speed, function and pin compatible with higher and lower density FIFOs from Micron. This upward compatibility with 2K FIFOs provides a single-chip depth-expansion solution.

FIFO

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: This pin is used to reset the device and load internal flag registers. During device reset, all internal pointers and registers are cleared.
2	1	$\overline{W}$	Input	Write: A LOW on this pin loads data into the device. The internal write pointer is incremented after the rising edge of the write input.
18	15	$\overline{R}$	Input	Read: A LOW on this pin puts the oldest valid data byte in the memory array on the output bus. The internal read pointer is incremented at the rising edge of the read signal. Outputs are High-Z when this pin is HIGH.
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$) of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$/DIR	Input	First Load/Retransmit/Direction: When in single-device mode, this pin can be used to initiate a reread of the previously read data. When in REGISTER LOAD mode, the pin is used for register loading direction. When it is LOW, registers are loaded through the data output pins. When it is HIGH, registers are loaded through the data input pins. In DEPTH EXPANSION mode, this pin should be tied LOW if the device is the first one in the chain and tied HIGH if it is not the first one.
7, 6, 5, 4, 31, 30 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs: Data on these lines are stored in the memory array or flag registers during array WRITE or register programming, respectively.
24	21	$\overline{EF}/\overline{AEF}$	Output	Empty Flag/Almost Empty Flag: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is an Empty Flag output. When in CONFIGURED mode, it is an Almost Empty Flag output. This pin is active LOW.
9	8	$\overline{FF}/\overline{AFF}$	Output	Full Flag/Almost Full Flags: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is a Full Flag output. When in CONFIGURED mode, it is an Almost Full Flag output. This pin is active LOW.
23	20	$\overline{XO}/\overline{HF}/\overline{FE}$	Output	Expansion Out/Half Full/Full/Empty: This pin's function is determined by its operation mode. When in SINGLE DEVICE mode, this pin is either HF Flag or a Full/Empty Flag, depending on the state of the most significant bit of Almost Full Flag Register. The pin is an $\overline{XO}$ output when the part is in DEPTH EXPANSION mode. This pin defaults to $\overline{XO}/\overline{HF}$ in NONCONFIGURED mode.
10, 11, 13, 14 19, 20, 21, 22,15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	I/O	Data Output: These pins may be used for data retrieval. The pins become inputs during register loading with DIR input HIGH. The outputs are disabled (High-Z) during device idle ($\overline{R}$ = HIGH).
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	GND	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9012 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For multiple function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing half-full flags, the $\overline{XO}/\overline{HF}/\overline{F\ E}$ pin will be shown as $(\overline{XO})/\overline{HF}/(\overline{F\ E})$.*

RESET

After Vcc is stable, Reset ($\overline{RS}$) must be taken LOW with both $\overline{R}$ and $\overline{W}$ HIGH to initialize the read and write pointers and flags. This also clears all internal registers. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is tied LOW. If $\overline{XI}$ is connected to $\overline{XO}/(\overline{HF})$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW and if the FIFO is not full. The WRITE cycle is initiated by the falling edge of $\overline{W}$. Data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is asserted, all writes are inhibited and previously stored data are unaffected. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$. Valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is full and a READ is initiated, the $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the expanded mode, the last location read from a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9012 allows the receiving device to request that data just read from the FIFO be repeated, when less than 1024 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}/(DIR)$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may start reading the data from the beginning of the FIFO ^tRTR after $(\overline{FL})/\overline{RT}/(DIR)$ is taken HIGH. Some or all flags may be affected depending on the location of the read and write pointers before and after the retransmit.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{W}$, and access time is measured from the rising edge of the empty flag.

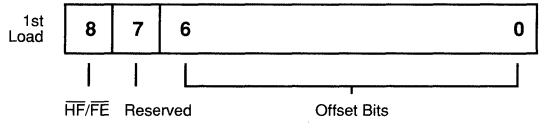
REGISTER LOAD MODE

This mode of operation is used to reset the device and program the internal flag registers. This yields an almost full and an almost empty flag (DIP package pins 8 and 21 respectively) and a half-full or $\overline{F}/\overline{E}$ flag (DIP package pin 20).

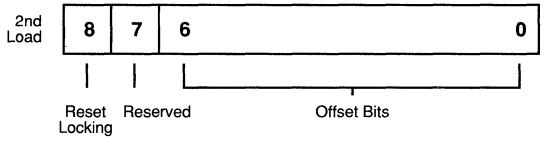
Two 9-bit internal registers have been provided for flag configuration. One is the almost full flag register (AFFR) and the other is the almost empty flag register (AEFR). Bit configurations of the two registers are shown below.

REGISTER SET FOR MT52C9012

Almost Full Flag Register (AFFR)



Almost Empty Flag Register (AEFR)



Note that bits 0-6 are used for offset setting. The offset value ranges from 1 to 127 words. Each offset value corresponds to a 2-byte increment. This provides a maximum offset of 254 bytes.

Bits 6 and 7 are reserved for future offset expansion. Bit 8 of the AFFR is used for configuration of $\overline{HF}/\overline{F}\,\overline{E}$ pin. When this bit is set LOW, the $HF/\overline{F}\,\overline{E}$ pin is configured as an $\overline{HF}$ flag output. When it is set high, the $HF/\overline{F}\,\overline{E}$ is configured as an $\overline{F}/\overline{E}$ flag output.

Bit 8 of the AEFR is used for reset locking. When this bit is set LOW, subsequent device RESET or REGISTER LOADING cycles reset the device. When the bit is programmed HIGH, subsequent RESET cycles are ignored. In this mode, the flag registers can be reconfigured without device reset. The part can be reset by cycling power to the device or by writing zero (0) into bit 8 of the AEFR register followed by a DEVICE RESET or REGISTER LOAD.

Flag registers are loaded by bringing $\overline{RS}$ LOW followed by the $\overline{R}$ input. The $\overline{R}$ pin should be brought LOW ^{t}RS after the $\overline{RS}$ becomes LOW. The registers may be loaded via the input pins or the output pins depending on the status of the DIR control input. Data is latched into the registers at the rising edge of the $\overline{W}$ control pin. The first WRITE loads the AFFR while the second WRITE loads the AEFR. This loading order is fixed.

BIDIRECTIONAL MODE

Applications requiring data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by using two MT52C9012s. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion may be used in this mode.

FLAG TIMING

A total of three flag outputs are provided in either CONFIGURED or NONCONFIGURED mode. In the NONCONFIGURED mode, the three flags are $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$. The $\overline{HF}$ flag goes active when more than half the FIFO is full. The flag goes inactive when the FIFO is half full or less.

The full and empty flags are asserted when the last byte is written to or read out of the FIFO, respectively. They are deasserted when the first byte is loaded into an empty FIFO or read out of a full FIFO, respectively. All three flag outputs are active LOW.

When the device is programmed, the $\overline{AFF}$ and $\overline{AEF}$ go active after a READ/WRITE cycle initiation of the location corresponding to the programmed offset value. For example, if the AEFR is programmed with a 10-byte offset (loading a Hex value of 05), the $\overline{AEF}$ flag goes active while reading the 10th location before the FIFO is empty. The flag goes inactive when there are 10 or more bytes left in the FIFO. The assertion timing and deassertion timing of the $\overline{AFF}$ are the same.

The third flag in the PROGRAM mode is either $\overline{HF}$ or $\overline{F}/\overline{E}$ flag depending on the state of the highest bit of the AFFR. If the device is programmed for $\overline{HF}$ flag, it functions like the $\overline{HF}$ flag in NONPROGRAMMED mode. If the device is configured for $\overline{F}/\overline{E}$ flag, the pin will be active (LOW) when the FIFO is either empty or full. The condition of the FIFO is determined by the state of $\overline{F}/\overline{E}$ together with states of $\overline{AFF}$ and $\overline{AEF}$ (example: if $\overline{F}/\overline{E}$ is LOW and $\overline{AFF}$ is LOW but $\overline{AEF}$ is HIGH, the FIFO is full).

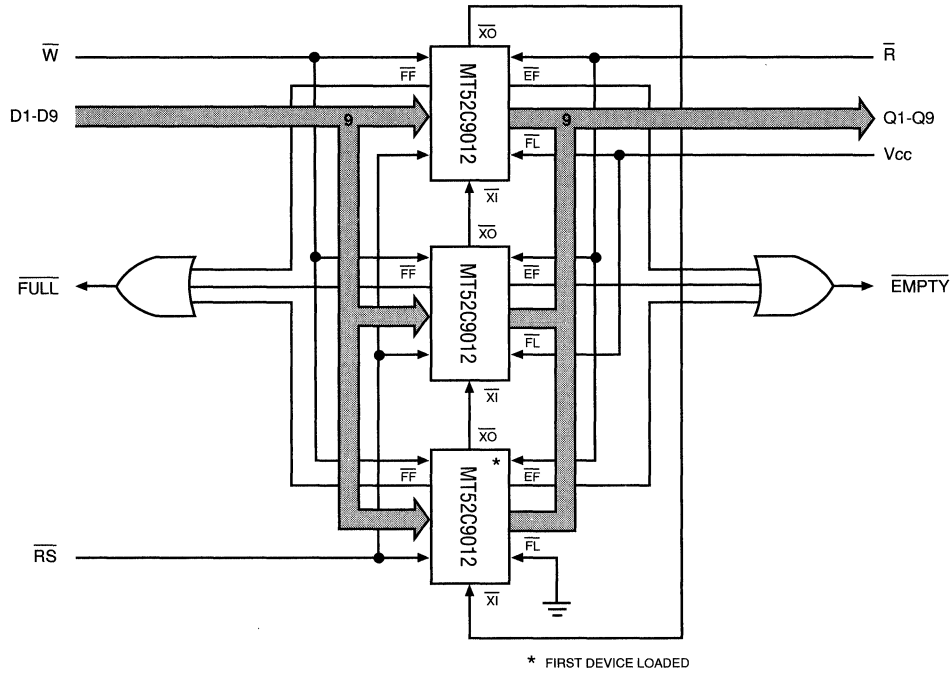


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9012s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$/$\overline{F}$ $\overline{E}$) and $\overline{FL}$/($\overline{RT}$/DIR). Figure 1 illustrates a typical three-device expansion. The depth-expansion mode is entered by tying the $\overline{XO}$/($\overline{HF}$/$\overline{F}$ $\overline{E}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$/DIR) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$/DIR) tied HIGH. Upon a reset, reads and writes to all FIFOs are disabled, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9012. The writes will continue to go to the second device until last location write. Then it will "pass" the write pointer to the third device. The full condition of the entire FIFO array is signaled when all the $\overline{FF}$/($\overline{AFF}$) pins are LOW.

On the last physical READ of the first device, its $\overline{XO}$ ($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. On the last READ, an empty condition is signaled by all of the $\overline{EF}$ pins being LOW. This inhibits further reads. While in the depth-expansion mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1

SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2

DEPTH-EXPANSION/COMPOUND-EXPANSION Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$/DIR= First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -0.5V to +7.0V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

FIFO

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	MIN	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}, \overline{R} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}		120	115	110	100	mA	3
Power Supply Current: Standby	$\overline{W}, \overline{R} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC	I_{SB1}		15	15	15	15	mA	
	$\overline{W}, \overline{R} \ge V_{CC}$ -0.2; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}		5	5	5	5	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	10	10	10	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	10	10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4					V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}					0.4	V	1

CAPACITANCE

($V_{IN} = 0V$; $V_{OUT} = 0V$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured and nonconfigured modes) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Shift frequency	^tRF		40		33.3		28.5		22.2	MHz	
READ cycle time	^tRC	25		30		35		45		ns	
Access time	^tA		15		20		25		35	ns	6
READ recovery time	^tRR	10		10		10		10		ns	
Read pulse width	^tRPW	15		20		25		35		ns	
Read LOW to Low-Z	^tRLZ	5		5		5		5		ns	7
Read to HIGH to High-Z	^tRHZ		15		15		18		20	ns	7
Data HOLD from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
WRITE Cycle											
WRITE cycle time	^tWC	25		30		35		45		ns	
Write pulse width	^tWPW	15		20		25		35		ns	6
WRITE recovery time	^tWR	10		10		10		10		ns	
Write HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5, 7
Data setup time	^tDS	10		12		15		18		ns	
Data hold time	^tDH	0		0		0		0		ns	
RETRANSMIT Cycle											
Restransmit cycle time	^tRTC	25		30		35		45		ns	
Retransmit pulse width	^tRT	15		20		25		35		ns	
Retransmit recovery time	^tRTR	10		10		10		12		ns	
Retransmit command setup time	^tRTS	15		20		25		35		ns	
RESET Cycle											
RESET cycle time (no register programming)	^tRSC	25		30		35		45		ns	
Reset pulse width	^tRSP	15		20		25		35		ns	6
Reset recovery time	^tRSR	10		10		10		10		ns	
$\overline{RS}$ LOW to $\overline{R}$ LOW	^tRS	15		20		25		35		ns	
Reset and register programming cycle time	^tRSPC	85		100		115		145		ns	
$\overline{R}$ LOW to DIR valid (register load cycle)	^tRDV	5		5		5		5		ns	
$\overline{R}$ LOW to register load	^tRW	10		10		10		10		ns	
$\overline{W}$ HIGH to $\overline{RS}$ LOW	^tWRS	0		0		0		0		ns	
$\overline{R}$ HIGH to $\overline{RS}$ LOW	^tRRS	0		0		0		0		ns	

FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.
7. Values guaranteed by design, not currently tested.
8. $\overline{R}$ and DIR signals must go inactive (HIGH) coincident with $\overline{RS}$ going inactive (HIGH).
9. DIR must become valid before $\overline{W}$ goes active (LOW).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured mode only) (T_A = 0°C to 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Mode Timing											
$\overline{R}/\overline{W}$ to $\overline{XO}$ LOW	tXOL		20		20		25		35	ns	
$\overline{R}/\overline{W}$ to $\overline{XO}$ HIGH	tXOH		20		20		25		35	ns	
$\overline{XI}$ pulse width	tXIP	15		20		25		35		ns	
$\overline{XI}$ command setup time to $\overline{R}/\overline{W}$	tXIS	10		12		15		15		ns	
$\overline{XI}$ command recovery time	tXIR	10		10		10		10		ns	
Flags Timing											
$\overline{W}$ HIGH to Flags Valid	tWFV		15		15		15		15	ns	
$\overline{RS}$ to $\overline{EF}$ LOW	tEFL		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{EF}$ LOW	tREF		20		20		25		35	ns	
$\overline{W}$ HIGH to $\overline{EF}$ HIGH	tWEF		20		20		25		35	ns	
$\overline{R}$ pulse after $\overline{EF}$ HIGH	tRPE	15		20		25		35		ns	5
$\overline{RS}$ to $\overline{HF}$, $\overline{FF}$ HIGH	tHFH, tFFH		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{FF}$	tRFF		15		20		25		30	ns	
$\overline{W}$ LOW to $\overline{FF}$ LOW	tWFF		20		20		25		35	ns	
$\overline{W}$ pulse width after $\overline{FF}$ HIGH	tWPF	15		20		25		35		ns	5
$\overline{W}$ LOW to $\overline{HF}$ LOW	tWHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{HF}$ HIGH	tRHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{AFF}$	tRAFF		25		30		35		45	ns	
$\overline{W}$ LOW to $\overline{AFF}$	tWAFF		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{AEF}$ LOW	tRAEF		25		30		35		45	ns	
$\overline{W}$ HIGH to $\overline{AEF}$	tWAEF		25		30		35		45	ns	

FIFO

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

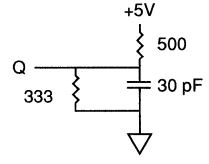
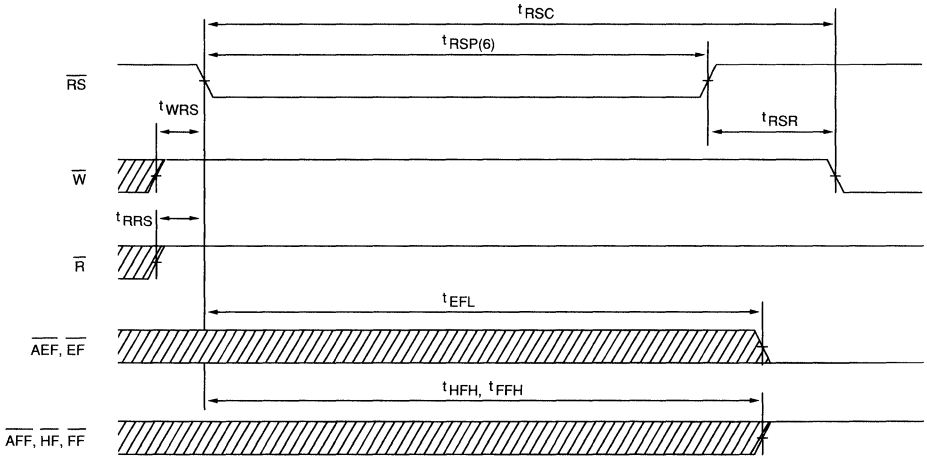
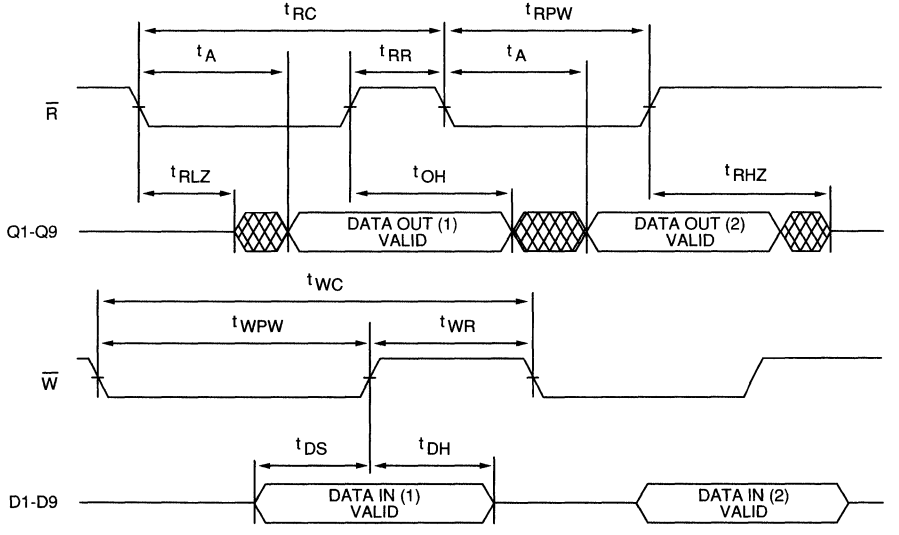


Figure 2
OUTPUT LOAD EQUIVALENT

RESET
(WITH NO REGISTER PROGRAMMING)

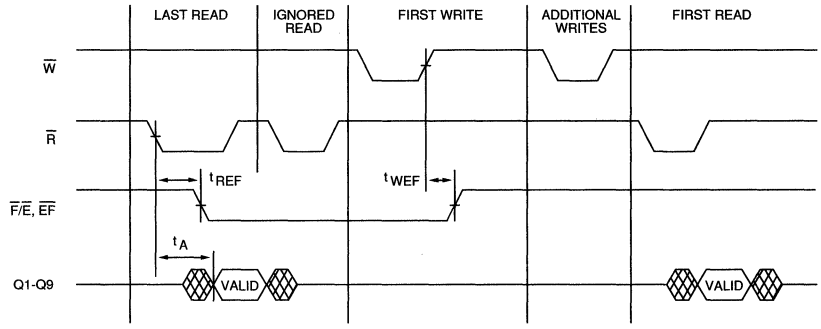


ASYNCHRONOUS READ AND WRITE

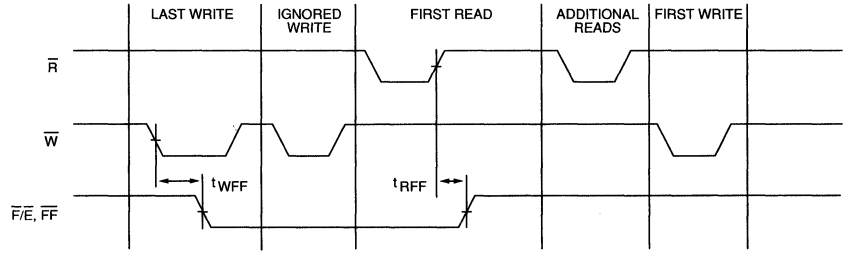


FIFO

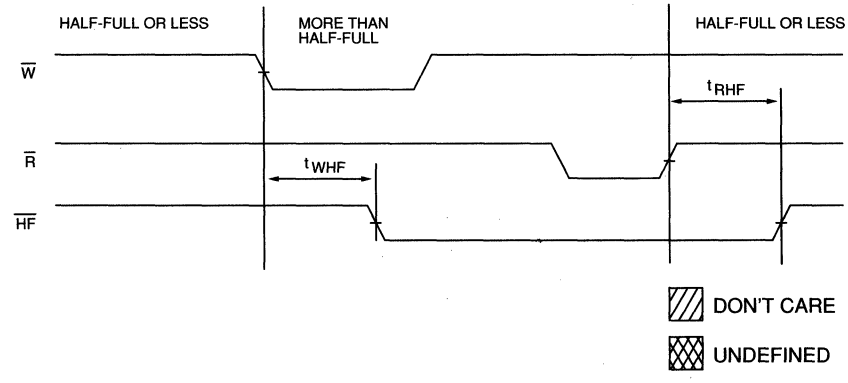
EMPTY FLAG



FULL FLAG

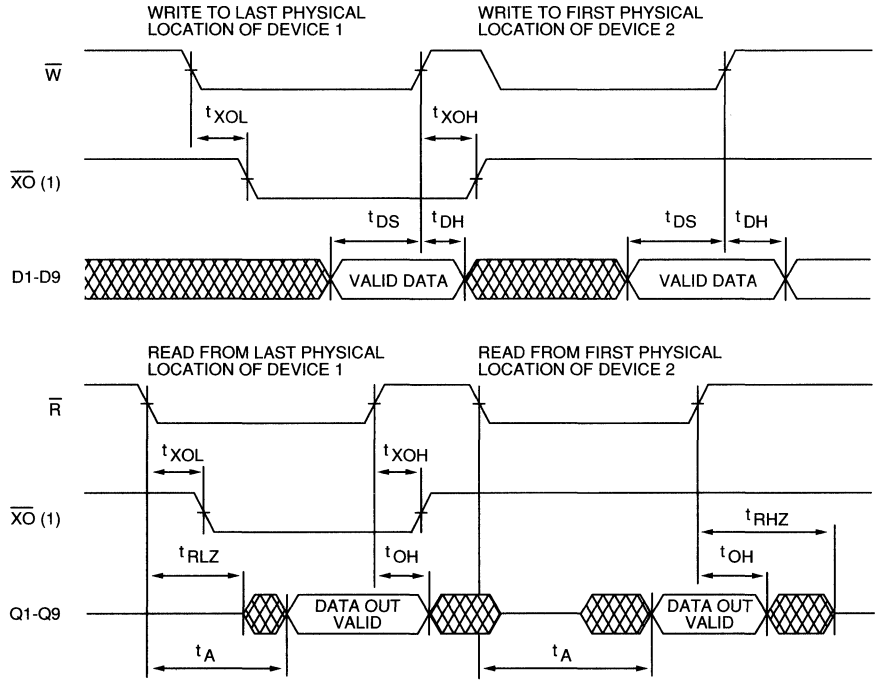


HALF-FULL FLAG
(FOR CONFIGURED AND NONCONFIGURED MODES)



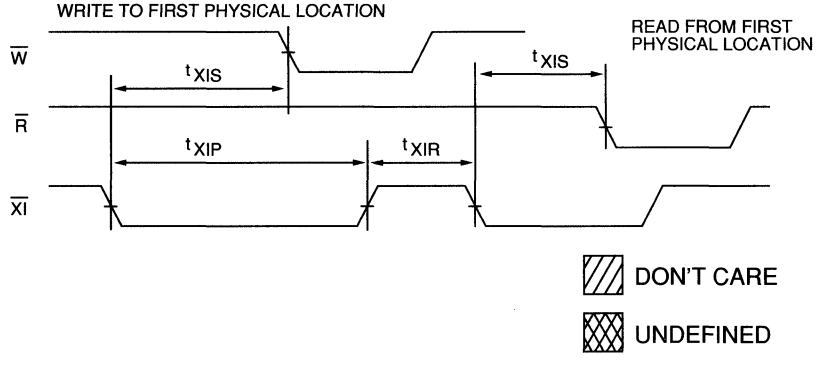
FIFO

EXPANSION MODE ($\overline{XO}$)



NOTE: 1. $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

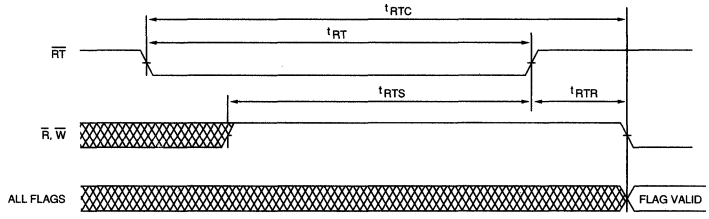
EXPANSION MODE ($\overline{XI}$)



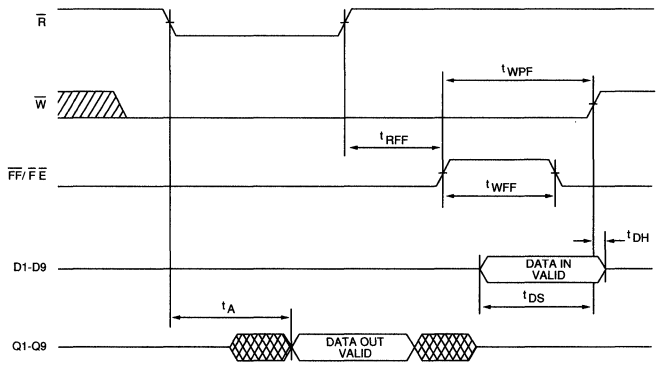
FIFO

FIFO

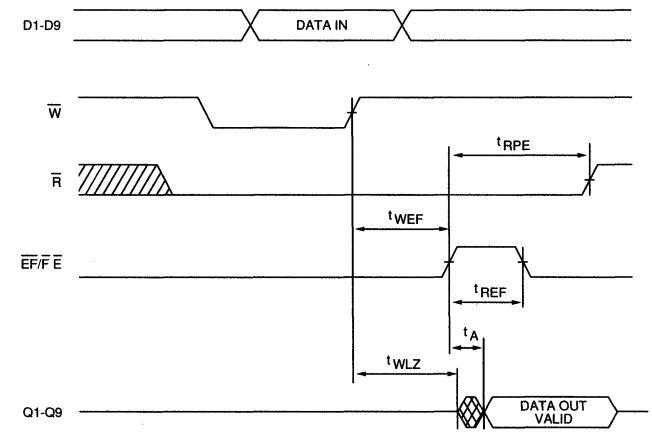
RETRANSMIT



WRITE FLOW-THROUGH



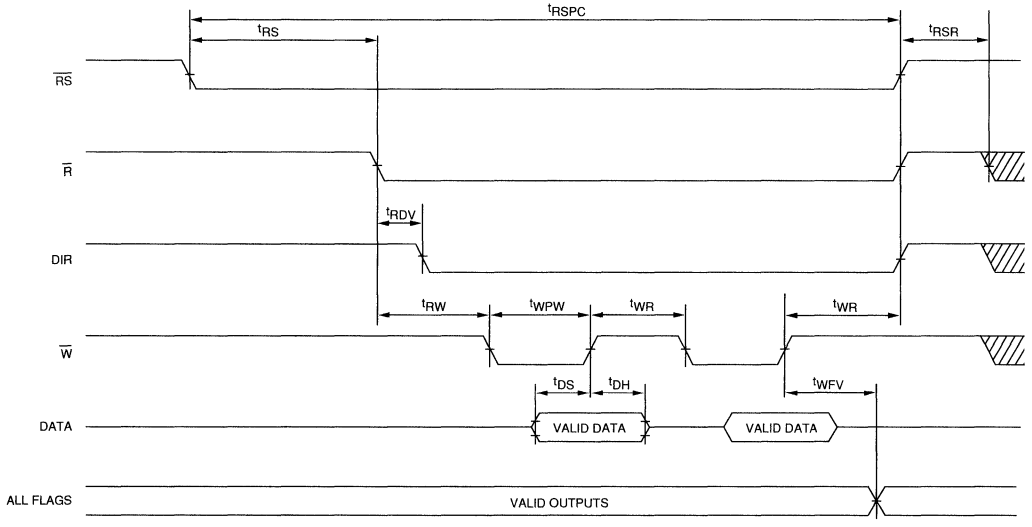
READ FLOW-THROUGH



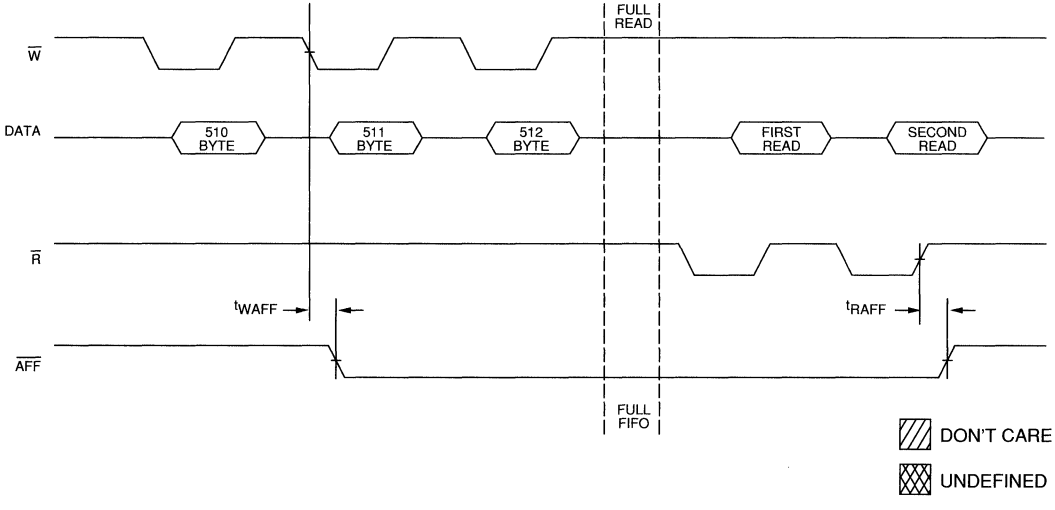
DON'T CARE

UNDEFINED

RESET/REGISTER PROGRAMMING CYCLE TIME [8, 9]

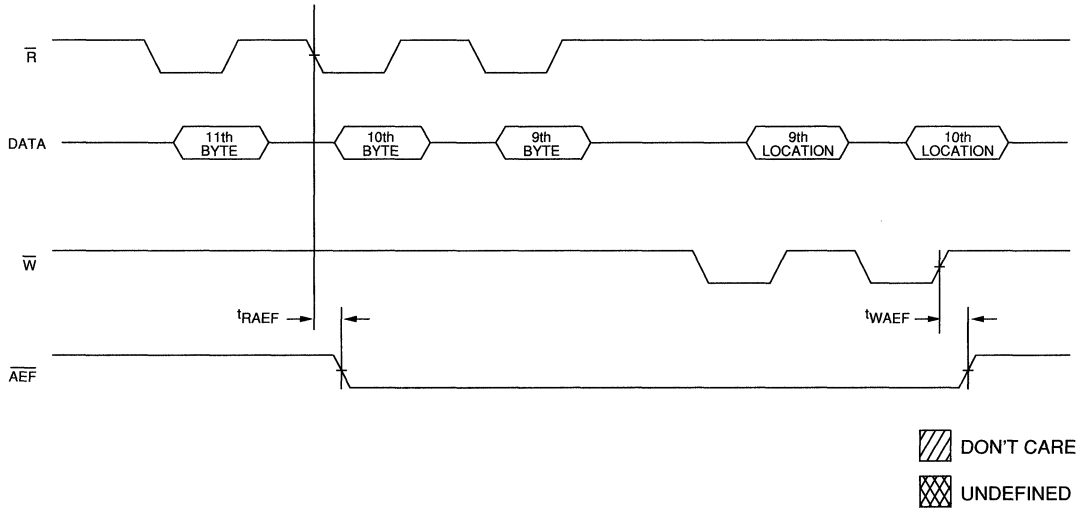


ALMOST FULL FLAG (2-BYTE OFFSET)



FIFO

ALMOST EMPTY FLAG (10-BYTE OFFSET)



FIFO

2K x 9 FIFO

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Half-Full Flag in STAND ALONE mode
- Auto-retransmit capability
- Fully expandable by width and depth
- Pin and function compatible with other standard FIFOs

OPTIONS — MARKING

- Timing

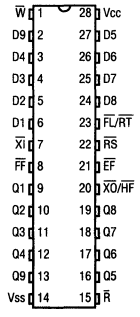
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35

- Packages

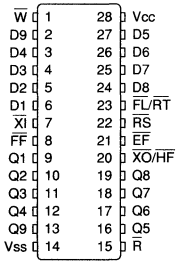
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Ceramic DIP (600 mil)	C
PLCC	EJ
Ceramic LCC	EC
SOJ (300 mil)	DJ

PIN ASSIGNMENT (Top View)

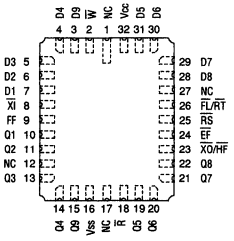
28L DIP (A-9, B-9)



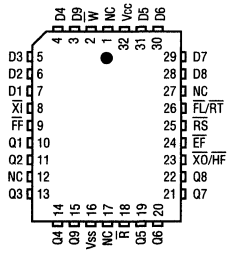
28L SOJ (E-8)



32L LCC (F-4)



32L PLCC (D-2)



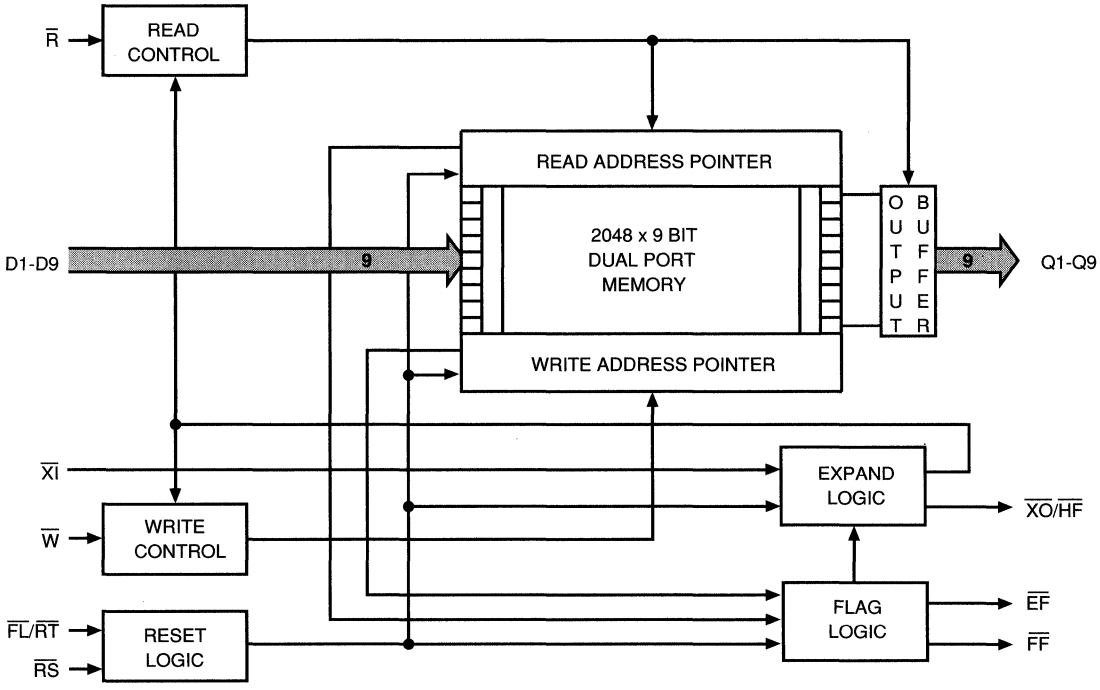
GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual port, six-transistor memory cell with resistor loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain in a high-impedance state. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1-D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1-Q9).
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$)of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$	Input	First Load: Acts as first load signal in DEPTH EXPANSION mode. $\overline{FL}$ if low, will enable the device as the first to be loaded (enables read and write pointers). $\overline{FL}$ should be tied low for the first FIFO in the chain, and tied high for all other FIFOs in the chain Retransmit: Acts as retransmit signal in STAND ALONE mode. $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO}/\overline{HF}$	Output	Expansion Out: Acts as expansion out pin in DEPTH EXPANSION mode. $\overline{XO}$ will pulse LOW on the last physical WRITE or the last physical read. $\overline{XO}$ should be connected to $\overline{XI}$ of the next FIFO in the daisy chain. Half-full Flag: Acts as Half Full Flag in STAND ALONE mode. $\overline{HF}$ goes LOW when the FIFO becomes more than Half-Full; will stay LOW until the FIFO becomes Half-Full or less.
10, 11, 13, 14, 19, 20, 21, 22, 15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	Output	Data Output: Output or high impedance.
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9020 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing the half-full flags the $\overline{XO}/\overline{HF}$ pin will be shown as $(\overline{XO})/\overline{HF}$.*

RESET

After Vcc is stable, RESET ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is LOW. If $\overline{XI}$ is tied to $\overline{XO}$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the STAND ALONE mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (2048/2 + 1) is written. It will stay asserted until the FIFO becomes half-full or less. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/\overline{HF}$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and the FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$ and valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is being used in the SINGLE DEVICE mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ LOW) and a READ is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read to a FIFO will cause $\overline{XO}/\overline{HF}$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9020 allows the receiving device to request that the data read earlier from the FIFO to be repeated, when less than 2047 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^tRTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. FLOW-THROUGH READs are initiated from the rising edge of $\overline{W}$ and access time is measured from the rising edge of $\overline{EF}$.

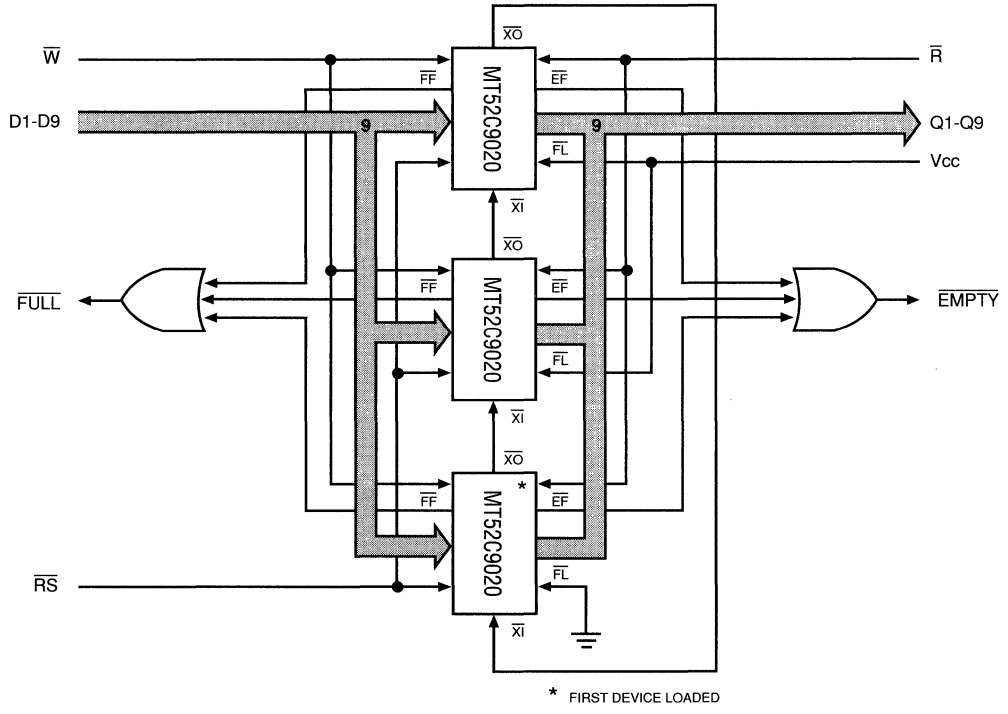


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the stand alone or groups of expanded-depth mode FIFOs. Expanded-width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1) when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9020s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}/(\overline{HF})$ and $\overline{FL}/(\overline{RT})$. Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered during a RESET cycle, by tying the $\overline{XO}/(\overline{HF})$ pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}/(\overline{RT})$ pin grounded. The remaining devices in the chain will have $\overline{FL}/(\overline{RT})$ tied HIGH. During RESET cycle, $\overline{XO}/(\overline{HF})$ of each device is held HIGH, disabling reads and writes to all FIFOs, except the first load device. When the last physical location of the first device is written, the $\overline{XO}/(\overline{HF})$ pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9020. The writes will continue to go to the second device until last location WRITE. Then it will "pass" the write pointer to the third device.

The full condition of the entire FIFO array is signaled by "OR-ing" all the $\overline{FF}$ pins. On the last physical READ of the first device, its $\overline{XO}/(\overline{HF})$ will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. An empty condition is signaled by OR-ing all of the $\overline{EF}$ pins. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1

SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2

DEPTH-EXPANSION/COMPOUND-EXPANSION Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
$\overline{RS}$ = Reset Input, $\overline{FL}$/$\overline{RT}$/DIR= First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -0.5V to +7.0V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

FIFO

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}, \overline{R} \le V_{IL}$; V_{CC} = MAX Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$W, \overline{R} \ge V_{IH}$; V_{CC} = MAX	I_{SB1}		15	mA	
	$\overline{W}, \overline{R} \ge V_{CC}$ -0.2; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}		5	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Shift Frequency	Fs		40		33.3		28.5		22.2	MHz	
Access time	^tA		15		20		25		35	ns	
Read cycle time	^tRC	25		30		35		45		ns	
Read command recovery time	^tRR	10		10		10		10		ns	
Read command pulse width	^tRPW	15		20		25		35		ns	6
Read LOW to Low-Z	^tRLZ	5		5		5		5		ns	
Read to HIGH to High-Z	^tRHZ		15		15		18		20	ns	
Data hold from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
Write cycle time	^tWC	25		30		35		45		ns	
Write command pulse width	^tWPW	15		20		25		35		ns	6
Write command recovery time	^tWR	10		10		10		10		ns	
Write HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5
Data setup time	^tDS	10		12		15		20		ns	
Data hold time	^tDH	0		0		0		0		ns	
Reset cycle time	^tRSC	25		30		35		45		ns	
Reset pulse width	^tRSP	15		20		25		35		ns	6
Reset recovery time	^tRSR	10		10		10		10		ns	
Read HIGH to Reset HIGH	^tRRS	15		20		25		35		ns	
Write HIGH to Reset HIGH	^tWRS	15		20		25		35		ns	
Retransmit cycle time	^tRTC	25		30		35		45		ns	
Retransmit pulse width	^tRT	15		20		25		35		ns	
Retransmit recovery time	^tRTR	10		10		10		12		ns	
Retransmit setup time	^tRTS	15		20		25		35		ns	
Reset to $\overline{EF}$ LOW	^tEFL		25		30		35		45	ns	
Reset to $\overline{HF}$ $\overline{FF}$ HIGH	^tHFH, ^tFFH		25		30		35		45	ns	
Read LOW to $\overline{EF}$ LOW	^tREF		20		20		25		35	ns	
Read HIGH to $\overline{FF}$ HIGH	^tRFF		20		20		25		35	ns	
Write LOW to $\overline{FF}$ LOW	^tWFF		20		20		25		35	ns	
Write HIGH to $\overline{EF}$ HIGH	^tWEF		20		20		25		35	ns	
Write LOW to $\overline{HF}$ LOW	^tWHF		25		30		35		45	ns	
Read HIGH to $\overline{HF}$ HIGH	^tRHF		25		30		35		45	ns	
Read pulse after $\overline{EF}$ HIGH	^tRPE	15		20		25		35		ns	5
Write pulse width after $\overline{FF}$ HIGH	^tWPF	15		20		25		35		ns	5
Read/Write to $\overline{XO}$ LOW	^tXOL		20		20		25		35	ns	
Read/Write to $\overline{XO}$ HIGH	^tXOH		20		20		25		35	ns	
$\overline{XI}$ pulse width	^tXIP	15		20		25		35		ns	
$\overline{XI}$ setup time	^tXIS	10		12		15		15		ns	
$\overline{XI}$ recovery time	^tXIR	10		10		10		10		ns	

FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Flow-through mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

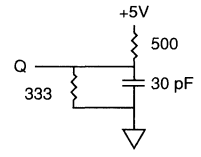
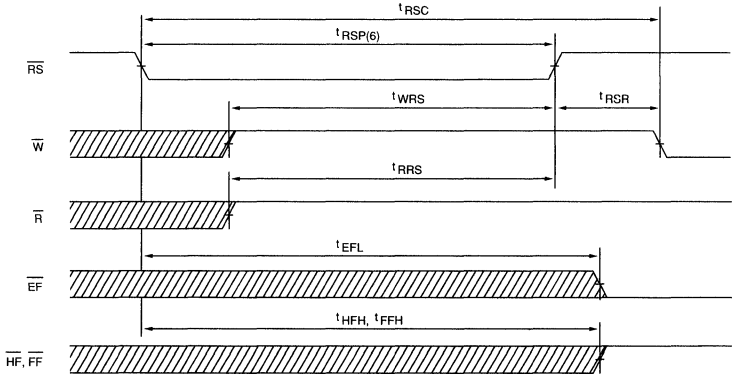
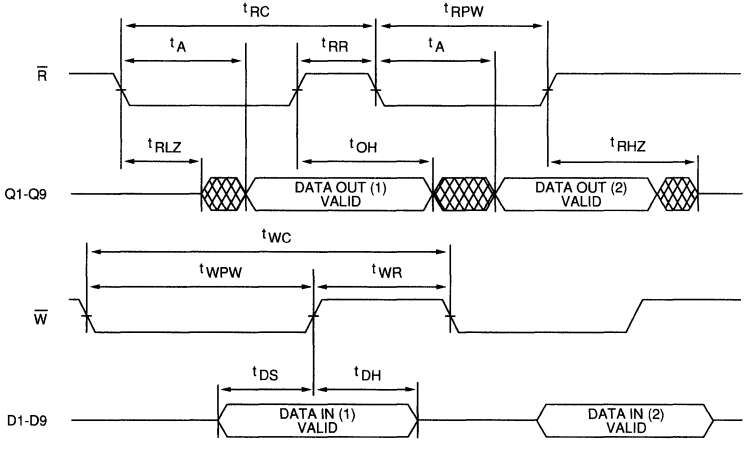


Fig. 2
OUTPUT LOAD EQUIVALENT

RESET



ASYNCHRONOUS READ AND WRITE

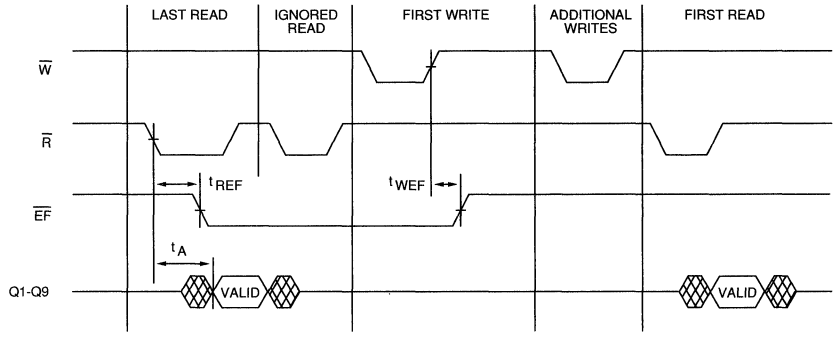


DON'T CARE

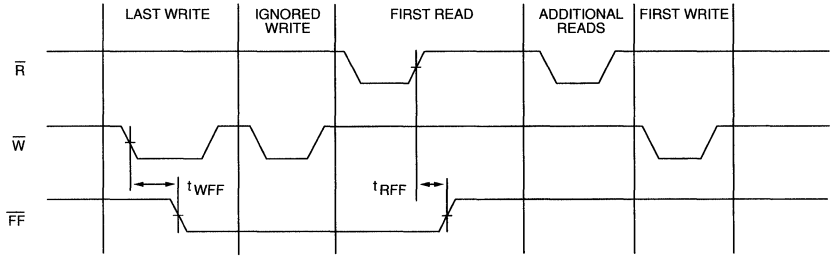
UNDEFINED

FIFO

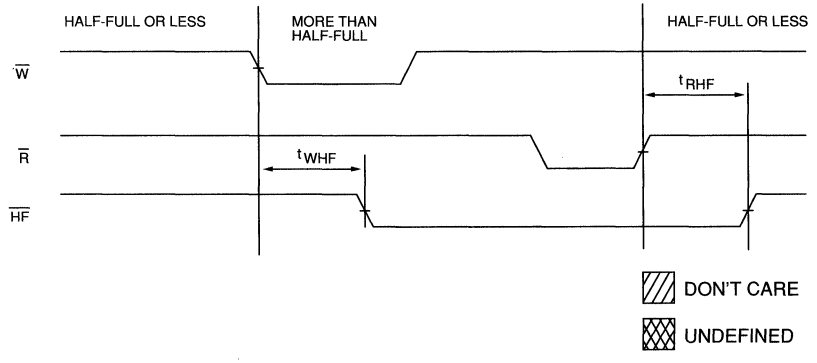
EMPTY FLAG



FULL FLAG

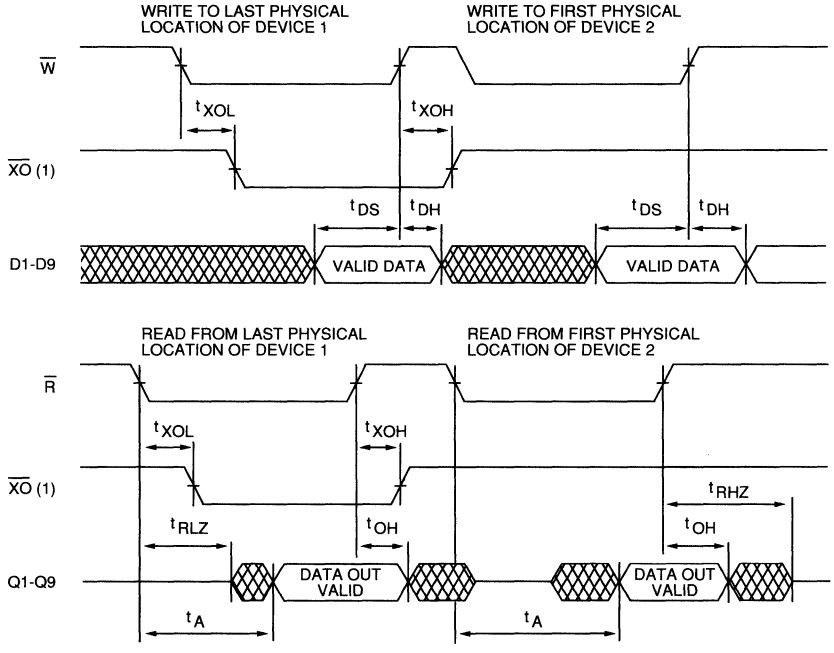


HALF-FULL FLAG



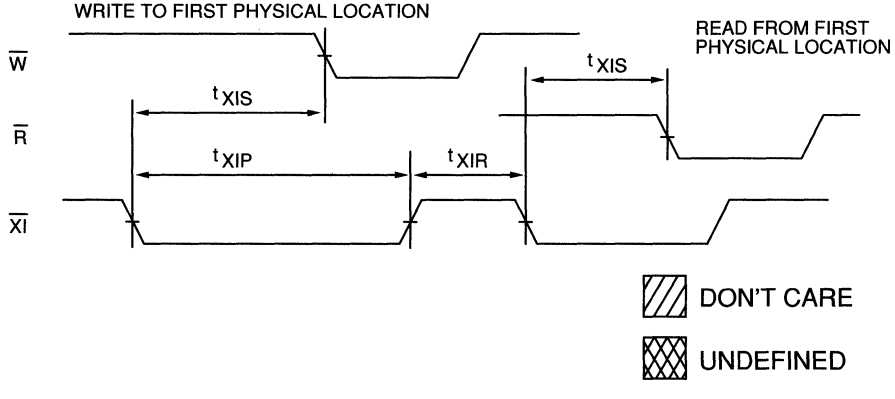
FIFO

EXPANSION MODE ($\overline{XO}$)



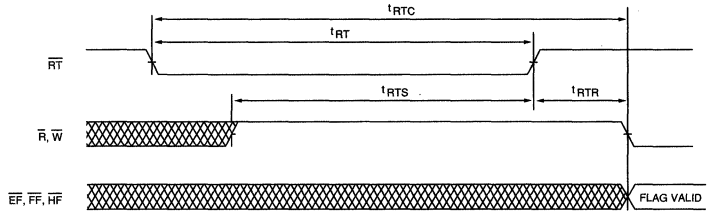
NOTE: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

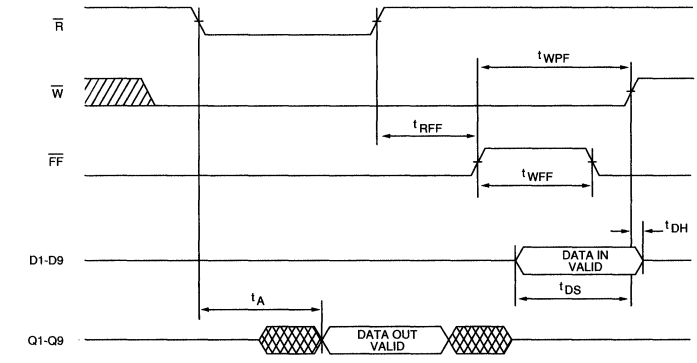


FIFO

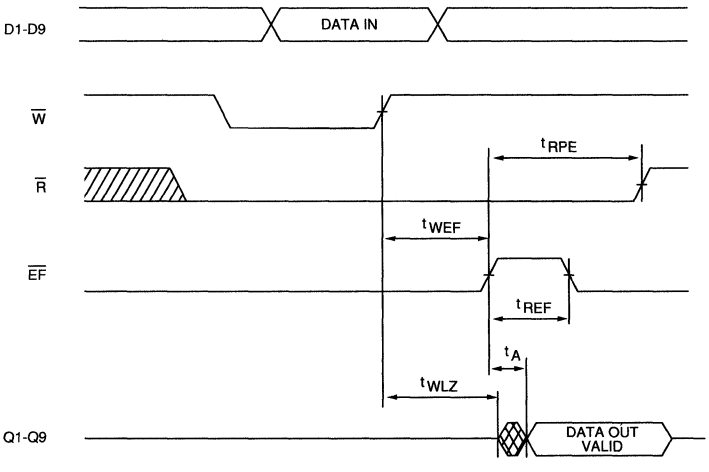
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



DON'T CARE

UNDEFINED

FIFO

FIFO

2K x 9 FIFO

WITH PROGRAMMABLE FLAGS

FEATURES

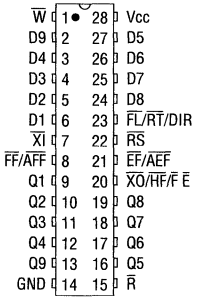
- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typical (standby); 350mW typical (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Two fully configurable Almost Full and Almost Empty Flags
- Programmable Half Full Flag or Full/Empty Flag option eliminates external counter requirement
- Register loading via the input or output pins
- Auto-retransmit capability in single-device mode
- Fully expandable by width and depth
- Pin and function compatible with standard FIFOs

OPTIONS

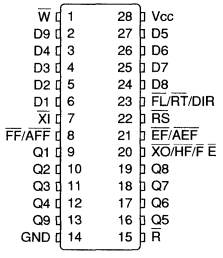
	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Ceramic DIP (600 mil)	C
PLCC	EJ
Ceramic LCC	EC
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

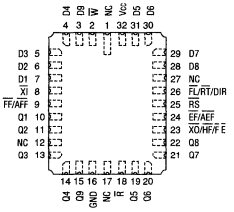
28L/DIP
(A-9, B-9)



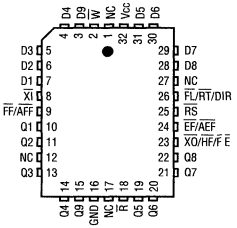
28L/SOJ
(E-8)



32L/LCC
(F-4)



32L/PLCC
(D-2)



GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

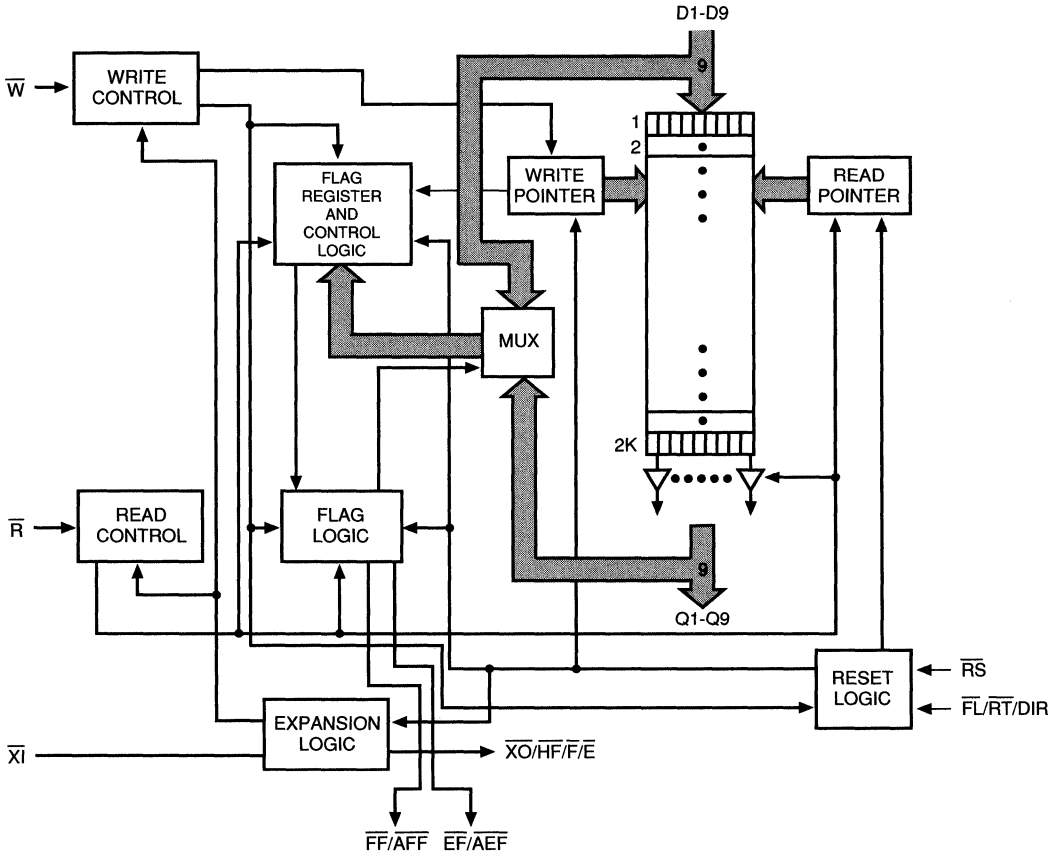
These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates.

When not configured, the MT52C9022 defaults to a standard FIFO with empty ($\overline{EF}$), full ($\overline{FF}$) and half-full ($\overline{HF}$) flag pins. The MT52C9022 can be configured for programmable flags by loading the internal flag registers (as described under "Register Load Mode" on page 8-73). In configured mode, up to three flags are provided. The first two are the almost empty flag ($\overline{AEF}$) and the almost full flag ($\overline{AFF}$) with independently programmable offsets. The third one is either an $\overline{HF}$ or a full and empty ($\overline{F}$ $\overline{E}$) flag, depending on the bit configuration of the registers. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. The MT52C9022 is speed, function and pin compatible with lower density FIFOs from Micron.

FIFO

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: This pin is used to reset the device and load internal flag registers. During device reset, all internal pointers and registers are cleared.
2	1	$\overline{W}$	Input	Write: A LOW on this pin loads data into the device. The internal write pointer is incremented after the rising edge of the write input.
18	15	$\overline{R}$	Input	Read: A LOW on this pin puts the oldest valid data byte in the memory array on the output bus. The internal read pointer is incremented at the rising edge of the read signal. Outputs are High-Z when this pin is HIGH.
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$) of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$/DIR	Input	First Load/Retransmit/Direction: When in single-device mode, this pin can be used to initiate a reread of the previously read data. When in REGISTER LOAD mode, the pin is used for register loading direction. When it is LOW, registers are loaded through the data output pins. When it is HIGH, registers are loaded through the data input pins. In DEPTH EXPANSION mode, this pin should be tied LOW if the device is the first one in the chain and tied HIGH if it is not the first one.
7, 6, 5, 4, 31, 30 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs: Data on these lines are stored in the memory array or flag registers during array WRITE or register programming, respectively.
24	21	$\overline{EF}/\overline{AEF}$	Output	Empty Flag/Almost Empty Flag: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is an Empty Flag output. When in CONFIGURED mode, it is an Almost Empty Flag output. This pin is active LOW.
9	8	$\overline{FF}/\overline{AFF}$	Output	Full Flag/Almost Full Flags: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is a Full Flag output. When in CONFIGURED mode, it is an Almost Full Flag output. This pin is active LOW.
23	20	$\overline{XO}/\overline{HF}/\overline{FE}$	Output	Expansion Out/Half Full/Full/Empty: This pin's function is determined by its operation mode. When in SINGLE DEVICE mode, this pin is either HF Flag or a Full/Empty Flag, depending on the state of the most significant bit of Almost Full Flag Register. The pin is an $\overline{XO}$ output when the part is in DEPTH EXPANSION mode. This pin defaults to $\overline{XO}/\overline{HF}$ in NONCONFIGURED mode.
10, 11, 13, 14 19, 20, 21, 22,15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	I/O	Data Output: These pins may be used for data retrieval. The pins become inputs during register loading with DIR input HIGH. The outputs are disabled (High-Z) during device idle ($\overline{R}$ = HIGH).
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	GND	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9022 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For multiple function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing half-full flags, the $\overline{XO}/\overline{HF}/\overline{F\ E}$ pin will be shown as $(\overline{XO})/\overline{HF}/(\overline{F\ E})$.*

RESET

After Vcc is stable, Reset ($\overline{RS}$) must be taken LOW with both $\overline{R}$ and $\overline{W}$ HIGH to initialize the read and write pointers and flags. This also clears all internal registers. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is tied LOW. If $\overline{XI}$ is connected to $\overline{XO}/(\overline{HF})$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW and if the FIFO is not full. The WRITE cycle is initiated by the falling edge of $\overline{W}$. Data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While the $\overline{FF}$ is asserted, all writes are inhibited and previously stored data are unaffected. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and FIFO is not empty ($\overline{EF}$ is High). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$. Valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is full and a READ is initiated, the $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the expanded mode, the last location read from a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9022 allows the receiving device to request that data just read from the FIFO be repeated, when less than 2047 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}/(DIR)$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may start reading the data from the beginning of the FIFO ^tRTR after $(\overline{FL})/\overline{RT}/(DIR)$ is taken HIGH. Some or all flags may be affected depending on the location of the read and write pointers before and after the retransmit.

DATA FLOW-THROUGH

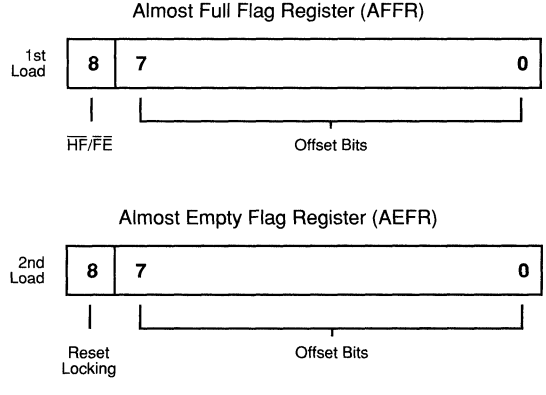
Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{W}$, and access time is measured from the rising edge of the empty flag.

REGISTER LOAD MODE

This mode of operation is used to reset the device and program the internal flag registers. This yields an almost full and an almost empty flag (DIP package pins 8 and 21 respectively) and a half-full or $\overline{F}/\overline{E}$ flag (DIP package pin 20).

Two 9-bit internal registers have been provided for flag configuration. One is the almost full flag register (AFFR) and the other is the almost empty flag register (AEFR). Bit configurations of the two registers are shown below.

REGISTER SET FOR MT52C9022



Note that bits 0-7 are used for offset setting. The offset value ranges from 1 to 255 words. Each offset value corresponds to a 2-byte increment. This provides a maximum offset of 510 bytes.

Bits 6 and 7 are reserved for future offset expansion. Bit 8 of the AFFR is used for configuration of $\overline{HF}/\overline{F}\,\overline{E}$ pin. When this bit is set LOW, the $HF/\overline{F}\,\overline{E}$ pin is configured as an $\overline{HF}$ flag output. When it is set high, the $HF/\overline{F}\,\overline{E}$ is configured as an $\overline{F}/\overline{E}$ flag output.

Bit 8 of the AEFR is used for reset locking. When this bit is set LOW, subsequent device RESET or REGISTER LOADING cycles reset the device. When the bit is programmed HIGH, subsequent RESET cycles are ignored. In this mode, the flag registers can be reconfigured without device reset. The part can be reset by cycling power to the device or by writing zero (0) into bit 8 of the AEFR register followed by a DEVICE RESET or REGISTER LOAD.

Flag registers are loaded by bringing $\overline{RS}$ LOW followed by the $\overline{R}$ input. The $\overline{R}$ pin should be brought LOW ^tRS after the $\overline{RS}$ becomes LOW. The registers may be loaded via the input pins or the output pins depending on the status of the DIR control input. Data is latched into the registers at the rising edge of the $\overline{W}$ control pin. The first WRITE loads the AFFR while the second WRITE loads the AEFR. This loading order is fixed.

BIDIRECTIONAL MODE

Applications requiring data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by using two MT52C9022s. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion may be used in this mode.

FLAG TIMING

A total of three flag outputs are provided in either CONFIGURED or NONCONFIGURED mode. In the NONCONFIGURED mode, the three flags are $\overline{HF}$ flag, $\overline{EF}$ and $\overline{FF}$. The $\overline{HF}$ flag goes active when more than half the FIFO if full. The flag goes inactive when the FIFO is half full or less.

The full and empty flags are asserted when the last byte is written to or read out of the FIFO, respectively. They are deasserted when the first byte is loaded into an empty FIFO or read out of a full FIFO, respectively. All three flag outputs are active LOW.

When the device is programmed, the $\overline{AFF}$ and $\overline{AEF}$ go active after a READ/WRITE cycle initiation of the location corresponding to the programmed offset value. For example, if the AEFR is programmed with a 10-byte offset (loading a Hex value of 05), the $\overline{AEF}$ flag goes active while reading the 10th location before the FIFO is empty. The flag goes inactive when there are 10 or more bytes left in the FIFO. The assertion timing and deassertion timing of the $\overline{AFF}$ are the same.

The third flag in the PROGRAM mode is either $\overline{HF}$ or $\overline{F}/\overline{E}$ flag depending on the state of the highest bit of the AFFR. If the device is programmed for $\overline{HF}$ flag, it functions like the $\overline{HF}$ flag in NONPROGRAMMED mode. If the device is configured for $\overline{F}/\overline{E}$ flag, the pin will be active (LOW) when the FIFO is either empty or full. The condition of the FIFO is determined by the state of $\overline{F}/\overline{E}$ together with states of $\overline{AFF}$ and $\overline{AEF}$ (example: if $\overline{F}/\overline{E}$ is LOW and $\overline{AFF}$ is LOW but $\overline{AEF}$ is HIGH, the FIFO is full).

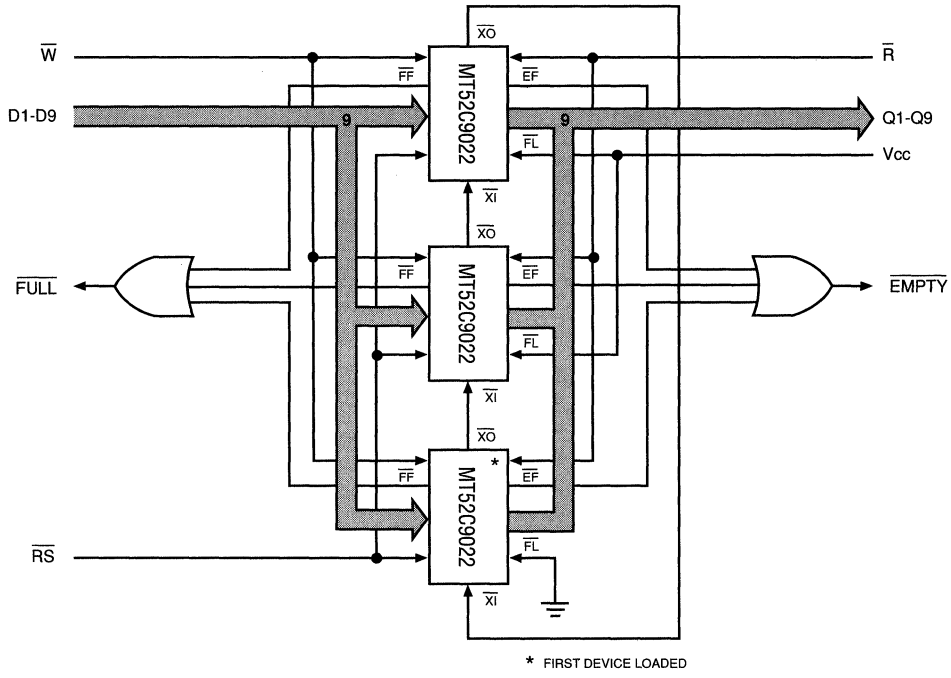


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9022s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) and $\overline{FL}$/($\overline{RT}$/DIR). Figure 1 illustrates a typical three-device expansion. The depth-expansion mode is entered by tying the $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$/DIR) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$/DIR) tied HIGH. Upon a reset, reads and writes to all FIFOs are disabled, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9022. The writes will continue to go to the second device until last location write. Then it will "pass" the write pointer to the third device. The full condition of the entire FIFO array is signaled when all the $\overline{FF}$/($\overline{AFF}$) pins are LOW.

On the last physical READ of the first device, its $\overline{XO}$ ($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The READ pointer never overtakes the write pointer. On the last READ, an empty condition is signaled by all of the $\overline{EF}$ pins being LOW. This inhibits further reads. While in the depth-expansion mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE 1

SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2

DEPTH-EXPANSION/COMPOUND-EXPANSION Mode

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
$\overline{RS}$ = Reset Input, $\overline{FL}$/$\overline{RT}$/DIR= First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -0.5V to +7.0V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

FIFO

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	MIN	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}, \overline{R} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{CC}		120	115	110	100	mA	3
Power Supply Current: Standby	$\overline{W}, \overline{R} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/^tRC	I_{SB1}		15	15	15	15	mA	
	$\overline{W}, \overline{R} \ge V_{CC}$ -0.2; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2, $V_{IH} \ge V_{CC}$ -0.2; f = 0	I_{SB2}		5	5	5	5	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	10	10	10	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	10	10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4					V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}					0.4	V	1

CAPACITANCE

($V_{IN} = 0V$; $V_{OUT} = 0V$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured and nonconfigured modes) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Shift frequency	^tRF		40		33.3		28.5		22.2	MHz	
READ cycle time	^tRC	25		30		35		45		ns	
Access time	^tA		15		20		25		35	ns	6
READ recovery time	^tRR	10		10		10		10		ns	
Read pulse width	^tRPW	15		20		25		35		ns	
Read LOW to Low-Z	^tRLZ	5		5		5		5		ns	7
Read to HIGH to High-Z	^tRHZ		15		15		18		20	ns	7
Data HOLD from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
WRITE Cycle											
WRITE cycle time	^tWC	25		30		35		45		ns	
Write pulse width	^tWPW	15		20		25		35		ns	6
WRITE recovery time	^tWR	10		10		10		10		ns	
Write HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5, 7
Data setup time	^tDS	10		12		15		18		ns	
Data hold time	^tDH	0		0		0		0		ns	
RETRANSMIT Cycle											
Restransmit cycle time	^tRTC	25		30		35		45		ns	
Retransmit pulse width	^tRT	15		20		25		35		ns	
Retransmit recovery time	^tRTR	10		10		10		12		ns	
Retransmit command setup time	^tRTS	15		20		25		35		ns	
RESET Cycle											
RESET cycle time (no register programming)	^tRSC	25		30		35		45		ns	
Reset pulse width	^tRSP	15		20		25		35		ns	6
Reset recovery time	^tRSR	10		10		10		10		ns	
$\overline{RS}$ LOW to $\overline{R}$ LOW	^tRS	15		20		25		35		ns	
Reset and register programming cycle time	^tRSPC	85		100		115		145		ns	
$\overline{R}$ LOW to DIR valid (register load cycle)	^tRDV	5		5		5		5		ns	
$\overline{R}$ LOW to register load	^tRW	10		10		10		10		ns	
$\overline{W}$ HIGH to $\overline{RS}$ LOW	^tWRS	0		0		0		0		ns	
$\overline{R}$ HIGH to $\overline{RS}$ LOW	^tRRS	0		0		0		0		ns	

FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.
7. Values guaranteed by design, not currently tested.
8. $\overline{R}$ and DIR signals must go inactive (HIGH) coincident with $\overline{RS}$ going inactive (HIGH).
9. DIR must become valid before $\overline{W}$ goes active (LOW).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured mode only) (T_A = 0°C to 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Mode Timing											
$\overline{R}/\overline{W}$ to $\overline{XO}$ LOW	tXOL		20		20		25		35	ns	
$\overline{R}/\overline{W}$ to $\overline{XO}$ HIGH	tXOH		20		20		25		35	ns	
$\overline{XI}$ pulse width	tXIP	15		20		25		35		ns	
$\overline{XI}$ command setup time to $\overline{R}/\overline{W}$	tXIS	10		12		15		15		ns	
$\overline{XI}$ command recovery time	tXIR	10		10		10		10		ns	
Flags Timing											
$\overline{W}$ HIGH to Flags Valid	tWFV		15		15		15		15	ns	
$\overline{RS}$ to $\overline{EF}$ LOW	tEFL		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{EF}$ LOW	tREF		20		20		25		35	ns	
$\overline{W}$ HIGH to $\overline{EF}$ HIGH	tWEF		20		20		25		35	ns	
$\overline{R}$ pulse after $\overline{EF}$ HIGH	tRPE	15		20		25		35		ns	5
$\overline{RS}$ to $\overline{HF}$, $\overline{FF}$ HIGH	tHFH, tFFH		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{FF}$	tRFF		15		20		25		30	ns	
$\overline{W}$ LOW to $\overline{FF}$ LOW	tWFF		20		20		25		35	ns	
$\overline{W}$ pulse width after $\overline{FF}$ HIGH	tWPF	15		20		25		35		ns	5
$\overline{W}$ LOW to $\overline{HF}$ LOW	tWHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{HF}$ HIGH	tRHF		25		30		35		45	ns	
$\overline{R}$ HIGH to $\overline{AFF}$	tRAFF		25		30		35		45	ns	
$\overline{W}$ LOW to $\overline{AFF}$	tWAFF		25		30		35		45	ns	
$\overline{R}$ LOW to $\overline{AEF}$ LOW	tRAEF		25		30		35		45	ns	
$\overline{W}$ HIGH to $\overline{AEF}$	tWAEF		25		30		35		45	ns	

FIFO

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

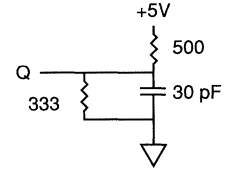
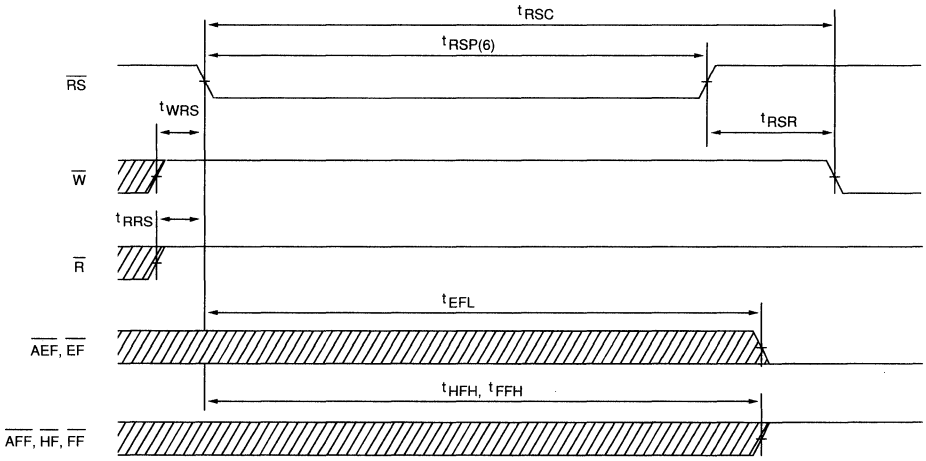
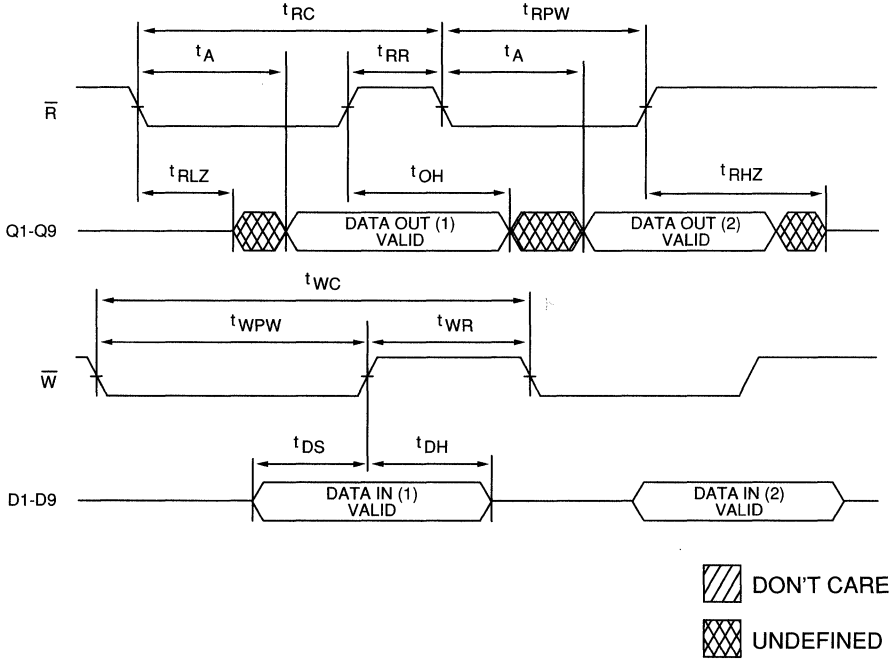


Figure 2
OUTPUT LOAD EQUIVALENT

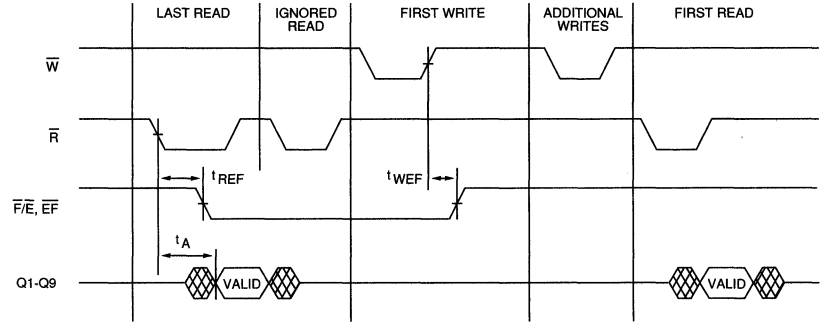
RESET
(WITH NO REGISTER PROGRAMMING)



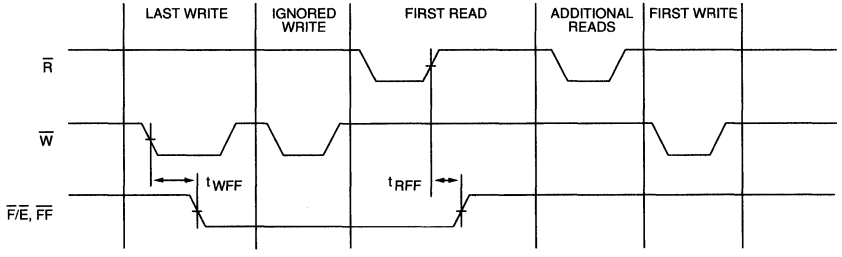
ASYNCHRONOUS READ AND WRITE



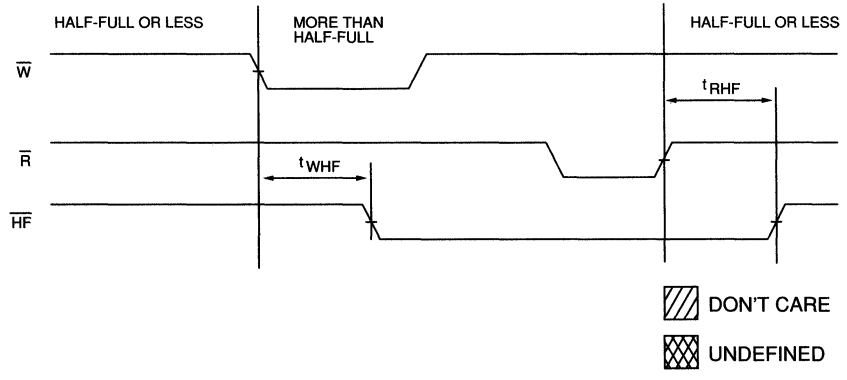
EMPTY FLAG



FULL FLAG

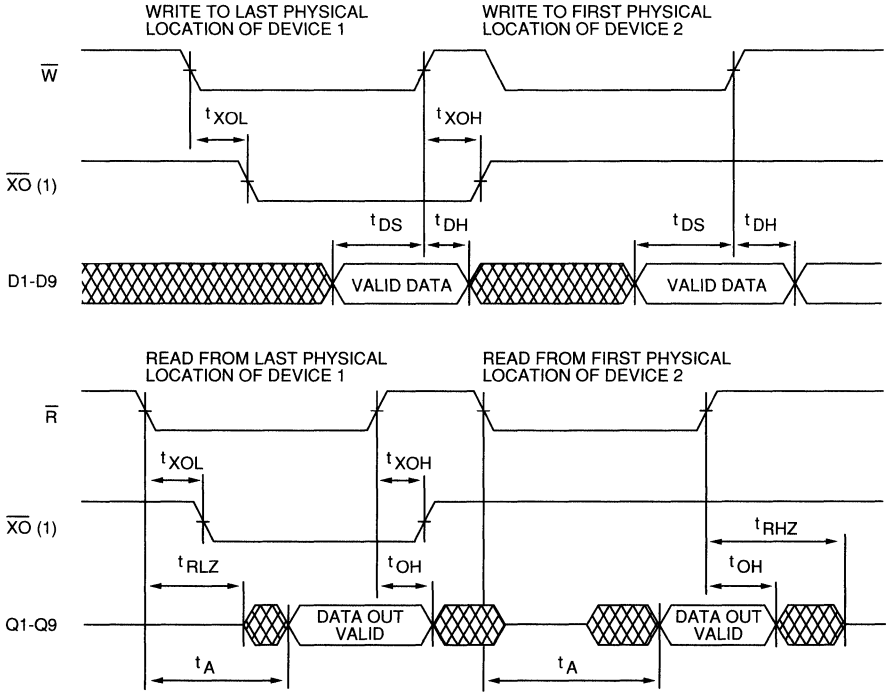


HALF-FULL FLAG
(FOR CONFIGURED AND NONCONFIGURED MODES)



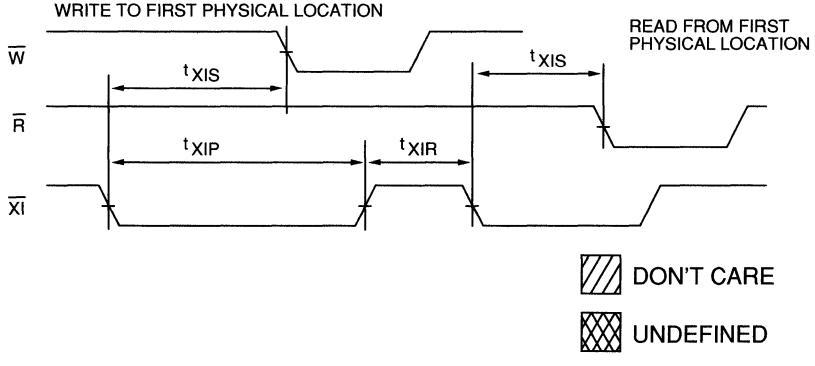
FIFO

EXPANSION MODE ($\overline{XO}$)

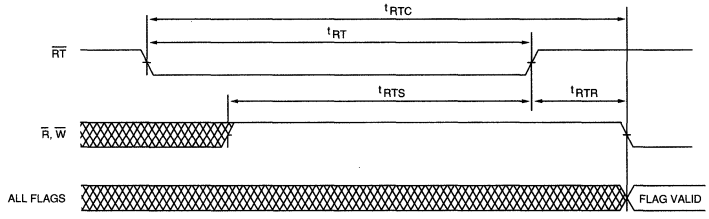


NOTE: 1. $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

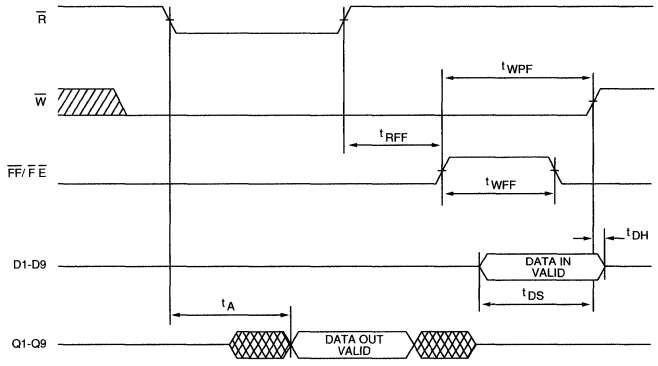
EXPANSION MODE ($\overline{XI}$)



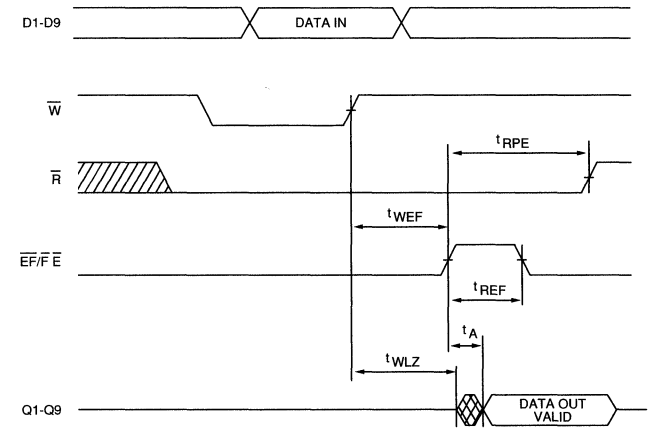
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH

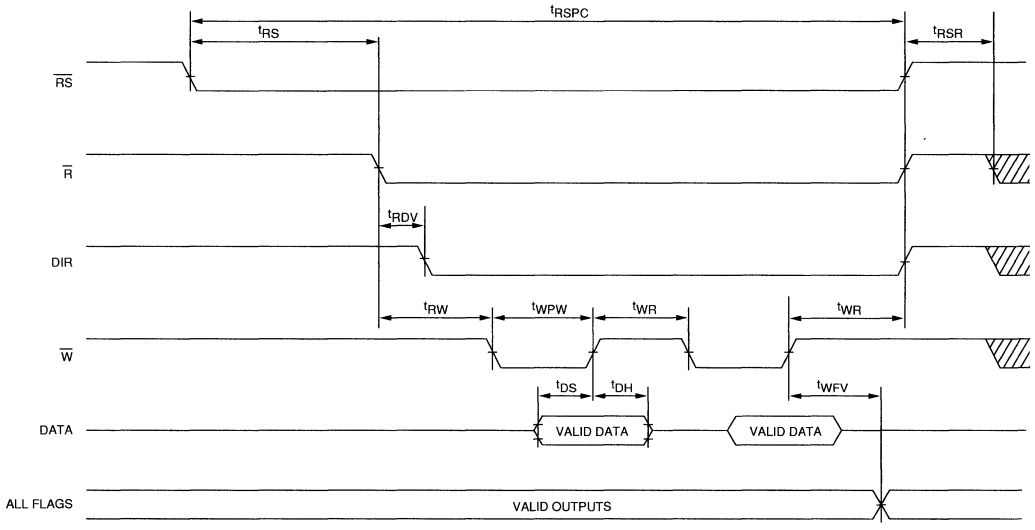


DON'T CARE

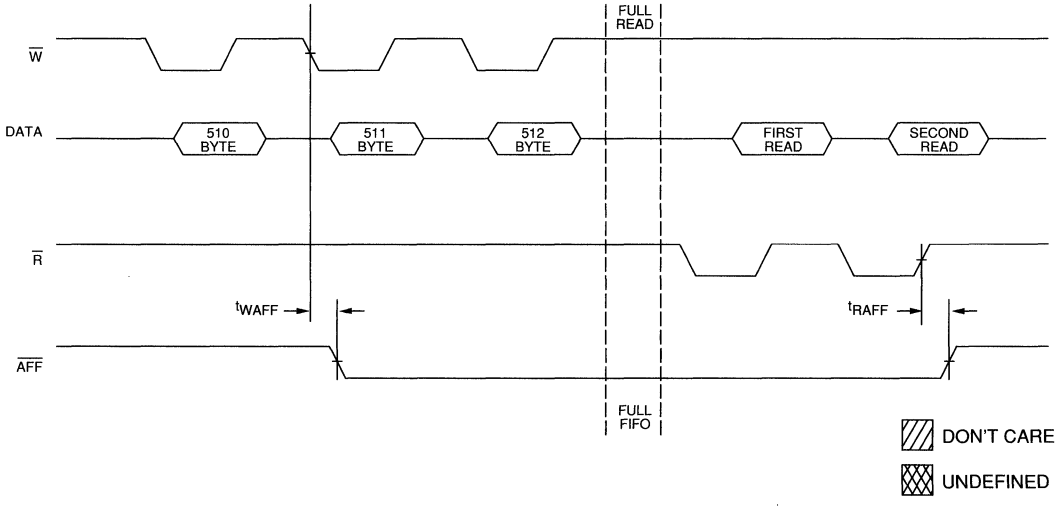
UNDEFINED

FIFO

RESET/REGISTER PROGRAMMING CYCLE TIME [8, 9]

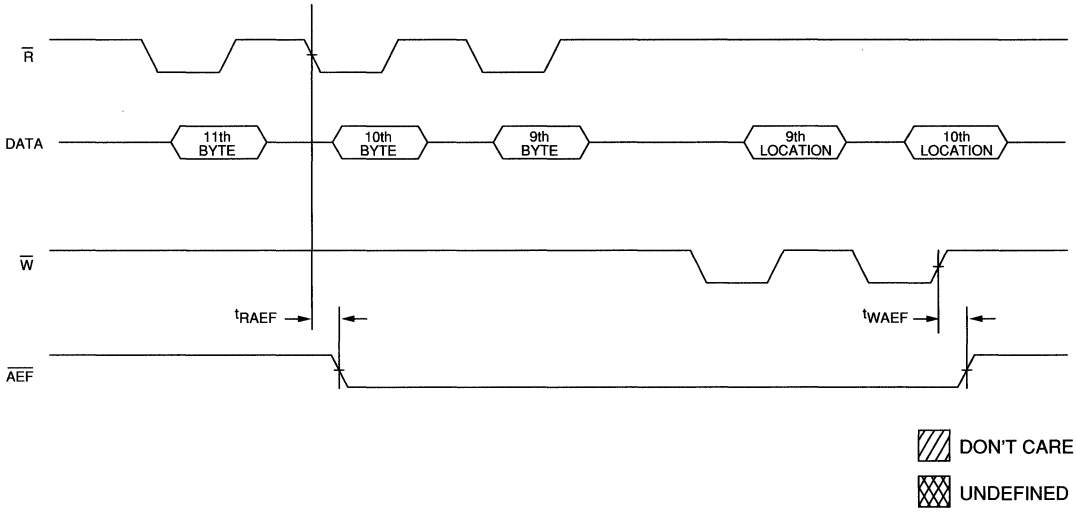


ALMOST FULL FLAG (2-BYTE OFFSET)



FIFO

ALMOST EMPTY FLAG (10-BYTE OFFSET)



MICRON TECHNOLOGY, INC.

APPLICATION/TECHNICAL NOTE SELECTION GUIDE

TECHNICAL NOTE

DRAM POWER-UP AND REFRESH CONSTRAINTS

INTRODUCTION

The JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding and addressing these incompatibilities and providing for them will offer designers and system users greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode to be a $\overline{W}$CBR, which is CBR with the $\overline{WE}$ pin held at a logical HIGH level.

The reason for $\overline{W}$CBR instead of CBR on the 4 Meg is that a CBR cycle with $\overline{WE}$ LOW will put the the 4 Meg into the JEDEC-specified test mode (WCBR). In contrast, the 1 Meg test mode is entered by applying a HIGH signal to the test pin (pin 4 on DIPs, pin 5 on SOJs and pin 8 on ZIPs). This HIGH signal is usually a "super voltage" (Vin ≥ 7.5V), so normal TTL or CMOS HIGH levels will not cause the part to enter the test mode.

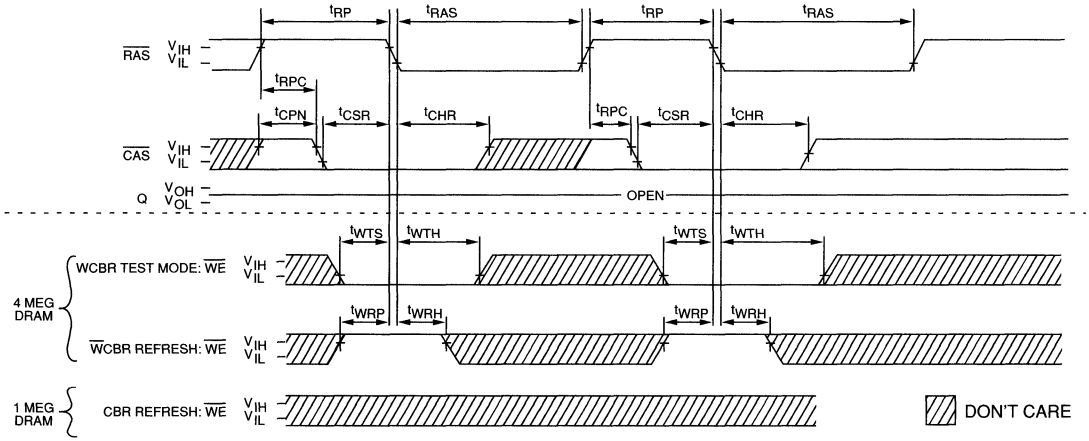
POWER-UP

The 4 Meg $\overline{W}$CBR constraint may also introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$-ONLY REFRESH or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a $\overline{W}$CBR REFRESH cycle.

SUMMARY

The 1 Meg and 4 Meg are compatible, with the following exceptions:

1. The 1 Meg test pin is the A10 pin on the 4 Meg.
2. For standard test mode, the 1 Meg requires a vaild HIGH on the test pin while the 4 Meg requires a CBR cycle with $\overline{WE}$ LOW.
3. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be a "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH ($\overline{W}$CBR).
4. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may use $\overline{RAS}$-ONLY REFRESH or $\overline{W}$CBR REFRESH cycles, exclusively.



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

APPLICATION/TECHNICAL INFORMATION

TECHNICAL NOTE

MT4C1664 AND MT4C1665 COMPATIBILITIES

INTRODUCTION

Micron provides the 64K x 16 DRAM in two versions: MT4C1664 and MT4C1665. The MT4C1664 has two $\overline{WE}$ pins which allow for BYTE-WRITE cycles. It does not support WRITE-PER-BIT. The MT4C1665 has one $\overline{WE}$ pin and offers nonpersistent, WRITE-PER-BIT (MASKED WRITE) cycles.

COMPATIBILITY

The MT4C1664 and MT4C1665 may be used interchangeably, provided precautions are taken ahead of time. The memory system may not utilize the WRITE-PER-BYTE feature of the MT4C1664 or the WRITE-PER-BIT feature of the MT4C1665 in order to maintain interchangeability.

At the system level, a special timing constraint exists. $\overline{WE}$ must be held HIGH when $\overline{RAS}$ transitions from HIGH to LOW (preventing the MT4C1665 from performing WRITE-PER-BIT cycles). The two $\overline{WE}$ traces must be connected together (pins 12 and 13 on SOJ or pins 22 and 23 on ZIP) in order to ensure that all 16 bits will be written on the MT4C1664.

The MT4C1664 and MT4C1665 are now interchangeable. The MT4C1664 will have twice the capacitive load on the write enable signal as the MT4C1665 due to its two $\overline{WE}$ pins. Its $\overline{WE}$ timing will be a "don't care" when $\overline{RAS}$ transitions from HIGH to LOW while the MT4C1665 will enter a WRITE-PER-BIT cycle if $\overline{WE}$ is LOW when $\overline{RAS}$ transitions from HIGH to LOW.

The MT4C1665 can provide the BYTE-WRITE capability of the MT4C1664 by allowing the mask register to be enabled by bytes. However, this may not be practical since it requires additional circuitry.

SUMMARY

An application that performs 16-bit word writes will allow either the MT4C1664 or MT4C1665 to be used. The MT4C1664 must have both $\overline{WE}$ pins connected, doubling capacitance on the write enable signal, but its timing is a "don't care" when $\overline{RAS}$ goes LOW. On the other hand, the MT4C1665 has only one $\overline{WE}$ for lower capacitance, but $\overline{WE}$ must always be held HIGH when $\overline{RAS}$ transitions from HIGH to LOW (refer to Note 1).

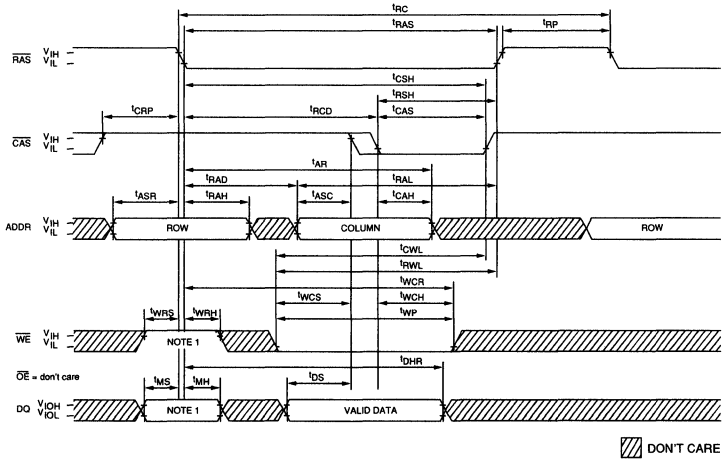


Figure 1
MT4C1665 TIMING CONSTRAINTS

NOTE: 1. Applies to MT4C1665 only. The MT4C1664 specifies these as "don't cares" during this portion of operation.

TECHNICAL NOTE

MT4C1664: 256 KILOBYTE MEMORY SYSTEM WITH FOUR $\overline{RAS}$ LINES

INTRODUCTION

Micron's MT4C1664 64K x 16 DRAM is a great solution for replacing 64K x 4 DRAMs in VGA systems. For a 256 kilobyte (KB) memory system, two MT4C1664s replace eight 64K x 4 DRAMs, resulting in improved reliability and performance margins, decreased power consumption, reduced costs and board savings, while maintaining state-of-the-art technology.

This application note shows how the MT4C1664 may be interfaced with a 256KB memory system using four $\overline{RAS}$ controls and EARLY-WRITE cycles ($\overline{OE}$ grounded). Reference to the MT4C1664 data sheet will be helpful in understanding how the MT4C1664 functions. The schematic in Figure 1 shows 256KB memory systems using four $\overline{RAS}$ controls and EARLY-WRITE cycles and how memory is implemented with both the MT4C1664 and 64K x 4 DRAMs.

The same schematic for the MT4C1664 may also be used in systems using LATE-WRITE cycles ($\overline{OE}$ controlled).

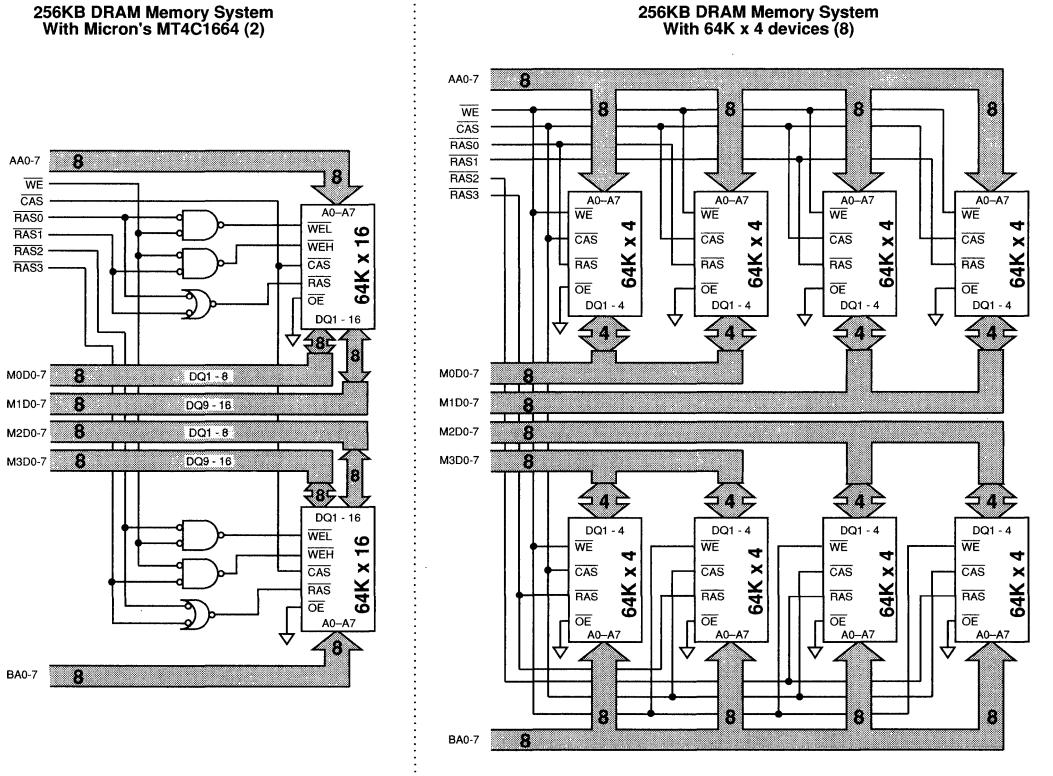


Figure 1
256KB EARLY-WRITE MEMORY

APPLICATION/TECHNICAL INFORMATION

TECHNICAL NOTE

MT4C1664: 256 KILOBYTE MEMORY SYSTEM WITH FOUR $\overline{CAS}$ LINES

INTRODUCTION

Micron's MT4C1664 64K x 16 DRAM is a great solution for replacing 64K x 4 DRAMs in VGA systems. For a 256 kilobyte (KB) memory system, two MT4C1664s will replace eight 64K x 4 DRAMs, resulting in improved reliability and performance margins, decreased power consumption, reduced costs and board savings while maintaining state-of-the-art technology.

This application note shows how the MT4C1664 may interface with a 256KB memory system using four $\overline{CAS}$ controls and EARLY-WRITE cycles ($\overline{OE}$ grounded). Reference to the MT4C1664 data sheet will be helpful in understanding how the MT4C1664 functions. The schematic in Figure 1 shows 256KB memory systems using four $\overline{CAS}$ controls and EARLY-WRITE cycles and how memory is implemented with both the MT4C1664 and 64K x 4 DRAMs.

The same schematic for the MT4C1664 may also be used in systems using LATE-WRITE cycles ($\overline{OE}$ controlled), except Note 1 no longer applies and the two delay paths may be equal.

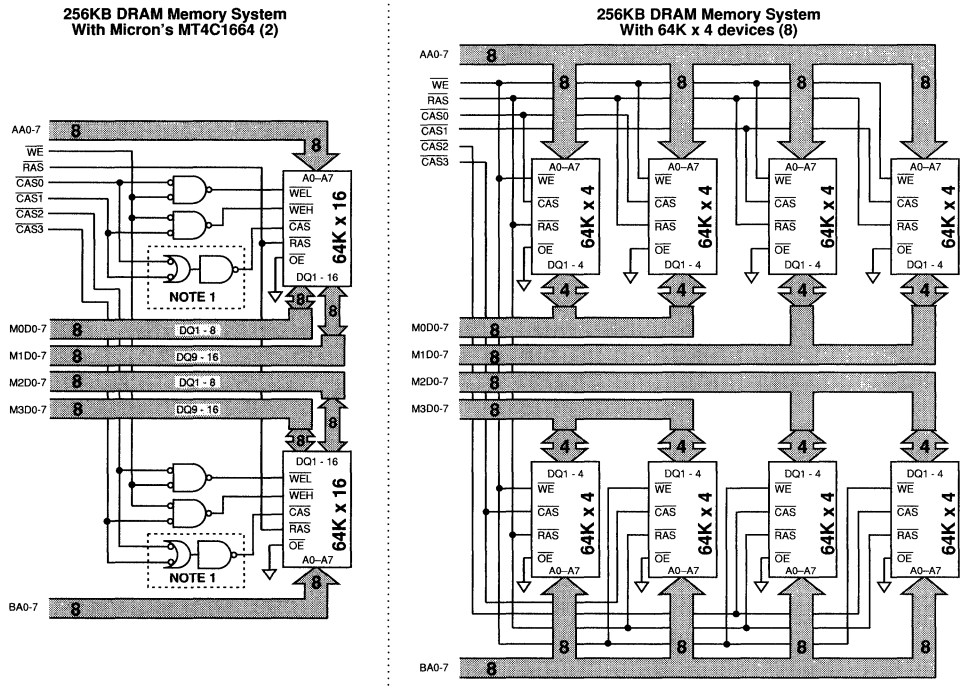


Figure 1
256KB EARLY-WRITE MEMORY

NOTE: 1. This delay path needs to be slightly longer than the two NAND gates to ensure the $\overline{WE}$ to $\overline{CAS}$ setup time is met. This will guarantee the DRAM will always be in EARLY-WRITE during WRITE cycles.

APPLICATION/TECHNICAL INFORMATION

TECHNICAL NOTE

4 MEG DRAM — DIRECT 1 MEG COMPATIBILITY

INTRODUCTION

The JEDEC 4 Meg DRAM introduces three potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up and the JEDEC test mode.

Micron provides two versions of the 4 Meg DRAM. The standard version will not have the JEDEC test mode allowing for 1 Meg DRAM compatibility. The second version will offer the JEDEC test mode.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode to be $\overline{W}$CBR, which is CBR with the $\overline{WE}$ pin held at a logical HIGH level.

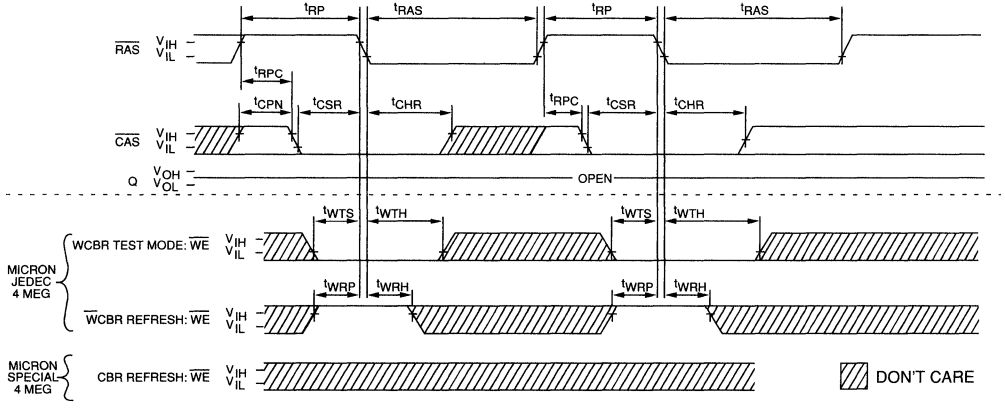
The reason for $\overline{W}$CBR instead of CBR on the 4 Meg is that a CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg $\overline{W}$CBR constraint may also introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP cycle is more restrictive in that eight $\overline{RAS}$-ONLY REFRESH or $\overline{W}$CBR REFRESH cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the test mode for normal operation. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a $\overline{W}$CBR REFRESH cycle.

SPECIAL FEATURE

A memory system currently using 1 Meg DRAMs with $\overline{WE}$ as a "don't care" during CBR REFRESH does not allow for direct upgrading to 4 Meg DRAMs. Micron, realizing some companies will have this situation, provides a special feature on its 4 Meg DRAM requiring "supervoltage" to access the 4 Meg JEDEC WCBR test function. This allows the Micron 4 Meg DRAM to be refreshed in the same manner as any 1 Meg DRAM. Note that the eight POWER-UP cycles should be refresh cycles only in order to guarantee that any 4 Meg DRAM, including Micron's, does not inadvertently power-up in the test mode.



COMPARISON OF JEDEC WCBR TO MICRON 4 MEG CBR

TECHNICAL NOTE

UNDERSTANDING DRAM LATE-WRITE CYCLES

INTRODUCTION

There are three different cycles possible to write to a DRAM: EARLY-WRITE cycles, READ-MODIFY-WRITE cycles and LATE-WRITE cycles. The industry standards for DRAM WRITE cycles are fairly consistent for both the EARLY-WRITE and READ-MODIFY-WRITE cycles. An exception exists for the "LATE-WRITE" cycle.

COMMON DQ DRAM

A LATE-WRITE cycle is a READ-MODIFY-WRITE (see Figure 1) except that the READ portion is not utilized. This is accomplished by keeping the output enable pin ($\overline{OE}$) HIGH throughout the cycle. The timing parameters ^{t}RWD, ^{t}AWD and ^{t}CWD no longer apply since $\overline{OE}$ is HIGH.

This condition can be viewed as an EARLY-WRITE with ^{t}WCS "sliding" past the $\overline{CAS}$ time and violating the 0ns setup time (WE going LOW prior to $\overline{CAS}$ going LOW). But, since the output buffers are not being used ($\overline{OE}$ is HIGH), ^{t}WCS and ^{t}CWD are no longer required.

Be cautious anytime $\overline{OE}$ is brought LOW (possibly a noise spike occurs), as the output buffers could turn on and cause contention with the data bus, which could corrupt input data.

The term used for such a WRITE cycle varies throughout the industry. The use of "$\overline{OE}$ controlled WRITE," "Delayed WRITE" and "LATE-WRITE" all signify the same WRITE cycle described above.

SPLIT D AND Q DRAM

A LATE-WRITE cycle is a READ-MODIFY-WRITE except the READ portion is not guaranteed and the D and Q pins are separate paths (D and Q cannot be connected together). This is accomplished by ignoring the timing parameters ^{t}RWD, ^{t}AWD and ^{t}CWD.

This condition can be viewed as an EARLY-WRITE with ^{t}WCS "sliding" past the $\overline{CAS}$ time and violating the 0ns setup time (WE going LOW prior to $\overline{CAS}$ going LOW). But, since the output buffers are a "don't care," ^{t}WCS and ^{t}CWD are no longer required.

This cycle is not available on applications that have the D and Q connected together as the output will contend with the input.

SUMMARY

A LATE-WRITE cycle is most useful on common DQ DRAMs. Use caution to ensure the output enable pin is properly controlled.

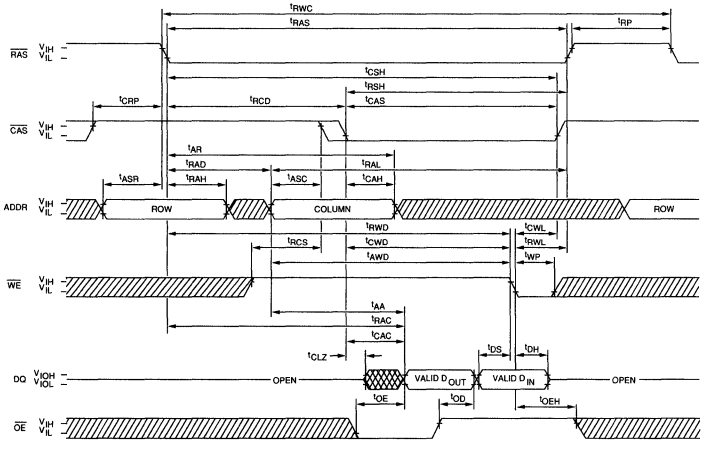


Figure 1
READ-MODIFY-WRITE (MULTIPLE DQ) TIMING

TECHNICAL NOTE

MT43C4257/MT43C4258 COMPARISON

INTRODUCTION

Micron Technology, Inc., offers its Triple Port DRAM (TPDRAM) in two versions. The MT43C4257 supports the JEDEC Split SAM Status Function (QSF) pin as defined for VRAMs. The MT43C4258 supports a variation of the QSF function called the Split SAM Special Function (SSF) input function. Other than this difference, the function and performance of the two devices are identical.

MT43C4257 — QSF OUTPUT

The QSF output pin of the MT43C4257 is identical in function to the QSF pin of the MT42C4255 256K x 4 VRAM. The QSF output pin indicates which half of the SAM is being accessed. When data is accessed from the lower half, the QSF is LOW; when data is accessed from the upper half, QSF is HIGH (see Figure 1). When using the MT43C4257 or any standard VRAM in the split SAM mode, the transition between SAM halves occurs only when the SAM-half boundary is reached by the Address Pointer. This is address count 255 for the lower half and 511 for the upper half. When this boundary is reached, the new Tap Address for the next SAM-half is loaded ("X" for the lower, "Y" for the upper). The following SC will access data from the new half.

MT43C4258 — SSF INPUT

The MT43C4258 introduces functionality to the TPDRAM that is not available on standard VRAMs. By making the "QSF" pin an input (SSF), a higher degree of design flexibility is offered to the system engineer. The SSF applies only to split transfer cycles. It will allow access to be switched from one half of the SAM to the other at will. If SSF is HIGH at the rising edge of serial clock, the split SAM access will be switched to the other half of the SAM (See Figure 2).

By taking SSF HIGH for the rising edge of a serial clock (location "A" for the lower half, "B" for the upper), the access from the current half may be terminated. Data from this clock will appear on the outputs when in serial output mode or will be written if in serial input mode.

The next serial clock will access data at the new Tap Address ("X" for the lower, "Y" for the upper) of the next half. The SSF input acts as a "stop address" input so the

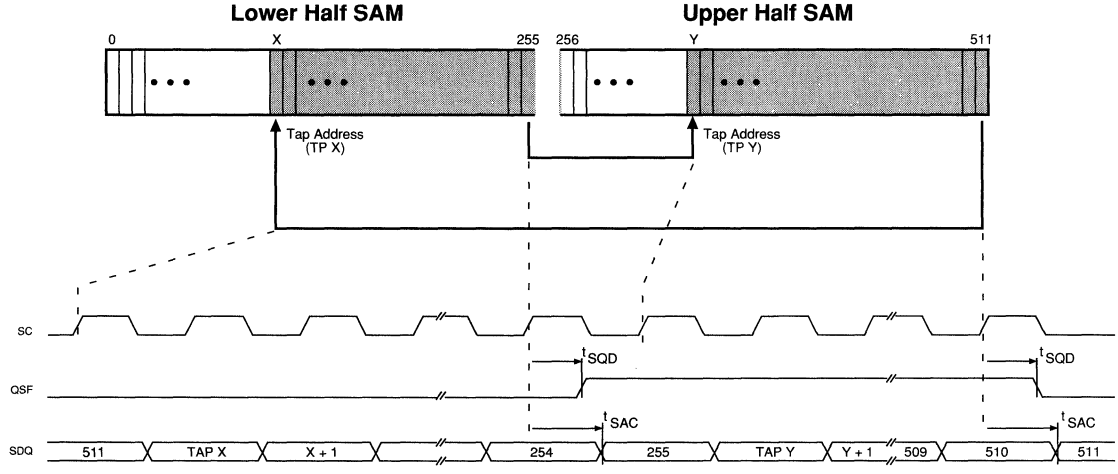


Figure 1
QSF OPERATION FOR THE MT43C4257 (SERIAL OUTPUT)

designer can "force" the access from one half to the next when desired. When operating in the split SAM mode, this option allows different sized "blocks" of data to be input or output from the SAM half regardless of the Tap Address and Stop Point. This feature is useful when performing pans, zooms and scrolling in video-graphics systems and for handling distinct packet sizes in networking or controller applications.

SUMMARY

The difference between the MT43C4257 and MT43C4258 is only the variance in the functionality of the "QSF" pin. The MT43C4258 SSF input pin results in more efficient handling and therefore higher throughput of input or output data in either SAM. This improves the performance of video-graphics and networking systems by providing high clock speed and no latency time between reaching the Stop Point of valid data in one half and the loading of the new Tap Address for the next half.

The SSF functionality is also available on the x8 versions of the TPDRAM, the MT43C8128 (QSF) and MT43C8129 (SSF). Refer to the data sheets for detailed timing and functional descriptions.

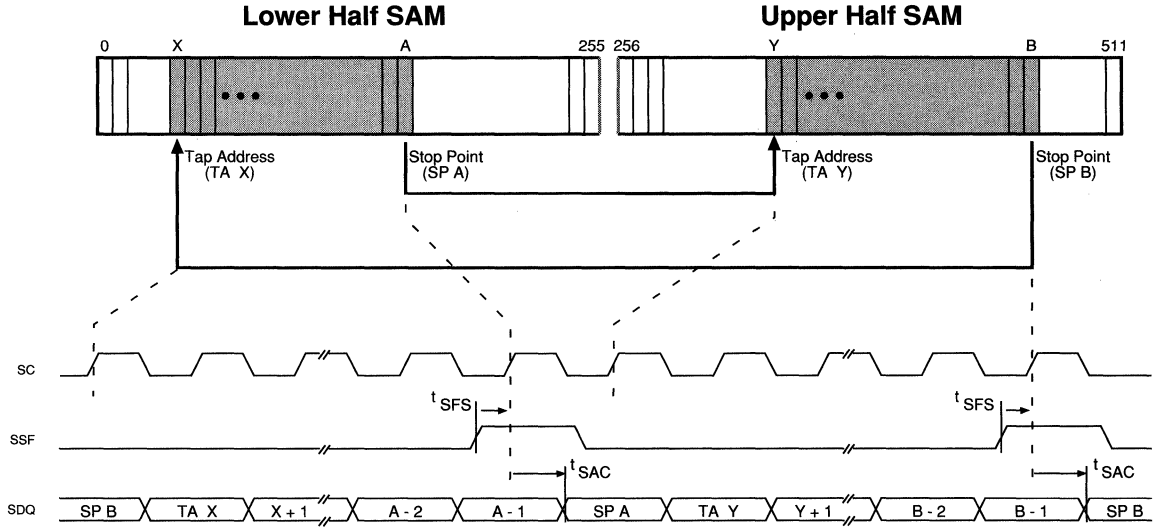


Figure 2
SSF OPERATION FOR THE MT43C4258 (SERIAL OUTPUT)

APPLICATION/TECHNICAL INFORMATION

TECHNICAL NOTE

SRAM BUS CONTENTION DESIGN CONSIDERATIONS

INTRODUCTION

High-speed SRAM memory systems normally share a common data bus with other memory devices, processors and memory management or caching devices. All of these devices are required to control data bus at one time or another. Turning off a device that is driving the bus before a new device takes control of the bus can be a difficult design problem when these systems are operating at minimum cycle times.

When two or more devices are driving the bus at the same time, a conflict known as "bus contention" occurs. This technical note discusses bus contention design issues and points out features in the design of Micron's fast SRAMs to help minimize bus contention problems.

BUS CONTENTION EFFECTS

System-design problems caused by bus contention are difficult to analyze. The effects are transient, normally not longer than 5ns. The most visible result of bus contention is observed as noise on power-supply lines and data lines connecting the contending devices. While these conflicts are not destructive, they potentially reduce long-term system reliability. However, in most cases, they do not affect system performance when all the active components are MOS.

MOS devices are inherently self-current limiting. As the current through a MOS transistor increases, the transistor heats up and its gain decreases. Bipolar transistors have the opposite behavior. When a bipolar transistor's temperature

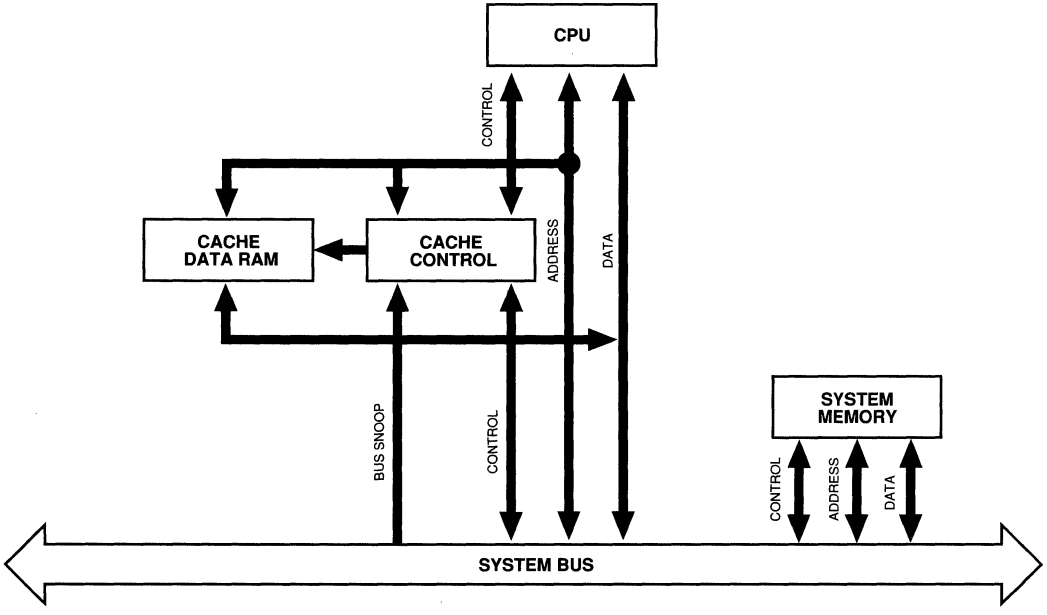


Figure 1
BLOCK DIAGRAM OF A CACHE MEMORY SYSTEM

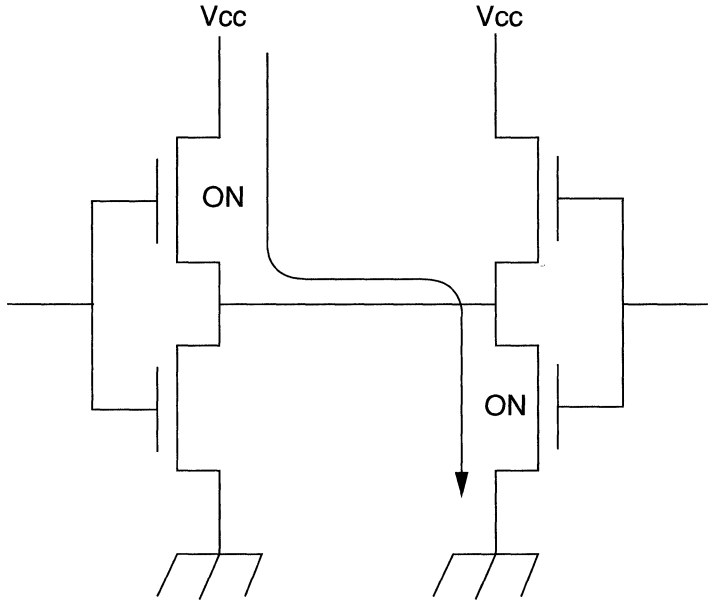


Figure 2
BUS CONTENTION CURRENT PATH

is elevated, the gain of the device increases, making it possible for the current through the transistor to increase to a destructive level. This phenomenon is known as thermal runaway. If CMOS SRAMs share any data lines with bipolar or BiCMOS output devices, the system should be designed to eliminate any possibility of bus contention.

Figure 2 is a schematic diagram of two contending SRAM output buffers. A high current path has been created by two SRAM output buffers. The current is flowing between the "on" transistor connected to Vcc in the buffer on the left and the transistor connected to ground in the buffer on the right.

SRAM SPECIFICATIONS

The critical parameters for calculating the amount of bus contention for a high-speed SRAM system design is the time it takes for a device to go to a low-impedance state (logic 1 or 0) on its output versus the time required for a contending output to go to a high-impedance state. A typical SRAM has three control signals; chip enable (CE), write enable (WE) and output enable (OE). ^{t}LZCE, ^{t}LZWE and ^{t}LZOE are the times it takes for the outputs to become active or low impedance upon the assertion of CE, WE and OE. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are the times required for the outputs to become inactive or high impedance after CE, WE and OE are removed. These times are shown in the READ and WRITE cycle timing diagram (Figure 3).

A preliminary review of a fast SRAM data sheet would imply that the worst case for bus contention could be calculated from the equation:

$$^{t}C = {}^{t}HZ\ (MAX) - {}^{t}LZ\ (MIN)$$

where ^{t}C is equal to the bus-contention overlap time. For an output enable change in an SRAM rated at 20ns access time, ^{t}HZ = 7ns and ^{t}LZ = 2ns; therefore ^{t}C = 5ns. If this calculation is correct, there would be a serious bus contention problem. Thus, for a system running with a 20ns cycle, almost 25 percent of the total cycle would be lost to bus contention and there would be a large increase in power dissipation in the output buffers.

Happily, the previous analysis is not valid because ^{t}HZ maximum occurs at completely different test conditions than ^{t}LZ minimum. ^{t}HZ maximum is worst-case at the highest operating temperature and the lowest power-supply voltage. On a commercial data sheet, this would be at 70° C and 4.5V. ^{t}LZ minimum is specified at the lowest operating

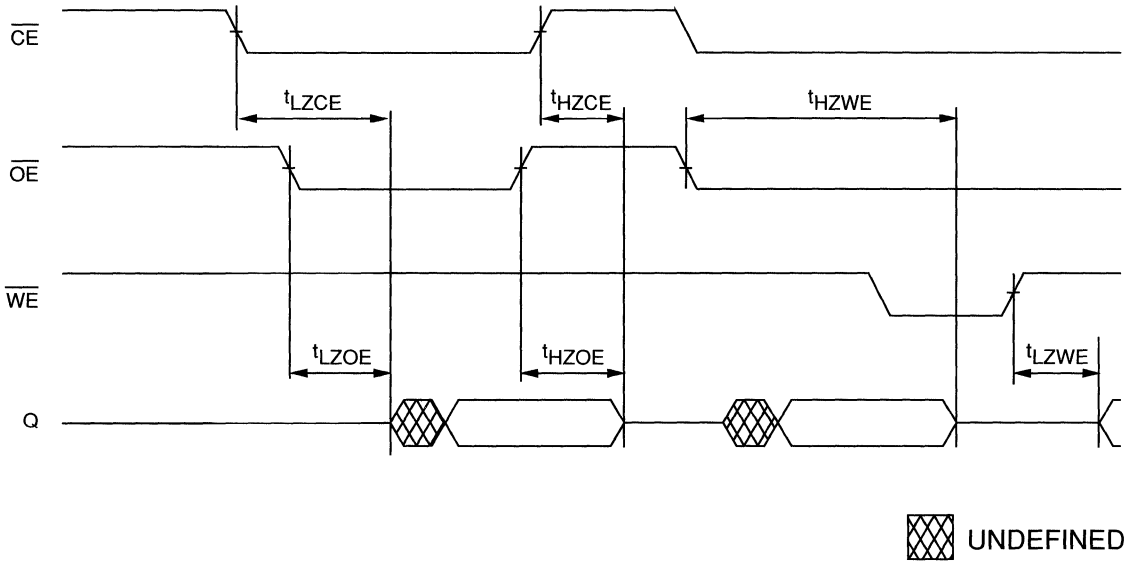


Figure 3
READ AND WRITE CYCLE TIMING

temperature and the highest voltage. Again, on the commercial data sheet, this would be 0° C and 5.5V. It is not possible for two SRAMs on the same board to be at such diverse temperatures and voltages. In a "real world" system — that is one with an equal operating environment for temperature and power supply voltage — $^{t}HZ - {}^{t}LZ$ is approximately 0.2ns.

Futhermore, Micron fast SRAMs have been designed to insure the outputs always turn off faster than the they turn on when operating at the same voltage and temperature: $^{t}HZ < {}^{t}LZ$. Since the devices will normally be mounted on the same board, the bus contention associated with the SRAM control signals has been minimized.

Care must be taken when mutiple vendors' SRAMs share the bus. An analysis of the output turn-off time must be done under the same operating and temperature conditions to insure that bus contention between the devices is minimized.

TECHNICAL NOTE

SRAM CAPACITIVE LOADING

INTRODUCTION

Many high-speed 16-bit and 32-bit microprocessor systems require fast SRAMs. SRAMs are used either in main memory or caching subsystems. In either case, the SRAMs are typically required to interface with a system bus that is shared by one or more microprocessors, several I/O devices and other types of memory (i.e. ROM, EPROM, etc.).

Even though transceivers and/or buffers interface with the actual bus, SRAMs are typically required to drive loads larger than what is specified in the data sheet timing parameters. Hence, the access time must be derated to reflect the actual performance of the SRAM under these circumstances.

SIMILARITY BETWEEN SRAM FAMILIES

Micron's 16K, 64K, 256K and 1 Meg SRAM families all have the same size output transistors and output architecture. Hence, all devices will have the same drive characteristics. The actual data presented in this technical note are derived from the 256K SRAM family.

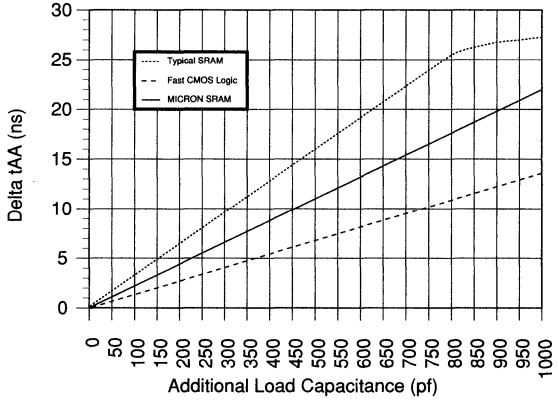


Figure 1
INCREASED ACCESS TIME vs ADDITIONAL OUTPUT LOADING

COMPARISON OF DEVICES

Figure 1 compares the effects of capacitive loading on the Micron SRAM family with SRAMs from a typical memory supplier and discrete CMOS logic, designed to drive heavy loads. The graph illustrates the additional access time required to drive various capacitive loads.

As expected, the Micron SRAM family does not drive heavy loads as well as the discrete CMOS logic, but does drive faster than the typical SRAM from other suppliers.

The graph line which represents the Micron SRAM family is based on data gathered on the Micron 256K SRAM. Access time measurements were taken with the SRAM subjected to various capacitive loads. In the range covered, the change in access time was seen to be a linear function of the capacitive load. The following equation may be used to determine the access time required for a specific load.

$$T_{AA}(\text{actual}) = T_{AA}(\text{data sheet}) + T_{AA}(\text{additional})$$

$$T_{AA}(\text{additional})\ (\text{ns}) = .022\ (\text{ns/pf})\ C_a$$

This applies where C_a is the additional capacitive load expressed in picofarads (pf).

For example, the access time needed for a 100pf total capacitive load is:

T_{AA}(actual) = 20ns + T_{AA}(additional) =
20ns + .022 * (total load - rated load) =
20ns + .022ns/pf * (100pf - 30pf) =
20ns + 1.5ns = 21.5ns

SUMMARY

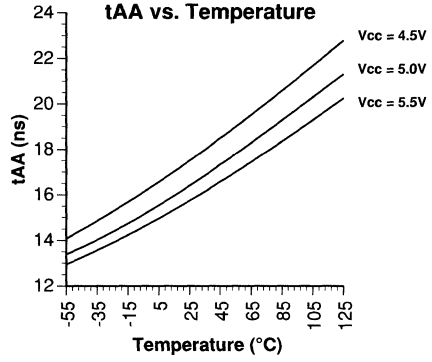
The SRAM timing specifications of all major vendors are based upon an industry-standard capacitive load of 30pf. In most applications, the SRAMs are required to drive much larger capacitive loads. In addition, today's designs are implemented around higher frequencies. This requires the system timing be more precise; hence, loading becomes a more important issue. Understanding how the SRAM will perform under specific loading conditions may result in a more reliable design.

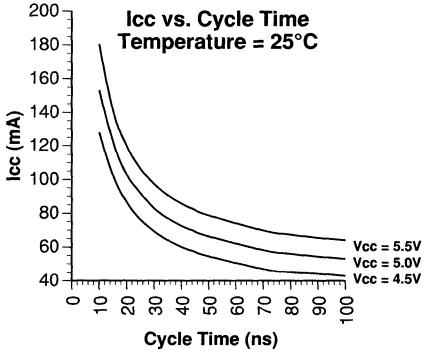
TECHNICAL NOTE

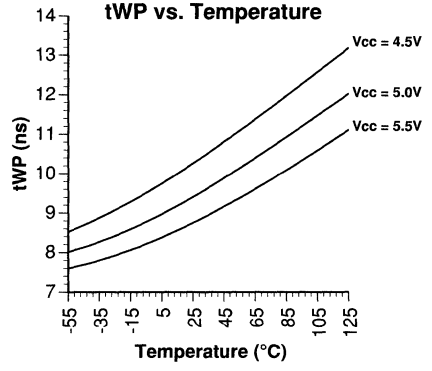
1 MEG FAST SRAM TYPICAL OPERATING CURVES

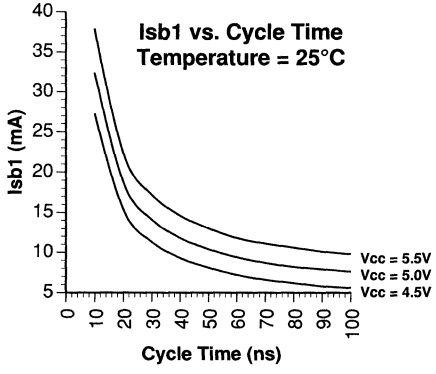
INTRODUCTION

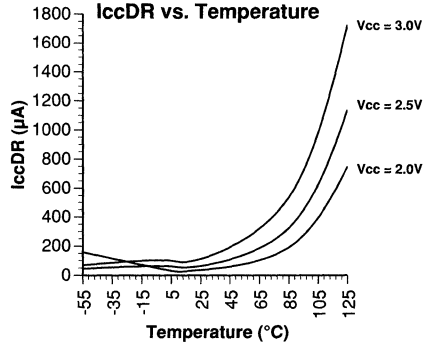
These curves represent the typical operating characteristics of Micron's 1 Meg, 25ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of the data book.

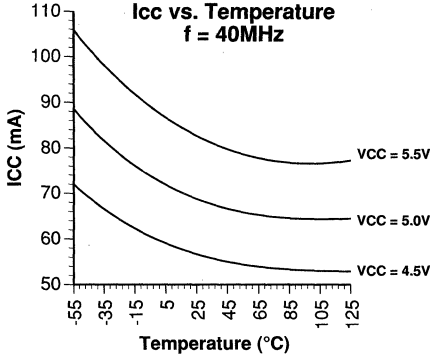


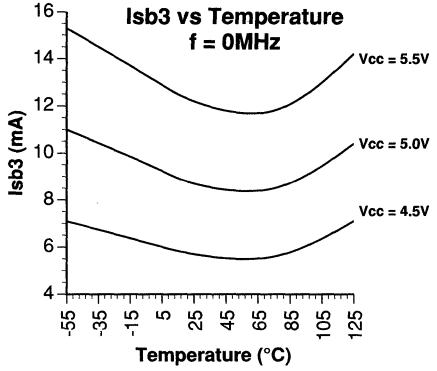


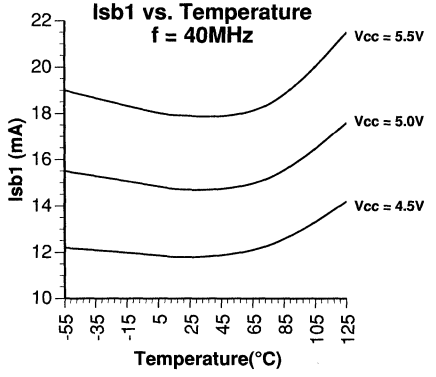


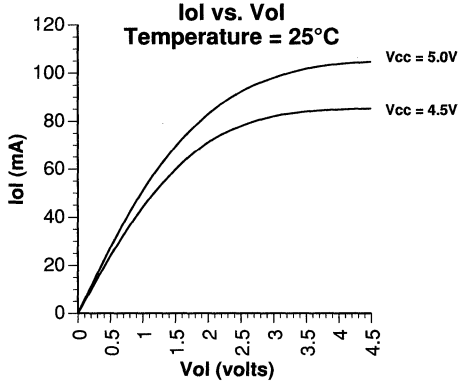


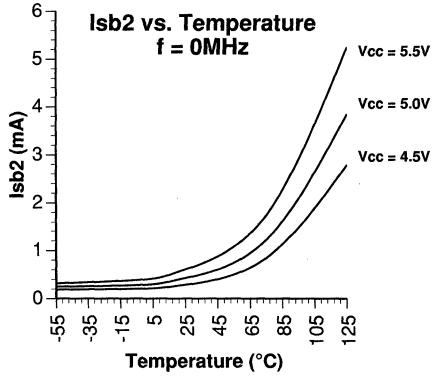


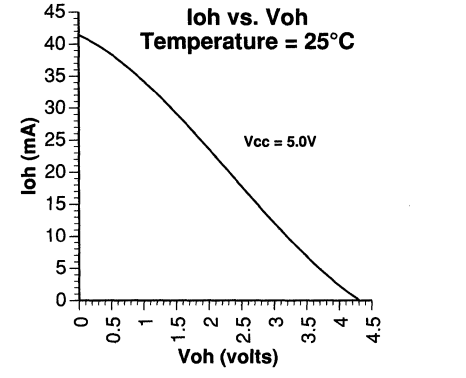

Icc vs. Temperature
f = 40MHz
ICC (mA)
110
100
90
80
70
60
50
VCC = 5.5V
VCC = 5.0V
VCC = 4.5V
-55 -35 -15 5 25 45 65 85 105 125
Temperature (°C)


Isb3 vs Temperature
f = 0MHz
Isb3 (mA)
16
14
12
10
8
6
4
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
-55 -35 -15 5 25 45 65 85 105 125
Temperature (°C)


Isb1 vs. Temperature
f = 40MHz
Isb1 (mA)
22
20
18
16
14
12
10
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
-55 -35 -15 5 25 45 65 85 105 125
Temperature(°C)


Iol vs. Vol
Temperature = 25°C
Iol (mA)
120
100
80
60
40
20
0
Vcc = 5.0V
Vcc = 4.5V
0 0.5 1 1.5 2 2.5 3 3.5 4 4.5
Vol (volts)


Isb2 vs. Temperature
f = 0MHz
Isb2 (mA)
6
5
4
3
2
1
0
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
-55 -35 -15 5 25 45 65 85 105 125
Temperature (°C)

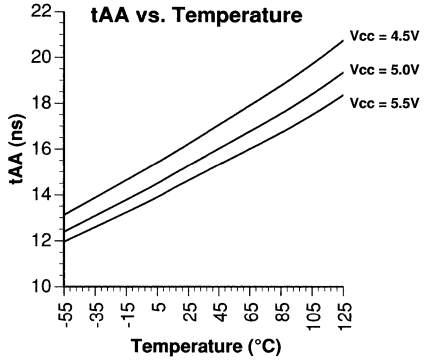

Ioh vs. Voh
Temperature = 25°C
Ioh (mA)
45
40
35
30
25
20
15
10
5
0
Vcc = 5.0V
0 0.5 1 1.5 2 2.5 3 3.5 4 4.5
Voh (volts)

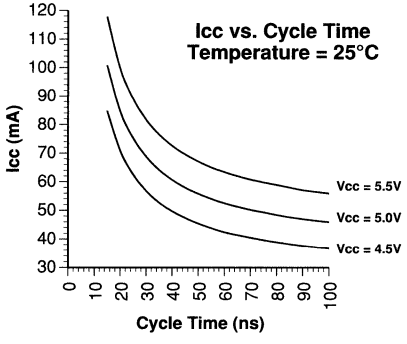
TECHNICAL NOTE

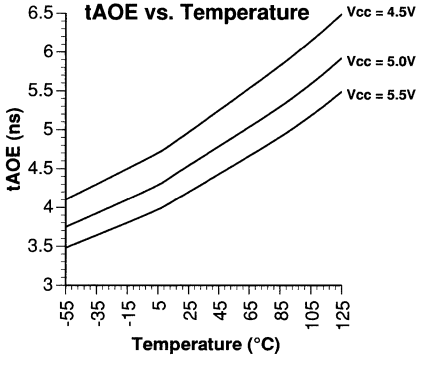
256K FAST SRAM TYPICAL OPERATING CURVES

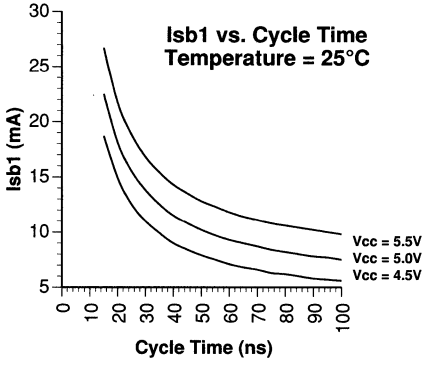
INTRODUCTION

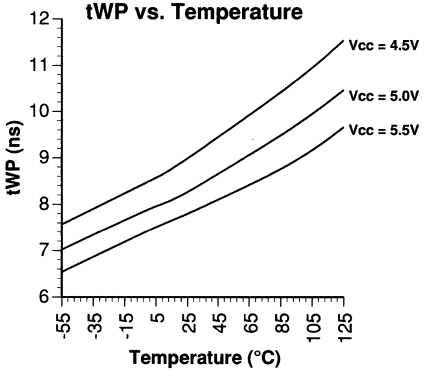
These curves represent the typical operating characteristics of Micron's 256K, 20ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of the data book.

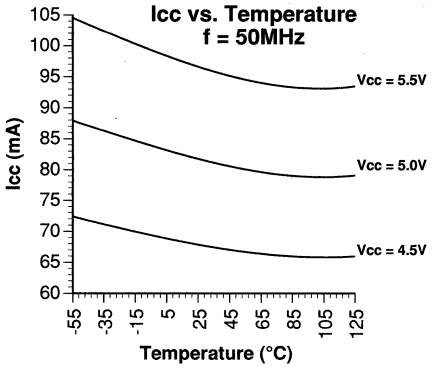


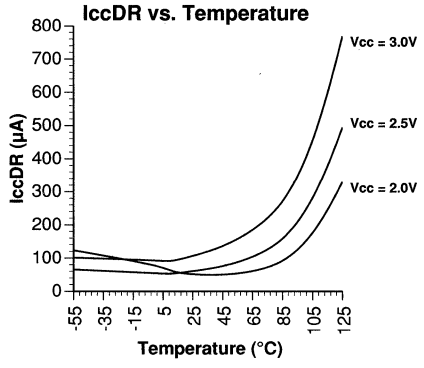


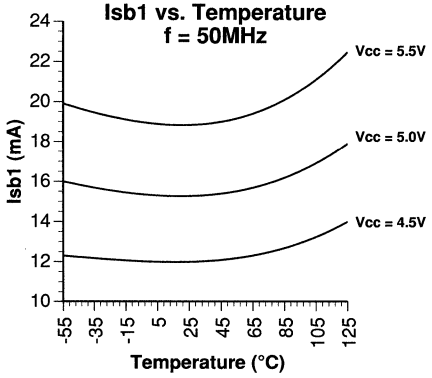


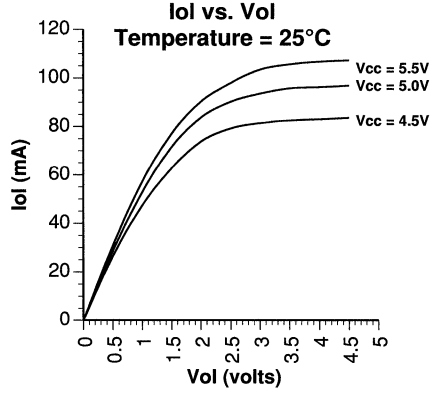


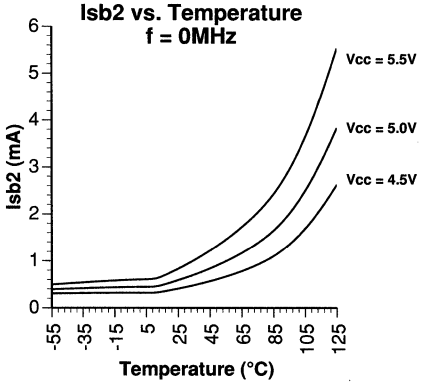


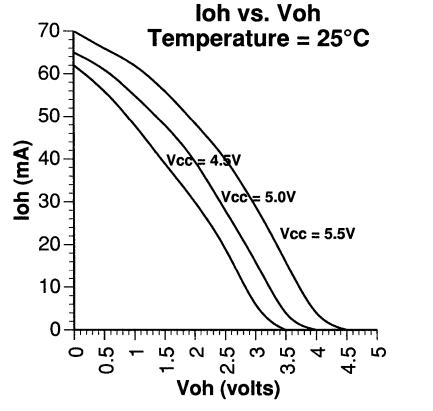

Icc vs. Temperature
f = 50MHz
Icc (mA)
105
100
95
90
85
80
75
70
65
60
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
-55 -35 -15 5 25 45 65 85 105 125
Temperature (°C)


IccDR vs. Temperature
IccDR (µA)
800
700
600
500
400
300
200
100
0
Vcc = 3.0V
Vcc = 2.5V
Vcc = 2.0V
-55 -35 -15 5 25 45 65 85 105 125
Temperature (°C)


Isb1 vs. Temperature
f = 50MHz
Isb1 (mA)
24
22
20
18
16
14
12
10
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
-55 -35 -15 5 25 45 65 85 105 125
Temperature (°C)


Iol vs. Vol
Temperature = 25°C
Iol (mA)
120
100
80
60
40
20
0
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
0 0.5 1 1.5 2 2.5 3 3.5 4 4.5 5
Vol (volts)


Isb2 vs. Temperature
f = 0MHz
Isb2 (mA)
6
5
4
3
2
1
0
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V
-55 -35 -15 5 25 45 65 85 105 125
Temperature (°C)

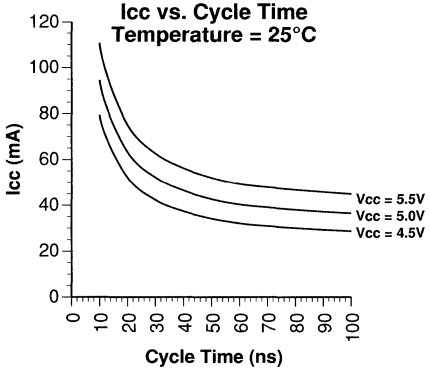

Ioh vs. Voh
Temperature = 25°C
Ioh (mA)
70
60
50
40
30
20
10
0
Vcc = 4.5V
Vcc = 5.0V
Vcc = 5.5V
0 0.5 1 1.5 2 2.5 3 3.5 4 4.5 5
Voh (volts)

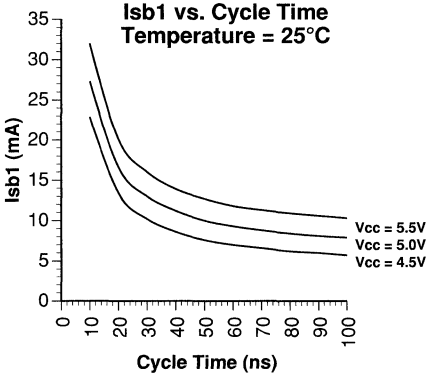
TECHNICAL NOTE

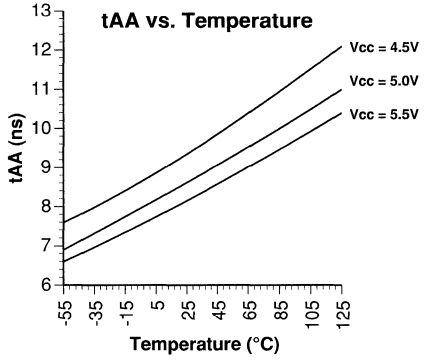
64K FAST SRAM TYPICAL OPERATING CURVES

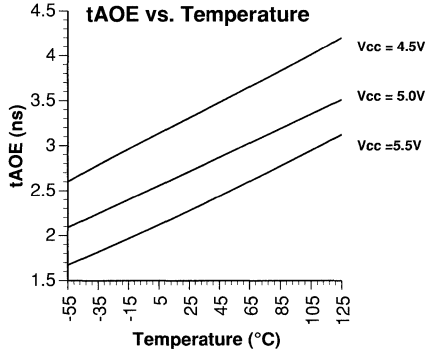
INTRODUCTION

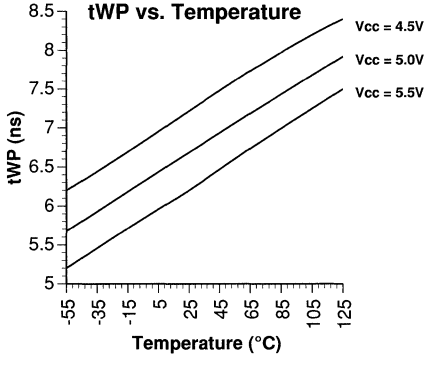
These curves represent the typical operating characteristics of Micron's 64K, 12ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of the data book.

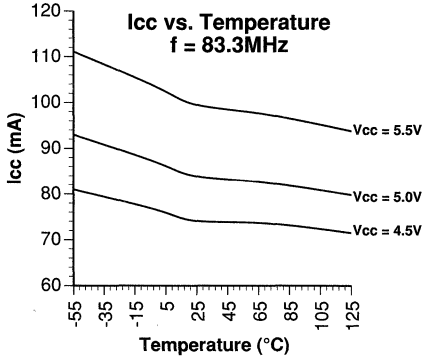


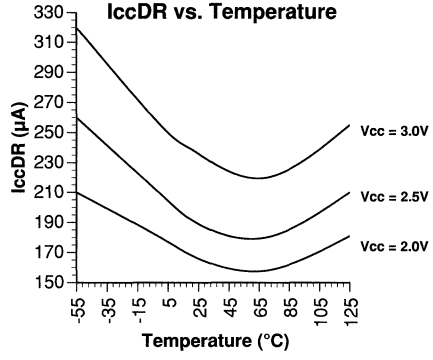


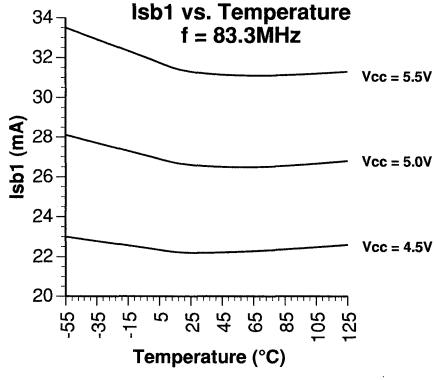


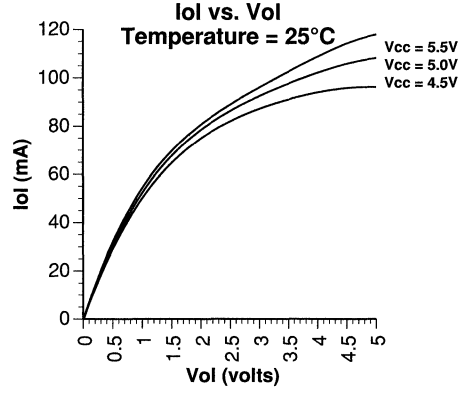


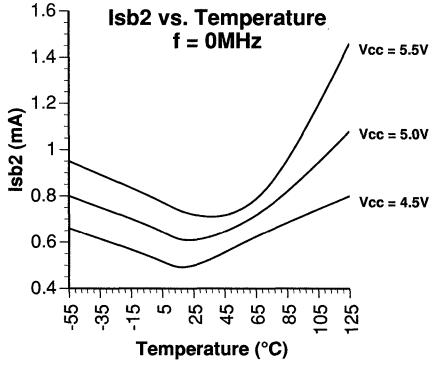


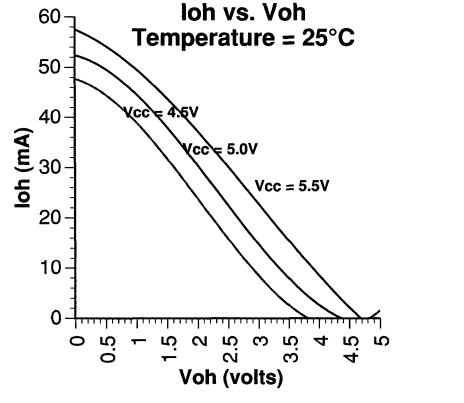

Icc vs. Temperature
f = 83.3MHz
Icc (mA)
120
110
100
90
80
70
60
-55 -35 -15 5 25 45 65 85 105 125
Temperature (°C)
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V


IccDR vs. Temperature
IccDR (µA)
330
310
290
270
250
230
210
190
170
150
-55 -35 -15 5 25 45 65 85 105 125
Temperature (°C)
Vcc = 3.0V
Vcc = 2.5V
Vcc = 2.0V


Isb1 vs. Temperature
f = 83.3MHz
Isb1 (mA)
34
32
30
28
26
24
22
20
-55 -35 -15 5 25 45 65 85 105 125
Temperature (°C)
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V


Iol vs. Vol
Temperature = 25°C
Iol (mA)
120
100
80
60
40
20
0
0 0.5 1 1.5 2 2.5 3 3.5 4 4.5 5
Vol (volts)
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V


Isb2 vs. Temperature
f = 0MHz
Isb2 (mA)
1.6
1.4
1.2
1
0.8
0.6
0.4
-55 -35 -15 5 25 45 65 85 105 125
Temperature (°C)
Vcc = 5.5V
Vcc = 5.0V
Vcc = 4.5V


Ioh vs. Voh
Temperature = 25°C
Ioh (mA)
60
50
40
30
20
10
0
0 0.5 1 1.5 2 2.5 3 3.5 4 4.5 5
Voh (volts)
Vcc = 4.5V
Vcc = 5.0V
Vcc = 5.5V

APPLICATION NOTE

MT56C0816 CACHE DATA SRAM FAMILY

INTRODUCTION

The Micron MT56C0816 Cache Data SRAM family was developed in response to a need for compact cache subsystems for the Intel™ 80386 microprocessor. Applications using the 80386 demand maximum performance, and DRAM technology cannot meet the fast access times required for zero-wait-state operation. Statistics show that a small cache subsystem allows the majority of 80386 memory accesses to be completed within the 80386 cycle time. This eliminates the need for wait states[1] to be added to the memory cycle, allowing the 80386 to operate at its maximum performance level. The cache can be designed using fast commodity SRAMs.

However, the Micron Cache Data SRAM allows cache subsystem designs requiring less space, using less power and offering greater reliability than the fast SRAM implementation. Design and debug times are also reduced, because the Micron MT56C0816 is designed to connect directly to off-the-shelf 80386 cache controllers.

This application note explores why caching is needed. It then discusses how a cache subsystem works, what influences the performance of the cache, and how different cache organizations and architectures compare.

In addition, this application note looks at the most popular off-the-shelf controllers available to implement a cache subsystem. It compares several fast SRAM and cache data SRAM implementations with those controllers. Finally, a summary of the cache data SRAM advantages is shown.

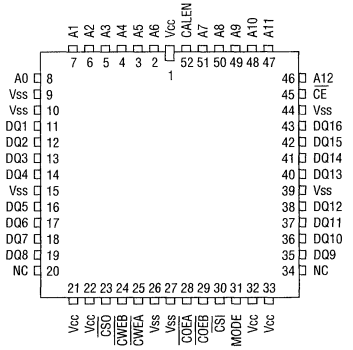
BACKGROUND

Microprocessors have typically interfaced directly to DRAM (dynamic random-access memory) main memory due to their relatively slow clock speeds and multiple clock instruction cycles. But over the past few years, complex-instruction-set computer (CISC) microprocessors have driven the clock frequencies into the 20, 25 and 33 megahertz (MHz) range. The two most dominant CISC architectures are the 80X86 and 680X0. The number of clock cycles needed to execute a specific instruction has steadily decreased and is now approaching a single clock cycle for many instructions.

The introduction of reduced-instruction-set computer (RISC) architectures has fueled the quest for higher clock frequencies and reduced clock cycles for each instruction executed. Some of the predominant RISC architectures include SPARC™, 80960, R3000, 29000 and 88000. RISC

MT56C0816
PIN ASSIGNMENT (Top View)

52-Pin PLCC
52-Pin PQFP



architectures requiring the absolute minimum number of clock cycles for each instruction are not only approaching single clock execution, but in some cases are able to sustain multiple instruction execution in a single clock cycle. CISC microprocessors are not far behind, and the competition between the CISC and RISC camps is driving processor designers to continuously reach for maximum performance.

This new era of performance is placing heavy demands on memory subsystems that heretofore have been able to

[1] Wait states are one or more additional processor clock cycles added to the memory access cycle. These extra clock cycles keep the processor idling while memory has time to respond to the memory request. For a given processor's clock speed, the number of wait states needed to complete a memory access is directly related to how fast the memory can respond to a read or write request initiated by the microprocessor.

For example, the 80386 can complete a memory cycle in two clock periods. With a 25MHz processor, this allows 80ns for the processor to output its address to the memory array. It also provides time for the decode circuitry to supply the necessary signals to the memory and enables the memory to respond once it has received the necessary signals. In typical applications, the speed of the memory array that is needed to avoid any wait states is 35ns.

keep pace. For example, an 80386 processor operating at 25 MHz requires a memory access time of close to 40ns if it is to operate at maximum performance (i.e. no wait states):

2 x clock cycle time - address delay - data setup - decode logic and buffer delay = (2 * 40) - 21 - 7 - 10 = 42ns

Current DRAM access speeds are in the 70ns to 80ns access range. Even with faster access techniques such as FAST PAGE and STATIC COLUMN modes, the DRAM access time is not sufficient to meet zero-wait-state access times.

The alternative to adding wait states to the system and thus degrading performance is to design a system architecture that makes the memory appear faster to the CPU. Approaches that have been implemented include organizing the DRAM in multiple banks, adding some fast SRAM for specific code and data or caching.

The use of a cache is applicable in high-end systems as well as cost-conscious, medium-performance systems. At the high end, where the goal is to maximize performance on every processor cycle, the only alternative to cache is the use of very fast SRAMs as the main memory to achieve zero-wait-state performance. This is a very expensive solution. The medium performance systems must constantly balance performance and cost. A small cache in these systems can achieve much higher performance with a relatively small, incremental cost.

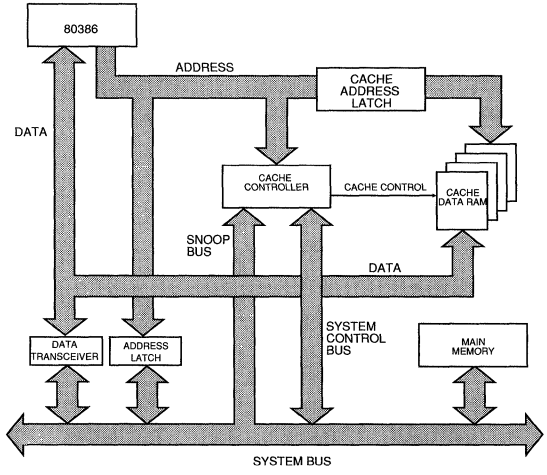


Figure 1
TYPICAL 80386-BASED CACHE SYSTEM

CACHE OVERVIEW

WHAT IS A CACHE

A cache is small, fast, local storage for frequently accessed code and data. It consists of high-speed memory (usually SRAM) that resides between the CPU and the main memory (usually DRAM) in a processor system. Figure 1 illustrates a typical block diagram of an 80386-based cache system.

The cache increases the effective speed of the main memory by responding quickly with a copy of the most frequently used items in main memory. The cache control logic checks the address of each memory access and, if it is present in the cache, allows the cache to respond instead of main memory. Accesses to the cache are much faster (typically zero wait states) than accesses to main memory. The more accesses that are made to the cache, the better the overall system performance. Hence the goal in designing a cache is to maximize accesses to the cache (known as the cache hit rate).

WHY A CACHE WORKS

The theory of a cache is based on two attributes of computer programs: temporal locality and spacial locality. Temporal locality (locality of time) is an attribute exhibited by computer programs where the same addressed code and data are used repeatedly in a short time. This behavior is typified by program loops, a very prevalent programming structure. Spacial locality (locality of place) is a computer program attribute in which the next needed information is found near the information that was just accessed. This occurs in most programs since related data are stored together (data tables, arrays, etc.) and instructions (code) are typically executed in sequence.

In a cache design, main memory may be thought of as a collection of many small, uniform segments. The cache contains a copy of one or more of these small memory segments that have been used recently. When the processor executes a read from main memory, the cache control determines if that address is contained in one of the small memory segments that are currently resident in the cache memory. If so, the access is completed by the cache. If not, the access is completed by main memory and the memory segment that has just been accessed is placed into the cache for future use. The attribute of spacial locality implies that the information needed next will also be found in the same memory segment just accessed, which is now located in the cache. The attribute of temporal locality implies that the memory location, just accessed, will be used again in the near future.

PERFORMANCE FACTORS

The performance of the cache (and hence the system) is measured by the cache hit rate, which is the percentage of successful cache accesses. The cache hit rate is determined by specific demands of software being executed and by cache-management policies.

The design factors that influence cache hit rate are: total cache memory size, cache memory organization (associativity), and cache transfer block size. These factors are all interrelated and each needs attention to obtain the optimum cost-effective result. Each factor presents trade-offs of performance, complexity and cost. One factor may be decreased for cost reasons while another may be increased to improve performance. The same or better hit rate may still be obtained. However, the complexity might be increased also. The cache designer must carefully weigh each factor to achieve the best overall cost/performance/complexity ratio. Table 1 compares the cache hit rate of several cache sizes with varying associativity and line sizes.

Table 1

CACHE HIT RATES			
Cache Configuration			
Hit Rate (%)*	Size (KB)	Associativity	Line Size (Bytes)
41	1	Direct	4
73	8	Direct	4
81	16	Direct	4
86	32	Direct	4
87	32	Two-way	4
88	64	Direct	4
89	64	Two-way	4
89	64	Four-way	4
89	128	Direct	4
89	128	Two-way	4
91	32	Direct	8
92	64	Direct	8
93	64	Two-way	8
93	128	Direct	8

* Rounded to the nearest whole percent.

COHERENCY

Since the cache is a temporary buffer for a section of main memory, the cache designer must take into consideration how to keep the data consistent between main memory and the cache. This is called cache coherency.

There are instances when an address in the cache might not contain the same information as the same address in main memory. One such situation occurs during a write cycle, where a cache data element is updated to a new value. Now the address in main memory and the same address in the cache have two different values, with the cache containing the newest value. The main memory needs to be updated to contain the same information. This is controlled by the write policy of the cache.

Another such instance occurs when another processor writes information to a main memory address that is also located in the cache. This situation is handled by "snooping". Snooping occurs when the main memory bus is always watched by the cache logic. If a write occurs to a main memory address identical to a cached address, that cache address is marked invalid. This guarantees that if that address is accessed, it will be updated as main memory is accessed for the requested data.

There are two types of cache write policies: write-through and copy-back. A write-through cache will write to both main memory and the cache on each write cycle whenever the addressed location is found to be resident in the cache. This ensures that the cache and main memory are always coherent, but it requires more main memory accesses, thus increasing bus usage. This also decreases performance due to the large amount of accesses to slower main memory. The main memory accesses may be made more efficient with the addition of write buffers, but this also adds significant complexity and coherency problems in the buffers.

The copy-back policy writes only to the cache, if the address location is present (cache hit), and allows the CPU to proceed. This allows maximum system performance. However, the main memory still needs to be updated. The update of main memory occurs when the line that contains the write address in the cache is replaced by a new line. Main memory write updates occur far less often than the update policy of a write-through design. The copy-back policy also has its drawbacks. Instead of only replacing the data element (possibly one byte) that was written, all the bytes in the line are replaced. This may be as many as four, eight, 16 or more. This can result in a large time penalty when a copy-back occurs.

CACHE CONTROLLERS

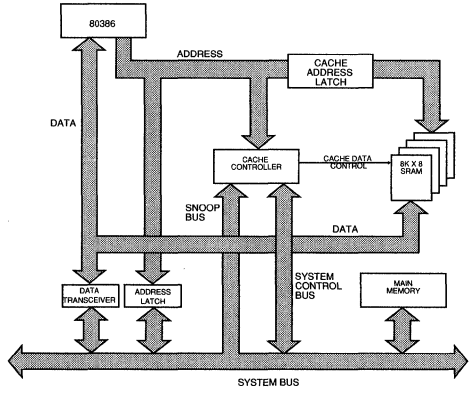
It quickly becomes apparent that all variables in cache design are interrelated and all have trade-offs. For most designs, especially those in the micro arena, caching represents a new realm and can bog down a design if done from scratch. Fortunately, several companies have designed off-the-shelf cache controllers, which take into consideration all the trade-offs and performance factors. These controller implementations meet the majority of the needs of the 80386 cache market.

The three most popular 80386 cache controllers — Intel's 82385, Austek's A38202 and Chips & Technologies' 82C307 and Peak™ — were designed to interface with standard SRAMs as well as additional address latches and possible transceivers.

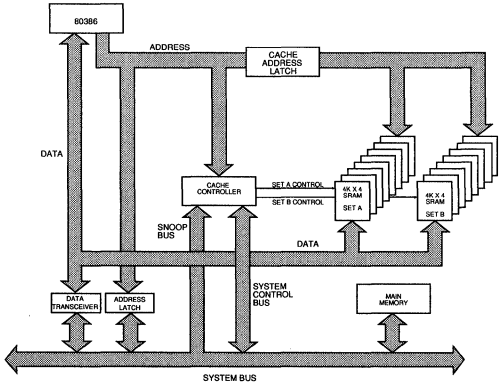
DIRECT-MAPPED VERSUS TWO-WAY-SET IMPLEMENTATION

The use of an off-the-shelf cache controller eliminates most of the decisions that would occur in a discrete design. The trade-offs that have been made include line size, write update policy, and in some cases, even the cache size and associativity. The majority of controllers allow the user to configure only the associativity (direct or two-way set) and the cache size. The controllers support, without additional logic, both the TWO-WAY-SET ASSOCIATIVE and DIRECT-MAPPED modes.

The trade-off between DIRECT-MAPPED and TWO-WAY-SET ASSOCIATIVE modes is typically one of increased hit rate versus added complexity. Since the controllers have integrated the complexity, it might seem that the only logical choice is to use the TWO-WAY-SET ASSOCIATIVE mode. Assuming a 32 kilobyte (KB) cache, the direct mode will require four 8K x 8 SRAMs (one bank of 8K x 32 bits) while two-way mode will require 16 4K x 4 SRAMs (two banks of 4K x 32 bits). Figure 2 contains typical block diagrams illustrating implementations of DIRECT-MAPPED and two-way-set designs.



DIRECT-MAPPED BLOCK DIAGRAM



TWO-WAY-SET BLOCK DIAGRAM

Figure 2

The trade-off then is in the additional SRAMs for two-way set. This is reflected as incremental cost, power and board space needed to achieve the higher hit rate obtained over the direct-mapped implementation. For the 32KB cache size, the additional hit rate of the two-way set implementation is generally chosen if the board space is available. In the medium-to-high-end performance market, the extra performance (see Table 1) delivered by the two-way set design is worth the extra cost.

Table 2 compares the board real estate and power requirements of each configuration. The two-way-set implementation requires eight 74F245 transceivers to control the flow of data between each bank and the common data bus. Figure 3 illustrates the board space requirements of each implementation.

The assumptions used for the board space comparison were .050 inch chip-to-chip spacing and .050 inch outside border around the circuitry. The power comparison is based on a 25MHz design assuming 10ns decoding delay. This gives the following equation for the cache 8K x 8 SRAM access time:

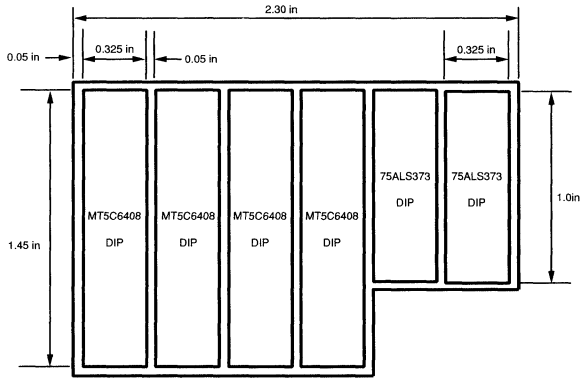
Cache SRAM available access time = 4 * 386CLK2 - 386 address delay - 386 ready setup - SRAM enable decode - 74F373 delay = (4 * 20ns) - 21ns - 9ns - 10ns - 9ns = 31ns.

The 8K x 8 configuration would require SRAMs with an access time of 25ns. For the two-way-set configuration, an additional 6ns must be subtracted for the delay through the 74F245 transceivers. This barely provides 25ns for the 4K x 4 SRAM access time in this latter implementation. Any other delays that exist in the data access path must also be taken into consideration. In the case of the 4K x 4 SRAMs, a 20ns part will probably be required.

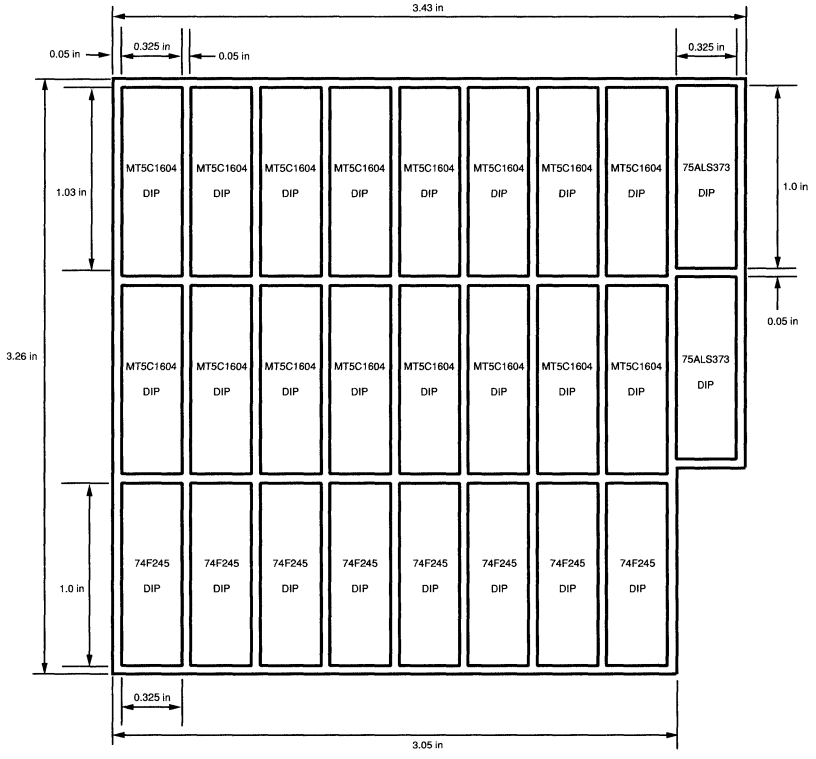
Table 2

32KB CACHE CONFIGURATION COMPARISON				
Configuration	**SRAM**	**# SRAMs**	**Area (in²)**	**Power (W)**
Direct-Mapped	8K x 8	4	3.23	2.75
Two-Way-Set	4K x 4	16	10.57	10.55*

* The 4K x 4 configuration incorporates two banks of eight SRAMs each. One bank is active while the other is in standby mode. This fact was used in the power calculations.



DIRECT-MAPPED SPACE REQUIREMENT USING 8K x 8 SRAMS



TWO-WAY-SET SPACE REQUIREMENT USING 4K x 4 SRAMS

Figure 3

MT56C0816 INTEGRATED CACHE SRAM

The MT56C0816 is an application-specific 8K x 16 SRAM designed for, but not limited to, cache data SRAM implementations. The MT56C0816 is designed to be used in either direct-mapped or two-way-set designs. It incorporates an on-chip address latch, on-chip multiplexing between the two SRAM banks (for two-way-set mode), fast output enable times, and low-power consumption.

Almost all designs have used the MT56C0816 in the two-way-set mode of operation. This is due to the fact that the MT56C0816 eliminates the major problems in implementing the two-way-set mode architecture, namely the cost, space and power. Before the MT56C0816, a two-way-set implementation required three times the board space and four times the power of a direct-mode design when using standard SRAMs.

Due to the integration of on-chip address latches and multiplexors, often a lower-speed MT56C0816 can be used in place of a higher-speed, more costly standard SRAM. The advantages of the MT56C0816 don't stop here. It is widely second-sourced by other suppliers, the access time has been reduced to 20ns and it is available in the smaller PQFP package.

Table 3 compares the board space, power and access time requirements of standard SRAMs and both packages of the MT56C0816 in a 32KB cache design. The numbers presented are applicable to both direct-mapped and two-way-set implementations for the MT56C0816 and 4K x 4 SRAMs. The use of 8K x 8 SRAMs in a two-way configuration requires a minimum of 64KB in the cache and are not considered in the comparison. The same board area assumptions are used in Table 3 as in Table 2 regarding chip-to-chip and circuitry border spacing. The area values are normalized to the MT56C0816 in the PQFP package.

Table 3

Cache SRAM Comparison (33MHz)				
Device	**Number of Devices**	**PC Board Area**	**Power (w)**	**Access Speed (ns) Required**
MT56C0816 PQFP	2	1.00	2.2	25
MT56C0816 PLCC	2	1.94	2.2	25
8K x 8 SOJ 74F373 SOIC	4 2	2.28	3.15	15
8K x 8 DIP 74F373 DIP	4 2	3.99	3.15	15
4K x 4 SOJ 74F373 SOIC 74F245 SOIC	16 2 8	8.58	12.15*	12
4K x 4 DIP 74F373 DIP 74F245 DIP	16 2 8	13.05	12.15*	12

* The 4K x 4 configuration incorporates two banks of eight SRAMs each. One bank is active while the other is in standby mode. This fact was used in the power calculations.

The SRAM access time and power considerations are based on a 33 MHz 80386 design assuming a 10ns enable decode time. The cache SRAM access time equation is as follows:

Cache SRAM access time = 4 * 386CLK2 - 386 address delay - 386 ready setup - SRAM enable decode - 74F373 delay = (4 * 15ns) - 15ns - 7ns - 10ns - 9ns = 19ns

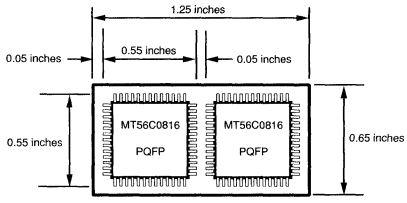
This will require 8K x 8 SRAMs with a 15ns access time. The 4K x 4 implementation requires that the transceiver delay time (6ns) also be subtracted, which leaves only 13ns. Hence, a 12ns part must be used. The MT56C0816 incorporates the address latch on-board and thus allows 9ns to be added back into the SRAM access time. This yields a 28ns access time for a MT56C0816 design, which is easily met by the 25ns part. This access time is applicable to both the direct mode and two-way set configurations since the data multiplexing is also on-chip.

Figures 4 and 5 illustrate the board space required by the MT56C0816 and the standard SRAM configurations that are summarized in Table 3.

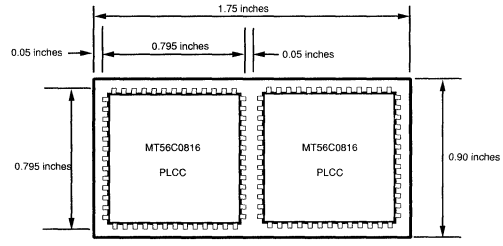
OPTIMUM SYSTEM

The available, off-the-shelf cache controllers allow very quick and efficient cache subsystem designs for 80386-based systems. And an off-the-shelf controller teamed with the MT56C0816 maximizes the system performance/cost ratio. The MT56C0816 allows the controller to be employed in its highest performance mode, two-way-set associativity, without the disadvantages incurred using standard SRAMs.

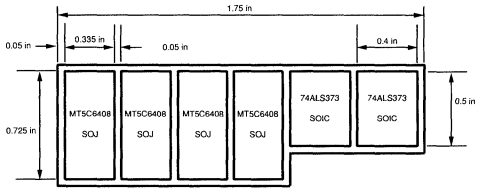
A two-way-set design using the MT56C0816 requires only two parts versus 10 for an 8K x 8 SRAM implementation and 26 for a 4K x 4 implementation. A direct-mapped design using the MT56C0816 requires only two parts versus six for an 8K x 8 SRAM implementation and 26 for a 4K x 4 implementation. In addition to the board-space, power, and integration advantages, the MT56C0816 offers a direct connection to the controllers. This means higher system reliability and easier design and debugging over the standard SRAM implementations. Figure 6 shows a detailed diagram of a system using the MT56C0816.



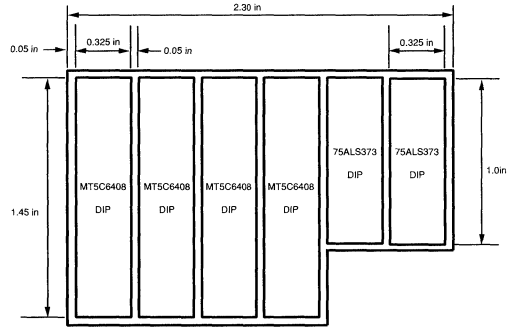
MT56C0816 PQFP



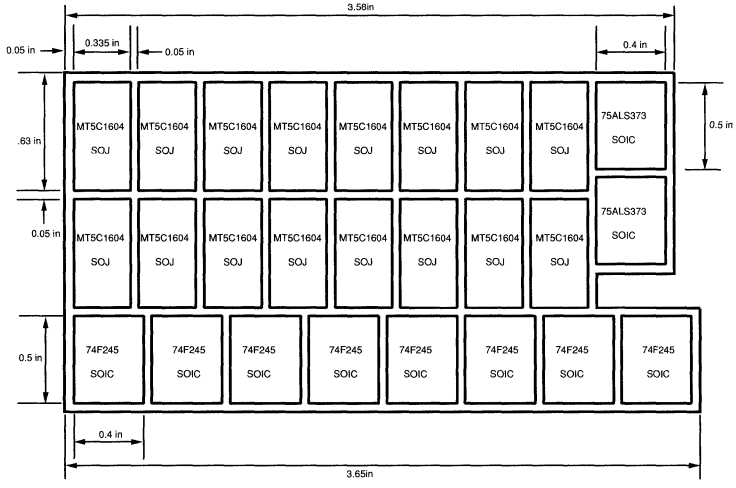
MT56C0816 PLCC



8K x 8 SOJ/SOIC

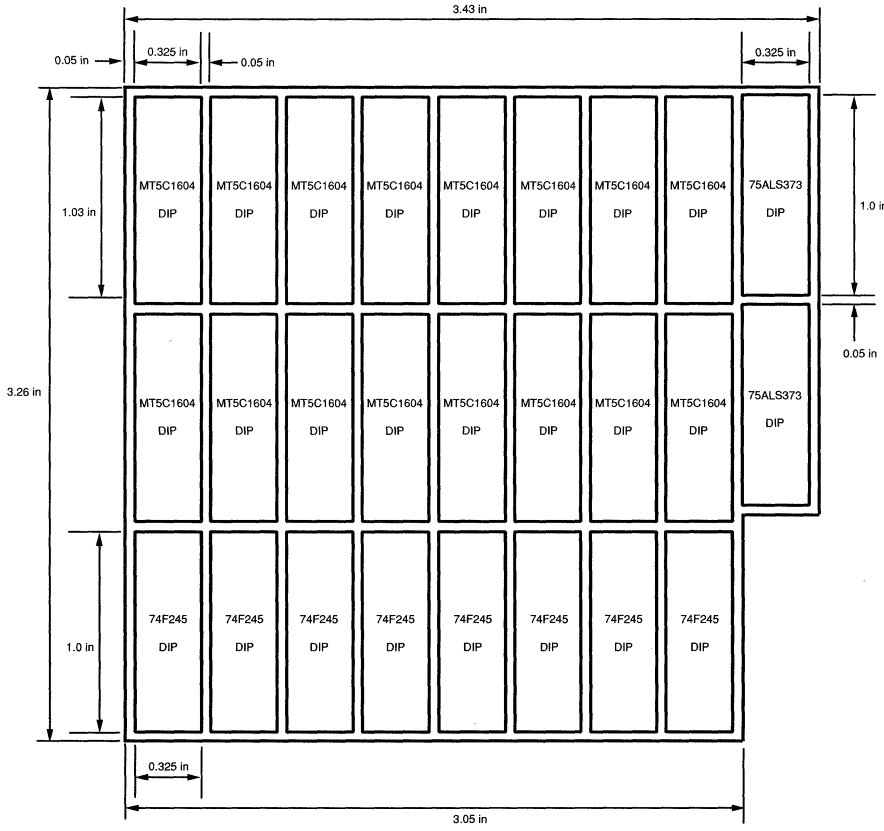


8K x 8 DIP



4K x 4 SOJ/SOIC

Figure 4



4K x 4 DIP

Figure 5

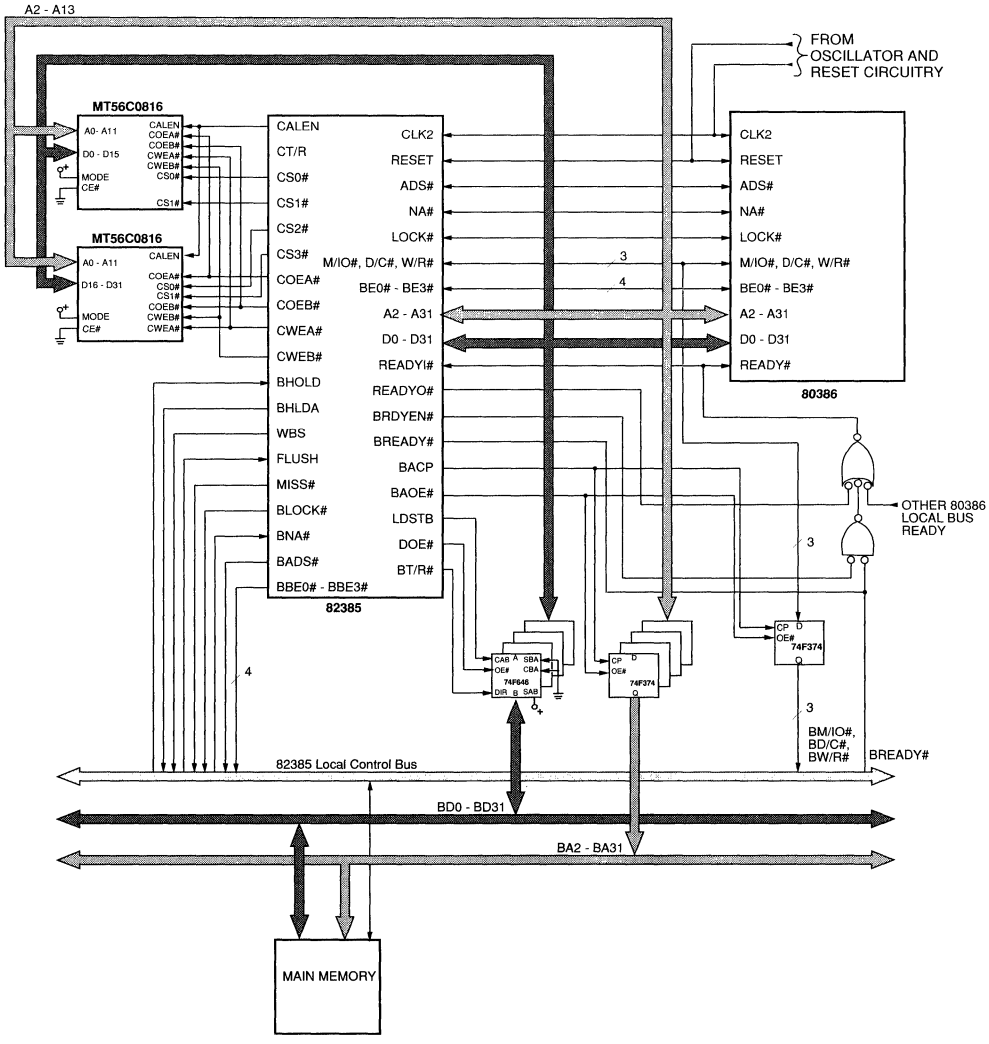

A2 - A13
MT56C0816
A0- A11
D0 - D15
MODE
CE#
CALEN
COEA#
COEB#
CWEA#
CWEB#
CS0#
CS1#
MT56C0816
A0 - A11
D16 - D31
MODE
CE#
CALEN
COEA#
CS0#
CS1#
COEB#
CWEB#
CWEA#
CALEN
CT/R
CS0#
CS1#
CS2#
CS3#
COEA#
COEB#
CWEA#
CWEB#
BHOLD
BHLDA
WBS
FLUSH
MISS#
BLOCK#
BNA#
BADS#
BBE0# - BBE3#
82385
CLK2
RESET
ADS#
NA#
LOCK#
M/IO#, D/C#, W/R#
BE0# - BE3#
A2 - A31
D0 - D31
READYI#
READYO#
BRDYEN#
BREADY#
BACP
BAOE#
LDSTB
DOE#
BT/R#
FROM OSCILLATOR AND RESET CIRCUITRY
CLK2
RESET
ADS#
NA#
LOCK#
M/IO#, D/C#, W/R#
BE0# - BE3#
A2 - A31
D0 - D31
READY#
80386
OTHER 80386 LOCAL BUS READY
74F374
74F646
74F374
BM/IO#, BD/C#, BW/R#
BREADY#
82385 Local Control Bus
BD0 - BD31
BA2 - BA31
MAIN MEMORY

Figure 6

Table 4

MICRON CACHE SRAM FAMILY				
Part #	**Description**	**Speed (ns)**	**Package**	**Availability**
MT56C0816	Dual 4K x 16 or 8K x 16 Addresses 0 through 11 are latched	20, 25, 35	PLCC PQFP	Now
MT56C0818	Dual 4K x 18 or 8K x 18 Addresses 0 through 11 are latched	20, 25, 35	PLCC PQFP	Now
MT56C2818	Dual 4K x 18 or 8K x 18 80486 self-timed write; used on Intel Turbocache486™ module	24, 28	PLCC PQFP	Now
MT56C3816	Dual 4K x 16 or 8K x 16 Addresses 0 through 12 are latched	20, 25, 35	PLCC PQFP	Feb. 1991
MT56C3818	Dual 4K x 18 or 8K x 18 Addresses 0 through 12 are latched	20, 25, 35	PLCC PQFP	Feb. 1991
MT56C1616	Dual 8K x 16 or 16K x 16 Addresses 0 through 12 are latched	15, 20, 25	PLCC PQFP	2H 1991
MT56C1618	Dual 8K x 18 or 16K x 18 Addresses 0 through 12 are latched	15, 20, 25	PLCC PQFP	2H 1991
MT56C3616	Dual 8K x 16 or 16K x 16 Addresses 0 through 13 are latched	15, 20, 25	PLCC PQFP	2H 1991
MT56C3618	Dual 8K x 18 or 16K x 18 Addresses 0 through 13 are latched	15, 20, 25	PLCC PQFP	2H 1991
MT56C2618	Dual 8K x 18 or 16K x 18 80486 self-timed write	17, 24, 28	PLCC PQFP	2H 1991

MORE SOLUTIONS

An entire family of cache-specific data SRAMs is available. Table 4 lists the members of the cache SRAM family.

In addition, Micron was the first to introduce the MT56C0816 both in a 20ns access speed and in the thin, small-outline PQFP package.

SPECIAL CONSIDERATIONS

The Micron MT56C0816 was designed for a specific generation of cache implementations for the 80386. That generation required a nonlatched A12 address and a faster A12 access time. Since then, designs employing certain off-the-shelf controllers are more efficiently implemented if address line A12 is latched on the cache data SRAM. These designs do not require the faster A12 access time. In order to keep pace with the everchanging design community Micron will introduce in the Q1/1991 time-frame versions of the MT56C0816 and the MT56C0818 with address A12 latched. The part numbers of these new devices are MT56C3816 and MT56C3818 respectively.

The latched A12 version of the cache data SRAM can be appealing in 80386DX designs where the cache uses a two-way-set associative architecture and the cache size is 64KB or larger. The latched A12 parts are applicable for 80386SX designs where the cache is structured using a two-way-set associative organization and the cache size is 32KB or larger. Designs using a direct-mapped architecture essentially use the cache data SRAM as an 8K x 16 SRAM and as such the latched version would be advantageous in all cases.

Whether the latched or unlatched A12 version of the cache data SRAM is more advantageous depends entirely on the specifics of each individual design.

SUMMARY

The Micron MT56C0816 has been as important to 80386 caching solutions as the off-the-shelf controllers from Intel, Austek and Chips & Technologies. The direct connection of the MT56C0816 to controllers makes the implementation more appealing for the designer from both a design and debug standpoint. The reduced board space, power and comparable cost to commodity SRAM implementations are advantages that make the MT56C0816 the right choice for new designs. Implementations using the MT56C0816 add reliability to the system due to the reduced component count. The MT56C0816 offers other less obvious cost advantages. Reduced board space requirements directly affect board manufacturing costs and allow more components to be placed on the board. Better reliability means lower costs due to fewer returns and fewer board revisions. Other costs that the MT56C0816 minimizes over the standard SRAM solutions are inventory and assembly costs.

Clearly the Micron MT56C0816 is a superior solution to standard SRAMs in cache designs.

MICRON TECHNOLOGY, INC.

GENERAL INFORMATION

As a major supplier to the defense electronics industry, Micron offers an extensive array of speeds and configurations compatible with military-standard pinouts. A wide selection of devices are available to fit both Standard Military Drawings (SMD) and Joint Army-Navy (JAN) Level-B specifications — SRAMs, DRAMs and Multiport DRAMs.

Micron maintains the MIL-M-38510 certification status for all its fabrication facilities. Micron's CMOS and NMOS process technologies are both JAN certified. Our military-grade SRAM modules meet or exceed the proposed standards of the JEDEC JC-13 Module Committee. Currently, we are waiting for DESC to announce approval of these MIL-STD-883 standards.

Micron's entire military assembly takes place in Boise, Idaho. Micron produces and tests our military products to specifications that meet or exceed the requirements of MIL-M-38510 and MIL-STD-883, methods 5004 and 5005. Every Micron product is tested on the AMBYX,™ a unique, intelligent burn-in system designed by Micron to eliminate infant mortalities. Our internal processes provide an extensive data base that allows complete statistical process control and test data in real time.

Many of Micron's military products have received military qualification, including the 1 Meg VRAM and 1 Meg SRAM. To date, military qualification is pending on Micron's 4 Meg DRAMs and various SRAM modules. Products under development include cache data SRAMs and FIFOs. New package configurations will include a ceramic vertical (CV) package that meets high-density, through-hole designs. Micron is also looking into J-leaded LCC packages for high-density boards.

Memory devices for military and space-level applications require both radiation tolerance and latch-up immunity. Micron is currently in the process of characterizing select CMOS SRAM and DRAM devices for total dose, dose rate and latch-up immunity.

Micron is continually evaluating and improving our radiation tolerance processes on our military and commercial products for future use on land, sea and in space. We're assessing our 1 Meg SRAM, 4 Meg DRAM and 1 Meg VRAM devices beyond standard MIL-STD-883 and JAN Level-B requirements. Micron is developing a process flow that parallels the requirements of Class-S to be used for products not requiring Class-S compliance. These products will offer the high density and speed necessary in space-level applications. For more information, please refer to Micron's ***Military MOS Data Book.***

MICRON MIL-STD-883C COMPLIANT PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev. C	Establish and implement a plan for a product assurance program	
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembled and tested in Boise, Idaho USA
MIL-STD 883 Fabrication		
5. Incoming Materials	Receiving inspection	Vendor audits
6. Wafer Fabrication	Method 2018, SEM monitors	Sample
7. Assembly	Process monitors	Sample
	Statistical process controls	Sample
MIL-STD 883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Thermal Shock	Method 1010, cond. B	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet	100%
13. Burn-in	Method 1015	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, paragraph 3.1.15, 5% PDA	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
18. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each inspection lot/sublot
20. Group B	Package functional and construction tests	Each inspection lot/sublot
21. Group C	Die related	Each microcircuit group, every 4 calendar quarters
22. Group D	Package-related test	Each package type, every 52 weeks

DRAM

Description	Speed	Micron Part Number	SMD Part Number (5962-)	JAN Part Number
64K x 1 CDIP	120ns	MT4264C-12 883C		
	150ns	MT4264C-15 883C	8201004EX (-55°C/+125°C)	
			8201006EX (-55°C/+110°C)	
	200ns	MT4264C-20 883C	8201005EX (-55°C/+125°C)	
			8201007EX (-55°C/+110°C)	
64K x 1 CLCC	120ns	MT4264EC-12 883C		
	150ns	MT4264EC-15 883C	820100406ZX	
	200ns	MT4264EC-20 883C	820100607ZX	
64K x 1 Flat Pack	120ns	MT4264F-12 883C	No Drawing	
	150ns	MT4264F-15 883C	No Drawing	
	200ns	MT4264F-20 883C	No Drawing	
256K x 1 CDIP	100ns	MT1259C-10 883C	No Drawing	
	120ns	MT1259C-12 883C	8515203EX	JM38510/2460103BEX
	150ns	MT1259C-15 883C	8515201EX	JM38510/2460204BEX
256K x 1 CLCC	100ns	MT1259EC-10 883C	No Drawing	
	120ns	MT1259EC-12 883C	8515203XX	JM38510/2460103BXX
	150ns	MT1259EC-15 883C	8515201XX	JM38510/2460204BXX
64K x 4 CDIP	100ns	MT4067C-10 883C	8767604VX	
	120ns	MT4067C-12 883C	8767601VX	
	150ns	MT4067C-15 883C	8767602VX	
	200ns	MT4067C-20 883C	8767603VX	
64K x 4 CLCC	100ns	MT4067EC-10 883C	8767604XX	
	120ns	MT4067EC-12 883C	8767601XX	
	150ns	MT4067EC-15 883C	8767602XX	
	200ns	MT4067EC-20 883C	8767603XX	
1 Meg x 1 CDIP	80ns	MT4C1024C-8 883C	No Drawing	JM38510/24901BVX
	100ns	MT4C1024C-10 883C	No Drawing	JM38510/24902BVX
	120ns	MT4C1024C-12 883C	No Drawing	JM38510/24903BVX
	150ns	MT4C1024C-15 883C	No Drawing	JM38510/24904BVX
1 Meg x 1 CLCC	80ns	MT4C1024EC-8 883C		JM38510/24901BZX
	100ns	MT4C1024EC-10 883C		JM38510/24902BZX
	120ns	MT4C1024EC-12 883C		JM38510/24903BZX
	150ns	MT4C1024EC-15 883C		JM38510/24904BZX
1 Meg x 1 Flat Pack	80ns	MT4C1024F-8 883C		JM38510/24901BXX
	100ns	MT4C1024F-10 883C		JM38510/24902BXX
	120ns	MT4C1024F-12 883C		JM38510/24903BXX
	150ns	MT4C1024F-15 883C		JM38510/24904BXX

DRAM

Description	Speed	Micron Part Number	SMD Part Number (5962-)	JAN Part Number (5962-)
1 Meg x 4 CDIP	80ns	MT4C4001C-8 883C	90847M_X	90847B_X
	100ns	MT4C4001C-10 883C	90847M_X	90847B_X
	120ns	MT4C4001C-12 883C	90847M_X	90847B_X
	150ns	MT4C4001C-15 883C	90847M_X	90847B_X
1 Meg x 4 LCC	80ns	MT4C4001EC-8 883C	90847M_X	90847B_X
	100ns	MT4C4001EC-10 883C	90847M_X	90847B_X
	120ns	MT4C4001EC-12 883C	90847M_X	90847B_X
	150ns	MT4C4001EC-15 883C	90847M_X	90847B_X
1 Meg x 4 Flat Pack	80ns	MT4C4001F-8 883C	90847M_X	90847B_X
	100ns	MT4C4001F-10 883C	90847M_X	90847B_X
	120ns	MT4C4001F-12 883C	90847M_X	90847B_X
	150ns	MT4C4001F-15 883C	90847M_X	90847B_X
4 Meg x 1 CDIP	80ns	MT4C1004C-8 883C	90622M_X	90622B_X
	100ns	MT4C1004C-10 883C	90622M_X	90622B_X
	120ns	MT4C1004C-12 883C	90622M_X	90622B_X
	150ns	MT4C1004C-15 883C	90622M_X	90622B_X
4 Meg x 1 LCC	80ns	MT4C1004EC-8 883C	90622M_X	90622B_X
	100ns	MT4C1004EC-10 883C	90622M_X	90622B_X
	120ns	MT4C1004EC-12 883C	90622M_X	90622B_X
	150ns	MT4C1004EC-15 883C	90622M_X	90622B_X
4 Meg x 1 Flat Pack	80ns	MT4C1004F-8 883C	90622M_X	90622B_X
	100ns	MT4C1004F-10 883C	90622M_X	90622B_X
	120ns	MT4C1004F-12 883C	90622M_X	90622B_X
	150ns	MT4C1004F-15 883C	90622M_X	90622B_X

MULTIPORT DRAM

Description	Speed	Micron Part Number	SMD Part Number (5962-)	JAN Part Number
64K x 4 CDIP	100ns	MT42C4064C-10 883C	89952M_X	
	120ns	MT42C4064C-12 883C	89952M_X	
	150ns	MT42C4064C-15 883C	89952M_X	
64K x 4 LCC	120ns	MT42C4064EC-10 883C	89952M_X	
	150ns	MT42C4064EC-12 883C	89952M_X	
	200ns	MT42C4064EC-15 883C	89952M_X	
128K x 8 CDIP	80ns	MT42C8128CW-8 883C	No Drawing	
	100ns	MT42C8128CW-10 883C	No Drawing	
	120ns	MT42C8128CW-12 883C	No Drawing	
256K x 4 CDIP	80ns	MT42C4256-8 883C	No Drawing	
	100ns	MT42C4256-12 883C	No Drawing	
	120ns	MT42C4256-15 883C	No Drawing	

SRAM

Description	Speed	Micron Part Number	SMD Part Number (5962-)	JAN Part Number
128K x 8 CDIP	25ns	MT5C1008C-25 883C	8959837MZX*	5962-8959837BZX*
	35ns	MT5C1008C-30 883C	8959836MZX*	5962-8959836BZX*
	45ns	MT5C1008C-45 883C	8959835MZX*	5962-8959835BZX*
256K x 1 CDIP	25ns	MT5C2561C-25 L 883C	8872505LX	JM38510/29310BLX
	35ns	MT5C2561C-35 L 883C	8872501LX	JM38510/29302BLX
	45ns	MT5C2561C-45 883C	8872502LX	JM38510/29301BLX
256K x 1 CLCC	25ns	MT5C2561EC-25 L 883C	8872505XX	JM38510/29310BNX
	35ns	MT5C2561EC-35 L 883C	8872501XX	JM38510/29302BNX
	45ns	MT5C2561EC-45 883C	8872502XX	JM38510/29301BNX
64K x 4 CDIP	25ns	MT5C2564C-25 L 883C	Note 1	JM38510/29311BLX
	35ns	MT5C2564C-35 L 883C	8868101LX	JM38510/29304BLX
	45ns	MT5C2564C-45 883C	8868102LX	JM38510/29303BLX
64K x 4 CLCC	25ns	MT5C2564EC-25 L 883C	Note 1	JM38510/29311BNX
	35ns	MT5C2564EC-30 L 883C	8868101XX	JM38510/29304BNX
	45ns	MT5C2564EC-45 883C	8868102XX	JM38510/29303BNX
64K x 4 CDIP w/$\overline{OE}$	25ns	MT5C2565C-25 L 883C	8952405XX	JM38510/29312BYX
	35ns	MT5C2565C-35 L 883C	8952404XX	JM38510/29315BYX
	45ns	MT5C2565C-45 883C	8952403XX	JM38510/29314BYX
64K x 4 CLCC w/$\overline{OE}$	25ns	MT5C2565EC-25 L 883C	8952405YX	JM38510/29312BNX
	35ns	MT5C2565EC-30 L 883C	8952404YX	JM38510/29315BNX
	45ns	MT5C2565EC-45 883C	8952403YX	JM38510/29314BNX
32K x 8 CDIP 300 MIL	25ns	MT5C2568C-25 L 883C	No Drawing	JM38510/29313BYX
	35ns	MT5C2568C-30 L 883C	No Drawing	JM38510/29309BYX
	45ns	MT5C2568C-45 883C	No Drawing	JM38510/29308BYX
	55ns	MT5C2568C-55 883C	No Drawing	JM38510/29307BYX
32K x 8 CDIP 600 MIL	25ns	MT5C2568CW-25 L 883C	Note 1	JM38510/29313BXX
	35ns	MT5C2568CW-35 L 883C	No Drawing	JM38510/29309BXX
	45ns	MT5C2568CW-45 L 883C	8866204XX	JM38510/29308BXX
	55ns	MT5C2568CW-55 L 883C	8866205XX	JM38510/29307BXX
32K x 8 CLCC 28 PIN	25ns	MT5C2568EC-25 L 883C	Note 1	JM38510/29313BNX
	35ns	MT5C2568EC-35 L 883C	No Drawing	JM38510/29309BNX
	45ns	MT5C2568EC-45 L 883C	8866204UX	JM38510/29308BNX
	55ns	MT5C2568EC-55 L 883C	8866205UX	JM38510/29307BNX

*Preliminary

Note: 1. The current SMDs are written for the slower grade devices. Micron has submitted new drawings to DESC for faster devices.

L: Optional 2V data retention is available on all parts indicated by "L" after speed.
Optional low-voltage data retention available on all SRAMs.

SRAM

Description	Speed	Micron Part Number	SMD Part Number (5962-)	JAN Part Number
32K x 8 CLCC	25ns	MT5C2568ECW-25 L 883C	No Drawing	JM38510/29313BTX
32 PIN	35ns	MT5C2568ECW-30 L 883C	No Drawing	JM38510/29309BTX
	45ns	MT5C2568ECW-45 L 883C	8866204YX	JM38510/29308BTX
	55ns	MT5C2568ECW-55 L 883C	8866205YX	JM38510/29307BTX
32K x 8 Flat Pack	25ns	MT5C2568F-25 L 883C	No Drawing	JM38510/29313BMX
	35ns	MT5C2568F-35 L 883C	No Drawing	JM38510/29309BMX
	45ns	MT5C2568F-45 L 883C	8866204TX	JM38510/29308BMX
	55ns	MT5C2568F-55 L 883C	8866205TX	JM38510/29307BMX
64K x 1 CDIP	20ns	MT5C6401C-20 L 883C	Note 1	
	25ns	MT5C6401C-25 L 883C	No Drawing	
	30ns	MT5C6401C-30 L 883C	No Drawing	
	35ns	MT5C6401C-35 L 883C	8601501XX	
64K x 1 CLCC	20ns	MT5C6401EC-20 L 883C	Note 1	
	25ns	MT5C6401EC-25 L 883C	No Drawing	
	30ns	MT5C6401EC-30 L 883C	No Drawing	
	35ns	MT5C6401EC-35 L 883C	8601501ZX	
16K x 4 CDIP	20ns	MT5C6404C-20 L 883C	8969204YX	
	25ns	MT5C6404C-25 L 883C	8969202YX	
16K x 4 CLCC	20ns	MT5C6404EC-20 L 883C	8969204ZX	
	25ns	MT5C6404EC-25 L 883C	8969202ZX	
8K x 8 CDIP	15ns	MT5C6408C-15 L 883C	3829418MZX	
300 MIL	15ns	MT5C6408C-15 883C	3829419MZX	
	20ns	MT5C6408C-20 L 883C	8969104ZX or 3829416MZX	
	25ns	MT5C6408C-25 L 883C	8969102ZX or 3829414MZX	
	30ns	MT5C6408C-30 L 883C	No Drawing	
	35ns	MT5C6408C-35 L 883C	3829412MZX	
8K x 8 CDIP	20ns	MT5C6408CW-20 L 883C	8969104XX	
600 MIL	25ns	MT5C6408CW-25 L 883C	8969102XX	
	30ns	MT5C6408CW-30 L 883C	No Drawing	
	35ns	MT5C6408CW-35 L 883C	No Drawing	
8K x 8 CLCC	15ns	MT5C6408EC-15 L 883C	3829418MUX	
28 PIN	20ns	MT5C6408EC-20 L 883C	8969104NX or 3829416MUX	
	25ns	MT5C6408EC-25 L 883C	8969102NX or 3829414MUX	
	30ns	MT5C6408EC-30 L 883C	No Drawing	
	35ns	MT5C6408EC-35 L 883C	3829412MUX	

Note: 1. The current SMDs are written for the slower grade devices. Micron has submitted new drawings to DESC for faster devices.

L: Optional 2V data retention is available on all parts indicated by "L" after speed.
Optional low-voltage data retention available on all SRAMs.

SRAM

Description	Speed	Micron Part Number	SMD Part Number	JAN Part Number
8K x 8 Flat Pack	25ns	MT5C6408F-25 L 883C	8969102YX	
32 PIN	35ns	MT5C6408F-35 L 883C	No Drawing	
2K x 8 CDIP	20ns	MT5C1608C-20 L 883C	8969002LX	
	25ns	MT5C1608C-25 L 883C	8969001LX	
	30ns	MT5C1608C-30 L 883C	No Drawing	
	35ns	MT5C1608C-35 L 883C	No Drawing	
2K x 8 CLCC	20ns	MT5C1608EC-20 L 883C	8969002ZX	
	25ns	MT5C1608EC-25 L 883C	8969001ZX	
	30ns	MT5C1608EC-30 L 883C	No Drawing	
	35ns	MT5C1608EC-35 L 883C	No Drawing	

SRAM MODULE

Description	Speed	Micron Part Number	SMD Part Number	JAN Part Number
128K x 8 CDIP	35ns	MT4S1288CW-35	No Drawing	
512K x 8 CDIP	35ns	MT4S5128CW-35	No Drawing	
64K x 16 CDIP	35ns	MT4S6416CW-35	No Drawing	
64K x 32 CDIP	35ns	MT4S6432CW-35	No Drawing	

CACHE DATA SRAM*

Description	Speed	Micron Part Number	SMD Part Number	JAN Part Number
8K x 16 CLCC	20ns	MT56C0816C-20 L 883C	No Drawing	
	25ns	MT56C0816C-25 L 883C	No Drawing	
	35ns	MT56C0816C-35 L 883C	No Drawing	

*Preliminary

Note: 1. The current SMDs are written for the slower grade devices. Micron has submitted new drawings to DESC for faster devices.

L: Optional 2V data retention is available on all parts indicated by "L" after speed.
Optional low-voltage data retention available on all SRAMs.

FIFO*

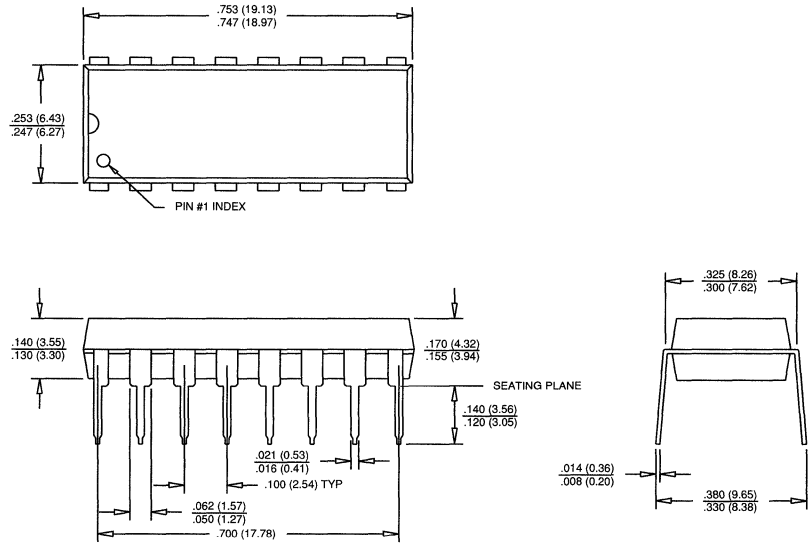
Description	Speed	Micron Part Number	SMD Part Number	JAN Part Number
512 x 9 CLCC	15ns	MT52C9005EC-15 883C	No Drawing	
	20ns	MT52C9005EC-20 883C	No Drawing	
	25ns	MT52C9005EC-25 883C	No Drawing	
	35ns	MT52C9005EC-35 883C	No Drawing	
1K x 9 CLCC	15ns	MT52C9010EC-15 883C	No Drawing	
	20ns	MT52C9010EC-20 883C	No Drawing	
	25ns	MT52C9010EC-25 883C	No Drawing	
	35ns	MT52C9010EC-35 883C	No Drawing	
2K x 9 CLCC	15ns	MT52C9020EC-15 883C	No Drawing	
	20ns	MT52C9020EC-20 883C	No Drawing	
	25ns	MT52C9020EC-25 883C	No Drawing	
	35ns	MT52C9020EC-35 883C	No Drawing	

*Preliminary

MICRON TECHNOLOGY, INC.

16-PIN PLASTIC DIP

A-1

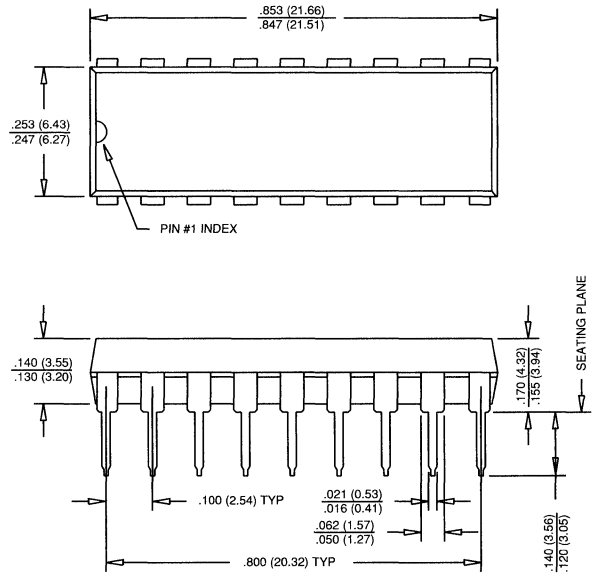


All dimensions in inches (millimeters) $\frac{\text{Max}}{\text{Min}}$ or typical where noted.

NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

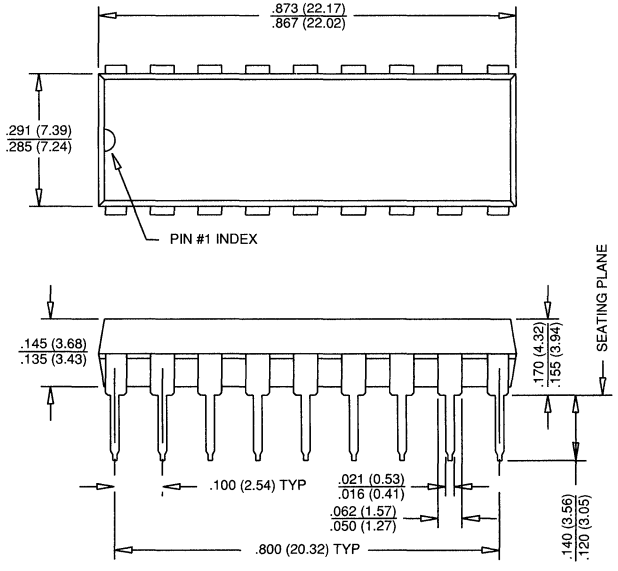
18-PIN PLASTIC DIP

A-2



18-PIN PLASTIC DIP

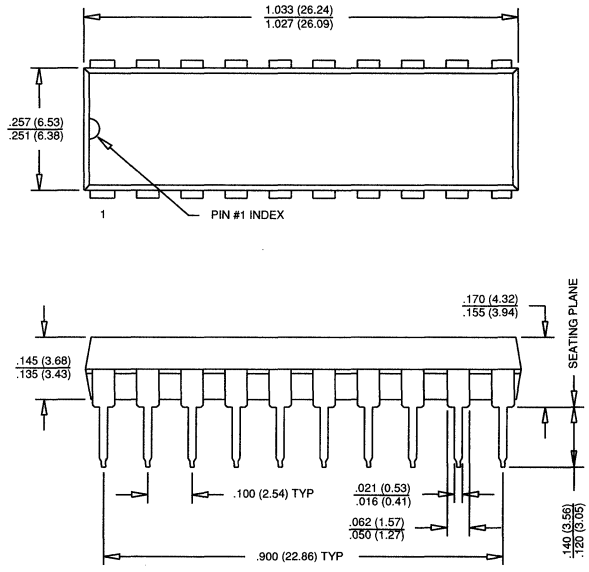
A-3



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

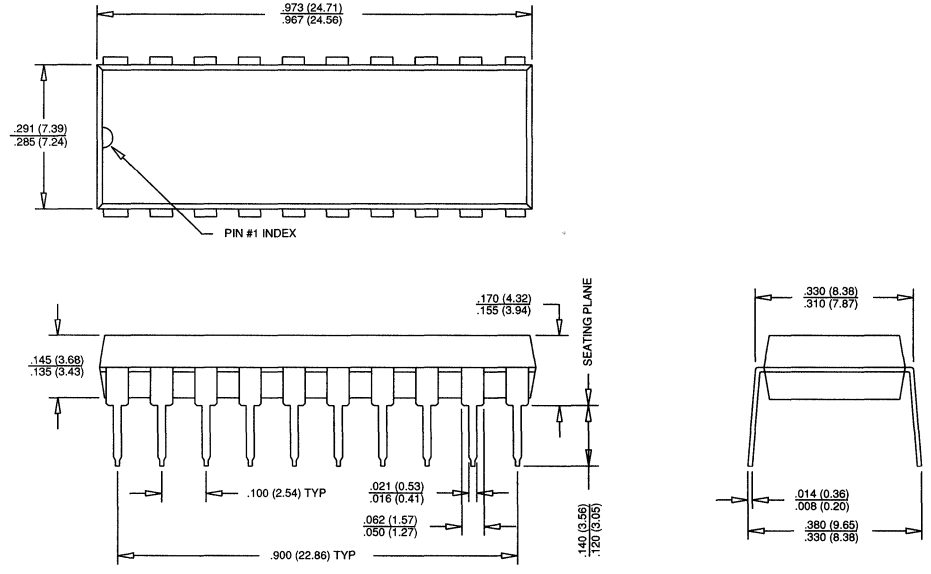
20-PIN PLASTIC DIP

A-4



20-PIN PLASTIC DIP

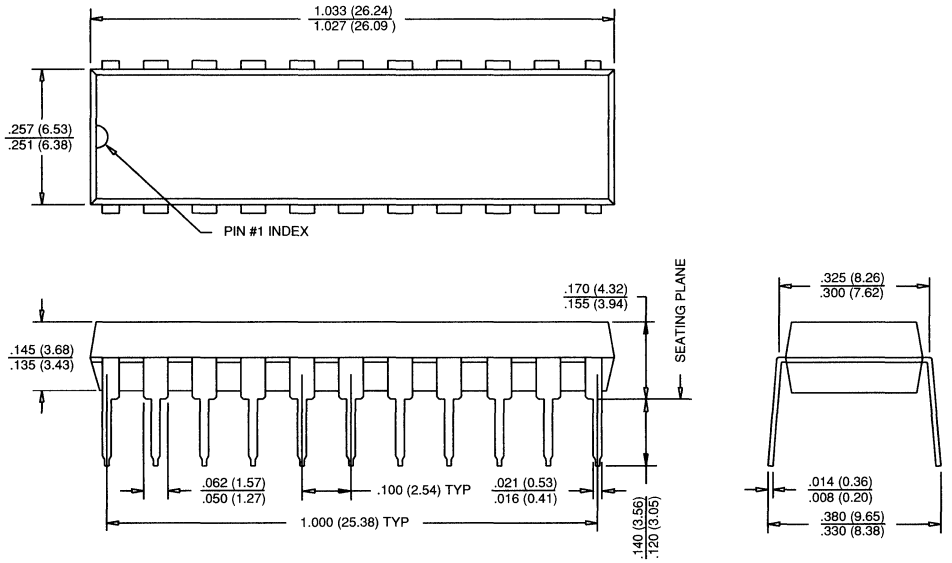
A-5



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

22-PIN PLASTIC DIP

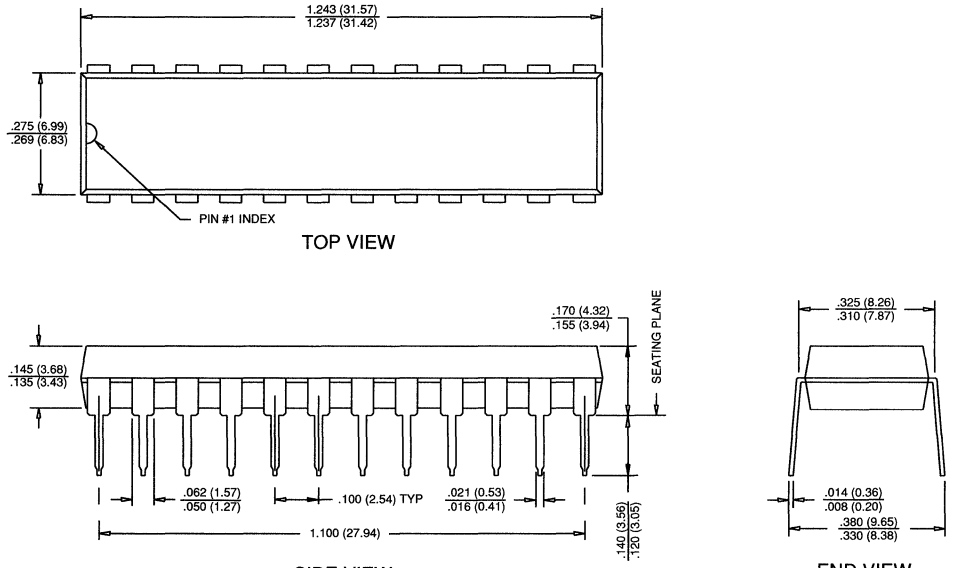
A-6



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

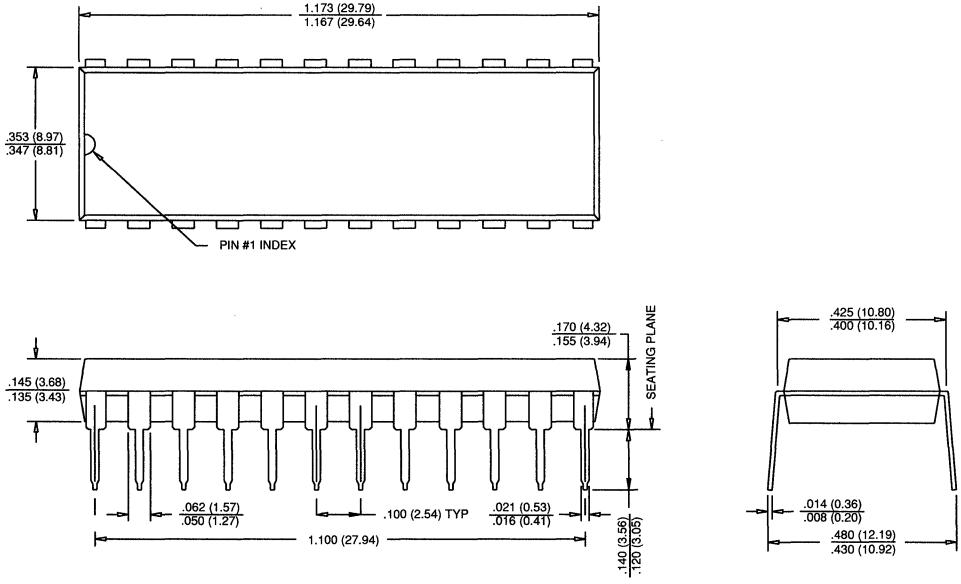
24-PIN PLASTIC DIP

A-7



24-PIN PLASTIC DIP

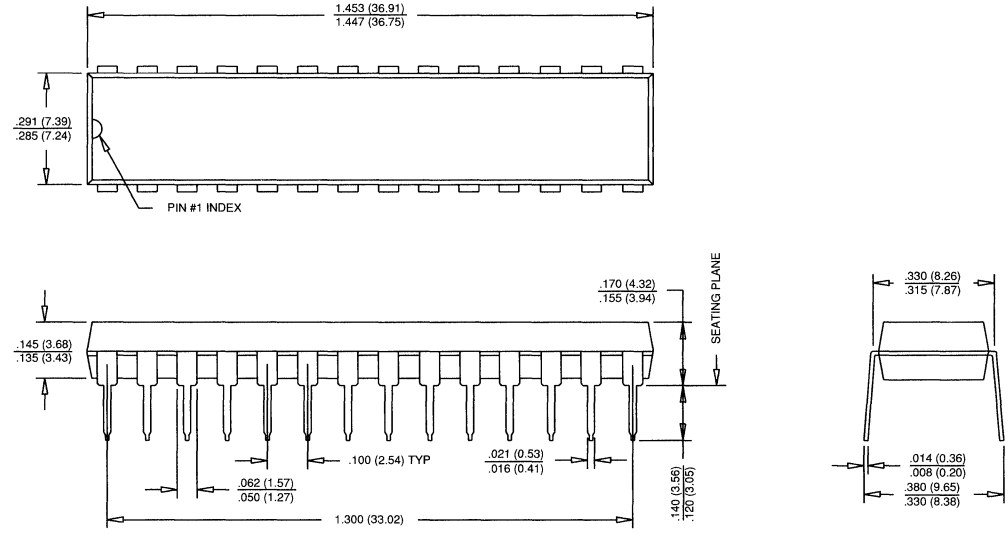
A-8



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

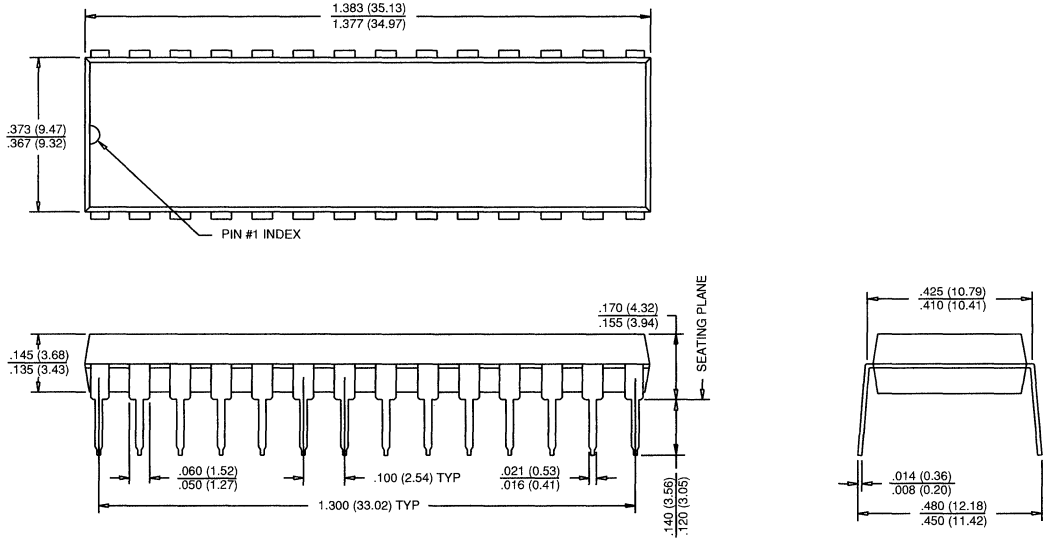
28-PIN PLASTIC DIP

A-9



28-PIN PLASTIC DIP

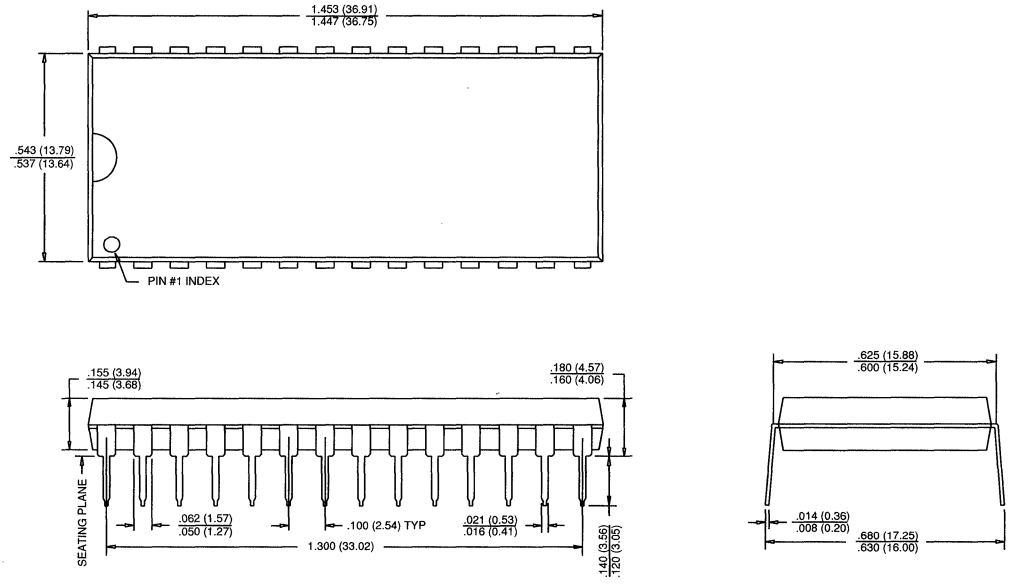
A-10



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

28-PIN PLASTIC DIP

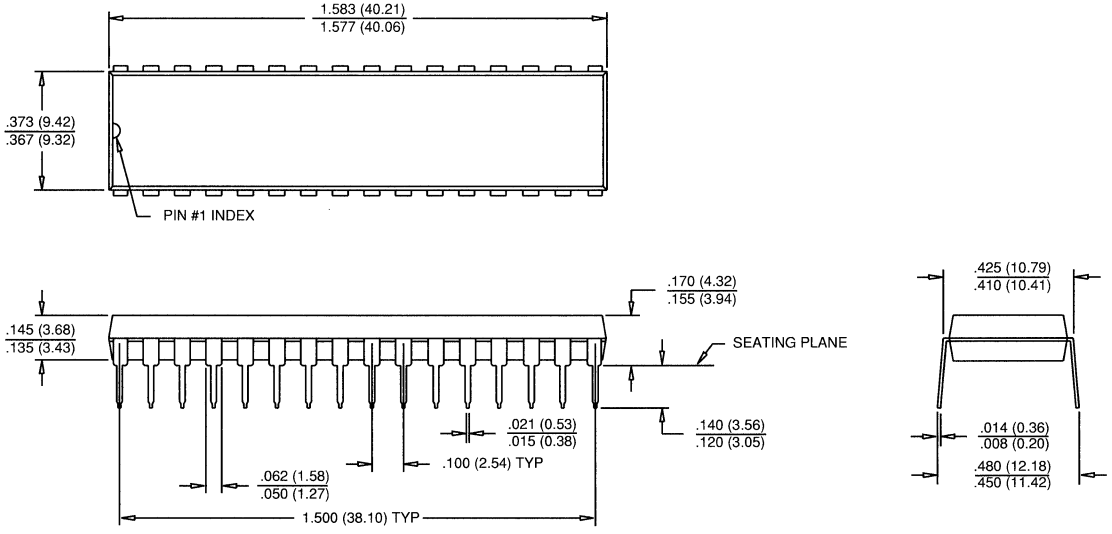
A-11



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

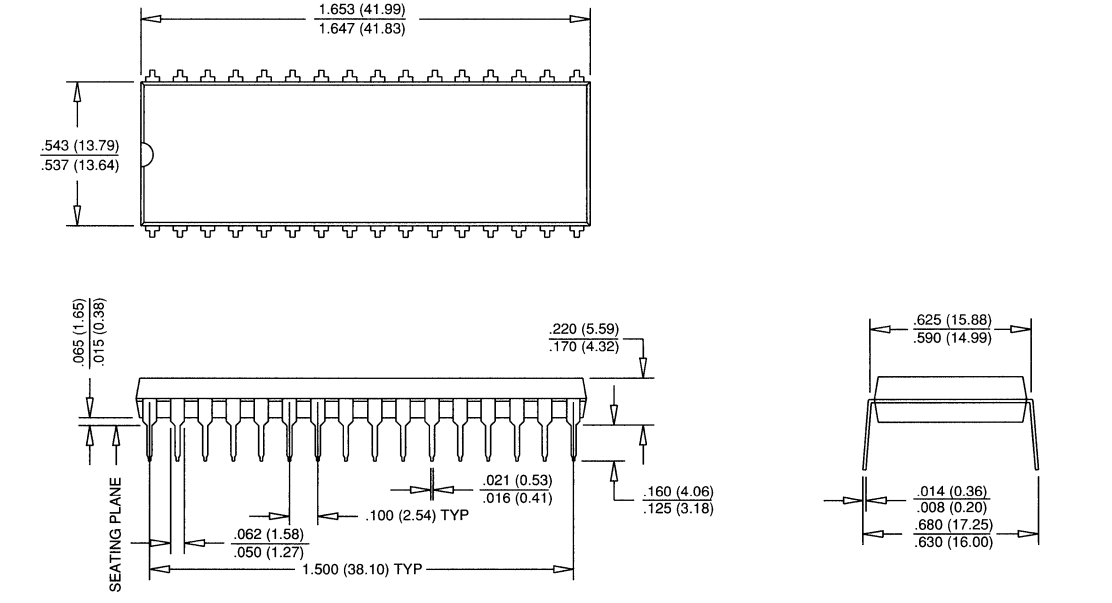
32-PIN PLASTIC DIP

A-12



32-PIN PLASTIC DIP

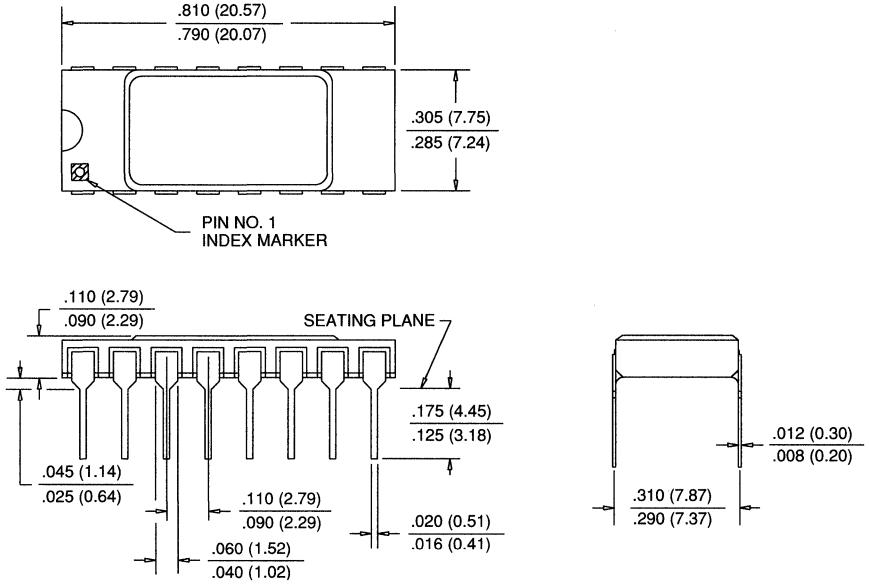
A-13



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

16-PIN CERAMIC DIP

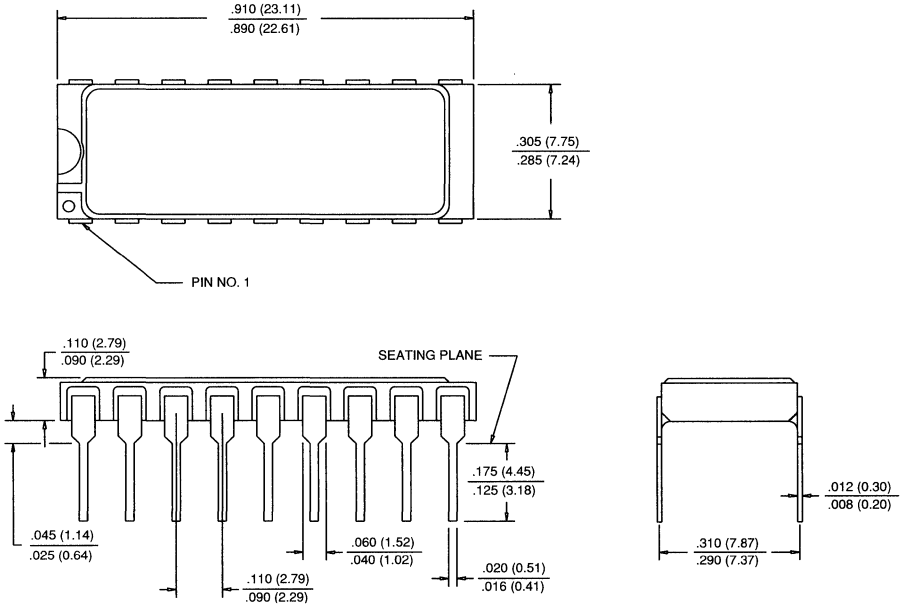
B-1



All dimensions in inches (millimeters) $\frac{\text{Max}}{\text{Min}}$ or typical where noted.

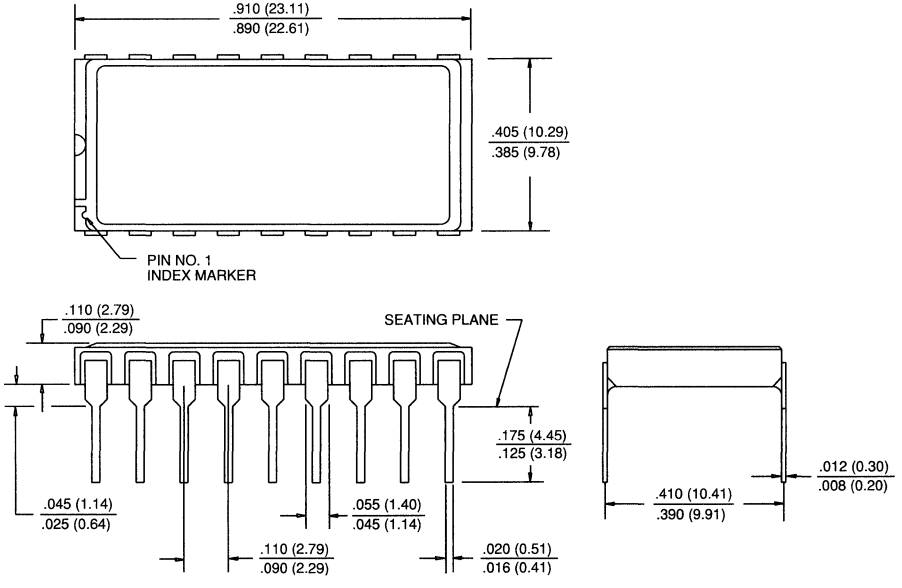
18-PIN CERAMIC DIP

B-2



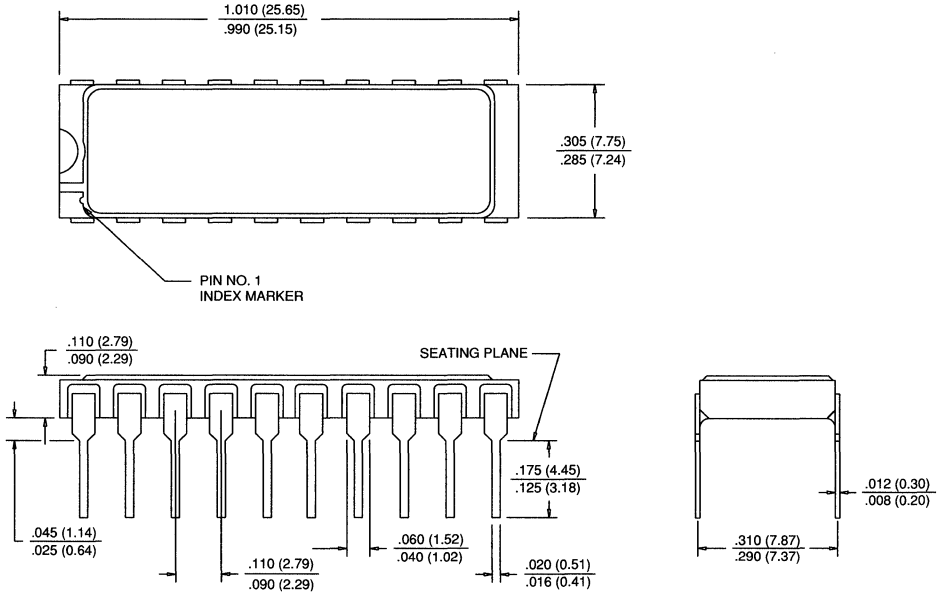
18-PIN CERAMIC DIP

B-3



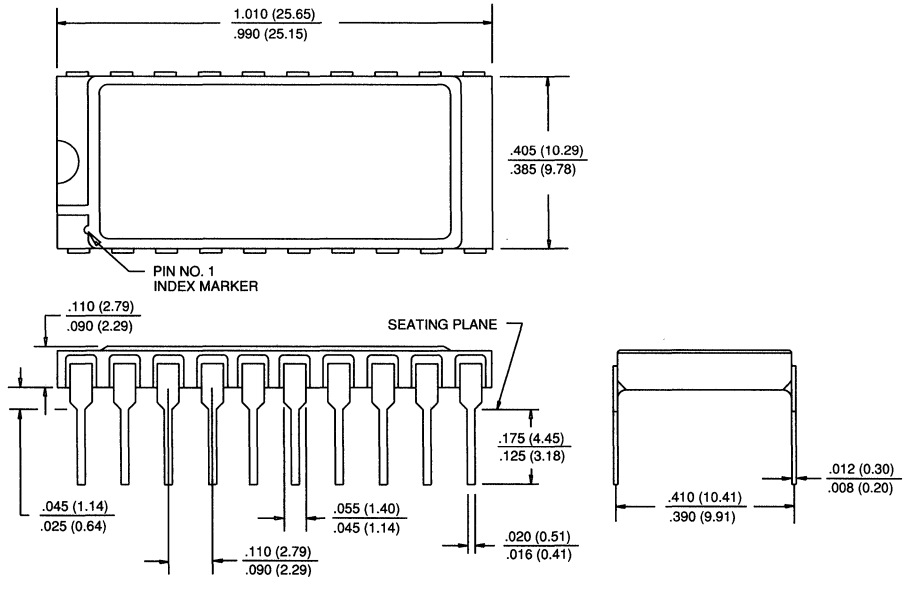
20-PIN CERAMIC DIP

B-4



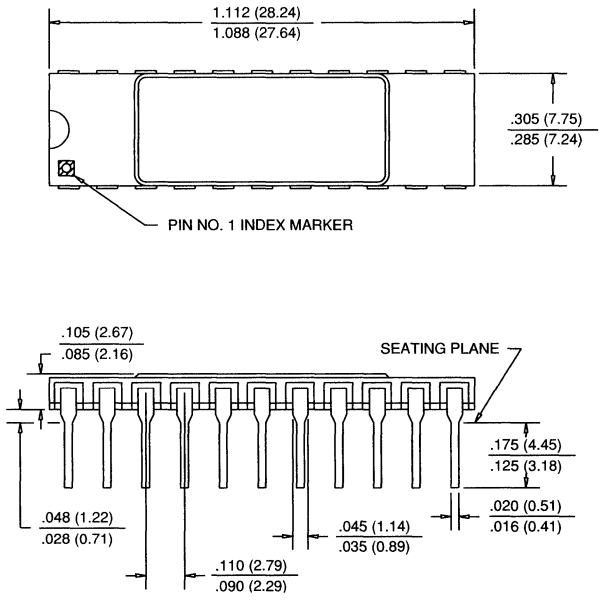
20-PIN CERAMIC DIP

B-5



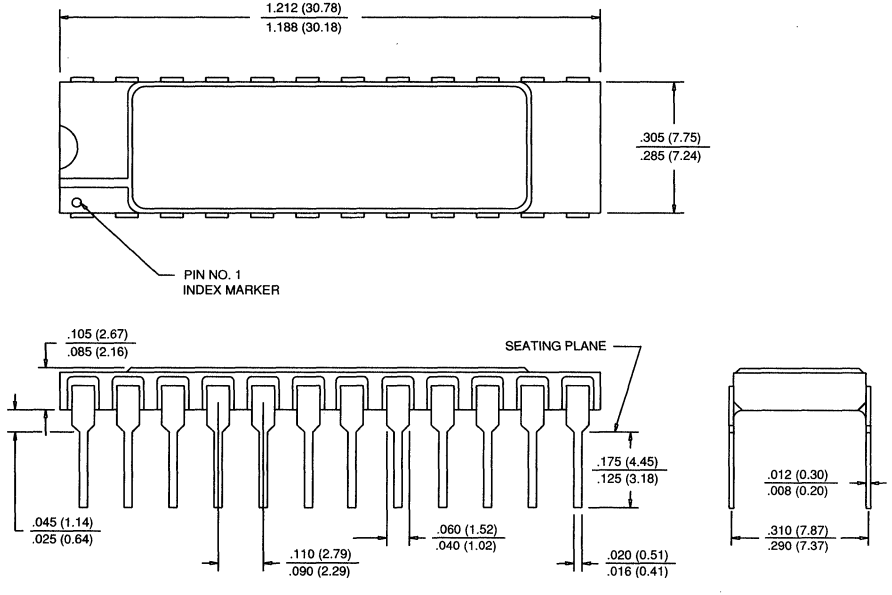
22-PIN CERAMIC DIP

B-6



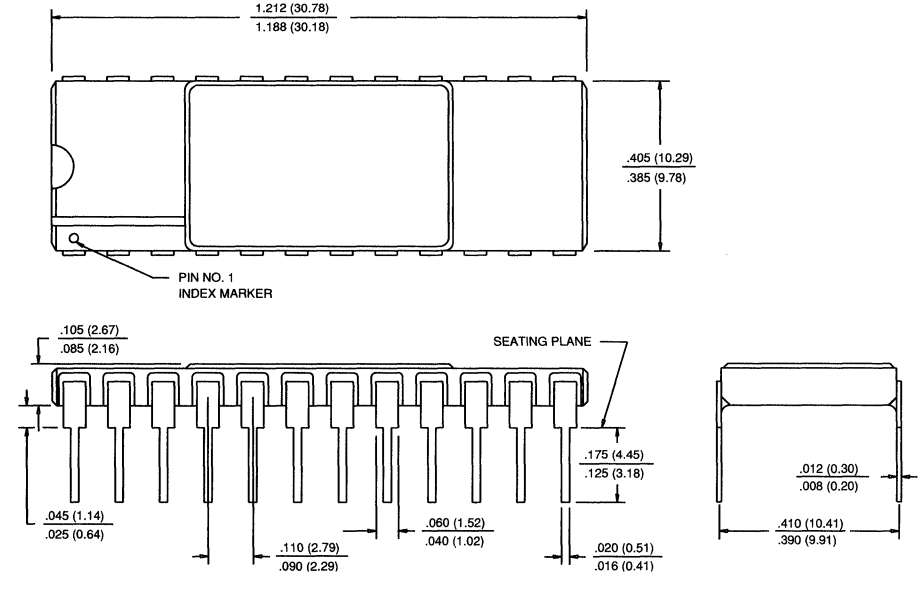
24-PIN CERAMIC DIP

B-7



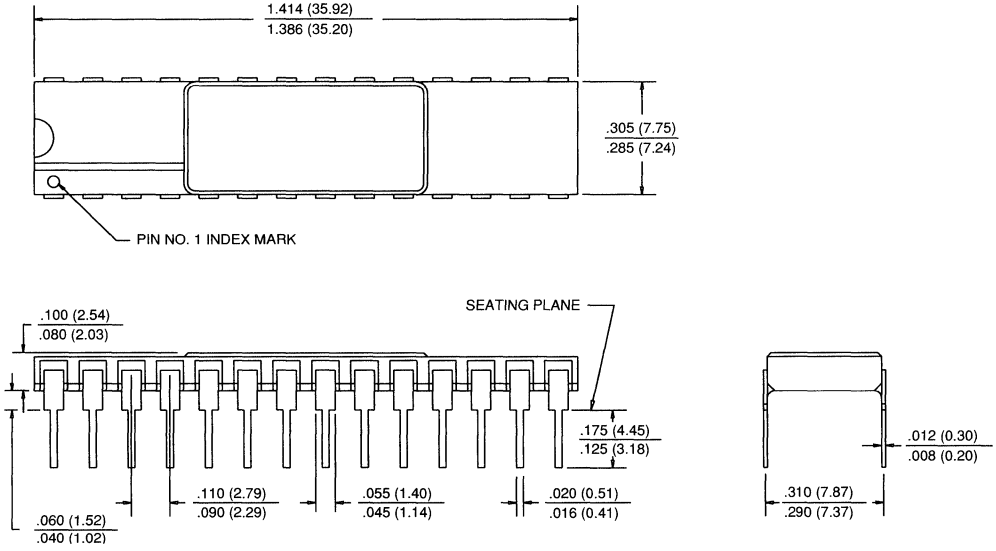
24-PIN CERAMIC DIP

B-8



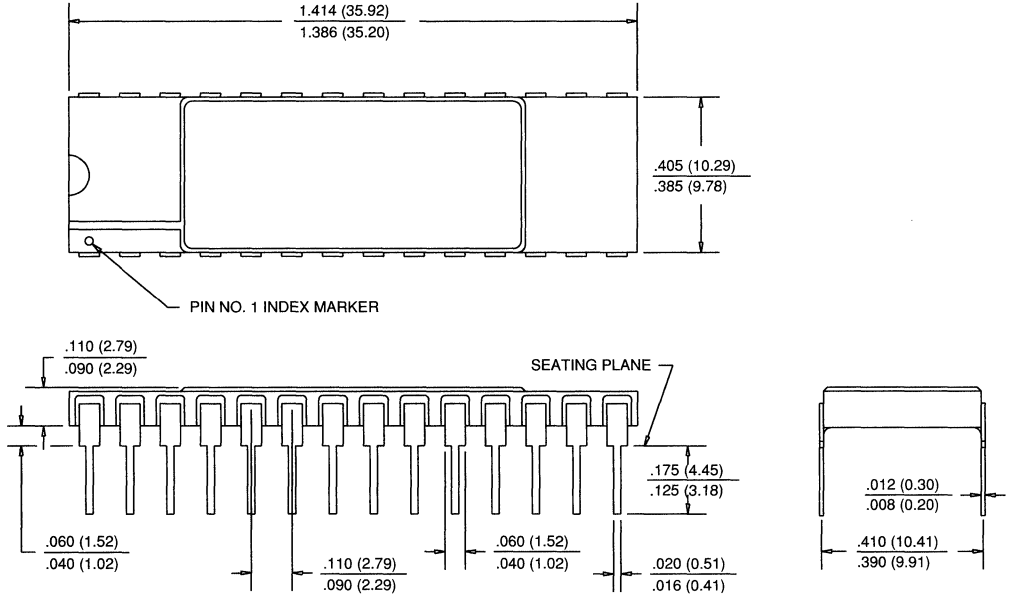
28-PIN CERAMIC DIP

B-9



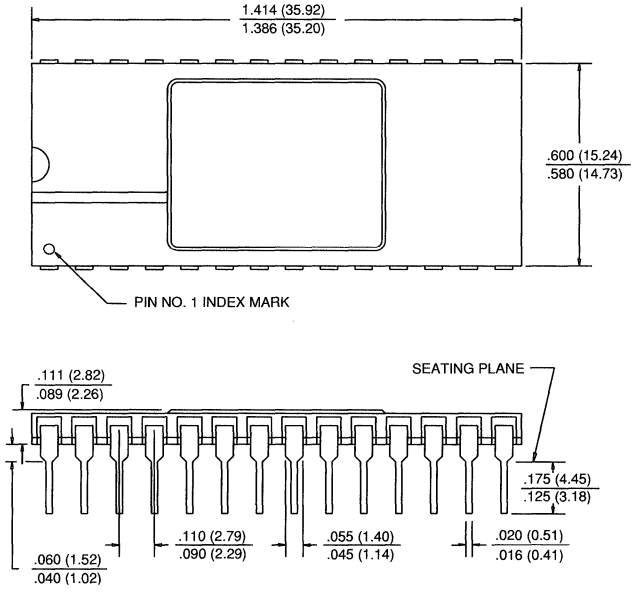
28-PIN CERAMIC DIP

B-10



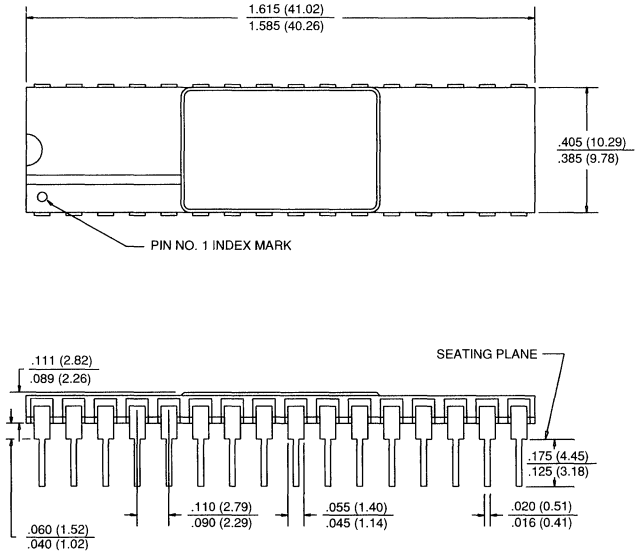
28-PIN CERAMIC DIP

B-11



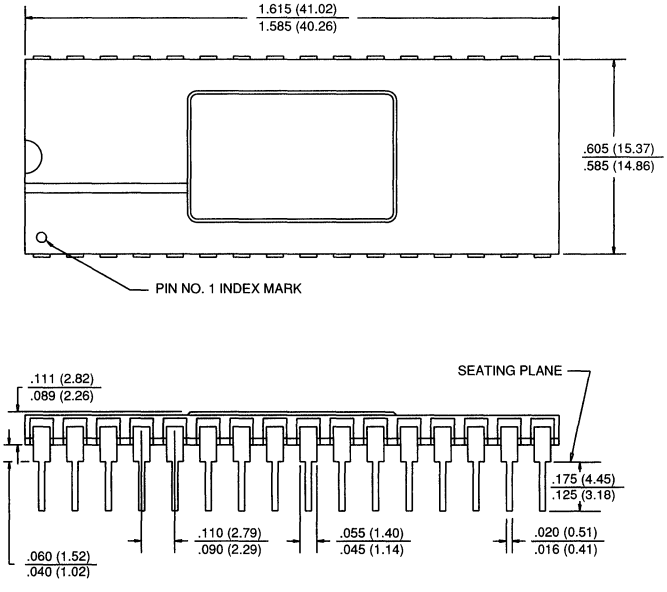
32-PIN CERAMIC DIP

B-12



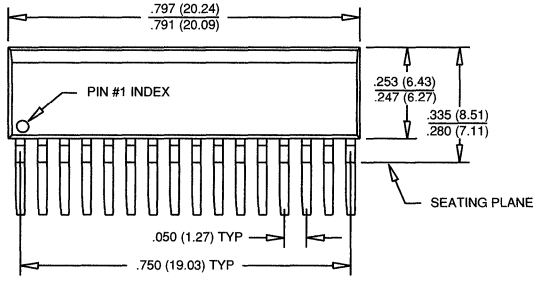
32-PIN CERAMIC DIP

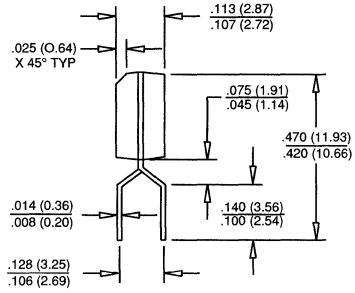
B-13

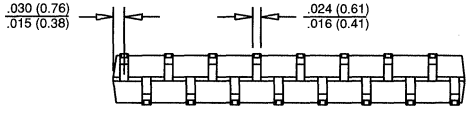


16-PIN PLASTIC ZIP

C-1

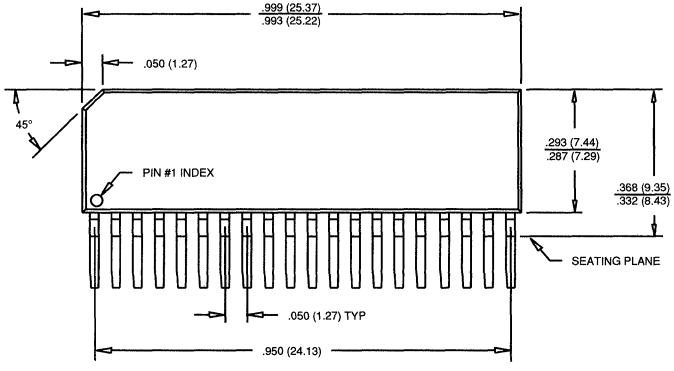


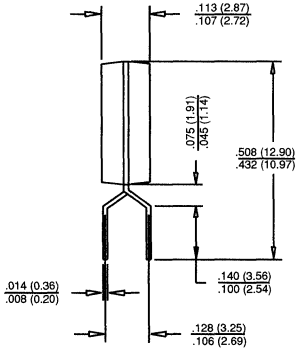


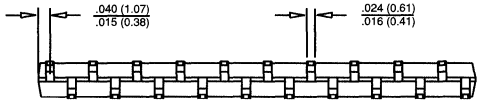


20-PIN PLASTIC ZIP

C-2







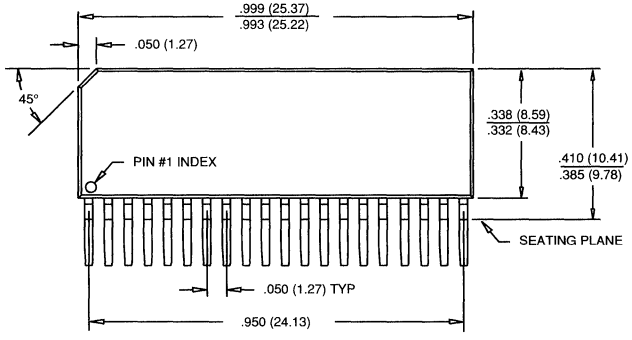
All dimensions in inches (millimeters) $\frac{\text{Max}}{\text{Min}}$ or typical where noted.

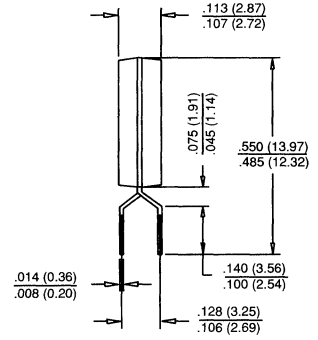
NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

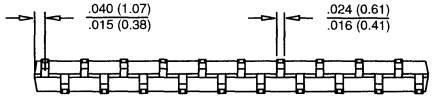
PACKAGE INFORMATION

20-PIN PLASTIC ZIP

C-3

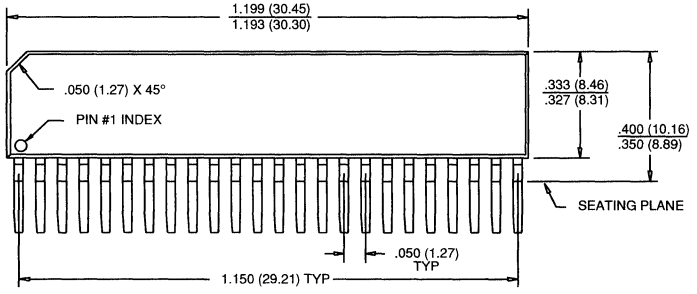


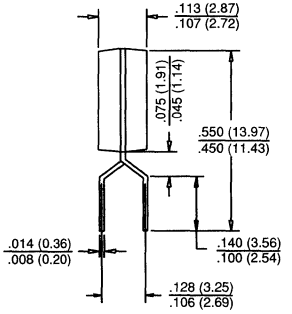


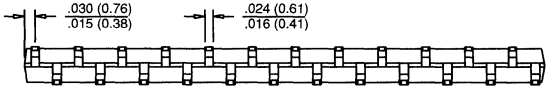


24-PIN PLASTIC ZIP

C-4



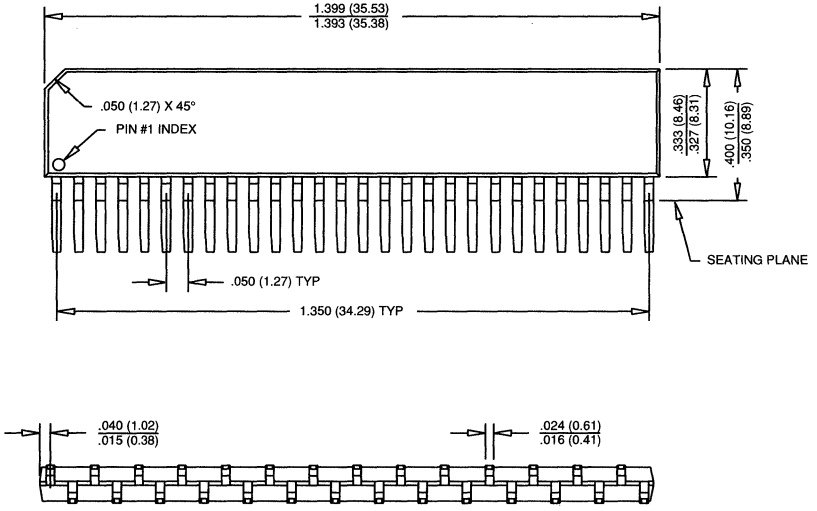




NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

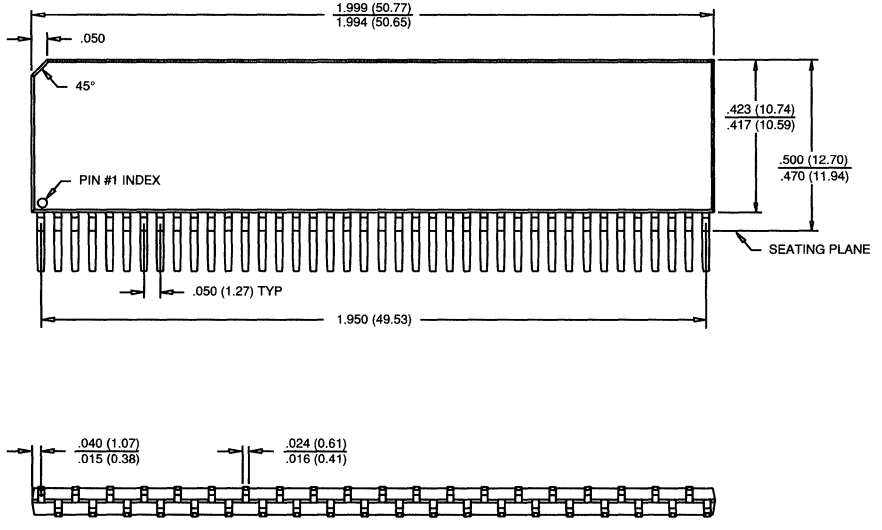
28-PIN PLASTIC ZIP

C-5



40-PIN PLASTIC ZIP

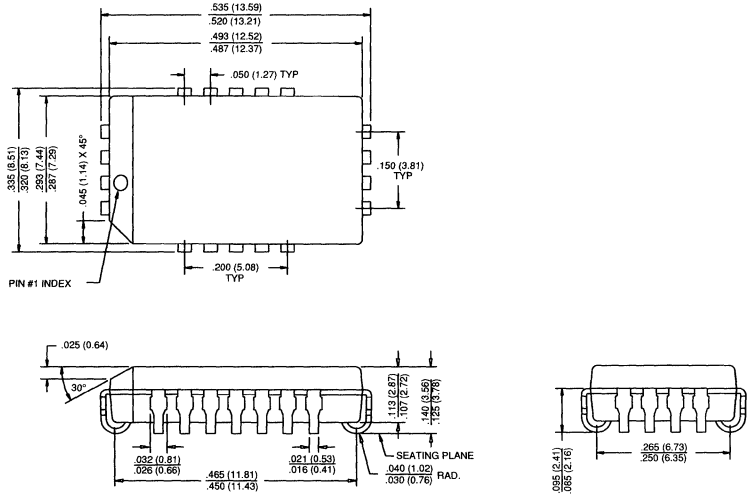
C-6



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

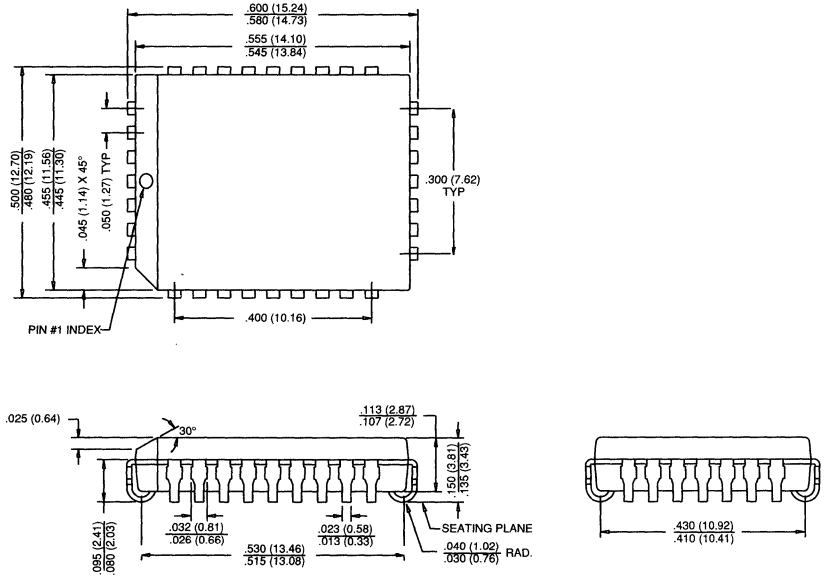
18-PIN PLCC

D-1



32-PIN PLCC

D-2

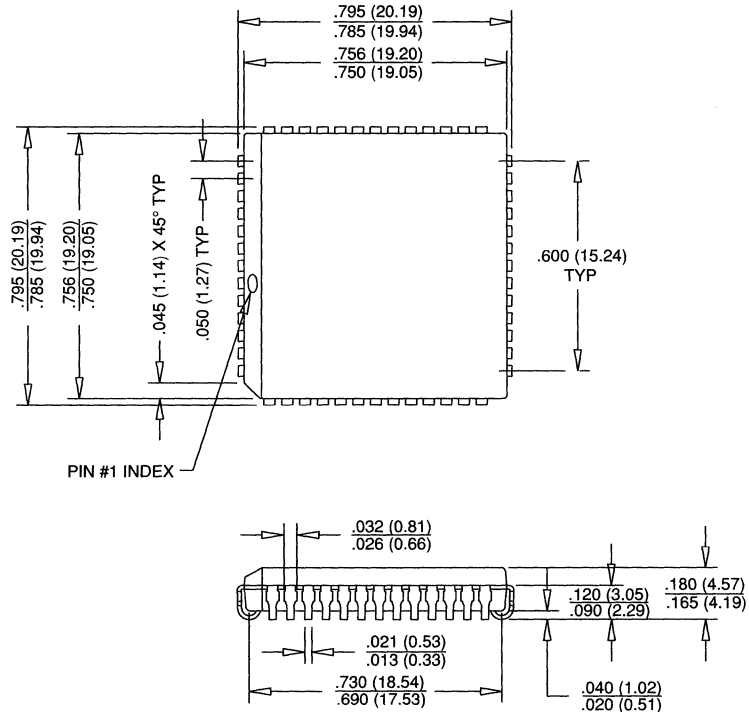


All dimensions in inches (millimeters) $\frac{\text{Max}}{\text{Min}}$ or typical where noted.

NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

52-PIN PLCC

D-3

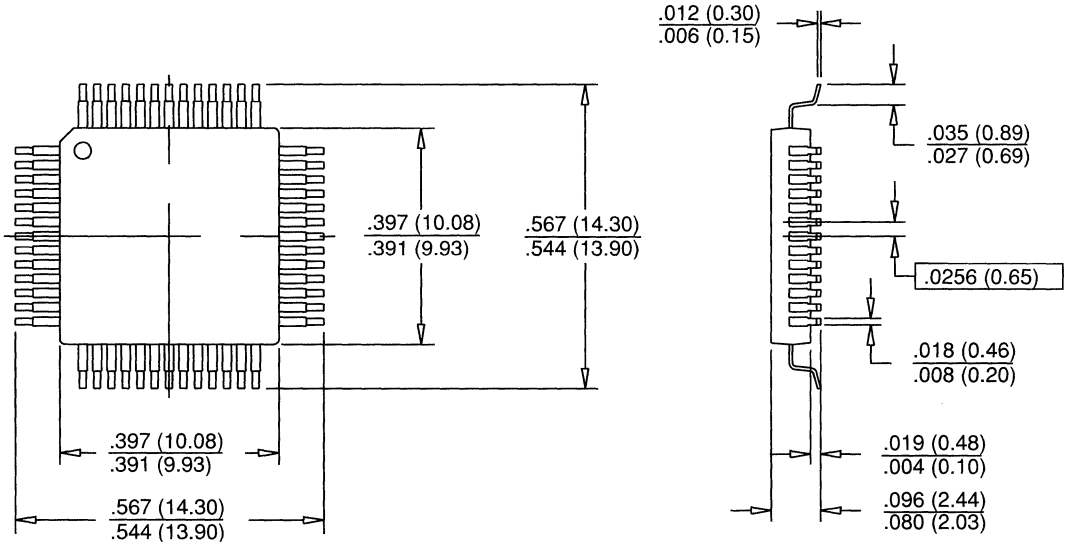


PACKAGE INFORMATION

NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

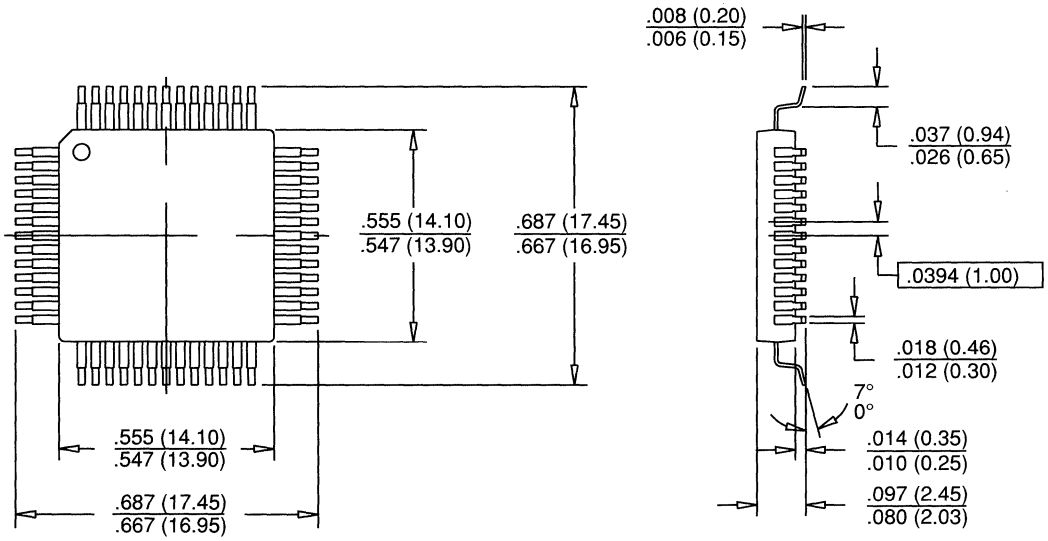
52-PIN LPQFP

D-4



52-PIN LPQFP

D-5

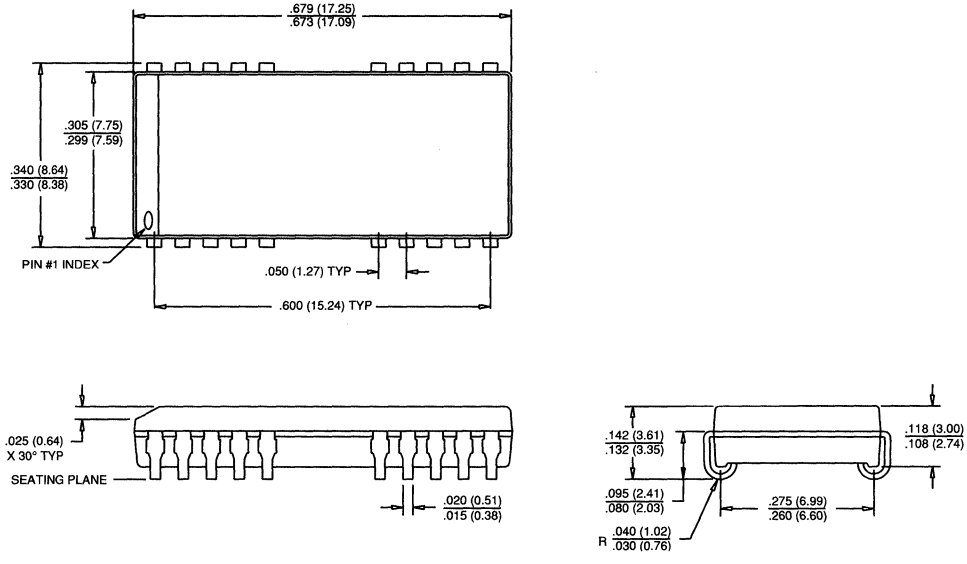


All dimensions in inches (millimeters) $\frac{\text{Max}}{\text{Min}}$ or typical where noted.

NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

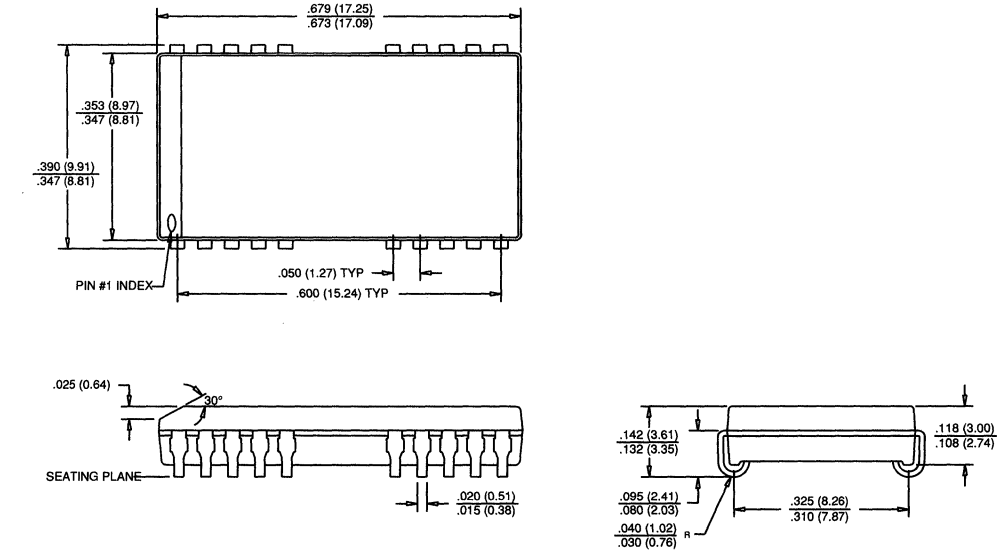
20/26-PIN PLASTIC SOJ

E-1



20/26-PIN PLASTIC SOJ

E-2

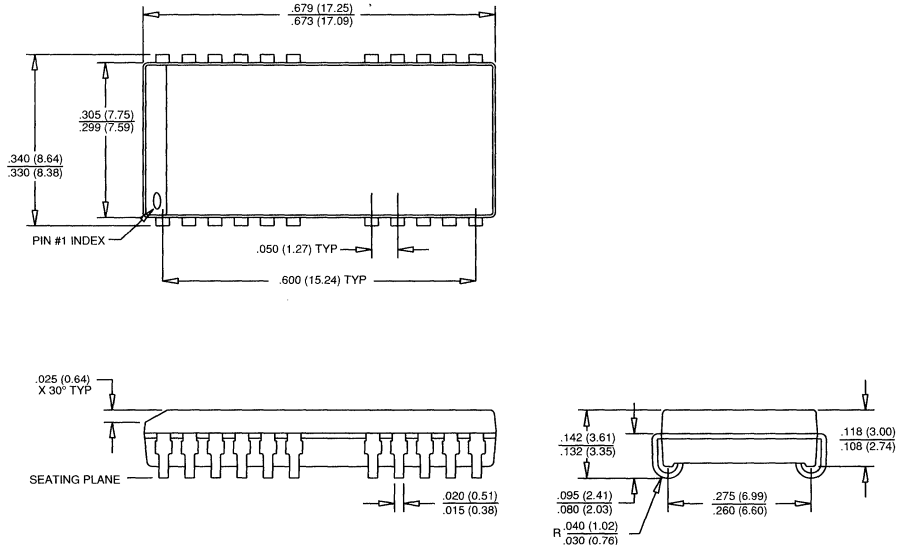


All dimensions in inches (millimeters) $\frac{\text{Max}}{\text{Min}}$ or typical where noted.

NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

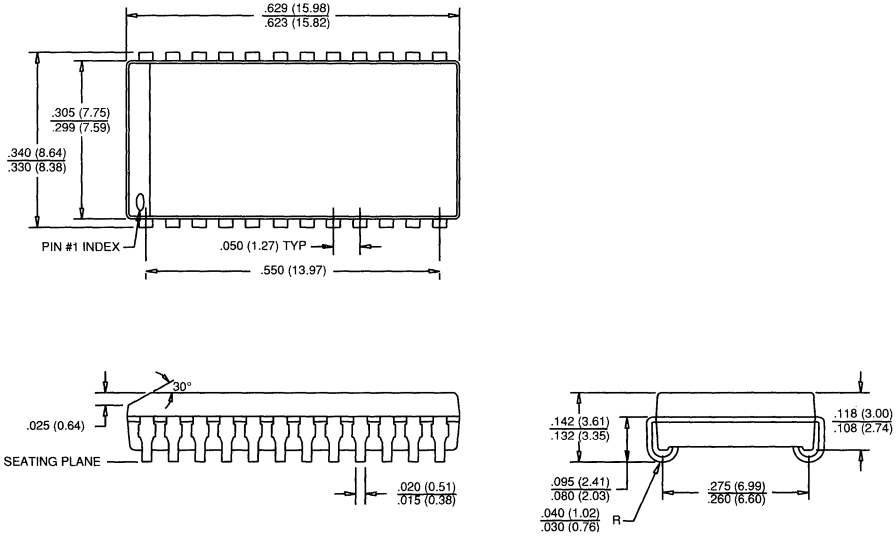
22/26-PIN PLASTIC SOJ

E-3



24-PIN PLASTIC SOJ

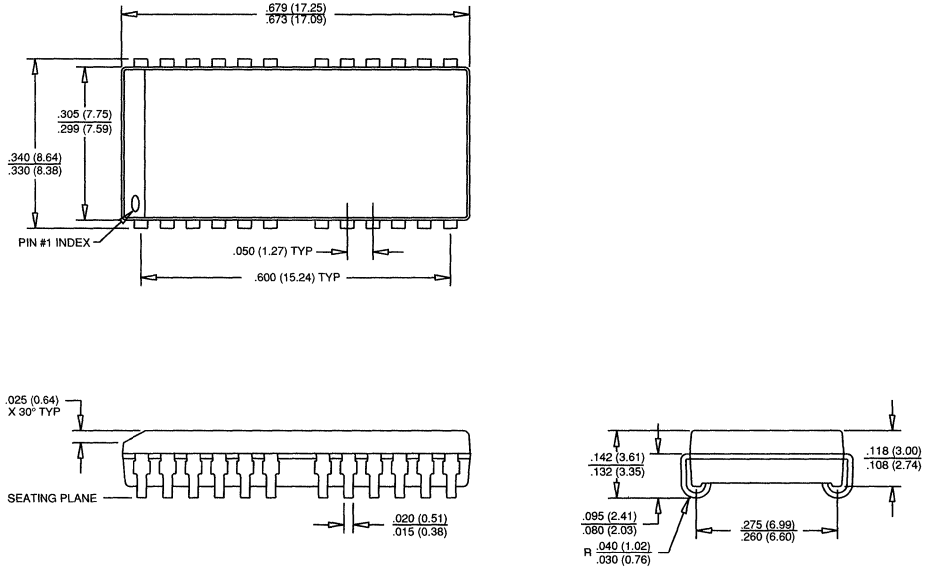
E-4



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

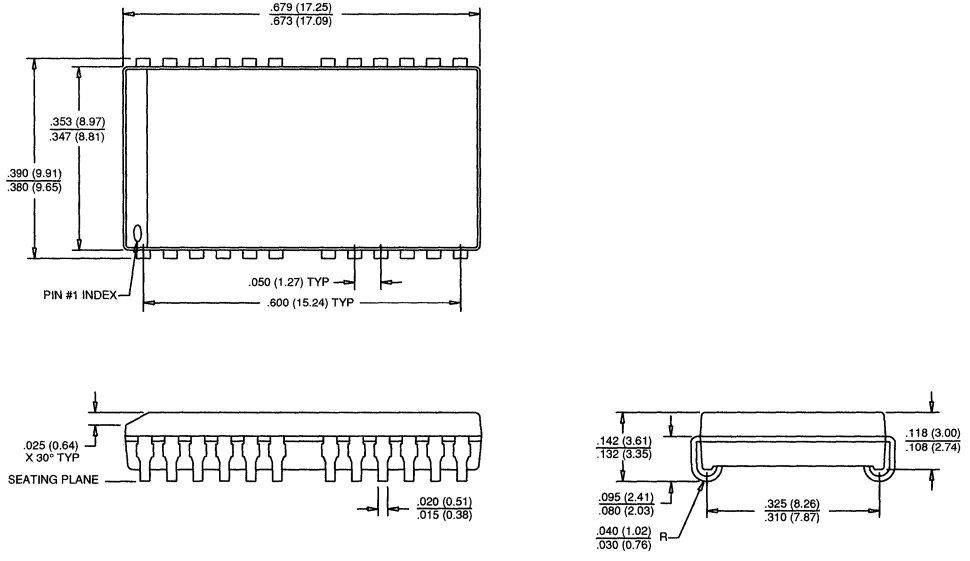
24/26-PIN PLASTIC SOJ

E-5



24/26-PIN PLASTIC SOJ

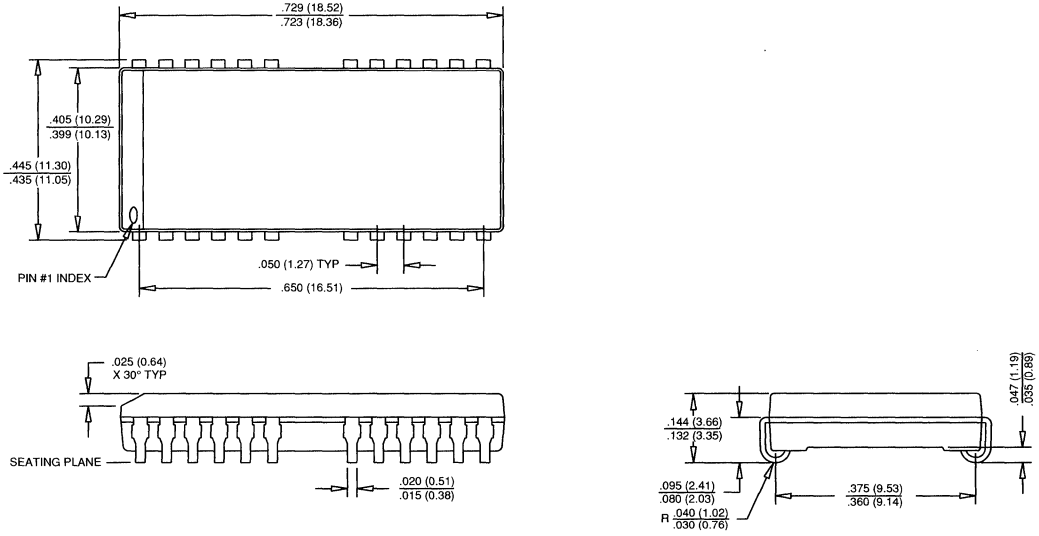
E-6



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

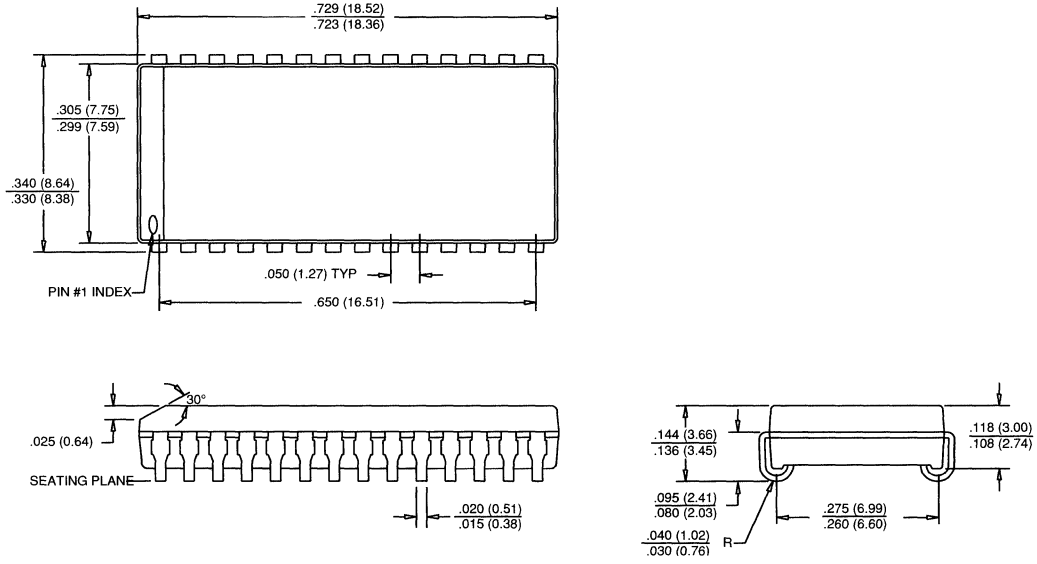
24/28-PIN PLASTIC SOJ

E-7



28-PIN PLASTIC SOJ

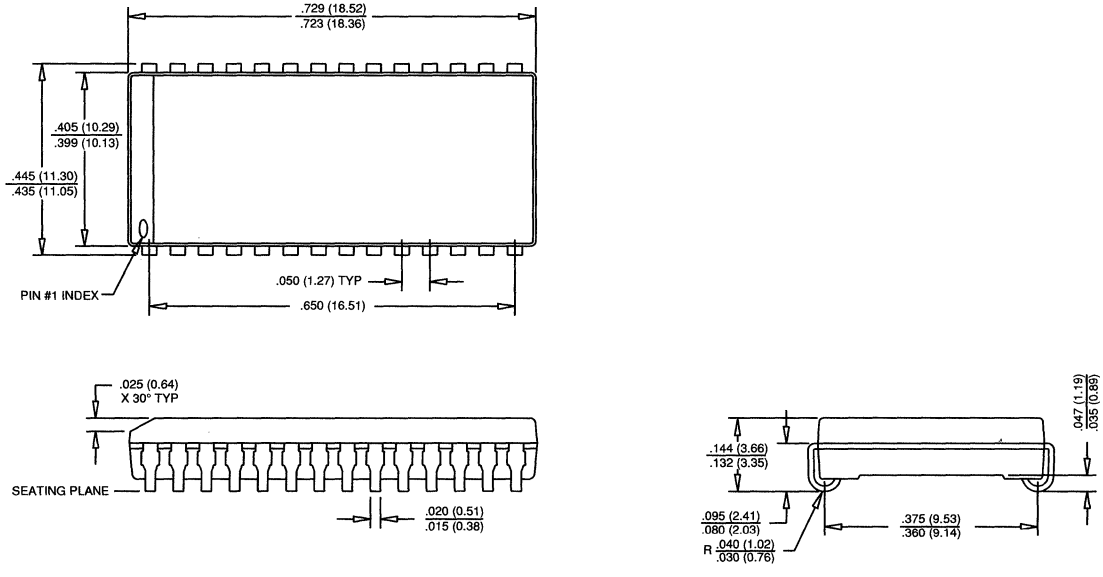
E-8



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

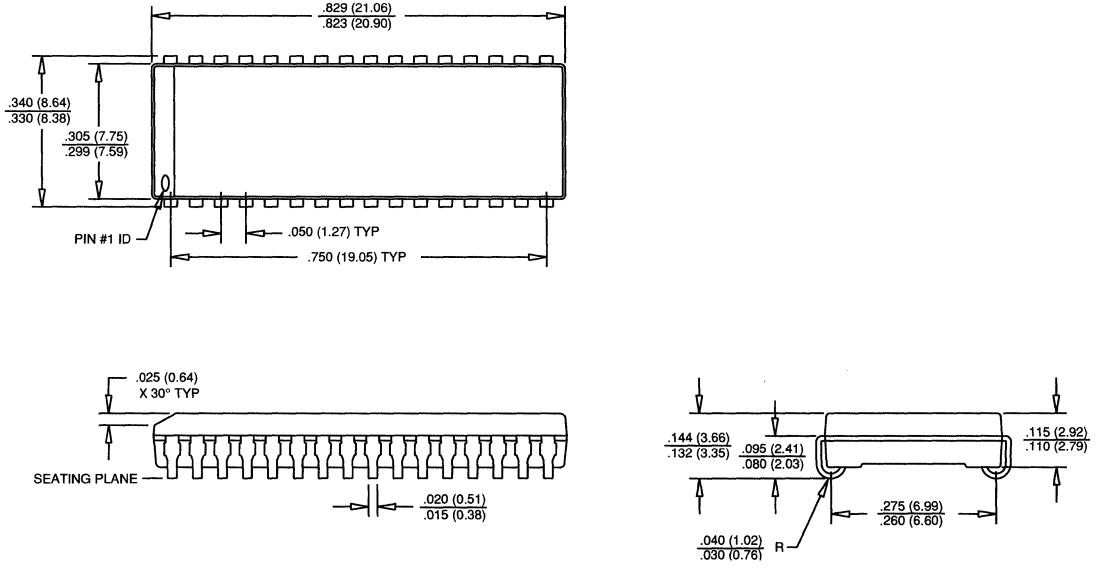
28-PIN PLASTIC SOJ

E-9



32-PIN PLASTIC SOJ

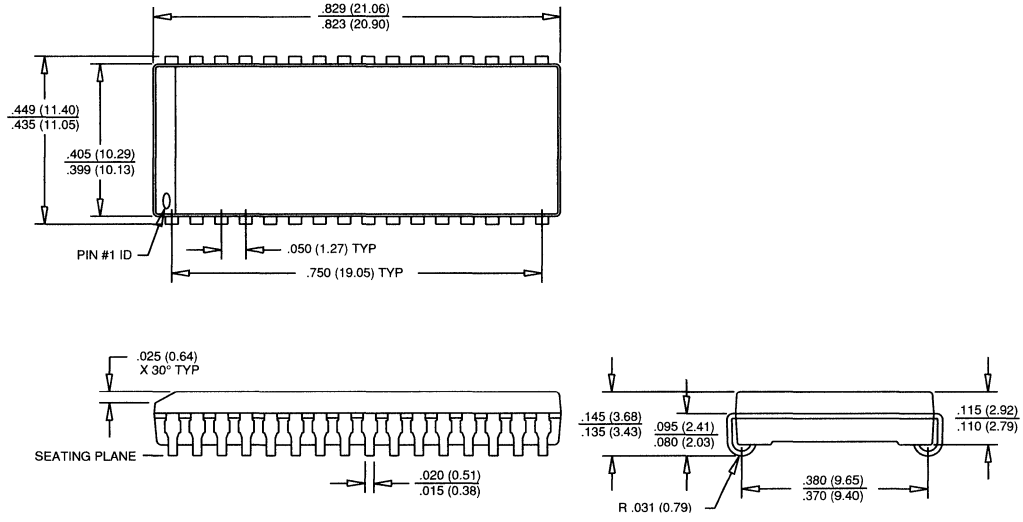
E-10



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

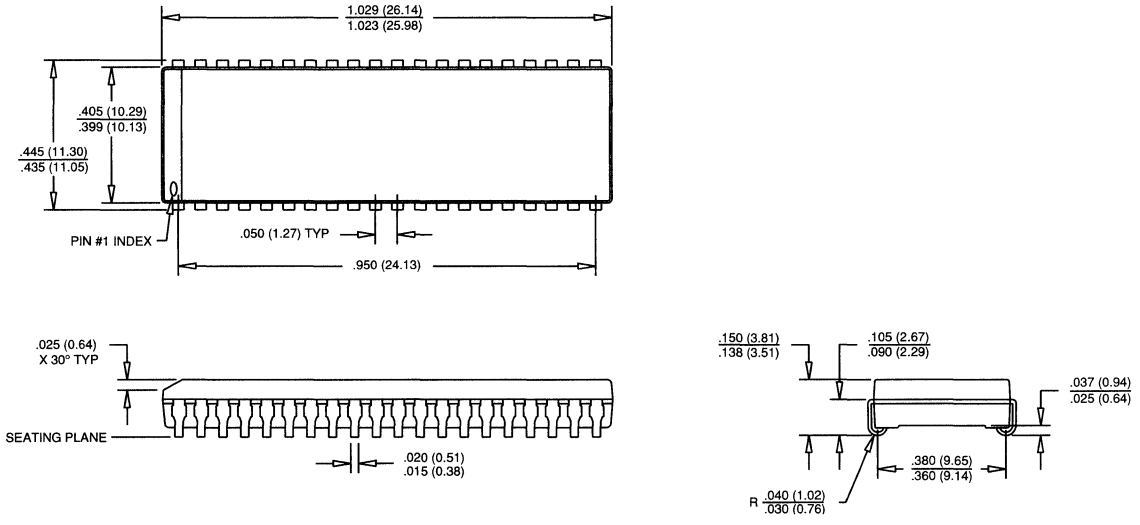
32-PIN PLASTIC SOJ

E-11



40-PIN PLASTIC SOJ

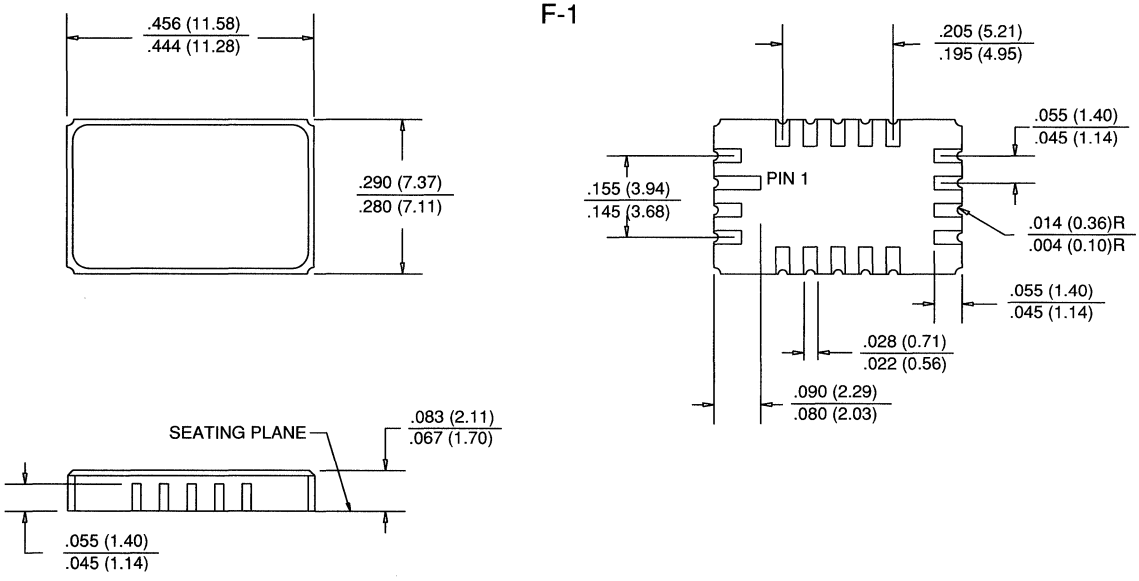
E-12



NOTE: Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

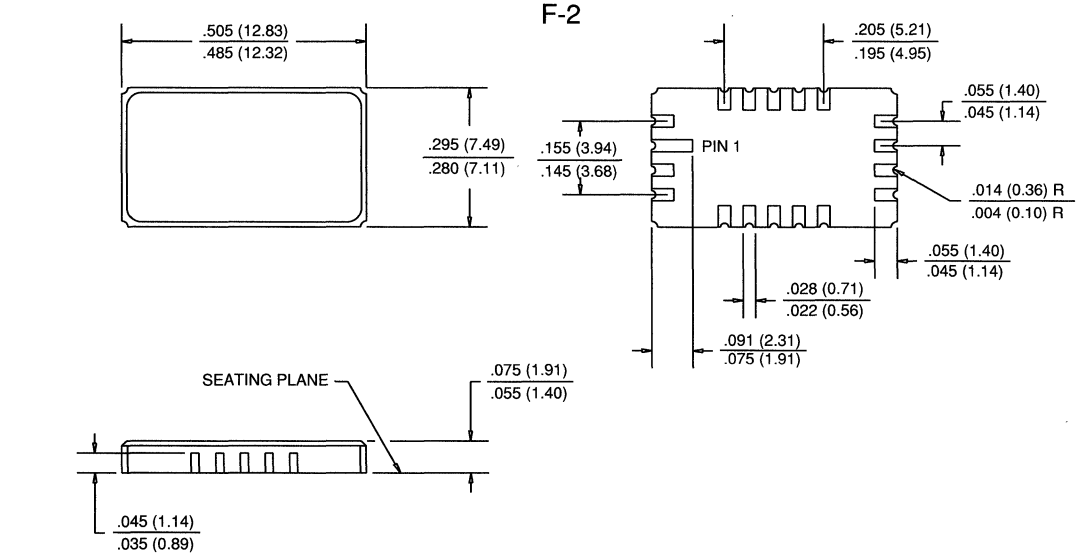
18-PIN CERAMIC LCC

F-1



18-PIN CERAMIC LCC

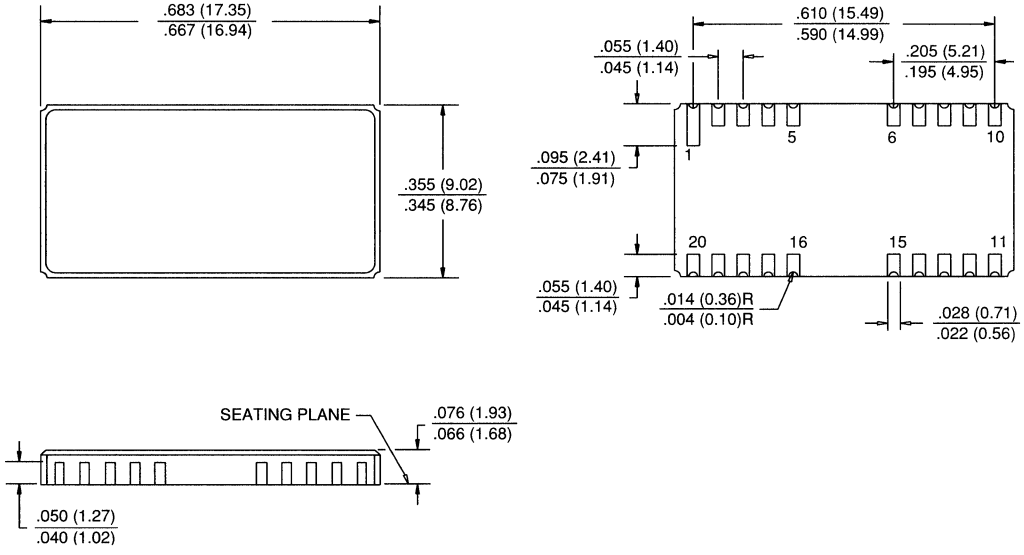
F-2



All dimensions in inches (millimeters) $\frac{\text{Max}}{\text{Min}}$ or typical where noted.

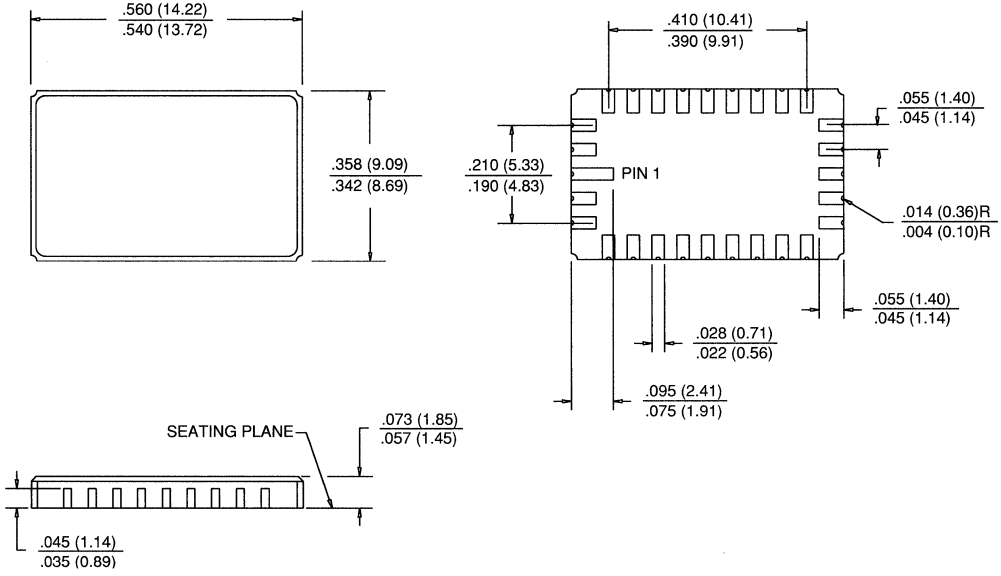
20-PIN CERAMIC LCC

F-3



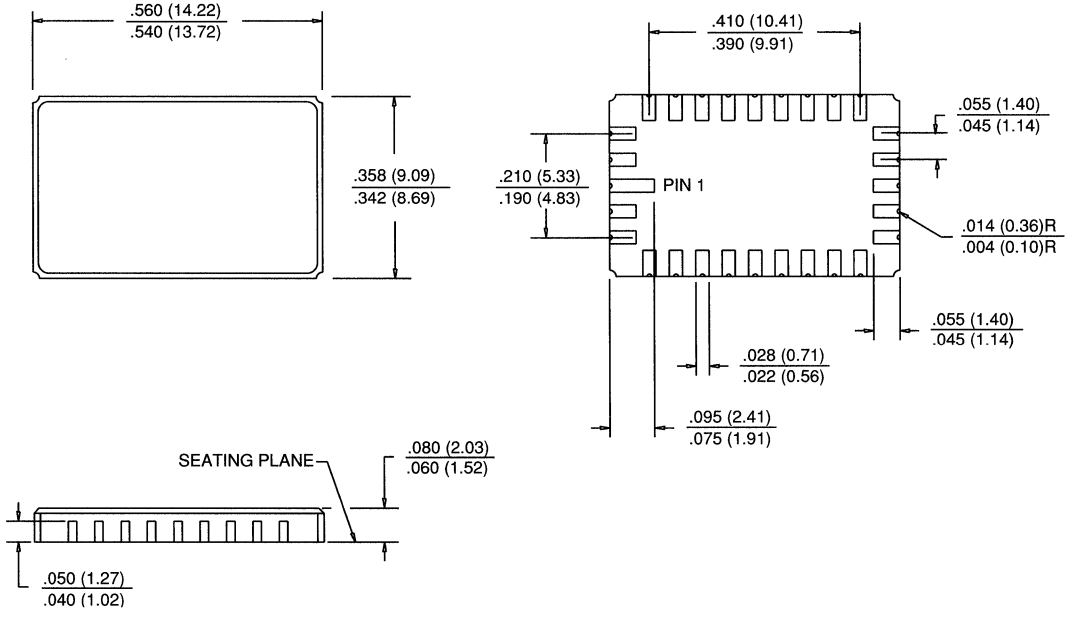
28-PIN CERAMIC LCC

F-4



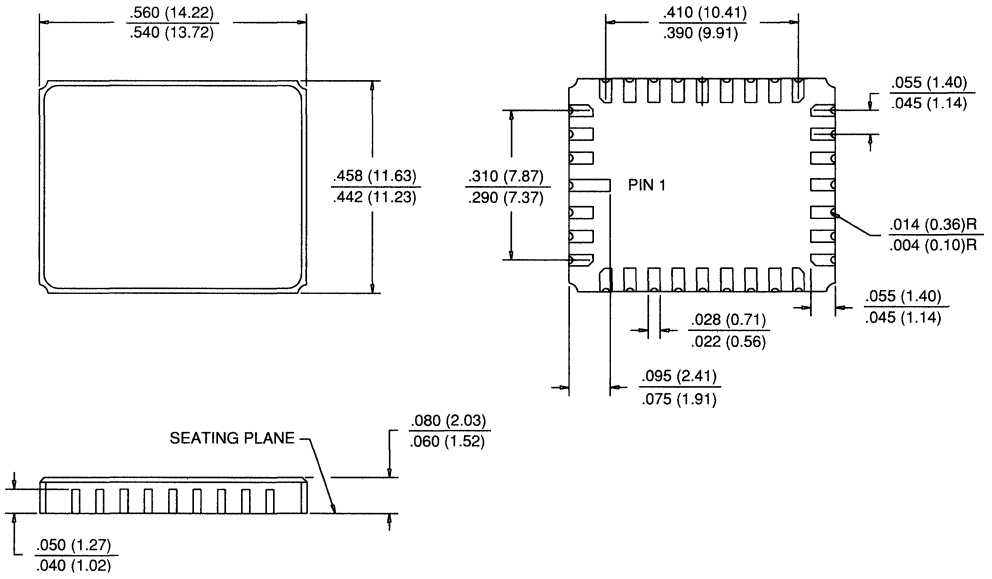
28-PIN CERAMIC LCC

F-5



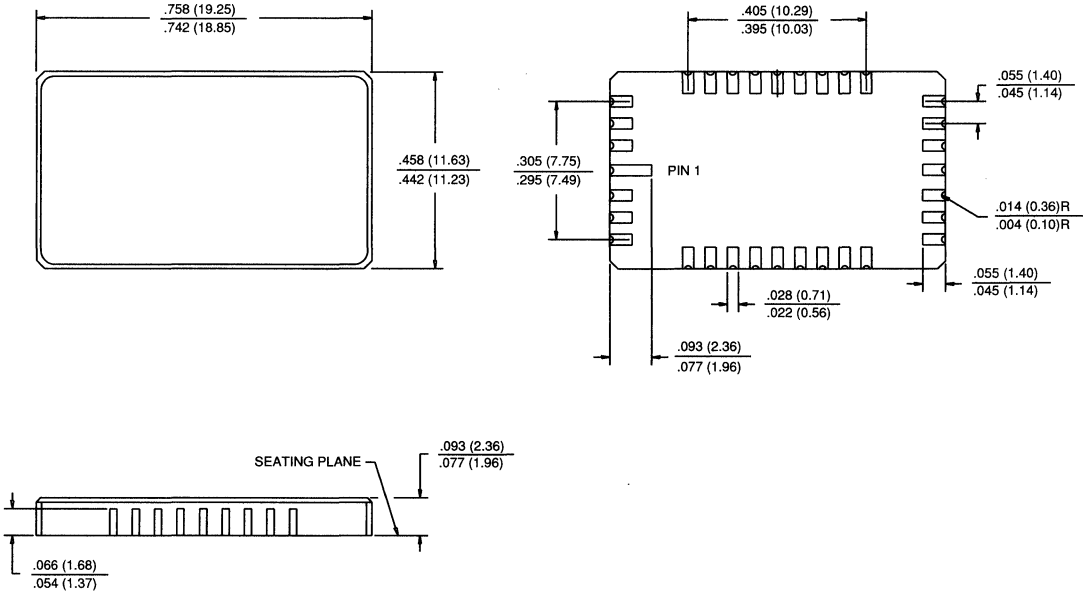
32-PIN CERAMIC LCC

F-6



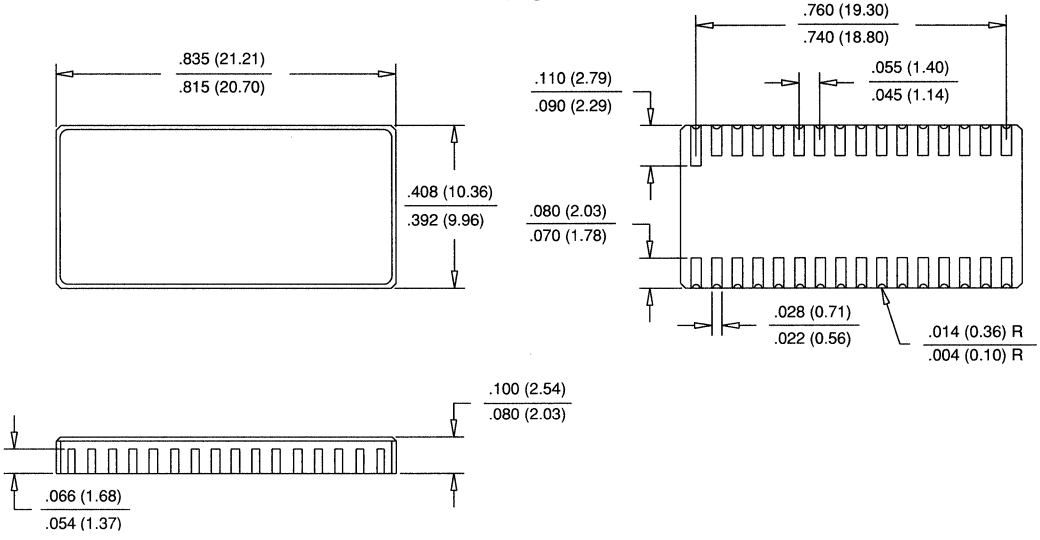
32-PIN CERAMIC LCC

F-7



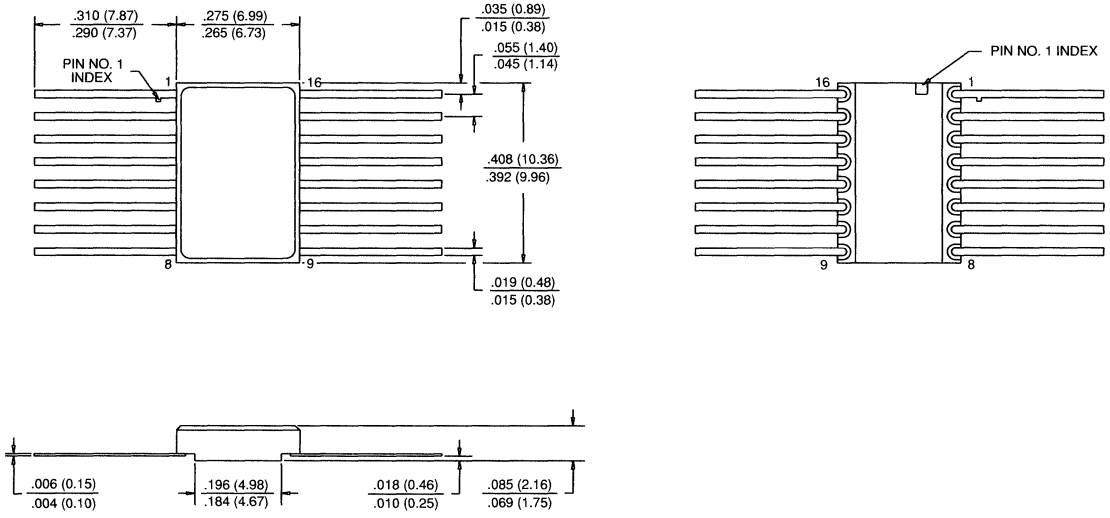
32-PIN CERAMIC LCC

F-8



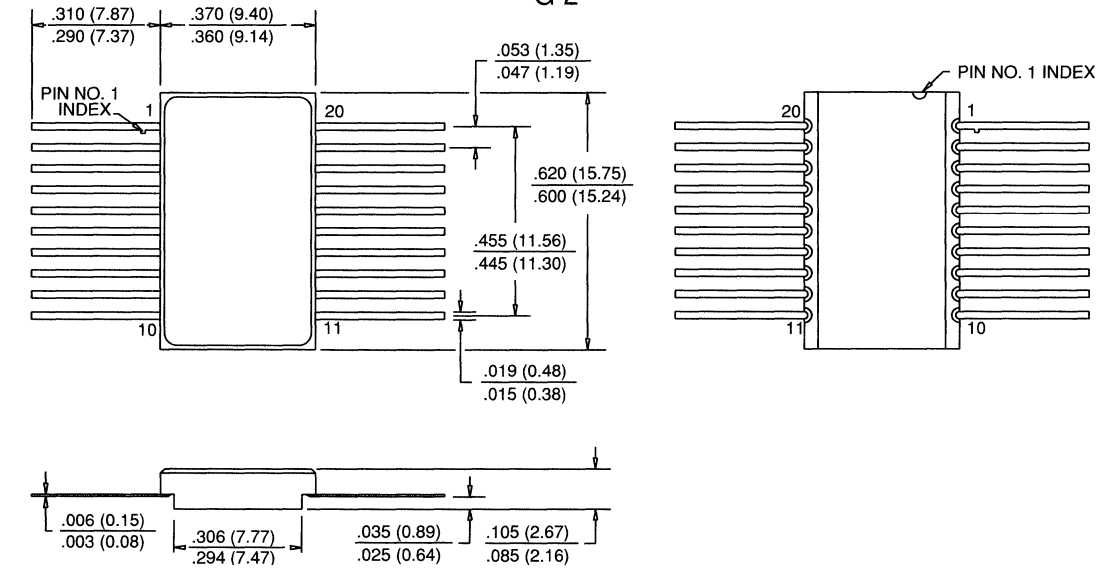
16-PIN FLAT PACK

G-1



20-PIN FLAT PACK

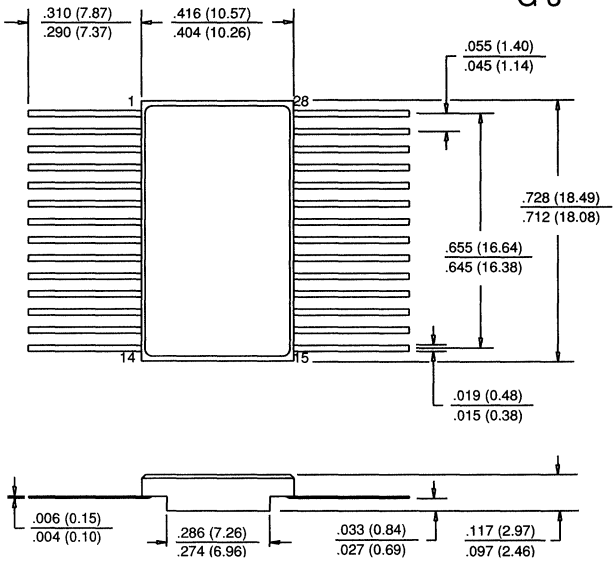
G-2

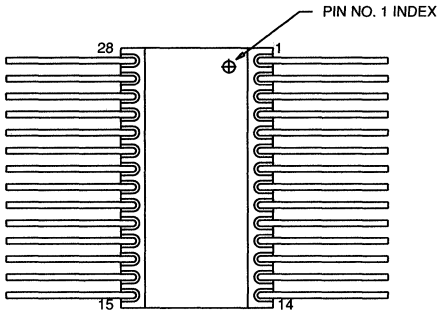


All dimensions in inches (millimeters) $\frac{\text{Max}}{\text{Min}}$ or typical where noted.

28-PIN FLAT PACK

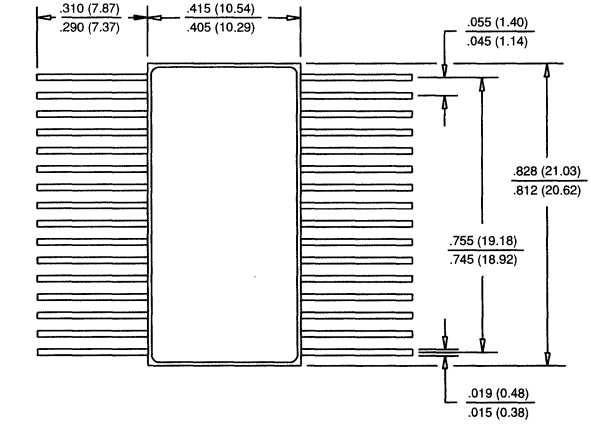
G-3

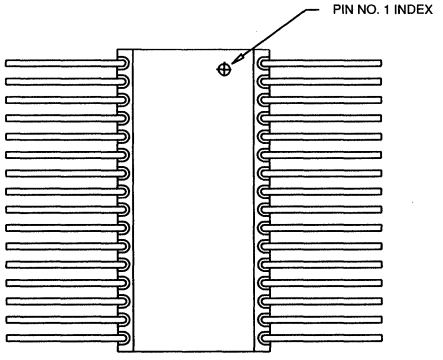




32-PIN FLAT PACK

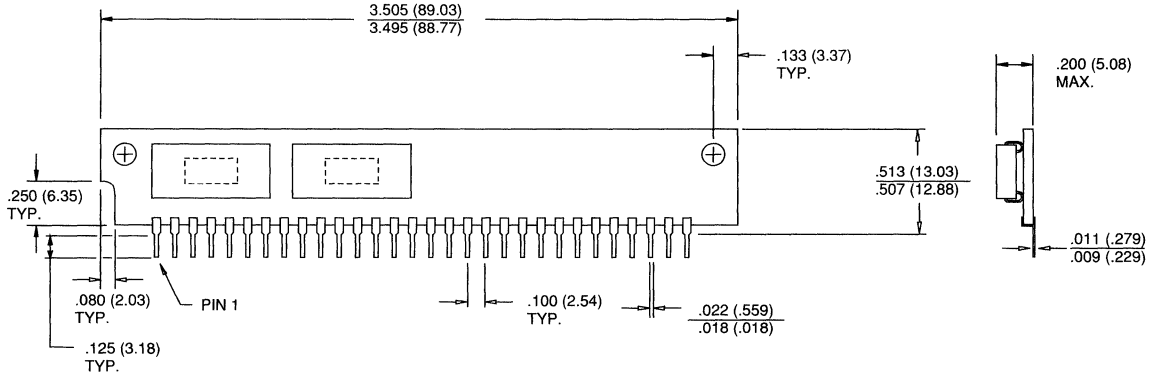
G-4





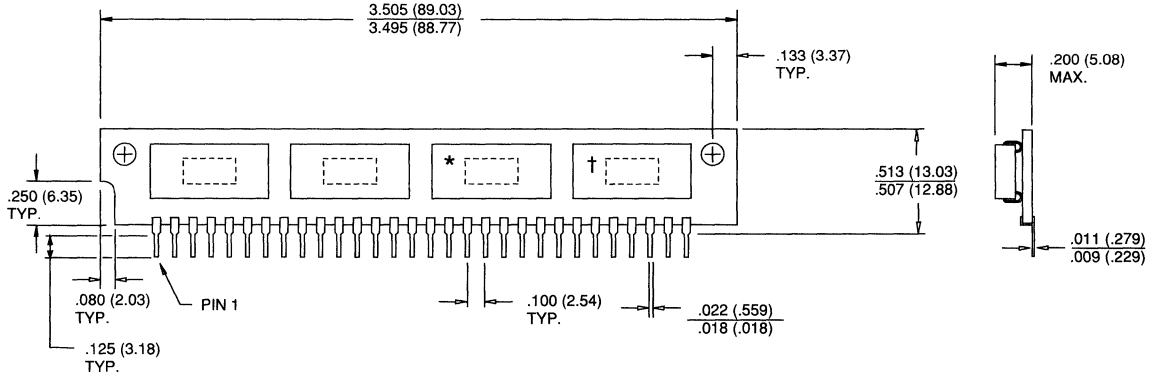
30-PIN MODULE SIP

H-1



30-PIN MODULE SIP

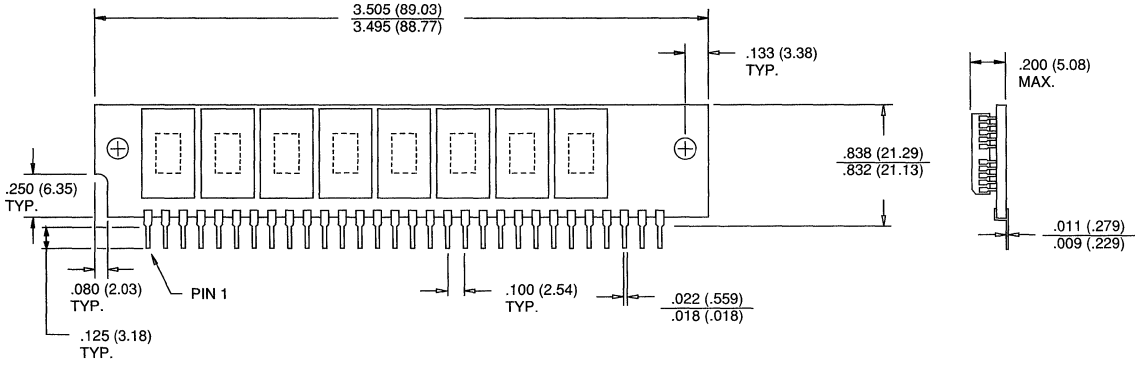
H-2



All dimensions in inches (millimeters) $\frac{\text{Max}}{\text{Min}}$ or typical where noted.

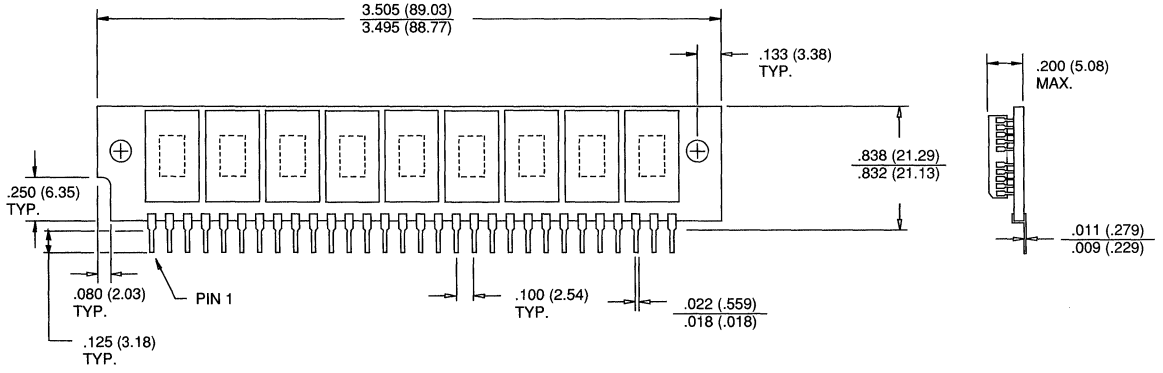
30-PIN MODULE SIP

H-3



30-PIN MODULE SIP

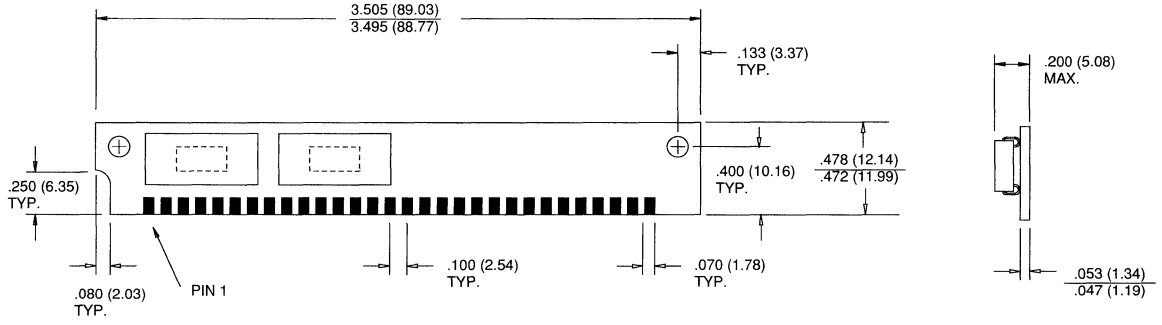
H-4



PACKAGE INFORMATION

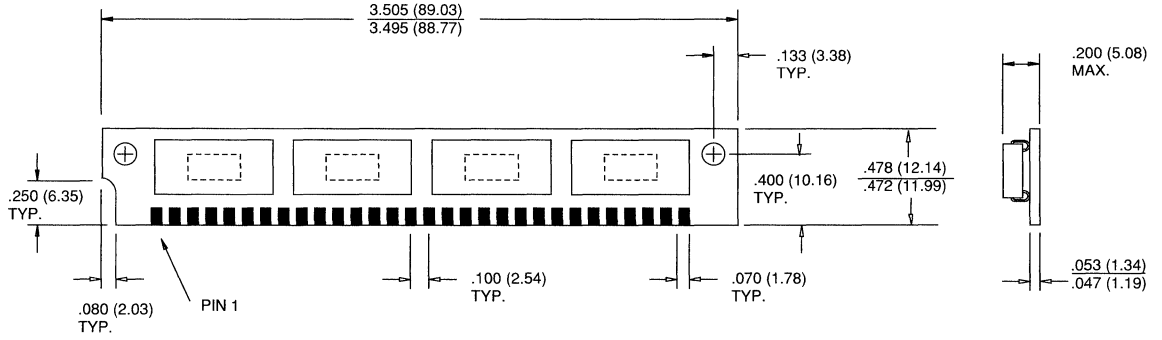
30-PIN MODULE SIMM

I-1



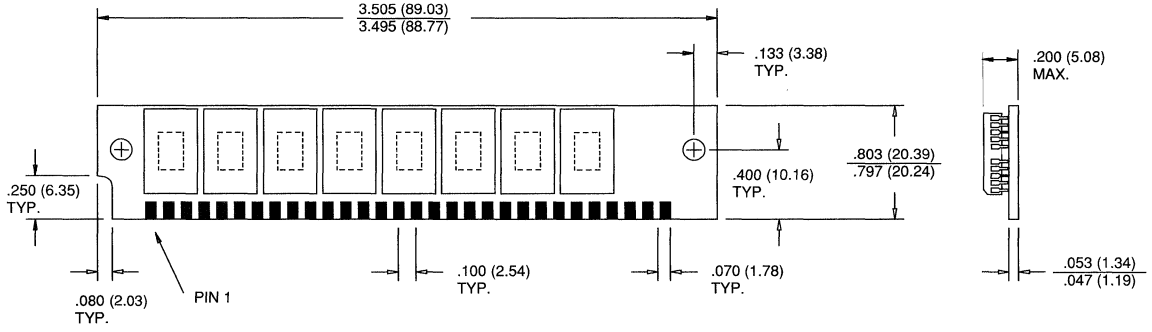
30-PIN MODULE SIMM

I-2



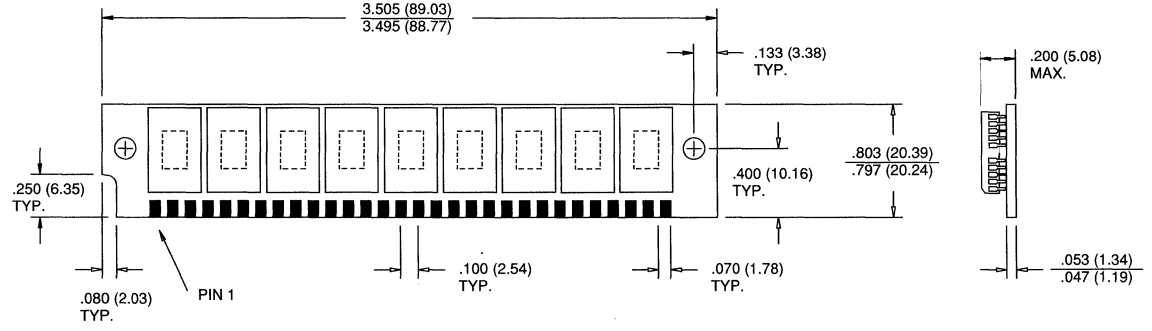
30-PIN MODULE SIMM

I-3



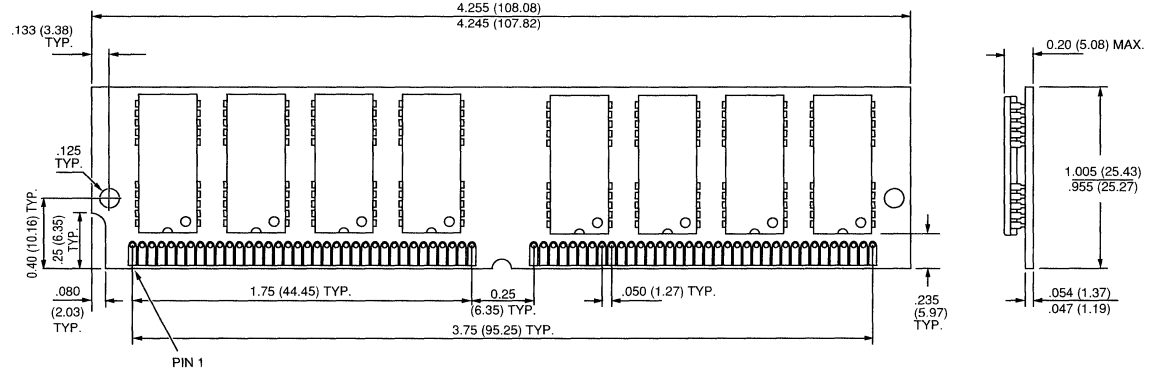
30-PIN MODULE SIMM

I-4



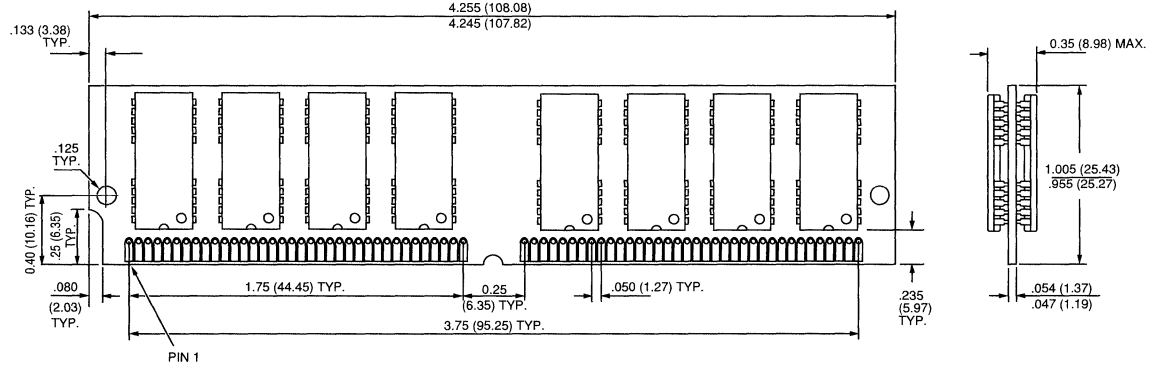
72-PIN MODULE SIMM

I-5



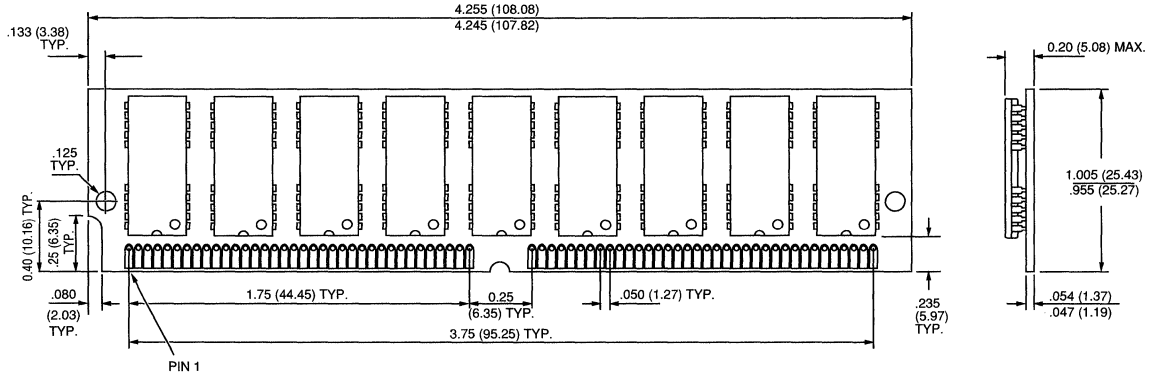
72-PIN MODULE SIMM

I-6



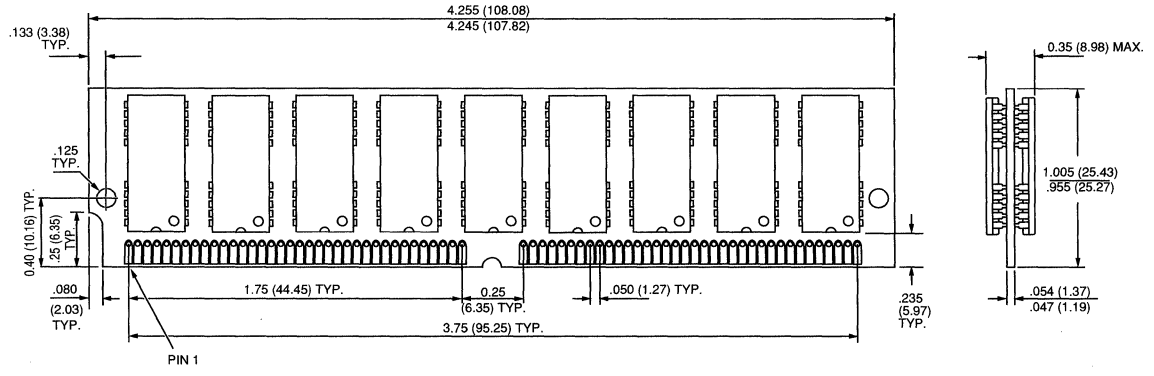
72-PIN MODULE SIMM

I-7



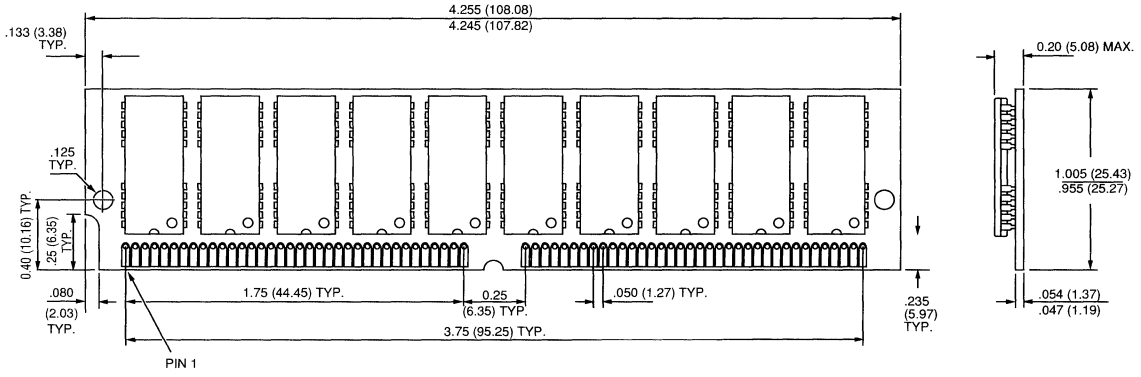
72-PIN MODULE SIMM

I-8



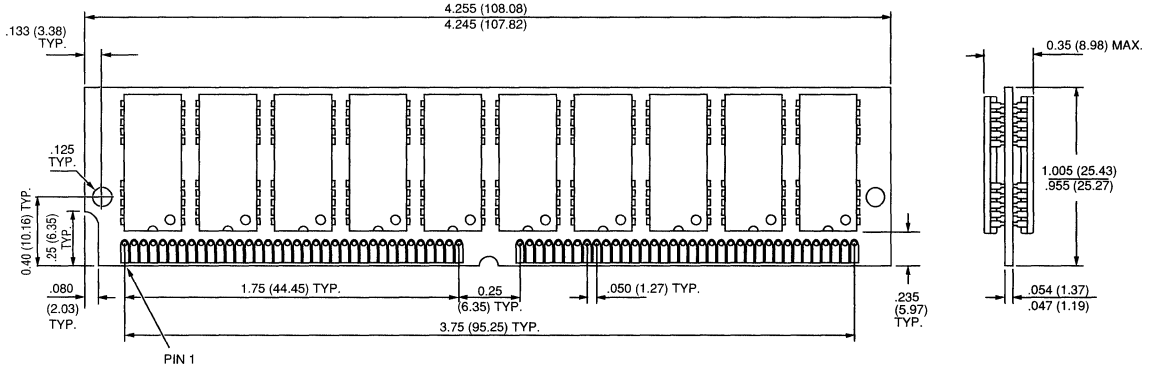
72-PIN MODULE SIMM

I-9



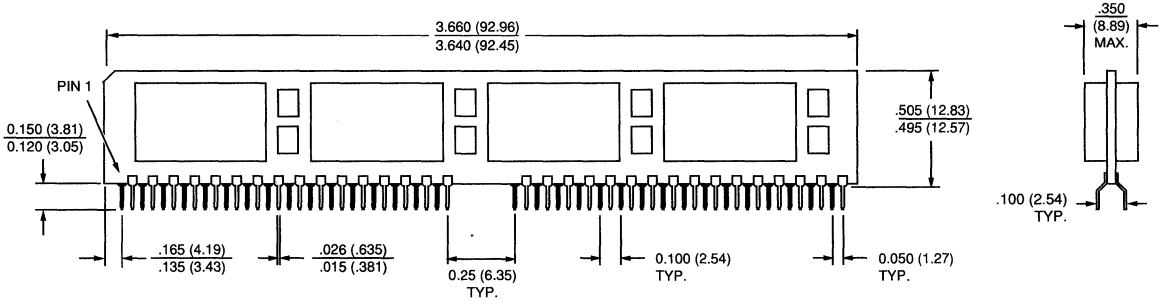
72-PIN MODULE SIMM

I-10



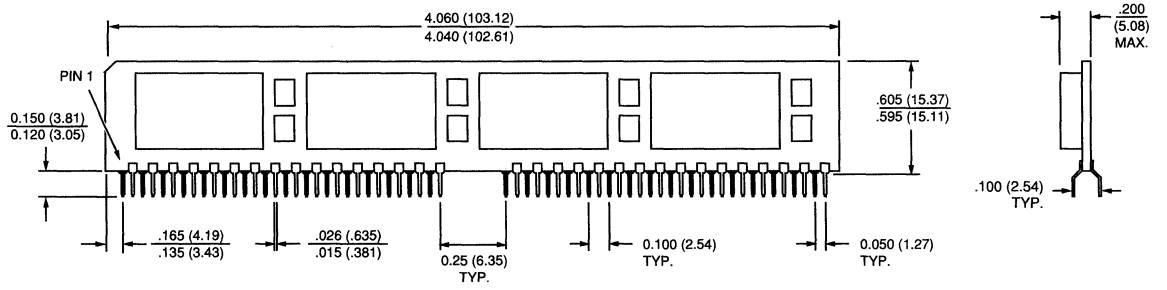
64-PIN MODULE ZIP

J-1



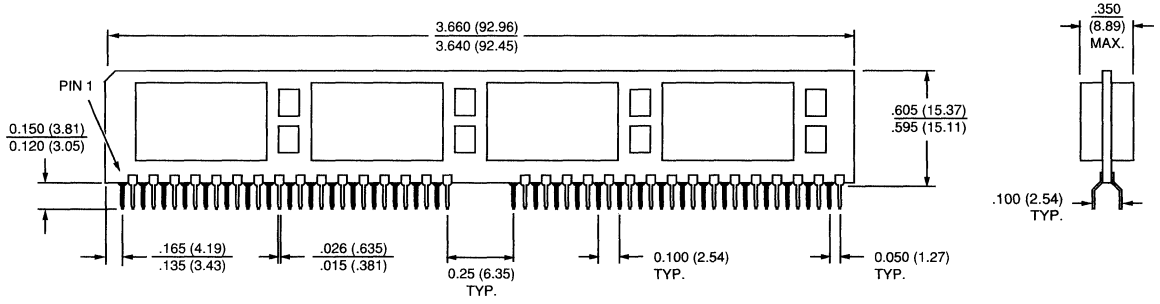
64-PIN MODULE ZIP

J-2



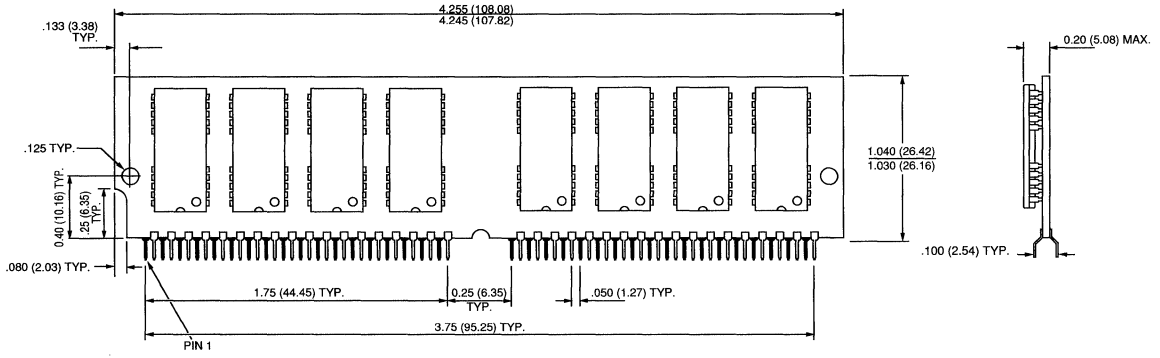
64-PIN MODULE ZIP

J-3



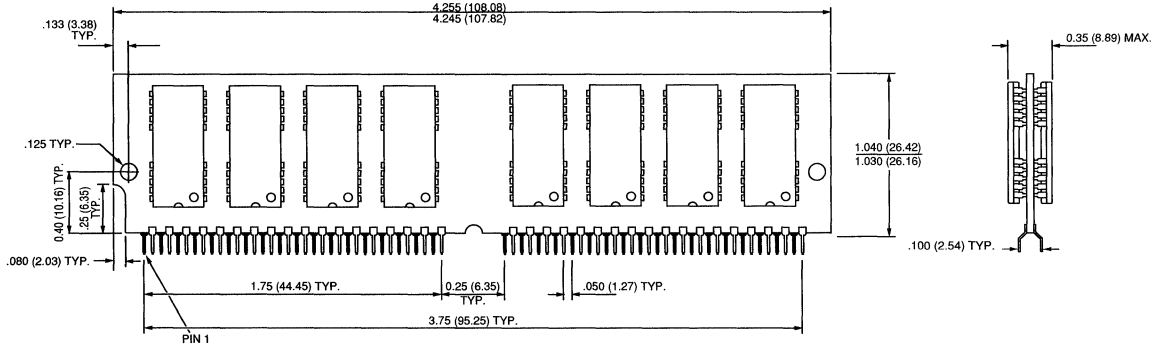
72-PIN MODULE ZIP

J-4



72-PIN MODULE ZIP

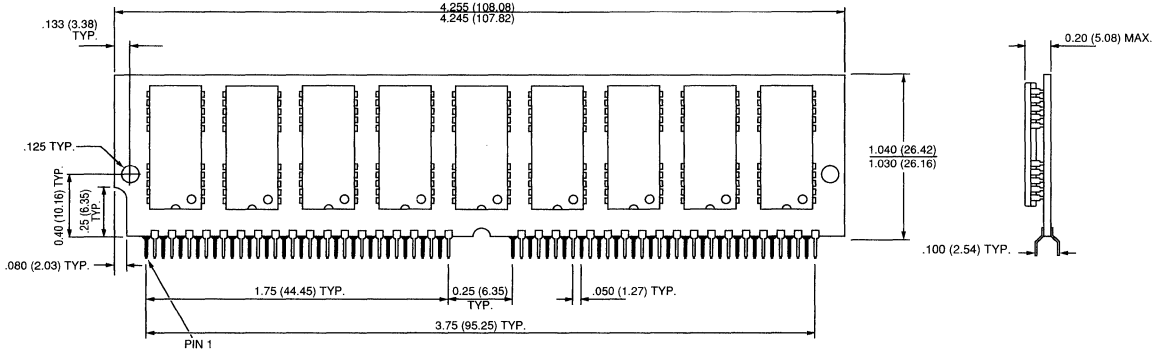
J-5



PACKAGE INFORMATION

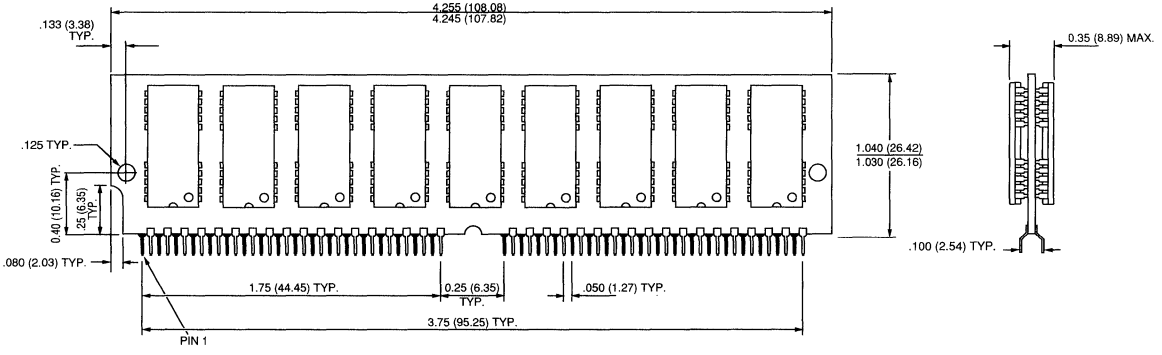
72-PIN MODULE ZIP

J-6



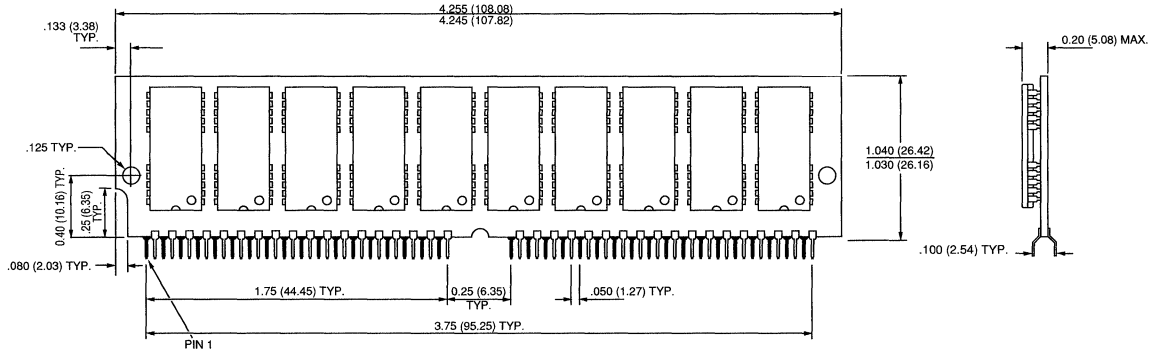
72-PIN MODULE ZIP

J-7



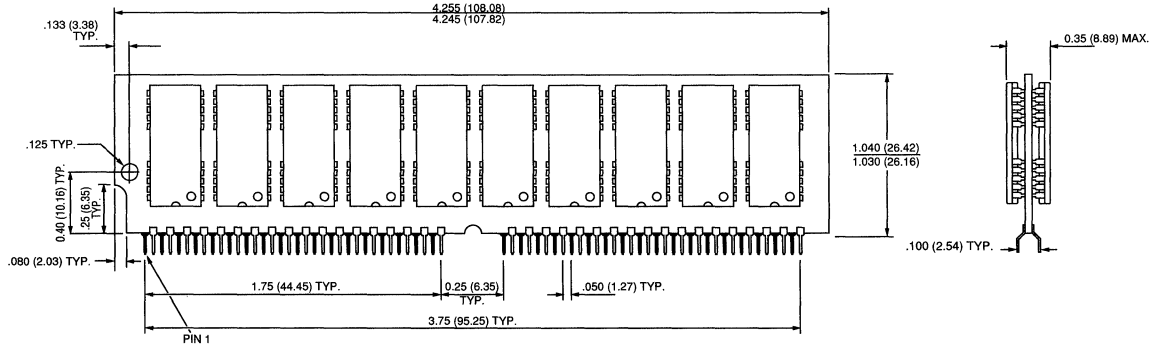
72-PIN MODULE ZIP

J-8



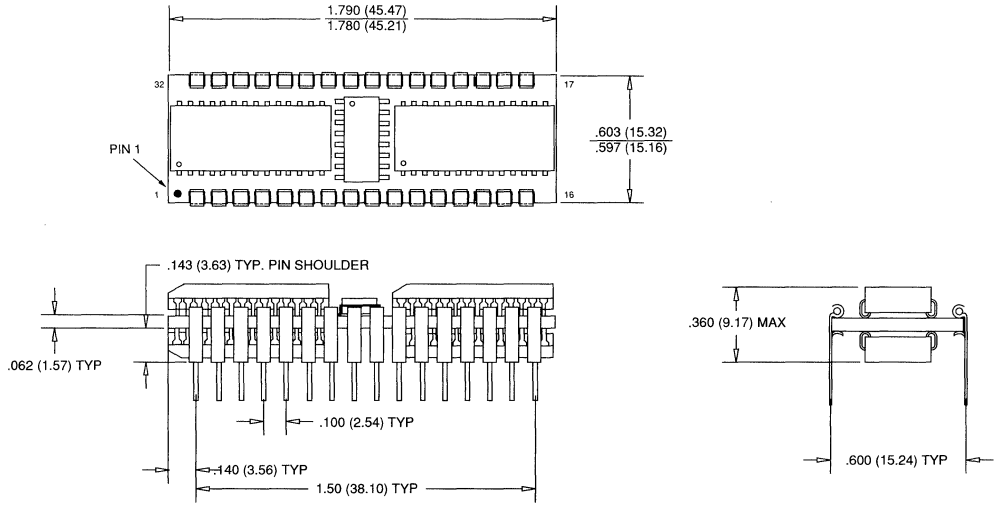
72-PIN MODULE ZIP

J-9



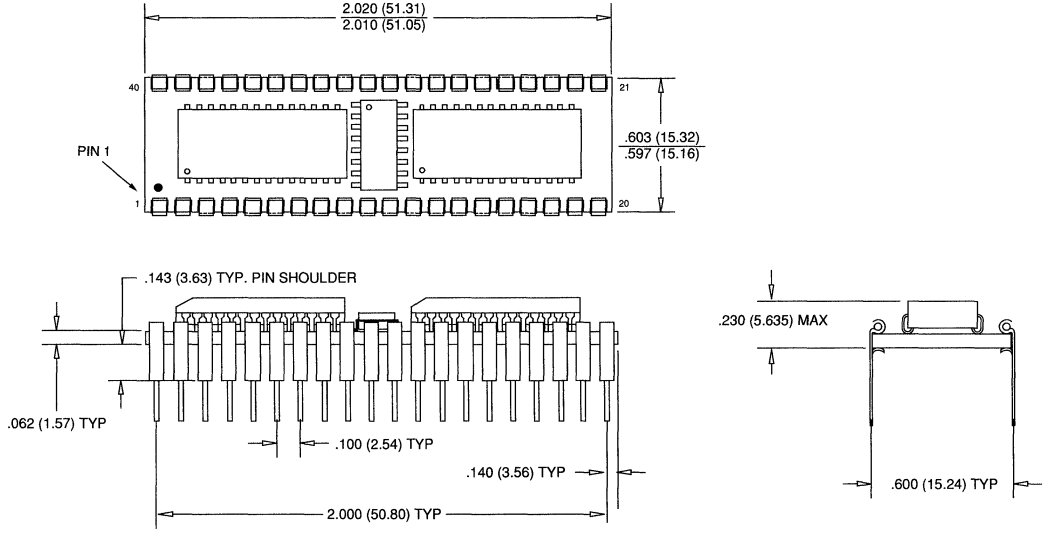
32-PIN MODULE DIP

K-1



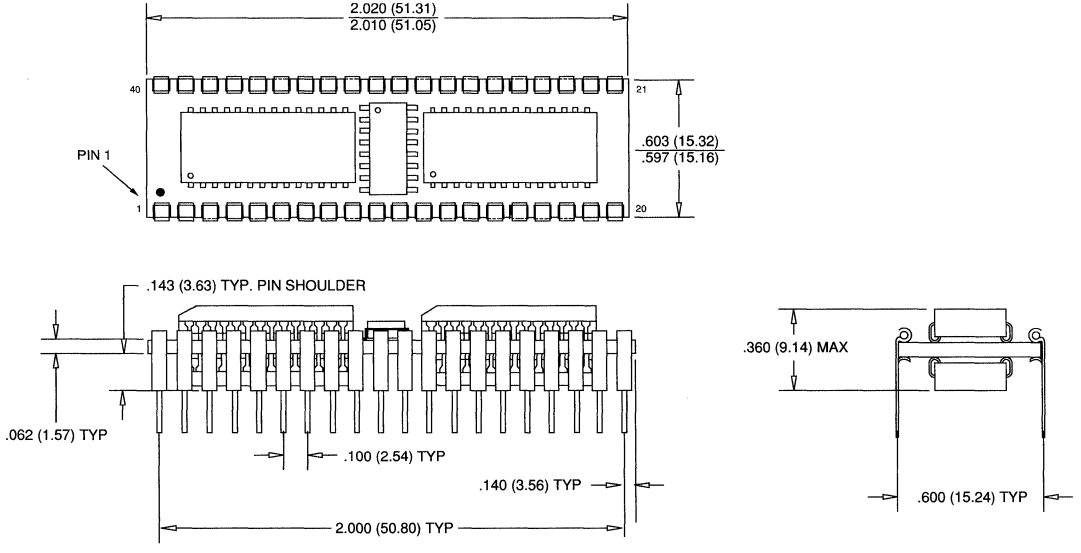
40-PIN MODULE DIP

K-2



40-PIN MODULE DIP

K-3



MICRON TECHNOLOGY, INC.

ORDER INFORMATION

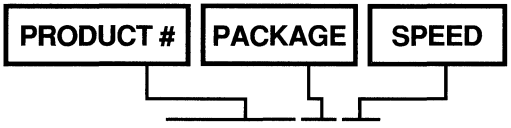
Each Micron component family is manufactured and quality-controlled in the USA at our modern Boise, Idaho, facility employing Micron's low power, high performance CMOS silicon gate process. Micron products are functionally equivalent to other manufacturers' products meeting JEDEC standards. Device functionality is consistently assured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous AMBYX™ system-level testing during many hours of accelerated burn-in prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's quality assured policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

ORDER EXAMPLES:

DRAM

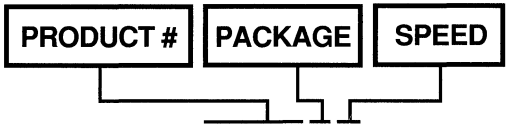
1 Meg x 1, 100ns in Plastic SOJ



MT4C1024DJ -10

DRAM MODULE

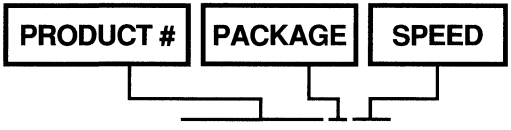
1 Meg x 8, 120ns Fast Page Mode Access, Leaded SIP



MT8D18M -8

MULTIPORT DRAM (VRAM)

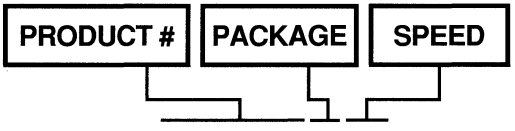
256K x 4, 100ns in ZIP



MT42C4256Z -10

CACHE DATA SRAM

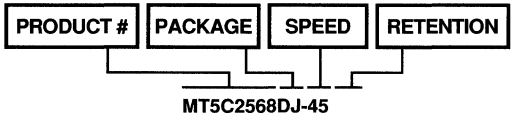
Dual 4K x 16, Single 8K x 16, 25ns in Plastic LCC



MT56C0816EJ -25

SRAM

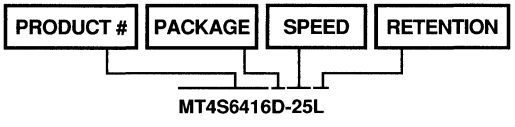
32K x 8, 45ns in Plastic SOJ



MT5C2568DJ-45

SRAM MODULE

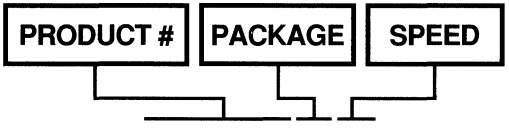
64K x 16, 25ns in DIP Module with 2V Data Retention



MT4S6416D-25L

Synchronous SRAM

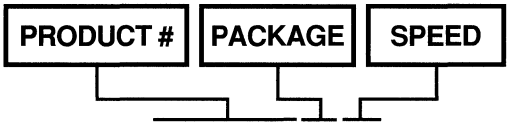
16K x 16, Clocked, Register Inputs,17ns in Plastic LCC



MT58C1616 EJ -17

FIFO

512 x 9, 15ns in 300mil DIP



MT52C9005 -15

Component Product Numbering System

Format = AA BB CC DDDD EEE-FF GG GG*

PRODUCT FAMILY

DRAM (< 1 MEG)	= BLANK
DRAM (≥1 MEG)	= 4
DPDRAM	= 42
TPDRAM	= 43
SRAM	= 5
FIFO	= 52
CACHE SRAM	= 56
SYNCHRONOUS SRAM	= 58

DEVICE NUMBER
(NUMBER CAN BE MODIFIED TO INDICATE VARIATIONS)

DRAM	= BITS, WORDS
DPDRAM	= BITS, WORDS
TPDRAM	= BITS, WORDS
CACHE SRAM	= WORDS, BITS
SRAM	= DENSITY, BITS
FIFO	= BITS, WORDS
SYNCHRONOUS SRAM	= WORDS, BITS

ACCESS TIME

-10 = 10ns or 100ns
-12 = 12ns or 120ns
-15 = 15ns or 150ns
-20 = 20ns or 200ns
-25 = 25ns or 250ns
-35 = 35ns or 350ns
-45 = 45ns
-55 = 55ns
-60 = 60ns
-70 = 70ns
-80 = 80ns
-85 = 85ns

AA	BB	CC	DDDD	EEE	FF	GG GG*

PRODUCT LINE IDENTIFIER

MT = Micron Technology Component Product

PROCESS TECHNOLOGY

NMOS	= BLANK
CMOS	= C

PACKAGE CODE

PLASTIC	
DIP	= BLANK
DIP (Wide Body)	= W
ZIP	= Z
LCC	= EJ
SOJ	= DJ
SOIC	= G
QFP	= LG
TSOP I	= VG
TSOP II	= TG
CERAMIC	
DIP	= C
DIP (Wide Body)	= CW
LCC (Narrow Body)	= ECN
LCC	= EC
LCC (Wide Body)	= ECW
SOIC	= CG
PGA	= CA
FLAT PACK	= F

PROCESSING* LEVEL/TEMP/SPECIAL

Commercial Process	
0°C to +70°C	= BLANK
-55°C to +125°C	= XT
-40°C to +125°C	= AT
-40°C to +85°C	= IT
MIL STD 883C	
-55°C to +125°C or +110°C (DRAMs)	= 883C
0°C to +70°C	= M070
2V Data Retention	= L
Tape and Reel	= TR
Bar Code	= BC

* Multiple processing codes are separated by a space.

Module Product Numbering System

Format = AA BB C DDD EE-FF GG*

PACKAGE CODE

DIP	= D
GOLD PLATE	= G
ZIP	= Z
SIP	= N
SIMM	= M

NUMBER OF PARTS

DENSITY

AA	BB	C	DDD	EE	F	GG*

PRODUCT LINE IDENTIFIER

MT = Micron Technology Component Product

RAM FAMILY

SRAM	= S
DRAM	= D

ORGANIZATION

WORDS x BITS

SPECIAL DESIGNATOR*

PARTIAL = P

* Multiple processing codes are separated by a space.

SALES INFORMATION

Overview

Product reliability pertains to product performance over time, i.e., a product's ability to perform its intended functions within specified performance limit, while operating under specified environmental conditions, for a specified length of time. This section contains a brief overview of some of the issues that affect the reliability of IC devices, and briefly describes Micron's reliability program. For a more in-depth discussion of reliability, the reader may refer to Micron's Quality/Reliability Literature.

Reliability Goals

Reliability goals of semiconductor ICs are typically discussed with reference to the traditional reliability curve of component life. The reliability curve, commonly known as the "bathtub curve," is shown in the bottom half of Figure 1, where h(t) is the hazard rate or the probability of a component failing at t_0+1 in time, given that it has survived at time t_0.

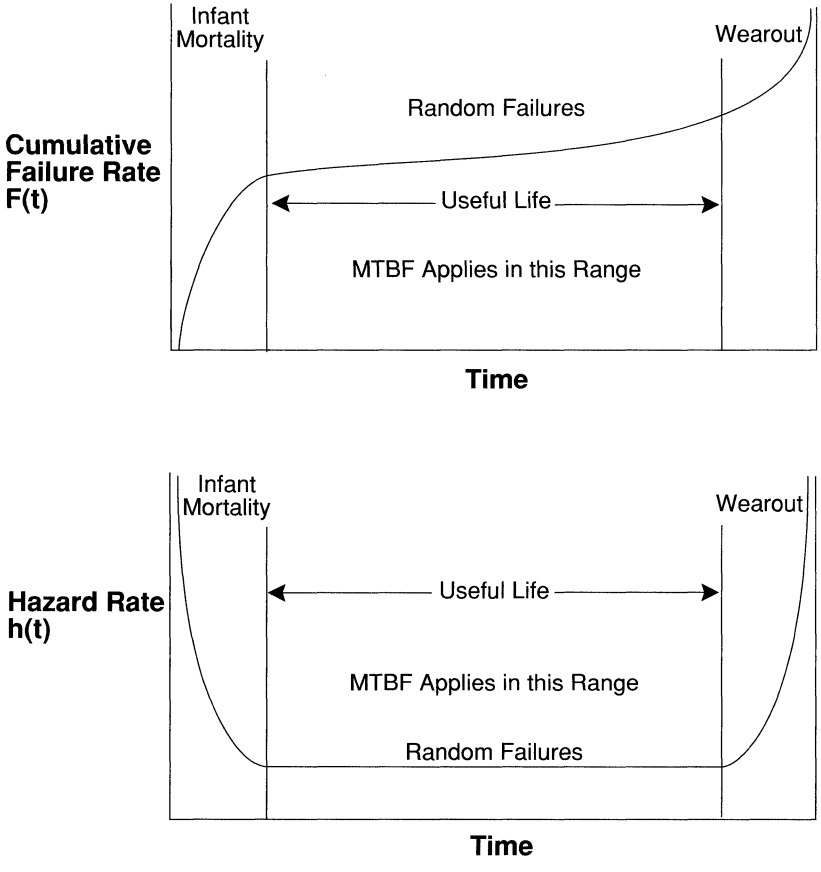


Figure 1
RELIABILITY CURVE

Figure 1 shows that the significant portion of this curve is the random failure segment. The first exponential segment (infant mortality) is attributed to gross manufacturing defects. Failures that occur in this region are screened out by Micron's in-house burn-in of all production material using the AMBYX™ intelligent burn-in/test system, which is described in the following section.

Micron's AMBYX™ Burn-in/Test System

To effectively screen out infant mortalities Micron believes it is critical to have the ability to functionally test devices without removing them from the burn-in oven, and to do so several times during the duration of the burn-in cycle. This enables the manufacturer to determine if the failure rate curves of *individual* production lots have reached the random failure region of the bathtub curve by the end of the burn-in cycle. Production lots that do not exhibit a stable failure rate towards the end of the burn-in cycle are subjected to additional burn-in. This burn-in flow also alerts the manufacturer to the slightest variation in a product's failure rate, so that any needed corrective action can be taken.

To meet this need for an intelligent burn-in system, Micron developed the AMBYX™ burn-in/test system. By "burn-in/test" we mean that devices are tested for functionality without removing the DUT (device-under-test) boards from the burn-in oven. This effectively eliminates failures resulting from handling, thereby minimizing "noise" from the test results. During the test phase, the output produced by the devices under test is compared to the pattern expected. If a discrepancy occurs, the AMBYX™ system hardware records the failure and provides the following information: bit address, device address, board address, temperature, Vcc voltage, test pattern, time set.

A functional test of the devices is conducted at burn-in conditions (125°C, 7.5V Vcc) at the beginning of the burn-in cycle, to verify that the devices under test are being properly exercised. All units that fail this test are screened from the production material. The burn-in cycle then proceeds. For our DRAM family, for example, Micron specifies that all production material is subjected to burn-in in four intervals at the following conditions: 125°C at 7.5V Vcc for the first two intervals and 6.0V Vcc for the last two intervals, with functional testing of the devices performed at 125°C between each interval. During temperature ramping to 125°C and back to 25°C, the AMBYX™ system tests for thermal intermittent opens. This flow is illustrated Figure 2.

It is also noteworthy that the stress conditions during the last two intervals of production burn-in (i.e., 125°C and 6.0V Vcc) are identical to the stress conditions for the extended high-temperature-operating-life (HTOL) test, with which we calculate the random failure rate (described on pages 5-6) of the device during its useful life. The usefulness of this scheme is that it allows for a comparison of the failure rate during the latter part of production burn-in and the HTOL test and, thus, enables Micron to determine whether production material has been effectively screened for infant mortalities.

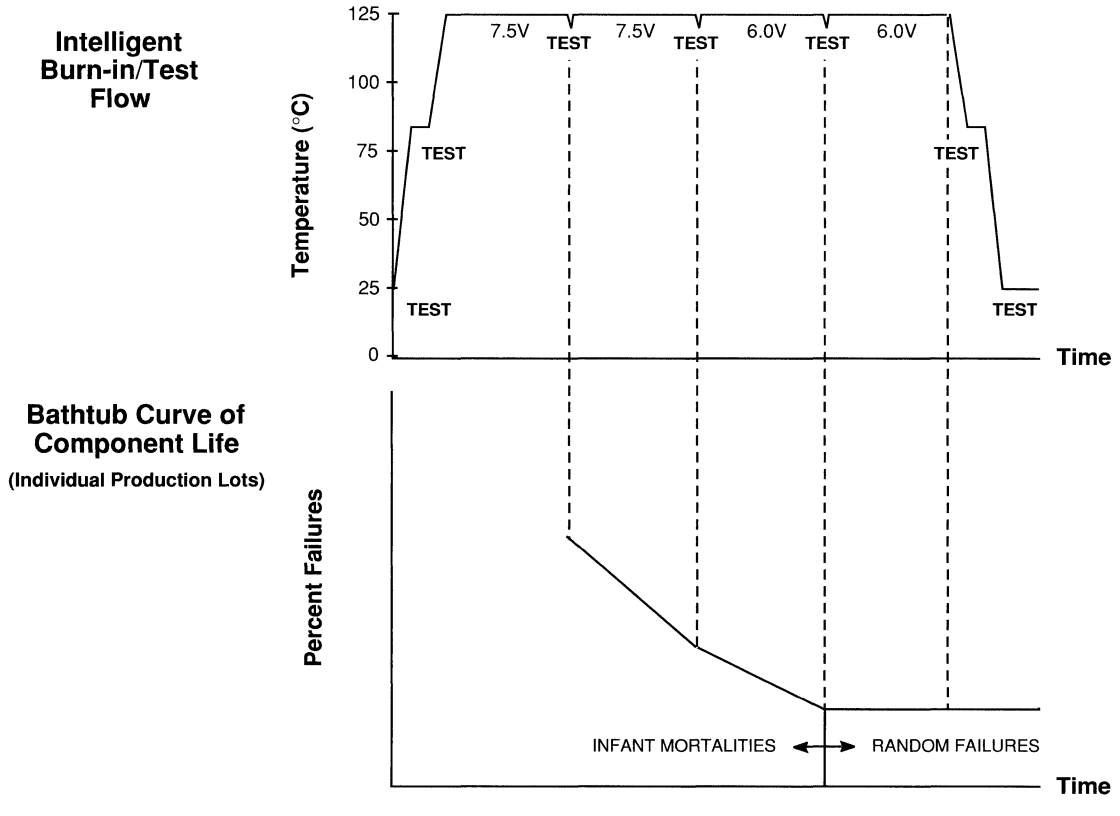


Figure 2
AMBYX™ BURN-IN/TEST FLOW AND TEST RESULTS

Environmental Process Monitor Program

Micron's environmental process monitor (EPM) program is designed to ensure the reliability of our standard products. Under this program, weekly samples of our various product and package types are subjected to a battery of environmental stress tests. During these tests, the devices are stressed for many hours under conditions designed to simulate years of normal field use. Equations, derived from intricate engineering models are applied to the data collected from these accelerated tests. From these calculations, we are able to predict failure rates under *normal use* conditions. The conditions for these tests, known as "accelerated environmental stress" tests are described in Figure 3. The EPM program described in this particular figure is for our 1 Meg DRAM.

Electrical Test

Finished Goods

Test Name and Description	Test Duration	Sample Size Per Week
HIGH TEMPERATURE OPERATING LIFE (125°C, 6.0V, ckbd / ckbd Complement Pattern)	1008 Hours 3024 Hours	100 Parts 100 Parts
TEMPERATURE AND HUMIDITY (85°C, 85% R.H., 5.5V, Alternating Bias)	1008 Hours 3024 Hours	100 Parts 100 Parts
AUTOCLAVE (121°C, 100% R.H., 15 PSI, No Bias)	288 Hours	50 Parts
LOW TEMPERATURE LIFE (-25°C, 7.0V, Dynamic Bias)	1008 Hours	10 Parts
TEMPERATURE CYCLE (-65°C TO +150°C, Air to Air)	1000 Cycles	100 Parts
THERMAL SHOCK (-55°C TO +125°C, Liquid to Liquid)	700 Cycles	25 Parts
HIGH TEMPERATURE STORAGE (150°C, No Bias)	1008 Hours	25 Parts
ELECTROSTATIC DISCHARGE (+ and -)	MIL STD 3015.7	24 Parts
NOTE: Samples Pulled from Five Different Lots at Finished Goods.		

Figure 3
ENVIRONMENTAL PROCESS MONITOR – 1 MEG DRAM

Failure Rate Calculation

The failure rate during the useful life of the device is expressed as percent failures per thousand device hours or as FITs (failures in time, per billion device hours), and is calculated as follows:

$$\text{Failure Rate} = Pn \div \left[\begin{array}{c} \text{Device hours at} \\ \text{accelerated environment} \end{array} \times \begin{array}{c} \text{A.F. relative to maximum} \\ \text{operating environment} \end{array} \right]$$

where: Pn = Poisson Statistic (at a given confidence level). For the data above, Pn at 60% confidence level equals .916.
Device hours = sample size multiplied by test time (in hours). In our example, to follow, device hours equal 1.929×10^6.
A.F. = acceleration factor between the stress environment and ***maximum*** use conditions. For the 1 Meg DRAM, the acceleration factor between 125°C, 6.0V (HTOL stress conditions) and 70°C, 5.5V (maximum operating conditions) equals 16.5. (Calculation of this acceleration factor is described in the following section).

Thus, the failure rate of the Micron 1 Meg DRAM family is computed as follows:

$$\text{Failure Rate} = .916 \div (1.929 \times 10^6)\,(16.5) = 2.878 \times 10^{-8}$$

where: Total device hours at test conditions = 1.929×10^6.
Equivalent device hours at maximum use conditions (70°C, 5.5V Vcc) using an acceleration factor of 16.5 = 32×10^6.

To translate the above failure rate into percent failures per thousand device hours, we multiply the failure rate obtained from the equation above by 10^5:

$$\text{Failure Rate} = (2.878 \times 10^{-8}) \times 10^5 = 0.0029\% \text{ per 1K device hours}$$

To state the failure rate in FITs, we multiply the failure rate obtained from the equation above by 10^9:

$$\text{Failure Rate} = (2.878 \times 10^{-8}) \times 10^9 = 29 \text{ FITs}$$

NOTE: ***Typical*** use conditions for the 1 Meg DRAM are 50°C and 5.0V Vcc. When we calculate the acceleration factor between the stress environment (70°C, 5.5V Vcc) and these typical conditions, we find that A.F. equals 125.4. Using the acceleration factor 125.4, the FIT rate for the 1 Meg DRAM is calculated as follows:

$$\begin{aligned} \text{Failure Rate} &= 916 \div (1.929 \times 10^6)\,(125.4) = 3.787 \times 10^{-9} \\ &= (3.787 \times 10^{-9}) \times 10^9 = 3.787 \\ &= 4 \text{ FITs (rounded)} \end{aligned}$$

Acceleration Factor Calculation:

Again, using the 1 Meg DRAM for our example, the acceleration factor between high temperature operating life stress conditions (125°C, 6.0V) and maximum operating conditions (70°C, 5.5V) is computed using the following models:

1. Acceleration factor due to temperature stress:

The acceleration factor due to temperature stress is computed using the Arrhenius equation, which is stated as follows:

$$A.F._{t1/t2} = \exp\left[\frac{E_a}{kT_1} - \frac{E_a}{kT_2}\right]$$

where: k = Boltzmann's constant , which is equal to 8.617×10^{-5}
T_1 and T_2 = operating and stress temperatures, respectively, in kelvins
E = activation energy in eV (For oxide defects, which is the most common failure mechanism for the 1 Meg DRAM, used in our example, the activation energy is determined to be 0.3eV).

Using these values, the temperature acceleration factor between 125°C and 70°C is computed to be 4.07.

2. Acceleration factor due to voltage stress:

The acceleration factor due to voltage stress is computed using the following model:

$$A.F._{v1/v2} = \exp[\beta (v_1 - v_2)]$$

where: v_1 and v_2 = stress voltage and operating voltage, respectively, in volts
β = constant, the value of which was derived experimentally by running several sessions of Micron's intelligent burn-in test sequence at different voltages on large numbers of the device. (For the 1 Meg DRAM, used in our example, ß equals 2.8).

Thus, the voltage acceleration factor for the 1 Meg DRAM between 6.0V (stress condition) and 5.5V (maximum operating condition) is computed to be 4.06.

Finally, the overall acceleration factor due to temperature and voltage stress is calculated as the product of the two respective acceleration factors or:

$$A.F._{overall} = A.F._{temperature} \times A.F._{voltage}$$

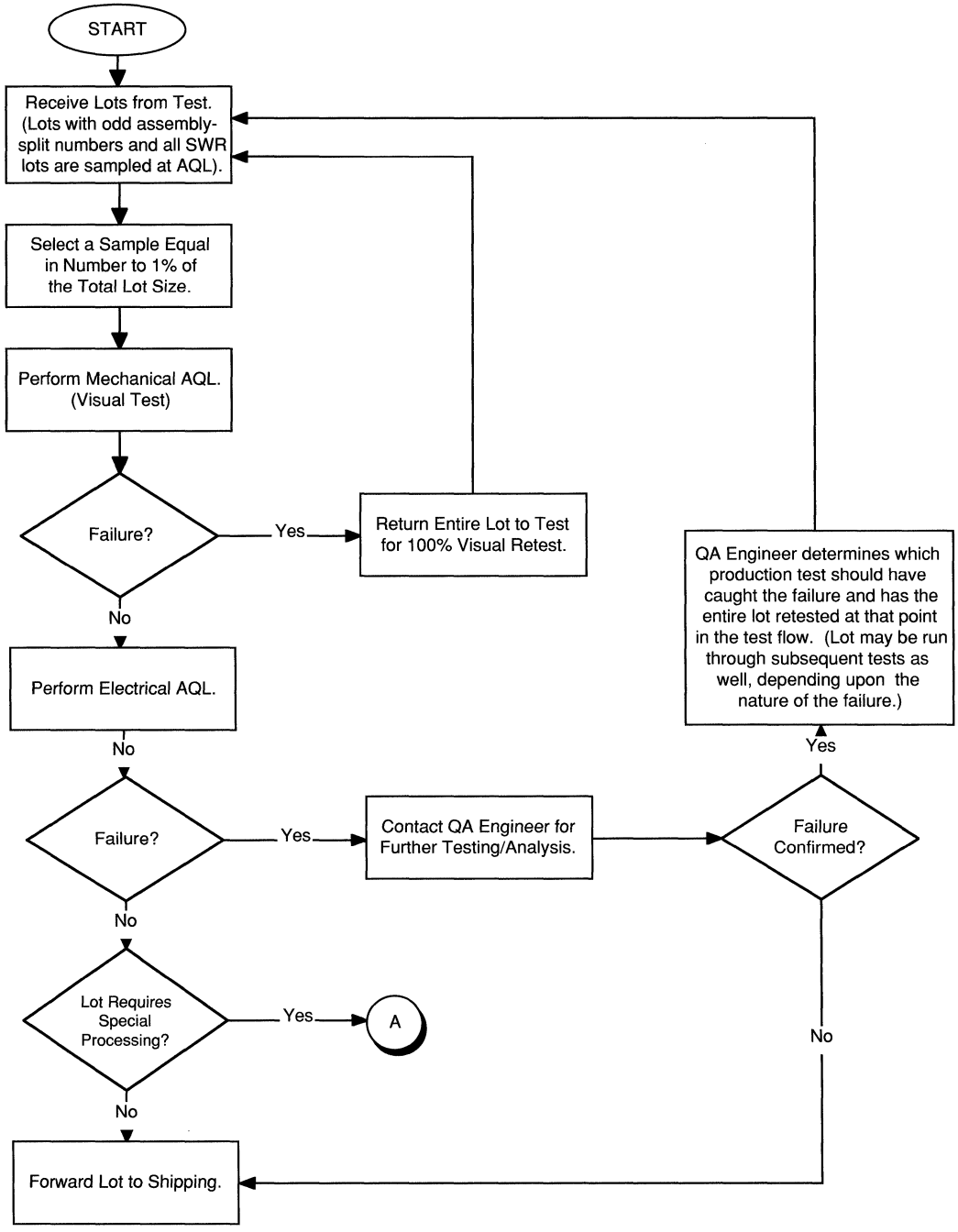
Outgoing Product Quality

Before being sent to our finished goods area, where products are prepared for shipping, a special unit within the quality assurance department takes a 1% sample from each production lot. These samples are subjected to visual and electrical testing in order to measure the AQL (acceptable quality level) of all outgoing product. A flowchart illustrating Micron's AQL test procedure is provided in Figure 4.

Visual or mechanical testing consists of an unaided visual inspection of the sample devices for any physical irregularities which could negatively affect their performance . If a sample device is found to have, for example, a bent lead, a package irregularity or excess solder, the entire lot is returned to our test area for a 100% visual inspection.

Electrical testing of the sample devices is performed using ATE (automatic test equipment) systems. Testing is conducted at room temperature (~25°C) and at 70°C. Should an electrical failure occur, the failing device is turned over to a quality assurance engineer for further testing and analysis. If after completing this analysis the electrical failure is confirmed, the QA engineer determines which production monitor/test should have caught the failure and the entire lot is retested at that point in the test flow. Correlating the failure to the test where it should originally have been detected, and discerning why it was not tested, are important steps in preserving the integrity of our test process.

The percent devices found to be defective in the total number of devices sampled weekly is recorded using a control chart. This control chart, containing AQL data for the previous 52 weeks, is presented in weekly management meetings, where plans for corrective action are made, as needed.


START
Receive Lots from Test. (Lots with odd assembly-split numbers and all SWR lots are sampled at AQL).
Select a Sample Equal in Number to 1% of the Total Lot Size.
Perform Mechanical AQL. (Visual Test)
Failure?
Yes
Return Entire Lot to Test for 100% Visual Retest.
No
Perform Electrical AQL.
No
Failure?
Yes
Contact QA Engineer for Further Testing/Analysis.
Failure Confirmed?
Yes
QA Engineer determines which production test should have caught the failure and has the entire lot retested at that point in the test flow. (Lot may be run through subsequent tests as well, depending upon the nature of the failure.)
No
Lot Requires Special Processing?
Yes
A
No
Forward Lot to Shipping.
No

Example of Special Processing:
Lot Mounted on Tape & Reel

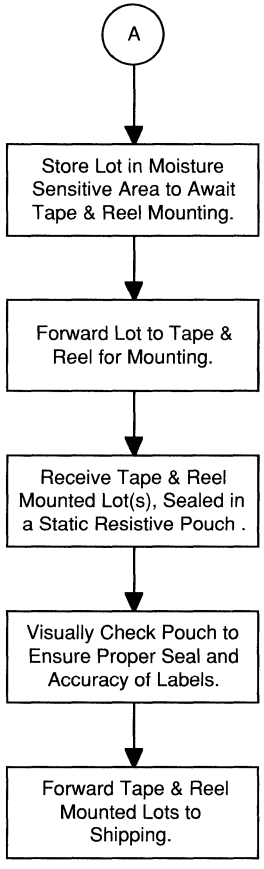


Figure 4
AQL TEST FLOW FOR ALL OUTGOING PRODUCT

Automated Data Capture & Analysis

Micron has developed a sophisticated data capture and analysis system with a computer network tailored to the needs of quality IC manufacturing. Figure 5 shows the various functional areas that provide the input to our VAX data bases.

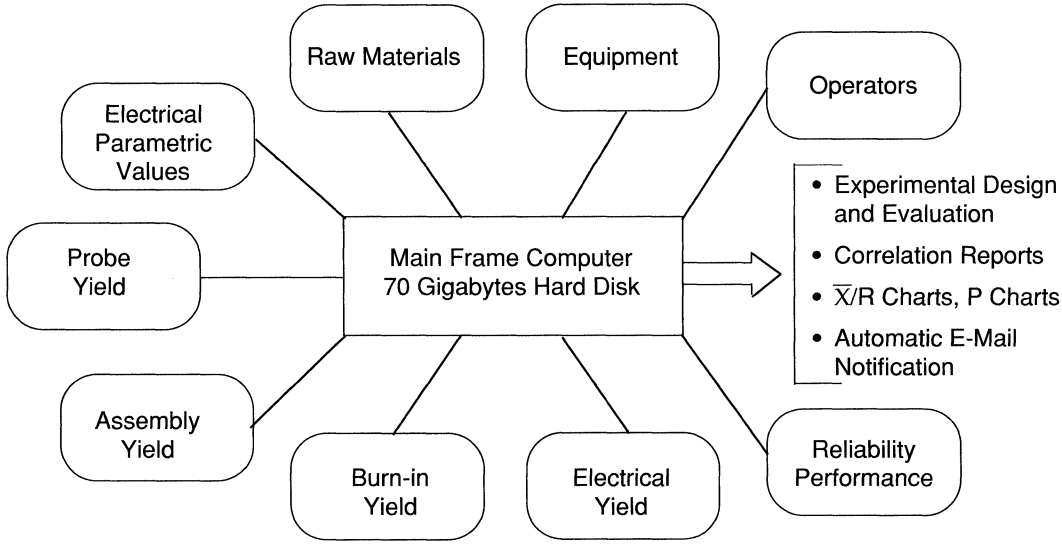


Figure 5
STATISTICAL CORRELATION

Data Capture

Automated, real-time data capture makes real-time charting ($\bar{X}$ and R charts, etc.) of all critical operations and processes possible, and ensures that appropriate manufacturing personnel are alerted on a timely basis, should unexpected variation occur. As production lots move through each manufacturing step, detailed information (including step number, lot number, machine number, date/time, and operator number) are entered into the production data base. In addition; automated, highly-programmable measurement systems are utilized to capture a host of parameters associated with equipment, on-line process material, and environmental variables.

Analytical Tools

By using highly flexible, on-line data extraction programs, system users have the ability to tap this vast data base and to design their own correlation and trend analyses. The ability to correlate process variables to product performance allows us to make on-line projections of the quality of our finished product for a given lot or process run. In addition, we can estimate the impact of process improvements on quality well in advance and can make the impact of process deviations more visible to our engineers. This approach allows us to model yield and quality parameters based on on-line parameters. We then use this model to predict the final product results. Following is a description of the various means by which we analyze data:

- GROUP SUMMARIES: Summaries, which provide the means and standard deviations of user-defined parametrics, enable system users to compare the parametric values of production lots as well as special engineering lots.

- TREND ANALYSIS: Trend charts are routinely generated for critical parameters. System users can trend the means and ranges of any probe or parametric data captured throughout the manufacturing process.

- CORRELATION ANALYSIS: Correlation analysis can be performed on any combination of factors; such as equipment, masks, or electrical parameters. One report, regularly produced and disseminated to key personnel, takes two groups of lots (one with a high failure rate, the other with a low failure rate) and identifies all the pieces of equipment that are **common** to one or the other group. The report, thus, quickly alerts us should there be a correlation between a lot with a high failure rate and a particular piece(s) of equipment in the wafer fabrication or assembly areas.

  Another regularly produced report analyzes a user-selected set of database parametrics against an index, such as manufacturing yield. Lots are divided into three sub-groups(upper yielding, middle yielding and lower yielding). The report then correlates the yields with all electrical parametric values taken on individual lots at wafer sort. Thus, the report helps us determine which processing step may have caused the yields to vary among the three subgroups.

- STATISTICAL PROCESS CONTROL CHARTS: SPC control charts are used throughout the company to monitor and evaluate critical process parameters, such as, critical dimensions (CDs), oxide thickness, chemical vapor depositions (CVDs), particle counts, temperature and humidity, and many other critical process and product quality parameters.

- OVERLAYS or WAFER MAPS: Maps, which are produced for all wafers during probe, show various parameters as a function of position on the wafer and are very useful for problem isolation. Maps may be analyzed individually or in groups. For example, wafers from an entire lot may be analyzed in relation to one particular parameter.

- RS/1 DISCOVER/EXPLORE: This analysis software is used for experimental design, and evaluation of results. The statistical approach supported by this software (i.e., the use of *t* tests, ANOVA tables, multiregression analysis, etc.) has proven invaluable in reducing time expended for product development and for trouble shooting. It is also used to determine the relationships between process output and probe and parametric data. Using multiregression analysis, for example, we are able to determine the relationship between L effective and CD dimensions to the speed of a device.

The use of automation in data capture, analysis, and feedback greatly enhances the flexibility and speed with which we are able to view all aspects of the manufacturing process. This effective data analysis and feedback system helps to reduce parametric deviations, improve margin to specifications, increase manufacturing yields, and provide for more accurate fabrication output planning.

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FAX - 214-644-5064

Military Distributors

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

Zeus Components, Inc.
1800 North Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

MAINE

Representative

Advanced Tech Sales Incorporated
348 Park Street, Ste 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 617-935-9777
FAX - 617-667-4129

Pioneer Standard
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Military Distributor

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone - 617-246-8200
FAX - 617-246-8293

MARYLAND

Representative

Electronic Engineering & Sales Inc.
235 Prince George Street
Annapolis, MD 21401
Phone - 301-269-6573
FAX - 301-269-6476

Distributors

Anthem Electronics
9020A Mendenhall Court
Columbia, MD 21045
Phone - 301-995-6640
FAX - 301-381-4379

Hall-Mark Electronics Corporation
10240 Old Columbia Road
Columbia, MD 21046
Phone - 301-988-9800
FAX - 301-381-2036

Pioneer Technologies
15810 Gaither Drive
Gaithersburg, MD 20877
Phone - 301-921-0660
FAX - 301-921-3852

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

MASSACHUSETTS

Representative

Advanced Tech Sales
348 Park Street, Ste 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics, Inc.
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Gerber Electornics
128 Carnegie Row
Norwood, MA 02062
Phone - 617-769-6000
FAX - 617-762-8931

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 617-935-9777
FAX - 617-667-4129

Pioneer Standard
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Wyle Laboratories
15 3rd Avenue
Burlington, MA 01803
Phone - 617-272-7300
FAX - 617-272-6809

Military Distributor

JAN Devices, Inc.
44 Cochrane St.
Melrose, MA 02176
Phone - 617-662-3901

Zeus Components, Inc.
11 Lakeside Office Park
Wakefield, MA 01880
Phone 617-246-8200
FAX - 617-246-8293

MICHIGAN

Representatives

Rathsburg Associates Incorporated
34605 Twelve Mile Rd.
Farmington Hills, MI 48331-3263
Phone - 313-489-1500
FAX - 313-489-1480

Rathsburg Associates Incorporated
2680 Horizon, S.E.
Grand Rapids, MI 49506
Phone - 616-949-7400
FAX - 616-949-1909

Distributors

Hall-Mark Electronics Corporation
38027 Schoolcraft Road
Livonia, MI 48150
Phone - 313-462-1205
FAX - 313-462-1830

Pioneer Standard
4505 Broadmoor Avenue, S.E.
Grand Rapids, MI 49512
Phone - 616-698-1800
FAX - 616-698-1831

Pioneer Standard
13485 Stamford
Livonia, MI 48150
Phone - 313-525-1800
FAX - 313-427 3720

Military Distributors

Zeus Components, Inc.
100 Midland Ave.
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Ste 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

MINNESOTA

Representative

HMR Incorporated
9065 Lyndale Avenue
Minneapolis, MN 55420-3520
Phone - 612-888-2122
FAX - 612-884-4768

Distributors

Anthem Electronics Inc.
7646 Golden Triangle Dr.
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
10300 Valley View Rd, Ste 101
Eden Prairie, MN 55344
Phone - 612-941-2600
FAX - 612-941-5778

Pioneer Standard
7625 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-3355
FAX - 612-944-3794

Military Distributors

Zeus Components, Inc.
100 Midland Ave.
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Ste 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

MISSISSIPPI

Representative

Southeast Technical Group
Route 10, Box 368
Meridian, MS 39301
Phone - 601-485-7055
FAX - 601-485-7063

Distributor

Hall-Mark Electronics Corporation
4900 Bradford Drive
Huntsville, AL 35805
Phone - 205-837-8700
FAX - 205-830-2565

Pioneer Technologies
4835 University Square, Ste #5
Huntsville, AL 35816
Phone - 205-837-9300
FAX - 205-837-9358

Military Distributor

Zeus Components, Inc.
1800 North Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

MISSOURI

Representatives

Advanced Technical Sales
1810 Craig Road, Suite #213
St. Louis, MO 63146
Phone - 314-878-2921
FAX - 314-878-1994

Distributors

Hall-Mark Electronics Corporation
3783 Rider Trail So.
Earth City, MO 63045
Phone - 314-291-5350
FAX - 314-291-0362

Pioneer Standard
2029 Woodland Pkwy #101
St Louis, MO 63146
Phone - 314-432-4350
FAX - 314-432-4854

Military Distributor

Zeus Components, Inc.
1800 North Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

MONTANA

Distributor

Almac Electronics
E 10905 Montgomery
Spokane, WA 99206
Phone - 509-924-9500
1-800-325-6545
FAX - 509-928-6096

Military Distributor

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

NEBRASKA

Representative

Advanced Technical Sales
601 North Mur-Len, Suite 8
Olathe, KS 66062
Phone - 913-782-8702
FAX - 913-782-8641

Distributors

Hall-Mark Electronics Corporation
10809 Lakeview Dr.
Lenexa, KS 66215
Phone - 913-888-4747
FAX - 913-888-0523

Wyle Laboratories
451 E 124th Street
Thornton, CO 80241
Phone - 303-457-9953
FAX - 303-457-4831

Military Distributor

Zeus Components, Inc.
1800 North Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

NEVADA

Representative

Bay Area Electronics Sales, Inc
2001 Gateway Place, Suite 315
San Jose, CA 95110
Phone - 408-452-8133
FAX - 408-452-8139

Distributors

Anthem Electronics Incorporated
580 Menlo Drive, Suite 8
Rocklin, CA 95677
Phone - 916-624-9744
FAX - 916-624-9750

Hall-Mark Electronics Corporation
580 Menlo Dr., Suite 2
Rocklin, CA 95677
Phone - 916-624-9781
FAX - 916-961-0922

Wyle Laboratories
2951 Sunrise Blvd., Suite 175
Rancho Cordova, CA 95742
Phone - 916-638-5282
FAX - 916-638-1491

Military Distributor

JAN Devices, Inc.
44 Cochrane St.
Melrose, MA 02176
Phone - 617-662-3901

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

NEW HAMPSHIRE

Representative

Advanced Tech Sales Incorporated
348 Park Street, Ste 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 617-935-9777
FAX - 617-667-4129

Pioneer Standard
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Military Distributor

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone - 617-246-8200
FAX - 617-246-8293

NEW JERSEY

Representative

Applied Technical Marketing
234 Main St., Suite 2
Huntington, NY 11743
Phone - 516-271-0200
FAX - 516-271-4450

Representative (Southern)

Omega Electronics
2655 Interplex Dr., Suite 104
Trevose, PA 19047
Phone - 215-244-4000
FAX - 215-244-4104

Distributors

Anthem Electronics
26 Chapin Road, Unit K
Pine Brook, NJ 07058
Phone - 201-227-7960
FAX - 201-227-9246

Hall-Mark Electronics Corporation
107 Fairfield Road
Fairfield, NJ 07006
Phone - 201-575-4415
FAX - 201-882-9389

Hall-Mark Electronics Corporation
11000 Midlantic Drive, Suite 5
Mt. Laurel, NJ 08054
Phone - 609-235-1900
FAX - 609-235-3381

Hall-Mark Electronics Corporation
200 Lanidex Plaza, 2nd Fl.
Parsippany, NJ 07054
Phone - 201-515-3000
FAX - 201-515-4475

Military Distributor

Zeus Components, Inc.
100 Midland Ave.
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

NEW MEXICO

Representative

Quatra Associates Incorporated
600 Autumnwood Place, S.E.
Albuquerque, NM 87123
Phone - 505-296-6781
FAX - 602-820-7054

Distributors

Anthem Electronics Inc.
1555 W. 10th Pl., Suite #101
Tempe, AZ 85281
Phone - 602-966-6600
FAX - 602-966-4826

Hall-Mark Electronics Corporation
4637 South 36th Place
Phoenix, AZ 85040
Phone - 602-437-1200
FAX - 602-437-2348

Wyle Laboratories
4141 E. Raymond St., Ste #1
Phoenix, AZ 85040
Phone - 602-437-2088
FAX - 602-437-2124

Military Distributor

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

NEW YORK

Representatives

Applied Technical Marketing
234 Main St., Suite 2
Huntington Village, NY 11743
Phone - 516-271-0200
FAX - 516-271-4450

Electra Sales Corporation
3000 Winston Rd. South
Rochester, NY 14623
Phone - 716-427-7860
FAX - 716-427-0614

Electra Sales Corporation
1 Alder Drive
East Syracuse, NY 13057
Phone - 315-463-1248
FAX - 315-463-1717

Distributors

Anthem Electronics-Military
47 Mall Drive
Commack, NY 11725-5703
Phone - 516-864-6600
FAX - 516-493-2244

Hall-Mark Electronics Corporation
6605 Pittsford - Palmyra Road, Suite E8
Fairport, NY 14450
Phone - 716-425-3300
FAX - 716-425-7195

Hall-Mark Electronics Corporation
3075 Veterans Memorial Hwy
Ronkonkoma, NY 11779
Phone - 516-737-0600
FAX - 516-737-0838

MAST Distributors, Inc.
710-2 Union Parkway
Ronkonkoma, NY 11799
Phone - 516-471-4422
FAX - 516-471-2040

Pioneer Standard
68 Corporate Drive
Binghamton, NY 13904
Phone - 607-722-9300
FAX - 607-722-9562

Pioneer Standard
840 Fairport Park
Fairport, NY 14450
Phone - 716-381-7070
FAX - 716-381-5955

Pioneer Standard
14A Madison Road
Fairfield, NY 07006
Phone - 201-575-3510
FAX - 201-575-3454

Pioneer Standard
60 Crossways Park West
Woodbury, NY 11797
Phone - 516-921-8700
FAX - 516-921-2143

Military Distributor

Zeus Components, Inc.
100 Midland Ave.
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2110 Smithtown Ave.
Ronkonkoma, L.I., NY 11779
Phone - 516-737-4500
FAX - 516-737-4520

Zeus Components, Inc.
2912 Springboro West, Ste 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

NORTH CAROLINA

Representatives

Southeast Technical Group
700 N. Arendell Ave
Zebulon, NC 27597
Phone - 919-269-5589
FAX - 919-269-5670

Distributors

Hall-Mark Electronics Corporation
5234 Green's Dairy Road
Raleigh, NC 27604
Phone - 919-872-0712
FAX - 919-878-8729

Pioneer Technologies
9401L Southern Pines Blvd
Charlotte, NC 28210
Phone - 704-526-8188
FAX - 704-522-8564

Pioneer Electronics
2810 Meridian Parkway , #148
Durham, NC 27713
Phone - 919-544-5400
FAX - 919-544-5885

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

NORTH DAKOTA

Representative

HMR Incorporated
9065 Lyndale Avenue
Minneapolis, MN 55420-3520
Phone - 612-888-2122
FAX - 612-884-4768

Distributors

Anthem Electronics Incorporated
7646 Golden Triangle Dr.
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
10300 Valley View Rd, Ste 101
Eden Prairie, MN 55344
Phone - 612-941-2600
FAX - 612-941-5778

Pioneer Standard
7625 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-3355
FAX - 612-944-3794

Military Distributors

Zeus Components, Inc.
100 Midland Ave.
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Ste 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

OHIO

Representatives

Scott Electronics, Inc.
Corporate Headquarters
360 Alpha Park
Cleveland OH 44143-2240
Phone - 216-473-5050
FAX - 216-473-5055

Scott Electronics, Inc.
3131 South Dixie Drive
Dayton, OH 45439-2223
Phone - 513-294-0539
FAX - 513-294-4769

Scott Electronics, Inc.
916 Eastwind Drive
Westerville, OH 43081-3379
Phone - 614-882-6100
FAX - 614-882-0900

Scott Electronics, Inc.
10901 Reed Hartman, Ste. 301
Cincinnati, OH 45242-2821
Phone - 513-791-2513
FAX - 513-791-8059

Distributors

Hall-Mark Electronics Corporation
5821 Harper Road
Solon, OH 44139
Phone - 216-349-4632
FAX - 216-248-4803

Hall-Mark Electronics Corporation
400 E. Wilson Bridge Rd, Ste S
Worthington, OH 43085
Phone - 614-888-3313
FAX - 614-888-0767

Pioneer Standard
4800 E 131st Street
Cleveland, OH 44105
Phone - 216-587-3600
FAX - 216-587-3906

Pioneer Standard
4433 Interpoint Blvd.
Dayton, OH 45424
Phone - 513-236-9900
FAX - 513-236-8133

Pioneer Standard
5440 Naiman Parkway
Solon, OH 44139
Phone - 216-349-1300
FAX - 216-349-0754

Military Distributors

Zeus Components, Inc.
100 Midland Ave.
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Ste 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

OKLAHOMA

Representative

Nova Marketing Incorporated
4924 S. Memorial, Suite 1339
Tulsa, OK 74145
Phone - 918-660-5105
FAX - 918-665-3815

Distributor

Hall-Mark Electronics Corporation
5411 S. 125th East Ave., #305
Tulsa, OK 74146
Phone - 918-254-6110
FAX - 918-254-6207

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Ste 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

OREGON

Representative

Northwest Marketing Associates
6975 SW Sandburg Rd, Ste 330
Portland, OR 97223
Phone - 503-620-0441
FAX - 503-684-2541

Distributors

Almac Electronics
1885 N.W. 169th Place
Beaverton, OR 97006
Phone - 503-629-8090
FAX - 503-645-0611

Anthem Electronics Incorporated
9090 S.W. Gemini Drive
Beaverton, OR 97005
Phone - 503-643-1114
FAX - 503-626-7928

Wyle Laboratories
9640 SW Sunshine Ct, Ste. 200
Beaverton, OR 97005
Phone - 503-643-7900
FAX - 503-646-5466

Military Distributor

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Ste E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

PENNSYLVANIA

Representatives

Omega Electronic Sales Incorporated
2655 Interplex Dr., #104
Trevose, PA 19047
Phone - 215-244-4000
FAX - 215-244-4104

Scott Electronics, Inc. (W. PA)
360 Alpha Park
Cleveland, OH 44143-2240
Phone - 216-473-5050
FAX - 216-473-5055

Distributors

Anthem Electronics, Inc.
355 Business Ctr. Dr.
Horsham, PA 19044
Phone - 215-443-5150
FAX - 215-675-9875

Hall-Mark Electronics Corporation
11000 Midlantic Drive, Suite 5
Mt. Laurel, NJ 08054
Phone - 609-235-1900
FAX - 609-235-3381

Hall-Mark Electronics Corporation (W. PA)
5821 Harper Road
Solon, OH 44139
Phone - 216-349-4632
FAX - 216-248-4803

Pioneer Technologies
500 Enterprise Road
Horsham, PA 19044
Phone - 215-674-4000
FAX - 215-674-3107

Pioneer Technologies (W. PA)
259 Kappa Drive
Pittsburgh, PA 15238
Phone - 412-782-2300
FAX - 412-963-8255

Military Distributors

Zeus Components, Inc.
100 Midland Ave.
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Ste 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

RHODE ISLAND

Representative

Advanced Tech Sales Incorporated
348 Park Street, Ste 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics
61 Mattatuck Heights
Waterbury, CT 06705
Phone - 203-575-1575
FAX - 203-596-3232

Hall-Mark Electronics Corporation
615 W. Johnson Ave., Bldg. 3
Cheshire, CT 06410
Phone - 203-271-2844
FAX - 203-272-1704

Pioneer Standard
112 Main Street
Norwalk, CT 06851
Phone - 203-853-1515
FAX - 203-838-9901

Military Distributor

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone - 617-246-8200
FAX - 617-246-8293

SOUTH CAROLINA

Representative

Southeast Technical Group
700 N. Arendell Ave.
Zebulon, NC 27597
Phone - 919-269-5589
FAX - 919-269-5670

Distributor

Pioneer Technologies
9401 L. Southern Pine Blvd
Charotte, NC 28210
Phone - 704-526-8188
FAX - 704-522-8564

Military Distributor

Zeus Components, Inc.
1750 West Broadway, Ste 114
Oviedo, FL 32765
Phone - 407-365-3000
FAX - 407-365-2356

SOUTH DAKOTA

Representative

HMR Incorporated
9065 Lyndale Avenue
Minneapolis, MN 55420-3520
Phone - 612-888-2122
FAX - 612-884-4768

Distributors

Anthem Electronics Incorporated
7646 Golden Triangle Dr.
Eden Prairie, MN 55344
Phone - 612-944-5454
FAX - 612-944-3045

Hall-Mark Electronics Corporation
10300 Valley View Rd, Ste 101
Eden Prairie, MN 55344
Phone - 612-941-2600
FAX - 612-941-5778

Pioneer Standard
7625 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-3355
FAX - 612-944-3794

Military Distributors

Zeus Components, Inc.
100 Midland Ave.
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Ste 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

TENNESSEE

Representative

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700 N. Arendell Ave.
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Phone - 919-269-5589
FAX - 919-269-5670

Distributors

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4900 Bradford Drive
Huntsville, AL 35805
Phone - 205-837-8700
FAX - 205-830-2565

Pioneer Technologies
4825 University Square, #5
Huntsville, AL 35816
Phone - 205-837-9300
FAX - 205-837-9358

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

TEXAS

Representatives

Nova Marketing Incorporated
8350 Meadow Road, Suite 174
Dallas, TX 75231
Phone - 214-750-6082
FAX - 214-750-6068

Nova Marketing Incorporated
9207 Country Creek #206
Houston, TX 77036
Phone - 713-988-6082
FAX - 713-774-1014

Nova Marketing Incorporated
Stillhouse Canyon Office Park
4807 Spicewood Springs Road
Building 3, Suite 3140
Austin, TX 78759
Phone - 512-343-2321
FAX - 512-343-2487

Distributors

Anthem Electronics, Inc.
651 N. Plano Road, Suite 429
Richardson, TX 75081
Phone - 214-238-7100
FAX - 214-238-0237

Hall-Mark Electronics Corporation
12211 Technology Boulevard
Austin, TX 78727
Phone - 512-258-8848
FAX - 512-258-3777

Hall-Mark Electronics Corporation
11333 Pagemill Road
Dallas, TX 75243
Phone - 214-343-5000
FAX - 214-343-5851

Hall-Mark Electronics Corporation
11420 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
FAX - 214-343-5988

Hall-Mark Electronics Corporation
8000 Westglen
Houston, TX 77063
Phone - 713-781-6100
FAX - 713-953-8420

Pioneer Standard
1826 Kramer Lane, Suite D
Austin, TX 78758
Phone - 512-835-4000
FAX - 512-835-9829

Pioneer Electronics
13765 Beta
Dallas, TX 75244
Phone - 214-386-7300
FAX - 214-490-6419

Pioneer Standard
10530 Rockley Rd., Suite 100
Houston, TX 77099
Phone - 713-495-4700
FAX - 713-495-5642

Wyle Laboratories
4030 W. Braker, Suite 330
Austin, TX 78759
Phone - 512-345-8853
FAX - 512-834-0981

Wyle Laboratories
1810 N. Greenville Avenue
Richardson, TX 75081
Phone - 214-235-9953
FAX - 214-644-5064

Wyle Laboratories
11001 S. Wilcrest, Suite 100
Houston, TX 77099
Phone - 713-879-9953
FAX - 713-879-6540

Military Distributor

Zeus Components, Inc.
1800 N. Glenville, Suite 120
Richardson, TX 75081
Phone - 214-783-7010
FAX - 214-234-4385

UTAH

Representative

Wescom Marketing
3500 So. Main, Suite 100
Salt Lake City, UT 84115
Phone - 801-269-0419
FAX - 801-269-0665

Distributors

Anthem Electronics Incorporated
1279 West 2200 South
Salt Lake City, UT 84119
Phone - 801-973-8555
FAX - 801-973-8909

Hall-Mark Electronics Corporation
2265 South 1300 West
West Valley City, UT 84119
Phone - 801-972-1008
FAX - 303-790-4991

Wyle Laboratories
1325 West 2200 South, Suite E
West Valley City, UT 84119
Phone - 801-974-9953
FAX - 801-972-2524

Military Distributor

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

VERMONT

Representative

Advanced Tech Sales Incorporated
348 Park Street, Ste 102
North Reading, MA 01864
Phone - 508-664-0888
FAX - 508-664-5503

Distributors

Anthem Electronics
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
FAX - 508-657-6008

Hall-Mark Electronics Corporation
Pinehurst Park, 6 Cook Street
Billerica, MA 01821
Phone - 617-935-9777
FAX - 617-667-4129

Pioneer Standard
44 Hartwell Avenue
Lexington, MA 02173
Phone - 617-861-9200
FAX - 617-863-1547

Military Distributor

Zeus Components, Inc.
11 Lakeside Office Park
607 North Avenue
Wakefield, MA 01880
Phone - 617-246-8200
FAX - 617-246-8293

VIRGINIA

Representative

Electronic Enginnering & Sales Incorporated
235 Prince George Street
Annapolis, MD 21401
Phone - 301-269-6573
FAX - 301-269-6476

Distributors

Anthem Electronics
9020A Mendenhall Court
Columbia, MD 21045
Phone - 301-995-6640
FAX - 301-381-4379

Hall-Mark Electronics Corporation
10240 Old Columbia Road
Columbia, MD 21046
Phone - 301-988-9800
FAX - 301-381-2036

Pioneer Technologies
15810 Gaither Drive
Gaithersburg, MD 20877
Phone - 301-921-0660
FAX - 301-921-3852

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

WASHINGTON

Representative

Northwest Marketing Associates, Inc.
12835 Bel-Red Road, Ste. 330
Bellevue, WA 98005
Phone - 206-455-5846
FAX - 206-451-1130

Distributors

Almac Electronics
14360 Southeast Eastgate West
Bellevue, WA 98007
Phone - 206-643-9992
FAX - 206-643-9709

Almac Electronics
East 10905 Montgomery
Spokane, WA 99206
Phone - 509-924-9500
1-800-325-6545
FAX - 509-928-6096

Anthem Electronics Incorporated
19017-120th Ave. N.E., Ste. 102
Bothell, WA 98011
Phone - 206-483-1700
FAX - 206-486-0571

Hall-Mark Electronics Corporation
250 Northwest 39th, Suite #4
Seattle, WA 98107
Phone - 206-547-0415
FAX - 314-291-0362

Wyle Laboratories
15385 NE 90th Street
Redmond, WA 98052-3522
Phone - 206-881-1150
FAX - 206-453-0071

Military Distributor

JAN Devices, Inc.
6925 Canby, Bldg. 109
Reseda, CA 91335
Phone - 818-708-1100
FAX - 818-708-7436

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose, CA 95119
Phone - 408-629-4789
FAX - 408-629-4892

WEST VIRGINIA

Representative

Scott Electronics, Inc.
916 Eastwind Drive
Westerville, OH 43081-3379
Phone - 614-882-6100
FAX - 614-882-0900

Distributor

Hall-Mark Electronics Corporation
400 E Wilson Bridge Rd, Ste S
Worthington, OH 43085
Phone - 614-888-3313
FAX - 614-888-0767

Military Distributor

Zeus Components, Inc.
8930-A Route 108
Columbia, MD 21045
Phone - 301-997-1118
FAX - 301-964-9784

WISCONSIN

Representative

Oasis Sales Corporation
1305 North Barker Road
Brookfield, WI 53005
Phone - 414-782-6660
FAX - 414-782-7921

Distributors

Hall-Mark Electronics Corporation
16255 West Lincoln Avenue
New Berlin, Wisconsin 53151
Phone - 414-797-7844
FAX - 414-797-9259

Pioneer Standard
120 Bishops Way, #163
Brookfield, WI 53005
Phone - 414-784-3480
FAX - 414-784-8207

Military Distributors

Zeus Components, Inc.
100 Midland Ave.
Port Chester, NY 10573
Phone - 914-937-7400
FAX - 914-937-2553

Zeus Components, Inc.
2912 Springboro West, Ste 106
Dayton, OH 45439
Phone - 513-293-6162
FAX - 513-293-1781

WYOMING

Representative

Wescom Marketing
3500 South Main, Suite 100
Salt Lake City, UT 84115
Phone - 801-269-0419
FAX - 801 - 269-0665

Distributors

Anthem Electronics Incorporated
1279 West 2200 South
Salt Lake City, UT 84119
Phone - 801-973-8555
FAX - 801-973-8909

Hall-Mark Electronics Coporation
2265 South 1300 West
West Valley City, UT 84119
Phone - 801-972-1008
FAX - 303-790-4991

Wyle Laboratories
1325 West 2200 South, Suite E
West Valley City, UT 84119
Phone - 801-974-9953
FAX - 801-972-2524

Military Distributor

JAN Devices, Inc.
6925 Canby, Bldg. 109
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FAX - 818-708-7436

Zeus Components, Inc.
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AUSTRALIA

Representative

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FAX - 612-953-9683

AUSTRIA

Distributor

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Hietzinger Hauptstrasse
22/A/2
A-1130 Vienna
Austria
Phone - 431-82-56-45
FAX - 431-82-84-920

BELGIUM

Representative & Distributor

MCA - Tronix SPRL
Parc De Recherches Du
Sart Tilman
Av. Des Noisetiers
B-4031 Angleur
Belgium
Phone - 32-41-67-4208
FAX - 32-41-67-6331

DENMARK

Distributor

Henckel Elektronik
Industriparken 4
4960 Holeby
Denmark
Phone - 45-53-906333
FAX - 45-53-906422

FINLAND

Representative & Distributor

Integrated Electronics OY AB
Turkhaudantie 1
P.O. Box 160
00700 Helsinki
Finland
Phone - 358-0-351-3133
FAX - 358-0-351-3134

FRANCE

Representative

Rep'Tronic, SA
1 bis, Rue Marcel Paul
Batiment A
Z.I. De La Bonde
91300 Massy
Phone - 33-1-60-13-9300
FAX - 33-1-60-13-9198

Distributors

Datadis
3 bis, rue Rene Cassin
BP 84-Z.I. de la Bonde
91303 Massy Cedex
France
Phone - 331-69-204141
FAX - 331-69-204900

LEX Electronics
60-62, rue des Gemeaux-Silic 580
94653 Rungis Cedex
France
Phone - 33-1-49-78-4848
FAX - 33-1-49-78-0699

Paris Sud Electronique
12, rue Rene Cassin
91300 Massy
France
Phone - 33-1-69-20-6699
FAX - 33-1-69-20-7532

RTF Diffusion
79 Rue Pierre Semard
92320 Chatillon
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Phone - 1-49-65-2626
FAX - 1-49-65-2649

GERMANY

Representative

Advanced Semi Conductor Products
Kapellenstrasse 9
D-8025 Unterhaching
Munich, Germany
Phone - 49-89-61-9076
FAX - 49-89-61-9070

Distributor

Metronik GmBH
Leonhardsweg 2
8025 Unterhaching
Germany
Phone - 089-611-08-0
FAX - 089-611-64-68

HONG KONG

Representative

Lestina International Ltd.
Rm 405, Park Tower
15 Austin Rd
Tsimshatsui, Kowloon
Hong Kong
Phone - 852-735-1736
FAX - 852-730-7538

INDIA

Distributor

Silicon Electronics
3350 Scott Blvd.
Suite 1201
Santa Clara, CA 95054
Phone - 408-988-4408
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INDONESIA

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Desner Electronics
(FE) Ltd.
42 Mactaggart Rd.
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Singapore, 1336
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IRELAND

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Malahide County Dublin
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Phone - 353-1-450635
FAX - 353-1-453625

Distributor

Lyco, Ltd.
Estuary House
New Street
Malahide, Dublin
Ireland
Phone - 353-1-452-020
FAX - 353-1-452-414

ISRAEL

Representative/Distributor

Rapac Electronic, Ltd.
Mailing Address:
P.O. Box 18053
Tel Aviv, Israel 61180
Office Address:
#7, Kehilat Saloniki Street
Tel Aviv, Israel 69513
Phone - 972-3-477115
FAX - 972-3-493-272

ITALY

Representative & Distributor

Moxel S.R.L.
Via C Frova 34
20092 Cinisello Balsamo
(MI) Italy
Phone - 39-261290521
FAX - 39-261-72582

Distributor

EUR Elettronica S.P.A.
20094 Assago (MI)
Sede: Via E. Fermi, 8
Partita IVA 00883800153
Italy
Phone - 02-4880022
FAX - 02-4880275

JAPAN

Distributor

Sanyo Electronic Co.
Natsume Bldg., 4th Floor
18-6, 2-Chome
Yushima, Bunkyo-Ku, Tokyo 113
Japan
Phone - 81-3-3818-4330
FAX - 813-3818-1124

KOREA

Representative

Eastern Electronics, Inc.
3rd Floor, Yoowha Bldg.
995-16, Daechi-Dong
Kangnam-Ku, Seoul, Korea
Phone - 822-553-2997
FAX - 822-553-2998

THE NETHERLANDS

Distributor

Microtron
Postbus 188
NL - 1243 ZK Graveland
The Netherlands
Phone - 31-35-61834
FAX - 31-35-62709

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3/36 Bydown Street
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NORWAY

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BIT Elektronikk AS
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FAX - 47-3-845510

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Bromma, Sweden
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FAX - 46-8-262286

SWITZERLAND

Representative

Micron Technology
Casa Fuchs CH-6984
Pura Switzerland
Phone - 41-9171-3785
FAX - 41-9171-3889

Distributor

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Switzerland
Phone - 41-42-412-441
FAX - 41-42-413-124

Pabstronic AG
Aarauerstrasse 20
5200 Brugg
Switzerland
Phone - 41-56-41-7957
FAX - 41-56-41-0792

TAIWAN, R.O.C.

Representative & Distributor

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7F, No. 344-1 Min-Sheng E Rd
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Distributor

Abacus Electronics PLC
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Newbury, Bukshire
RG14 5SF
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FAX - 0635-38670

Bytech Computers, Ltd.
12 A Cedarwood, Chineham
Business Park
Crockford Lane, Basingstoke
Hampshire, RG24 OWD
United Kingdom
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FAX - 44-256-707-162

Thame Components
Thame Park Road
Thame, Oxon, 0X9 3UQ
United Kingdom
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