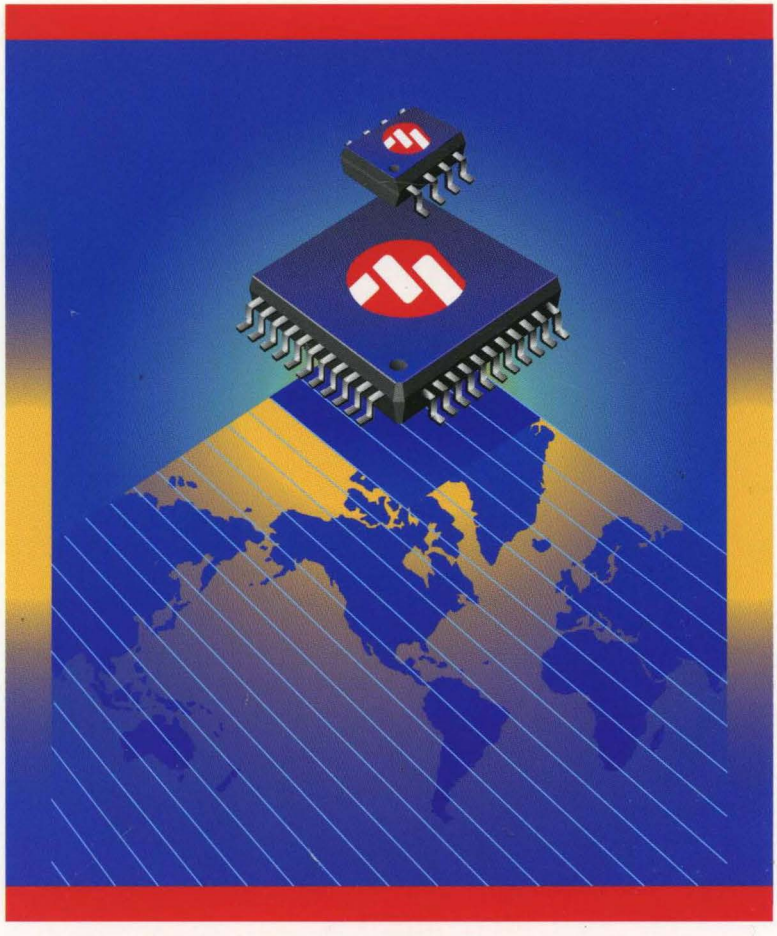
MICROCHIP DATA BOOK

1994

MICROCHIP

MICROCHIP DATABOOK



1994

MICROCHIP

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Microchip Data Book

1994 Edition

SERVING A COMPLEX AND COMPETITIVE
WORLD WITH FIELD-PROGRAMMABLE
EMBEDDED CONTROL
SYSTEM SOLUTIONS

April 1994 /DS00018G

MICROCHIP

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SECTION 1
INTRODUCTION TO MICROCHIP TECHNOLOGY INC.

SERVING A COMPLEX AND COMPETITIVE WORLD WITH FIELD-PROGRAMMABLE EMBEDDED CONTROL SYSTEM SOLUTIONS

Motivated by customer requirements....

"Microchip Technology draws its impetus from the technology expectations of a large base of long-standing customers. Microchip is small enough to respond quickly with technology to serve our customers' needs. Moreover, as a fully integrated IC manufacturer, Microchip deploys its panoply of resources to act timely and efficiently, and on a worldwide scale: Technology Development, Design, Wafer Fabrication, Assembly and Test, Quality, Reliability and Customer Support.

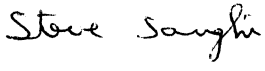
...and powered by continuous improvement...

"Worldwide competition leaves no room for divergence or mediocrity. Microchip Technology, committed to focus on and continuously improve all the aspects of its business, has a unique corporate culture. To improve performance, our employees are encouraged to analyze their methods continually. Personal empowerment expands the capability of personal responsibility to continually serve our customers better.

...riding, leading and pushing the wave of technological change.

"Our industry's life-line is innovation. The fast pace of technological change is inherent in our industry. Microchip Technology has accelerated the rate of change of its technology and products to leadership in providing user-programmable space-sensitive embedded control solutions.

"Change is our ally. Driving and managing customer-focused change is our winning strategy."



Steve Sanghi
President & Chief Executive Officer

MICROCHIP TECHNOLOGY INCORPORATED

Company Profile

HIGHLIGHTS

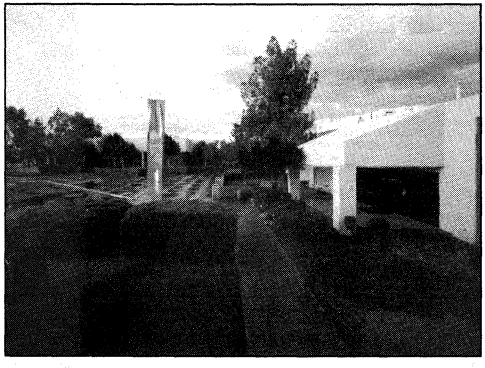
- Focused on providing high-performance, field-programmable embedded control solutions
- An experienced executive team focussed on innovation
- Offers RISC 8-bit user-programmable microcontrollers and supporting logic products
- Offers Serial and Parallel EEPROMs and EPROMs
- Complementary Application Specific Standard Products
- Fully integrated manufacturing
- A global network of manufacturing and customer support facilities
- A unique corporate culture dedicated to continuous improvement

BUSINESS SCOPE

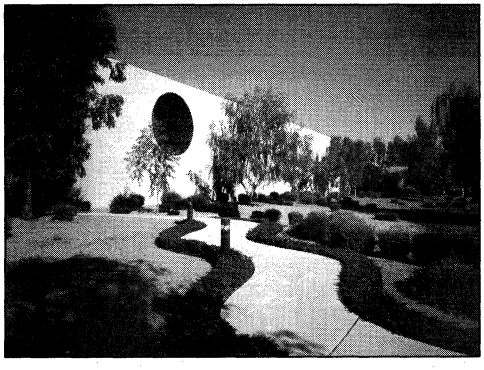
Microchip Technology Inc. manufactures and markets a variety of VLSI CMOS semiconductor components to support the field-programmable embedded control market. In particular, the company specializes in highly integrated, field-programmable RISC microcontrollers, application specific standard products and related non-volatile memory products to meet growing market requirements for high performance, yet economical embedded control capability in an increasing number of price-sensitive products. Microchip's products feature the industry's most economical OTP (one-time programmable) capability, along with the compact size, integrated functionality, ease of development and technical support so essential to timely and cost-effective product development by our customers.

MARKET FOCUS

Microchip targets selected markets where our advanced designs, progressive process technology and industry leading operating speeds enable us to deliver decidedly superior performance. The company has positioned itself to maintain a dominant role as a supplier of high performance field-programmable microcontrollers and associated memory and logic products for embedded control applications.



Chandler, Arizona:
Company headquarters near Phoenix, Arizona; executive offices, R & D and wafer fabrication occupy this 142,000-square-foot facility.



Tempe, Arizona:
New 170,000-square-foot wafer fabrication facility.

MICROCHIP

- Mission Statement -

Microchip Technology Incorporated is a leading supplier of field-programmable embedded control solutions by providing RISC microcontrollers and related non-volatile memory products. In order to contribute to the ongoing success of customers, shareholders and employees, our mission is to focus resources on high value, high quality products and to continuously improve all aspects of our business, providing a competitive return on investment.

- Guiding Values -

Customers Are Our Focus: We establish successful customer partnerships by exceeding customer expectations for products, services and attitude. We start by listening to our customers, earning our credibility by producing quality products, delivering comprehensive services and meeting commitments. We believe each employee must effectively serve their internal customers in order for Microchip's external customers to be properly served.

Quality Comes First: We will perform correctly the first time, maintain customer satisfaction and measure our quality against requirements. We practice effective and standardized improvement methods, such as statistical process control to anticipate problems and implement root cause solutions. We believe that when quality comes first, reduced costs follow.

Continuous Improvement Is Essential: We utilize the concept of "Vital Few" to establish our priorities. We concentrate our resources on continuously improving the Vital Few while empowering each employee to make continuous improvements in their area of responsibility. We strive for constructive and honest self-criticism to identify improvement opportunities.

Employees Are Our Greatest Strength: We design jobs and provide opportunities promoting employee teamwork, productivity, creativity, pride in work, trust, integrity, fairness, involvement, development and empowerment. We base recognition, advancement and compensation on an employee's achievement of excellence in team and individual performance. We provide for employee health and welfare by offering competitive and comprehensive employee benefits.

Products And Technology Are Our Foundation: We make ongoing investments and advancements in the design and development of our manufacturing process, device, circuit, system and software technologies to provide timely, innovative, reliable and cost effective products to support current and future market opportunities.

Total Cycle Times Are Optimized: We focus resources to optimize cycle times to our internal and external customers by empowering employees to achieve efficient cycle times in their area of responsibility. We believe that cycle time reduction is achieved by streamlining processes through the systematic removal of barriers to productivity.

Safety Is Never Compromised: We place our concern for safety of our employees and community at the forefront of our decisions, policies and actions. Each employee is responsible for safety.

Profits And Growth Provide For Everything We Do: We strive to generate and maintain competitive rates of company profits and growth as they allow continued investment for the future, enhanced employee opportunity and represent the overall success of Microchip.

Communication Is Vital: We encourage appropriate, honest, constructive, and ongoing communication in company, customer and community relationships to resolve issues, exchange information and share knowledge.

Suppliers, Representatives, And Distributors Are Our Partners: We strive to maintain professional and mutually beneficial partnerships with suppliers, representatives, and distributors who are an integral link in the achievement of our mission and guiding values.

Professional Ethics Are Practiced: We manage our business and treat customers, employees, shareholders, investors, suppliers, distributors, representatives, community and government in a manner that exemplifies our honesty, ethics and integrity. We recognize our responsibility to the community and are proud to serve as an equal opportunity employer.

FULLY INTEGRATED MANUFACTURING

Microchip delivers fast turnaround through total control over all phases of production. Research and development, design, mask making, wafer fabrication, assembly and quality assurance testing are conducted at facilities owned and operated by Microchip. Our integrated approach to manufacturing along with rigorous use of advanced statistical process control (SPC) and a continuous improvement culture has brought forth tight product consistency levels and high yields which enable Microchip to compete successfully in world markets. Microchip's unique approach to SPC provides customers with excellent costs, quality, reliability and on-time delivery.

A GLOBAL NETWORK OF PLANTS AND FACILITIES

Microchip is a global competitor providing local service to the world's technology centers. The Company's focal point is the design and technology advancement facility in Chandler, Arizona. Product and technology development is here, along with front-end wafer fabrication and electrical probing.

In late 1993, Microchip purchased a second wafer fabrication facility in Tempe, Arizona - thirteen miles from its existing Chandler, Arizona, operations. The additional 170,000 square foot facility will be equipped with process equipment for use in meeting future production volumes beyond those which could be efficiently produced in Microchip's single existing wafer facility. Initial production from the new Tempe facility is anticipated to begin by late 1994.

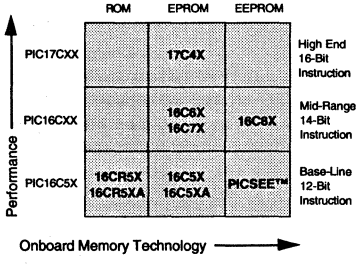
Microchip's assembly and test facility in Kaohsiung, Taiwan houses the technology and modern assembly methods necessary for plastic and ceramic packaging. Other quality-conscious firms which fabricate wafers in the Pacific Rim use Microchip's Kaohsiung plant for assembly.

Sales and application offices are located in key cities throughout the Western Hemisphere, Pacific Rim and Europe. Offices are staffed to meet the high quality expectations of our customers, and can be accessed for technical support, purchasing information and failure analysis.

A PRODUCT FAMILY OF SHARED STRENGTHS

Microchip's product focus is CMOS field-programmable microcontrollers, non-volatile memories and peripherals, and application specific standard products (ASSP). These product lines include PIC16/17 microcontrollers, Serial and Parallel EEPROMs, high-speed EPROMs, and peripherals in a broad range of product densities, speeds and packages.

MICROCONTROLLERS



CMOS PIC16/17 Microcontroller Families

PIC16/17 microcontrollers from Microchip combine high performance, low cost and small package size. They offer the best price/performance ratio in the industry. Large numbers of these devices are used in automotive and cost-sensitive consumer products, computer peripherals, office automation, automotive control systems, security and telecommunication applications.

The widely-accepted CMOS PIC16CXX and PIC17CXX families are the industry's only 8-bit microcontrollers using a high-speed RISC architecture. Microchip pioneered the use of RISC architecture to obtain high speed and instruction efficiency. The CMOS PIC16CXX family is in high-volume production, with more than 60 million units shipped, and has achieved more than five thousand design wins worldwide.

The PIC17CXX family offers the world's fastest execution performance of any 8-bit microcontroller family. The PIC17CXX family extends the PIC16/17 microcontroller's high-performance RISC architecture with a 16-bit instruction word, enhanced instruction set and powerful vectored interrupt handling capabilities. The first member of the family, the PIC17C42, includes a powerful array of intelligent and precise on-chip peripheral features that are ideally suited for many demanding real-time embedded control applications including motor control, process control, security, automotive and medical applications. In addition, the PIC17C42 can function either as a stand-alone microcontroller or can execute instructions from up to 64K words of external

program memory. The PIC17C42 features comprehensive timer/counter resources and I/O handling capabilities to address the requirements of complex embedded control applications.

Current CMOS PIC16/17 microcontroller product families include advanced features such as sophisticated timers, embedded A/D, extended instruction/data memory, inter-processor communication and ROM, EPROM and EEPROM memories.

Both PIC16CXX and PIC17CXX families are supported by user-friendly development systems including programmers and emulators.

DEVELOPMENT SYSTEMS

The PICMASTER™ is an advanced real-time in-circuit emulator system using the user-friendly Windows™ software environment. The PICMASTER is a Microchip-designed universal emulator for both PIC16CXX and PIC17CXX families. The PRO MATE™ is an advanced full-featured programmer. PICSTART™ is a low-cost development kit which includes an assembler, simulator and programmer.

SOFTWARE SUPPORT

Both PIC16/17 microcontroller families are supported by assemblers, linker/loaders, libraries and a source-level debugger. The PIC16CXX family is also supported by a software simulator.

Customers can obtain on-line updates on Microchip Development Systems and Support Software via the Bulletin Board System (BBS). Please refer to the Microchip BBS product brief in Section 9 for specific access information.

SERIAL EEPROMS

Microchip offers one of the broadest selections of CMOS Serial EEPROMs on the market for embedded control systems. Serial EEPROMs are available in variety of densities, operating voltages, bus interface protocols, operating temperature ranges and space saving packages. The company has developed the world's first 64K Smart Serial™ EEPROM which currently offers four times the speed, four times the memory and four times the features of any competitive 2-wire Serial EEPROM. Device densities range from 256K bits up to 64K bits. In addition to 5 volt-only operation, Microchip offers Serial EEPROMs that read and write down to 2.5, 2 or 1.8 volts. I²C™, Microwire™ and 4-wire bus interface protocols are standard. Devices come in three standard operating temperature ranges; commercial, industrial and automotive. Small footprint packages include: 8-lead DIP, 8-lead SOIC in JEDEC and EIAJ body widths and 14-lead SOIC. Other key features of the Serial EEPROM product line include: electrostatic discharge (ESD) protection greater than 4K volts and endurance of 100K cycles minimum and one million typical.

Microchip is a high-volume supplier of Serial EEPROMs to all the major markets worldwide, including consumer, automotive, industrial, computer and communications. To date, more than 100 million units have been produced. Microchip is continuing to develop additional unique Serial EEPROMs.

PARALLEL EEPROMS

The CMOS Parallel EEPROM devices from Microchip are available in 4K, 16K and 64K densities. The manufacturing process used for these EEPROMs ensures 10,000 to 100,000 write and erase cycles typically. Data retention is more than 10 years. Fast write times are less than 200 μsec. These EEPROMs work reliably under demanding conditions and operate efficiently at temperatures from –40°C to +125°C. Microchip's expertise in advanced SOIC, TSOP and VSOP surface mount packaging supports our customers' needs in space-sensitive applications.

Typical applications include computer peripherals, engine control, pattern recognition and telecommunications.

EPROMS

Microchip's CMOS EPROM devices are produced in densities from 64K to 512K. High Speed EPROMs have access times as low as 55 nanoseconds. Typical applications include computer peripherals, instrumentation, and automotive devices. Microchip's expertise in Surface Mount Packaging on SOIC, TSOP and VSOP packages led to the development of the Surface Mount one-time-programmable (OTP) EPROM market where Microchip is the #1 supplier today. Microchip is also a leading supplier of low-voltage EPROMs for battery powered applications.

APPLICATION SPECIFIC STANDARD PRODUCTS (ASSP)

Microchip's new Application Specific Standard Product (ASSP) Division provides value-added embedded control solutions by combining PIC16/17 microcontroller architecture with innovative software, silicon and assembly technology. These products incorporate technology that will offer a complete solution that is both unique to the customer and standard in manufacture to Microchip. The mission of this family is to offer a complete solution which reduces or removes the barriers for customers to use Microchip solutions in their products through the use of software embedded in secure OTP- or ROM-based microcontrollers. The family is packaged to provide the highest integration to the customer at the best overall system cost.

The MTA11XXX family is the most accurate and most integrated battery management and charging solution available today. The family incorporates Microchip/SPAN patented *TrueGauge*™ technology which digitally integrates battery charge and discharge current to provide an accurate (<3% typical) state of charge indication. The family operates with NiCd and NiMH battery packs from 3 Vdc to 30 Vdc. These products are ideal for portable PC, cellular phone and portable consumer product applications.

Ease of use, low voltage and low cost make the MTA41XXX mouse and trackball MCU firmware solutions ideal for implementing new designs for both PCs and Apple®computers. The products in the MTA41XXX family are 18-lead, low-power CMOS microcontroller ICs combined with application-specific software. By adding a few external components, the user can easily realize a complete mouse or trackball system.

The MTA810XX PICSEE™ family of cost-effective system solutions integrate PIC16/17 microcontrollers with EEPROM technology. These PICSEE devices are ideally suited for automotive security, keyless entry, remote control, data acquisition and telecommunication applications. The combined product assembly techniques provide the user the highest performance solution in a compact and cost-effective package.

Future ASSP products will include advanced features such as mixed analog and digital capability as well as an ever broadening family of turnkey software solutions for the embedded control market.

OTHER MICROCHIP PRODUCTS

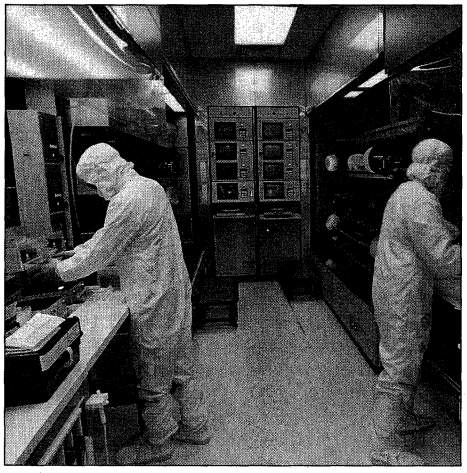
Other Microchip products, such as Liquid Crystal Display Drivers, are mature products with proven track record and a large, repeat customer base.

A HISTORY OF INNOVATION

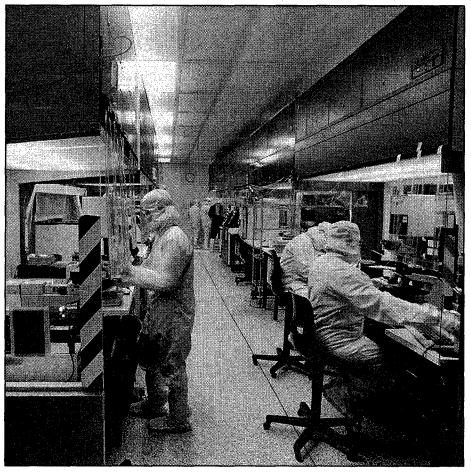
Microchip has a long history of innovation in the semiconductor industry. For more than a quarter century, Microchip and its former parent company have been developers of leading-edge, cost-effective logic and memory products.

Microchip is credited with a number of firsts: The Metal-Oxide-Silicon (MOS) Integrated Circuit, DRAM, Serial EEPROM, Reduced Instruction Set Computer (RISC) microcontroller product family, UART, CMOS 64K EEPROM, and CMOS single chip DSP are all innovations that were originally developed and introduced by Microchip engineers.

CHANDLER, AZ FACILITY



Chandler Wafer Fabrication: Diffusion Area



Chandler Wafer Fab: Sub-micron Alignment Area

TAIWAN FACILITY

Microchip's assembly and test operation in Kaohsiung, Taiwan received the prestigious Ishikawa Award for assembly and testing excellence.

The Microchip Kaohsiung plant's excellent track record and continuing efforts to achieve higher levels of quality and technological advancement has resulted in superior yields and fast turnaround.

FUTURE PRODUCTS AND TECHNOLOGY

New process technology is constantly being developed for microcontroller, ASSP, EEPROM and high-speed EPROM products. Advanced process technology modules are being developed that will be integrated into present product lines to continue to achieve a range of compatible processes. Current production technology utilizes dimensions down to 0.9 microns.

Microchip's research and development activities, include exploring new process technologies and products that have industry leadership potential. Particular emphasis is placed on products that can be put to work in high-performance broad-based markets.

Equipment is continually updated to bring the most sophisticated process, CAD and testing tools on line. Cycle times for new technology development are continuously reduced by using in-house mask making, a high-speed pilot line within the manufacturing facility and continuously improving methodologies.

More advanced technologies are under development, as well as advanced CMOS RISC-based microcontroller, ASSP and CMOS EEPROM and EPROM products. Objective specifications for new products are developed by listening to our customers and by close cooperation with our many customer-partners worldwide.

QUALITY WITHOUT COMPROMISE

Product reliability is designed into Microchip products at the outset. Wide design margins are established to guarantee that every product can be produced easily, error-free and within the tolerances of the manufacturing process.

All quality assurance tests are tighter than customer specifications. Products are tested at least two machine tolerances tighter than those specified by the customer.

Every new product is qualified under accelerated stress testing. Test samples encompass the full range of processed tolerances at each step. Data sheets detailing these processes enable customers to reach accurate decisions based on known quantitative values.

To determine whether a process is within normal manufacturing variation, industry-leading statistical control techniques are put to work at each process step. In-process controls are performed by operators in the wafer fabrication division and immediate corrective action is taken if they deem a process is out of tight control limits. Products are also sampled weekly through a variety of carefully monitored stress and accelerated life tests.

Microchip's documentation control program assures the correct document is always available at the point of use. Active documents are serialized and stamped to eliminate the possibility of performing a job from obsolete or incorrect instructions.

Individuals in all departments continuously analyze the methods employed at their positions and formulate plans to improve performance. In all areas of our business, everyone is expected to make continuous improvement.

A QUALITY AND RELIABILITY ALLIANCE WITH CUSTOMERS

Microchip works together with customers to establish mutual programs to improve the performance of our products in their systems. We go beyond the incoming inspection level and specification by extending our quality and reliability support to the point where the customer ships the system. Microchip's quality programs ensure that our products can be used with such impunity, a customer can implement improvement programs based on Microchip as your leading supplier.

SECTION 2
8-BIT MICROCONTROLLER PRODUCT SPECIFICATIONS

PIC16/17 Family of 8-Bit Microcontrollers Cross-Reference Guide

		Clock	Memory					Peripherals					Features‡						
		Maximum Frequency of Operation (MHz)	Program Memory EPROM	Program Memory ROM	Data Memory EEPROM	Data Memory (bytes)	Data EEPROM (bytes)	Timer Module(s) †	Capture/Compare/PWM Module	Serial Port (s) (SPI/I²C, SCI)	Parallel Slave Port	Analog to Digital Converter (8-bit)	External Interrupts	Interrupts Sources	I/O	Voltage Range (Volts)	Number of Instructions	Packages	Page #
High-end	PIC17C42§	25	2K	—	—	128	—	TMR0, TMR1, TMR2,TMR3	—	SCI	—	—	Yes	11	33	4.5 - 5.5	55	40-pin DIP, 44-pin PLCC 44 pin QFP	2-603
Mid-range	PIC16C64	20	2K	—	—	128	—	TMR0, TMR0, TMR2	1	SPI/I²C	Yes	—	Yes	8	33	2.5 - 6.0	35	40-pin DIP, 44-pin PLCC 44 pin QFP	2-221
	PIC16C71	16	1K	—	—	36	—	TMR0	—	—	—	4 ch	Yes	4	13	3.0 - 6.0	35	18-pin DIP, 18-pin SOIC 44 pin QFP	2-327
	PIC16C74	20	4K	—	—	192	—	TMR0, TMR1, TMR2	2	SPI/I²C, SCI	Yes	8 ch	Yes	12	33	2.5 - 6.0	35	40-pin DIP, 44-pin PLCC 44 pin QFP	2-399
	PIC16C84	10	—	—	1K	36	64	TMR0	—	—	—	—	Yes	4	13	2.0 - 6.0	35	18 pin DIP, 18 pin SOIC 20-pin SSOP	2-535
Base Line	PIC16C54	20	512	—	—	25	—	RTCC	—	—	—	—	—	0	12	2.5 - 6.25	33	18-pin DIP, 18-pin SOIC 20-pin SSOP	2-3
	PIC16C54A	20	512	—	—	25	—	RTCC	—	—	—	—	—	0	12	2.5 - 6.25	33	18-pin DIP, 18-pin SOIC 20-pin SSOP	2-95
	PIC16CR54	20	—	512	—	25	—	RTCC	—	—	—	—	—	0	12	2.5 - 6.25	33	18-pin DIP, 18-pin SOIC 20-pin SSOP	2-55
	PIC16C55	20	1K	—	—	25	—	RTCC	—	—	—	—	—	0	20	2.5 - 6.25	33	28-pin DIP, 28-pin SOIC 28-pin SSOP	2-3
	PIC16C56	20	1K	—	—	25	—	RTCC	—	—	—	—	—	0	12	2.5 - 6.25	33	18-pin DIP, 18-pin SOIC 20-pin SSOP	2-3
	PIC16C57	20	2K	—	—	72	—	RTCC	—	—	—	—	—	0	20	2.5 - 6.25	33	28-pin DIP, 28-pin SOIC 28-pin SSOP	2-3
	PIC16CR57A	20	—	2K	—	72	—	RTCC	—	—	—	—	—	0	20	2.5 - 6.25	33	28-pin DIP, 28-pin SOIC 28-pin SSOP	2-181
	PIC16C58A	20	2K	—	—	72	—	RTCC	—	—	—	—	—	0	12	2.5 - 6.25	33	18-pin DIP, 18-pin SOIC 20-pin SSOP	2-137

† PIC17C42 can concantinate Timer1 and Timer2 to form a 16-bit Timer. Timer0 is 16-bit with 8-bit prescaler.
‡ All PIC16/17 Family devices have Power-on Reset, fuse selectable Watchdog Timer, fuse selectable code protect and high output current (20mA source / 25mA sink).
§ The PIC17C42 can also operate in microprocessor or external microcontroller mode.

NOTES:

MICROCHIP

PIC16C5X

EPROM-Based 8-Bit CMOS Microcontroller Series

FEATURES

High-Performance RISC-like CPU

- Only 33 single word instructions to learn
- All single cycle instructions (200ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200ns instruction cycle
- 12-bit wide instructions
- 8-bit wide data path
- 512 - 2K x 12 on-chip EPROM program memory
- 25 - 72 x 8 general purpose registers (SRAM)
- Seven special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features

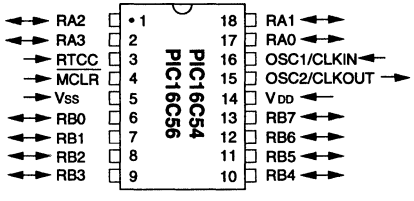
- 12 - 20 I/O pins with individual direction control
- 8-bit real time clock/counter (RTCC) with 8-bit programmable prescaler
- Power-On Reset
- Oscillator Start-up Timer
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security EPROM fuse for code-protection
- Power saving SLEEP mode
- EPROM fuse selectable oscillator options:
  - Low-cost RC oscillator: RC
  - Standard crystal/resonator: XT
  - High-speed crystal/resonator: HS
  - Power saving, low frequency crystal: LP

CMOS Technology

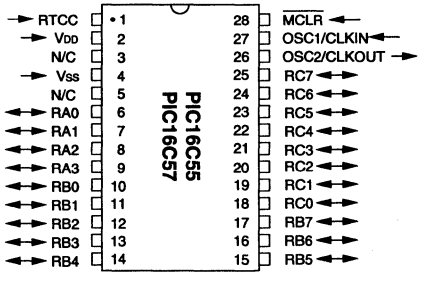
- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide-operating voltage range:
  - Commercial: 2.5V to 6.25V
  - Industrial: 2.5V to 6.25V
  - Automotive: 2.5V to 6.0V
- Low-power consumption
  - < 2mA typical @ 5V, 4 MHz
  - 15μA typical @ 3V, 32 KHz
  - < 3μA typical standby current @ 3V, 0°C to 70°C

FIGURE A - PIN CONFIGURATIONS

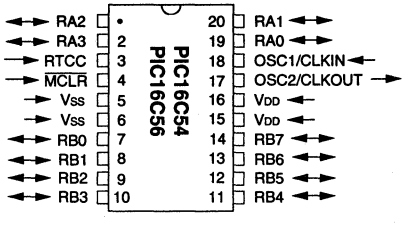
PDIP, SOIC, CERDIP Window



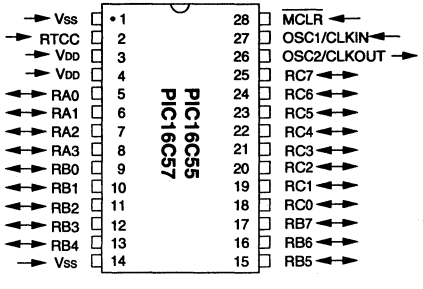
PDIP, SOIC, CERDIP Window



SSOP



SSOP



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1.0 GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family low-cost, high-performance, 8-bit, fully static, EPROM-based CMOS microcontrollers. It employs a RISC-like architecture with only 33 single word/single cycle instructions to learn. All instructions are single cycle (200ns) except for program branches which take two cycles. The PIC16C5X delivers performance an order of magnitude higher than its competitors in similar price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special microcontroller like features that reduce system cost and power requirements. The Power-On Reset and oscillator start-up timer eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator and cost-saving RC oscillator. Power saving SLEEP mode, watchdog timer and code protection features improves system cost, power and reliablity.

The UV-erasable cerdip-packaged versions are ideal for code development, while the cost-effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontroller while benefiting from the OTP flexibility.

The PIC16C5X products are supported by an assembler, a software simulator, an in-circuit emulator and a production quality programmer. All the tools are supported by IBM PC® and compatible machines.

1.1 Applications

The PIC16C5X series fits perfectly in applications ranging from high-speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages for through hole or surface mounting make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

TABLE 1.0.1 - OVERVIEW OF PIC16C5X DEVICES

Part #	EPROM	RAM*	I/O	Package Options
PIC16C54	512 x 12	32 x 8	12	18L windowed CERDIP, 18L PDIP, 18L SOIC (300 mil), 20L SSOP
PIC16C55	512 x 12	32 x 8	20	28L windowed CERDIP, 28L PDIP (600 mil), 28L PDIP (300 mil), 28L SOIC (300 mil), 28L SSOP
PIC16C56	1K x 12	32 x 8	12	18L windowed CERDIP, 18L PDIP, 18L SOIC (300 mil), 20L SSOP
PIC16C57	2K x 12	80 x 8	20	28L windowed CERDIP, 28L PDIP (600 mil), 28L PDIP (300 mil), 28L SOIC (300 mil), 28L SSOP
* Including special function registers.				

2.0 ARCHITECTURAL DESCRIPTION

2.1 Harvard Architecture

The PIC16C5X single-chip microcomputers are low-power, high-speed, full static CMOS devices containing EPROM, RAM, I/O and a central processing unit on a single chip.

The architecture is based on a register file concept with separate bus and memories for data and instructions (Harvard architecture). The data bus and memory (RAM) are 8-bits wide, while the program bus and program memory (EPROM) have a width of 12-bits. This concept allows a simple yet powerful instruction set designed to emphasize bit, byte and register operations under high speed with overlapping instruction fetch and execution cycles. That means that, while one instruction is executed, the following instruction is already being read from the program memory. A block diagram of the PIC16C5X series is given in Figure 2.1.1.

2.2 Clocking Scheme/Instruction Cycle

The clock input (from pin OSC1) is internally divided by four to generate four non overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, PC is incremented every Q1, instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 2.2.1.

FIGURE 2.1.1 - PIC16C5X SERIES BLOCK DIAGRAM

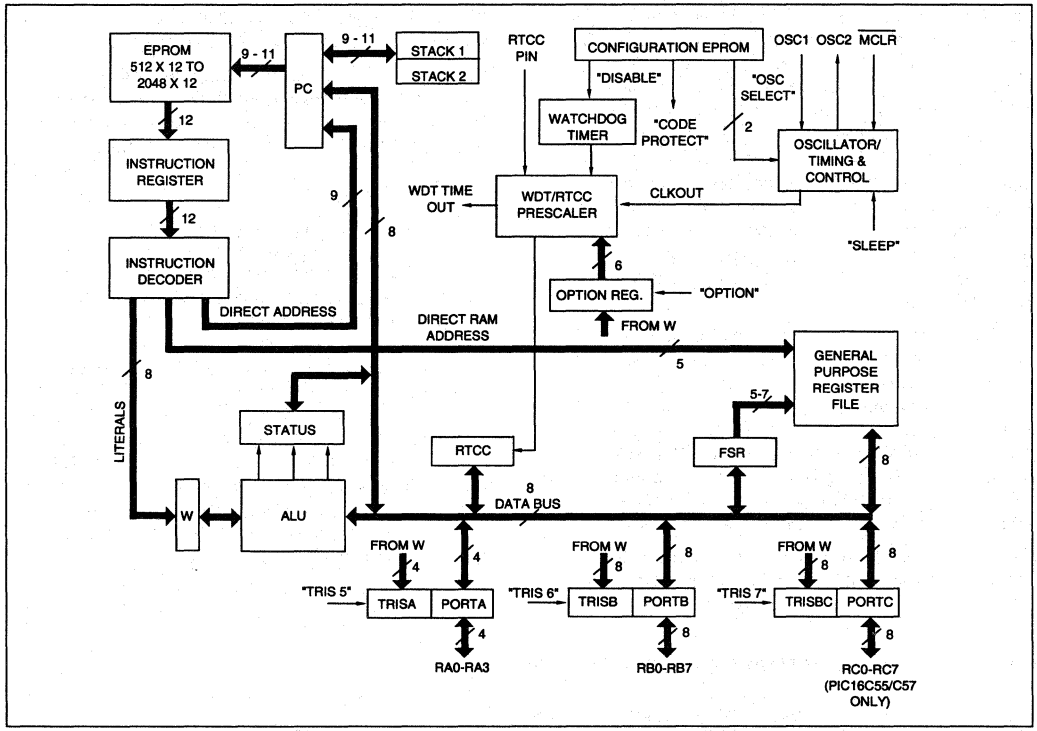


TABLE 2.1.1 - PIN FUNCTIONS

Name	Function
RA0 - RA3	I/O PORTA
RB0 - RB7	I/O PORTB
RC0 - RC7	I/O PORTC (C55/57 only)
RTCC	Real Time Clock/Counter
$\overline{MCLR}$	Master Clear
OSC1/CLKIN	Oscillator (input)
OSC2/CLKOUT	Oscillator (output)
V_{DD}	Power supply
V_{SS}	Ground
N/C	No (internal) Connection

2.3 Data Register File

The 8-bit data bus connects two basic functional elements together: the Register File composed of up to 80 addressable 8-bit registers including the I/O Ports, and an 8-bit wide Arithmetic Logic Unit. The 32 bytes of RAM are directly addressable while a "banking" scheme, with banks of 16 bytes each, is employed to address larger data memories (Figure 4.2.1). Data can be addressed direct, or indirect using the file select register. Immediate data addressing is supported by special "literal" instructions which load data from program memory into the W register.

The register file is divided into two functional groups: operational registers and general purpose registers. The operational registers include the Real Time Clock Counter (RTCC) register, the Program Counter (PC), the Status Register, the I/O registers (PORTs) and the File Select Register. The general purpose registers are used for data and control information under command of the instructions.

In addition, special purpose registers are used to control the I/O port configuration and the prescaler options.

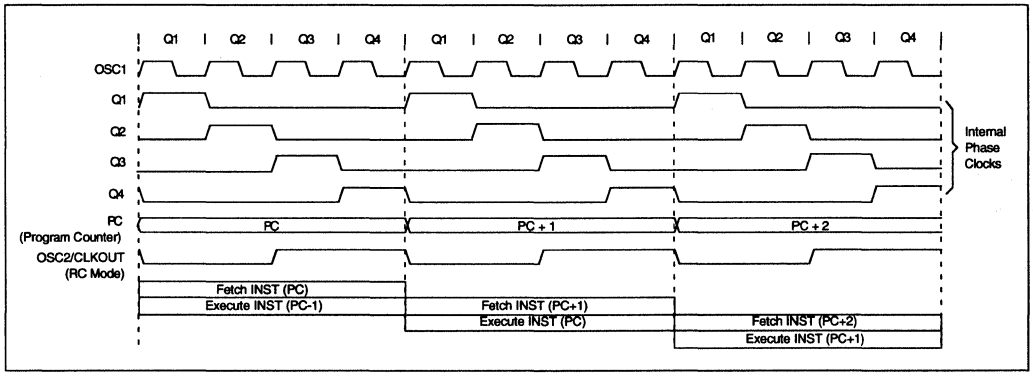
2.4 Arithmetic/Logic Unit (ALU)

The 8-bit wide ALU contains one temporary working register (W Register). It performs arithmetic and Boolean functions between data held in the W Register and any file register. It also does single operand operations on either the W register or any file register.

2.5 Program Memory

Up to 512 words of 12-bit wide on-chip program memory (EPROM) can be directly addressed. Larger program memories can be addressed by selecting one of up to four available pages with 512 words each (Figure 4.3.1). Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments

FIGURE 2.2.1 - CLOCKS/INSTRUCTION CYCLE



to execute in-line programs. Program control operations, supporting direct, indirect, relative addressing modes, can be performed by Bit Test and Skip instructions, Call instructions, Jump instructions or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting.

3.0 PIC16C5X SERIES OVERVIEW

A wide variety of EPROM and RAM sizes, number of I/O pins, oscillator types, frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information and tables in this section. When placing orders, please use the "PIC16C5X Product Identification System" on the back page of this data sheet to specify the correct part number.

3.1 UV Erasable Devices

Four different device versions, as listed in Table 1.0.1, are available to accommodate the different EPROM, RAM, and I/O configurations. These devices are optimal for prototype development and pilot series. The desired oscillator configuration is EPROM programmable as "RC", "XT", "HS" or "LP". An erased device is configured as "RC" type by default. Depending on the selected oscillator type and frequency, the operating supply voltage must be within the same range as a OTP/QTP part would be specified for.

3.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates. OTP devices have the oscillator type pre-configured by the factory, and they are tested only for this special configuration (including voltage and frequency ranges, current consumption).

The program EPROM is erased, allowing the user to write the application code into it. In addition, the watchdog timer can be disabled, and/or the code protection logic can be activated by programming special EPROM fuses. The 16 special EPROM bits for ID code storage are also user programmable.

3.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

4.0 OPERATIONAL REGISTER FILES

4.1 Indirect Data Addressing(INDF)

This is not a physically implemented register. Addressing INDF calls for the contents of the File Select Register to be used to select a file register. INDF is useful as an indirect address pointer. For example, in the instruction ADDWF INDF, W will add the contents of the register pointed to by the FSR to the content of the W Register and place the result in W.

If INDF itself is read through indirect addressing (i.e. FSR = 0h), then 00h is read. If INDF is written to via indirect addressing, the result will be a NOP.

4.2 Real Time Clock/Counter Register (RTCC)

This register can be loaded and read by the program as any other register. In addition, its contents can be incremented by an external signal edge applied to the RTCC pin, or by the internal instruction cycle clock (CLKOUT=fosc/4). Figure 4.1.1 is a simplified block diagram of RTCC.

An 8-bit prescaler can be assigned to the RTCC by writing the proper values to the PSA bit and the PS bits in the OPTION register. OPTION register is a special register (not mapped in data memory) addressable using the 'OPTION' instruction. See Section 7.5 for details. If the prescaler is assigned to the RTCC, instructions writing to RTCC (e.g. CLRF RTCC, or BSF RTCC,5, ...etc.) clear the prescaler.

The bit "RTS" (RTCC signal Source) in the OPTION register determines if RTCC is incremented internally or externally.

RTS=1: The clock source for the RTCC or the prescaler, if assigned to it, is the signal on the RTCC pin. Bit 4 of the OPTION register (RTE) determines, if an increment occurs on the falling (RTE=1) or rising (RTE=0) edge of the signal presented to the RTCC pin.

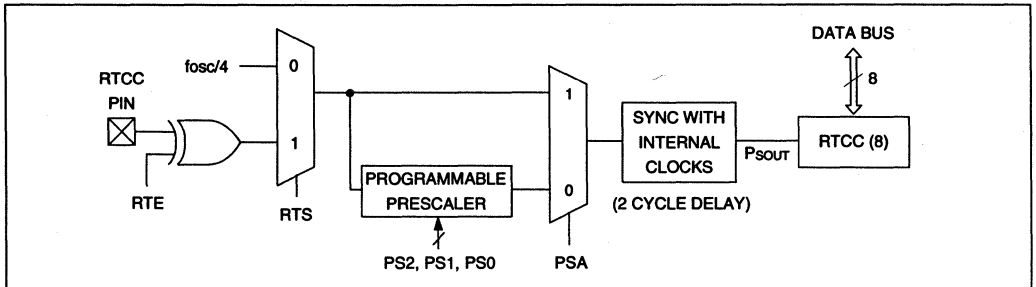
RTS=0: The RTCC register or its prescaler, respectively, will be incremented with the internal instruction clock (= Fosc/4). The "RTE" bit in the OPTION register and the RTCC pin are "don't care" in this case. The RTCC pin must not be left floating (tie to either VDD or Vss). This prevents unintended entering of test modes and to reduce the current consumption in low power applications.

As long as clocks are applied to the RTCC (from internal or external source, with or without prescaler), RTCC keeps incrementing and just rolls over when the value "FFh" is reached. All increment pulses for RTCC are delayed by two instruction cycles. After writing to RTCC, for example, no increment takes place for the following two instruction cycles. This is independent if internal or external clock source is selected. If a prescaler is assigned to the RTCC, the output of the prescaler will be delayed by two cycles before RTCC is incremented. This is true for instructions that either write to or read-modify-write RTCC (e.g. MOVF RTCC, CLRF RTCC). For applications where RTCC needs to be tested for zero without affecting its count, use of MOVF RTCC, W instruction is recommended. Timing diagrams in Figure 4.2.2 show RTCC read, write and increment timing.

4.2.1 USING RTCC WITH EXTERNAL CLOCK

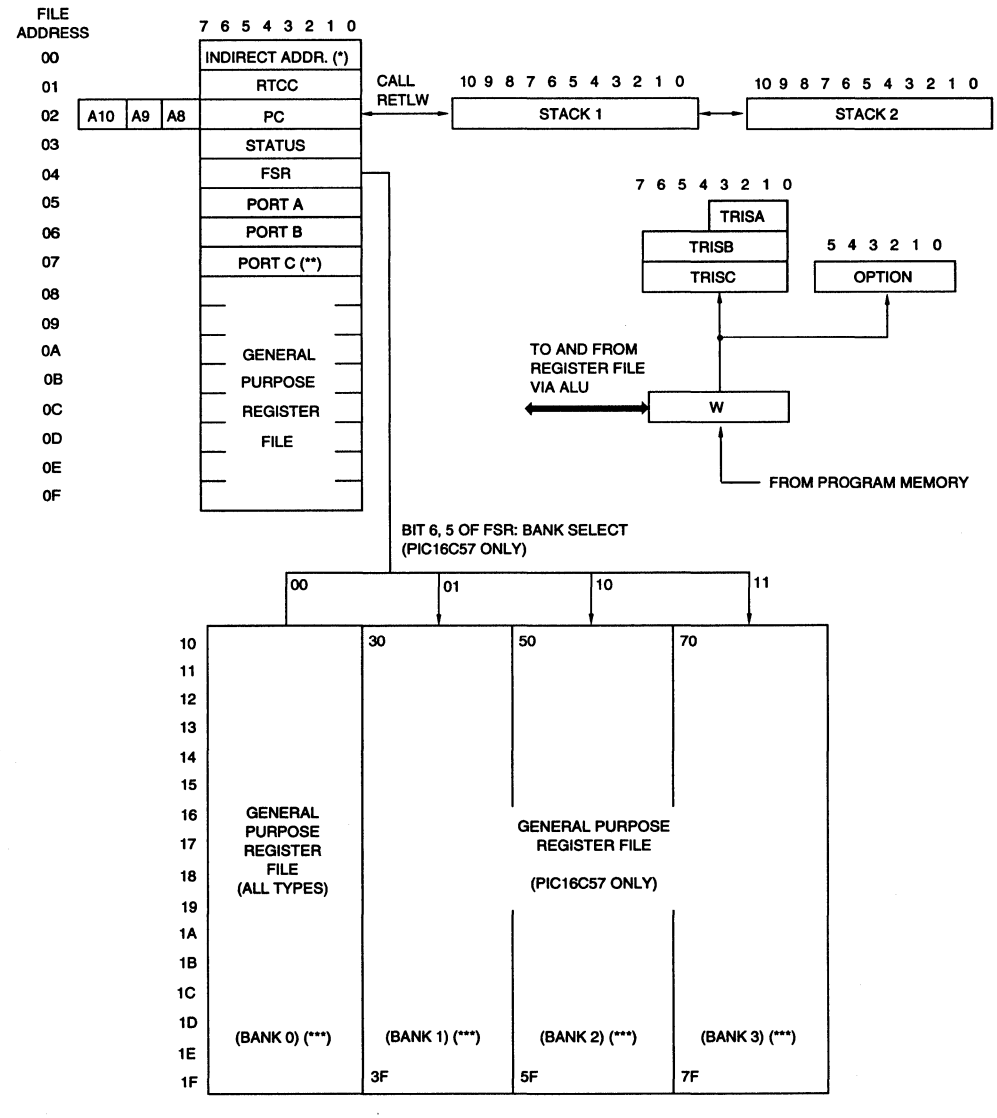
When external clock input is used for RTCC, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements. Also, there is some delay from the occurance of the external clock edge to the actual incrementing of RTCC. Referring to Figure 4.1.1, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where tosc = oscillator time period.

FIGURE 4.1.1 - RTCC BLOCK DIAGRAM (SIMPLIFIED)



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 are located in option register.
2. The prescaler is shared with Watchdog Timer (see Figure 9.0.1).

FIGURE 4.2.1 - PIC16C5X DATA MEMORY MAP



(*) NOT A PHYSICALLY IMPLEMENTED REGISTER. SEE SECTION 4.0 FOR DETAILS.

(**) FILE ADDRESS 7h IS A GENERAL PURPOSE REGISTER ON THE PIC16C54/C56

(***) BANK 0 IS AVAILABLE ON ALL MICROCONTROLLERS WHILE BANK 1 TO BANK 3 ARE ONLY AVAILABLE ON THE PIC16C57. (SEE SECTION 4.6 FOR DETAILS)

When no prescaler is used, PSOUT (Prescaler output, see Figure 4.1.1) is the same as RTCC clock input and therefore the requirements are:
TRTH = RTCC high time ≥ 2tosc + 20 ns
TRTL = RTCC low time ≥ 2tosc + 20 ns

When prescaler is used, the RTCC input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.
Then: PSOUT high time = PSOUT low time = N • TRT/2
where TRT = RTCC input period and N = prescale value (2, 4, ..., 256). The requirement is, therefore N • TRT/2 ≥ 2 tosc + 20 ns, or $T_{RT} \geq \frac{4\ tosc + 40\ ns}{N}$.

The user will notice that no requirement on RTCC high time or low time is specified. However, if the high time or low time on RTCC is too small then the pulse may not be detected, hence a minimum high or low time of 10ns is required. In summary, the RTCC input requirements are:
TRT = RTCC period ≥ (4 tosc + 40ns)/N
TRTH = RTCC high time ≥ 10ns
TRTL = RTCC low time ≥ 10ns

Delay from external clock edge: Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the RTCC is actually incremented. Referring to Figure 4.2.3, the reader can see that this delay is between 3 tosc and 7 tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±200 ns @ 20 MHz).

4.3 Program Counter

The program counter generates the addresses for up to 2048 x 12 on-chip EPROM cells containing the program instruction words (Figure 4.3.1).

Depending on the device type, the program counter and its associated two-level hardware stack is 9 - 11-bits wide.

TABLE 4.3.1 - PROGRAM COUNTER STACK WIDTH

Part #	PC width	Stack width
PIC16C54/PIC16C55	9-bit	9-bit
PIC16C56	10-bit	10-bit
PIC16C57	11-bit	11-bit

The program counter is set to all "1"s upon a RESET condition. During program execution it is auto incremented with each instruction unless the result of that instruction changes the PC itself:

a) "GOTO" instructions allow the direct loading of the lower nine program counter bits (PC<8:0>). In case of PIC16C56/PIC16C57, the upper two bits of PC (PC<10:9>) are loaded with page select bits PA1, PA0 (bits 6,5 status register). Thus, GOTO allows jump to any location on any page.
b) "CALL" instructions load the lower 8-bits of the PC directly, while the ninth bit is cleared to "0". The PC value, incremented by one, will be pushed into the stack. In case of PIC16C56, PIC16C57, the upper 2-bits of PC (PC<10:9>) are loaded with Page Select bits PA1, PA0 (bits 6,5 status register).

FIGURE 4.2.2A - RTCC TIMING: INT CLOCK/NO PRESCALE

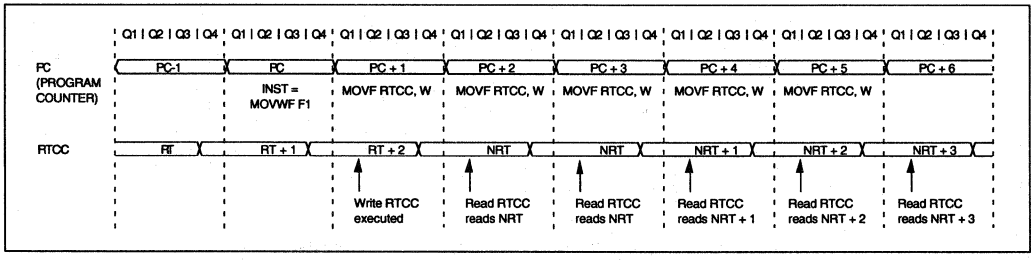
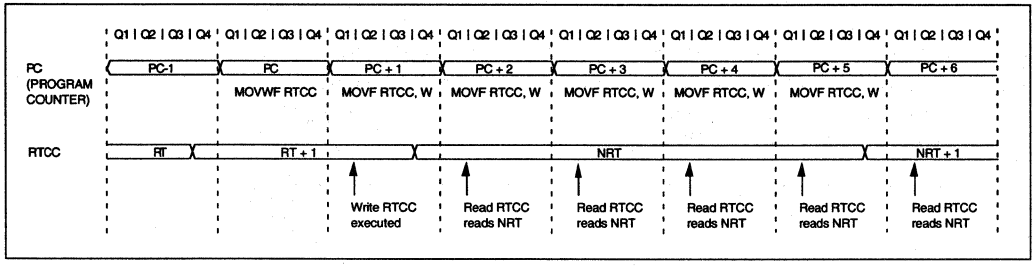


FIGURE 4.2.2B - RTCC TIMING: INT CLOCK/PRESCALE 1:2



c) "RETLW" instructions load the program counter with the top of stack contents.

d) If PC is the destination in any instruction (e.g. MOVWF PC, ADDWF PC, or BSF PC,5) then the computed 8-bit result will be loaded into the lower 8-bits of program counter. The ninth bit of PC will be cleared. In case of PIC16C56/PIC16C57, PC<10:9> will be loaded with Page Select bits PA1, PA0 (bits 6,5 in status register).

It should be noted that because bit 8 (ninth bit) of PC is cleared in CALL instruction or any instruction which writes to the PC (e.g. MOVWF PC), all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

MORE ON PROGRAM MEMORY PAGE SELECT (PIC16C56/PIC16C57 ONLY):

Incrementing the program counter when it is pointing to the last address of a selected memory page is also possible and will cause the program to continue in the next higher page. However, the page pre-select bits in f3 will not be changed, and the next "GOTO", "CALL", "ADDWF PC", "MOVWF PC" instruction will return to the previous page, unless the page pre-select bits have been updated under program control. For example, a "NOP" at location "1FF" (page 0) increments the PC to "200" (page 1). A "GOTO xxx" at "200" will return the program to address "xxx" on page "0" (assuming that the page preselect bits in file register STATUS are "0").

Upon a RESET condition, page 0 is pre-selected while the program counter addresses the last location in the last page. Thus, a "GOTO" instruction at this location will automatically cause the program to continue in page 0.

4.4 Stack

The PIC16C5X series employs a two-level hardware push/pop stack (Figure 4.3.1).

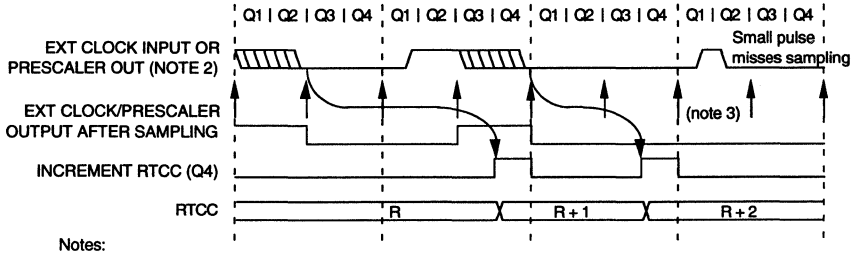
CALL instructions push the current program counter value, incremented by "1", into stack level 1. Stack level 1 is automatically pushed to level 2. If more than two subsequent "CALL"s are executed, only the most recent two return addresses are stored.

For the PIC16C56 and PIC16C57, the page preselect bits of STATUS will be loaded into the most significant bits of the program counter. The ninth bit is always cleared to "0" upon a CALL instruction. This means that subroutine entry addresses have to be located always within the lower half of a memory page (addresses 000-0FF, 200-2FF, 400-4FF, 600-6FF). However, as the stack has always the same width as the PC, subroutines can be called from anywhere in the program.

RETLW instructions load the contents of stack level 1 into the program counter while stack level 2 gets copied into level 1. If more than two subsequent "RETLW"s are executed, the stack will be filled with the address previously stored in level 2. For the PIC16C56 and PIC16C57, the return will be always to the page from where the subroutine was called, regardless of the current setting of the page pre-select bits in file register STATUS. Note that the W register will be loaded with the literal value specified in the RETLW instruction. This is particularly useful for the implementation of "data" tables within the program memory.

2

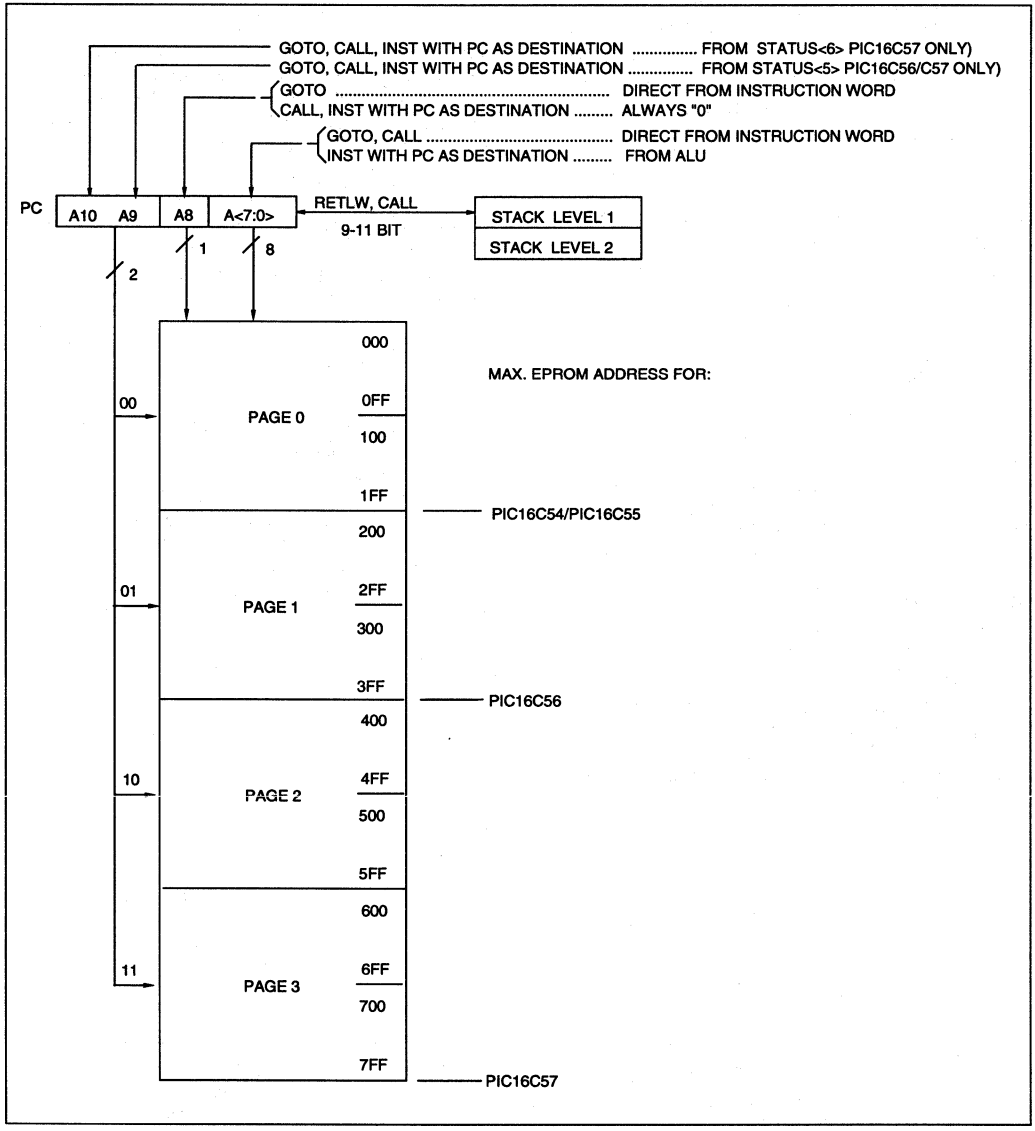
FIGURE 4.2.3 - RTCC TIMING WITH EXTERNAL CLOCK



Notes:

1. Delay from clock input change to RTCC increment is 3 tosc to 7 tosc. (Duration of Q = tosc). Therefore, the error in measuring the interval between two edges on RTCC input = ± 4 tosc max.
2. External clock if no prescaler selected, Prescaler output otherwise.
3. The arrows indicate the points in time where sampling occurs.

FIGURE 4.3.1 - PROGRAM MEMORY ORGANIZATION



4.5 STATUS Word Register

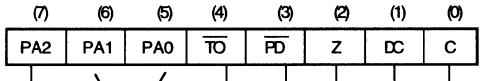
This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for larger program memories than 512 words (PIC16C56, PIC16C57).

The STATUS register can be destination for any instruction like any other register. However, the STATUS bits are set after the following write. Furthermore, $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with STATUS register as destination may be different than intended. For example, CLRF STATUS will clear all bits except for $\overline{TO}$ and $\overline{PD}$ and then set the Z bit and leave status register as 000UU100 (where U = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the STATUS registers because these instructions do not affect any STATUS bit.

For other instructions, affecting any STATUS bits, see Section "Instruction Set Summary" (Table 10.0.1).

FIGURE 4.5.1 - STATUS WORD REGISTER



RESET CONDITION:
PA2,PA1, PA0 cleared to '0'.
TO, PD are set or reset as shown in Table 4.5.2.1
Z, DC, C are unknown on power on reset and unchanged in any other reset.

CARRY/$\overline{BORROW}$ BIT:
For ADDWF and SUBWF instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
Note that a subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

DIGIT CARRY/$\overline{BORROW}$ BIT:
For ADDWF and SUBWF instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

ZERO BIT:
Set if the result of an arithmetic or logic operation is zero.

POWER DOWN BIT:
Set to "1" during power up or by a CLRWDT command. This bit is reset to "0" by a SLEEP instruction.

TIME-OUT BIT:
Set to "1" during power up and by the CLRWDT and SLEEP command. This bit is reset to "0" by a watchdog timer time out.

PIC16C54/C55 : Two general purpose read/write bits

PIC16C56 : BIT 5 ... Page preselect bit
0 = Page 0 (000 - 1FF)
1 = Page 1 (200 - 3FF)

BIT 6 ... General purpose read/write bit

PIC16C57 : Two page preselect bits
00 = Page 0 (000 - 1FF)
01 = Page 1 (200 - 3FF)
10 = Page 2 (400 - 5FF)
11 = Page 3 (600 - 7FF)

BIT 7: General purpose read/write bit (reserved for future use)

4.5.1 CARRY/BORROW AND DIGIT CARRY/ BORROW BITS:

The Carry bit (C) is a carry out in addition operation (ADDWF) and a borrow out in subtract operation (SUBWF).

It is also affected by RRF and RLF instructions. The following examples explain carry/borrow bit operation:

```
;SUBWF Example #1
;
clrf   0x20    ;f(20h)=0
movlw  1       ;wreg=1
subwf  0x20    ;f(20h)=f(20h)-wreg=0-1=FFh
               ;Carry=0: Result is negative
;
;SUBWF Example #2
movlw  0xFF    ;
movwf  0x20    ;f(20h)=FFh
clrw           ;wreg=0
subwf  0x20    ;f(20h)=f(20h)-wreg=FFh-
0=FFh
               ;Carry=1:Result is positive
;
```

The digit carry operates in the same way as the carry bit, i.e. it is a borrow in subtract operation.

4.5.2 TIME OUT AND POWER DOWN STATUS BITS ($\overline{TO}$, $\overline{PD}$)

The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be tested to determine if a RESET condition has been caused by a Watchdog Timer time-out, a power-up condition, or a wake-up from SLEEP by the Watchdog Wimer or $\overline{MCLR}$ pin.

These STATUS bits are only affected by events listed in Table 4.5.2.1.

TABLE 4.5.2.1 - EVENTS AFFECTING $\overline{PD}$/ $\overline{TO}$ STATUS BITS

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
WDT Timeout	0	X	No effect on PD
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Note: A WDT timeout will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{PD}$ bit. Table 4.5.2.2 reflects the status of $\overline{PD}$ and $\overline{TO}$ after the corresponding event.

TABLE 4.5.2.2 - $\overline{PD}$/$\overline{TO}$ STATUS AFTER RESET

$\overline{TO}$	$\overline{PD}$	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT time-out (not during SLEEP)
1	0	$\overline{MCLR}$ wake-up from SLEEP
1	1	Power-up
X	X	= Low pulse on $\overline{MCLR}$ input

Note: The $\overline{PD}$ and $\overline{TO}$ bit maintain their status (X) until an event of Table 4.5.2.1 occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{PD}$ and $\overline{TO}$ status bits.

4.5.3 PROGRAM PAGE PRESELECT (PIC16C56, PIC16C57 ONLY)

Bits 5-6 of the STATUS register are defined as PAGE address bits PA0<1:0>, and are used to preselect a program memory page. When executing a GOTO, CALL, or an instruction with PC as destination (e.g. MOVWF PC), PA<1:0> are loaded into bit A<10:9> of the program counter, selecting one of the available program memory pages. The direct address specified in the instruction is only valid within this particular memory page.

RETLW instructions do not change the page preselect bits.

Upon a RESET condition, PA<2:0> are cleared to "0"s.

4.6 File Select Register (FSR)

PIC16C54/C55/C56

Bits 0-4 select one of the 32 available file registers in the indirect addressing mode (that is, calling the INDF register in any of the file oriented instructions).

Bits 5-7 of the FSR are read-only and are always read as "one"s.

If no indirect addressing is used, the FSR can be used as a 5-bit wide general purpose register.

PIC16C57 ONLY

Bits 5 and 6 of the FSR select the current data memory bank (Figure 4.2.1).

The lower 16 bytes of each bank are physically identical and are always selected when bit 4 of the FSR (in case of indirect addressing) is "0", or bit 4 of the direct file register address of the currently executing instruction is "0" (e.g. MOVWF 08).

Only if bit 4 in the above mentioned cases is "1", bits 5 and 6 of the FSR select one of the four available register banks with 16 bytes each.

Bit 7 is read-only and is always read as "one."

5.0 I/O REGISTERS (PORTS)

The I/O registers can be written and read under program control like any other register of the register file. However, "read" instructions (e.g. MOVF PORTB,W) always read the I/O pins, regardless if a pin is defined as "input" or "output." Upon a RESET condition, all I/O ports are defined as "input" (= high impedance mode) as the I/O control registers (TRISA, TRISB, TRISC) are all set to "ones."

The execution of a "TRIS f" instruction with corresponding "zeros" in the W-register is necessary to define any of the I/O pins as output.

5.1 PORTA

4-bit I/O register. Low order 4-bits only are used (RA0 - RA3). Bits 4 - 7 are unimplemented and read as "zeros."

5.2 PORTB

8-bit I/O register.

5.3 PORTC

PIC16C55/C57: 8-bit I/O register.

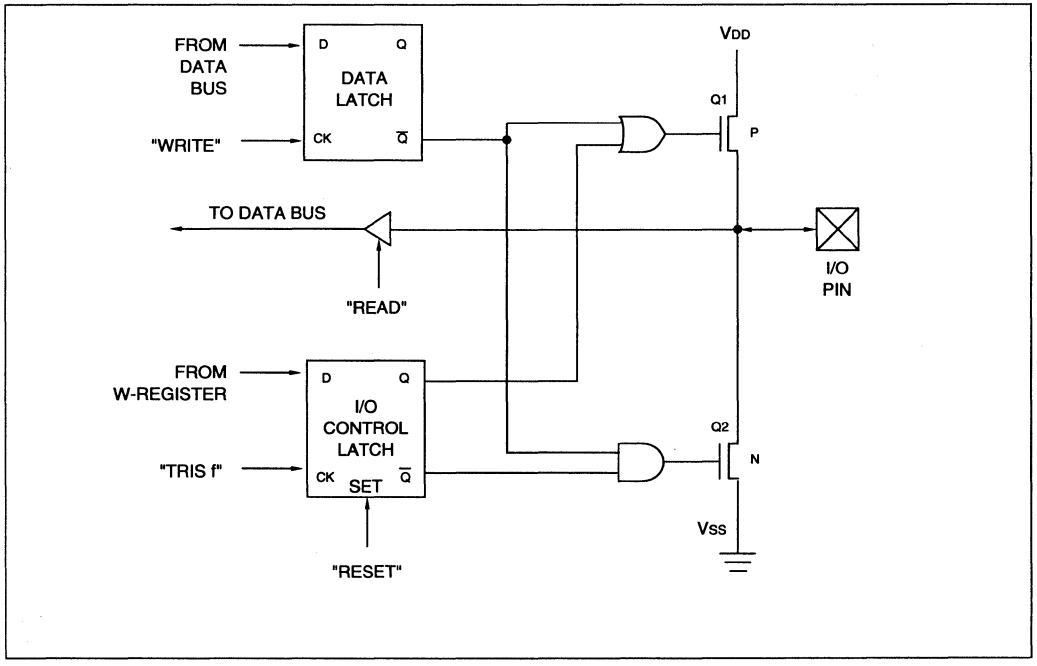
PIC16C54/C56: General purpose register.

5.4 I/O Interfacing

The equivalent circuit for an I/O port bit is shown in Figure 5.4.1. All ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g. MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be set to zero. For use as an input, the corresponding TRIS bit must be "one". Any I/O pin can be programmed individually as input or output.

2

FIGURE 5.4.1 - EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



5.5 I/O Programming Considerations

5.5.1 BIDIRECTIONAL I/O PORTS

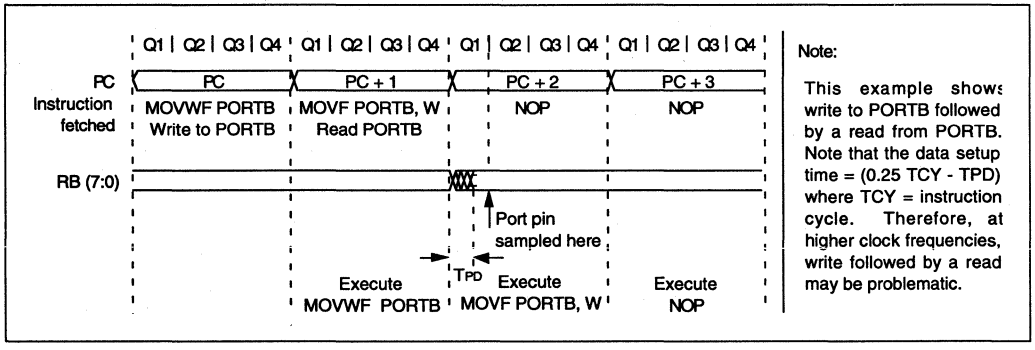
Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of PORTB will cause all eight bits of f6 to be read into the CPU. Then the BSF operation takes place on bit 5 and PORTB is re-output to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see Figure 5.5.2.1). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

FIGURE 5.5.2.1 - I/O PORT READ/WRITE TIMING



6.0 GENERAL PURPOSE REGISTERS

PIC16C54/C55/C56:

f08h - f1Fh: are general purpose register files.

PIC16C57 only:

f08h - f0Fh: are general purpose register files which are always selected, independent of bank select.
f10h - f1Fh: general purpose register files in memory bank 0.
f20h - f2Fh: physically identical to f00 - f0F.
f30h - f3Fh: general purpose register files in memory bank 1.
f40h - f4Fh: physically identical to f00 - f0F.
f50h - f5Fh: general purpose register files in memory bank 2.
f60h - f6Fh: physically identical to f00 - f0.
f70h - f7Fh: general purpose register files in memory bank 3.

7.0 SPECIAL PURPOSE REGISTERS

7.1 W Working Register

Holds second operand in two operand instructions and/or supports the internal data transfer.

7.2 TRISA I/O Control Register For PORTA

Only bits 0 - 3 are available. The corresponding I/O port (f5) is only 4-bit wide.

7.3 TRISB I/O Control Register For PORTB

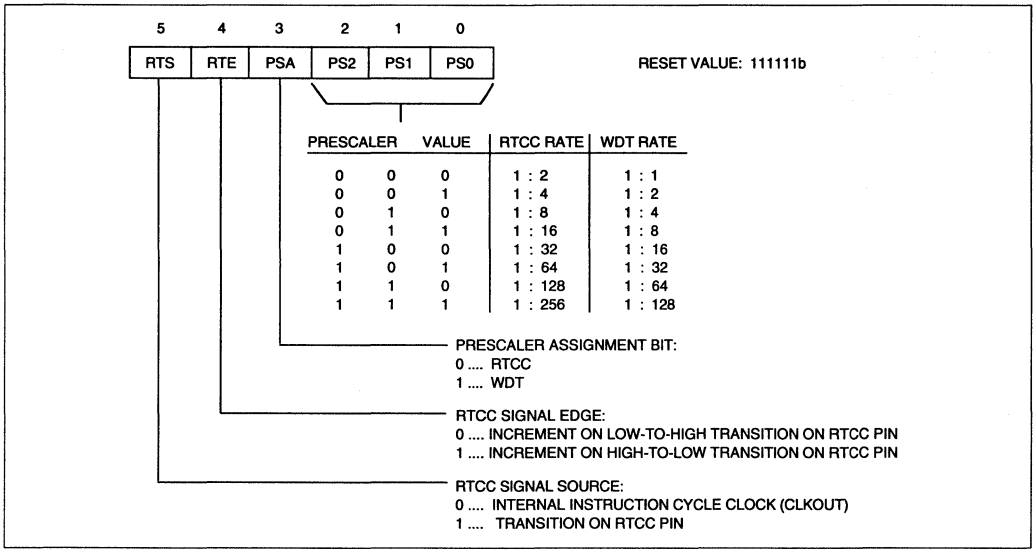
7.4 TRISC I/O Control Register For PORTC

The I/O control registers will be loaded with the content of the W register by executing of the TRIS f instruction. A "1" in the I/O control register puts the corresponding I/O pin into a high impedance mode. A "0" puts the contents of file register PORTA, PORTB, or PORTC, respectively, out on the selected I/O pins.
These registers are "write-only" and are set to all "ones" upon a RESET condition.

7.5 OPTION Prescaler/RTCC Option Register

Defines prescaler assignment (RTCC or WDT), prescaler value, signal source and signal edge for the RTCC. The OPTION register is "write-only" and is 6-bit wide. By executing the "OPTION" instruction, the contents of the "W" register will be transferred to the option register. Upon a RESET condition, the option register is set to all "ones."

FIGURE 7.5.1 - OPTION REGISTER



8.0 RESET CONDITION

A RESET condition can be caused by applying power to the chip (power-up), pulling the MCLR input "low", or by a Watchdog Timer timeout. The device will stay in RESET as long as the oscillator start-up timer (OST) is active or the MCLR input is "low."

The oscillator start-up timer is activated as soon as MCLR input is sensed to be high. This implies that in case of Power-On Reset with MCLR tied to VDD the OST starts from power-up. In case of WDT time-out, it will start at the end of the time-out (since MCLR is high). In case of MCLR reset, the OST will start when MCLR goes high. The nominal OST time-out period is 18ms. See Section 13.0 for detailed information on OST and power on reset.

During a RESET condition the state of the PIC16C5X is defined as :

- The oscillator is running, or will be started (power-up or wake-up from SLEEP).
- All I/O port pins (RA0 - RA3, RB0 - RB7, RC0 - RC7) are put into the high-impedance state by setting the "TRIS" registers to all "ones" (= input mode).
- The Program Counter is set to all "ones" (1FFh in PIC16C54/55, 3FFh in PIC16C56 and 7FFh in PIC16C57).
- The OPTION register is set to all "ones".
- The Watchdog Timer and its prescaler are cleared.
- The upper-three bits (page select bits) in the STATUS Register are cleared to "zero."
- "RC" devices only: The "CLKOUT" signal on the OSC2 pin is held at a"low" level.

9.0 PRESCALER

An 8-bit counter is available as a prescaler for the RTCC, or as a post-scaler for the Watchdog Timer, respectively (Figure 9.0.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the RTCC and the Watchdog Timer. Thus, a prescaler assignment for the RTCC means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS0-PS2 bits in the OPTION register determine the prescaler assignment and pre-scale ratio.

When assigned to the RTCC, all instructions writing to the RTCC (e.g. CLRF RTCC, MOVWF RTCC, BSF RTCC,x ....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer.

9.1 Switching Prescaler Assignment

CHANGING PRESCALER FROM RTCC TO WDT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence must be executed when changing the prescaler assignment from RTCC to WDT:

```
1. MOVLW  B'xx0x0xxx'  ; Select internal clock and select new
2. OPTION              ; prescaler value. If new prescale value
                       ; is = '000' or '001', then select any other
                       ; prescale value temporarily.
3. CLRF 1              ; Clear RTCC and prescaler.
4. MOVLW  B'xxxx1xxx'  ; Select WDT, do not change prescale
                       ; value.
5. OPTION              ;
6. CLRWDT;             Clears WDT and prescaler.
7. MOVLW  B'xxxx1xxx'  ; Select new prescale value.
8. OPTION              ;
```

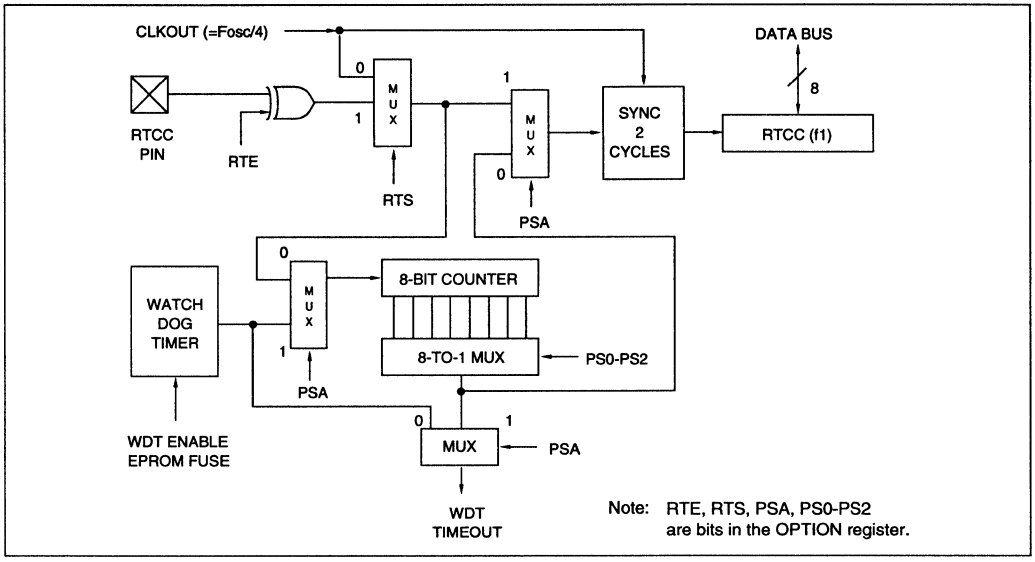
Steps 1 and 2 are only required if an external RTCC source is used. Steps 7 and 8 are necessary only if the desired prescale value is '000' or '001'.

CHANGING PRESCALER FROM WDT TO RTCC

To change prescaler from WDT to RTCC use the following sequence:

```
1. CLRWDT;             Clear WDT and prescaler
2. MOVLWB'xxxx0xxx'    ; Select RTCC, new prescale value
                       ; and clock source
3. OPTION              ;
```

FIGURE 9.0.1 - BLOCK DIAGRAM RTCC/WDT PRESCALER



10.0 BASIC INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 10.0.1 lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC16C5X file registers is to be utilized by the instruction. For the PIC16C57, bits 5 and 6 in the FSR determine the selected register bank.

The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an 8- or 9-bit constant or literal value.

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Notes to Table 10.0.1

Note 1: The ninth bit of the program counter will be forced to a "zero" by any instruction that writes to the PC except for GOTO (e.g. CALL, MOVWF PC etc.). See Section 4.3 on page 8 for details.

Note 2: When an I/O register is modified as a function of itself (e.g. MOVF PORTB,1), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as output and is driven low by an external device, the data will be written back with a '0'.

Note 3: The instruction "TRIS f" , where f = 5,6, or 7 causes the contents of the W register to be written to the tristate latches of the specified file (port). A "one" forces the pin to a high impedance state and disables the output buffers.

Note 4: If this instruction is executed on file register RTCC (and, where applicable, d=1), the prescaler will be cleared if assigned to the RTCC.

TABLE 10.0.1 - INSTRUCTION SET SUMMARY

BYTE -ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4 - 0)
OPCODE	d	f(FILE #)

d = 0 for destination W
d = 1 for destination f

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0001 11df ffff 1Cf	Add W and f	**ADDWF**	f, d	W + f → d	C,DC,Z	1,2,4
0001 01df ffff 14f	AND W and f	**ANDWF**	f, d	W & f → d	Z	2,4
0000 011f ffff 06f	Clear f	**CLRF**	f	0 → f	Z	4
0000 0100 0000 040	Clear W	**CLRW**	-	0 → W	Z	
0010 01df ffff 24f	Complement f	**COMF**	f, d	$\bar{f}$ → d	Z	2,4
0000 11df ffff 0Cf	Decrement f	**DECF**	f, d	f -1 → d	Z	2,4
0010 11df ffff 2Cf	Decrement f,Skip if Zero	**DECFSZ**	f, d	f - 1 → d, skip if zero	None	2,4
0010 10df ffff 28f	Increment f	**INCF**	f, d	f + 1 → d	Z	2,4
0011 11df ffff 3Cf	Increment f,Skip if zero	**INCFSZ**	f, d	f + 1 → d, skip if zero	None	2,4
0001 00df ffff 10f	Inclusive OR W and f	**IORWF**	f, d	W v f → d	Z	2,4
0010 00df ffff 20f	Move f	**MOVF**	f, d	f → d	Z	2,4
0000 001f ffff 02f	Move W to f	**MOVWF**	f	W → f	None	1,4
0000 0000 0000 000	No Operation	**NOP**	-	-	None	
0011 01df ffff 34f	Rotate left f	**RLF**	f, d	f(n) → d(n+1), C → d(0), f(7) → C	C	2,4
0011 00df ffff 30f	Rotate right f	**RRF**	f, d	f(n) → d(n-1), C → d(7), f(0) → C	C	2,4
0000 10df ffff 08f	Subtract W from f	**SUBWF**	f, d	f - W → d [f + $\overline{W}$ + 1 → d]	C,DC,Z	1,2,4
0011 10df ffff 38f	Swap halves f	**SWAPF**	f, d	f(0-3) ↔ f(4-7) → d	None	2,4
0001 10df ffff 18f	Exclusive OR W and f	**XORWF**	f, d	W ⊕ f → d	Z	2,4

BIT- ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4 - 0)
OPCODE	b(BIT #)	f(FILE #)

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0100 bbbf ffff 4bf	Bit Clear f	**BCF**	f, b	0 → f(b)	None	2,4
0101 bbbf ffff 5bf	Bit Set f	**BSF**	f, b	1 → f(b)	None	2,4
0110 bbbf ffff 6bf	Bit Test f,Skip if Clear	**BTFSC**	f, b	Test bit (b) in file (f): Skip if clear	None	
0111 bbbf ffff 7bf	Bit Test f, Skip if Set	**BTFSS**	f, b	Test bit (b) in file (f): Skip if set	None	

LITERAL AND CONTROL OPERATIONS

(11-8)	(7 - 0)
OPCODE	k (LITERAL)

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
1110 kkkk kkkk Ekk	AND Literal and W	**ANDLW**	k	k & W→ W	Z	
1001 kkkk kkkk 9kk	Call subroutine	**CALL**	k	PC + 1 → Stack, k → PC	None	1
0000 0000 0100 004	Clear Watchdog timer	**CLRWDT**	-	0 → WDT (and prescaler, if assigned)	TO, PD	
101k kkkk kkkk Akk	Go To address (k is 9 bit)	**GOTO**	k	k → PC (9 bits)	None	
1101 kkkk kkkk Dkk	Incl. OR Literal and W	**IORLW**	k	k v W → W	Z	
1100 kkkk kkkk Ckk	Move Literal to W	**MOVLW**	k	k → W	None	
0000 0000 0010 002	Load OPTION register	**OPTION**	-	W → OPTION register	None	
1000 kkkk kkkk 8kk	Return,place Literal in W	**RETLW**	k	k → W, Stack → PC	None	
0000 0000 0011 003	Go into standby mode	**SLEEP**	-	0 → WDT, stop oscillator	TO, PD	
0000 0000 0fff 00f	Tristate port f	**TRIS**	f	W→ I/O control register f	None	3
1111 kkkk kkkk Fkk	Excl. OR Literal and W	**XORLW**	k	k ⊕ W → W	Z	

Notes: See previous page

10.1 Instruction Description

ADDWF ADD W to f

Syntax: ADDWF f,d

Encoding:	0001	11df	ffff

Words: 1

Cycles: 1

Operation: (W + f) → d

Status bits: C, DC, Z

Description: Add the contents of the W register to register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

ANDLW AND Literal and W

Syntax: ANDLW k

Encoding:	1110	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .AND. k) → W

Status bits: Z

Description: The contents of W register are AND'ed with the 8-bit literal "k". The result is placed in the W register.

ANDWF AND W with f

Syntax: ANDWF f,d

Encoding:	0001	01df	ffff

Words: 1

Cycles: 1

Operation: (W .AND. f) → d

Status bits: Z

Description: AND the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

BCF Bit Clear f

Syntax: BCF f,b

Encoding:	0100	bbbf	ffff

Words: 1

Cycles: 1

Operation: 0 → f(b)

Status bits: None

Description: Bit "b" in register "f" is reset to 0.

BSF Bit Set f

Syntax: BSF f,b

Encoding:	0101	bbbf	ffff

Words: 1

Cycles: 1

Operation: 1 → f(b)

Status bits: None

Description: Bit "b" in register "f" is set to 1.

BTFSC Bit Test, skip if Clear

Syntax: BTFSC f,b

Encoding:	0110	bbbf	ffff

Words: 1

Cycles: 1(2)

Operation: skip if f(b) = 0

Status bits: None

Description: If bit "b" in register "f" is "0" then the next instruction is skipped.

If bit "b" is "0", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a two-cycle instruction.

BTFSS Bit Test, skip if Set

Syntax: BTFSS f,b

Encoding:	0111	bbbf	ffff

Words: 1

Cycles: 1 (2)

Operation: skip if f(b) = 1

Status bits: None

Description: If bit "b" in register "f" is "1" then the next instruction is skipped.

If bit "b" is "1", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a two-cycle instruction.

CALL Subroutine Call

Syntax: CALL k

Encoding:	1001	kkkk	kkkk

Words: 1

Cycles: 2

Operation: PC + 1 → TOS; k → PC<7:0>, '0' → PC<8>, PA2, PA1, PA0 → PC<11:9>;

Status bits: None

Description: Subroutine call. First, return address (PC + 1) is pushed into the stack. The eight bit value is loaded into PC bits <7:0>. PC bit 8 is cleared. PA<2:0> bits are loaded into PC <11:9>. CALL is a two cycle instruction.

CLRF Clear f

Syntax: CLRF f

Encoding:	0000	011f	ffff

Words: 1

Cycles: 1

Operation: 00h → f

Status bits: Z

Description: The contents of register "f" are set to 0.

CLRW Clear W Register

Syntax: CLRW

Encoding:	0000	0100	0000

Words: 1

Cycles: 1

Operation: 00h →W

Status bits: Z

Description: W registered is cleared. Zero bit (Z) is set.

CLRWDT Clear Watchdog Timer

Syntax: CLRWDT

Encoding:	0000	0000	0100

Words: 1

Cycles: 1

Operation: 00h →WDT, 0 → WDT prescaler,

Status bits: 1 → $\overline{TO}$, 1 → $\overline{PD}$

Description: CLRWDT instruction resets the Watchdog Timer.It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

COMF Complement f

Syntax: COMF f,d

Encoding:	0010	01df	ffff

Words: 1

Cycles: 1

Operation: $\overline{f}$ → d

Status bits: Z

Description: The contents of register "f" are complemented. If "d" is 0 the result is stored in W. If "d" is 1 the result is stored back in register "f".

DECF Decrement f

Syntax: DECF f,d

Encoding:	0000	11df	ffff

Words: 1

Cycles: 1

Operation: (f-1) → d

Status bits: Z

Description: Decrement register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

DECFSZ Decrement f, skip if 0

Syntax: DECFSZ f,d

Encoding:	0010	11df	ffff

Words: 1

Cycles: 1 (2)

Operation: (f - 1) → d; skip if result = 0

Status bits: None

Description: The contents of register "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f". If the result is 0 the next instruction is skipped.

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.

GOTO Unconditional Branch

Syntax: GOTO k

Encoding:	101k	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → PC<8:0>, PA2, PA1, PA0

→ PC<11:9>;

Status bits: None

Description: The low order nine bits come from the immediate value. The upper-three bits are loaded from the PA <2:0> bits in the STATUS register.

INCF Increment f

Syntax: INCF f,d

Encoding:	0010	10df	ffff

Words: 1

Cycles: 1

Operation: (f + 1) → d

Status bits: Z

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

INCFSZ Increment f, skip if 0

Syntax: INCFSZ f,d

Encoding:

0011	11df	ffff

Words: 1

Cycles: 1 (2)

Operation: (f + 1) → d, skip if result = 0

Status bits: None

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f". If the result is 0 the next instruction is skipped.

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.

IORLW Inclusive OR Literal with W

Syntax: IORLW k

Encoding:

1101	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .OR. k) → W

Status bits: Z

Description: The contents of the W register are OR'ed with the 8-bit literal "k". The result is placed in the W register.

IORWF Inclusive OR W with f

Syntax: IORWF f,d

Encoding:

0001	00df	ffff

Words: 1

Cycles: 1

Operation: (W .OR. f) → d

Status bits: Z

Description: Inclusive OR the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

MOVF Move f

Syntax: MOVF f,d

Encoding:

0010	00df	ffff

Words: 1

Cycles: 1

Operation: (f) → d

Status bits: Z

Description: The contents of register "f" are moved. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

MOVLW Move Literal to W

Syntax: MOVLW k

Encoding:

1100	kkkk	kkkk

Words: 1

Cycles: 1

Operation: k → W

Status bits: None

Description: The 8-bit literal "k" is loaded into W register.

MOVWF Move W to f

Syntax: MOVWF f

Encoding:

0000	001f	ffff

Words: 1

Cycles: 1

Operation: W → f

Status bits: None

Description: Move data from W register to register "f".

NOP No Operation

Syntax: NOP

Encoding:

0000	0000	0000

Words: 1

Cycles: 1

Operation: No operation

Status bits: None

Description: No operation

OPTION Load Option Register

Syntax: OPTION

Encoding:

0000	0000	0010

Words: 1

Cycles: 1

Operation: W → OPTION;

Status bits: None

Description: The contents of the W register is loaded in the OPTION register.

RETLW Return Literal to W

Syntax: RETLW k

Encoding:	1000	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → W; TOS → PC;

Status bits: None

Description: The W register is loaded with the eight bit literal "k". The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RLF Rotate Left f through Carry

Syntax: RLF f,d

Encoding:	0011	01df	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n+1>, f<7> → C, C → d<0>;

Status bits: C

Description: The contents of register "f" are rotated one bit to the left through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is stored back in register "f".

RRF Rotate Right f through Carry

Syntax: RRF f,d

Encoding:	0011	00df	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n-1>, f<0> → C, C → d<7>;

Status bits: C

Description: The contents of register "f" are rotated one bit to the right through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

SLEEP

Syntax: SLEEP

Encoding:	0000	0000	0011

Words: 1

Cycles: 1

Operation: 0 → PD, 1 → TO;
00h → WDT, 0 → WDT prescaler;

Status bits: $\overline{TO}$, $\overline{PD}$

Description: The power-down status bit ($\overline{PD}$) is cleared. Time-out status bit ($\overline{TO}$) is set. Watchdog Timer and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP mode for more details.

SUBWF Subtract W from f

Syntax: SUBWF f,d

Encoding:	0000	10df	ffff

Words: 1

Cycles: 1

Operation: (f-W) → d

Status bits: C, DC, Z

```
;SUBWF Example #1
;
clrf   0x20   ;f(20h)=0
movlw  1      ;wreg=1
subwf  0x20   ;f(20h)=f(20h)-wreg=0-1=FFh
              ;Carry=0; Result is negative
;
;SUBWF Example #2
;
movlw  0xFF   ;
movwf  0x20   ;f(20h)=FFh
clrw          ;wreg=0
subwf  0x20   ;f(20h)=f(20h)-wreg=FFh-
0=FFh
              ;Carry=1:Result is positive
;
```

Description: Subtract (2's complement method) the W register from register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

SWAPF Swap f

Syntax: SWAPF f,d

Encoding:	0011	10df	ffff

Words: 1

Cycles: 1

Operation: f<0:3> → d<4:7>, f<4:7> → d<0:3>;

Status bits: None

Description: The upper and lower nibbles of register "f" are exchanged. If "d" is 0 the result is placed in W register. If "d" is 1 the result is placed in register "f".

TRIS Load TRIS Register

Syntax: TRIS f

Encoding:	0000	0000	0fff

Words: 1

Cycles: 1

Operation: W → TRIS register f;

Status bits: None

Description: TRIS register f (f = 5, 6 or 7) is loaded with the contents of the W register.

XORLW Exclusive OR literal with W

Syntax: XORLW k

Encoding:	1111	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .XOR. k) → W

Status bits: Z

Description: The contents of the W register are XOR'ed with the 8-bit literal "k". The result is placed in the W register.

XORWF Exclusive OR W with f

Syntax: XORWF f,d

Encoding:	0001	10df	ffff

Words: 1

Cycles: 1

Operation: (W .XOR. f) → d

Status bits: Z

Description: Exclusive OR the contents of the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

11.0 WATCHDOG TIMER (WDT)

The Watchdog Timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1/OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by programming a "zero" into a special EPROM fuse which is not part of the normal program memory EPROM.

11.1 WDT Period

The WDT has a nominal time-out period of 18ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.5 seconds can be realized.

The "CLRWDT" and "SLEEP" instructions clear the WDT and the prescaler count, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit, $\overline{TO}$, in the STATUS register, will be cleared upon a Watchdog Timer timeout.

The WDT period is a function of the supply voltage, operating temperature, and will also vary from unit to unit due to variations in the manufacturing process. Please refer to the graphs in Section 18.0 and DC specs for more details.

11.2 WDT Programming Considerations

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

12.0 OSCILLATOR CIRCUITS

2

12.1 Oscillator Types

The PIC16C5X series is available with four different oscillator options. On windowed devices, a particular oscillator circuit can be selected by programming the configuration EPROM accordingly. On OTP and QTP devices, the oscillator configuration is programmed by the factory and the parts are tested only to the according specifications.

12.2 Crystal Oscillator

The PIC16C5X-XT, -HS, or LP needs a crystal or ceramic resonator connected to the OSC1 and OSC2 pins to establish oscillation (Figure 12.2.1). XT = Standard crystal oscillator, HS = High speed crystal oscillator. The series resistor RS may be required for the "HS" oscillator, especially at lower than 20 MHz oscillation frequency. It may also be required in XT mode with AT strip-cut type crystals to avoid overdriving.

12.3 RC Oscillator

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation to due tolerance of external R and C components used. Figure 12.3.1 shows how the R/C combination is connected to the PIC16C5X. For Rext values below 2.2 kOhm, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 5 kOhm and 100 kOhm.

Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

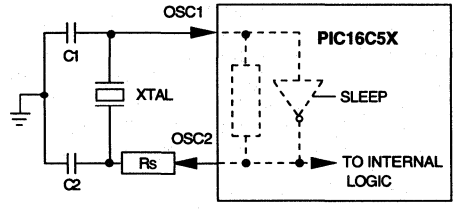
See the table in Section 18.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characteristics in Section 18.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 2.2.1 for timing).

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

FIGURE 12.2.1 - CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP TYPES ONLY)



Rs may be required in HS and XT modes for AT strip-cut crystals to avoid overdriving. See Tables 12.2.1 and 12.2.2 for recommended values of C1, C2 per oscillator type and frequency.

TABLE 12.2.1 - CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	150 - 330 pF
	2.0 MHz	20 - 330 pF
	4.0 MHz	20 - 330 pF
HS	8.0 MHz	20 - 200 pF

FIGURE 12.2.2 - EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP TYPES ONLY)

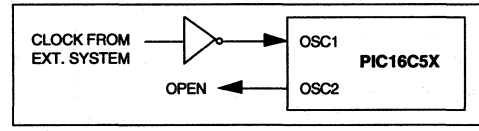


TABLE 12.2.2 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	15 pF	15 pF
XT	100 KHz	15 - 30 pF	200 - 300 pF
	200 KHz	15 - 30 pF	100 - 200 pF
	455 KHz	15 - 30 pF	15 - 100 pF
	1 MHz	15 - 30 pF	15 - 30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

FIGURE 12.3.1 - RC OSCILLATOR (RC TYPE ONLY)

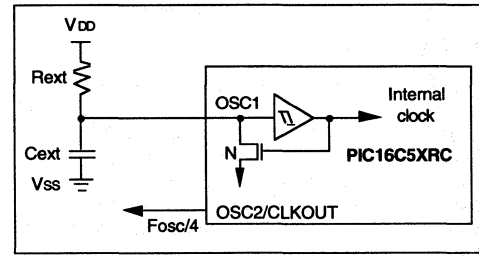
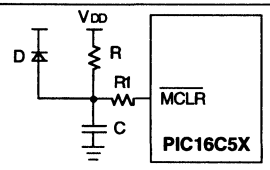


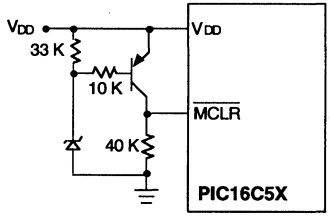
FIGURE 13.1.1 - EXTERNAL POWER ON RESET CIRCUIT



Notes:

1. External power on reset circuit is required only if VDD power-up slope is too slow or if a low frequency crystal oscillator is being used that need a long start-up time. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40 KΩ must be observed to make sure that voltage drop across R does not exceed 0.2 V (max leakage current spec on MCLR pin is 5 μA). A larger voltage drop will degrade VIH level on MCLR pin.
3. R1= 100Ω to 1KΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to ESD or EOS.

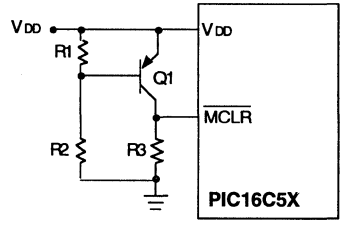
FIGURE 13.1.2 - BROWN OUT PROTECTION CIRCUIT



Notes:

1. This circuit will activate reset when VDD goes below (VZ + 0.7 V) where VZ = Zener voltage.

FIGURE 13.1.3 - BROWN OUT PROTECTION CIRCUIT



Notes:

1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7\ V.$$

13.0 OSCILLATOR START-UP TIMER (OST)

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. An on-chip oscillator start-up timer is provided which keeps the device in a RESET condition for approximately 18ms after the voltage on the MCLR pin has reached a logic high (VIHMC) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The OST will also be triggered upon a Watchdog Timer timeout. This is particularly important for applications using the WDT to awake the PIC16C5X from SLEEP mode automatically.

The OST is not adequate for low frequency crystals which require much longer than 18ms to start-up and stabilize.

13.1 Power-On Reset (POR)

The PIC16C5X incorporates an on chip Power-On Reset (POR) circuitry which provides internal chip reset for most power-up situations. To use this feature the user merely needs to tie MCLR pin to VDD. A simplified block diagram of the on-chip power on reset circuit is shown in Figure 13.1.4. The Power-On Reset circuit and the oscillator start-up timer circuit are closely related. On power-up the reset latch is set and the start-up timer (see Figure 13.1.4) is reset. The start-up timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18ms, it will reset the reset-latch and thus end the on-chip reset signal.

Figures 13.1.5 and 13.1.6 are two power-up situations with relatively fast rise time on VDD. In Figure 13.1.5, VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset tOST ms after MCLR goes high. In Figure 13.1.6, the on chip Power-On Reset feature is being utilized (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper reset. Figure 13.1.7 depicts a potentially problematic situation where VDD rises too slowly. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly.

To summarize, the on-chip Power-On Reset is guaranteed to work if the rate of rise of VDD is no slower than 0.05 V/ms. It is also necessary that the VDD starts from 0V. The on-chip Power-On Reset is also not adequate for low frequency crystals which require much longer than 18ms to start-up and stabilize. For such situations, we recommend that external RC circuits are used for longer Power-On Reset.

FIGURE 13.1.4 - SIMPLIFIED POWER ON RESET BLOCK DIAGRAM

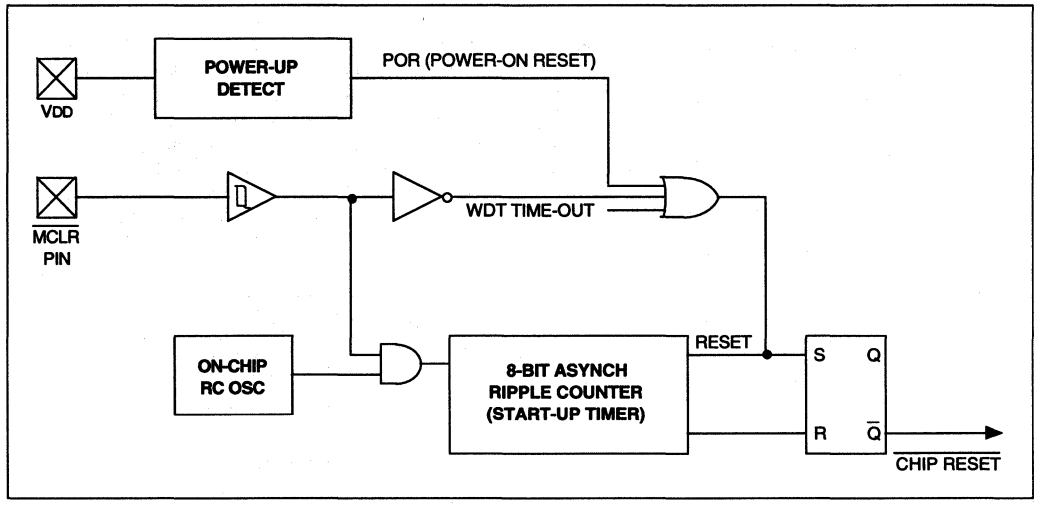
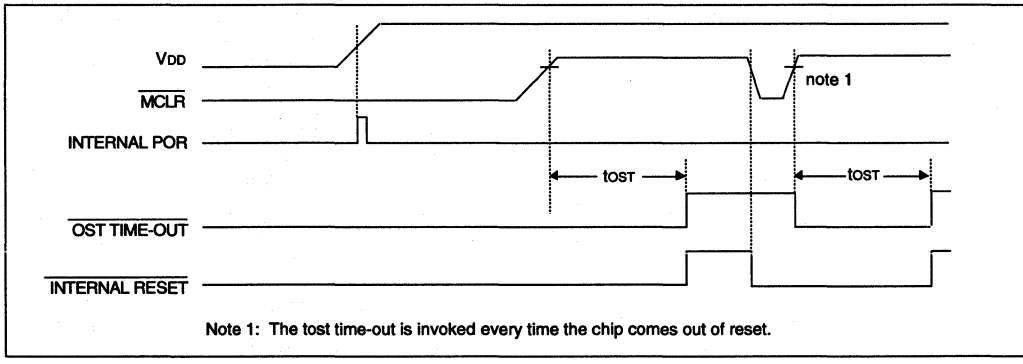


FIGURE 13.1.5 - USING EXTERNAL RESET INPUT



Note 1: The tost time-out is invoked every time the chip comes out of reset.

FIGURE 13.1.6 - USING ON-CHIP POR (FAST VDD RISE TIME)

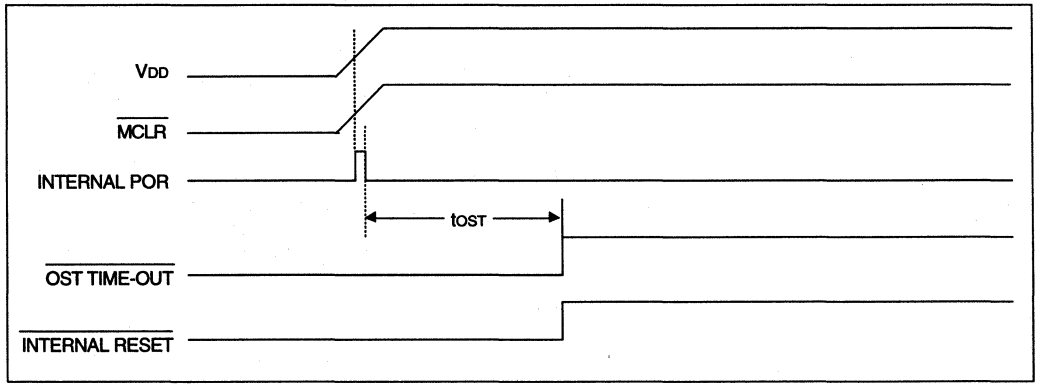
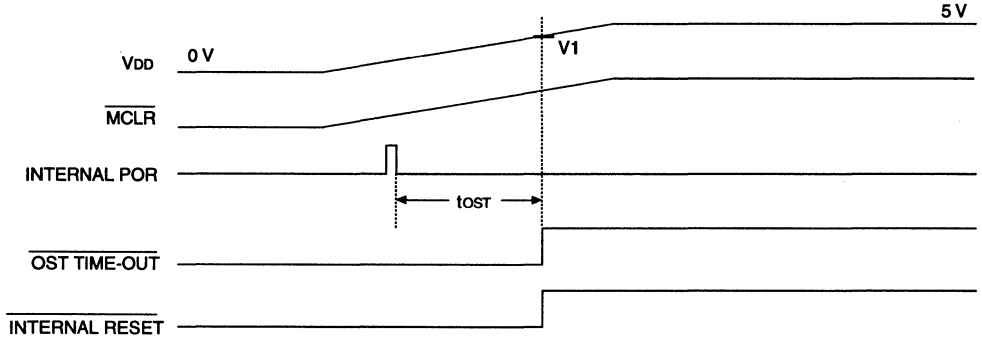


FIGURE 13.1.7 - USING ON-CHIP POR (SLOW VDD RISE TIME)



When VDD rises slowly, the internal time-out period expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1≥ VDDMIN.

14.0 POWER DOWN MODE (SLEEP)

The power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the bit $\overline{PD}$ in the STATUS register is cleared, the $\overline{TO}$ bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or Vss, with no external circuitry drawing current from the I/O pin. I/O pins that are in the High-Z mode should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC input should also be at VDD or Vss for lowest current consumption.

The $\overline{MCLR}$ pin must be at VIHMC.

14.1 Wake-Up

The device can be awakened by a Watchdog Timer timeout (if it is enabled) or an externally applied "low" pulse at the $\overline{MCLR}$ pin. In both cases the PIC16C5X will stay in RESET mode for one oscillator start-up timer period (triggered from rising edge on $\overline{MCLR}$ or WDT timeout) before normal program execution resumes.

The $\overline{PD}$ bit in the STATUS register, which is set to one during power-on , but cleared by the "SLEEP" command, can be used to determine if the processor was powered up or awakened from the power-down mode (Table 4.5.1.2). The $\overline{TO}$ bit in the STATUS register can be used to determine if the "wake up" was caused by an external $\overline{MCLR}$ signal or a Watchdog Timer timeout.

NOTE: Some applications may require external R/C networks on the $\overline{MCLR}$ pin in order to allow for oscillator startup times longer than one OST period. In this case, a WDT wake up from power-down mode is not recommended, because a RESET generated by a WDT time out does not discharge the external capacitor, and the PIC16C5X will be in RESET only for the Oscillator Start-up Timer period.

15.0 CONFIGURATION FUSES

The configuration EPROM consists of four EPROM fuses which are not part of the normal EPROM for program storage.

Two are for the selection of the oscillator type, one is the Watchdog Timer enable fuse, and one is the code protection fuse.

OTP or QTP devices have the oscillator configuration programmed by the factory and the parts are tested accordingly. The packages are marked with the suffixes "XT", "RC", "HS" or "LP" following the part number to identify the oscillator type and operating range.

15.1 Customer ID Code

The PIC16C5X series has 16 special EPROM bits which are not part of the normal program memory. These bits are available to the user to store an Identifier (ID) code, checksum, or other informative data. They cannot be accessed during normal program execution.

15.2 Code Protection

The program code written into the EPROM can be protected by programming the code protection fuse with "0".

When code protected, the contents of the program EPROM cannot be read out in a way that the program code can be reconstructed. In addition, all memory locations starting at 040h and above are protected against programming.

It is still possible to program locations 000h - 03Fh, the ID locations and the configuration fuses.

Note that the configuration fuses and the ID bits can still be read, even if the code protection logic is active.

15.2.1 Verifying a Code-protected Part

When code protected verifying any program memory location will read a scrambled output which looks like "00000000XXXX" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

a. First, program and verify a good device without code protecting it.
b. Next, blow its code protection fuse and then load its contents in a file.
c. Verify any code-protected Part against this file.

16.0 ELECTRICAL CHARACTERISTICS

16.1 Absolute Maximum Ratings*

Ambient temperature under bias ..... -55°C to +125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss
(except VDD and MCLR) ..... -0.6V to VDD +0.6 V
Voltage on VDD with respect to Vss ..... 0 to +7.5 V
Voltage on MCLR with respect to Vss
(Note 2) ..... 0 to +14 V
Total power Dissipation (Note 1) ..... 800 mW
Max. Current out of Vss pin ..... 150 mA
Max. Current into VDD pin ..... 50 mA
Max. Current into an input pin ..... ±500 µA
Input clamp current, IIK (VI<0 or VI>VDD) ..... ±20 mA
Output clamp current, IOK (V0<0 or V0>VDD) . ±20 mA
Max. Output Current sinked by any I/O pin ..... 25 mA
Max. Output Current sourced by any I/O pin .... 20 mA
Max. Output Current sourced by a single
I/O port (Port A, B, or C) ..... 40 mA
Max. Output Current sinked by a single
I/O port (Port A, B, or C) 50mA

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
$Pdis = VDD \times \{IDD - \sum Ioh\} + \sum\{(VDD-Voh) \times Ioh\} + \sum(Vol \times Iol)$

2. Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.

2

TABLE 16.2 - PIN DESCRIPTIONS

Name	Function	Description
RA0 - RA3	I/O PORTA	Four input/output lines.
RB0 - RB7	I/O PORTB	Eight input/output lines.
RC0 - RC7	I/O PORTC	Eight input/output lines, (PIC16C55/C57 only).
RTCC	Real Time Clock/Counter	Schmitt Trigger Input. Clock input to RTCC register. Must be tied to Vss or VDD if not in use to avoid unintended entering of test modes and to reduce current consumption.
MCLR	Master Clear	Schmitt Trigger Input. A "Low" voltage on this input generates a RESET condition for the PIC16C5X microcontroller. A rising voltage triggers the on-chip oscillator start-up timer which keeps the chip in RESET mode for about 18ms. This input must be tied directly, or via a pull-up resistor, to VDD.
OSC1	Oscillator (input)	"XT", "HS" and "LP" devices: Input terminal for crystal, ceramic resonator, or external clock generator. "RC" devices : Driver terminal for external RC combination to establish oscillation.
OSC2/CLKOUT	Oscillator (output)	For "XT", "HS" and "LP" devices: Output terminal for crystal and ceramic resonator. Do not connect any other load to this output. Leave open if external clock generator is used. For "RC" devices : A "CLKOUT" signal with a frequency of 1/4 Fosc1 is put out on this pin.
VDD	Power supply	
Vss	Ground	
N/C	No (internal) Connection	

16.3 DC CHARACTERISTICS: PIC16C5X-RC, XT, HS, LP (Commercial)

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions Operating temperature 0 ≤ TA ≤ +70°C, unless otherwise stated Operating voltage VDD = 3.0V to 5.5V unless otherwise stated					
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage						
PIC16C5X-XT	VDD	3.0		6.25	V	Fosc = DC to 4 MHz
PIC16C5X-RC		3.0		6.25	V	Fosc = DC to 4 MHz
PIC16C5X-HS		4.5		5.5	V	Fosc = DC to 20 MHz
PIC16C5X-LP		2.5		6.25	V	Fosc = DC to 40 KHz
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See Section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See Section 13.1 for details on power on
Supply Current (Note 2)						
PIC16C5X-XT	IDD		1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
PIC16C5X-RC (Note 5)			1.8	3.3	mA	Fosc = 4 MHz , VDD = 5.5V
PIC16C5X-HS			4.8	10	mA	Fosc =10 MHz, VDD = 5.5V
			9.0	20	mA	Fosc = 20 MHz, VDD = 5.5V
PIC16C5X-LP			15	32	µA	Fosc = 32 KHz, VDD=3.0V, WDT disabled
Power Down Current (Note 4)						
PIC16C5X	IPD		4	12	µA	VDD = 3.0V, WDT enabled
			0.6	9	µA	VDD = 3.0V, WDT disabled

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
a) The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.4 DC CHARACTERISTICS: PIC16C5XI-RC, XT, HS, LP (Industrial)

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions Operating temperature -40 ≤ TA ≤ +85°C, unless otherwise stated Operating voltage VDD = 3.5V to 5.5V unless otherwise stated					
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage						
PIC16C5X-XT	VDD	3.0		6.25	V	FOSC = DC to 4 MHz
PIC16C5X-RC		3.0		6.25	V	FOSC = DC to 4 MHz
PIC16C5X-HS		4.5		5.5	V	FOSC = DC to 20 MHz
PIC16C5X-LP		2.5		6.25	V	FOSC = DC to 40 KHz
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on reset
Supply Current (Note 2)						
PIC16C5X-XT	IDD		1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-RC (Note 5)			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-HS			4.8	10.0	mA	FOSC = 10 MHz, VDD = 5.5V
			9.0	20.0	mA	FOSC = 20 MHz, VDD = 5.5V
PIC16C5X-LP			19	40	µA	FOSC = 32 KHz, VDD = 3.0V, WDT disabled
Power Down Current (Note 4)						
PIC16C5X	IPD		5	14	µA	VDD = 3.0V, WDT enabled
			0.8	12	µA	VDD = 3.0V, WDT disabled

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
a) The test conditions for all IDD measurements in active operation mode are:
OSC1= external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.5 DC CHARACTERISTICS: PIC16C5XE-RC, XT, HS, LP (Automotive)

DC CHARACTERISTICS, POWER SUPPLY PINS		Standard Operating Conditions Operating temperature -40 ≤ TA ≤ +125°C, unless otherwise stated Operating voltage VDD = 3.5V to 5.5V unless otherwise stated				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage						
PIC16C5X-XT	VDD	3.25		6.0	V	Fosc = DC to 4 MHz
PIC16C5X-RC		3.25		6.0	V	Fosc = DC to 4 MHz
PIC16C5X-HS		4.5		5.5	V	Fosc = DC to 20 MHz
PIC16C5X-LP		2.5		6.0	V	Fosc = DC to 40 KHz
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on reset
Supply Current (Note 2)						
PIC16C5X-XT	IDD		1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
PIC16C5X-RC (Note 5)			1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
PIC16C5X-HS			4.8	10.0	mA	Fosc = 10 MHz, VDD = 5.5V
			9.0	20.0	mA	Fosc = 16 MHz, VDD = 5.5V
PIC16C5X-LP			25	55	µA	Fosc = 32 KHz, VDD = 3.25V, WDT disabled
Power Down Current (Note 4)						
PIC16C5X	IPD		5	22	µA	VDD = 3.25V, WDT enabled
			0.8	18	µA	VDD = 3.25V, WDT disabled

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
OSC1= external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.6 DC CHARACTERISTICS: PIC16C5X-RC, XT, HS, LP (Commercial) PIC16C5XI-RC, XT, HS, LP (Industrial)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY		Standard Operating Conditions (unless otherwise stated) Operating temperature -40 < TA < +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec tables 16.3 and 16.4				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Input Low Voltage						
I/O ports	VIL	VSS		0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt trigger)		VSS		0.15 VDD	V	
RTCC (Schmitt trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt trigger)		VSS		0.15 VDD	V	PIC16C5XRC only (Note 5)
OSC1		VSS		0.3 VDD	V	PIC16C5X-XT, HS, LP
Input High Voltage						
I/O ports	VIH	0.45 VDD		VDD	V	For all VDD (Note 6)
		2.0		VDD	V	4.0 V < VDD ≤ 5.5 V (Note 6)
		0.36 VDD		VDD	V	VDD > 5.5 V
MCLR (Schmitt trigger)		0.85 VDD		VDD	V	
RTCC (Schmitt trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt trigger)		0.85 VDD		VDD	V	PIC16C5X-RC only (Note 5)
OSC1		0.7 VDD		VDD	V	PIC16C5X-XT, HS, LP
Input Leakage Current (Notes 3, 4)						**For VDD ≤ 5.5V**
I/O ports	IIL	-1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		-5			µA	VPIN = VSS + 0.25V
MCLR			0.5	+5	µA	VPIN = VDD
RTCC		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, HS, LP
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT (PIC16C5X-RC)				0.6	V	IOL = 1.6 mA, VDD = 4.5V
Output High Voltage						
I/O Ports (Note 4)	VOH	VDD-0.7			V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT (PIC16C5X-RC)		VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : For PIC16C5XRC devices, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

Note 6: The user may use better of the two specifications.

16.7 DC CHARACTERISTICS: PIC16C5X-RC, XT, HS, LP (Automotive)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY		Standard Operating Conditions (unless otherwise stated) Operating temperature -40 < TA < +125°C Operating voltage VDD range as described in DC spec tables 16.3 and 16.4				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Input Low Voltage						
I/O ports	VIL	VSS		0.15 VDD	V	Pin at high-impedance
MCLR (Schmitt trigger)		VSS		0.15 VDD	V	
RTCC (Schmitt trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt trigger)		VSS		0.15 VDD	V	PIC16C5XRC only (Note 5)
OSC1		VSS		0.3 VDD	V	PIC16C5X-XT, HS, LP
Input High Voltage						
I/O ports	VIH	0.45 VDD		VDD	V	For all VDD (Note 6)
		2.0		VDD	V	4.0 V < VDD ≤ 5.5 V (Note 6)
		0.36 VDD		VDD	V	VDD > 5.5 V
MCLR (Schmitt trigger)		0.85 VDD		VDD	V	
RTCC (Schmitt trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt trigger)		0.85 VDD		VDD	V	PIC16C5X-RC only (Note 5)
OSC1		0.7 VDD		VDD	V	PIC16C5X-XT, HS, LP
Input Leakage Current (Notes 3, 4)						**For VDD ≤ 5.5V**
I/O ports	IIL	-1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		-5			µA	VPIN = VSS + 0.25V
MCLR			0.5	+5	µA	VPIN = VDD
RTCC		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD , PIC16C5X-XT, HS, LP
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT (PIC16C5X-RC)				0.6	V	IOL = 1.6 mA, VDD = 4.5V
Output High Voltage						
I/O Ports (Note 4)	VOH	VDD-0.7			V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT (PIC16C5X-RC)		VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : For PIC16C5XRC devices, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

Note 6: The user may use better of the two specifications.

16.8 AC CHARACTERISTICS: PIC16C5X-RC, XT, HS, LP (Commercial) PIC16C5XI-RC, XT, HS, LP (Industrial) PIC16C5XI-RC, XT, HS, LP (Automotive)

AC CHARACTERISTICS **Standard Operating Conditions (unless otherwise stated)**
Operating temperature T_A = -40°C to +85°C (industrial),
T_A = -40°C to +125°C (automotive) and 0°C ≤ T_A ≤ +70°C (commercial)
Operating voltage V_{DD} range as described in DC spec tables 16.3 and 16.4

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
External CLOCKIN Frequency (Note 2)	FOSC	DC		4	MHz	RC mode
		DC		4	MHz	XT mode
		DC		20	MHz	HS mode (Com/Ind)
		DC		16	MHz	HS mode (Automotive)
		DC		40	KHz	LP mode
Oscillator Frequency (Note 2)	FOSC	DC		4	MHz	RC mode
		0.1		4	MHz	XT mode
		4		20	MHz	HS mode (Com/Ind)
		4		16	MHz	HS mode (Automotive)
		DC		40	KHz	LP mode
Instruction Cycle Time (Note 2)	TCY	1.0	4/FOSC	DC	µs	RC mode
		1.0		DC	µs	XT mode
		0.2		DC	µs	HS mode
		100		DC	µs	LP mode
External Clock in Timing (Note 4)						
Clock in (OSC1) High or Low Time						
XT oscillator type	TCKHLXT	50*			ns	
LP oscillator type	TCKHLLP	2*			µs	
HS oscillator type	TCKHLHS	20*			ns	
Clock in (OSC1) Rise or Fall Time						
XT oscillator type	TCKRFXT	25*			ns	
LP oscillator type	TCKRFLP	50*			ns	
HS oscillator type	TCKRFHS	25*			ns	
RESET Timing						
$\overline{MCLR}$ Pulse Width (low)	TMCL	100*			ns	
RTCC Input Timing, No Prescaler						
RTCC High Pulse Width	TRTH	0.5 TCY+ 20*			ns	Note 3
RTCC Low Pulse Width	TRTL	0.5 TCY+ 20*			ns	Note 3
RTCC Input Timing, With Prescaler						
RTCC High Pulse Width	TRTH	10*			ns	Note 3
RTCC Low Pulse Width	TRTL	10*			ns	Note 3
RTCC Period	TRTP	$\frac{T_{CY} + 40}{N}$ *			ns	Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Timeout Period (No Prescaler)	TWDT	9*	18*	30*	ms	VDD = 5.0V
Oscillation Start-up Timer Period	TOST	9*	18*	30*	ms	VDD = 5.0V
I/O Timing						
I/O Pin Input Valid Before CLKOUT↑ (RC Mode)	TDS	0.25 TCY+ 30*			ns	
I/O Pin Input Hold After CLKOUT↑ (RC Mode)	TDH	0*			ns	
I/O Pin Output Valid After CLKOUT↓ (RC Mode)	TPD			40*	ns	

* Guaranteed by characterization, but not tested.

(Notes on next page)

NOTES TO TABLE 16.8:

1. Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.
2. Instruction cycle period (Tcy) equals four times the input oscillator time base period.
   All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
   When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.
3. For a detailed explanation of RTCC input clock requirements see section 4.2.1.
4. Clock-in high-time is the duration for which clock input is at VIHOSC or higher.
   Clock-in low-time is the duration for which clock input is at VILOSC or lower.

16.9 Electrical Structure of Pins

FIGURE 16.9.1 - ELECTRICAL STRUCTURE OF I/O PINS (RA, RB, RC)

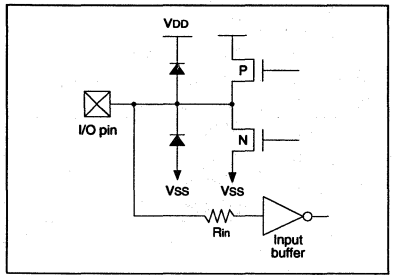
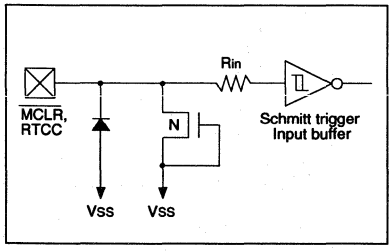


FIGURE 16.9.2 - ELECTRICAL STRUCTURE OF MCLR AND RTCC PINS



Notes to Figures 16.9.1 and 16.9.2: The diodes and the grounded gate (or output driver) NMOS device are carefully designed to protect against ESD (Electrostatic discharge) and EOS (Electrical overstress). Rin is a small resistance to further protect the input buffer from ESD.

17.0 TIMING DIAGRAMS

FIGURE 17.0.1 - RTCC TIMING

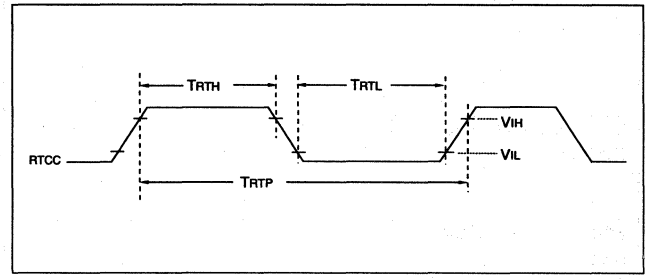


FIGURE 17.0.2 - OSCILLATOR START-UP TIMING (PIC16C5XRC)

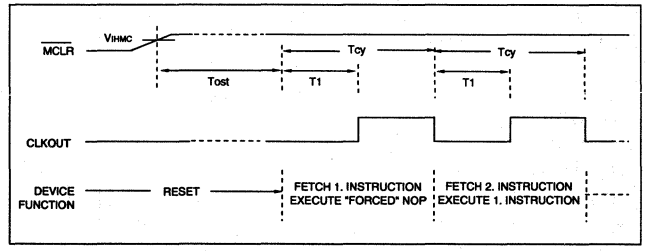
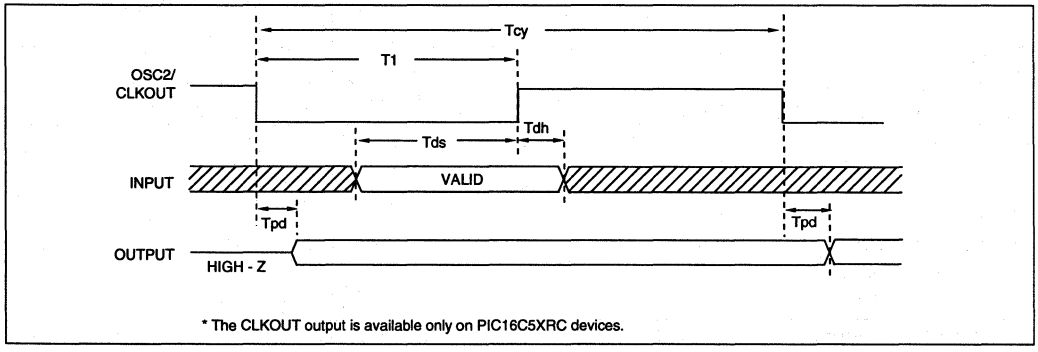


FIGURE 17.0.3 - INPUT/OUTPUT TIMING FOR I/O PORTS (PIC16C5XRC*)



* The CLKOUT output is available only on PIC16C5XRC devices.

18.0 DC AND AC CHARACTERISTICS GRAPHS/TABLES:

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

FIGURE 18.0.1 - TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

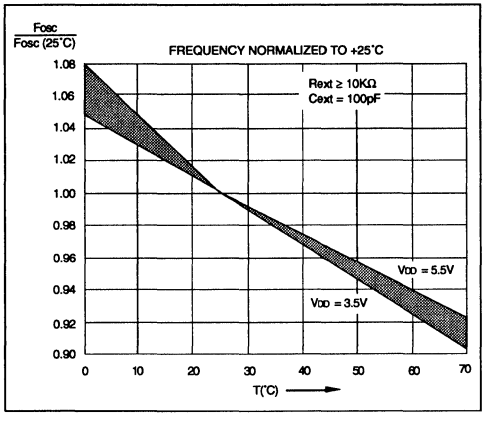
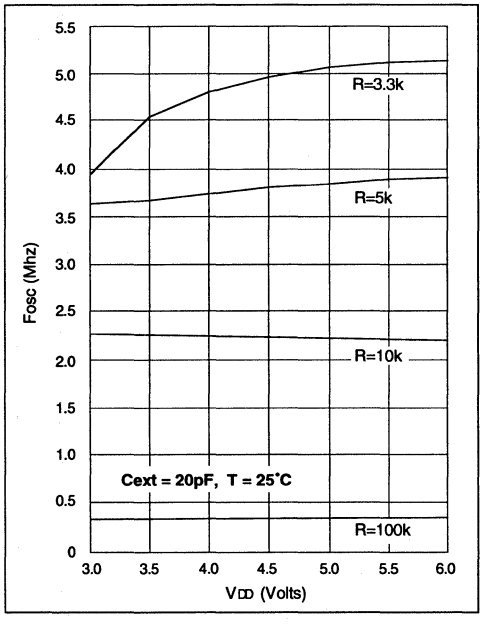
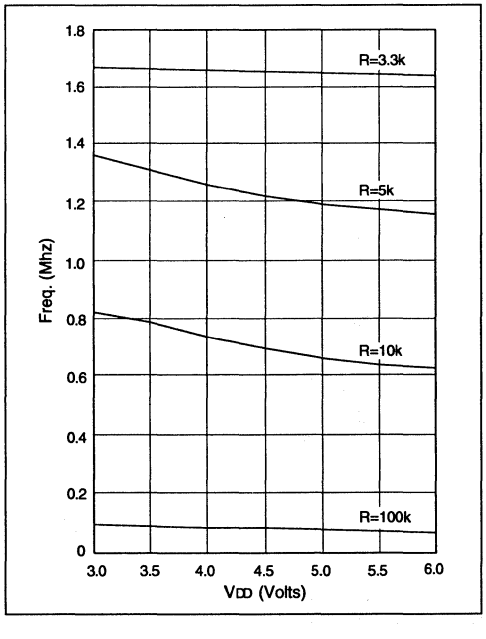


FIGURE 18.0.2 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD*



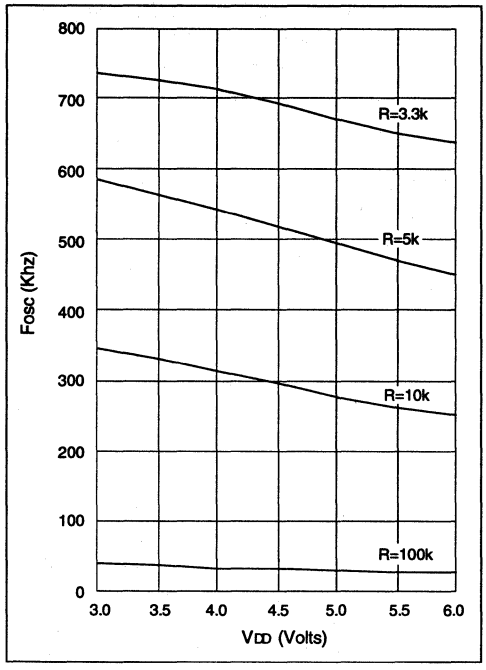
* Measured on DIP packages.

FIGURE 18.0.3 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD*



* Measured on DIP packages.

FIGURE 18.0.4 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD*



* Measured on DIP packages.

TABLE 18.0.1 - RC OSCILLATOR FREQUENCIES*

Cext	Rext	Average Fosc @ 5V, 25°C	
20pF	3.3k	4.973 MHz	± 27%
	5k	3.82 MHz	± 21%
	10k	2.22 MHz	± 21%
	100k	262.15 KHz	± 31%
100pF	3.3k	1.63 MHz	± 13%
	5k	1.19 MHz	± 13%
	10k	648.64 KHz	± 18%
	100k	71.56 KHz	± 25%
300pF	3.3k	660.0 KHz	± 10%
	5k	484.1 KHz	± 14%
	10k	267.63 KHz	± 15%
	100k	29.44 KHz	± 19%

* Measured on DIP packages.

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.

FIGURE 18.0.5 - TYPICAL Ipd vs VDD WATCHDOG DISABLED 25°C

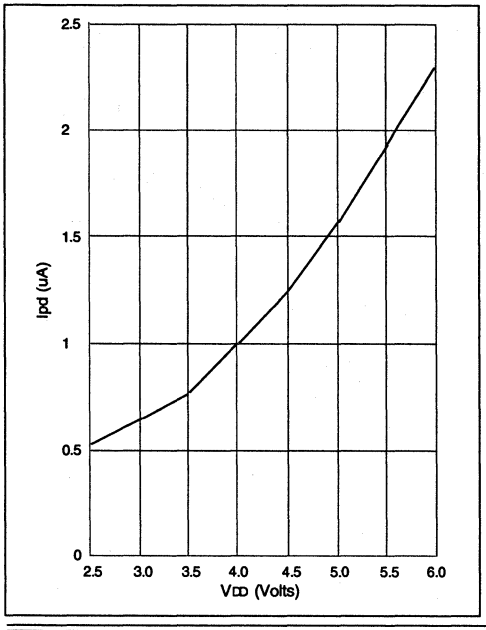


FIGURE 18.0.6 - TYPICAL Ipd vs VDD WATCHDOG ENABLED 25°C

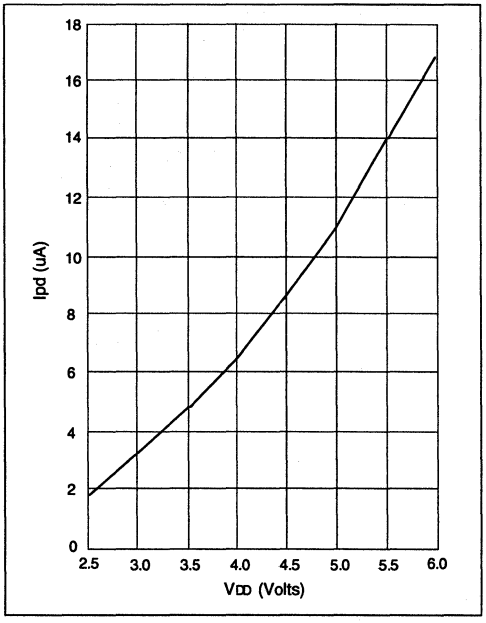


FIGURE 18.0.7 - MAXIMUM Ipd vs VDD WATCHDOG DISABLED

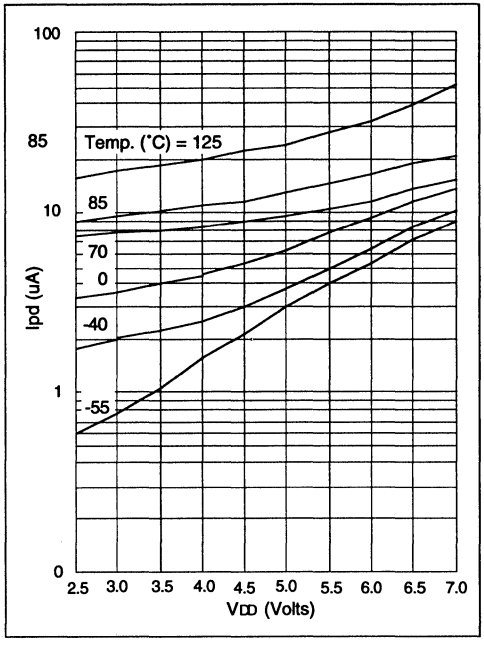
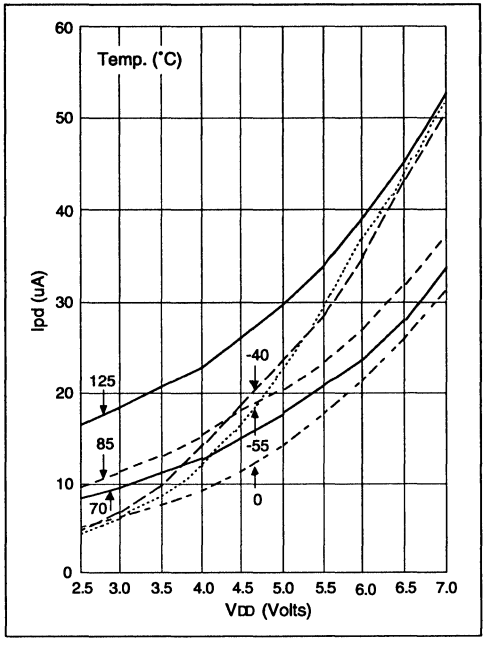


FIGURE 18.0.8 - MAXIMUM Ipd vs VDD WATCHDOG ENABLED*



* IPD, with watchdog timer enabled, has two components: The leakage current which increases with higher temperature and the operating current of the watchdog timer logic which increases with lower temperature. At -40°C, the latter dominates explaining the apparently anomalous behavior.

FIGURE 18.0.9 - VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs VDD

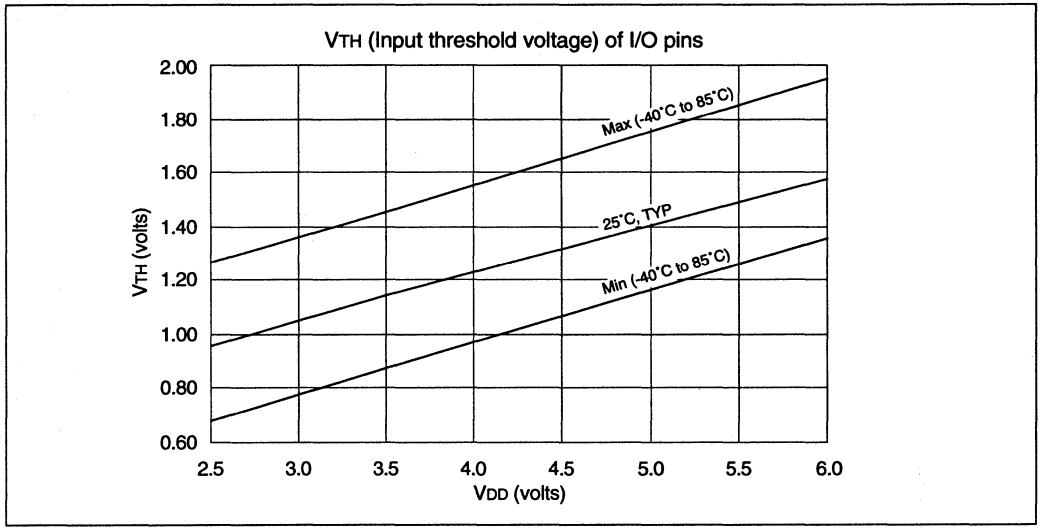
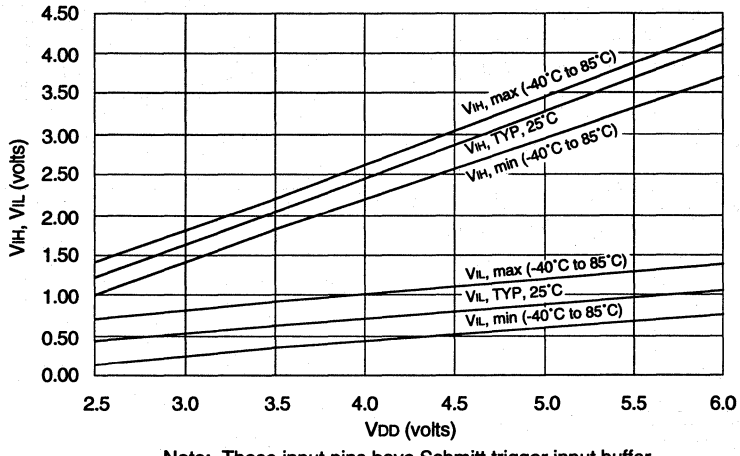


FIGURE 18.0.10 - V_{IH}, V_{IL} OF $\overline{MCLR}$, RTCC AND OSC1 (IN RC MODE) vs V_{DD}



Note: These input pins have Schmitt trigger input buffer.

FIGURE 18.0.11 - V_{TH} (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs V_{DD}

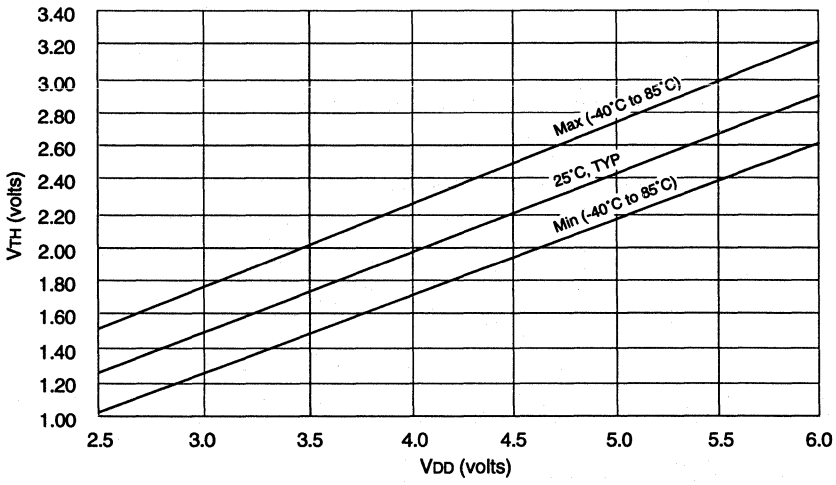


FIGURE 18.0.12 - TYPICAL IDD vs FREQ (EXT CLOCK, 25°C)

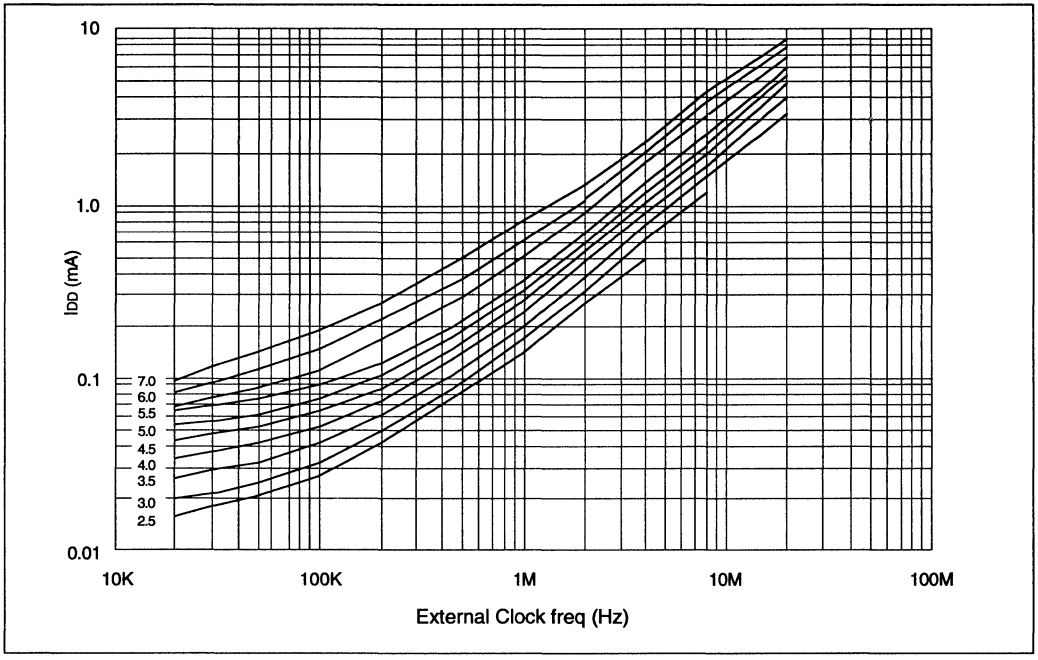


FIGURE 18.0.13 - MAXIMUM IDD vs FREQ (EXT CLOCK, -40° to +85°C)

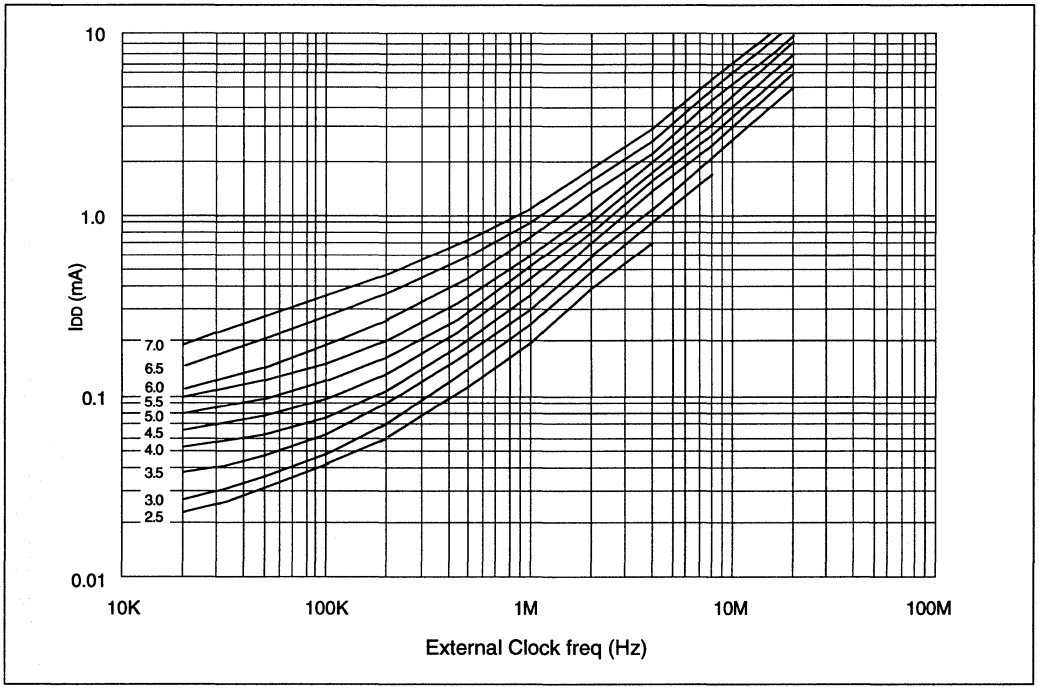


FIGURE 18.0.14 - MAXIMUM IDD vs FREQ (EXT CLOCK, -55° to +125°C)

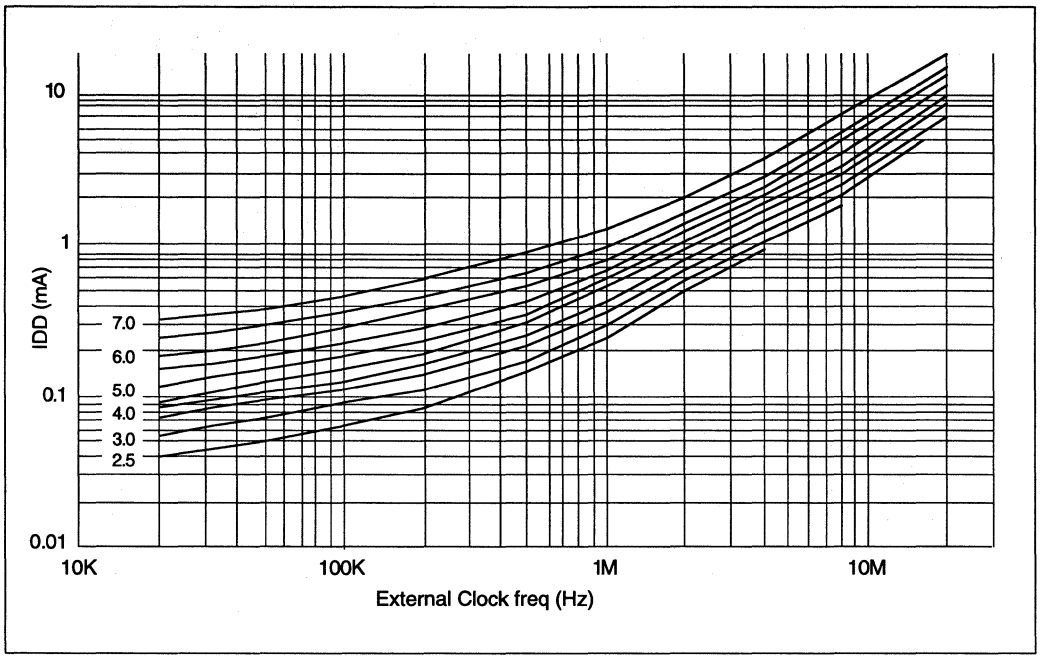


FIGURE 18.0.15 - WDT Timer Time-out Period vs VDD

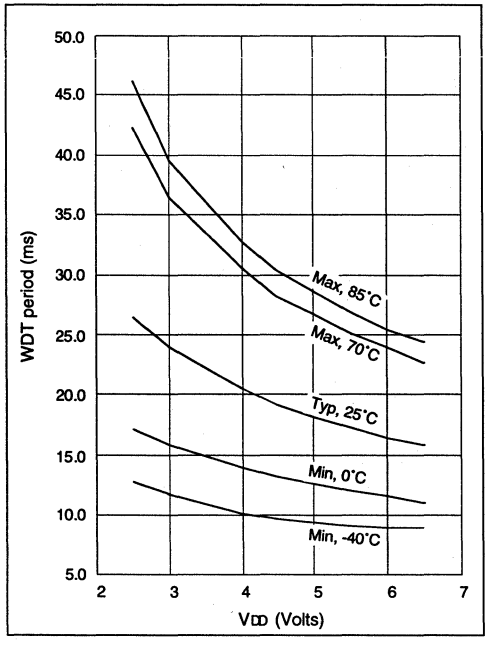


FIGURE 18.0.16 - Transconductance (gm) of HS Oscillator vs VDD

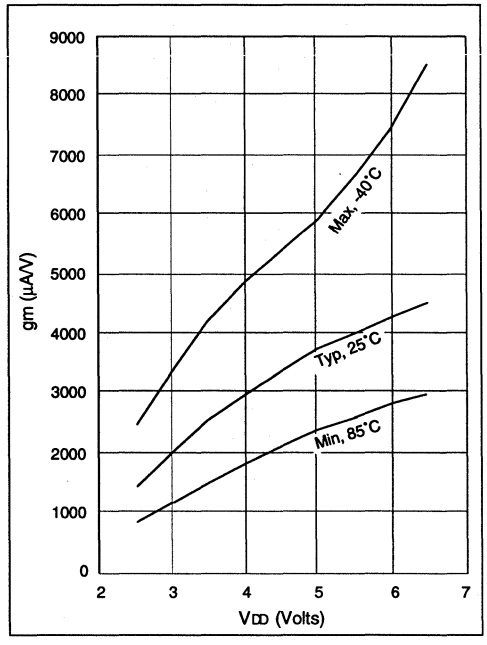


FIGURE 18.0.17 - Transconductance (gm) of LP Oscillator vs VDD

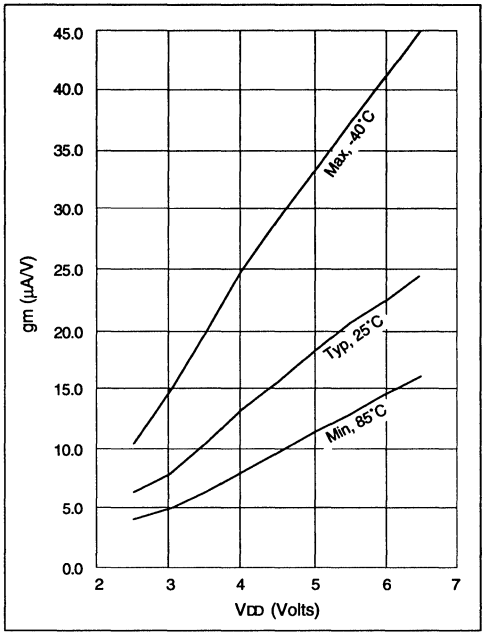


FIGURE 18.0.18 - Transconductance (gm) of XT Oscillator vs VDD

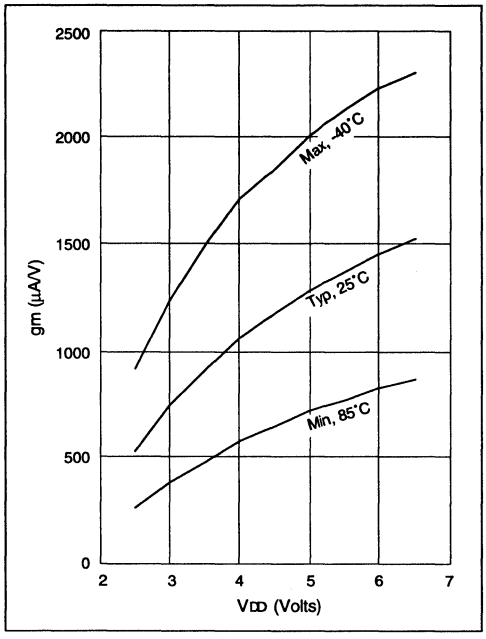


FIGURE 18.0.19 - IOH vs VOH, VDD = 3V

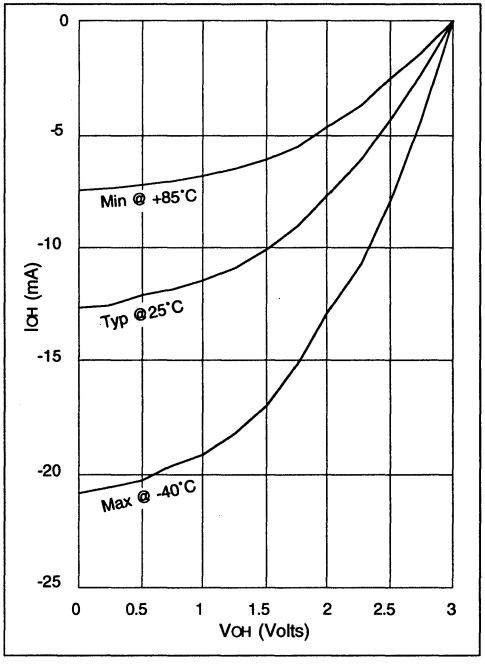


FIGURE 18.0.20 - IOH vs VOH, VDD = 5V

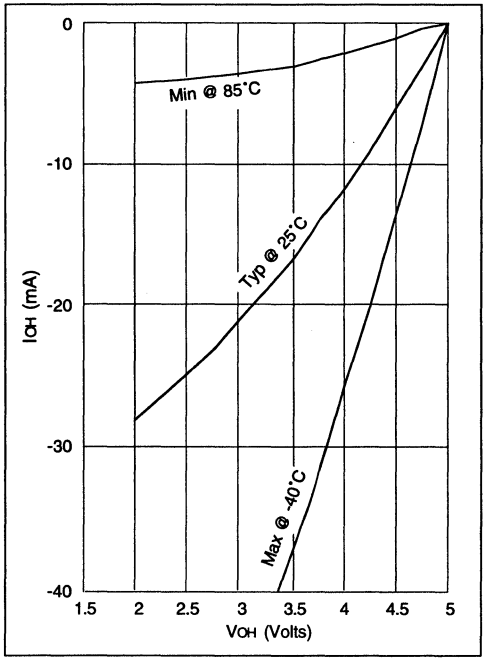


FIGURE 18.0.21 - IOL vs VOL, VDD = 3V

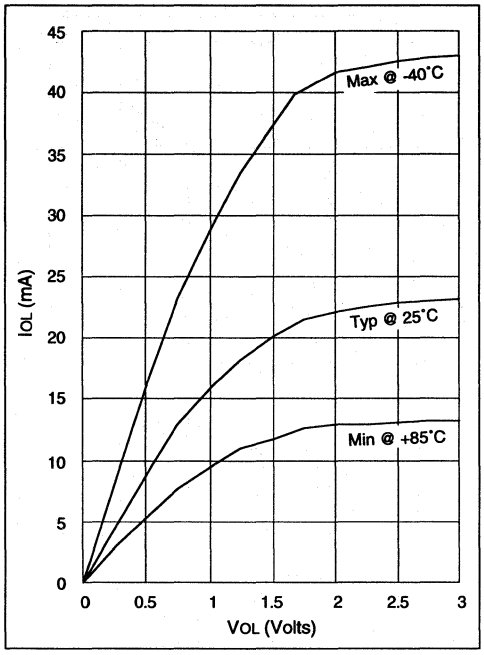


FIGURE 18.0.22 - IOL vs VOL, VDD = 5V

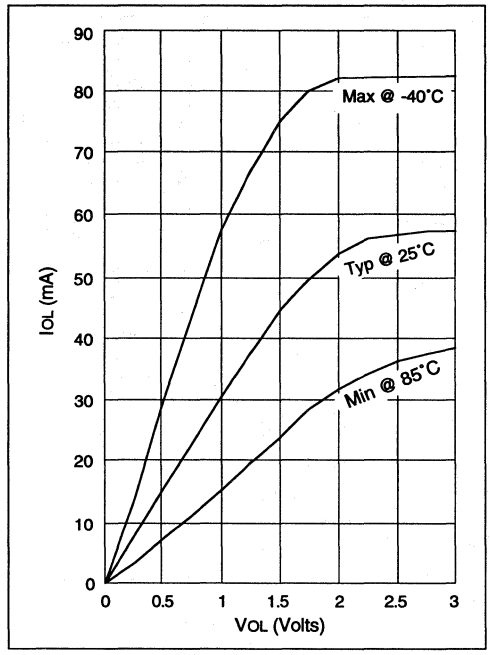


TABLE 18.0.2 - INPUT CAPACITANCE FOR PIC16C54/56 *

Pin Name	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
RTCC	3.2	2.8

* All capacitance values are typical at 25°C and measured at 1 MHz. A part to part variation of ±25% (three standard deviations) should be taken into account.

TABLE 18.0.3 - INPUT CAPACITANCE FOR PIC16C55/57 *

Pin Name	Typical Capacitance (pF)	
	28L PDIP (600 mil)	28L SOIC
RA port	5.2	4.8
RB port	5.6	4.7
RC port	5.0	4.1
MCLR	17.0	17.0
OSC1	6.6	3.5
OSC2/CLKOUT	4.6	3.5
RTCC	4.5	3.5

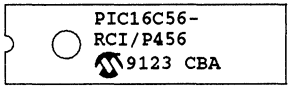
19.0 PACKAGING INFORMATION

See Section 11 of the Data Book.

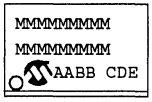
19.1 Package Marking Information

18L PDIP

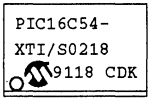
Example



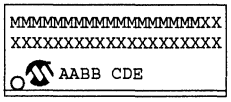
18L SOIC



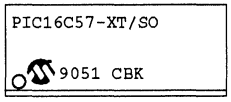
Example



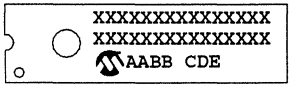
28L SOIC



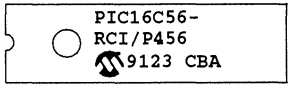
Example



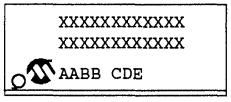
28L PDIP (.300 mil)



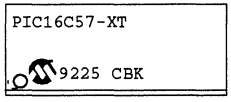
Example



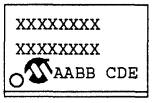
28L SSOP



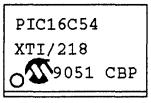
Example



20L SSOP



Example



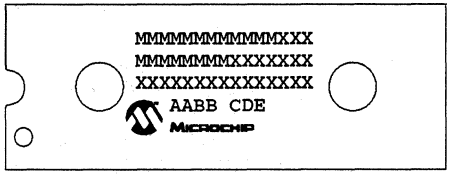
Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

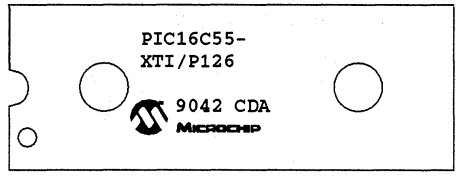
*Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are incuded in QTP price.

19.1 Package Marking Information (Cont.)

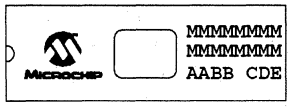
28L PDIP (.600 mil)



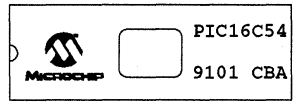
Example



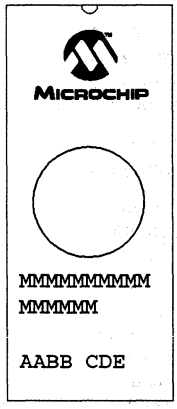
18L Cerdip



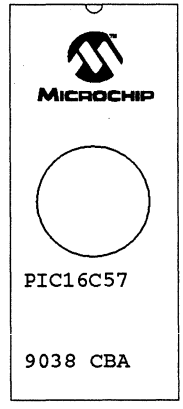
Example



28L Cerdip



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
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	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

20.0 DEVELOPMENT SUPPORT

20.1 Development Tools

The PIC16C5X and PIC16CXX microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER™ Real-Time In-Circuit Emulator
- PRO MATE™ Universal Programmer
- PICSTART™ Low-Cost Prototype Programmer
- Assembler
- Software Simulator

20.2 PICMASTER™: High Performance Universal In-Circuit Emulator

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X, PIC16CXX and PIC17CXX families.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16C5X, PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on PC compatible machines ranging from 80286-AT® class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.1 environment, allowing the operator access to a wide range of supporting software and accessories.

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.1 environment was chosen to best make these features available to you, the end user.

The PICMASTER Emulator Universal System consists primarily of four major components:

- Host-Interface Card
- Emulator Control Pod
- Target-Specific Emulator Probe
- PC Host Emulation Control Software

The Windows 3.1 System is a multitasking operating system which will allow the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window.

Dynamic Data Exchange (DDE), a feature of Windows 3.1, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

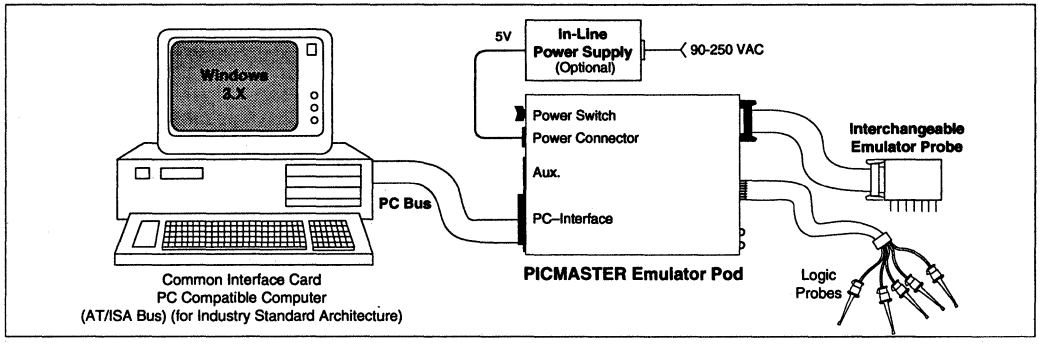
Under Windows 3.1, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16CXX processor and a PIC17CXX processor).

20.3 PRO MATE™: Universal Programmer

The PRO MATE Universal Programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MATE has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability . It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MATE can read, verify or program PIC16C5X, PIC16CXX and PIC17CXX devices. It can also set fuse configuration and code-protect in this mode. Its EEPROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.

FIGURE 20.2 - PICMASTER SYSTEM CONFIGURATION



In PC-hosted mode, the PRO MATE connects to the PC via one of the COM (RS232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of VDD min, VDD max and VPP levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different serial number, sequential or random.

The PRO MATE has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. PRO MATE supports all PIC16C5X, PIC16CXX and PIC17CXX processors.

20.4 PICSTART™ Programmer

The PICSTART™ programmer is an easy to use, very low-cost prototype programmer. It connects to the PC via one of the COM (RS232) ports. A PC based user interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based.

20.5 Assembler (MPASM)

Cross Assembler is a PC hosted symbolic assembler. It supports all microcontroller series including the PIC16C5X CMOS, PIC16CXX and PIC17CXX families.

MPASM offers fully featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from the Microchip Universal Emulator System (PICMASTER).

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro Assembly Capability
- Provides Object, Listing, Symbol and special files required for debugging with one of the Microchip Emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a full feature directive language represented by four basic classes of directives:

- **Data Directives** are those that control the allocation of memory and provide a way to refer to data items symbolically, by meaningful names.
- **Listing Directives** control the MPASM listing display. They allow the specification of titles and subtitles, page ejects and other listing control.
- **Control Directives** permit sections of conditionally assembled code.
- **Macro Directives** control the execution and data allocation within macro body definitions.

20.6 Software Simulator (MPSIM)

The Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16C5X and PIC16CXX series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in single step, execute until break or in a trace mode. Two forms of symbolic debugging are available: an internal symbol table for disassembling opcodes and the displaying of source code from a listing file. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

20.7 Development Systems

For convenience, the development tools are packaged into comprehensive systems as listed in Table 19-1:

TABLE 20-1: DEVELOPMENT SYSTEM PACKAGES

Item	Name	System Description
1.	PICMASTER™ System	PICMASTER In-Circuit Emulator with your choice of Target Probe, PRO MATE Programmer, Assembler, Software Simulator and Samples.
2.	PICSTART™ System	PICSTART™ Low-Cost Prototype Programmer, Assembler, Software Simulator and Samples

20.8 Probe Specifications

The PICMASTER probes currently meet the following specifications:

PICMASTER PROBE	Devices Supported	PROBE Maximum Frequency	PROBE Operating Voltage
PROBE - 16A	PIC16C54, PIC16C55, PIC16C56, and PIC16C57	4 MHZ	4.5V - 5.5V
PROBE - 16D	PIC16C54, PIC16C55, PIC16C56, PIC16C57, and PIC16C58	20 MHz	4.5V - 5.5V

21.0 EPROM PROGRAMMING

21.1 Prototype Programmers

Microchip's proprietary low cost PICSTART programmer is ideal for programming during development and prototyping. It is not recommended for production programming.

21.2 Production Quality Programmers

Microchip's PRO MATE programmer can be used for reliable programming for production. High volume programming is also supported by production quality programmers from third party sources. See Table 21.2.1.

Microchip assumes no responsibility for replacing defective units related to mechanical and/or electrical problems of any third party programming equipment or the improper use of such equipment.

Programming of the code protection bit (also called "security bit" or "security fuse") implies that the contents of the PIC16C5X EPROM can no longer be verified, thus making programming related failure analysis an impossibility.

Microchip warrants that PIC16C5X units will not exceed a programming failure rate of 1% of shipment quality. Programming related failures beyond this level can be returned for replacement, again, if the security bit has not been programmed.

21.3 Gang Programmers

Gang programmers are available from third party sources. See Table 21.2.1.

21.4 Factory Programming

High volume factory programming (QTP) is an available service from Microchip Technology. A small price adder and minimum quantity requirements apply.

TABLE 21.2.1 - LIST OF THIRD PARTY PROGRAMMERS*

Company	Model	Contact	Company	Model	Contact
ADVIN Systems, Inc.	PILOT™-U40	408-243-7000 U.S.	HI-LO	ALL-03	02 7640215 Taiwan
Application Solutions Ltd.	Programmer	273 476608 U.K.	Link Computer Graphics	CLK-3100	201-808-8990 U.S.
Baradine Products Ltd.	Micro-Burner™	604-988-9853 Canada	Logical Devices, Inc.	ALLPRO™-88	305-428-6868 U.S.
BP Microsystems	CP-1128™	800-225-2102 U.S. 713-668-4600 U.S.	Parallax, Inc.	PIC16C5X-PGM	916-624-8333 U.S.
Citadel Products Ltd.	PC-82	44-819-511-848 U.K.	Stag Microsystems	PP39	44-707-332-148 U.K.
Data I/O Corporation	Unisite™ with Site-48™ module	800-332-8246 U.S. 31(0) 6622866 Europe (03) 432-6991 Japan	Transdata	PGM16 PGM 16x8 Gang Programmer	(214) 980 2960
Elan Digital Systems Ltd.	EF-PER™ 5000 Series Gang Programmer	0489 579 799 U.K. (800) 541-3526 U.S.			

* For a complete listing of all Microchip third party support, please refer to the *Third Party Support Handbook* (DS00104A).

All trademarks shown in table 21.2.1 belong to their respective holders.

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CONNECTING TO MICROCHIP BBS

Connect world wide to the Microchip BBS using the CompuServe® communications network. In most cases a local call is your only expense. The Microchip BBS connection does not use CompuServe membership services, therefore **you do not need Compuserve membership to join Microchip's BBS.**

The procedure to connect will vary slightly from country to country. Please check with your local CompuServe agent for details if you have a problem. CompuServe services allows multiple users at baud rates up to 9600.

To connect:

1. Set your modem to 8 bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.

2. Dial your local CompuServe phone number.

3. Depress **<ENTER>** and a garbage string will appear because CompuServe is expecting a 7E1 setting.

4. Type **+ <ENTER>** and `Host Name:` will appear.

5. Type **MCHIPBBS<ENTER>** and you will be connected to the Microchip BBS.

In the United States, to find CompuServe's phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600 baud connection. After the system responds with `Host Name:`, type

NETWORK<ENTER> and follow CompuServe's directions.

For voice information (or calling from overseas), you may call (614) 457-1550 for your local CompuServe number.

PIC16C5X Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NO. - XX X /XX XXX

Pattern:	3-Digit Pattern Code for QTP (blank for OTP and Window Parts)	
Package:	P = PDIP	SS = SSOP (209 mil)
	SO = 300 mil SOIC (Gull Wing Lead)	JW* = CERDIP Window
	SP = 28L PDIP (300 mil)	S = Die in Waffle Pack
Temperature Range:	- = 0°C to +70°C (T for tape/reel)	
	I = -40°C to +85°C (S for tape/reel)	
	E = -40°C to +125°C	
Oscillator Type:	RC, HS	
	XT, LP	
Device:	PIC16C54	
	PIC16C55	
	PIC16C56	
	PIC16C57	

Examples:

a) PIC16C54 - XT/PXXX = "XT" oscillator, commercial temp., PDIP, QTP pattern

b) PIC16C55 - XTI/SO = "XT" oscillator, industrial temp., SOIC (OTP device)

c) PIC16C55 - JW = Commercial temp. CERDIP with WINDOW

d) PIC16C57-RCI/S = "RC oscillator", industrial temp., dice in waffle pack.

Notes: * For UV-erasable devices, the oscillator type is RC by default (= erased device). The user can select XT, HS, or LP oscillators by programming the appropriate fuses.

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local Compuserve number.

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

PIC16CR54

ROM-Based 8-Bit CMOS Microcontroller

FEATURES

High-Performance RISC-like CPU

- Only 33 single word instructions to learn
- All single cycle instructions (200ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200ns instruction cycle
- 12-bit wide instructions
- 8-bit wide data path
- 512 x 12 on-chip ROM program memory
- 25 x 8 general purpose registers (SRAM)
- Seven special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes

Peripheral Features

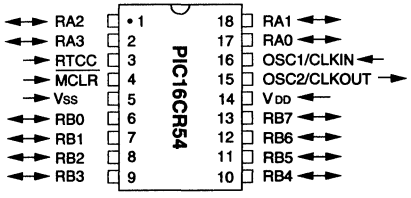
- 12 I/O pins with individual direction control
- 8-bit real time clock/counter (RTCC) with 8-bit programmable prescaler
- Power-on Reset
- Oscillator Start-up Timer
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security bit for code-protection
- Power saving SLEEP mode
- ROM mask selectable oscillator options:
  - Low-cost RC oscillator: RC
  - Standard crystal/resonator: XT
  - High-speed crystal/resonator: HS
  - Power saving, low frequency crystal: LP

CMOS Technology

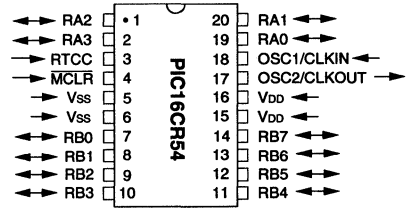
- Low-power, high-speed CMOS ROM technology
- Fully static design
- Wide-operating voltage range:
  - Commercial: 2.0V to 6.25V
  - Industrial: 2.0V to 6.25V
- Low-power consumption
  - < 2mA typical @ 5V, 4 MHz
  - 15μA typical @ 3V, 32 KHz
  - < 1μA typical standby current @ 3V

FIGURE A - PIN CONFIGURATION

PDIP, SOIC, CERDIP Window



SSOP



OVERVIEW

PIC16CR54 is a fully compatible ROM-version of the PIC16C54 EPROM based microcontroller and a member of the PIC16C5X microcontroller family. The PIC16CR54 is a low-cost, high performance, 8-bit, fully static CMOS microcontroller. It employs a RISC-like architecture with only 33 single word/single cycle instructions to learn. All instructions are single cycle (200ns) except in the case of program branches which take two cycles. The PIC16CR54 delivers performance an order of magnitude higher than its competitors in similar price category.The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression advantage over other 8-bit microcontrollers in its category. The easy to use and easy to remember instruction set reduces development time significantly.

The customer can also take full advantage of the UV-erasable PIC16C54 EPROM version for code development. The cost-effective One Time Programmable (OTP) version allows the customer to move in to production without committing to a final ROM code.

The PIC16CR54 is supported by an assembler, a software simulator and an in-circuit emulator. All the tools are supported by IBM PC® and compatible machines.

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1.0 GENERAL DESCRIPTION

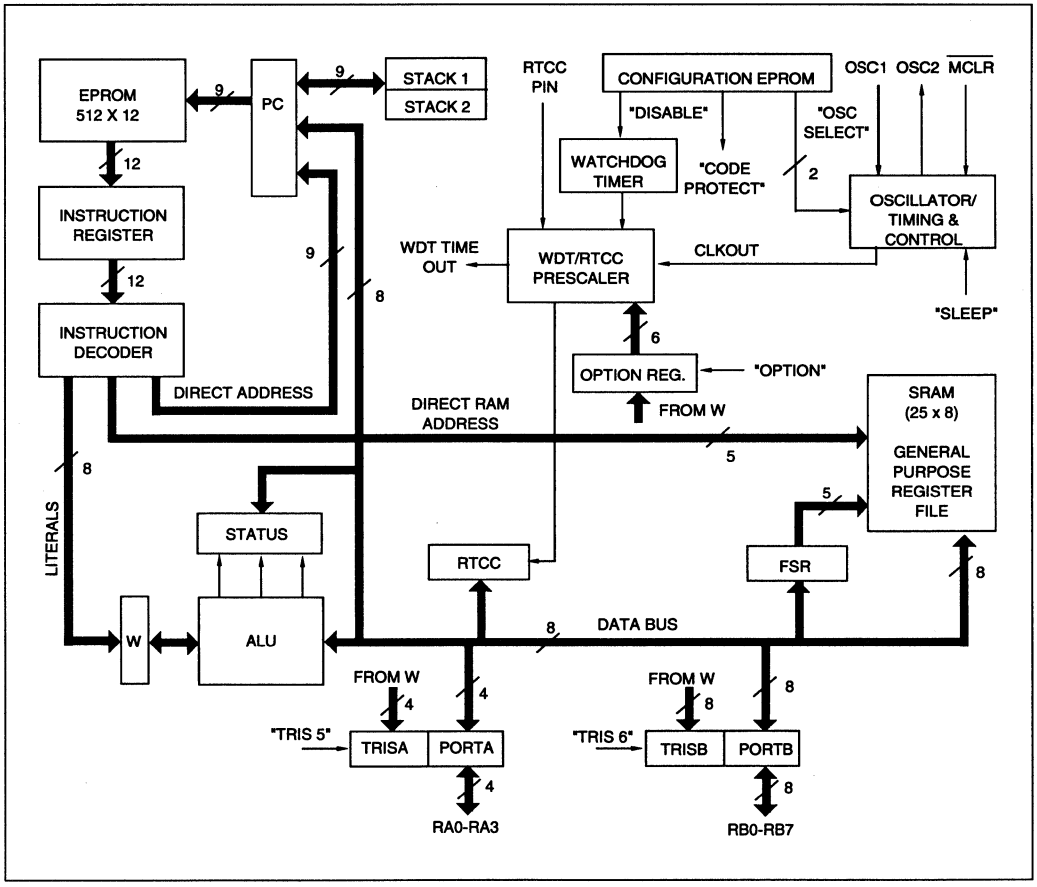
The Microchip Technology PIC16CR54 microcontroller is based on the proven architecture of the PIC16C5X product family. The PIC16CR54 is pin for pin compatible with the EPROM based PIC16C54, but it has the added advantage of an extended operating voltage.

1.1 Applications

The PIC16CR54 fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices, and telecommunications processors. The small footprint package for through hole or surface mounting make this microcontroller perfect for all applications with space limitations. Low-cost, low-power, high-performance, ease of use, and I/O flexibility make the PIC16CR54 very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

2

FIGURE 2.1.1 - PIC16CR54 BLOCK DIAGRAM



2.0 ARCHITECTURAL DESCRIPTION

2.1 Harvard Architecture

The PIC16CR54 single-chip microcomputer is a low-power, high-speed, fully static CMOS device containing ROM, RAM, I/O, and a central processing unit on a single chip.

The architecture is based on a register file concept with separate bus and memories for data and instructions (Harvard architecture). The data bus and memory (RAM) are 8-bits wide while the program bus and program memory (ROM) have a width of 12-bits. This concept allows a simple yet powerful instruction set designed to emphasize bit, byte and register operations under high speed with overlapping instruction fetch and execution cycles. In other words, while one instruction is executed, the following instruction is already being read from the program memory. A block diagram of the PIC16CR54 is given in Figure 2.1.1.

TABLE 2.1.1 - PIN FUNCTION TABLE

Name	Function
RA0 - RA3	I/O PORTA
RB0 - RB7	I/O PORTB
RTCC	Real Time Clock/Counter
$\overline{MCLR}$	Master Clear
OSC1/CLKIN	Oscillator (input)/External Clock Input
OSC2/CLKOUT	Oscillator (output)
VDD	Power supply
VSS	Ground

2.2 Clocking Scheme/Instruction Cycle

The clock input (from pin OSC1) is internally divided by four to generate four non overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, PC is incremented every Q1, instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 2.2.1.

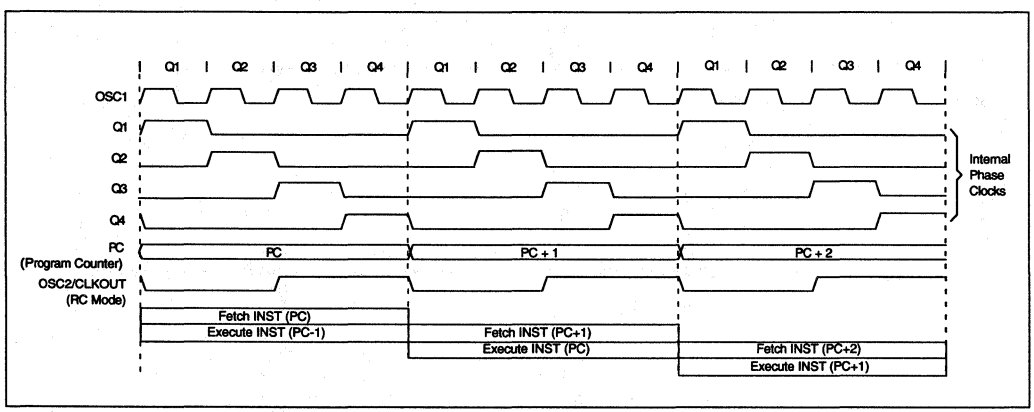
2.3 Data Register File

The 8-bit data bus connects two basic functional elements together: the Register File composed of 32 addressable 8-bit registers including the I/O Ports, and an 8-bit wide Arithmetic Logic Unit. The 32 bytes of RAM are directly addressable (Figure 2.3.1). Data can be addressed direct, or indirect using the file select register (f4). Immediate data addressing is supported by special "literal" instructions which load data from program memory into the W register.

The register file is divided into two functional groups: operational registers and general purpose registers. The operational registers include the Real Time Clock Counter (RTCC) register, the Program Counter (PC), the Status Register, the I/O registers (PORTs), and the File Select Register. The general purpose registers are used for data and control information under command of the instructions.

In addition, special purpose registers are used to control the I/O port configuration, and the prescaler options.

FIGURE 2.2.1 - CLOCKS/INSTRUCTION CYCLE



2.4 Arithmetic/Logic Unit (ALU)

The 8-bit wide ALU contains one temporary working register (W Register). It performs arithmetic and Boolean functions between data held in the W Register and any file register. It also does single operand operations on either the W register or any file register.

2.5 Program Memory

512 words of 12-bit wide on-chip read only program memory (ROM) can be directly addressed. Sequencing of instructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations, supporting direct, indirect, relative addressing modes, can be performed by Bit Test and Skip instructions, Call instructions, Jump instructions or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting.

3.0 PIC16CR54 OVERVIEW

A wide variety of oscillator types, frequency ranges, and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information and tables in this section. When placing orders, please refer to the part numbering system on the back page of this document.

To facilitate development and initial production phases, Microchip offers UV erasable EPROM version, One Time Programmable (OTP) version as well as Quick-Turnaround-Production (QTP) devices as described in the following sections. For more details on these, please refer to "PIC16C5X data-sheet" (Literature number DS30015) or contact your nearest sales office.

3.1 UV Erasable Device for Program Development

Microchip offers PIC16C54, the EPROM based version of the PIC16CR54 for program development. This device is optimal for prototype development and pilot series. The desired oscillator configuration is EPROM programmable as "RC", "XT", "HS" or "LP". An erased device is configured as "RC" type by default. The user should refer to the PIC16C5X data sheet for full electrical specification of these parts.

3.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates. OTP devices are ideal for initial production runs. OTP devices have the oscillator type pre-configured by the factory.

3.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. QTP devices are also ideal for initial production. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

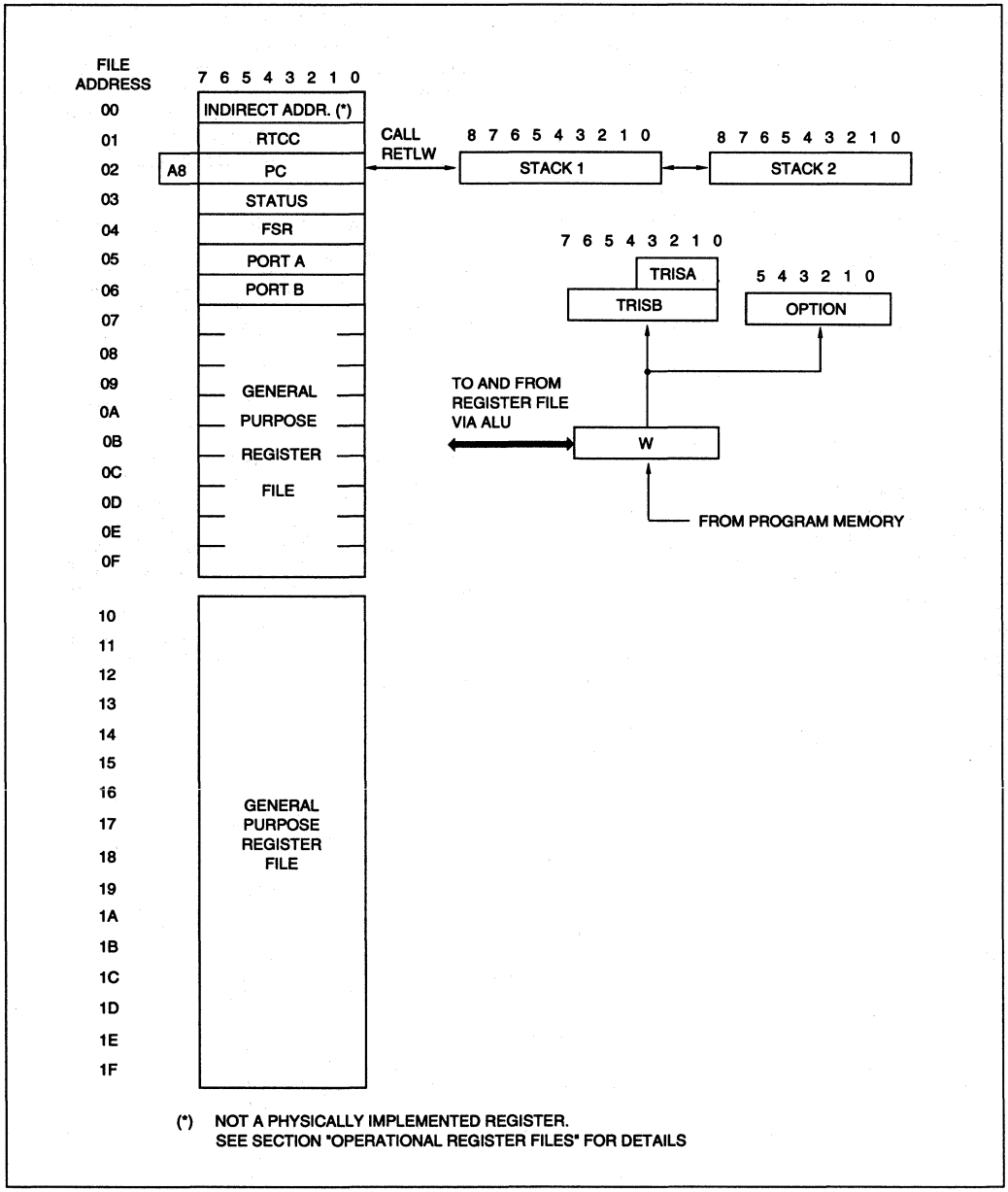
TABLE 3.0.1 - OVERVIEW OF PIC16CR54 DEVICES

Part #	ROM	RAM*	I/O	Supply Voltage	Frequency Range**	Package Options
PIC16CR54RC	512 x 12	32 x 8	12	2.5 - 6.25 V	DC - 4 MHz	18L PDIP, 18L SOIC (300 mil), 20L SSOP
PIC16CR54XT	512 x 12	32 x 8	12	2.5 - 6.25 V	0.1 - 4 MHz	18L PDIP, 18L SOIC (300 mil), 20L SSOP
PIC16CR54HS	512 x 12	32 x 8	12	4.5 - 5.5 V	4 - 20 MHz	18L PDIP, 18L SOIC (300 mil), 20L SSOP
PIC16CR54LP	512 x 12	32 x 8	12	2.0 - 6.25 V	DC - 200 KHz	18L PDIP, 18L SOIC (300 mil), 20L SSOP

* Including special function registers.

** All devices operate down to DC when external clock is applied.

FIGURE 2.3.1 - PIC16CR54 DATA MEMORY MAP



4.0 OPERATIONAL REGISTER FILES

4.1 Indirect Data Addressing (INDF)

This is not a physically implemented register. Addressing INDF calls for the contents of the File Select Register to be used to select a file register. INDF is useful as an indirect address pointer. For example, in the instruction ADDWF INDF, W will add the contents of the register pointed to by the FSR to the content of the W Register and place the result in W.

If INDF itself is read through indirect addressing (i.e. FSR = 0h), then 00h is read. If INDF is written to via indirect addressing, the result will be a NOP.

4.2 Real Time Clock/Counter Register (RTCC)

This register can be loaded and read by the program as any other register. In addition, its contents can be incremented by an external signal edge applied to the RTCC pin, or by the internal instruction cycle clock (CLKOUT=fosc/4). Figure 4.2.1 is a simplified block diagram of RTCC.

An 8-bit prescaler can be assigned to the RTCC by writing the proper values to the PSA bit and the PS bits in the OPTION register. OPTION register is a special register (not mapped in data memory) addressable using the 'OPTION' instruction. See Section 7.4 for details. If the prescaler is assigned to the RTCC, instructions writing to RTCC (e.g. CLRF RTCC, or BSF RTCC,5, ...etc.) clear the prescaler.

The bit "RTS" (RTCC signal Source) in the OPTION register determines, if RTCC is incremented internally or externally.

RTS=1: The clock source for the RTCC or the prescaler, if assigned to it, is the signal on the RTCC pin. Bit 4 of the OPTION register (RTE) determines, if an increment occurs on the falling (RTE=1) or rising (RTE=0) edge of the signal presented to the RTCC pin.

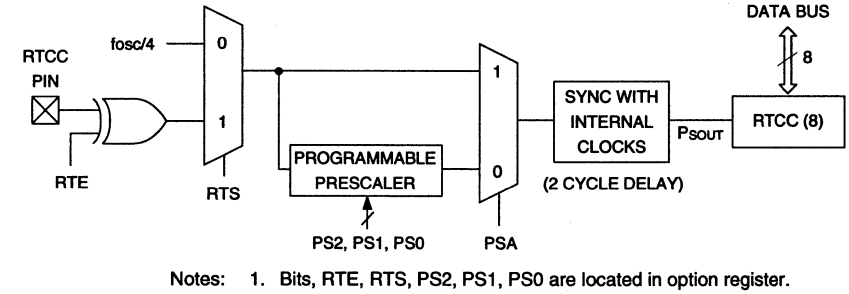
RTS=0: The RTCC register or its prescaler, respectively, will be incremented with the internal instruction clock (= Fosc/4). The "RTE" bit in the OPTION register and the RTCC pin are "don't care" in this case. The RTCC pin must not be left floating (tie to either VDD or VSS). This prevents unintended entering of test modes and to reduce the current consumption in low power applications.

As long as clocks are applied to the RTCC (from internal or external source, with or without prescaler), RTCC keeps incrementing and just rolls over when the value "FFh" is reached. All increment pulses for RTCC are delayed by two instruction cycles. After writing to RTCC, for example, no increment takes place for the following two instruction cycles. This is independent if internal or external clock source is selected. If a prescaler is assigned to the RTCC, the output of the prescaler will be delayed by two cycles before RTCC is incremented. This is true for instructions that either write to or read-modify-write RTCC (e.g. MOVF RTCC, CLRF RTCC). For applications where RTCC needs to be tested for zero without affecting its count, use of MOVF RTCC, W instruction is recommended. Timing diagrams in Figure 4.2.2 show RTCC read, write and increment timing.

4.2.1 USING RTCC WITH EXTERNAL CLOCK

When external clock input is used for RTCC, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements. Also, there is some delay from the occurance of the external clock edge to the actual incrementing of RTCC. Referring to Figure 4.2.1, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where tosc = oscillator time period.

FIGURE 4.2.1 - RTCC BLOCK DIAGRAM (SIMPLIFIED)



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 are located in option register.
2. The prescaler is shared with Watchdog Timer (see Figure 9.0.1).

When no prescaler is used, PSOUT (Prescaler output, see Figure 4.2.2.1) is the same as RTCC clock input and therefore the requirements are:

T_{RTH} = RTCC high time ≥ 2tosc + 20 ns
T_{RTL} = RTCC low time ≥ 2tosc + 20 ns

When prescaler is used, the RTCC input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.
Then: P_{SOUT} high time = P_{SOUT} low time = $\frac{N \bullet T_{RT}}{2}$
where T_{RT} = RTCC input period and N = prescale value (2, 4, ..., 256). The requirement is, therefore $\frac{N \bullet T_{RT}}{2}$ ≥ 2 tosc + 20 ns, or $T_{RT} \geq \frac{4 \text{ tosc} + 40 \text{ ns}}{N}$.

The user will notice that no requirement on RTCC high time or low time is specified. However, if the high time or low time on RTCC is too small then the pulse may not be detected, hence a minimum high or low time of 10ns is required. In summary, the RTCC input requirements are:

T_{RT} = RTCC period ≥ (4 tosc + 40 ns)/N
T_{RTH} = RTCC high time ≥ 10ns
T_{RTL} = RTCC low time ≥ 10ns

4.2.2 DELAY FROM EXTERNAL CLOCK EDGE

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the RTCC is actually incremented. Referring to Figure 4.2.2.1, the reader can see that this delay is between 3 tosc and 7 tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±500ns @ 8 MHz).

4.3 Program Counter (PC)

The program counter generates the addresses for on-chip ROM containing the program instruction words (Figure 4.3.1).

The program counter is set to all "1"s upon a RESET condition. During program execution it is auto incremented with each instruction unless the result of that instruction changes the PC itself:

a) "GOTO" instructions allow the direct loading of the lower nine program counter bits (PC <8:0>).
b) "CALL" instructions load the lower 8-bit of the PC directly while the ninth bit is cleared to "0". The PC value, incremented by one, will be pushed into the stack.
c) "RETLW" instructions load the program counter with the top of stack contents.

FIGURE 4.2.2A - RTCC TIMING: INT CLOCK/NO PRESCALE

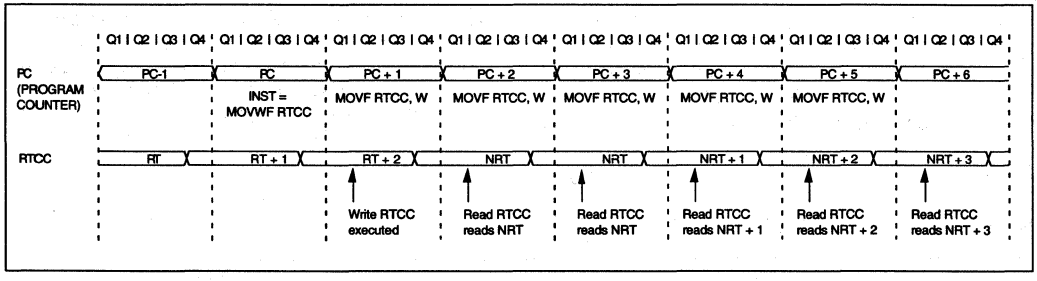
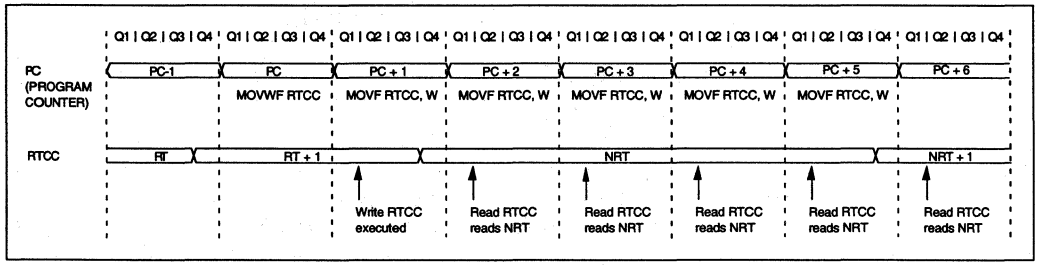


FIGURE 4.2.2B - RTCC TIMING: INT CLOCK/PRESCALE 1:2



d) If PC is the destination in any instruction (e.g. MOVWF PC, ADDWF PC, or BSF PC,5) then the computed 8-bit result will be loaded into the low 8-bits of program counter. The ninth bit of PC will be cleared.

It should be noted that because bit 8 (ninth bit) of PC is cleared in CALL instruction or any instruction which writes to the PC (e.g. MOVWF PC), all subroutine calls or computed jumps are limited to the first 256 locations of the program memory page (512 words long).

4.4 STACK

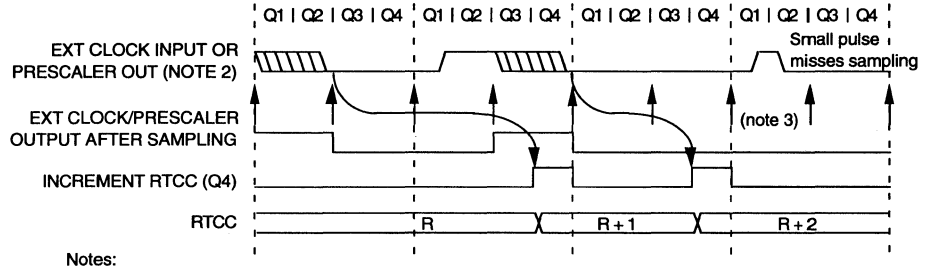
The PIC16CR54 has a two-level (9-bit wide) hardware push/pop stack (Figure 4.3.1).

CALL instructions push the current program counter value, incremented by "1", into stack level 1. Stack level 1 is automatically pushed to level 2. If more than two subsequent "CALL"s are executed, only the most recent two return addresses are stored.

RETLW instructions load the contents of stack level 1 into the program counter while stack level 2 gets copied into level 1. If more than two subsequent "RETLW"s are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the RETLW instruction. This is particularly useful for the implementation of "data" tables within the program memory.

2

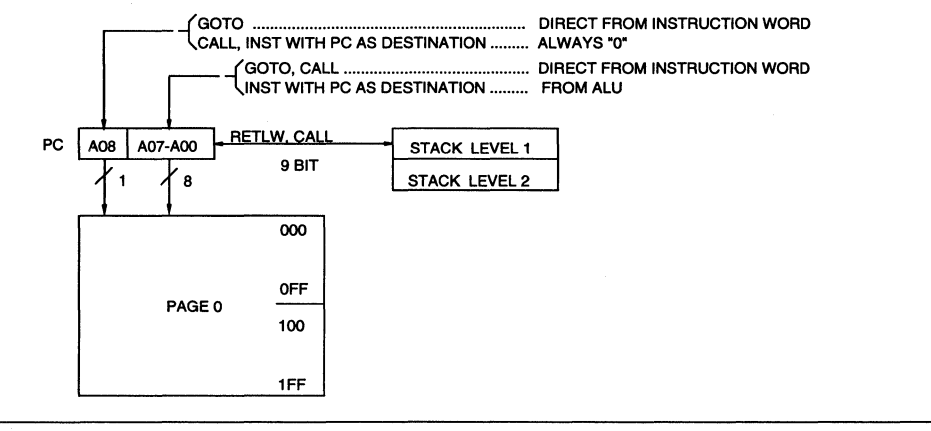
FIGURE 4.2.2.1 - RTCC TIMING WITH EXTERNAL CLOCK



Notes:

1. Delay from clock input change to RTCC increment is 3 tosc to 7 tosc. (Duration of Q = tosc). Therefore, the error in measuring the interval between two edges on RTCC input = ± 4 tosc max.
2. External clock if no prescaler selected, Prescaler output otherwise.
3. The arrows indicate the points in time where sampling occurs.

FIGURE 4.3.1 - PROGRAM MEMORY ORGANIZATION



4.5 Status Word Register

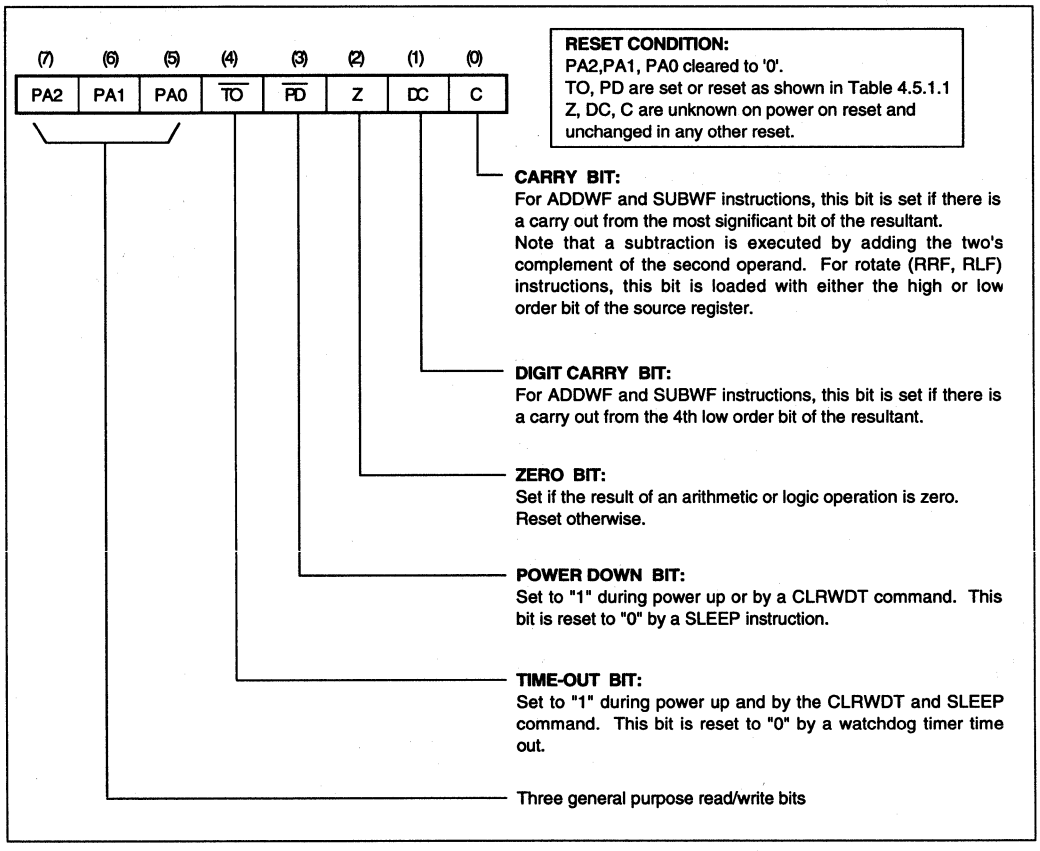
This register contains the arithmetic status of the ALU, and the RESET status.

The STATUS register can be destination for any instruction like any other register. However, the status bits are set after the following write. Furthermore, $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with STATUS register as destination may be different than intended. For example, CLRF STATUS will clear all bits except for $\overline{TO}$ and $\overline{PD}$ and then set the Z bit and leave the STATUS register as 000XX100 (where X = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the STATUS registers because these instructions do not affect any status bit.

For other instructions affecting status bits, see Section "Instruction Set Summary."

FIGURE 4.5.1 - STATUS WORD REGISTER



4.5.1 TIME OUT AND POWER DOWN STATUS BITS (TO, PD)

The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be tested to determine if a RESET condition has been caused by a Watchdog Timer time-out, a power-up condition, or a wake-up from SLEEP by the Watchdog Timer or $\overline{MCLR}$ pin.

These status bits are only affected by events listed in Table 4.5.1.1.

TABLE 4.5.1.1 - EVENTS AFFECTING $\overline{PD}$/$\overline{TO}$ STATUS BITS

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
WDT Timeout	0	X	No effect on $\overline{PD}$
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Note: A WDT timeout will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the PD bit. Table 4.5.1.2 reflects the status of $\overline{PD}$ and $\overline{TO}$ after the corresponding event.

TABLE 4.5.1.2 - $\overline{PD}$/$\overline{TO}$ STATUS AFTER RESET

TO	PD	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT time-out (not during SLEEP)
1	0	$\overline{MCLR}$ wake-up from SLEEP
1	1	Power-up
X	X	= Low pulse on $\overline{MCLR}$ input

Note: The $\overline{PD}$ and $\overline{TO}$ bit maintain their status (X) until an event of Table 4.5.1.1 occurs. A low-pulse on the MCLR input does not change the $\overline{PD}$ and $\overline{TO}$ status bits.

4.6 File Select Register (FSR)

Bits 0-4 select one of the 32 available file registers in the indirect addressing mode (that is, calling for file INDF in any of the file oriented instructions).

Bits 5-7 of the FSR are read-only and are always read as "one"s.

If no indirect addressing is used, the FSR can be used as a 5-bit wide general purpose register.

5.0 I/O REGISTERS (PORTS)

The I/O registers can be written and read under program control like any other register of the register file. However, "read" instructions (e.g. MOVF PORTB,W) always read the I/O pins, regardless if a pin is defined as "input" or "output." Upon a RESET condition, all I/O ports are defined as "input" (= high impedance mode) as the I/O control registers (TRISA, TRISB) are all set to "ones."

The execution of a "TRIS f" instruction with corresponding "zeros" in the W-register is necessary to define any of the I/O pins as output.

5.1 PORTA

4-bit I/O register. Low order 4-bits only are used (RA0 - RA3). Bits 4 - 7 are unimplemented and read as "zeros."

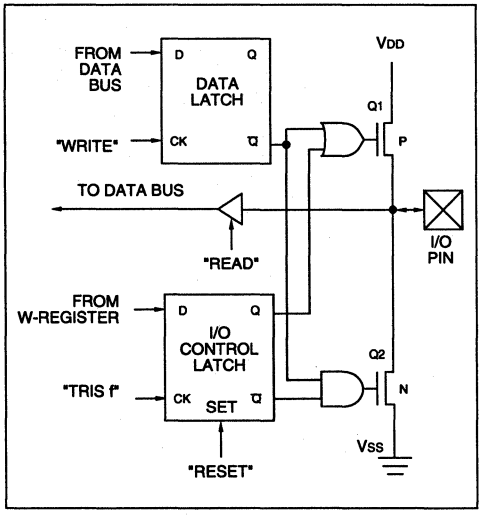
5.2 PORTB

8-bit I/O register.

5.3 I/O Interfacing

The equivalent circuit for an I/O port bit is shown in Figure 5.3.1. All ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g. MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB) must be set to zero. For use as an input, the corresponding TRIS bit must be "one". Any I/O pin can be programmed individually as input or output.

FIGURE 5.3.1 - EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



5.4 I/O Programming Considerations

5.4.1 BIDIRECTIONAL I/O PORTS

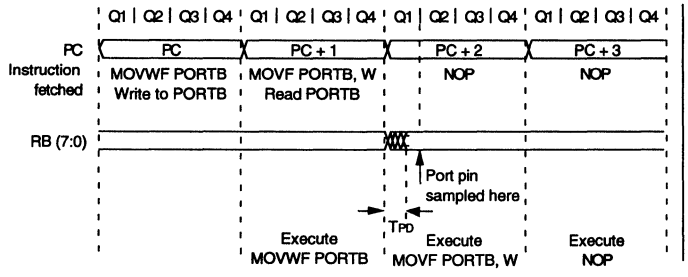
Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit 5 and PORTB is re-output to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

5.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see Figure 5.5.2.1). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

FIGURE 5.4.2.1 - I/O PORT READ/WRITE TIMING



2

6.0 GENERAL PURPOSE REGISTERS

f07h - f1Fh: are general purpose register files.

7.0 SPECIAL PURPOSE REGISTERS

7.1 W Working Register

Holds second operand in two operand instructions and/ or supports the internal data transfer.

7.2 TRISA I/O Control Register For PORTA

Only bits 0 - 3 are available. The I/O PORTA is only 4-bits wide.

7.3 TRISB I/O Control Register For PORTB

The I/O control registers will be loaded with the content of the W register by executing of the TRIS f instruction. A "1" in the I/O control register puts the corresponding I/O pin into a high impedance mode. A "0" puts the contents of file register PORTA or PORTB, respectively, out on the selected I/O pins.

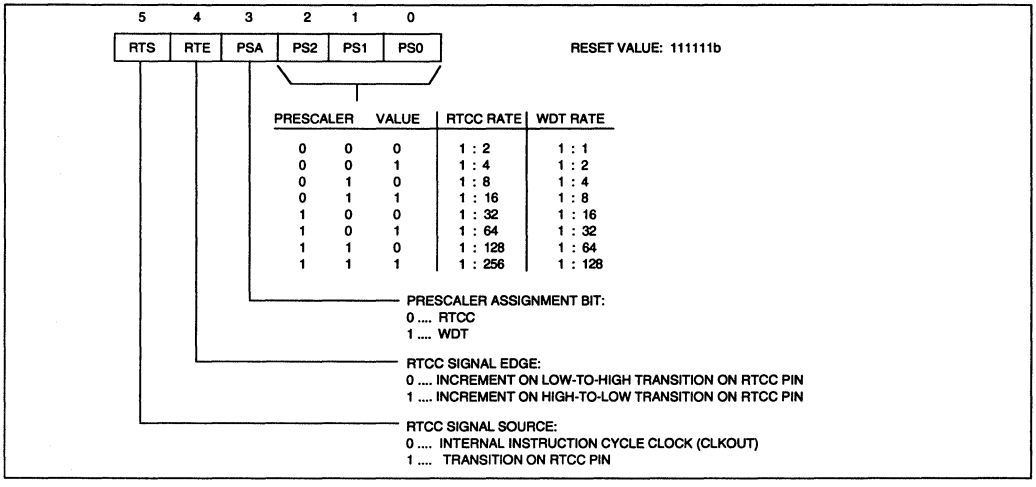
These registers are "write-only" and are set to all "ones" upon a RESET condition.

7.4 OPTION Prescaler/RTCC Option Register

Defines prescaler assignment (RTCC or WDT), prescaler value, signal source and signal edge for the RTCC. The OPTION register is "write-only" and is 6-bits wide.

By executing the "OPTION" instruction, the contents of the "W" register will be transferred to the option register. Upon a RESET condition, the option register is set to all "ones."

FIGURE 7.4.1 - OPTION REGISTER



8.0 RESET CONDITION

A RESET condition can be caused by applying power to the chip (power-up), pulling the MCLR input "low", or by a Watchdog Timer timeout. The device will stay in RESET as long as the Oscillator Start-up Timer (OST) is active or the MCLR input is "low."

The Oscillator Start-up Timer is activated as soon as MCLR input is sensed to be high. This implies that in case of power on reset with MCLR tied to VDD the OST starts from power-up. In case of a WDT timeout, it will start at the end of the time-out (since MCLR is high). In case of MCLR reset, the OST will start when MCLR goes high. The nominal OST time-out period is 18ms. See Section 13.0 for detailed information on OST and Power-On Reset.

During a RESET condition the state of the PIC16CR54 is defined as:

- The oscillator is running, or will be started (power-up or wake-up from SLEEP).
- All I/O port pins (RA0 - RA3, RB0 - RB7) are put into the high-impedance state by setting the "TRIS" registers to all "ones" (= input mode).
- The Program Counter is set to all "ones" (1FFh).
- The OPTION register is set to all "ones".
- The Watchdog Timer and its prescaler are cleared.
- The upper-three bits (page select bits) in the STATUS Register are cleared to "zero."
- "RC" devices only: The "CLKOUT" signal on the OSC2 pin is held at a"low" level.

9.0 PRESCALER

An 8-bit counter is available as a prescaler for the RTCC, or as a post-scaler for the Watchdog Ttimer, respectively (Figure 9.0.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the RTCC and the watchdog timer. Thus, a prescaler assignment for the RTCC means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS0-PS2 bits in the OPTION register determine the prescaler assignment and pre-scale ratio.

When assigned to the RTCC, all instructions writing to the RTCC (e.g. CLRF RTCC, MOVWF RTCC, BSF RTCC, x ....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer.

9.1 Switching Prescaler Assignment

CHANGING PRESCALER FROM RTCC TO WDT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence must be executed when changing the prescaler assignment from RTCC to WDT:

```
1. MOVLW  B'xx0x0xxx'   ; Select internal clock and select new
2. OPTION               ; prescaler value. If new prescale value
                        ; is = '000' or '001', then select any other
                        ; prescale value temporarily.
3. CLRF 1               ; Clear RTCC and prescaler.
4. MOVLW  B'xxxx1xxx'   ; Select WDT, do not change prescale
                        ; value.
5. OPTION               ;
6. CLRWDT               ; Clears WDT and prescaler.
7. MOVLW  B'xxxx1xxx'   ; Select new prescale value.
8. OPTION               ;
```

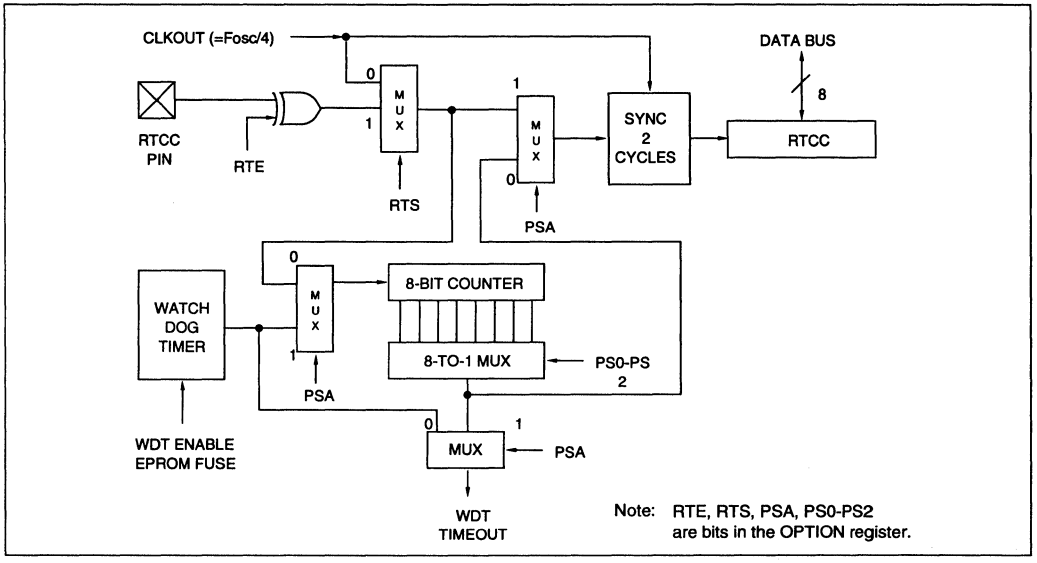
Steps 1 and 2 are only required if an external RTCC source is used. Steps 7 and 8 are necessary only if the desired prescale value is '000'or '001'.

CHANGING PRESCALER FROM WDT TO RTCC

To change prescaler from WDT to RTCC use the following sequence:

```
1. CLRWDT               ; Clear WDT and prescaler
2. MOVLW  B'xxxx0xxx'   ; Select RTCC, new prescale value
                        ; and clock source
3. OPTION               ;
```

FIGURE 9.0.1 - BLOCK DIAGRAM RTCC/WDT PRESCALER



10.0 BASIC INSTRUCTION SET SUMMARY

Each PIC16CR54 instruction is a 12-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CR54 instruction set summary in Table 10.0.1 lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC16CR54 file registers is to be utilized by the instruction.

The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an 8- or 9-bit constant or literal value.

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Notes to Table 10.0.1

Note 1: The 9th bit of the program counter will be forced to a "zero" by any instruction that writes to the PC except for GOTO (e.g. CALL, MOVWF PC etc.). See Section 4.3 for details.

Note 2: When an I/O register is modified as a function of itself (e.g. MOVF PORTB,1), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as input, and it is driven low by an external device, the data latch will be written back with a '0'.

Note 3: The instruction "TRIS f", where f = 5 or 6 causes the contents of the W register to be written to the tristate latches of the specified file (port). A "one" forces the pin to a high impedance state and disables the output buffers.

Note 4: If this instruction is executed on file register RTCC (and, where applicable, d=1), the prescaler will be cleared if assigned to the RTCC.

TABLE 10.0.1 - INSTRUCTION SET SUMMARY

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4 - 0)
OPCODE	d	f(FILE #)

d = 0 for destination W
d = 1 for destination f

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0001 11df ffff 1cf	Add W and f	**ADDWF**	f, d	W + f → d	C,DC,Z	1,2,4
0001 01df ffff 14f	AND W and f	**ANDWF**	f, d	W & f → d	Z	2,4
0000 011f ffff 06f	Clear f	**CLRF**	f	0 → f	Z	4
0000 0100 0000 040	Clear W	**CLRW**	-	0 → W	Z	
0010 01df ffff 24f	Complement f	**COMF**	f, d	$\bar{f}$ → d	Z	2,4
0000 11df ffff 0cf	Decrement f	**DECF**	f, d	f -1 → d	Z	2,4
0010 11df ffff 2cf	Decrement f,Skip if Zero	**DECFSZ**	f, d	f - 1 → d, skip if zero	None	2,4
0010 10df ffff 28f	Increment f	**INCF**	f, d	f + 1 → d	Z	2,4
0011 11df ffff 3cf	Increment f,Skip if zero	**INCFSZ**	f, d	f + 1 → d, skip if zero	None	2,4
0001 00df ffff 10f	Inclusive OR W and f	**IORWF**	f, d	W v f → d	Z	2,4
0010 00df ffff 20f	Move f	**MOVF**	f, d	f → d	Z	2,4
0000 001f ffff 02f	Move W to f	**MOVWF**	f	W → f	None	1,4
0000 0000 0000 000	No Operation	**NOP**	-	-	None	
0011 01df ffff 34f	Rotate left f	**RLF**	f, d	f(n) → d(n+1), C → d(0), f(7) → C	C	2,4
0011 00df ffff 30f	Rotate right f	**RRF**	f, d	f(n) → d(n-1), C → d(7), f(0) → C	C	2,4
0000 10df ffff 08f	Subtract W from f	**SUBWF**	f, d	f - W → d [f + $\overline{W}$ + 1 → d]	C,DC,Z	1,2,4
0011 10df ffff 38f	Swap halves f	**SWAPF**	f, d	f(0-3) ↔ f(4-7) → d	None	2,4
0001 10df ffff 18f	Exclusive OR W and f	**XORWF**	f, d	W ⊕ f → d	Z	2,4

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4 - 0)
OPCODE	b(BIT #)	f(FILE #)

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0100 bbbf ffff 4bf	Bit Clear f	**BCF**	f, b	0 → f(b)	None	2,4
0101 bbbf ffff 5bf	Bit Set f	**BSF**	f, b	1 → f(b)	None	2,4
0110 bbbf ffff 6bf	Bit Test f,Skip if Clear	**BTFSC**	f, b	Test bit (b) in file (f): Skip if clear	None	
0111 bbbf ffff 7bf	Bit Test f, Skip if Set	**BTFSS**	f, b	Test bit (b) in file (f): Skip if set	None	

LITERAL AND CONTROL OPERATIONS

(11-8)	(7 - 0)
OPCODE	k (LITERAL)

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
1110 kkkk kkkk Ekk	AND Literal and W	**ANDLW**	k	k & W→ W	Z	
1001 kkkk kkkk 9kk	Call subroutine	**CALL**	k	PC + 1 → Stack, k → PC	None	1
0000 0000 0100 004	Clear Watchdog timer	**CLRWDT**	-	0 → WDT (and prescaler, if assigned)	TO, PD	
101k kkkk kkkk Akk	Go To address (k is 9 bit)	**GOTO**	k	k → PC (9 bits)	None	
1101 kkkk kkkk Dkk	Incl. OR Literal and W	**IORLW**	k	k v W → W	Z	
1100 kkkk kkkk Ckk	Move Literal to W	**MOVLW**	k	k → W	None	
0000 0000 0010 002	Load OPTION register	**OPTION**	-	W → OPTION register	None	
1000 kkkk kkkk 8kk	Return,place Literal in W	**RETLW**	k	k → W, Stack → PC	None	
0000 0000 0011 003	Go into standby mode	**SLEEP**	-	0 → WDT, stop oscillator	TO, PD	
0000 0000 0fff 00f	Tristate port f	**TRIS**	f	W→ I/O control register f	None	3
1111 kkkk kkkk Fkk	Excl. OR Literal and W	**XORLW**	k	k ⊕ W → W	Z	

Notes: See previous page

11.0 WATCHDOG TIMER (WDT)

The Watchdog Timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1/OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by specifying the WDT mask option.

11.1 WDT Period

The WDT has a nominal time-out period of 18ms (with no prescaler). The time-out period varies with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, timeout periods up to 2.5 seconds can be realized.

The "CLRWDT" and "SLEEP" instructions clear the WDT and the prescaler count, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit, $\overline{TO}$, in the STATUS register, will be cleared upon a Watchdog Timer timeout.

The WDT period is a function of the supply voltage, operating temperature, and will also vary from unit to unit due to variations in the manufacturing process. Please refer to graphs in Section 18.0 and DC specs for more details.

11.2 WDT Programming Considerations:

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

12.0 OSCILLATOR CIRCUITS

12.1 Oscillator Types

The PIC16CR54 series is available with four different oscillator options. Two bits in the configuration word select one of these four modes. The customer specifies the desired oscillator type along with the ROM pattern. The parts are tested for the specific oscillator type.

12.2 Crystal Oscillator

The PIC16CR54-XT, -HS, or LP needs a crystal or ceramic resonator connected to the OSC1 and OSC2 pins to establish oscillation (Figure 12.2.1). Note that the series resistor RS is only required for the "HS" oscillator.

12.3 RC Oscillator

For timing insensitive applications the "RC" oscillator option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation to due tolerance of external R and C components used. Figure 12.3.1 shows how the R/C combination is connected to the PIC16CR54. For Rext values below 2.2 kOhm, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 5 kOhm and 100 kOhm.

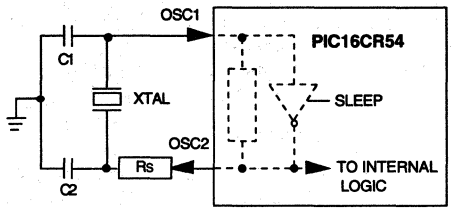
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See the tables in Section 18.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See graphs and tables in Section 18.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 2.2.1 for timing).

FIGURE 12.2.1 - CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP TYPES ONLY)



Rs is recommended for "HS" devices(100Ω < Rs < 1KΩ). RS may also be needed in XT mode for AT strip-out crystals to avoid overdriving. See Tables 12.2.1 and 12.2.2 for recommended values of C1, C2 and RS.

TABLE 12.2.1 - CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator frequencyf	Capacitor Range
XT	455 KHz	150 - 330 pF
	2.0 MHz	20 - 330 pF
	4.0 MHz	20 - 330 pF
HS	8.0 MHz	20 - 200 pF
	20 MHz	0 - 20 pF

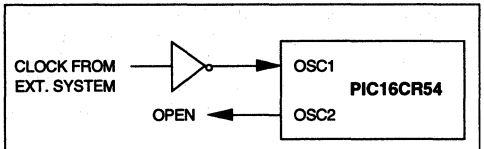
Higher capacitance increases stability of oscillation but also increases start-up time.

TABLE 12.2.2 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	15 pF	15 pF
	100 KHz	15 pF	15 pF
	200 KHz	0 - 15 pF	0 - 15 pF
XT	200 KHz	15 - 50 pF	15 - 50 pF
	100 KHz	15 - 30 pF	200 - 300 pF
	200 KHz	15 - 30 pF	100 - 200 pF
	455 KHz	15 - 30 pF	15 - 100 pF
	1 MHz	15 - 30 pF	15 - 30 pF
	2 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Higher capacitance increases stability of oscillator but also increases start-up time. These values are for design guidance only. RS may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

FIGURE 12.2.2 - EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP TYPES ONLY)



Note: Load on OSC2 must not exceed 15 pF for external clock operation.

FIGURE 12.3.1 - RC OSCILLATOR (RC TYPE ONLY)

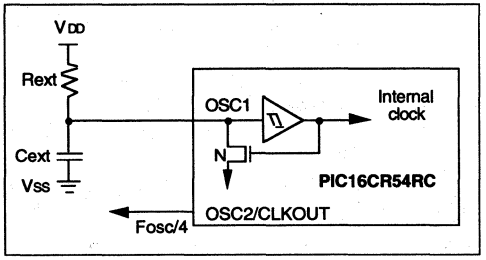
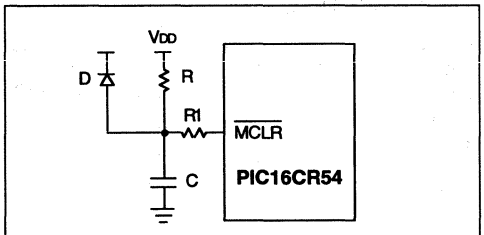


FIGURE 13.1.1 - EXTERNAL POWER ON RESET CIRCUIT



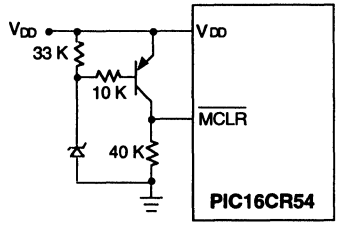
Notes:

1. External power on reset circuit is required only if VDD power-up slope is too slow or if a low frequency crystal oscillator is being used that need a long start-up time. The diode D helps discharge the capacitor quickly when VDD powers down.

2. R < 40 KΩ must be observed to make sure that voltage drop across R does not exceed 0.2 V (max leakage current spec on MCLR pin is 5 µA). A larger than 0.2 V drop across R may cause a VIH level violation on MCLR pin.

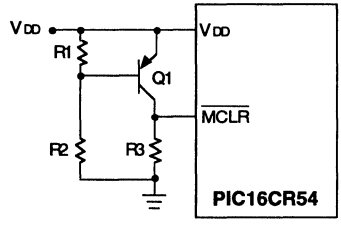
3. R1= 100Ω to 1KΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to ESD or EOS.

FIGURE 13.1.2 - BROWN OUT PROTECTION CIRCUIT



Notes:
1. This circuit will activate reset when VDD goes below (VZ + 0.7 V) where VZ = Zener voltage.

FIGURE 13.1.3 - BROWN OUT PROTECTION CIRCUIT



Notes:
1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$VDD \bullet \frac{R1}{R1 + R2} = 0.7\ V.$$

13.0 OSCILLATOR START-UP TIMER (OST)

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. An on-chip oscillator start-up timer is provided which keeps the device in a RESET condition for approximately 18ms after the voltage on the $\overline{MCLR}$ pin has reached a logic high (VIHMC) level. Thus, external RC networks connected to the $\overline{MCLR}$ input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The OST will also be triggered upon a watchdog timer timeout. This is particularly important for applications using the WDT to awake the PIC16CR54 from SLEEP mode automatically.

The OST is not adequate for low frequency crystals which require much longer than 18ms to start-up and stabilize.

13.1 Power-On Reset (POR)

The PIC16CR54 incorporates an on-chip Power-On Reset (POR) circuitry which provides internal chip reset for most power-up situations. To use this feature, the user merely needs to tie $\overline{MCLR}$ pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 13.1.4. The Power-On Reset circuit and the Oscillator Start-up Timer circuit are closely related. On power-up, the reset latch is set and the start-up timer (see Figure 13.1.4) are reset. The start-up timer begins counting once it detects $\overline{MCLR}$ to be high. After the timeout period, which is typically 18ms, it will reset the reset-latch and thus end the on-chip reset signal.

Figures 13.1.5 and 13.1.6 show two power-up situations with relatively fast rise time on VDD. In Figure 13.1.5, VDD is allowed to rise and stabilize before bringing $\overline{MCLR}$ high. The chip will actually come out of reset tOST ms after $\overline{MCLR}$ goes high. In Figure 13.1.6, the on chip Power-On Reset feature is being utilized ($\overline{MCLR}$ and VDD are tied together). The VDD is stable before the startup timer times out and there is no problem in getting a proper reset. Figure 13.1.7 depicts a potentially problematic situation where VDD rises too slowly. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is therefore not guaranteed to function correctly.

To summarize, the on-chip power-on reset is guaranteed to work if the rate of rise of VDD is no slower than 0.05 V/ms. It is also necessary that the VDD starts from 0V. The on-chip Power-On Reset is also not adequate for low frequency crystals which require much longer than 18ms to start-up and stabilize. For such situations, we recommend that external RC circuits are used for longer Power-On Reset.

FIGURE 13.1.4 - SIMPLIFIED POWER ON RESET BLOCK DIAGRAM

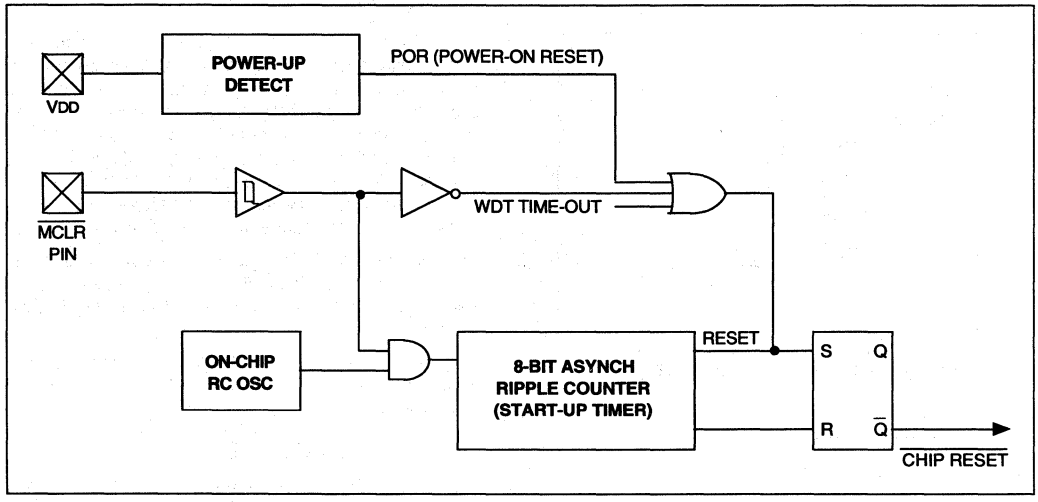


FIGURE 13.1.5 - USING EXTERNAL RESET INPUT

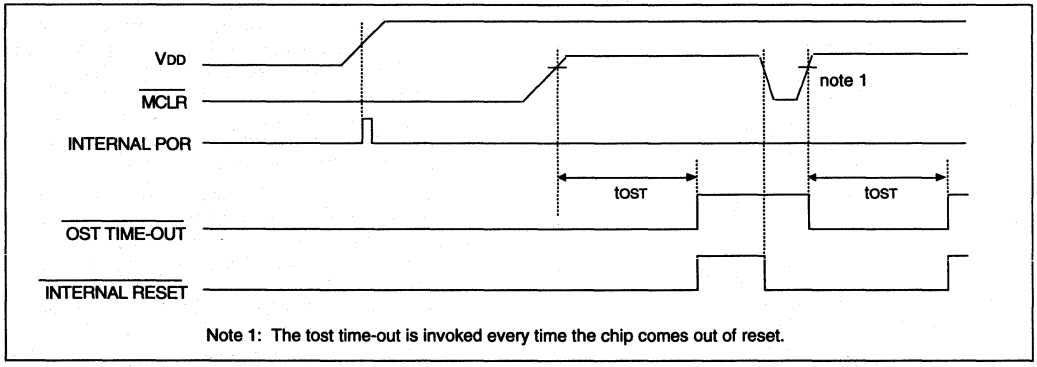


FIGURE 13.1.6 - USING ON-CHIP POR (FAST VDD RISE TIME)

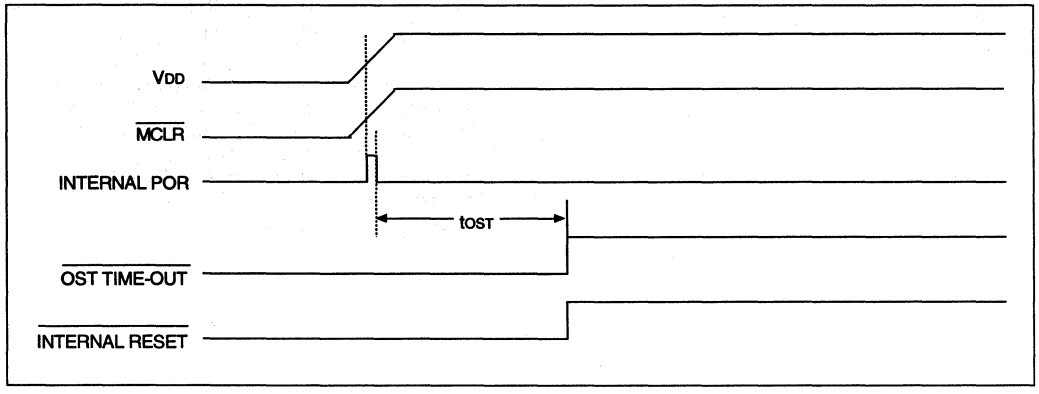
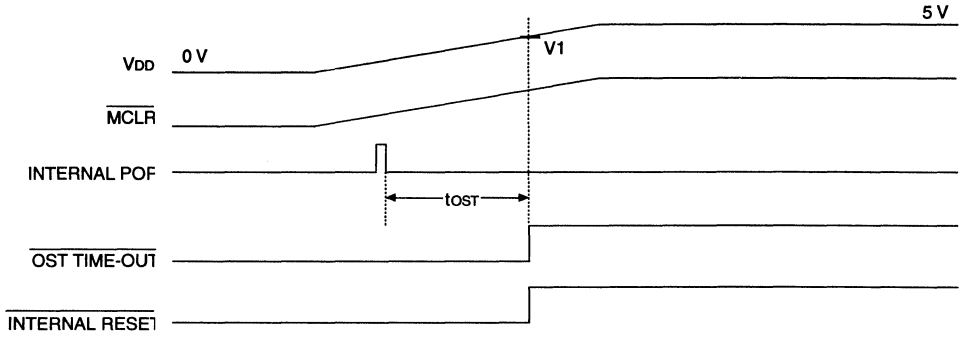


FIGURE 13.1.7 - USING ON-CHIP POR (SLOW VDD RISE TIME)



When VDD rises slowly, the internal time-out period expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1≥ VDDMIN.

14.0 POWER DOWN MODE (SLEEP)

The power down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the bit $\overline{PD}$ in the STATUS register is cleared, the $\overline{TO}$ bit is set and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low or hi-impedence).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are in the High-Z mode should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC pin should also be at VDD or Vss for lowest current consumption.

The $\overline{MCLR}$ pin must be at VIHMC.

14.1 Wake-Up

The device can be awakened by a Watchdog Timer timeout (if it is enabled) or an externally applied "low" pulse at the $\overline{MCLR}$ pin. In both cases the PIC16CR54 will stay in RESET mode for one Oscillator Start-up Timer period (triggered from rising edge on $\overline{MCLR}$ or WDT timeout) before normal program execution resumes.

The $\overline{PD}$ bit in the STATUS register, which is set to one during power-on, but cleared by the "SLEEP" command, can be used to determine if the processor was powered up or awakened from the power down mode (Table 4.5.1.2). The $\overline{TO}$ bit in the Status register can be used to determine, if the "wake up" was caused by an external $\overline{MCLR}$ signal or a Watchdog Timer timeout.

NOTE: Some applications may require external R/C networks on the $\overline{MCLR}$ pin in order to allow for oscillator start-up times longer than one OST period. In this case, a WDT wake up from power down mode is not recommended, because a RESET generated by a WDT time out does not discharge the external capacitor, and the PIC16CR54 will be in RESET only for the oscillator start-up timer period.

15.0 CONFIGURATION FUSES

The configuration word consists of four ROM fuses.

Two are for the selection of the oscillator type, one is the Watchdog Timer enable fuse, and one is the code protection fuse.

The customer makes the selection for these and the parts are tested accordingly. The packages are marked with the suffixes "XT", "RC", "HS" or "LP" following the part number to identify the oscillator type and operating range.

15.1 Customer ID Code

The PIC16CR54 has four special ROM locations which are not part of the normal program memory. These locations are available to the user to store an Identifier (ID) code, checksum or other informative data. They cannot be accessed during normal program execution but can be read out using any programmer that supports the PIC16C5X, such as PRO MATE™.

15.2 Code Protection

The code in the ROM can be protected by selecting the code protection fuse to be "0".

When code protected, the contents of the program ROM cannot be read out in a way that the program code can be reconstructed. The factory can verify every bit in a code protected ROM through a special ROM-verify test mode. In this test mode data is presented to the chip for every ROM location and a pass/fail bit at the end of the sequence indicates if the ROM matched the externally supplied pattern sequence. This mode does not output the ROM pattern and therefore does not compromise code security.

Another way to verify a code protected ROM without supplying the actual code is as follows:

When code protected, verifying any program memory location will read a scrambled output which looks like "00000000XXXX" (binary) where X is 1 or 0. To verify a code protected device, follow this procedure:

a. First, read in a code-protected device known to be good into a file. The data will look scrambled.
b. Verify any code-protected PIC16CR54 against this file.

16.0 ELECTRICAL CHARACTERISTICS

16.1 Absolute Maximum Ratings*

Ambient temperature under bias ..... -55°C to +125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss
(except VDD and MCLR) ..... -0.6V to VDD +0.6V
Voltage on VDD with respect to Vss ..... 0 to +7.5 V
Voltage on MCLR with respect to Vss
(Note 2) ..... 0 to +14 V
Total power Dissipation (Note 1) ..... 800 mW
Max. Current out of Vss pin ..... 150 mA
Max. Current into VDD pin ..... 50 mA
Max. Current into an input pin ..... ±500 µA
Input clamp current, IIK (VI<0 or VI>VDD) ..... ±20 mA
Output clamp current, IOK (V0<0 or V0>VDD) . ±20 mA
Max. Output Current sinked by any I/O pin ..... 25 mA
Max. Output Current sourced by any I/O pin .... 20 mA
Max. Output Current sourced by a single
I/O port (Port A or B) ..... 40 mA
Max. Output Current sinked by a single
I/O port (Port A or B) 50mA

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
$Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum\{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

2. Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.

16.2 Pin Descriptions

Name	Function	Description
RA0 - RA3	I/O PORT A	4 input/output lines.
RB0 - RB7	I/O PORT B	8 input/output lines.
RTCC	Real Time Clock/Counter	Schmitt Trigger Input. Clock input to RTCC register. Must be tied to Vss or VDD if not in use to avoid unintended entering of test modes and to reduce current consumption.
MCLR	Master Clear	Schmitt Trigger Input. A "Low" voltage on this input generates a RESET condition for the PIC16CR54 microcontroller. A rising voltage triggers the on-chip oscillator start-up timer which keeps the chip in RESET mode for about 18ms. This input must be tied directly, or via a pull-up resistor, to VDD.
OSC1/CLKIN	Oscillator (input)	"XT", "HS" and "LP" devices: Input terminal for crystal, ceramic resonator, or external clock generator. "RC" devices : Driver terminal for external RC combination to establish oscillation.
OSC2/CLKOUT	Oscillator (output)	For "XT", "HS" and "LP" devices: Output terminal for crystal and ceramic resonator. Do not connect any other load to this output. Leave open if external clock generator is used. For "RC" devices : A "CLKOUT" signal with a frequency of 1/4 Fosc1 is put out on this pin.
VDD	Power supply	
Vss	Ground	
N/C	No (internal) Connection	

16.3 DC CHARACTERISTICS: PIC16CR54-RC, XT, HS, LP (Commercial) PIC16CR54-RC, XT, HS, LP (Industrial)

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions Operating temperature -40 ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial					
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage						
PIC16CR54-XT, RC	VDD	2.5		6.25	V	Fosc = DC to 4 MHz
PIC16CR54-HS		4.5		5.5	V	Fosc = DC to 20 MHz
PIC16CR54-LP		2.0		6.25	V	Fosc = DC to 200 KHz
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD starting voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power-on-reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power-on-reset
Supply Current (Note 2)						
PIC16CR54-XT, RC (Note 5)	IDD		2.0	3.6	mA	Fosc = 4 MHz, VDD = 6.0V
			0.8	1.8	mA	Fosc = 4 MHz, VDD = 3.0V
			90	350	µA	Fosc = 200 KHz, VDD = 2.5V
PIC16CR54-HS			3.8	10	mA	Fosc = 8 MHz, VDD = 5.5V
			9.0	20.0	mA	Fosc = 20 MHz, VDD = 5.5V
PIC16CR54-LP			10.0	20.0	µA	Fosc = 32 KHz, VDD = 2.0V
				70.0	µA	Fosc = 32 KHz, VDD = 6.0V
Power Down Current Commercial (Note 4)						
PIC16CR54	IPD		1	6	µA	VDD = 2.5V, WDT disabled
			2	8*	µA	VDD = 4.0V, WDT disabled
			3	15	µA	VDD = 6.0V, WDT disabled
			5	25	µA	VDD = 6.0V, WDT enabled
Power Down Current Industrial (Note 4)						
PIC16CR54	IPD		1	8	µA	VDD = 2.5V, WDT disabled
			2	10*	µA	VDD = 4.0V, WDT disabled
			3	20*	µA	VDD = 4.0V, WDT enabled
			3	18	µA	VDD = 6.0V, WDT disabled
			5	45	µA	VDD = 6.0V, WDT enabled

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
a) The test conditions for all IDD measurements in active operation mode are: OSC1= external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. It is measured in SLEEP with all I/O pins in hi-impedence state and connected to VDD or VSS.

Note 5: In RC mode does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.4 DC CHARACTERISTICS: PIC16CR54E-RC, XT, HS, LP (Automotive)

DC CHARACTERISTICS, POWER SUPPLY PINS		Standard Operating Conditions Operating temperature -40 ≤ TA ≤ +125°C, unless otherwise stated Operating voltage VDD = 3.5V to 5.5V unless otherwise stated				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage						
PIC16CR54-XT, RC	VDD	3.25		6.0	V	Fosc = DC to 4 MHz
PIC16CR54-HS		4.5		5.5	V	Fosc = DC to 20 MHz
PIC16CR54-LP		2.5		6.0	V	Fosc = DC to 200 KHz
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on reset
Supply Current (Note 2)						
PIC16CR54-XT	IDD		1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
PIC16CR54-RC (Note 5)			1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
PIC16CR54-HS			4.8	10.0	mA	Fosc = 10 MHz, VDD = 5.5V
			9.0	20.0	mA	Fosc = 16 MHz, VDD = 5.5V
PIC16C5X-LP			25	55	µA	Fosc = 32 KHz, VDD = 3.25V, WDT disabled
Power Down Current (Note 4)						
PIC16CR54	IPD		5	22	µA	VDD = 3.25V, WDT enabled
			0.8	18	µA	VDD = 3.25V, WDT disabled

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
OSC1= external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.5 DC CHARACTERISTICS: PIC16CR54-RC, XT, HS, LP (Commercial) PIC16CR54-RC, XT, HS, LP (Industrial)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as in table 16.3 unless otherwise stated				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Input Low Voltage						
I/O ports	VIL	VSS		0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt trigger)		VSS		0.15 VDD	V	
RTCC (Schmitt trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt trigger)		VSS		0.15 VDD	V	PIC16CR54RC only (Note 5)
OSC1		VSS		0.15 VDD	V	PIC16CR54-XT, HS, LP
Input High Voltage						
I/O ports	VIH	2.0		VDD	V	VDD = 3.0V to 5.5V (Note 6)
		0.6 VDD		VDD	V	Full VDD range (Note 6)
MCLR (Schmitt trigger)		0.85 VDD		VDD	V	
RTCC (Schmitt trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt trigger)		0.85 VDD		VDD	V	PIC16CR54-RC only (Note 5)
OSC1		0.85 VDD		VDD	V	PIC16CR54-XT, HS, LP
Input Leakage Current (Notes 3, 4)						**For VDD ≤ 5.5V**
I/O ports	IIL	-1		+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		-5			µA	VPIN = VSS + 0.25V
MCLR			0.5	+5	µA	VPIN = VDD
RTCC		-3	0.5	+5	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, PIC16CR54-XT, HS, LP
Output Low Voltage						
I/O Ports	VOL			0.5	V	IOL = 10 mA, VDD = 6.0V
OSC2/CLKOUT				0.5	V	IOL = 1.9 mA, VDD = 6.0V
Output High Voltage						
I/O Ports (Note 4, 5)	VOH	VDD-0.5V			V	IOH = -4.0 mA, VDD = 6.0V
OSC2/CLKOUT		VDD-0.5V			V	IOH = -0.8 mA, VDD = 6.0V

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : For PIC16CR54-RC devices, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16CR54 be driven with external clock in RC mode.

Note 6: The user may use the better of the two specs. TTL level is guaranteed in 3.0V to 5.5V range.

16.6 DC CHARACTERISTICS: PIC16CR54-RC, XT, HS, LP (Automotive)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY		Standard Operating Conditions (unless otherwise stated) Operating temperature -40 < TA < +125°C Operating voltage VDD range as described in DC spec tables 16.3 and 16.4				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Input Low Voltage						
I/O ports	VIL	VSS		0.15 VDD	V	Pin at hi-impedance
$\overline{\text{MCLR}}$ (Schmitt trigger)		VSS		0.15 VDD	V	
RTCC (Schmitt trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt trigger)		VSS		0.15 VDD	V	PIC16CR54-RC only (Note 5)
OSC1		VSS		0.3 VDD	V	PIC16CR54-XT, HS, LP
Input High Voltage						
I/O ports	VIH	0.45 VDD		VDD	V	For all VDD (Note 6)
		2.0		VDD	V	4.0 V < VDD ≤ 5.5 V (Note 6)
		0.36 VDD		VDD	V	VDD > 5.5 V
$\overline{\text{MCLR}}$ (Schmitt trigger)		0.85 VDD		VDD	V	
RTCC (Schmitt trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt trigger)		0.85 VDD		VDD	V	PIC16CR54-RC only (Note 5)
OSC1		0.7 VDD		VDD	V	PIC16CR54-XT, HS, LP
Input Leakage Current (Notes 3, 4)						**For VDD ≤ 5.5V**
I/O ports	IIL	-1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{\text{MCLR}}$		-5			µA	VPIN = VSS + 0.25V
$\overline{\text{MCLR}}$			0.5	+5	µA	VPIN = VDD
RTCC		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, PIC16CR54-XT, HS, LP
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT (PIC16CR54-RC)				0.6	V	IOL = 1.6 mA, VDD = 4.5V
Output High Voltage						
I/O Ports (Note 4)	VOH	VDD-0.7			V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT (PIC16CR54-RC)		VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : For PIC16CR54-RC devices, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16CR54 be driven with external clock in RC mode.

Note 6: The user may use better of the two specifications.

16.7 AC CHARACTERISTICS: PIC16CR54-RC, XT, HS, LP (Commercial) PIC16CR54-RC, XT, HS, LP (Industrial) PIC16CR54-RC, XT, HS, LP (Automotive)

AC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature T_A = -40°C to +85°C (industrial),
T_A = -40°C to +125°C (automotive) and 0°C ≤ T_A ≤ +70°C (commercial)
Operating voltage V_{DD} range as described in DC spec tables 16.3 and 16.4

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Oscillator Frequency (Note 2)	FOSC	DC 0.1 4 DC		4.0 4 20 200	MHz MHz MHz KHz	RC mode, V_{DD} = 2.5 to 6.25V XT mode, V_{DD} = 2.5 to 6.25V HS mode, V_{DD} = 4.5 to 5.5V LP mode, V_{DD} = 2.0 to 6.25V
Instruction Cycle Time	TCY		4/Fosc			
External Clock in Timing (Note 4)						
Clock in High or Low Time						
XT oscillator type	TCKHLXT	50*			ns	
LP oscillator type	TCKHLLP	2*			µs	
HS oscillator type	TCKHLHS	20*			ns	
Clock in Rise or Fall Time						
XT oscillator type	TCKRFXT	25*			ns	
LP oscillator type	TCKRFLP	50*			ns	
HS oscillator type	TCKRFHS	25*			ns	
RESET Timing						
MCLR Pulse Width (low)	TMCL	100*			ns	
RTCC Input Timing, No Prescaler						
RTCC High Pulse Width	TRTH	0.5 TCY+ 20*			ns	Note 3
RTCC Low Pulse Width	TRTL	0.5 TCY+ 20*			ns	Note 3
RTCC Input Timing, With Prescaler						
RTCC High Pulse Width	TRTH	10*			ns	Note 3
RTCC Low Pulse Width	TRTL	10*			ns	Note 3
RTCC Period	TRTP	$\frac{T_{CY}+40}{N}$ *			ns	Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Timeout Period (No Prescaler)	TWDT	7*	18	30*	ms	V_{DD} = 5V, -40°C to 85°C
Oscillation Start-up Timer Period	TOST	7*	18	30*	ms	V_{DD} = 5V, -40°C to 85°C
I/O Timing						
I/O Pin Input Valid Before CLKOUT↑ (RC Mode)	TDS	0.25 TCY+ 30*			ns	
I/O Pin Input Hold After CLKOUT↑ (RC Mode)	TDH	0*			ns	
I/O Pin Output Valid After CLKOUT↓ (RC Mode)	TPD			40*	ns	
Capacitive Loading Specs on Output Pins						
OSC2	COSC2			15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
All I/O pins and OSC2 (in RC mode)	CIO			50	pF	

* Based on characterization, but not tested.

(Notes on next page)

NOTES TO AC CHARACTERISTICS: PIC16CR54-RC, XT, HS, LP (COMMERCIAL) PIC16CR54-RC, XT, HS, LP (INDUSTRIAL)

1. Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.
2. Instruction cycle period (Tcy) equals four times the input oscillator time base period.
   All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
   When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.
3. For a detailed explanation of RTCC input clock requirements see Section 4.2.1.
4. Clock-in high time is the duration for which clock input is at VIHOSC or higher.
   Clock-in low time is the duration for which clock input is at VILOSC or lower.

2

16.8 Electrical Structure of Pins

FIGURE 16.8.1 - ELECTRICAL STRUCTURE OF I/O PINS (RA, RB)

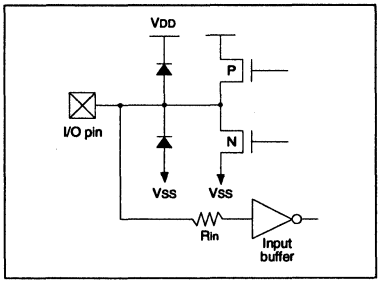
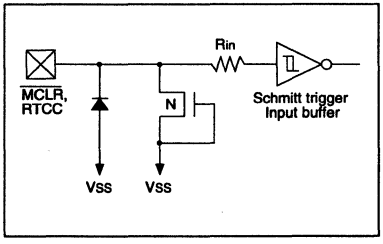


FIGURE 16.8.2 - ELECTRICAL STRUCTURE OF MCLR AND RTCC PINS



17.0 TIMING DIAGRAMS

FIGURE 17.0.1 - RTCC TIMING

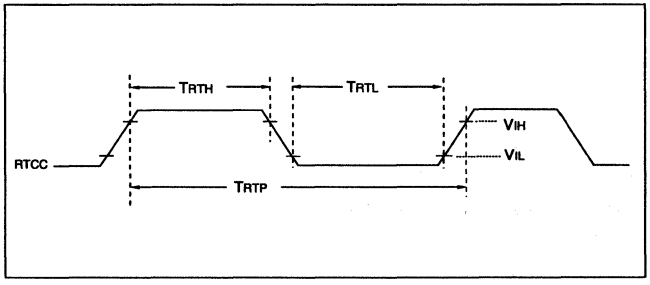
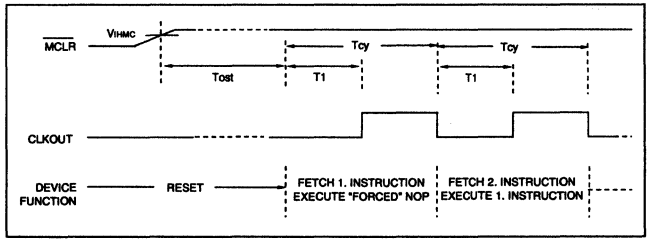
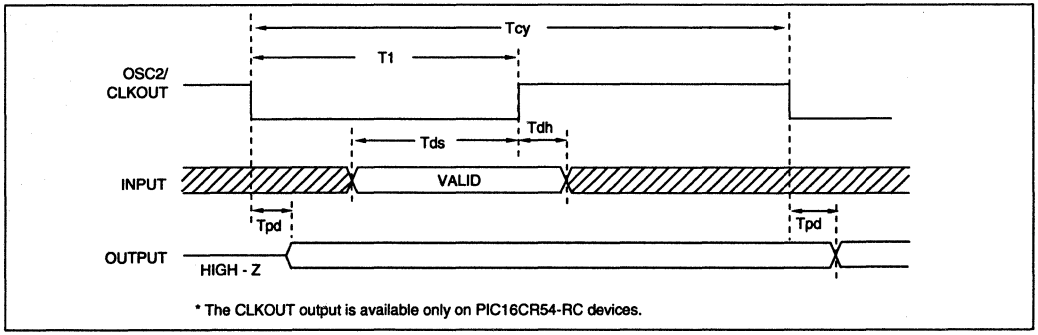


FIGURE 17.0.2 - OSCILLATOR START-UP TIMING (PIC16CR54RC)



Note to figures 16.8.1 and 16.8.2: The diodes and the grounded gate (or output driver) NMOS device are carefully designed to protect against ESD (Electrostatic discharge) and EOS (Electrical overstress). Rin is a small resistance to further protect the input buffer from ESD.

FIGURE 17.0.3 - INPUT/OUTPUT TIMING FOR I/O PORTS (PIC16CR54RC*)



* The CLKOUT output is available only on PIC16CR54-RC devices.

18.0 DC AND AC CHARACTERISTICS GRAPHS/TABLES

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected from units from different lots over a period of time. 'Typical' represents the mean of the distribution while 'max' and 'min' represents (mean + 3s) and (mean - 3s) respectively where s is standard deviation.

FIGURE 18.0.1 - TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

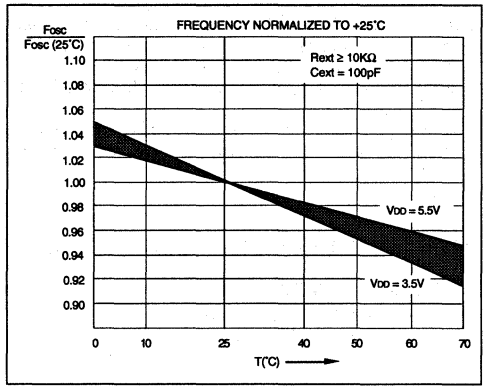
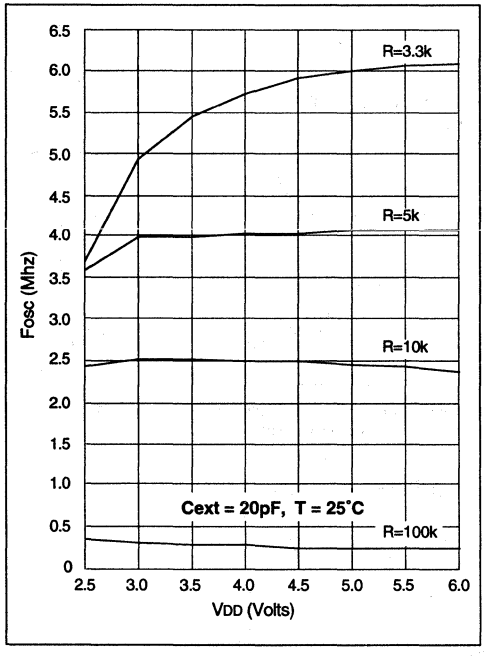
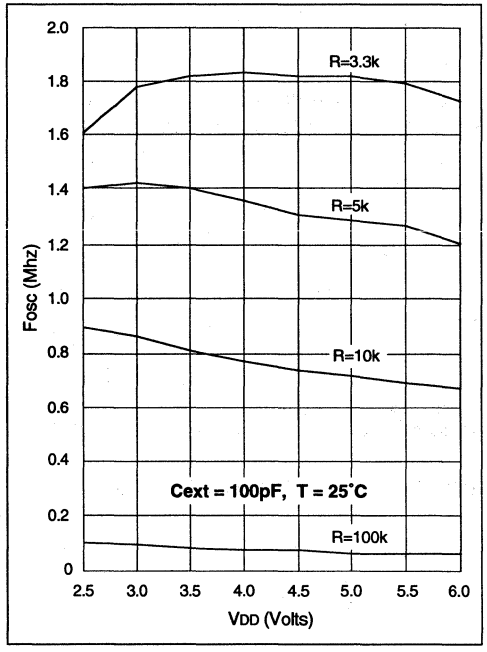


FIGURE 18.0.2 - TYPICAL RC OSCILLATOR FREQUENCY vs. VDD*



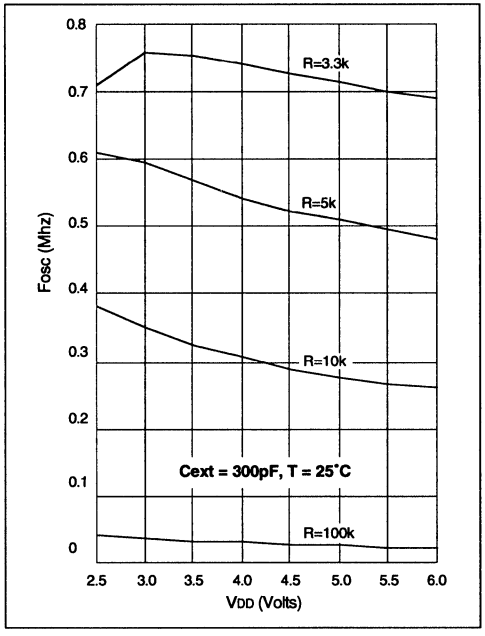
*Measured on PDIP Packages

FIGURE 18.0.3 - TYPICAL RC OSCILLATOR FREQUENCY vs. VDD*



*Measured on PDIP Packages

FIGURE 18.0.4 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD*



*Measured on PDIP Packages

TABLE 18.0.1 - RC OSCILLATOR FREQUENCY VARIATION FROM UNIT TO UNIT*

Cext	Rext	Average Fosc @ 5V, 25°C	
20pf	3.3k	6.02 MHz	± 28%
	5k	4.06 MHz	± 25%
	10k	2.47 MHz	± 24%
	100k	261 KHz	± 39%
100pf	3.3k	1.82 MHz	± 18%
	5k	1.28 MHz	± 21%
	10k	715 KHz	± 18%
	100k	72.4 KHz	± 28%
300pf	3.3k	712.4 KHz	± 14%
	5k	508 KHhz	± 13%
	10k	278 KHz	± 13%
	100k	28 KHz	± 23%

*Measured on PDIP Packages

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for full VDD range.

FIGURE 18.0.5 - TYPICAL IPD vs VDD WATCHDOG TIMER ENABLED 25°C

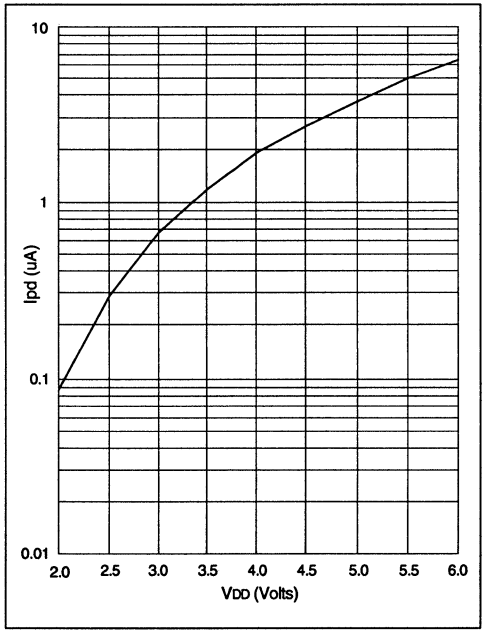


FIGURE 18.0.6 - MAXIMUM IPD vs VDD WATCHDOG TIMER ENABLED

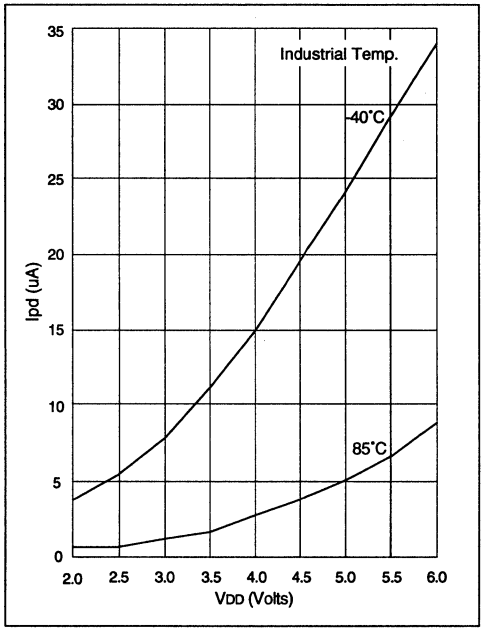


FIGURE 18.0.7 - VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs VDD

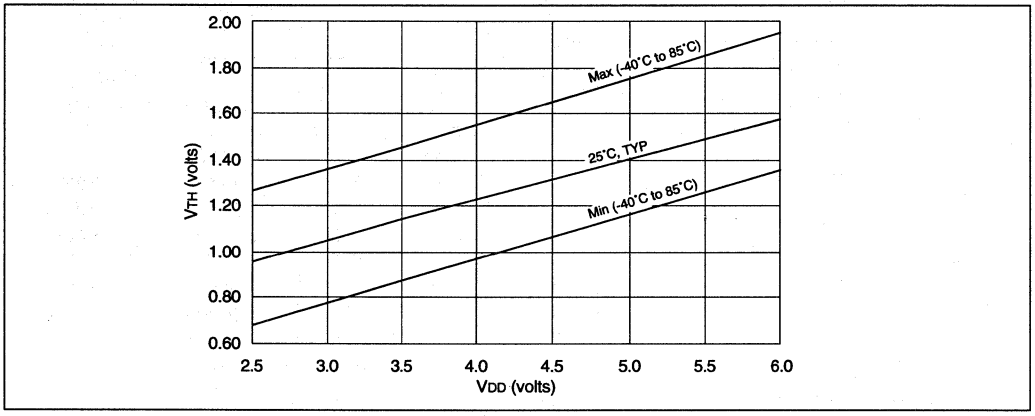
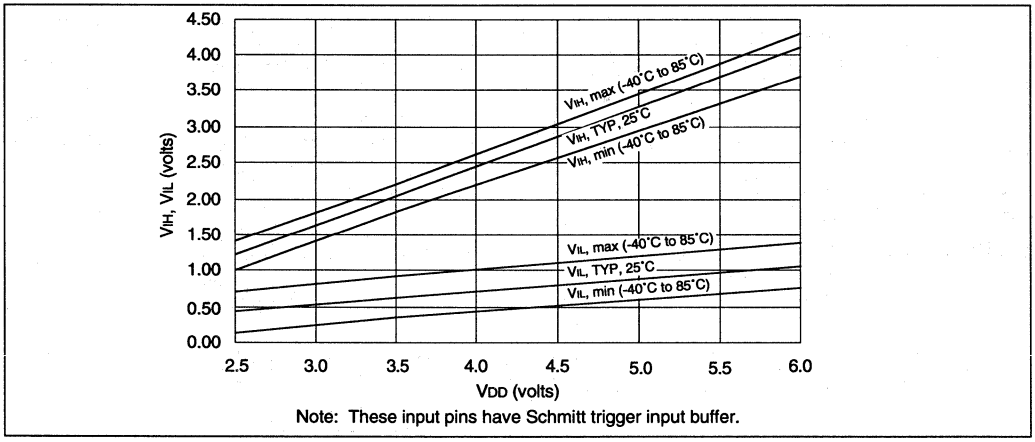


FIGURE 18.0.8 - VIH, VIL OF $\overline{MCLR}$, RTCC AND OSC1 (IN RC MODE) vs VDD



Note: These input pins have Schmitt trigger input buffer.

FIGURE 18.0.9 - VTH, (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs VDD

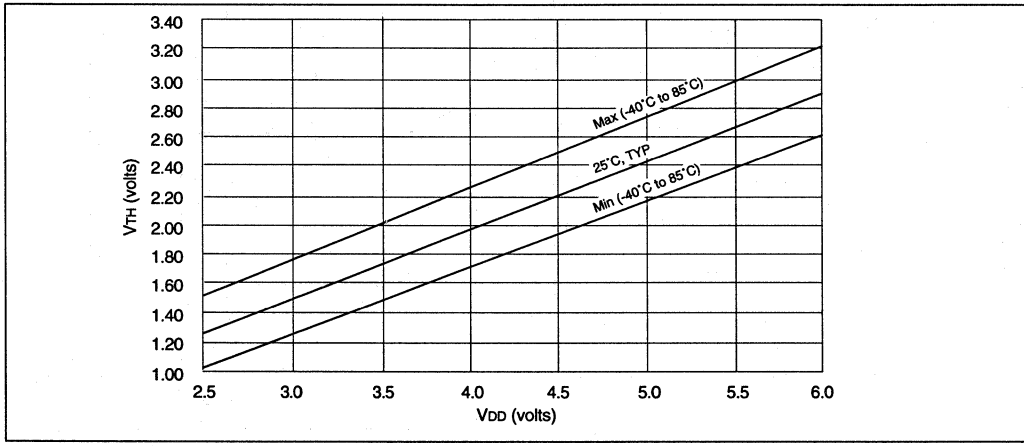


FIGURE 18.0.10 - TYPICAL IDD vs FREQ (EXT CLOCK, 25°C)

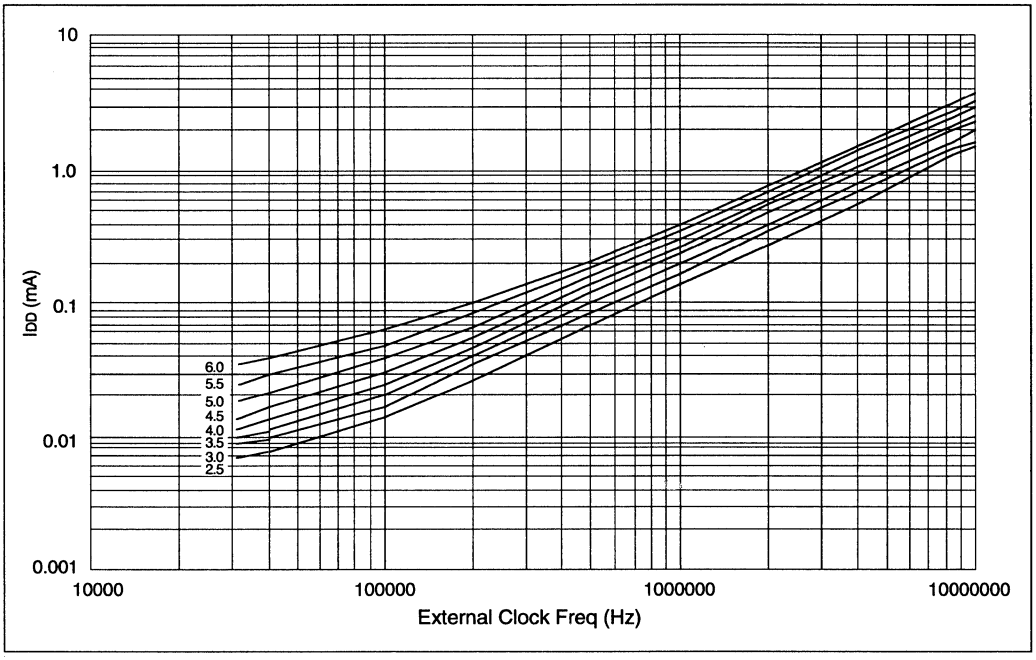


FIGURE 18.0.11 - MAXIMUM IDD vs FREQ (EXT CLOCK, -40°C TO +85°C)

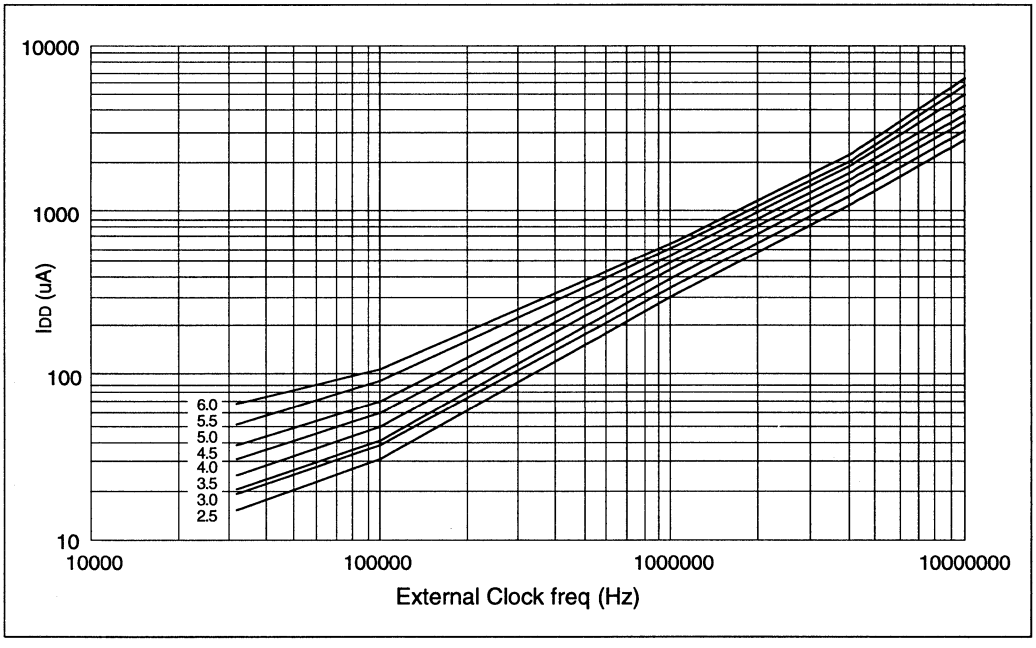


FIGURE 18.0.12 - WDT Timer Time-out Period vs VDD

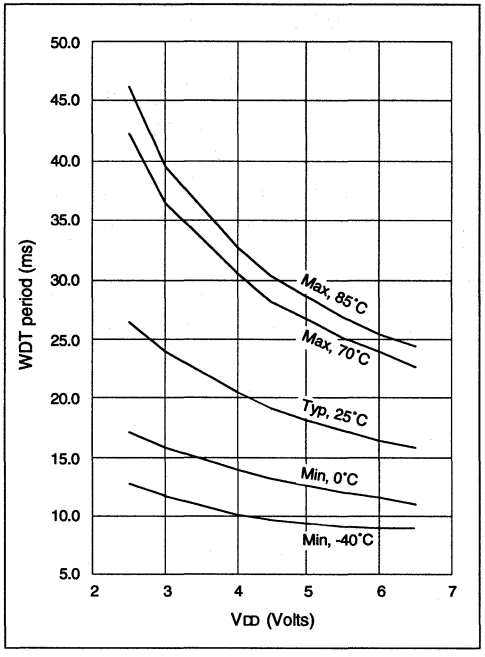


FIGURE 18.0.13 - Transconductance (gm) of HS Oscillator vs VDD

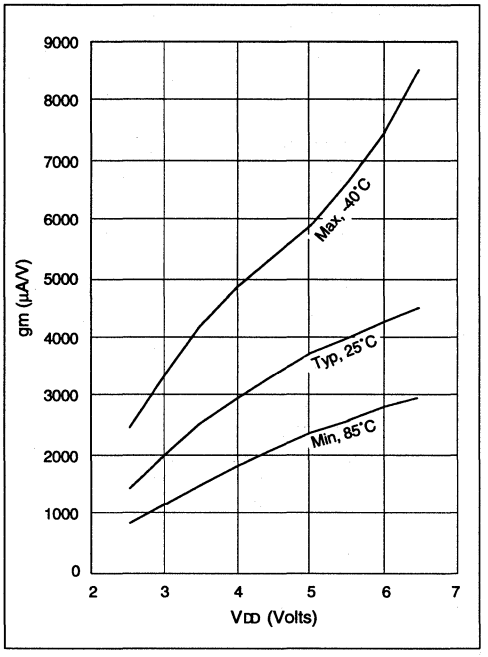


FIGURE 18.0.14 - Transconductance (gm) of LP Oscillator vs VDD

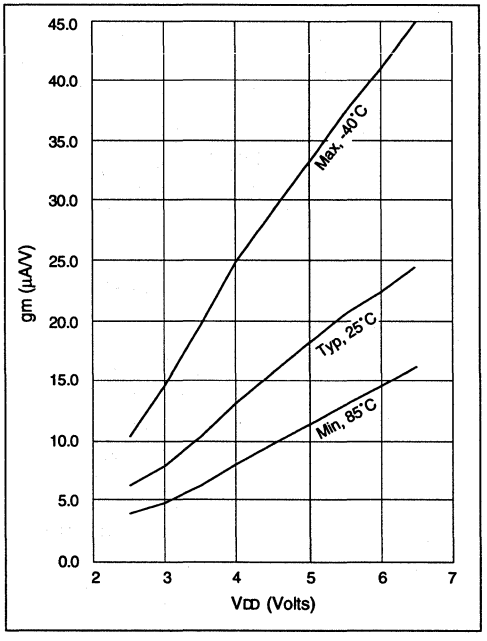


FIGURE 18.0.15 - Transconductance (gm) of XT Oscillator vs VDD

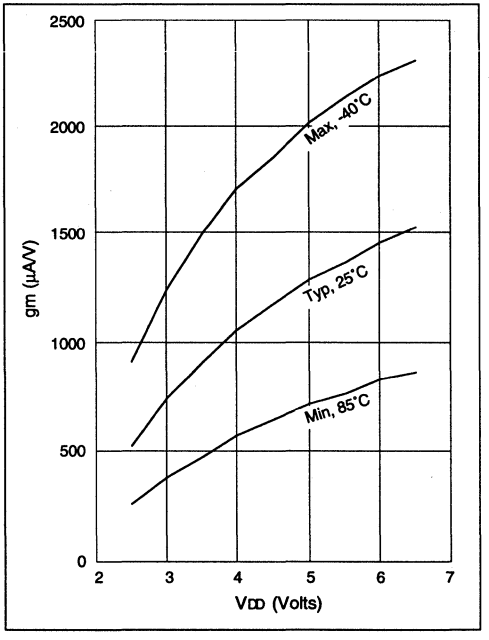


FIGURE 18.0.16 - IOH vs VOH, VDD = 3V

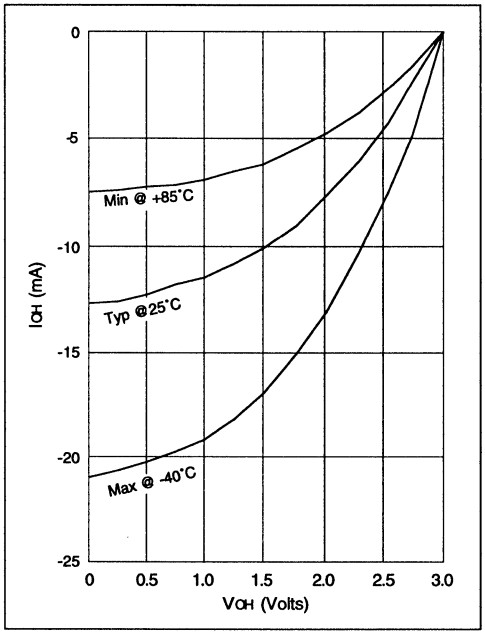


FIGURE 18.0.17 - IOH vs VOH, VDD = 5V

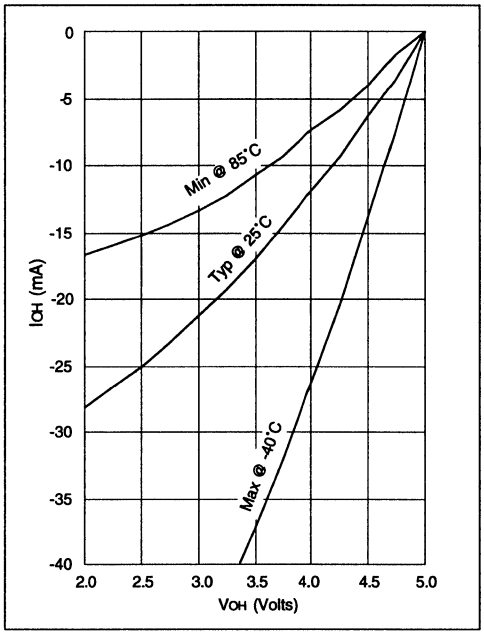


FIGURE 18.0.18 - IOL vs VOL, VDD = 3V

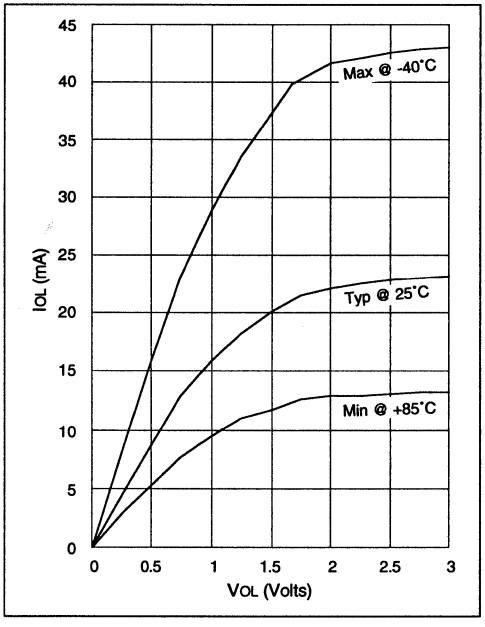
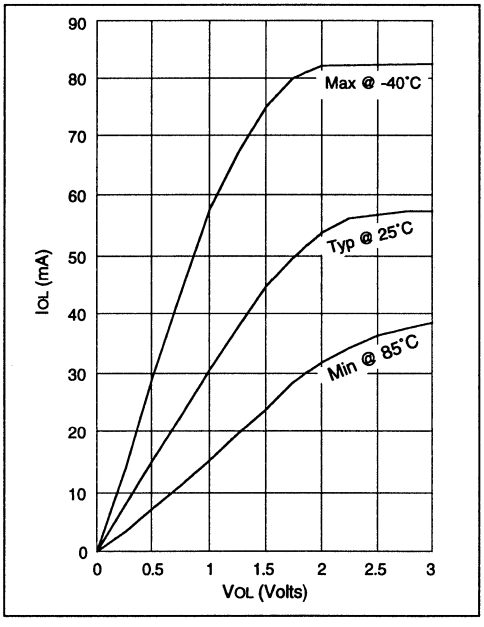


FIGURE 18.0.19 - IOL vs VOL, VDD = 5V



2

TABLE 18.0.2 - INPUT CAPACITANCE FOR PIC16CR54 *

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA, RB port	5.0	4.3
$\overline{\text{MCLR}}$	2.0	2.0
OSC1,OSC2/CLKOUT	4.0	3.5
RTCC	3.2	2.8

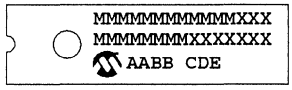
* All capacitance values are typical at 25°C. A part to part variation of ±25% (three standard deviations) should be taken into account.

19.0 PACKAGING INFORMATION

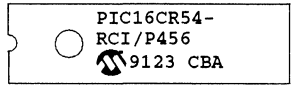
See Section 11 of the Data Book.

19.1 Package Marking Information

18L PDIP

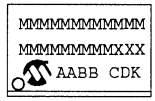


Example



18L SOIC

Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

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CONNECTING TO MICROCHIP BBS

Connect world wide to the Microchip BBS using the CompuServe® communications network. In most cases a local call is your only expense. The Microchip BBS connection does not use CompuServe membership services, therefore **you do not need CompuServe membership to join Microchip's BBS.**

The procedure to connect will vary slightly from country to country. Please check with your local CompuServe agent for details if you have a problem. CompuServe services allows multiple users at baud rates up to 9600.

To connect:

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.

2. Dial your local CompuServe phone number.

3. Depress **<ENTER>** and a garbage string will appear because Compuserve is expecting a 7E1 setting.

4. Type **+ <ENTER>** and `Host Name:` will appear.

5. Type **MCHIPBBS<ENTER>** and you will be connected to the Microchip BBS.

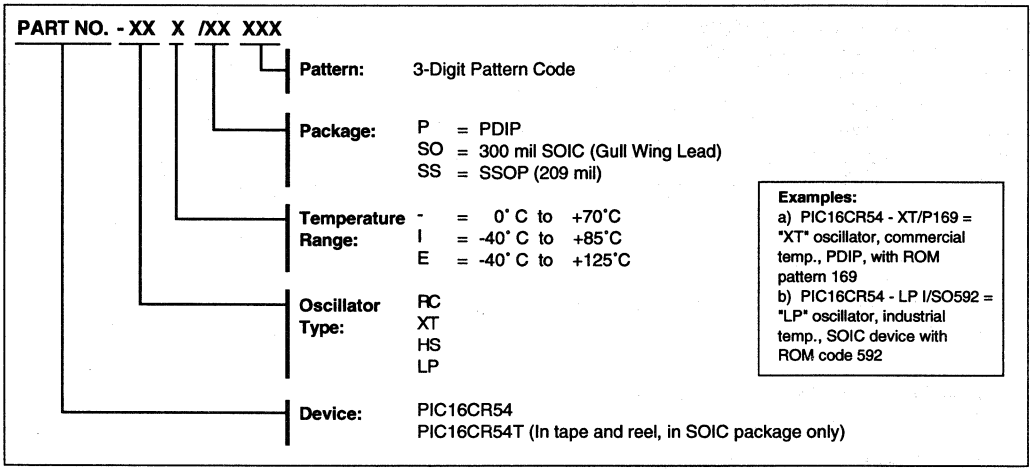
In the United States, to find CompuServe's phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600 baud connection. After the system responds with `Host Name:`, type

NETWORK<ENTER> and follow CompuServe's directions.

For voice information (or calling from overseas), you may call (614) 457-1550 for your local CompuServe number.

PIC16CR54 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local Compuserve number.

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

PIC16C54A

EPROM-Based 8-Bit CMOS Microcontroller

FEATURES

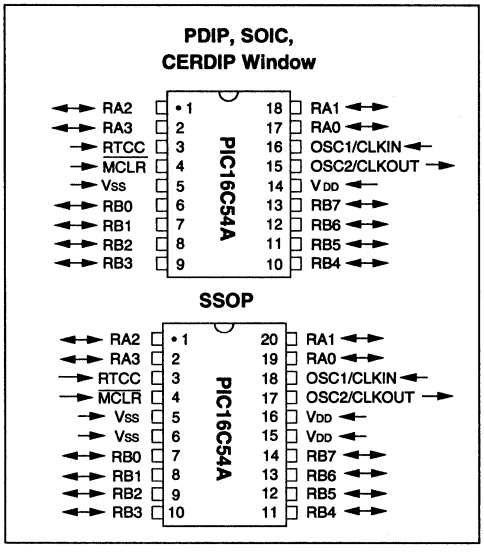
Compatibility
- Pin and software compatible with PIC16C54 device

High-Performance RISC-like CPU
- Only 33 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200ns instruction cycle
- 12-bit wide instructions
- 8-bit wide data path
- 512 x 12 on-chip EPROM program memory
- 25 x 8 general purpose registers (SRAM)
- Seven special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features
- 12 I/O pins with individual direction control
- 8-bit real time clock/counter (RTCC) with 8-bit programmable prescaler
- Power-On Reset
- Oscillator Start-up Timer
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security EPROM fuse for code-protection
- Power saving SLEEP mode
- EPROM fuse selectable oscillator options:
  - Low-cost RC oscillator: RC
  - Standard crystal/resonator: XT
  - High-speed crystal/resonator: HS
  - Power saving, low frequency crystal: LP

CMOS Technology
- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide-operating voltage range:
  - Commercial: 2.5V to 6.25V
  - Industrial: 2.5V to 6.25V
- Low-power consumption
  - < 2mA typical @ 5V, 4 MHz
  - 15μA typical @ 3V, 32 KHz
  - < 3μA typical standby current @ 3V, 0°C to 70°C

FIGURE A - PIN CONFIGURATIONS



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1.0 GENERAL DESCRIPTION

The PIC16C54A from Microchip Technology is a new member of the PIC16C5X family of low-cost, high-performance, 8-bit, fully static, EPROM based CMOS microcontrollers. This device is pin and software compatible with the PIC16C54. It employs a RISC-like architecture with only 33 single word/single cycle instructions to learn. All instructions are single cycle (200ns) except for program branches which take two cycles. The PIC16C54A delivers performance an order of magnitude higher than its competitors in similar price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C54A is equipped with special microcontroller-like features that reduce system cost and power requirements. The Power-On Reset and Oscillator Start-Up Timer eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including power saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, watchdog timer and code protection features improves system cost, power and reliablity.

The UV-erasable cerdip-packaged versions are ideal for code development while the cost-effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontroller while benefiting from the OTP flexibility.

The PIC16C54A is supported by an assembler, a software simulator, an in-circuit emulator and a production quality programmer. All the tools are supported by IBM PC® and compatible machines.

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TABLE 1.0.1 - OVERVIEW OF PIC16C5X AND PIC16C5XA DEVICES

Device	Memory Program (12-bit Words)	User RAM (Bytes)	I/O	Package Options
PIC16C54	512 (OTP)	25	12	18-lead windowed CERDIP, 18-lead PDIP (300 mil), 18-lead SOIC (300 mil), 20-lead SSOP
PIC16C54A†				
PIC16CR54	512 (ROM)			
PIC16C55	512 (OTP)	24	21	28-lead windowed CERDIP, 28-lead PDIP (300 and 600 mil), 28-lead SOIC (300 mil), 28-lead SSOP
PIC16C56	1024 (OTP)	25	12	18-lead windowed CERDIP, 18-lead PDIP (300 mil), 18-lead SOIC (300 mil), 20-lead SSOP
PIC16C57	2048 (OTP)	72	21	28-lead windowed CERDIP, 28-lead PDIP (300 and 600 mil), 28-lead SOIC (300 mil), 28-lead SSOP
PIC16CR57A†	2048 (OTP)			
PIC16C58A†	2048 (OTP)	73	12	18-lead windowed CERDIP, 18-lead PDIP (300 mil), 18-lead SOIC (300 mil), 20-lead SSOP

1.1 Applications

The PIC16C54A device fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices, and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages for through hole or surface mounting make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16C54A very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

TABLE 1.0.2 - CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	C-04	C-20	LC-04
RC	VDD: 3.0V to 6.25V Idd: 3.3mA Max. at 5.5V Ipd: 9uA Max. at 3V WDT dis Freq.: 4MHz Max.	VDD: 4.5V to 5.5V Idd: 1.8mA typ. at 5.5V Ipd: 0.6uA typ. at 3V WDT dis Freq.: 4 MHz Max.	VDD: 2.5 to 5.5V Idd: 1.8mA typ at 5.5V Ipd: 0.6uA typ at 3V WDT dis Freq.: 4MHz Typ.
XT	VDD: 3.0V to 6.25V Idd: 3.3mA Max. at 5.5V Ipd: 9uA Max. at 3V WDT dis Freq.: 4MHz Max.	VDD: 4.5V to 5.5V Idd: 1.8mA typ. at 5.5V Ipd: 0.6uA typ. at 3V WDT dis Freq.: 4 MHz Max.	VDD: 2.5 to 5.5V Idd: 1.8mA typ at 5.5V Ipd: 0.6uA typ at 3V WDT dis Freq.: 4MHz Typ.
HS	VDD: 4.5V to 5.5V Idd: 9mA Typ. at 5.5V Ipd: 0.6uA Typ. at 4.5V WDT dis Freq.: 4MHz	VDD: 4.5V to 5.5V Idd: 20mA Max. at 5.5Vtyp at 5.5V Ipd: 0.6uA typ. at 4.5V WDT dis Freq.: 20 MHz Max.	Do not use in HS mode
LP	VDD: 3.0V to 6.25V Idd: 15uA Typ. at 32 KHz, 3.0V Ipd: 0.6uA Typ. at 3.0V WDT dis Freq.: 200KHz Typ.	Do not use in LP mode	VDD: 2.5 to 6.25V Idd: 32uA Max. at 32KHz, 3.0V Ipd: 9uA Max. at 3.0V WDT dis Freq.: 200KHz Max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user selects the device type that guarantees the specifications required.

2.0 ARCHITECTURAL DESCRIPTION

2.1 Harvard Architecture

The PIC16C54A single-chip microcomputer is a low-power, high-speed, full static CMOS devices containing EPROM, RAM, I/O and a central processing unit on a single chip.

The architecture is based on a register file concept with separate bus and memories for data and instructions (Harvard architecture). The data bus and memory (RAM) are 8-bits wide while the program bus and program memory (EPROM) have a width of 12-bits. This concept allows a simple yet powerful instruction set designed to emphasize bit, byte and register operations under high speed with overlapping instruction fetch and execution cycles. That means that, while one instruction is executed, the following instruction is already being read from the program memory. A block diagram of the PIC16C54A is given in Figure 2.1.1.

2.2 Clocking Scheme/Instruction Cycle

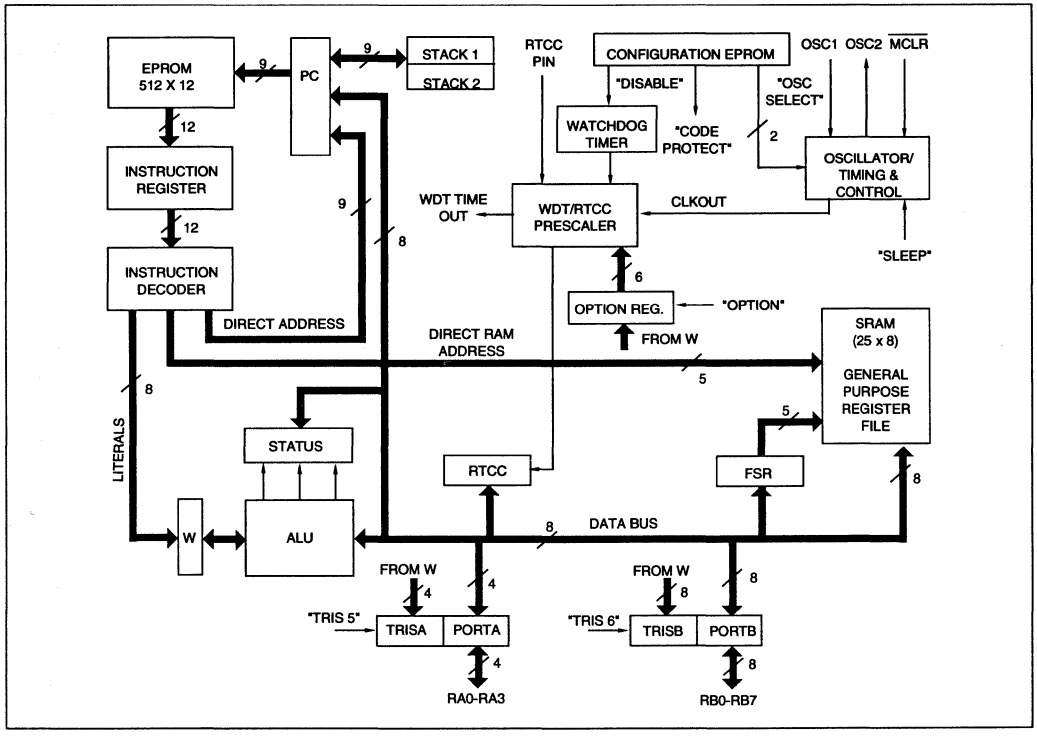
The clock input (from pin OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, PC is incremented every Q1, instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 2.2.1.

TABLE 2.1.1 - PIN FUNCTIONS

Name	Function
RA0 - RA3	I/O PORTA
RB0 - RB7	I/O PORTB
RTCC	Real Time Clock/Counter
$\overline{MCLR}$	Master Clear
OSC1/CLKIN	Oscillator (input)
OSC2/CLKOUT	Oscillator (output)
VDD	Power supply
Vss	Ground
N/C	No (internal) Connection

2

FIGURE 2.1.1 - PIC16C54A SERIES BLOCK DIAGRAM



2.3 Data Register File

The 8-bit data bus connects two basic functional elements together: the Register File composed of 32 addressable 8-bit registers including the I/O Ports, and an 8-bit wide Arithmetic Logic Unit. The 32 bytes of RAM are directly addressable while a "banking" scheme, with banks of 16 bytes each, is employed to address larger data memories (Figure 4.2.1). Data can be addressed direct, or indirect using the file select register (f4). Immediate data addressing is supported by special "literal" instructions which load data from program memory into the W register.

The register file is divided into two functional groups: operational registers and general purpose registers. The operational registers include the Real Time Clock Counter (RTCC) register, the Program Counter (PC), the Status Register, the I/O registers (PORTs), and the File Select Register. The general purpose registers are used for data and control information under command of the instructions.

In addition, special purpose registers are used to control the I/O port configuration, and the prescaler options.

2.4 Arithmetic/Logic Unit (ALU)

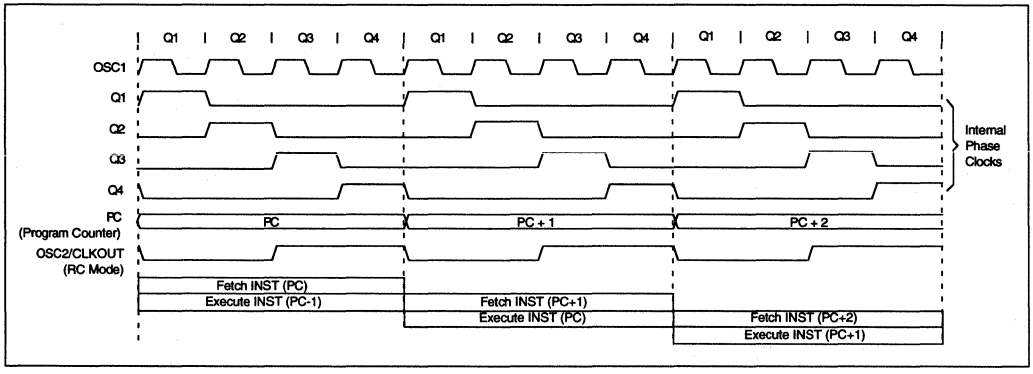
The 8-bit wide ALU contains one temporary working register (W Register). It performs arithmetic and Boolean functions between data held in the W Register and any file register. It also does single operand operations on either the W register or any file register.

2.5 Program Memory

512 words of 12-bit wide on-chip program memory (EPROM) can be directly addressed.

Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations, supporting direct, indirect, relative addressing modes, can be performed by Bit Test and Skip instructions, Call instructions, Jump instructions or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting.

FIGURE 2.2.1 - CLOCKS/INSTRUCTION CYCLE



3.0 PIC16C54A SERIES OVERVIEW

A wide variety of EPROM and RAM sizes, number of I/O pins, oscillator types, frequency ranges, and packaging options is available. Depending on application and production requirements the proper device option can be selected using the information and tables in this section. When placing orders, please use the "PIC16C54A Product Identification System" on the back page of this data sheet to specify the correct part number.

3.1 UV Erasable Devices

These devices are optimal for prototype development and pilot series. The desired oscillator configuration is EPROM programmable as "RC", "XT", "HS" or "LP". An erased device is configured as "RC" type by default. Depending on the selected oscillator type and frequency, the operating supply voltage must be within the same range as a OTP/QTP part would be specified for.

3.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates. OTP devices have the oscillator type pre-configured by the factory, and they are tested only for this special configuration (including voltage and frequency ranges, current consumption).

The program EPROM is erased, allowing the user to write the application code into it. In addition, the Watchdog Timer can be disabled, and/or the code protection logic can be activated by programming special EPROM fuses. The 16 special EPROM bits for ID code storage are also user programmable.

3.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

3.4 Serialized-Quick-Turnaround-Production (SQTP) Devices

Microchip offers the unique programming service where few locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

4.0 OPERATIONAL REGISTER FILES

4.1 Indirect Data Addressing

This is not a physically implemented register. Addressing INDF calls for the contents of the File Select Register to be used to select a file register. INDF is useful as an indirect address pointer. For example, in the instruction ADDWF INDF, W will add the contents of the register pointed to by the FSR to the content of the W Register and place the result in W.

If INDF itself is read through indirect addressing (i.e. FSR = 0h), then 00h is read. If INDF is written to via indirect addressing, the result will be a NOP.

4.2 Real Time Clock/Counter Register (RTCC)

This register can be loaded and read by the program as any other register. In addition, its contents can be incremented by an external signal edge applied to the RTCC pin, or by the internal instruction cycle clock (CLKOUT=fosc/4). Figure 4.1.1 is a simplified block diagram of RTCC.

An 8-bit prescaler can be assigned to the RTCC by writing the proper values to the PSA bit and the PS bits in the OPTION register. OPTION register is a special register (not mapped in data memory) addressable using the 'OPTION' instruction. See Section 7.4 for details. If the prescaler is assigned to the RTCC, instructions writing to RTCC (e.g. CLRF RTCC, or BSF RTCC,5, ...etc.) clear the prescaler.

The bit "RTS" (RTCC signal Source) in the OPTION register determines if RTCC is incremented internally or externally.

RTS=1: The clock source for the RTCC or the prescaler, if assigned to it, is the signal on the RTCC pin. Bit 4 of the OPTION register (RTE) determines if an increment occurs on the falling (RTE=1) or rising (RTE=0) edge of the signal presented to the RTCC pin.

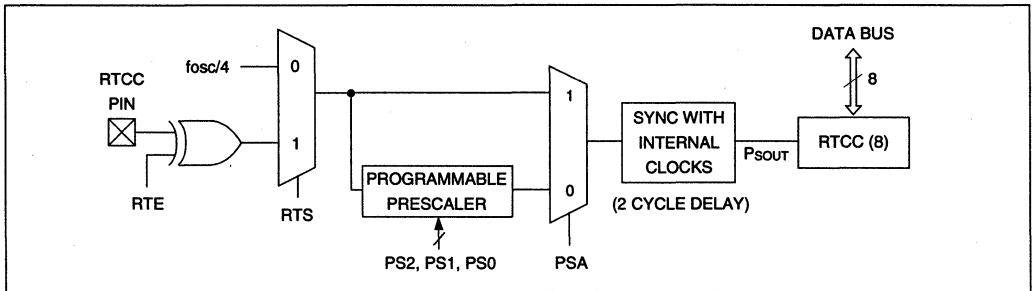
RTS=0: The RTCC register or its prescaler, respectively, will be incremented with the internal instruction clock (= $F_{OSC}/4$). The "RTE" bit in the OPTION register and the RTCC pin are "don't care" in this case. The RTCC pin must not be left floating (tie to V_{DD} or V_{SS}). This prevents unintended entering of test modes and to reduce the current consumption in low power applications.

As long as clocks are applied to the RTCC (from internal or external source, with or without prescaler), RTCC keeps incrementing and just rolls over when the value "FFh" is reached. All increment pulses for RTCC are delayed by two instruction cycles. After writing to RTCC, for example, no increment takes place for the following two instruction cycles. This is independent if internal or external clock source is selected. If a prescaler is assigned to the RTCC, the output of the prescaler will be delayed by two cycles before RTCC is incremented. This is true for instructions that either write to or read-modify-write RTCC (e.g. MOVF RTCC, CLRF RTCC). For applications where RTCC needs to be tested for zero without affecting its count, use of MOVF RTCC, W instruction is recommended. Timing diagrams in Figure 4.2.2 show RTCC read, write and increment timing.

4.2.1 USING RTCC WITH EXTERNAL CLOCK

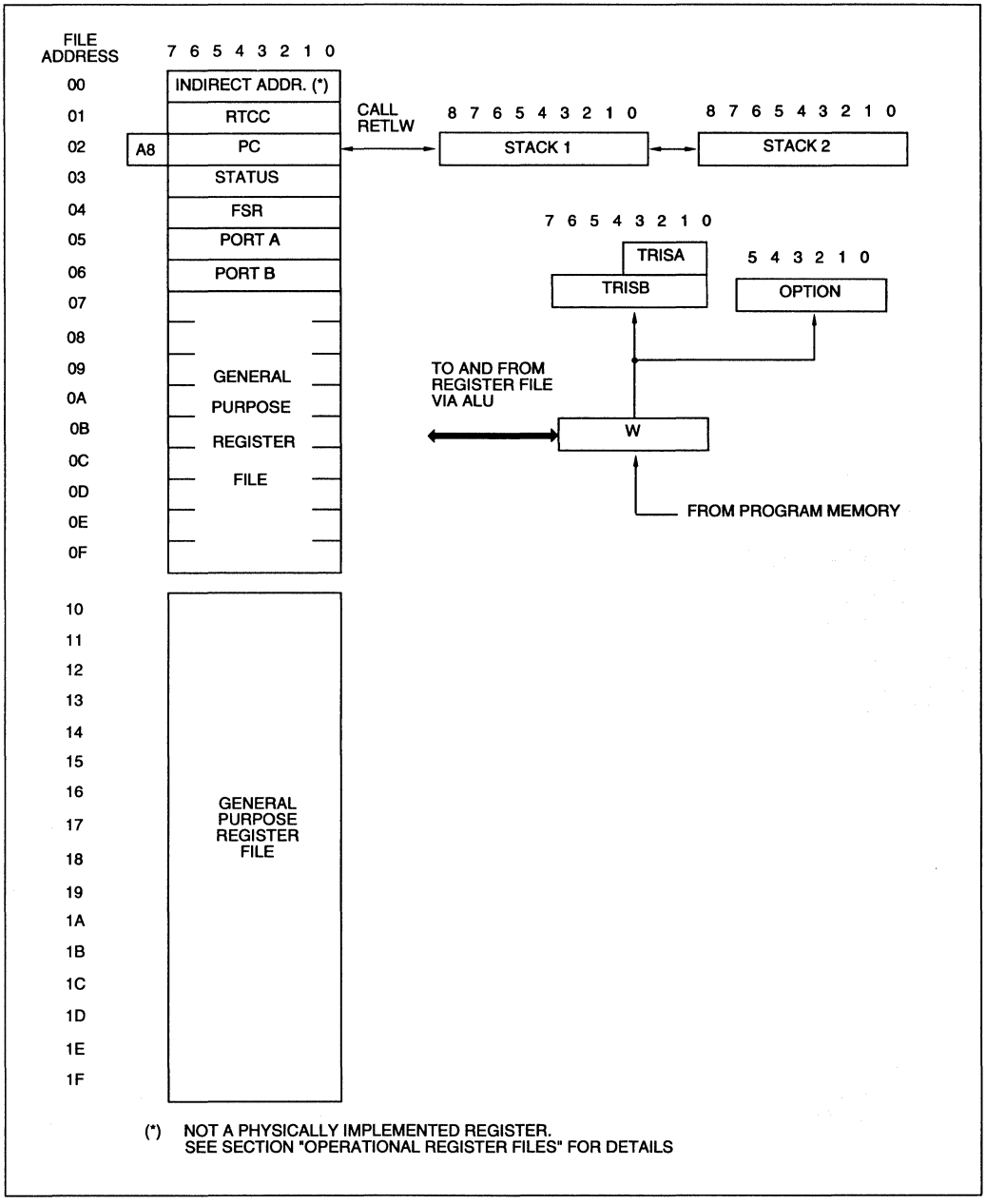
When external clock input is used for RTCC, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements. Also there is some delay from the occurance of the external clock edge to the actual incrementing of RTCC. Referring to Figure 4.1.1, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where tosc = oscillator time period.

FIGURE 4.1.1 - RTCC BLOCK DIAGRAM (SIMPLIFIED)



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 are located in option register.
2. The prescaler is shared with Watchdog Timer (see Figure 9.0.1).

FIGURE 4.2.1 - PIC16C54A DATA MEMORY MAP



When no prescaler is used, PSOUT (Prescaler output, see Figure 4.1.1) is the same as RTCC clock input and therefore the requirements are:

T_{RTH} = RTCC high time ≥ 2tosc + 20ns

T_{RTL} = RTCC low time ≥ 2tosc + 20ns

When prescaler is used, the RTCC input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.

Then: PSOUT high time = PSOUT low time = $\frac{N \bullet T_{RT}}{2}$

where T_{RT} = RTCC input period and N = prescale value (2, 4, ..., 256). The requirement is, therefore $\frac{N \bullet T_{RT}}{2}$ ≥ 2 tosc + 20 ns, or $T_{RT} \geq \frac{4 \text{ tosc} + 40 \text{ ns}}{N}$.

The user will notice that no requirement on RTCC high time or low time is specified. However, if the high time or low time on RTCC is too small then the pulse may not be detected, hence a minimum high or low time of 10ns is required. In summary, the RTCC input requirements are:

T_{RT} = RTCC period ≥ (4 tosc + 40ns)/N

T_{RTH} = RTCC high time ≥ 10ns

T_{RTL} = RTCC low time ≥ 10ns

Delay from external clock edge: Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the RTCC is actually incremented. Referring to Figure 4.2.3, the reader can see that this delay is between 3 tosc and 7 tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±200ns @ 20 MHz).

4.3 Program Counter (PC)

The program counter generates the addresses for on-chip ROM containing the program instruction words (Figure 4.3.1).

The program counter is set to all "1"s upon a RESET condition. During program execution it is auto incremented with each instruction unless the result of that instruction changes the PC itself:

a) "GOTO" instructions allow the direct loading of the lower nine program counter bits (PC <8:0>).
b) "CALL" instructions load the lower 8-bits of the PC directly while the ninth bit is cleared to "0". The PC value, incremented by one, will be pushed into the stack.
c) "RETLW" instructions load the program counter with the top of stack contents.
d) If PC is the destination in any instruction (e.g. MOVWF PC, ADDWF PC, or BSF PC,5) then the computed 8-bit result will be loaded into the lower 8-bits of program counter. The ninth bit of PC will be cleared.

FIGURE 4.2.2A - RTCC TIMING: INT CLOCK/NO PRESCALE

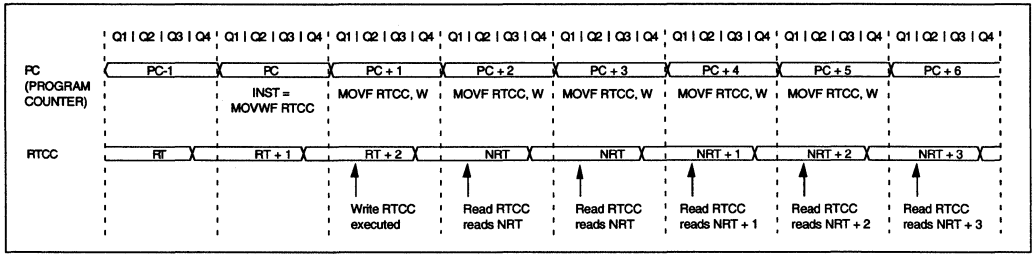


FIGURE 4.2.2B - RTCC TIMING: INT CLOCK/PRESCALE 1:2

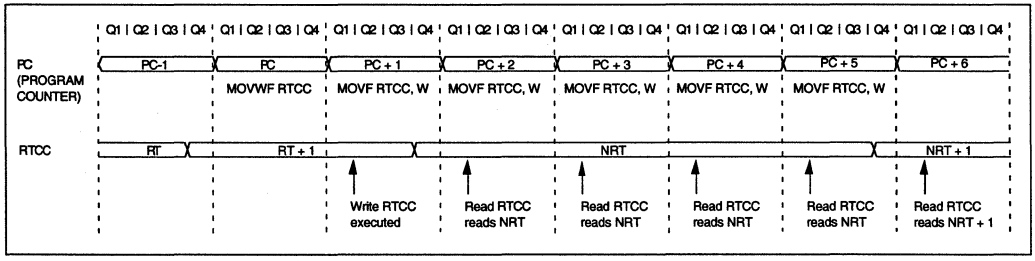
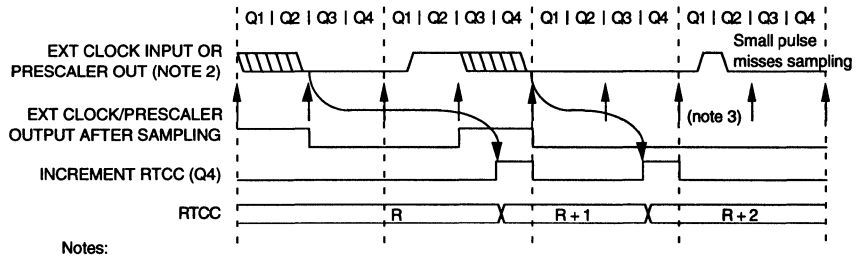


FIGURE 4.2.3 - RTCC TIMING WITH EXTERNAL CLOCK

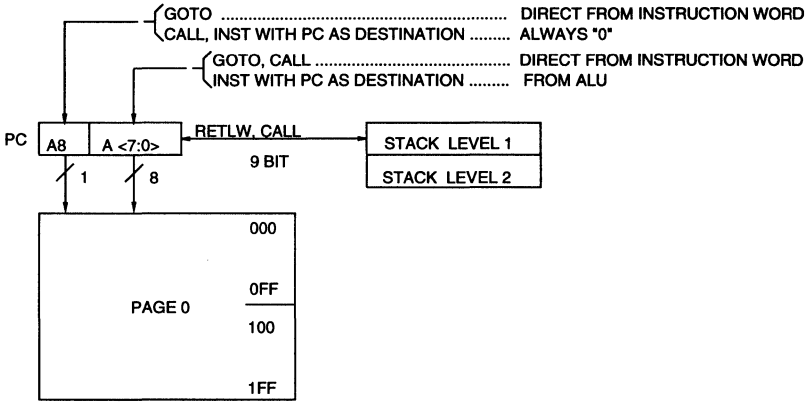


Notes:

1. Delay from clock input change to RTCC increment is 3 tosc to 7 tosc. (Duration of Q = tosc). Therefore, the error in measuring the interval between two edges on RTCC input = ± 4 tosc max.
2. External clock if no prescaler selected, Prescaler output otherwise.
3. The arrows indicate the points in time where sampling occurs.

2

FIGURE 4.3.1 - PROGRAM MEMORY ORGANIZATION



4.4 Stack

The PIC16C54A series employs a two-level hardware push/pop stack (Figure 4.3.1).

CALL instructions push the current program counter value, incremented by "1", into stack level 1. Stack level 1 is automatically pushed to level 2. If more than two subsequent "CALL"s are executed, only the most recent two return addresses are stored.

RETLW instructions load the contents of stack level 1 into the program counter while stack level 2 gets copied into level 1. If more than two subsequent "RETLW"s are executed, the stack will be filled with the address previously stored in level 2.

4.5 Status Word Register (STATUS)

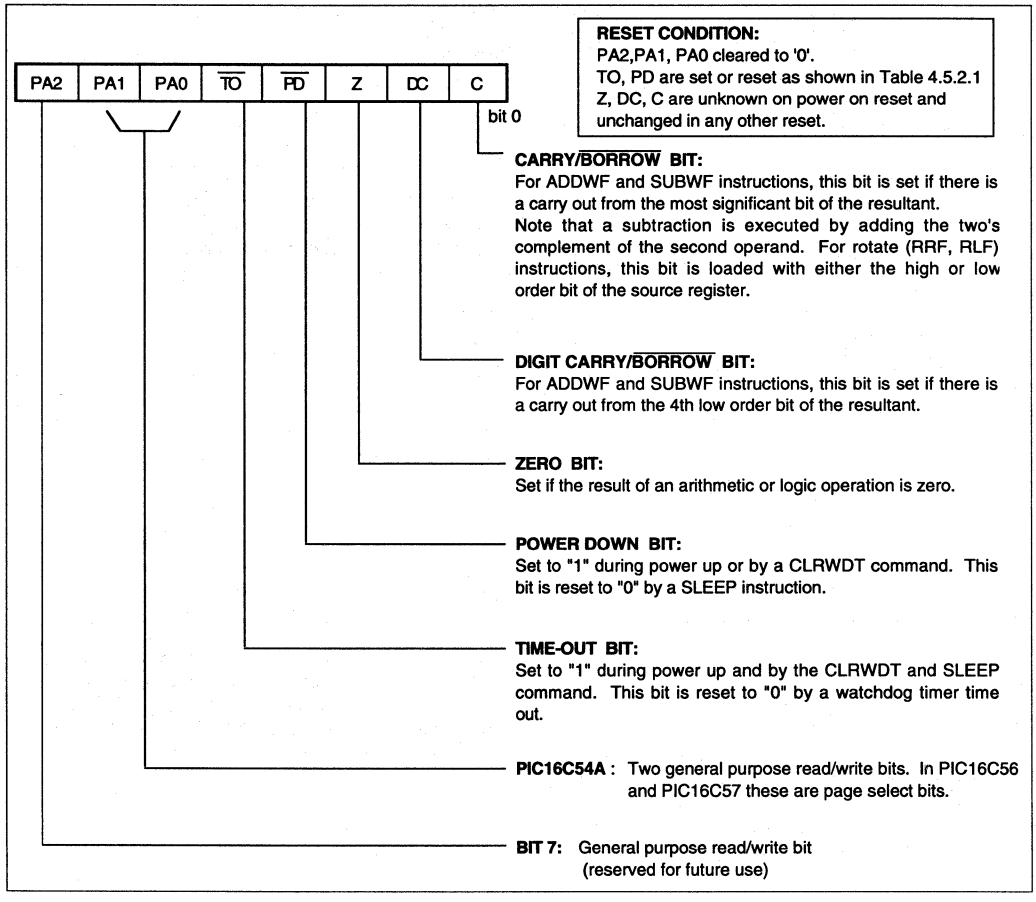
This register contains the arithmetic status of the ALU, the RESET status.

The STATUS register can be destination for any instruction like any other register. However, the status bits are set after the following write. Furthermore, $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with STATUS register as destination may be different than intended. For example, CLRF STATUS will clear all bits except for $\overline{TO}$ and $\overline{PD}$ and then set the Z bit and leave STATUS register as 000UU100 (where U = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the STATUS registers because these instructions do not affect any status bit.

For other instructions, affecting any status bits, see Section "Instruction Set Summary" (Table 10.0.1).

FIGURE 4.5.1 - STATUS WORD REGISTER



4.5.1 CARRY/BORROW AND DIGIT CARRY/ BORROW BITS:

The Carry bit (C) is a carry out in addition operation (ADDWF) and a borrow out in subtract operation (SUBWF).

It is also affected by RRF and RLF instructions. The following examples explain carry/borrow bit operation:

```
;SUBWF Example #1
;
clrf   0x20    ;f(20h)=0
movlw  1       ;wreg=1
subwf  0x20    ;f(20h)=f(20h)-wreg=0-1=FFh
               ;Carry=0: Result is negative
;
;SUBWF Example #2
movlw 0xFF     ;
movwf  0x20    ;f(20h)=FFh
clrw           ;wreg=0
subwf  0x20    ;f(20h)=f(20h)-wreg=FFh-
0=FFh
               ;Carry=1:Result is positive
;
```

The digit carry operates in the same way as the carry bit, i.e. it is a borrow in subtract operation.

4.5.2 TIME OUT AND POWER DOWN STATUS BITS (TO, PD)

The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be tested to determine if a RESET condition has been caused by a Watchdog Timer timeout, a power-up condition, or a wake-up from SLEEP by the Watchdog Timer or $\overline{MCLR}$ pin.

These status bits are only affected by events listed in Table 4.5.2.1.

TABLE 4.5.2.1 - EVENTS AFFECTING $\overline{PD}$/ $\overline{TO}$ STATUS BITS

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
WDT Timeout	0	X	No effect on PD
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Note: A WDT timeout will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{PD}$ bit. Table 4.5.2.2 reflects the status of $\overline{PD}$ and $\overline{TO}$ after the corresponding event.

TABLE 4.5.2.2 - $\overline{PD}$/$\overline{TO}$ STATUS AFTER RESET

$\overline{TO}$	$\overline{PD}$	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT time-out (not during SLEEP)
1	0	$\overline{MCLR}$ wake-up from SLEEP
1	1	Power-up
U	U	= Low pulse on $\overline{MCLR}$ input

Note: The $\overline{PD}$ and $\overline{TO}$ bit maintain their status (U) until an event of Table 4.5.2.1 occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{PD}$ and $\overline{TO}$ status bits.

4.6 File Select Register (FSR)

PIC16C54A

Bits 0-4 select one of the 32 available file registers in the indirect addressing mode (that is, calling for file INDF in any of the file oriented instructions).

Bits 5-7 of the FSR are read-only and are always read as "one"s.

If no indirect addressing is used, the FSR can be used as a 5-bit wide general purpose register.

5.0 I/O REGISTERS (PORTS)

The I/O registers can be written and read under program control like any other register of the register file. However, "read" instructions (e.g. MOVF PORTB,W) always read the I/O pins, regardless if a pin is defined as "input" or "output." Upon a RESET condition, all I/O ports are defined as "input" (= high impedance mode) as the I/O control registers (TRISA, TRISB) are all set to "ones."

The execution of a "TRIS f" instruction with corresponding "zeros" in the W-register is necessary to define any of the I/O pins as output.

5.1 PORTA

4-bit I/O register. Low-order 4-bits only are used (RA0 - RA3). Bit 4 - 7 are unimplemented and read as "zeros."

5.2 PORTB

8-bit I/O register.

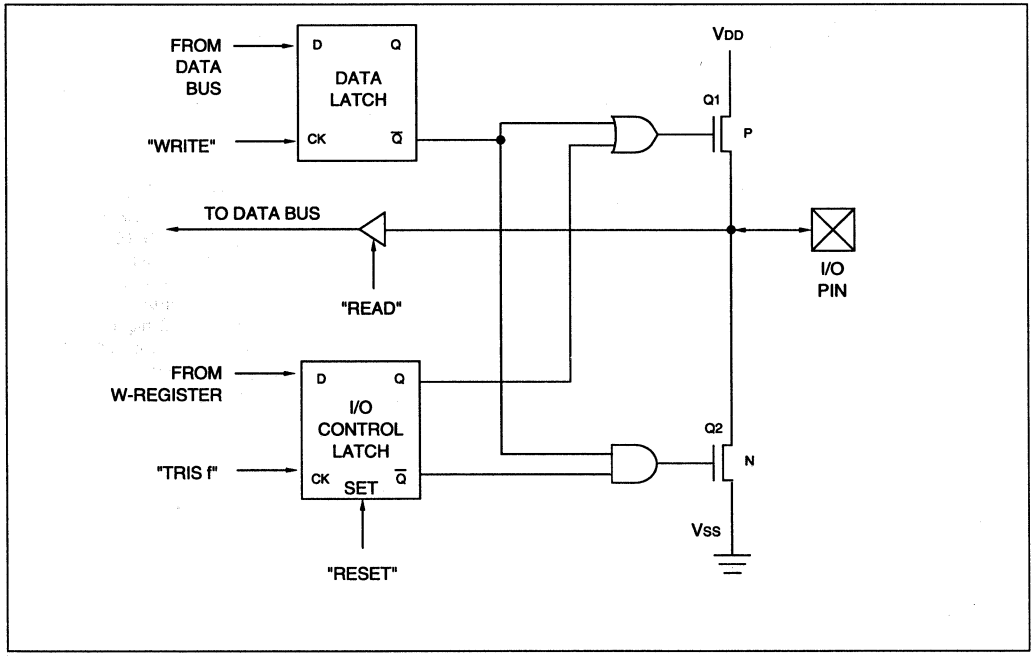
5.3 f7

In PIC16C54A, file register f7 is a general purpose register.

5.4 I/O Interfacing

The equivalent circuit for an I/O port bit is shown in Figure 5.4.1. All ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g. MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB) must be set to zero. For use as an input, the corresponding TRIS bit 5.5 I/O Programming Considerationsmust be "one". Any I/O pin can be programmed individually as input or output.

FIGURE 5.4.1 - EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



5.5 I/O Programming Considerations

5.5.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit 5 and PORTB is re-output to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

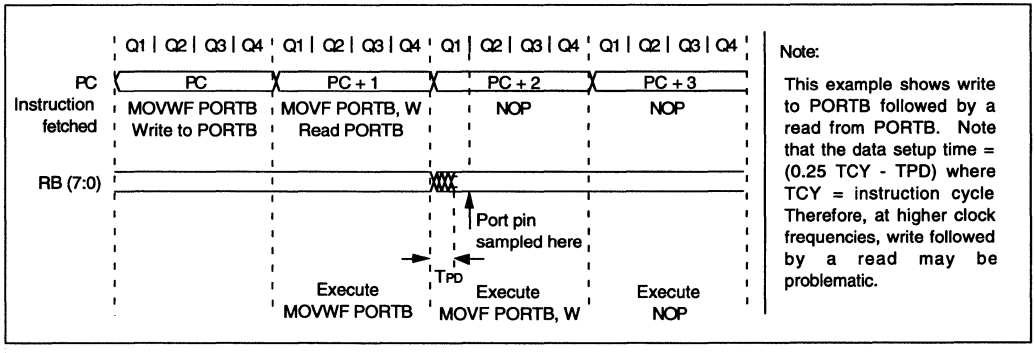
A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see Figure 5.5.2.1). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

2

FIGURE 5.5.2.1 - I/O PORT READ/WRITE TIMING



6.0 GENERAL PURPOSE REGISTERS

f07h - f1Fh: are general purpose register files.

7.0 SPECIAL PURPOSE REGISTERS

7.1 W Working Register

Holds second operand in two operand instructions and/ or supports the internal data transfer.

7.2 TRISA I/O Control Register For PORTA

Only bits 0 - 3 are available. The corresponding I/O port (f5) is only 4-bit wide.

7.3 TRISB I/O Control Register For PORTB

The I/O control registers will be loaded with the content of the W register by executing of the TRIS f instruction.

A "1" in the I/O control register puts the corresponding I/O pin into a high impedance mode. A "0" puts the contents of file register PORTA or PORTB, respectively, out on the selected I/O pins.

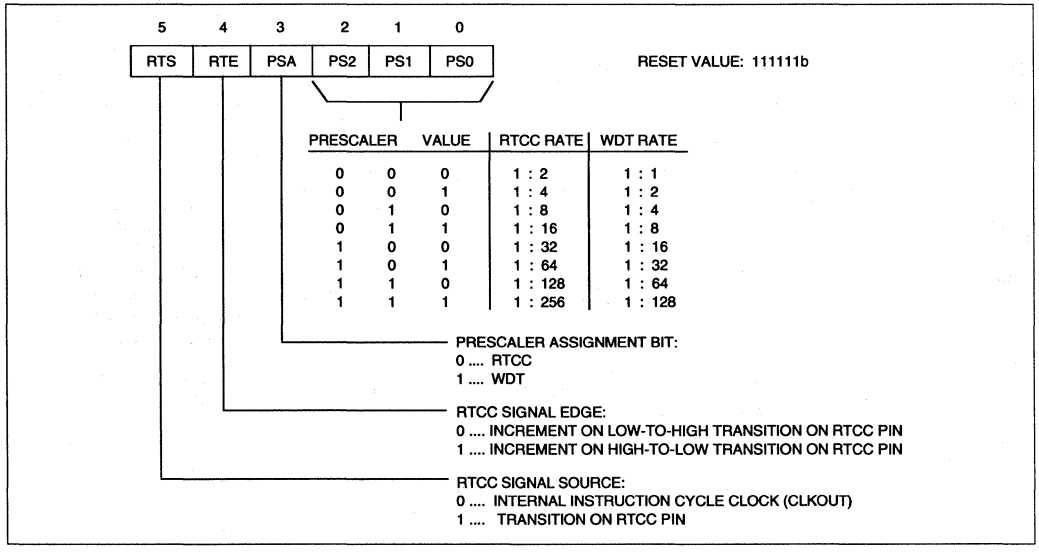
These registers are "write-only" and are set to all "ones" upon a RESET condition.

7.4 OPTION Prescaler/RTCC Option Register

Defines prescaler assignment (RTCC or WDT), prescaler value, signal source and signal edge for the RTCC. The OPTION register is "write-only" and is 6 bit wide.

By executing the "OPTION" instruction, the contents of the "W" register will be transferred to the option register. Upon a RESET condition, the option register is set to all "ones."

FIGURE 7.4.1 - OPTION REGISTER



8.0 RESET CONDITION

A RESET condition can be caused by applying power to the chip (power-up), pulling the MCLR input "low", or by a Watchdog Timer timeout. The device will stay in RESET as long as the Oscillator Start-up Timer (OST) is active or the MCLR input is "low."

The Oscillator Start-up Timer is activated as soon as MCLR input is sensed to be high. This implies that in case of Power-On Reset with MCLR tied to VDD the OST starts from power-up. In case of WDT timeout, it will start at the end of the timeout (since MCLR is high). In case of MCLR reset, the OST will start when MCLR goes high. The nominal OST timeout period is 18ms. See Section 13.0 for detailed information on OST and Power-On Reset.

During a RESET condition the state of the PIC16C54A is defined as :

- The oscillator is running, or will be started (power-up or wake-up from SLEEP).
- All I/O port pins (RA0 - RA3, RB0 - RB7 are put into the high-impedance state by setting the "TRIS" registers to all "ones" (= input mode).
- The Program Counter is set to all "ones" (1FFh).
- The OPTION register is set to all "ones".
- The Watchdog Timer and its prescaler are cleared.
- The upper-three bits (page select bits) in the Status Register (f3) are cleared to "zero."
- "RC" devices only: The "CLKOUT" signal on the OSC2 pin is held at a"low" level.

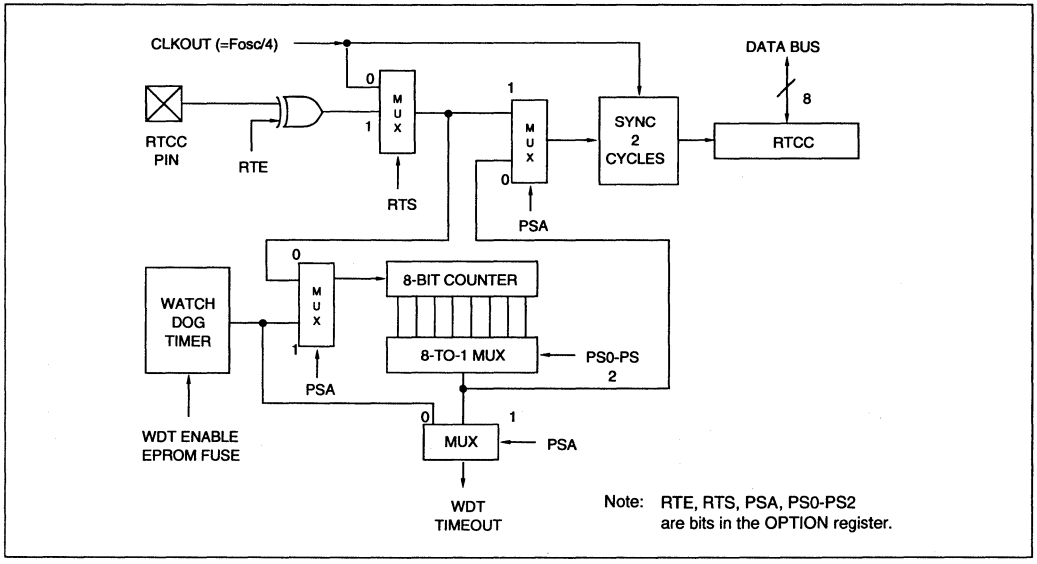
9.0 PRESCALER

An 8-bit counter is available as a prescaler for the RTCC, or as a post-scaler for the Watchdog Timer, respectively (Figure 9.0.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the RTCC and the Watchdog Timer. Thus, a prescaler assignment for the RTCC means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS0-PS2 bits in the OPTION register determine the prescaler assignment and pre-scale ratio. When assigned to the RTCC, all instructions writing to the RTCC (e.g. CLRF RTCC, MOVWF RTCC, BSF RTCC,x ....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer.

2

FIGURE 9.0.1 - BLOCK DIAGRAM RTCC/WDT PRESCALER



9.1 Switching Prescaler Assignment

CHANGING PRESCALER FROM RTCC TO WDT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence must be executed when changing the prescaler assignment from RTCC to WDT:

```
1. MOVLW  B'xx0x0xxx'   ; Select internal clock and select new
2. OPTION               ; prescaler value. If new prescale value
                        ; is = '000' or '001', then select any other
                        ; prescale value temporarily.
3. CLRF 1               ; Clear RTCC and prescaler.
4. MOVLW  B'xxxx1xxx'   ; Select WDT, do not change prescale
                        ; value.
5. OPTION               ;
6. CLRWDT               ; Clears WDT and prescaler.
7. MOVLW  B'xxxx1xxx'   ; Select new prescale value.
8. OPTION               ;
```

Steps 1 and 2 are only required if an external RTCC source is used. Steps 7 and 8 are necessary only if the desired prescale value is '000' or '001'.

CHANGING PRESCALER FROM WDT TO RTCC

To change prescaler from WDT to RTCC use the following sequence:

```
1. CLRWDT               ; Clear WDT and prescaler
2. MOVLW  B'xxxx0xxx'   ; Select RTCC, new prescale value
                        ; and clock source
3. OPTION               ;
```

10.0 BASIC INSTRUCTION SET SUMMARY

Each instruction is a 12-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The instruction set summary in Table 10.0.1 lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 file registers is to be utilized by the instruction.

The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Notes to Table 10.0.1

Note 1: The ninth bit of the program counter will be forced to a "zero" by any instruction that writes to the PC except for GOTO (e.g. CALL, MOVWF PC etc.). See Section 4.3 on page 8 for details.

Note 2: When an I/O register is modified as a function of itself (e.g. MOVF PORTB,1), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as output and is driven low by an external device, the data will be written back with a '0'.

Note 3: The instruction "TRIS f", where f = 5,6, or 7 causes the contents of the W register to be written to the tristate latches of the specified file (port). A "one" forces the pin to a high impedance state and disables the output buffers.

Note 4: If this instruction is executed on file register f1 (and, where applicable, d=1), the prescaler will be cleared if assigned to the RTCC.

TABLE 10.0.1 - INSTRUCTION SET SUMMARY

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4 - 0)
OPCODE	d	f(FILE #)

d = 0 for destination W
d = 1 for destination f

Instruction-Binary	(Hex)	Name	Mnemonic,	Operands	Operation	Status Affected	Notes
0001 11df ffff	1Cf	Add W and f	**ADDWF**	**f, d**	W + f → d	C,DC,Z	1,2,4
0001 01df ffff	14f	AND W and f	**ANDWF**	**f, d**	W & f → d	Z	2,4
0000 011f ffff	06f	Clear f	**CLRF**	**f**	0 → f	Z	4
0000 0100 0000	040	Clear W	**CLRW**	**-**	0 → W	Z	
0010 01df ffff	24f	Complement f	**COMF**	**f, d**	$\bar{f}$ → d	Z	2,4
0000 11df ffff	0Cf	Decrement f	**DECF**	**f, d**	f -1 → d	Z	2,4
0010 11df ffff	2Cf	Decrement f,Skip if Zero	**DECFSZ**	**f, d**	f - 1 → d, skip if zero	None	2,4
0010 10df ffff	28f	Increment f	**INCF**	**f, d**	f + 1 → d	Z	2,4
0011 11df ffff	3Cf	Increment f,Skip if zero	**INCFSZ**	**f, d**	f + 1 → d, skip if zero	None	2,4
0001 00df ffff	10f	Inclusive OR W and f	**IORWF**	**f, d**	W v f → d	Z	2,4
0010 00df ffff	20f	Move f	**MOVF**	**f, d**	f → d	Z	2,4
0000 001f ffff	02f	Move W to f	**MOVWF**	**f**	W → f	None	1,4
0000 0000 0000	000	No Operation	**NOP**	**-**	-	None	
0011 01df ffff	34f	Rotate left f	**RLF**	**f, d**	f(n) → d(n+1), C → d(0), f(7) → C	C	2,4
0011 00df ffff	30f	Rotate right f	**RRF**	**f, d**	f(n) → d(n-1), C → d(7), f(0) → C	C	2,4
0000 10df ffff	08f	Subtract W from f	**SUBWF**	**f, d**	f - W → d [f + $\overline{W}$ + 1 → d]	C,DC,Z	1,2,4
0011 10df ffff	38f	Swap halves f	**SWAPF**	**f, d**	f(0-3) ↔ f(4-7) → d	None	2,4
0001 10df ffff	18f	Exclusive OR W and f	**XORWF**	**f, d**	W ⊕ f → d	Z	2,4

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4 - 0)
OPCODE	b(BIT #)	f(FILE #)

Instruction-Binary	(Hex)	Name	Mnemonic,	Operands	Operation	Status Affected	Notes
0100 bbbf ffff	4bf	Bit Clear f	**BCF**	**f, b**	0 → f(b)	None	2,4
0101 bbbf ffff	5bf	Bit Set f	**BSF**	**f, b**	1 → f(b)	None	2,4
0110 bbbf ffff	6bf	Bit Test f,Skip if Clear	**BTFSC**	**f, b**	Test bit (b) in file (f): Skip if clear	None	
0111 bbbf ffff	7bf	Bit Test f, Skip if Set	**BTFSS**	**f, b**	Test bit (b) in file (f): Skip if set	None	

LITERAL AND CONTROL OPERATIONS

(11-8)	(7 - 0)
OPCODE	k (LITERAL)

Instruction-Binary	(Hex)	Name	Mnemonic,	Operands	Operation	Status Affected	Notes
1110 kkkk kkkk	Ekk	AND Literal and W	**ANDLW**	**k**	k & W→ W	Z	
1001 kkkk kkkk	9kk	Call subroutine	**CALL**	**k**	PC + 1 → Stack, k → PC	None	1
0000 0000 0100	004	Clear Watchdog timer	**CLRWDT**	**-**	0 → WDT (and prescaler, if assigned)	TO, PD	
101k kkkk kkkk	Akk	Go To address (k is 9 bit)	**GOTO**	**k**	k → PC (9 bits)	None	
1101 kkkk kkkk	Dkk	Incl. OR Literal and W	**IORLW**	**k**	k v W → W	Z	
1100 kkkk kkkk	Ckk	Move Literal to W	**MOVLW**	**k**	k → W	None	
0000 0000 0010	002	Load OPTION register	**OPTION**	**-**	W → OPTION register	None	
1000 kkkk kkkk	8kk	Return,place Literal in W	**RETLW**	**k**	k → W, Stack → PC	None	
0000 0000 0011	003	Go into standby mode	**SLEEP**	**-**	0 → WDT, stop oscillator	TO, PD	
0000 0000 0fff	00f	Tristate port f	**TRIS**	**f**	W→ I/O control register f	None	3
1111 kkkk kkkk	Fkk	Excl. OR Literal and W	**XORLW**	**k**	k ⊕ W → W	Z	

Notes: See previous page

11.0 WATCHDOG TIMER (WDT)

The Watchdog Timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1/OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by programming a "zero" into an EPROM fuse which is not part of the normal program memory EPROM.

11.1 WDT Period

The WDT has a nominal timeout period of 18ms, (with no prescaler). The timeout periods vary with temperature, V_{DD} and process variations from part to part (see DC specs). If longer timeout periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.5 seconds can be realized.

The "CLRWDT" and "SLEEP" instructions clear the WDT and the prescaler count, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit $\overline{TO}$ in file register STATUS will be cleared upon a watchdog timer timeout.

The WDT period is a function of the supply voltage, operating temperature, and will also vary from unit to unit due to variations in the manufacturing process. Please refer to the graphs in Section 18.0 and DC specs for more details.

11.2 WDT Programming Considerations

It should also be taken in account that under worst case conditions (V_{DD} = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

12.0 OSCILLATOR CIRCUITS

12.1 Oscillator Types

The PIC16C54A series is available with four different oscillator options. On windowed devices, a particular oscillator circuit can be selected by programming the configuration EPROM accordingly.

On OTP and QTP devices, the oscillator configuration is programmed by the factory and the parts are tested only to the according specifications.

12.2 Crystal Oscillator

The PIC16C54A crystal options (-XT, -HS, or LP) need a crystal or ceramic resonator connected to the OSC1 and OSC2 pins to establish oscillation (Figure 12.2.1). XT = Standard crystal oscillator, HS = High speed crystal oscillator. The series resistor RS may be required for the "HS" oscillator, especially at lower than 20 MHz oscillation frequency. It may also be required in XT mode with AT™ strip-cut type crystals to avoid overdriving.

12.3 RC Oscillator

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation to due tolerance of external R and C components used. Figure 12.3.1 shows how the R/C combination is connected to the PIC16C54A. For Rext values below 2.2 kOhm, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 kOhm and 100 kOhm.

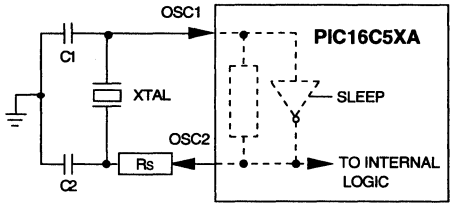
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See the table in Section 18.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characteristics in Section 18.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 2.2.1 for timing).

FIGURE 12.2.1 - CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP TYPES ONLY)



Rs may be required in HS and XT modes for AT strip-cut crystals to avoid overdriving. See Tables 12.2.1 and 12.2.2 for recommended values of C1, C2 per oscillator type and frequency.

TABLE 12.2.1 - CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	TBD
	2.0 MHz	TBD
	4.0 MHz	TBD
HS	8.0 MHz	TBD

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

FIGURE 12.2.2 - EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP TYPES ONLY)

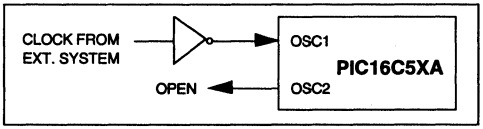


TABLE 12.2.2 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	TBD	TBD
XT	100 KHz	TBD	TBD
	200 KHz	TBD	TBD
	455 KHz	TBD	TBD
	1 MHz	TBD	TBD
	2 MHz	TBD	TBD
	4 MHz	TBD	TBD
HS	4 MHz	TBD	TBD
	8 MHz	TBD	TBD
	20 MHz	TBD	TBD

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

FIGURE 12.3.1 - RC OSCILLATOR (RC TYPE ONLY)

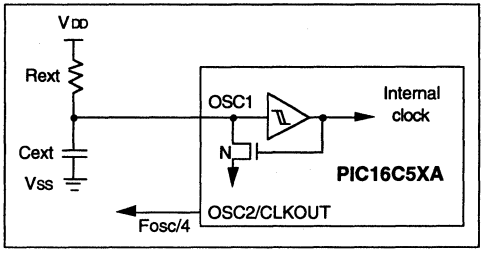
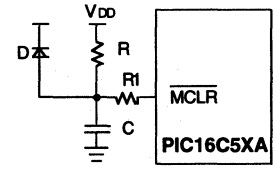


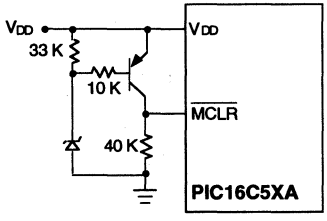
FIGURE 13.1.1 - EXTERNAL POWER ON RESET CIRCUIT (FOR SLOW POWER-UP)



Notes:

1. External power on reset circuit is required only if VDD power-up slope is too slow or if a low frequency crystal oscillator is being used that need a long start-up time. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40 KΩ must be observed to make sure that voltage drop across R does not exceed 0.2 V (max leakage current spec on MCLR pin is 5 μA). A larger voltage drop will degrade VIH level on MCLR pin.
3. R1= 100Ω to 1KΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to ESD or EOS.

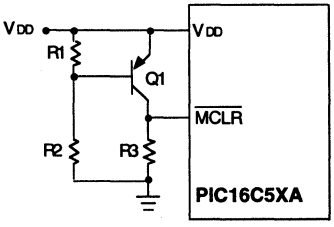
FIGURE 13.1.2 - BROWN OUT PROTECTION CIRCUIT



Notes:

1. This circuit will activate reset when VDD goes below (VZ + 0.7 V) where VZ = Zer voltage.

FIGURE 13.1.3 - BROWN OUT PROTECTION CIRCUIT



Notes:

1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7\ V.$$

13.0 OSCILLATOR START-UP TIMER (OST)

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. An on-chip oscillator start-up timer is provided which keeps the device in a RESET condition for approximately 18ms after the voltage on the MCLR pin has reached a logic high (VIHMC) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The OST will also be triggered upon a watchdog timer timeout. This is particularly important for applications using the WDT to awake the PIC16C54A from SLEEP mode automatically.

The OST is not adequate for low frequency crystals which require much longer than 18ms to start up and stabilize.

13.1 Power-On Reset (POR)

The PIC16C54A incorporates an on chip Power-On Reset (POR) circuitry which provides internal chip reset for most power-up situations. To use this feature the user merely needs to tie MCLR pin to VDD. A simplified block diagram of the on-chip power on reset circuit is shown in Figure 13.1.4. The Power-On Reset circuit and the Oscillator Start-up Timer circuit are closely related. On power-up the reset latch is set and the start-up timer (see Figure 13.1.4) is reset. The start-up timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18ms, it will reset the reset-latch and thus end the on-chip reset signal.

Figures 13.1.5 and 13.1.6 are two power-up situations with relatively fast rise time on VDD. In Figure 13.1.5, VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset tOST ms after MCLR goes high. In Figure 13.1.6, the on-chip Power-On Reset feature is being utilized (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper reset. Figure 13.1.7 depicts a potentially problematic situation where VDD rises too slowly. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is therefore not guaranteed to function correctly.

To summarize, the on chip Power-On Reset is guaranteed to work if the rate of rise of VDD is no slower than 0.05 V/ms. It is also necessary that the VDD starts from 0V. The on chip Power-On Reset is also not adequate for low frequency crystals which require much longer than 18ms to start up and stabilize. For such situations, we recommend that external RC circuits are used for longer Power-On reset.

FIGURE 13.1.4 - SIMPLIFIED POWER-ON RESET BLOCK DIAGRAM

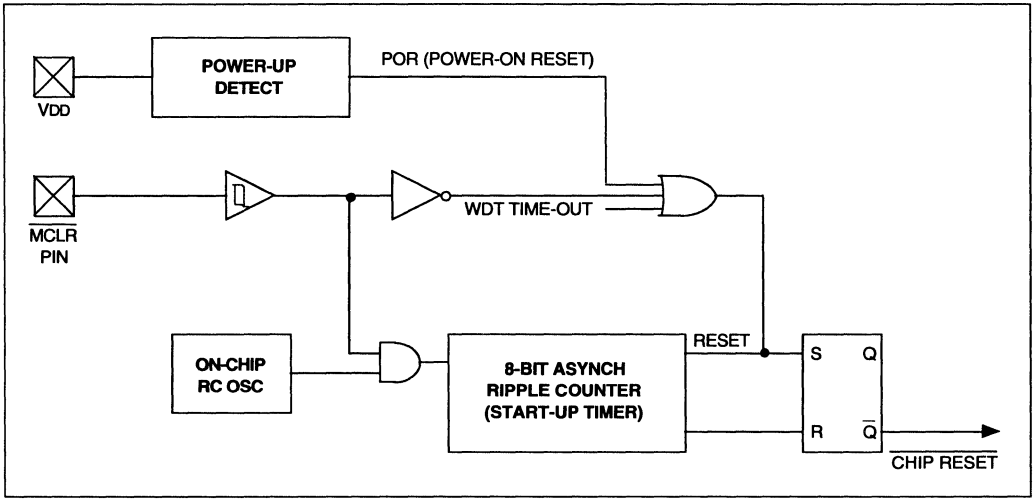
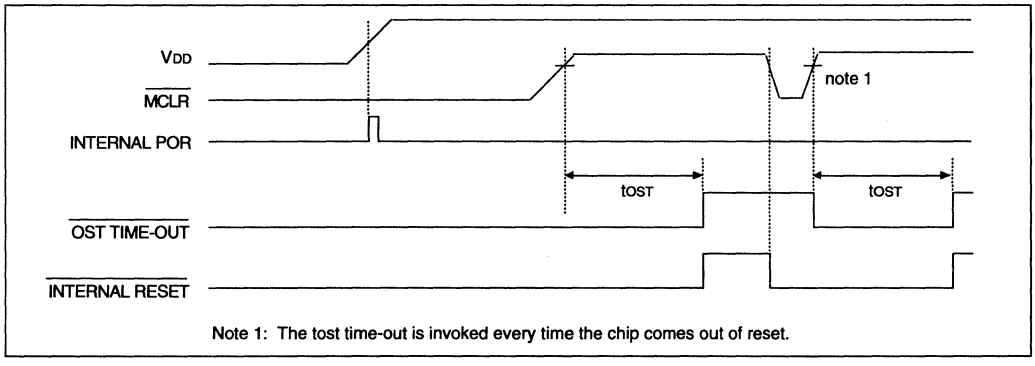
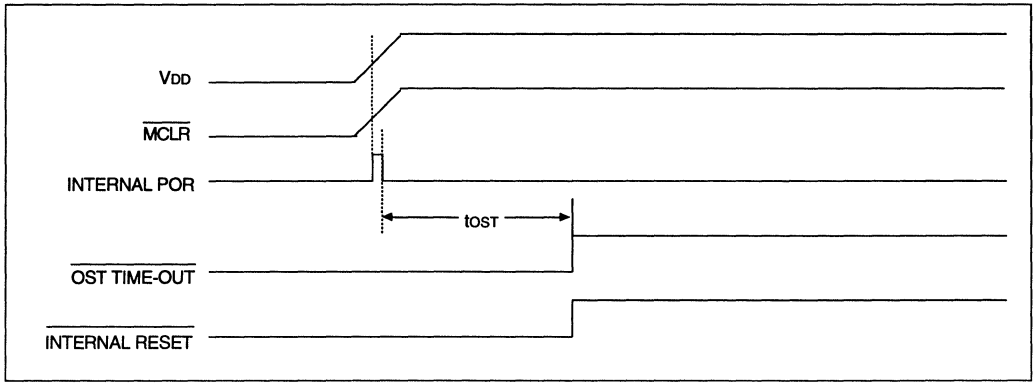


FIGURE 13.1.5 - USING EXTERNAL RESET INPUT



Note 1: The tost time-out is invoked every time the chip comes out of reset.

FIGURE 13.1.6 - USING ON-CHIP POR (FAST VDD RISE TIME)



14.0 POWER DOWN MODE (SLEEP)

The power down mode is entered by executing a SLEEP instruction.

If enabled, the WatchdogTimer will be cleared but keeps running, the bit $\overline{PD}$ in the STATUS register is cleared, the $\overline{TO}$ bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or Vss, with no external circuitry drawing current from the I/O pin. I/O pins that are in the High-Z mode should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC input should also be at VDD or Vss for lowest current consumption.

The $\overline{MCLR}$ pin must be at VIHMC.

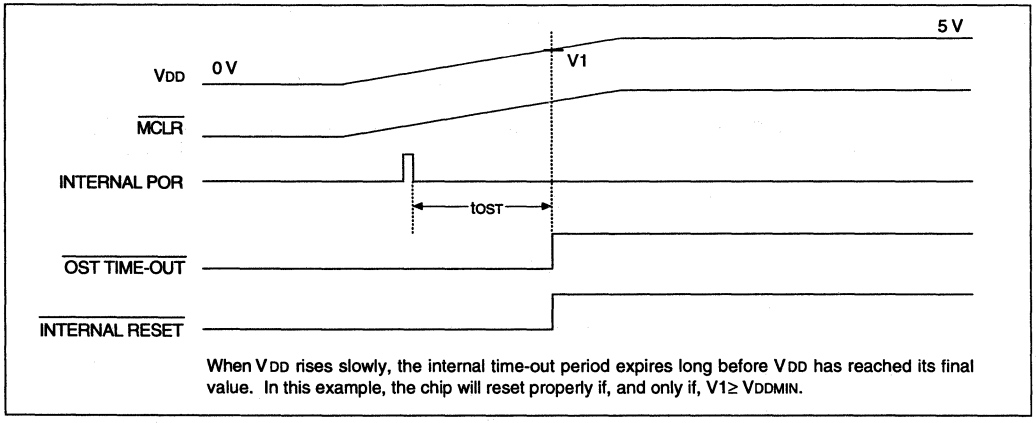
14.1 Wake-Up

The device can be awakened by a Watchdog Timer timeout (if it is enabled) or an externally applied "low" pulse at the $\overline{MCLR}$ pin. In both cases the PIC16C54A will stay in RESET mode for one oscillator start-up timer period (triggered from rising edge on $\overline{MCLR}$ or WDT timeout) before normal program execution resumes.

The $\overline{PD}$ bit in the STATUS register, which is set to one during power-on, but cleared by the "SLEEP" command, can be used to determine if the processor was powered up or awakened from the power down mode (Table 4.5.2.2). The $\overline{TO}$ bit in the STATUS register can be used to determine, if the "wake up" was caused by an external $\overline{MCLR}$ signal or a Watchdog Timer timeout.

NOTE: Some applications may require external R/C networks on the $\overline{MCLR}$ pin in order to allow for oscillator start-up times longer than one OST period. In this case, a WDT wake up from power down mode is not recommended, because a RESET generated by a WDT time out does not discharge the external capacitor, and the PIC16C54A will be in RESET only for the Oscillator Start-up Timer period.

FIGURE 13.1.7 - USING ON-CHIP POR (SLOW VDD RISE TIME)



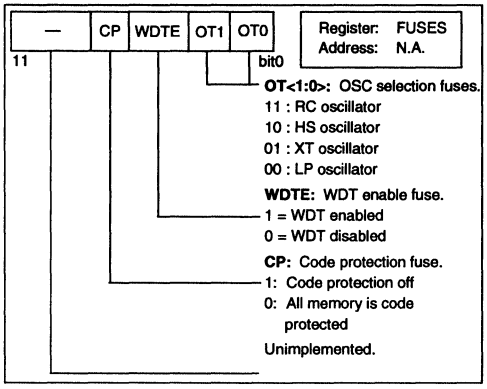
When VDD rises slowly, the internal time-out period expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1≥ VDDMIN.

15.0 CONFIGURATION FUSES

The configuration EPROM consists of four EPROM fuses which are not part of the normal EPROM for program storage.

Two are for the selection of the oscillator type, one is the Watchdog Timer enable fuse, and one is the code protection fuse.

FIGURE 15.1: CONFIGURATION WORD



15.1 Customer ID Code

The PIC16C54A series has 16 special EPROM bits which are not part of the normal program memory. These bits are available to the user to store an Identifier (ID) code, checksum, or other informative data. They cannot be accessed during normal program execution.

15.2 Code Protection

The program code written into the EPROM can be protected by programming the code protection fuse with "0".

When code protected, the contents of the program EPROM cannot be read out in a way that the program code can be reconstructed. In addition, all memory locations starting at 040h and above are protected against programming.

It is still possible to program locations 000h - 03Fh, the ID locations and the configuration fuses.

Note that the configuration fuses and the ID bits can still be read, even if the code protection logic is active.

15.2.1 VERIFYING A CODE-PROTECTED PART

When code protected verifying any program memory location will read a scrambled output which looks like "00000000XXXX" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

a. First, program and verify a good device without code protecting it.
b. Next, blow its code protection fuse and then load its contents in a file.
c. Verify any code-protected PIC16C54A against this file.

2

16.0 ELECTRICAL CHARACTERISTICS

16.1 Absolute Maximum Ratings*

Ambient temperature under bias ..... -55°C to +125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss
(except VDD and MCLR) ..... -0.6V to VDD +0.6V
Voltage on VDD with respect to Vss ..... 0 to +7.5 V
Voltage on MCLR with respect to Vss
(Note 2) ..... 0 to +14 V
Total power Dissipation (Note 1) 800mW
Max. Current out of Vss pin 150mA
Max. Current into VDD pin 50mA
Max. Current into an input pin ..... ±500µA
Input clamp current, IIK (VI<0 or VI<VDD) ..... ±20mA
Output clamp current, IOK (V0<0 or V0<VDD) .. ±20mA
Max. Output Current sinked by any I/O pin 25mA
Max. Output Current sourced by any I/O pin 20mA
Max. Output Current sourced by a single
I/O port (PORT A, B, or C) 40mA
Max. Output Current sinked by a single
I/O port (PORT A, B, or C) 50mA

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
$Pdis = V_{DD} \times \{I_{DD} - \sum Ioh\} + \sum\{(V_{DD}-Voh) \times Ioh\} + \sum(Vol \times Iol)$

TABLE 16.2 - PIN DESCRIPTIONS

Name	Function	Description
RA0 - RA3	I/O PORTA	4 input/output lines.
RB0 - RB7	I/O PORTB	8 input/output lines.
RTCC	Real Time Clock/Counter	Schmitt Trigger Input. Clock input to RTCC register. Must be tied to Vss or VDD if not in use to avoid unintended entering of test modes and to reduce current consumption.
MCLR	Master Clear	Schmitt Trigger Input. A "Low" voltage on this input generates a RESET condition for the PIC16C54A microcontroller. A rising voltage triggers the on-chip oscillator start-up timer which keeps the chip in RESET mode for about 18ms. This input must be tied directly, or via a pull-up resistor, to VDD.
OSC1	Oscillator (input)	"XT", "HS" and "LP" devices: Input terminal for crystal, ceramic resonator, or external clock generator. "RC" devices : Driver terminal for external RC combination to establish oscillation.
OSC2/CLKOUT	Oscillator (output)	For "XT", "HS" and "LP" devices: Output terminal for crystal and ceramic resonator. Do not connect any other load to this output. Leave open if external clock generator is used. For "RC" devices : A "CLKOUT" signal with a frequency of 1/4 Fosc1 is put out on this pin.
VDD	Power supply	
Vss	Ground	
N/C	No (internal) Connection	

16.3 DC CHARACTERISTICS: PIC16C54A-04 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial					
Characteristic	**Sym**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	3.0		6.25	V	XT, RC and LP options
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on
Supply Current (Note 2)	IDD					XT and RC options
			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
						LP option, Commercial
			15		µA	FOSC = 32 KHz, VDD = 3.0V, WDT disabled
						LP option, Industrial
			19		µA	FOSC = 32 KHz, VDD = 3.0V, WDT disabled
Power Down Current (Note 4)						
WDT enabled	IPD		4	12	µA	VDD = 3.0V, Commercial
			5	14	µA	VDD = 3.0V, Industrial
WDT disabled			0.6	9	µA	VDD = 3.0V, Commercial
			0.8	12	µA	VDD = 3.0V, Industrial

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.4 DC CHARACTERISTICS: PIC16C54A-10 (COMMERCIAL, INDUSTRIAL) PIC16C54A-20 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS		Standard Operating Conditions Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Characteristic	**Sym**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	3.0 4.5		6.25 5.5	V V	XT and RC options HS option
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on
Supply Current (Note 2)	IDD					XT and RC options
			1.8		mA	FOSC = 4 MHz, VDD = 5.5V
						HS option
			4.8	10	mA	FOSC = 10 MHz , VDD = 5.5V
			9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
Power Down Current (Note 4)						
WDT enabled	IPD		4	12	µA	VDD = 3.0V, Commercial
			5	14	µA	VDD = 3.0V, Industrial
WDT disabled			0.6	9	µA	VDD = 3.0V, Commercial
			0.8	12	µA	VDD = 3.0V, Industrial

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.5 DC CHARACTERISTICS: PIC16LC54A-04 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial					
Characteristic	**Sym**	**Min**	**Typ ***	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.5		6.25	V	XT, RC and LP options
		4.5		5.5	V	HS option
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on reset
Supply Current (Note 2)	IDD					XT and RC options
			1.8		mA	FOSC = 4 MHz, VDD = 5.5V
						HS option
			4.8		mA	FOSC = 4 MHz, VDD = 5.5V
			15	32	µA	LP option, Commercial
						FOSC = 32 KHz, VDD = 2.5V, WDT disabled
						LP option, Industrial
			19	40	µA	FOSC = 32 KHz, VDD = 2.5V, WDT disabled
Power Down Current (Note 4)						
WDT enabled	IPD		4	12	µA	VDD = 2.5V, Commercial
			5	14	µA	VDD = 2.5V, Industrial
WDT disabled			0.6	9	µA	VDD = 2.5V, Commercial
			0.8	12	µA	VDD = 2.5V, Industrial

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
a) The test conditions for all IDD measurements in active operation mode are:
OSC1= external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.6 DC CHARACTERISTICS: PIC16C54A-04 (COMMERCIAL, INDUSTRIAL)
PIC16LC54A-04 (COMMERCIAL, INDUSTRIAL)
PIC16C54A-10 (COMMERCIAL, INDUSTRIAL)
PIC16C54A-20 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY

Standard Operating Conditions
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Input Low Voltage						
I/O ports	VIL	VSS		0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt trigger)		VSS		0.15 VDD	V	
RTCC (Schmitt trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt trigger)		VSS		0.15 VDD	V	RC option only (Note 5)
OSC1		VSS		0.3 VDD	V	XT, HS and LP options
Input High Voltage						
I/O ports	VIH	0.2 VDD+1V		VDD	V	For all VDD (Note 6)
		2.0		VDD	V	4.0 V < VDD ≤ 5.5 V (Note 6)
MCLR (Schmitt trigger)		0.85 VDD		VDD	V	
RTCC (Schmitt trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt trigger)		0.85 VDD		VDD	V	RC option only (Note 5)
OSC1		0.7 VDD		VDD	V	XT, HS and LP options
Input Leakage Current (Note 4)						**For VDD ≤ 5.5V**
I/O ports	IIL	-1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		-5			µA	VPIN = VSS + 0.25V (Note 3)
MCLR			0.5	+5	µA	VPIN = VDD (Note 3)
RTCC		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD , XT, HS and LP options
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT (RC option only)				0.6	V	IOL = 1.6 mA, VDD = 4.5V
Output High Voltage						
I/O Ports (Note 4)	VOH	VDD-0.7			V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT (RC option only)		VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : In RC oscillator mode, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C54A be driven with external clock in RC mode.

Note 6: The user may use better of the two specifications.

16.7 AC CHARACTERISTICS: PIC16C54A-04 (COMMERCIAL, INDUSTRIAL) PIC16C54A-10 (COMMERCIAL, INDUSTRIAL) PIC16C54A-20 (COMMERCIAL, INDUSTRIAL)

AC CHARACTERISTICS **Standard Operating Conditions**
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
External CLOCKIN Frequency (Note 2)	FOSC	DC		4	MHz	RC mode
		DC		4	MHz	XT mode
		DC		20	MHz	HS mode (Com/Ind) (Note 5)
		DC		200	KHz	LP mode
Oscillator Frequency (Note 2)	FOSC	DC		4	MHz	RC mode
		0.1		4	MHz	XT mode
		4		20	MHz	HS mode (Com/Ind) (Note 5)
		DC		200	KHz	LP mode
Instruction Cycle Time (Note 2)	TCY	1.0		DC	µs	RC mode
		1.0	4/FOSC	DC	µs	XT mode
		0.2		DC	µs	HS mode (Note 5)
		20		DC	µs	LP mode
External Clock in Timing (Note 4)						
Clock in (OSC1) High or Low Time						
XT oscillator type	TCKHLXT	50*			ns	
LP oscillator type	TCKHLLP	2*			µs	
HS oscillator type	TCKHLHS	20*			ns	
Clock in (OSC1) Rise or Fall Time						
XT oscillator type	TCKRFXT	25*			ns	
LP oscillator type	TCKRFLP	50*			ns	
HS oscillator type	TCKRFHS	25*			ns	
RESET Timing						
$\overline{MCLR}$ Pulse Width (low)	TMCL	100*			ns	
RTCC Input Timing, No Prescaler						
RTCC High Pulse Width	TRTH	0.5 TCY+ 20*			ns	Note 3
RTCC Low Pulse Width	TRTL	0.5 TCY+ 20*			ns	Note 3
RTCC Input Timing, With Prescaler						
RTCC High Pulse Width	TRTH	10*			ns	Note 3
RTCC Low Pulse Width	TRTL	10*			ns	Note 3
RTCC Period	TRTP	$\frac{T_{CY} + 40}{N}$ *			ns	Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Timeout Period (No Prescaler)	TWDT	9*	18*	30*	ms	VDD = 5.0V
Oscillation Start-up Timer Period	TOST	9*	18*	30*	ms	VDD = 5.0V
I/O Timing						
I/O Pin Input Valid Before CLKOUT↑ (RC Mode)	TDS	0.25 TCY+ 30*			ns	
I/O Pin Input Hold After CLKOUT↑ (RC Mode)	TDH	0*			ns	
I/O Pin Output Valid After CLKOUT↓ (RC Mode)	TPD			40*	ns	

* Guaranteed by characterization, but not tested.

(Cont. on next page)

16.7 AC CHARACTERISTICS: PIC16C54A-04 (COMMERCIAL, INDUSTRIAL) (Cont.) PIC16C54A-10 (COMMERCIAL, INDUSTRIAL) PIC16C54A-20 (COMMERCIAL, INDUSTRIAL)

AC CHARACTERISTICS **Standard Operating Conditions**
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
I/O Timing (cont.)						
I/O pin input valid before OSC↑ (I/O setup time)	TioV2osH	TBD			ns	
OSC1↑ to I/O pin input invalid (I/O hold time)	TosH2ioL	TBD			ns	
OSC1↑ to I/O pin output valid	TosH2ioV			TBD	ns	
I/O pin output rise time	TioR			TBD	ns	
I/O pin output fall time	TioF			TBD	ns	
Capacitive Loading Specs on Output Pins						
OSC2 pin	COSC2			15	pF	In XT, HS or LP modes when external clock is used to drive OSC1
All I/O pins and OSC2 (in RC mode)	CIO			50	pF	

* Guaranteed by characterization, but not tested.

Note 1. Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2. Instruction cycle period (Tcy) equals four times the input oscillator time base period.
All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Note 3. For a detailed explanation of RTCC input clock requirements see section 4.2.1.

Note 4. Clock-in high-time is the duration for which clock input is at VIHOSC or higher.
Clock-in low-time is the duration for which clock input is at VILOSC or lower.

Note 5. This HS specification is only for the -20 device. The -10 device has a maximum of 10 MHz and the -04 device has a maximum of 4 MHz.

16.8 Electrical Structure of Pins

FIGURE 16.8.1 - ELECTRICAL STRUCTURE OF I/O PINS (RA, RB)

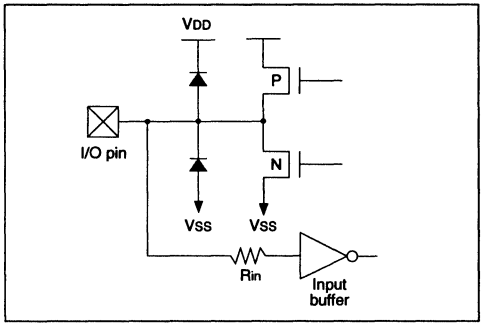
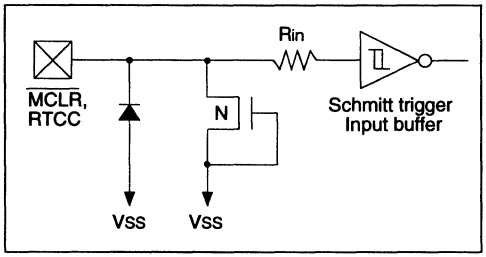


FIGURE 16.8.2 - ELECTRICAL STRUCTURE OF $\overline{MCLR}$ AND RTCC PINS



Notes to Figures 16.7.1 and 16.7.2: The diodes and the grounded gate (or output driver) NMOS device are carefully designed to protect against ESD (Electrostatic discharge) and EOS (Electrical overstress). Rin is a small resistance to further protect the input buffer from ESD.

2

17.0 TIMING DIAGRAMS

FIGURE 17.0.1 - RTCC TIMING

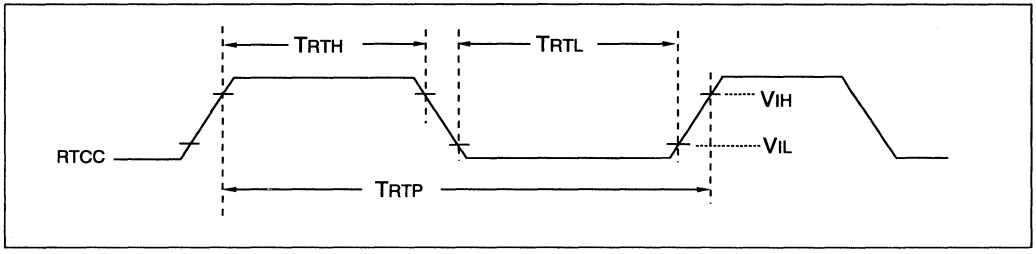


FIGURE 17.0.2 - OSCILLATOR START-UP TIMING (PIC16C54ARC)

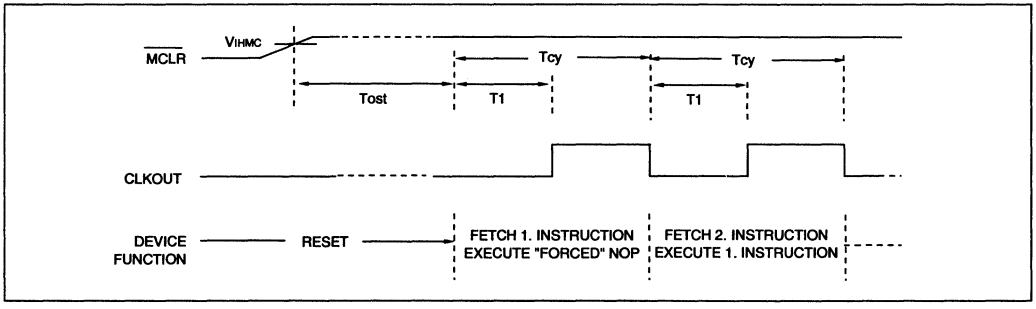
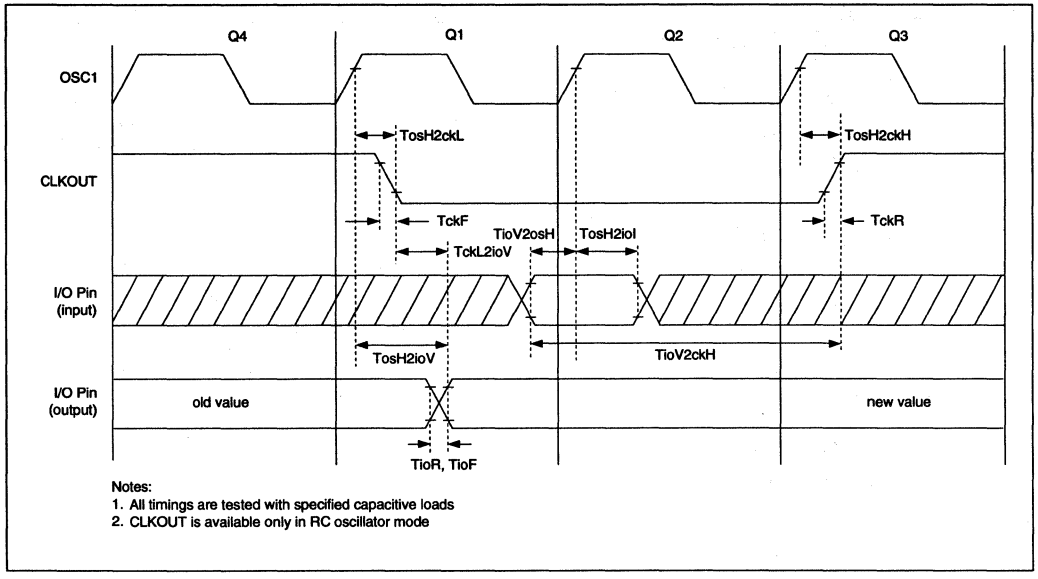


FIGURE 17.0.3 - INPUT/OUTPUT TIMING FOR I/O PORTS



Notes:
1. All timings are tested with specified capacitive loads
2. CLKOUT is available only in RC oscillator mode

18.0 DC & AC CHARACTERISTICS GRAPHS/TABLES

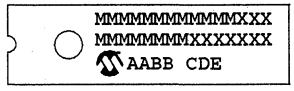
NOT AVAILABLE AT THIS TIME

19.0 PACKAGING INFORMATION

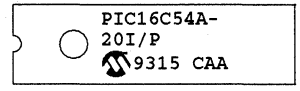
See Section 11 of the Data Book.

19.1 Package Marking Information

18L PDIP

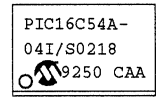


Example

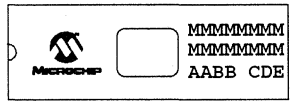


18L SOIC

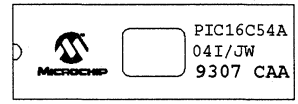
Example



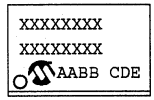
18L Cerdip



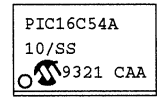
Example



20L SSOP



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.
Note:	In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

*Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are incuded in QTP price.

20.0 DEVELOPMENT SUPPORT

20.1 Development Tools

The PIC16C5X and PIC16CXX microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER™ Real-Time In-Circuit Emulator
- PRO MATE™ Universal Programmer
- PICSTART™ Low-Cost Prototype Programmer
- Assembler
- Software Simulator

20.2 PICMASTER™: High Performance Universal In-Circuit Emulator

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X, PIC16CXX and PIC17CXX families.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16C5X, PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on PC compatible machines ranging from 80286-AT® class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.1 environment, allowing the operator access to a wide range of supporting software and accessories.

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.1 environment was chosen to best make these features available to you, the end user.

The PICMASTER Emulator Universal System consists primarily of four major components:

- Host-Interface Card
- Emulator Control Pod
- Target-Specific Emulator Probe
- PC Host Emulation Control Software

The Windows 3.1 System is a multitasking operating system which will allow the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window.

Dynamic Data Exchange (DDE), a feature of Windows 3.1, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

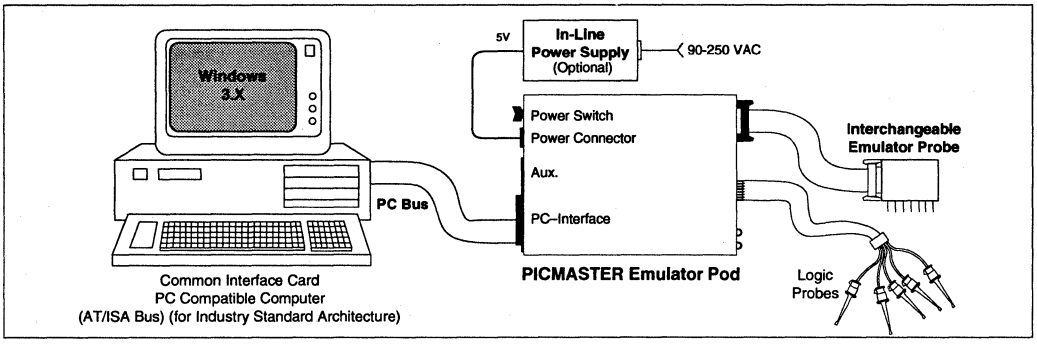
Under Windows 3.1, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16CXX processor and a PIC17CXX processor).

20.3 PRO MATE™: Universal Programmer

The PRO MATE Universal Programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MATE has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability . It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MATE can read, verify or program PIC16C5X, PIC16CXX and PIC17CXX devices. It can also set fuse configuration and code-protect in this mode. Its EEPROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.

FIGURE 20.2 - PICMASTER SYSTEM CONFIGURATION



In PC-hosted mode, the PRO MATE connects to the PC via one of the COM (RS232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of V_{DD} min, V_{DD} max and V_{PP} levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different serial number, sequential or random.

The PRO MATE has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. PRO MATE supports all PIC16C5X, PIC16CXX and PIC17CXX processors.

20.4 PICSTART™ Programmer

The PICSTART™ programmer is an easy to use, very low-cost prototype programmer. It connects to the PC via one of the COM (RS232) ports. A PC based user interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based.

20.5 Assembler (MPASM)

Cross Assembler is a PC hosted symbolic assembler. It supports all microcontroller series including the PIC16C5X CMOS, PIC16CXX and PIC17CXX families.

MPASM offers fully featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from the Microchip Universal Emulator System (PICMASTER).

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro Assembly Capability
- Provides Object, Listing, Symbol and special files required for debugging with one of the Microchip Emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a full feature directive language represented by four basic classes of directives:

- **Data Directives** are those that control the allocation of memory and provide a way to refer to data items symbolically, by meaningful names.
- **Listing Directives** control the MPASM listing dis play. They allow the specification of titles and subtitles, page ejects and other listing control.
- **Control Directives** permit sections of conditionally assembled code.
- **Macro Directives** control the execution and data allocation within macro body definitions.

20.6 Software Simulator (MPSIM)

The Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16C5X and PIC16CXX series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in single step, execute until break or in a trace mode. Two forms of symbolic debugging are available: an internal symbol table for disassembling opcodes and the displaying of source code from a listing file. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

20.7 Development Systems

For convenience, the development tools are packaged into comprehensive systems as listed in Table 20-1:

TABLE 20-1: DEVELOPMENT SYSTEM PACKAGES

Item	Name	System Description
1.	PICMASTER™ System	PICMASTER In-Circuit Emulator with your choice of Target Probe, PRO MATE Programmer, Assembler, Software Simulator and Samples.
2.	PICSTART™ System	PICSTART™ Low-Cost Prototype Programmer, Assembler, Software Simulator and Samples

20.8 Probe Specifications

The PICMASTER probes currently meet the following specifications:

PICMASTER PROBE	Devices Supported	PROBE Maximum Frequency	PROBE Operating Voltage
PROBE - 16A	PIC16C54, PIC16C55, PIC16C56, and PIC16C57	4 MHZ	4.5V - 5.5V
PROBE - 16D	PIC16C54, PIC16C55, PIC16C56, PIC16C57, and PIC16C58	20 MHz	4.5V - 5.5V

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2

CONNECTING TO MICROCHIP BBS

Connect world wide to the Microchip BBS using the Compuserve communications network. In most cases a local call is your only expense. The Microchip BBS connection does not use CompuServe membership services, therefore **you do not need CompuServe membership to join Microchip's BBS.**

The procedure to connect will vary slightly from country to country. Please check with your local CompuServe agent for details if you have a problem. CompuServe services allows multiple users at baud rates up to 9600.

To connect:

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.

2. Dial your local CompuServe phone number.

3. Depress **<ENTER>** and a garbage string will appear because CompuServe is expecting a 7E1 setting.

4. Type **+ <ENTER>** and `Host Name:` will appear.

5. Type **MCHIPBBS<ENTER>** and you will be connected to the Microchip BBS.

In the United States, to find CompuServe's phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600 baud connection. After the system responds with `Host Name:`, type

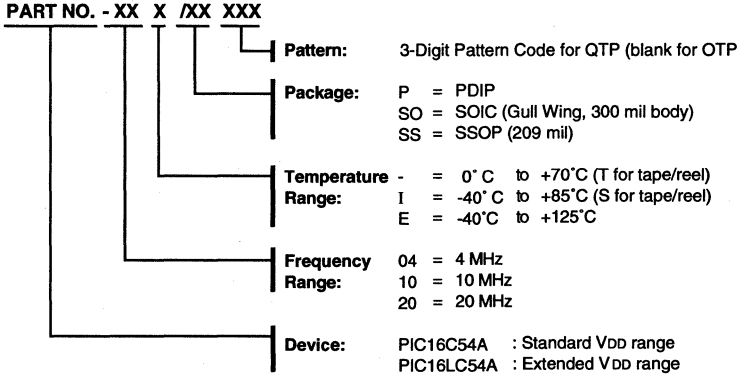
NETWORK<ENTER> and follow CompuServe's directions.

For voice information (or calling from overseas), you may call (614) 457-1550 for your local CompuServe number.

NOTES:

PIC16C54A PRODUCT IDENTIFICATION SYSTEM

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Examples:
a) PIC16C54A - 04/P301 = Commercial temp., PDIP package, 4 MHz, standard VDD limits, QTP pattern # 301
b) PIC16LC54A- 04I /SO = Industrial temp., SOIC package, 4 MHz, extended VDD limits
c) PIC16C54A - 20I /P Industrial temp., PDIP package, 20 MHz, standard VDD limits

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local Compuserve number.

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

PIC16C58A

EPROM-Based 8-Bit CMOS Microcontroller

FEATURES

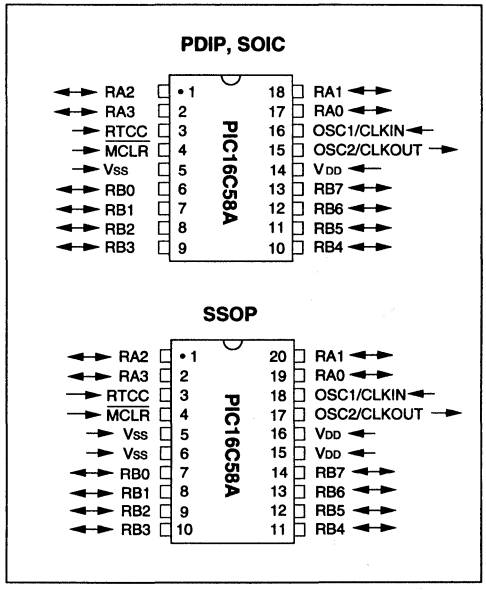
Compatibility
- Pin and software compatible with PIC16C54, PIC16CR54, PIC16C54A and PIC16C56 devices

High-Performance RISC-like CPU
- Only 33 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200ns instruction cycle
- 12-bit wide instructions
- 8-bit wide data path
- 2K x 12 on-chip EPROM program memory
- 72 x 8 general purpose registers (SRAM)
- Eight special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features
- 12 I/O pins with individual direction control
- 8-bit real time clock/counter (RTCC) with 8-bit programmable prescaler
- Power-on Reset
- Oscillator Start-up Timer
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security EPROM fuse for code-protection
- Power saving SLEEP mode
- EPROM fuse selectable oscillator options:
  - Low-cost RC oscillator: RC
  - Standard crystal/resonator: XT
  - High-speed crystal/resonator: HS
  - Power saving, low frequency crystal: LP

CMOS Technology
- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide-operating voltage range for Commercial and Industrial (2.5V to 6.25V)
- Low-power consumption
  - < 2mA typical @ 5V, 4 MHz
  - 15μA typical @ 3V, 32 KHz
  - < 3μA typical standby current (with WDT disabled) @ 3V, 0°C to 70°C

FIGURE A - PIN CONFIGURATIONS



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Preliminary

1.0 GENERAL DESCRIPTION

The PIC16C58A from Microchip Technology is a new member of the family of low-cost, high-performance, fully static, EPROM-based 8-bit CMOS microcontrollers. This device is pin and software compatible with the PIC16C54, PIC16CR54, PIC16C54A and PIC16C56 devices. It employs a RISC-like architecture with only 33 single word/single cycle instructions to learn. All instructions are single cycle (200ns) except for program branches which take two cycles. The PIC16C58A delivers performance an order of magnitude higher than its competitors in similar price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C58A is equipped with special microcontroller-like features that reduce system cost and power requirements. The power on reset and oscillator start up timer eliminate the need for external reset circuitry. There are four user selectable oscillator configurations to choose from, including power saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, watchdog timer and code protection features improve system cost, power and reliablity.

The PIC16C58A is supported by an assembler, a software simulator, an in-circuit emulator and a production quality programmer. All the tools are supported by IBM® PC and compatible machines.

2

TABLE 1.1 - OVERVIEW OF PIC16C5X AND PIC16C5XA DEVICES

Device	Memory Program (12-bit Words)	User RAM (Bytes)	I/O	Package Options
PIC16C54	512 (OTP)	25	12	18-lead windowed CERDIP, 18-lead PDIP (300 mil), 18-lead SOIC (300 mil), 20-lead SSOP
PIC16C54A†				
PIC16CR54	512 (ROM)			
PIC16C55	512 (OTP)	24	21	28-lead windowed CERDIP, 28-lead PDIP (300 and 600 mil), 28-lead SOIC (300 mil), 28-lead SSOP
PIC16C56	1024 (OTP)	25	12	18-lead windowed CERDIP, 18-lead PDIP (300 mil), 18-lead SOIC (300 mil), 20-lead SSOP
PIC16C57	2048 (OTP)	72	21	28-lead windowed CERDIP, 28-lead PDIP (300 and 600 mil), 28-lead SOIC (300 mil), 28-lead SSOP
PIC16CR57A†	2048 (OTP)			
PIC16C58A†	2048 (OTP)	73	12	18-lead windowed CERDIP, 18-lead PDIP (300 mil), 18-lead SOIC (300 mil), 20-lead SSOP

†These devices have a lower voltage operation.

1.1 Applications

The PIC16C58A device fits perfectly in applications ranging from high speed automotive and appliance motor control to battery powered remote transmitters/ receivers, low-power pointing devices and telecom processors. The small footprint packages for through-hole or surface mounting make this microcontroller perfect for all applications with space limitations. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the PIC16C58A very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

TABLE 1.0.2 - CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	C-04	C-20	LC-04
RC	VDD: 3.0V to 6.25V Idd: 3.3mA Max. at 5.5V Ipd: 9uA Max. at 3V WDT dis Freq.: 4MHz Max.	VDD: 4.5V to 5.5V Idd: 1.8mA typ. at 5.5V Ipd: 0.6uA typ. at 3V WDT dis Freq.: 4 MHz Max.	VDD: 2.5 to 5.5V Idd: 1.8mA typ at 5.5V Ipd: 0.6uA typ at 3V WDT dis Freq.: 4MHz Typ.
XT	VDD: 3.0V to 6.25V Idd: 3.3mA Max. at 5.5V Ipd: 9uA Max. at 3V WDT dis Freq.: 4MHz Max.	VDD: 4.5V to 5.5V Idd: 1.8mA typ. at 5.5V Ipd: 0.6uA typ. at 3V WDT dis Freq.: 4 MHz Max.	VDD: 2.5 to 5.5V Idd: 1.8mA typ at 5.5V Ipd: 0.6uA typ at 3V WDT dis Freq.: 4MHz Typ.
HS	VDD: 4.5V to 5.5V Idd: 9mA Typ. at 5.5V Ipd: 0.6uA Typ. at 4.5V WDT dis Freq.: 4MHz	VDD: 4.5V to 5.5V Idd: 20mA Max. at 5.5Vtyp at 5.5V Ipd: 0.6uA typ. at 4.5V WDT dis Freq.: 20 MHz Max.	Do not use in HS mode
LP	VDD: 3.0V to 6.25V Idd: 15uA Typ. at 32 KHz, 3.0V Ipd: 0.6uA Typ. at 3.0V WDT dis Freq.: 200KHz Typ.	Do not use in LP mode	VDD: 2.5 to 6.25V Idd: 32uA Max. at 32KHz, 3.0V Ipd: 9uA Max. at 3.0V WDT dis Freq.: 200KHz Max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user selects the device type that guarantees the specifications required.

2.0 ARCHITECTURAL DESCRIPTION

2.1 Harvard Architecture

The PIC16C58A single-chip microcomputer is a low-power, high-speed, fully static CMOS device containing EPROM, RAM, I/O and a Central Processing Unit on a single chip.

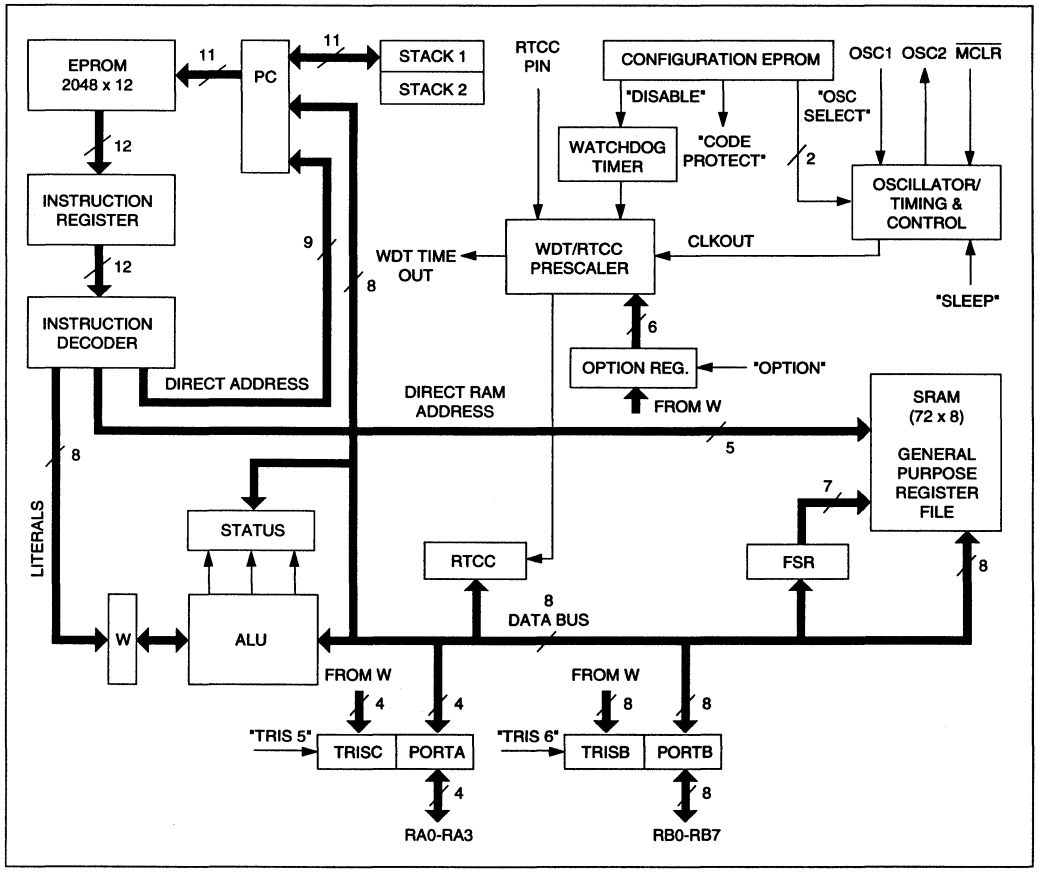
The architecture is based on a register file concept with separate bus and memories for data and instructions (Harvard architecture). The data bus and memory (RAM) are 8-bits wide while the program bus and program memory (EPROM) have a width of 12-bits. This concept allows a simple yet powerful instruction set designed to emphasize bit, byte and register operations under high speed with overlapping instruction fetch and execution cycles. This means that, while one instruction is executed, the following instruction is already being read from the program memory. A block diagram of the PIC16C58A is given in Figure 2.1.

TABLE 2.1 - PIN FUNCTIONS

Name	Function
RA0 - RA3	I/O PORTA
RB0 - RB7	I/O PORTB
RTCC	Real Time Clock/Counter
$\overline{MCLR}$	Master Clear
OSC1/CLKIN	Oscillator (input)
OSC2/CLKOUT	Oscillator (output)
VDD	Power supply
VSS	Ground

2

FIGURE 2.1 - PIC16C58A BLOCK DIAGRAM



2.2 Clocking Scheme/Instruction Cycle

The clock input (from pin OSC1/CLKIN) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1, an instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 2.2.

2.3 Data Register File

The 8-bit data bus connects two basic functional elements together: the Register File composed of 80 addressable 8-bit registers including the I/O Ports and an 8-bit wide Arithmetic Logic Unit. The first 32 bytes of the register file is directly addressable. A "banking" scheme, with banks of 16 bytes each, is employed to address 80 byte data memory (Figure 4.2). Data can be addressed directly or indirectly using the file select register. Immediate data addressing is supported by special "literal" instructions which load data from program memory into the W register.

The register file is divided into two functional groups: operational registers and general purpose registers. The operational registers include the Real Time Clock Counter (RTCC) register, the Program Counter (PC), the Status Register, the I/O registers (PORTs), and the File Select Register. The general purpose registers are used for data and control information under command of the instructions.

In addition, special purpose registers are used to control the I/O port configuration, and the prescaler options.

2.4 Arithmetic/Logic Unit (ALU)

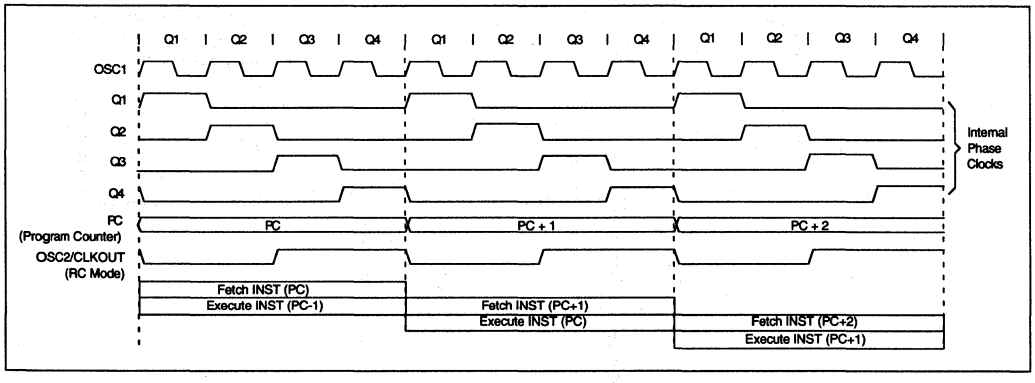
The 8-bit wide ALU contains one temporary working register (W Register). It performs arithmetic and Boolean functions between data held in the W Register and any file register. It also does single operand operations on either the W register or any file register.

2.5 Program Memory

2048 words of 12-bit wide on-chip program memory (EPROM) are available. The memory can be directly addressed in pages of 512 words.

Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations supporting direct, indirect and relative addressing modes can be performed by Bit Test and Skip instructions, Call instructions and Jump instructions or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting.

FIGURE 2.2 - CLOCKS/INSTRUCTION CYCLE



3.0 PIC16C58A SERIES OVERVIEW

A wide variety of oscillator types, frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information and tables in this section. When placing orders, please use the "PIC16C58A Product Identification System" on the back page of this data sheet to specify the correct part number.

3.1 UV Erasable Devices

These devices are optimal for prototype development and pilot series. The desired oscillator configuration is EPROM programmable as "RC", "XT", "HS" or "LP". An erased device is configured as "RC" type by default. Depending on the selected oscillator type and frequency, the operating supply voltage must be within the same range as a OTP/QTP part would be specified for.

The available PIC16C5X development tools (PICSTART™ and PRO MATE™) can program all PIC16C5X devices for prototyping. PRO MATE is recommended for production programming.

3.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The program EPROM is erased allowing the user to write the application code into it. In addition, the watchdog timer can be disabled and/or the code protection logic can be activated by programming special EPROM fuses. The sixteen special EPROM bits for an identification (ID) code storage are also user programmable.

3.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium-to-high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

4.0 OPERATIONAL REGISTER FILES

4.1 Indirect Data Addressing (INDF)

This is not a physically implemented register. Addressing INDF calls for the contents of the File Select Register to be used to select a file register. The INDF register is useful as an indirect address pointer. For example, in the instruction `ADDWF INDF, W` will add the contents of the register pointed to by the FSR to the content of the W Register and place the result in W.

If INDF itself is read through indirect addressing (i.e. FSR = 0h), then 00h is read. If the INDF register is written to via indirect addressing, the result will be a no operation (NOP).

4.2 Real Time Clock/Counter Register (RTCC)

This register can be loaded and read by the program as any other register. In addition, its contents can be incremented by an external signal edge applied to the RTCC pin or by the internal instruction cycle clock (CLKOUT=fosc/4). Figure 4.1 is a simplified block diagram of the RTCC module.

An 8-bit prescaler can be assigned to the RTCC by writing the proper values to the PSA bit and the PS bits in the OPTION register. The OPTION register is a special register (not mapped in data memory) addressable using the 'OPTION' instruction. See section 7.5 for details. If the prescaler is assigned to the RTCC, instructions writing to the RTCC register (e.g. `CLRF RTCC`, or `BSF RTCC,5`, ...etc.) clear the prescaler.

The bit "RTS" (RTCC signal Source) in the OPTION register determines if the RTCC register is incremented internally or externally.

RTS=1: The clock source for the RTCC or the prescaler, if assigned to it, is the signal on the RTCC pin. Bit 4 of the OPTION register (RTE) determines if an increment occurs on the falling (RTE=1) or rising (RTE=0) edge of the signal presented to the RTCC pin.

RTS=0: The RTCC register or its prescaler, respectively, will be incremented with the internal instruction clock (= Fosc/4). The "RTE" bit in the OPTION register and the RTCC pin are "don't care" in this case. However, the RTCC pin must not be left floating (tie to VDD or VSS). This prevents unintended operation and to reduce the current consumption in low-power applications.

As long as clocks are applied to the RTCC (from internal or external source, with or without prescaler), the RTCC register keeps incrementing and just rolls over when the value "FFh" is reached. All increment pulses for the RTCC register are delayed by two instruction cycles. After writing to the RTCC register, for example, no increment takes place for the following two instruction cycles. This is independent if internal or external clock source is selected. If a prescaler is assigned to the RTCC, the output of the prescaler will be delayed by two cycles before the RTCC register is incremented. This is true for instructions that either write to or read-modify-write RTCC (e.g. `MOVF RTCC, CLRF RTCC`). For applications where RTCC needs to be tested for zero without affecting its count, use of the `MOVF RTCC, W` instruction is recommended. Timing diagrams in Figure 4.3 show RTCC read, write and increment timing.

4.2.1 USING RTCC WITH EXTERNAL CLOCK

When external clock input is used for RTCC, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements. Also there is some delay from the occurance of the external clock edge to the actual incrementing of RTCC. Referring to Figure 4.1, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where:

tosc = oscillator time period.

When no prescaler is used, PSOUT (Prescaler output, see Figure 4.1) is the same as RTCC clock input and, therefore, the requirements are:

T_{RTH} = RTCC high time ≥ 2 tosc + 20 ns

T_{RTL} = RTCC low time ≥ 2 tosc + 20 ns

When prescaler is used, the RTCC input is divided by the asynchronous ripple counter-type prescaler so the prescaler output is symmetrical.

Then: PSOUT high time = PSOUT low time = $\frac{N \cdot T_{RT}}{2}$

where T_{RT} = RTCC input period and N = prescale value (2, 4, ..., 256). The requirement is, therefore, $\frac{N \cdot T_{RT}}{2}$ ≥ 2 tosc + 20 ns, or $T_{RT} \geq \frac{4 \text{ tosc} + 40 \text{ ns}}{N}$.

The user will notice that no requirement on RTCC high time or low time is specified. However, if the high time or low time on RTCC is too small, then the pulse may not be detected. Hence, a minimum high or low time of 10 ns is required. In summary, the RTCC input requirements are:

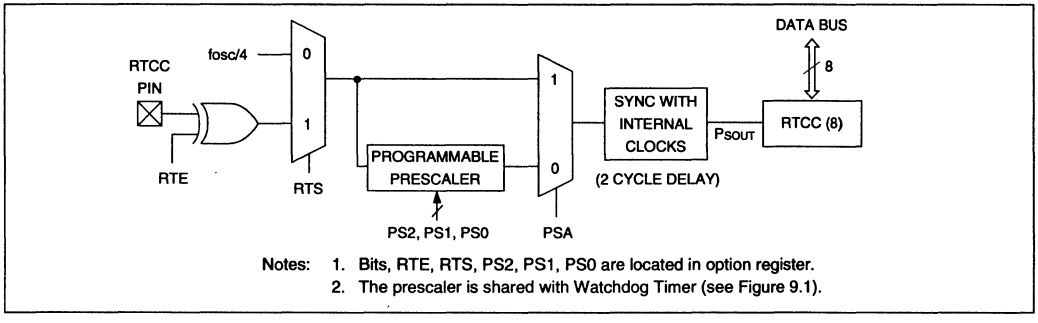
T_{RT} = RTCC period ≥ (4 tosc + 40 ns)/N

T_{RTH} = RTCC high time ≥ 10 ns

T_{RTL} = RTCC low time ≥ 10 ns

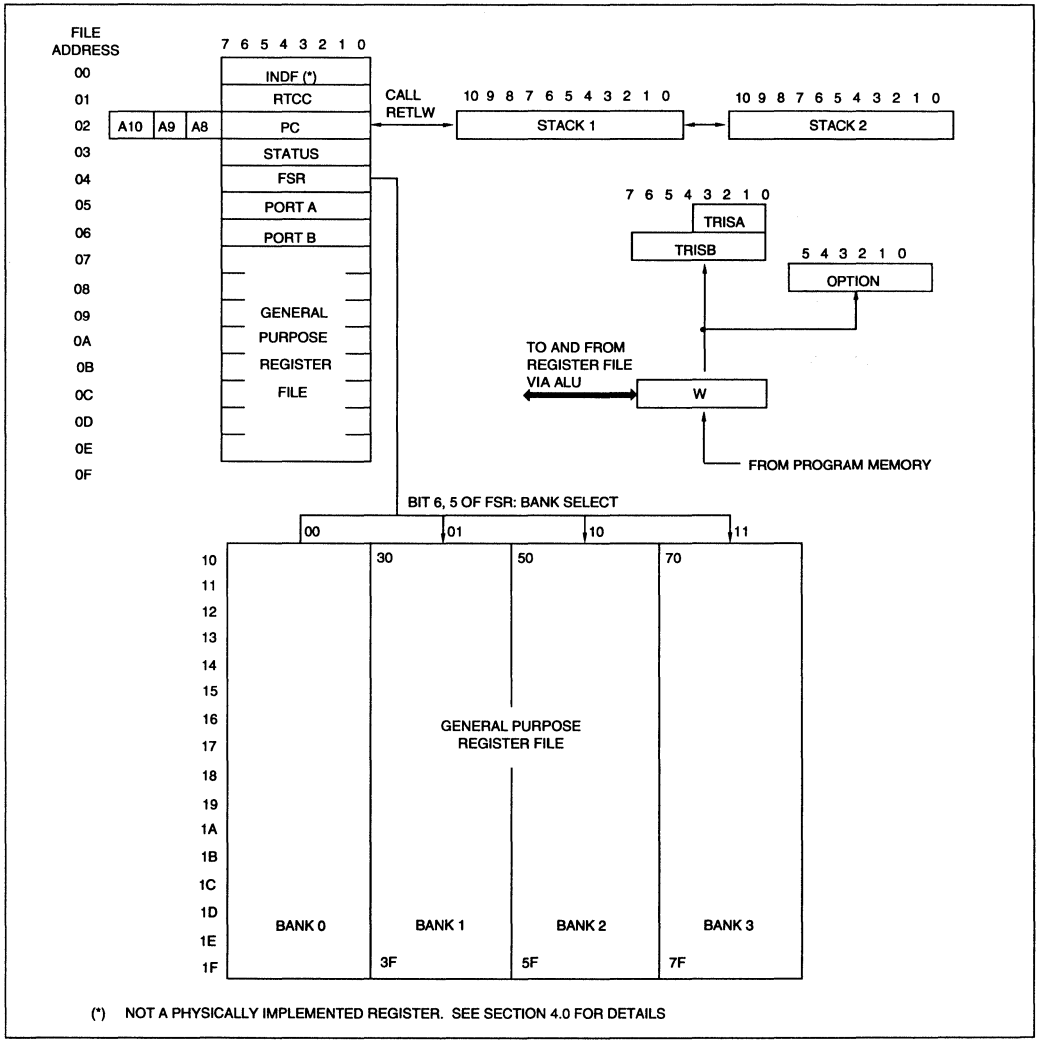
Delay from external clock edge: Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the RTCC is actually incremented. This delay is between 3 tosc and 7 tosc (see Figure 4.4). Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±200 ns @ 20 MHz).

FIGURE 4.1 - RTCC BLOCK DIAGRAM (SIMPLIFIED)



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 are located in option register.
2. The prescaler is shared with Watchdog Timer (see Figure 9.1).

FIGURE 4.2 - PIC16C58A DATA MEMORY MAP



(*) NOT A PHYSICALLY IMPLEMENTED REGISTER. SEE SECTION 4.0 FOR DETAILS

FIGURE 4.3A - RTCC TIMING: INT CLOCK/NO PRESCALE

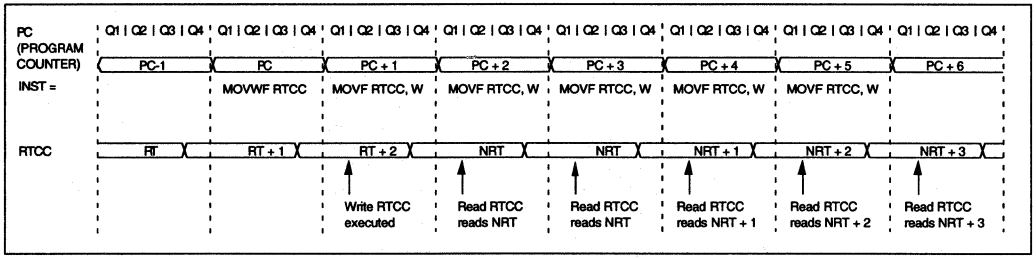


FIGURE 4.3B - RTCC TIMING: INT CLOCK/PRESCALE 1:2

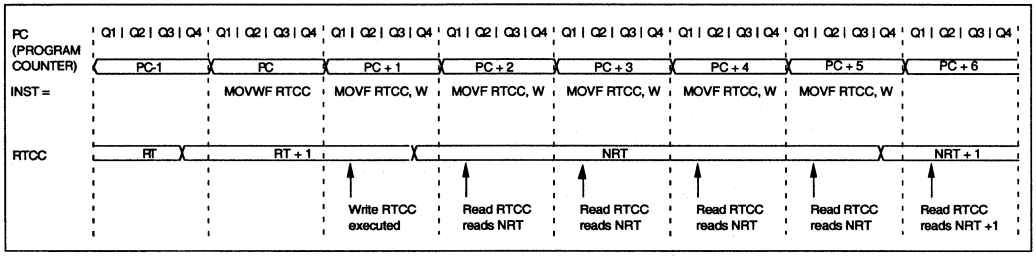
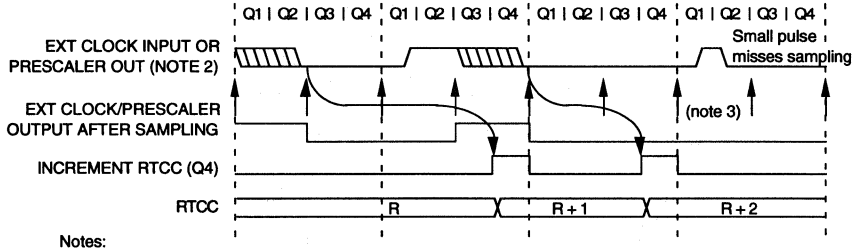


FIGURE 4.4 - RTCC TIMING WITH EXTERNAL CLOCK



Notes:

1. Delay from clock input change to RTCC increment is 3 tosc to 7 tosc. (Duration of Q = tosc). Therefore, the error in measuring the interval between two edges on RTCC input = ± 4 tosc max.
2. External clock if no prescaler selected, Prescaler output otherwise.
3. The arrows indicate the points in time where sampling occurs.

4.3 Program Counter

The program counter generates the addresses for on-chip EPROM containing the program instruction words (Figure 4.5).

The program counter is set to all "1"s upon a RESET condition. During program execution, it is auto incremented with each instruction unless the result of that instruction changes the PC itself:

a) GOTO instructions allow the direct loading of the lower nine program counter bits (PC <8:0>). The upper two bits of PC (PC<10:9>) are loaded with page select bits PA1, PA0 (bits 6,5 status register). Thus GOTO permits jumping to any location on any page.

b) CALL instructions load the lower 8-bits of the PC directly while the 9-bits is cleared to "0". The PC value, incremented by one, will be pushed into the stack. The upper two bits of PC (PC<10:9>) are loaded with Page Select bits PA1, PA0 (STATUS <6:5>).

c) RETLW instructions load the program counter with the top of stack contents.

d) If the PC is the destination in any instruction (e.g. MOVWF PC, ADDWF PC, or BSF PC,5), then the computed 8-bit result will be loaded into the low 8-bits of program counter. The ninth bit of PC will be cleared. PC<10:9> will be loaded with Page Select bits PA1, PA0 (STATUS <6:5>).

It should be noted that because bit 8 (ninth bit) of PC is cleared in CALL instruction or any instruction which writes to the PC (e.g. MOVWF PC), all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

Incrementing the program counter when it is pointing to the last address of a selected memory page is also possible and will cause the program to continue in the next higher page. However, the page pre-select bits in the STATUS register will not be changed and the next GOTO, CALL, ADDWF PC, MOVWF PC instruction will return to the previous page unless the page pre-select bits have been updated under program control. For example, a NOP at location "1FF" (page 0) increments the PC to "200" (page 1). A "GOTO xxx" at "200" will return the program to address "xxx" on page "0" (assuming that the page preselect bits in The STATUS register are "0").

Upon a RESET condition, page 0 is pre-selected while the program counter addresses the last location in the last page. Thus, a GOTO instruction at this location will automatically cause the program to continue in page 0.

4.4 Stack

The PIC16C58A employs a two-level hardware push/pop stack (Figure 4.5).

The CALL instruction pushes the current program counter value, incremented by "1", into stack level 1. Stack level 1 is automatically pushed to level 2. If more than 2 subsequent "CALL"s are executed, only the most recent two return addresses are stored.

The page preselect bits of the STATUS register will be loaded into the most significant bits of the program counter. The ninth bit is always cleared to "0" upon a CALL instruction. This means that subroutine entry addresses have to be located always within the lower half of a memory page (addresses 000-0FF, 200-2FF, 400-4FF, 600-6FF). However, as the stack has the same width as the PC, subroutines can be called from anywhere in the program.

The RETLW instruction loads the contents of the stack level 1 into the program counter while stack level 2 gets copied into level 1. If more than 2 subsequent "RETLW"s are executed, the stack will be filled with the address previously stored in level 2. The return will be always to the page from where the subroutine was called, regardless of the current setting of the page pre-select bits in the STATUS register. Note that the W register will be loaded with the literal value specified in the RETLW instruction. This is particularly useful for the implementation of "data" tables within the program memory.

4.5 Status Word Register

This register contains the arithmetic status of the ALU, the RESET status and page preselect bits for program memory.

The STATUS register can be destination for any instruction like any other register. However, the status bits are set after the write. Furthermore, $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with status register as destination may be different than intended. For example, CLRF STATUS will clear all bits except for $\overline{TO}$ and $\overline{PD}$ and then set the Z bit and leave status register as 000UU100 (where U = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the status registers because these instructions do not affect any status bit.

For other instructions, affecting any status bits, see section "Instruction Set Summary" (Table 10.1).

4.5.1 CARRY/BORROW AND DIGIT CARRY/ BORROW BITS:

The carry bit (C) is a carry out in addition operation (ADDWF) and a borrow out in subtract operation (SUBWF).

It is also affected by RRF and RLF instructions. The following examples explain carry/borrow bit operation:

```
;SUBWF Example #1
;
clrf   0x1f        ;f(1fh)=0
movlw  1           ;wreg=1
subwf  0x1f        ;f(1fh) =f(1fh)- wreg
                   ;=0-1=FFh
                   ;Carry=0: Result is
                       negative
;
;SUBWF Example #2
movlw  0xFF        ;
movwf  0x1F        ;f(0x1F)=FFh
clrw               ;wreg=0
subwf  0x1F        ;f(0x1F)=f(0x1F)-wreg
                   ;=FFh-0=FFh
                   ;Carry=1:Result is
                       positive
;
```

The digit carry operates in the same way as the carry bit, i.e. it is a borrow in a subtract operation.

FIGURE 4.5 - PROGRAM MEMORY ORGANIZATION

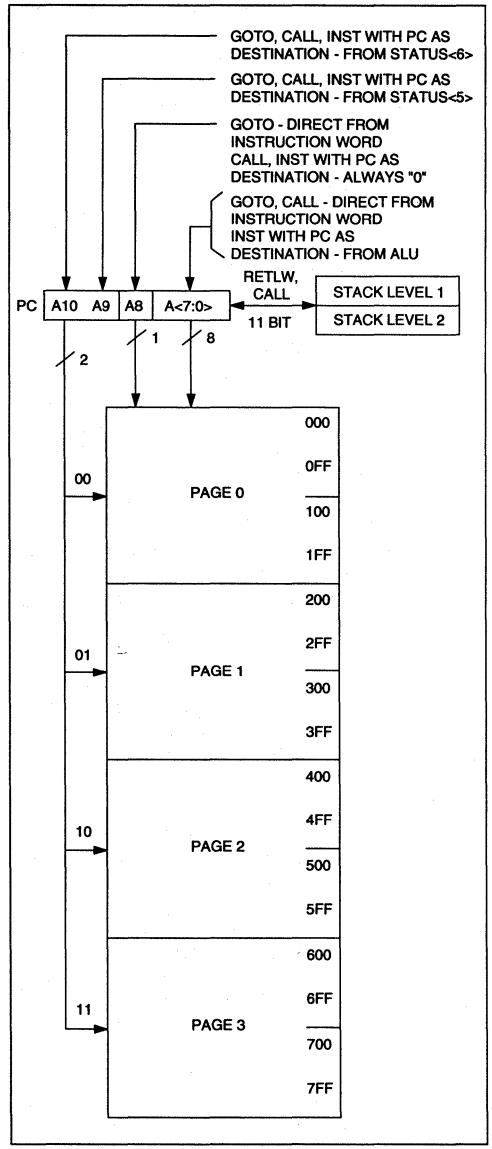
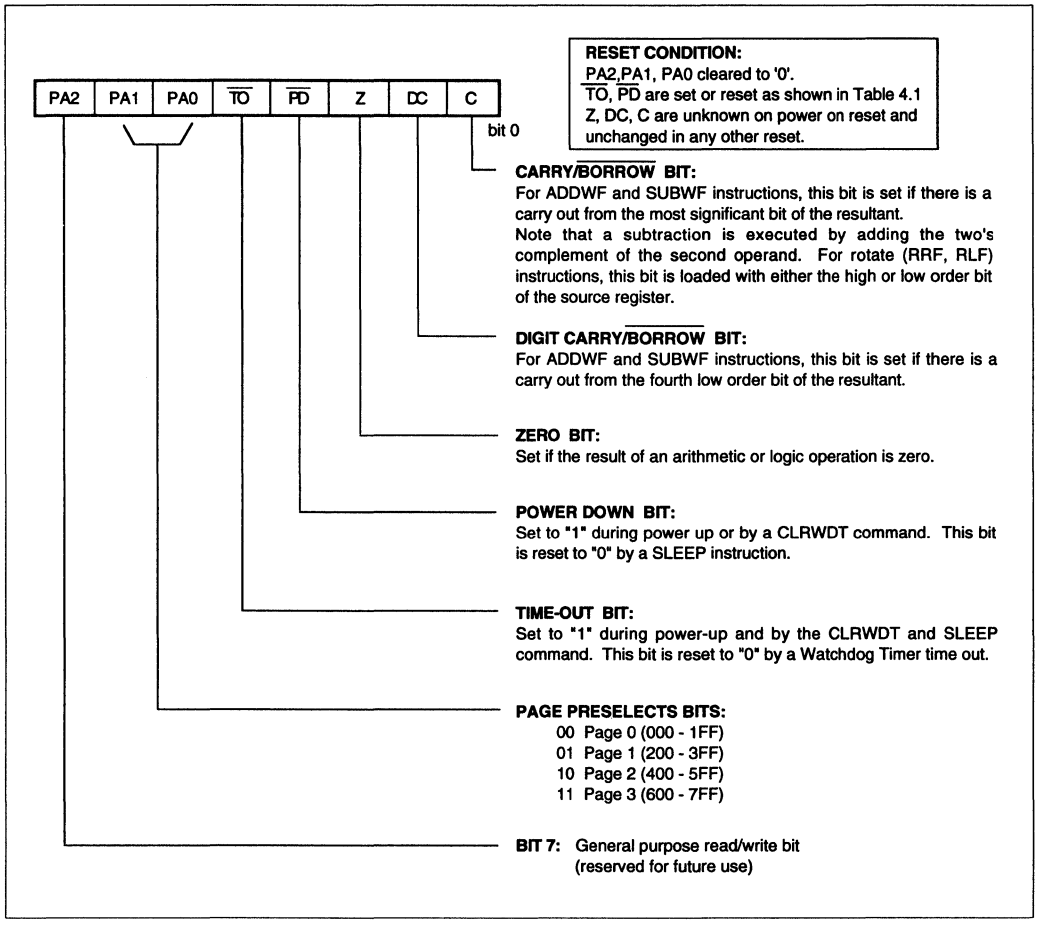


FIGURE 4.6 - STATUS WORD REGISTER



2

4.5.2 TIME OUT AND POWER DOWN STATUS BITS ($\overline{TO}$, $\overline{PD}$)

The $\overline{TO}$ and $\overline{PD}$ bits in the status register can be tested to determine if a RESET condition has been caused by a Watchdog Timer time-out, a power-up condition, or a wake-up from SLEEP by the Watchdog Timer or $\overline{MCLR}$ pin.

These status bits are only affected by events listed in Table 4.1.

TABLE 4.1 - EVENTS AFFECTING $\overline{PD}$/$\overline{TO}$ STATUS BITS

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
WDT Timeout	0	X	No effect on PD
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Note: A WDT time-out will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{PD}$ bit. Table 4.2 reflects the status of $\overline{PD}$ and $\overline{TO}$ after the corresponding event.

TABLE 4.2 - $\overline{PD}$/$\overline{TO}$ STATUS AFTER RESET

$\overline{TO}$	$\overline{PD}$	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT time-out (not during SLEEP)
1	0	$\overline{MCLR}$ wake-up from SLEEP
1	1	Power-up
U	U	Low pulse on $\overline{MCLR}$ input

Note: The $\overline{PD}$ and $\overline{TO}$ bit maintain their status (U) until an event of Table 4.1 occurs. A low pulse on the $\overline{MCLR}$ input does not change the $\overline{PD}$ and $\overline{TO}$ status bits.

4.5.3 PROGRAM PAGE PRESELECT

Bits 5-6 of the STATUS register are defined as page address bits PA<1:0> and are used to preselect a program memory page. When executing a `GOTO`, `CALL`, or an instruction with PC as destination (e.g. `MOVWF PC`), PA<1:0> are loaded into bit A<10:9> of the program counter, selecting one of the available program memory pages. The direct address specified in the instruction is only valid within this particular memory page.

`RETLW` instructions do not change the page preselect bits.

Upon a RESET condition, PA<2:0> are cleared to "0"s.

4.6 File Select Register (FSR)

Bits 0-4 select one of the 32 available file registers in the indirect addressing mode (that is, calling for the INDF register in any of the file oriented instructions).

Bit 7 of the FSR is read-only and is always read as a "one".

If no indirect addressing is used, the FSR can be used as a 5-bit wide general purpose register.

Bits 5 and 6 of the FSR select the current data memory bank (Figure 4.2).

The lower 16 bytes of each bank are physically identical and are always selected when bit 4 of the FSR (in case of indirect addressing) is "0", or bit 4 of the direct file register address of the currently executing instruction is "0" (e.g. `MOVWF DATAMEM`).

Only if bit 4 in the above mentioned cases is "1", bits 5 and 6 of the FSR select one of the four available register banks with 16 bytes each.

Bit 7 is read-only and is always read as "one."

5.0 I/O REGISTERS (PORTS)

The I/O registers can be written and read under program control like any other register of the register file. However, "read" instructions (e.g. `MOVF PORTB,W`) always read the I/O pins, regardless if a pin is defined as "input" or "output." Upon a RESET condition, all I/O ports are defined as "input" (= high impedance mode) as the I/O control registers (TRISA, TRISB) are all set to "ones."

The execution of a "`TRIS f`" instruction with corresponding "zeros" in the W-register is necessary to define any of the I/O pins as output.

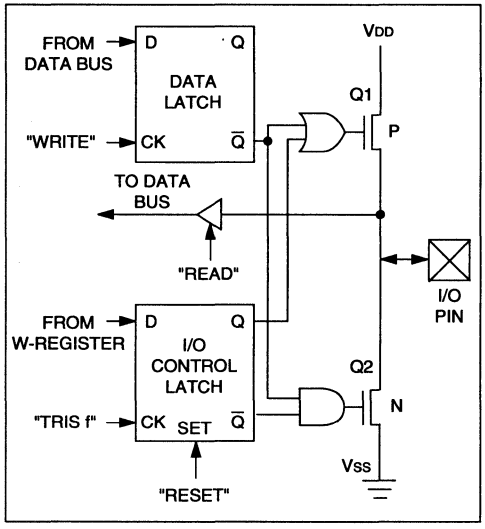
5.1 PORTA

PORTA is a 4-bit I/O register. Only the low order 4 bits are used (RA0 - RA3). Bits 4 - 7 are unimplemented and read as "zeros."

5.2 PORTB

PORTB is an 8-bit I/O register.

FIGURE 5.1 - EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



5.3 I/O Interfacing

The equivalent circuit for an I/O port bit is shown in Figure 5.1. All ports may be used for both input and output operations. For input operations, these ports are non-latching. Any input must be present until read by an input instruction (e.g. `MOVF PORTB, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be set to zero. For use as an input, the corresponding TRIS bit must be "one". Any I/O pin can be programmed individually as input or output.

5.4 I/O Programming Considerations

5.4.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The `BCF` and `BSF` instructions, for example, read the entire port into the CPU, execute the bit operation and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a `BSF` operation on bit 5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the `BSF` operation takes place on bit 5 and PORTB is re-output to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

5.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see Figure 5.2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

6.0 GENERAL PURPOSE REGISTERS

f08h - f0Fh: general purpose register files which are always selected, independent of bank select

f10h - f1Fh: general purpose register files in memory bank 0

f20h - f2Fh: physically identical to f00 - f0F

f30h - f3Fh: general purpose register files in memory bank 1

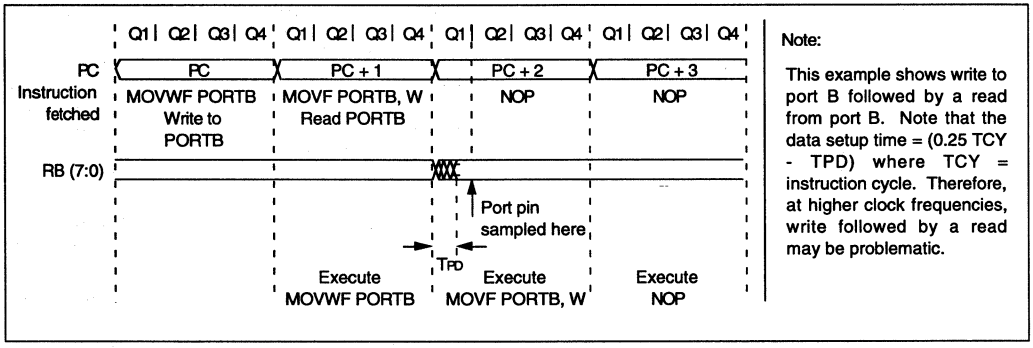
f40h - f4Fh: physically identical to f00 - f0F

f50h - f5Fh: general purpose register files in memory bank 2

f60h - f6Fh: physically identical to f00 - f0F

f70h - f7Fh: general purpose register files in memory bank 3

FIGURE 5.2 - I/O PORT READ/WRITE TIMING



7.0 SPECIAL PURPOSE REGISTERS

7.1 W Working Register

Holds second operand in two operand instructions and/ or supports the internal data transfer.

7.2 TRISA I/O Control Register For PORTA

Only bits 0 - 3 are available. PORT A is only 4-bits wide.

7.3 TRISB I/O Control Register For PORTB

The I/O control register will be loaded with the content of the W register by executing of the `TRIS PORT B` instruction. A "1" in the I/O control register puts the corresponding I/O pin into a high impedance (input) mode. A "0" puts the contents of file register PORTB out on the selected I/O pins.

This register is "write-only" and is set to all "ones" upon a RESET condition.

7.4 OPTION Prescaler/RTCC Option Register

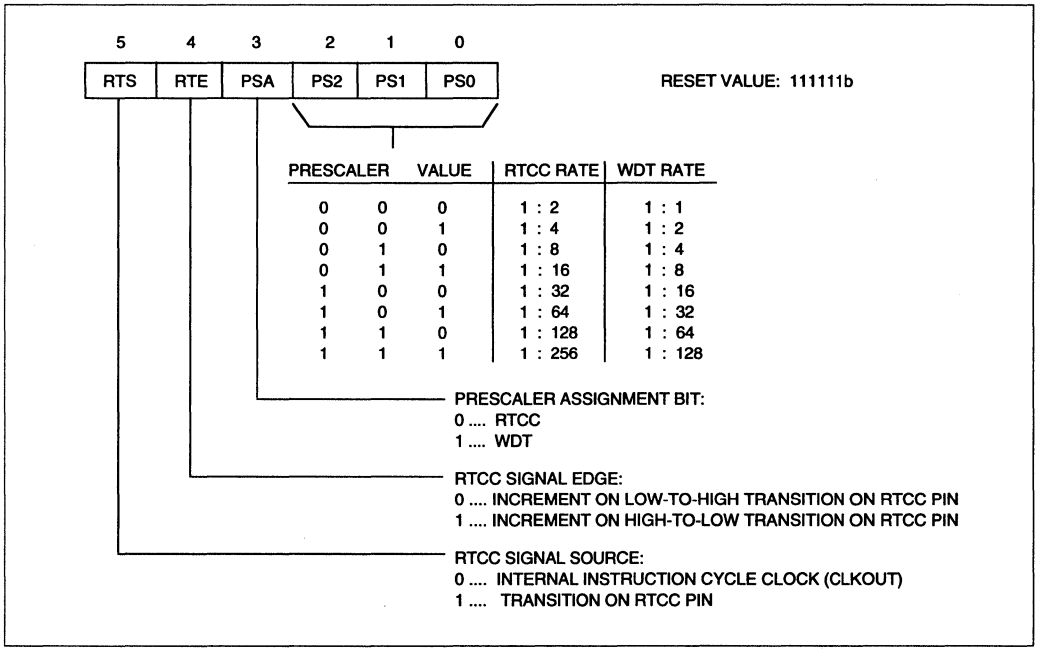
Defines prescaler assignment (RTCC or WDT), prescaler value, signal source and signal edge for the RTCC. The OPTION register is "write-only" and is 6-bits wide.

By executing the "`OPTION`" instruction, the contents of the "W" register will be transferred to the option register. Upon a RESET condition, the option register is set to all "ones."

Figure 7.1 show the bit descriptions for the OPTION register. This register is write only.

2

FIGURE 7.1 - OPTION REGISTER



8.0 RESET CONDITION

A RESET condition can be caused by applying power to the chip (power-up), pulling the MCLR input "low" or by a Watchdog Timer timeout. The device will stay in RESET as long as the oscillator start-up timer (OST) is active or the MCLR input is "low."

The Oscillator Start-up Timer is activated as soon as MCLR input is sensed to be high. This implies that in case of Power-On Reset with MCLR tied to VDD the OST starts from power-up. In case of WDT time-out, it will start at the end of the timeout (since MCLR is high). In case of MCLR reset, the OST will start when MCLR goes high. The nominal OST timeout period is 18ms. See Section 13.0 for detailed information on OST and Power-On Reset.

During a RESET condition the state of the PIC16C58A is defined as :

- The oscillator is running or will be started (power-up or wake-up from SLEEP).
- All I/O port pins (RA0 - RA3 and RB0 - RB7) are put into the high-impedance state by setting the "TRIS" registers to all "ones" (= input mode).
- The Program Counter is set to all "ones" (7FFh).
- The OPTION register is set to all "ones".
- The Watchdog Timer and its prescaler are cleared.
- The upper-three bits (page select bits) in the STATUS Register are cleared to "zero."
- "RC" mode only: The "CLKOUT" signal on the OSC2 pin is held at a"low" level.

TABLE 8-1: RESET CONDITION FOR REGISTERS

Register	Address	• Power-on Reset	• MCLR Reset during: - normal operation - SLEEP • WDT timeout during normal operation	• Wake up from SLEEP through WDT timeout
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu
OPTION	-	0011 1111	0011 1111	0011 1111
INDF	00h	-	-	-
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	02h	000h	000h	PC + 1
STATUS	03h	0001 1xxx	000? ?uuu	uuu? ?uuu
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', ? = value depends on condition

9.0 PRESCALER

An 8-bit counter is available as a prescaler for the RTCC, or as a post-scaler for the Watchdog Timer, respectively (Figure 9.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the RTCC and the Watchdog Timer. Thus, a prescaler assignment for the RTCC means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS0-PS2 bits in the OPTION register determine the prescaler assignment and pre-scale ratio. When assigned to the RTCC, all instructions writing to the RTCC (e.g. `CLRF RTCC`, `MOVWF RTCC`, `BSF RTCC,x`....etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer.

9.1 Switching Prescaler Assignment

CHANGING PRESCALER FROM RTCC TO WDT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence must be executed when changing the prescaler assignment from RTCC to WDT:

```
1. MOVLW  B'xx0x0xxx'   ; Select internal clock and select new
2. OPTION               ; prescaler value. If new prescale value
                        ; is = '000' or '001', then select any other
                        ; prescale value temporarily.
3. CLRF 1               ; Clear RTCC and prescaler.
4. MOVLW  B'xxxx1xxx'   ; Select WDT, do not change prescale
                        ; value.
5. OPTION               ;
6. CLRWDT               ; Clears WDT and prescaler.
7. MOVLW  B'xxxx1xxx'   ; Select new prescale value.
8. OPTION               ;
```

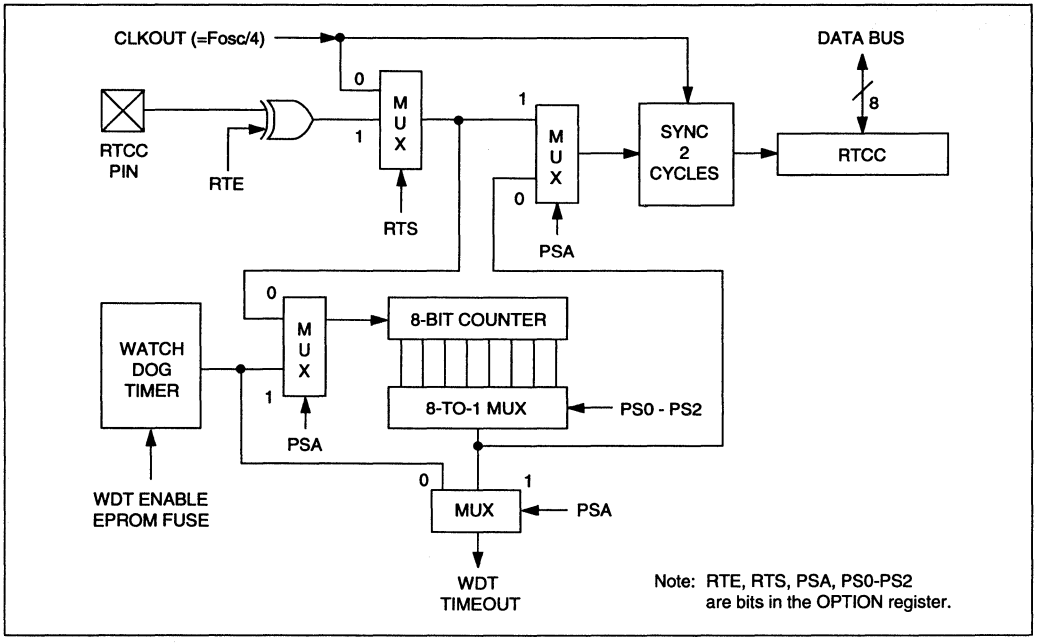
Steps 1 and 2 are only required if an external RTCC source is used. Steps 7 and 8 are necessary only if the desired prescale value is '000' or '001'.

CHANGING PRESCALER FROM WDT TO RTCC

To change prescaler from WDT to RTCC use the following sequence:

```
1. CLRWDT               ; Clear WDT and prescaler
2. MOVLW  B'xxxx0xxx'   ; Select RTCC, new prescale value
                        ; and clock source
3. OPTION               ;
```

FIGURE 9.1 - BLOCK DIAGRAM RTCC/WDT PRESCALER



10.0 BASIC INSTRUCTION SET SUMMARY

Each instruction is a 12-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The Instruction Set Summary in Table 10.1 lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 file registers is to be utilized by the instruction.

The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Notes to Table 10.1

Note 1: The ninth bit of the program counter will be forced to a "zero" by any instruction that writes to the PC except for `GOTO` (e.g. `CALL`, `MOVWF PC` etc.). See section 4.3 for details.

Note 2: When an I/O register is modified as a function of itself (e.g. `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as output and is driven low by an external device, the data will be written back with a '0'.

Note 3: The instruction "`TRIS f`" , where f = PORTA, PORTB, or PORTC causes the contents of the W register to be written to the three-state latches of the specified file (port). A "one" forces the pin to a high impedance state and disables the output buffers.

Note 4: If this instruction is executed on The RTCC register (and, where applicable, d=1), the prescaler will be cleared if assigned to the RTCC.

TABLE 10.1 - INSTRUCTION SET SUMMARY

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4 - 0)
OPCODE	d	f(FILE #)

d = 0 for destination W
d = 1 for destination f

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0001 11df ffff 1Cf	Add W and f	**ADDWF**	**f, d**	W + f → d	C,DC,Z	1,2,4
0001 01df ffff 14f	AND W and f	**ANDWF**	**f, d**	W & f → d	Z	2,4
0000 011f ffff 06f	Clear f	**CLRF**	**f**	0 → f	Z	4
0000 0100 0000 040	Clear W	**CLRW**	**-**	0 → W	Z	
0010 01df ffff 24f	Complement f	**COMF**	**f, d**	$\bar{f}$ → d	Z	2,4
0000 11df ffff 0Cf	Decrement f	**DECF**	**f, d**	f -1 → d	Z	2,4
0010 11df ffff 2Cf	Decrement f,Skip if Zero	**DECFSZ**	**f, d**	f - 1 → d, skip if zero	None	2,4
0010 10df ffff 28f	Increment f	**INCF**	**f, d**	f + 1 → d	Z	2,4
0011 11df ffff 3Cf	Increment f,Skip if zero	**INCFSZ**	**f, d**	f + 1 → d, skip if zero	None	2,4
0001 00df ffff 10f	Inclusive OR W and f	**IORWF**	**f, d**	W v f → d	Z	2,4
0010 00df ffff 20f	Move f	**MOVF**	**f, d**	f → d	Z	2,4
0000 001f ffff 02f	Move W to f	**MOVWF**	**f**	W → f	None	1,4
0000 0000 0000 000	No Operation	**NOP**	**-**	-	None	
0011 01df ffff 34f	Rotate left f	**RLF**	**f, d**	f(n) → d(n+1), C → d(0), f(7) → C	C	2,4
0011 00df ffff 30f	Rotate right f	**RRF**	**f, d**	f(n) → d(n-1), C → d(7), f(0) → C	C	2,4
0000 10df ffff 08f	Subtract W from f	**SUBWF**	**f, d**	f - W → d [f + $\overline{W}$ + 1 → d]	C,DC,Z	1,2,4
0011 10df ffff 38f	Swap halves f	**SWAPF**	**f, d**	f(0-3) ↔ f(4-7) → d	None	2,4
0001 10df ffff 18f	Exclusive OR W and f	**XORWF**	**f, d**	W ⊕ f → d	Z	2,4

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4 - 0)
OPCODE	b(BIT #)	f(FILE #)

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0100 bbbf ffff 4bf	Bit Clear f	**BCF**	**f, b**	0 → f(b)	None	2,4
0101 bbbf ffff 5bf	Bit Set f	**BSF**	**f, b**	1 → f(b)	None	2,4
0110 bbbf ffff 6bf	Bit Test f,Skip if Clear	**BTFSC**	**f, b**	Test bit (b) in file (f): Skip if clear	None	
0111 bbbf ffff 7bf	Bit Test f, Skip if Set	**BTFSS**	**f, b**	Test bit (b) in file (f): Skip if set	None	

LITERAL AND CONTROL OPERATIONS

(11-8)	(7 - 0)
OPCODE	k (LITERAL)

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
1110 kkkk kkkk Ekk	AND Literal and W	**ANDLW**	**k**	k & W→ W	Z	
1001 kkkk kkkk 9kk	Call subroutine	**CALL**	**k**	PC + 1 → Stack, k → PC	None	1
0000 0000 0100 004	Clear Watchdog Timer	**CLRWDT**	**-**	0 → WDT (and prescaler, if assigned)	$\overline{TO}$/$\overline{PD}$	
101k kkkk kkkk Akk	Go To address (k is 9 bit)	**GOTO**	**k**	k → PC (9 bits)	None	
1101 kkkk kkkk Dkk	Incl. OR Literal and W	**IORLW**	**k**	k v W → W	Z	
1100 kkkk kkkk Ckk	Move Literal to W	**MOVLW**	**k**	k → W	None	
0000 0000 0010 002	Load OPTION register	**OPTION**	**-**	W → OPTION register	None	
1000 kkkk kkkk 8kk	Return,place Literal in W	**RETLW**	**k**	k → W, Stack → PC	None	
0000 0000 0011 003	Go into standby mode	**SLEEP**	**-**	0 → WDT, stop oscillator	$\overline{TO}$/$\overline{PD}$	
0000 0000 0fff 00f	Three-state port f	**TRIS**	**f**	W→ I/O control register f	None	3
1111 kkkk kkkk Fkk	Excl. OR Literal and W	**XORLW**	**k**	k ⊕ W → W	Z	

Notes: See previous page

11.0 WATCHDOG TIMER (WDT)

TheWatchdog Timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1/OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by programming the WDTE EPROM fuse (to zero).

11.1 WDT Period

The WDT has a nominal timeout period of 18ms, (with no prescaler). The timeout periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer timeout periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, timeout periods up to 2.5 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the prescaler count, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit $\overline{TO}$ in the STATUS register will be cleared upon a Watchdog Timer timeout.

The WDT period is a function of the supply voltage, operating temperature and will also vary from unit to unit due to variations in the manufacturing process. Please refer to the graphs in Section 18.0 and DC specs for more details.

11.2 WDT Programming Considerations

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

12.0 OSCILLATOR CIRCUITS

12.1 Oscillator Types

The PIC16C58A series is available with four different oscillator options. The two OT1:OT0 EPROM fuses in the configuaration word select one of these four modes.

12.2 Crystal Oscillator

The PIC16C58A crystal options (XT, HS, or LP) need a crystal or ceramic resonator connected to the OSC1 and OSC2 pins to establish oscillation (Figure 12.1). XT = Standard crystal oscillator, HS = High speed crystal oscillator. The series resistor RS may be required for the "HS" oscillator, especially at lower than 20 MHz oscillation frequency. It may also be required in XT mode with AT strip-cut type crystals to avoid overdriving.

12.3 RC Oscillator

For timing insensitive applications, the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 12.3 shows how the R/C combination is connected to the PIC16C58A. For Rext values below 2.2kOhm, the oscillator operation may become unstable or stop completely. For very high Rext values (e.g. 1MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3kOhm and 100kOhm.

Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See table in Section 18.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characteristics in Section 18.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin and can be used for test purposes or to synchronize other logic (see Figure 2.2 for timing).

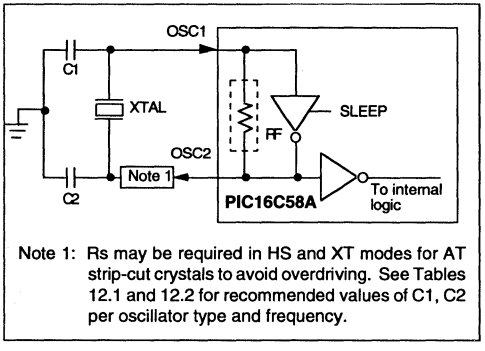
Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal/ ceramic resonator has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

TABLE 12.1 - CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	150-330 pF
	2.0 MHz	20-330 pF
	4.0 MHz	20-330 pF
HS	8.0 MHz	20-200 pF

Note: The capacitor values may change after characterization of the device. These values should be considered design targets.

FIGURE 12.1 - CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP TYPES ONLY)



Note 1: Rs may be required in HS and XT modes for AT strip-cut crystals to avoid overdriving. See Tables 12.1 and 12.2 for recommended values of C1, C2 per oscillator type and frequency.

FIGURE 12.2 - EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP TYPES ONLY)

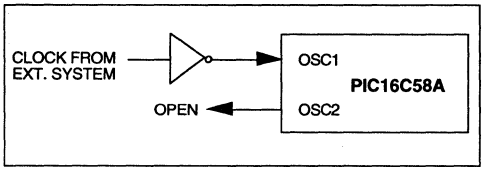
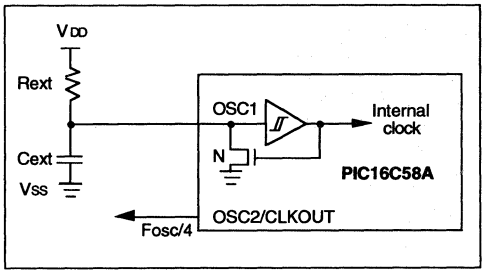


TABLE 12.2 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	15 pF	15 pF
XT	100 KHz	15-30 pF	200-300 pF
	200 KHz	15-30 pF	100-200 pF
	455 KHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Note: The capacitor values may change after characterization of the device. These values should be considered design targets.

FIGURE 12.3 - RC OSCILLATOR (RC TYPE ONLY)



2

13.0 OSCILLATOR START-UP TIMER (OST)

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. An on-chip oscillator start-up timer is provided which keeps the device in a RESET condition for approximately 18ms after the voltage on the MCLR pin has reached a logic high (VIHMC) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The OST will also be triggered upon a Watchdog Timer timeout. This is particularly important for applications using the WDT to awake the PIC16C58A from SLEEP mode automatically.

The OST is not adequate for low frequency crystals which require much longer than 18ms to start-up and stabilize.

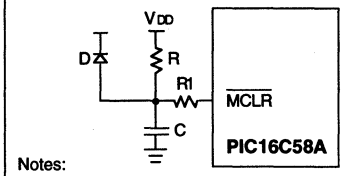
13.1 Power-On Reset (POR)

The PIC16C58A incorporates an on-chip Power-On Reset (POR) circuitry which provides internal chip reset for most power-up situations. To use this feature the user merely needs to tie MCLR pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 13.4. The Power-On Reset circuit and the Oscillator Start-up Timer circuit are closely related. On power-up the reset latch is set and the start-up timer (see Figure 13.4) is reset. The start-up timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18ms, it will clear the reset-latch and thus end the on-chip reset signal.

Figures 13.5 and 13.6 are two power-up situations with relatively fast rise time on VDD. In Figure 13.5, VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset tOST ms after MCLR goes high. In Figure 13.1.6, the on-chip Power-On Reset feature is being utilized (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper reset. Figure 13.7 depicts a potentially problematic situation where VDD rises too slowly. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is therefore not guaranteed to function correctly.

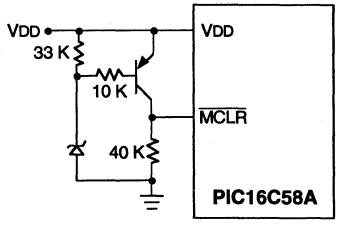
To summarize, the on-chip Power-On Reset is guaranteed to work if the rate of rise of VDD is no slower than 0.05 V/ms. It is also necessary that the VDD starts from 0V. The on-chip Power-On Reset is also not adequate for low frequency crystals which require much longer than 18ms to start up and stabilize. For such situations, we recommend that external RC circuits are used for longer Power-On Reset.

FIGURE 13.1 - EXTERNAL POWER ON RESET CIRCUIT (FOR SLOW POWER-UP)



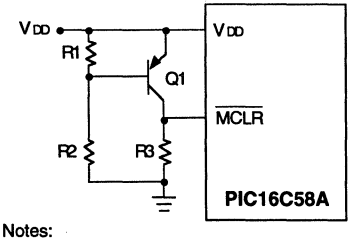
Notes:
1. External power on reset circuit is required only if VDD power-up slope is too slow or if a low frequency crystal oscillator is being used that needs a long start-up time. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40 KΩ must be observed to make sure that voltage drop across R does not exceed 0.2 V (max leakage current spec on MCLR pin is 5 μA). A larger voltage drop will degrade VIH level on MCLR pin.
3. R1= 100Ω to 1KΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to ESD or EOS.

FIGURE 13.2 - BROWN OUT PROTECTION CIRCUIT



Notes:
1. This circuit will activate reset when VDD goes below (VZ + 0.7 V) where VZ = Zener voltage.

FIGURE 13.3 - BROWN OUT PROTECTION CIRCUIT



Notes:
1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$VDD \cdot \frac{R1}{R1 + R2} = 0.7\ V.$$

FIGURE 13.4 - SIMPLIFIED POWER ON RESET BLOCK DIAGRAM

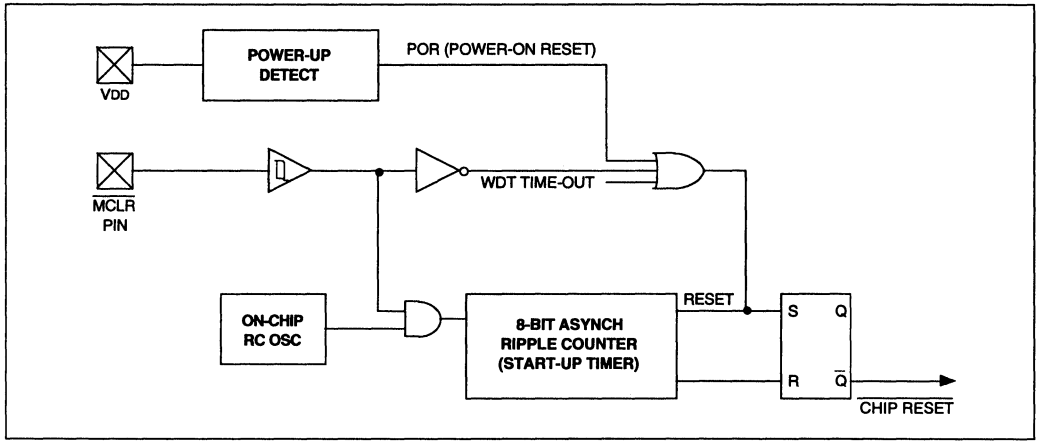
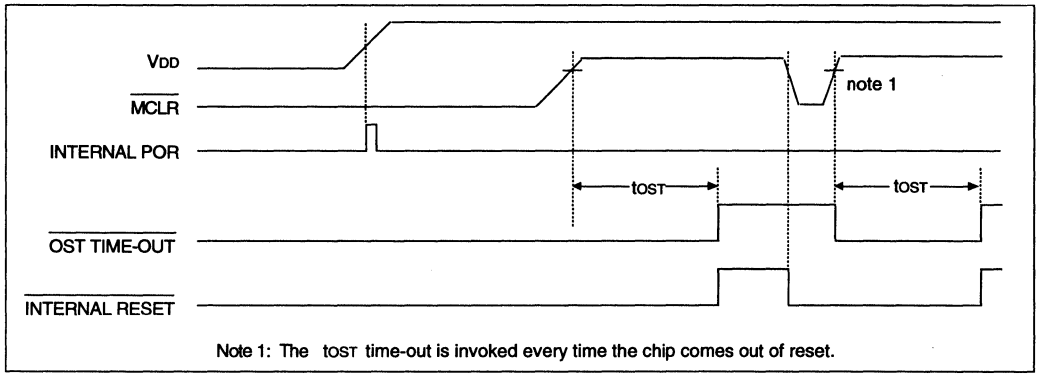


FIGURE 13.5 - USING EXTERNAL RESET INPUT



Note 1: The tOST time-out is invoked every time the chip comes out of reset.

FIGURE 13.6 - USING ON-CHIP POR (FAST VDD RISE TIME)

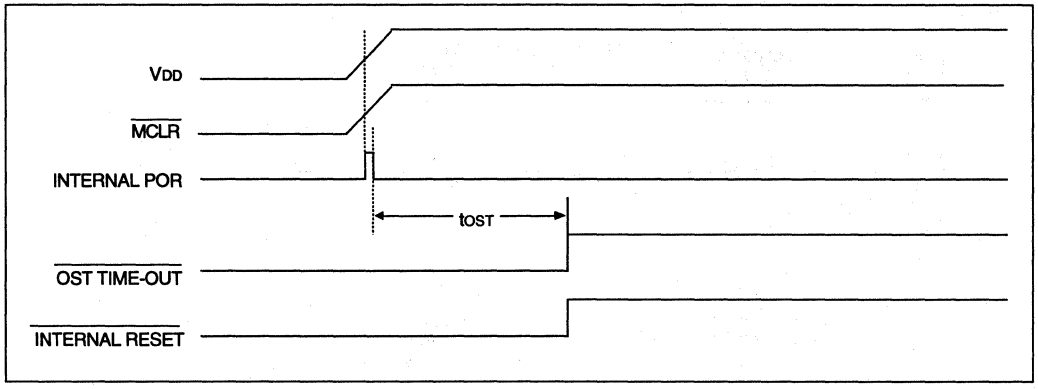
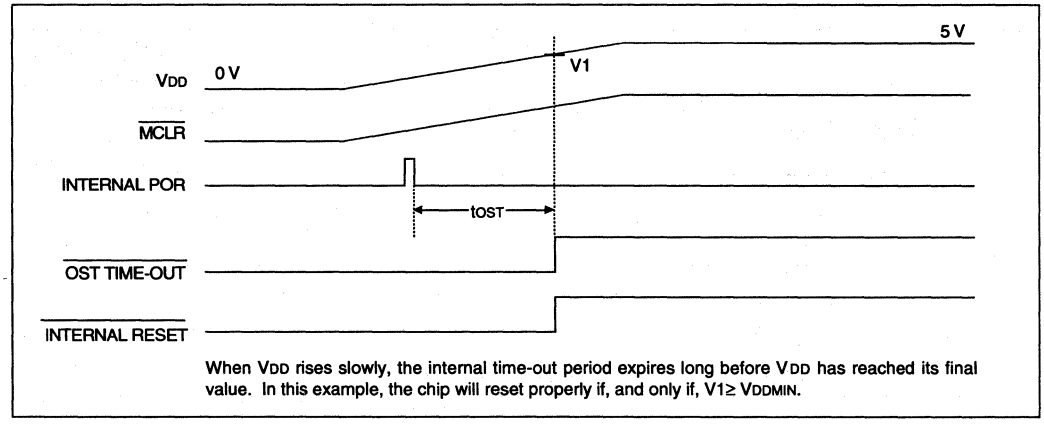


FIGURE 13.7 - USING ON-CHIP POR (SLOW VDD RISE TIME)



When VDD rises slowly, the internal time-out period expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1≥ VDDMIN.

14.0 POWER DOWN MODE (SLEEP)

The power down mode is entered by executing a SLEEP instruction.

If enabled, the WatchdogTimer will be cleared but keeps running, the bit $\overline{PD}$ in the STATUS register is cleared, the $\overline{TO}$ bit is set and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP command was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are in the High-impedance mode should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC input should also be at VDD or VSS for lowest current consumption.

The $\overline{MCLR}$ pin must be at VDD.

14.1 Wake-Up

The device can be awakened by a Watchdog Timer timeout (if it is enabled) or an externally applied "low" pulse at the $\overline{MCLR}$ pin. In both cases, the PIC16C58A will stay in RESET mode for one Oscillator Start-up Ttimer period (triggered from rising edge on $\overline{MCLR}$ or WDT timeout) before normal program execution resumes.

The $\overline{PD}$ bit in the STATUS register, which is set to one during power on , but cleared by the SLEEP command, can be used to determine if the processor was powered up or awakened from the power down mode (Table 4.2). The $\overline{TO}$ bit in the STATUS register can be used to determine, if the "wake up" was caused by an external $\overline{MCLR}$ signal or a Watchdog Timer timeout.

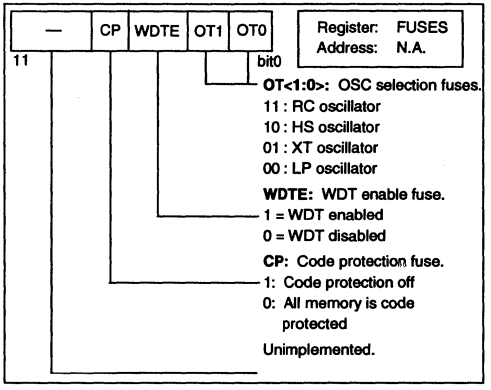
NOTE: Some applications may require external R/C networks on the $\overline{MCLR}$ pin in order to allow for oscillator start-up times longer than one OST period. In this case, a WDT wake up from power down mode is not recommended, because a RESET generated by a WDT time out does not discharge the external capacitor, and the PIC16C58A will be in RESET only for the Oscillator Start-up Timer period.

15.0 CONFIGURATION FUSES

The configuration EPROM consists of four EPROM fuses.

Two are for the selection of the oscillator type, one is the watchdog timer enable fuse and one is the code protection fuse.

FIGURE 15.1: CONFIGURATION WORD



15.1 Customer ID Code

The PIC16C58A series has 16 special EPROM bits which are not part of the normal program memory. These bits are available to the user to store an Identifier (ID) code, checksum, or other informative data. They cannot be accessed during normal program execution.

15.2 Code Protection

The program code written into the EPROM can be protected by programming the code protection fuse with "0".

When code protected, the contents of the program EPROM cannot be read out in a way that the program code can be reconstructed. In addition, all memory locations starting at 040h and above are protected against programming.

It is still possible to program locations 000h - 03Fh, the ID locations and the configuration fuses.

Note that the configuration fuses and the ID bits can still be read, even if the code protection logic is active.

15.2.1 VERIFYING A CODE-PROTECTED PART

When code protected verifying any program memory location will read a scrambled output which looks like "00000000XXXX" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

a. First, program and verify a good device without code protecting it.
b. Next, write '0' to the code protection fuse and then load its contents in a file.
c. Verify any code-protected PIC16C58A (with this program) against this file.

16.0 DEVELOPMENT SUPPORT

16.1 Development Tools

The PIC16C5X and PIC16CXX microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER™ Real-Time In-Circuit Emulator
- PRO MATE™ Universal Programmer
- PICSTART™ Low-Cost Prototype Programmer
- MPASM Assembler
- MPSIM Software Simulator

16.2 PICMASTER™: High Performance Universal In-Circuit Emulator

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X, PIC16CXX and PIC17CXX families.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16C5X, PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on low-cost PC-compatible machines ranging from 286-AT™ class ISA bus systems through the new 486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.X environment, allowing the operator access to a wide range of supporting software and accessories.

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.X environment was chosen to best make these features available to you, the end user.

The PICMASTER Emulator Universal System consists primarily of four major components:

- Host-Interface Card
- Emulator Control Pod
- Target-Specific Emulator Probe
- PC Host Emulation Control Software

The Windows 3.X System is a multitasking operating system which will allow the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window. Dynamic Data Exchange (DDE), a feature of Windows 3.X, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

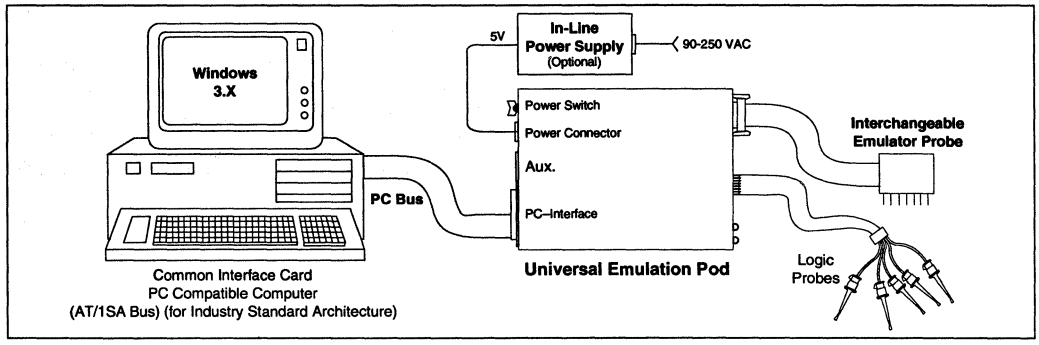
Under Windows 3.X, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16CXX processor and a PIC17CXX processor).

16.3 PRO MATE™: Universal Programmer

The PRO MATE Universal Programmer is a production quality programmer capable of operating in a stand alone mode as well as a PC-hosted mode.

The PRO MATE has programmable V_{DD} and V_{PP} supplies which allows it to verify programmed memory at V_{DD} min and V_{DD} max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MATE can read, verify or program PIC16C5X, PIC16CXX and PIC17CXX devices. It can also set the fuse configuration and code-protect in this mode. Its ROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.

FIGURE 16.1 - PICMASTER SYSTEM CONFIGURATION



In PC-hosted mode, the PRO MATE connects to the PC via one of the COM (RS232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of VDD min, VDD max and VPP levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different serial number, sequential or random.

The PRO MATE has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. PRO MATE supports all PIC16C5X, PIC16CXX and PIC17CXX processors.

16.4 PICSTART™ Programmer

The PICSTART programmer is an easy to use, very low-cost prototype programmer. It connects to the PC via one of the COM (RS232) ports. A PC based user interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based.

16.5 Assembler (MPASM)

Cross Assembler is a PC hosted symbolic assembler. It supports all microcontroller series including the PIC16C5X CMOS, PIC16CXX, and PIC17CXX families.

MPASM offers fully featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from the Microchip Universal Emulator System (PICMASTER).

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro Assembly Capability
- Provides Object, Listing, Symbol and special files required for debugging with one of the Microchip Emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a full feature directive language represented by four basic classes of directives:

- **Data Directives** are those that control the allocation of memory and provide a way to refer to data items symbolically, by meaningful names.
- **Listing Directives** control the MPASM listing dis play. They allow the specification of titles and subtitles, page ejects and other listing control.
- **Control Directives** permit sections of conditionally assembled code.
- **Macro Directives** control the execution and data allocation within macro body definitions.

16.6 Software Simulator (MPSIM)

The Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16C5X and PIC16CXX series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in single step, execute until break or in a trace mode. Two forms of symbolic debugging are available: an internal symbol table for disassembling opcodes and the displaying of source code from a listing file. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

16.7 Development Systems

For convenience, the development tools are packaged into comprehensive systems as listed below:

Item	Name	System Description
1.	PICMASTER System	PICMASTER In-Circuit Emulator with your choice of Target Probe, PRO MATE Programmer, Assembler, Software Simulator and Samples.
2.	PICSTART System	PICSTART Low-Cost Prototype Programmer, Assembler, Software Simulator and Samples

16.8 Probe Specifications

The PICMASTER probes currently meet the following specifications:

PICMASTER PROBE	Devices Supported	PROBE Maximum Frequency	PROBE Operating Voltage
PROBE - 16A	PIC16C54, PIC16C55, PIC16C56, and PIC16C57	4 MHZ	4.5V - 5.5V
PROBE - 16D	PIC16C54, PIC16C55, PIC16C56, PIC16C57, and PIC16C58	20 MHz	4.5V - 5.5V

17.0 ELECTRICAL CHARACTERISTICS

17.1 Absolute Maximum Ratings*

Ambient temperature under bias ..... -55°C to +125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss
(except VDD, $\overline{MCLR}$ and RTCC) ... -0.6V to VDD +0.6V
Voltage on VDD with respect to Vss ..... 0 to +7.5 V
Voltage on $\overline{MCLR}$ and RTCC with respect
to Vss ..... 0 to +14 V
Total power Dissipation (Note 1) ..... 800 mW
Max. Current out of Vss pin ..... 150 mA
Max. Current into VDD pin ..... 100 mA
Input Clamp Current, IIK (VI<0 or VI>VDD) ..... ±20 mA
Output Clamp Current, IOK (VO<0 or VO>VDD) ±20 mA
Max. Output Current sinked by any I/O pin ..... 25 mA
Max. Output Current sourced by any I/O pin .... 20 mA
Max. Output Current sourced by a single
I/O port Port A ..... 50 mA
Port B ..... 100 mA
Max. Output Current sinked by a single
I/O port Port A ..... 50 mA
Port B ..... 100 mA

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum\{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

TABLE 17.1 - PIN DESCRIPTIONS

Name	Function	Observation
RA0 - RA3	I/O PORTA	4 input/output lines. TTL input buffers.
RB0 - RB7	I/O PORTB	8 input/output lines. TTL input buffers.
RTCC	Real Time Clock/Counter	Schmitt Trigger Input. Clock input to RTCC register. Must be tied to Vss or VDD if not in use to avoid unintended operation and to reduce current consumption.
$\overline{MCLR}$	Master Clear	Schmitt Trigger Input. A "Low" voltage on this input generates a RESET condition. A rising voltage triggers the on-chip oscillator start-up timer which keeps the chip in RESET mode for about 18ms. This input must be tied directly, or via a pull-up resistor, to VDD.
OSC1/CLKIN	Oscillator (input)	In "XT", "HS" and "LP" oscillator configuration: Input terminal for crystal, ceramic resonator, or external clock generator. In "RC" oscillator configuration: Driver terminal for external RC combination to establish oscillation.
OSC2/CLKOUT	Oscillator (output)	In "XT", "HS" and "LP" oscillator configuration: Output terminal for crystal and ceramic resonator. Do not connect any other load to this output. Leave open if external clock generator is used. In "RC" oscillator configuration: A "CLKOUT" signal with a frequency of 1/4 Fosc1 is put out on this pin.
VDD	Power supply	
Vss	Ground	

17.2 DC CHARACTERISTICS: PIC16C58A-04 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS		Standard Operating Conditions Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Characteristic	**Sym**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	3.0		6.25	V	XT, RC and LP options
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See Section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See Section 13.1 for details on power on
Supply Current (Note 2)	IDD					XT and RC options
			1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
						LP option, Commercial
			15		µA	Fosc = 32 KHz, VDD = 3.0V, WDT disabled
						LP option, Industrial
			19		µA	Fosc = 32 KHz, VDD = 3.0V, WDT disabled
Power Down Current (Note 4)						
WDT enabled	IPD		4	12	µA	VDD = 3.0V, Commercial
			5	14	µA	VDD = 3.0V, Industrial
WDT disabled			0.6	9	µA	VDD = 3.0V, Commercial
			0.8	12	µA	VDD = 3.0V, Industrial

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

17.3 DC CHARACTERISTICS: PIC16C58A-10 (COMMERCIAL, INDUSTRIAL)
PIC16C58A-20 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS		Standard Operating Conditions Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Characteristic	**Sym**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	3.0 4.5		6.25 5.5	V V	XT and RC options HS option
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on
Supply Current (Note 2)	IDD					XT and RC options
			1.8		mA	FOSC = 4 MHz, VDD = 5.5V
						HS option
			4.8	10	mA	FOSC = 10 MHz , VDD = 5.5V
			9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
Power Down Current (Note 4)						
WDT enabled	IPD		4	12	µA	VDD = 3.0V, Commercial
			5	14	µA	VDD = 3.0V, Industrial
WDT disabled			0.6	9	µA	VDD = 3.0V, Commercial
			0.8	12	µA	VDD = 3.0V, Industrial

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

17.4 DC CHARACTERISTICS: PIC16LC58A-04 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS		Standard Operating Conditions Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Characteristic	**Sym**	**Min**	**Typ ***	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.5 4.5		6.25 5.5	V V	XT, RC and LP options HS option
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on reset
Supply Current (Note 2)	IDD					XT and RC options
			1.8		mA	FOSC = 4 MHz, VDD = 5.5V
						HS option
			4.8		mA	FOSC = 4 MHz, VDD = 5.5V
						LP option, Commercial
			15	32	µA	FOSC = 32 KHz, VDD = 2.5V, WDT disabled
						LP option, Industrial
			19	40	µA	FOSC = 32 KHz, VDD = 2.5V, WDT disabled
Power Down Current (Note 4)						
WDT enabled	IPD		4	12	µA	VDD = 2.5V, Commercial
			5	14	µA	VDD = 2.5V, Industrial
WDT disabled			0.6	9	µA	VDD = 2.5V, Commercial
			0.8	12	µA	VDD = 2.5V, Industrial

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1= external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

17.5 DC CHARACTERISTICS: PIC16C58A-04 (COMMERCIAL, INDUSTRIAL)
PIC16LC58A-04 (COMMERCIAL, INDUSTRIAL)
PIC16C58A-10 (COMMERCIAL, INDUSTRIAL)
PIC16C58A-20 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY

Standard Operating Conditions
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Input Low Voltage						
I/O ports	VIL	VSS		0.2 VDD	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt trigger)		VSS		0.15 VDD	V	
RTCC (Schmitt trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt trigger)		VSS		0.15 VDD	V	RC option only (Note 5)
OSC1		VSS		0.3 VDD	V	XT, HS and LP options
Input High Voltage						
I/O ports	VIH	0.2 VDD + 1V	VDD	V		For all VDD (Note 6)
		2.0		VDD	V	4.0 V < VDD ≤ 5.5 V (Note 6)
$\overline{MCLR}$ (Schmitt trigger)		0.85 VDD		VDD	V	
RTCC (Schmitt trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt trigger)		0.85 VDD		VDD	V	RC option only (Note 5)
OSC1		0.7 VDD		VDD	V	XT, HS and LP options
Input Leakage Current (Note 4)						**For VDD ≤ 5.5V**
I/O ports	IIL	-1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{MCLR}$		-5			µA	VPIN = VSS + 0.25V (Note 3)
$\overline{MCLR}$			0.5	+5	µA	VPIN = VDD (Note 3)
RTCC		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT (RC option only)				0.6	V	IOL = 1.6 mA, VDD = 4.5V
Output High Voltage						
I/O Ports (Note 4)	VOH	VDD-0.7			V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT (RC option only)		VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : In RC oscillator mode, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C58A be driven with external clock in RC mode.

Note 6: The user may use lower VIH voltage of the two specifications.

17.6 AC CHARACTERISTICS: PIC16C58A-04 (COMMERCIAL, INDUSTRIAL)
PIC16LC58A-04 (COMMERCIAL, INDUSTRIAL)
PIC16C58A-10 (COMMERCIAL, INDUSTRIAL)
PIC16C58A-20 (COMMERCIAL, INDUSTRIAL)

AC CHARACTERISTICS **Standard Operating Conditions**
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
External CLOCKIN Frequency (Note 2)	FOSC	DC		4	MHz	RC mode
		DC		4	MHz	XT mode
		DC		20	MHz	HS mode (Com/Ind) (Note 5)
		DC		200	KHz	LP mode
Oscillator Frequency (Note 2)	FOSC	DC		4	MHz	RC mode
		0.1		4	MHz	XT mode
		4		20	MHz	HS mode (Com/Ind) (Note 5)
		DC		200	KHz	LP mode
Instruction Cycle Time (Note 2)	TCY	1.0		DC	µs	RC mode
		1.0	4/FOSC	DC	µs	XT mode
		0.2		DC	µs	HS mode (Note 5)
		20		DC	µs	LP mode
External Clock in Timing (Note 4)						
Clock in (OSC1) high or low time						
XT oscillator configuration	TCKHLXT	50*			ns	
LP oscillator configuration	TCKHLLP	2*			µs	
HS oscillator configuration	TCKHLHS	20*			ns	
Clock in (OSC1) rise or fall time						
XT oscillator configuration	TCKRFXT	25*			ns	
LP oscillator configuration	TCKRFLP	50*			µs	
HS oscillator configuration	TCKRFHS	25*			ns	
RESET Timing						
$\overline{MCLR}$ pulse width (low)	TMCL	100*			ns	
RTCC Input Timing, No Prescaler						
RTCC high pulse width	TRTH	0.5 TCY+ 20*			ns	Note 3
RTCC low pulse width	TRTL	0.5 TCY+ 20*			ns	Note 3
RTCC Input Timing, With Prescaler						
RTCC high pulse width	TRTH	10*			ns	Note 3
RTCC low pulse width	TRTL	10*			ns	Note 3
RTCC period	TRTP	$\frac{T_{CY} + 40}{N}$ *			ns	Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Timeout Period (No Prescaler)	TWDT	9*	18*	30*	ms	VDD = 5.0V
Oscillation Start-up Timer Period	TOST	9*	18*	30*	ms	VDD = 5.0V

* Guaranteed by characterization, but not tested.

(Cont. on next page)

17.6 AC CHARACTERISTICS: (Cont.)

PIC16C58A-04 (COMMERCIAL, INDUSTRIAL)
PIC16LC58A-04 (COMMERCIAL, INDUSTRIAL)
PIC16C58A-10 (COMMERCIAL, INDUSTRIAL)
PIC16C58A-20 (COMMERCIAL, INDUSTRIAL)

AC CHARACTERISTICS **Standard Operating Conditions**
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
I/O Timing						
I/O pin input valid before CLKOUT↑ (RC Mode)	TDS	0.25 TCY+ 30*			ns	
I/O pin input hold after CLKOUT↑ (RC Mode)	TDH	0*			ns	
I/O pin output valid after CLKOUT↓ (RC Mode)	TPD			40*	ns	
I/O pin input valid before OSC↑ (I/O setup time)	TioV2osH	TBD	13		ns	VDD = 5.0V
OSC1↑ to I/O pin input invalid (I/O hold time)	TosH2ioL	TBD			ns	VDD = 5.0V
OSC1↑ to I/O pin output valid	TosH2ioV	TBD	63		ns	VDD = 5.0V
OSC1↑ to CLKOUT low	TosH2ckL	TBD	57		ns	VDD = 5.0V
OSC1↑ to CLKOUT high	TosH2ckH	TBD	56		ns	VDD = 5.0V
I/O pin input valid before CLKOUT high	TioV2ckH	TBD	13		ns	VDD = 5.0V
CLKOUT low to I/O valid	TckL2ioV	TBD			ns	VDD = 5.0V
CLKOUT rise time	TckR		12	TBD	ns	VDD = 5.0V
CLKOUT fall time	TckF		12	TBD	ns	VDD = 5.0V
I/O pin output rise time	TioR		17	TBD	ns	VDD = 5.0V
I/O pin output fall time	TioF		10	TBD	ns	VDD = 5.0V
Capacitive Loading Specs on Output Pins						
OSC2 pin	COSC2			15	pF	In XT, HS or LP modes when external clock is used to drive OSC1
All I/O pins and OSC2 (in RC mode)	CIO			50	pF	

* Guaranteed by characterization, but not tested.

Note 1. Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2. Instruction cycle period (Tcy) equals four times the input oscillator time base period.
All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Note 3. For a detailed explanation of RTCC input clock requirements see section 4.2.1.

Note 4. Clock-in high-time is the duration for which clock input is at VIHOSC or higher.
Clock-in low-time is the duration for which clock input is at VILOSC or lower.

Note 5. This HS specification is only for the -20 device. The -10 device has a maximum of 10 MHz and the -04 device has a maximum of 4 MHz.

17.7 Electrical Structure of Pins

FIGURE 17.1 - ELECTRICAL STRUCTURE OF I/O PINS (RA and RB)

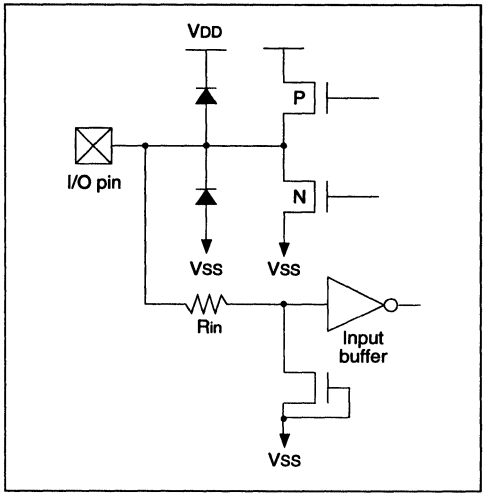
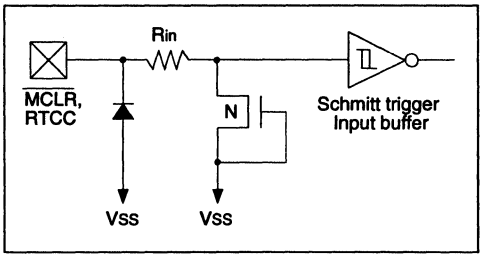


FIGURE 17.2 - ELECTRICAL STRUCTURE OF $\overline{MCLR}$ AND RTCC PINS



Notes to Figures 17.1 and 17.2: The diodes and the grounded gate (or output driver) NMOS device are carefully designed to protect against ESD (Electrostatic discharge) and EOS (Electrical overstress). Rin is a small resistance to further protect the input buffer from ESD.

18.0 TIMING DIAGRAMS

FIGURE 18.1 - RTCC TIMING

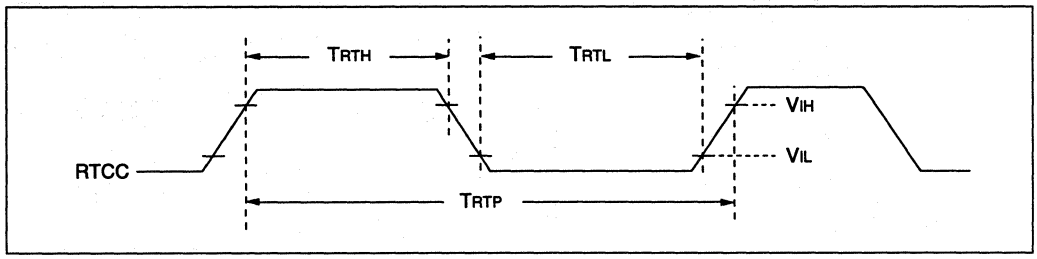


FIGURE 18.2 - OSCILLATOR START-UP TIMING (RC mode)

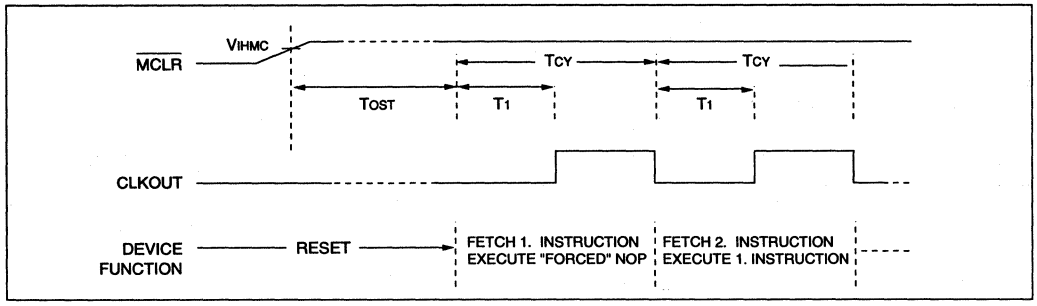
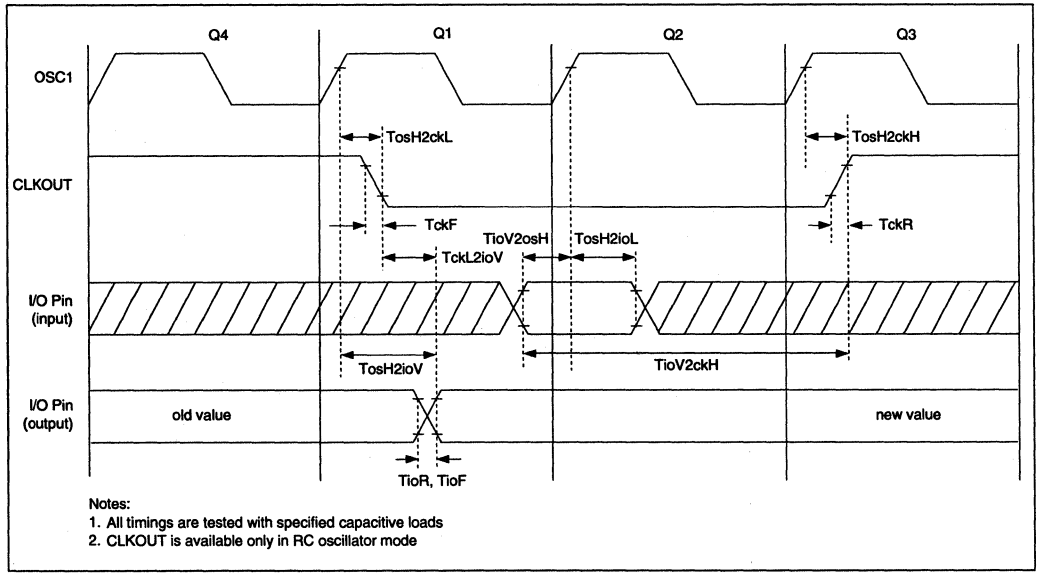


FIGURE 18.3 - INPUT/OUTPUT TIMING FOR I/O PORTS



Notes:
1. All timings are tested with specified capacitive loads
2. CLKOUT is available only in RC oscillator mode

19.0 DC AND AC CHARACTERISTICS GRAPHS/TABLES

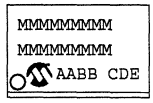
NOT AVAILABLE AT THIS TIME

20.0 PACKAGING INFORMATION

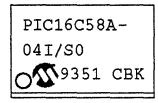
See Section 11 of the Data Book.

20.1 Package Marking Information

18L SOIC

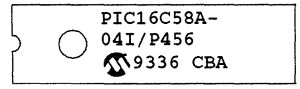


Example

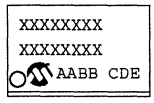


18L PDIP

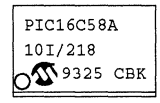
Example



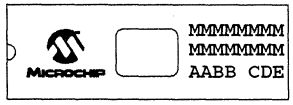
20L SSOP



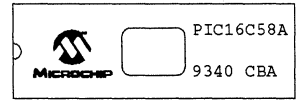
Example



18L Cerdip



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

*Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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CONNECTING TO MICROCHIP BBS

Connect world wide to the Microchip BBS using the CompuServe communications network. In most cases a local call is your only expense. The Microchip BBS connection does not use CompuServe membership services, therefore **you do NOT need CompuServe membership to join Microchip's BBS.**

The procedure to connect will vary slightly from country to country. Please check with your local CompuServe agent for details if you have a problem. CompuServe services allows multiple users at baud rates up to 9600.

To connect:

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.
2. Dial your local CompuServe phone number.
3. Depress **<ENTER>** and a garbage string will appear because CompuServe is expecting a 7E1 setting.
4. Type **+ <ENTER>** and `Host Name:` will appear.
5. Type **MCHIPBBS<ENTER>** and you will be connected to the Microchip BBS.

In the United States, to find CompuServe's phone number closest to you set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600 baud connection. After the system responds with `Host Name:`, type

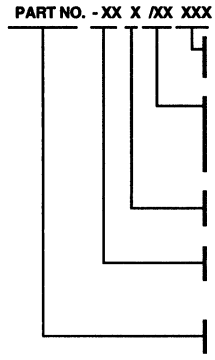
NETWORK<ENTER> and follow CompuServe's directions.

For voice information (or calling from overseas), you may call (614) 457-1550 for your local CompuServe number.

NOTES:

PIC16C58A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the listed sales offices below or contact Corporate Headquarters for the representative or distributor in your area.



Pattern:	3-Digit Pattern Code for QTP (factory specified) (blank for OTP and Windowed Parts)	
Package:	P = PDIP (300 mil) SO = SOIC (Gull Wing, 300 mil body) SS = SSOP (209 mil) JW = Ceramic Window	
Temperature Range:	- = 0°C to +70°C (T for tape/reel) I = -40°C to +85°C (S for tape/reel)	
Frequency Range:	04 = 4 MHz 10 = 10 MHz 20 = 20 MHz	
Device:	PIC16C58A : Standard VDD range PIC16LC58A : Extended VDD range	

Examples:

a) PIC16C58A - 04/P301
= Commercial temp.,
PDIP package,
4 MHz, standard VDD limits,
QTP pattern # 301

b) PIC16LC58A - 04I/SO
= Industrial temp.,
SOIC package,
4 MHz, extended VDD limits

c) PIC16C58A - 20I/P
= Industrial temp.,
PDIP package,
20 MHz, standard VDD limits

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local Compuserve number.

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

PIC16CR57A

ROM-Based 8-Bit CMOS Microcontroller

FEATURES

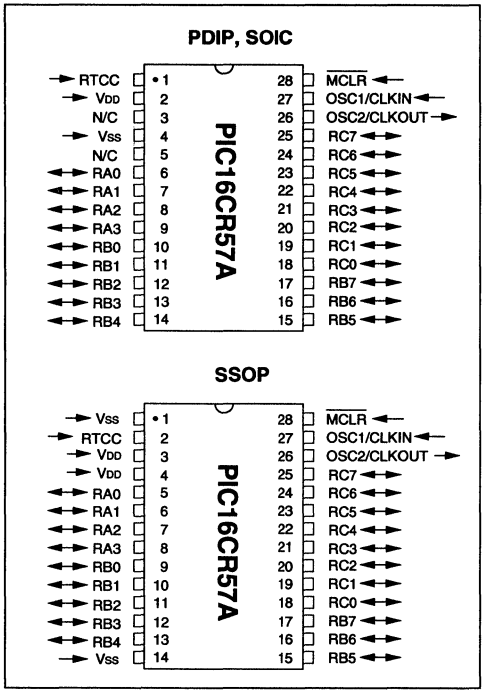
Compatibility
- Pin and software compatible with PIC16C57 device

High-Performance RISC-like CPU
- Only 33 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200ns instruction cycle
- 12-bit wide instructions
- 8-bit wide data path
- 2K x 12 on-chip ROM program memory
- 72 x 8 general purpose registers (SRAM)
- Eight special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features
- 20 I/O pins with individual direction control
- 8-bit real time clock/counter (RTCC) with 8-bit programmable prescaler
- Power-On Reset
- Oscillator Start-up Timer
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security ROM fuse for code-protection
- Power saving SLEEP mode
- Mask selectable oscillator options:
  - Low-cost RC oscillator: RC
  - Standard crystal/resonator: XT
  - High-speed crystal/resonator: HS
  - Power saving low frequency crystal: LP

CMOS Technology
- Low-power, high-speed CMOS ROM technology
- Fully static design
- Wide-operating voltage range:
  - Commercial: 2.5V to 6.25V
  - Industrial: 2.5V to 6.25V
- Low-power consumption
  - < 2mA typical @ 5V, 4 MHz
  - 15μA typical @ 3V, 32 KHz
  - < 3μA typical standby current (with WDT disabled) @ 3V, 0°C to 70°C

FIGURE A - PIN CONFIGURATIONS



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1.0 GENERAL DESCRIPTION

The PIC16CR57A from Microchip Technology is a new member of the family of low-cost, high-performance, 8-bit, fully static, ROM based CMOS microcontrollers. This device is pin and software compatible with the PIC16C57. It employs a RISC-like architecture with only 33 single word/single cycle instructions to learn. All instructions are single cycle (200ns) except for program branches which take two cycles. The PIC16CR57A delivers performance an order of magnitude higher than its competitors in similar price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16CR57A is equipped with special microcontroller-like features that reduce system cost and power requirements. The Power-On Reset and oscillator start up timer eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including power saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and code protection features improves system cost, power and reliablity.

The PIC16CR57A is supported by an assembler, a software simulator, an in-circuit emulator and a production quality programmer. All the tools are supported by IBM PC and compatible machines.

1.1 Applications

The PIC16CR57A device fits perfectly in applications ranging from high-speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices, and telecom processors. The small footprint packages for through hole or surface mounting make this microcontroller perfect for all applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16CR57A very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

2.0 ARCHITECTURAL DESCRIPTION

2.1 Harvard Architecture

The PIC16CR57A single-chip microcomputer is a low-power, high-speed, full static CMOS device containing ROM, RAM, I/O, and a central processing unit on a single chip.

The architecture is based on a register file concept with separate bus and memories for data and instructions (Harvard architecture). The data bus and memory (RAM) are 8-bits wide while the program bus and program memory (ROM) have a width of 12-bits. This concept allows a simple yet powerful instruction set designed to emphasize bit, byte and register operations under high speed with overlapping instruction fetch and execution cycles. That means that, while one instruction is executed, the following instruction is already being read from the program memory. A block diagram of the PIC16CR57A is given in Figure 2.1.

2.2 Clocking Scheme/Instruction Cycle

The clock input (from pin OSC1) is internally divided by four to generate four non overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1, an instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 2.2.

TABLE 2.1 - PIN FUNCTIONS

Name	Function
RA0 - RA3	I/O PORTA
RB0 - RB7	I/O PORTB
RC0 - RC7	I/O PORTC
RTCC	Real Time Clock/Counter
MCLR	Master Clear
OSC1/CLKIN	Oscillator (input)/External Clock Input
OSC2/CLKOUT	Oscillator (output)
VDD	Power supply
VSS	Ground

TABLE 1.1 - OVERVIEW OF PIC16CR57A DEVICE

Part #	ROM	RAM*	I/O	Package Options
PIC16CR57A	2048 x 12	80 x 8	20	28L PDIP (300 mil and 600 mil wide), 28L SOIC (300 mil), 28L SSOP
* Including special function registers.				

FIGURE 2.1 - PIC16CR57A SERIES BLOCK DIAGRAM

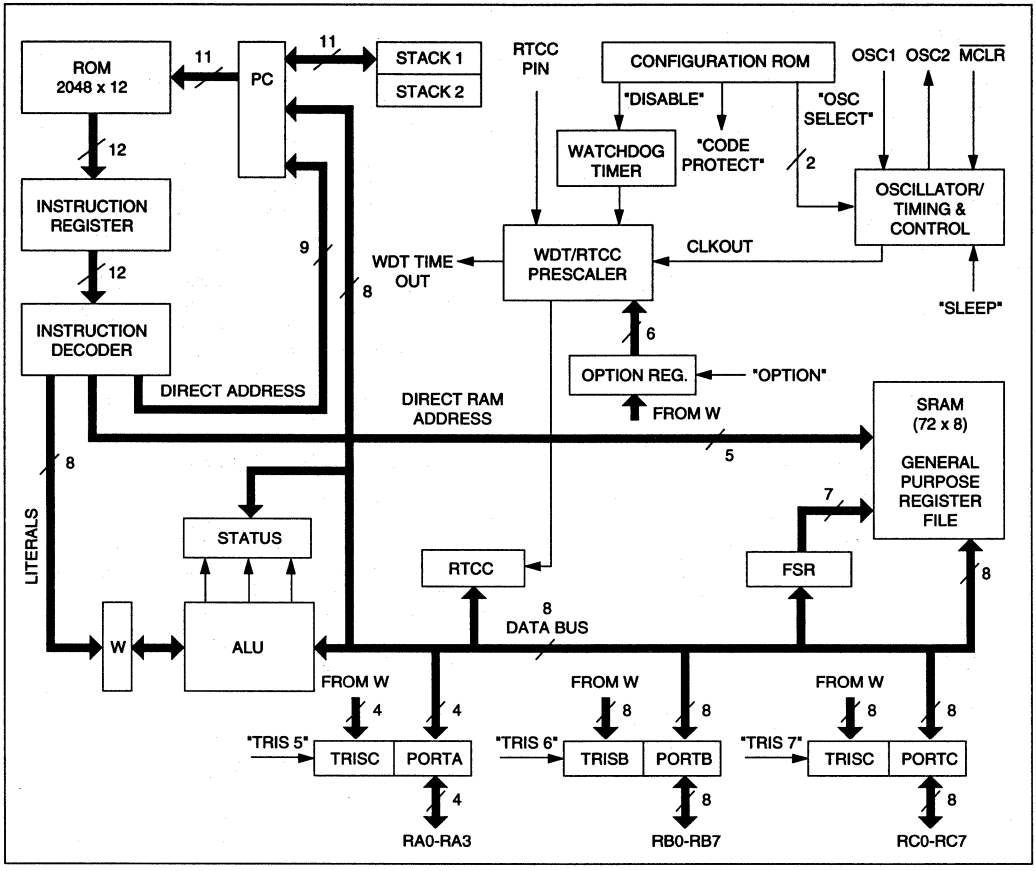
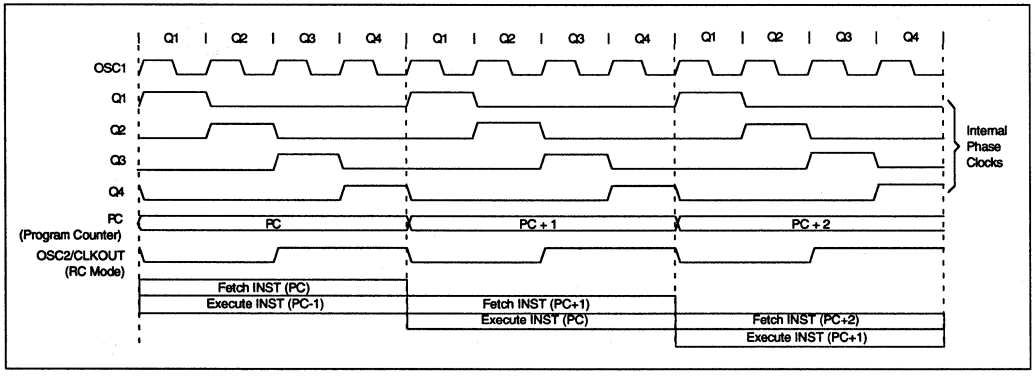


FIGURE 2.2 - CLOCKS/INSTRUCTION CYCLE



2.3 Data Register File

The 8-bit data bus connects two basic functional elements together: the Register File composed of 80 addressable 8-bit registers including the I/O Ports, and an 8-bit wide Arithmetic Logic Unit. The 32 bytes of RAM are directly addressable. A "banking" scheme, with banks of 16 bytes each, is employed to address larger data memories (Figure 4.2). Data can be addressed direct, or indirect using the file select register. Immediate data addressing is supported by special "literal" instructions which load data from program memory into the W register.

The register file is divided into two functional groups: operational registers and general purpose registers. The operational registers include the Real Time Clock Counter (RTCC) register, the Program Counter (PC), the Status Register, the I/O registers (PORTs), and the File Select Register. The general purpose registers are used for data and control information under command of the instructions.

In addition, special purpose registers are used to control the I/O port configuration, and the prescaler options.

2.4 Arithmetic/Logic Unit (ALU)

The 8-bit wide ALU contains one temporary working register (W Register). It performs arithmetic and Boolean functions between data held in the W Register and any file register. It also does single operand operations on either the W register or any file register.

2.5 Program Memory

2048 words of 12-bit wide on-chip program memory (ROM) are available. The memory can be directly addressed in pages of 512 words.

Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations, supporting direct, indirect, relative addressing modes, can be performed by Bit Test and Skip instructions, Call instructions, Jump instructions or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting.

3.0 PIC16CR57A OVERVIEW

A variety of oscillator types, frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information and tables in this section. When placing orders, please use the "PIC16CR57A Product Identification System" on the back page of this data sheet to specify the correct part number.

4.0 OPERATIONAL REGISTER FILES

4.1 Indirect Data Addressing (INDF)

This is not a physically implemented register. Addressing INDF calls for the contents of the File Select Register to be used to select a file register. The INDF register is useful as an indirect address pointer. For example in the instruction `ADDWF INDF, W` will add the contents of the register pointed to by the FSR to the content of the W Register and place the result in W.

If INDF itself is read through indirect addressing (i.e. FSR = 0h), then 00h is read. If the INDF register is written to via indirect addressing, the result will be a NOP.

4.2 Real Time Clock/Counter Register (RTCC)

This register can be loaded and read by the program as any other register. In addition, its contents can be incremented by an external signal edge applied to the RTCC pin, or by the internal instruction cycle clock (CLKOUT=fosc/4). Figure 4.1 is a simplified block diagram of the RTCC module.

An 8-bit prescaler can be assigned to the RTCC by writing the proper values to the PSA bit and the PS bits in the OPTION register. The OPTION register is a special register (not mapped in data memory) addressable using the 'OPTION' instruction. See section 7.5 for details. If the prescaler is assigned to the RTCC, instructions writing to the RTCC register (e.g. `CLRF RTCC`, or `BSF RTCC, 5`, ...etc.) clears the prescaler.

The bit "RTS" (RTCC signal Source) in the OPTION register determines, if the RTCC register is incremented internally or externally.

RTS=1: The clock source for the RTCC or the prescaler, if assigned to it, is the signal on the RTCC pin. Bit 4 of the OPTION register (RTE) determines, if an increment occurs on the falling (RTE=1) or rising (RTE=0) edge of the signal presented to the RTCC pin.

RTS=0: The RTCC register or its prescaler, respectively, will be incremented with the internal instruction clock (= Fosc/4). The "RTE" bit in the OPTION register and the RTCC pin are "don't care" in this case. The RTCC pin must not be left floating (tie to either VDD or VSS). This prevents unintended entering of test modes and reduces the current consumption in low-power applications.

As long as clocks are applied to the RTCC (from internal or external source, with or without prescaler), the RTCC register keeps incrementing and just rolls over when the value "FFh" is reached. All increment pulses for the RTCC register are delayed by two instruction cycles. After writing to the RTCC register, for example, no increment takes place for the following two instruction cycles. This is independent if internal or external clock source is selected. If a prescaler is assigned to the RTCC, the output of the prescaler will be delayed by two cycles before the RTCC register is incremented. This is true for instructions that either write to or read-modify-write RTCC (e.g. `MOVF RTCC, CLRF RTCC`). For applications where RTCC needs to be tested for zero without affecting its count, use of `MOVF RTCC, W` instruction is recommended. Timing diagrams in Figure 4.3 show RTCC read, write and increment timing.

4.2.1 USING RTCC WITH EXTERNAL CLOCK

When external clock input is used for RTCC, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements. Also there is some delay from the occurance of the external clock edge to the actual incrementing of RTCC. Referring to Figure 4.1, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where:

tosc = oscillator time period.

When no prescaler is used, PSOUT (Prescaler output, see Figure 4.1) is the same as RTCC clock input and therefore the requirements are:

T_{RTH} = RTCC high time ≥ 2tosc + 20 ns

T_{RTL} = RTCC low time ≥ 2tosc + 20 ns

When prescaler is used, the RTCC input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.

Then: PSOUT high time = PSOUT low time = $\frac{N \bullet T_{RT}}{2}$

where T_{RT} = RTCC input period and N = prescale value (2, 4, ..., 256). The requirement is, therefore $\frac{N \bullet T_{RT}}{2}$ ≥ 2 tosc + 20ns, or $T_{RT} \geq \frac{4\ tosc + 40\ ns}{N}$.

The user will notice that no requirement on RTCC high time or low time is specified. However, if the high time or low time on RTCC is too small then the pulse may not be detected, hence a minimum high or low time of 10ns is required. In summary, the RTCC input requirements are:

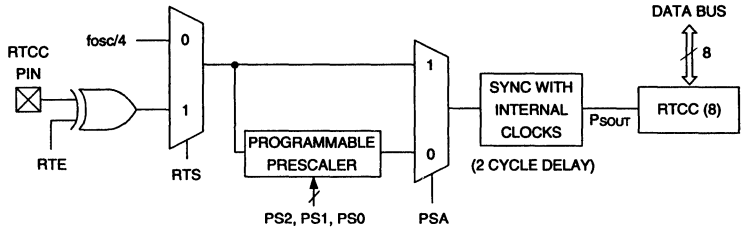
T_{RT} = RTCC period ≥ (4 tosc + 40 ns)/N

T_{RTH} = RTCC high time ≥ 10 ns

T_{RTL} = RTCC low time ≥ 10 ns

Delay from external clock edge: Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the RTCC is actually incremented. This delay is between 3 tosc and 7 tosc (See Figure 4.4). Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±200 ns @ 20 MHz).

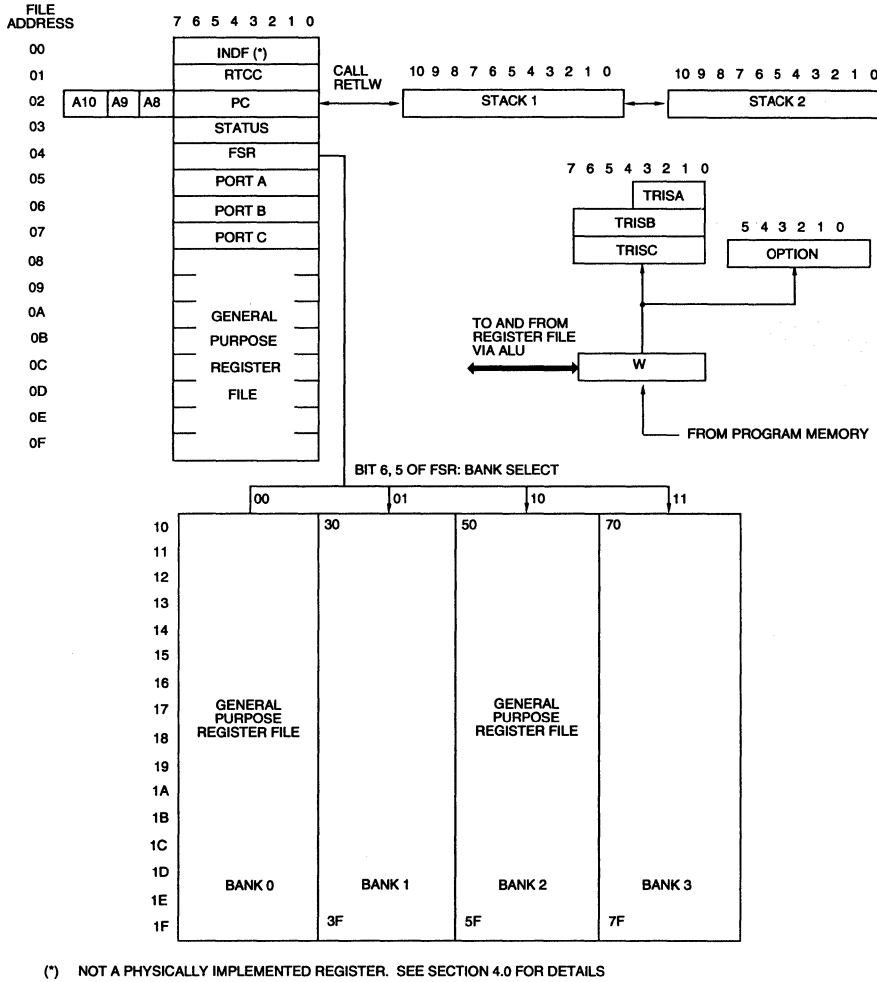
FIGURE 4.1 - RTCC BLOCK DIAGRAM (SIMPLIFIED)



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 are located in option register.
2. The prescaler is shared with Watchdog Timer (see Figure 9.1).

2

FIGURE 4.2 - PIC16CR57A DATA MEMORY MAP



(*) NOT A PHYSICALLY IMPLEMENTED REGISTER. SEE SECTION 4.0 FOR DETAILS

FIGURE 4.3A - RTCC TIMING: INT CLOCK/NO PRESCALE

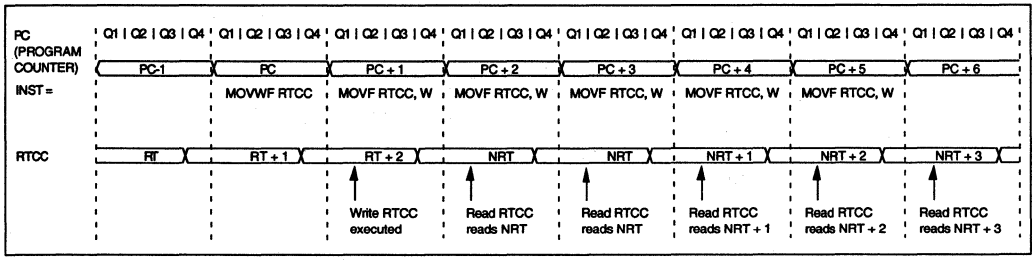


FIGURE 4.3B - RTCC TIMING: INT CLOCK/PRESCALE 1:2

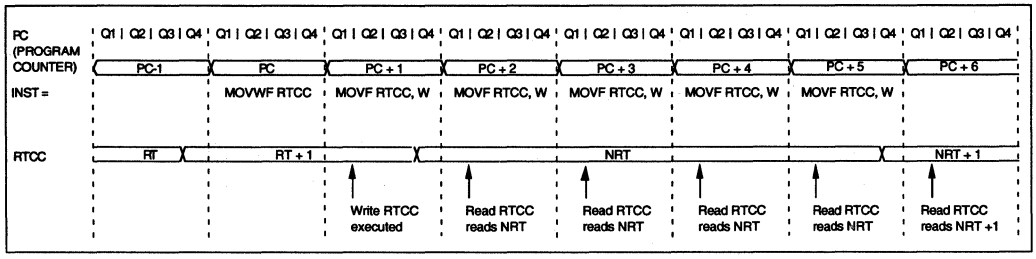
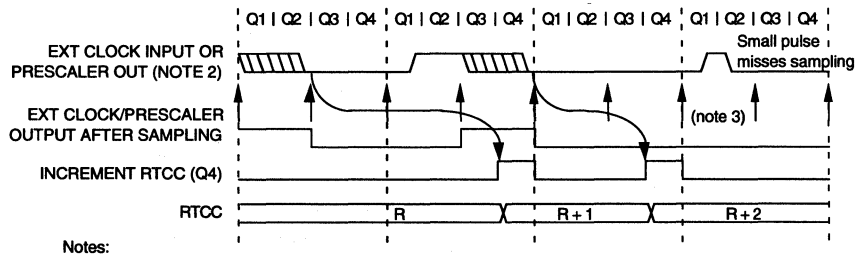


FIGURE 4.4 - RTCC TIMING WITH EXTERNAL CLOCK



Notes:

1. Delay from clock input change to RTCC increment is 3 tosc to 7 tosc. (Duration of Q = tosc). Therefore, the error in measuring the interval between two edges on RTCC input = ± 4 tosc max.
2. External clock if no prescaler selected, Prescaler output otherwise.
3. The arrows indicate the points in time where sampling occurs.

4.3 Program Counter

The program counter generates the addresses for on-chip ROM containing the program instruction words (Figure 4.5).

The program counter is set to all "1"s upon a RESET condition. During program execution it is auto incremented with each instruction unless the result of that instruction changes the PC itself:

a) GOTO instructions allow the direct loading of the lower nine program counter bits (PC <8:0>). The upper 2-bits of PC (PC<10:9>) are loaded with page select bits PA1, PA0 (bits 6,5 status register). Thus GOTO allows jump to any location on any page.

b) CALL instructions load the lower 8-bits of the PC directly while the ninth bit is cleared to "0". The PC value, incremented by one, will be pushed into the stack. The upper two bits of PC (PC<10:9>) are loaded with Page Select bits PA1, PA0 (STATUS <6:5>).

c) RETLW instructions load the program counter with the top of stack contents.

d) If the PC is the destination in any instruction (e.g. MOVWF PC, ADDWF PC, or BSF PC,5) then the computed 8-bit result will be loaded into the low 8-bits of program counter. The ninth bit of PC will be cleared. PC<10:9> will be loaded with Page Select bits PA1, PA0 (STATUS <6:5>).

It should be noted that because bit 8 (ninth bit) of PC is cleared in CALL instruction or any instruction which writes to the PC (e.g. MOVWF PC), all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

Incrementing the program counter when it is pointing to the last address of a selected memory page is also possible and will cause the program to continue in the next higher page. However, the page pre-select bits in the STATUS register will not be changed, and the next GOTO, CALL, ADDWF PC, MOVWF PC instruction will return to the previous page, unless the page pre-select bits have been updated under program control. For example, a NOP at location "1FF" (page 0) increments the PC to "200" (page 1). A "GOTO xxx" at "200" will return the program to address "xxx" on page "0" (assuming that the page preselect bits in The STATUS register are "0").

Upon a RESET condition, page 0 is pre-selected while the program counter addresses the last location in the last page. Thus, a GOTO instruction at this location will automatically cause the program to continue in page 0.

4.4 Stack

The PIC16CR57A series employs a two-level hardware push/pop stack (Figure 4.5).

The CALL instruction pushes the current program counter value, incremented by "1", into stack level 1. Stack level 1 is automatically pushed to level 2. If more than 2 subsequent "CALL"s are executed, only the most recent two return addresses are stored.

The page preselect bits of the STATUS register will be loaded into the most significant bits of the program counter. The ninth bit is always cleared to "0" upon a CALL instruction. This means that subroutine entry addresses have to be located always within the lower half of a memory page (addresses 000-0FF, 200-2FF, 400-4FF, 600-6FF). However, as the stack has the same width as the PC, subroutines can be called from anywhere in the program.

The RETLW instruction loads the contents of stack level 1 into the program counter while stack level 2 gets copied into level 1. If more than two subsequent "RETLW"s are executed, the stack will be filled with the address previously stored in level 2. The return will be always to the page from where the subroutine was called, regardless of the current setting of the page pre-select bits in the STATUS register. Note that the W register will be loaded with the literal value specified in the RETLW instruction. This is particularly useful for the implementation of "data" tables within the program memory.

4.5 Status Word Register

This register contains the arithmetic status of the ALU, the RESET status, and page preselect bits for program memory.

The STATUS register can be destination for any instruction like any other register. However, the status bits are set after the write. Furthermore, $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with status register as destination may be different than intended. For example, CLRF STATUS will clear all bits except for $\overline{TO}$ and $\overline{PD}$ and then set the Z bit and leave status register as 000UU100 (where U = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the status registers because these instructions do not affect any status bit.

For other instructions, affecting any status bits, see Section "Instruction Set Summary" (Table 10.1).

4.5.1 CARRY/BORROW AND DIGIT CARRY/ BORROW BITS:

The Carry bit (C) is a carry out in addition operation (ADDWF) and a borrow out in subtract operation (SUBWF).

It is also affected by RRF and RLF instructions. The following examples explain carry/borrow bit operation:

```
                ;SUBWF Example #1
                ;
clrf   0x1f     ;f(1fh)=0
movlw  1        ;wreg=1
subwf  0x1f     ;f(1fh) =f(1fh)-
                ;wreg=0-1=FFh
                ;Carry=0: Result is
                ;   negative
                ;
                ;SUBWF Example #2
movlw  0xFF     ;
movwf  0x1F     ;f(0x1F)=FFh
clrw            ;wreg=0
subwf  0x1F     ;f(0x1F)=f(0x1F)- wreg
                ;=FFh-0=FFh
                ;Carry=1:Result is
                ;   positive
                ;
```

The digit carry operates in the same way as the carry bit, i.e. it is a borrow in subtract operation.

FIGURE 4.5 - PROGRAM MEMORY ORGANIZATION

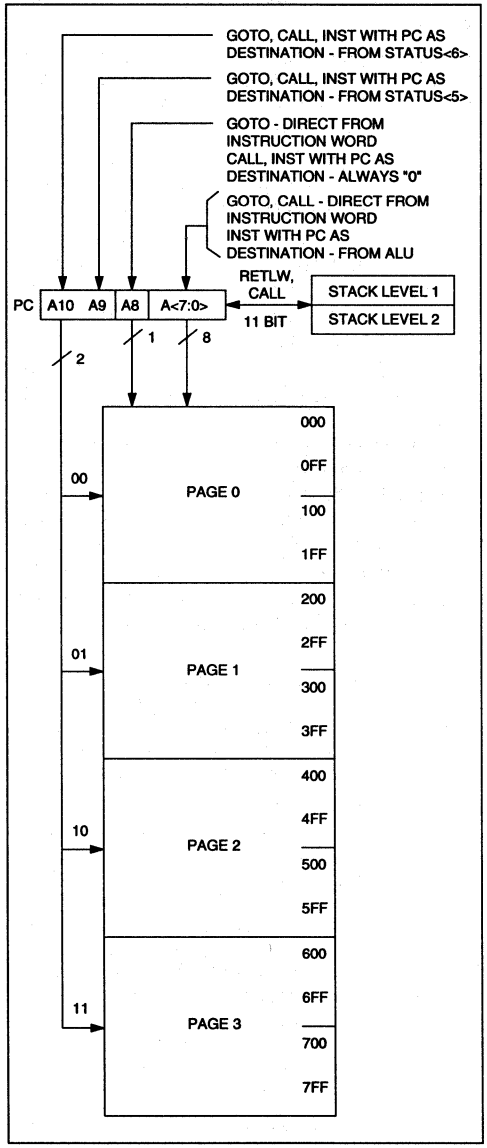
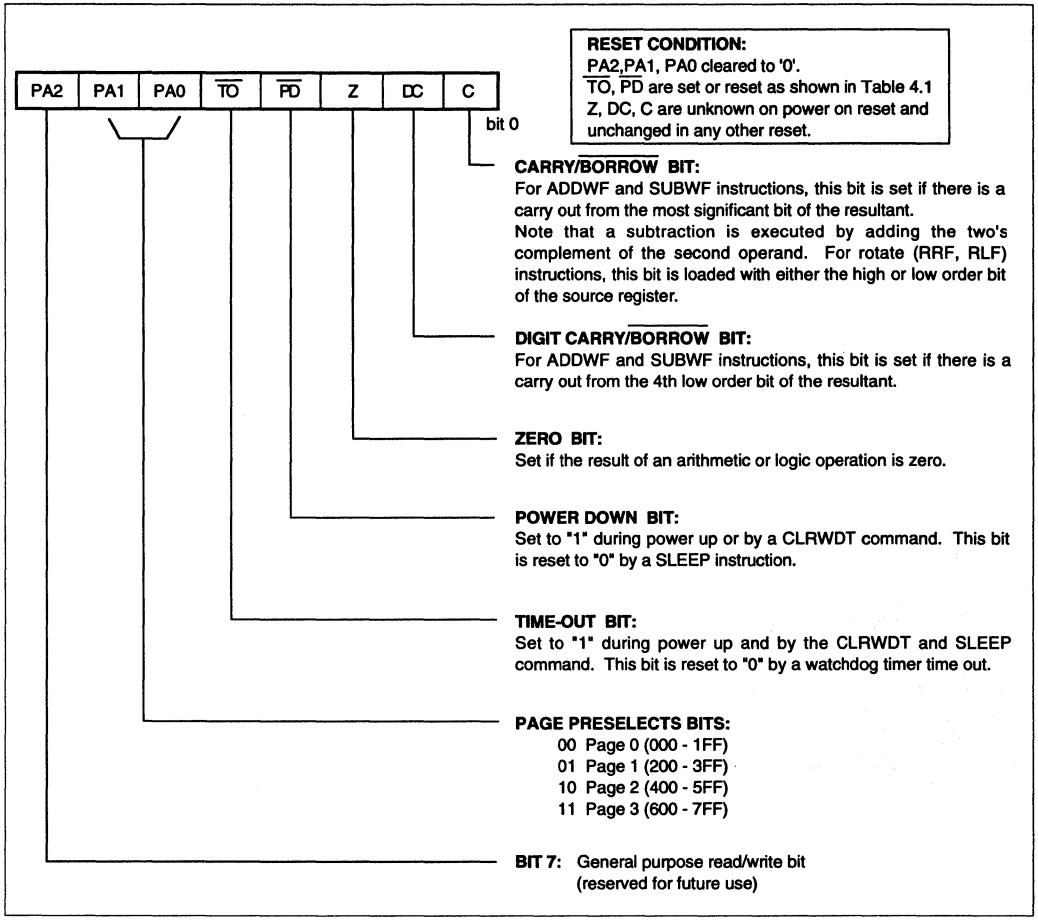


FIGURE 4.6 - STATUS WORD REGISTER



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4.5.2 TIME OUT AND POWER DOWN STATUS BITS ($\overline{TO}$, $\overline{PD}$)

The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be tested to determine if a RESET condition has been caused by a watchdog timer time-out, a power-up condition, or a wake-up from SLEEP by the Watchdog Timer or $\overline{MCLR}$ pin.

These status bits are only affected by events listed in Table 4.1.

TABLE 4.1 - EVENTS AFFECTING $\overline{PD}$/$\overline{TO}$ STATUS BITS

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
WDT Timeout	0	X	No effect on PD
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Note: A WDT timeout will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{PD}$ bit. Table 4.2 reflects the status of $\overline{PD}$ and $\overline{TO}$ after the corresponding event.

TABLE 4.2 - $\overline{PD}$/$\overline{TO}$ STATUS AFTER RESET

$\overline{TO}$	$\overline{PD}$	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT time-out (not during SLEEP)
1	0	$\overline{MCLR}$ wake-up from SLEEP
1	1	Power-up
U	U	Low pulse on $\overline{MCLR}$ input

Note: The $\overline{PD}$ and $\overline{TO}$ bit maintain their status (U) until an event of Table 4.1 occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{PD}$ and $\overline{TO}$ status bits.

4.5.3 PROGRAM PAGE PRESELECT

Bits 5-6 of the STATUS register are defined as page address bits PA<1:0>, and are used to preselect a program memory page. When executing a `GOTO`, `CALL`, or an instruction with PC as destination (e.g. `MOVWF PC`), PA<1:0> are loaded into bit A<10:9> of the program counter, selecting one of the available program memory pages. The direct address specified in the instruction is only valid within this particular memory page.

`RETLW` instructions do not change the page preselect bits.

Upon a RESET condition, PA<2:0> are cleared to "0"s.

4.6 File Select Register (FSR)

Bits 0-4 select one of the 32 available file registers in the indirect addressing mode (that is, calling for the INDF register in any of the file oriented instructions).

Bits 5-7 of the FSR are read-only and are always read as "one"s.

If no indirect addressing is used, the FSR can be used as a 5-bit wide general purpose register.

Bits 5 and 6 of the FSR select the current data memory bank (Figure 4.2).

The lower 16 bytes of each bank are physically identical and are always selected when bit 4 of the FSR (in case of indirect addressing) is "0", or bit 4 of the direct file register address of the currently executing instruction is "0" (e.g. `MOVWF DATAMEM`).

Only if bit 4 in the above mentioned cases is "1", bits 5 and 6 of the FSR select one of the four available register banks with 16 bytes each.

Bit 7 is read-only and is always read as "one."

5.0 I/O REGISTERS (PORTS)

The I/O registers can be written and read under program control like any other register of the register file. However, "read" instructions (e.g. `MOVF PORTB,W`) always read the I/O pins, regardless if a pin is defined as "input" or "output." Upon a RESET condition, all I/O ports are defined as "input" (= high impedance mode) as the I/O control registers (TRISA, TRISB and TRISC) are all set to "ones."

The execution of a "`TRIS f`" instruction with corresponding "zeros" in the W-register is necessary to define any of the I/O pins as output.

5.1 PORT A

4-bit I/O register. Low order 4-bits only are used (RA0 - RA3). Bits 4 - 7 are unimplemented and read as "zeros."

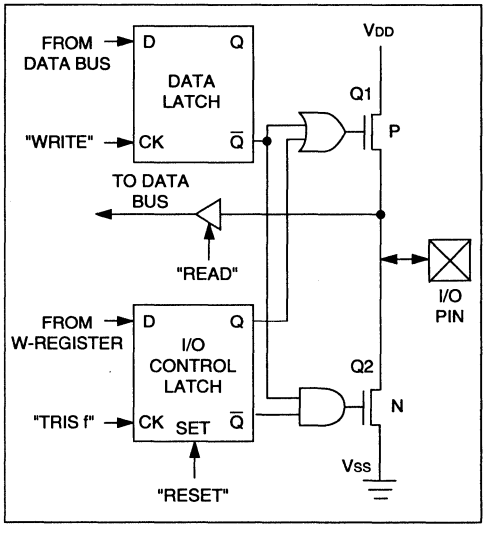
5.2 PORT B

8-bit I/O register.

5.3 PORT C

8-bit I/O Register.

FIGURE 5.1 - EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



5.4 I/O Interfacing

The equivalent circuit for an I/O port bit is shown in Figure 5.1. All ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g. `MOVF PORTB, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be set to zero. For use as an input, the corresponding TRIS bit must be "one". Any I/O pin can be programmed individually as input or output.

5.5 I/O Programming Considerations

5.5.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The `BCF` and `BSF` instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a `BSF` operation on bit 5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the `BSF` operation takes place on bit 5 and PORTB is re-output to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see Figure 5.2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

6.0 GENERAL PURPOSE REGISTERS

f08h - f0Fh: are general purpose register files which are always selected, independent of bank select.

f10h - f1Fh: general purpose register files in memory bank 0.

f20h - f2Fh: physically identical to f00 - f0F.

f30h - f3Fh: general purpose register files in memory bank 1.

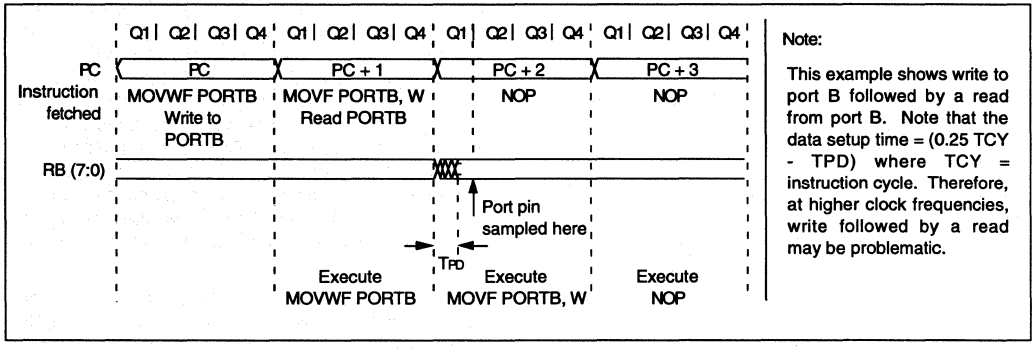
f40h - f4Fh: physically identical to f00 - f0F.

f50h - f5Fh: general purpose register files in memory bank 2.

f60h - f6Fh: physically identical to f00 - f0F.

f70h - f7Fh: general purpose register files in memory bank 3.

FIGURE 5.2 - I/O PORT READ/WRITE TIMING



7.0 SPECIAL PURPOSE REGISTERS

7.1 W Working Register

Holds second operand in two operand instructions and/ or supports the internal data transfer.

7.2 TRISA I/O Control Register For PORTA

Only bits 0 - 3 are available. PORT A is only 4-bits wide.

7.3 TRISB I/O Control Register For PORTB

The I/O control register will be loaded with the content of the W register by executing of the `TRIS PORT B` instruction. A "1" in the I/O control register puts the corresponding I/O pin into a high impedance mode. A "0" puts the contents of file register PORTB out on the selected I/O pins.

This register is "write-only" and is set to all "ones" upon a RESET condition.

7.4 TRISC I/O Control Register For PORTC

The I/O control register will be loaded with the content of the W register by executing of the `TRIS PORT C` instruction. A "1" in the I/O control register puts the corresponding I/O pin into a high impedance mode. A "0" puts the contents of the PORTC registe out on the selected I/O pins.

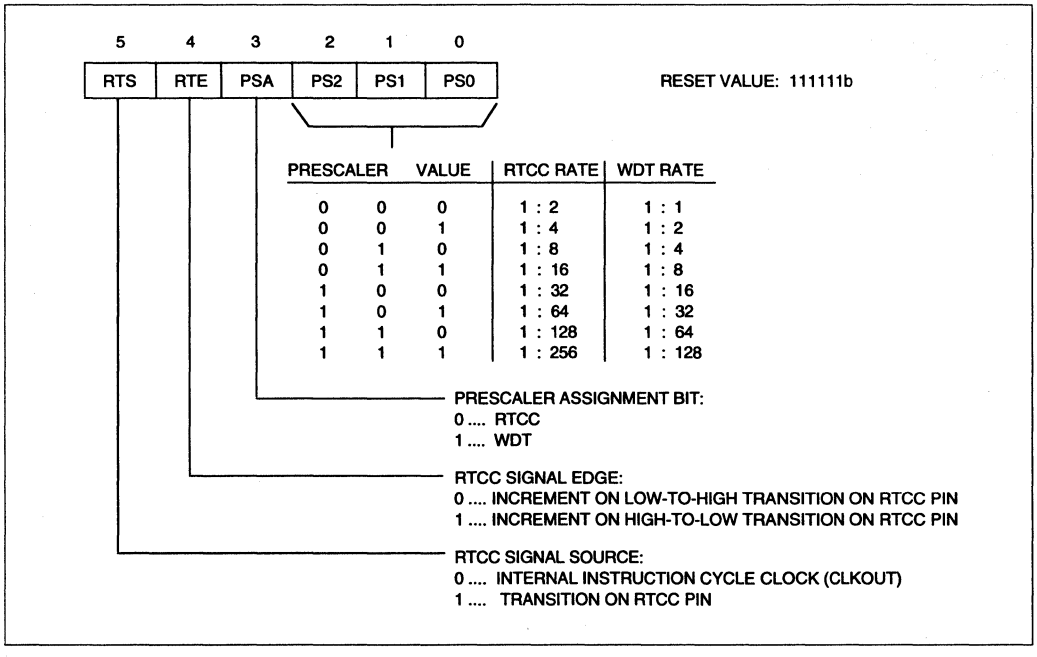
This register is "write-only" and is set to all "ones" upon a RESET condition.

7.5 OPTION Prescaler/RTCC Option Register

Defines prescaler assignment (RTCC or WDT), prescaler value, signal source and signal edge for the RTCC. The OPTION register is "write-only" and is 6 bit wide.

By executing the "`OPTION`" instruction, the contents of the "W" register will be transferred to the option register. Upon a RESET condition, the option register is set to all "ones."

FIGURE 7.1 - OPTION REGISTER



8.0 RESET CONDITION

A RESET condition can be caused by applying power to the chip (power-up), pulling the $\overline{MCLR}$ input "low", or by a Watchdog Timer timeout. The device will stay in RESET as long as the Oscillator Start-up Timer (OST) is active or the $\overline{MCLR}$ input is "low."

The Oscillator Start-up Timer is activated as soon as $\overline{MCLR}$ input is sensed to be high. This implies that in case of Power-On Reset with $\overline{MCLR}$ tied to V_{DD} the OST starts from power-up. In case of WDT time-out, it will start at the end of the time-out (since $\overline{MCLR}$ is high). In case of $\overline{MCLR}$ reset, the OST will start when $\overline{MCLR}$ goes high. The nominal OST time-out period is 18ms. See Section 13.0 for detailed information on OST and Power-On Reset.

During a RESET condition the state of the PIC16CR57A is defined as :

- The oscillator is running, or will be started (power-up or wake-up from SLEEP).
- All I/O port pins (RA0 - RA3, RB0 - RB7, and RC0-RC7) are put into the high-impedance state by setting the "TRIS" registers to all "ones" (= input mode).
- The Program Counter is set to all "ones" (1FFh).
- The OPTION register is set to all "ones".
- The Watchdog Timer and its prescaler are cleared.
- The upper three bits (page select bits) in the Status Register are cleared to "zero."
- "RC" mode only: The "CLKOUT" signal on the OSC2 pin is held at a"low" level.

TABLE 8-1: RESET CONDITION FOR REGISTERS (PIC16CR5XA):

Register	Address	• Power-on Reset	• $\overline{MCLR}$ Reset during: - normal operation - SLEEP • WDT timeout during normal operation	• Wake up from SLEEP through WDT timeout
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRISA	-	---- 1111	---- 1111	---- uuuu
TRISB	-	1111 1111	1111 1111	uuuu uuuu
TRISC	-	1111 1111	1111 1111	uuuu uuuu
OPTION	-	--11 1111	--11 1111	--uu uuuu
INDF	00h	-	-	-
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	02h	1FF/7FFh	000h	PC + 1
STATUS	03h	0001 1xxx	000? ?uuu	uuu0 0uuu
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu

Legend: u = unchanged
x = unknown
- = unimplemented bit, reads as '0'
? = value of $\overline{TO}$, $\overline{PD}$ bits depend on condition

9.0 PRESCALER

An 8-bit counter is available as a prescaler for the RTCC, or as a post-scaler for the Watchdog Timer, respectively (Figure 9.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the RTCC and the Watchdog Timer. Thus, a prescaler assignment for the RTCC means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS0-PS2 bits in the OPTION register determine the prescaler assignment and pre-scale ratio. When assigned to the RTCC, all instructions writing to the RTCC (e.g. `CLRF RTCC`, `MOVWF RTCC`, `BSF RTCC,x`....etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer.

9.1 Switching Prescaler Assignment

CHANGING PRESCALER FROM RTCC TO WDT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence must be executed when changing the prescaler assignment from RTCC to WDT:

```
1. MOVLW  B'xx0x0xxx'   ; Select internal clock and select new
2. OPTION               ; prescaler value. If new prescale value
                        ; is = '000' or '001', then select any other
                        ; prescale value temporarily.
3. CLRF 1               ; Clear RTCC and prescaler.
4. MOVLW  B'xxxx1xxx'   ; Select WDT, do not change prescale
                        ; value.
5. OPTION               ;
6. CLRWDT               ; Clears WDT and prescaler.
7. MOVLW  B'xxxx1xxx'   ; Select new prescale value.
8. OPTION               ;
```

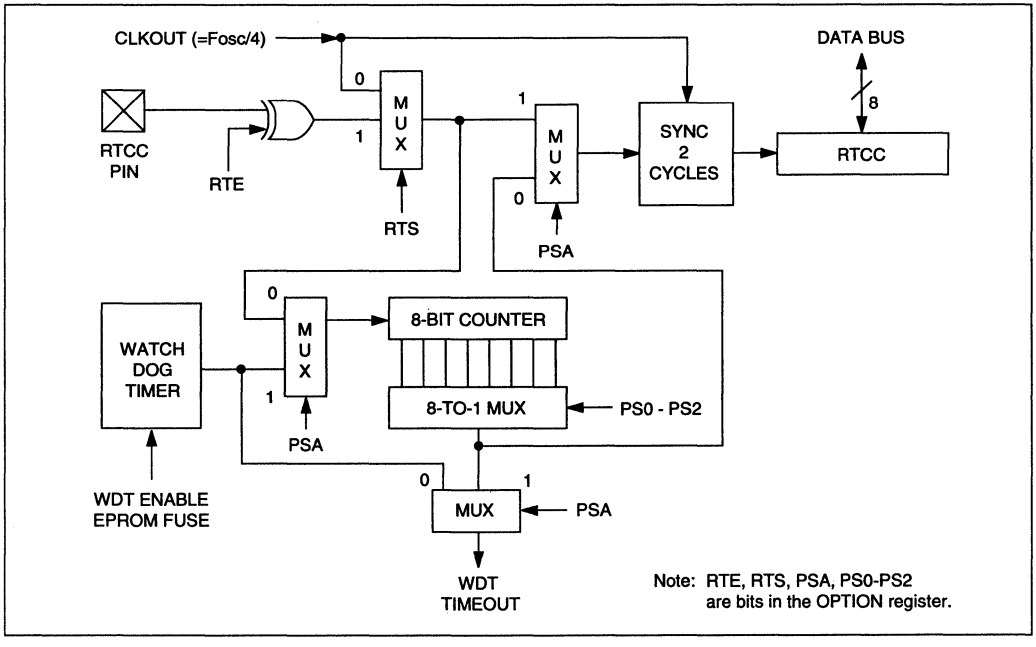
Steps 1 and 2 are only required if an external RTCC source is used. Steps 7 and 8 are necessary only if the desired prescale value is '000' or '001'.

CHANGING PRESCALER FROM WDT TO RTCC

To change prescaler from WDT to RTCC use the following sequence:

```
1. CLRWDT               ; Clear WDT and prescaler
2. MOVLW  B'xxxx0xxx'   ; Select RTCC, new prescale value
                        ; and clock source
3. OPTION               ;
```

FIGURE 9.1 - BLOCK DIAGRAM RTCC/WDT PRESCALER



10.0 BASIC INSTRUCTION SET SUMMARY

Each instruction is a 12-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The instruction set summary in Table 10.1 lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 file registers is to be utilized by the instruction.

The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Notes to Table 10.1

Note 1: The 9th bit of the program counter will be forced to a "zero" by any instruction that writes to the PC except for `GOTO` (e.g. `CALL`, `MOVWF PC` etc.). See Section 4.3 for details.

Note 2: When an I/O register is modified as a function of itself (e.g. `MOVF PORTB,1`), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as output and is driven low by an external device, the data will be written back with a '0'.

Note 3: The instruction "`TRIS f`", where f = PORTA, PORTB, or PORTC causes the contents of the W register to be written to the tristate latches of the specified file (port). A "one" forces the pin to a high impedance state and disables the output buffers.

Note 4: If this instruction is executed on The RTCC register (and, where applicable, d=1), the prescaler will be cleared if assigned to the RTCC.

TABLE 10.1 - INSTRUCTION SET SUMMARY

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4 - 0)
OPCODE	d	f(FILE #)

d = 0 for destination W
d = 1 for destination f

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0001 11df ffff 1Cf	Add W and f	**ADDWF**	f, d	W + f → d	C,DC,Z	1,2,4
0001 01df ffff 14f	AND W and f	**ANDWF**	f, d	W & f → d	Z	2,4
0000 011f ffff 06f	Clear f	**CLRF**	f	0 → f	Z	4
0000 0100 0000 040	Clear W	**CLRW**	-	0 → W	Z	
0010 01df ffff 24f	Complement f	**COMF**	f, d	$\bar{f}$ → d	Z	2,4
0000 11df ffff 0Cf	Decrement f	**DECF**	f, d	f -1 → d	Z	2,4
0010 11df ffff 2Cf	Decrement f,Skip if Zero	**DECFSZ**	f, d	f - 1 → d, skip if zero	None	2,4
0010 10df ffff 28f	Increment f	**INCF**	f, d	f + 1 → d	Z	2,4
0011 11df ffff 3Cf	Increment f,Skip if zero	**INCFSZ**	f, d	f + 1 → d, skip if zero	None	2,4
0001 00df ffff 10f	Inclusive OR W and f	**IORWF**	f, d	W v f → d	Z	2,4
0010 00df ffff 20f	Move f	**MOVF**	f, d	f → d	Z	2,4
0000 001f ffff 02f	Move W to f	**MOVWF**	f	W → f	None	1,4
0000 0000 0000 000	No Operation	**NOP**	-	-	None	
0011 01df ffff 34f	Rotate left f	**RLF**	f, d	f(n) → d(n+1), C → d(0), f(7) → C	C	2,4
0011 00df ffff 30f	Rotate right f	**RRF**	f, d	f(n) → d(n-1), C → d(7), f(0) → C	C	2,4
0000 10df ffff 08f	Subtract W from f	**SUBWF**	f, d	f - W → d [f + $\overline{W}$ + 1 → d]	C,DC,Z	1,2,4
0011 10df ffff 38f	Swap halves f	**SWAPF**	f, d	f(0-3) ↔ f(4-7) → d	None	2,4
0001 10df ffff 18f	Exclusive OR W and f	**XORWF**	f, d	W ⊕ f → d	Z	2,4

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4 - 0)
OPCODE	b(BIT #)	f(FILE #)

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0100 bbbf ffff 4bf	Bit Clear f	**BCF**	f, b	0 → f(b)	None	2,4
0101 bbbf ffff 5bf	Bit Set f	**BSF**	f, b	1 → f(b)	None	2,4
0110 bbbf ffff 6bf	Bit Test f,Skip if Clear	**BTFSC**	f, b	Test bit (b) in file (f): Skip if clear	None	
0111 bbbf ffff 7bf	Bit Test f, Skip if Set	**BTFSS**	f, b	Test bit (b) in file (f): Skip if set	None	

LITERAL AND CONTROL OPERATIONS

(11-8)	(7 - 0)
OPCODE	k (LITERAL)

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
1110 kkkk kkkk Ekk	AND Literal and W	**ANDLW**	k	k & W→ W	Z	
1001 kkkk kkkk 9kk	Call subroutine	**CALL**	k	PC + 1 → Stack, k → PC	None	1
0000 0000 0100 004	Clear Watchdog timer	**CLRWDT**	-	0 → WDT (and prescaler, if assigned)	$\overline{TO}$/$\overline{PD}$	
101k kkkk kkkk Akk	Go To address (k is 9 bit)	**GOTO**	k	k → PC (9 bits)	None	
1101 kkkk kkkk Dkk	Incl. OR Literal and W	**IORLW**	k	k v W → W	Z	
1100 kkkk kkkk Ckk	Move Literal to W	**MOVLW**	k	k → W	None	
0000 0000 0010 002	Load OPTION register	**OPTION**	-	W → OPTION register	None	
1000 kkkk kkkk 8kk	Return,place Literal in W	**RETLW**	k	k → W, Stack → PC	None	
0000 0000 0011 003	Go into standby mode	**SLEEP**	-	0 → WDT, stop oscillator	$\overline{TO}$/$\overline{PD}$	
0000 0000 0fff 00f	Tristate port f	**TRIS**	f	W→ I/O control register f	None	3
1111 kkkk kkkk Fkk	Excl. OR Literal and W	**XORLW**	k	k ⊕ W → W	Z	

Notes: See previous page

11.0 WATCHDOG TIMER (WDT)

The watchdog timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1/OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by specifying the WDT mask option.

11.1 WDT Period

The WDT has a nominal time-out period of 18ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.5 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the prescaler count, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit $\overline{TO}$ in the STATUS register will be cleared upon a watchdog timer timeout.

The WDT period is a function of the supply voltage, operating temperature, and will also vary from unit to unit due to variations in the manufacturing process. Please refer to the graphs in Section 18.0 and DC specs for more details.

11.2 WDT Programming Considerations

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

12.0 OSCILLATOR CIRCUITS

12.1 Oscillator Types

The PIC16CR57A series is available with four different oscillator options. Two bits in the configuaration word select one of these four modes. The customer specifies the desired oscillator type along with the ROM pattern. The parts are tested for the specific oscillator type.

12.2 Crystal Oscillator

The PIC16CR57A crystal options (XT, HS, or LP) need a crystal or ceramic resonator connected to the OSC1 and OSC2 pins to establish oscillation (Figure 12.1). XT = Standard crystal oscillator, HS = High speed crystal oscillator. The series resistor RS may be required for the "HS" oscillator, especially at lower than 20 MHz oscillation frequency. It may also be required in XT mode with AT strip-cut type crystals to avoid overdriving.

12.3 RC Oscillator

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 12.3 shows how the R/C combination is connected to the PIC16CR57A. For Rext values below 2.2kOhm, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3kOhm and 100kOhm.

Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See table in Section 18.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characteristics in Section 18.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 2.2 for timing).

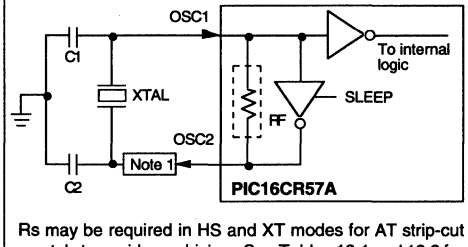
Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 12.1 - CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	150-330 pF
	2.0 MHz	20-330 pF
	4.0 MHz	20-330 pF
HS	8.0 MHz	20-200 pF

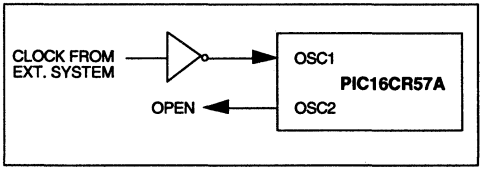
Note: The capacitor valves may change after characterization of the device. These values should be considered design targets.

FIGURE 12.1 - CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP TYPES ONLY)



Rs may be required in HS and XT modes for AT strip-cut crystals to avoid overdriving. See Tables 12.1 and 12.2 for recommended values of C1, C2 per oscillator type and frequency.

FIGURE 12.2 - EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP TYPES ONLY)



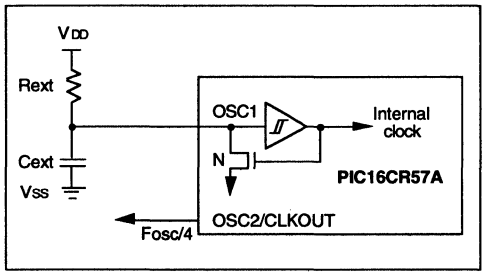
Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

TABLE 12.2 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	15 pF	15 pF
XT	100 KHz	15-30 pF	200-300 pF
	200 KHz	15-30 pF	100-200 pF
	455 KHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Note: The capacitor valves may change after characterization of the device. These values should be considered design targets.

FIGURE 12.3 - RC OSCILLATOR (RC TYPE ONLY)



13.0 OSCILLATOR START-UP TIMER (OST)

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. An on-chip Oscillator Start-up Timer is provided which keeps the device in a RESET condition for approximately 18ms after the voltage on the $\overline{MCLR}$ pin has reached a logic high (VIHMC) level. Thus, external RC networks connected to the $\overline{MCLR}$ input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The OST will also be triggered upon a watchdog timer timeout. This is particularly important for applications using the WDT to awake the PIC16CR57A from SLEEP mode automatically.

The OST is not adequate for low frequency crystals which require much longer than 18ms to start up and stabilize.

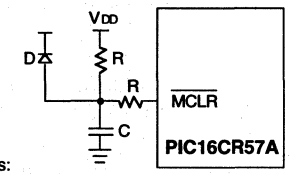
13.1 Power-On Reset (POR)

The PIC16CR57A incorporates an on chip Power-On Reset (POR) circuitry which provides internal chip reset for most power-up situations. To use this feature the user merely needs to tie $\overline{MCLR}$ pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 13.4. The power on reset circuit and the oscillator start-up timer circuit are closely related. On power-up the reset latch is set and the start-up timer (see Figure 13.4) is reset. The start-up timer begins counting once it detects $\overline{MCLR}$ to be high. After the time-out period, which is typically 18ms, it will reset the reset-latch and thus end the on-chip reset signal.

Figures 13.5 and 13.6 are two power-up situations with relatively fast rise time on VDD. In Figure 13.5, VDD is allowed to rise and stabilize before bringing $\overline{MCLR}$ high. The chip will actually come out of reset tOST ms after $\overline{MCLR}$ goes high. In Figure 13.1.6, the on chip Power-On Reset feature is being utilized ($\overline{MCLR}$ and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper reset. Figure 13.7 depicts a potentially problematic situation where VDD rises too slowly. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is therefore not guaranteed to function correctly.

To summarize, the on chip Power-On Reset is guaranteed to work if the rate of rise of VDD is no slower than 0.05 V/ms. It is also necessary that the VDD starts from 0V. The on-chip Power-On Reset is also not adequate for low frequency crystals which require much longer than 18ms to start up and stabilize. For such situations, we recommend that external RC circuits are used for longer Power-On Reset.

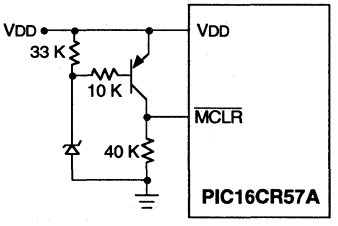
FIGURE 13.1 - EXTERNAL POWER ON RESET CIRCUIT (FOR SLOW POWER-UP)



Notes:

1. External power on reset circuit is required only if VDD power-up slope is too slow or if a low frequency crystal oscillator is being used that need a long start-up time. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40 KΩ must be observed to make sure that voltage drop across R does not exceed 0.2 V (max leakage current spec on $\overline{MCLR}$ pin is 5 μA). A larger voltage drop will degrade VIH level on $\overline{MCLR}$ pin.
3. R1= 100Ω to 1KΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$ pin breakdown due to ESD or EOS.

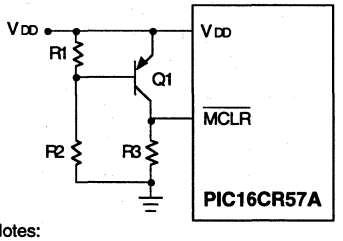
FIGURE 13.2 - BROWN OUT PROTECTION CIRCUIT



Notes:

1. This circuit will activate reset when VDD goes below (VZ + 0.7 V) where VZ = Zener voltage.

FIGURE 13.3 - BROWN OUT PROTECTION CIRCUIT



Notes:

1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$VDD \cdot \frac{R1}{R1 + R2} = 0.7\ V.$$

Preliminary

FIGURE 13.4 - SIMPLIFIED POWER ON RESET BLOCK DIAGRAM

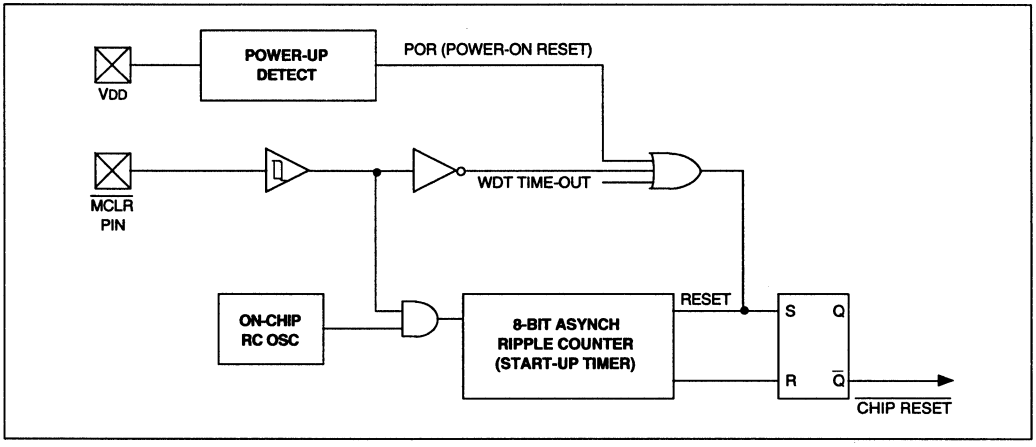
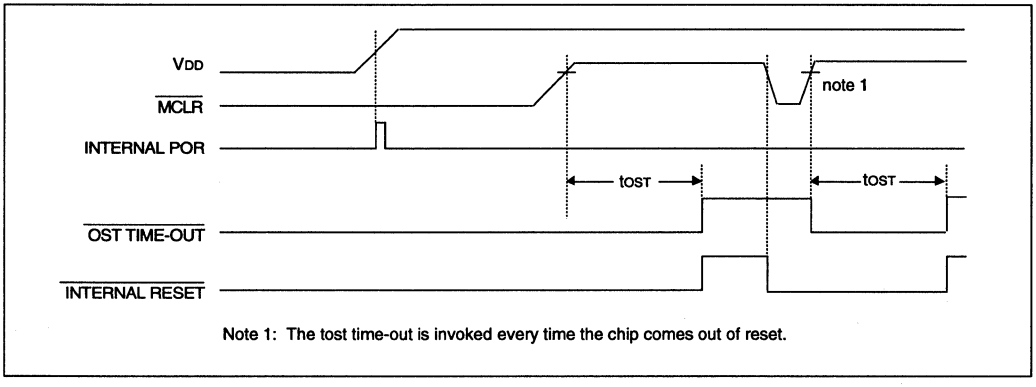


FIGURE 13.5 - USING EXTERNAL RESET INPUT



Note 1: The tost time-out is invoked every time the chip comes out of reset.

FIGURE 13.6 - USING ON-CHIP POR (FAST VDD RISE TIME)

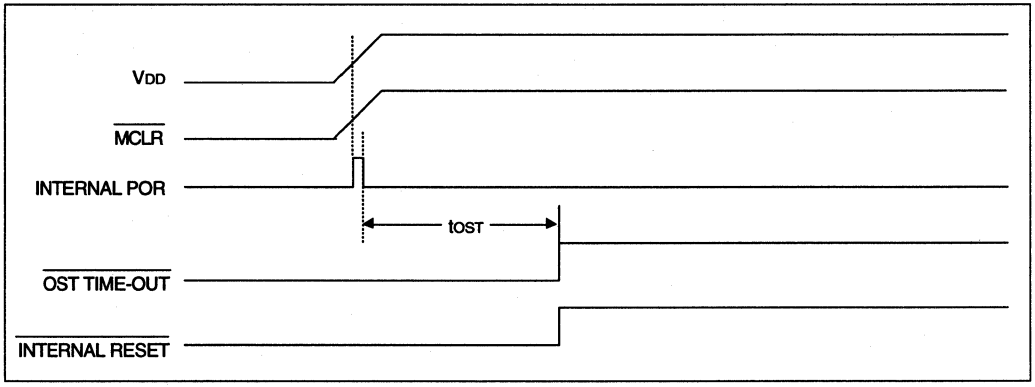
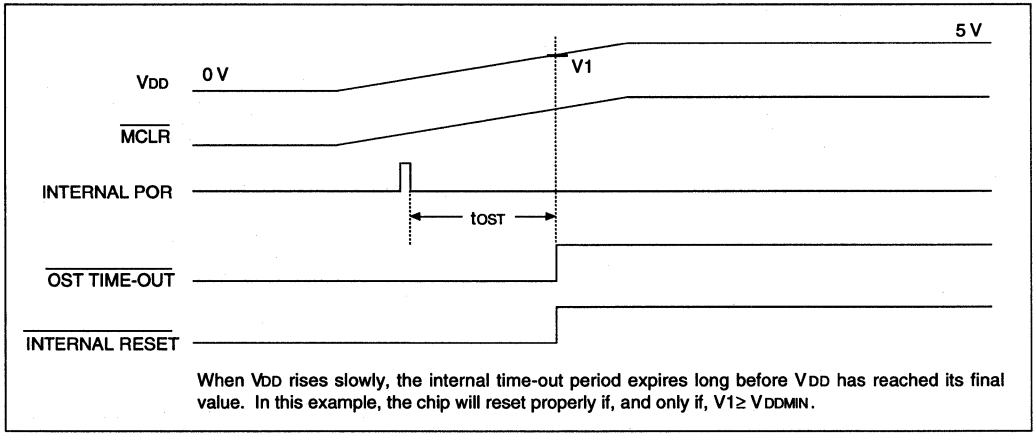


FIGURE 13.7 - USING ON-CHIP POR (SLOW VDD RISE TIME)



When VDD rises slowly, the internal time-out period expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1≥ VDDMIN.

14.0 POWER DOWN MODE (SLEEP)

The power down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the bit "PD " in the STATUS register is cleared, the "TO " bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are in the High-impedance mode should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC input should also be at VDD or VSS for lowest current consumption.

The $\overline{MCLR}$ pin must be at VIHMC.

14.1 Wake-Up

The device can be awakened by a Watchdog Timer time-out (if it is enabled) or an externally applied "low" pulse at the $\overline{MCLR}$ pin. In both cases the 16CR57A will stay in RESET mode for one Oscillator Start-up Timer period (triggered from rising edge on $\overline{MCLR}$ or WDT time-out) before normal program execution resumes.

The "PD" bit in the STATUS register, which is set to one during power-on, but cleared by the "SLEEP" command, can be used to determine if the processor was powered up or awakened from the power down mode (Table 4.2). The $\overline{TO}$ bit in the STATUS register can be used to determine, if the "wake up" was caused by an external $\overline{MCLR}$ signal or a Watchdog Timer time-out.

NOTE: Some applications may require external R/C networks on the $\overline{MCLR}$ pin in order to allow for oscillator start-up times longer than one OST period. In this case, a WDT wake up from power down mode is not recommended, because a RESET generated by a WDT time out does not discharge the external capacitor, and the 16CR57A will be in RESET only for the oscillator start-up timer period.

15.0 CONFIGURATION FUSES

The configuration ROM consists of four ROM fuses.

Two are for the selection of the oscillator type, one is the Watchdog Timer enable fuse, and one is the code protection fuse.

15.1 Customer ID Code

The PIC16CR57A series has 16 special ROM bits which are not part of the normal program memory. These bits are available to the user to store an Identifier (ID) code, checksum, or other informative data. They cannot be accessed during normal program execution.

15.2 Code Protection

The program code written into the ROM can be protected by programming the code protection fuse with "0".

When code protected, the contents of the program ROM cannot be read out in a way that the program code can be reconstructed.

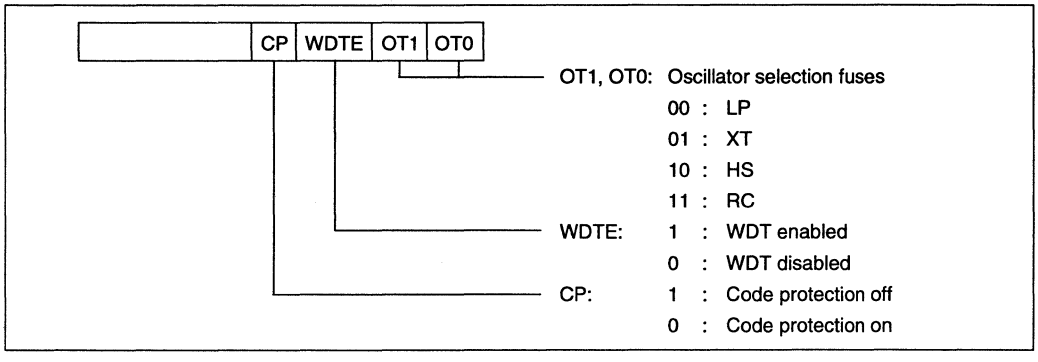
Note that the configuration fuses and the ID bits can still be read, even if the code protection logic is active.

15.2.1 VERIFYING A CODE-PROTECTED PART

When code protected verifying any program memory location will read a scrambled output which looks like "00000000XXXX" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

a. First, program and verify a good PIC16C57 without code protecting it.
b. Next, blow its code protection fuse and then load its contents in a file.
c. Verify any code-protected PIC16CR57A (with this program) against this file.

FIGURE 15.1 - CONFIGURATION FUSES



16.0 DEVELOPMENT SUPPORT

16.1 Development Tools

The PIC16C5X and PIC16CXX microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER™ Real-Time In-Circuit Emulator
- PRO MATE™ Universal Programmer
- PICSTART™ Low-Cost Prototype Programmer
- Assembler
- Software Simulator

16.2 PICMASTER™: High Performance Universal In-Circuit Emulator

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X, PIC16CXX and PIC17CXX families.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16C5X, PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on PC compatible machines ranging from 80286-AT® class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.1 environment, allowing the operator access to a wide range of supporting software and accessories.

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.1 environment was chosen to best make these features available to you, the end user.

The PICMASTER Emulator Universal System consists primarily of four major components:

- Host-Interface Card
- Emulator Control Pod
- Target-Specific Emulator Probe
- PC Host Emulation Control Software

The Windows 3.1 System is a multitasking operating system which will allow the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window.

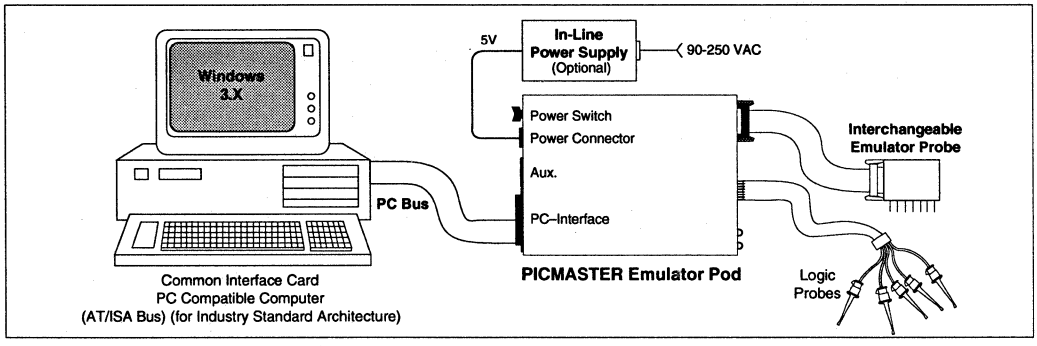
Dynamic Data Exchange (DDE), a feature of Windows 3.1, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

Under Windows 3.1, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16CXX processor and a PIC17CXX processor).

16.3 PRO MATE™: Universal Programmer

The PRO MATE Universal Programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MATE has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability . It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MATE can read, verify or program PIC16C5X, PIC16CXX and PIC17CXX devices. It can also set fuse configuration and code-protect in this mode. Its EEPROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.



In PC-hosted mode, the PRO MATE connects to the PC via one of the COM (RS232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of VDD min, VDD max and VPP levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different serial number, sequential or random.

The PRO MATE has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. PRO MATE supports all PIC16C5X, PIC16CXX and PIC17CXX processors.

16.4 PICSTART™ Programmer

The PICSTART™ programmer is an easy to use, very low-cost prototype programmer. It connects to the PC via one of the COM (RS232) ports. A PC based user interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based.

16.5 Assembler (MPASM)

Cross Assembler is a PC hosted symbolic assembler. It supports all microcontroller series including the PIC16C5X CMOS, PIC16CXX, and PIC17CXX families.

MPASM offers fully featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from the Microchip Universal Emulator System (PICMASTER).

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro Assembly Capability
- Provides Object, Listing, Symbol and special files required for debugging with one of the Microchip Emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a full feature directive language represented by four basic classes of directives:

- **Data Directives** are those that control the allocation of memory and provide a way to refer to data items symbolically, by meaningful names.
- **Listing Directives** control the MPASM listing dis play. They allow the specification of titles and subtitles, page ejects and other listing control.
- **Control Directives** permit sections of conditionally assembled code.
- **Macro Directives** control the execution and data allocation within macro body definitions.

16.6 Software Simulator (MPSIM)

The Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16C5X and PIC16CXX series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in single step, execute until break or in a trace mode. Two forms of symbolic debugging are available: an internal symbol table for disassembling opcodes and the displaying of source code from a listing file. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

16.7 Development Systems

For convenience, the development tools are packaged into comprehensive systems as listed in Table 16-1:

TABLE 16-1: DEVELOPMENT SYSTEM PACKAGES

Item	Name	System Description
1.	PICMASTER™ System	PICMASTER In-Circuit Emulator with your choice of Target Probe, PRO MATE Programmer, Assembler, Software Simulator and Samples.
2.	PICSTART™ System	PICSTART™ Low-Cost Prototype Programmer, Assembler, Software Simulator and Samples

16.8 Probe Specifications

The PICMASTER probes currently meet the following specifications:

PICMASTER PROBE	Devices Supported	PROBE Maximum Frequency	PROBE Operating Voltage
PROBE - 16A	PIC16C54, PIC16C55, PIC16C56, and PIC16C57	4 MHZ	4.5V - 5.5V
PROBE - 16D	PIC16C54, PIC16C55, PIC16C56, PIC16C57, and PIC16C58	20 MHz	4.5V - 5.5V

17.0 ELECTRICAL CHARACTERISTICS

17.1 Absolute Maximum Ratings*

Ambient temperature under bias ..... -55°C to +125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss
(except VDD, $\overline{MCLR}$ and RT) ..... -0.6V to VDD +0.6V
Voltage on VDD with respect to Vss ..... 0 to +7.5 V
Voltage on $\overline{MCLR}$ and RT with respect to Vss
(Note 2) ..... 0 to +14 V
Total power Dissipation (Note 1) ..... 800 mW
Max. Current out of Vss pin ..... 150 mA
Max. Current into VDD pin ..... 100 mA
Input Clamp Current, IIK (VI<0 or VI>VDD) ..... ±20 mA
Output Clamp Current, IOK (VO<0 or VO>VDD) ±20 mA
Max. Output Current sinked by any I/O pin ..... 25 mA
Max. Output Current sourced by any I/O pin .... 20 mA
Max. Output Current sourced by a single
I/O port Port A ..... 50 mA
Port B or Port C..... 100 mA
Max. Output Current sinked by a single
I/O port Port A ..... 50 mA
Port B or Port C..... 100 mA

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
$Pdis = V_{DD} \times \{I_{DD} - \Sigma Ioh\} + \Sigma\{(V_{DD}-Voh) \times Ioh\} + \Sigma(Vol \times Iol)$

TABLE 17.1 - PIN DESCRIPTIONS

Name	Function	Observation
RA0 - RA3	I/O PORT A	4 input/output lines. TTL input buffers.
RB0 - RB7	I/O PORT B	8 input/output lines. TTL input buffers.
RC0 - RC7	I/O PORT C	8 input/output lines. TTL input buffers.
RTCC	Real Time Clock/Counter	Schmitt Trigger Input. Clock input to RTCC register. Must be tied to Vss or VDD if not in use to avoid unintended entering of test modes and to reduce current consumption.
$\overline{MCLR}$	Master Clear	Schmitt Trigger Input. A "Low" voltage on this input generates a RESET condition. A rising voltage triggers the on-chip oscillator start-up timer which keeps the chip in RESET mode for about 18ms. This input must be tied directly, or via a pull-up resistor, to VDD.
OSC1/CLKIN	Oscillator (input)/External Clock Input	"XT", "HS" and "LP" devices: Input terminal for crystal, ceramic resonator, or external clock generator. "RC" devices : Driver terminal for external RC combination to establish oscillation.
OSC2/CLKOUT	Oscillator (output)	For "XT", "HS" and "LP" devices: Output terminal for crystal and ceramic resonator. Do not connect any other load to this output. Leave open if external clock generator is used. For "RC" devices : A "CLKOUT" signal with a frequency of 1/4 Fosc1 is put out on this pin.
VDD	Power supply	
Vss	Ground	
N/C	No (internal) Connection	

17.2 DC CHARACTERISTICS: PIC16CR57A-04 (COMMERCIAL, INDUSTRIAL)
PIC16CR57A-10 (COMMERCIAL, INDUSTRIAL)
PIC16CR57A-20 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS		Standard Operating Conditions Operating temperature				-40°C ≤ TA ≤ +125°C for automotive, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial
Characteristic	**Sym**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
Supply Voltage						
	VDD	3.0		6.25	V	XT, RC and LP options
		4.5		5.5	V	HS option
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on
Supply Current (Note 2)						
	IDD					XT and RC options
			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
						HS option
			4.8	10	mA	FOSC = 10 MHz , VDD = 5.5V
			9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
						LP option, Commercial
			15	32	µA	FOSC = 32 KHz, VDD = 3.0V, WDT disabled
						LP option, Industrial
			19	48	µA	FOSC = 32 KHz, VDD = 3.0V, WDT disabled
Power Down Current (Note 4)						
WDT enabled	IPD		4	12	µA	VDD = 3.0V, Commercial
			5	14	µA	VDD = 3.0V, Industrial
WDT disabled			0.6	9	µA	VDD = 3.0V, Commercial
			0.8	12	µA	VDD = 3.0V, Industrial

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

17.3 DC CHARACTERISTICS: PIC16LCR57A-04 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial					
Characteristic	**Sym**	**Min**	**Typ ***	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.5		6.25	V	XT, RC and LP options
		4.5		5.5	V	HS option
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on reset
Supply Current (Note 2)	IDD					XT and RC options
			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
						HS option
			4.8	10	mA	FOSC = 4 MHz, VDD = 5.5V
						LP option, Commercial
			15	32	µA	FOSC = 32 KHz, VDD = 2.5V, WDT disabled
						LP option, Industrial
			19	40	µA	FOSC = 32 KHz, VDD = 2.5V, WDT disabled
Power Down Current (Note 4)						
WDT enabled	IPD		4	12	µA	VDD = 2.5V, Commercial
			5	14	µA	VDD = 2.5V, Industrial
WDT disabled			0.6	9	µA	VDD = 2.5V, Commercial
			0.8	12	µA	VDD = 2.5V, Industrial

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1= external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

17.4 DC CHARACTERISTICS: PIC16CR57A-04 (COMMERCIAL, INDUSTRIAL)
PIC16LCR57A-04 (COMMERCIAL, INDUSTRIAL)
PIC16CR57A-10 (COMMERCIAL, INDUSTRIAL)
PIC16CR57A-20 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY

Standard Operating Conditions
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Input Low Voltage						
I/O ports	VIL	VSS		0.2 VDD	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt trigger)		VSS		0.15 VDD	V	
RTCC (Schmitt trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt trigger)		VSS		0.15 VDD	V	RC option only (Note 5)
OSC1		VSS		0.3 VDD	V	XT, HS and LP options
Input High Voltage						
I/O ports	VIH	0.45 VDD		VDD	V	For all VDD (Note 6)
		2.0		VDD	V	4.0 V < VDD ≤ 5.5 V (Note 6)
		0.36 VDD		VDD	V	VDD > 5.5 V
$\overline{MCLR}$ (Schmitt trigger)		0.85 VDD		VDD	V	
RTCC (Schmitt trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt trigger)		0.85 VDD		VDD	V	RC option only (Note 5)
OSC1		0.7 VDD		VDD	V	XT, HS and LP options
Input Leakage Current (Note 4)						**For VDD ≤ 5.5V**
I/O ports	IIL	-1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{MCLR}$		-5			µA	VPIN = VSS + 0.25V (Note 3)
$\overline{MCLR}$			0.5	+5	µA	VPIN = VDD (Note 3)
RTCC		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD , XT, HS and LP options
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT (RC option only)				0.6	V	IOL = 1.6 mA, VDD = 4.5V
Output High Voltage						
I/O Ports (Note 4)	VOH	VDD-0.7			V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT (RC option only)		VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : In RC oscillator mode, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16CR57A be driven with external clock in RC mode.

Note 6: The user may use better of the two specifications.

17.5 AC CHARACTERISTICS: PIC16CR57A-04 (COMMERCIAL, INDUSTRIAL)
PIC16LCR57A-04 (COMMERCIAL, INDUSTRIAL)
PIC16CR57A-10 (COMMERCIAL, INDUSTRIAL)
PIC16CR57A-20 (COMMERCIAL, INDUSTRIAL)

AC CHARACTERISTICS **Standard Operating Conditions**
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
External CLOCKIN Frequency (Note 2)	FOSC	DC		4	MHz	RC mode
		DC		4	MHz	XT mode
		DC		20	MHz	HS mode (Com/Ind) (Note 5)
		DC		40	KHz	LP mode
Oscillator Frequency (Note 2)	FOSC	DC		4	MHz	RC mode
		0.1		4	MHz	XT mode
		4		20	MHz	HS mode (Com/Ind) (Note 5)
		DC		40	KHz	LP mode
Instruction Cycle Time (Note 2)	TCY	1.0		DC	µs	RC mode
		1.0	4/FOSC	DC	µs	XT mode
		0.2		DC	µs	HS mode (Note 5)
		100		DC	µs	LP mode
External Clock in Timing (Note 4)						
Clock in (OSC1) High or Low Time						
XT oscillator type	TCKHLXT	50*			ns	
LP oscillator type	TCKHLLP	2*			µs	
HS oscillator type	TCKHLHS	20*			ns	
Clock in (OSC1) Rise or Fall Time						
XT oscillator type	TCKRFXT	25*			ns	
LP oscillator type	TCKRFLP	50*			ns	
HS oscillator type	TCKRFHS	25*			ns	
RESET Timing						
$\overline{MCLR}$ Pulse Width (low)	TMCL	100*			ns	
RTCC Input Timing, No Prescaler						
RTCC High Pulse Width	TRTH	0.5 TCY+ 20*			ns	Note 3
RTCC Low Pulse Width	TRTL	0.5 TCY+ 20*			ns	Note 3
RTCC Input Timing, With Prescaler						
RTCC High Pulse Width	TRTH	10*			ns	Note 3
RTCC Low Pulse Width	TRTL	10*			ns	Note 3
RTCC Period	TRTP	$\frac{T_{CY}+40}{N}$ *			ns	Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Timeout Period (No Prescaler)	TWDT	9*	18*	30*	ms	VDD = 5.0V
Oscillation Start-up Timer Period	TOST	9*	18*	30*	ms	VDD = 5.0V

* Guaranteed by characterization, but not tested.

(Cont. on next page)

17.5 AC CHARACTERISTICS: (Cont.)

PIC16CR57A-04 (COMMERCIAL, INDUSTRIAL)
PIC16LCR57A-04 (COMMERCIAL, INDUSTRIAL)
PIC16CR57A-10 (COMMERCIAL, INDUSTRIAL)
PIC16CR57A-20 (COMMERCIAL, INDUSTRIAL)

AC CHARACTERISTICS **Standard Operating Conditions**
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
I/O Timing						
I/O pin input valid before CLKOUT↑ (RC Mode)	TDS	0.25 TCY+ 30*			ns	
I/O pin input hold after CLKOUT↑ (RC Mode)	TDH	0*			ns	
I/O pin output valid after CLKOUT↓ (RC Mode)	TPD			40*	ns	
I/O pin input valid before OSC↑ (I/O setup time)	TioV2osH	TBD	13		ns	VDD = 5.0V
OSC1↑ to I/O pin input valid (I/O hold time)	TosH2ioL	TBD			ns	VDD = 5.0V
OSC1↑ to I/O pin output valid	TosH2ioV	TBD	63		ns	VDD = 5.0V
OSC1↑ to CLKOUT low	TosH2ckL	TBD	57		ns	VDD = 5.0V
OSC1↑ to CLKOUT high	TosH2ckH	TBD	56		ns	VDD = 5.0V
I/O pin input valid before CLKOUT high	TioV2ckH	TBD	13		ns	VDD = 5.0V
CLKOUT low to I/O valid	TckL2ioV	TBD			ns	VDD = 5.0V
CLKOUT rise time	TckR		12	TBD	ns	VDD = 5.0V
CLKOUT fall time	TioF		12	TBD	ns	VDD = 5.0V
I/O pin output rise time	TioR		17	TBD	ns	VDD = 5.0V
I/O pin output fall time	TioF		10	TBD	ns	VDD = 5.0V
Capacitive Loading Specs on Output Pins						
OSC2 pin	COSC2			15	pF	In XT, HS or LP modes when external clock is used to drive OSC1
All I/O pins and OSC2 (in RC mode)	CIO			50	pF	

* Guaranteed by characterization, but not tested.

Note 1. Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2. Instruction cycle period (Tcy) equals four times the input oscillator time base period.
All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Note 3. For a detailed explanation of RTCC input clock requirements see section 4.2.1.

Note 4. Clock-in high-time is the duration for which clock input is at VIHOSC or higher.
Clock-in low-time is the duration for which clock input is at VILOSC or lower.

Note 5. This HS specification is only for the -20 device. The -10 device has a maximum of 10 MHz and the -04 device has a maximum of 4 MHz.

17.6 Electrical Structure of Pins

FIGURE 17.1 - ELECTRICAL STRUCTURE OF I/O PINS (RA, RB, and RC)

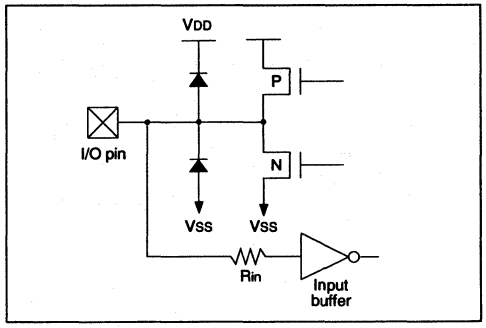
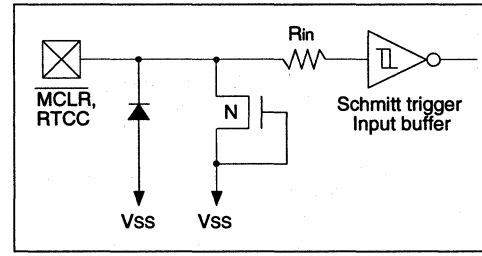


FIGURE 17.2 - ELECTRICAL STRUCTURE OF $\overline{MCLR}$ AND RTCC PINS



Notes to Figures 17.1 and 17.2: The diodes and the grounded gate (or output driver) NMOS device are carefully designed to protect against ESD (Electrostatic discharge) and EOS (Electrical overstress). Rin is a small resistance to further protect the input buffer from ESD.

18.0 TIMING DIAGRAMS

FIGURE 18.1 - RTCC TIMING

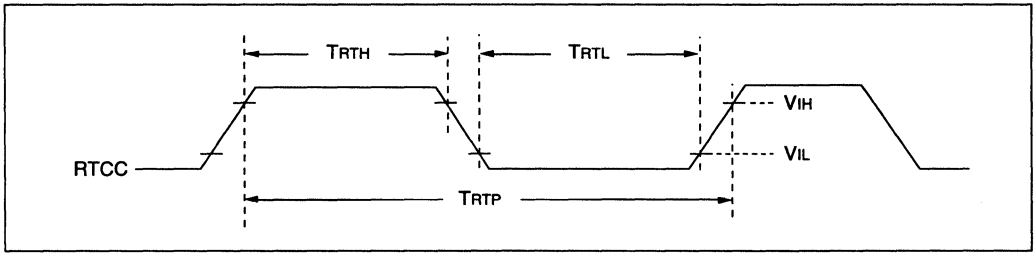


FIGURE 18.2 - OSCILLATOR START-UP TIMING (RC mode)

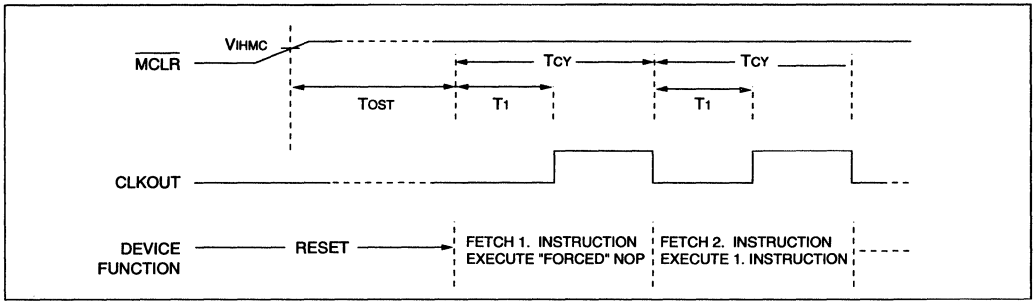
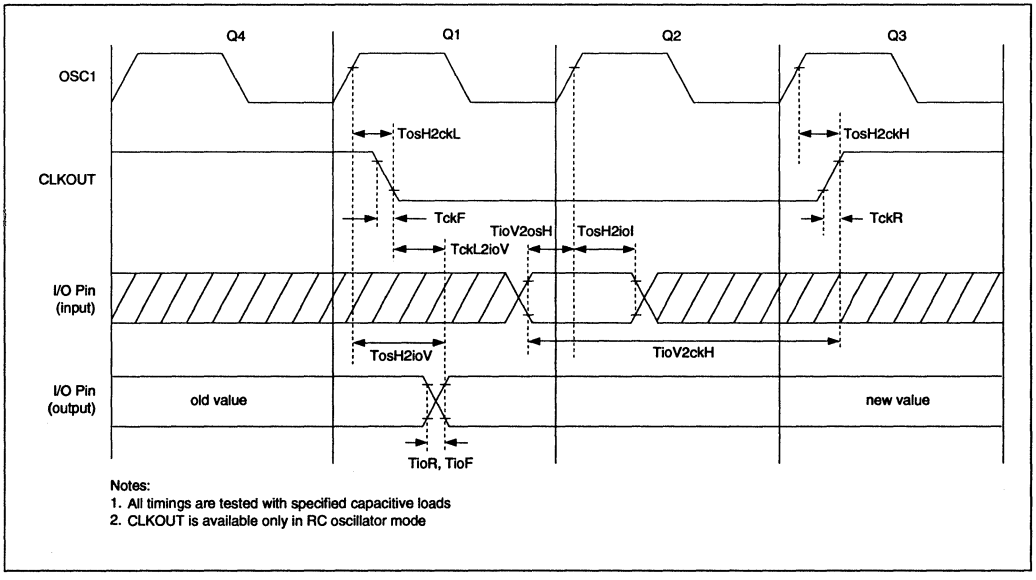


FIGURE 18.3 - INPUT/OUTPUT TIMING FOR I/O PORTS



Notes:
1. All timings are tested with specified capacitive loads
2. CLKOUT is available only in RC oscillator mode

19.0 DC & AC CHARACTERISTICS GRAPHS/TABLES

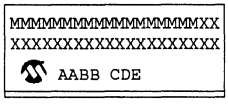
NOT AVAILABLE AT THIS TIME

20.0 PACKAGING DIAGRAMS AND DIMENSIONS

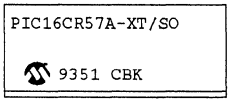
See Section 11 of the Data Book.

20.1 Package Marking Information

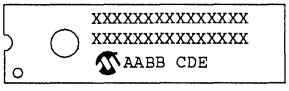
28L SOIC



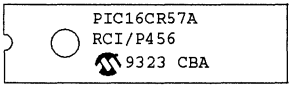
Example



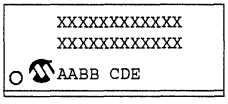
28L PDIP (.300 mil)



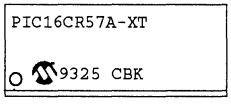
Example



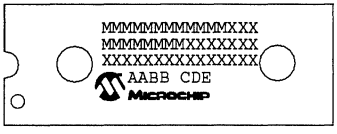
28L SSOP



Example



28L PDIP (.600 mil)



Example

Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

*Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are incuded in QTP price.

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CONNECTING TO MICROCHIP BBS

Connect world wide to the Microchip BBS using the CompuServe communications network. In most cases a local call is your only expense. The Microchip BBS connection does not use CompuServe membership services, therefore **you do not need CompuServe membership to join Microchip's BBS.**

The procedure to connect will vary slightly from country to country. Please check with your local CompuServe agent for details if you have a problem. CompuServe services allows multiple users at baud rates up to 9600.

To connect:

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.

2. Dial your local CompuServe phone number.

3. Depress **<ENTER>** and a garbage string will appear because CompuServe is expecting a 7E1 setting.

4. Type **+ <ENTER>** and `Host Name:` will appear.

5. Type **MCHIPBBS<ENTER>** and you will be connected to the Microchip BBS.

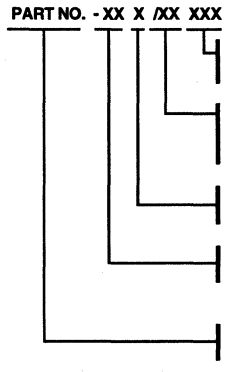
In the United States, to find CompuServe's phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600 baud connection. After the system responds with `Host Name:`, type

NETWORK<ENTER> and follow CompuServe's directions.

For voice information (or calling from overseas), you may call (614) 457-1550 for your local CompuServe number.

PIC16CR57A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Pattern:	3-Digit Pattern Code for QTP (factory specified) (blank for OTP and Windowed Parts)	
Package:	P = PDIP (300 or 600 mil)	
	SO = SOIC (Gull Wing, 300 mil body)	
	SS = SSOP (209 mil)	
Temperature Range:	- = 0°C to +70°C (T for tape/reel)	
	I = -40°C to +85°C (S for tape/reel)	
Frequency Range:	04 = 4 MHz	
	10 = 10 MHz	
	20 = 20 MHz	
Device:	PIC16CR57A : Standard VDD range	
	PIC16LCR57A : Extended VDD range	

Examples:

a) PIC16CR57A - 04/P301
= Commercial temp.,
PDIP package,
4 MHz, standard VDD limits,
QTP pattern # 301

b) PIC16LCR57A - 04I/SO495
= Industrial temp.,
SOIC package,
4 MHz, extended VDD limits

c) PIC16CR57A - 20I/P351
= Industrial temp.,
PDIP package,
20 MHz, standard VDD limits

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local Compuserve number.

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

PIC16C64

40-Pin EPROM-Based 8-Bit CMOS Microcontroller

FEATURES

High-performance RISC-like CPU

- Only 35 single word instructions to learn
- All single cycle instructions (200ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200ns instruction cycle
- 14-bit wide instructions and 8-bit wide data path
- 2048 x 14 on-chip EPROM program memory
- 128 x 8 general purpose registers (SRAM)
- Interrupt capability
- 33 special function hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes

Peripheral Features

- 33 I/O pins with individual direction control
- High current sink/source for direct LED drive
- One pin that can be configured as capture input, PWM output, or compare output
  - Capture is 16-bit, max resolution 200ns
  - Compare is 16-bit, max resolution 200ns
  - PWM resolution is 1- to 10-bit. 8-bit resolution gives 80 KHz maximum frequency and 10-bit resolution gives 20 KHz maximum frequency
- TMR1: 16-bit timer/counter (time-base for capture/compare)
- TMR2: 8-bit timer/counter with 8-bit period register (time-base for PWM), prescaler and postscaler
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler
- Parallel Slave Port (PSP): 8-bit wide, with external RD, WR and CS controls (microprocessor bus interface)
- Synchronous serial port (SSP) with two modes of operation:
  - 3-wire SPI
  - I²C™/ACCESS.bus™ compatible

Special Microcontroller Features

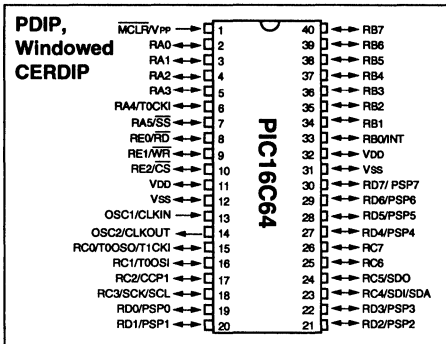
- Power-On Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security EPROM fuses for code-protection
- Power saving SLEEP mode
- EPROM fuse selectable oscillator options: (RC oscillator, Standard crystal/resonator, High-speed crystal/resonator, Low frequency crystal)
- Serial in-system programming (via two pins)

CMOS Technology

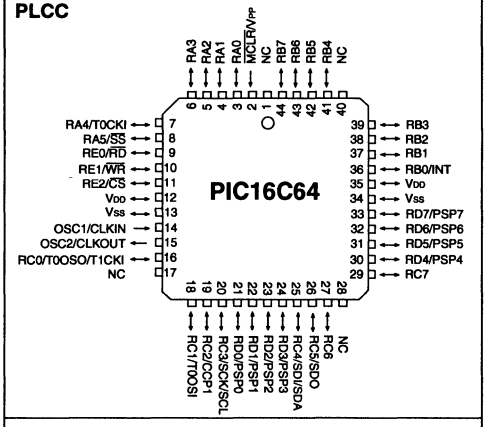
- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide-operating voltage range (2.5V to 6.0V)
- Commercial, Industrial, and Automotive Temp. Range
- Low-power consumption
  - < 2mA @ 5V, 4 MHz
  - 15μA typical @ 3V, 32 KHz
  - < 1μA typical standby current

PACKAGE TYPES

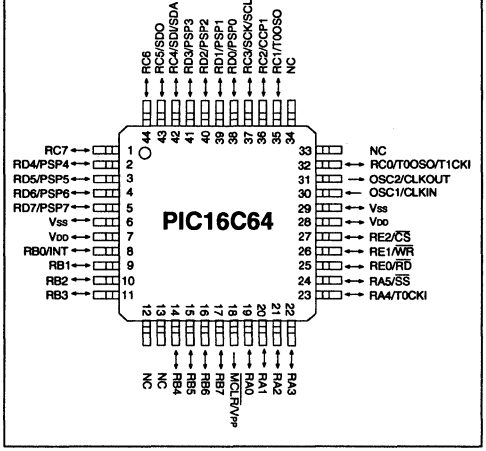
PDIP, Windowed CERDIP



PLCC



PQFP



1.0 GENERAL DESCRIPTION

The PIC16C64 is the first 4- pin member of the versatile PIC16CXX family of low-cost, high-performance, CMOS, fully static, EPROM-based 8-bit microcontrollers.

All PIC16CXX microcontrollers employ an advanced RISC-like architecture. The PIC16CXX has enhanced core features, 8-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance. PIC16CXX microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in its class.

The PIC16C64 has 128 bytes of RAM and 33 I/O pins. In addition, the PIC16C64 adds several peripheral features useful in many high performance applications including; three timer/counters, capture, compare, PWM features and serial ports. The synchronous serial port can be configured as either a 3-wire SPI or I^2C. An 8-bit Parallel slave port is also provided.

The PIC16C64 has special features which reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High-Speed crystals. The SLEEP (power- down) mode offers power saving. The user can wake up the chip from SLEEP through several external and internal interrupts and reset.

A highly reliable watchdog timer with its own on-chip RC oscillator provides protection against software malfunction.

A UV-erasable cerdip-packaged version is ideal for code development while the cost-effective One Time Programmable (OTP) version is suitable for production in any volume.

Table 1-1 shows the features of the PIC16C64 as well as the other members of the PIC16CXX enhanced core family.

A simplified block diagram of the PIC16C64 is shown in Figure 3-1.

The PIC16C64 fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote sensors, keyboards and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages for through hole or surface mounting make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16C64 very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of modifications. Code written for PIC16C5X can be easily ported to PIC16CXX family of devices (see Appendix B).

1.2 Development Support

The PIC16CXX family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a production quality programmer. A "C" compiler and fuzzy logic support tools are in development.

TABLE 1-1: PIC16CXX FAMILY OF DEVICES

		PIC16C74†	PIC16C64	PIC16C71†	PIC16C84†
Maximum Frequency of Operation		20 MHz	20 MHz	16 MHz	10 MHz
Program Memory (14-bit wide)	EPROM	4K	2K	1K	-
	EEPROM	-	-	-	1K
Data Memory (bytes)		192	128	36	36
Data EEPROM (bytes)		-	-	-	64
Timer 0 (8-bit + 8-bit prescaler)		Yes	Yes	Yes	Yes
Timer 1 (16-bit)		Yes	Yes	-	-
Timer 2 (8-bit)		Yes	Yes	-	-
Capture/Compare/PWM Module(s)		2	1	-	-
Synchronous Serial Port (SPI/I²C)		Yes	Yes	-	-
Serial Communications Interface (USART)		Yes	-	-	-
Parallel Slave Port		Yes	Yes	-	
Analog to Digital Converter (8-bit)		8 ch.	-	4 ch.	-
Power On Reset		Yes	Yes	Yes	Yes
Watchdog Timer		Yes	Yes	Yes	Yes
External Interrupts		Yes	Yes	Yes	Yes
Interrupt Sources		12	8	4	4
Program Memory Code Protect		Yes	Yes	Yes	Yes
I/O		33	33	13	13
I/O High Current Capability	Source	25mA	25mA	20mA	20mA
	Sink	25mA	25mA	25mA	25mA
Package Types		40-pin DIP, 44-pin PLCC, 44-pin PQFP	40-pin DIP, 44-pin PLCC, 44-pin PQFP	18-pin DIP 18-pin SOIC	18-pin DIP 18-pin SOIC

† For information on these devices please refer to their respective data sheets.

2.0 PIC16C64 DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information and tables in this section. When placing orders, please use the "PIC16C64 Product Identification System" on the back page of this data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in cerdip package is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the oscillator modes etc. Microchip's PICSTART™ and PRO MATE™ programmers supports programming of the PIC16C64.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages permit the user to program them once. In addition to the program memory, the configuration fuses must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTP) Devices

Microchip offers the unique programming service where a few user defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories. This improves bandwidth over traditional Von-Neuman architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. Instruction opcodes are 14-bit wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (see Figure 3-1). Consequently, all instructions (35) execute in a single cycle (200ns @ 20 MHz) except for program branches.

The PIC16C64 addresses 2K x 14 program memory space, all on-chip. Program execution in microcontroller mode is internal only.

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16CXX has a fairly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16CXX device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

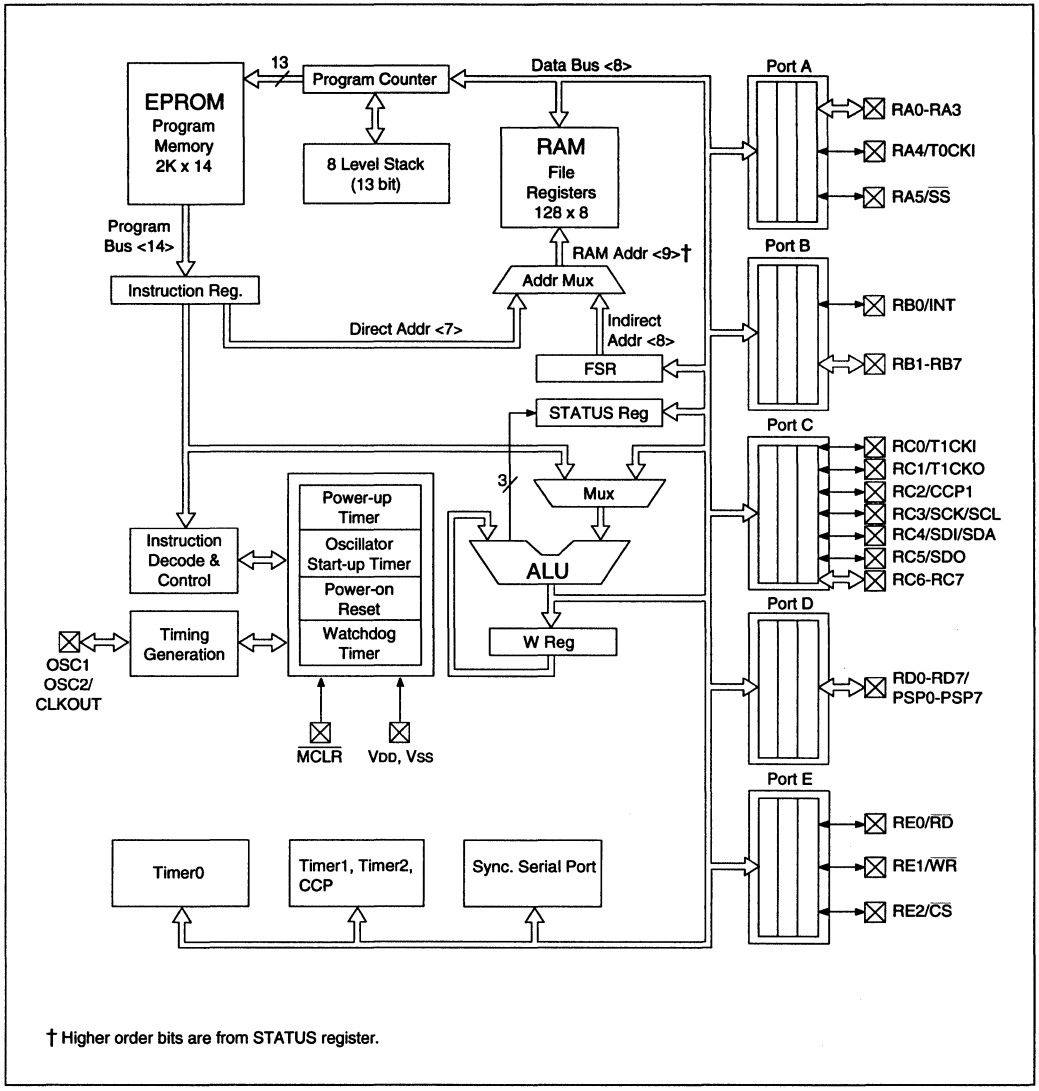
The ALU is 8-bit wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow out bit in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with a description of the device pins in Table 3-1.

FIGURE 3-1: PIC16C64 BLOCK DIAGRAM



† Higher order bits are from STATUS register.

TABLE 3-1: PIC16C64 PINOUT DESCRIPTION

Pin Name	DIP No.	PLCC No.	PQFP No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	CMOS	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	2	18	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
						PORTA is a bidirectional I/O port.
RA0	2	3	19	I/O	TTL	
RA1	3	4	20	I/O	TTL	
RA2	4	5	21	I/O	TTL	
RA3	5	6	22	I/O	TTL	
RA4/T0CKI	6	7	23	I/O	ST	Can also be selected to be the clock input to the TMR0 timer/counter. Output is open collector type.
RA5/$\overline{SS}$	7	8	24	I/O	TTL	Can also be the slave select for the synchronous serial port.
						PORTB is a bidirectional I/O port. Port B can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST†	RB0/INT can also be selected as an external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3	36	39	11	I/O	TTL	
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6	39	43	16	I/O	TTL/ST‡	Interrupt on change pin. Serial programming clock.
RB7	40	44	17	I/O	TTL/ST‡	Interrupt on change pin. Serial programming data.
						PORTC is a bidirectional I/O port.
RC0/T0OSO /T1CKI	15	16	32	I/O	ST	RC0/T1CKI can also be selected as a Timer1 clock/ oscillator input.
RC1/T0OSI	16	18	35	I/O	ST	RC1/T1CKO can also be selected as a Timer1 oscillator output.
RC2/CCP1	17	19	36	I/O	ST	RC2/CCP1 can also be selected as a capture1 input/ compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock for both SPI and I²C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I²C mode).
RC5/SDO	24	26	43	I/O	ST	RC5/SDO can also be selected as the SPI Data Out (SPI mode).
RC6	25	27	44	I/O	ST	
RC7	26	29	1	I/O	ST	

Legend: I = input, O = output, I/O = input/output, P = power; (Cont.)
— = Not used, TTL = TTL input, ST = Schmitt trigger input

† This buffer is a Schmitt triger input when configured as the external interrupt.

‡ This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 3-1: PIC16C64 PINOUT DESCRIPTION (CONT.)

Name	Pin DIP No.	PLCC No.	PQFP No.	I/O/P Type	Buffer Type	Description
						PORTD is a bidirectional I/O port or parallel slave port for interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL§	
RD1/PSP1	20	22	39	I/O	ST/TTL§	
RD2/PSP2	21	23	40	I/O	ST/TTL§	
RD3/PSP3	22	24	41	I/O	ST/TTL§	
RD4/PSP4	27	30	2	I/O	ST/TTL§	
RD5/PSP5	28	31	3	I/O	ST/TTL§	
RD6/PSP6	29	32	4	I/O	ST/TTL§	
RD7/PSP7	30	33	5	I/O	ST/TTL§	
RE0/$\overline{RD}$	8	9	25	I/O	ST/TTL§	Bidirectional I/O pin or read control for parallel slave port.
RE1/$\overline{WR}$	9	10	26	I/O	ST/TTL§	Bidirectional I/O pin or write control for parallel slave port.
RE2/$\overline{CS}$	10	11	27	I/O	ST/TTL§	Bidirectional I/O pin or select control for parallel slave port.
VSS	12,31	13,34	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17 28,40	12,13 33,34		—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input, O = output, I/O = input/output, P = power;
— = Not used, TTL = TTL input, ST = Schmitt trigger input

§ This buffer is a Schmitt trigger input when configured as general purpose I/O and a TTL input when used in the parallel slave port mode (for interfacing to a microprocessor bus).

3.1 Clocking Scheme/Instruction Cycle

The clock input (from pin OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

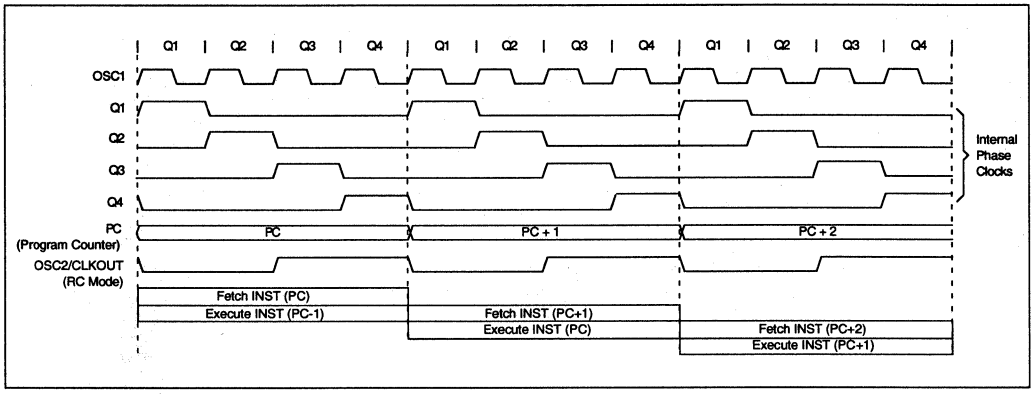
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction (see Example 3-1).

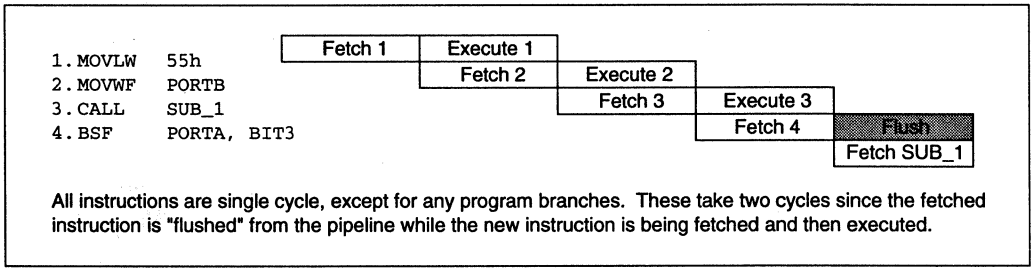
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



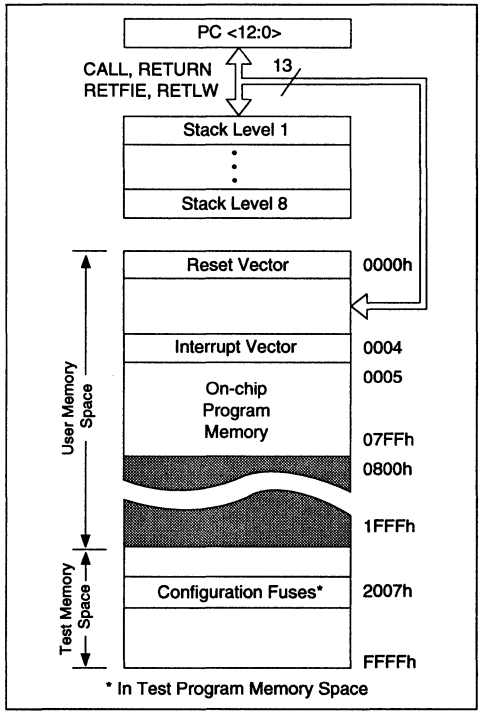
All instructions are single cycle, except for any program branches. These take two cycles since the fetched instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

4.0 MEMORY ORGANIZATION

4.1 Program Memory Organization

The PIC16C64 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 2K x 14 (0000h - 07FFh) are physically implemented. Accessing a location above 7FFh will cause a wrap-around within the first 2K x 14 space. The reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 4-1).

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

The data memory (see Figure 4-2) is composed of the general purpose register file and the special registers. The data memory extends up to 7Fh. The first 32 locations are used to map special function registers. Locations 20h - 7Fh (Bank 0) and A0h-BFh (Bank 1) are general purpose registers implemented as static RAM. There are two register file page select bits in the STATUS register allowing selection from up to four Banks. Some special function registers are mapped in Bank 1.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file, in PIC16C64 is organized as 128 x 8. It is accessed either directly or indirectly through the file select register FSR.

FIGURE 4-2: REGISTER FILE MAP

File address	Bank 0	Bank 1	
00	Indirect addr.(*)	Indirect addr.(*)	80
01	TMR0	OPTION	81
02	PCL	PCL	82
03	STATUS	STATUS	83
04	FSR	FSR	84
05	PORT A	TRIS A	85
06	PORT B	TRIS B	86
07	PORT C	TRIS C	87
08	PORT D	TRIS D	88
09	PORT E	TRIS E	89
0A	PCLATH	PCLATH	8A
0B	INTCON	INTCON	8B
0C	PIR1	PIE1	8C
0D			8D
0E	TMR1L	PCON	8E
0F	TMR1H		8F
10	T1CON		90
11	TMR2		91
12	T2CON	PR2	92
13	SSPBUF	SSPADD	93
14	SSPCON	SSPSTAT	94
15	CCPR1L		95
16	CCPR1H		96
17	CCP1CON		97
18			98
19			99
1A			9A
1B			9B
1C			9C
1D			9D
1E			9E
1F			9F
20	General Purpose Register	General Purpose Register	A0
			BF
			C0
7F			FF

* Not a physical register

Unimplemented data memory locations; read as '0's

4.2.2 SPECIAL FUNCTION REGISTERS:

The special function registers are registers used by the CPU and Peripheral functions for controlling the desired operation of the device (see Table 4-1). These registers are static RAM.

The special registers can be classified into two sets. The special registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16C64

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0									
00†	INDF (Indirect Address)	Addressing this location uses contents of FSR to address data memory (not a physical register)							
01	TMR0	Timer0							
02†	PCL	Program Counter's (PC's) Least Significant Byte							
03†	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
04†	FSR	Indirect data memory address pointer							
05	PORTA	PortA Data Latch where written to PortA pins when read							
06	PORTB	PortB Data Latch where written to PortB pins when read							
07	PORTC	PortC Data Latch where written to PortC pins when read							
08	PORTD	PortD Data Latch where written to PortD pins when read							
09	PORTE	PortE Data Latch where written to PortE pins when read							
0A†	PCLATH	Buffered Register for the upper 5 bits of the Program Counter (PC)							
0B†	INTCON	GIE	PEIE	RTIE	INTE	RBIE	RTIF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
0D	Reserved								
0E	TMR1L	Timer1 Least Significant Byte							
0F	TMR1H	Timer1 Most Significant Byte							
10	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1INSYNC	TMR1CS	TMR1ON
11	TMR2	Timer2							
12	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
13	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register							
14	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
15	CCPR1L	Capture/Compare/Duty Cycle Register (LSB)							
16	CCPR1H	Capture/Compare/Duty Cycle Register (MSB)							
17	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0
Bank 1									
80†	INDF (Indirect Address)	Addressing this location uses contents of FSR to address data memory (not a physical register)							
81	OPTION	$\overline{RBPU}$	INTEDG	RTS	RTE	PSA	PS2	PS1	PS0
82†	PCL	Program Counter's (PC's) Least Significant Byte							
83†	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
84†	FSR	Indirect data memory address pointer							
85	TRISA	PortA Data Direction Register							
86	TRISB	PortB Data Direction Register							
87	TRISC	PortC Data Direction Register							
88	TRISD	PortD Data Direction Register							
89	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0
8A†	PCLATH	Shadow Register for the upper 5 bits of the Program Counter (PC)							
8B†	INTCON	GIE	PEIE	RTIE	INTE	RBIE	RTIF	INTF	RBIF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
8D	Reserved								
8E	PCON	—	—	—	—	—	—	$\overline{POR}$	—
8F	Reserved								
90	Reserved								
91	Reserved								
92	PR2	Timer2 Period Register							
93	SSPADD	Synchronous Serial Port (I^2C mode) Address Register							
94	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
95	Reserved								
96	Reserved								
97	Reserved								

Legend — = Unimplemented locations, Read as '0'
† These registers can be addressed from either bank.

4.2.2.1 **STATUS** Register

The STATUS register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for data memory.

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the logic.

Furthermore, $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the status register as 000UU1UU (where U = unchanged).

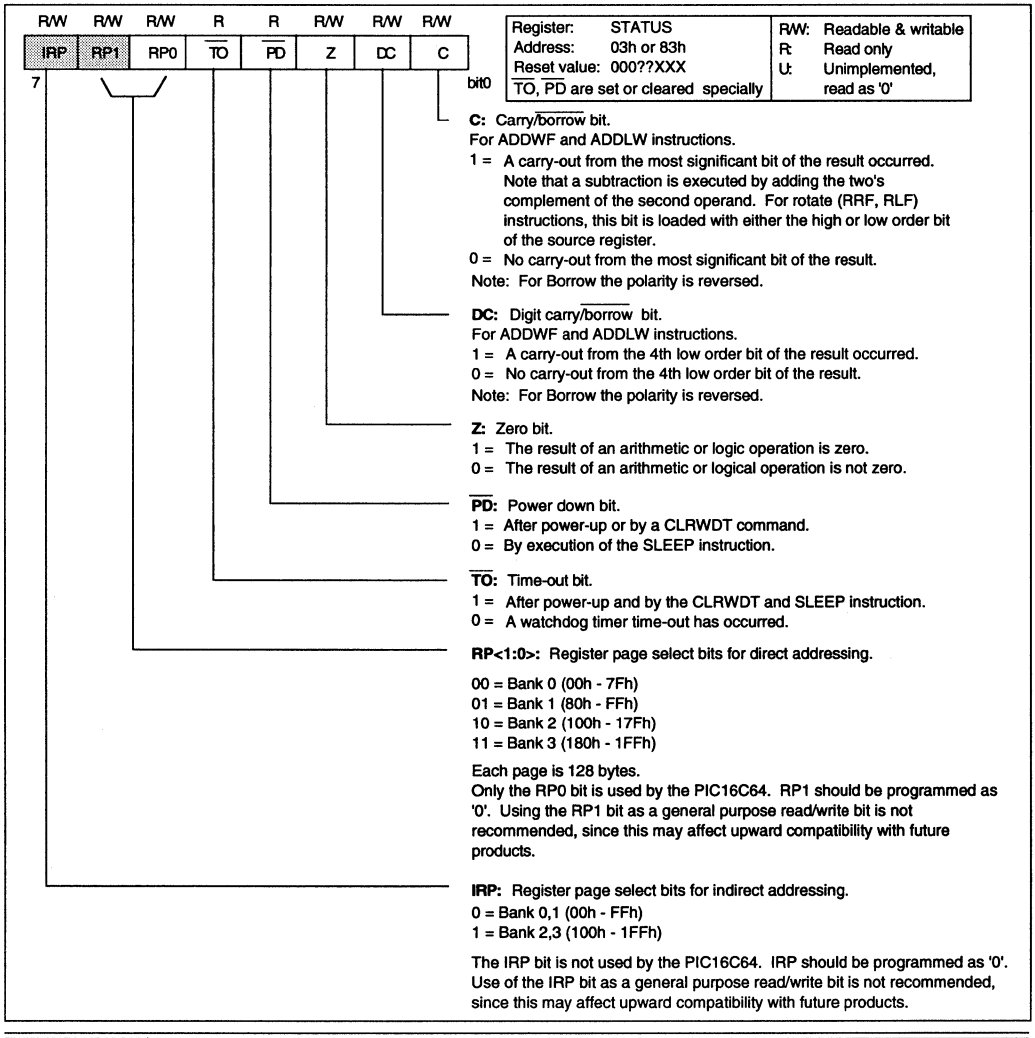
It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions are used to alter the status registers because these instructions do not affect any status bit. For other instructions, affecting any status bits, see the "Instruction Set Summary".

Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16C64 and should be programmed as '0'. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

Note 2: The C and DC bits operate as a $\overline{borrow}$ out bit in subtraction. See the SUBLW and SUBWF instructions for examples.

2

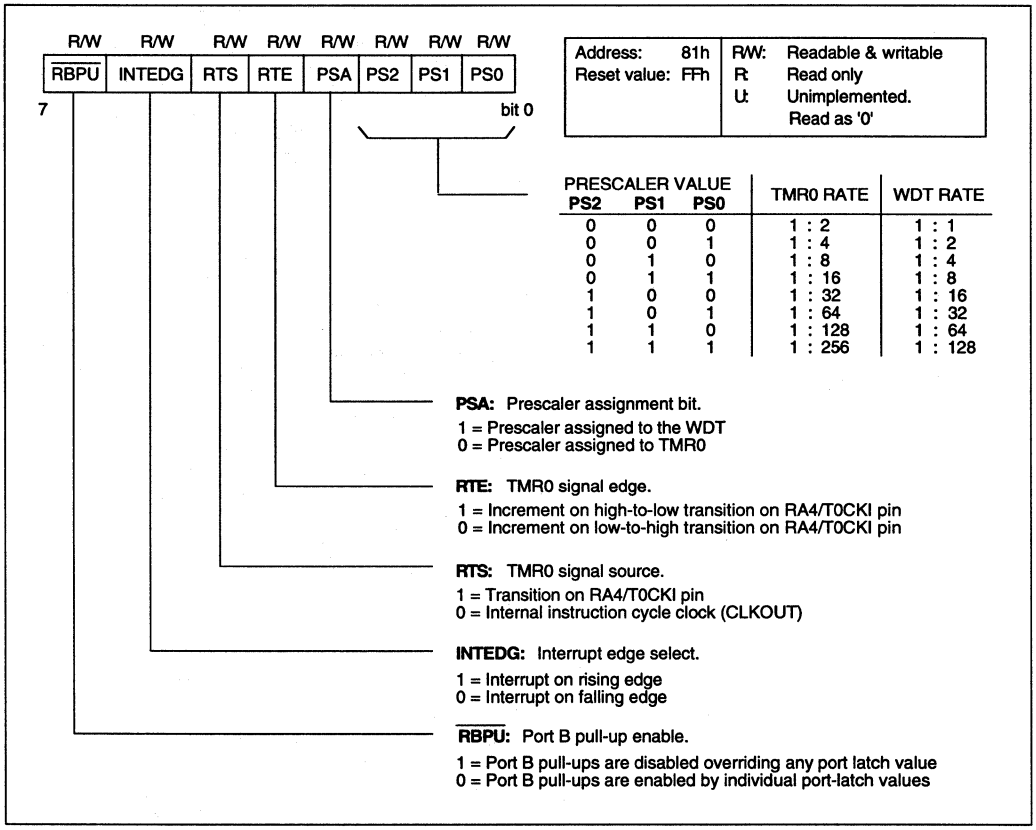
FIGURE 4-3: STATUS REGISTER



4.2.2.2 **OPTION** Register

The OPTION register (address 81h) is a readable and writable register which contains various control bits to configure the prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

FIGURE 4-4: OPTION REGISTER



4.2.2.3 **INTCON** Register

The PIC16C64 has eight sources of interrupt:

- External interrupt from RB0/INT pin
- Timer0 overflow
- Interrupt on change on RB<7:4> pins
- Timer1 overflow
- Timer2 matches period register
- A capture, a compare, or a PWM output is reset
- The synchronous serial port
- The parallel slave port read/write

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global enable bits. The peripheral interrupt flags reside in the PIR1 register (Addr 0Ch).

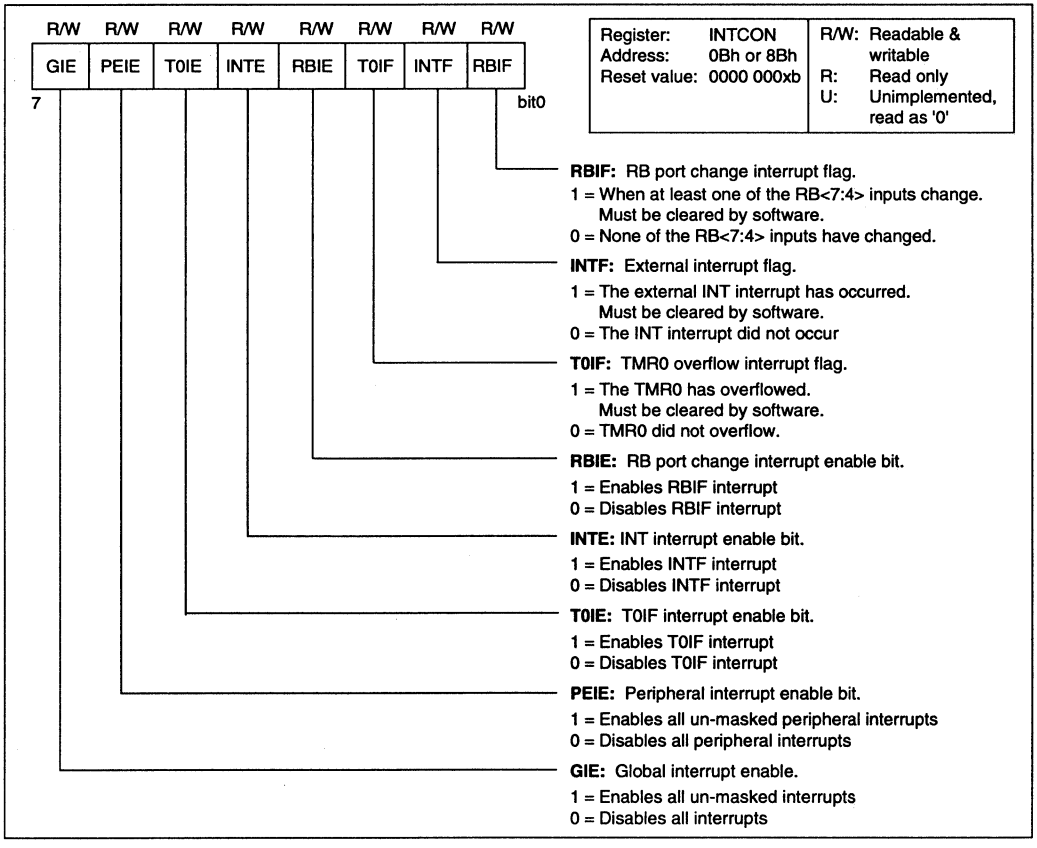
A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding mask bit in INTCON register (Figure 4-5). GIE is cleared on reset.

When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be 3-4 instruction cycles. The exact latency depends when the interrupt event occurs (see Figure 12-15). The latency is the same for 1 or 2 cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

The "return from interrupt" instruction, RETFIE, exits interrupt routine as well as sets the GIE bit to re-enable interrupts.

Note: The T0IF, INTF, or RBIF will be set by the specified condition even if the corresponding Interrupt Enable Bit is cleared (interrupt disabled) or the GIE bit is cleared (all interrupts disabled).

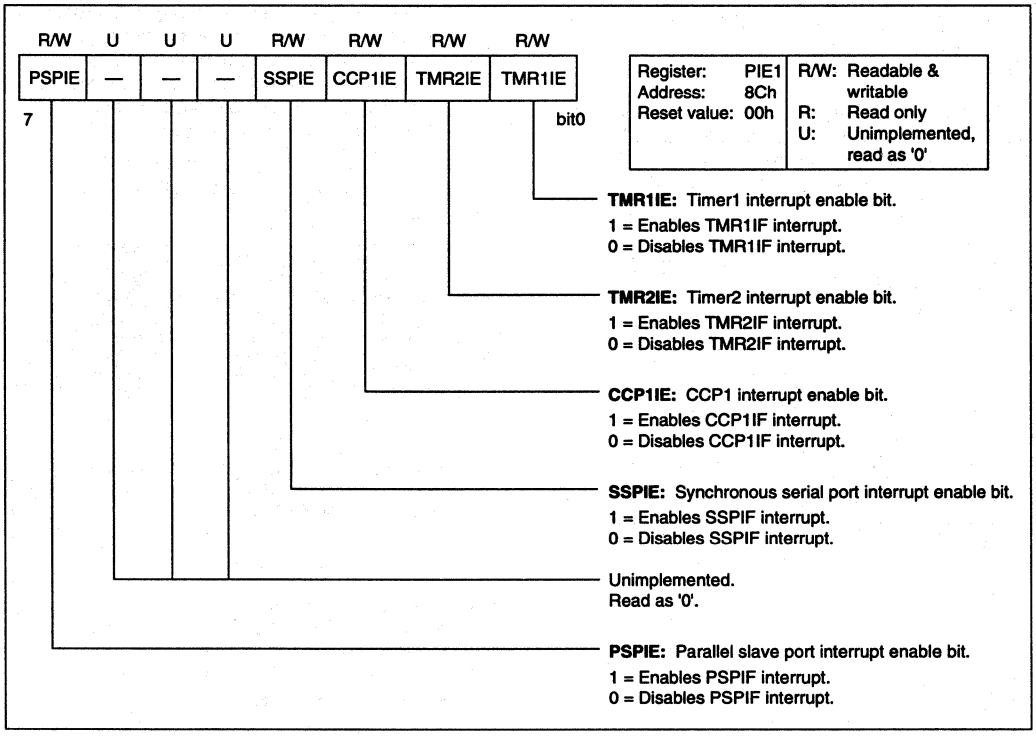
FIGURE 4-5: INTCON REGISTER



4.2.2.4 PIE1 Register

This register contains the individual enable bits for the Peripheral Interrupts.

FIGURE 4-6: PIE1 REGISTER

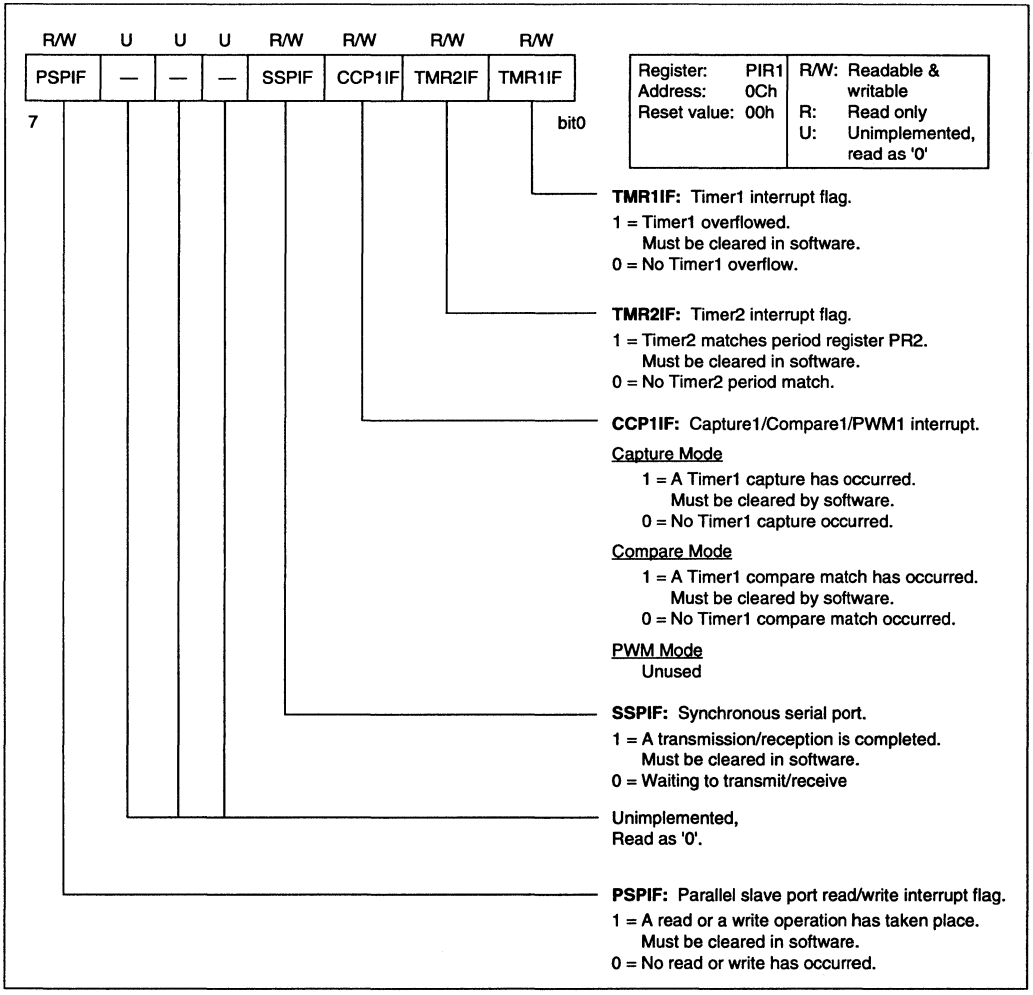


4.2.2.5 **PIR1** Register

This register contains the individual flag bit for the Peripheral Interrupts.

Note: These bits will be set by the specified condition, even if the corresponding Interrupt Enable bit is cleared (interrupt disabled) or the GIE bit is cleared (all interrupts disabled). Before enabling an Interrupt, the user may wish to clear the interrupt flag, to ensure that the program does not immediately branch to the Peripheral Interrupt service routine.

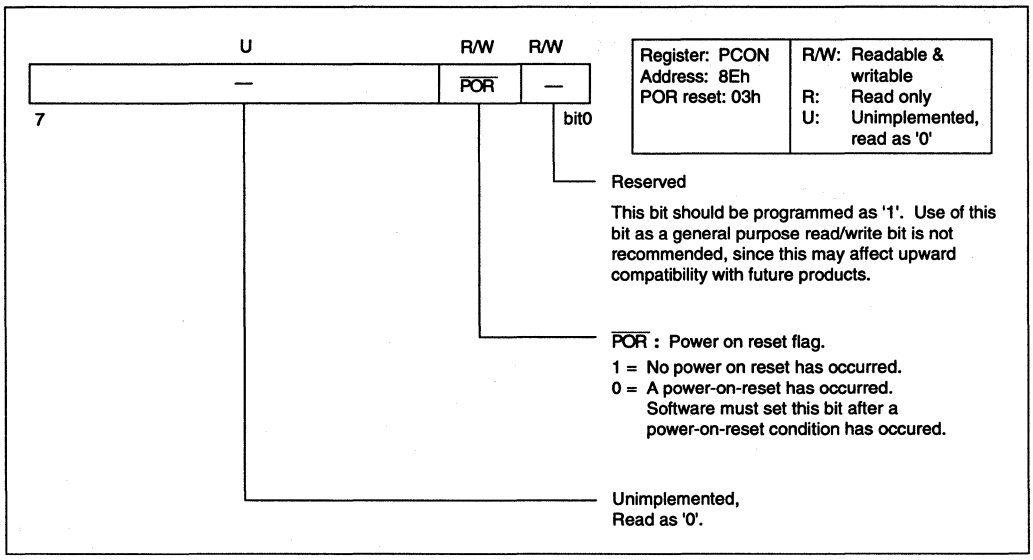
FIGURE 4-7: PIR1 REGISTER



4.2.2.6 **PCON** Register

The PCON register contains flag bits to allow differentiation between a Power-On Reset to an external $\overline{MCLR}$ reset, WDT reset.

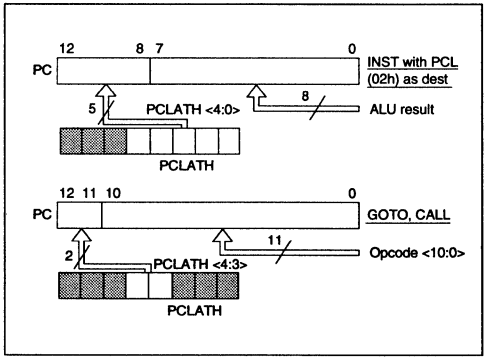
FIGURE 4-8: PCON REGISTER



4.3 PCL and PCLATH

The program counter (PC) is 13-bit wide. The low byte, PCL is a readable and writable register (02h or 82h). The high byte of the PC, PCH is not directly readable or writable. The high byte of the PC can be written through the PCLATH register (0Ah or 8Ah). When the PC is loaded with a new value during a CALL, GOTO or a write to PCL, the high bits of PC are loaded from PCLATH, as shown in Figure 4-9.

FIGURE 4-9: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to "Table Read Using the PIC16CXX" (AN556).

4.3.2 Stack

The PIC16CXX has an 8-deep x 13-bit wide hardware stack (see Figure 4-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is pushed in the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is popped in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a "PUSH" or a "POP" operation.

The stack operates as a circular buffer. This means that after the stack has been "PUSHed" eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on). This means that the user can implement "software resets" for the system.

Note: There are no STATUS bits to indicate stack overflows or stack underflow conditions.

4.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause an indirect addressing.

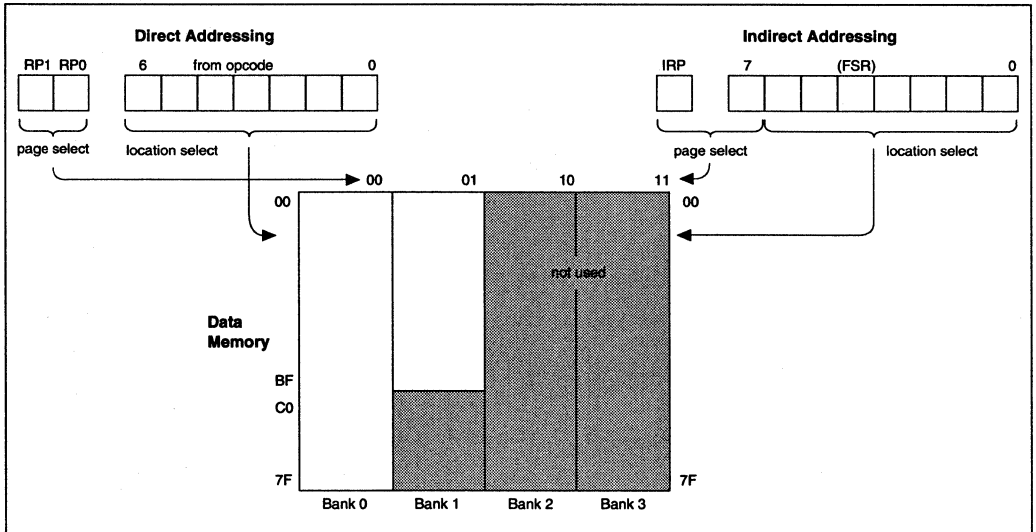
Indirect addressing is possible by using file address 00h. Any instruction using the INDF register, actually accesses data pointed to by the file select register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concantenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-10. However, IRP is not used in the PIC16C64.

A simple program to clear RAM location20h-2Fh using indirect addressing is shown in Example 4-1.

EXAMPLE 4-1: INDIRECT ADDRESSING

```
        movlw   0x20    ;initialize pointer
        movwf   FSR     ;to RAM
NEXT    clrf    INDF    ;clear indent by
        incrf   FSR     ;inc pointer
        btfss   FSR,4   ;all done?
        goto    NEXT    ;no clear next
CONTINUE:               ;yes continue
```

FIGURE 4-10: DIRECT/INDIRECT ADDRESSING



Note: For memory map detail, see Figure 4.2

5.0 I/O PORTS

The PIC16C64 has five ports, PORTA through PORTE. These ports pins may be multiplexed with an alternate function for the peripheral features on the device.

5.1 PORTA and TRISA Registers

PORTA is a 6-bit wide latch. RA4 is a Schmitt trigger input and an open collector output. All other RA port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as output or input.

A '1' in the TRISA register configures the corresponding port pin as input.

Port RA4 is multiplexed with TMR0 clock input.

Reading PORTA register reads the status of the pins, whereas writing to it will write to the port latch.

EXAMPLE 5-1: INITIALIZING PORTA

```
BSF     STATUS, RP0 ;Select Bank1
MOVLW   0xCF        ;Value used to initialize
                    ;data direction
MOVWF   TRISA       ;Set RA<3:0> as inputs
                    ;    RA<5:4> as outputs
                    ;TRISA<7:6> are always
                    ;read as '0'.
```

2

FIGURE 5-1: BLOCK DIAGRAM OF PORT PINS RA<3:0> and RA<5>

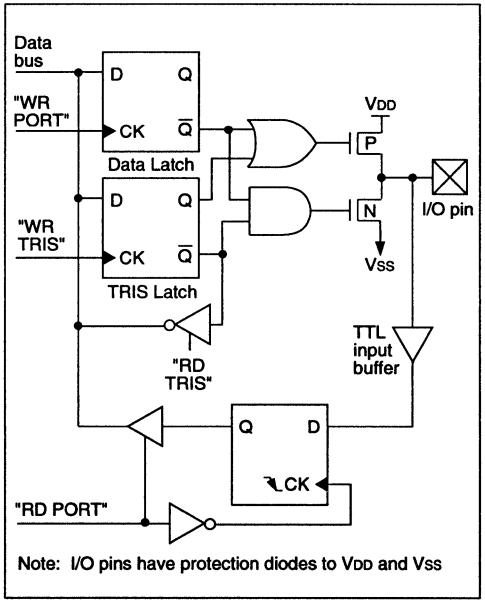


FIGURE 5-2: BLOCK DIAGRAM OF RA4 PIN

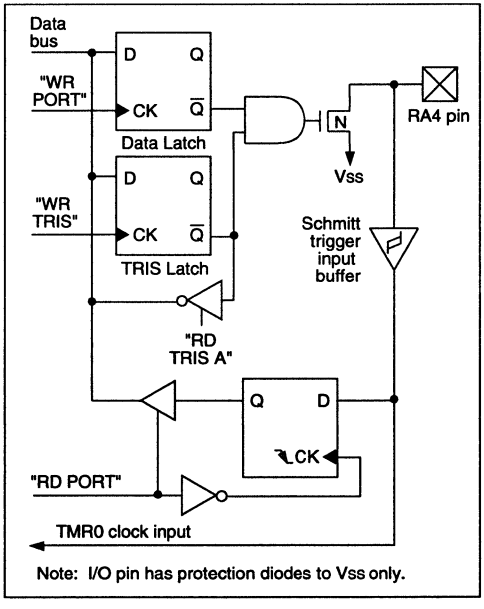


TABLE 5-1: PORTA FUNCTIONS

Name	Bit	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open collector type
RA5/$\overline{SS}$	bit5	TTL	Input/output or slave select input for synchronous serial port

Legend: TTL = TTL input, ST = Schmitt trigger input

TABLE 5-2: SUMMARY OF PORTA REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTA	PORTA pins when read PORTA latch when written	05h	--xx xxxx
TRISA	PORTA data direction register 0 = output, 1 = input	85h	--11 1111

Notes: 1: x = unknown, - = unimplemented, reads as a '0'.
2: For reset values of registers in other reset situations refer to Table 12-6.

5.2 PORTB and TRISB Registers

PORTB is an 8-bit wide bidirectional port (file register address 06h). The corresponding data direction register is TRISB (address 86h). A '1' in TRISB configures the corresponding port pin as an input. Reading PORTB register reads the status of the pins whereas writing to it will write to the port latch.

Each of the PORTB pins has a weak internal pull-up (~100 µA typical). A single control bit can turn on all the pull-ups. This is done by clearing the $\overline{\text{RBPU}}$ (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on power-on reset.

Four of PORTB's pins, RB<7:4>, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7–RB4 pin configured as an output is excluded from the interrupt on change comparison). On every instruction cycle, the input pins (of RB7–RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7–RB4 are OR'ed together to generate the RBIF interrupt (flag latched in INTCON<0>).

This interrupt can wake the device up from SLEEP. The user, in the interrupt service routine, can clear the interrupt in one of two ways:

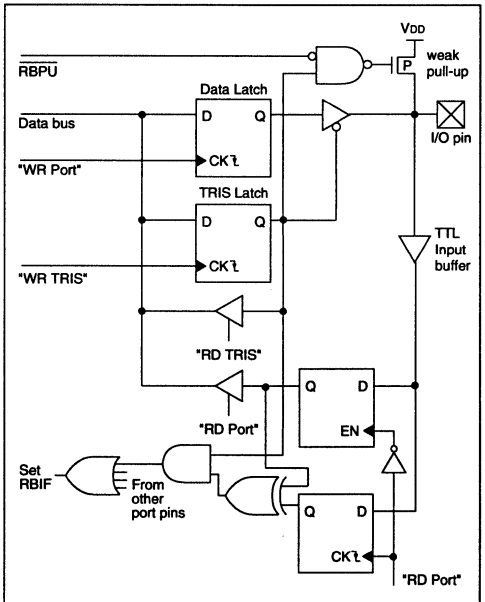
a) Disable the interrupt by clearing RBIE (INTCON<3>) bit.
b) Read PORTB. This will end mismatch condition. Then, clear RBIF bit.

A mismatch condition will continue to set the RBIF bit. Reading PORTB will end the mismatch condition, and allow the RBIF bit to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression. (See AN552 in the *Embedded Control Handbook*).

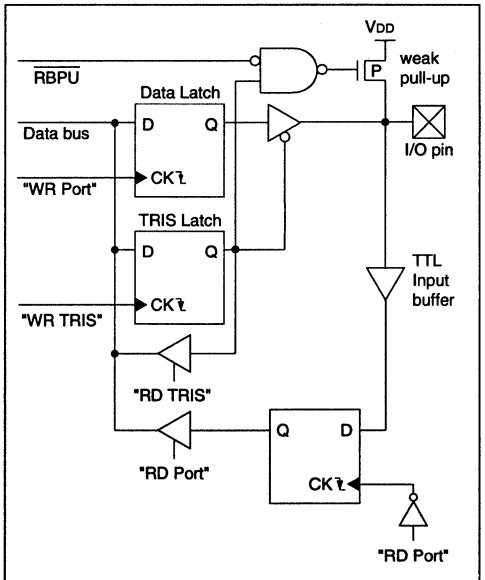
Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not be set.

FIGURE 5-3: BLOCK DIAGRAM OF PORT PINS RB<7:4>



Note: 1. Port latch = 1 and TRISB = 1 enables weak pull-up if $\overline{\text{RBPU}}$ = 0 in OPTION register.
2. I/O pins have diode protection to VDD and Vss.

FIGURE 5-4: BLOCK DIAGRAM OF PORT PINS RB<3:0>



Notes: 1. TRISB = 1 enables weak pull-up if RBPU = 0 in OPTION register.
2. For RB0/INT pin, the INT input comes through a Schmitt trigger input buffer.
3. I/O pins have diode protection to VDD and Vss.

TABLE 5-3: PORTB FUNCTIONS

Name	Bit	Buffer Type	Function
RB0/INT	bit0	TTL/ST†	Input/output pin or external interrupt input. Internal software programmable weak pull-up
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up
RB6	bit6	TTL/ST‡	Input/output pin (with interrupt on change). Internal software programmable weak pull-up
RB7	bit7	TTL/ST‡	Input/output pin (with interrupt on change). Internal software programmable weak pull-up

Legend: TTL = TTL input, ST = Schmitt Trigger
† This buffer is a Schmitt triger input when configured as the external interrupt.
‡ This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 5-4: SUMMARY OF PORTB REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTB	PORTB pins when read PORTB latch when written	06h	xxxx xxxx
TRISB	PORTB data direction register 0 = output, 1 = input	86h	1111 1111
$\overline{\text{OPTION}}$	Weak pull-up on/off control ($\overline{\text{RBPU}}$ bit)	81h	1111 1111

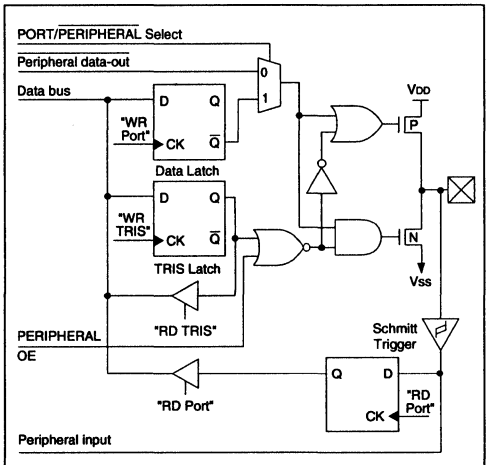
5.3 PORTC and TRISC Registers

I/O PORTC is an 8-bit bidirectional port. Each pin is individually configurable as input and output through the TRISC register. PORTC is multiplexed with several peripheral functions (see Table 5-5). PORTC pins have Schmitt trigger input buffers.

EXAMPLE 5-2: INITIALIZING PORTC

```
BSF     STATUS, RP0 ;Select Bank1
MOVLW   0xCF        ;Value used to initialize
                    ;data direction
MOVWF   TRISC       ;Set RC<3:0> as inputs
                    ;    RC<5:4> as outputs
                    ;    RC<7:6> as inputs
```

FIGURE 5-5: PORTC BLOCK DIAGRAM



Notes: 1. Port/Peripheral select signal selects between port data and peripheral output.
2. Peripheral OE (output enable) is only activated if peripheral select is active.
3. I/O pins have diode protection to VDD and Vss.

TABLE 5-5: PORTC FUNCTIONS

Name	Bit	Buffer Type	Function
RC0/T1CKI	bit0	ST	Input/output port pin or Timer1 clock input/Timer1 oscillator input
RC1/T1CKO	bit1	ST	Input/output port pin or Timer1 oscillator output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/ PWM1 output
RC3/SCK/SCL	bit3	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock for both SPI and I²C modes.
RC4/SDI/SDA	bit4	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I²C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous serial port data output
RC6	bit6	ST	Input/output port pin
RC7	bit7	ST	Input/output port pin

Legend: ST = Schmitt Trigger Input

TABLE 5-6: SUMMARY OF PORTC REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTC	PORTC pins when read PORTC latch when written	07h	XXXX XXXX
TRISC	PORTC data direction register 0 = output, 1 = input	87h	1111 1111

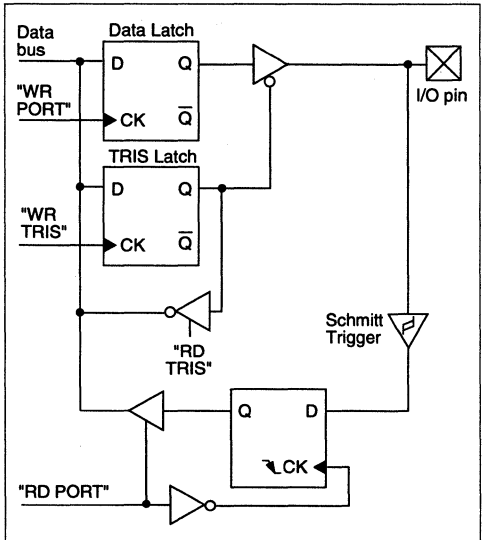
Notes: 1: x = unknown, - = unimplemented, reads as a '0'.
2: For reset values of registers in other reset situations refer to Table.

5.4 PORTD and TRISD Registers

I/O PORTD is an 8-bit port with Schmitt trigger input buffers. Each pin is individually configurable as input or output.

PORTD can be configured as an 8-bit wide microprocessor port (or parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

FIGURE 5-6: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)



Note: I/O pins have protection diodes to VDD and VSS.

TABLE 5-7: PORTD FUNCTIONS

Name	Bit	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL	Input/output port pin or parallel slave port bit 0
RD1/PSP1	bit1	ST/TTL	Input/output port pin or parallel slave port bit 1
RD2/PSP2	bit2	ST/TTL	Input/output port pin or parallel slave port bit 2
RD3/PSP3	bit3	ST/TTL	Input/output port pin or parallel slave port bit 3
RD4/PSP4	bit4	ST/TTL	Input/output port pin or parallel slave port bit 4
RD5/PSP5	bit5	ST/TTL	Input/output port pin or parallel slave port bit 5
RD6/PSP6	bit6	ST/TTL	Input/output port pin or parallel slave port bit 6
RD7/PSP7	bit7	ST/TTL	Input/output port pin or parallel slave port bit 7

Legend: ST = Schmitt Trigger Input, TTL = TTL input

TABLE 5-8: SUMMARY OF PORTD REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTD	PORTD pins when read PORTD latch when written	08h	xxxx xxxx
TRISD	PORTD data direction register 0 = output, 1 = input	88h	1111 1111

Notes: 1: x = unknown, - = unimplemented, reads as a '0'.
2: For reset values of registers in other reset situations refer to Table.

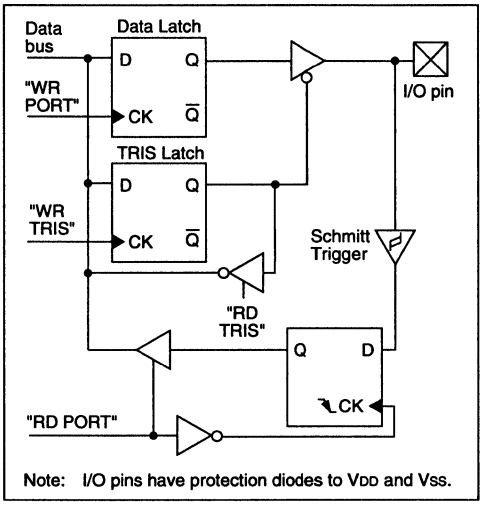
5.5 PORTE and TRISE Register

I/O PORTE has three pins RE0, RE1 and RE2 which are individually configurable as inputs or outputs. These have Schmitt trigger input buffers.

I/O PORTE becomes control inputs for the microprocessor port when the PSPMODE bit (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs). In this mode the input buffers are TTL.

Figure 5-7 shows the TRISE register, which also controls the synchronous slave port operation.

FIGURE 5-7: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)



Note: I/O pins have protection diodes to VDD and Vss.

FIGURE 5-8: TRISE REGISTER

R	R	R/W	R/W	U	R/W	R/W	R/W
IBF	OBF	IBOV	PSPMODE	-	TRISE2	TRISE1	TRISE0
							bit0

Register: TRISE	R/W: Readable & writable
Address: 89h	R: Read only
POR value: 07h	U: Unimplemented, read as '0'

TRISE0: Direction control bit for port pin RE0
1 = Input
0 = Output

TRISE1: Direction control bit for port pin RE1
1 = Input
0 = Output

TRISE2: Direction control bit for port pin RE2
1 = Input
0 = Output

Unimplemented.
Read as '0'

PSPMODE: Selects parallel slave port mode for ports RD and RE.
1 = Parallel slave port mode.
0 = General purpose I/O.

IBOV: Input buffer overflow in microprocessor mode.
1 = A write occurred when a previous input word has not been read.
Must be cleared in software.
0 = No overflow has occurred.

OBF: Output buffer full.
1 = The output buffer still holds a previously written word.
0 = Output buffer has been read.

IBF: Input buffer full.
1 = A word has been received and waiting to be read by the CPU.
0 = No word has been received.

TABLE 5-9: PORTE FUNCTIONS

Name	Bit	Buffer Type	Function
RE0/$\overline{RD}$	bit0	ST/TTL	Input/output port pin or Read control input in parallel slave port mode $\overline{RD}$ 1 = Not a read operation 0 = Read operation. The system reads the 16C64 PortD register (if chip selected)
RE1/$\overline{WR}$	bit1	ST/TTL	Input/output port pin or Write control input in parallel slave port mode $\overline{WR}$ 1 = Not a write operation 0 = Write operation. The system writes to the 16C64 PortD register (if chip selected)
RE2/$\overline{CS}$	bit2	ST/TTL	Input/output port pin or Chip select control input in parallel slave port mode $\overline{CS}$ 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger Input, TTL = TTL input

TABLE 5-10: SUMMARY OF PORTE REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTE	PORTE pins when read PORTE latch when written	09h	---- -XXX
TRISE	PORTE data direction control bits and PORTD mode control	89h	0000 -111

5.6 I/O Programming Considerations

5.6.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation, and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit 5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit 5 and PORTB is written to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (for example, bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

Reading the PORT register, reads the values of the PORT pins. Writing to the PORT register writes the value to the PORT latch. When using read modify write instructions (ex. BCF, BSF, etc.) on a PORT, the value of the PORT pins is read, the desired operation is done to this value, and this value is then written to the PORT latch.

Example 5-3 shows the effect of two sequential read modify write instructions (ex. BCF, BSF, etc.) on an I/O PORT.

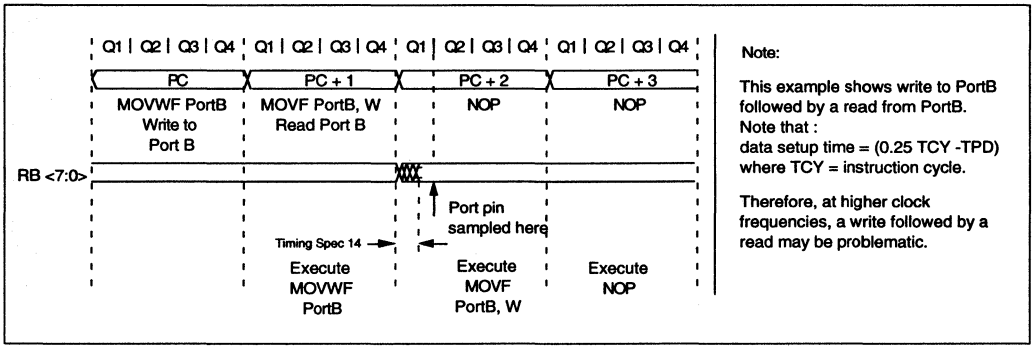
EXAMPLE 5-3: READ MODIFY WRITE INSTRUCTIONS ON AN I/O PORT

```
; Initial PORT settings:  PORTB<7:4> Inputs
;                         PORTB<3:0> Outputs
; PORTB<7:6> have external pull-up and are not
; connected to other circuitry.
;
;                           PORT latch   PORT pins
;                           ----------   ----------
      BCF     PORTB, 7    ; 01pp pppp    11pp pppp
      BCF     PORTB, 6    ; 10pp pppp    11pp pppp
      BSF     STATUS, RP0 ;
      BCF     TRISB, 7    ; 10pp pppp    11pp pppp
      BCF     TRISB, 6    ; 10pp pppp    10pp pppp
;
; Note that the user may have expected the pin
; values to be 00pp pppp. The 2nd BCF caused RB7
; to be latched as the pin value (High).
```

5.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see Figure 5-9). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

FIGURE 5-9: SUCCESSIVE I/O OPERATION



5.7 Parallel Slave Port

PORTD operates as an 8-bit wide parallel slave port, or microprocessor port when control bit PSPMODE (TRISE<4>) is set. In slave mode it is asynchronously readable and writable by the external world through RD control input (RE0/RD) and WR control input (RE1/WR).

It can directly interface to an 8-bit microprocessor data bus. The microprocessor can read or write the PORTD latch as an 8-bit latch. Setting PSPMODE also enables the port pin RE0 to be the RD input, RE1 to be the WR input and RE2 to be the CS (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set).

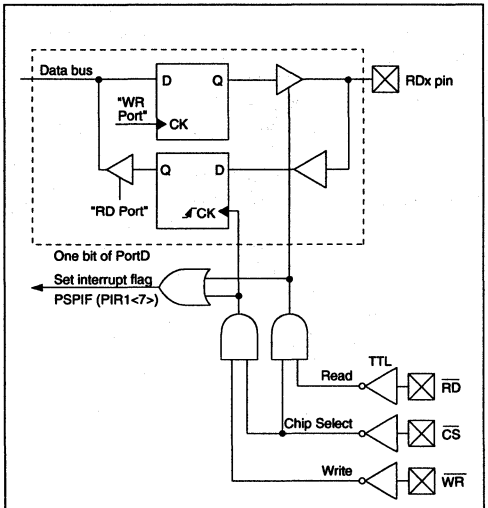
There are actually two 8-bit latches, one for data-out (from the PIC16CXX) and one for data input. The user writes 8-bit data to PORTD data latch and reads data from the port pin latch (note that they have the same address). In this mode the TRISD register is ignored, since the microprocessor is controlling the direction of data flow.

Status flag IBF, Input Buffer Full (TRISE<7>), is set if a received word is waiting to be read by the CPU. The IBF is cleared when PORTD is read by the CPU. IBF is a read only status bit. Status flag OBF, Output Buffer Full (TRISE<6>), is set if a word written to PORTD latch is waiting to be read by the external bus. The OBF flag is cleared when PORTD is read by the external device. Status flag IBOV, Input Buffer Overflow (TRISE<5>), is set if a second word is written to the microprocessor port when the previous word has not been read by the CPU. It is a read/write bit and must be cleared by the CPU.

When not in PSPMODE, IBF and OBF bits are held as cleared. However, if the IBOV flag was previously set, it must be cleared in the software.

An interrupt is generated and latched into control bit PSPIF (PIR1<7>) when a read or a write operation is completed. The PSPIF interrupt flag must be cleared by the CPU and the interrupt can be disabled by clearing the interrupt enable bit PSPIE (PIE1<7>).

FIGURE 5-10: PORTD AND PORTE AS A PARALLEL SLAVE PORT



Note: I/O pins have protection diodes to VDD and Vss.

TABLE 5-11: SUMMARY OF PARALLEL SLAVE PORT REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTD	Parallel slave port Read/Write Data	08h	xxxx xxxx
TRISD	PORTD data direction register	88h	1111 1111
PORTE	Parallel slave port Read/Write/Chip Select signals	09h	---- -xxx
TRISE	Control bits for PORTD peripheral	89h	0000 -111
PIR1	Interrupt register (PSPIF bit)	0Ch	0000 0000
PIE1	Interrupt Enable register (PSPIE bit)	8ch	0000 0000

6.0 OVERVIEW OF TIMER MODULES

The PIC16C64 has three timer modules. Each module can generate an interrupt to indicate that an event has occurred (i.e. timer overflow). Each of these modules is explained in full detail in the following sections. The timer modules are:

- Timer0 (TMR0) module (see Section 7)
- Timer1 (TMR1) module (see Section 8)
- Timer2 (TMR2) module (see Section 9)

For enhanced time-based functionality, the following module can be used with either of the TMR1 or TMR2 modules. This module is the:

- Capture/Compare/PWM (CCP1) module (see Section 10)

6.1 Timer0 (TMR0) Overview

The TMR0 module is identical to the RTCC module of other PIC16CXX enhanced core products (and very similar to the PIC16C5X products). The TMR0 module is a simple 8-bit overflow counter. The clock source can be either the internal system clock (OSC/4) or an external clock. When the clock source is an external clock, the TMR0 module can be selected to increment on either the rising or falling edge.

The TMR0 module also has a programmable prescaler option. This prescaler can be assigned to either the RTCC module or the Watchdog Timer. The PSA bit (OPTION<3>) assigns the prescaler, and the PS2 -PS0 (OPTION<2:0>) determines the prescaler value. The RTCC can increment at the following rates: 1:1 (when prescaler assigned to Watchdog Timer), 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, 1:256.

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher then the device's frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

When the clock source is an external clock, the TMR0 module can be selected to increment on either the rising or falling edge.

6.2 Timer1 (TMR1) Overview

Timer1 (TMR1) is a 16-bit timer/counter. The clock source can be either the internal system clock (OSC/4), an external clock, or an external crystal. TMR1 can operate as either a timer or a counter. When operating as a counter (external clock source), the counter can either operate synchronized to the device or asynchonously to the device. Asynchonous operation allows TMR1 to operate during sleep, which is useful for applications that require a real time clock as well as the power savings of sleep mode.

TMR1 also has a prescaler option which allows the TMR1 to increment at the following rates: 1:1, 1:2, 1:4, 1:8. TMR1 can be used in conjunction with the Capture / Compare / PWM (CCP1) module. When used with the CCP1 module, TMR1 is the timebase for 16-bit capture or the 16-bit compare. When using the TMR1 module with the CCP1 module, TMR1 must be synchronized to the device (timer or synchronized counter mode).

6.3 Timer2 (TMR2) Overview

Timer2 (TMR2) is an 8-bit timer. TMR2 has both a programmable prescaler and postscaler, as well as an 8-bit period register (PR2). TMR2 can be used with the CCP1 module as well as the baud rate generator for the Synchronous Serial Port (SSP). The prescaler option which allows the TMR2 to increment at the following rates: 1:1, 1:4, 1:16.

The postscaler allows TMR2 to match the period register (PR2) a programmable number of times before generating an interrupt. The postscaler can be programmed from 1:1 to 1:16 (inclusive).

6.4 CCP1 Overview

The CCP1 module can operate in one of these three modes: 16-bit capture, 16-bit compare, or 10-bit Pulse Width Modulation (PWM)

Capture mode, captures the 16-bit value of TMR1 into the CCPR1H:CCPR1L register pair. The capture event can be programmed for either the falling edge, rising edge, fourth rising edge, or the sixteenth rising edge of the CCP1 pin.

Compare mode, compares the TMR1H:TMR1L register pair to the CCPR1H:CCPR1L register pair. When a match occurs an interrupt can be generated, and the output pin CCP1 can be forced to given state (High or Low) or TMR1 can be reset. This depends on the control bits CCP1M3 - CCP1M0.

PWM mode, compares TMR2 to a 10-bit duty cycle register as well as to an 8-bit period register (PR2). When the TMR2 = PR2, TMR2 is reset to 00h, an interrupt can be generated, and the CCP1 pin (if an output) will be forced high. When the TMR2 = Duty Cycle register, the CCP1 pin will be forced low.

7.0 TIMER0 (TMR0) MODULE

The TMR0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable (file address 01h)
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

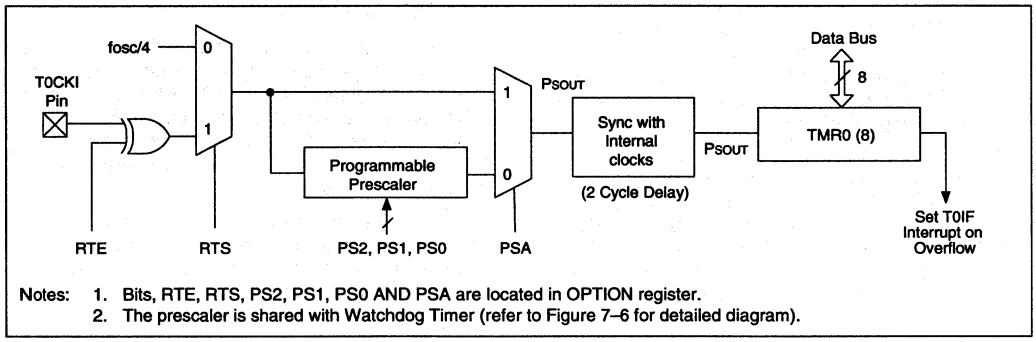
Figure 7-1 is a simplified block diagram of the TMR0 module.

Timer mode is selected by clearing the RTS bit (OPTION<5>). In timer mode, the TMR0 module will increment every instruction cycle (without prescaler). If TMR0 is written, increment is inhibited for the following two cycles (see Figures 7-2 and 7-3). The user can work around this by writing an adjusted value to the TMR0 module.

Counter mode is selected by setting the RTS bit (OPTION<5>). In this mode TMR0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by control bit RTE (OPTION<4>). Clearing the RTE bit selects the rising edge. Restrictions on the external clock input is discussed in detail in Section 7.2.

The prescaler is shared between the TMR0 module and the Watchdog Timer. The prescaler assignment is controlled in software by control bit, PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to TMR0. The prescaler is not readable or writable. When the prescaler is assigned to the TMR0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable. Section 7.3 details the operation of the prescaler.

FIGURE 7-1: TIMER0 (TMR0) BLOCK DIAGRAM



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 AND PSA are located in OPTION register.
2. The prescaler is shared with Watchdog Timer (refer to Figure 7–6 for detailed diagram).

FIGURE 7-2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALE

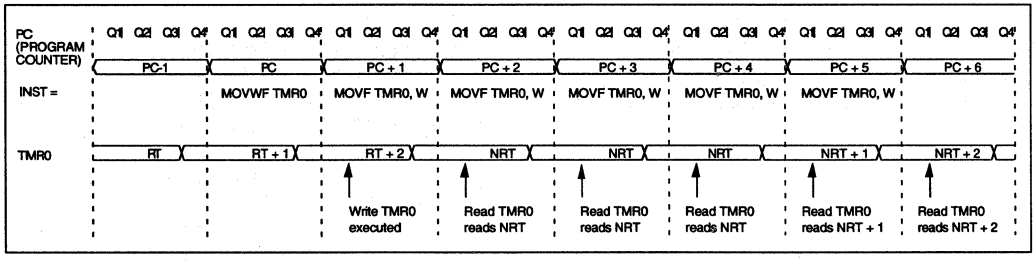
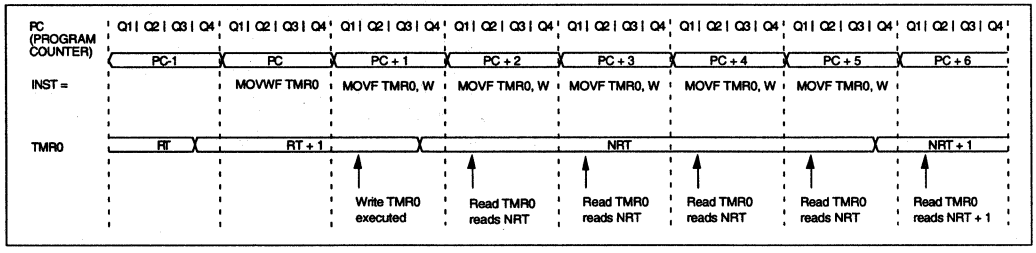


FIGURE 7-3: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/PRESCALE 1:2



7.1 TIMER0 (TMR0) Interrupt

TMR0 interrupt is generated when the TMR0 module timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the TMR0 module interrupt service routine before re-enabling this interrupt. The TMR0 module interrupt can not wake the processor from SLEEP since the timer is shut off during SLEEP. See Figure 7-4 for TMR0 interrupt timing.

7.2 Using TMR0 with External Clock

When external clock input is used for TMR0, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements.

Also there is some delay from the occurance of the external clock edge to the actual incrementing of TMR0. Referring to Figure 7-5, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where:

tosc = oscillator time period.

When no prescaler is used, PSOUT (Prescaler output, see Figure 7-1) is the same as TMR0 clock input and therefore the requirements are:

T_{RTH} = TMR0 high time ≥ 2tosc + ΔT (See parameter #40)

T_{RTL} = TMR0 low time ≥ 2tosc + ΔT (See parameter #41)

When prescaler is used, the TMR0 module input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.

Then:

$$P_{SOUT}\text{ high time} = P_{SOUT}\text{ low time} = \frac{N \cdot T_{RT}}{2}$$

where

T_{RT} = TMR0 input period

N = prescale value (2, 4, ..., 256).

The requirement is, therefore:

$$\frac{N \cdot T_{RT}}{2} \geq 2\,tosc + \Delta T, \text{ or } T_{RT} \geq \frac{4\,tosc + 2\,\Delta T}{N}$$

where

ΔT = small RC delay (see Timing Specifications).

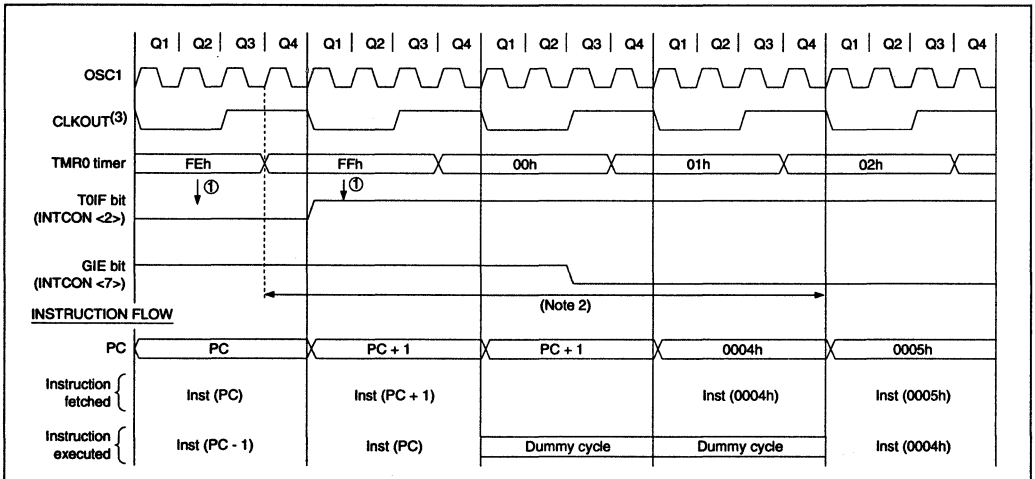
The user will notice that no requirement on TMR0 high time or low time is specified. However, if the high time or low time on TMR0 is too small then the pulse may not be detected, hence a minimum high or low time of 10 ns is required. In summary, the TMR0 module input requirements are:

T_{RT} = TMR0 period ≥ (4 tosc + 2 ΔT)/N

T_{RTH} = TMR0 high time ≥ ΔT

T_{RTL} = TMR0 low time ≥ ΔT

FIGURE 7-4: TIMER0 (TMR0) INTERRUPT TIMING



Notes:
1. T0IF interrupt flag is sampled here (every Q1).
2. Interrupt latency = 4 Tcy where Tcy = instruction cycle time.
3. CLKOUT is available only in RC oscillator mode.

Delay from external clock edge: Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 module is actually incremented. Referring to Figure 7-5, the reader can see that this delay is between 3 tosc and 7 tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±200ns @ 20 MHz).

7.3 Prescaler

An 8-bit counter is available as a prescaler for the TMR0 module, or as a post-scaler for the Watchdog Timer, respectively (see Figure 7-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the TMR0 module and the Watchdog Timer. Thus, a prescaler assignment for the TMR0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2-PS0 bits (OPTION<3:0>) determine the prescaler assignment and pre-scale ratio.

When assigned to the TMR0 module, all instructions writing to the TMR0 module (e.g. `CLRF 1`, `MOVWF 1`, `BSF 1,x`....etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK

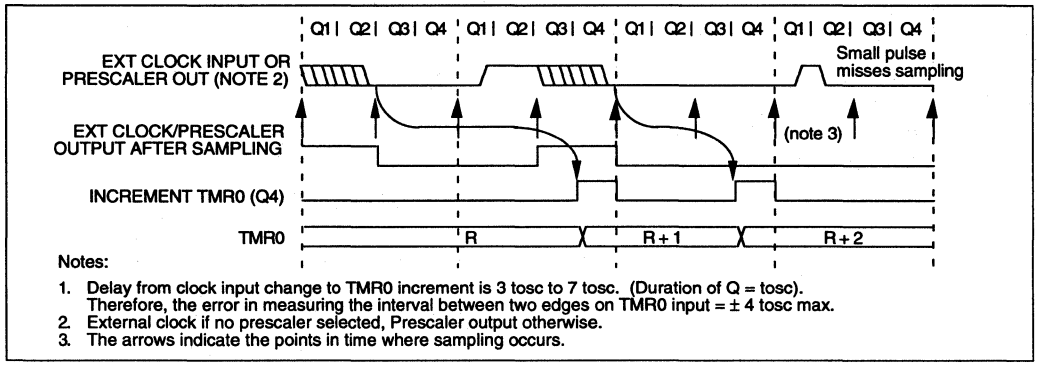
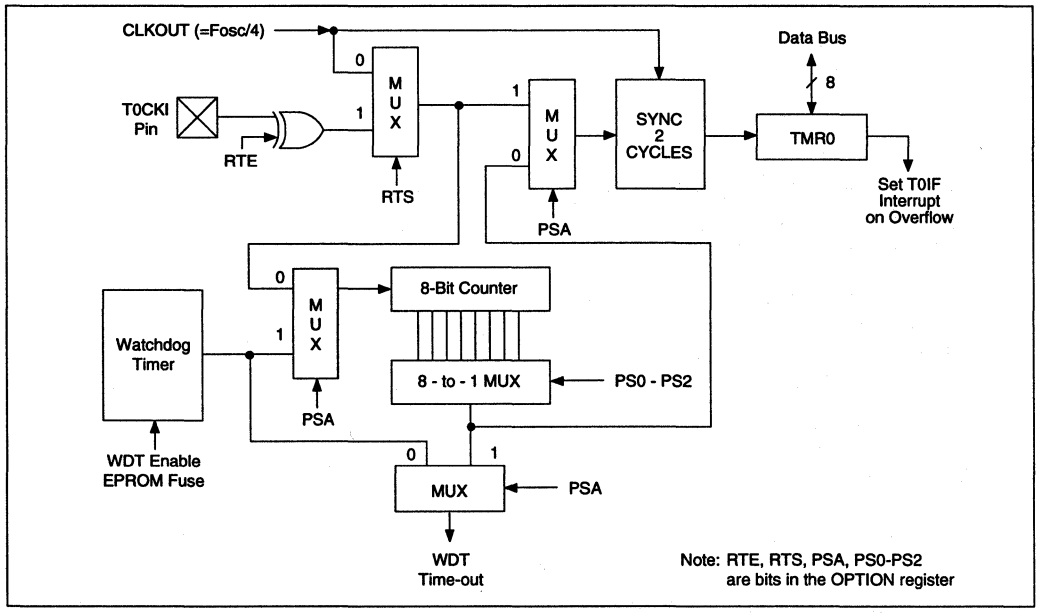


FIGURE 7-6: BLOCK DIAGRAM OF THE TMR0/WDT PRESCALER



7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence (shown in Example 7-1) must be executed when changing the prescaler assignment from TMR0 to WDT. Depending on the selected prescaler value (lines 2 and 3) determines if lines 9 and 10 are required:

EXAMPLE 7-1: CHANGING PRESCALER (TMR0→WDT)

```
1. BCF     STATUS, RP0   ;Bank 0
2. CLRF    TMR0          ;Clear TMR0
3. BSF     STATUS, RP0   ;Bank 1
4. CLRWDT                ;Clears WDT and
                         ;   prescale
5. MOVLW   B'xxxx1xxx'   ;Select new prescale
6. MOVWF   OPTION        ;   value
7. BCF     STATUS, RP0   ;Bank 0
```

Steps 2 and 3 are only required if an external TMR0 source is used. Steps 9 and 10 are necessary only if the desired prescale value is '000' or '001'.

To change prescaler from the WDT to the TMR0 module use the sequence shown in Example 7-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TMR0)

```
1. CLRWDT                ;Clear WDT and
                         ;prescaler
2. BSF STATUS, RP0
3. MOVLW B'xxxx0xxx'     ;Select TMR0, new
                         ;prescale value and
                         ;clock source
4. MOVWF OPTION          ;
5. BCF STATUS, RP0
```

2

TABLE 7-1: SUMMARY OF TMR0 REGISTERS

Register Name	Function	Address	Power-on Reset Value
TMR0	Timer/counter register	01h	XXXX XXXX
OPTION	Configuration and prescaler assignment bits for TMR0. See Figure 4-4	81h	1111 1111
INTCON	TMR0 overflow interrupt flag and mask bits See Figure 4-5	0Bh	0000 000X

TABLE 7-2: REGISTERS ASSOCIATED WITH TMR0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01	TMR0	TIMER0							
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
81	OPTION	RBPU	INTEDG	RTS	RTE	PSA	PS2	PS1	PS0
85	TRISA	—	—	TRISA 5	TRISA 4	TRISA 3	TRISA 2	TRISA 1	TRISA 0

Legend — = Unimplemented locations, Read as '0'
Shaded boxes are not used by TMR0 module.

8.0 TIMER1 (TMR1) MODULE

Timer1 is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. TMR1 increments from 0000h to FFFFh and rolls over to 0000h. An interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled or disabled using the timer1 interrupt enable bit TMR1IE (PIE1<0>).

TMR1 can operate in one of two modes:

- As a timer
- As a counter

This is determined by the clock select bit, TMR1CS (TICON<1>).

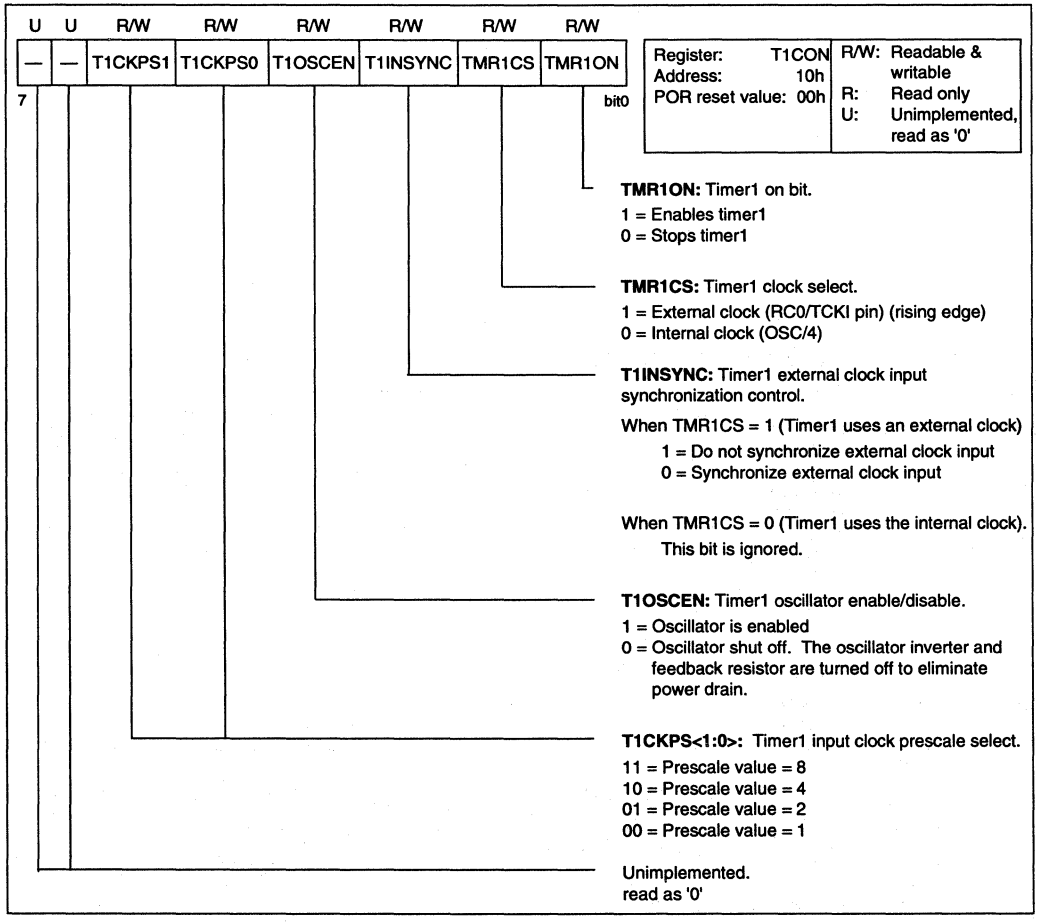
In timer mode, TMR1 increments every instruction cycle. In counter mode, it increments on every rising edge of external clock input on pin RC0/T1CKI.

Timer1 can be turned on or off using the control bit TMR1ON (T1CON<0>). See description of T1CON control register for all control bits related to Timer1.

Timer1 also has an internal "reset input". This reset can be generated by CCP1 (Capture/compare/PWM) module. See Section 10 for details. Figure 8-1 shows the Timer1 control register.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1CKO pin becomes an output. That is, the TRISC<1> value is ignored. The RC0/T1CKI pin should normally be configured as an input (for external clock). However, this pin can be configured as an output, if self-clocking (through the output pin) is desired.

FIGURE 8-1: T1CON: TIMER1 CONTROL REGISTER



8.1 TMR1 Operation in Timer Mode

Timer mode is selected by clearing the TMR1CS (T1CON<1>) bit. In this mode, the input clock to the timer is OSC/4. The synchronize control bit T1INSYNC (T1CON<2>) has no effect since the internal clock is always in sync.

8.2 TMR1 Operation in Synchronized Counter Mode

Counter mode is selected by setting the TMR1CS bit. In this mode the timer increments on every rising edge of clock input on pin RC0/T1OSCO/T1CKI.

If T1INSYNC is cleared, then the external clock input is synchronized with internal phase clocks. The synchronization is done after the prescaler stage. The prescaler stage is an asynchronous ripple counter.

In this configuration, during SLEEP mode, TMR1 will not increment even if external clock is present, since the synchronization circuit is shut off. The prescaler however will continue to increment.

8.2.1 EXTERNAL CLOCK INPUT TIMING FOR SYNCHRONIZED COUNTER MODE

In synchronized counter mode, the prescaler output is sampled twice every instruction cycle. Therefore, the following restrictions apply to external clock input:

when prescaler is 1:1:

T_{TCKIH} = T1CKI high time $\geq 2\ tosc + \Delta T$

T_{TCKIL} = T1CKI low time $\geq 2\ tosc + \Delta T$

where ΔT = small RC delay (see timing specifications)

when prescaler is higher:

The input clock is divided by two or more, so the prescaler output is symmetrical. The requirements are then:

Prescaler out high time = Prescaler out low time

$$= \frac{N \bullet T_{T1CKIP}}{2} \geq 2\ tosc + \Delta T$$

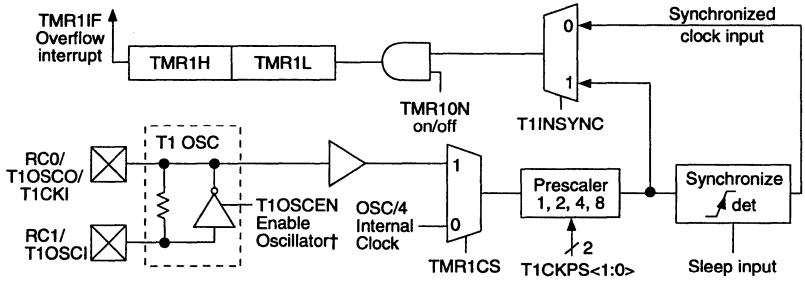
$$\text{or } T_{T1CKIP} \geq \frac{4\ tosc + \Delta T}{N}$$

where T_{T1CKIP} = T1CKI input clock period
N = prescale value (2, 4, 8)
ΔT = small RC delay (see timing specifications)

Note that no requirement on minimum high time or low time is mentioned. However, if the pulse is too small it may not be recognized. Hence a minimum high and low time is specified.

$T_{T1CKIH} \geq \Delta T$ (see timing specification #45)
$T_{T1CKIL} > \Delta T$ (see timing specification # 46)

FIGURE 8-2: TMR1 BLOCK DIAGRAM



† When the T1 OSCEN bit is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

8.3 TMR1 Operation in Asynchronous Counter Mode

If the control bit T1INSYNC is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and generate an interrupt on overflow which will wake up the processor. However, special precautions in software are needed to read/write the timer (see Section 8.3.2).

In asynchronous counter mode, Timer1 can not be used as timebase for capture or compare operations.

8.3.1 EXTERNAL CLOCK INPUT TIMING WITH UNSYNCHRONIZED CLOCK

If T1INSYNC is set, the timer will increment completely asynchronously. The input clock must meet a certain minimum high time and low time requirements, as specified in timing specifications #45 and #46.

8.3.2 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running off external asynchronous clock will guarantee a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers while the register is incrementing. This may produce an unpredictable value in the timer register.

Writing to the timer is no problem, if the clock is slower than the instruction cycle time. Reading the 16-bit value requires some care. Example 8-1 is an example routine to read the 16-bit timer value. This is useful if the timer cannot be stopped.

EXAMPLE 8-1: READING A 16-BIT FREE-RUNNING TIMER

```
;  All Interrupts are disabled
    MOVF    TMR1H, Wreg     ; Read high byte
    MOVWF   TMPH            ;
    MOVF    TMR1L, Wreg     ; Read low byte
    MOVWF   TMPL            ;
    MOVF    TMR1H, Wreg     ; Read high byte
    SUBWF   TMPH, Wreg      ; Sub 1st read
                            ;   with 2nd read
    BTFSC   STATUS,  Z      ;   is result = 0
    GOTO    CONTINUE        ; Good 16-bit read
;
; TMR1L may have rolled over between the read
; of the high and low bytes. Reading the high
; and low bytes now will read a good value.
;
    MOVF    TMR1H, Wreg     ; Read high byte
    MOVWF   TMPH            ;
    MOVF    TMR1L, Wreg     ; Read low byte
    MOVWF   TMPL            ;
;  Re-enable Interrupt (if required)
CONTINUE    :               ; Continue with your
                            ; code
```

8.4 Timer1 Oscillator

A crystal oscillator circuit is built in between T1CKI pin (input) and T1CKO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low-power oscillator rated up to 200KHz. It will continue to run during SLEEP. It is primarily intended for a 32KHz crystal. Table 8-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must allow software time-out to ensure proper oscillator start-up.

TABLE 8-1: CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz§	15 pF	15 pF
	100 KHz	15 pF	15 pF
	200 KHz	0 - 15 pF	0 - 15 pF
Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. §For V_{DD} > 4.5V, C1 = C2 ~ 30pf is recommended.			

8.5 Resetting Timer1 using CCP1 Trigger Output

If CCP1 module is configured in compare mode to generate a "special event" trigger (CCP1M<3:0> = 1011), this signal will reset timer1.

Timer1 must be configured for timer or synchronized counter mode operation to take advantage of this feature. If the Timer1 is running in asynchronous counter mode, this reset operation may not work.

In the event that a write to Timer1 coincides with a reset trigger from CCP1, the write will take precedence.

In this mode of operation, the CCPR1H:CCPR1L registers pair effectively becomes the period register for the timer1.

8.6 Resetting of Timer Registers

TMR1H and TMR1L registers are not reset on POR or any other reset except by the CCP1 special reset trigger.

T1CON register is reset to 00h on Power-On Reset. In any other reset, the register is unaffected.

8.7 Prescaler

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

2

TABLE 8-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
0E	TMR1L	Timer1 Least Significant Byte							
0F	TMR1H	Timer1 Most Significant Byte							
10	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1INSYNC	TMR1CS	TMR1ON

Legend — = Unimplemented locations, Read as '0'
Note: Shaded boxes are not used by Timer1 module.

9.0 TIMER2 (TMR2) MODULE

Timer2 is an 8-bit timer with a prescaler and a postscaler. It is especially suitable as PWM time-base (for PWM mode of CCP module). TMR2 is a readable and writable register.

The input clock (osc/4) has a prescale option of 1, 4 or 16 (selected by control bits TCKPS1, TCKPS0, register T2CON).

Timer2 has an 8-bit period register PR2. Timer2 increments from 00h until it matches PR2 and then resets t0 00h. PR2 is a readable and writable register.

The overflow (or match) output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling) to generate timer2 interrupt (latched in TMR2IF bit, PIR<1>).

Timer2 can be shut off using TMR2ON (T2CON<2>) control bit to minimize power consumption.

Figure 9-2 shows the Timer2 control register.

9.1 Prescaler and Postscaler

The prescaler and postscaler counters are cleared when any of the following occurs: a write to the TMR2 register, a write to the T2CON register, or any device reset (Power-On Reset, MCLR reset, or Watchdog Timer reset).

9.2 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the synchronous serial port module which optionally uses it to generate shift clock.

FIGURE 9-1: TIMER2 BLOCK DIAGRAM

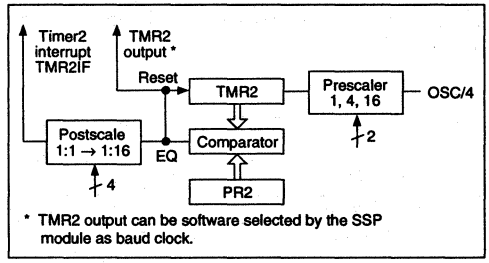


FIGURE 9-2: T2CON: TIMER2 CONTROL REGISTER

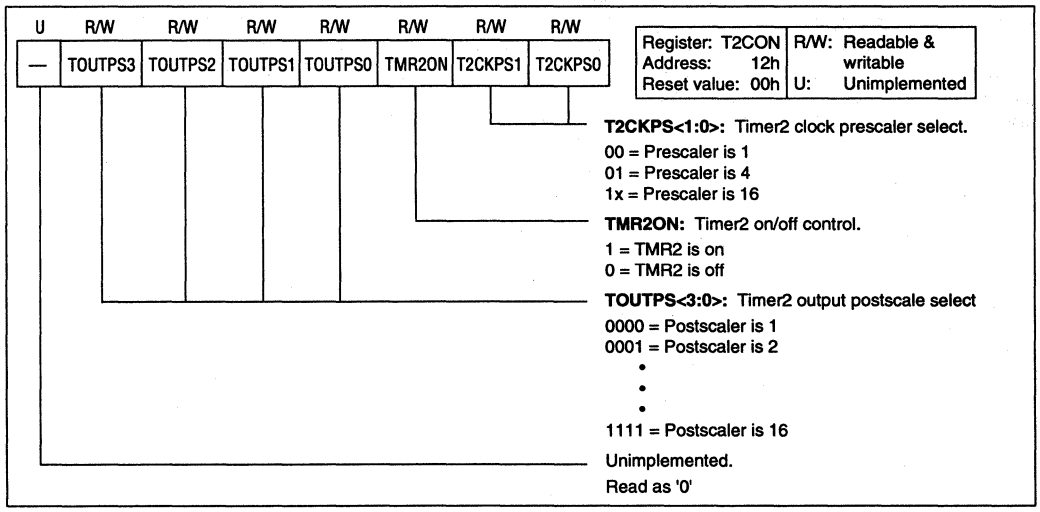


TABLE 9-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
11	TMR2	Timer2							
12	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
92	PR2	Timer2 period Register							

Legend — = Unimplemented locations, Read as '0'
Note: Shaded boxes are not used by Timer2 module.

10.0 CAPTURE/COMPARE/PWM MODULE

The PIC16C64 has a Capture/Compare/PWM (CCP) module consisting of a 16-bit register which can operate as a 16-bit capture register, as a 16-bit compare register or as a PWM output.

CCP1 module:

Capture/compare/PWM register1 (CCPR1) is made up of two 8-bit sections: low byte, CCPR1L and high byte, CCPR1H. Both are readable and writable.

10.1 Capture Mode

In Capture mode, CCPR1 captures the 16-bit value of TMR1 when an event occurs on pin RC2/CCP1. An event is defined as:

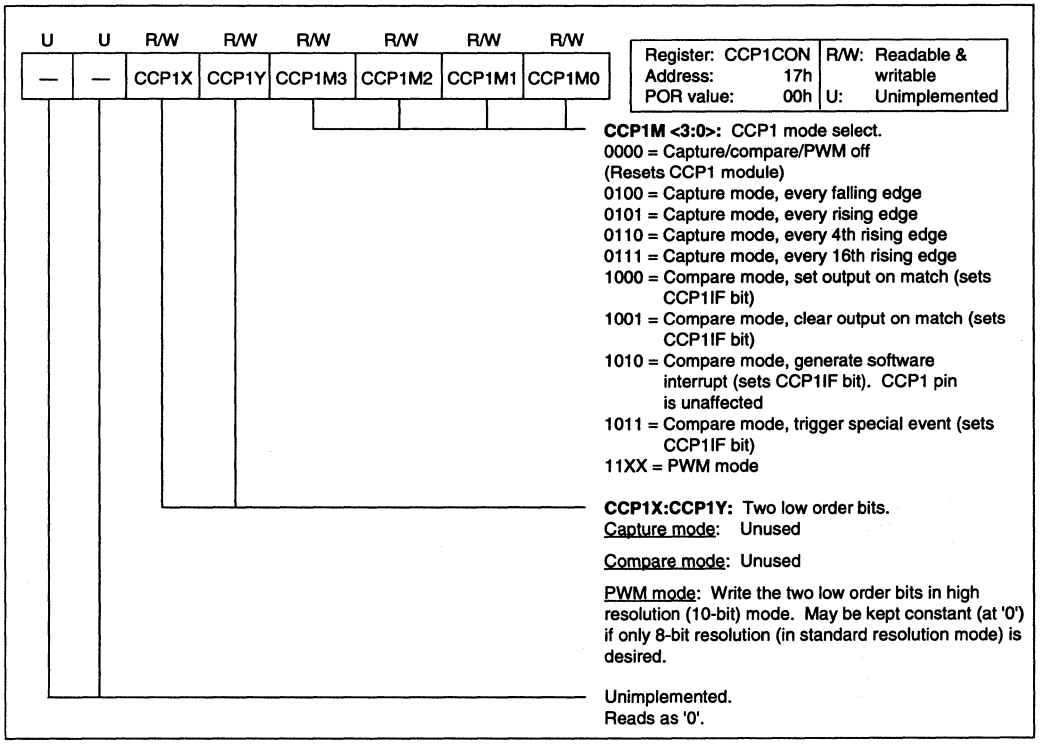
1. A falling edge
2. A rising edge
3. Every 4 rising edges
4. Every 16 rising edges

One of these is selected by the control bits CCP1M <3:0> in register CCP1CON. When a capture is made the interrupt request flag, CCP1IR bit (PIR<2>) is set. It must be reset in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost. In capture mode, the RC2/CCP1 pin should be configured as an input through its corresponding TRIS bit.

Note: If the RC2/CCP1 is configured as an output, a write to the port can cause a capture condition.

When the capture mode is changed, a false capture interrupt may be generated. The user should clear the CCP1IF bit following any such change in operating mode.

FIGURE 10-1: CCP1CON REGISTER



10.1.1 PRESCALER DETAILS

There are four prescaler setting, specified by the CCP1M3-CCP1M0 bits. Whenever the CCP module is turned off, or the CCP module is not in capture mode, the prescaler counter is cleared. This means that any reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, and therefore the first capture may be from a non-zero prescaler. Example 10-1 shows the recommended way to switch between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

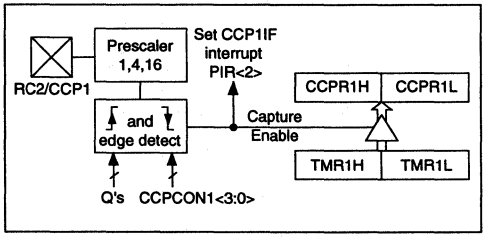
EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF    CCP1CON      ; Turn CCP module off
MOVLW   NEW_CAPT_PS  ; Load the W reg with
                     ;   the new prescaler
                     ;   mode value
MOVWF   CCP1CON      ; Load CCP1CON with
                     ;   this value
```

10.1.2 TIMER1 MODE SELECTION

Timer1 must be running in timer mode or synchronized counter mode for the CCP1 modules to use the capture feature. In asynchronous counter mode the capture operation may not work.

FIGURE 10-2: CAPTURE MODE OPERATION



10.2 Compare Mode

In compare mode, the 16-bit CCPR1 register value is constantly compared against the timer1. When a match occurs, the RC2/CCP1 pin is:

- Driven High
- Driven Low
- Remains Unchanged

The action on the pin is based on the control bits CCP1M <3:0> in register CCP1CON. At the same time, a compare interrupt is also generated (bit CCP1IR, register CCP1CON). The user must set the RC2/CCP1 pin as an output through the TRISC<2> bit.

Note: Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the data latch.

10.2.1 TIMER1 MODE SELECTION

Timer1 must be running in timer mode or synchronized counter mode if the CCP1 module is using the compare feature. In asynchronous counter mode the compare operation may not work.

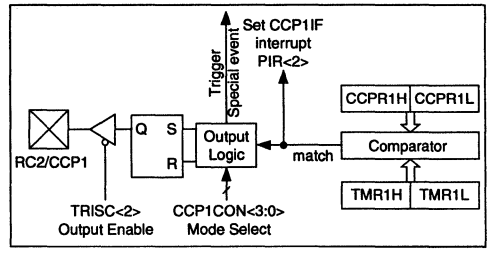
10.2.2 SOFTWARE INTERRUPT MODE

Another compare mode is software interrupt mode in which the CCP1 pin is not affected. Only CCP1IF interrupt is generated.

10.2.3 SPECIAL TRIGGER

The special trigger output of CCP1 is an internal Hardware Trigger which can be used to reset the timer1. This allows the CCPR1 register to effectively be a 16-bit programmable period register for timer1.

FIGURE 10-3: COMPARE MODE OPERATION



10.3 PWM Mode

In Pulse Width Modulation (PWM) mode, the RC2/CCP1 produces up to 10-bit resolution PWM output. This pin must be configured as an output through the TRISC<2> bit. In PWM mode, the user writes the 8-bit duty-cycle value to the low byte of the CCPR1 register, namely CCPR1L. The high-byte, CCPR1H is used as the slave buffer to the low byte. The 8-bit data is transferred from the master to the slave when the PWM1 output is set (i.e. at the beginning of the duty cycle). This double buffering is essential for glitchless PWM output. In PWM mode CCPR1H is readable but not writable. The period of the PWM is determined by timer2 period register (PR2).

PWM period is =
[(PR2) + 1] • 4 tosc • (TMR2 prescale value)

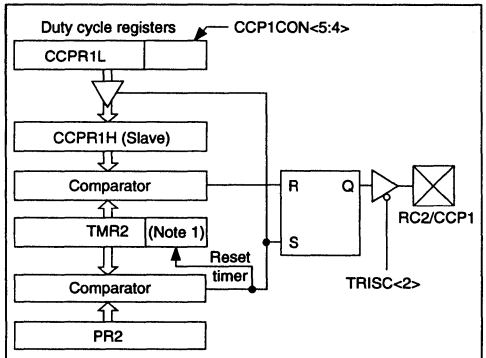
PWM duty cycle =
(DC1) • tosc • (TMR2 prescale value)

where DC1 = 10 bit value from CCPR1L and CCP1CON<5:4> concantenated.

The PWM output resolution is therefore programmable up to a maximum of 10-bit.

Note: Clearing the CCP1CON register will force the RC2/CCP1 PWM output latch to the default low level. This is not the I/O data latch.

FIGURE 10-4: SIMPLIFIED PWM BLOCK DIAGRAM



Note: 8-bit timer is concantenated with 2-bit internal Q clock or 2 bits of the prescaler to create 10-bit time base.

TABLE 10-1: PWM FREQUENCY VS RESOLUTION AT 20 MHZ

Max Resolution (High Resolution Mode)	Frequency		
	TMR2 Prescale = 1	TMR2 Prescale = 4	TMR2 Prescale = 16
10 bit	19.53 KHz	4.88 KHz	1.22 KHz
9 bit	39.06 KHz	9.77 KHz	2.44 KHz
8 bit	78.13 KHz	19.53 KHz	4.88 KHz

TABLE 10-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 KHz	4.88 KHz	19.53 KHz	78.13 KHz	157.5 KHz	210.53 KHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0xFF	0x7F	0x5F
Resoution (High-resolution mode†)	10-bit	10-bit	10-bit	8-bit	7-bit	6.5-bit
Resolution (Standard-resolution mode†)	8-bit	8-bit	8-bit	6-bit	5-bit	4.5-bit

† Standard resolution mode has the CCPIX:CCPIY bit constant (or '0'), and only compares the TMR2 against the PR2. The Q-cycles are not used.

TABLE 10-3: REGISTERS ASSOCIATED WITH TIMER1 AND CAPTURE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
0E	TMR1L	Timer1 Least Significant Byte							
0F	TMR1H	Timer1 Most Significant Byte							
10	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1INSYNC	TMR1CS	TMR1ON
15	CCPR1L	Timer1 Capture Register (LSB)							
16	CCPR1H	Timer1 Capture Register (MSB)							
17	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0

Legend — = Unimplemented locations, Read as '0' Note: Shaded boxes are not used in this mode.

TABLE 10-4: REGISTERS ASSOCIATED WITH TIMER1 AND COMPARE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
0E	TMR1L	Timer1 Least Significant Byte							
0F	TMR1H	Timer1 Most Significant Byte							
10	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1INSYNC	TMR1CS	TMR1ON
15	CCPR1L	Timer1 Compare Register (LSB)							
16	CCPR1H	Timer1 Compare Register (MSB)							
17	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0

Legend — = Unimplemented locations, Read as '0' Note: Shaded boxes are not used in this mode.

TABLE 10-5: REGISTERS ASSOCIATED WITH TIMER2 AND PWM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
11	TMR2	Timer2							
92	PR2	Timer2 period Register							
12	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
15	CCPR1L	Timer2 Duty Cycle Register							
16	CCPR1H	Timer2 Duty Cycle Register (Slave)							
17	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0

Legend — = Unimplemented locations, Read as '0' Note: Shaded boxes are not used in this mode.

11.0 SYNCHRONOUS SERIAL PORT (SSP)

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)

FIGURE 11-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER

U	U	R	R	R	R	R	R
—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
							Bit 0

Register SSPSTAT	R/W: Readable & writable bit
Addr: 94h	R: Read only bit
POR value: 00h	U: Unimplemented, read as '0'

BF: Buffer full
Receive Mode
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty
Transmit Mode
1 = Transmit in progress, SSPBUF is full
0 = Transmit complete, SSPBUF is empty

UA: Update Address (10-bit I^2C slave mode only).
1 = Indicate that the user needs to update the address in the SSPADD register. See Section 11.2 for details.
0 = Address does not need to be updated.

R/$\overline{W}$: Read/write bit information (I^2C mode only)
This bit holds the R/$\overline{W}$ bit information received following the last address match. This bit is only valid during the transmission.
The user may use this bit in software to determine whether transmission or reception is in progress.
1 = Read
0 = Write

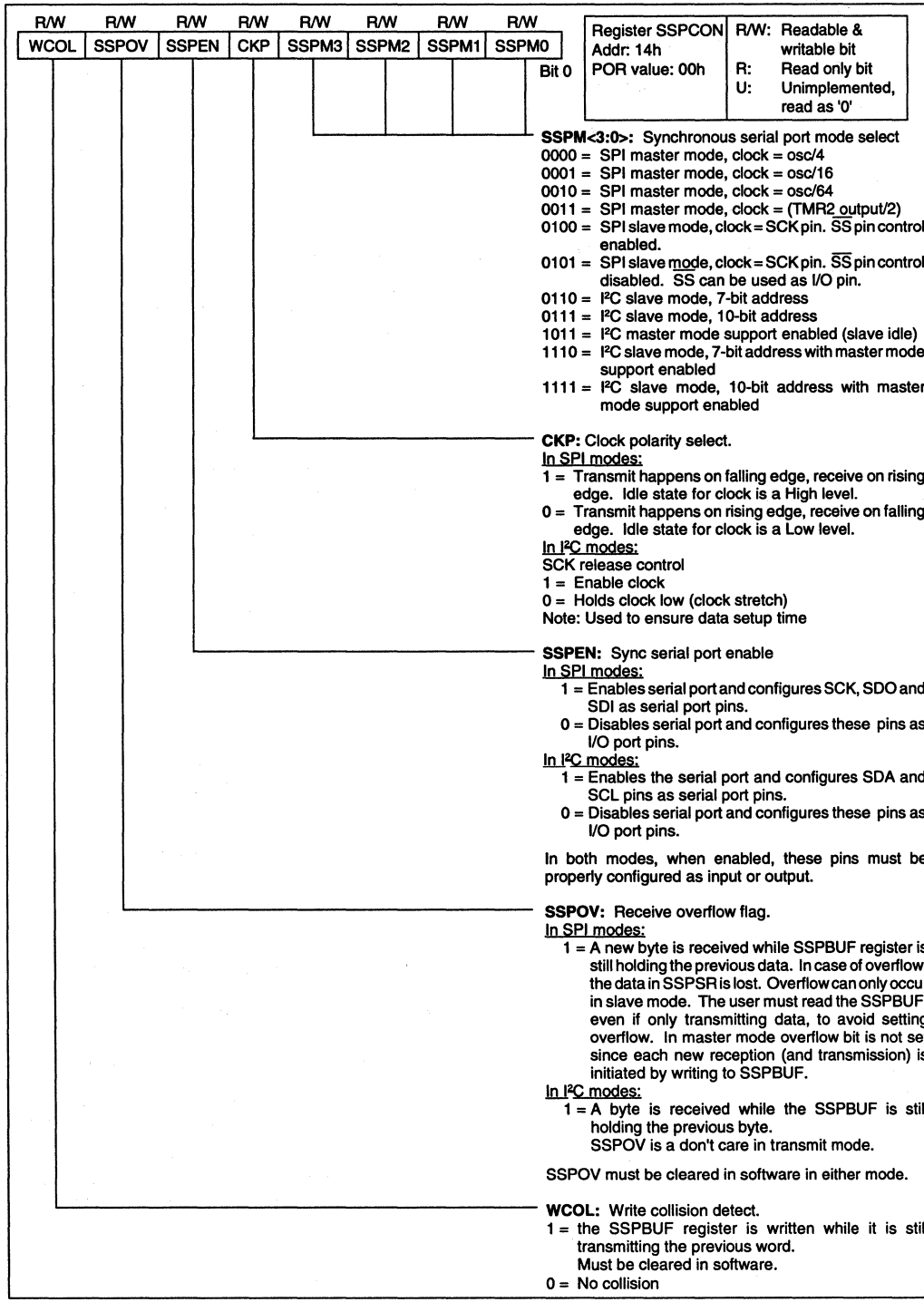
S: Start bit (I^2C mode only) Flag
This bit is cleared when the SSP module is disabled (SSPEN is cleared)
1 = Indicates that a start bit has been detected last. This bit is 0 on reset.
0 = Start bit was not detected last
Note: This bit also operates in the Master Modes

P: Stop bit (I^2C mode only) Flag
This bit is cleared when the SSP module is disabled (SSPEN is cleared)
1 = Indicates that a stop bit has been detected last.
0 = Stop bit was not detected last
Note: This bit also operates in the Master Modes

D/$\overline{A}$: Data/Address bit (I^2C mode only)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was address

Unimplemented.
Reads as '0'.

FIGURE 11-2: SSPCON: SYNC SERIAL PORT CONTROL REGISTER



11.1 SPI Mode

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO)
- Serial Data In (SDI)
- Serial Clock (SCK)

Additionally a fourth pin may be used when in a slave mode of operation:

- Slave Select ($\overline{SS}$)

When initializing the SPI, several options need to be specified. This is done by appropriately programming the control bit in the SSPCON register (SSPCON<5:0>). These control bits allow the following to be specified:

- Master Mode (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Output/Input data on the Rising/Falling edge of SCK)
- Clock Rate(Master mode only)
- Slave Select Mode (Slave mode only)

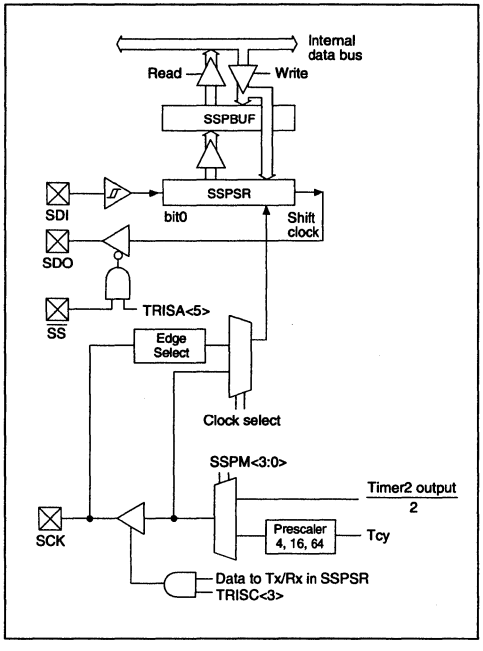
The SSP consists of a transmit/receive Shift Register (SSPSR) and a Buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, while the SSPBUF holds the data that was written to the SSPSR, until the received data is ready. Once the 8-bits of data have been received, that information is moved to the SSPBUF register, the Buffer Full (BF) bit (SSPSTAT <0>) and the SSPIF bit are set. This double buffering of the received data (SSPBUF), allows the next byte to start reception before reading the data that was received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect (WCOL) bit (SSPCON<7>) will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF completed successfully. When the application software is expecting to receive valid data, the SPPBUF should be read before the next byte of data to transfer is written to the SSPBUF. The Buffer Full (BF) bit (SSPSTAT<0>) indicates when the SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally the SSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF can then be read (if data is meaningful) and/or the SSPBUF (SSPSR) can be written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 11-1 shows the loading of the SSPBUF (SSPSR) for data transmission. The instructions with the comment fields beginning with ;*** are only required if the received data is meaningful.

EXAMPLE 11-1: LOADING THE SSPBUF (SSPSR) REGISTER

```
LOOP BSF    STATUS, RP0   ;Specify Bank 1
     BTFSS  SSPSTAT, BF   ;Has data been
                          ;received
                          ;(transmit complete)?
     GOTO   LOOP          ;No
     BCF    STATUS, RP0   ;Specify Bank 0
     MOVF   SSPBUF, W     ;W reg = contents
                          ;of SSPBUF
     MOVWF  RXDATA        ;*** Save in user RAM
     MOVF   TXDATA, W     ;W reg = contents of
                          ;TXDATA
     MOVWF  SSPBUF        ;New data to xmit.
```

The block diagram of the SSP module, when in SPI mode (Figure 11-3), shows that the SSPSR is not directly readable or writable, and can only be accessed from addressing the SSPBUF register. Additionally, the SSP status register (SSPSTAT) indicates the various status conditions.

FIGURE 11-3: SSP BLOCK DIAGRAM (SPI MODE)



To enable the serial port, the SSP enable bit (SSPEN) must be set. This configures the SDI, SDO, SCK, and $\overline{SS}$ pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- $\overline{SS}$ must have TRISA<5> set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value. An example would be in master mode where you are only sending data (to a display driver), then both SDI and $\overline{SS}$ could be used as general purpose inputs by clearing their corresponding TRIS register bits.

Figure 11-4 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data — Slave sends dummy data
- Master sends data — Slave sends data
- Master sends dummy data — Slave sends data

The master can initiate the data transfer at any time because it controls the SCK. How the master knows when the slave (Processor 2) wishes to broadcast data is determined by the software protocol

In master mode the data is transmitted/received as soon as the SSPBUF is written to. If the SPI is only going to receive, the SCK output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "line activity monitor" mode.

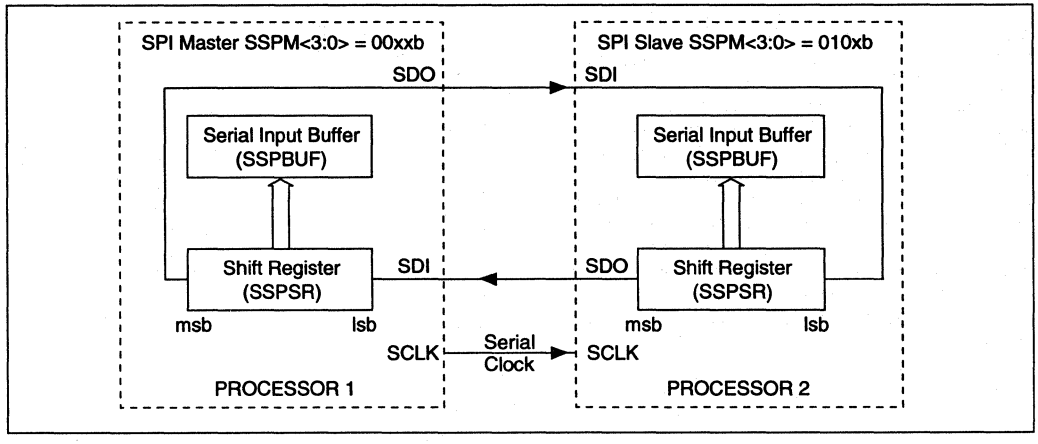
In slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched the interrupt flag (SSPIF) is set (PIR1<3>).

The clock polarity is selected by appropriately programming the CKP bit (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figures 11-5 and 11-6. In master mode the SPI clock rate (bit rate) is user programmable to be one of the following:

- OSC / 4 (or Tcy)
- OSC / 16 (or 4 • Tcy)
- OSC / 64 (or 16 • Tcy)
- Timer2 output / 2

This allows a maximum bit clock frequency (at 20 MHz) of 5 MHz. When in slave mode the external clock must meet the minimum high and low times as specified in timing parameters 71 and 72.

FIGURE 11-4: SPI MASTER / SLAVE CONNECTION



The $\overline{SS}$ pin allows a synchronous slave mode. The SPI must be in slave mode (SSPCON<3:0> = 04h) and the TRISA<5> bit must be set the for the synchronous slave mode to be enabled. When the $\overline{SS}$ pin is low, transmission and reception are enabled and the SDO pin is driven. When the $\overline{SS}$ pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. External pull-up / pull-down resisters may be desirable, depending on the application.

To emulate 2-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 11-5: SPI MODE TIMING (MASTER MODE OR SLAVE MODE W/O $\overline{SS}$ CONTROL)

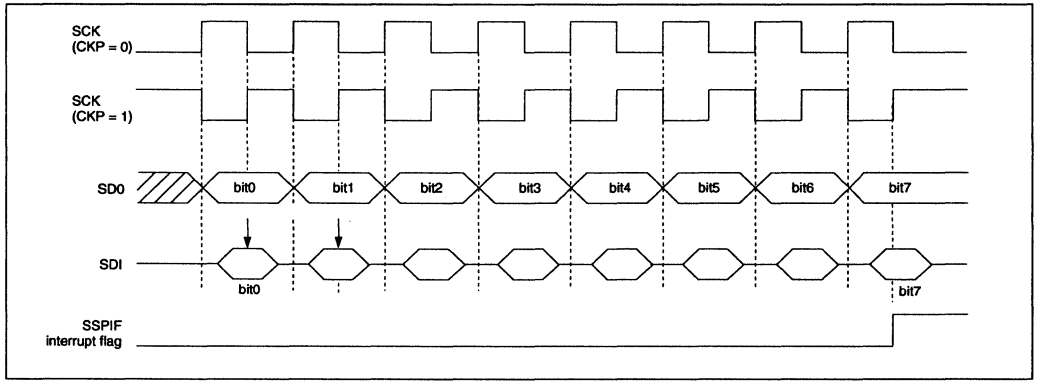


FIGURE 11-6: SPI MODE TIMING (SLAVE MODE WITH $\overline{SS}$ CONTROL)

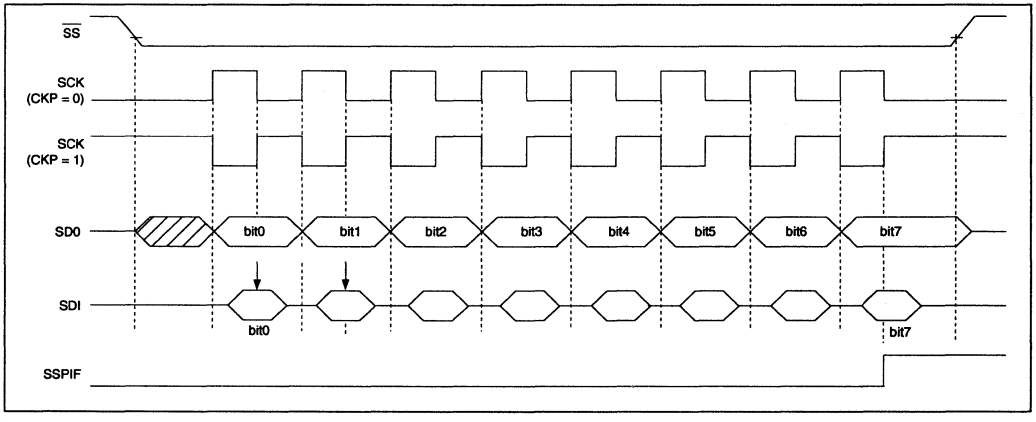


TABLE 11-1: REGISTERS ASSOCIATED WITH SPI OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
13	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register							
14	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
94	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF

Legend — = Unimplemented locations, Read as '0' Note: Shaded boxes are not used by SSP module in SPI mode.

11.2 I²C Overview

This section gives an overview of the Inter-IC (I²C) bus, with Section 11.3 discussing the operation of the SSP module in I²C mode. The Inter-IC (I²C) bus is a two-wire serial interface developed by Philips/Signetics™. The original specification, or standard mode, was for data transfers of up to 100-Kbps. An enhanced specification, or fast mode, supports data transmission up to 400 Kbps. Both standard mode and fast mode devices will inter-operate if attached to the same bus.

The I²C interface employs a comprehensive protocol to ensure reliable transmission and reception of data. When transmitting data, one device is the "master" (generates the clock), while the other device(s) acts as the "slave". All Portions of the slave protocol are implemented in the SSP module's hardware, while portions of the master protocol will need to be addressed in the PIC16CXX software. Table 11-2 defines some of the I²C-bus terminology. For additional information on the I²C interface specification, please refer to the Philips/ Signetics™ document " The I²C-bus and how to use it". The order number for this document is 98-8080-575.

In the I²C interface protocol each device has an address. When a master wishes to initiate a data transfer, it first transmits the address of the device that it wishes to "talk" to. All devices "listen" to see if this is their address. Within this address, a bit specifies if the master wishes to read / write from / to the slave device. The master and slave are always in opposite modes (transmitter/receiver) of operation during a data transfer. That is they can be thought of operating in either of these two relations:

- Master-transmitter and Slave-receiver
- Slave-transmitter and Master-receiver

In both cases the master generates the clock signal.

The output stages of the clock (SCL) and data (SDA) lines must have an open-drain or open-collector in order to perform the wired-AND function of the bus. External pull-up resistors are used to ensure a high level, when no device is pulling the line down.. The number of devices that may be attached to the I²C bus is limited only by the maximum bus loading specification of 400 pF.

11.2.1 INITIATING AND TERMINATING DATA TRANSFER

During times of no data transfer (idle time), both the clock line (SCL) and the data line (SDA) are pulled high through the external pull-up resistors. The START and STOP conditions determine the start and stop of data transmission. The START condition is defined as a high to low transition of the SDA when the SCL is high. The STOP condition is defined as a low to high transition of the SDA when the SCL is high. Figure 11-7 shows the START and STOP conditions. The master generates these conditions for starting and terminating data transfer. Due to the definition of the START and STOP conditions, when data is being transmitted the SDA line can only change state when the SCL line is low.

FIGURE 11-7: START AND STOP CONDITIONS

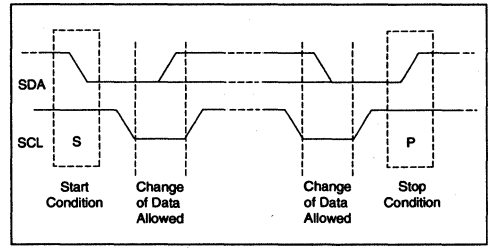


TABLE 11-2: I²C-BUS TERMINOLOGY

Term	Description
Transmitter	The device that sends the data to the bus
Receiver	The device that receives the data from the bus
Master	The device which initiates the transfer, generates the clock, and terminates the transfer
Slave	The device addressed by a master
Multi-master	More than one master device in a system. These masters can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure that ensures that only one of the master devices will control the bus. This ensures that the transfer data does not get corrupted.
Synchronization	Procedure where the clock signals of two or more devices are synchronized.

11.2.2 ADDRESSING I²C DEVICES

There are two address formats. The simplest is the 7-bit address format with a R/W bit (see Figure 11-8). The more complex is the 10-bit address with a R/W bit (see Figure 11-9). For 10-bit address format, two bytes must be transmitted with the first five bits specifying this to be a 10-bit address.

FIGURE 11-8: 7-BIT ADDRESS FORMAT

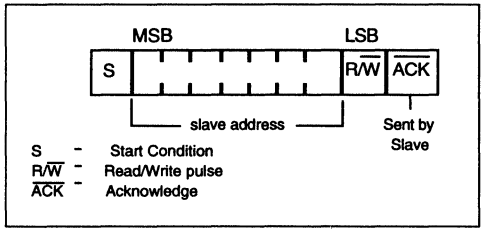
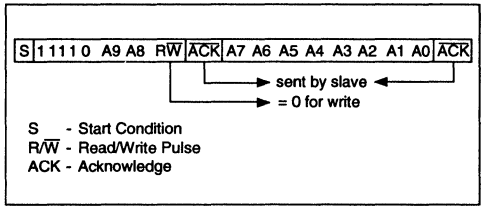


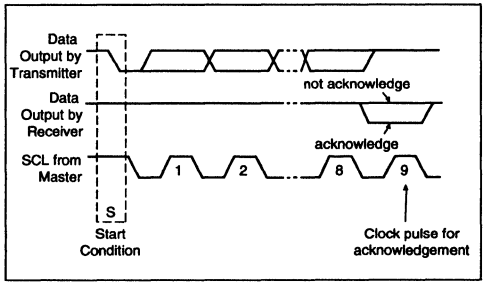
FIGURE 11-9: I²C 10-BIT ADDRESS FORMAT



11.2.3 TRANSFER ACKNOWLEDGE

All data must be transmitted per byte, with no limit to the number of bytes transmitted per data transfer. After each byte, the slave-receiver generates an acknowledge bit (ACK). This is shown in Figure 11-10. When a slave-receiver doesn't acknowledge the slave address or received data, the master must abort the transfer. The slave must leave SDA high so that the master can generate the STOP condition (see Figure 11-7).

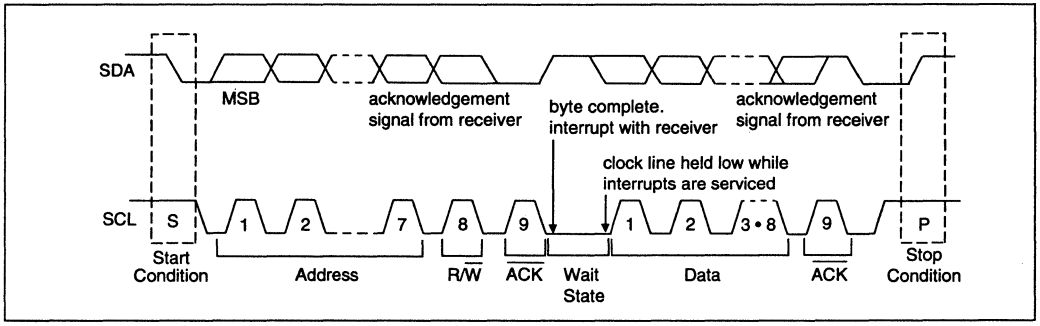
FIGURE 11-10: SLAVE-RECEIVER ACKNOWLEDGE



If the master is receiving the data (master-receiver), it generates an acknowledge signal for each received byte of data, except for the last byte. To signal the end of data to the slave-transmitter, the master does not generate an acknowledge (not acknowledge). The slave then releases the SDA line so the master can generate the STOP condition. The master can also generate the STOP condition during the acknowledge pulse for valid termination of data transfer.

If the slave needs to delay the transmission of the next byte, holding the SCL line low will force the master into a wait state. Data transfer continues when the slave releases the SCL line. This allows the slave to move the received data or fetch the data it needs to transfer before allowing the clock to start. This wait state technique can also be implemented at the bit level. Figure 11-11 shows a data transfer waveform.

FIGURE 11-11: A DATA TRANSFER



Figures 11-12 and 11-13 show Master-transmitter and Master-receiver data transfer sequences.

When a master does not wish to relinquish the bus (by generating a STOP condition), a repeated START condition (Sr) must be generated. This condition is identical to the start condition (SDA goes high-to-low while SCL is high), but occurs after a data transfer acknowledge pulse (not the bus-free state). This allows a master to send "commands" to the slave and then receive the requested information or to address a different slave device. This sequence is shown in Figure 11-14.

FIGURE 11-12: MASTER-TRANSMITTER SEQUENCE

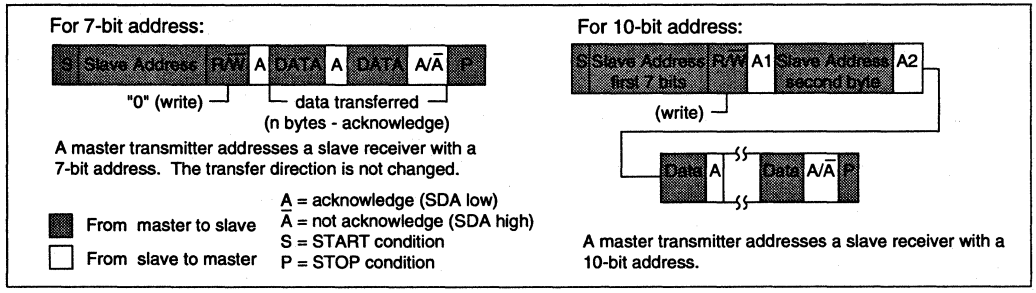


FIGURE 11-13: MASTER-RECEIVER SEQUENCE

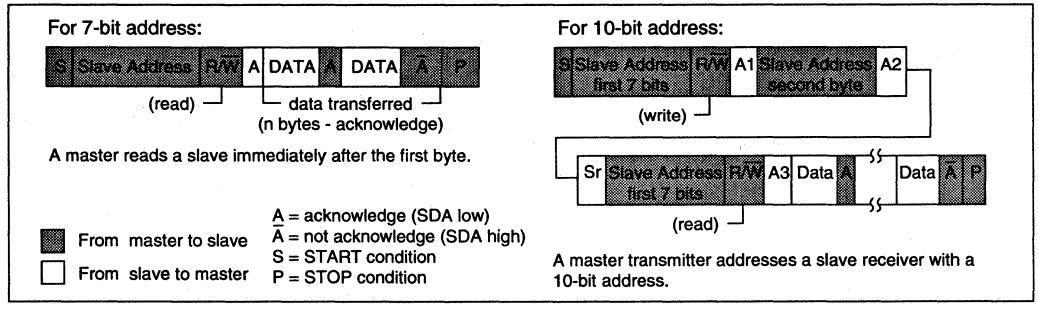
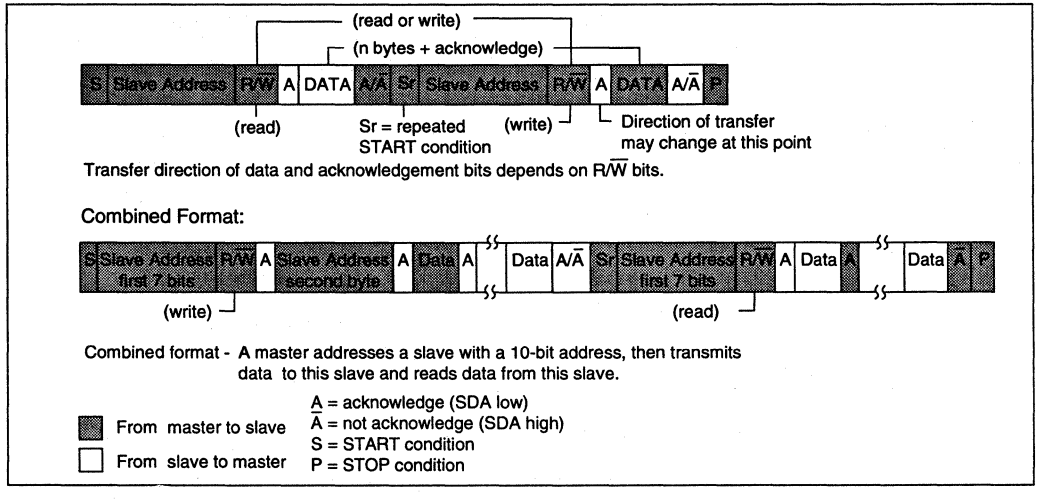


FIGURE 11-14: COMBINED FORMAT



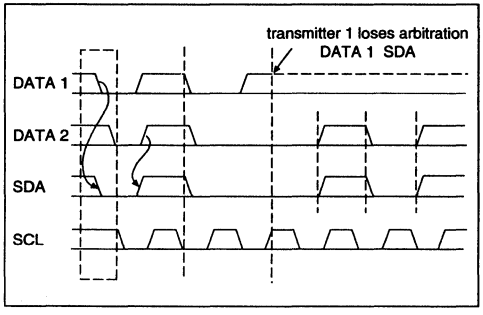
11.2.4 Multi-master

The I²C protocol allows a system to have more than one master. This is called multi-master. When two or more masters try to transfer data at the same time, arbitration and synchronization occur.

11.2.4.1 ARBITRATION

Arbitration takes place on the SDA line, while the SCL line is high. The master which transmits a high when the other master transmits a low loses arbitration (see Figure 11-15), and turns off its data output stage. A master which lost arbitration can generate clock pulses until the end of the data byte where it lost arbitration. When the master devices are addressing the same device, arbitration continues into the data.

FIGURE 11-15: MULTI-MASTER ARBITRATION (2 MASTERS)



Masters that also incorporate the slave function, and have lost arbitration must immediately switch over to slave-receiver mode. This is because the winning master-transmitter may be addressing it.

Arbitration is not allowed between:

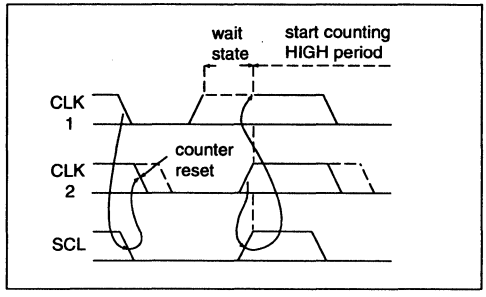
- A repeated START condition
- A STOP condition and a data bit
- A repeated START condition and a STOP condition

Care needs to be taken to ensure that these conditions do not occur.

11.2.4.2 CLOCK SYNCHRONIZATION

Clock synchronization occurs after the devices have started arbitration. This is performed using a wired-AND connection to the SCL line. A high to low transition on the SCL line causes the concerned devices to start counting off their low period. Once a device clock has gone low, it will hold the SCL line low until its SCL high state is reached. The low to high transition of this clock may not change the state of the SCL line, if another device clock is still within its low period. The SCL line is held low by the device with the longest low period. Devices with shorter low periods enter a high wait-state, until the SCL line comes high. When the SCL line comes high, all devices start counting off their high periods. The first device to complete its high period will pull the SCL line low. The SCL line high time is determined by the device with the shortest high period. This is shown in Figure 11-16.

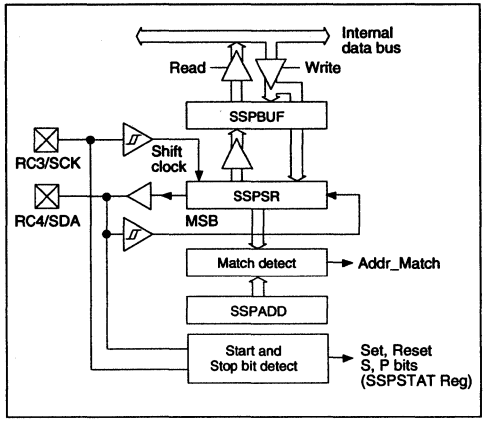
FIGURE 11-16: CLOCK SYNCHRONIZATION



11.3 SSP I²C Operation

The SSP module in I²C mode fully implements all slave functions, and provides support in hardware to facilitate software implementations of the master functions. The SSP module implements the standard and fast mode specifications as well as 7-bit and 10-bit addressing. Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits. A block diagram of the SSP module in I²C mode is shown in Figure 11-17. The SSP module functions are enabled by setting the SSP Enable (SSPEN) bit (SSPCON<5>).

FIGURE 11-17: SSP BLOCK DIAGRAM (I²C MODE)



The SSP module has five registers for I²C operation. These are the:

- SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive / Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) - Not directly accessible
- Address Register (SSPADD)

The SSPCON register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allows one of the following I²C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with master-mode support
- I²C Slave mode (10-bit address), with master-mode support
- I²C Master mode, slave is idle

Selection of any I²C mode and with the SSPEN bit set, forces the SCL and SDA pins to be open collector, provided these pins are set to inputs through the TRISC bits.

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START or STOP bit, specifies if the received byte was data or address, if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer. The SSPSTAT register is read only.

The SSPBUF is the register to which transfer data is written to or read from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF and the SSPIF is set. If another complete byte is received before the SSPBUF is read, a receiver overflow has occurred and the SSPOV bit (SSPCON<6> is set.

The SSPADD register holds the slave address. In 10-bit mode, the user needs to write the high byte of the address (1 1 1 1 0 A9 A8 0). Following the high byte address match, the low byte of the address needs to be loaded (A7 - A0).

11.3.1 Slave Mode

In slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer from an address match is received, the hardware automatically will generate the acknowledge ($\overline{ACK}$) pulse, and then load the SSPBUF with the received value in the SSPSR.

There are certain conditions that will cause the SSP module not to give this $\overline{ACK}$ pulse. These are if either (or both):

- The Buffer Full (BF) bit was set before the transfer was received.
- The Overflow (SSPOV) bit was set before the transfer was received.

In this case, the SSPSR value is not loaded into the SSPBUF, but the SSPIF bit is set. Table 11-3 shows what happens when a data transfer byte is received, given the status of the BF and SSPOV bits. The shaded boxes shows the condition where user software did not properly clear the overflow condition. The BF flag is cleared by reading the SSPBUF register while the SSPOV bit is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the I^2C specification as well as the requirement of the SSP module is shown in timing specifications #90 and 91.

11.3.1.1 ADDRESSING

Once the SSP module has been enabled, The SSP waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR. All incoming bits are sampled with the rising edge of the clock (SCL) line. The SSPSR<7:1> is compared to the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following things happen:

- SSPSR loaded into SSPBUF
- Buffer Full (BF) bit is set
- $\overline{ACK}$ pulse is generated
- SSP Interrupt Flag (SSPIF) is set (interrupt is generated if enabled) - on falling edge of ninth SCL pulse

In 10-bit address mode, two address bytes need to be received by the slave (see Figure 11-9). The five Most Significant bits (MSbs) of the first address byte, specify if this is a 10-bit address. The $R/\overline{W}$ bit (bit 0) must specify a write, so the slave device will receive the second address byte. For a 10-bit address the first byte would equal '1 1 1 1 0 A9 A8 0', where A9 and A8 are the two MSbs of the address. The sequence of events for 10-bit address are as follows, with steps 7-9 for slave-transmitter:

1. Receive first (high) byte of Address (SSPIF, BF and UA are set)
2. Update SSPADD with second (low) byte of Address (clears UA and releases SCL line)
3. Read SSPBUF (clears BF) and clear SSPIF
4. Receive second (low) byte of Address (SSPIF, BF and UA are set)
5. Update SSPADD with first (high) byte of Address (clears UA, if match releases SCL line)
6. Read SSPBUF (clears BF) and clear SSPIF
7. Receive Repeated START condition
8. Receive first (high) byte of Address (SSPIF and BF are set)
9. Read SSPBUF (clears BF) and clear SSPIF

TABLE 11-3: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received				
BF	SSPOV	SSPSR→SPBUF	Generate $\overline{ACK}$ Pulse	Set SSPIF bit (SSP Interrupt if Enabled)
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

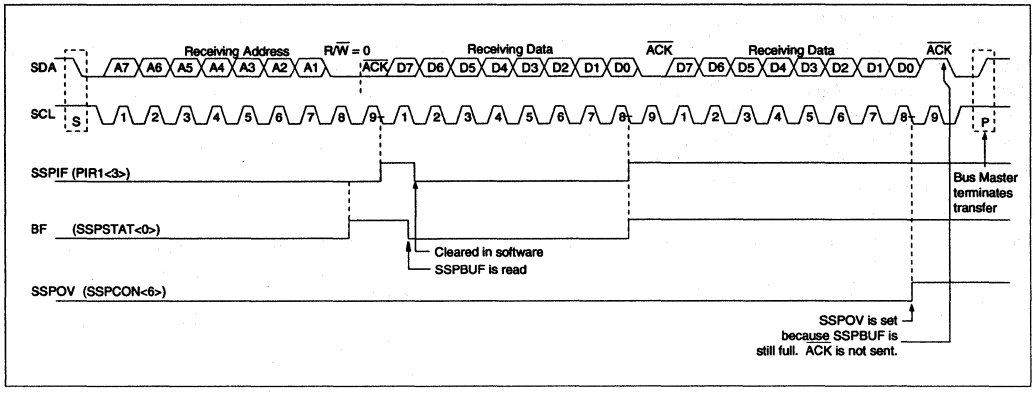
11.3.1.2 RECEPTION

When the R/$\overline{W}$ bit of the address byte is clear and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF.

When the address byte overflow condition exists then no acknowledge ($\overline{ACK}$) pulse is given. An overflow condition is defined as either the BF bit (SSPSTAT<0>) is set or the SSPOV bit (SSPCON<6>) is set.

A SSPIF interrupt is generated for each data transfer byte. The SSPIF bit must be cleared in software, and the SSPSTAT register is used to determine the status of the byte.

FIGURE 11-18: I²C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



11.3.1.3 TRANSMISSION

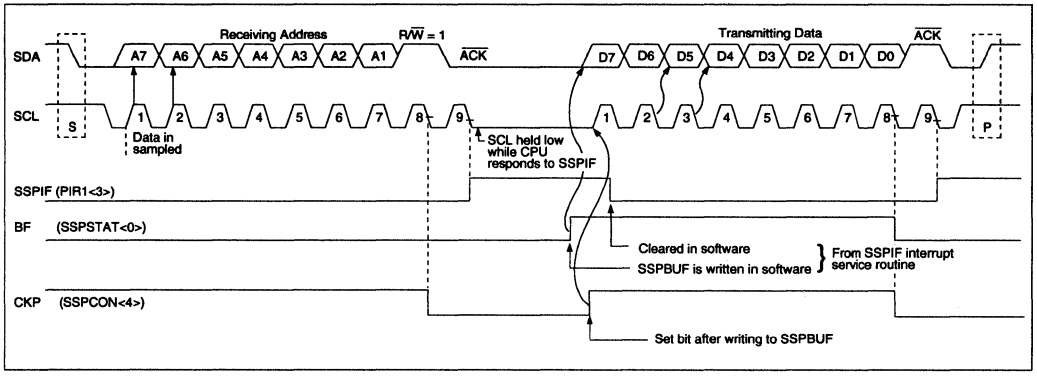
When the R/$\overline{W}$ bit of the address byte is set and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF. The $\overline{ACK}$ pulse will be sent on the ninth bit, and the SCL pin is held low. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then the SCL pin should be enabled by setting the CKP bit (SSPCON<4>). The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (see Figure 11-19).

A SSPIF interrupt is generated for each data transfer byte. The SSPIF bit must be cleared in software, and the SSPSTAT register is used to determine the status of the byte. The SSPIF bit is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the $\overline{ACK}$ pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not $\overline{ACK}$), then the data transfer is complete. The slave then monitors for another occurrence of the START bit. If the SDA line was low ($\overline{ACK}$), the transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then the SCL pin should be enabled by setting the CKP bit (SSPCON<4>).

2

FIGURE 11-19: I²C WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



11.3.2 Master Mode

Master mode of operation is supported by interrupt generation on the detection of the START and STOP conditions. The STOP (P)and START (S) bits are cleared from a reset or when the SSP module is disabled. Control of the I²C bus may be taken when the P-bit is set, or the bus is idle and both the S- and P-bits are cleared.

In master mode the SCL and SDA lines are manipulated by changing the corresponding TRISC<4:3> bit(s) to an output (cleared). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a "1" data bit must have the TRISC<4> bit set (input) and a "0" data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit.

The following events will cause the SSP Interrupt Flag (SSPIF) to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- Data transfer byte transmitted/received

Master mode of operation can be done with either the slave mode idle (SSPM3 - SSPM0 = 1011) or with the slave active. When both master and slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

11.3.3 Multi-master Mode

In multi-master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P)and START (S) bits are cleared from a reset or when the SSP module is disabled. Control of the I²C bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are cleared. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the stop condition occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, the device may be being addressed. If addressed an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

TABLE 11-4: REGISTERS ASSOCIATED WITH I²C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
13	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register							
93	SSPADD	Synchronous Serial Port (I²C mode) Address Register							
14	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
94	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF

Legend — = Unimplemented locations, Read as '0'
Note: Shaded boxes are not used by the SSP module in I²C mode.

FIGURE 11-20: OPERATION OF THE I²C MODULE IN IDLE_MODE, RCV_MODE OR XMIT_MODE

```
IDLE_MODE (7-bit):
if (Addr_match)                 {   Set interrupt;
                                    if (R/W = 1)   {Send ACK = 0;
                                                    set XMIT_MODE;
                                                   }
                                    else if (R/W = 0) set RCV_MODE;
                                }
```

```
RCV_MODE:
if ((SSPBUF=Full) OR (SSPOV = 1))
        {Set SSPOV;
        Do not acknowledge;
        }
else    { transfer SSPSR → SSPBUF;
        send ACK = 0;
        }
Receive 8-bits in SSPSR;
Set interrupt;
```

```
XMIT_MODE:
While ((SSPBUF = Empty) AND (CKP=0)) Hold SCL Low;
Send byte;
Set interrupt;
if (ACK Received = 1)           {End of transmission;
                                Go back to IDLE_MODE;
                                }
else if (ACK Received = 0)      Go back to XMIT_MODE;
```

```
IDLE_MODE (10-Bit):
If (High_byte_addr_match AND (R/W = 0))
    { PRIOR_ADDR_MATCH = FALSE;
      Set interrupt;
      if ((SSPBUF = Full) OR ((SSPOV = 1))
            { Set SSPOV;
              Do not acknowledge;
            }
      else  { Set UA = 1;
              Send ACK = 0;
              While (SSPADD not updated) Hold SCL low;
              Clear UA = 0;
              Receive Low_addr_byte;
              Set interrupt;
              Set UA = 1;
              If (Low_byte_addr_match)
                    { PRIOR_ADDR_MATCH = TRUE;
                      Send ACK = 0;
                      while (SSPADD not updated) Hold SCL low;
                      Clear UA = 0;
                      Set RCV_MODE;
                    }
            }
    }
else if (High_byte_addr_match AND (R/W = 1)
            { if (PRIOR_ADDR_MATCH)
                    { send ACK = 0;
                      set XMIT_MODE;
                    }
              else PRIOR_ADDR_MATCH = FALSE;
            }
```

12.0 SPECIAL FEATURES OF THE CPU

What sets apart a microcontroller from other processors are special circuits to deal with the needs of real time applications. The PIC16CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

1. OSC selection
2. Reset
   - Power-On Reset (POR)
   - Power-Up Timer (PWRT)
   - Oscillator Start-Up Timer (OST)
3. Interrupts
4. Watchdog Timer (WDT)
5. SLEEP
6. Code protection
7. In-circuit serial programming

The PIC16CXX has a Watchdog Timer which can be shut off only through EPROM fuses. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the oscillator start-up timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

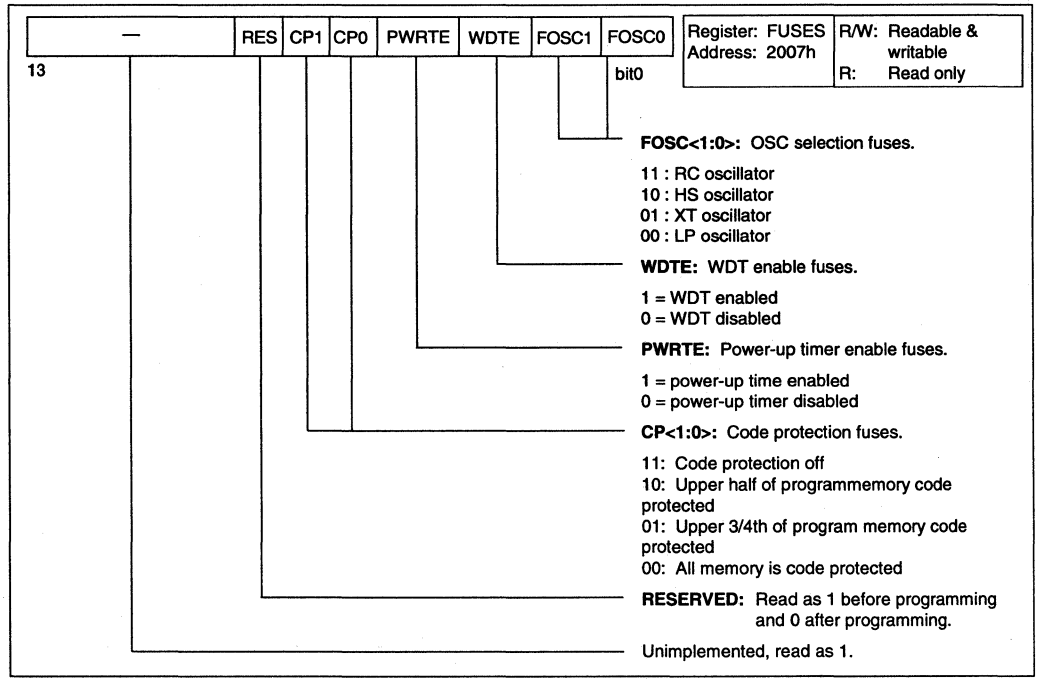
The SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer timeout or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of EPROM configuration bits (fuses) are used to select various options.

12.1 Configuration Fuses

The PIC16CXX has six configuration fuses which are EPROM bits. These fuses can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed during programming.

FIGURE 12-1: CONFIGURATION WORD



12.2 Oscillator Configurations

12.2.1 OSCILLATOR TYPES

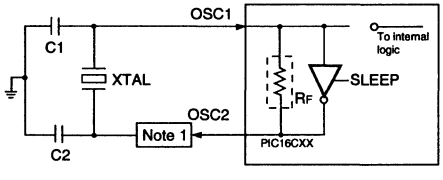
The PIC16CXX can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal
- HS High Speed Crystal
- RC Resistor/Capacitor

12.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 12-2). The PIC16CXX Oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin. This is shown in Figure 12-3.

FIGURE 12-2: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Tables 12-1 and 12-2 for recommended values of C1 and C2.

Note1: A series resistor may be required for AT strip cut crystals.

FIGURE 12-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP OSC CONFIGURATION)

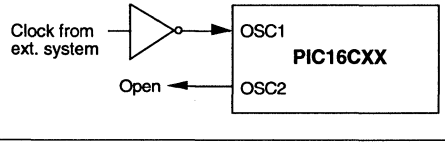


TABLE 12-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	150 - 330 pF
	2.0 MHz	20 - 330 pF
	4.0 MHz	20 - 330 pF
HS	8.0 MHz	20 - 200 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 12-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz§	15 pF	15 pF
	100 KHz	15 pF	15 pF
	200 KHz	0 - 15 pF	0 - 15 pF
XT	100 KHz	15 - 30 pF	200 - 300 pF
	200 KHz	15 - 30 pF	100 - 200 pF
	455 KHz	15 - 30 pF	15 - 100 pF
	1 MHz	15 - 30 pF	15 - 30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

§ For V_{DD} > 4.5V, C1 = C2 ≃ 30pf is recommended.

2

12.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance, or one with parallel resonance.

Figure 12-4 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 12-4: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

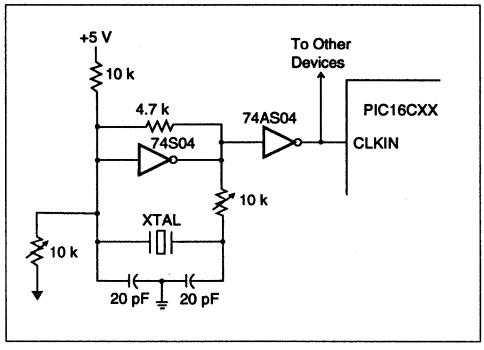
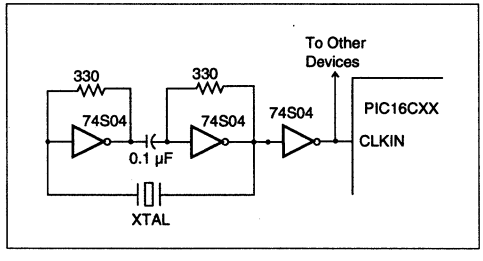


Figure 12-5 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330-Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 12-5 : EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



12.2.4 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 12-6 shows how the R/C combination is connected to the PIC16CXX. For Rext values below 2.2 kOhm, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 kOhm and 100 kOhm.

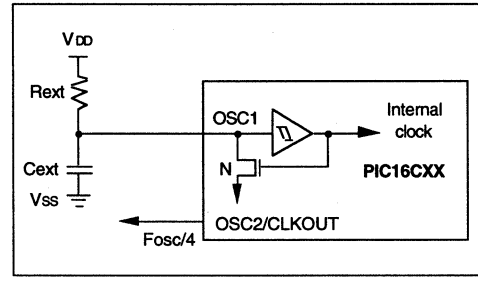
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 17.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 17.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-2 for waveform).

FIGURE 12-6: RC OSCILLATOR MODE



12.3 Reset

The PIC16CXX differentiates between various kinds of reset:

a) Power-On Reset (POR)
b) $\overline{MCLR}$ Reset during normal operation
c) $\overline{MCLR}$ reset during SLEEP
d) WDT time-out reset during normal operation
e) WDT time-out reset during SLEEP

Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on power-on reset (POR), on $\overline{MCLR}$ or WDT reset during normal operation and on $\overline{MCLR}$ reset during SLEEP. They are not affected by a WDT reset during SLEEP, since this reset is viewed as the resumption of normal operation. $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations as indicated in Table 12-4. These bits are used in software to determine the nature of reset. See Table 12-6 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 12-7.

12.4 Power-On Reset (POR), Power-Up-Timer (PWRT) and Oscillator Start-up Timer (OST)

12.4.1 Power-On Reset (POR)

A Power-On Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.6V - 1.8V). To take advantage of the POR, just tie $\overline{MCLR}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-On Reset. A minimum rise time for VDD is required. See Electrical Specifications for details.

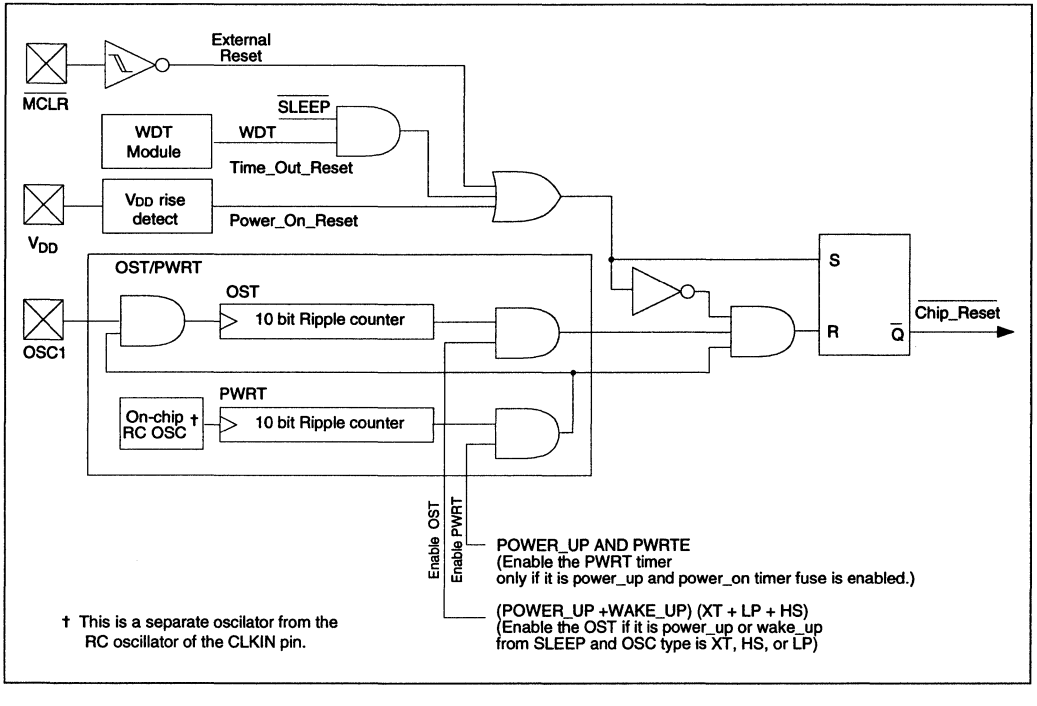
The POR circuit does not produce internal reset when VDD declines.

12.4.2 POWER-UP TIMER (PWRT)

The Power-Up Timer provides a fixed 72ms time-out on power-up only from POR. The power-up timer operates on an internal RC oscillator. The chip is kept in reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration fuse, PWRTE can enable (if set) or disable (if cleared or programmed) the power-up timer.

The Power-Up Time delay will vary from chip to chip and due to VDD and temperature. See the DC Parameters section for details.

FIGURE 12-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



12.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-Up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This guarantees that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-On Reset or wake-up from SLEEP.

12.4.4 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and PWRTE fuse status. For example, in RC mode with PWRTE fuse cleared (PWRT disabled), there will be no time-out at all. Figures 12-8 to 12-10 depict time-out sequences.

TABLE 12-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power up		Wake up from SLEEP
	PWRTE = 1	PWRTE = 0	
XT, HS, LP	72 ms + 1024 tosc	1024 tosc	1024 tosc
RC	72 ms	–	–

Since the time-outs occur from POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately (see Figure 12-9). This is useful for testing purposes or to synchronize more than one PIC16CXX device operating in parallel.

Table 12-5 shows the reset conditions for some special registers, while Table 12-6 shows the reset conditions for all the registers.

12.4.1 POWER CONTROL/STATUS REGISTER (PCON)

The power control/status register, PCON (address 8Eh) has only one bit.

Bit1 is $\overline{POR}$ (Power-on-reset). It is cleared on power-on-reset and unaffected otherwise. The user must set this bit following power-on-reset. On a subsequent reset if $\overline{POR}$ is 'cleared, it will indicate that a Power-On Reset must have occured (V_{DD} may have gone too low).

TABLE 12-4: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{TO}$	$\overline{PD}$	
0	1	1	Power-on-reset
0	0	X	Illegal, $\overline{TO}$ is set on POR
0	X	0	Illegal, $\overline{PD}$ is set on POR
1	0	1	WDT reset during normal operation
1	0	0	WDT timeout wakeup from SLEEP
1	1	1	$\overline{MCLR}$ reset during normal operation
1	1	0	$\overline{MCLR}$ reset during SLEEP or interrupt wake-up from SLEEP

TABLE 12-5: RESET CONDITION FOR SPECIAL REGISTERS

	PCL Addr: 02h	STATUS Addr: 03h	PCON Addr: 8Eh
Power-On Reset	000h	0001 1xxx	---- --0-
$\overline{MCLR}$ reset during normal operation	000h	0001 1uuu	---- --u-
$\overline{MCLR}$ reset during SLEEP	000h	0001 0uuu	---- --u-
WDT reset during normal operation	000h	0000 1uuu	---- --u-
WDT during SLEEP	PC + 1	uuu0 0uuu	---- --u-
Interrupt wake-up from SLEEP	PC + 1 (1)	uuu1 0uuu	---- --u-

Legend: u = unchanged
x = unknown
- = unimplemented bit, reads as '0'

Notes: 1. When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 12-6: RESET CONDITION FOR REGISTERS

Register	Address	• Power-on Reset	• $\overline{MCLR}$ Reset during: - normal operation - SLEEP • WDT timeout during normal operation	• Wake up from SLEEP through interrupt • Wake up from SLEEP through WDT timeout
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	-	-	-
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	02h	0000h	0000h	PC + 1 (2)
STATUS	03h	0001 1xxx	000? ?uuu (3)	uuu? ?uuu (3)
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--xx xxxx	--uu uuuu	--uu uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTE	09h	---- -xxx	---- -uuu	---- -uuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 0000	uuuu uuuu(1)
PIR1	0Ch	0--- 0000	0--- 0000	u--- uuuu(1)
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	--00 0000	--uu uuuu	--uu uuuu
TMR2	11h	xxxx xxxx	uuuu uuuu	uuuu uuuu
T2CON	12h	-000 0000	-000 0000	-uuu uuuu
SSPBUF	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	14h	0000 0000	0000 0000	uuuu uuuu
CCPR1L	15h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	17h	--00 0000	--00 0000	--uu uuuu
INDF	80h	-	-	-
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
PC	82h	0000h	0000h	PC + 1
STATUS	83h	0001 1xxx	000? ?uuu (3)	uuu? ?uuu (3)
FSR	84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
TRISC	87h	1111 1111	1111 1111	uuuu uuuu
TRISD	88h	1111 1111	1111 1111	uuuu uuuu
TRISE	89h	0000 -111	0000 -111	uuuu -uuu
PCLATH	8Ah	---0 0000	---0 0000	---u uuuu
INTCON	8Bh	0000 000x	0000 0000	uuuu uuuu(1)
PIE1	8Ch	0--- 0000	0--- 0000	u--- uuuu
PCON	8Eh	---- --0-	---- --1-	---- --1-
PR2	92h	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPADD	93h	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	94h	--00 0000	--00 0000	--uu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', ? = value depends on condition

Notes:
1. One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).
2. When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
3. See Table 12-5 for reset value for specific condition.

FIGURE 12-8 : TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD): Case 1

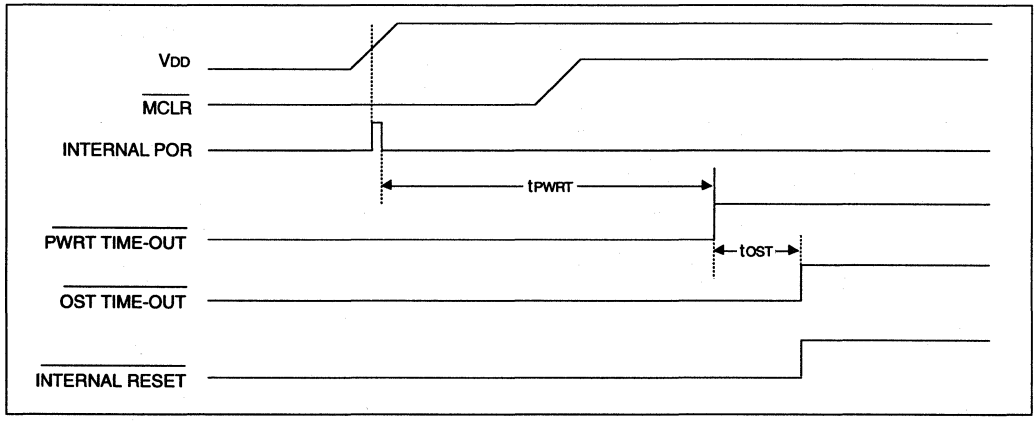


FIGURE 12-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD): Case 2

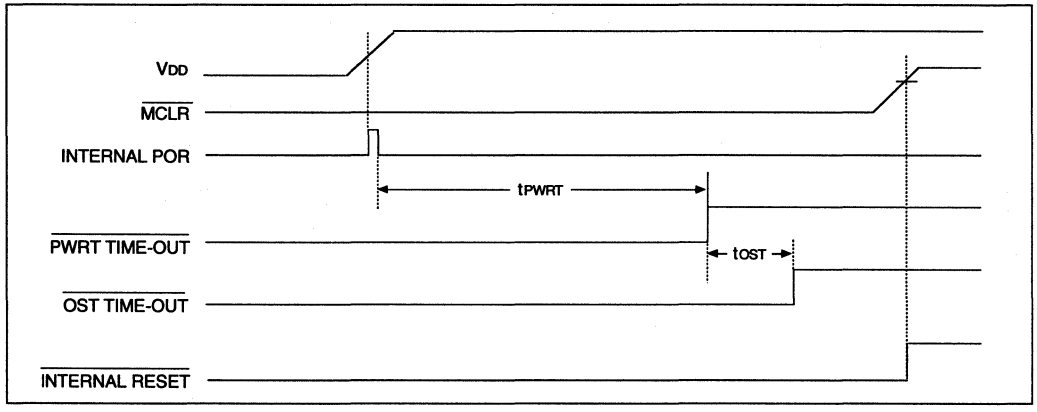


FIGURE 12-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD)

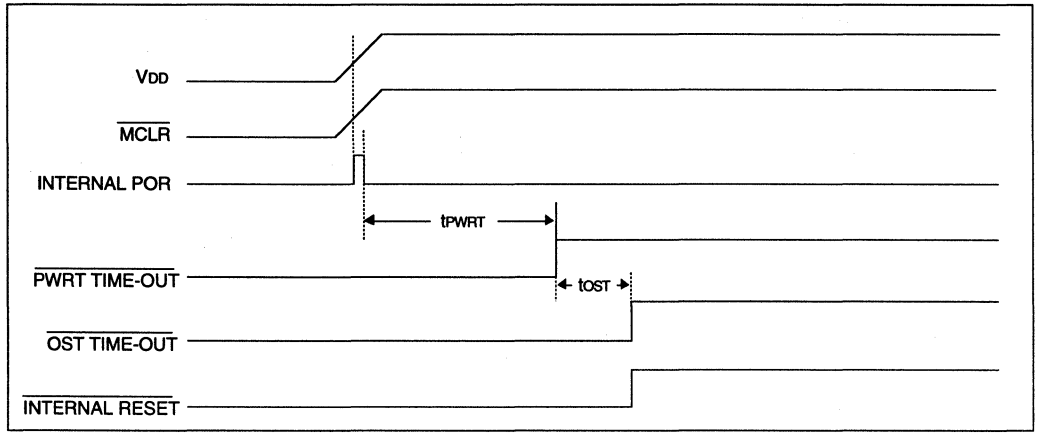
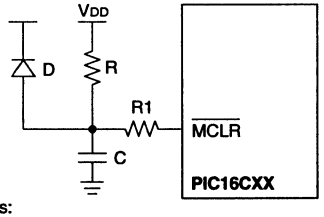
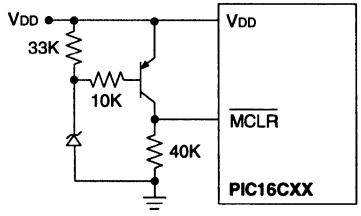


FIGURE 12-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



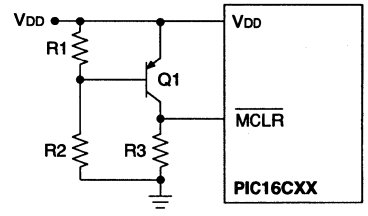
Notes:
1. External power-on reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40KΩ is recommended to make sure that voltage drop across R does not exceed 0.2V (max leakage current spec on $\overline{MCLR}$ pin is 5μA). A larger voltage drop will degrade VIH level on $\overline{MCLR}$ pin.
3. R1 = 100Ω to 1KΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$ pin breakdown due to ESD or EOS.

FIGURE 12-12: BROWN-OUT PROTECTION CIRCUIT 1



Notes:
1. This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

FIGURE 12-13: BROWN-OUT PROTECTION CIRCUIT 2



Notes:
1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V.$$

12.5 Interrupts

The PIC16C64 has eight sources of interrupt:

- External interrupt RB0/INT
- RTCC timer/counter overflow interrupt
- PortB change interrupts (pins RB<7:4>)
- Timer1 overflow interrupt
- Timer2 interrupt
- CCP1 interrupt
- Sync serial port interrupt
- Microprocessor port read/write interrupt

The interrupt control register (INTCON, addr 0Bh) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. GIE is cleared on reset.

The `RETFIE` instruction allows user to return from interrupt and enable interrupt at the same time.

The INT pin interrupt, the RB port change interrupt and the RTCC overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the special register PIR1 (0Ch). The corresponding interrupt enable bits are contained in special registers PIE1 (8Ch).

When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

Note 1: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

Note 2: If an interrupt occurs while the Global Interrupt Enable (GIE) bit is being cleared, the GIE bit may unintentionally be re-enabled by the user's Interrupt Service Routine (the `RETFIE` instruction). The events that would cause this to occur are:

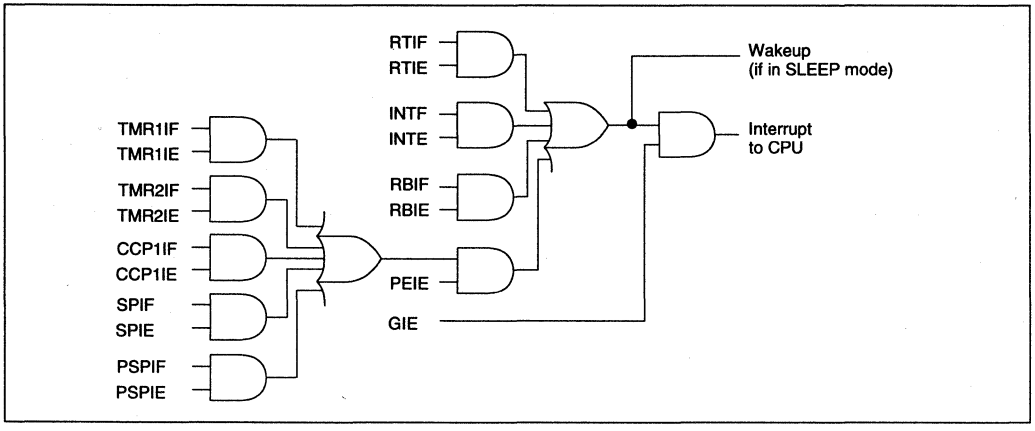
1. An instruction clears the GIE bit while an interrupt is acknowledged.
2. The program branches to the Interrupt vector and executes the Interrupt Service Routine.
3. The Interrupt Service Routine completes with the execution of the `RETFIE` instruction. This causes the GIE bit to be set (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.

The method to ensure that interrupts are globally disabled is:

1. Ensure that the GIE bit was cleared by the instruction, as shown in the following code:

```
LOOP   BCF   INTCON, GIE   ; Disable Global
                           ;   Interrupts
       BTFSC INTCON, GIE   ; Global Interrupts
                           ;   Disabled?
       GOTO  LOOP          ; NO, try again
       :                   ; Yes, continue
                           ;   with program
                           ;   flow
```

FIGURE 12-14: INTERRUPT LOGIC



12.5.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake up the processor from SLEEP, if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 12.8 for details on SLEEP and Figure 12-16 for timing of wake-up from SLEEP through INT interrupt.

12.5.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the TMR0 module, see Section 7.0.

12.5.3 PORT RB INTERRUPT

An input change on PORTB <7:4> will set the RBIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the RBIE (INTCON<4>) bit. For operation of PORTB, see Section 5.2.

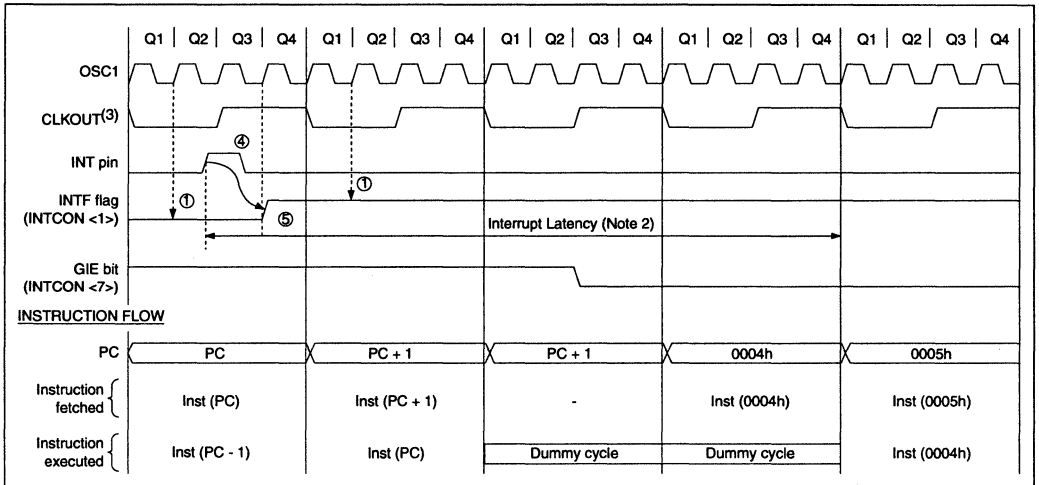
12.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt e.g. W register and status register. This will have to be implemented in software.

EXAMPLE 12-1: SAVING W REGISTER AND STATUS IN RAM:

```
push:   movwf    temp_w        ;Saving Values
        swapf    STATUS,W      ;
        movwf    temp_stat     ;
        :                      ;Interrupt
        :                      ; Service Routine
pop:    swapf    temp_stat,W   ;Restoring
                               ; Values
        movwf    STATUS        ;
        swapf    temp_w, F     ;Do not want to
        swapf    temp_w, W     ;  affect the
                               ;  z-bit
```

FIGURE 12-15: INT PIN INTERRUPT TIMING



Notes:
1. INTF flag is sampled here (every Q1)
2. Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time.
   Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3. CLKOUT is available only in RC oscillator mode.
4. For minimum width spec of INT pulse, refer to AC specs.
5. INTF is enabled to be set anytime during the Q4-Q1 cycles.

12.7 Watchdog Timer (WDT)

The watchdog timer is realized as a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT timeout generates a device RESET. If the device is in SLEEP mode, a WDT timeout causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration fuse WDTE as a '0' (Section 12.1).

12.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a watchdog timer time-out.

12.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

FIGURE 12-16: WATCHDOG TIMER BLOCK DIAGRAM

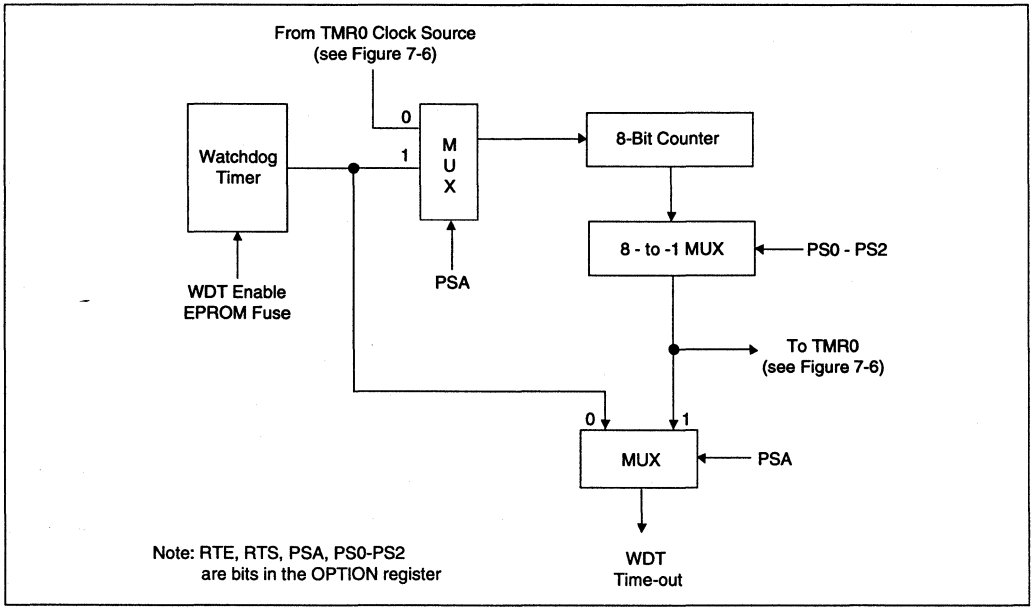


FIGURE 12-17: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007	Config. Fuses	—	—	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
81	OPTION	RBPU	INTEDG	RTS	RTE	PSA	PS2	PS1	PS0

12.8 Power-Down Mode (SLEEP)

The Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{PD}$ bit in the STATUS register is cleared, the $\overline{TO}$ bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low, or hi-impedance).

For lowest curent consumption in this mode, all I/O pins should be either at V_{DD}, or V_{SS}, with no external circuitry drawing current from the I/O pin. I/O pins that are hi-impedence inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC input should also be at V_{DD} or V_{SS} for lowest current consumption. The contribution from on chip pull-ups on PortB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (V_{IHMC}).

It should be noted that a RESET generated by a WDT time-out does not drive $\overline{MCLR}$ pin low.

14.8.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. External reset input on $\overline{MCLR}$ pin
2. Watchdog timer time-out reset (if WDT was enabled)
3. Interrupt from INT pin, RB port change, TMR0 overflow, or some Peripheral Interrupts.

The following peripheral interrupts can wake-up from SLEEP:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. SSP Start/Stop bit detect interrupt.
3. CCP capture mode interrupt.
4. Slave port read or write.

Other peripherals can not generate interrupts since during SLEEP, no on-chip Q clocks are present.

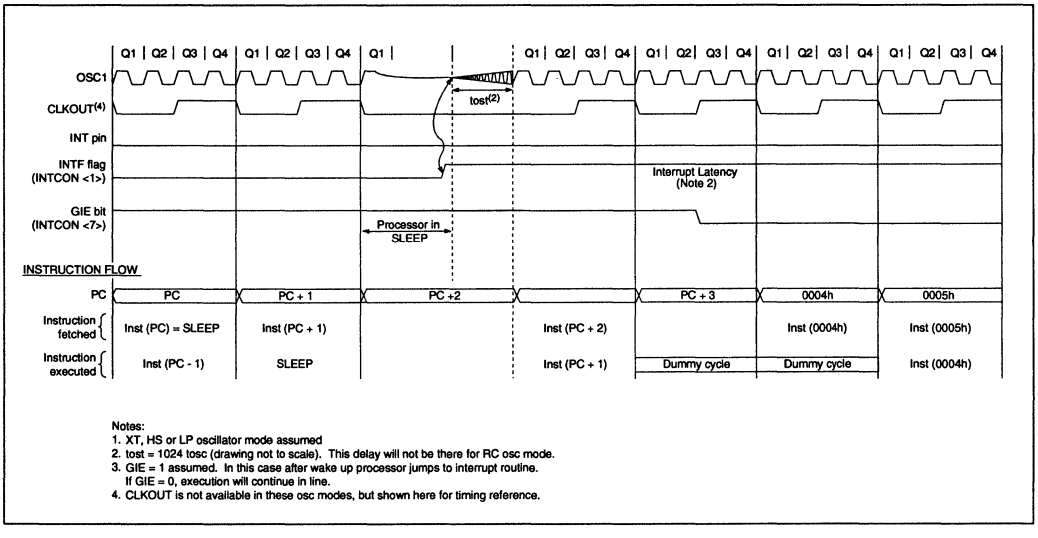
The first event will cause a device reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. $\overline{PD}$ bit, which is set on power-up is cleared when SLEEP is invoked. $\overline{TO}$ bit is cleared if WDT time-out occurred (and caused wake-up).

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and the branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

Note: If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake from sleep.

The WDT is cleared when the device wakes-up from sleep, regardless of the source of wake-up.

FIGURE 12-18: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Notes:
1. XT, HS or LP oscillator mode assumed
2. tost = 1024 tosc (drawing not to scale). This delay will not be there for RC osc mode.
3. GIE = 1 assumed. In this case after wake up processor jumps to interrupt routine. If GIE = 0, execution will continue in line.
4. CLKOUT is not available in these osc modes, but shown here for timing reference.

12.9 Code Protection

The code in the program memory can be protected by blowing the code protect fuses (CP<1:0>).

When code protected, the contents of the program memory cannot be read out in a way that the program code can be reconstructed.

In code-protected mode, the configuration word (2007h) will not be scrambled, allowing reading of all fuses.

12.9.1 CODE PROTECTION FUSES:

The PIC16/17 microcontroller code protection scheme has been enhanced. These enhancements allow the user to selectively code protect portions of the program memory. The two code protect fuses (CP<1:0>) allow the selection of the following code protection mappings:

11 Program memory not code protected
01 Upper 3/4 of program memory code protected (200h - 7FF)
10 Upper 1/2 of program memory code protected (400h - 7FF)
00 Entire program memory code protected

Any word of a protected memory section will read out a scrambled version as shown in Figure 12-17:

FIGURE 12-19: PROTECTED MEMORY READ FORMAT

13							7	6							0
0	0	0	0	0	0	0		b6	b5	b4	b3	b2	b1	b0	

where b0 = XNOR of bit0 and bit7 of the program memory location.
b1 = XNOR of bit1 and bit8 of the programmemory location.
•
•
•
b6 = XNOR of bit6 and bit13 of the program.

The configuration word is not code protected, and therefore no scrambling is done. Unprotected segments read normally. Once the program memory location(s) have been code protected, those memory locations can not be further programmed.

12.9.2 VERIFYING A CODE-PROTECTED PART

When code protected, verifying any program memory location will read a scrambled output which looks like "0000000xxxxxxx" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

1. First, program and verify a good device without code protecting it.
2. Next, blow its code protection fuse and then load its contents in a file.
3. Verify any code-protected PIC16C64 against this file.

12.10 In-Circuit Serial Programming

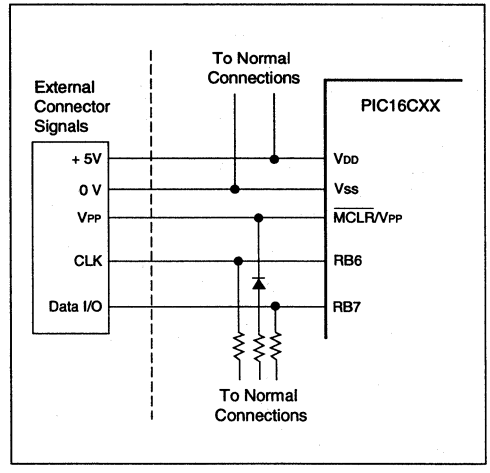
The PIC16CXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and date and three other lines for power, ground and programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low while raising the MCLR (Vpp) pin from Vil to Vihh. RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are schmidt trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program date are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X Programming Specifications (Literature #DS30153).

A typical in-system serial programming connection is shown in Figure 12-18.

FIGURE 12-20: TYPICAL IN-SYSTEM SERIAL PROGRAMMING CONNECTION



13.0 INSTRUCTION SET SUMMARY

Each PIC16CXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 13-2 lists byte-oriented, bit-oriented, and literal and control operations. Table 13-1 shows the opcode field descriptions.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which file register is to be utilized by the instruction.

The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an 8- or 11-bit constant or literal value.

TABLE 13-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8 bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
PCLATH	Program Counter High Latch
GIE	Global Interrupt Enable Bit
WDT	Watchdog Timer Counter
$\overline{TO}$	Time-out Bit
$\overline{PD}$	Power-down Bit
dest	Destination either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term

The instruction set is highly orthogonal and is grouped into three basic categories:

- Byte oriented operations
- Bit oriented operations
- Literal and control operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Table13-2 lists the instructions recognized by the MPASM assembler.

Figure 13-1 shows the three general formats that the instructions can have.

Note: To maintain upward compatibility with future PIC16CXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexidecimal number:

0xhh

where h signifies a hexidecimal digit.

FIGURE 13-1: GENERAL FORMAT FOR INSTRUCTIONS

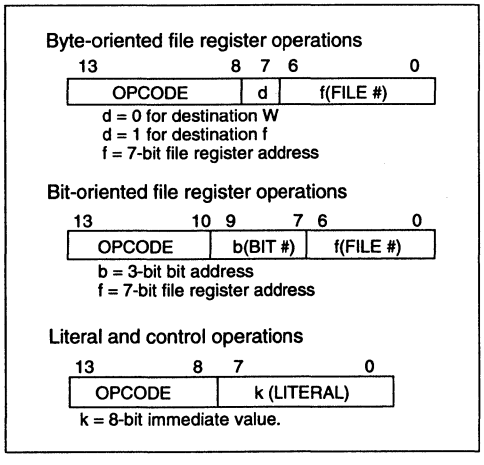


TABLE 13-2: INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode msb	lsb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS							
ADDWF	f, d	Add W and f	1	00 0111	dfff ffff	C, DC, Z	1, 2
ANDWF	f, d	AND W and f	1	00 0101	dfff ffff	Z	1, 2
CLRF	f	Clear f	1	00 0001	1fff ffff	Z	2
CLRW	-	Clear W	1	00 0001	0xxx xxxx	Z	
COMF	f, d	Complement f	1	00 1001	dfff ffff	Z	1, 2
DECF	f, d	Decrement f	1	00 0011	dfff ffff	Z	1, 2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00 1011	dfff ffff		1, 2, 3
INCF	f, d	Increment f	1	00 1010	dfff ffff	Z	1, 2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00 1111	dfff ffff		1, 2, 3
IORWF	f, d	Inclusive OR W and f	1	00 0100	dfff ffff	Z	1, 2
MOVF	f, d	Move f	1	00 1000	dfff ffff	Z	1, 2
MOVWF	f	Move W to f	1	00 0000	1fff ffff		
NOP	-	No Operation	1	00 0000	0xx0 0000		
RLF	f, d	Rotate left f through carry	1	00 1101	dfff ffff	C	1, 2
RRF	f, d	Rotate right f through carry	1	00 1100	dfff ffff	C	1, 2
SUBWF	f, d	Subtract W from f	1	00 0010	dfff ffff	C, DC, Z	1, 2
SWAPF	f, d	Swap halves f	1	00 1110	dfff ffff		1, 2
XORWF	f, d	Exclusive OR W and f	1	00 0110	dfff ffff	Z	1, 2
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF	f, b	Bit Clear f	1	01 00bb	bfff ffff		1, 2
BSF	f, b	Bit Set f	1	01 01bb	bfff ffff		1, 2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01 10bb	bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01 11bb	bfff ffff		3
LITERAL AND CONTROL OPERATIONS							
ADDLW	k	Add literal to W	1	11 111x	kkkk kkkk	C, DC, Z	
ANDLW	k	AND literal to W	1	11 1001	kkkk kkkk	Z	
CALL	k	Call subroutine	2	10 0kkk	kkkk kkkk		
CLRWDT	-	Clear watchdog timer	1	00 0000	0110 0100	$\overline{TO}$, $\overline{PD}$	
GOTO	k	Go to address	2	10 1kkk	kkkk kkkk		
IORLW	k	Inclusive OR literal to W	1	11 1000	kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11 00xx	kkkk kkkk		
RETFIE	-	Return from interrupt	2	00 0000	0000 1001		
RETLW	k	Return with literal in W	2	11 01xx	kkkk kkkk		
RETURN	-	Return from subroutine	2	00 0000	0000 1000		
SLEEP	-	Go into standby mode	1	00 0000	0110 0011	$\overline{TO}$, $\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11 110x	kkkk kkkk	C, DC, Z	
XORLW	k	Excl. OR literal to W	1	11 1010	kkkk kkkk	Z	

Notes: 1. When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1) the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2. If this instruction is executed on the TMR0 register (and, where applicable, d=1), the prescaler will be cleared if assigned to the TMR0.

3. If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

13.1 Instruction Descriptions

ADDLW Add Literal to W

Syntax: [*label*] ADDLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) + k → W

Status Affected: C, DC, Z

Encoding:

11	111X	kkkk	kkkk

Description: The contents of the W register are added to the 8-bit literal "k" and the result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ADDLW   0x15
```
Before Instruction
W = 0x10

After Instruction
W = 0x25

ANDLW AND Literal and W

Syntax: [*label*] ANDLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .AND. (k) → W

Status Affected: Z

Encoding:

11	1001	kkkk	kkkk

Description: The contents of W register are AND'ed with the 8-bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ANDLW   0x5F
```
Before Instruction
W = 0xA3

After Instruction
W = 0x03

ADDWF ADD W to f

Syntax: [*label*] ADDWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

00	0111	dfff	ffff

Description: Add the contents of the W register to register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
ADDWF   FSR, 0
```
Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0xD9
FSR = 0xC2

ANDWF AND W with f

Syntax: [*label*] ANDWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (W) .AND. (f) → dest

Status Affected: Z

Encoding:

00	0101	dfff	ffff

Description: AND the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
ANDWF   FSR, 1
```
Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0x17
FSR = 0x02

BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: 0 → f<b>

Status Affected: None

Encoding:

01	00bb	bfff	ffff

Description: Bit "b" in register "f" is reset to 0.

Words: 1

Cycles: 1

Example:
```
BCF     FLAG_REG, 7
```
Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47

BSF **Bit Set f**

Syntax: [*label*] BSF f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: 1 → f<b>

Status Affected: None

Encoding:

01	01bb	bfff	ffff

Description: Bit "b" in register "f" is set to 1.

Words: 1

Cycles: 1

Example:
```
BSF     FLAG_REG, 7
```
Before Instruction
FLAG_REG = 0x0A
After Instruction
FLAG_REG = 0x8A

BTFSC **Bit Test, skip if Clear**

Syntax: [*label*] BTFSC f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

01	10bb	bfff	ffff

Description: If bit 'b' in register 'f' is '0' then the next instruction is skipped.

If bit 'b' is '0', the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address HERE
After Instruction
if FLAG<1> = 0, PC = address TRUE
if FLAG<1> = 1, PC = address FALSE

BTFSS **Bit Test, skip if Set**

Syntax: [*label*] BTFSS f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

01	11bb	bfff	ffff

Description: If bit "b" in register "f" is "1" then the next instruction is skipped.

If bit '"b" is "0", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address HERE
After Instruction
if FLAG<1> = 0, PC = address FALSE
if FLAG<1> = 1,PC = address TRUE

CALL Subroutine Call

Syntax: [*label*] CALL k

Operands: 0 ≤ k ≤ 2048

Operation: (PC) + 1 → TOS,
k → PC<10:0>,
(PCLATH<4:3>) → PC<12:11>;

Status Affected: None

Encoding:

10	0kkk	kkkk	kkkk

Description: Subroutine call. First, return address (PC + 1) is pushed onto the stack. The eleven bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH (f03). CALL is a two-cycle instruction.

Words: 1

Cycles: 2

Example:
```
HERE    CALL    THERE
```
Before Instruction
PC = Address HERE
After Instruction
PC = Address THERE
TOS = Address HERE

CLRF Clear f

Syntax: [*label*] CLRF f

Operands: 0 ≤ f ≤ 127

Operation: 00h → f
1 → Z

Status Affected: Z

Encoding:

00	0001	1fff	ffff

Description: The contents of register "f" are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example:
```
CLRF    FLAG_REG
```
Before Instruction
FLAG_REG = 0x5A
After Instruction
FLAG_REG = 0x00
Z = 1

CLRW Clear W Register

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W)
1 → Z

Status Affected: Z

Encoding:

00	0001	0XXX	XXXX

Description: W registered is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example:
```
CLRW
```
Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

CLRWDT Clear Watchdog Timer

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0100

Description: CLRWDT instruction resets the watchdog timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example:
```
CLRWDT
```
Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescale = 0
$\overline{TO}$ = 0
$\overline{PD}$ = 0

COMF Complement f

Syntax: [*label*] COMF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: $\overline{(f)} \rightarrow$ (dest)

Status Affected: Z

Encoding:

00	1001	dfff	ffff

Description: The contents of register "f" are complemented. If "d" is 0 the result is stored in W. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
COMF    REG1, 0
```
Before Instruction
REG1 = 0x13

After Instruction
REG1 = 0x13
W = 0xEC

DECF Decrement f

Syntax: [*label*] DECF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f)-1 → (dest)

Status Affected: Z

Encoding:

00	0011	dfff	ffff

Description: Decrement register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
DECF    CNT, 1
```
Before Instruction
CNT = 0x01
Z = 0

After Instruction
CNT = 0x00
Z = 1

DECFSZ Decrement f, skip if 0

Syntax: [*label*] DECFSZ f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - 1 → d; skip if result = 0

Status Affected: None

Encoding:

00	1011	dfff	ffff

Description: The contents of register "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two -ycle instruction.

Words: 1

Cycles: 1 (2)

Example:
```
HERE    DECFSZ    CNT, 1
          GOTO      LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address `HERE`

After Instruction
CNT = CNT - 1
if CNT = 0, PC = address `CONTINUE`
if CNT ≠ 0, PC = address `HERE + 1`

GOTO Unconditional Branch

Syntax: [*label*] GOTO k

Operands: $0 \le k \le 2048$

Operation: k → PC<10:0>,
(PCLATH<4:3>) → PC<12:11>

Status Affected: None

Encoding:

10	1kkk	kkkk	kkkk

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH <4:3>. GOTO is a two-cycle instruction.

Words: 1

Cycles: 2

Example:
```
GOTO THERE
```
After Instruction
PC = Address of `THERE`

INCF — Increment f

Syntax: [*label*] INCF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) + 1 → (dest)

Status Affected: Z

Encoding:

00	1010	dfff	ffff

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

Words: 1

Cycles: 1

Example:
```
INCF    CNT, 1
```
Before Instruction
CNT = 0xFF
Z = 0

After Instruction
CNT = 0x00
Z = 1

INCFSZ — Increment f, skip if 0

Syntax: [*label*] INCFSZ f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) + 1 → (dest), skip if result = 0

Status Affected: None

Encoding:

00	1111	dfff	ffff

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1 (2)

Example:
```
HERE    INCFSZ  CNT, 1
        GOTO    LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address HERE

After Instruction
CNT = CNT + 1
if CNT = 0, PC = address CONTINUE
if CNT ≠ 0, PC = address HERE + 1

IORLW — Inclusive OR Literal with W

Syntax: [*label*] IORLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .OR. (k) → (W)

Status Affected: Z

Encoding:

11	1000	kkkk	kkkk

Description: The contents of the W register are OR'ed with the eight bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
IORLW   0x35
```
Before Instruction
W = 0x9A

After Instruction
W = 0xBF

IORWF — Inclusive OR W with f

Syntax: [*label*] IORWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (W) .OR. (f) → (dest)

Status Affected: Z

Encoding:

00	0100	dfff	ffff

Description: Inclusive OR the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
IORWF   RESULT, 0
```
Before Instruction
RESULT = 0x13
W = 0x91

After Instruction
RESULT = 0x13
W = 0x93

MOVLW Move Literal to W

Syntax: [*label*] MOVLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W)

Status Affected: None

Encoding:

11	00XX	kkkk	kkkk

Description: The 8-bit literal "k" is loaded into W register.

Words: 1

Cycles: 1

Example:

```
MOVLW   0x5A
```

After Instruction
W = 0x5A

MOVWF Move W to f

Syntax: [*label*] MOVWF f

Operands: 0 ≤ f ≤ 127

Operation: (W) → (f)

Status Affected: None

Encoding:

00	0000	1fff	ffff

Description: Move data from W register to register "f".

Words: 1

Cycles: 1

Example:

```
MOVWF   OPTION
```

Before Instruction
OPTION = 0xFF
W = 0x4F

After Instruction
OPTION = 0x4F
W = 0x4F

MOVF Move f

Syntax: [*label*] MOVF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) → (dest)

Status Affected: Z

Encoding:

00	1000	dfff	ffff

Description: The contents of register f is moved to destination d. If d=0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example:

```
MOVF    FSR, 0
```

After Instruction
W = value in FSR register

NOP No Operation

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

00	0000	0XX0	0000

Description: No operation

Words: 1

Cycles: 1

Example:

```
NOP
```

OPTION **Load Option Register**

Syntax: [*label*] OPTION

Operands: None

Operation: W → OPTION;

Status Affected: None

Encoding:

00	0000	0110	0010

Description: The contents of the W register is loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.

Words: 1

Cycles: 1

Example:

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

RETFIE **Return from Interrupt**

Syntax: [*label*] RETFIE

Operands: None

Operation: TOS → PC,
1 → GIE;

Status Affected: None

Encoding:

00	0000	0000	1001

Description: Return from Interrupt. Stack is popped and Top of the Stack (TOS) is loaded in PC. Interrupts are enabled by setting the GIE bit. GIE is the global interrupt enable bit (INTCON<7>). This is a two-cycle instruction.

Words: 1

Cycles: 2

Example: `RETFIE`

After Interrupt
PC = TOS
GIE = 1

RETLW **Return Literal to W**

Syntax: [*label*] RETLW k

Operands: $0 \le k \le 255$

Operation: k → W; TOS → PC;

Status Affected: None

Encoding:

11	01XX	kkkk	kkkk

Description: The W register is loaded with the eight bit literal "k". The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

Words: 1

Cycles: 2

Example:

```
      CALL   TABLE ; W contains table offset
                   ; value
      •            ; W now has table value
      •
      •
TABLE ADDWF PC     ; W = offset
      RETLW k1     ; Begin table
      RETLW k2     ;
      •
      •
      •
      RETLW kn     ; End of table
```

Before Instruction
W = 0x07

After Instruction
W = value of k7

RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: TOS → PC;

Status Affected: None

Encoding:

00	0000	0000	1000

Description: Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

Words: 1

Cycles: 2

Example: `RETURN`

After Interrupt
PC = TOS

RLF — Rotate Left f through Carry

Syntax: [*label*] RLF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

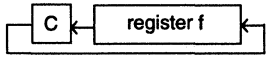
Operation: f<n> → d<n+1>, f<7> → C, C → d<0>;

Status Affected: C

Encoding:

00	1101	dfff	ffff

Description: The contents of register "f" are rotated 1-bit to the left through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is stored back in register "f".



Words: 1

Cycles: 1

Example:

```
RLF     REG1,0
```

Before Instruction
REG1 = 11100110
C = 0

After Instruction
REG1 = 11100110
W = 11001100
C = 1

RRF — Rotate Right f through Carry

Syntax: [*label*] RRF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

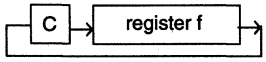
Operation: f<n> → d<n-1>,
f<0> → C,
C → d<7>;

Status Affected: C

Encoding:

00	1100	dfff	ffff

Description: The contents of register "f" are rotated one bit to the right through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".



Words: 1

Cycles: 1

Example:

```
RRF     REG1,0
```

Before Instruction
REG1 = 11100110
C = 0

After Instruction
REG1 = 11100110
W = 01110011
C = 1

SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler
1 → $\overline{TO}$,
0 → PD

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0011

Description: The Power Down status bit (PD) is cleared. Time-out status bit (TO) is set. Watchdog Timer and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP mode for more details.

Words: 1

Cycles: 1

Example:

```
SLEEP
```

SUBLW — Subtract W from Literal

Syntax: [*label*] SUBLW k

Operands: 0 ≤ k ≤ 255

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Encoding:

11	110X	kkkk	kkkk

Description: The W register is subtracted (2's complement method) from the 8-bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example 1:

```
SUBLW     0X02
```

Before Instruction
W = 1
C = ?

After Instruction
W = 1
C = 1 ; result is positive

Example 2: Before Instruction
W = 3
C = ?

After Instruction
W = FF
C = 0 ; result is negative

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f)-(W) → (dest)

Status Affected: C, DC, Z

Encoding:

00	0010	dfff	ffff

Description: Subtract (2's complement method) the W register from register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example 1:
```
SUBWF  REG1,1
```
Before Instruction
REG1 = 0
W = 1
C = ?
After Instruction
REG1 = FF
W = 1
C = 0 ; result is negative

Example 2: Before Instruction
REG1 = FF
W = 0
C = ?
After Instruction
REG1 = FF
W = 0
C = 1 ; result is positive

TRIS **Load TRIS Register**

Syntax: [*label*] TRIS f

Operands: 5 ≤ f ≤ 7

Operation: W → TRIS register f;

Status Affected: None

Encoding:

00	0000	0110	0fff

Description: This instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.

Words: 1

Cycles: 1

Example:

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

SWAPF **Swap f**

Syntax: [*label*] SWAPF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: f<0:3> → d<4:7>,
f<4:7> → d<0:3>;

Status Affected: None

Encoding:

00	1110	dfff	ffff

Description: The upper and lower nibbles of register "f" are exchanged. If "d" is 0 the result is placed in W register. If "d" is 1 the result is placed in register "f".

Words: 1

Cycles: 1

Example:
```
SWAPF  REG, 0
```
Before Instruction
REG = 0xA5
After Instruction
REG = 0xA5
W = 0x5A

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

11	1010	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the 8-bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
XORLW  0xAF
```
Before Instruction
W = 0xB5
After Instruction
W = 0x1A

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 128$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

00	0110	dfff	ffff

Description: Exclusive OR the contents of the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:

```
XORWF  REG, 1
```

Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

14.0 DEVELOPMENT SUPPORT

14.1 Development Tools

The PIC16C5X and PIC16CXX microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER™ Real-Time In-Circuit Emulator
- PRO MATE™ Universal Programmer
- PICSTART™ Low-Cost Prototype Programmer
- Assembler
- Software Simulator

14.2 PICMASTER™: High Performance Universal In-Circuit Emulator

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X, PIC16CXX and PIC17CXX families.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16C5X, PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on PC compatible machines ranging from 80286-AT® class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.1 environment, allowing the operator access to a wide range of supporting software and accessories.

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.1 environment was chosen to best make these features available to you, the end user.

The PICMASTER Emulator Universal System consists primarily of four major components:

- Host-Interface Card
- Emulator Control Pod
- Target-Specific Emulator Probe
- PC Host Emulation Control Software

The Windows 3.1 System is a multitasking operating system which will allow the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window.

Dynamic Data Exchange (DDE), a feature of Windows 3.1, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

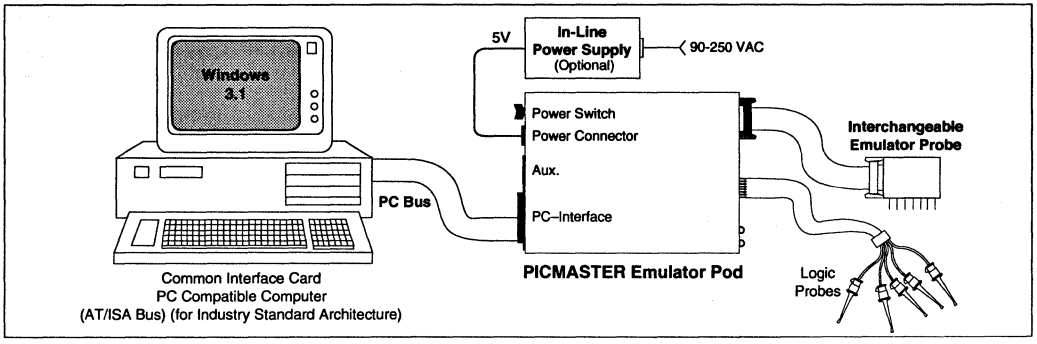
Under Windows 3.1, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16Cxx processor and a PIC17Cxx processor).

14.3 PRO MATE™: Universal Programmer

The PRO MATE Universal Programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MATE has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability . It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE can read, verify or program PIC16C5X, PIC16CXX and PIC17CXX devices. It can also set fuse configuration and code-protect in this mode. Its EEPROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.

FIGURE 14-1: PICMASTER SYSTEM CONFIGURATION



In PC-hosted mode, the PRO MATE connects to the PC via one of the COM (RS232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of VDD min, VDD max and VPP levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different serial number, sequential or random.

The PRO MATE has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. PRO MATE supports all PIC16C5X, PIC16CXX and PIC17CXX processors.

14.4 PICSTART™ Programmer

The PICSTART™ programmer is an easy to use, very low-cost prototype programmer. It connects to the PC via one of the COM (RS232) ports. A PC based user interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based.

14.5 Assembler (MPASM)

Cross Assembler is a PC hosted symbolic assembler. It supports all microcontroller series including the PIC16C5X CMOS, PIC16CXX, and PIC17CXX families.

MPASM offers fully featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from the Microchip Universal Emulator System (PICMASTER).

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro Assembly Capability
- Provides Object, Listing, Symbol and special files required for debugging with one of the Microchip Emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a full feature directive language represented by four basic classes of directives:

- **Data Directives** are those that control the allocation of memory and provide a way to refer to data items symbolically, by meaningful names.
- **Listing Directives** control the MPASM listing dis play. They allow the specification of titles and subtitles, page ejects and other listing control.
- **Control Directives** permit sections of conditionally assembled code.
- **Macro Directives** control the execution and data allocation within macro body definitions.

14.6 Software Simulator (MPSIM)

The Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16C5X and PIC16CXX series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in single step, execute until break or in a trace mode. Two forms of symbolic debugging are available: an internal symbol table for disassembling opcodes and the displaying of source code from a listing file. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

14.7 Development Systems

For convenience, the development tools are packaged into comprehensive systems as listed in Table 14-1:

TABLE 14-1: DEVELOPMENT SYSTEM PACKAGES

Item	Name	System Description
1.	PICMASTER™ System	PICMASTER In-Circuit Emulator with your choice of Target Probe, PRO MATE Programmer, Assembler, Software Simulator and Samples.
2.	PICSTART™ System	PICSTART™ Low-Cost Prototype Programmer, Assembler, Software Simulator and Samples

14.8 Probe Specifications

The PICMASTER probes currently meet the following specifications:

PICMASTER PROBE	Devices Supported	PROBE Maximum Frequency	PROBE Operating Voltage
PROBE - 16E	PIC16C64	10 MHZ	4.5V - 5.5V

16.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... .-55 to+ 125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss (except VDD and $\overline{MCLR}$) ..... -0.6V to VDD +0.6V
Voltage on VDD with respect toVss ..... 0 to +7.5 V
Voltage on $\overline{MCLR}$ with respect to Vss (Note 2) ..... 0 to +14 V
Total power Dissipation (Note 1) ..... 1.0 W
Maximum Current out of Vss pin 300mA
Maximum Current into VDD pin 250mA
Input clamp current, IIK (VI<0 or VI> VDD) ..... ±20mA
Output clamp current, IOK (V0 <0 or V0>VDD) ..... ±20mA
Maximum Output Current sunk by any I/O pin 25mA
Maximum Output Current sourced by any I/O pin 25mA
Maximum Current sunk by PORTA, PORTB, and PORTE (combined) 200mA
Maximum Current sourced by PORTA, PORTB, and PORTE (combined) 200mA
Maximum Current sunk by PORTC and PORTD (combined) 200mA
Maximum Current sourced by PORTC and PORTD (combined) 200mA

Notes: 1. Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ Ioh} + Σ {(VDD-Voh) x Ioh} + Σ(Vol x Iol)

2. Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low' level to the $\overline{MCLR}$ pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

16.1 DC CHARACTERISTICS: PIC16C64-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C64-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ + 125°C for automotive, -40°C ≤ TA ≤ + 85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD = 4.0V to 6.0V			
Characteristic	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	4.0 4.5		6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
RAM Data Retention Voltage (Note 1)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section on power on reset for details
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section on power on reset for details
Supply Current (Note 2, 5)	IDD		2.7 52.5 13.5	5 105 30	mA µA mA	FOSC = 4 MHz, VDD = 5.5V (Note 4) LP osc configuration FOSC = 32 KHz, VDD = 4.0V, WDT disabled HS osc configuration FOSC = 20 MHz, VDD = 5.5V (PIC16C64-20)
Power Down Current (Note 3, 5)	IPD		10.5 1.5 1.5 1.5	42 21 24 TBD	µA µA µA µA	VDD = 4.0V, WDT enabled, -40°C to +85°C VDD = 4.0V, WDT disabled, 0°C to +70°C VDD = 4.0V, WDT disabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -40°C to +125°C

* These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Notes: 1. This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2. The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
   The test conditions for all IDD measurements in active operation mode are:
   OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3. The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

4. For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5. Timer1 oscilator (when enabled) adds approximately xmA to the specification. This value is from characterization and is for design guidance only. This is not tested.

16.2 DC CHARACTERISTICS: PIC16LC64-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS						**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ + 125°C for automotive, -40°C ≤ TA ≤ + 85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD = 2.5V to 6.0V
Characteristic	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.5		6.0	V	XT, RC and LP osc configuration
		4.5		5.5	V	HS osc configuration
RAM Data Retention Voltage (Note 1)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section on power on reset for details
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section on power on reset for details
Supply Current (Note 2, 5)	IDD		2.7	5	mA	Fosc = 4 MHz, VDD = 5.5V (Note 4)
			22.5	46	µA	Fosc = 32 KHz, VDD = 3.0V, WDT disabled
Power Down Current (Note 3, 5)	IPD		7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
			0.9	13.5	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
			0.9	18	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
			0.9	24	µA	VDD = 3.0V, WDT disabled, -40°C to +125°C

* These parameters are characterized but not tested.

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Notes: 1. This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2. The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
   The test conditions for all IDD measurements in active operation mode are:
   OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3. The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

4. For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5. Timer1 oscilator (when enabled) adds approximately xmA to the specification. This value is from characterization and is for design guidance only. This is not tested.

16.3 DC CHARACTERISTICS: PIC16C64-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C64-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16LC64-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40 ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec tables 14.1/14.2					
Characteristic	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
Input Low Voltage						
I/O ports	VIL					
- with TTL buffer		VSS		0.8 V	V	
- with Schmitt Trigger buffer		VSS		0.2 VDD	V	
MCLR, RA4/T0CKI, OSC1 (in RC mode)		VSS		0.2 VDD	V	Note 1
OSC1 (in XT, HS and LP)		VSS		0.3 VDD	V	
Input High Voltage						
I/O ports	VIH					
- with TTL buffer		2.0		VDD	V	
- with Schmitt Trigger buffer		0.8 VDD		VDD		
MCLR, RA4/T0CKI		0.8 VDD		VDD	V	
OSC1 (in RC mode)		0.7 VDD		VDD	V	Note 1
PORTB weak pull-up current	IPURB	50	100	150	µA	VDD = 5V, VPIN = VSS
Input Leakage Current (Notes 2, 3)						
I/O ports	IIL			±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR, RA4/T0CKI				±5	µA	VSS ≤ VPIN ≤ VDD
OSC1				±5	µA	VSS ≤ VPIN ≤ VDD , XT, HS and LP osc configuration
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
				0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
OSC2/CLKOUT				0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
(RC osc configuration)				0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C
Output High Voltage						
I/O Ports (Note 3)	VOH	VDD-0.7			V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
		VDD-0.7			V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
OSC2/CLKOUT		VDD-0.7			V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
(RC osc configuration)		VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
Capacitive Loading Specs on Output Pins						
OSC2 pin	COSC2			15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
All I/O pins and OSC2 (in RC mode)	CIO			50	pF	
SCL, SDA in I²C mode	Cb			400	pF	

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Notes: 1. In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C64 be driven with external clock in RC mode.

2. The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
3. Negative current is defined as coming out of the pin.
4. The user may use better of the two specs.

16.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. Tcc:st (I²C specifications only)
4. Ts (I²C specifications only)

T			
F	Frequency	T	Time

Lowercase subscripts (pp) and their meanings:

pp			
cc	CCP1	os	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Upper case letters and their meanings:

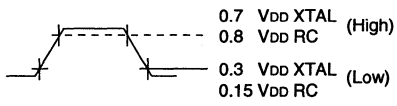
S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedence)	V	Valid
L	Low	Z	High Impedence
I²C only			
AA	output access	High	High
BUF	Bus free	Low	Low

Tcc:st (I²C specifications only)

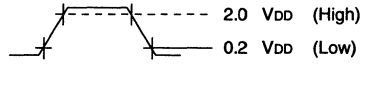
CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

PARAMETER MEASUREMENT INFORMATION

All timings are measured between high and low measurement points as indicated in the figures below.



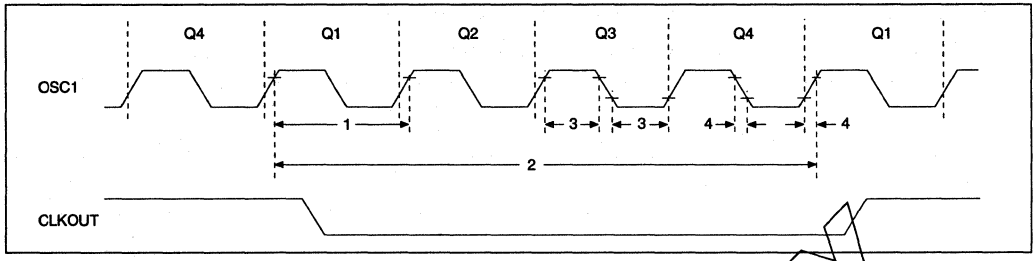
OSC1 MEASUREMENT POINTS



I/O PORT MEASUREMENT POINTS

16.5 Timing Diagrams and Specifications

External Clock Timing



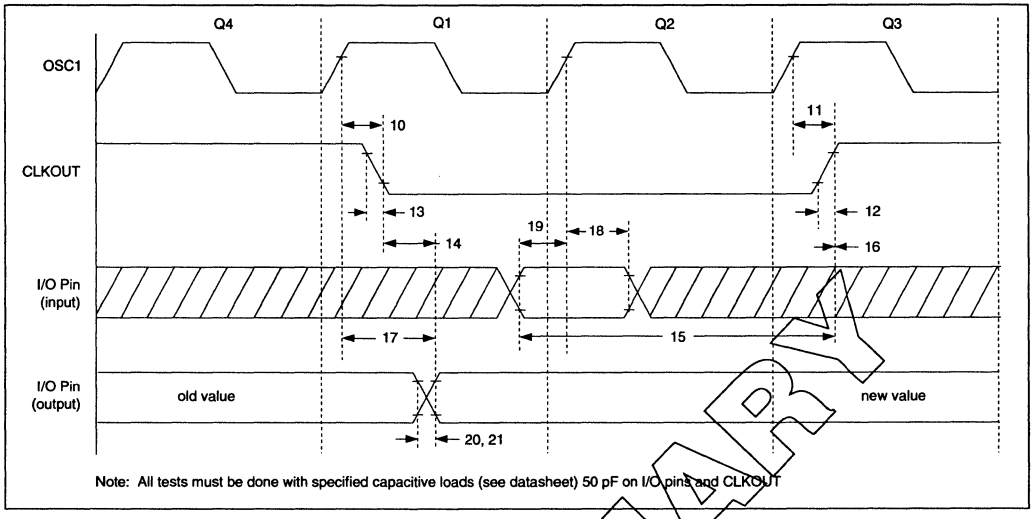
External Clock Timing Requirements

Parameter No.	Sym	Characteristic	Min	Typ †	Max	Units	Conditions
	Fos	**External CLKIN Frequency (Note 1)**	DC		4	MHz	XT and RC osc mode
			DC		4	MHz	HS osc mode (PIC16C64-04, PIC16LC64-04)
				-			
			DC		20	MHz	HS osc mode (PIC16C64-20)
			DC		200	KHz	LP osc mode
		Oscillator Frequency (Note 1)	DC		4	MHz	RC osc mode
			0.1		4	MHz	XT osc mode
			1		4	MHz	HS osc mode (PIC16C64-04 PIC16LC64-04)
				-			
			1		20	MHz	HS osc mode (PIC16C64-20)
			DC		200	KHz	LP osc mode
1	Tos	**External CLKIN Period (Note 1)**	250		-	ns	XT and RC osc mode
			250		-	ns	HS osc mode (PIC16C64-04, PIC16LC64-04)
				-			
			50		-	ns	HS osc mode (PIC16C64-20)
			50		-	µs	LP osc mode
		Oscillator Period (Note 1)	250			ns	RC osc mode
			250		10,000	ns	XT osc mode
			250		1,000	ns	HS osc mode (PIC16C64-04 PIC16LC64-04)
			50		1,000	ns	HS osc mode (PIC16C64-20)
			5			µs	LP osc mode
2	Tcy	**Instruction Cycle Time (Note 1)**	1.0	$4/F_{os}$	DC	µs	
3	TosL, TosH	Clock in (OSC1) High or Low Time	50	-	-	ns	XT oscillator
			2	-	-	µs	LP oscillator
			20	-	-	ns	HS oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	25	-	-	ns	XT oscillator
			50	-	-	ns	LP oscillator
			25	-	-	ns	HS oscillator

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

CLKOUT and I/O Timing



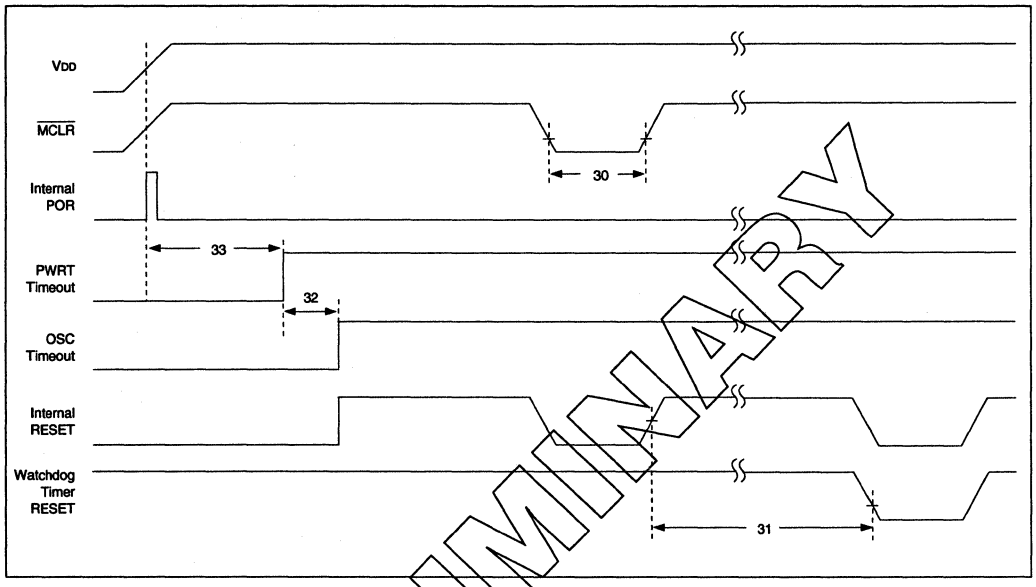
CLKOUT and I/O Timing Requirements

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓ (RC mode)	-	15	30	ns	
11	TosH2ckH	OSC1↑ to CLKOUT↑ (RC mode)	-	15	30	ns	
12	TckR	CLKOUT rise time (RC mode)	-	5	15	ns	
13	TckF	CLKOUT fall time (RC mode)	-	5	15	ns	
14	TckL2ioV	CLKOUT ↓ to Port out valid	-	-	0.5Tcy+20	ns	
15	TioV2ckH	Port in valid before CLKOUT ↑ (RC mode)	0.25 Tcy+25	-	-	ns	
16	TckH2ioI	Port in hold after CLKOUT ↑ (RC mode)	0	-	-	ns	
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	-	-	TBD	ns	
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	-	-	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	-	-	ns	
20	TioR	Port output rise time	-	10	25	ns	
21	TioF	Port output fall time	-	10	25	ns	

* These parameters are characterized but not tested.

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Reset, Watchdog Timer, Oscillator Start-Up Timer and Power-Up Timer Timing



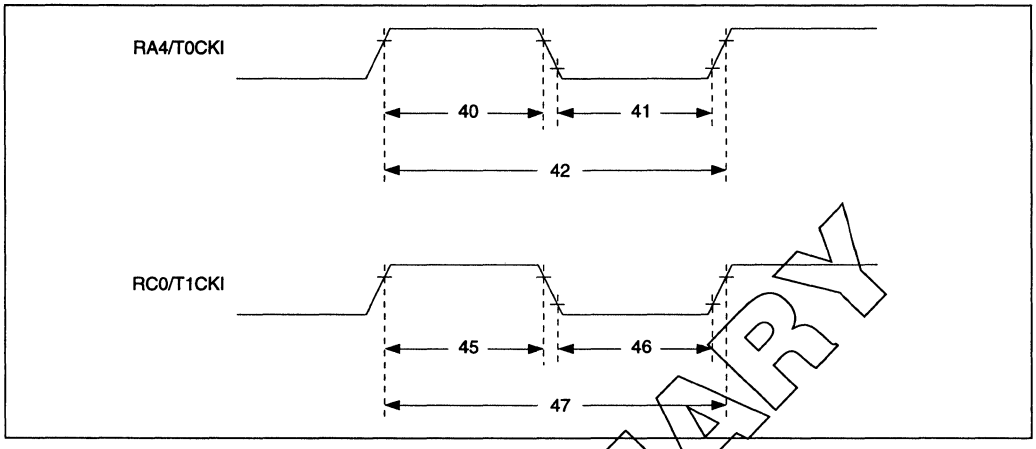
Reset, Watchdog Timer, Oscillator Start-Up Timer and Power-Up Timer Requirements

Parameter No.	Sym	Characteristic	Min	Typ †	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	100	-	-	ns	
31	Twdt	Watchdog Timer Timeout Period (No Prescaler)	7*	18	33*	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period		1024 tosc		ms	tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	VDD = 5V, -40°C to +125°C

* These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Timer0 and Timer1 Clock Timings



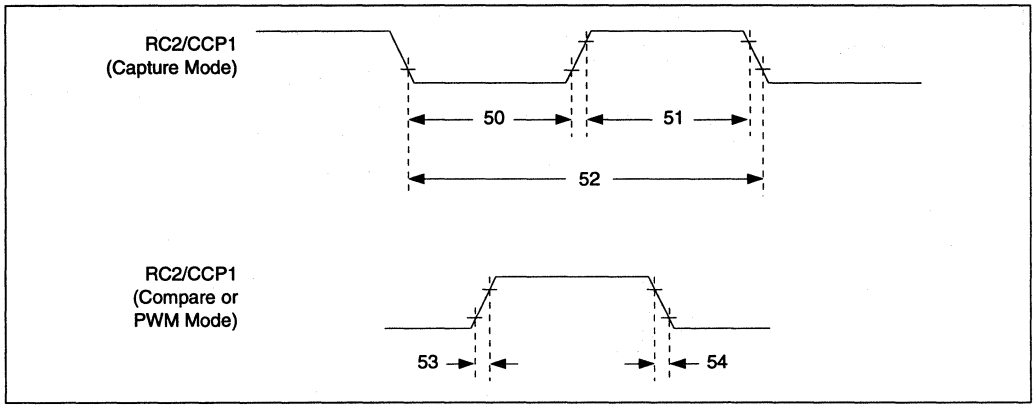
Timer0 and Timer1 Clock Requirements

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	T_{t0H}	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20*	-	-	ns	
			With Prescaler	10*	-	-	ns	
41	T_{t0L}	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20*	-	-	ns	
			With Prescaler	10*	-	-	ns	
42	T_{t0P}	T0CKI Period		$\frac{T_{CY} + 40^*}{N}$	-	-	ns	Where N = prescale value (2, 4, ..., 256)
45	T_{t1H}	T1CKI High Time	Synchronous, No Prescaler	0.5Tcy + 20	-	-	ns	
			Synchronous, With Prescaler	10*	-	-	ns	
			Asynchronous	2 Tcy	-	-	ns	
46	T_{t1L}	T1CKI Low Time	Synchronous, No Prescaler	0.5Tcy + 20*	-	-	ns	
			Synchronous, With Prescaler	10*	-	-	ns	
			Asynchronous	2 Tcy	-	-	ns	
47	T_{t1P}	T1CKI input period	Synchronous	$\frac{T_{CY} + 40^*}{N}$	-	-	ns	N=prescale value (1, 2, 4, 8)
			Asynchronous	4 Tcy	-	-	ns	
	F_{t1}	Timer1 oscillator input frequency range (oscillator enabled by setting the T1OSCEN bit)		DC	-	200	KHz	

* These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Capture/Compare/PWM Timings



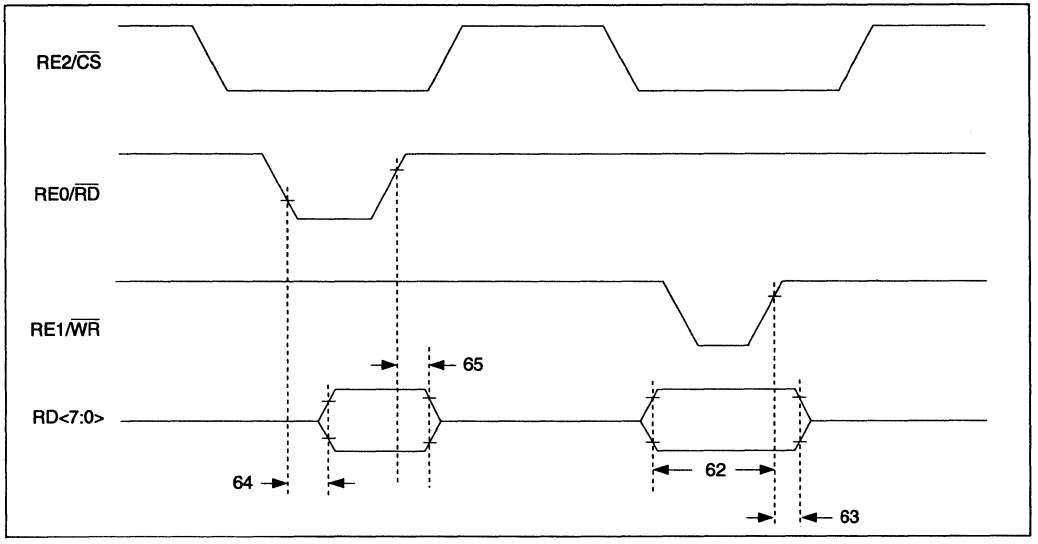
Capture/Compare/PWM Requirements

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
50	TccL	CCP1 input low time	No Prescaler	0.5 Tcy + 20	-	-	ns	
			With Prescaler	10	-	-	ns	
51	TccH	CCP1 input high time	No Prescaler	0.5 Tcy + 20	-	-	ns	
			With Prescaler	10	-	-	ns	
52	TccP	CCP1 input period		$\frac{Tcy + 40}{N}$	-	-	ns	N = prescale value (4 or 16)
53	TccR	CCP1 output rise time		-	10	25	ns	
54	TccF	CCP1 output fall time		-	10	25	ns	

* These parameters are characterized but not tested.

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Parallel Slave Port Timing

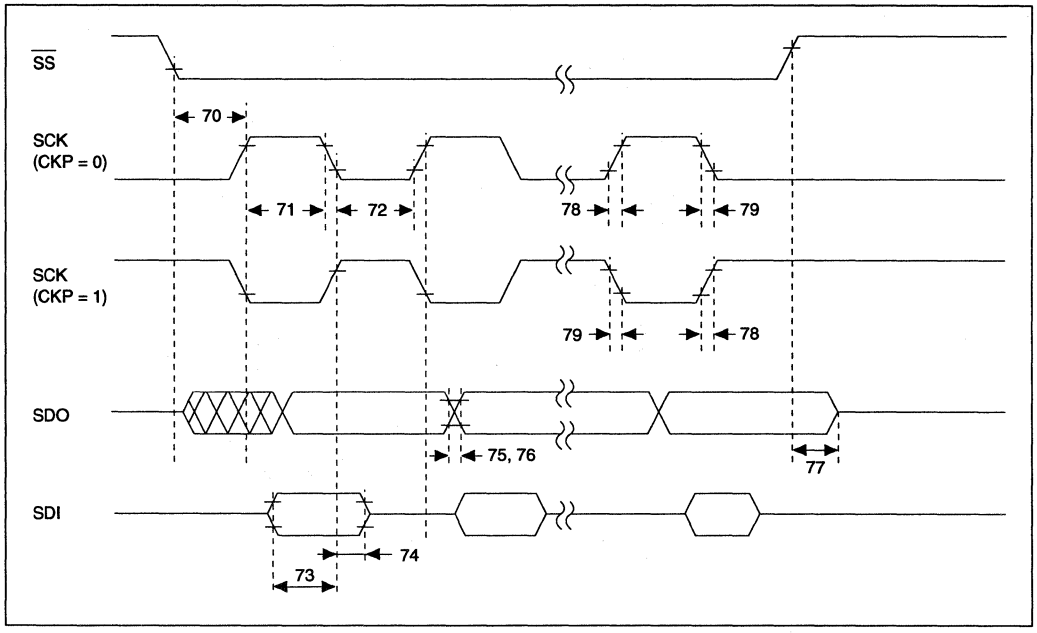


Parallel Slave Port Requirements

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before WR↑ or CS↑ (setup time)	20	-	-	ns	
63	TwrH2dtI	WR↑ or CS↑ to data–in invalid (hold time)	20	-	-	ns	
64	TrdL2dtV	RD↓ and CS↓ to data–out valid	-	-	40	ns	
65	TrdH2dtI	RD↑ or CS↓ to data–out invalid	10	-	30	ns	

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

SPI Mode Timing

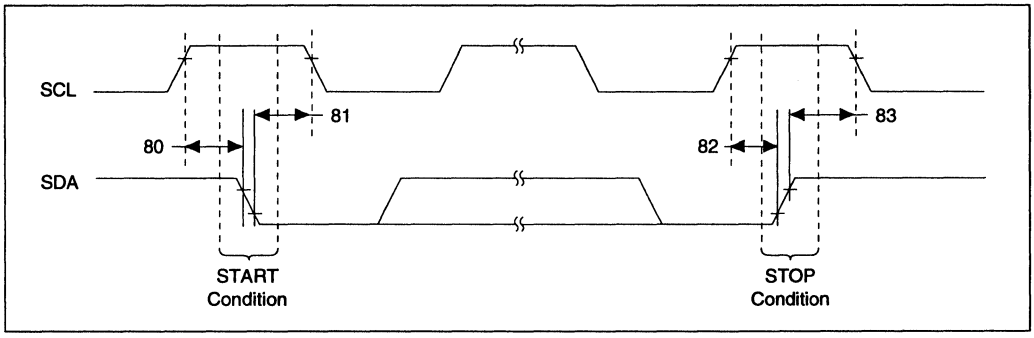


SPI Mode Requirements

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL,	$\overline{SS}$↓ to SCK↓ or SCK↑ input	Tcy	-	-	ns	
71	TscH	SCK input high time (slave mode)	Tcy + 20	-	-	ns	
72	TscL	SCK input low time (slave mode)	Tcy + 20	-	-	ns	
73	TdiV2scH, TdiV2scL	SDI data input valid before SCK edge	Tcy	-	-	ns	
74	TscH2dil, TscL2dil,	SDI data input invalid after SCK edge	0.5Tcy	-	-	ns	
75	TdoR	SDO data output rise time	-	10	25	ns	
76	TdoF	SDO data output fall time	-	10	25	ns	
77	TssH2doZ	$\overline{SS}$↓ to SDO output hi-impedence	10	-	50	ns	
78	TscR	SCK output rise time (master mode)	-	10	25	ns	
79	TscF	SCK output fall time (master mode)	-	10	25	ns	

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

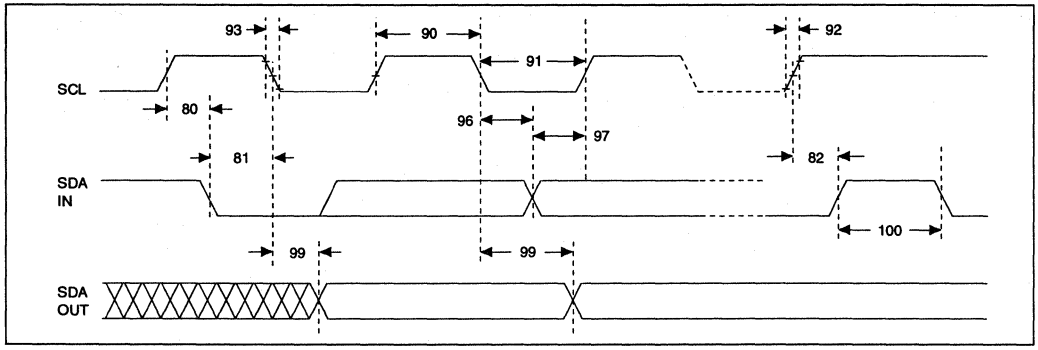
I²C Bus Start/Stop Bits Timing



I²C Bus Start/Stop Bits Requirements

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
80	TSU:STA	START condition	100 KHZ mode	4700	-	-	ns	Only relevant for repeated
		Setup time	400 KHz mode	600	-	-		START condition
81	THD:STA	START condition	100 KHz mode	4000	-	-	ns	After this period the
		Hold time	400 KHz mode	600	-	-		first clock pulse is generated
82	TSU:STO	STOP condition	100 KHZ mode	4700	-	-	ns	
		Setup time	400 KHz mode	600	-	-		
83	THD:STO	STOP condition	100 KHz mode	4000	-	-	ns	
		Hold time	400 KHz mode	600	-	-		

I²C Bus Data Timing



I²C Bus Data Requirements

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
90	THIGH	Clock high time	100 KHz mode	4.0	-	µs	PIC16C64 must operate at a minimum of 1.5 MHz
			400 KHz mode	0.6	-	µs	PIC16C64 must operate at a minimum of 10 MHz
			SSP Module	1.5 Tcy	-		
91	TLOW	Clock low time	100 KHz mode	4.7	-	µs	PIC16C64 must operate at a minimum of 1.5 MHz
			400 KHz mode	1.3	-	µs	PIC16C64 must operate at a minimum of 10 MHz
			SSP Module	1.5 Tcy	-		
92	TR	SDA and SCL rise time	100 KHz mode	-	1000	ns	
			400 KHz mode	20+0.1 Cb	300	ns	Cb is specified to be from 10-400 pF
93	TF	SDA and SCL fall time	100 KHz mode	-	300	ns	
			400 KHz mode	20+0.1 Cb	300	ns	Cb is specified to be from 10-400 pF
80	TSU:STA	START condition setup time	100 KHz mode	4.7	-	µs	Only relevant for repeated START condition
			400 KHz mode	0.6	-	µs	
81	THD:STA	START condition hold time	100 KHz mode	4.0	-	µs	After this period the first clock pulse is generated
			400 KHz mode	0.6	-	µs	
96	THD:DAT	Data input hold time	100 KHz mode	0	-	ns	
			400 KHz mode	0	0.9	µs	
97	TSU:DAT	Data input setup time	100 KHz mode	250	-	ns	
			400 KHz mode	100	-	ns	Note 2
82	TSU:STO	STOP condition setup time	100 KHz mode	4.7	-	µs	
			400 KHz mode	0.6		µs	
99	TAA	Output valid from clock	100 KHz mode	300	3500	ns	Note 1
			400 KHz mode	-	-	-	
100	TBUF	Bus free time	100 KHz mode	4.7	-	µs	Time the bus must be free before a new transmission can start
			400 KHz mode	1.3	-	µs	
	Cb	Bus capacitive loading		-	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement tsu;DAT≥250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max.+tsu;DAT=1000+250=1250ns (according to the standard-mode I²C bus specification) before the SCL line is released.

17.0 DC AND AC CHARACTERISTICS (GRAPHS/TABLES)

NOT AVAILABLE AT THIS TIME

20.0 PACKAGING INFORMATION

See Section 11 of the Data Book.

20.1 Package Marking Information

44L PLCC

TBD

Example

TBD

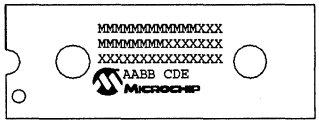
44L PQFP

TBD

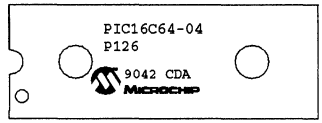
Example

TBD

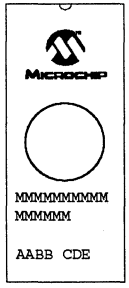
40L PDIP (.600 mil)



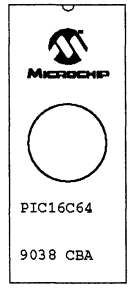
Example



40L Cerdip



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country or origin in which part was assmebled

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

APPENDIX A

The following are the list of modifications over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14-bit. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and register file (128 bytes now versus 32-bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from status register.
3. Data memory paging is redefined slightly. Status register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.

   Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressible.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to eight deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers oscillator start-up timer (OST) and power-up timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change feature.
13. RTCC pin is also a port pin (RA4) now.
14. FSR is made a full eight bit register.
15. "In system programming" is made possible. The user can program PIC16CXX devices using only five pins: V_{DD}, V_{SS}, $\overline{MCLR}/V_{PP}$, RB6 (clock) and RB7 (data in/out).
16. PCON status register is added with a Power-On Reset (POR) status bit.
17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.

APPENDIX B

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

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CONNECTING TO MICROCHIP BBS

Connect world wide to the Microchip BBS using the CompuServe communications network. In most cases a local call is your only expense. The Microchip BBS connection does not use CompuServe membership services, therefore **you do not need CompuServe membership to join Microchip's BBS.**

The procedure to connect will vary slightly from country to country. Please check with your local CompuServe agent for details if you have a problem. CompuServe services allows multiple users at baud rates up to 9600.

To connect:

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.

2. Dial your local CompuServe phone number.

3. Depress **<ENTER>** and a garbage string will appear because CompuServe is expecting a 7E1 setting.

4. Type **+ <ENTER>** and `Host Name:` will appear.

5. Type **MCHIPBBS<ENTER>** and you will be connected to the Microchip BBS.

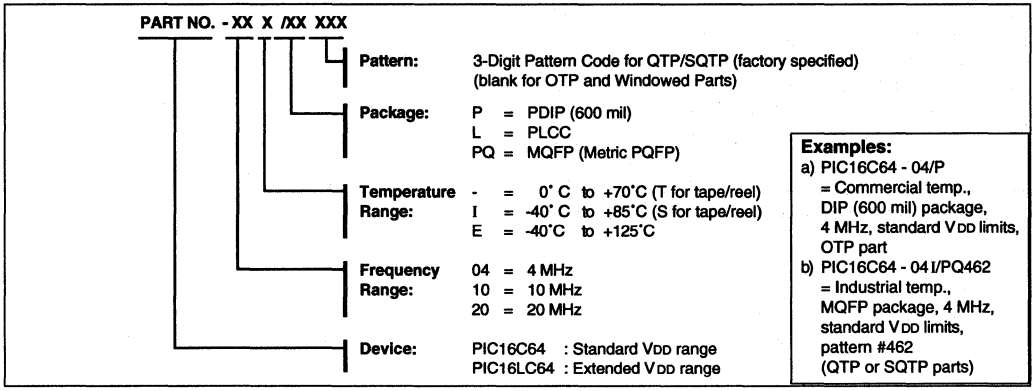
In the United States, to find CompuServe's phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600 baud connection. After the system responds with `Host Name:`, type

NETWORK<ENTER> and follow CompuServe's directions.

For voice information (or calling from overseas), you may call (614) 457-1550 for your local CompuServe number.

PIC16C64 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local Compuserve number.

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

PIC16C71

8-Bit CMOS EPROM Microcontroller with A/D Converter

FEATURES

High-Performance RISC-like CPU

- Only 35 single word instructions to learn
- All single cycle instructions (250ns) except for program branches which are two-cycle
- Operating speed: DC - 16 MHz clock input
  DC - 250ns instruction cycle
- 14-bit wide instructions
- 8-bit wide data path
- 1024 x 14 on-chip EPROM program memory
- 36 x 8 general purpose registers (SRAM)
- 15 special function hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
  - External INT pin
  - TMR0 timer
  - A/D conversion completion
  - PortB<7:4> interrupt on change

Peripheral Features

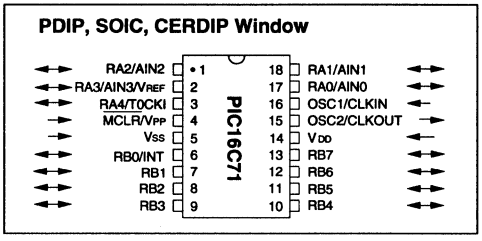
- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25mA sink max. per pin
  - 20mA source max. per pin
- TMR0: 8-bit real time clock/counter with 8-bit programmable prescaler
- A/D converter module:
  - Four analog inputs multiplexed into one A/D converter
  - Sample and hold
  - 20µs conversion time/channel
  - 8-bit resolution with ±1 LSB accuracy
  - External reference input, VREF (VREF ≤ VDD)
  - Analog input range: VSS to VREF

Special Microcontroller Features

- Power-On Reset
- Power-up Timer
- Oscillator Start-up Timer
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security EPROM fuse for code-protection
- Power saving SLEEP mode
- User selectable oscillator options:
  - RC oscillator: RC
  - Crystal/resonator: XT
  - High-speed crystal/resonator: HS
  - Power saving, low frequency crystal: LP
- Serial, In-System Programming (ISP) of EPROM program memory using only two pins

FIGURE A - PIN CONFIGURATION

PDIP, SOIC, CERDIP Window



CMOS Technology

- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide-operating voltage range:
  - Commercial: 3.0V to 6.0V
  - Industrial: 3.0V to 6.0V
  - Automotive: 3.0V to 6.0V
- Low-power consumption
  - < 2mA @ 5V, 4 MHz
  - 15µA typical @ 3V, 32 KHz (with A/D off)
  - < 1µA typical standby current @ 3V

INTRODUCTION

The PIC16C71 is a high-performance, low-cost, CMOS, fully-static EPROM-based 8-bit microcontroller with on-chip Analog to Digital converter. It is the first member of a new and improved family of PIC16CXX microcontrollers (customers familiar with the PIC16C5X products may refer to Appendix A for a list of enhancements).

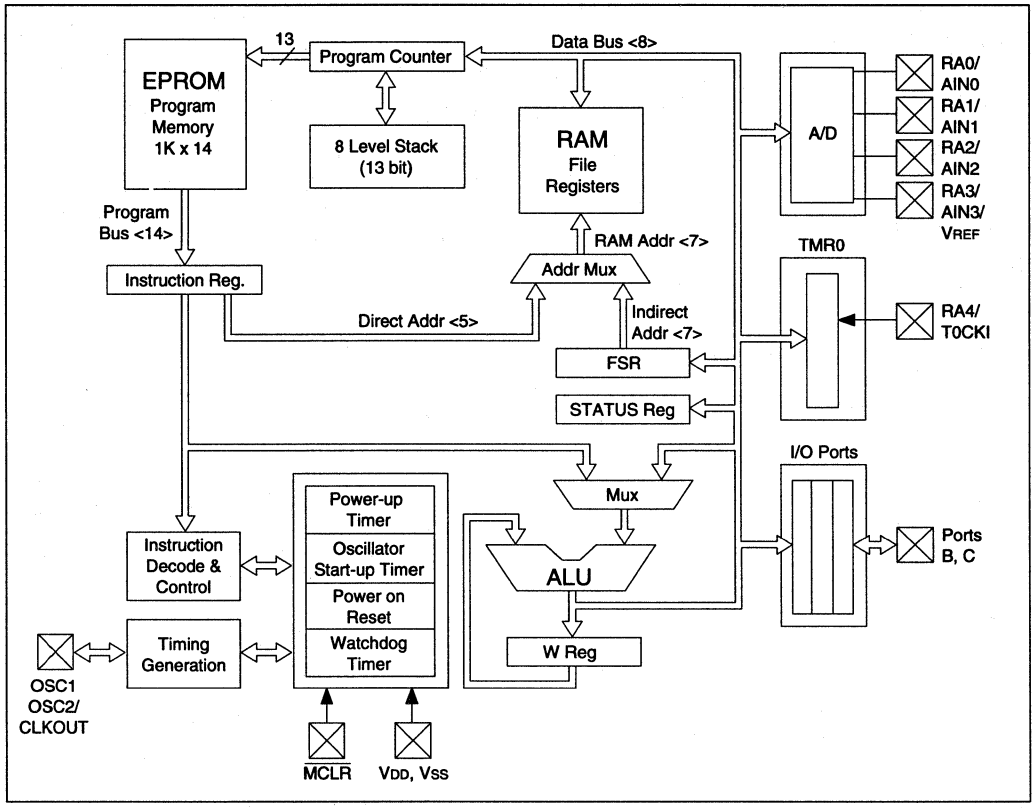
The PIC16C71's high performance is due to all single word instructions (14-bit wide) that are executed in single cycle (250ns at 16 MHz clock) except for program-branches which take two cycles (500 ns). In addition, the PIC16C71 has four interrupt sources and an eight level hardware stack.

The peripherals include an 8-bit timer/counter with an 8-bit prescaler (effectively a 16-bit timer), 13 bi-directional I/O pins and an 8-bit A/D converter. The high current drive (25mA max. sink, 20 mA max source) of the I/O pins help reduce external drivers and therefore, system cost.

The A/D converter has four channels, sample and hold, 8-bit resolution with ±1 LSB accuracy. Conversion time is typically 30µs including sampling time.

The PIC16C71 product is supported by an assembler, an in-circuit emulator and a production quality programmer. All the tools are supported on IBM PC® and compatible machines.

FIGURE B - PIC16C71 BLOCK DIAGRAM



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1.0 GENERAL DESCRIPTION

The PIC16C71 is a low-cost, high-performance, CMOS, fully static, EPROM-based 8-bit microcontroller with on-chip analog to digital converter. It employs an advanced RISC-like architecture. A reduced set of 35 instructions, all single word instructions (14-bit wide), all single cycle instructions (200ns) except for two-cycle program branches, instruction pipe-lining, large register set and separate instruction and data memory (Harvard architecture) schemes are some of the architectural innovation used to achieve very high performance. The PIC16C71 typically achieves a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in its class.

The PIC16C71 has special features which reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution and the LP oscillator minimizes power consumption. The SLEEP (power down) mode offers power saving. The user can wake up the chip from SLEEP through several external and internal interrupts and reset.

A highly reliable watchdog timer with its own on-chip RC oscillator provides protection against software malfunction.

A UV-erasable cerdip-packaged version is ideal for code development while the cost-effective One Time Programmable (OTP) version is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers while benefiting from the OTP flexibility.

1.1 Upward Compatibility with PIC16C5X

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an improved version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of modifications. Code written for PIC16C5X can be easily ported to PIC16C71 (see Appendix B).

1.2 Applications

The PIC16C71 fits perfectly in applications ranging from high-speed automotive and appliance motor control to low-power remote sensors, battery chargers, gas gauges, pointing devices, and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages for through hole or surface mounting make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease of use, and I/O flexibility makes the PIC16C71 very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications). Additionally, the on chip high speed, multi-channel A/D offers good analog capabilities at a reduced cost. The 8-bit accuracy A/D is ideally suited for a low cost application requiring an analog interface e.g. thermostat control, pressure sensing, etc.

2.0 PIC16C71 DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information and tables in this section. When placing orders, please use the "PIC16C71 Product Identification System" on the back page of this data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in cerdip package is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the oscillator modes etc. Microchip's PICSTART and PRO MATE™ programmers supports programming of the PIC16C71.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages permit the user to program them once. In addition to the program memory, the oscillator fuses, configuration fuses and the ID locations (if used) must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTP) Devices

Microchip offers the unique programming service where few locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C71 can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C71 uses a Harvard architecture, in which, program and data are accessed from separate memories. This improves bandwidth over traditional Von-Neuman architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. In PIC16C71, op-codes are 14-bit wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single cycle (250ns @ 16 MHz) except for program branches.

The PIC16C71 address 1K x 14 program memory space, all on-chip. Program execution is internal only (microcontroller mode).

The PIC16C71 can directly or indirectly address its 48 register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C71 has a fairly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C71 simple yet efficient. In addition, the learning curve is reduced significantly.

2

TABLE 3.1 - PIC16C71 PINOUT DESCRIPTION

Pin name	Pin Type	Pin function	
		Normal operation	Serial In-System Programming (ISP) Mode
VDD	P	Power	Power
VSS	P	Ground	Ground
OSC 1/CLKIN	I	Clock input/oscillator connection	-
OSC2/CLKOUT	I/O	Oscillator connection/CLKOUT output. It is CLKOUT in RC oscillator mode and oscillator connection in all other modes.	-
$\overline{MCLR}$/VPP	I/P	Master clear (external reset) input. Active low. It has Schmitt trigger input buffer.	Master clear/programming voltage (VPP) supply
RA4/T0CKI	I/O	Open-drain output/input pin. It is also the clock input to TMR0 timer/counter: Schmitt trigger input buffer	-
RA0/AIN0	I/O	Bidirectional I/O pin/Analog input channel 0. As digital input it has TTL input levels	-
RA1/AIN1	I/O	Bidirectional I/O pin/Analog input channel 1. As digital input it has TTL input levels	-
RA2/AIN2	I/O	Bidirectional I/O pin/Analog input channel 2. As digital input it has TTL input levels	-
RA3/AIN3/VREF	I/O	Bidirectional I/O pin/Analog input channel 3/Analog reference voltage input . As digital input it has TTL input levels	-
RB0/INT	I/O	Bidirectional I/O pin/External interrupt input. TTL input levels	-
RB1	I/O	Bidirectional I/O pin. TTL input levels	-
RB2	I/O	Bidirectional I/O pin. TTL input levels	-
RB3	I/O	Bidirectional I/O pin. TTL input levels	-
RB4	I/O	Bidirectional I/O pin. TTL input levels	-
RB5	I/O	Bidirectional I/O pin. TTL input levels	-
RB6	I/O	Bidirectional I/O pin. TTL input levels	Clock input Schmitt Trigger
RB7	I/O	Bidirectional I/O pin. TTL input levels	Data input/output Schmitt Trigger

Legend: I = input, O = output, I/O = input/output, P = power. -: Not used.

3.2 Clocking Scheme/Instruction Cycle

The clock input (from pin OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, PC is incremented every Q1, instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3.1.

3.3 Instruction Flow/Pipelining

An "Instruction Cycle" in PIC16C71 consists of Q1, Q2, Q3 and Q4. Instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction.

A fetch cycle begins with the program counter (PC) incrementing in Q1.

The fetched instruction is latched into the "Instruction Register (IR)" which is decoded and executed during Q2, Q3 and Q4. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

3.4 Program Memory Organization

The PIC16C71 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h - 03FFh) are physically implemented. Accessing a location above 3FFh will cause a wrap-around within the first 1K x 14 space. The reset vector is at 0000h and the interrupt vector is at 0004h. Refer to Figure 3.2.

FIGURE 3.2 - PROGRAM MEMORY MAP AND STACK

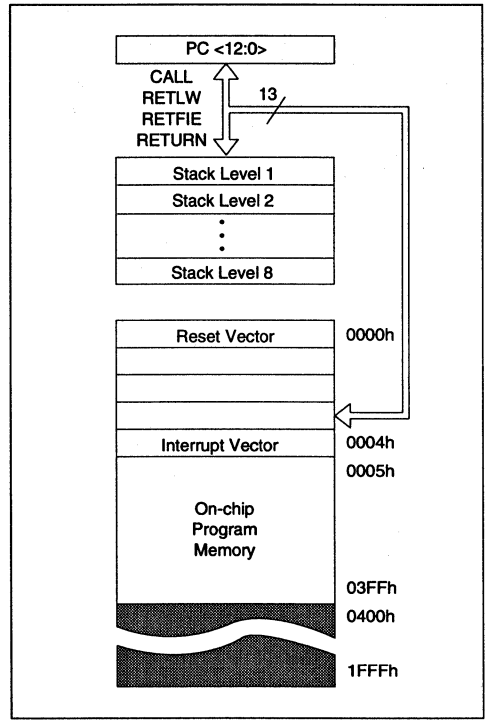
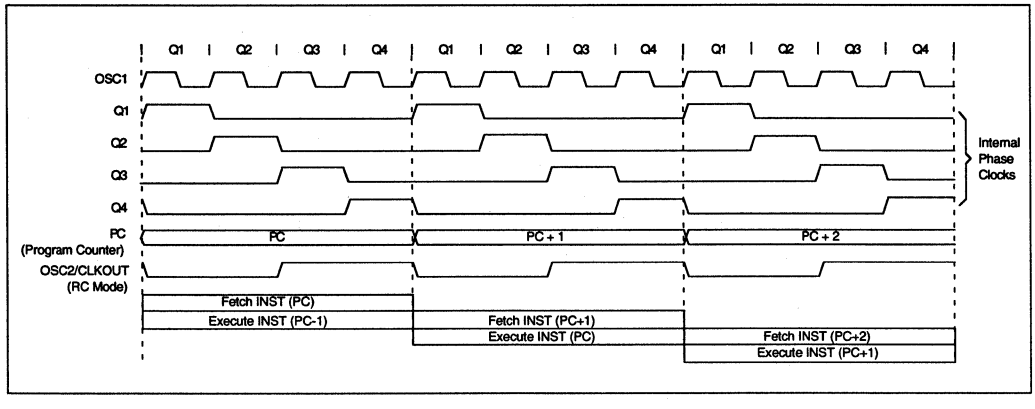


FIGURE 3.1 - CLOCK/INSTRUCTION CYCLE



Preliminary

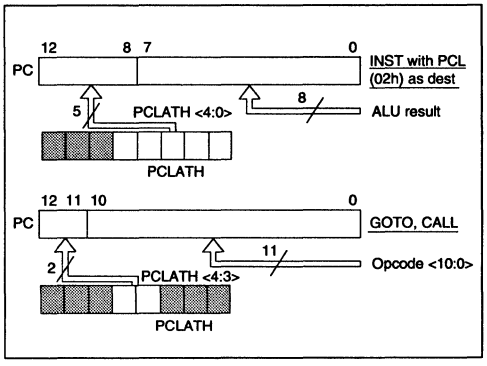
3.5 Program Counter Module

The program counter (PC) is 13-bits wide. The low byte, PCL is a readable and writable register. The high byte of the PC, PCH, is not directly readable or writable. The high byte of the PC can be written through the PCLATH register (0Ah). In a CALL or GOTO instruction, PC<10:0> are loaded from the opcode and PC<12:11> are loaded from the PCLATCH <4:3>. Since only 1K bytes are implemented, the destination address would be entirely contained in the opcode. In any instruction where the PCL is the destination, PC <12:8> are loaded directly from PC LATCH<4:0>. See Figure 3.3.

3.5.1 COMPUTED GOTO

When doing a table read using a computed goto method, care should be exercised if the table location crosses page boundaries. Please refer to the Application Brief "Table Read Using PIC16CXX" for further details.

FIGURE 3.3 - LOADING OF PC IN DIFFERENT SITUATIONS



3.6 Stack

The PIC16C71 has an 8-deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed on the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is POPped in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH (0Ah) is not affected by a "PUSH" or a "POP" operation.

3.7 Register File Organization

The register file, in PIC16C71 is organized as 128 x 8. It is accessed either directly or indirectly through file select register FSR. It is also referred to as the data memory. There are two register file page select bits in the STATUS register allowing selection from up to four pages. However, the data memory extends only up to 2Fh. The first 12 locations are used to map special function registers. Locations 0Ch - 2Fh are general purpose registers implemented as static RAM. Some special function registers are mapped in page 1. When in page 1, accessing locations 8Ch - AFh will access the RAM in page 0 (Figure 3.4).

FIGURE 3.4 - REGISTER FILE MAP

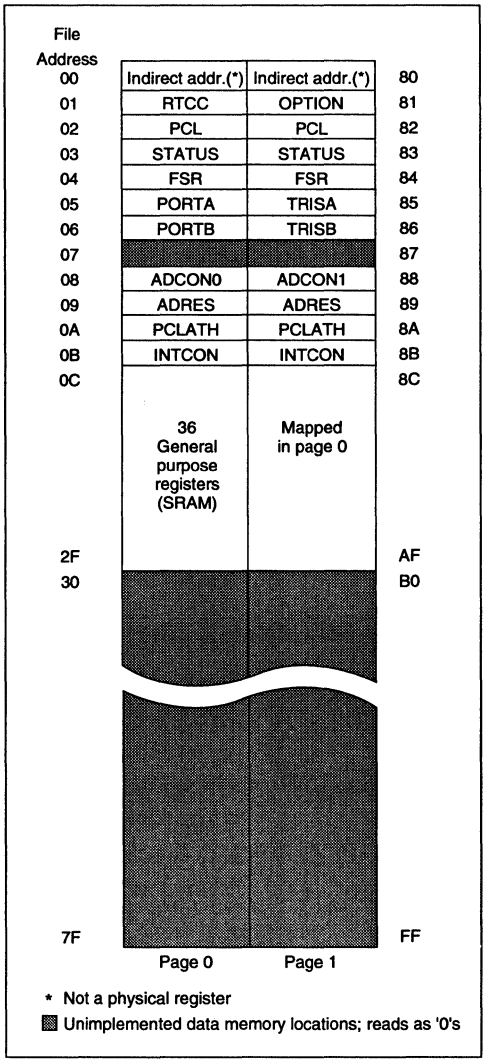
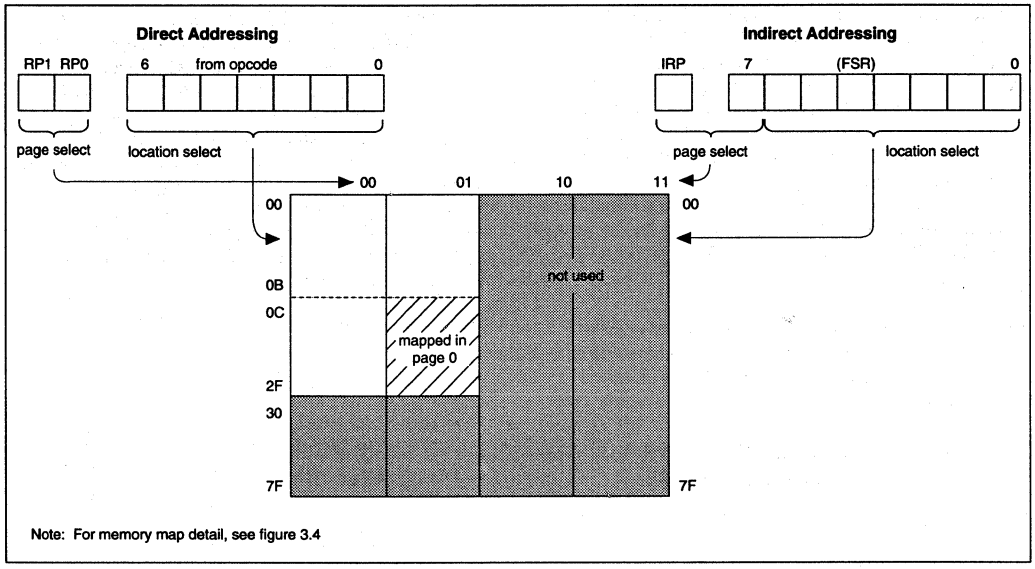


FIGURE 3.5 - DIRECT/INDIRECT ADDRESSING



Note: For memory map detail, see figure 3.4

FIGURE 3.6 - REGISTER FILE SUMMARY (PIC16C71)

Filename		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0	Value on power on reset (Note 3)
Page 0:										
00	INDO	Uses contents of FSR to address data memory (not a physical register)								00000000
01	TMR0	8 Bit Real Time clock counter								XXXXXXXX
02	PCL	Low order 8 bits of PC								00000000
03	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	00011XXX
04	FSR	Indirect data memory, address pointer 0								XXXXXXXX
05	PORTA	-	-	-	RA4/T0CKI	RA3/AIN3/V_{REF}	RA2/AIN2	RA1/AIN1	RA0/AIN0	XXXXXXXX
06	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	XXXXXXXX
07		Not implemented								
08	ADCON0	ADCS1	ADCS0	-	CHSI	CHS0	GO/DONE	ADIF	ADON	00000000
09	ADRES	8-Bit A/D result register								XXXXXXXX
0A	PCLATH	Holding register for high byte of PC (Note 1)								---00000
0B	INTCON	GIE	ADIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000000X
Page 1:										
80	INDO	MAPPED IN PAGE 0								
81	OPTION	$\overline{RBPU}$	INTEDG	RTS	RTE	PSA	PS2	PS1	PS0	11111111
82	PCL	Mapped in page 0								
83	STATUS	Mapped in page 0								
84	FSR	Mapped in page 0								
85	TRISA	PORTA (f05) data direction register								---11111
86	TRISB	PORTB (f06) data direction register								11111111
87		Not implemented								
88	ADCON1	-	-	-	-	-	-	PCFG1	PCFG0	------00
89	ADRES	Mapped in page 0								
8A	PCLATH	Mapped in page 0								
8B	INTCON	Mapped in page 0								

x = unknown
u = unchanged

Notes:

1. The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<15:8> whose contents are updated from or transfered to the upper byte of the program counter.
2. The reset values of the special function register depend on the type of reset. See Table 4.1.
3. Special function registers are reset to different values under certain conditions. Refer to Figure 4.1 for details.

3.7.1 REGISTER FILE ADDRESSING MODES

The register file can be addressed directly or indirectly. In both modes, up to 512 register locations can be addressed.

Direct addressing mode: An effective 9-bit direct address is obtained by concantenating 7-bits of direct address from the opcode and 2-bits (RP1, RP0) from the STATUS register<6,5> as shown in Figure 3.5.

Indirect addressing mode: Indirect addressing is possible by using file address 00h. Any instruction using INDF as file register actually accesses data pointed to by the file select register, FSR (address 04h). Reading INDF itself indirectly will produce 00h. Writing to INDF indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concantenating the 8-bit FSR register and the IRP bit from the STATUS register<7> as shown in Figure 3.5.

Please note that some special function registers are mapped in page 1. It will be necessary to set RP0 bit to address them. Both RP1 and IRP bits are essentially not used.

For convenience, the general purpose registers are mapped both in page 0 and page 1.

3.8 Indirect Addressing Register (INDF)

It is not a physical register. Addressing INDF will cause indirect addressing. See Sections 3.7.1 and 3.7.1.1 for details.

3.8.1 TMR0

8-Bit Real Time Clock Counter

See Section 5.4 for details.

3.8.2 PCL

Low order 8-bits of the PC

See Section 3.5 for details.

3.9 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for data memory.

The STATUS register can be destination for any instruction like any other register. However, the status bits are set following the write operation (Q4). Furthermore, $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with STATUS register as destination may be different than intended. For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the status register as 000UU1UU (where U = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the STATUS registers because these instructions do not affect any status bit.

For other instructions, affecting any status bits, see the section "Instruction Set Summary" (Section 4.0)

3.9.1 CARRY/$\overline{BORROW}$ AND DIGIT CARRY/ $\overline{BORROW}$ BITS

The carry bit (C) is a carry out in addition operations (ADDWF, ADDLW) and a borrow out in subtract operations (SUBWF, SUBLW). The following examples explain operation of carry/borrow bit:

```
;SUBLW Example #1
;
movlw   0x01    ;wreg=1
sublw   0x02    ;wreg= 2-wreg = 2-1=1
                ;Carry=1: result is positive
;
;SUBLW Example #2
;
movlw   0x02    ;wreg=2
sublw   0x01    ;wreg=1-wreg=1-2=FFh
                ;Carry=0: Result is negative
;
;SUBWF Example #1
;
clrf    0x20    ;f(20h)=0
movlw   1       ;wreg=1
subwf   0x20    ;f(20h)=f(20h)-wreg=0-1=FFh
                ;Carry=0:Result is negative
;
;SUBWF Example #2
movlw   0xFF    ;
movwf   0x20    ;f(20h)=FFh
clrw            ;wreg=0
subwf   0x20    ;f(20h)=f(20h)-wreg=FFh-0=FFh
                ;Carry=1: Result is positive
;
```

The digit carry operates in the same way as the carry bit, i.e.: it is a borrow in subtract operations.

3.9.2 TIME OUT AND POWER DOWN STATUS BITS ($\overline{TO}$, $\overline{PD}$)

The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be tested to determine if a RESET condition has been caused by a Watchdog Timer timeout, a power-up condition, or a wake-up from SLEEP by the Watchdog Timer or $\overline{MCLR}$ pin.

These status bits are only affected by events listed in Table 3.2.

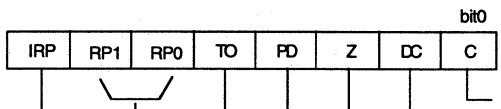
TABLE 3.2 - EVENTS AFFECTING $\overline{PD}$/$\overline{TO}$ STATUS BITS

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
WDT Timeout	0	U	No effect on PD
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

U: unchanged

Note: A WDT timeout will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{PD}$ bit. Table 3.2 reflects the status of $\overline{PD}$ and $\overline{TO}$ after the corresponding event.

FIGURE 3.7 - STATUS REGISTER



ADDRESS: 03h
RESET CONDITION: 000??XXX
TO, PD are set or reset as shown in Table 3.1

CARRY/$\overline{\text{BORROW}}$ BIT:
For ADDWF, SUBWF , ADDLW and SUBLW instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
Note that a subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

DIGIT CARRY/$\overline{\text{BORROW}}$ BIT:
For ADDWF, SUBWF , ADDLW and SUBLW instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

ZERO BIT:
Set if the result of an arithmetic or logic operation is zero. Reset otherwise.

POWER DOWN BIT:
Set to "1" during power up or by a CLRWDT command. This bit is reset to "0" by a SLEEP instruction.

TIME-OUT BIT:
Set to "1" during power up and by the CLRWDT and SLEEP command. This bit is reset to "0" by a watchdog timer time out.

REGISTER PAGE SELECT BITS FOR DIRECT ADDRESSING:

RP1,0: 00 : page 0 (00h - 7Fh)
01 : page 1 (80h - FFh)
10 : page 2 (100h - 17Fh)
11 : page 3 (180h - 1FFh)

Each page is 128 bytes.
Only RP0 is useful in PIC16C71. Bit RP1 can be used as a general purpose read/write bit. However, this may affect upward compatibility with future products.

REGISTER PAGE SELECT BITS FOR INDIRECT ADDRESSING:

IRP: 0 : page 0,1 (00h - FFh)
1 : page 2,3 (100h - 1FFh)

This bit is effectively not used in the PIC16C71.
It may be used as a general purpose read/write bit However, this may affect upward compatibility with future product.

TABLE 3.3 - $\overline{\text{PD}}$/$\overline{\text{TO}}$ STATUS AFTER RESET

$\overline{\text{TO}}$	$\overline{\text{PD}}$	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT timeout (not during SLEEP)
U	0	$\overline{\text{MCLR}}$ wake up from SLEEP
1	1	Power-up
U	U	$\overline{\text{MCLR}}$ reset during normal operation

U: unchanged
Note: The $\overline{\text{PD}}$ and $\overline{\text{TO}}$ bit maintain their status until an event of Table 3.2 occurs. A low-pulse on the $\overline{\text{MCLR}}$ input does not change the $\overline{\text{PD}}$ and $\overline{\text{TO}}$ status bits.

3.10 Arithmetic and Logic Unit (ALU)

The ALU is 8-bit wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register) or the accumulator. The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

3.11 W Register

The W register is an 8-bit working register (or accumulator) used for ALU operations. It is not an addressable register.

3.12 Interrupts

The PIC16C71 has four sources of interrupt:

- External interrupt from RB0/INT pin
- Timer0 timer/counter overflow interrupt
- End of conversion interrupt from A/D module
- Interrupt on change on RB<7:4> pins

The interrupt control register (INTCON, addr 0Bh) records individual interrupt requests in flag bits. It also has individual and global enable bits. The A/D conversion completion interrupt flag (ADIF) resides in the ADCON<1> register.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. GIE is cleared on reset.

The `RETFIE` instruction allows user to return from interrupt and enable interrupt at the same time.

The INT pin interrupt, the RB port change interrupt and the RTCC overflow interrupt flags are contained in the INTCON register.

When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. Once in the interrupt service routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in the software before re-enabling interrupts to avoid recursive interrupts.

3.12.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising (if INTEDG = 1, OPTION<6>) or falling (if INTEDG = 0). When a valid edge appears on INT pin, INTF bit is set (INTCON<1>). This interrupt can be disabled by setting INTE control bit (INTCON<4>) to '0'. INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake up the processor from SLEEP if INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See section 5.5 for details on SLEEP and Figure 4.11 for timing of wake-up from SLEEP through INT interrupt.

Note 1: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

Note 2: If an interrupt occurs while the Global Interrupt Enable (GIE) bit is being cleared, the GIE bit may unintentionally be re-enabled by the user's Interrupt Service Routine (the `RETFIE` instruction). The events that would cause this to occur are:

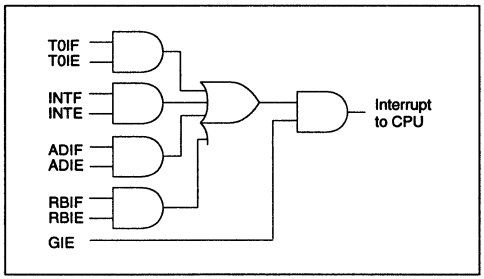
1. An instruction clears the GIE bit while an interrupt is acknowledged
2. The program branches to the interrupt vector and executes the Interrupt Service Routine.
3. The Interrupt Service Routine completes with the execution of the `RETFIE` instruction. This causes the GIE bit to be set (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.

The method to ensure that interrupts are globally disabled is:

1. Ensure that the GIE bit was cleared by the instruction, as shown in the following code:

```
LOOP  BCF   INTCON, GIE  ; Disable Global
                         ;   Interrupts
      BTFSC INTCON, GIE  ; Global Interrupts
                         ;   Disabled?
      GOTO  LOOP         ; NO, try again
      :                  ; Yes, continue
                         ;   with program
                         ;     flow
```

FIGURE 3.8 - INTERRUPT LOGIC



3.12.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. See Section 6.4 for details.

3.12.3 PORT RB INTERRUPT

An input change on PORTB <7:4> will set the RBIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing RBIE (INTCON<4>) bit. See Section 6.2 for details.

3.12.4 A/D INTERRUPT

The A/D converter sets the end of conversion interrupt flag, ADIF (ADCON<1>) when a conversion is complete. The interrupt can be disabled by clearing ADIE bit (INTCON<6>). See Section 6.6 for details on A/D interrupt.

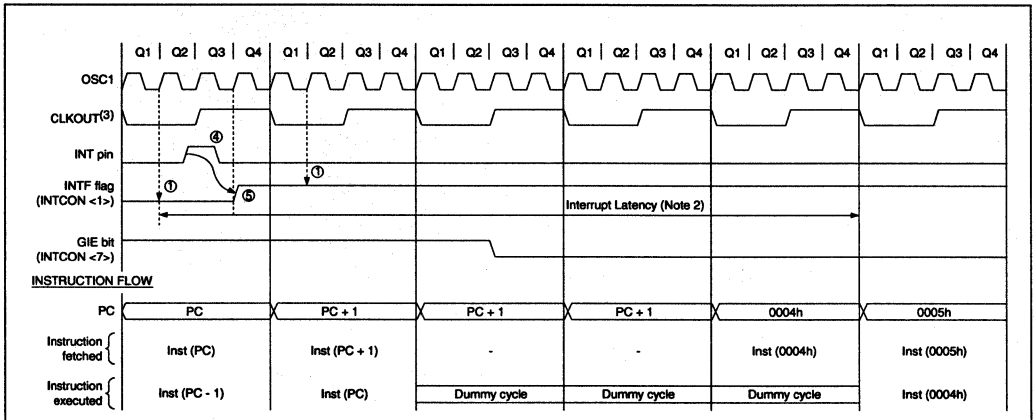
3.13 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt e.g. W register and status register. This will have to be implemented in software.

EXAMPLE 3-1: SAVING W REGISTER AND STATUS IN RAM

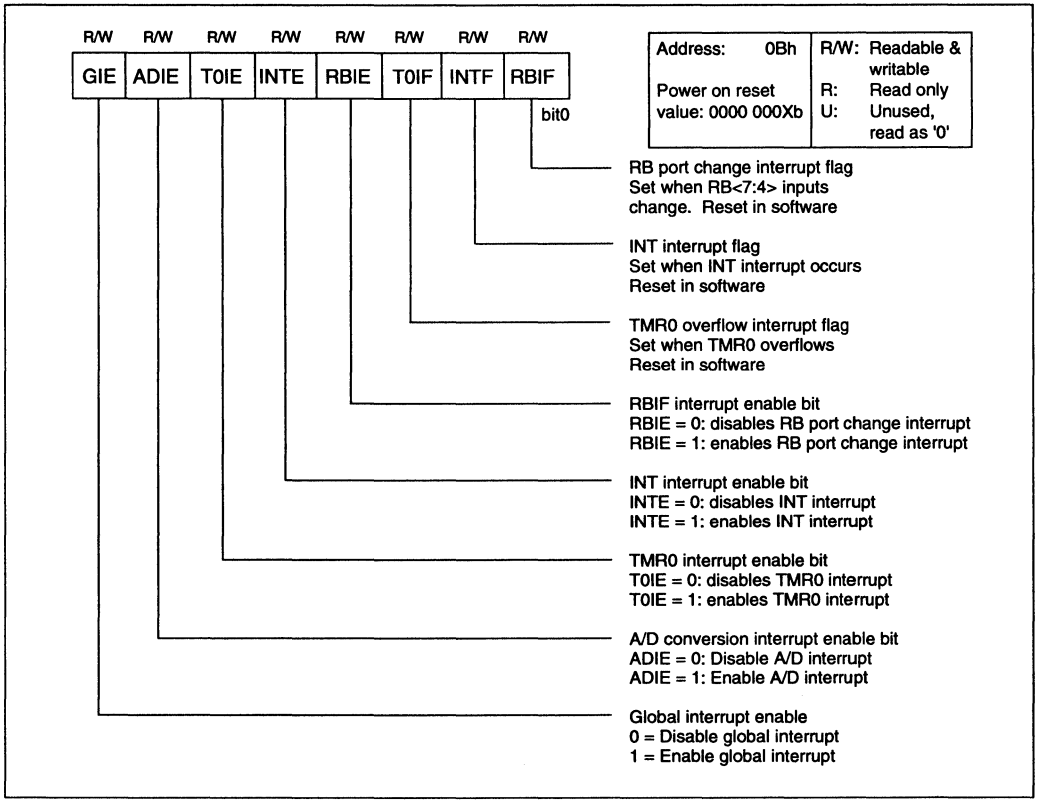
```
push:   movwf    temp_w          ;Saving Values
        swapf    STATUS,W        ;
        movwf    temp_stat       ;
        :                        ;Interrupt
        :                        ; Service Routine
pop:    swapf    temp_stat,W     ;Restoring
                                 ; Values
        movwf    STATUS          ;
        swapf    temp_w, F       ;Do not want to
        swapf    temp_w, W       ;  affect Z-bit
```

FIGURE 3.9 - INT PIN INTERRUPT TIMING



Notes:
1. INTF flag is sampled here (every Q1)
2. Interrupt latency = 3 - 4 Tcy where Tcy = instruction cycle time.
   Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3. CLKOUT is available only in RC oscillator mode.
4. For minimum width spec of INT pulse, refer to AC specs.
5. INTF is enbled to be set anytime during the Q4-Q1 cycles.

FIGURE 3.10 - INTCON REGISTER



4.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real time applications. The PIC16C71 has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

The PIC16C71 has a Watchdog Timer which can be shut off only through EPROM fuses. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake up from SLEEP through external reset, Watchdog Timer timeout or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of EPROM configuration bits (fuses) are used to select various options (Section 4.6).

4.1 RESET

The PIC16C71 differentiates between various kinds of reset:

a) Power-On Reset (POR)

b) $\overline{\text{MCLR}}$ Reset during normal operation

c) $\overline{\text{MCLR}}$ reset during SLEEP

d) WDT timeout reset during normal operation

e) WDT timeout reset during SLEEP

Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-On Reset (POR), on $\overline{\text{MCLR}}$ or WDT reset during normal operation and on $\overline{\text{MCLR}}$ reset during SLEEP. They are not affected by a WDT reset during SLEEP, since this reset is viewed as the resumption of normal operation. There are a few exceptions to this. The PC is always reset to all 0's (0000h). Finally, $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different reset situations as indicated in Section 3.9.1. These bits are used in software to determine the nature of reset. See Table 4.1 for a full description of reset states of all registers.

4.2 Power-On Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)

Power-On Reset (POR): A Power-On Reset pulse is generated on-chip when V_{DD} rise is detected (in the range of 1.2V - 1.8V). To take advantage of the POR, just tie MCLR pin directly (or through a resistor) to V_{DD}. This will eliminate external RC components usually needed to create Power-On Reset.

FIGURE 4.1 - SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

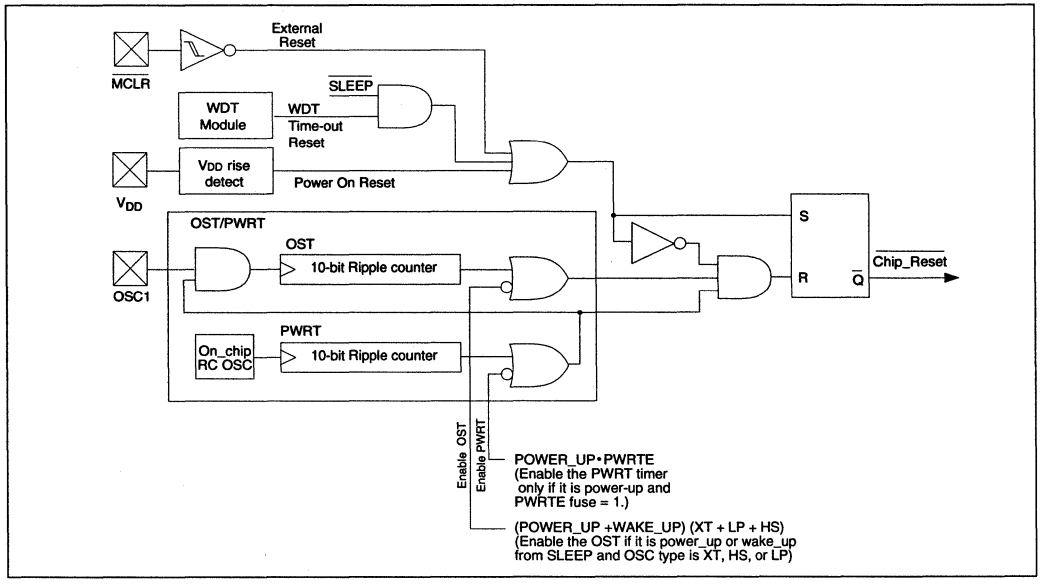


TABLE 4.1 - RESET CONDITIONS FOR REGISTERS

Register	Address	Power-on reset (POR)	WDT time-out reset during normal operation	WDT time-out reset during SLEEP	$\overline{MCLR}$ reset during normal	$\overline{MCLR}$ reset during SLEEP	Wake-up through interrupt
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
INDIR	00h	-	-	-	-	-	-
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PC	02h	0000h	0000h	PC + 1	0000h	0000h	PC + 1
STATUS	03h	0001 1xxx	0000 1uuu	uuu0 0uuu	000u uuuu	000u 0uuu	uuu1 0uuu
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PORT A	05h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TRIS A	85h	---1 1111	---1 1111	---u uuuu	---1 1111	---1 1111	---u uuuu
TRIS B	86h	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111	uuuu uuuu
OPTION	81h	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111	uuuu uuuu
ADCON0	08h	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu
ADCON1	88h	---- --00	---- --00	---- --uu	---- --00	---- --00	---- --uu
ADRES	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu	0000 000u	0000 0000	uuuu uuuu*

Legend: - = unimplemented, reads as '0'
u = unchanged
x = unknown

* In the event of wake-up through interrupt, one or more of the interrupt flags will be set. Other bits in INTCON will remain unchanged.

The POR circuit does not produce internal reset when VDD declines (or goes through a brown-out).

Power-up Timer (PWRT): The Power-up Timer provides a fixed 72ms time-out on power-up only, from POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration fuse, PWRTE can enable (if = 1) or disable (if = 0 or programmed) the Power-up Ttimer (Section 4.6).

The power-up time delay will vary from chip to chip due to VDD and temperature. See DC parameters for details.

Oscillator Start-up Timer (OST): The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This guarantees that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-On Reset or wake-up from SLEEP.

Time-out Sequence: On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and PWRTE fuse status. For example, in RC mode with PWRTE set to '0' (PWRT disabled), there will be no time-out at all. Figures 4.2 and 4.3 depict time-out sequences.

Since the time-outs occur from POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately. This is useful for testing purposes or to synchronize more than one PIC16C71 operating in conjunction.

TABLE 4.2 - TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Wake up from SLEEP
	PWRTE = 1	PWRTE = 0	
XT, HS, LP	72 ms + 1024 tosc	1024 tosc	1024 tosc
RC	72 ms	-	-

FIGURE 4.2 - TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): Case 1

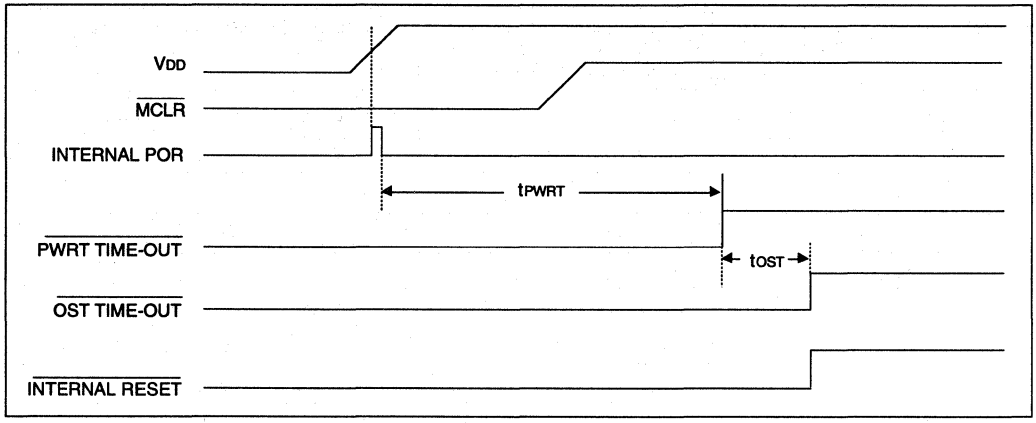


FIGURE 4.3 - TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): Case 2

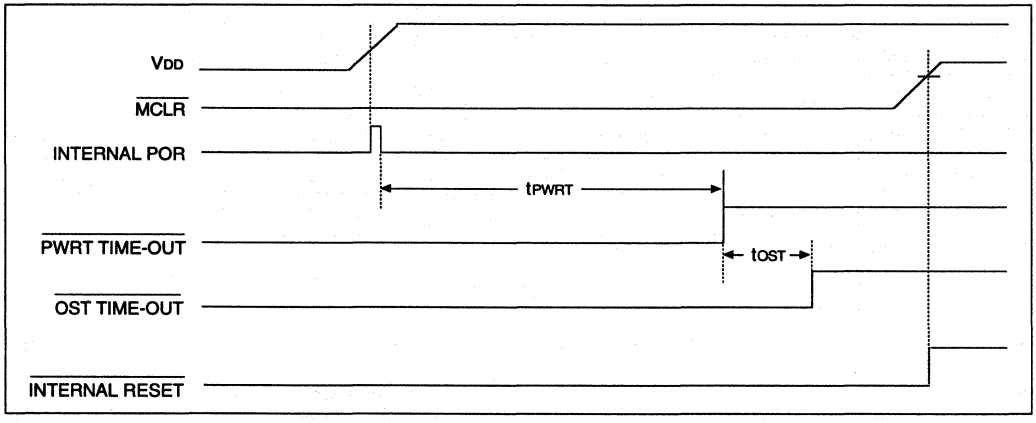


FIGURE 4.4 - TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

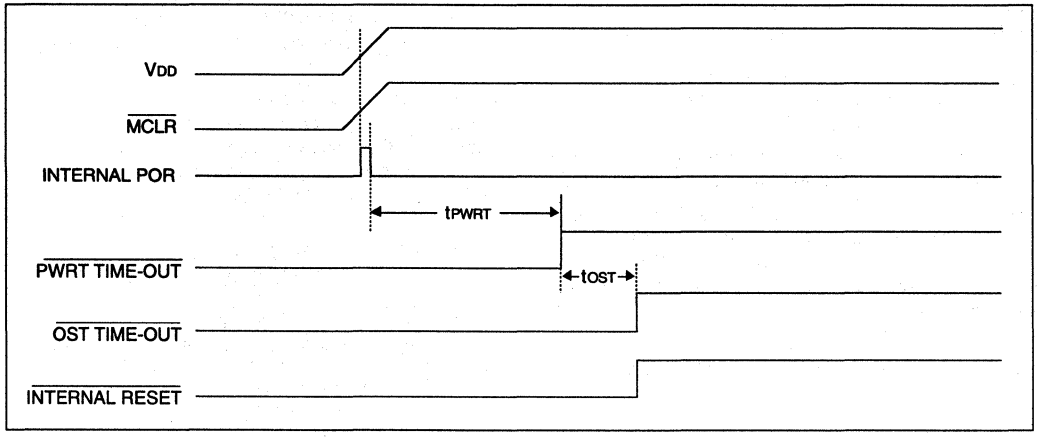
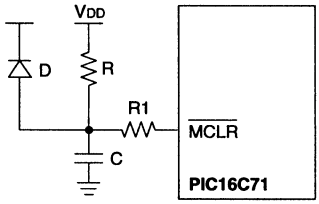
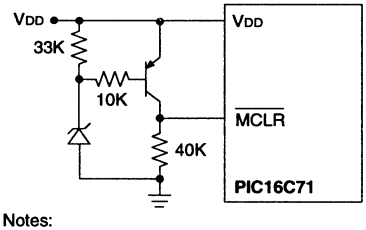


FIGURE 4.5 - EXTERNAL POWER ON RESET CIRCUIT (FOR SLOW VDD POWER UP)



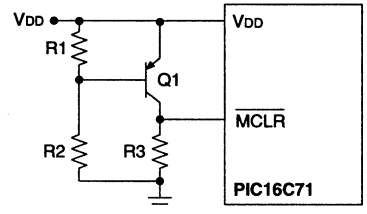
Notes:
1. External power on reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40KΩ is recommended to make sure that voltage drop across R does not exceed 0.2V (max leakage current spec on $\overline{MCLR}$ pin is 5μA). A larger voltage drop will degrade VIH level on $\overline{MCLR}$ pin.
3. R1 = 100Ω to 1KΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$ pin breakdown due to ESD or EOS.

FIGURE 4.6 - BROWN OUT PROTECTION CIRCUIT 1



Notes:
1. This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

FIGURE 4.7 - BROWN OUT PROTECTION CIRCUIT 2



Notes:
1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V.$$

4.3 Watchdog Timer (WDT)

The Watchdog Timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by programming the configuration fuse WDTE as a '0' (Section 4.6).

4.3.1 WDT PERIOD

The WDT has a nominal time-out period of 18ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The "CLRWDT" and "SLEEP" instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit $\overline{TO}$ in the STATUS register will be cleared upon a Watchdog Timer time-out.

4.3.2 WDT PROGRAMMING CONSIDERATIONS

In a noisy application environment the OPTION register can get corrupted. The OPTION register should be updated at regular intervals.

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

4.4 Oscillator Configurations

4.4.1 OSCILLATOR TYPES

The PIC16C71 can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power
- XT Crystal
- HS High Speed
- RC Resistor/Capacitor

4.4.2 CRYSTAL OSCILLATOR

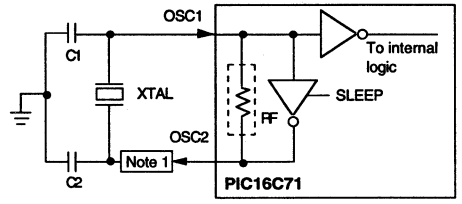
In XT, HS, or LP modes a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 4.8).

TABLE 4.3 - CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	150 - 330 pF
	2.0 MHz	20 - 330 pF
	4.0 MHz	20 - 330 pF
HS	8.0 MHz	20 - 200 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

FIGURE 4.8 - CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



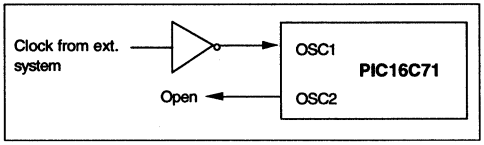
See Tables 4.3 and 4.4 for recommended values of C1 and C2.
Note 1: A series resistor may be required for AT strip cut crystals.

TABLE 4.4 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	15 pF	15 pF
	100 KHz	15 pF	15 pF
	200 KHz	15 pF	15 pF
XT	100 KHz	15 - 30 pF	200 - 300 pF
	200 KHz	15 - 30 pF	100 - 200 pF
	455 KHz	15 - 30 pF	15 - 100 pF
	1 MHz	15 - 30 pF	15 - 30 pF
HS	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	16 MHz	15 pF	15 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

FIGURE 4.9 - EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP OSC CONFIGURATION)



4.4.3 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 4.10 shows how the R/C combination is connected to the PIC16C71. For Rext values below 2.2 kOhm, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 kOhm and 100 kOhm.

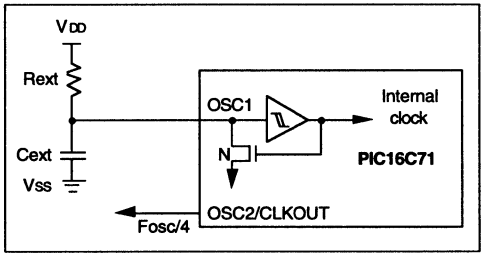
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See the table in Section 10.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See the characteristics in Section 9.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3.1 for timing).

FIGURE 4.10 - RC OSCILLATOR (RC TYPE ONLY)



4.5 Power Down Mode (SLEEP)

The power down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the bit $\overline{PD}$ in the STATUS register is cleared, the $\overline{TO}$ bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low, or hi-impedance).

For lowest curent consumption in this mode, all I/O pins should be either at V_{DD}, or V_{SS}, with no external circuitry drawing current from the I/O pin. I/O pins that are in the High-Z mode should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC input should also be at V_{DD} or V_{SS} for lowest current consumption. The contribution from on chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (V_{IHMC}).

It should be noted that a RESET generated by a WDT time out does not drive $\overline{MCLR}$ pin low.

4.5.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

a. External reset input on $\overline{MCLR}$ pin

b. Watchdog timer timeout reset (if WDT was enabled)

c. Interrupt from INT pin, RB port change or A/D converter.

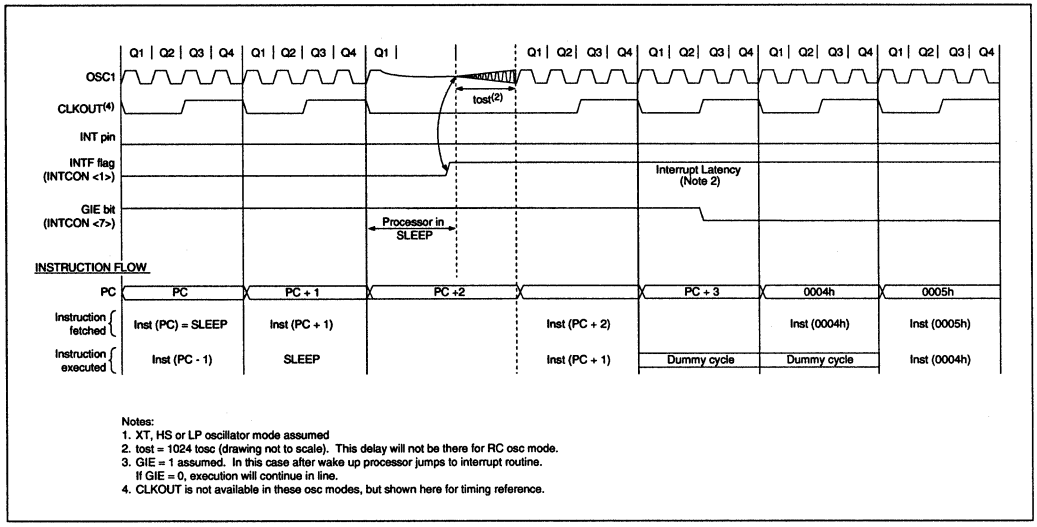
The first event will cause a device reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. $\overline{PD}$ bit, which is set on power-up is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if WDT time-out occurred (and caused wake-up).

When the `SLEEP` instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the GIE bit is set (enabled), the device executes the instruction after the `SLEEP` instruction and the branches to the interrupt address (0004h). In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

Note: If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake from sleep.

The WDT is cleared when the device wakes-up from sleep, regardless of the source of wake-up.

FIGURE 4.11 - WAKE UP FROM SLEEP THROUGH INTERRUPT



Notes:
1. XT, HS or LP oscillator mode assumed
2. tost = 1024 tosc (drawing not to scale). This delay will not be there for RC osc mode.
3. GIE = 1 assumed. In this case after wake up processor jumps to interrupt routine. If GIE = 0, execution will continue in line.
4. CLKOUT is not available in these osc modes, but shown here for timing reference.

4.6 Configuration Fuses

The PIC16C71 has five configuration fuses which are EPROM bits. These fuses can be programmed (reads '0') or left unprogrammed (reads '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh). However, through a special mode, this location can be accessed during programming.

See the description of fuses in Figure 4.12.

4.7 ID LOCATIONS

The PIC16C71 has four ID locations (2000h - 2003h) mapped in the test program memory for storing code revision number, manufacturing information or other useful information. As with the configuration word, these locations are readable and writable through a programmer. They are not accessible during normal code execution.

If the chip is code protected, it is recommended that the user uses only the lower seven bits of the ID locations and program the higher seven bits as '1'. This way the ID locations will be readable even after code protection.

4.8 Code Protection

The code in the program memory can be protected by blowing the code protect fuse (CP).

When code protected, the contents of the program memory cannot be read out in a way that the program code can be reconstructed. In addition, all memory locations starting at 0040h and above are protected against programming.

It is still possible to program locations 0000h - 003Fh, the ID locations and the configuration fuses.

Note: The configuration fuses and the ID bits can still be read in code protect mode.

4.8.1 VERIFYING A CODE-PROTECTED PIC16C71

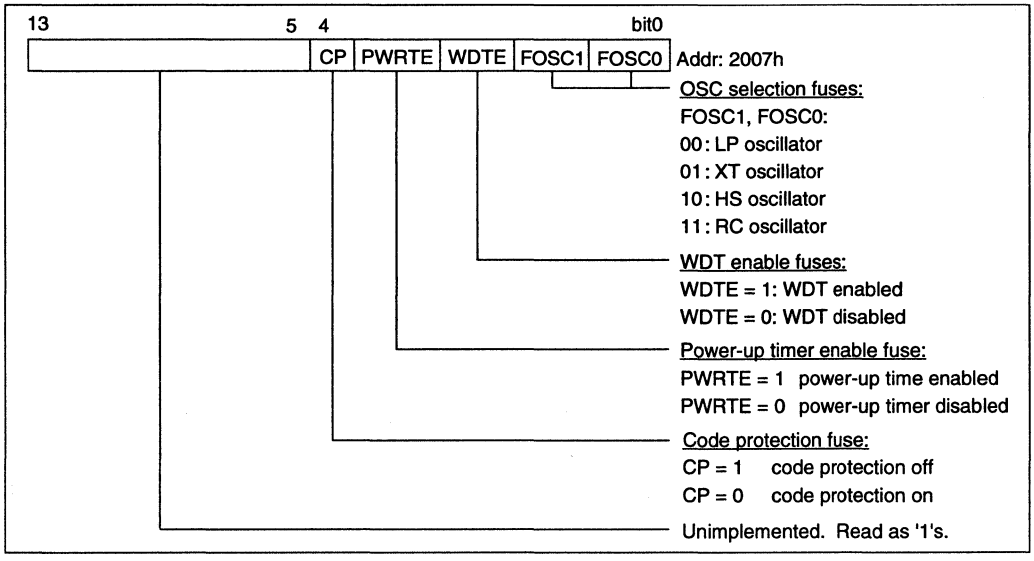
When code protected, verifying any program memory location will read a scrambled output which looks like "0000000xxxxxxx" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

a. First, program and verify a good device without code protecting it.

b. Next, blow its code protection fuse and then load its contents in a file.

c. Verify any code-protected PIC16C71 against this file.

FIGURE 4.12 - CONFIGURATION WORD



5.0 OVERVIEW OF PERIPHERALS

The PIC16C71 has 13 I/O pins organized as two I/O ports, PORTA (5 bit) and PORTB (8-bit). It has an 8-bit timer/counter (RTCC) with a programmable 8-bit prescaler and an analog to digital converter module. The A/D converter has up to four analog inputs, internal or external reference, 8-bit resolution and a typical 20µs conversion time.

5.1 PORTA

PORTA is a 5-bit wide port with pins RA0 - RA4. Port pins RA<3:0> are bidirectional whereas RA4 has a open-collector output. PORTA is file register 05h. Its corresponding direction control register TRISA is mapped in page 1 of register file at address 85h. TRISA is a five-bit wide register with bits <4:0>. Refer to Figure 5.1 and Figure 5.2 for block diagrams of PORTA pins.

Pins RA<3:0> are multiplexed with analog input channels AIN3 - AIN0. Pin RA3 is further multiplexed with external reference voltage VREF for the A/D. Two bits in control register ADCON1 (file register 88h) are used to configure these pins as digital (i.e. port) or analog pins. When configured as analog inputs, these pins will read as '0's. Upon power-on reset, RA<3:0> are configured as analog inputs.

RA4 should be tied to either VDD or VSS in order to present excessive current being drawn by a floating Schmitt trigger input (see Figure 5.2).

FIGURE 5.1 - BLOCK DIAGRAM OF RA0 - RA3 PINS

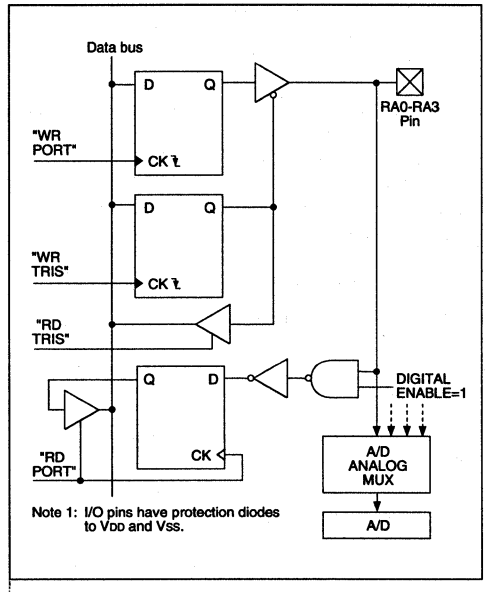


TABLE 5.1 - PORTA FUNCTIONS

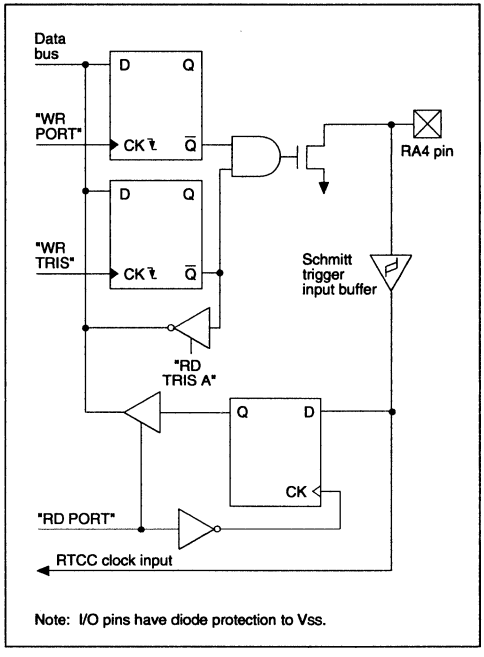
Port Pin	Bit	Pin Function	Alternate Function
RA0/AIN0	bit0	Input/output port. TTL input levels	Analog input channel 0
RA1/AIN1	bit1	Input/output port. TTL input levels	Analog input channel 1
RA2/AIN2	bit2	Input/output port. TTL input levels	Analog input channel 2
RA3/AIN3/VREF	bit3	Input/output port. TTL input levels	Analog input channel 3 or external reference voltage input (VREF)
RA4/T0CKI	bit4	Input/output port. Output is open collector type. Input is Schmitt trigger type.	External clock input for TMR0 timer/counter

TABLE 5.2 - SUMMARY OF PORTA REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTA	PORTA pins when read PORTA latch when written	05h	---X XXXX
TRISA	PORTA data direction register	85h	---1 1111
ADCON1	A/D converter control register	88h	---- --00

Notes: 1: x = unknown, - = unimplemented, reads as a '0'.
2: For reset values of registers in other reset situations refer to Table 4.1.

FIGURE 5.2 - BLOCK DIAGRAM OF RA4 PIN



Note: I/O pins have diode protection to Vss.

5.2 PORTB

PORTB is an 8-bit wide bidirectional port (file register address 06h). The corresponding data direction register is TRISB (address 86h). A '1' in TRISB sets the corresponding port pin as an input. Reading PORTB register reads the status of the pins whereas writing to it will write to the port latch. See Figures 5.3 and 5.4 for block diagrams of PORTB pins.

Each of the PORTB pins has a weak internal pull-up (~250µA typical). The weak pull-up is automatically turned off if the port pin is configured as an output. Furthermore, bit RBPU (OPTION<7>) can turn off (RBPU is set) all the pull-ups. The pull-ups are disabled on power on reset.

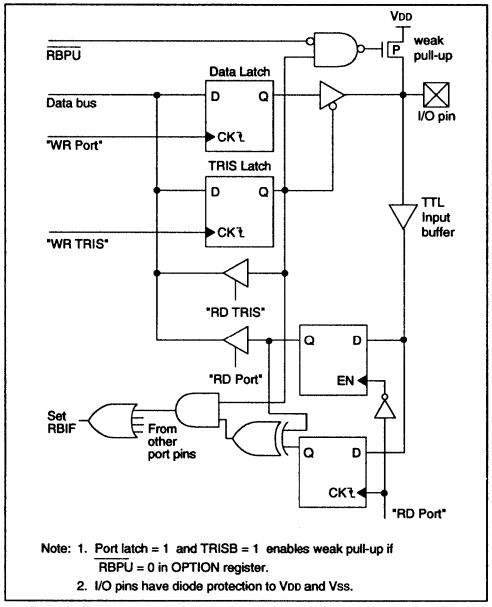
PORTB has an interrupt on change feature on four of its pins, RB<7:4>. When configured as input, the inputs on these pins are sampled and latched every Q1. The new input is compared with the old latched value in every instruction cycle. An active high output is generated on mismatch between the pin and the latch. The "mismatch" outputs of RB4, RB5, RB6 and RB7 are OR'ed together to generate the RBIF interrupt (latched in INTCON<0>). Any pin configured as output is excluded from the comparison. This interrupt can wake the chip up from SLEEP. The user, in interrupt service routine can clear the interrupt in one of two ways:

a) Disable the interrupt by clearing RBIE (INTCON<3>) bit.
b) Read PORTB. This will end mismatch condition, then clear RBIF bit.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression.

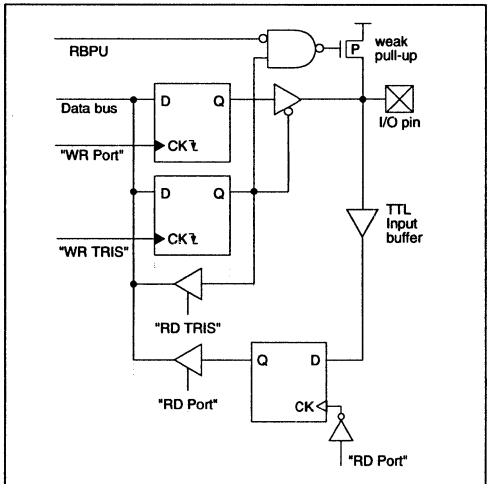
Finally, port pin RB0 is multiplexed with external interrupt input INT.

FIGURE 5.3 - BLOCK DIAGRAM OF PORT PINS RB<7:4>



Note: 1. Port latch = 1 and TRISB = 1 enables weak pull-up if RBPU = 0 in OPTION register.
2. I/O pins have diode protection to VDD and Vss.

FIGURE 5.4 - BLOCK DIAGRAM OF PORT PINS RB<3:0>



Notes: 1. DDR = 1 enables weak pull-up if RBPU = 0 in OPTION register.
2. I/O pins have diode protection to VDD and Vss.

TABLE 5.3 - PORTB FUNCTIONS

Port Pin	Bit	Pin Function	Alternate Function
RB0/INT	bit0	Input/output port pin. TTL input levels and internal software programmable weak pull-up	External interrupt input (Schmitt Trigger)
RB1	bit1	Input/output port pin. TTL input levels and internal software programmable weak pull-up	-
RB2	bit2	Input/output port pin. TTL input levels and internal software programmable weak pull-up	-
RB3	bit3	Input/output port pin. TTL input levels and internal software programmable weak pull-up	-
RB4	bit4	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change
RB5	bit5	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change
RB6	bit6	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change
RB7	bit7	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change

TABLE 5.4 - SUMMARY OF PORTB REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTB	PORTB pins when read PORTB latch when written	06h	xxxx xxxx
TRISB	PORTB data direction register	86h	1111 1111
OPTION	Weak pull-up on/off control ($\overline{RBPU}$ bit) See Figure 5.12	81h	1111 1111

5.3 I/O PROGRAMMING CONSIDERATIONS

5.3.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of f6 (PORTB) will cause all eight bits of f6 to be read into the CPU. Then the BSF operation takes place on bit 5 and f6 is re-output to the output latches. If another bit of f6 is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

Reading the PORT register, reads the values of the PORT pins. Writing to the PORT register writes the value to the PORT latch. When using read modify write instructions (ex. BCF, BSF, etc.) on a PORT, the value of the PORT pins is read, the desired operation is done to this value, and this value is then written to the PORT latch.

Example 5-1 shows the effect of two sequential read modify write instructions (ex. BCF, BSF, etc.) on an I/O PORT.

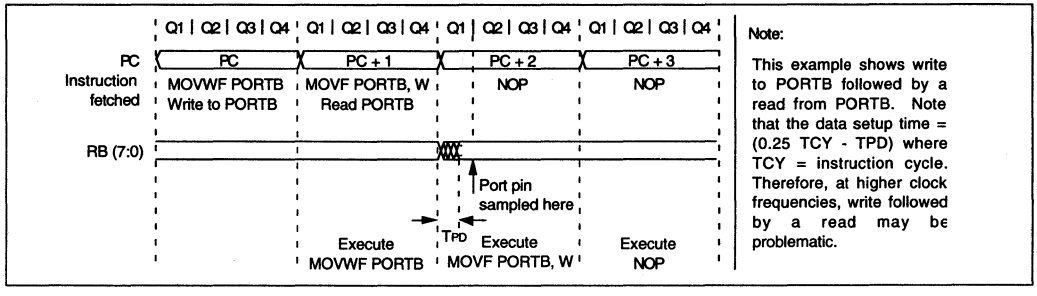
EXAMPLE 5-1: READ MODIFY WRITE INSTRUCTIONS ON AN I/O PORT

```
; Initial PORT settings:  PORTB<7:4> Inputs
;                         PORTB<3:0> Outputs
; PORTB<7:6> have external pull-up and are NC
;
;                           PORT latch   PORT pins
;                           ----------   ----------
      BCF     PORTB, 7    ; 01pp pppp    11pp pppp
      BCF     PORTB, 6    ; 10pp pppp    11pp pppp
      BSF     STATUS, RP0 ;
      BCF     TRISB, 7    ; 10pp pppp    11pp pppp
      BCF     TRISB, 6    ; 10pp pppp    10pp pppp
;
; Note that the user may have expected the pin
; values to be 00pp pppp. The 2nd BCF caused RB7
; to be latched as the pin value (High).
```

5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see Figure 5.5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

FIGURE 5.5 - SUCCESSIVE I/O OPERATION



Note:

This example shows write to PORTB followed by a read from PORTB. Note that the data setup time = (0.25 TCY - TPD) where TCY = instruction cycle. Therefore, at higher clock frequencies, write followed by a read may be problematic.

5.4 TIMER0 (TMR0) Module

The TMR0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable (file address 01h)
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

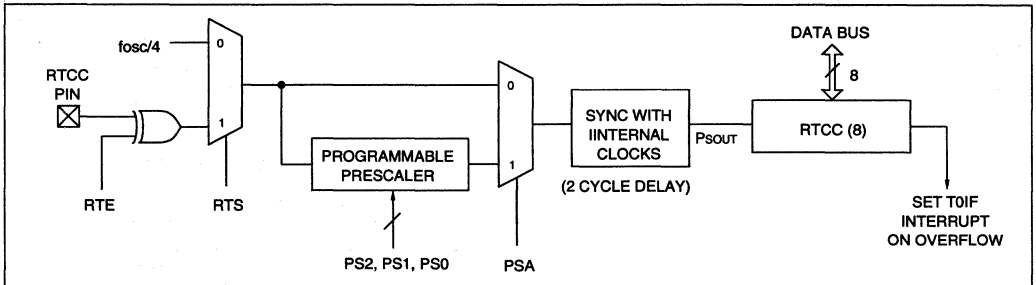
Figure 5-6 is a simplified block diagram of the TMR0 module.

Timer mode is selected by clearing the RTS bit (OPTION<5>). In timer mode, the TMR0 module will increment every instruction cycle (without prescaler). If TMR0 is written, increment is inhibited for the following two cycles (see Figures 5-7 and 5-8). The user can work around this by writing an adjusted value to the TMR0 module.

Counter mode is selected by setting the RTS bit (OPTION<5>). In this mode TMR0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by control bit RTE (OPTION<4>). Clearing the RTE bit selects the rising edge. Restrictions on the external clock input is discussed in detail in Section 5.4.2.

The prescaler is shared between the TMR0 module and the watchdog timer. The prescaler assignment is controlled in software by control bit, PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to TMR0. The prescaler is not readable or writable. When the prescaler is assigned to the TMR0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 5.4.3 details the operation of the prescaler.

FIGURE 5-6: TIMER0 (TMR0) BLOCK DIAGRAM



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 AND PSA are located in OPTION register.
2. The prescaler is shared with Watchdog Timer (refer to Figure 7–6 for detailed diagram).

FIGURE 5-7: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALE

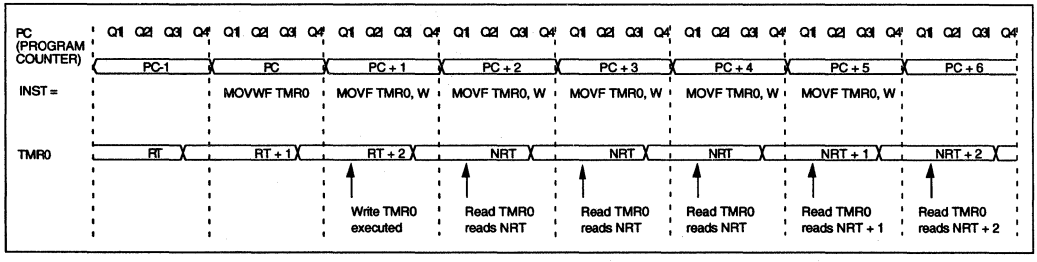
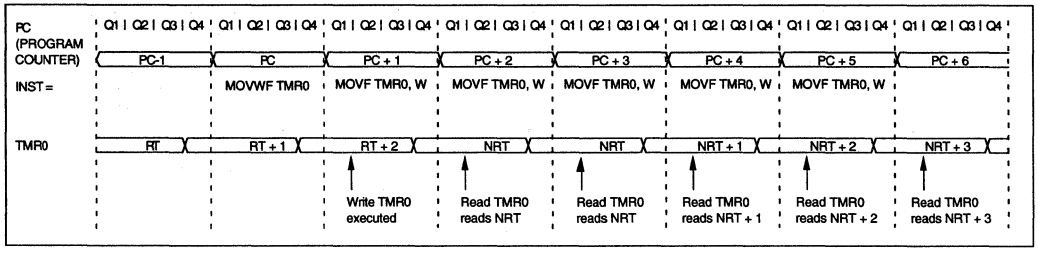


FIGURE 5-8: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/PRESCALE 1:2



4.5.1 TIMER0 (TMR0) Interrupt

TMR0 interrupt is generated when the TMR0 module timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the TMR0 module interrupt service routine before re-enabling this interrupt. The TMR0 module interrupt cannot wake the processor from SLEEP since the timer is shut off during SLEEP. See Figure 5-9 for TMR0 interrupt timing.

4.5.2 Using TMR0 with external clock

When external clock input is used for TMR0, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements.

Also there is some delay from the occurance of the external clock edge to the actual incrementing of TMR0. Referring to Figure 5-10, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where:

tosc = oscillator time period.

When no prescaler is used, PSOUT (Prescaler output, see Figure 5-6) is the same as TMR0 clock input and therefore the requirements are:

T_{RTH} = TMR0 high time ≥ 2tosc + ΔT (See parameter #40)

T_{RTL} = TMR0 low time ≥ 2tosc + ΔT (See parameter #41)

When prescaler is used, the TMR0 module input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.

Then:

$$P_{SOUT}\text{ high time} = P_{SOUT}\text{ low time} = \frac{N \cdot T_{RT}}{2}$$

where

T_{RT} = TMR0 input period

N = prescale value (2, 4, ..., 256).

The requirement is, therefore:

$$\frac{N \cdot T_{RT}}{2} \geq 2\,tosc + \Delta T, \text{ or } T_{RT} \geq \frac{4\,tosc + 2\,\Delta T}{N}$$

where

ΔT = small RC delay (see Timing Specifications).

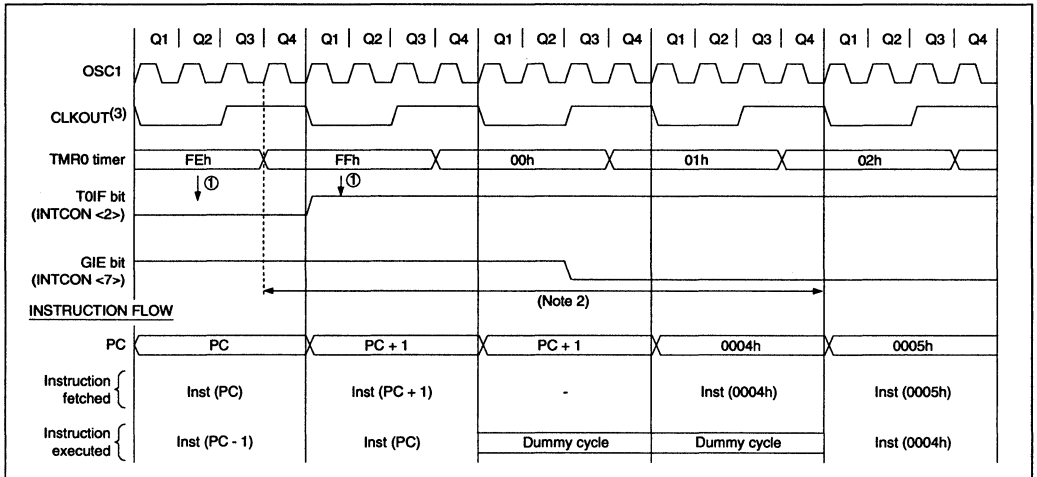
The user will notice that no requirement on TMR0 high time or low time is specified. However, if the high time or low time on TMR0 is too small then the pulse may not be detected, hence a minimum high or low time of 10ns is required. In summary, the TMR0 module input requirements are:

T_{RT} = TMR0 period ≥ (4 tosc + 2 ΔT)/N

T_{RTH} = TMR0 high time ≥ ΔT

T_{RTL} = TMR0 low time ≥ ΔT

FIGURE 5-9: TIMER0 (TMR0) INTERRUPT TIMING



Notes:
1. T0IF interrupt flag is sampled here (every Q1).
2. Interrupt latency = 4 Tcy where Tcy = instruction cycle time.
3. CLKOUT is available only in RC oscillator mode.

Delay from external clock edge: Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 module is actually incremented. Referring to Figure 5-10, the reader can see that this delay is between 3 tosc and 7 tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±200ns @ 20 MHz).

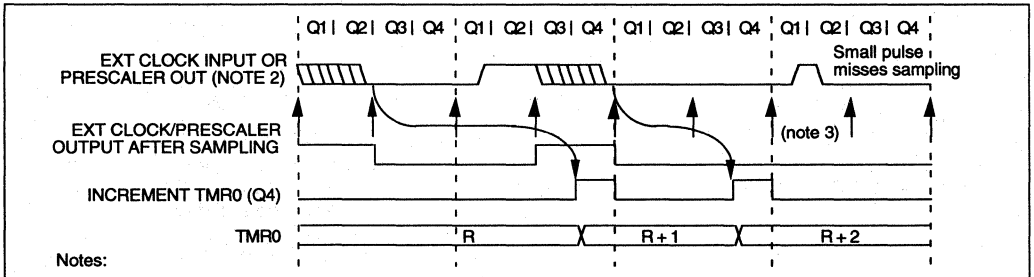
5.4.3 Prescaler

An 8-bit counter is available as a prescaler for the TMR0 module, or as a post-scaler for the watchdog timer, respectively (see Figure 5-11). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the TMR0 module and the Watchdog Timer. Thus, a prescaler assignment for the TMR0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2-PS0 bits (OPTION<3:0>) determine the prescaler assignment and pre-scale ratio.

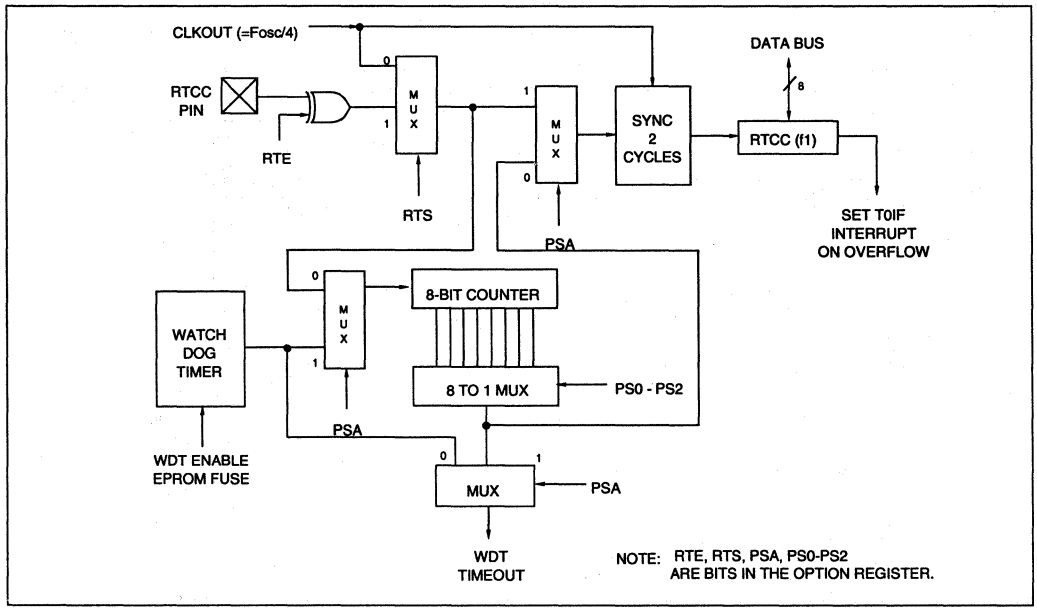
When assigned to the TMR0 module, all instructions writing to the TMR0 module (e.g. CLRF TMR0, MOVWF TMR0, BSF 1,x ....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 5-10: TIMER0 TIMING WITH EXTERNAL CLOCK



Notes:
1. Delay from clock input change to TMR0 increment is 3 tosc to 7 tosc. (Duration of Q = tosc). Therefore, the error in measuring the interval between two edges on TMR0 input = ± 4 tosc max.
2. External clock if no prescaler selected, Prescaler output otherwise.
3. The arrows indicate the points in time where sampling occurs.

FIGURE 5-11: BLOCK DIAGRAM OF THE TMR0/WDT PRESCALER



5.4.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence (shown in Example 5-2) must be executed when changing the prescaler assignment from TMR0 to WDT. Depending on the selected prescaler value (lines 2 and 3) determines if lines 9 and 10 are required:

EXAMPLE 5-2: CHANGING PRESCALER (TMR0→WDT)

```
1. BCF     STATUS, RP0   ;Bank 0
2. CLRF    TMR0          ;Clear TMR0
3. BSF     STATUS, RP0   ;Bank 1
4. CLRWDT                ;Clears WDT and
                         ;   prescale
5. MOVLW   B'xxxx1xxx'   ;Select new prescale
6. MOVWF   OPTION        ;   value
7. BCF     STATUS, RP0   ;Bank 0
```

Note: This method is valid for revision B silicon and greater. Revision A silicon shoudl use the method shown in revision D of the data sheet.

Steps 2 and 3 are only required if an external TMR0 source is used. Steps 9 and 10 are necessary only if the desired prescale value is '000' or '001'.

To change prescaler from the WDT to the TMR0 module use the sequence shown in Example 5-3. This precaution must be taken even if the WDT is disabled.

EXAMPLE 5-3: CHANGING PRESCALER (WDT→TMR0)

```
1. CLRWDT                ;Clear WDT and
                         ;prescaler
2. BSF STATUS, RP0
3. MOVLW B'xxxx0xxx'     ;Select TMR0, new
                         ;prescale value and
                         ;clock source
4. MOVWF OPTION          ;
5. BCF STATUS, RP0
```

2

TABLE 5-5: SUMMARY OF TMR0 REGISTERS

Register Name	Function	Address	Power-on Reset Value
TMR0	Timer/counter register	01h	XXXX XXXX
OPTION	Configuration and prescaler assignment bits for TMR0. See Figure 4-4	81h	1111 1111
INTCON	TMR0 overflow interrupt flag and mask bits See Figure 4-5	0Bh	0000 000X

TABLE 5-6: REGISTERS ASSOCIATED WITH TMR0

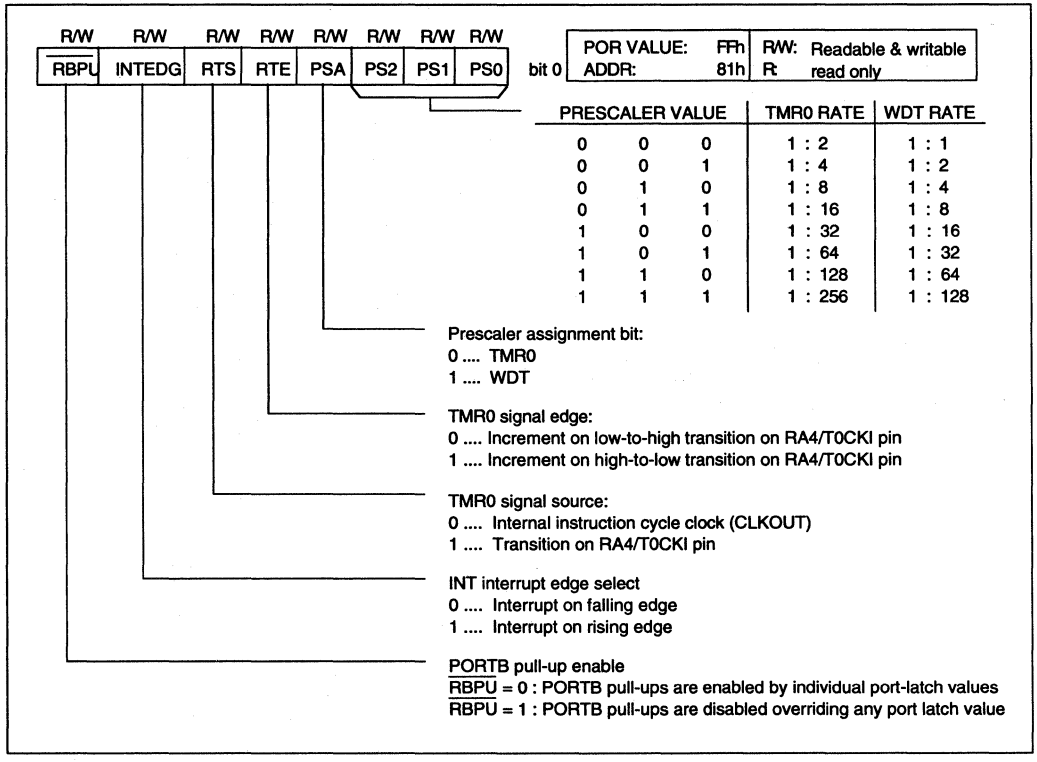
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01	TMR0	TIMER0							
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
81	OPTION	$\overline{\text{RBPU}}$	INTEDG	RTS	RTE	PSA	PS2	PS1	PS0
85	TRISA	—	—	TRISA 5	TRISA 4	TRISA 3	TRISA 2	TRISA 1	TRISA 0

Legend — = Unimplemented locations, Read as '0'
Shaded boxes are not used by TMR0 module.

5.5 OPTION Register

The OPTION register (address 81h) is a readable and writable register which contains various control bits to configure the prescaler, the external INT interrupt, the TMR0 and the weak pull-ups on PORTB.

FIGURE 5.12 - OPTION REGISTER



5.6 A/D converter

The A/D converter module has four analog input channels multiplexed into one sample and hold and A/D converter. Reference voltage VREF can come externally on RA3/AIN3/VREF pin or internally from VDD. The converter itself is a successive approximation type and produces an 8-bit result in the ADRES register (f09h). A conversion is initiated by setting a control bit (GO/DONE , ADCON<2>). Prior to starting conversion, the appropriate channel must be selected and enough time allowed for sampling. The conversion time is a function of the oscillator cycle. The minimum conversion time required is 20µs. At the end of conversion the GO/DONE bit is cleared and the A/D flag interrupt is set (ADIF). The overall accuracy (zero error, full scale error, integral error and quantization error) is less than ±1 LSB for VDD = 5.12V and VREF = VDD. The resolution and accuracy is less when VREF is less than VDD or for VDD less than 5.12V (see specifications for details).

The following steps should be followed in making an A/D conversion:

1) Configure register ADCON1 (see Figure 5.14)
   - Select analog/digital/VREF inputs (ADCON1<1:0>)
2) Configure register ADCON0 (see Figure 5.13)
   - Select A/D conversion clock (ADCON0<7:6>)
   - Select A/D channel (ADCON<4:3>)
   - Turn on A/D module (ADCON0<0>)
3) Configure A/D interrupt (if required)
   - Clear ADIF (ADCON0<1>)
   - Set ADIE (INTCON<6>)
   - Set global interrupt GIE (INTCON<7>)
4) Start conversion
   - Set GO/DONE bit (ADCON0<27>)

Example:

Configure RA0 and RA1 as analog inputs, VREF = VDD, RA2 and RA3 as digital inputs, use A/D interrupt, internal RC clock.

```
BSF     STATUS,5  ;select page 1
MOVLW   00000010B ;configure A/D inputs
MOVWF   ADCON1    ;configure A/D inputs
BCF     STATUS,5  ;select page 0
MOVLW   11000001B ;CH0 = on, clear ADIF
MOVWF   ADCON0    ;tad = trc
MOVLW   11XXXXXXB ;enable A/D interrupts
MOVWF   INTCON    ;and global INT
BSF     ADCON0,2  ;start conversion
```

Note: The GO/DONE bit should not be set in the same instruction which turns on the A/D.

Example:

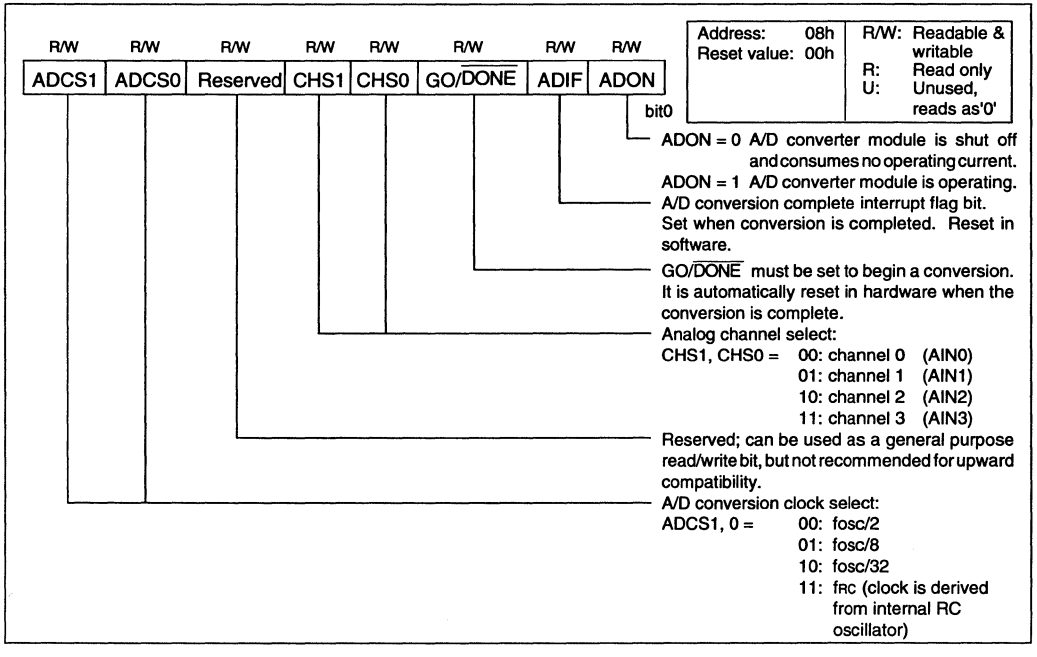
Wrong:

```
MOVLW   B'11000111"
MOVWF   ADCON0
```

Correct:

```
MOVLW   B'11000011'
MOWF    ADCON0
BSF     ADCON0, 2
```

FIGURE 5.13 - A/D CONTROL AND STATUS REGISTER (ADCON0, ADDRESS 08h)



5.6.1 A/D CLOCKING SCHEME

The A/D converter operates on its own clock, tad, derived from either the OSC1 clock input or from its own on-chip RC oscillator as follows:

Control bit ADCS1, ADCS0	tad (must be > 2 μs)
00	2 tosc
01	8 tosc
10	32 tosc
11	tRC (2μs-6μs, 4μs nominal)

The conversion time for each bit is tad. The total conversion time is 10tad. Selection must be made such that tad is at least 2 μs.

At low frequencies, the RC oscillator can be selected to maintain shorter conversion time. The RC oscillator frequency varies considerably with voltage, temperature and process parameters (2μs to 6μs period, nominally 4μs).

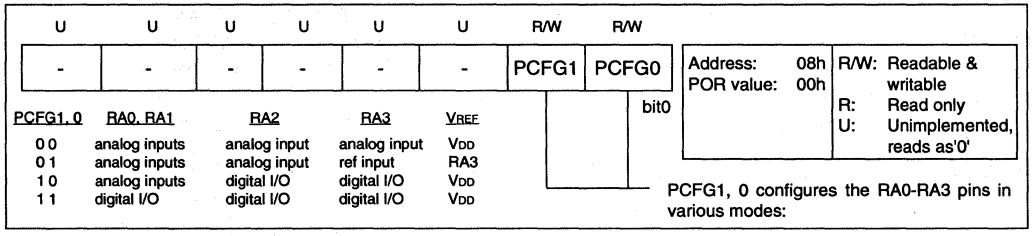
5.6.2 A/D OPERATION DURING SLEEP

To reduce operating current all biasing circuits in the A/D block that consume DC current are shut off when ADON bit is a '0'. If a conversion is in progress using RC oscillator, it will be completed. The ADIF interrupt flag bit will be set and the chip will wake up if the ADIE interrupt enable bit is a '1'. Since, during SLEEP, the switching noise is eliminated, the conversion accuracy will be the maximum possible. This provides a means for getting accurate conversions while operating the processor at high clock rates.

If SLEEP is invoked during a conversion that uses OSC1 clock, the conversion will be aborted. The A/D converter will be shut off. The user must re-initialize the conversion, starting with resampling.

Aside from the "GO" and "ADIF", all configuration bits change only when written to. In A/D RC mode, conversion will wait one instruction cycle after GO bit has been set. This is to allow the processor to execute a sleep instruction before conversion is started.

FIGURE 5.14 - A/D CONTROL REGISTER (ADCON1, ADDRESS 88h)



5.6.3 ANALOG INPUT CONNECTION CONSIDERATIONS

A simplified circuit for an analog input is shown in Figure 5.15. First, the user must configure the TRISA register such that the analog pins are configured as inputs. Second, since the analog pins are connected to digital output, they have reverse biased diodes to VDD and Vss. The analog input, therefore must be between Vss and VDD. If input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10KΩ is recommended for the analog sources. At this impedance, the maximum possible error caused by the leakage current is ±5 mV or ±0.25 LSB at VDD = VREF = 5V (10KΩ x 0.5 μA).

The other reason to limit the maximum source impedance is to be able to capture the analog input voltage on to the holding capacitor. The time constant to charge Chold is (see Figure 5.15):

$= C_{hold}(R_{ic} + R_{SS} + R_S)$ where R_S = source impedance

$\approx 51.2\ pF\ (2K\Omega + R_S)$ $R_{ic} + R_{SS} \approx 2K\Omega$

$\approx 51.2\ pF \times 12K\Omega$ (assuming $R_S = 10K\Omega$)

$= 0.6144\ \mu s = T$

from the capacitive charging equation:

$V_{hold} = V_A (1 - e^{-t/T})$

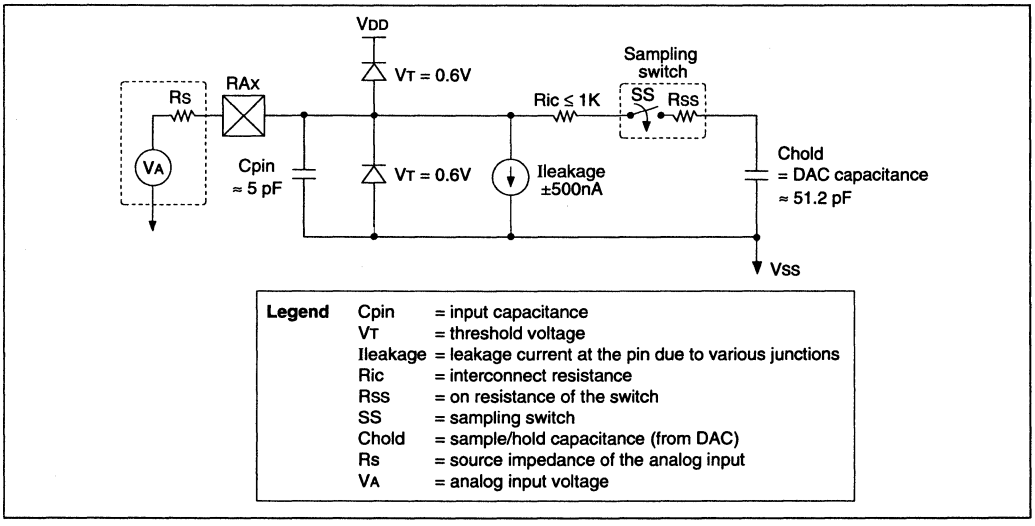
for 1/8 LSB error at VDD = 5V

$e^{-t/T} = \frac{2.5\ mV}{5000\ mV}$

or $t \approx 7.6T = 4.67\mu s$ (required sampling time)

External RC filter is sometimes added for anti-aliasing. Once again, the value of the R should be such that the total source impedance is kept under 10KΩ. Any external component connected to an analog input pin, such as a capacitor or a zener diode, should have very little leakage current.

FIGURE 5.15 - ANALOG INPUT MODEL



Legend		
	Cpin	= input capacitance
	VT	= threshold voltage
	Ileakage	= leakage current at the pin due to various junctions
	Ric	= interconnect resistance
	RSS	= on resistance of the switch
	SS	= sampling switch
	Chold	= sample/hold capacitance (from DAC)
	RS	= source impedance of the analog input
	VA	= analog input voltage

5.6.4 SAMPLE AND HOLD (S/H)

The sample and hold circuit consists of a sampling switch SS (Figure 5.15) and the S/H capacitor whose value is typically 51 pF.

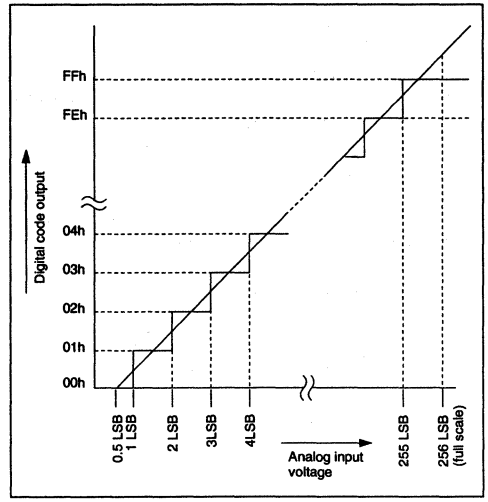
As long as ADON control bit is '1' (bit 0, ADCON 0) and a valid analog input channel is selected, the input will be continuously sampled. There is no command to start or stop sampling. When a conversion is started, sampling is ended and conversion begins on the voltage across the S/H capacitor. The sample and hold, therefore can be more accurately described as "track and hold".

After a conversion is completed, sampling begins after a delay of 2tad. (tad = A/D conversion clock). The user must keep this in mind when allowing for adequate sampling time.

5.6.5 TRANSFER FUNCTION

The ideal transfer function of the A/D converter is as follows: The first transition occurs when input voltage (VA) is 1 LSB (or full scale/256). Figure 5.16 shows the ideal transfer function.

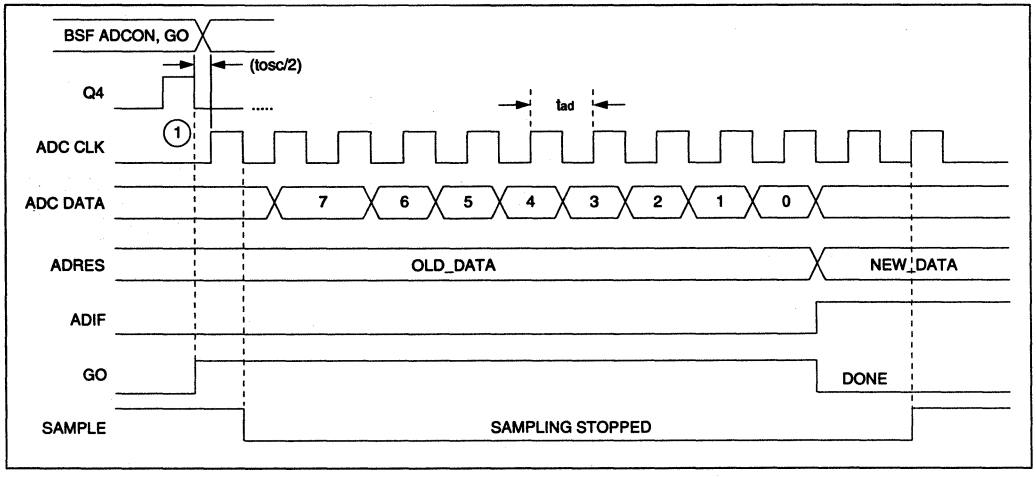
FIGURE 5.16 - TRANSFER FUNCTION



5.6.6 SUMMARY OF A/D REGISTERS

Register name/bits	Function	Address
ADRES	A/D result register	09h
ADCON0	A/D control and status register	08h
ADCON1	A/D control register	88h
INTCON (bit ADIE)	Interrupt control register	0Bh

FIGURE 5.17 - A/D CONVERSION TIMING DIAGRAM



1. For A/D RC mode, this edge is delayed by one instruction cycle to allow the processor to execute a sleep instruction.

6.0 INSTRUCTION SET SUMMARY

Each PIC16C71 instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C71 instruction set summary in Table 6.2 lists byte-oriented, bit-oriented, and literal and control operations. Table 6.1 shows the opcode field descriptions.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which file register is to be utilized by the instruction.

The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or eleven bit constant or literal value.

TABLE 6.1 - OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
PCLATH	Program Counter High Latch
GIE	Global Interrupt Enable Bit
WDT	Watchdog Timer Counter
$\overline{TO}$	Time-out Bit
$\overline{PD}$	Power-down Bit
dest	Destination either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term

The instruction set is highly orthogonal and is grouped into three basic categories:

- Byte oriented operations
- Bit oriented operations
- Literal and control operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Table 6.2 lists the instructions recognized by the MPASM assembler.

Figure 6.1 shows the three general formats that the instructions can have.

Note: To maintain upward compatibility with future PIC16CXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexidecimal number:

0xhh

where h signifies a hexidecimal digit.

FIGURE 6.1 - GENERAL FORMAT FOR INSTRUCTIONS

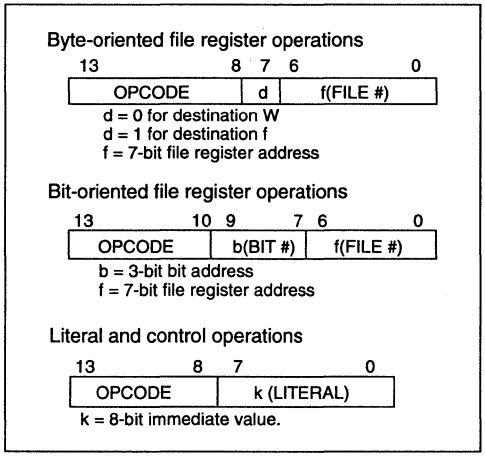


TABLE 6.2 - INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode msb lsb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f, d	Add W and f	1	00 0111 dfff ffff	C, DC, Z	1, 2
ANDWF	f, d	AND W and f	1	00 0101 dfff ffff	Z	1, 2
CLRF	f	Clear f	1	00 0001 1fff ffff	Z	2
CLRW	-	Clear W	1	00 0001 0xxx xxxx	Z	
COMF	f, d	Complement f	1	00 1001 dfff ffff	Z	1, 2
DECF	f, d	Decrement f	1	00 0011 dfff ffff	Z	1, 2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00 1011 dfff ffff		1, 2, 3
INCF	f, d	Increment f	1	00 1010 dfff ffff	Z	1, 2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00 1111 dfff ffff		1, 2, 3
IORWF	f, d	Inclusive OR W and f	1	00 0100 dfff ffff	Z	1, 2
MOVF	f, d	Move f	1	00 1000 dfff ffff	Z	1, 2
MOVWF	f	Move W to f	1	00 0000 1fff ffff		
NOP	-	No Operation	1	00 0000 0xx0 0000		
RLF	f, d	Rotate left f through carry	1	00 1101 dfff ffff	C	1, 2
RRF	f, d	Rotate right f through carry	1	00 1100 dfff ffff	C	1, 2
SUBWF	f, d	Subtract W from f	1	00 0010 dfff ffff	C, DC, Z	1, 2
SWAPF	f, d	Swap halves f	1	00 1110 dfff ffff		1, 2
XORWF	f, d	Exclusive OR W and f	1	00 0110 dfff ffff	Z	1, 2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	01 00bb bfff ffff		1, 2
BSF	f, b	Bit Set f	1	01 01bb bfff ffff		1, 2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01 10bb bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01 11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW	k	Add literal to W	1	11 111x kkkk kkkk	C, DC, Z	
ANDLW	k	AND literal to W	1	11 1001 kkkk kkkk	Z	
CALL	k	Call subroutine	2	10 0kkk kkkk kkkk		
CLRWDT	-	Clear watchdog timer	1	00 0000 0110 0100	$\overline{TO}$, $\overline{PD}$	
GOTO	k	Go to address	2	10 1kkk kkkk kkkk		
IORLW	k	Inclusive OR literal to W	1	11 1000 kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11 00xx kkkk kkkk		
RETFIE	-	Return from interrupt	2	00 0000 0000 1001		
RETLW	k	Return with literal in W	2	11 01xx kkkk kkkk		
RETURN	-	Return from subroutine	2	00 0000 0000 1000		
SLEEP	-	Go into standby mode	1	00 0000 0110 0011	$\overline{TO}$, $\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11 110x kkkk kkkk	C, DC, Z	
XORLW	k	Excl. OR literal to W	1	11 1010 kkkk kkkk	Z	

Notes: 1. When an I/O register is modified as a function of itself (e.g. MOVF Port B,1), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2. If this instruction is executed on the RTCC register (and, where applicable, d=1), the prescaler will be cleared if assigned to the RTCC.

3. If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

6.1 Instruction Descriptions

ADDLW Add Literal to W

Syntax: [*label*] ADDLW k

Operands: 0 ≤ k ≤ 255

Operation: (PC) + 1 → (PC)
(W) + k → W

Status Affected: C, DC, Z

Encoding:

11	111X	kkkk	kkkk

Description: The contents of the W register are added to the 8-bit literal "k" and the result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ADDLW   0x15
```
Before Instruction
W = 0x10

After Instruction
W = 0x25

ANDLW AND Literal and W

Syntax: [*label*] ANDLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .AND. (k) → W

Status Affected: Z

Encoding:

11	1001	kkkk	kkkk

Description: The contents of W register are AND'ed with the 8-bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ANDLW   0x5F
```
Before Instruction
W = 0xA3

After Instruction
W = 0x03

ADDWF ADD W to f

Syntax: [*label*] ADDWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

00	0111	dfff	ffff

Description: Add the contents of the W register to register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
ADDWF   FSR, 0
```
Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0xD9
FSR = 0xC2

ANDWF AND W with f

Syntax: [*label*] ANDWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (W) .AND. (f) → dest

Status Affected: Z

Encoding:

00	0101	dfff	ffff

Description: AND the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
ANDWF   FSR, 1
```
Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0x17
FSR = 0x02

BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: 0 → f<b>

Status Affected: None

Encoding:

01	00bb	bfff	ffff

Description: Bit "b" in register "f" is reset to 0.

Words: 1

Cycles: 1

Example:
```
BCF     FLAG_REG, 7
```
Before Instruction
FLAG_REG = 0xC7

After Instruction
FLAG_REG = 0x47

BSF **Bit Set f**

Syntax: [*label*] BSF f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: 1 → f<b>

Status Affected: None

Encoding:

01	01bb	bfff	ffff

Description: Bit "b" in register "f" is set to 1.

Words: 1

Cycles: 1

Example:
```
BSF     FLAG_REG, 7
```
Before Instruction
FLAG_REG = 0x0A

After Instruction
FLAG_REG = 0x8A

BTFSC **Bit Test, skip if Clear**

Syntax: [*label*] BTFSC f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

01	10bb	bfff	ffff

Description: If bit 'b' in register 'f' is '0' then the next instruction is skipped.

If bit 'b' is '0', the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address HERE

After Instruction
if FLAG<1> = 0, PC = address TRUE
if FLAG <1> - 1, PC = address FALSE

BTFSS **Bit Test, skip if Set**

Syntax: [*label*] BTFSS f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

01	11bb	bfff	ffff

Description: If bit "b" in register "f" is "1" then the next instruction is skipped.

If bit "b" is "0", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address HERE

After Instruction
if FLAG<1> = 0, PC = address FALSE
if FLAG <1> - 1,PC = address TRUE

CALL Subroutine Call

Syntax: [*label*] CALL k

Operands: $0 \le k \le 2048$

Operation: (PC) + 1 → TOS,
k → PC<10:0>,
(PCLATH<4:3>) → PC<12:11>;

Status Affected: None

Encoding:

10	0kkk	kkkk	kkkk

Description: Subroutine call. First, return address (PC + 1) is pushed onto the stack. The 11-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH (f03). CALL is a two-cycle instruction.

Words: 1

Cycles: 2

Example:
```
HERE    CALL    THERE
```
Before Instruction
PC = Address HERE

After Instruction
PC = Address THERE
TOS = Address HERE

CLRF Clear f

Syntax: [*label*] CLRF f

Operands: $0 \le f \le 127$

Operation: 00h → f

Status Affected: Z

Encoding:

00	0001	1fff	ffff

Description: The contents of register "f" are cleared.

Words: 1

Cycles: 1

Example:
```
CLRF    FLAG_REG
```
Before Instruction
FLAG_REG = 0x5A

After Instruction
FLAG_REG = 0x00

CLRW Clear W Register

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W), 1 → Z

Status Affected: Z

Encoding:

00	0001	0XXX	XXXX

Description: W registered is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example:
```
CLRW
```
Before Instruction
W = 0x5A

After Instruction
W = 0x00
Z = 1

CLRWDT Clear Watchdog Timer

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0100

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example:
```
CLRWDT
```
Before Instruction
WDT counter = ?

After Instruction
WDT counter = 0x00

2

COMF Complement f

Syntax: [*label*] COMF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: $\overline{(f)} \rightarrow$ (dest)

Status Affected: Z

Encoding:

00	1001	dfff	ffff

Description: The contents of register "f" are complemented. If "d" is 0 the result is stored in W. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
COMF    REG1, 0
```
Before Instruction
REG1 = 0xA5

After Instruction
REG1 = 0xA5
W = 0x5A

DECF Decrement f

Syntax: [*label*] DECF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f)-1 → (dest)

Status Affected: Z

Encoding:

00	0011	dfff	ffff

Description: Decrement register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
DECF    CNT, 1
```
Before Instruction
CNT = 0x01
Z = 0

After Instruction
CNT = 0x00
Z = 1

DECFSZ Decrement f, skip if 0

Syntax: [*label*] DECFSZ f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) - 1 → d; skip if result = 0

Status Affected: None

Encoding:

00	1011	dfff	ffff

Description: The contents of register "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Example:
```
HERE    DECFSZ  CNT, 1
        GOTO    LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address HERE

After Instruction
CNT = CNT - 1
if CNT = 0, PC = address CONTINUE
if CNT ≠ 0, PC = address HERE + 1

GOTO Unconditional Branch

Syntax: [*label*] GOTO k

Operands: 0 ≤ k ≤ 2048
d ∈ [0,1]

Operation: k → PC<10:0>,
(PCLATH<4:3>) → PC<12:11>

Status Affected: None

Encoding:

10	1kkk	kkkk	kkkk

Description: GOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH <4:3>. GOTO is a two-cycle instruction.

Words: 1

Cycles: 2

Example:
```
GOTO THERE
```
After Instruction
PC = Address of THERE

INCF **Increment f**

Syntax: [*label*] INCF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (dest)

Status Affected: Z

Encoding:

00	1010	dfff	ffff

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

Words: 1

Cycles: 1

Example:
```
INCF     CNT 1,
```
Before Instruction
CNT = 0xFF
Z = 0

After Instruction
CNT = 0x00
Z = 1

INCFSZ **Increment f, skip if 0**

Syntax: [*label*] INCFSZ f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (dest), skip if result = 0

Status Affected: None

Encoding:

00	1111	dfff	ffff

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Example:
```
HERE     INCFSZ    CNT, 1
         GOTO      LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address HERE

After Instruction
CNT = CNT - 1
if CNT = 0, PC = address CONTINUE
if CNT ≠ 0, PC = address HERE + 1

IORLW **Inclusive OR Literal with W**

Syntax: [*label*] IORLW k

Operands: $0 \le k \le 255$

Operation: (W) .OR. (k) → (W)

Status Affected: Z

Encoding:

11	1000	kkkk	kkkk

Description: The contents of the W register are OR'ed with the eight bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
IORLW    0x35
```
Before Instruction
W = 0x9A

After Instruction
W = 0xBF

IORWF **Inclusive OR W with f**

Syntax: [*label*] IORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .OR. (f) → (dest)

Status Affected: Z

Encoding:

00	0100	dfff	ffff

Description: Inclusive OR the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
IORWF    RESULT, 0
```
Before Instruction
RESULT = 0x13
W = 0x91

After Instruction
RESULT = 0x13
W = 0x93

2

MOVLW **Move Literal to W**

Syntax: [*label*] MOVLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W)

Status Affected: None

Encoding:

11	00XX	kkkk	kkkk

Description: The eight bit literal "k" is loaded into W register.

Words: 1

Cycles: 1

Example:
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: 0 ≤ f ≤ 127

Operation: (W) → (f)

Status Affected: None

Encoding:

00	0000	1fff	ffff

Description: Move data from W register to register "f".

Words: 1

Cycles: 1

Example:
```
MOVWF   OPTION
```
Before Instruction
OPTION = 0xFF
W = 0x4F

After Instruction
OPTION = 0x4F
W = 0x4F

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) → (dest)

Status Affected: Z

Encoding:

00	1000	dfff	ffff

Description: The contents of register f is moved to destination d. If d=0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example:
```
MOVF    FSR, 0
```
After Instruction
W = value in FSR register

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

00	0000	0XX0	0000

Description: No operation

Words: 1

Cycles: 1

Example:
```
NOP
```

OPTION **Load Option Register**

Syntax: [*label*] OPTION

Operands: None

Operation: W → OPTION;

Status Affected: None

Encoding:

00	0000	0110	0010

Description: The contents of the W register is loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.

Words: 1

Cycles: 1

Example:

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

RETFIE **Return from Interrupt**

Syntax: [*label*] RETFIE

Operands: None

Operation: TOS → PC,
1 → GIE;

Status Affected: None

Encoding:

00	0000	0000	1001

Description: Return from Interrupt. Stack is popped and Top of the Stack (TOS) is loaded in PC. Interrupts are enabled by setting the GIE bit. GIE is the global interrupt enable bit (INTCON<7>). This is a two-cycle instruction.

Words: 1

Cycles: 2

Example:

```
RETFIE
```

After Interrupt
PC = TOS
GIE = 1

RETLW **Return Literal to W**

Syntax: [*label*] RETLW k

Operands: 0 ≤ k ≤ 255

Operation: k → W; TOS → PC;

Status Affected: None

Encoding:

11	01XX	kkkk	kkkk

Description: The W register is loaded with the 8-bit literal "k". The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

Words: 1

Cycles: 2

Example:

```
      CALL   TABLE ; W contains table offset
                   ; value
      •            ; W now has table value
      •
      •
TABLE ADDWF PC     ; W = offset
      RETLW k1     ; Begin table
      RETLW k2     ;
      •
      •
      •
      RETLW kn     ; End of table
```

Before Instruction
W = 0x07

After Instruction
W = value of k7

RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: TOS → PC;

Status Affected: None

Encoding:

00	0000	0000	1000

Description: Return from subroutine. The stack is popped and the Top Of the Stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

Words: 1

Cycles: 2

Example:

```
RETURN
```

After Interrupt
PC = TOS

RLF — Rotate Left f through Carry

Syntax: [*label*] RLF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

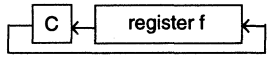
Operation: f<n> → d<n+1>, f<7> → C, C → d<0>;

Status Affected: C

Encoding:

00	1101	dfff	ffff

Description: The contents of register "f" are rotated one bit to the left through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is stored back in register "f".



Words: 1

Cycles: 1

Example:
```
RLF     REG1, 0
```
Before Instruction
REG1 = 11100110
C = 0

After Instruction
REG1 = 11100110
W = 11001100
C = 1

RRF — Rotate Right f through Carry

Syntax: [*label*] RRF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

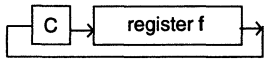
Operation: f<n> → d<n-1>,
f<0> → C,
C → d<7>;

Status Affected: C

Encoding:

00	1100	dfff	ffff

Description: The contents of register "f" are rotated one bit to the right through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".



Words: 1

Cycles: 1

Example:
```
RRF     REG1, 0
```
Before Instruction
REG1 = 11100110
C = 0
After Instruction
REG1 = 11100110
W = 01110011
C = 0

SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0011

Description: The power down status bit ($\overline{PD}$) is cleared. Time-out status bit ($\overline{TO}$) is set. Watchdog Timer and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP mode for more details.

Words: 1

Cycles: 1

Example:
```
SLEEP
```

SUBLW — Subtract W from Literal

Syntax: [*label*] SUBLW k

Operands: 0 ≤ k ≤ 255

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Encoding:

11	110X	kkkk	kkkk

Description: The W register is subtracted (2's complement method) from the 8-bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example 1:
```
SUBLW   0X02
```
Before Instruction
W = 1
C = ?
After Instruction
W = 1
C = 1 ;result is positive

Example 2: Before Instruction
W = 3
C = ?
After Instruction
W = FF
C = 0 ;result is negative

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f)-(W) → (dest)

Status Affected: C, DC, Z

Encoding:

00	0010	dff	ffff

Description: Subtract (two's complement method) the W register from register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:

Example 1:
```
SUBLW    REG1,1
```
Before Instruction
REG1 = 0
W = 1
C = ?
After Instruction
REG1 = FF
W = 1
C = 0 ;result is negative

Example 2: Before Instruction
REG1 = FF
W = 0
C = ?
After Instruction
REG1 = FF
W = 0
C = 1 ;result is positive

SWAPF **Swap f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: f<0:3> → d<4:7>,
f<4:7> → d<0:3>;

Status Affected: None

Encoding:

00	1110	dfff	ffff

Description: The upper and lower nibbles of register "f" are exchanged. If "d" is 0 the result is placed in W register. If "d" is 1 the result is placed in register "f".

Words: 1

Cycles: 1

Example:
```
SWAPF  REG, 0
```
Before Instruction
REG = 0xA5
After Instruction
REG = 0xA5
W = 0x5A

TRIS **Load TRIS Register**

Syntax: [*label*] TRIS f

Operands: $5 \le f \le 7$

Operation: W → TRIS register f;

Status Affected: None

Encoding:

00	0000	0110	0fff

Description: This instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.

Words: 1

Cycles: 1

Example:

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

11	1010	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the 8-bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
XORLW  0xAF
```
Before Instruction
W = 0xB5
After Instruction
W = 0x1A

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 128$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

00	0110	dfff	ffff

Description: Exclusive OR the contents of the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:

```
XORWF  REG, 1
```

Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

7.0 DEVELOPMENT SUPPORT

7.1 Development Tools

The PIC16C5X and PIC16CXX microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER™ Real-Time In-Circuit Emulator
- PRO MATE™ Universal Programmer
- PICSTART™ Low-Cost Prototype Programmer
- Assembler
- Software Simulator

7.2 PICMASTER™: High Performance Universal In-Circuit Emulator

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X, PIC16CXX and PIC17CXX families.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16C5X, PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on low-cost PC compatible machines ranging from 80286-AT® class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.X environment, allowing the operator access to a wide range of supporting software and accessories.

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.X environment was chosen to best make these features available to you, the end user.

The PICMASTER Emulator Universal System consists primarily of four major components:

- Host-Interface Card
- Emulator Control Pod
- Target-Specific Emulator Probe
- PC Host Emulation Control Software

The Windows 3.X System is a multitasking operating system which will allow the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window. Dynamic Data Exchange (DDE), a feature of Windows 3.X, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

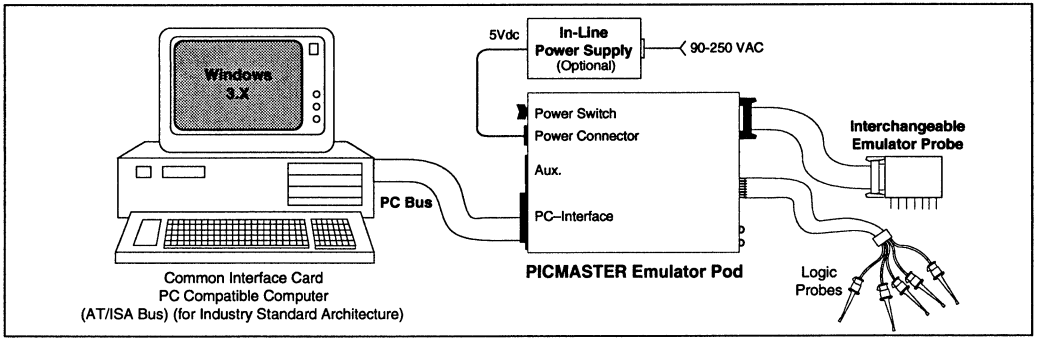
Under Windows 3.X, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16CXX processor and a PIC17CXX processor).

7.3 PRO MATE™: Universal Programmer

The PRO MATE Universal Programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MATE has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability . It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MATE can read, verify or program PIC16C5X, PIC16CXX and PIC17CXX devices. It can also set fuse configuration and code-protect in this mode. Its EEPROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.

FIGURE 7.1 - PICMASTER SYSTEM CONFIGURATION



In PC-hosted mode, the PRO MATE connects to the PC via one of the COM (RS232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of V_{DD} min, V_{DD} max and V_{PP} levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different serial number, sequential or random.

The PRO MATE has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. PRO MATE supports all PIC16C5X, PIC16CXX and PIC17CXX processors.

7.4 PICSTART™ Programmer

The PICSTART programmer is an easy to use, very low-cost prototype programmer. It connects to the PC via one of the COM (RS232) ports. A PC based user interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based.

7.5 Assembler (MPASM)

Cross Assembler is a PC hosted symbolic assembler. It supports all microcontroller series including the PIC16C5X CMOS, PIC16CXX and PIC17CXX families.

MPASM offers fully featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from the Microchip Universal Emulator System (PICMASTER).

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro Assembly Capability
- Provides Object, Listing, Symbol and special files required for debugging with one of the Microchip Emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a full feature directive language represented by four basic classes of directives:

- **Data Directives** are those that control the allocation of memory and provide a way to refer to data items symbolically, by meaningful names.
- **Listing Directives** control the MPASM listing dis play. They allow the specification of titles and sub-titles, page ejects and other listing control.
- **Control Directives** permit sections of conditionally assembled code.
- **Macro Directives** control the execution and data allocation within macro body definitions.

7.6 Software Simulator (MPSIM)

The Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16C5X and PIC16CXX series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in single step, execute until break or in a trace mode. Two forms of symbolic debugging are available: an internal symbol table for disassembling opcodes and the displaying of source code from a listing file. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

7.7 Development Systems

For convenience, the development tools are packaged into comprehensive systems as listed in Table 7-1:

TABLE 7-1: DEVELOPMENT SYSTEM PACKAGES

Item	Name	System Description
1.	PICMASTER™ System	PICMASTER In-Circuit Emulator with your choice of Target Probe, PRO MATE Programmer, Assembler, Software Simulator and Samples.
2.	PICSTART™ System	PICSTART™ Low-Cost Prototype Programmer, Assembler, Software Simulator and Samples

7.8 Probe Specifications

The PICMASTER probes currently meet the following specifications:

PICMASTER PROBE	Devices Supported	PROBE Maximum Frequency	PROBE Operating Voltage
PROBE - 16B	PIC16C71	10 MHZ	4.5V - 5.5V

8.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Ambient temperature under bias ..... -55 to+ 125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss (except VDD and $\overline{MCLR}$) ..... -0.6V to VDD +0.6 V
Voltage on VDD with respect to Vss ..... 0 to +7.5 V
Voltage on $\overline{MCLR}$ with respect to Vss (Note 2) ..... 0 to +14 V
Total power Dissipation (Note 1) 800mW
Max. Current out of Vss pin 150mA
Max. Current into VDD pin 100mA
Input Clamping Current, IIK (VI<0 or VI>VDD) ..... ±20mA
Output Clamping Current, IOK (V0<0 or V0>VDD) ..... ±20mA
Max. Output Current sunk by any I/O pin 25mA
Max. Output Current sourced by any I/O pin 20mA
Max. Output Current sunk by I/O PORTA 80mA
Max. Output Current sunk by I/O PORTB 150mA
Max. Output Current sourced by I/O PORTA 50mA
Max. Output Current sourced by I/O PORTB 100mA

Notes:
1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
   Pdis = VDD x {IDD - Σ Ioh} + Σ {(VDD-Voh) x Ioh} + Σ(Vol x Iol)
2. Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low' level to the $\overline{MCLR}$ pin rather than pulling this pin directly to Vss.

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or compliance to AC and DC parametric specifications at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

8.1 DC CHARACTERISTICS: PIC16C71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C71-16 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS, POWER SUPPLY PINS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ + 125°C for automotive,
-40°C ≤ TA ≤ + 85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD = 4.0V to 6.0V

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Supply Voltage	VDD	4.0		6.0	V	XT, RC and LP osc configuration
		4.5		5.5	V	HS osc configuration
RAM Data Retention Voltage (Note 2)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See Section 5.2 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See Section 5.2 for details on power on reset
Supply Current (Note 3)	IDD		1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V (Note 5)
			35	70	µA	FOSC = 32 KHz, VDD = 4.0V, WDT disabled, LP osc config., A/D off (Note 6)
			9	20	mA	FOSC = 16 MHz, VDD = 5.5V, HS osc configuration (PIC16C71-16)
Power Down Current (Note 4)	IPD		7	28	µA	VDD = 4.0V, WDT enabled, -40°C to +125°C
			1.0	14	µA	VDD = 4.0V, WDT disabled, 0°C to +70°C
			1.0	16	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
			1.0	20	µA	VDD = 4.0V, WDT disabled, -40°C to +125°C

* These parameters are characterized but not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

Note 6: For current contribution due to A/D module, see section 8.5.

8.2 DC CHARACTERISTICS: PIC16LC71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS, POWER SUPPLY PINS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ + 125°C for automotive, -40°C ≤ TA ≤ + 85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD = 3.0V to 6.0V				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	3.0 4.5		6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
RAM Data Retention Voltage (Note 2)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See Section 5.2 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See Section 5.2 for details on power on reset
Supply Current (Note 3)	IDD		1.8 15	3.3 32	mA µA	FOSC = 4 MHz, VDD = 5.5V (Note 5) FOSC = 32 KHz, VDD = 3.0V, WDT disabled, LP osc config., A/D off (Note 6)
Power Down Current (Note 4)	IPD		5 0.6 0.6 0.6	20 9 12 16	µA µA µA µA	VDD = 3.0V, WDT enabled, -40°C to +125°C VDD = 3.0V, WDT disabled, 0°C to +70°C VDD = 3.0V, WDT disabled, -40°C to +85°C VDD = 3.0V, WDT disabled, -40°C to +125°C

* These parameters are characterized but not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

Note 6: For current contribution due to A/D module, see section 8.5.

8.3 DC CHARACTERISTICS: PIC16C71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C71-16 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16LC71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40 ≤ TA ≤ +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec table 8.1

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Input Low Voltage						
I/O ports	VIL	VSS		0.2 VDD	V	
MCLR, T0CKI, OSC1 (in RC configuration)		VSS		0.2 VDD	V	Note 2
OSC1 (in XT, HS and LP configuration)		VSS		0.3 VDD	V	
Input High Voltage						
I/O ports	VIH	0.36 VDD 0.45 VDD		VDD	V	4.5V≤VDD ≤ 5.5V Otherwise
MCLR, T0CKI, OSC1 (in RC configuration)		0.85 VDD		VDD	V	Note 2, 5
OSC1 (in XT, HS or LP configurations)		0.7 VDD		VDD		
Input Leakage Current (Notes 3, 4)						
I/O port RB	IIL			±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
I/O port RA				±0.5	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR, T0CKI				±5	µA	VSS ≤ VPIN ≤ VDD
OSC1				±5	µA	VSS ≤ VPIN ≤ VDD , XT, HS and LP osc configuration
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
				0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
OSC2/CLKOUT (RC osc configuration)				0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
				0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C
Output High Voltage						
I/O Ports (Note 4)	VOH	VDD-0.7			V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
		VDD-0.7			V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
OSC2/CLKOUT (RC osc configuration)		VDD-0.7			V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
		VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C71 be driven with external clock in RC mode.

Note 3 : The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : RA4/T0CKI open collector output. Maximum pull-up voltage = VDD.

8.4 AC CHARACTERISTICS: PIC16C71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C71-16 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16LC71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

AC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40 ≤ TA ≤ +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec table 8.1

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
External CLOCKIN Frequency (Note 2)	FOSC	DC		4	MHz	XT and RC osc mode
	FOSC	DC		4	MHz	HS osc mode (PIC16C71-04, PIC16LC71-04)
	FOSC	DC		16	MHz	HS osc mode (PIC16C71-16)
	FOSC	DC		200	KHz	LP osc mode
Oscillator Frequency (Note 2)	FOSC	DC		4	MHz	RC osc mode
	FOSC	0.1		4	MHz	XT osc mode
	FOSC	1		4	MHz	HS osc mode (PIC16C71-04 PIC16LC71-04)
	FOSC	1		16	MHz	HS osc mode (PIC16C71-16)
	FOSC	DC		200	KHz	LP osc mode
Instruction Cycle Time (Note 2)	TCY	0.25	4/FOSC	DC	µs	
External Clock in Timing (Note 4)						
Clock in (OSC1) High or Low Time						
XT oscillator type	TCKHLXT	50*			ns	
LP oscillator type	TCKHLLP	2.5			µs	
HS oscillator type	TCKHLHS	20*			ns	
Clock in (OSC1) Rise or Fall Time						
XT oscillator type	TCKRFXT	25*			ns	
LP oscillator type	TCKRFLP	50*			ns	
HS oscillator type	TCKRFHS	25*			ns	
RESET Timing						
MCLR Pulse Width (low)	TMCL	200*			ns	
TMR0 Input Timing, No Prescaler						
T0CKI High Pulse Width	TRTH	0.5 TCY+ 20*			ns	Note 3
T0CKI Low Pulse Width	TRTL	0.5 TCY+ 20*			ns	Note 3
TMR0 Input Timing, With Prescaler						
T0CKI High Pulse Width	TRTH	10*			ns	Note 3
T0CKI Low Pulse Width	TRTL	10*			ns	Note 3
T0CLI Period	TRTP	$\frac{T_{CY} + 40}{N}$ *			ns	Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Timeout Period (No Prescaler)	TWDT	7*	18	33*	ms	VDD = 5V, -40°C to +125°C
OST/PWRT Timings						
Oscillation Start-up Timer Pewriod	TOST		1024 tosc		ms	tosc = OSC1 period
Power up timer period	TPWRT	28*	72	132*	ms	VDD = 5V, -40°C to +125°C
I/O Timing						
I/O Pin Input Valid Before CLKOUT↑	TioV2ckH	0.25 TCY+ 30			ns	
I/O Pin Input Hold After CLKOUT↑	TckH2ioI	0			ns	
I/O Pin Output Valid After CLKOUT↓	TioV2ckL			40	ns	

* These parameters are characterized but not tested.

For notes refer to top of page 54.

NOTES TO TABLE 8.4

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: Instruction cycle period (Tcy) equals four times the input oscillator time base period.
All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Note 3: For a detailed explanation of TMR0 input clock requirements see section 5.4.1.

Note 4: Clock-in high-time is the duration for which clock input is at VIHOSC or higher. Clock-in low-time is the duration for which clock input is at VIHOSC or lower.

8.5 A/D CONVERTER CHARACTERISTICS:

PIC16C71-04 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)
PIC16C71-16 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)
PIC16LC71-04 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)

AC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40 ≤ TA ≤ +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec table 8.1

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Resolution	NR	-	-	8 Bits	-	VREF = VDD = 5.12V (Note 2)
Integral error	NINT	-	-	less than ±1 LSB	-	VREF = VDD = 5.12V (Note 2)
Differential error	NDIF	-	-	less than ±1 LSB	-	VREF = VDD = 5.12V (Note 2)
Full scale error	NFS	-	-	less than ±1 LSB	-	VREF = VDD = 5.12V (Note 2)
Offset error	NOFF	-	-	less than ±1 LSB	-	VREF = VDD = 5.12V (Note 2)
Monotonicity	-	-	guaranteed		-	
Reference voltage	VREF	3.0 V	-	VDD + 0.3	V	
Analog input voltage	VAIN	VSS - 0.3	-	VREF	V	
Recommended impedance of analog voltage source	ZAIN	-	-	10.0	KΩ	
A/D clock period	tad	- - - 2.0	2tosc 8tosc 32tosc 4.0	- - - 6.0	- - - µs	ADCS1,0 = 00 (for tosc ≥ 1 µs) ADCS1,0 = 01 (for tosc ≥0.25 µs) ADSC1,0 = 10 (for tosc ≥ 62.5 ns) ADSC1,0 = 11 (RC oscillator source is selected)
Conversion time (not including S/H time)	TCNV	-	10tad	-	-	-
Sampling time	TSMP	5	-	-	µs	The minimum time is the amplifier settling time. This may be used of the "new" input voltage has not changed by more than 1 Lsb (i.e. 20mV @ 5.12V) from the last sampled voltage (as stated on C_{HOLD}).
A/D conversion current (VDD)	Iad	-	180	-	µA	Average current consumption when A/D is on (Note 3)
VREF input current (Note 4)	IREF	-	-	1 40	mA µA	During charging All other times

Note 1: All entries in the "typ" column are at 5V, 25°C unless otherwise stated.

Note 2: The error will be more for lower VREF and/or lower VDD.

Note 3: When A/D is off, it will not consume any current other than minor leakage current. The power down current spec includes any such leakage from the A/D module.

Note 4: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

8.6 A/D CONVERTER CHARACTERISTICS: PIC16LC71-04 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)

AC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40 ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec table 8.1			
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Resolution	NR	-	-	8 Bits	-	VREF = VDD = 3.0V (Note 2)
Integral error	NINT	-	-	less than ±2 LSB	-	VREF = VDD = 3.0V (Note 2)
Differential error	NDIF	-	-	less than ±2 LSB	-	VREF = VDD = 3.0V (Note 2)
Full scale error	NFS	-	-	less than ±2 LSB	-	VREF = VDD = 3.0V (Note 2)
Offset error	NOFF	-	-	less than ±2 LSB	-	VREF = VDD = 3.0V (Note 2)
Monotonicity	-	-	guaranteed	-	-	
Reference voltage	VREF	3.0 V	-	VDD + 0.3	V	
Analog input voltage	VAIN	VSS - 0.3	-	VREF	V	
Recommended impedance of analog voltage source	ZAIN	-	-	10.0	KΩ	
A/D clock period	tad	- - - 3.0	2tosc 8tosc 32tosc 6.0	- - - 9.0	- - - µs	ADCS1,0 = 00 (for tosc ≥ 1 µs) ADCS1,0 = 01 (for tosc ≥0.25 µs) ADSC1,0 = 10 (for tosc ≥ 62.5 ns) ADSC1,0 = 11 (RC oscillator source is selected)
Conversion time (not including S/H time)	TCNV	-	10tad	-	-	-
Sampling time	TSMP	5	-	-	µs	The minimum time is the amplifier settling time. This may be used of the "new" input voltage has not changed by more than 1 Lsb (i.e. 20mV @ 5.12V) from the last sampled voltage (as stated on C_{HOLD}).
A/D conversion current (VDD)	Iad	-	90	-	µA	Average current consumption when A/D is on (Note 3)
VREF input current (Note 4)	IREF	-	-	1 10	mA µA	During charging All other times

Note 1: All entries in the "typ" column are at 5V, 25°C unless otherwise stated.

Note 2: These specifications apply if VREF = 3.0V and if VDD ≥ 3.0V.

Note 3: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

Note 4: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

8.7 AC CHARACTERISTICS: PIC16C71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C71-16 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16LC71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

AC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40 ≤ TA ≤ +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec table 8.1

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
I/O Timing (cont.)						
I/O Pin Input Valid Before OSC↑ (I/O Setup Time)	TioV2osH	TBD			ns	
OSC1↑ to I/O pin input invalid (I/O hold time)	TosH2ioL	TBD			ns	
OSC1↑ to I/O pin output valid	TosH2ioV			TBD	ns	
I/O pin output rise time	TioR			TBD	ns	
I/O pin output fall time	TioF			TBD	ns	
Interrupt Timing						
INT pin high or low time	TinP	20			ns	
RB <7:4> input change time for interrupt to be recognized	TrbP	20			ns	
Capacitive Loading Specs on Output Pins						
OSC2 pin	COSC2			15	pF	In XT, HS and LP modes, when external clock is used to drive OSC1.
All I/O pins and OSC2 (in RC mode)	CIO			50	pF	

* These parameters are characterized, but not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: Instruction cycle period (Tcy) equals four times the input oscillator time base period.
All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Note 3: For a detailed explanation of RTCC input clock requirements see section 5.4.1.

Note 4: Clock-in high-time is the duration for which clock input is at VIHOSC or higher. Clock-in low-time is the duration for which clock input is at VIHOSC or lower.

Note 5: All AC parameters are tested or characterized with these capacitive loads.

Note 6: CLKOUT is available only in RC oscillator mode.

8.7.1 ELECTRICAL STRUCTURE OF PINS

FIGURE 8.1 - ELECTRICAL STRUCTURE OF I/O PINS (RB)

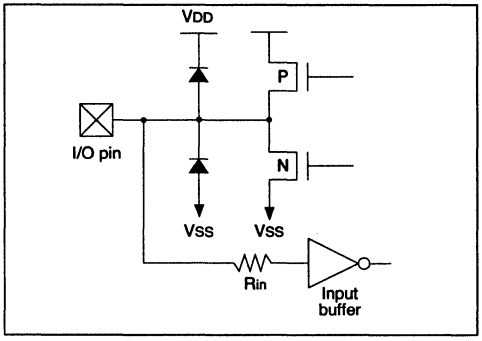


FIGURE 8.2 - ELECTRICAL STRUCTURE OF I/O PINS (RA)

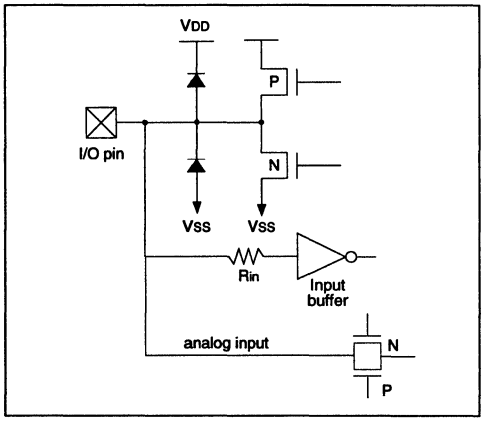
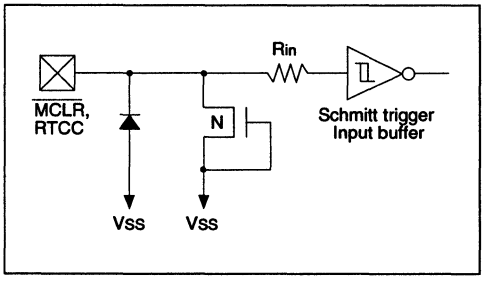


FIGURE 8.3 - ELECTRICAL STRUCTURE OF MCLR AND RTCC PINS



Notes to Figures 8.1 and 8.2: The diodes and the grounded gate (or output driver) NMOS device are carefully designed to protect against ESD (Electrostatic discharge) and EOS (Electrical overstress). Rin is a small resistance to further protect the input buffer from ESD.

9.0 TIMING DIAGRAMS

FIGURE 9.1 - TMR0 TIMING

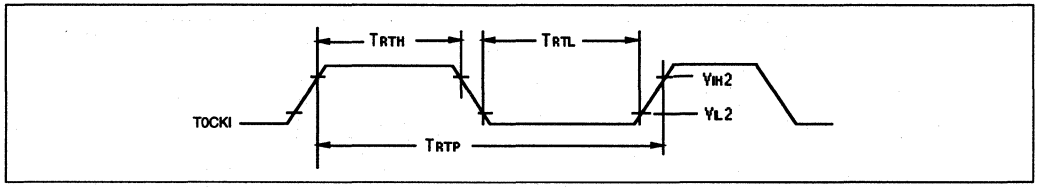
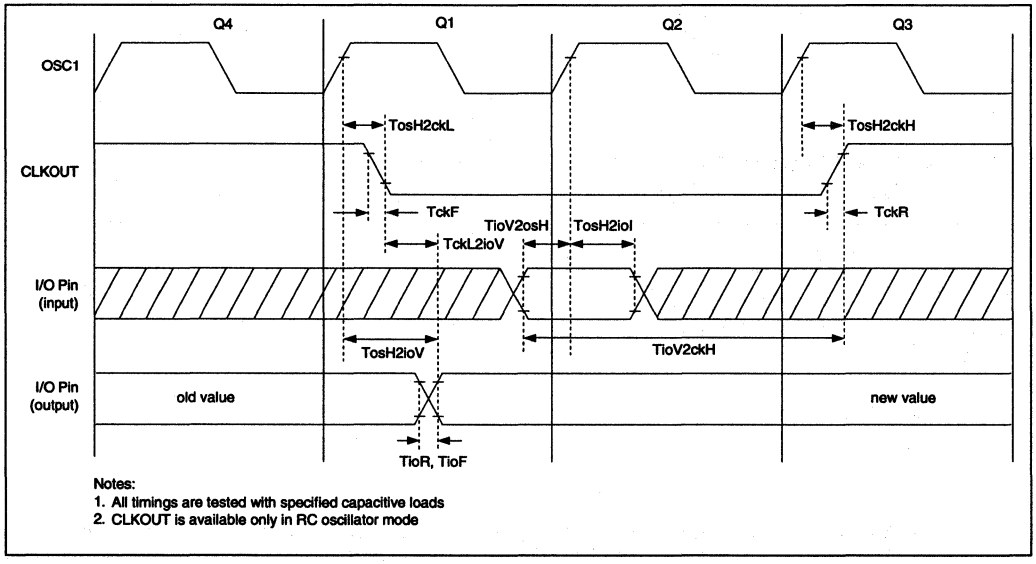


FIGURE 9.2 - INPUT/OUTPUT TIMING FOR I/O PORTS



Notes:
1. All timings are tested with specified capacitive loads
2. CLKOUT is available only in RC oscillator mode

10.0 DC & AC CHARACTERISTICS GRAPHS/TABLES

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. **In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.**

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean + 3s) and (mean - 3s) respectively where s is standard deviation.

FIGURE 10.1 - TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

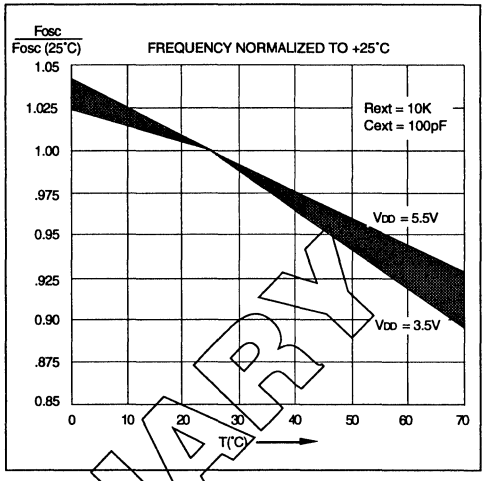


FIGURE 10.2 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

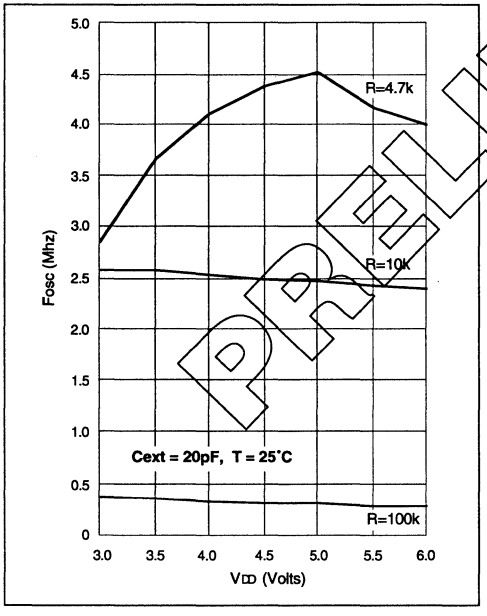


FIGURE 10.3 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

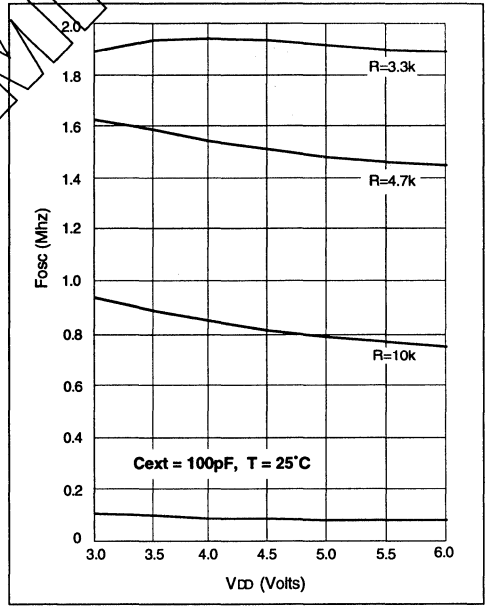


FIGURE 10.4 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

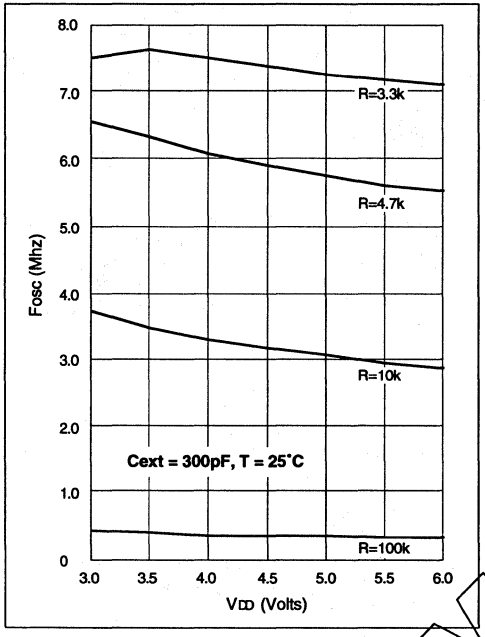


TABLE 10.1 - RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
20pf	4.7k	4.52 MHz	± 17.35%
	10k	2.47 MHz	± 10.10%
	100k	290.86 KHz	± 11.90%
100pf	3.3k	1.92 MHz	± 9.43%
	4.7k	1.48 MHz	± 9.83%
	10k	788.77 KHz	± 10.92%
	100k	88.11 KHz	± 16.03%
300pf	3.3k	726.89 KHz	± 10.97%
	4.7k	573.95 KHz	± 10.14%
	10k	307.31 KHz	± 10.43%
	100k	33.82 KHz	± 11.24%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.

FIGURE 10.5 - TYPICAL Ipd vs VDD WATCHDOG DISABLED 25°C

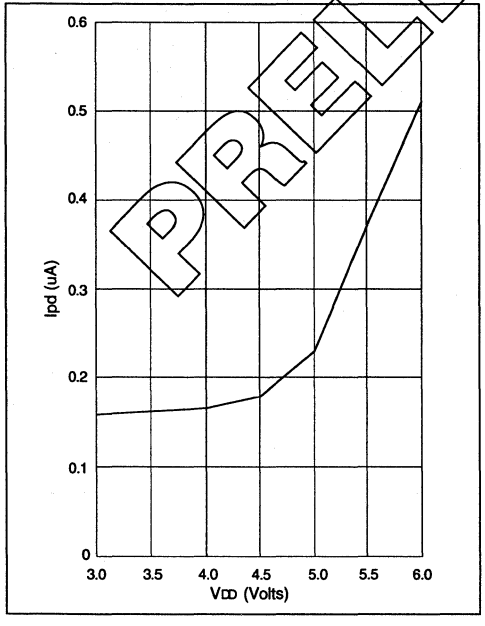


FIGURE 10.6 - TYPICAL Ipd vs VDD WATCHDOG ENABLED 25°C

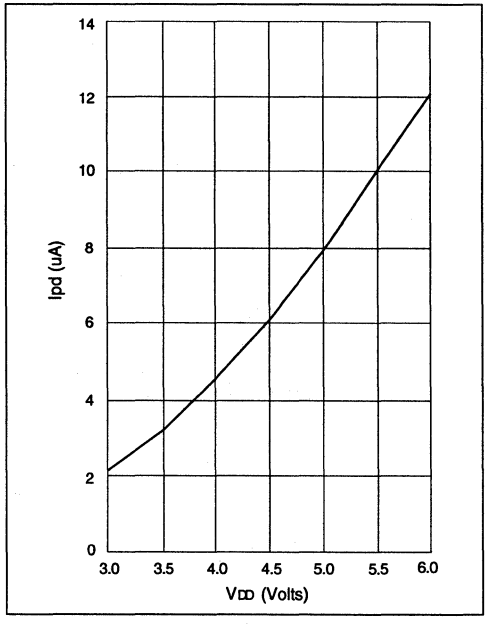


FIGURE 10.7 - MAXIMUM Ipd vs VDD WATCHDOG DISABLED

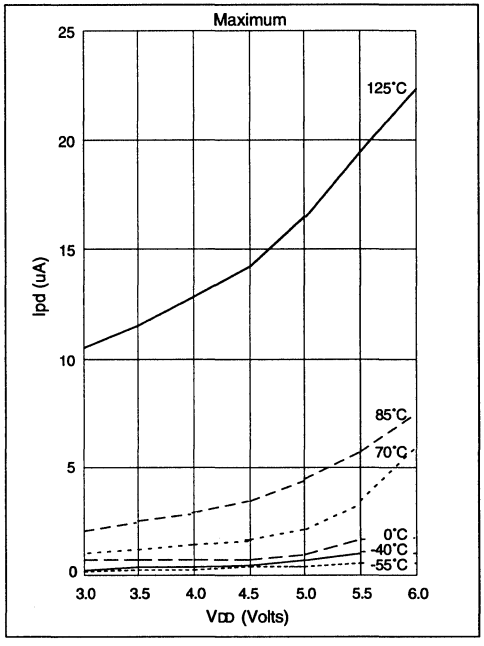
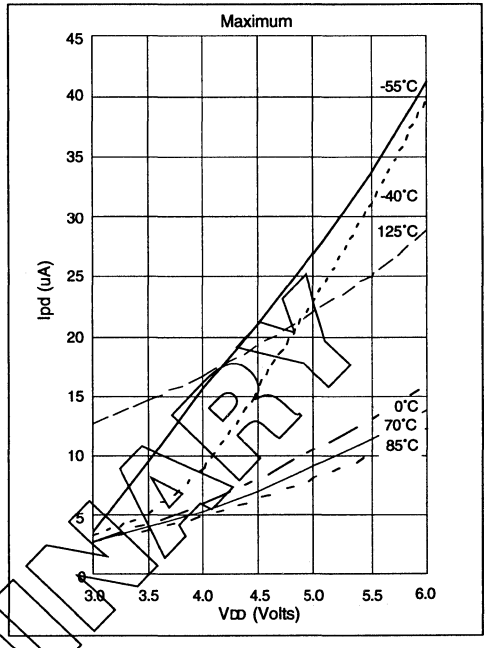


FIGURE 10.8 - MAXIMUM Ipd vs VDD WATCHDOG ENABLED*



* IPD, with watchdog timer enabled, has two components: The leakage current which increases with higher temperature and the operating current of the watchdog timer logic which increases with lower temperature. At -40°C, the latter dominates explaining the apparently anomalous behavior.

FIGURE 10.9 - VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs VDD

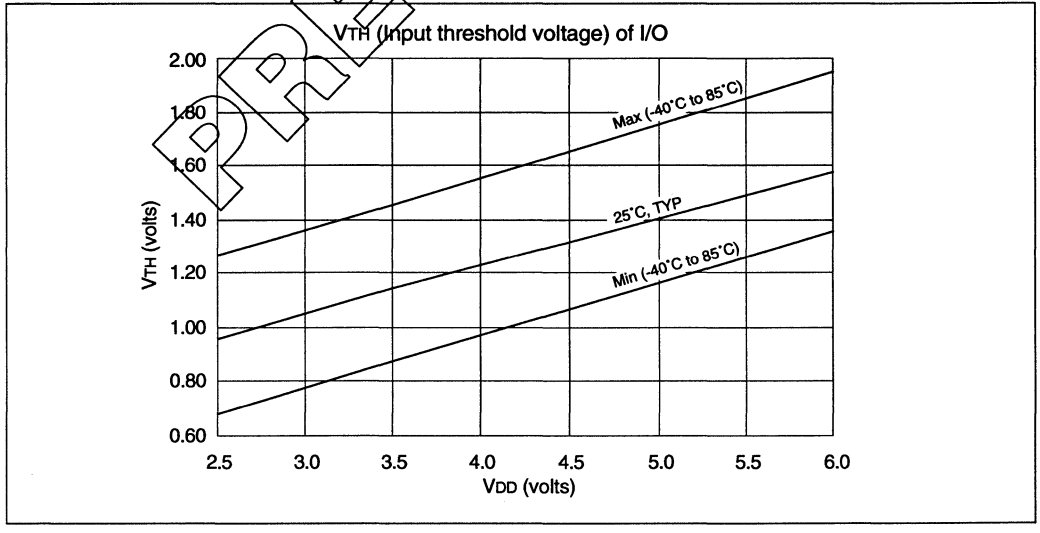
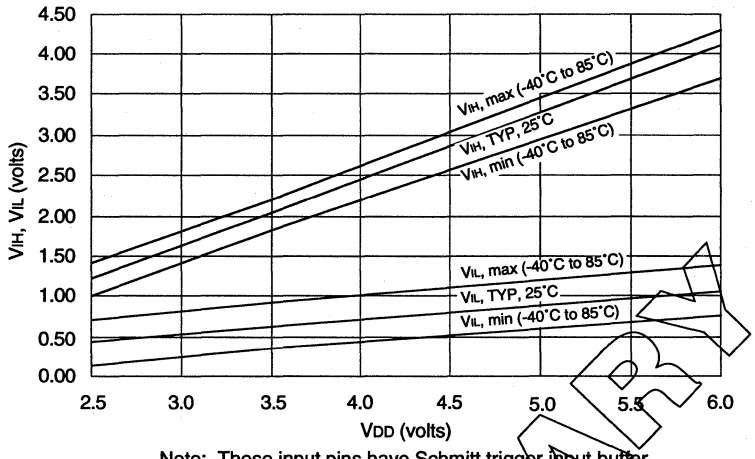


FIGURE 10.10 - VIH, VIL OF $\overline{\text{MCLR}}$, RTCC AND OSC1 (IN RC MODE) vs VDD



Note: These input pins have Schmitt trigger input buffer.

FIGURE 10.11 - VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs VDD

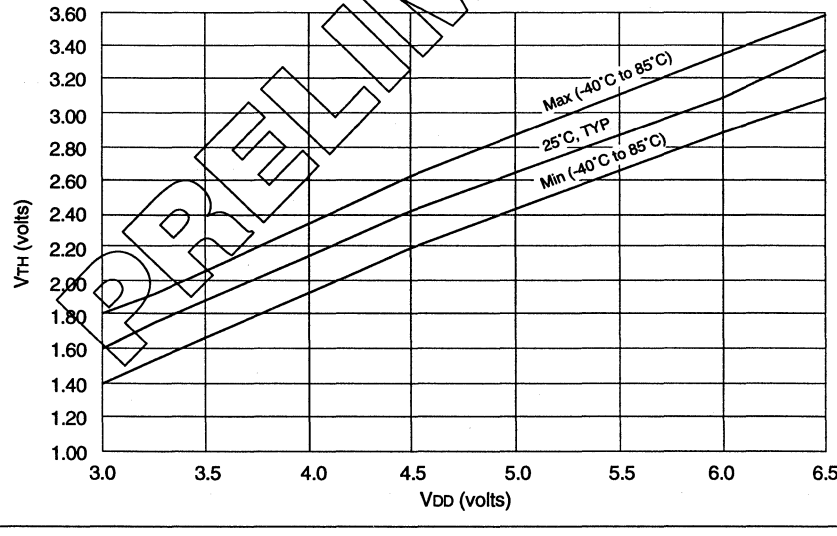


FIGURE 10.12 - TYPICAL IDD vs FREQ (EXT CLOCK, 25°C)

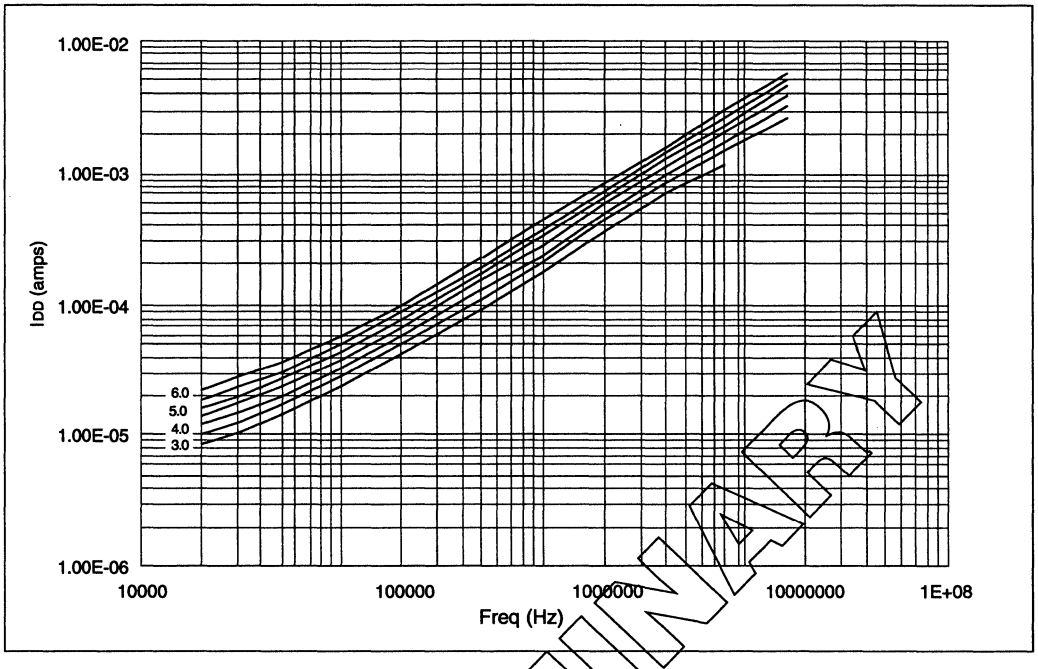


FIGURE 10.13 - MAXIMUM IDD vs FREQ (EXT CLOCK, -40° to +85°C)

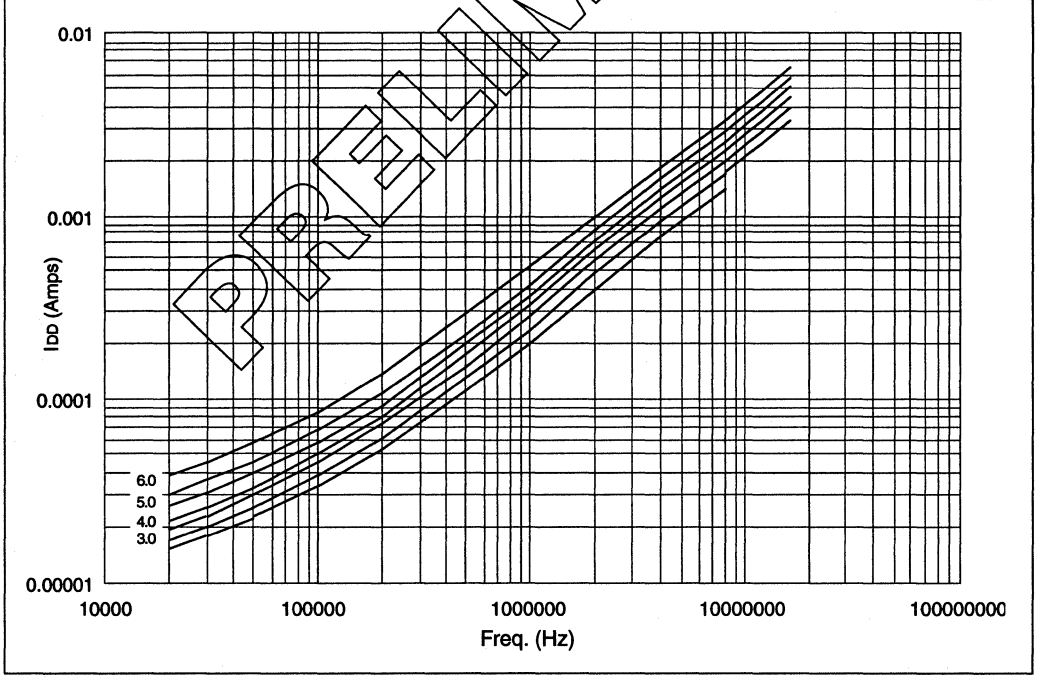


FIGURE 10.13A - MAXIMUM IDD vs FREQ WITH A/D OFF (EXT CLOCK, -55° to +125°C)

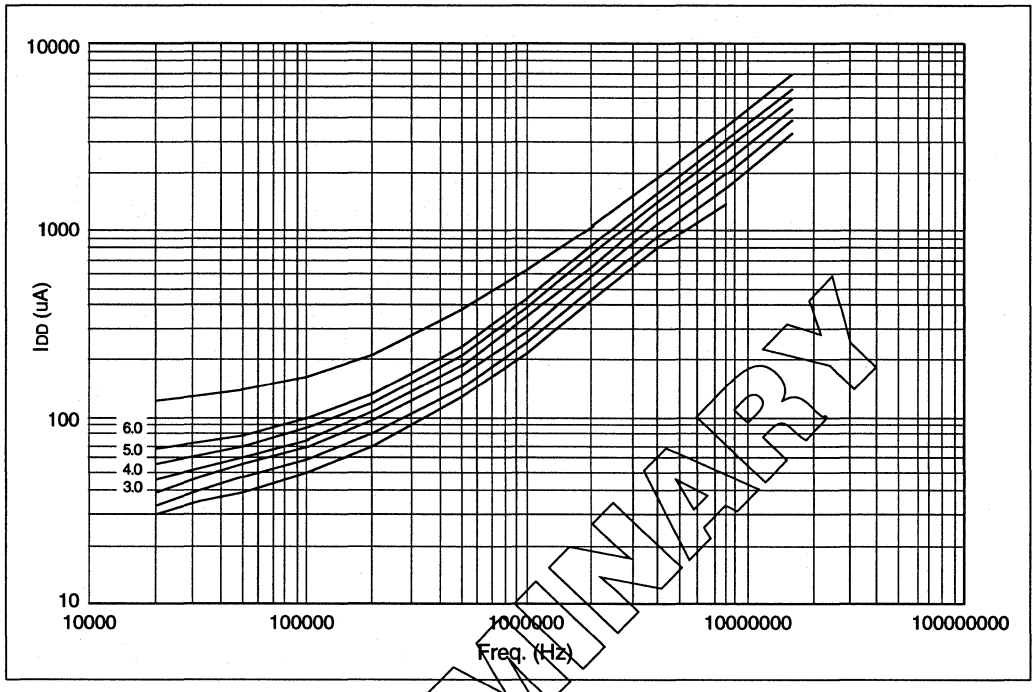


FIGURE 10.14 - WDT Timer Time-out Period vs VDD

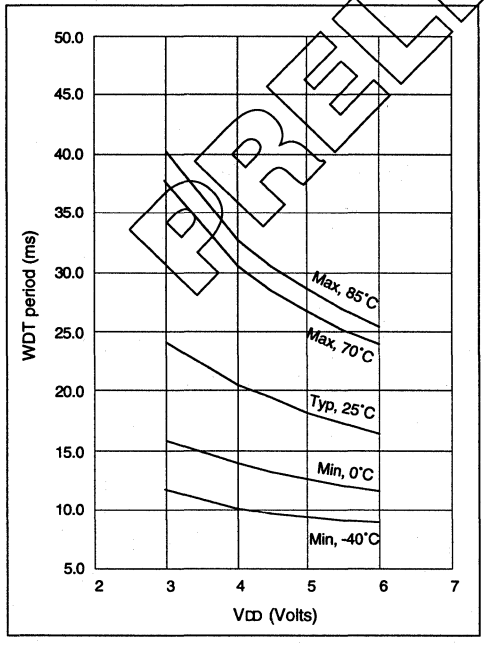


FIGURE 10.15 - Transconductance (gm) of HS Oscillator vs VDD

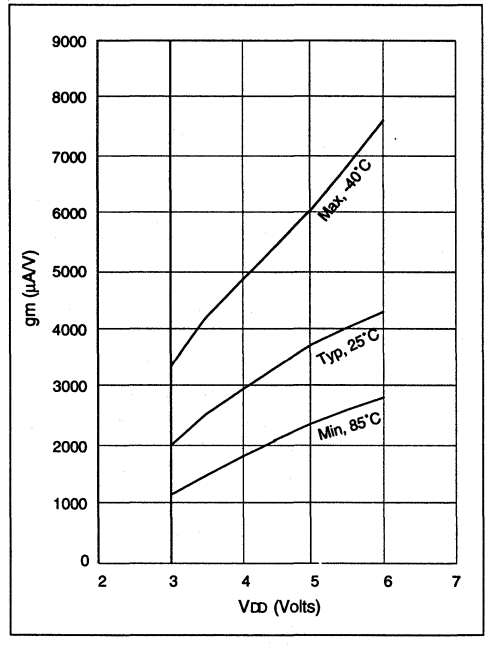


FIGURE 10.16 - Transconductance (gm) of LP Oscillator vs VDD

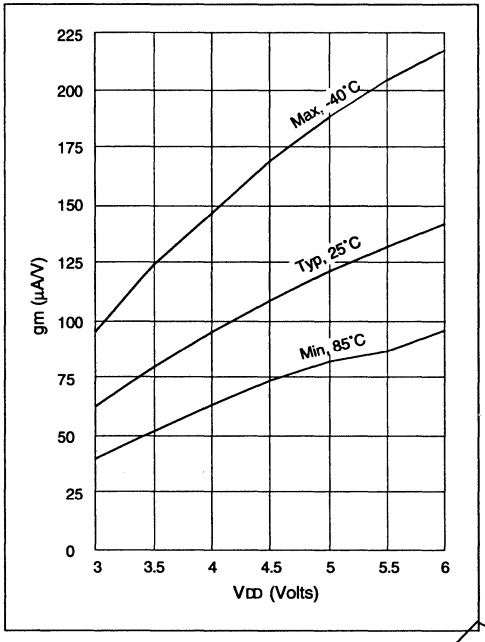


FIGURE 10.17 - Transconductance (gm) of XT Oscillator vs VDD

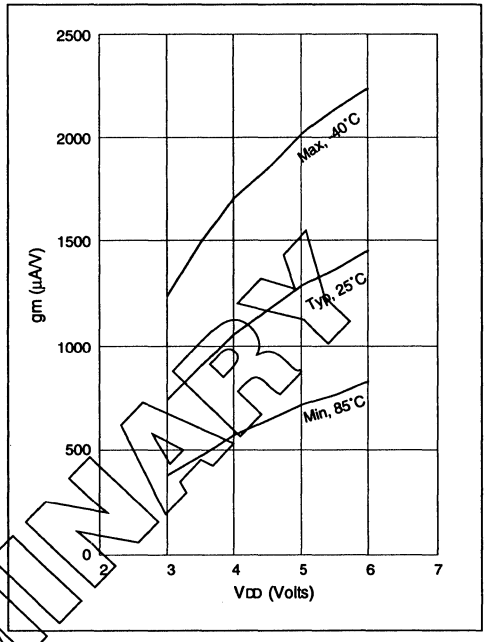


FIGURE 10.18 - IOH vs VOH, VDD = 3V

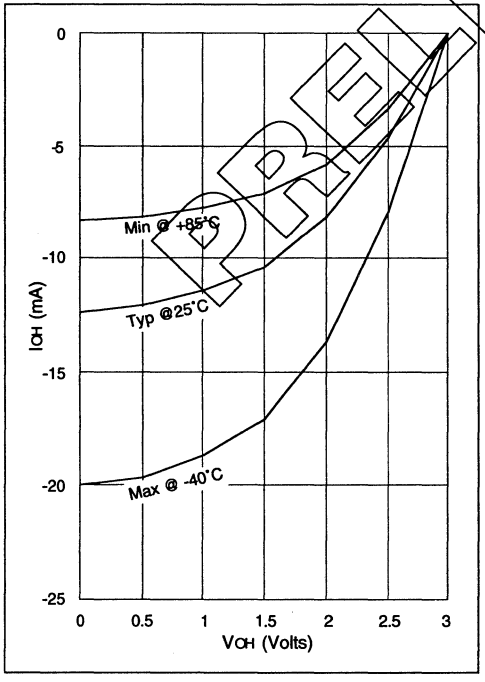


FIGURE 10.19 - IOH vs VOH, VDD = 5V

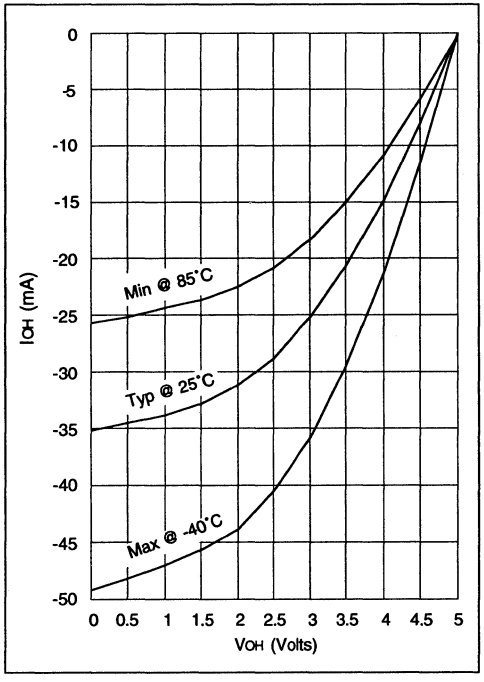


FIGURE 10.20 - IOL vs VOL, VDD = 3V

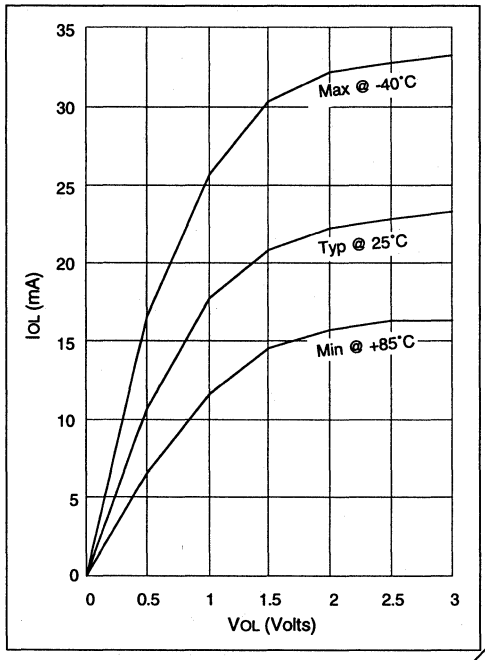


FIGURE 10.21 - IOL vs VOL, VDD = 5V

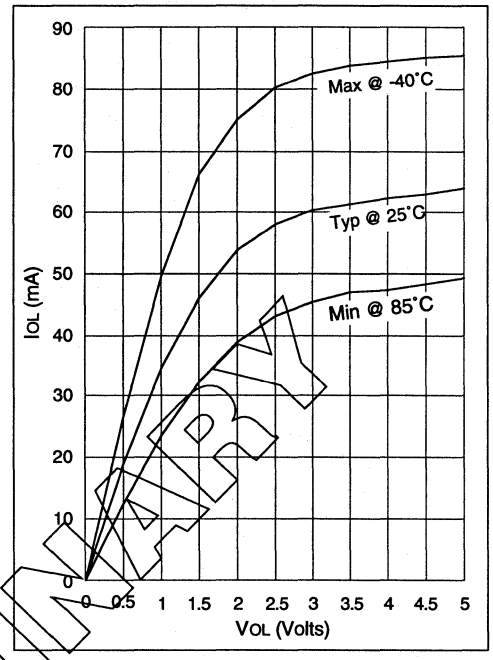


TABLE 10.2 - INPUT CAPACITANCE *

Pin Name	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{MCLR}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
RTCC	3.2	2.8

* All capacitance values are typical at 25°C. A part to part variation of ±25% (three standard deviations) should be taken into account.

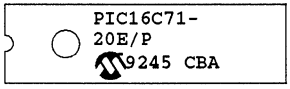
11.0 PACKAGING INFORMATION

See Section 11 of the Data Book.

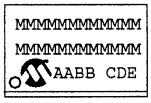
11.1 Package Marking Information

18L PDIP

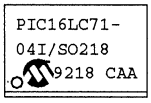
Example



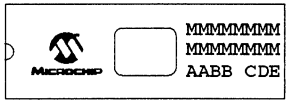
18L SOIC



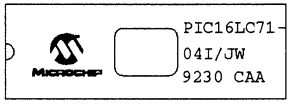
Example



18L Cerdip



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

12.0 PROGRAMMING THE PIC16C71

The PIC16C71 is programmed using one of two methods, serial or parallel. The serial mode will allow the PIC16C71 to be programmed while in the users system using only five pins: VDD, VSS, MCLR/VPP, RB6 and RB7. This allows for increased design flexability. The parallel mode will provide faster programming as the data is loaded into the PIC16C71 with a greater throughput. Either mode may be selected at the start of the programming process. The parallel mode is intended for programmers. In either mode, both program and data memory can be programmed. You can get complete programming information in the PIC16C6X/7X programming specification (DS30228C).

APPENDIX A

The following are the list of modifications over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bit. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and register file (128 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from status register.
3. Data memory paging is redefined slightly. Status register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.

   Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressible.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to eight deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change feature.
13. RTCC pin is also a port pin (RA4) now.
14. Location 07h (PORTC) is unimplemented and not a general purpose register.
15. FSR is made a full 8-bit register.
16. "In system programming" is made possible. The user can program the PIC16C71 using only five pins: V_{DD}, V_{SS}, $\overline{MCLR}/V_{PP}$, RB6 (clock) and RB7 (data in/out).

APPENDIX B

To convert code written for PIC16C5X to PIC16C71, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.
6. Note that location 07h is an unimplemented data memory location.

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CONNECTING TO MICROCHIP BBS

Connect world wide to the Microchip BBS using the CompuServe communications network. In most cases a local call is your only expense. The Microchip BBS connection does not use CompuServe membership services, therefore **you do not need CompuServe membership to join Microchip's BBS.**

The procedure to connect will vary slightly from country to country. Please check with your local CompuServe agent for details if you have a problem. CompuServe services allows multiple users at baud rates up to 9600.

To connect:

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.

2. Dial your local CompuServe phone number.

3. Depress **<ENTER>** and a garbage string will appear because CompuServe is expecting a 7E1 setting.

4. Type **+ <ENTER>** and `Host Name:` will appear.

5. Type **MCHIPBBS<ENTER>** and you will be connected to the Microchip BBS.

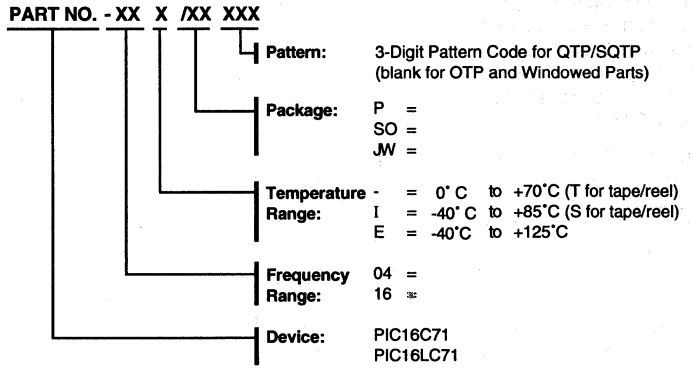
In the United States, to find CompuServe's phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600 baud connection. After the system responds with `Host Name:`, type

NETWORK<ENTER> and follow CompuServe's directions.

For voice information (or calling from overseas), you may call (614) 457-1550 for your local CompuServe number.

PIC16C71 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local Compuserve number.

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

PIC16C74

40-Pin EPROM-Based 8-Bit CMOS Microcontroller

FEATURES

High-Performance RISC-like CPU

- Only 35 single word instructions to learn
- All single cycle instructions (200ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- 4096 x 14 on-chip EPROM program memory
- 192 x 8 general purpose registers (SRAM)
- Interrupt capability
- 45 special function hardware registers
- Eight levels deep hardware stack
- Direct, indirect and relative addressing modes

Peripheral Features

- 33 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Two pins that can be configured as capture input, PWM output, or compare output
  - Capture is 16-bit, max resolution 200ns
  - Compare is 16-bit, max resolution 200ns
  - PWM resolution is 1- to 10-bit.
    8-bit resolution gives 80 KHz maximum frequency and 10-bit resolution gives 20 KHz maximum frequency
- TMR1: 16-bit timer/counter (time-base for capture/compare) TMR1 can be incremented during sleep via external crystal/clock (for real-time clock)
- TMR2: 8-bit timer/counter with 8-bit period register (time-base for PWM), prescaler and postscaler
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler
- 8-bit A/D converter with eight input channels
  - 16 µsec conversion time/channel
- Serial Communications Interface (SCI)
  - Full-duplex Asynchronous Communication or Half-Duplex Synchronous Communication
- Synchronous serial port (SSP) with two modes of operation:
  - 3-wire SPI
  - I²C™/ACCESS.bus compatible
- Parallel Slave Port (PSP): 8-bit wide, with external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls (microprocessor bus interface)

Special Microcontroller Features

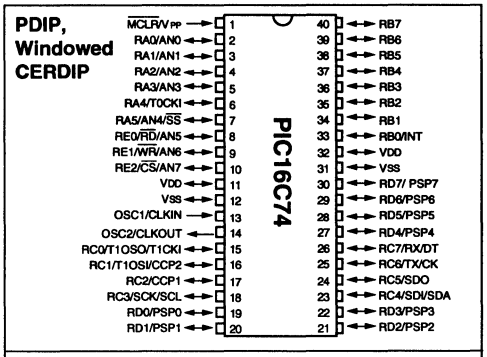
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security EPROM fuse for code-protection
- Power saving SLEEP mode
- EPROM fuses selectable oscillator options: (RC oscillator, Standard crystal/resonator, High speed crystal/resonator, Low frequency crystal)
- Serial in-system programming (via two pins)

CMOS Technology

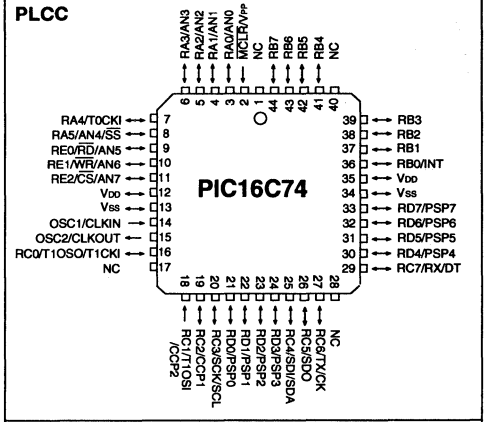
- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide-operating voltage range (2.5V to 6.0V)
- Commercial, Industrial, and Automotive Temp. Range
- Low power consumption
  - < 2mA @ 5V, 4 MHz
  - 15µA typical @ 3V, 32 KHz
  - <1µA typical standby current

PACKAGE TYPES

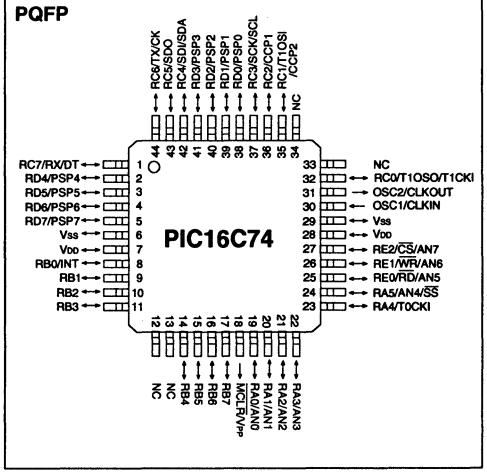
PDIP, Windowed CERDIP



PLCC



PQFP



1.0 GENERAL DESCRIPTION

The PIC16C74 is another 40-pin member of the versatile PIC16CXX family of low-cost, high-performance, CMOS, fully-static, EPROM-based 8-bit microcontrollers.

All PIC microcontrollers employ an advanced RISC-like architecture. The PIC16CXX has enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance. PIC16CXX microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in its class.

The PIC16C74 has 192 bytes of RAM and 33 I/O pins. In addition, the PIC16C74 adds several peripheral features useful in many high performance applications including; three timer/counters, two capture/compare/PWM modules and two serial ports. The synchronous serial port can be configured as either a 3-wire Serial Peripheral Interface (SPI) or the two-wire Inter-Intergrate Circuit (I^2C) bus. The Serial Communicatons Interface can be configured as either synchronous or asynchronous (USART). An 8-bit Parallel slave port is provided and eight channels of high-speed 8-bit A/D. The 8-bit resolution is ideally suited for appplications requireing low-cost analog interface, e.g. thermostat control, pressure sensing, etc.

These special features reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power- down) mode offers power saving. The user can wake up the chip from SLEEP through several external and internal interrupts and reset.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software malfunction.

A UV-erasable cerdip-packaged version is ideal for code development while the cost-effective One-Time Programmable (OTP) version is suitable for production in any volume.

Table 1-1 shows the features of the PIC16C74 as well as the other members of the PIC16CXX enhanced core family.

A simplified block diagram of the PIC16C74 is shown in Figure 3-1.

The PIC16C74 fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote sensors, keyboards and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16C74 very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of modifications. Code written for PIC16C5X can be easily ported to PIC16CXX family of devices (see Appendix B).

1.2 Development Support

The PIC16CXX family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a production quality programmer. A "C" compiler and fuzzy logic support tools are in development.

TABLE 1-1: PIC16CXX FAMILY OF DEVICES

		PIC16C74	PIC16C64 †	PIC16C71†	PIC16C84†
Maximum Frequency of Operation		20 MHz	20 MHz	16 MHz	10 MHz
Program Memory (14-bit wide)	EPROM	4K	2K	1K	-
	EEPROM	-	-	-	1K
Data Memory (bytes)		192	128	36	36
Data EEPROM (bytes)		-	-	-	64
Timer 0 (8-bit + 8-bit prescaler)		Yes	Yes	Yes	Yes
Timer 1 (16-bit)		Yes	Yes	-	-
Timer 2 (8-bit)		Yes	Yes	-	-
Capture/Compare/PWM Module(s)		2	1	-	-
Synchronous Serial Port (SPI/I²C)		Yes	Yes	-	-
Serial Communications Interface (USART)		Yes	-	-	-
Parallel Slave Port		Yes	Yes	-	
Analog to Digital Converter (8-bit)		8 ch.	-	4 ch.	-
Power On Reset		Yes	Yes	Yes	Yes
Watchdog Timer		Yes	Yes	Yes	Yes
External Interrupts		Yes	Yes	Yes	Yes
Interrupt Sources		12	8	4	4
Program Memory Code Protect		Yes	Yes	Yes	Yes
I/O		33	33	13	13
I/O High Current Capability	Source	25mA	25mA	20mA	20mA
	Sink	25mA	25mA	25mA	25mA
Package Types		40-pin DIP, 44-pin PLCC, 44-pin PQFP	40-pin DIP, 44-pin PLCC, 44-pin PQFP	18-pin DIP 18-pin SOIC	18-pin DIP 18-pin SOIC

† For information on these devices please refer to their respective data sheets.

2.0 PIC16C74 DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information and tables in this section. When placing orders, please use the "PIC16C74 Product Identification System" on the back page of this data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in cerdip package is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the oscillator modes etc. Microchip's PICSTART™ and PRO MATE™ programmers both support programming of the PIC16C74.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages permit the user to program them once. In addition to the program memory, the configuration fuses must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTP) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories. This improves bandwidth over traditional Von-Neuman architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. Instruction opcodes are 14-bit wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (see Figure 3-1). Consequently, all instructions (35) execute in a single cycle (200ns @ 20 MHz) except for program branches.

The PIC16C74 addresses 4K x 14 program memory space, all on-chip. Program execution is in internal memory only.

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16CXX has a fairly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16CXX device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

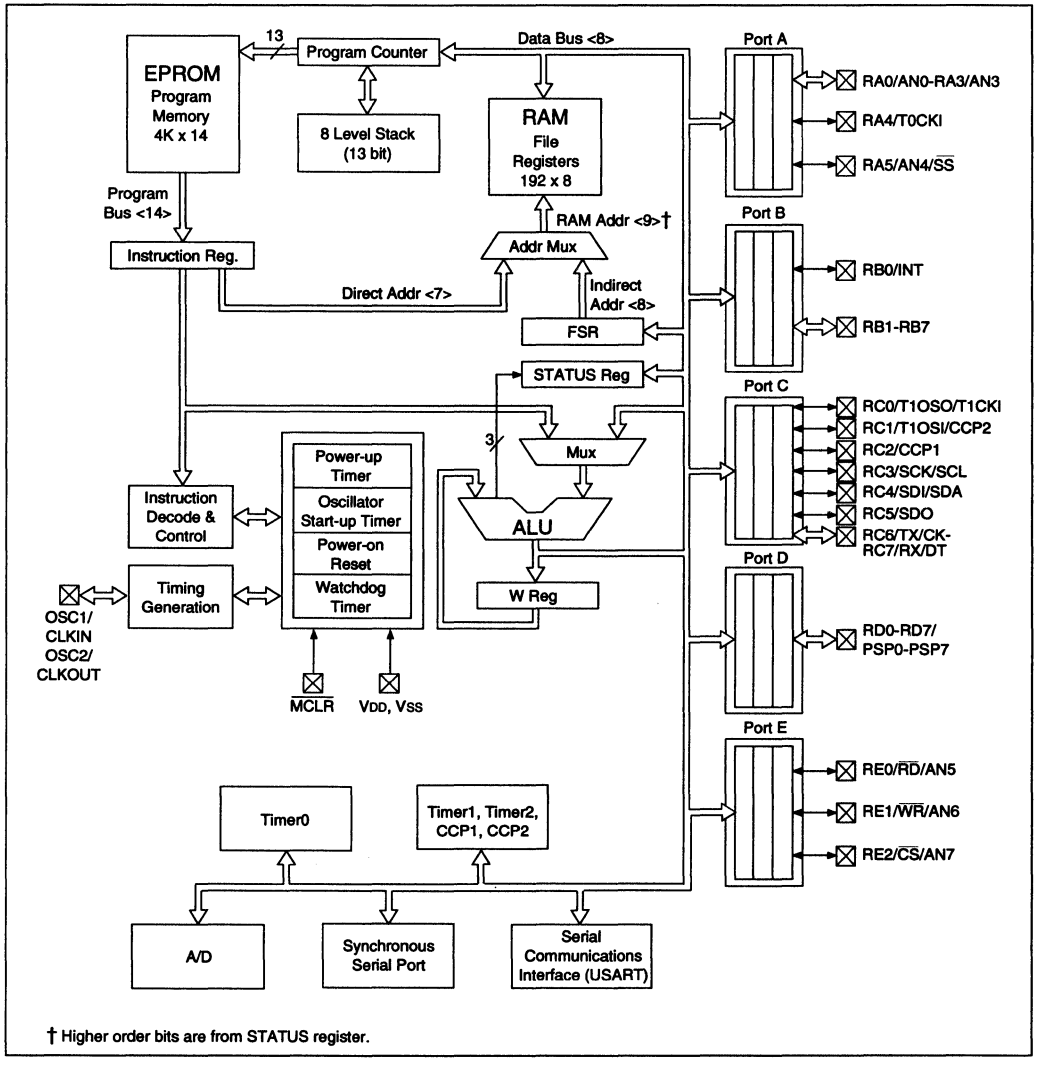
The ALU is 8-bit wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow out bit in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with a description of the device pins in Table 3-1.

FIGURE 3-1: PIC16C74 BLOCK DIAGRAM



† Higher order bits are from STATUS register.

TABLE 3-1: PIC16C74 PINOUT DESCRIPTION

Pin Name	DIP No.	PLCC No.	PQFP No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	CMOS	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	2	18	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
						PORTA is a bidirectional I/O port.
RA0/AN0	2	3	19	I/O	TTL	Analog input 0
RA1/AN1	3	4	20	I/O	TTL	Analog input 1
RA2/AN2	4	5	21	I/O	TTL	Analog input 2
RA3/AN3	5	6	22	I/O	TTL	Analog input 3
RA4/T0CKI	6	7	23	I/O	ST	Can also be selected to be the clock input to the TMR0 timer/counter. Output is open collector type.
RA5/AN4/$\overline{SS}$	7	8	24	I/O	TTL	Can also be the slave select for the synchronous serial port or analog input 4.
						PORTB is a bidirectional I/O port. Port B can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST†	RB0/INT can also be selected as an external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3	36	39	11	I/O	TTL	
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6	39	43	16	I/O	TTL/ST‡	Interrupt on change pin. Serial programming clock.
RB7	40	44	17	I/O	TTL/ST‡	Interrupt on change pin. Serial programming data.

Legend: I = input, O = output, I/O = input/output, P = power;
— = Not used, TTL = TTL input, ST = Schmitt trigger input

† This buffer is a Schmitt triger input when configured as the external interrupt.

‡ This buffer is a Schmitt Trigger input when used in serial programming mode.

(Cont.)

TABLE 3-1: PIC16C74 PINOUT DESCRIPTION (CONT.)

Name	Pin DIP No.	PLCC No.	PQFP No.	I/O/P Type	Buffer Type	Description
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	15	16	32	I/O	ST	RC0/T1OSO/T1CKI can also be selected as a Timer1 oscillator output/Timer1 clock input.
RC0/T1OSI/CCP2	16	18	35	I/O	ST	RC0/T1OSI/CCP2 can also be selected as a Timer1 oscillator input or Capture 2, input/Compare 2 output/ PWM 2 output.
RC2/CCP1	17	19	36	I/O	ST	RC2/CCP1 can also be selected as a capture1 input/ compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock for both SPI and I²C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I²C mode).
RC5/SDO	24	26	43	I/O	ST	RC5/SDO can also be selected as the SPI Data Out (SPI mode).
RC6/TX/CK	25	27	44	I/O	ST	RC6/TX/CK can also be selected as Asynchronous Transmit or SCI Synchronous Clock
RC7/RX/DT	26	29	1	I/O	ST	RC7/RX/DT can also be selected as the Asynchronous Receive or SCI Synchronous Data
						PORTD is a bidirectional I/O port or parallel slave port for interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL§	
RD1/PSP1	20	22	39	I/O	ST/TTL§	
RD2/PSP2	21	23	40	I/O	ST/TTL§	
RD3/PSP3	22	24	41	I/O	ST/TTL§	
RD4/PSP4	27	30	2	I/O	ST/TTL§	
RD5/PSP5	28	31	3	I/O	ST/TTL§	
RD6/PSP6	29	32	4	I/O	ST/TTL§	
RD7/PSP7	30	33	5	I/O	ST/TTL§	
RE0/$\overline{RD}$/AN5	8	9	25	I/O	ST/TTL§	Bidirectional I/O pin, read control for parallel slave port, or analog input 5 .
RE1/$\overline{WR}$/AN6	9	10	26	I/O	ST/TTL§	Bidirectional I/O pin, write control for parallel slave port, or analog input 6.
RE2/$\overline{CS}$/AN7	10	11	27	I/O	ST/TTL§	Bidirectional I/O pin, select control for parallel slave port, or analog input 7.
VSS	12,31	13,34	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17 28,40	12,13 33,34		—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input, O = output, I/O = input/output, P = power;
— = Not used, TTL = TTL input, ST = Schmitt trigger input

§ This buffer is a Schmitt trigger input when configured as general purpose I/O and a TTL input when used in the parallel slave port mode (for interfacing to a microprocessor bus).

3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

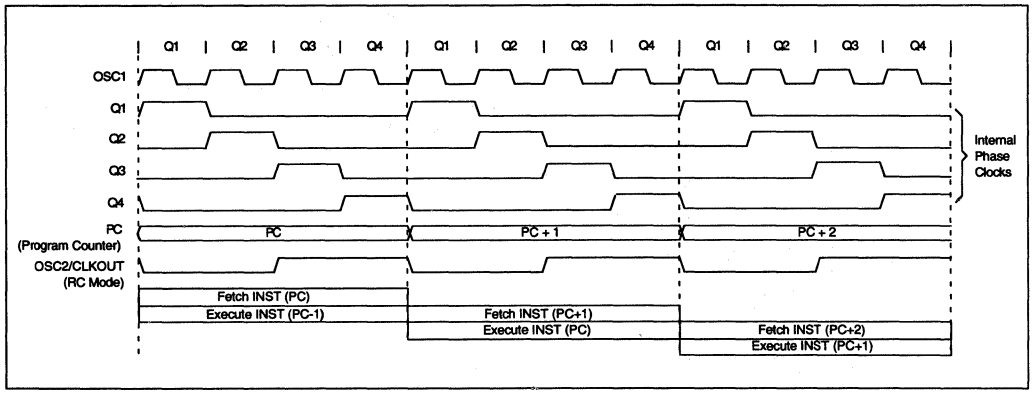
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction (see Example 3-1).

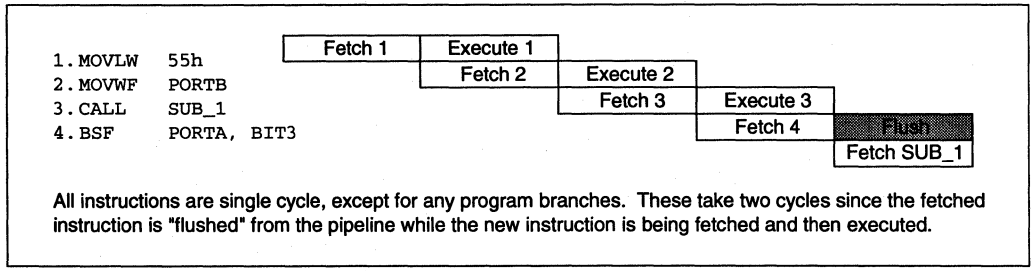
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



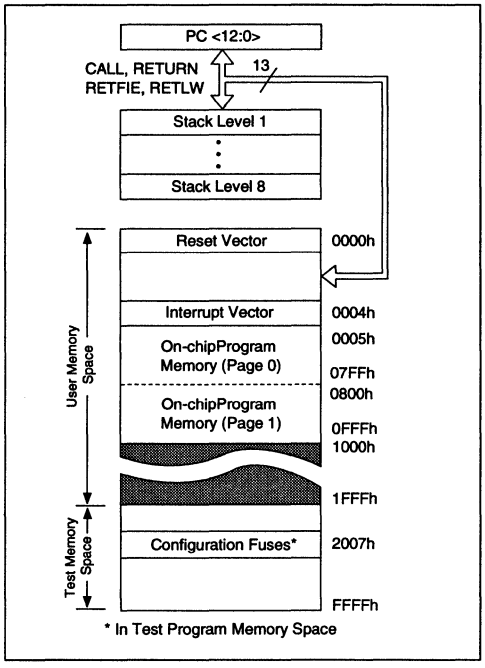
All instructions are single cycle, except for any program branches. These take two cycles since the fetched instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

4.0 MEMORY ORGANIZATION

4.1 Program Memory Organization

The PIC16C74 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 4K x 14 (0000h - 0FFFh) are physically implemented. Accessing a location above FFFh will cause a wrap-around within the first 4K x 14 space. The reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 4-1).

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

The data memory (see Figure 4-2) is partitioned into two Banks which contain the general purpose registers and the special function registers. Bank 0 is selected when the RP0 bit in the STATUS register is cleared. Bank 1 is selected when the RP0 bit in the STATUS register is set. Each Bank extends up to 7Fh (128 bytes). The first 32 locations of each Bank are reserved for the Special Function Registers. Register locations 20h-7Fh (Bank 0) and A0h-FFh (Bank 1) are general purpose registers implemented as static RAM. Some special function registers are mapped in Bank 1.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file, in PIC16C74 is organized as 192 x 8. It is accessed either directly or indirectly through the file select register FSR (see Section 4.4).

FIGURE 4-2: REGISTER FILE MAP

File address	Bank 0	Bank 1	
00	Indirect addr.(*)	Indirect addr.(*)	80
01	TMR0	OPTION	81
02	PCL	PCL	82
03	STATUS	STATUS	83
04	FSR	FSR	84
05	PORT A	TRIS A	85
06	PORT B	TRIS B	86
07	PORT C	TRIS C	87
08	PORT D	TRIS D	88
09	PORT E	TRIS E	89
0A	PCLATH	PCLATH	8A
0B	INTCON	INTCON	8B
0C	PIR1	PIE1	8C
0D	PIR2	PIE2	8D
0E	TMR1L	PCON	8E
0F	TMR1H		8F
10	T1CON		90
11	TMR2		91
12	T2CON	PR2	92
13	SSPBUF	SSPADD	93
14	SSPCON	SSPSTAT	94
15	CCPR1L		95
16	CCPR1H		96
17	CCP1CON		97
18	RCSTA	TXSTA	98
19	TXREG	SPBRG	99
1A	RCREG		9A
1B	CCPR2L		9B
1C	CCPR2H		9C
1D	CCP2CON		9D
1E	ADRES		9E
1F	ADCON0	ADCON1	9F
20	General Purpose Register	General Purpose Register	A0
7F			FF

* Not a physical register

Unimplemented data memory locations; read as '0's

4.2.2 SPECIAL FUNCTION REGISTERS:

The special function registers are registers used by the CPU and Peripheral functions for controlling the desired operation of the device (see Table 4-1). These registers are static RAM.

The special registers can be classified into two sets. The special registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16C74

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0									
00†	INDF (Indirect Address)	Addressing this location uses contents of FSR to address data memory (not a physical register)							
01	TMR0	Timer0							
02†	PCL	Program Counter's (PC's) Least Significant Byte							
03†	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
04†	FSR	Indirect data memory address pointer							
05	PORTA	PORTA Data Latch where written to PORTA pins when read							
06	PORTB	PORTB Data Latch where written to PORTB pins when read							
07	PORTC	PORTC Data Latch where written to PORTC pins when read							
08	PORTD	PORTD Data Latch where written to PORTD pins when read							
09	PORTE	PORTE Data Latch where written to PORTE pins when read							
0A†	PCLATH	Buffered Register for the upper 5 bits of the Program Counter (PC)							
0B†	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
0D	PIR2	–	–	–	—	–	–	–	CCP2IF
0E	TMR1L	Timer1 Least Significant Byte							
0F	TMR1H	Timer1 Most Significant Byte							
10	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1INSYNC	TMR1CS	TMR1ON
11	TMR2	Timer2							
12	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
13	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register							
14	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
15	CCPR1L	Capture/Compare/Duty Cycle Register (LSB)							
16	CCPR1H	Capture/Compare/Duty Cycle Register (MSB)							
17	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0
18	RCSTA	SPEN	RC8/9	SREN	CREN	–	FERR	OERR	RCD8
19	TXREG	SCI Transmit Data Register							
1A	RCREG	SCI Receive Data Register							
1B	CCPR2L	Capture/Compare/Duty Cycle Register 2 (LSB)							
1C	CCPR2H	Capture/Compare/Duty Cycle Register 2 (MSB)							
1D	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0
1E	ADRES	A/D Result Register							
1F	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	–	ADON

Legend — = Unimplemented locations, Read as '0'

(Cont.)

† These registers can be addressed from either bank.

TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16C74 (CONT.)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1									
80†	INDF (Indirect Address)	Addressing this location uses contents of FSR to address data memory (not a physical register)							
81	OPTION	$\overline{RBPU}$	INTEDG	RTS	RTE	PSA	PS2	PS1	PS0
82†	PCL	Program Counter's (PC's) Least Significant Byte							
83†	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
84†	FSR	Indirect data memory address pointer							
85	TRISA	PORTA Data Direction Register							
86	TRISB	PORTB Data Direction Register							
87	TRISC	PORTC Data Direction Register							
88	TRISD	PORTD Data Direction Register							
89	TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0
8A†	PCLATH	Shadow Register for the upper 5 bits of the Program Counter (PC)							
8B†	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
8C	PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
8D	PIE2	—	—	—	—	—	—	–	CCP2IE
8E	PCON	—	—	—	—	—	—	$\overline{POR}$	—
8F	Reserved								
90	Reserved								
91	Reserved								
92	PR2	Timer2 Period Register							
93	SSPADD	Synchronous Serial Port (I^2C mode) Address Register							
94	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
95	Reserved								
96	Reserved								
97	Reserved								
98	TXSTA	CSRC	TX8/9	TXEN	SYNC	–	BRGH	TRMT	TXD8
99	SPBRG	Baud Rate Register							
9A	Reserved								
9B	Reserved								
9C	Reserved								
9D	Reserved								
9E	Reserved								
9F	ADCON1	–	–	–	–	–	PCFG2	PCFG1	PCFG0

Legend — = Unimplemented locations, Read as '0'
† These registers can be addressed from either bank.

4.2.2.1 **STATUS** Register

The STATUS register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for data memory.

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the logic. Furthermore, $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

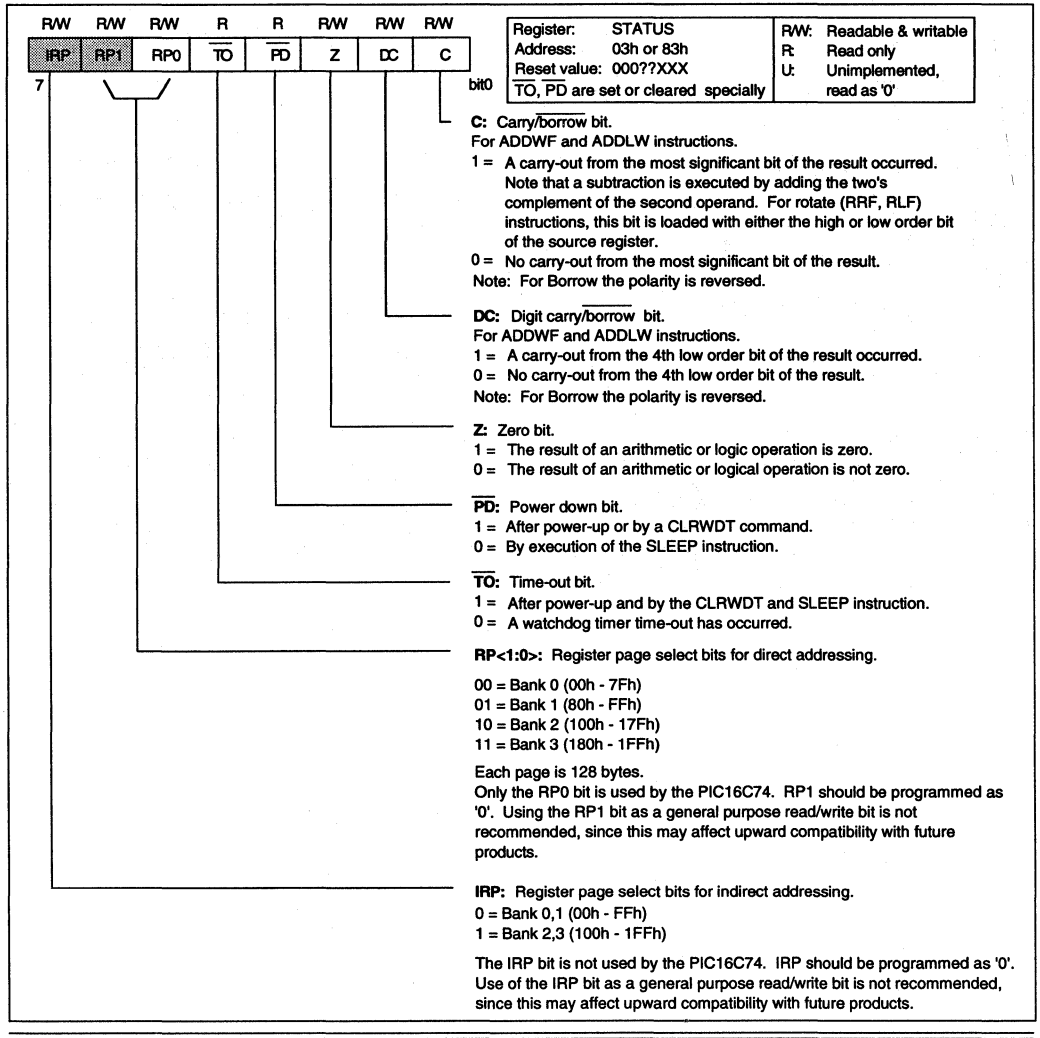
For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the status register as 000UU1UU (where U = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the status registers because these instructions do not affect any status bit. For other instructions, affecting any status bits, see the "Instruction Set Summary".

Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16C74 and should be programmed as '0'. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

Note 2: The C and DC bits operate as a $\overline{borrow}$ out bit in subtraction. See the SUBLW and SUBWF instructions for examples.

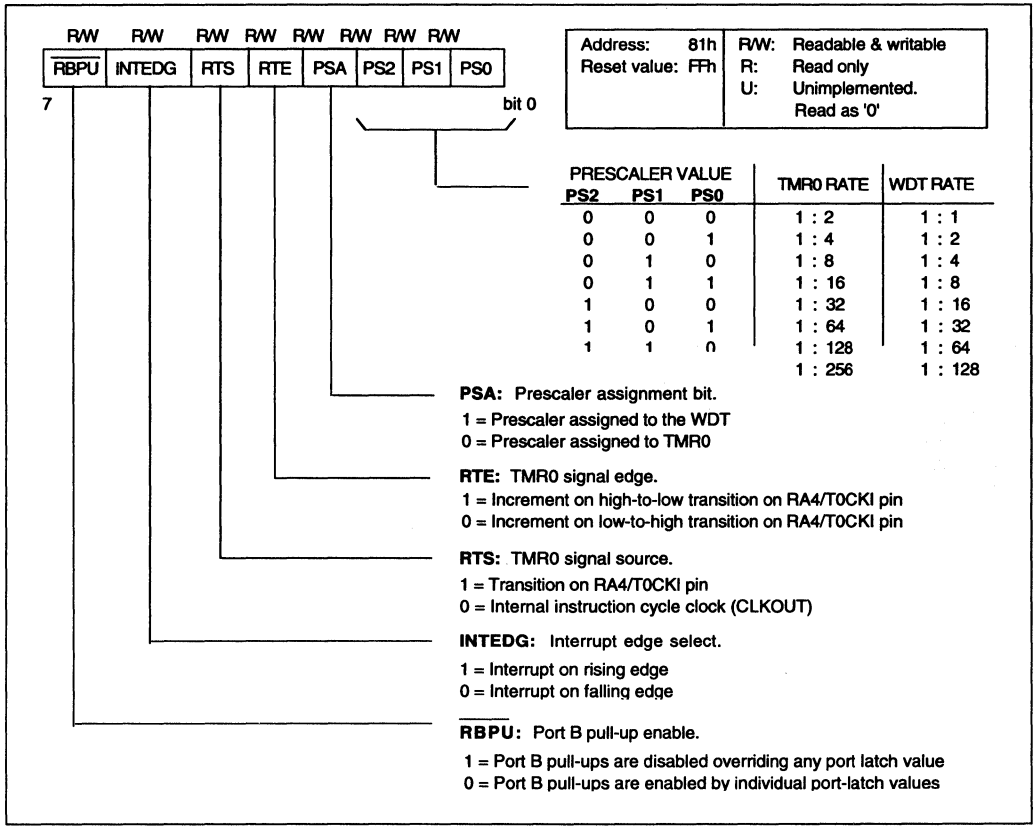
FIGURE 4-3: STATUS REGISTER



4.2.2.2 **OPTION** Register

The OPTION register (address 81h) is a readable and writable register which contains various control bits to configure the prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

FIGURE 4-4: OPTION REGISTER



4.2.2.3 **INTCON** Register

The PIC16C74 has twelve sources of interrupt:

- External interrupt from RB0/INT pin
- Timer0 overflow
- Interrupt on change on RB<7:4> pins
- Timer1 overflow
- Timer2 matches period register
- A capture, a compare, or a PWM output is reset
- The synchronous serial port
- The parallel slave port read/write
- A/D complete interrupt
- USART receive/transmit interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global enable bits. The peripheral interrupt flags reside in the PIR1 register (Addr 0Ch).

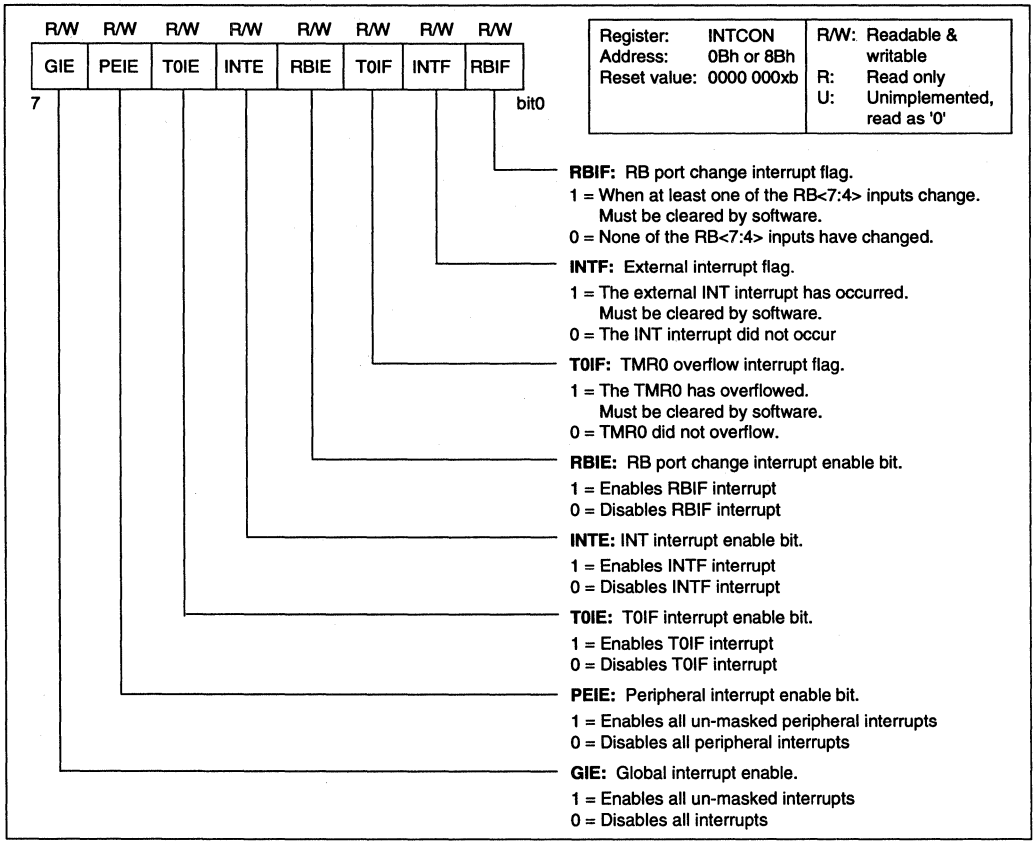
A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding mask bit in INTCON register (Figure 4-5). GIE is cleared on reset.

When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs (see Figure 12-15). The latency is the same for one or two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

The "return from interrupt" instruction, RETFIE, exits interrupt routine as well as sets the GIE bit to re-enable interrupts.

Note: The T0IF, INTF, or RBIF will be set by the specified condition even if the corresponding Interrupt Enable Bit is cleared (interrupt disabled) or the GIE bit is cleared (all interrupts disabled).

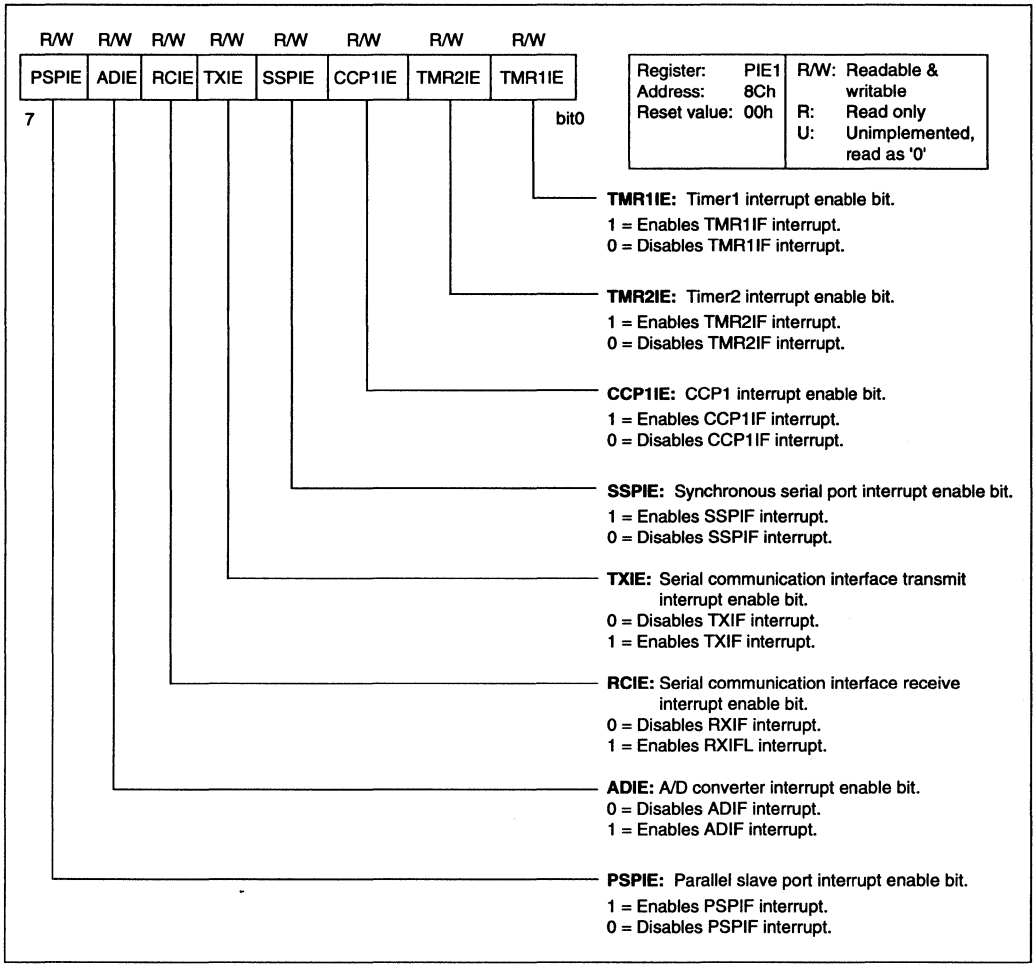
FIGURE 4-5: INTCON REGISTER



4.2.2.4 **PIE1** Register

This register contains the individual enable bits for the Peripheral Interrupts.

FIGURE 4-6: PIE1 REGISTER

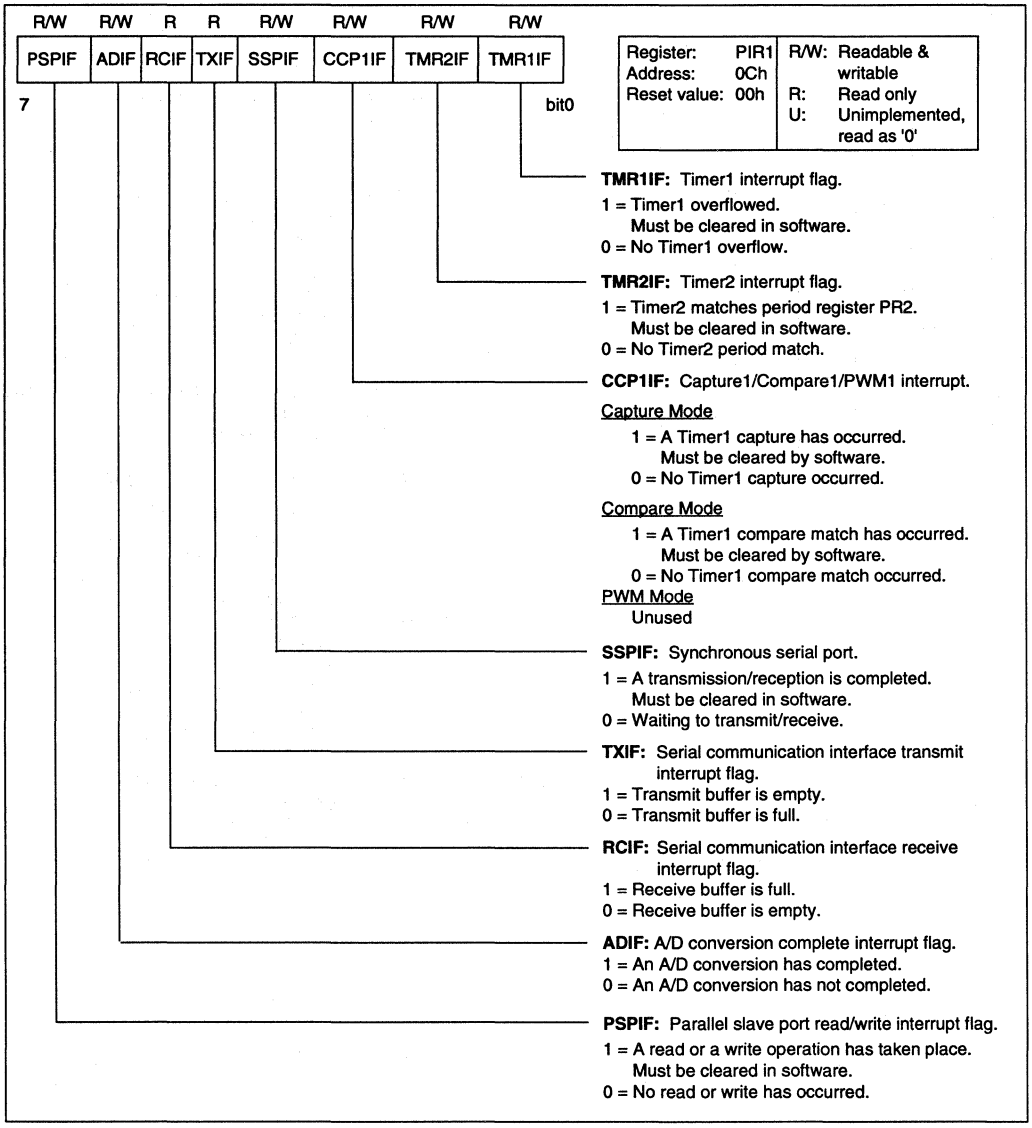


4.2.2.5 PIR1 Register

This register contains the individual flag bits for the Peripheral Interrupts.

Note: These bits will be set by the specified condition, even if the corresponding Interrupt Enable bit is cleared (interrupt disabled) or the GIE bit is cleared (all interrupts disabled). Before enabling an Interrupt, the user may wish to clear the interrupt flag, to ensure that the program does not immediately branch to the Peripheral Interrupt service routine.

FIGURE 4-7: PIR1 REGISTER



4.2.2.6 **PIE2** Register

This register contains the individual enable bit for the Peripheral Interrupts.

4.2.2.7 **PIR2** Register

This register contains the individual flag bit for the Peripheral Interrupts.

Note: This bit will be set by the specified condition, even if the corresponding Interrupt Enable bit is cleared (interrupt disabled) or the GIE bit is cleared (all interrupts disabled). Before enabling an interrupt, the user may wish to clear the interrupt flag, to ensure that the program does not immediately branch to the Peripheral Interrupt service routine.

2

FIGURE 4-8: PIR2 REGISTER

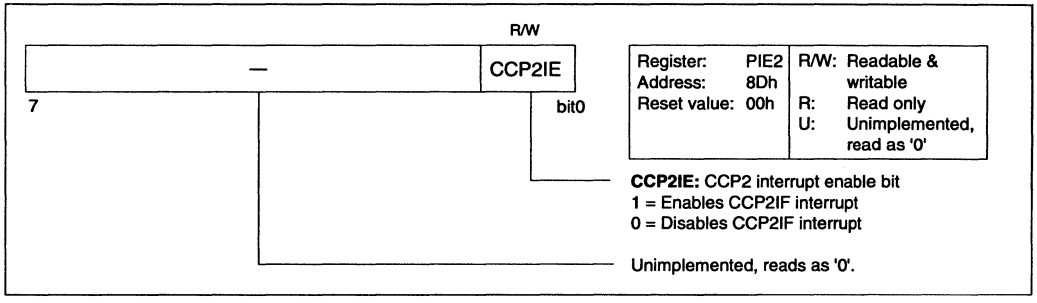
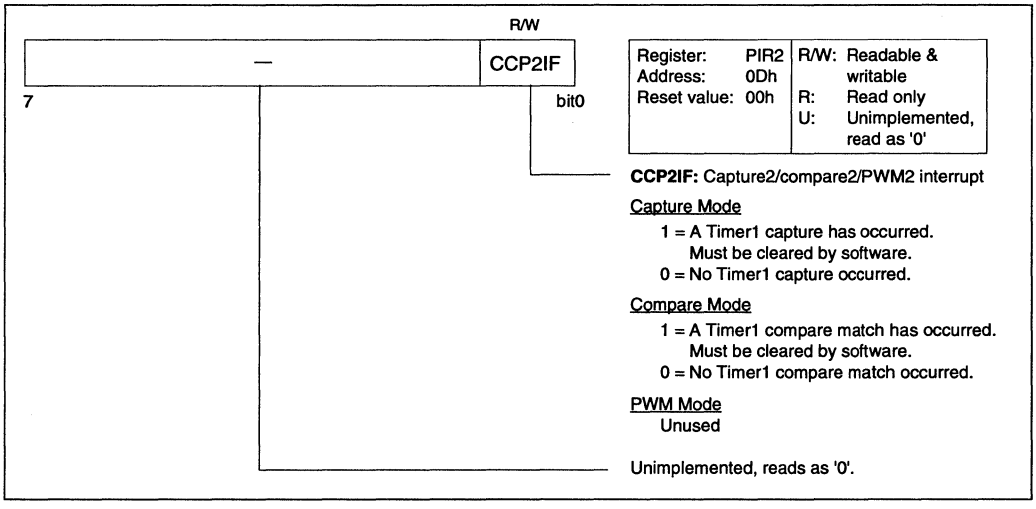


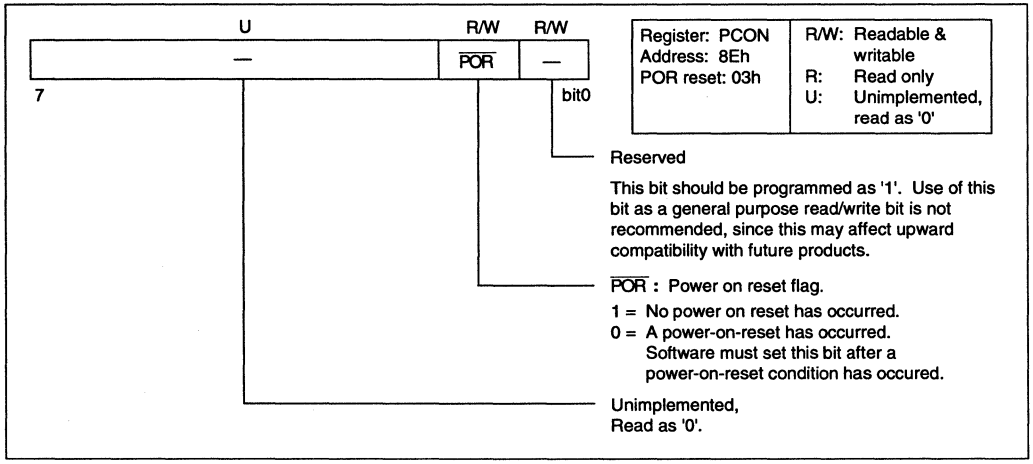
FIGURE 4-9: PIE2 REGISTER



4.2.2.8 **PCON** Register

The PCON register contains flag bits to allow differentiation between a Power-on Reset to an external MCLR reset, WDT reset.

FIGURE 4-10: PCON REGISTER

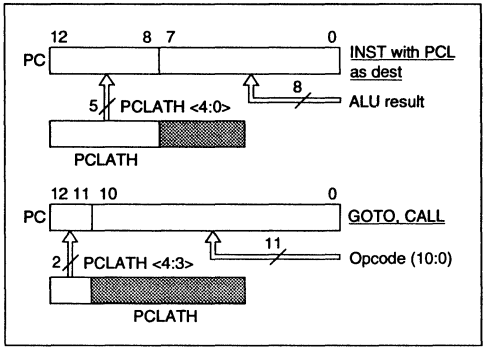


For further details on interrupts, please refer to the "Interrupts" Section.

4.3 PCL and PCLATH

The program counter (PC) is 13-bit wide. The low byte, PCL is a readable and writable register (addr 02h or 82h). The high byte of the PC (PCH) is not directly readable or writable. The high byte of the PC can be written through the PCLATH register (addr 0Ah or 8Ah). When the PC is loaded with a new value during a CALL, GOTO or a write to PCL, the high bits of PC are loaded from PCLATH as shown in Figure 4-11.

FIGURE 4-11: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note "Table Read Using the PIC16CXX" (AN556).

4.3.2 Stack

The PIC16CXX has an 8-bit deep x 13-bit wide hardware stack (see Figure 4-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed in the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is POPped in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a "PUSH" or a "POP" operation.

The stack operates as a circular buffer. This means that after the stack has been "PUSHed" eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on). This means that the user can implement "software resets" for the system.

Note: There are no STATUS bits to indicate stack overflows or stack underflow conditions.

4.3.3 Program Memory Paging

The PIC16C74 has 4-Kbytes of program memory, but the CALL and GOTO instructions only have a 11-bit address range. This 11-bit address range allows a branch within a 2-Kbyte program memory page size. To allow CALL and GOTO instructions to address the entire 4-Kbyte program memory address range, there must be another bit to specify the program memory page. This paging bit comes from the PCLATH<3> bit (see Figure 4-11). When doing a CALL or GOTO instruction, the user must ensure that this page bit (PCLATH<3>) is programmed to the desired program memory page. If a CALL instruction (or interrupt) is executed, the entire 13-bit PC is pushed onto the stack. Therefore, manipulation of the PCLATH<3> is not required for the return instructions (which pops the PC from the stack).

Note: The PIC16C74 ignores the PCLATH<4> bit, which is used for program memory pages 2 and 3 (1000h - 1FFFh). The use of PCLATH<4> as a general purpose read/write bit is not recommended since this may affect upward compatibility with future products.

Example 4-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that the PCLATH is saved and restored by the interrupt service routine (if interrupts are used).

EXAMPLE 4-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

```
ORG 0X500
BSF     PCLATH, 3  ; Select page 1 (800h-FFFh)

CALL    SUB1_P1    ; Call subroutine in
        :          ; page 1 (800h-FFh)
        :
        :
ORG     0x900
SUB1-P1 :          ; called subroutine
        :          ; page 1 (800h-FFh)
        :
RETURN             ; return to page 0
                   ; (000h-7FFh)
```

4.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause an indirect addressing.

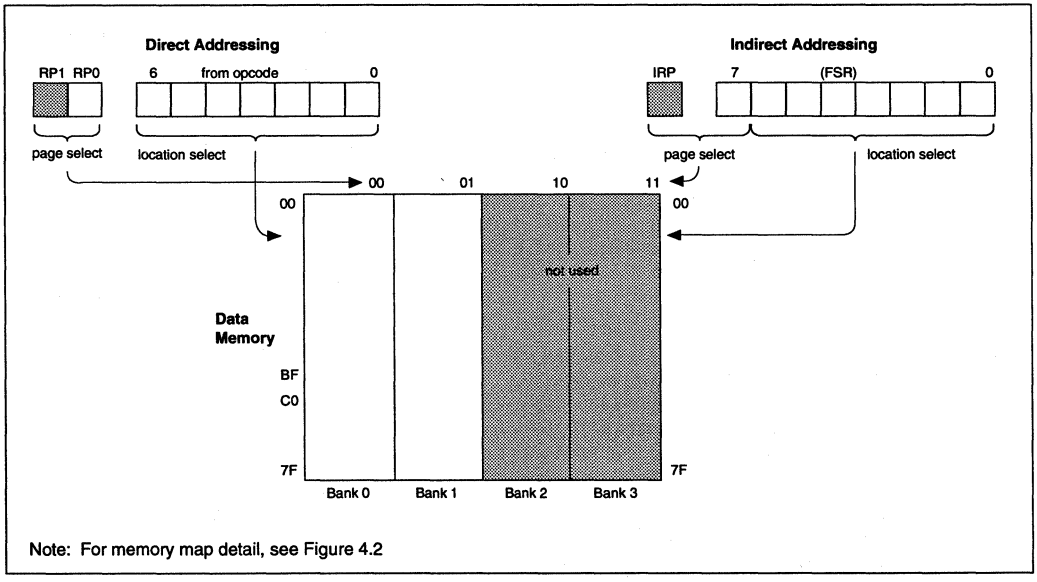
Indirect addressing is possible by using the INDF register (address 00h). Any instruction using the INDF register actually accesses data pointed to by the file select register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-10. However, IRP is not used in this PIC16C74.

A simple program to clear RAM location20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: INDIRECT ADDRESSING

```
        movlw   0x20    ;initialize pointer
        movwf   FSR     ;to RAM
NEXT    clrf    INDF    ;clear indent by
        incrf   FSR     ;inc pointer
        btfss   FSR,4   ;all done?
        goto    NEXT    ;no clear next
CONTINUE:               ;yes continue
```

FIGURE 4-12: DIRECT/INDIRECT ADDRESSING



Note: For memory map detail, see Figure 4.2

5.0 I/O PORTS

The PIC16C74 has five ports, PORTA through PORTE. These ports pins may be multiplexed with an alternate function for the peripheral features on the device.

5.1 PORTA and TRISA Registers

PORTA is a 6-bit wide latch. RA4 is a Schmitt trigger input and an open collector output. All other RA port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as output or input.

A '1' in the TRISA register configures the corresponding port pin as input.

Reading PORTA register reads the status of the pins whereas writing to it will write to the port latch.

Port RA4 is multiplexed with TMR0 clock input.

Other PORTA pins are multiplexed with analog inputs and analog VREF input. The operation of these pins are selected by control bits in ADCON1 (A/D control register1) register. When selected as an analog input, these pins will read as '0's.

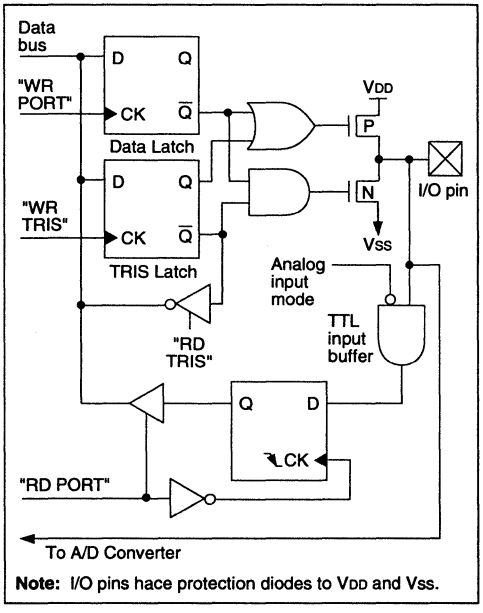
Note: On Power-on Reset, these pins are configured as analog inputs.

TRISA controls the direction of the RA pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

EXAMPLE 5-1: INITIALIZING PORTA

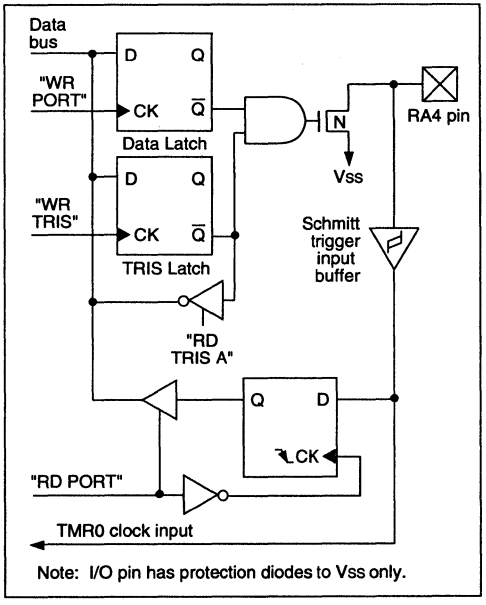
```
CLRF    PORTA       ;Initialize PORTA by setting
                    ; output data latches
BSF     STATUS, RP0 ;Select Bank1
MOVLW   0xCF        ;Value used to initialize
                    ;data direction
MOVWF   TRISA       ;Set RA<3:0> as inputs
                    ;    RA<5:4> as outputs
                    ;TRISA<7:6> are always
                    ;read as '0'.
```

FIGURE 5-1: BLOCK DIAGRAM OF PORT PINS RA<3:0> and RA<5>



Note: I/O pins hace protection diodes to VDD and Vss.

FIGURE 5-2: BLOCK DIAGRAM OF RA4 PIN



Note: I/O pin has protection diodes to Vss only.

TABLE 5-1: PORTA FUNCTIONS

Name	Bit	Buffer Type	Function
RA0/AN0	bit0	TTL	Input/output or analog input
RA1/AN1	bit1	TTL	Input/output or analog input
RA2/AN2	bit2	TTL	Input/output or analog input
RA3/AN3	bit3	TTL	Input/output or analog input
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open collector type
RA5/AN4/$\overline{SS}$	bit5	TTL	Input/output, slave select input for synchronous serial port, or analog input

Legend: TTL = TTL input, ST = Schmitt trigger input

TABLE 5-2: SUMMARY OF PORTA REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTA	PORTA pins when read PORTA latch when written	05h	--XX XXXX
TRISA	PORTA data direction register 0 = output, 1 = input	85h	--11 1111

Notes: 1: x = unknown, - = unimplemented, reads as a '0'.
2: For reset values of registers in other reset situations refer to Table 12-6.

5.2 PORTB and TRISB Registers

PORTB is an 8-bit wide bidirectional port (file register address 06h). The corresponding data direction register is TRISB (address 86h). A '1' in TRISB configures the corresponding port pin as an input. Reading PORTB register reads the status of the pins, whereas writing to it will write to the port latch.

Each of the PORTB pins has a weak internal pull-up (~100 µA typical). A single control bit can turn on all the pull-ups. This is done by clearing the RBPU (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on power-on reset.

Four of PORTB's pins, RB<7:4>, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7–RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7–RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7–RB4 are OR'ed together to generate the RBIF interrupt (flag latched in INTCON<0>).

This interrupt can wake the device up from SLEEP. The user, in the interrupt service routine, can clear the interrupt in one of two ways:

a) Disable the interrupt by clearing RBIE (INTCON<3>) bit.

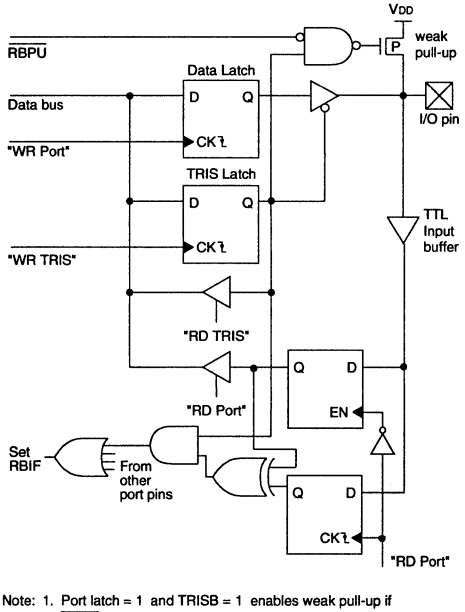
b) Read PORTB. This will end mismatch condition. Then, clear the RBIF bit.

A mismatch condition will continue to set the RBIF bit. Reading PORTB will end the mismatch condition, and allow the RBIF bit to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression. (See AN552 in the *Embedded Control Handbook*).

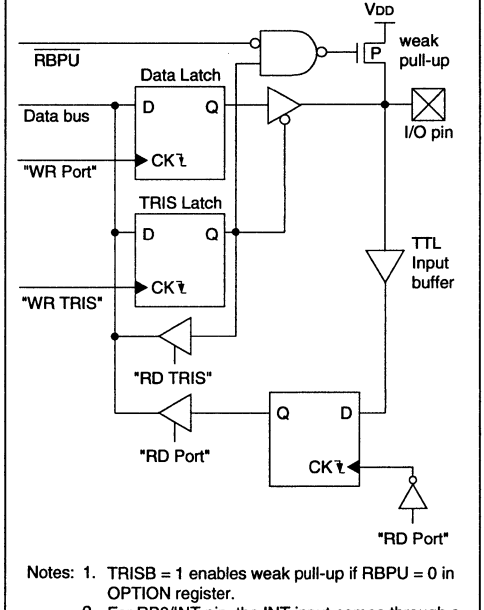
Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not be set.

FIGURE 5-3: BLOCK DIAGRAM OF PORT PINS RB<7:4>



Note: 1. Port latch = 1 and TRISB = 1 enables weak pull-up if $\overline{RBPU}$ = 0 in OPTION register.
2. I/O pins have diode protection to VDD and Vss.

FIGURE 5-4: BLOCK DIAGRAM OF PORT PINS RB<3:0>



Notes: 1. TRISB = 1 enables weak pull-up if RBPU = 0 in OPTION register.
2. For RB0/INT pin, the INT input comes through a Schmitt trigger input buffer.
3. I/O pins have diode protection to VDD and Vss.

TABLE 5-3: PORTB FUNCTIONS

Name	Bit	Buffer Type	Function
RB0/INT	bit0	TTL/ST†	Input/output pin or external interrupt input. Internal software programmable weak pull-up
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up
RB6	bit6	TTL/ST‡	Input/output pin (with interrupt on change). Internal software programmable weak pull-up
RB7	bit7	TTL/ST‡	Input/output pin (with interrupt on change). Internal software programmable weak pull-up

Legend: TTL = TTL input, ST = Schmitt Trigger
† This buffer is a Schmitt triger input when configured as the external interrupt.
‡ This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 5-4: SUMMARY OF PORTB REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTB	PORTB pins when read PORTB latch when written	06h	xxxx xxxx
TRISB	PORTB data direction register 0 = output, 1 = input	86h	1111 1111
$\overline{\text{OPTION}}$	Weak pull-up on/off control ($\overline{\text{RBPU}}$ bit)	81h	1111 1111

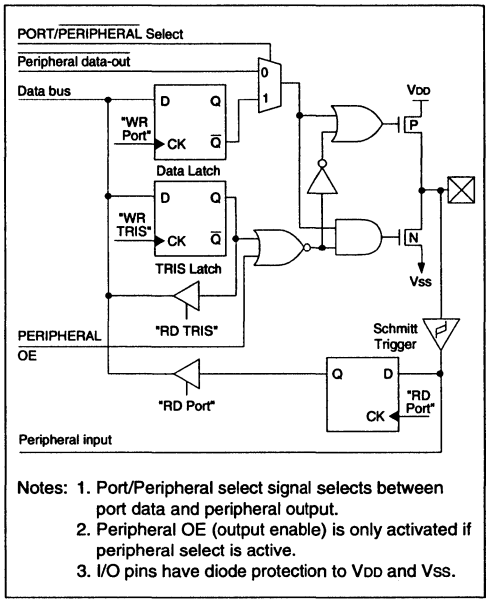
5.3 PORTC and TRISC Registers

I/O PORTC is an 8-bit bidirectional port. Each pin is individually configurable as input and output through the TRISC register. PORTC is multiplexed with several peripheral functions (see Table 5-5). PORTC pins have Schmitt trigger input buffers.

EXAMPLE 5-2: INITIALIZING PORTC

```
CLRF    PORTC       ;Initialize PORTC data
                    ;    latches before setting
                    ;    the data direction
                    ;    register
BSF     STATUS, RP0 ;Select Bank1
MOVLW   0xCF        ;Value used to initialize
                    ;data direction
MOVWF   TRISC       ;Set RC<3:0> as inputs
                    ;    RC<5:4> as outputs
                    ;    RC<7:6> as inputs
```

FIGURE 5-5: PORTC BLOCK DIAGRAM



Notes: 1. Port/Peripheral select signal selects between port data and peripheral output.
2. Peripheral OE (output enable) is only activated if peripheral select is active.
3. I/O pins have diode protection to VDD and VSS.

TABLE 5-5: PORTC FUNCTIONS

Name	Bit	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin, Timer1 oscillator input, Timer or Capture 2 input/Compare 2 output/PWM 2 output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/ PWM1 output
RC3/SCK/SCL	bit3	ST	RC3/SCK/SCL can also be selected as the synchronous serial clock for both SPI and I²C modes.
RC4/SDI/SDA	bit4	ST	RC4/SDI/SDA can also be selected as the SPI Data In (SPI mode) or data I/O (I²C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous serial port data output
RC6/TX/CK	bit6	ST	Input/output port pin, SCI Asynchronous Transmit, or SCI Synchronous Clock
RC7/RX/DT	bit7	ST	Input/output port pin SCI Asynchronous Receive, or SCI Synchronous Data

Legend: ST = Schmitt Trigger Input

TABLE 5-6: SUMMARY OF PORTC REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTC	PortC pins when read PortC latch when written	07h	XXXX XXXX
TRISC	PortC data direction register 0 = output, 1 = input	87h	1111 1111

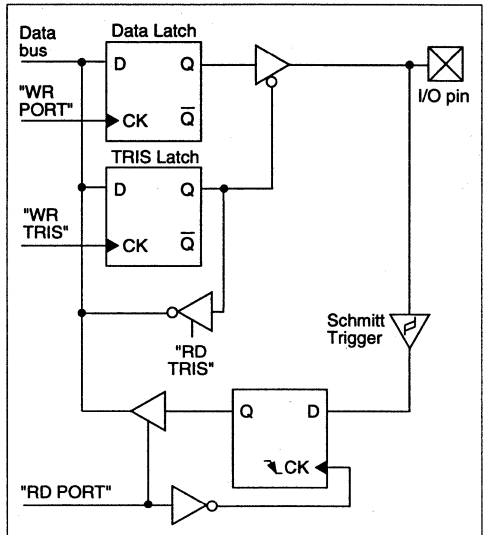
Notes: 1: x = unknown, - = unimplemented, reads as a '0'.
2: For reset values of registers in other reset situations refer to Table.

5.4 PORTD and TRISD Registers

I/O PortD is an 8-bit port with Schmitt trigger input buffers. Each pin is individually configurable as input or output.

PORTD can be configured as an 8-bit wide microprocessor port (or parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

FIGURE 5-6: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)



Note: I/O pins have protection diodes to VDD and Vss.

TABLE 5-7: PORTD FUNCTIONS

Name	Bit	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL	Input/output port pin or parallel slave port bit 0
RD1/PSP1	bit1	ST/TTL	Input/output port pin or parallel slave port bit 1
RD2/PSP2	bit2	ST/TTL	Input/output port pin or parallel slave port bit 2
RD3/PSP3	bit3	ST/TTL	Input/output port pin or parallel slave port bit 3
RD4/PSP4	bit4	ST/TTL	Input/output port pin or parallel slave port bit 4
RD5/PSP5	bit5	ST/TTL	Input/output port pin or parallel slave port bit 5
RD6/PSP6	bit6	ST/TTL	Input/output port pin or parallel slave port bit 6
RD7/PSP7	bit7	ST/TTL	Input/output port pin or parallel slave port bit 7

Legend: ST = Schmitt Trigger Input, TTL = TTL input

TABLE 5-8: SUMMARY OF PORTD REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTD	PORTD pins when read PORTD latch when written	08h	xxxx xxxx
TRISD	PORTD data direction register 0 = output, 1 = input	88h	1111 1111

Notes: 1: x = unknown, - = unimplemented, reads as a '0'.
2: For reset values of registers in other reset situations refer to Table.

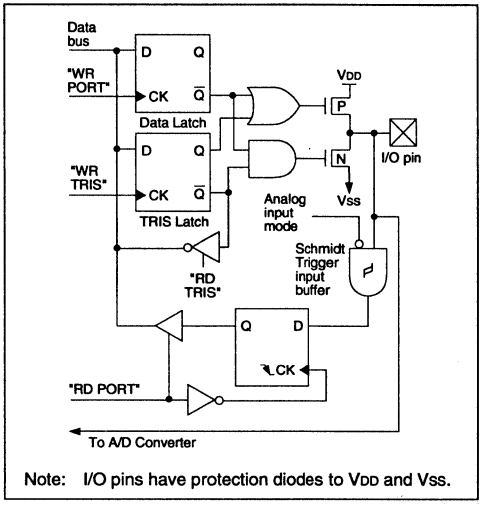
5.5 PORTE and TRISE Register

I/O PORTE has three pins RE0, RE1 and RE2, which are individually configurable as inputs or outputs. These have Schmitt trigger input buffers.

I/O PORTE becomes control inputs for the microprocessor port when the PSPMODE bit (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs). In this mode the input buffers are TTL.

Figure 5-8 shows the TRISE register, which also controls the synchronous slave port operation.

FIGURE 5-7: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)



Note: I/O pins have protection diodes to VDD and Vss.

FIGURE 5-8: TRISE REGISTER

R	R	R/W	R/W	U	R/W	R/W	R/W
IBF	OBF	IBOV	PSPMODE	-	TRISE2	TRISE1	TRISE0
							bit0

Register: TRISE Address: 89h POR value: 07h	R/W: Readable & writable R: Read only U: Unimplemented, read as '0'

TRISE0: Direction control bit for port pin RE0
1 = Input
0 = Output

TRISE1: Direction control bit for port pin RE1
1 = Input
0 = Output

TRISE2: Direction control bit for port pin RE2
1 = Input
0 = Output

Unimplemented.
Read as '0'

PSPMODE: Selects parallel slave port mode for ports RD and RE.
1 = Parallel slave port mode.
0 = General purpose I/O.

IBOV: Input buffer overflow in microprocessor mode.
1 = A write occurred when a previous input word has not been read.
Must be cleared in software.
0 = No overflow has occurred.

OBF: Output buffer full.
1 = The output buffer still holds a previously written word.
0 = Output buffer has been read.

IBF: Input buffer full.
1 = A word has been received and waiting to be read by the CPU.
0 = No word has been received.

TABLE 5-9: PORTE FUNCTIONS

Name	Bit	Buffer Type	Function
RE0/$\overline{RD}$/AN5	bit0	ST/TTL	Input/output port pin, Read control input in parallel slave port mode, or analog input $\overline{RD}$ 1 = Not a read operation 0 = Read operation. The system reads the PIC16C74 PORTD register (if chip selected)
RE1/$\overline{WR}$/AN6	bit1	ST/TTL	Input/output port pin, Write control input in parallel slave port mode, or analog input $\overline{WR}$ 1 = Not a write operation 0 = Write operation. The system writes to the PIC16C74 PORTD register (if chip selected)
RE2/$\overline{CS}$/AN7	bit2	ST/TTL	Input/output port pin, Chip select control input in parallel slave port mode, or analog input $\overline{CS}$ 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger Input, TTL = TTL input

TABLE 5-10: SUMMARY OF PORTE REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTE	PORTE pins when read PORTE latch when written	09h	---- -XXX
TRISE	PORTE data direction control bits and PORTD mode control	89h	0000 -111

5.6 I/O Programming Considerations

5.6.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit 5 of PORTB will cause all eight bits of PORTtB to be read into the CPU. Then the BSF operation takes place on bit 5 and PORTB is written to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

Reading the PORT register, reads the values of the PORT pins. Writing to the PORT register writes the value to the PORT latch. When using read modify write instructions (ex. BCF, BSF, etc.) on a PORT, the value of the PORT pins is read, the desired operation is done to this value, and this value is then written to the PORT latch.

Example 5-3 shows the effect of two sequential read modify write instructions (ex. BCF, BSF, etc.) on an I/O PORT.

EXAMPLE 5-3: READ MODIFY WRITE INSTRUCTIONS ON AN I/O PORT

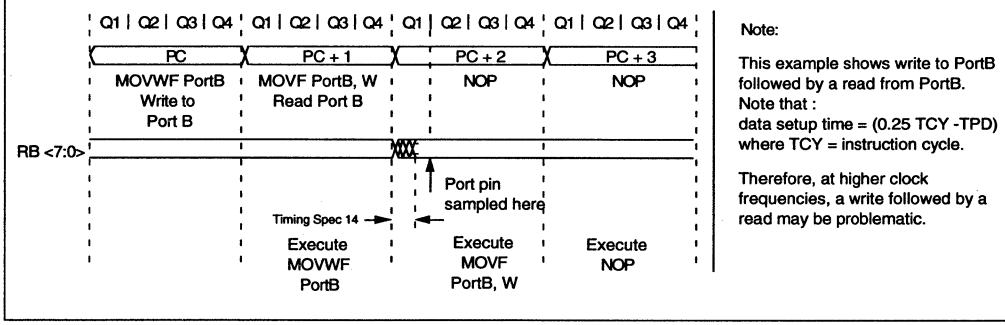
```
; Initial PORT settings:  PORTB<7:4> Inputs
;                         PORTB<3:0> Outputs
; PORTB<7:6> have external pull-up and are not
; connected to other circuitry.
;
;                          PORT latch   PORT pins
;                          ----------   ---------

    BCF    PORTB, 7      ; 01pp pppp   11pp pppp
    BCF    PORTB, 6      ; 10pp pppp   11pp pppp
    BSF    STATUS, RP0   ;
    BCF    TRISB, 7      ; 10pp pppp   11pp pppp
    BCF    TRISB, 6      ; 10pp pppp   10pp pppp
;
; Note that the user may have expected the pin
; values to be 00pp pppp. The 2nd BCF caused RB7
; to be latched as the pin value (High).
```

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

5.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see Figure 5-9). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

FIGURE 5-9: SUCCESSIVE I/O OPERATION



5.7 Parallel Slave Port

PORTD operates as an 8-bit wide parallel slave port, or microprocessor port when control bit PSPMODE (TRISE<4>) is set. In slave mode it is asynchronously readable and writable by the external world through $\overline{RD}$ control input (RE0/$\overline{RD}$) and $\overline{WR}$ control input (RE1/$\overline{WR}$).

It can directly interface to an 8-bit microprocessor data bus. The microprocessor can read or write the port D latch as an 8-bit latch. Setting PSPMODE also enables the port pin RE0 to be the $\overline{RD}$ input, RE1 to be the $\overline{WR}$ input and RE2 to be the $\overline{CS}$ (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set).

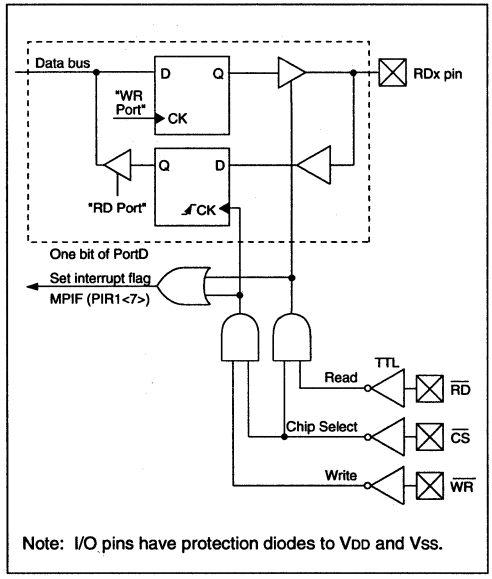
There are actually two 8-bit latches, one for data-out (from the PIC16/17) and one for data input. The user writes 8-bit data to port D data latch and reads data from the port pin latch (note that they have the same address). In this mode the TRISD register is ignored, since the microprocessor is controlling the direction of data flow.

Status flag IBF, Input Buffer Full (TRISE<7>), is set if a received word is waiting to be read by the CPU. Once the PORTD input latch is read by the PIC16C74, IBF is cleared. IBF is a read only status bit. Status flag OBF, Output Buffer Full (TRISE<6>), is set if a word written to PORTD latch is waiting to be read by the external bus. Once the PORTD output latch is read by the microprocessor, OBF is cleared. Status flag IBOV, Input Buffer Overflow (TRISE<5>), is set if a second word is written to the microprocessor port when the previous word has not been read by the CPU. It is a read/write bit and must be cleared by the CPU.

When not in PSPMODE, IBF and OBF bits are held as cleared. However, if the IBOV flag was previously set, it must be cleared in the software.

An interrupt is generated and latched into control bit PSPIF (PIR1<7>) when a read or a write operation is completed. The PSPIF interrupt flag must be cleared by the CPU and the interrupt can be disabled by clearing the interrupt enable bit PSPIE (PIE1<7>).

FIGURE 5-10: PORTD AND PORTE AS A PARALLEL SLAVE PORT



Note: I/O pins have protection diodes to VDD and VSS.

TABLE 5-11: SUMMARY OF PARALLEL SLAVE PORT REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTD	Parallel slave port Read/Write Data	08h	xxxx xxxx
TRISD	PortD data direction register	88h	1111 1111
PORTE	Parallel slave port Read/Write/Chip Select signals	09h	---- -xxx
TRISE	Control bits for Port D peripheral	89h	0000 -111
PIR1	Interrupt register (PSPIF bit)	0Ch	0000 0000
PIE1	Interrupt Enable register (PSPIE bit)	8Ch	0000 0000

6.0 OVERVIEW OF TIMER MODULES

The PIC16C74 has three timer modules. Each module can generate an interrupt to indicate that an event has occurred (i.e. timer overflow). Each of these modules is explained in full detail in the following sections. The timer modules are:

- Timer 0 (TMR0) module(see Section 7)
- Timer 1 (TMR1) module (see Section 8)
- Timer 2 (TMR2) module (see Section 9)

For enhanced time-based functionality, two additional modules can be used with either of the TMR1 or TMR2 modules. There are:

- Capture/Compare/PWM1 (CCP1) module (see Section 10)
- Capture/Compare/PWM2 (CCP2) module (see Section 10)

6.1 Timer0 (TMR0) Overview

The TMR0 module is identical to the RTCC module of other PIC16CXX enhanced core products (and very similar to the PIC16C5X products). The TMR0 module is a simple 8-bit overflow counter. The clock source can be either the internal system clock (OSC/4) or an external clock. When the clock source is an external clock, the TMR0 module can be selected to increment on either the rising or falling edge.

The TMR0 module also has a programmable prescaler option. This prescaler can be assigned to either the TMR0 module or the Watchdog timer. The PSA bit (OPTION<3>) assigns the prescaler, and the PS2 -PS0 (OPTION<2:0>) determines the prescaler value. The TMR0 can increment at the following rates: 1:1 (when prescaler assigned to Watchdog timer), 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, 1:256.

Synchronization of the external clock occurs after the prescaler. When the prescaler is used, the external clock frequency may be higher then the device's frequency. The maximum frequency is 50 MHz, given the high and low time requirements of the clock.

When the clock source is an external clock, the TMR0 module can be selected to increment on either the rising or falling edge.

6.2 Timer1 (TMR1) Overview

Timer1 (TMR1) is a 16-bit timer/counter. The clock source can be either the internal system clock (OSC/4), an external clock, or an external crystal. TMR1 can operate as either a timer or a counter. When operating as a counter (external clock source), the counter can either operate synchronized to the device or asynchonously to the device. Asynchonous operation allows TMR1 to operate during sleep, which is useful for applications that require a real time clock as well as the power savings of sleep mode.

TMR1 also has a prescaler option which allows the TMR1 to increment at the following rates: 1:1, 1:2, 1:4, 1:8. TMR1 can be used in conjunction with the Capture / Compare / PWM (CCP1 or CCP2) module. When used with the CCP1or CCP2 module, TMR1 is the timebase for 16-bit capture or the 16-bit compare. When using the TMR1 module with the CCP1or CCP2 module, TMR1 must be synchronized to the device (timer or synchronized counter mode).

6.3 Timer2 (TMR2) Overview

Timer2 (TMR2) is an 8-bit timer. TMR2 has both a programmable prescaler and postscaler, as well as an 8-bit period register (PR2). TMR2 can be used with the CCP1 module as well as the baud rate generator for the Synchronous Serial Port (SSP). The prescaler option which allows the TMR2 to increment at the following rates: 1:1, 1:4, 1:16.

The postscaler allows TMR2 to match the period register (PR2) a programmable number of times before generating an interrupt. The postscaler can be programmed from 1:1 to 1:16 (inclusive).

6.4 CCP1 and CCP2 Overview

The CCP modules can operate in one of these three modes: 16-bit capture, 16-bit compare, or 10-bit Pulse Width Modulation (PWM)

Capture mode, captures the 16-bit value of TMR1 into the CCPRxH:CCPRxL register pair. The capture event can be programmed for either the falling edge, rising edge, fourth rising edge, or the sixteenth rising edge of the CCPx pin.

Compare mode, compares the TMR1H:TMR1L register pair to the CCPRxH:CCPRxL register pair. When a match occurs an interrupt can be generated, and the output pin CCP1 can be forced to given state (High or Low) TMR1 can be reset (CCP1) or TMR1 reset and start A/D conversion (CCP2). This depends on the control bits CCPxM3 - CCPxM0.

PWM mode, compares TMR2 to a 10-bit duty cycle register as well as to an 8-bit period register (PR2). When the TMR2 = PR2, TMR2 is reset to 00h, an interrupt can be generated, and the CCPx pin (if an output) will be forced high. When the TMR2 = Duty Cycle register, the CCPx pin will be forced low.

7.0 TIMER0 (TMR0) MODULE

The TMR0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable (file address 01h)
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

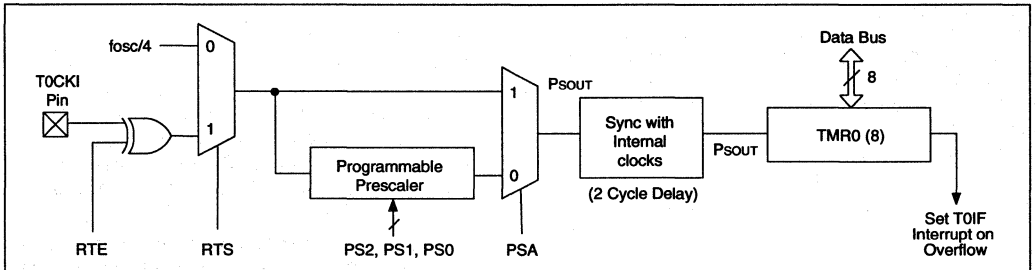
Figure 7-1 is a simplified block diagram of the TMR0 module.

Timer mode is selected by clearing the RTS bit (OPTION<5>). In timer mode, the TMR0 module will increment every instruction cycle (without prescaler). If TMR0 is written, increment is inhibited for the following two cycles (see Figures 7-2 and 7-3). The user can work around this by writing an adjusted value to the TMR0 module.

Counter mode is selected by setting the RTS bit (OPTION<5>). In this mode TMR0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by control bit RTE (OPTION<4>). Clearing the RTE bit selects the rising edge. Restrictions on the external clock input is discussed in detail in Section 7.2.

The prescaler is shared between the TMR0 module and the watchdog timer. The prescaler assignment is controlled in software by control bit, PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to TMR0. The prescaler is not readable or writable. When the prescaler is assigned to the TMR0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 7.3 details the operation of the prescaler.

FIGURE 7-1: TIMER0 (TMR0) BLOCK DIAGRAM



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 AND PSA are located in OPTION register.
2. The prescaler is shared with Watchdog Timer (refer to Figure 7–6 for detailed diagram).

FIGURE 7-2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALE

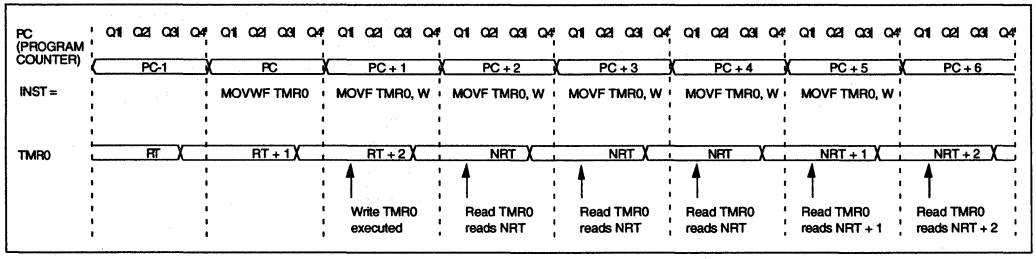
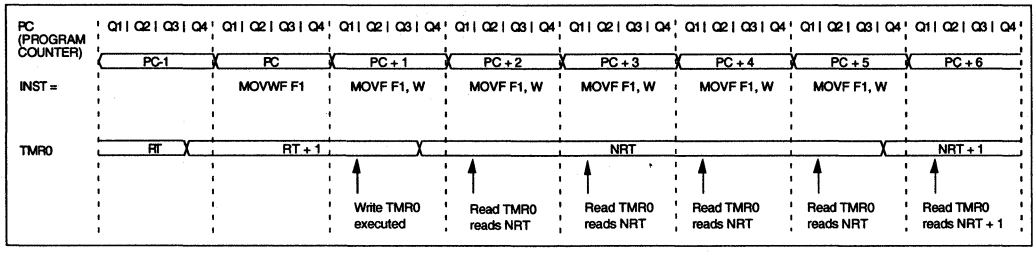


FIGURE 7-3: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/PRESCALE 1:2



7.1 TIMER0 (TMR0) Interrupt

TMR0 interrupt is generated when the TMR0 module timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the TMR0 module interrupt service routine before re-enabling this interrupt. The TMR0 module interrupt can not wake the processor from SLEEP since the timer is shut off during SLEEP. See Figure 7-4 for TMR0 interrupt timing.

7.2 Using TMR0 with External Clock

When external clock input is used for TMR0, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements.

Also there is some delay from the occurance of the external clock edge to the actual incrementing of TMR0. Referring to Figure 7-5, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where:

tosc = oscillator time period.

When no prescaler is used, PSOUT (Prescaler output, see Figure 7-1) is the same as TMR0 clock input and therefore the requirements are:

T_{RTH} = TMR0 high time ≥ 2tosc + ΔT (See parameter #40)

T_{RTL} = TMR0 low time ≥ 2tosc + ΔT (See parameter #41)

When prescaler is used, the TMR0 module input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.

Then:

$$P_{SOUT}\text{ high time} = P_{SOUT}\text{ low time} = \frac{N \cdot T_{RT}}{2}$$

where

T_{RT} = TMR0 input period

N = prescale value (2, 4, ..., 256).

The requirement is, therefore:

$$\frac{N \cdot T_{RT}}{2} \geq 2\,tosc + \Delta T, \text{ or } T_{RT} \geq \frac{4\,tosc + 2\,\Delta T}{N}$$

where

ΔT = small RC delay (see Timing Specifications).

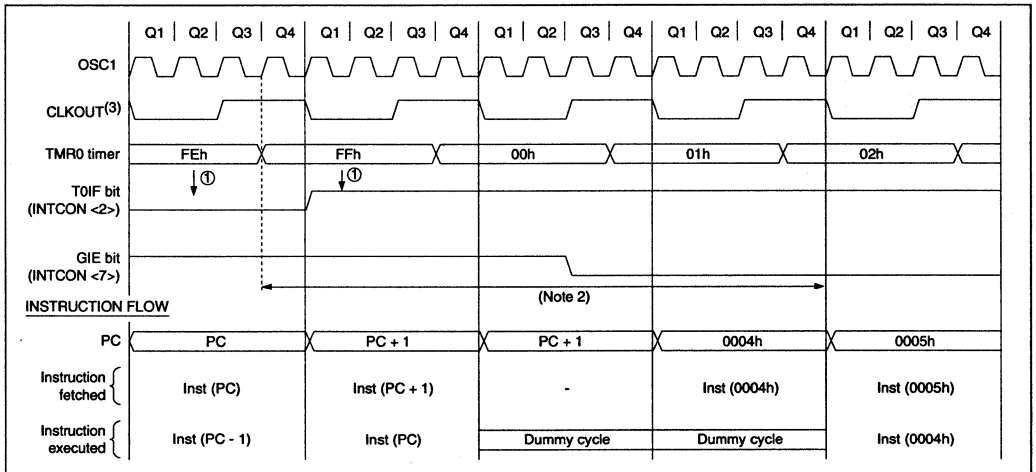
The user will notice that no requirement on TMR0 high time or low time is specified. However, if the high time or low time on TMR0 is too small then the pulse may not be detected, hence a minimum high or low time of 10ns is required. In summary, the TMR0 module input requirements are:

T_{RT} = TMR0 period ≥ (4 tosc + 2 ΔT)/N

T_{RTH} = TMR0 high time ≥ ΔT

T_{RTL} = TMR0 low time ≥ ΔT

FIGURE 7-4: TIMER0 (TMR0) INTERRUPT TIMING



Notes:
1. T0IF interrupt flag is sampled here (every Q1).
2. Interrupt latency = 4 Tcy where Tcy = instruction cycle time.
3. CLKOUT is available only in RC oscillator mode.

Delay from external clock edge: Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 module is actually incremented. Referring to Figure 7-5, the reader can see that this delay is between 3 tosc and 7 tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±200ns @ 20 MHz).

7.3 Prescaler

An 8-bit counter is available as a prescaler for the TMR0 module, or as a post-scaler for the Watchdog Timer, respectively (see Figure 7-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the TMR0 module and the Watchdog Timer. Thus, a prescaler assignment for the TMR0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2-PS0 bits (OPTION<3:0>) determine the prescaler assignment and pre-scale ratio.

When assigned to the TMR0 module, all instructions writing to the TMR0 module (e.g. `CLRF 1`, `MOVWF 1`, `BSF 1,x`....etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK

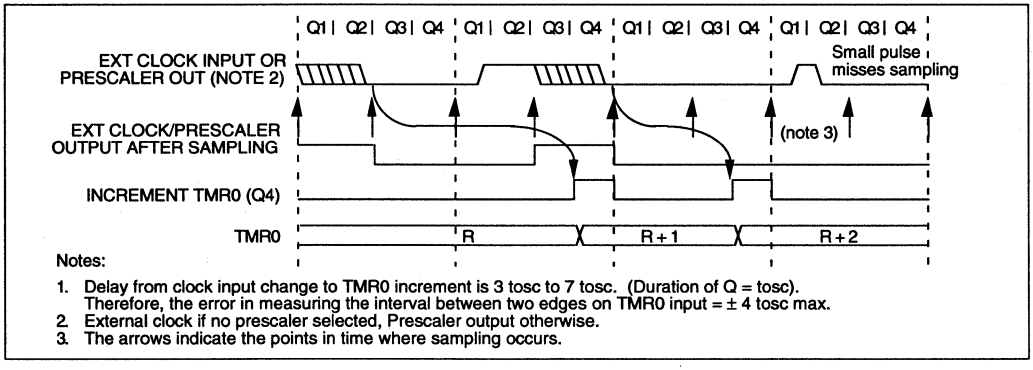
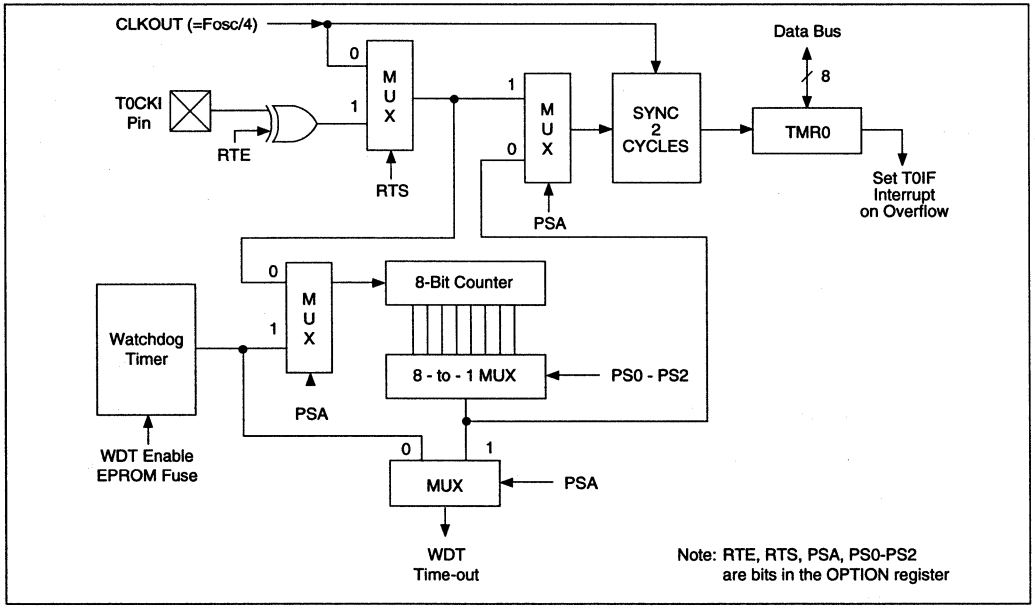


FIGURE 7-6: BLOCK DIAGRAM OF THE TMR0/WDT PRESCALER



7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence (shown in Example 7-1) must be executed when changing the prescaler assignment from TMR0 to WDT. Depending on the selected prescaler value (lines 2 and 3) determines if lines 9 and 10 are required:

EXAMPLE 7-1: CHANGING PRESCALER (TMR0→WDT)

```
1. BCF     STATUS, RP0   ;Bank 0
2. CLRF    TMR0          ;Clear TMR0
3. BSF     STATUS, RP0   ;Bank 1
4. CLRWDT                ;Clears WDT and
                         ;   prescale
5. MOVLW   B'xxxx1xxx'   ;Select new prescale
6. MOVWF   OPTION        ;   value
7. BCF     STATUS, RP0   ;Bank 0
```

Steps 2 and 3 are only required if an external TMR0 source is used. Steps 9 and 10 are necessary only if the desired prescale value is '000' or '001'.

To change prescaler from the WDT to the TMR0 module use the sequence shown in Example 7-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TMR0)

```
1. CLRWDT                ;Clear WDT and
                         ;prescaler
2. BSF STATUS, RP0
3. MOVLW B'xxxx0xxx'     ;Select TMR0, new
                         ;prescale value and
                         ;clock source
4. MOVWF OPTION          ;
5. BCF STATUS, RP0
```

TABLE 7-1: SUMMARY OF TMR0 REGISTERS

Register Name	Function	Address	Power-on Reset Value
TMR0	Timer/counter register	01h	XXXX XXXX
OPTION	Configuration and prescaler assignment bits for TMR0. See Figure 4-4	81h	1111 1111
INTCON	TMR0 overflow interrupt flag and mask bits See Figure 4-5	0Bh	0000 000X

TABLE 7-2: REGISTERS ASSOCIATED WITH TMR0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01	TMR0	TIMER0							
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
81	OPTION	RBPU	INTEDG	RTS	RTE	PSA	PS2	PS1	PS0
85	TRISA	—	—	TRISA 5	TRISA 4	TRISA 3	TRISA 2	TRISA 1	TRISA 0

Legend — = Unimplemented locations, Read as '0'
Shaded boxes are not used by TMR0 module.

8.0 TIMER1 (TMR1) MODULE

Timer1 is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. TMR1 increments from 0000h to FFFFh and rolls over to 0000h. An interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled or disabled using the timer1 interrupt enable bit TMR1IE (PIE1<0>).

TMR1 can operate in one of two modes:

- As a timer
- As a counter

This is determined by the clock select bit, TMR1CS (TICON<1>).

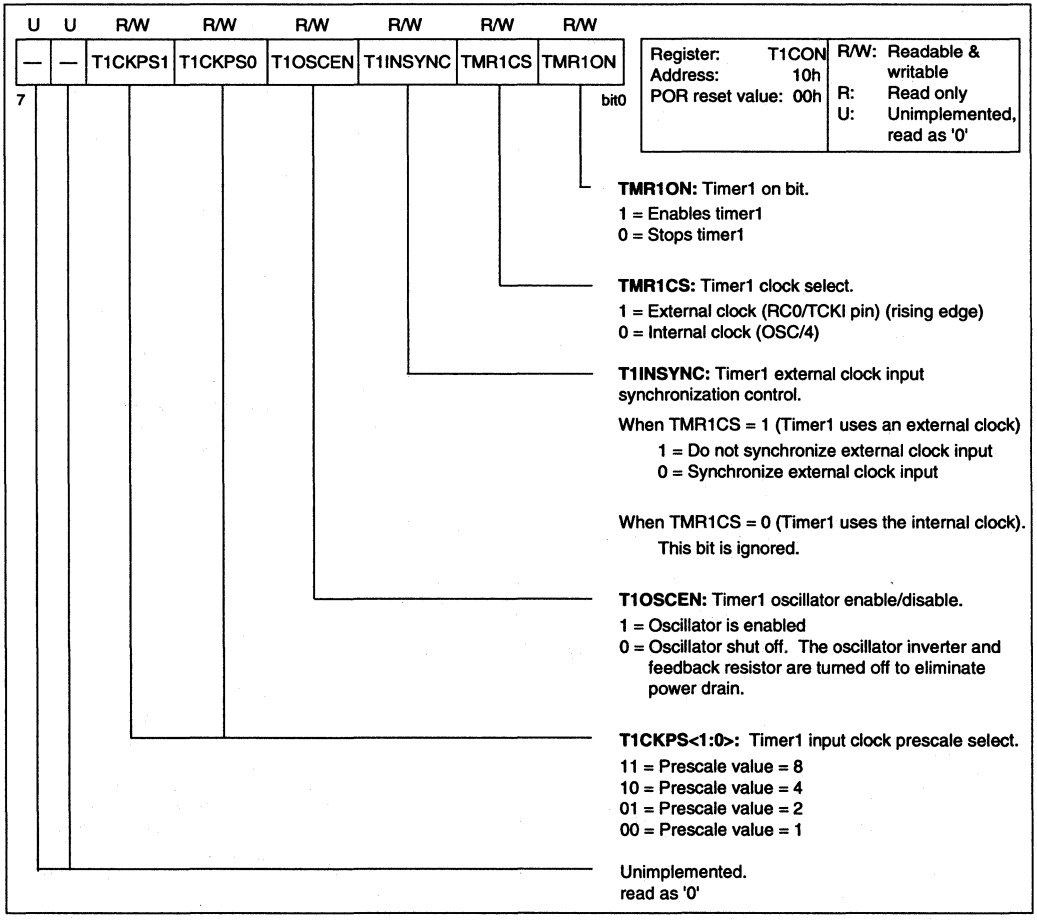
In timer mode, TMR1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input on RC0/T1OSO/T1CKI.

Timer1 can be turned on or off using the control bit TMR1ON (T1CON<0>). See description of T1CON control register for all control bits related to Timer1.

Timer1 also has an internal "reset input". This reset can be generated by CCP1 or CCP2 (Capture/compare/PWM) module. See Section 10 for details. Figure 8-1 shows the Timer1 control register.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI/CCP2 pin becomes an input. That is, the TRISC<1> value is ignored. The RC0/T1OSO/T1CKI pin should normally be configured as an input (for external clock). However, this pin can be configured as an output if self-clocking (through the output pin) is desired.

FIGURE 8-1: T1CON: TIMER1 CONTROL REGISTER



8.1 TMR1 Operation in Timer Mode

Timer mode is selected by clearing the TMR1CS (T1CON<1>) bit. In this mode, the input clock to the timer is OSC/4. The synchronize control bit T1INSYNC (T1CON<2>) has no effect since the internal clock is always in sync.

8.2 TMR1 Operation in Synchronized Counter Mode

Counter mode is selected by setting the TMR1CS bit. In this mode the timer increments on every rising edge of clock input on pin RC1/T1OSI/CCP2 (when T1OSCEN is set) or the RC0/T1OSO/T1CKI.

If T1INSYNC is cleared, then the external clock input is synchronized with internal phase clocks. The synchronization is done after the prescaler stage. The prescaler stage is an asynchronous ripple counter.

In this configuration, during SLEEP mode, TMR1 will not increment even if external clock is present, since the synchronization circuit is shut off. The prescaler however will continue to increment.

8.2.1 EXTERNAL CLOCK INPUT TIMING FOR SYNCHRONIZED COUNTER MODE

In synchronized counter mode, the prescaler output is sampled twice every instruction cycle. Therefore, the following restrictions apply to external clock input:

when prescaler is 1:1:

T_{CKIH} = T1OSI high time $\geq$ 2 tosc + ΔT

T_{CKIL} = T1OSI low time $\geq$ 2 tosc + ΔT

where ΔT = small RC delay (see timing specifications)

when prescaler is higher:

The input clock is divided by two or more, so the prescaler output is symmetrical. The requirements are then:

Prescaler out high time = Prescaler out low time

$$= \frac{N \bullet T_{T1CKIP}}{2} \geq 2 \text{ tosc} + \Delta T$$

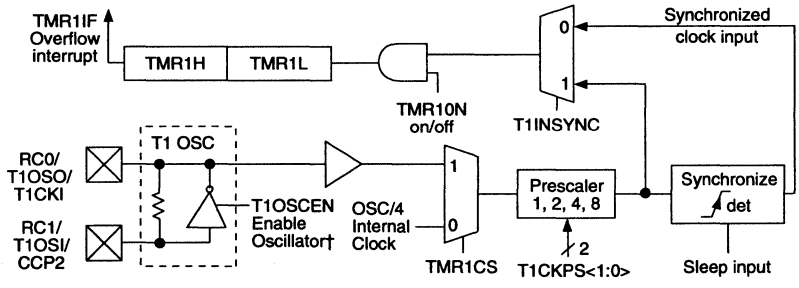
$$\text{or } T_{T1CKIP} \geq \frac{4 \text{ tosc} + \Delta T}{N}$$

where T_{T1CKIP} = T1OSI input clock period
N = prescale value (2, 4, 8)
ΔT = small RC delay (see timing specifications)

Note that no requirement on minimum high time or low time is mentioned. However, if the pulse is too small it may not be recognized. Hence a minimum high and low time is specified.

$T_{T1CKIH} \geq \Delta T$ (see timing specification #45)
$T_{T1CKIL} > \Delta T$ (see timing specification # 46)

FIGURE 8-2: TMR1 BLOCK DIAGRAM



† When the T1 OSCEN bit is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

8.3 TMR1 Operation in Asynchronous Counter Mode

If the control bit T1INSYNC is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and generate an interrupt on overflow which will wake up the processor. However, special precautions in software are needed to read/write the timer (see Section 8.3.2).

In asynchronous counter mode, Timer1 can not be used as timebase for capture or compare operations.

8.3.1 EXTERNAL CLOCK INPUT TIMING WITH UNSYNCHRONIZED CLOCK

If T1INSYNC is set, the timer will increment completely asynchronously. The input clock must meet a certain minimum high time and low time requirements, as specified in timing specifications #45 and #46.

8.3.2 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running off external asynchronous clock will guarantee a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers while the register is incrementing. This may produce an unpredictable value in the timer register.

Writing to the timer is no problem, if the timer clock is slower than the instruction cycle time. Reading the 16-bit value requires some care. Example 8-1 is an example routine to read the 16-bit timer value. This is useful if the timer cannot be stopped.

EXAMPLE 8-1: READING A 16-BIT FREE-RUNNING TIMER

```
;  All Interrupts are disabled
    MOVF    TMR1H, Wreg     ; Read high byte
    MOVWF   TMPH            ;
    MOVF    TMR1L, Wreg     ; Read low byte
    MOVWF   TMPL            ;
    MOVF    TMR1H, Wreg     ; Read high byte
    SUBWF   TMPH, Wreg      ; Sub 1st read
                            ;   with 2nd read
    BTFSC   STATUS,  Z      ;   is result = 0
    GOTO    CONTINUE        ; Good 16-bit read
;
; TMR1L may have rolled over between the read
; of the high and low bytes. Reading the high
; and low bytes now will read a good value.
;
    MOVF    TMR1H, Wreg     ; Read high byte
    MOVWF   TMPH            ;
    MOVF    TMR1L, Wreg     ; Read low byte
    MOVWF   TMPL            ;
; Re-enable Interrupt (if required)
CONTINUE                    ; Continue with your
    :                       ; code
```

8.4 Timer1 Oscillator

A crystal oscillator circuit is built in between T1OSI pin (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200KHz. It will continue to run during SLEEP. It is primarily intended for a 32KHz crystal. Table 8-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must allow software time-out to ensure proper oscillator start-up.

TABLE 8-1: CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz§	15 pF	15 pF
	100 KHz	15 pF	15 pF
	200 KHz	0 - 15 pF	0 - 15 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only.
§For V_{DD} > 4.5V, C1 = C2 ~ 30pf is recommended.

8.5 Resetting Timer1 using a CCP Trigger Output

If CCP1 or CCP2 module is configured in compare mode to generate a "special event" trigger (CCP1M<3:0> = 1011), this signal will reset timer1.

Timer1 must be configured for timer or synchronized counter mode operation to take advantage of this feature. If the Timer1 is running in asynchronous counter mode, this reset operation may not work.

In the event that a write to Timer1 coincides with a reset trigger from CCP1 or CCP2, the write will take precedence.

In this mode of operation, the CCPRxH:CCPRxL registers pair effectively becomes the period register for the timer1.

8.6 Resetting of Timer Registers

TMR1H and TMR1L registers are not reset on POR or any other reset except by the CCP1 special reset trigger.

T1CON register is reset to 00h on Power-on Reset. In any other reset, the register is unaffected.

8.7 Prescaler

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

2

TABLE 8-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
0E	TMR1L	Timer1 Least Significant Byte							
0F	TMR1H	Timer1 Most Significant Byte							
10	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1INSYNC	TMR1CS	TMR1ON

Legend — = Unimplemented locations, Read as '0'
Note: Shaded boxes are not used by Timer1 module.

9.0 TIMER2 (TMR2) MODULE

Timer2 is an 8-bit timer with a prescaler and a postscaler. It is especially suitable as PWM time-base (for PWM mode of CCP modules). TMR2 is a readable and writable register.

The input clock (osc/4) has a prescale option of 1, 4 or 16 (selected by control bits TCKPS1, TCKPS0, register T2CON).

Timer2 has an 8-bit period register PR2. Timer2 increments from 00h until it matches PR2 and then resets t0 00h. PR2 is a readable and writable register.

The overflow (or match) output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling) to generate timer2 interrupt (latched in TMR2IF bit, PIR<1>).

Timer2 can be shut off using TMR2ON (T2CON<2>) control bit to minimize power consumption.

Figure 9-2 shows the Timer2 control register.

9.1 Prescaler and Postscaler

The prescaler and postscaler counters are cleared when any of the following occurs: a write to the TMR2 register, a write to the T2CON register, or any device reset (Power-on Reset, MCLR reset, or Watchdog Timer reset).

9.2 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the synchronous serial port module which optionally uses it to generate shift clock.

FIGURE 9-1: TIMER2 BLOCK DIAGRAM

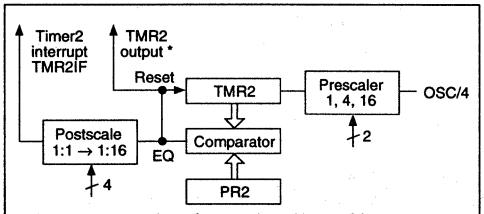


FIGURE 9-2: T2CON: TIMER2 CONTROL REGISTER

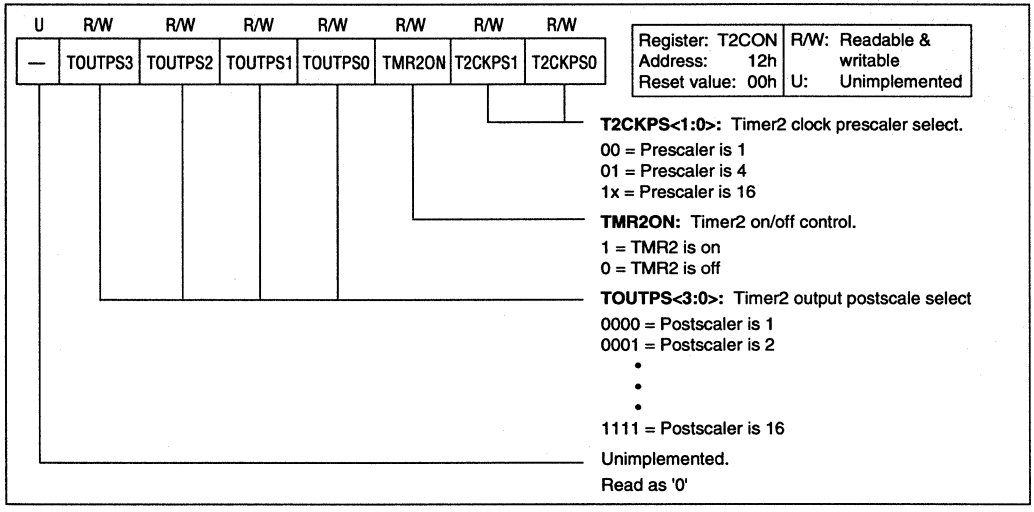


TABLE 9-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
11	TMR2	Timer2							
12	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
92	PR2	Timer2 period Register							

Legend — = Unimplemented locations, Read as '0'
Note: Shaded boxes are not used by Timer2 module.

10.0 CAPTURE/COMPARE/PWM MODULE

The PIC16C74 has two Capture/Compare/PWM (CCP) modules consisting of a 16-bit register which can operate as a 16-bit capture register, as a 16-bit compare register or as a PWM output. (Both the CCP1 and CCP2 modules are identical in operation, with the exception of the special trigger.) In the following sections, the operation of a CCP module is decribed with respect to CCP1. Please note that CCP2 is similar to CCP1, except where noted.

CCP1 module:

Capture/compare/PWM register1 (CCPR1) is made up of two 8-bit sections: low byte, CCPR1L and high byte, CCPR1H. Both are readable and writable.

CCP2 module:

Capture/compare/PWM register1 (CCPR2) is made up of two eight bit sections: low byte, CCPR2L and high byte, CCPR2H. Both are readable and writable.

10.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of TMR1 when an event occurs on pin RC2/CCP1. An event is defined as:

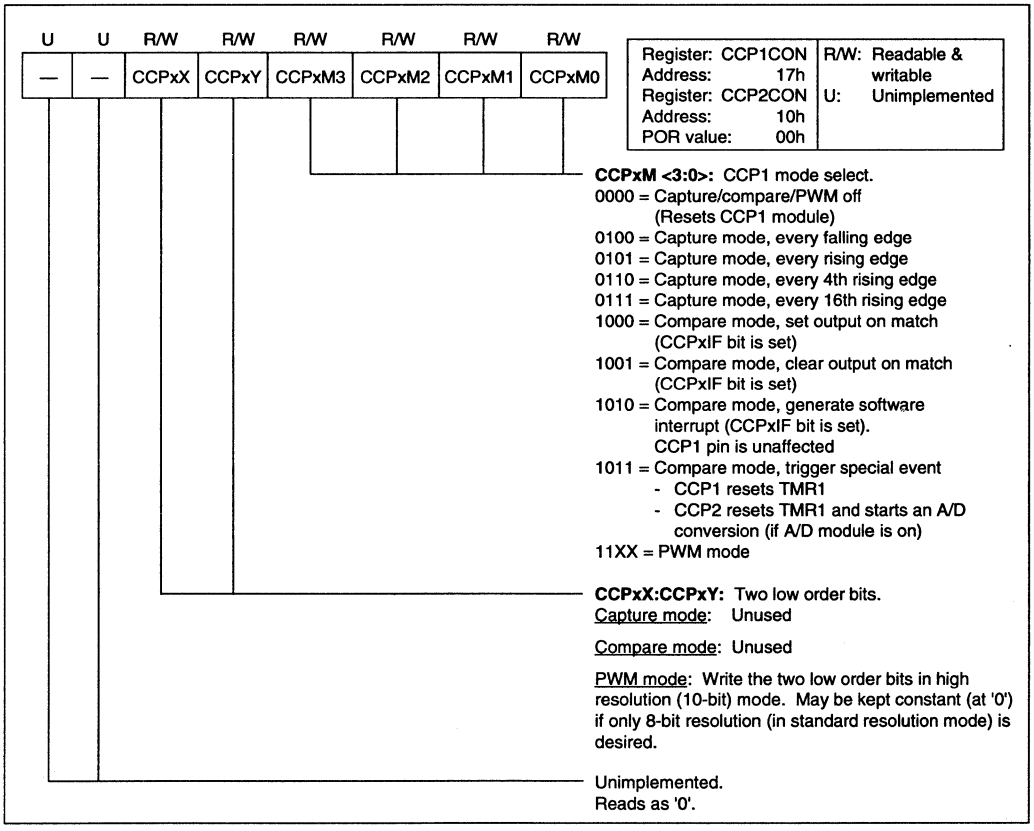
1. A falling edge
2. A rising edge
3. Every 4 rising edges
4. Every 16 rising edges

One of these is selected by the control bits CCP1M <3:0> in register CCP1CON. When a capture is made the interrupt request flag, CCP1IF bit (PIR<2>) is set. It must be reset in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost. In capture mode, the RC2/CCP1 pin should be configured as an input through its corresponding TRIS bit.

Note: If the RC2/CCP1 is configured as an output, a write to the port can cause a capture condition.

When the capture mode is changed, a false capture interrupt may be generated. The user should clear the CCP1IF bit following any such change in operating mode.

FIGURE 10-1: CCP1CON REGISTER



10.1.1 PRESCALER DETAILS

There are four prescaler setting, specified by the CCP1M3-CCP1M0 bits. Whenever the CCP module is turned off, or the CCP module is not in capture mode, the prescaler counter is cleared. This means that any reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, and therefore the first capture may be from a non-zero prescaler. Example 10-1 shows the recommended way to switch between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

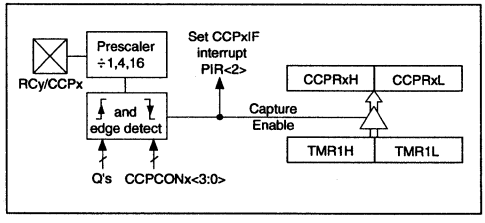
EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF    CCP1CON     ; Turn CCP module off
MOVLW   NEW_CAPT_PS ; Load the W reg with
                    ;   the new prescaler
                    ;  mode value and CCP ON
MOVWF   CCP1CON     ; Load CCP1CON with
                    ;   this value
```

10.1.2 TIMER1 MODE SELECTION

Timer1 must be running in timer mode or synchronized counter mode for the CCP1 modules to use the capture feature. In asynchronous counter mode the capture operation may not work.

FIGURE 10-2: CAPTURE MODE OPERATION



10.2 Compare Mode

In compare mode, the 16-bit CCPR1 register value is constantly compared against the timer1. When a match occurs, the RC2/CCP1 pin is:

- Driven High
- Driven Low
- Remains Unchanged

The action on the pin is based on the control bits CCP1M <3:0> in register CCP1CON. At the same time, a compare interrupt is also generated (bit CCP1IR, register CCP1CON). The user must set the RC2/CCP1 pin as an output through the TRISC<2> bit.

Note: Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the data latch.

10.2.1 TIMER1 MODE SELECTION

Timer1 must be running in timer mode or synchronized counter mode if the CCP1 module is using the compare feature. In asynchronous counter mode, the compare operation may not work.

10.2.2 SOFTWARE INTERRUPT MODE

Another compare mode is software interrupt mode in which the CCP1 pin is not affected. Only CCP1IF interrupt is generated.

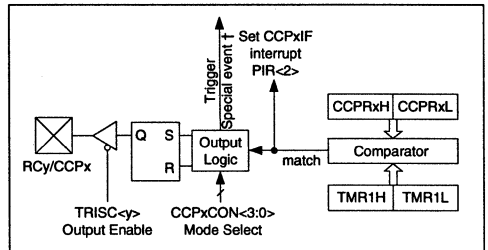
10.2.3 SPECIAL TRIGGER

In this mode, an internal hardware trigger is generated which may be used to initiate an action.

The special trigger output of CCP1 resets the timer1. This allows the CCPR1 register to effectively be a 16-bit programmable period register for timer1.

The special trigger output of CCP2 starts an A/D conversion (if the A/D module is on) and resets Timer1. This allows A/D conversions to be done at a constant (sampling) frequency without software overhead.

FIGURE 10-3: COMPARE MODE OPERATION



† For CCP1 (if enabled), reset Timer1.
For CCP2 (if enabled), resetTimer1 one set GO bit (ADCON0<2>).

10.3 PWM Mode

In Pulse Width Modulation (PWM) mode, the RC2/CCP1 produces up to 10-bit resolution PWM output. This pin must be configured as an output through the TRISC<2> bit. In PWM mode, the user writes the 8-bit duty-cycle value to the low byte of the CCPR1 register, namely CCPR1L. The high-byte, CCPR1H is used as the slave buffer to the low byte. The 8-bit data is transferred from the master to the slave when the PWM1 output is set (i.e. at the beginning of the duty cycle). This double buffering is essential for glitchless PWM output. In PWM mode, CCPR1H is readable but not writable. The period of the PWM is determined by the timer2 period register (PR2).

PWM period is =
[(PR2) + 1] • 4 tosc • (TMR2 prescale value)

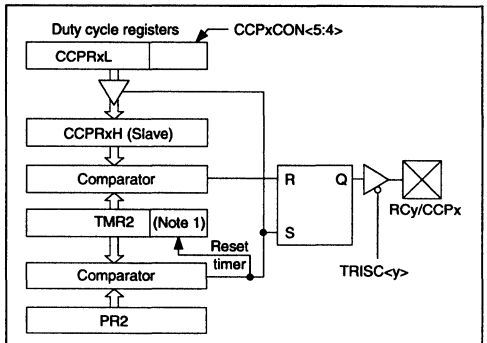
PWM duty cycle =
(DC1) • tosc • (TMR2 prescale value)

where DC1 = 10 bit value from CCPRxL and CCPxCON<5:4> concantenated.

The PWM output resolution is therefore programmable up to a maximum of 10-bit.

Note: Clearing the CCP1CON register will force the RC2/CCP1 PWM output latch to the default low level. This is not the I/O data latch.

FIGURE 10-4: SIMPLIFIED PWM BLOCK DIAGRAM



Note: 8-bit timer is concantenated with 2-bit internal Q clock or 2 bits of the prescaler to create 10-bit time base.

TABLE 10-1: PWM FREQUENCY VS RESOLUTION AT 20 MHZ

Max Resolution (High Resolution Mode)	Frequency		
	TMR2 Prescale = 1	TMR2 Prescale = 4	TMR2 Prescale = 16
10 bit	19.53 KHz	4.88 KHz	1.22 KHz
9 bit	39.06 KHz	9.77 KHz	2.44 KHz
8 bit	78.13 KHz	19.53 KHz	4.88 KHz

TABLE 10-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 KHz	4.88 KHz	19.53 KHz	78.13 KHz	157.5 KHz	210.53 KHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0xFF	0x7F	0x5F
Resoution (High-resolution mode†)	10-bit	10-bit	10-bit	8-bit	7-bit	6.5-bit
Resolution (Standard-resolution mode†)	8-bit	8-bit	8-bit	6-bit	5-bit	4.5-bit

† Standard resolution mode has the CCPIX:CCPIY bit constant (or '0'), and only compares the TMR2 against the PR2. The Q-cycles are not used.

TABLE 10-3: REGISTERS ASSOCIATED WITH TIMER1 AND CAPTURE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
0E	TMR1L	Timer1 Least Significant Byte							
0F	TMR1H	Timer1 Most Significant Byte							
10	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1INSYNC	TMR1CS	TMR1ON
15	CCPR1L	Timer1 Capture Register (LSB)							
16	CCPR1H	Timer1 Capture Register (MSB)							
17	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0
1A	CCPR2L	Timer1 Capture Register (LSB)							
1B	CCPR2H	Timer1 Capture Register (MSB)							
1C	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0

Legend — = Unimplemented locations, Read as '0' Note: Shaded boxes are not used in this mode.

TABLE 10-4: REGISTERS ASSOCIATED WITH TIMER1 AND COMPARE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
0E	TMR1L	Timer1 Least Significant Byte							
0F	TMR1H	Timer1 Most Significant Byte							
10	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1INSYNC	TMR1CS	TMR1ON
15	CCPR1L	Timer1 Compare Register (LSB)							
16	CCPR1H	Timer1 Compare Register (MSB)							
17	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0
1A	CCPR2L	Timer1 Compare Register (LSB)							
1B	CCPR2H	Timer1 Compare Register (MSB)							
1C	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0

Legend — = Unimplemented locations, Read as '0' Note: Shaded boxes are not used in this mode.

TABLE 10-5: REGISTERS ASSOCIATED WITH TIMER2 AND PWM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
11	TMR2	Timer2							
92	PR2	Timer2 period Register							
12	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
15	CCPR1L	Timer2 Duty Cycle Register							
16	CCPR1H	Timer2 Duty Cycle Register (Slave)							
17	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0
1A	CCPR2L	Timer2 Duty Cycle Register							
1B	CCPR2H	Timer2 Duty Cycle Register (Slave)							
1C	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0

Legend — = Unimplemented locations, Read as '0' Note: Shaded boxes are not used in this mode.

11.0 SYNCHRONOUS SERIAL PORT (SSP)

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)

FIGURE 11-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER

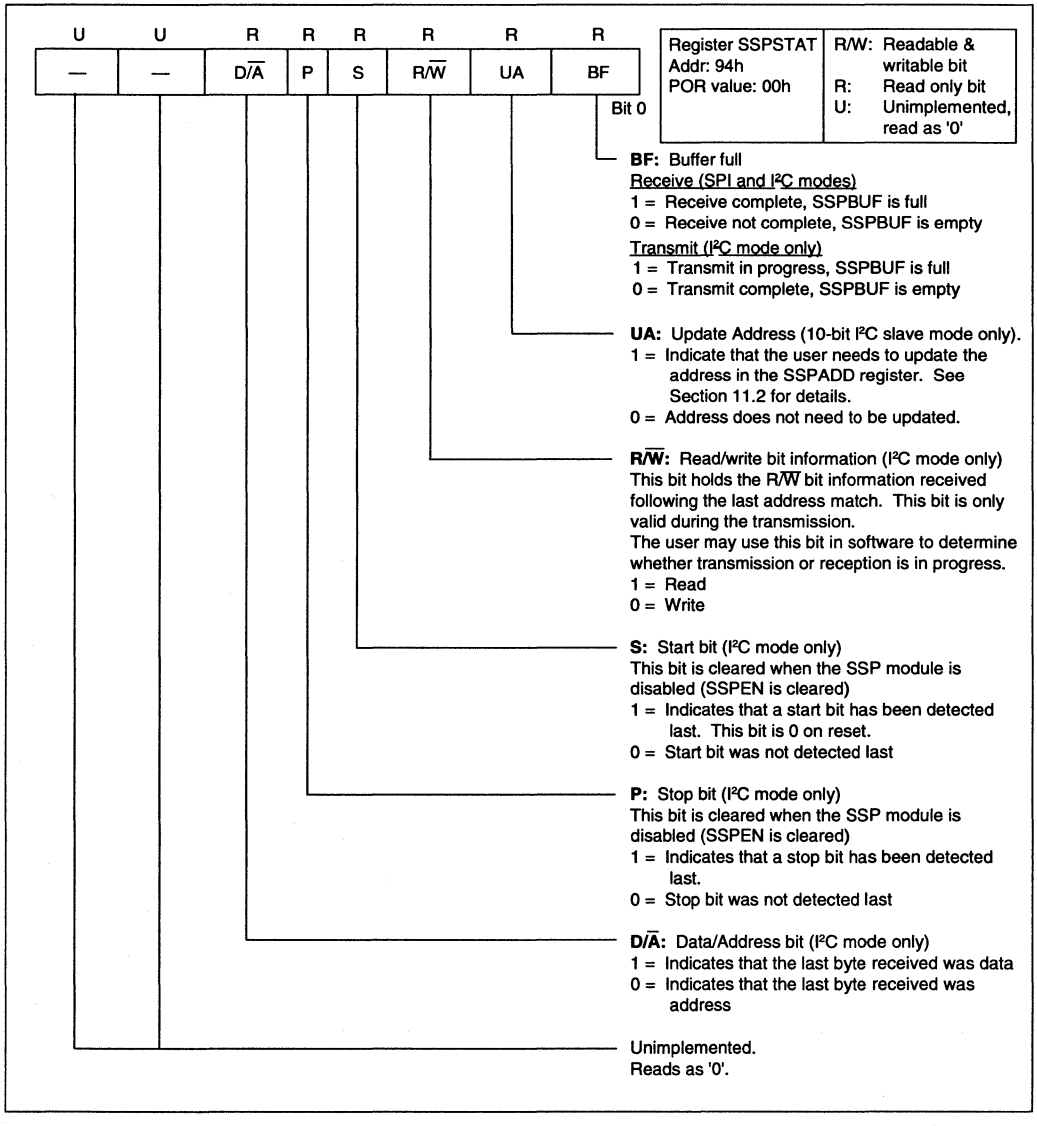
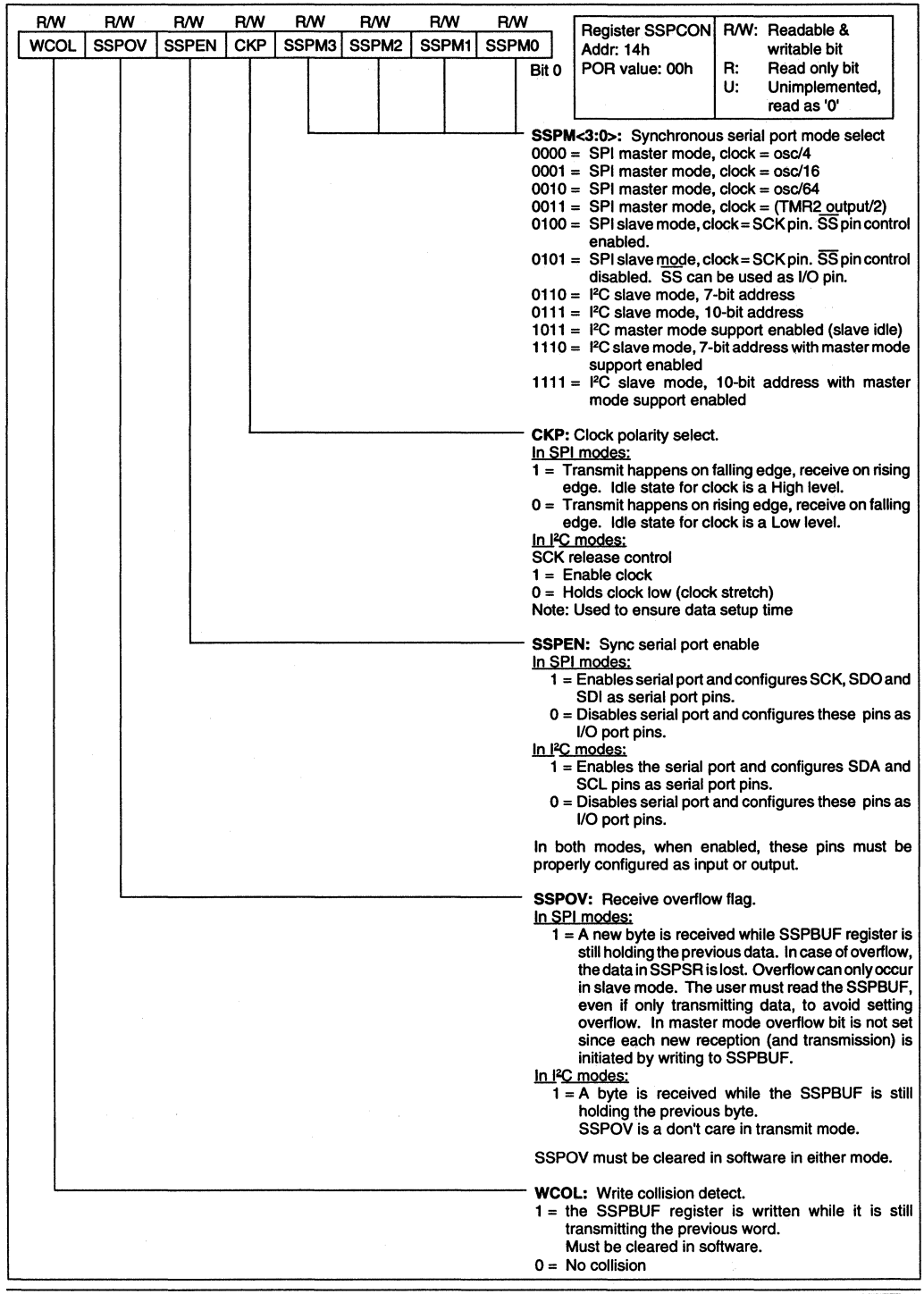


FIGURE 11-2: SSPCON: SYNC SERIAL PORT CONTROL REGISTER



11.1 SPI Mode

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO)
- Serial Data In (SDI)
- Serial Clock (SCK)

Additionally a fourth pin may be used when in a slave mode of operation:

- Slave Select ($\overline{SS}$)

When initializing the SPI, several options need to be specified. This is done by appropriately programming the control bit in the SSPCON register (SSPCON<5:0>). These control bits allow the following to be specified:

- Master Mode (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Output/Input data on the Rising/Falling edge of SCK)
- Clock Rate(Master mode only)
- Slave Select Mode (Slave mode only)

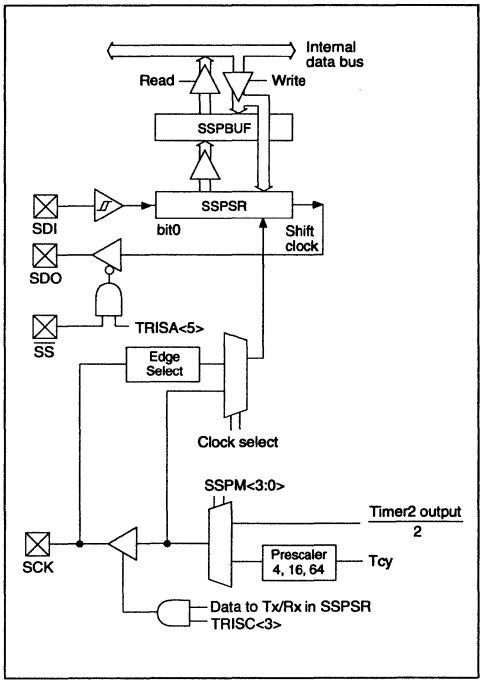
The SSP consists of a transmit/receive Shift Register (SSPSR) and a Buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, while the SSPBUF holds the data that was written to the SSPSR, until the received data is ready. Once the 8-bits of data have been received, that information is moved to the SSPBUF register, the Buffer Full (BF) bit (SSPSTAT <0>) and the SSPIF bit are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect (WCOL) bit (SSPCON<7>) will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF completed successfully. When the application software is expecting to receive valid data, the SPPBUF should be read before the next byte of data to transfer is written to the SSPBUF. The Buffer Full (BF) bit (SSPSTAT<0>) indicates when the SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally the SSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF can then be read (if data is meaningful) and/or the SSPBUF (SSPSR) can be written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 11-1 shows the loading of the SSPBUF (SSPSR) for data transmission. The instructions with the comment fields beginning with ;*** are only required if the received data is meaningful.

EXAMPLE 11-1: LOADING THE SSPBUF (SSPSR) REGISTER

```
LOOP BSF    STATUS, RP0  ;Specify Bank 1
     BTFSS  SSPSTAT, BF  ;Has data been
                         ;received
                         ;(transmit
                         ;  complete)?
     GOTO   LOOP         ;No
     BCF    STATUS, RP0  ;Specify Bank 0
     MOVF   SSPBUF, W    ;W reg = contents
                         ;  of SSPBUF
     MOVWF  RXDATA       ;*** Save in user
                         ;  RAM
     MOVF   TXDATA, W    ;W reg = contents of
                         ;  TXDATA
     MOVWF  SSPBUF       ;New data to xmit.
```

The block diagram of the SSP module, when in SPI mode (Figure 11-3), shows that the SSPSR is not directly readable or writable, and can only be accessed from addressing the SSPBUF register. Additionally, the SSP status register (SSPSTAT) indicates the various status conditions.

FIGURE 11-3: SSP BLOCK DIAGRAM (SPI MODE)



To enable the serial port, the SSP enable bit (SSPEN) must be set. This configures the SDI, SDO, SCK, and $\overline{SS}$ pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- $\overline{SS}$ must have TRISA<5> set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value. An example would be in master mode where you are only sending data (to a display driver), then both SDI and $\overline{SS}$ could be used as general purpose inputs by clearing their corresponding TRIS register bits.

Figure 11-4 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data — Slave sends dummy data
- Master sends data — Slave sends data
- Master sends dummy data — Slave sends data

The master can initiate the data transfer at any time because it controls the SCK. How the master knows when the slave (Processor 2) wishes to broadcast data is determined by the software protocol.

In master mode the data is transmitted/received as soon as the SSPBUF is written to. If the SPI is only going to receive, the SCK output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "line activity monitor" mode.

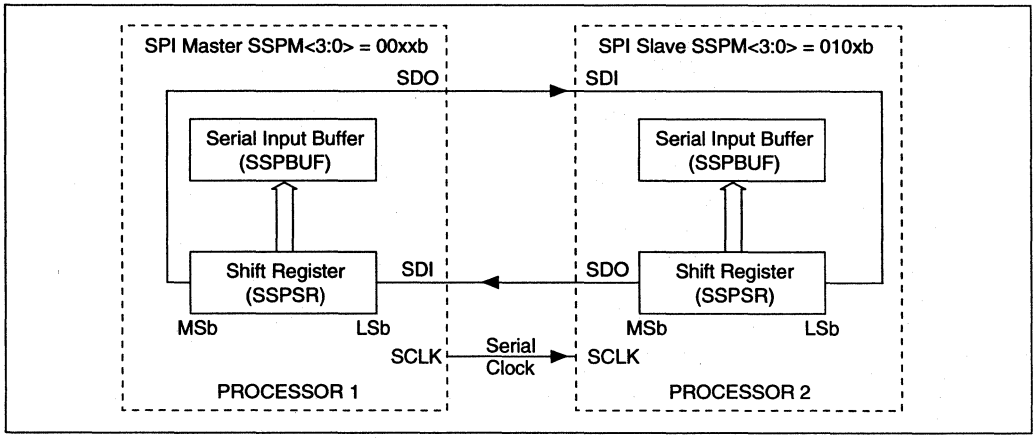
In slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched the interrupt flag (SSPIF) is set (PIR1<3>).

The clock polarity is selected by appropriately programming the CKP bit (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figures 11-5 and 11-6. In master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- OSC / 4 (or Tcy)
- OSC / 16 (or 4 • Tcy)
- OSC / 64 (or 16 • Tcy)
- Timer2 output / 2

This allows a maximum bit clock frequency (at 20 MHz) of 5 MHz. When in slave mode the external clock must meet the minimum high and low times as specified in timing parameters 71 and 72.

FIGURE 11-4: SPI MASTER / SLAVE CONNECTION



The $\overline{SS}$ pin allows a synchronous slave mode. The SPI must be in slave mode (SSPCON<3:0> = 04h) and the TRISA<5> bit must be set the for the synchronous slave mode to be enabled. When the $\overline{SS}$ pin is low, transmission and reception are enabled and the SDO pin is driven. When the $\overline{SS}$ pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. External pull-up / pull-down resisters may be desirable, depending on the application.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 11-5: SPI MODE TIMING (MASTER MODE OR SLAVE MODE W/O $\overline{SS}$ CONTROL)

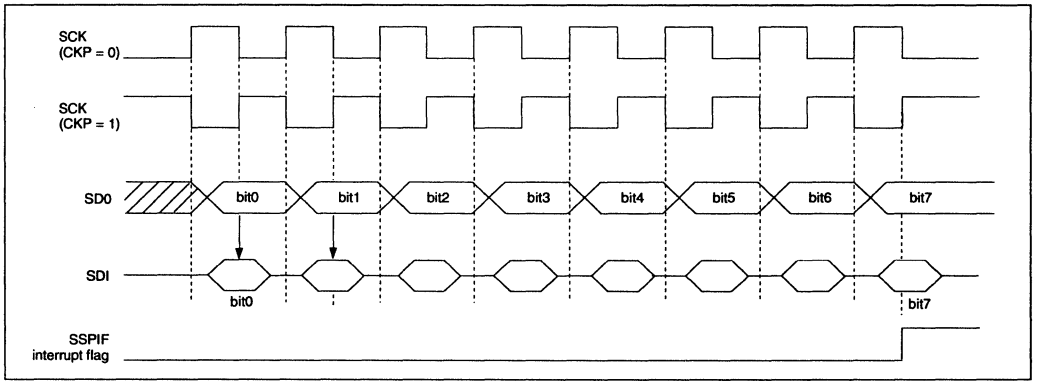


FIGURE 11-6: SPI MODE TIMING (SLAVE MODE WITH $\overline{SS}$ CONTROL)

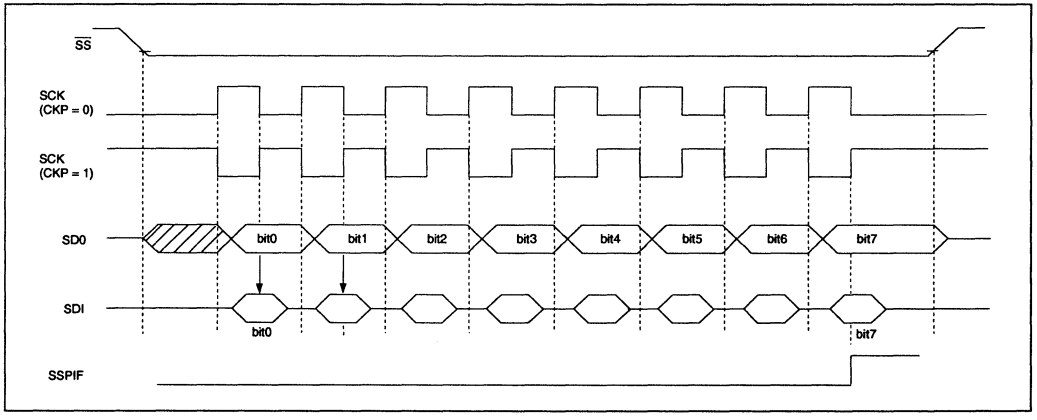


TABLE 11-1: REGISTERS ASSOCIATED WITH SPI OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
13	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register							
14	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
94	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF

Legend — = Unimplemented locations, Read as '0' Note: Shaded boxes are not used by SSP module in SPI mode.

11.2 I²C™ Overview

This section gives an overview of the Inter-IC (I²C) bus, with Section 11.3 discussing the operation of the SSP module in I²C mode. The Inter-IC (I²C) bus is a two-wire serial interface developed by Phillips/Signetics™. The original specification, or standard mode, was for data transfers of up to 100-Kbps. An enhanced specification, or fast mode, supports data transmission up to 400 Kbps. Both standard mode and fast mode devices will inter-operate if attached to the same bus.

The I²C interface employs a comprehensive protocol to ensure reliable transmission and reception of data. When transmitting data, one device is the "master" (generates the clock), while the other device(s) acts as the "slave". All Portions of the slave protocol are implemented in the SSP module's hardware, while portions of the master protocol will need to be addressed in the PIC16CXX software. Table 11-2 defines some of the I²C-bus terminology. For additional information on the I²C interface specification, please refer to the Philips/ Signetics™ document " The I²C-bus and how to use it". The order number for this document is 98-8080-575.

In the I²C interface protocol each device has an address. When a master wishes to initiate a data transfer, it first transmits the address of the device that it wishes to "talk" to. All devices "listen" to see if this is their address. Within this address, a bit specifies if the master wishes to read / write from / to the slave device. The master and slave are always in opposite modes (transmitter/receiver) of operation during a data transfer. That is they can be thought of operating in either of these two relations:

- Master-transmitter and Slave-receiver
- Slave-transmitter and Master-receiver

In both cases the master generates the clock signal.

The output stages of the clock (SCL) and data (SDA) lines must have an open-drain or open-collector in order to perform the wired-AND function of the bus. External pull-up resistors are used to ensure a high level, when no device is pulling the line down.. The number of devices that may be attached to the I²C bus is limited only by the maximum bus loading specification of 400 pF.

11.2.1 INITIATING AND TERMINATING DATA TRANSFER

During times of no data transfer (idle time), both the clock line (SCL) and the data line (SDA) are pulled high through the external pull-up resistors. The START and STOP conditions determine the start and stop of data transmission. The START condition is defined as a high to low transition of the SDA when the SCL is high. The STOP condition is defined as a low to high transition of the SDA when the SCL is high. Figure 11-7 shows the START and STOP conditions. The master generates these conditions for starting and terminating data transfer. Due to the definition of the START and STOP conditions, when data is being transmitted the SDA line can only change state when the SCL line is low.

FIGURE 11-7: START AND STOP CONDITIONS

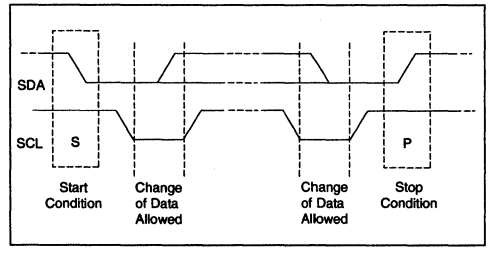


TABLE 11-2: I²C-BUS TERMINOLOGY

Term	Description
Transmitter	The device that sends the data to the bus
Receiver	The device that receives the data from the bus
Master	The device which initiates the transfer, generates the clock, and terminates the transfer
Slave	The device addressed by a master
Multi-master	More than one master device in a system. These masters can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure that ensures that only one of the master devices will control the bus. This ensures that the transfer data does not get corrupted.
Synchronization	Procedure where the clock signals of two or more devices are synchronized.

11.2.2 ADDRESSING I²C DEVICES

There are two address formats. The simplest is the 7-bit address format with a R/$\overline{W}$ bit (see Figure 11-8). The more complex is the 10-bit address with a R/$\overline{W}$ bit (see Figure 11-9). For 10-bit address format, two bytes must be transmitted with the first five bits specifying this to be a 10-bit address.

FIGURE 11-8: 7-BIT ADDRESS FORMAT

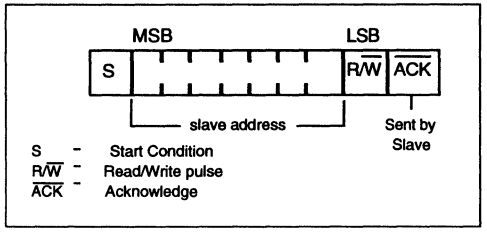
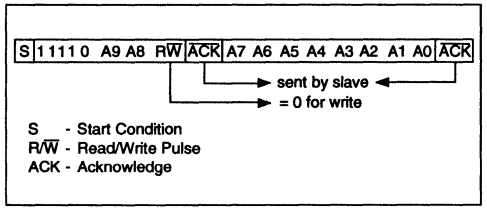


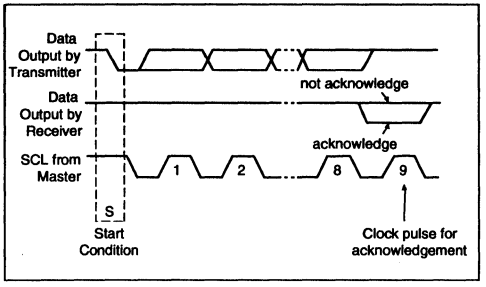
FIGURE 11-9: I²C 10-BIT ADDRESS FORMAT



1.2.3 TRANSFER ACKNOWLEDGE

All data must be transmitted per byte, with no limit to the number of bytes transmitted per data transfer. After each byte, the slave-receiver generates an acknowledge bit (ACK). This is shown in Figure 11-10. When a slave-receiver doesn't acknowledge the slave address or received data, the master must abort the transfer. The slave must leave SDA high so that the master can generate the STOP condition (see Figure 11-7).

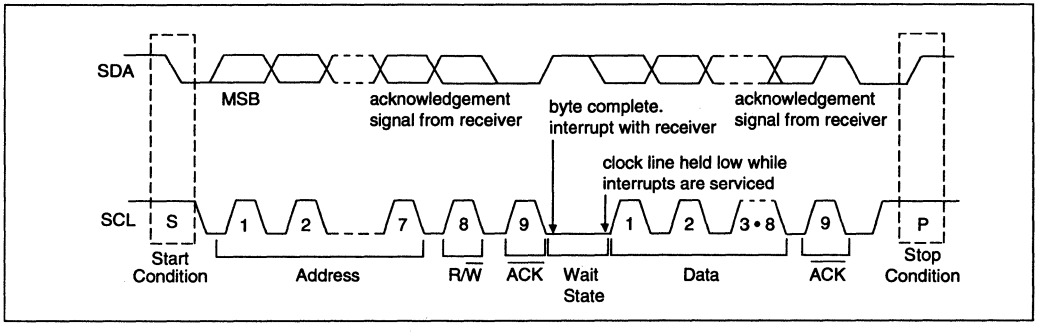
FIGURE 11-10: SLAVE-RECEIVER ACKNOWLEDGE



If the master is receiving the data (master-receiver), it generates an acknowledge signal for each received byte of data, except for the last byte. To signal the end of data to the slave-transmitter, the master does not generate an acknowledge (not acknowledge). The slave then releases the SDA line so the master can generate the STOP condition. The master can also generate the STOP condition during the acknowledge pulse for valid termination of data transfer.

If the slave needs to delay the transmission of the next byte, holding the SCL line low will force the master into a wait state. Data transfer continues when the slave releases the SCL line. This allows the slave to move the received data or fetch the data it needs to transfer before allowing the clock to start. This wait state technique can also be implemented at the bit level. Figure 11-11 shows a data transfer waveform.

FIGURE 11-11: A DATA TRANSFER



Figures 11-12 and 11-13 show Master-transmitter and Master-receiver data transfer sequences.

When a master does not wish to relinquish the bus (by generating a STOP condition), a repeated START condition (Sr) must be generated. This condition is identical to the start condition (SDA goes high-to-low while SCL is high), but occurs after a data transfer acknowledge pulse (not the bus-free state). This allows a master to send "commands" to the slave and then receive the requested information or to address a different slave device. This sequence is shown in Figure 11-14.

FIGURE 11-12: MASTER-TRANSMITTER SEQUENCE

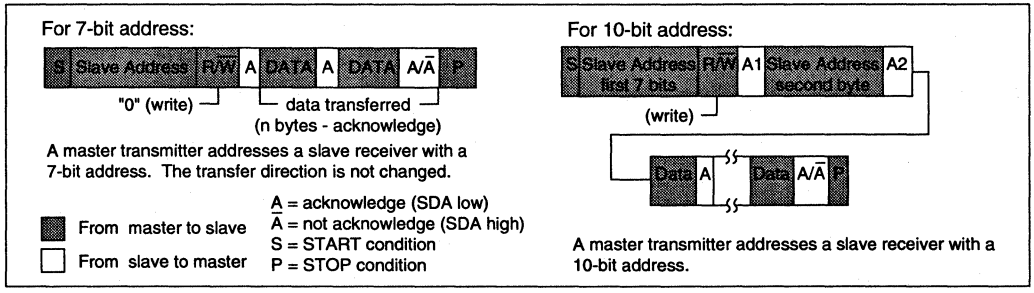


FIGURE 11-13: MASTER-RECEIVER SEQUENCE

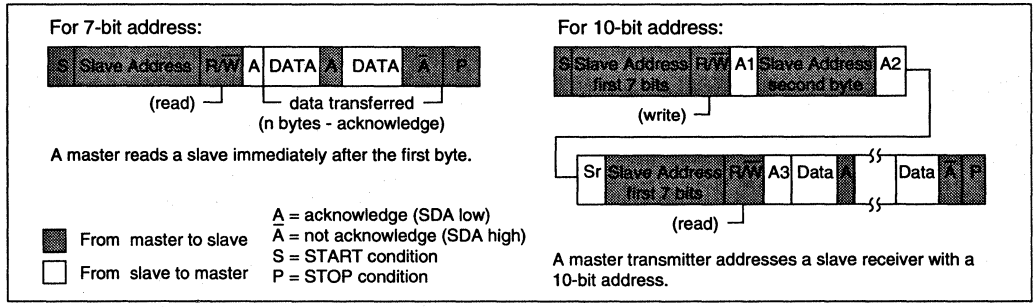
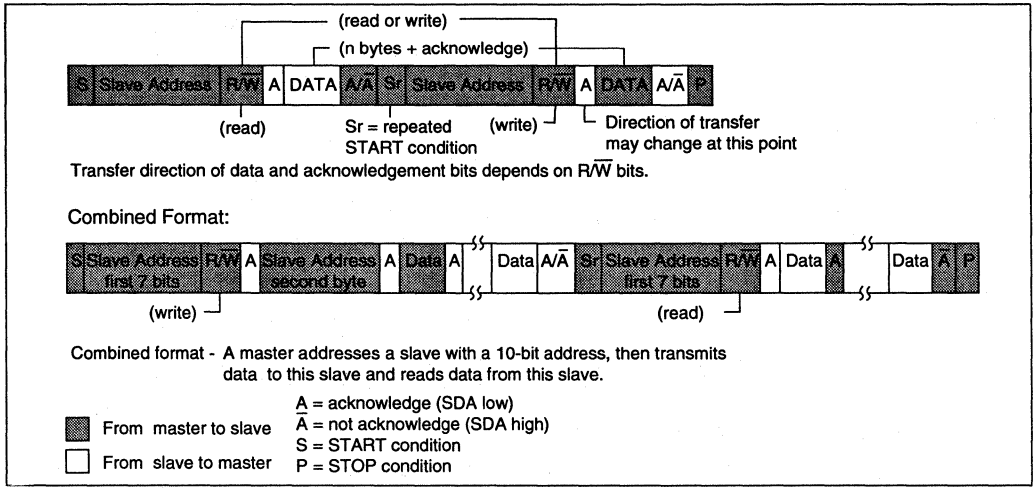


FIGURE 11-14: COMBINED FORMAT



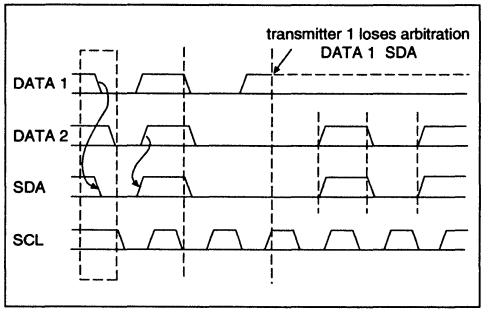
1.2.4 Multi-master

The I²C protocol allows a system to have more than one master. This is called multi-master. When two or more masters try to transfer data at the same time, arbitration and synchronization occur.

11.2.4.1 ARBITRATION

Arbitration takes place on the SDA line, while the SCL line is high. The master which transmits a high when the other master transmits a low loses arbitration (see Figure 11-15), and turns off its data output stage. A master which lost arbitration can generate clock pulses until the end of the data byte where it lost arbitration. When the master devices are addressing the same device, arbitration continues into the data.

FIGURE 11-15: MULTI-MASTER ARBITRATION (2 MASTERS)



Masters that also incorporate the slave function, and have lost arbitration must immediately switch over to slave-receiver mode. This is because the winning master-transmitter may be addressing it.

Arbitration is not allowed between:

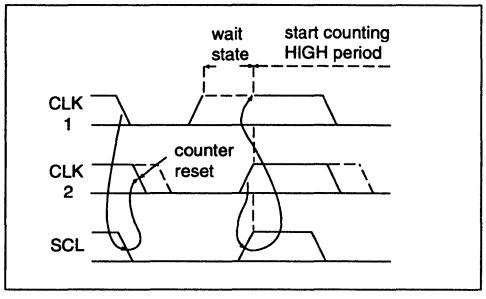
- A repeated START condition
- A STOP condition and a data bit
- A repeated START condition and a STOP condition

Care needs to be taken to ensure that these conditions do not occur.

11.2.4.2 CLOCK SYNCHRONIZATION

Clock synchronization occurs after the devices have started arbitration. This is performed using a wired-AND connection to the SCL line. A high to low transition on the SCL line causes the concerned devices to start counting off their low period. Once a device clock has gone low, it will hold the SCL line low until its SCL high state is reached. The low to high transition of this clock may not change the state of the SCL line, if another device clock is still within its low period. The SCL line is held low by the device with the longest low period. Devices with shorter low periods enter a high wait-state, until the SCL line comes high. When the SCL line comes high, all devices start counting off their high periods. The first device to complete its high period will pull the SCL line low. The SCL line high time is determined by the device with the shortest high period. This is shown in Figure 11-16.

FIGURE 11-16: CLOCK SYNCHRONIZATION



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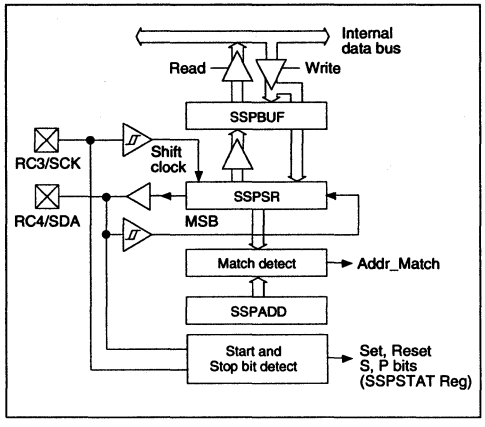
11.3 SSP I²C Operation

The SSP module in I²C mode fully implements all slave functions, and provides support in hardware to facilitate software implementations of the master functions. The SSP module implements the standard and fast mode specifications as well as 7-bit and 10-bit addressing. Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits. A block diagram of the SSP module in I²C mode is shown in Figure 11-17. The SSP module functions are enabled by setting the SSP Enable (SSPEN) bit (SSPCON<5>).

FIGURE 11-17: SSP BLOCK DIAGRAM (I²C MODE)



The SSP module has five registers for I²C operation. These are the:

- SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive / Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) - Not directly accessible
- Address Register (SSPADD)

The SSPCON register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allows one of the following I²C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with master-mode support
- I²C Slave mode (10-bit address), with master-mode support
- I²C Master mode, slave is idle

Selection of any I²C mode and with the SSPEN bit set, forces the SCL and SDA pins to be open collector, provided these pins are set to inputs through the TRISC bits.

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START or STOP bit, specifies if the received byte was data or address, if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer. The SSPSTAT register is read only.

The SSPBUF is the register to which transfer data is written to or read from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF and the SSPIF is set. If another complete byte is received before the SSPBUF is read, a receiver overflow has occurred and the SSPOV bit (SSPCON<6> is set.

The SSPADD register holds the slave address. In 10-bit mode, the user needs to write the high byte of the address (1 1 1 1 0 A9 A8 0). Following the high byte address match, the low byte of the address needs to be loaded (A7 - A0).

11.3.1 Slave Mode

In slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer from an address match is received, the hardware automatically will generate the acknowledge ($\overline{ACK}$) pulse, and then load the SSPBUF with the received value in the SSPSR.

There are certain conditions that will cause the SSP module not to give this $\overline{ACK}$ pulse. These are if either (or both):

- The Buffer Full (BF) bit was set before the transfer was received.
- The Overflow (SSPOV) bit was set before the transfer was received.

In this case, the SSPSR value is not loaded into the SSPBUF, but the SSPIF bit is set. Table 11-3 shows what happens when a data transfer byte is received, given the status of the BF and SSPOV bits. The shaded boxes shows the condition where user software did not properly clear the overflow condition. The BF flag is cleared by reading the SSPBUF register while the SSPOV bit is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the I^2C specification as well as the requirement of the SSP module is shown in timing specifications #90 and 91.

11.3.1.1 ADDRESSING

Once the SSP module has been enabled, The SSP waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR. All incoming bits are sampled with the rising edge of the clock (SCL) line. The SSPSR<7:1> is compared to the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following things happen:

- SSPSR loaded into SSPBUF
- Buffer Full (BF) bit is set
- $\overline{ACK}$ pulse is generated
- SSP Interrupt Flag (SSPIF) is set (interrupt is generated if enabled) - on falling edge of ninth SCL pulse

In 10-bit address mode, two address bytes need to be received by the slave (see Figure 11-9). The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. The R/$\overline{W}$ bit (bit 0) must specify a write, so the slave device will receive the second address byte. For a 10-bit address the first byte would equal '1 1 1 1 0 A9 A8 0', where A9 and A8 are the two MSbs of the address. The sequence of events for 10-bit address are as follows, with steps 7- 9 for slave-transmitter:

1. Receive first (high) byte of Address (SSPIF, BF and UA are set)
2. Update SSPADD with second (low) byte of Address (clears UA and releases SCL line)
3. Read SSPBUF (clears BF) and clear SSPIF
4. Receive second (low) byte of Address (SSPIF, BF and UA are set)
5. Update SSPADD with first (high) byte of Address (clears UA, if match releases SCL line)
6. Read SSPBUF (clears BF) and clear SSPIF
7. Receive Repeated START condition
8. Receive first (high) byte of Address (SSPIF and BF are set)
9. Read SSPBUF (clears BF) and clear SSPIF

TABLE 11-3: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received				
BF	SSPOV	SSPSR→SPBUF	Generate $\overline{ACK}$ Pulse	Set SSPIF bit (SSP Interrupt if Enabled)
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

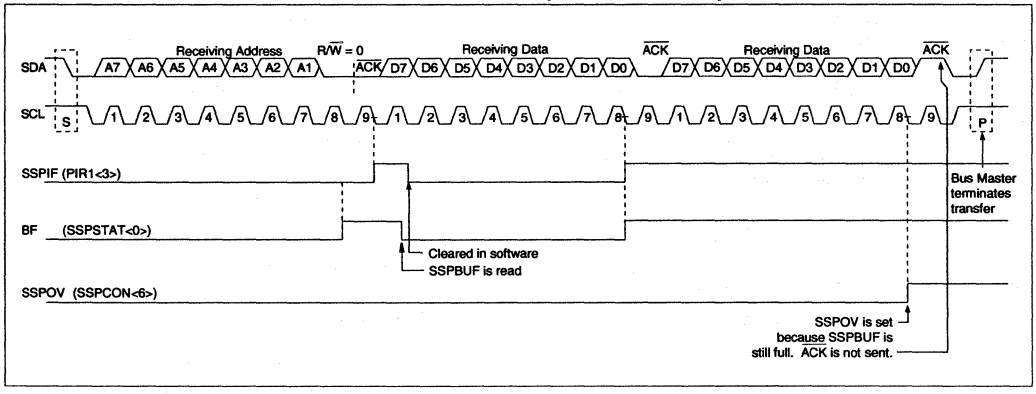
11.3.1.2 RECEPTION

When the R/$\overline{W}$ bit of the address byte is clear and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF.

When the address byte overflow condition exists then no acknowledge ($\overline{ACK}$) pulse is given. An overflow condition is defined as either the BF bit (SSPSTAT<0>) is set or the SSPOV bit (SSPCON<6>) is set.

A SSPIF interrupt is generated for each data transfer byte. The SSPIF bit must be cleared in software, and the SSPSTAT register is used to determine the status of the byte.

FIGURE 11-18: I²C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



11.3.1.3 TRANSMISSION

When the R/$\overline{W}$ bit of the address byte is set and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF. The $\overline{ACK}$ pulse will be sent on the ninth bit, and the SCL pin is held low. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then the SCL pin should be enabled by setting the CKP bit (SSPCON<4>). The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (see Figure 11-19).

A SSPIF interrupt is generated for each data transfer byte. The SSPIF bit must be cleared in software, and the SSPSTAT register is used to determine the status of the byte. The SSPIF bit is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the $\overline{ACK}$ pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not $\overline{ACK}$), then the data transfer is complete. The slave then monitors for another occurrence of the START bit. If the SDA line was low ($\overline{ACK}$), the transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then the SCL pin should be enabled by setting the CKP bit (SSPCON<4>).

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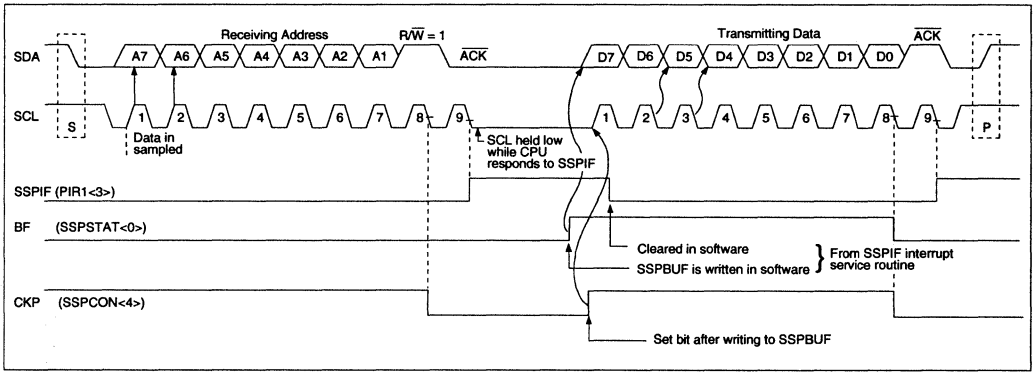
FIGURE 11-19: I²C WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



11.3.2 Master Mode

Master mode of operation is supported by interrupt generation on the detection of the START and STOP conditions. The STOP (P)and START (S) bits are cleared from a reset or when the SSP module is disabled. Control of the I²C bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are cleared

In master mode the SCL and SDA lines are manipulated by changing the corresponding TRISC<4:3> bit(s) to an output (cleared). The output level is always low, irrespective of the value(s) in PORTB<4:3>. So when transmitting data, a "1" data bit must have the TRISC<4> bit set (input) and a "0" data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit.

The following events will cause the SSP Interrupt Flag (SSPIF) to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- Data transfer byte transmitted/received

Master mode of operation can be done with either the slave mode idle (SSPM3 - SSPM0 = 1011) or with the slave active. When both master and slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

11.3.3 Multi-master Mode

In multi-master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P)and START (S) bits are cleared from a reset or when the SSP module is disabled. Control of the I²C bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are cleared. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the stop condition occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, the device may be being addressed. If addressed an $\overline{ACK}$ pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

TABLE 11-4: REGISTERS ASSOCIATED WITH I²C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
0C	PIR1	PSPIF	—	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	—	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
13	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register							
93	SSPADD	Synchronous Serial Port (I²C mode) Address Register							
14	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
94	SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF

Legend — = Unimplemented locations, Read as '0'
Note: Shaded boxes are not used by the SSP module in I²C mode.

FIGURE 11-20: OPERATION OF THE I²C MODULE IN IDLE_MODE, RCV_MODE OR XMIT_MODE

```
IDLE_MODE (7-bit):
if (Addr_match)              {   Set interrupt;
                                 if (R/W = 1)  {Send ACK = 0;
                                                set XMIT_MODE;
                                                }
                                 else if (R/W = 0) set RCV_MODE;
                             }
```

```
RCV_MODE:
if ((SSPBUF=Full) OR (SSPOV = 1))
      {Set SSPOV;
      Do not acknowledge;
      }
else  { transfer SSPSR → SSPBUF;
      send ACK = 0;
      }
Receive 8-bits in SSPSR;
Set interrupt;
```

```
XMIT_MODE:
While ((SSPBUF = Empty) AND (CKP=0)) Hold SCL Low;
Send byte;
Set interrupt;
if (ACK Received = 1)        {End of transmission;
                              Go back to IDLE_MODE;
                              }
else if (ACK Received = 0)   Go back to XMIT_MODE;
```

```
IDLE_MODE (10-Bit):
If (High_byte_addr_match AND (R/W = 0))
    { PRIOR_ADDR_MATCH = FALSE;
      Set interrupt;
      if ((SSPBUF = Full) OR ((SSPOV = 1))
            { Set SSPOV;
              Do not acknowledge;
            }
      else  { Set UA = 1;
              Send ACK = 0;
              While (SSPADD not updated) Hold SCL low;
              Clear UA = 0;
              Receive Low_addr_byte;
              Set interrupt;
              Set UA = 1;
              If (Low_byte_addr_match)
                    { PRIOR_ADDR_MATCH = TRUE;
                      Send ACK = 0;
                      while (SSPADD not updated) Hold SCL low;
                      Clear UA = 0;
                      Set RCV_MODE;
                    }
            }
    }
else if (High_byte_addr_match AND (R/W = 1)
            { if (PRIOR_ADDR_MATCH)
                    { send ACK = 0;
                      set XMIT_MODE;
                    }
              else PRIOR_ADDR_MATCH = FALSE;
            }
```

12.0 SERIAL COMMUNICATION INTERFACE (SCI) MODULE

The Serial Communication Interface (SCI) module is one of the two serial I/O modules. The SCI can be configured as a full duplex asynchronous system that can communicate with peripheral devices such as CRT terminals and personal computers, or it can be configured as a half duplex synchronous system that can communicate with peripheral devices such as A/D or D/A integrated circuits, Serial EEPROMs etc. The SCI can be configured in the following modes:

- Asynchronous (full duplex)
- Synchronous - Master (half duplex)
- Synchronous - Slave (half duplex)

The SPEN (RCSTA<7>) bit has to be set in order to configure RC6 and RC7 as the Serial Communication Interface.

FIGURE 12-1: TXSTA: TRANSMIT STATUS AND CONTOL REGISTER

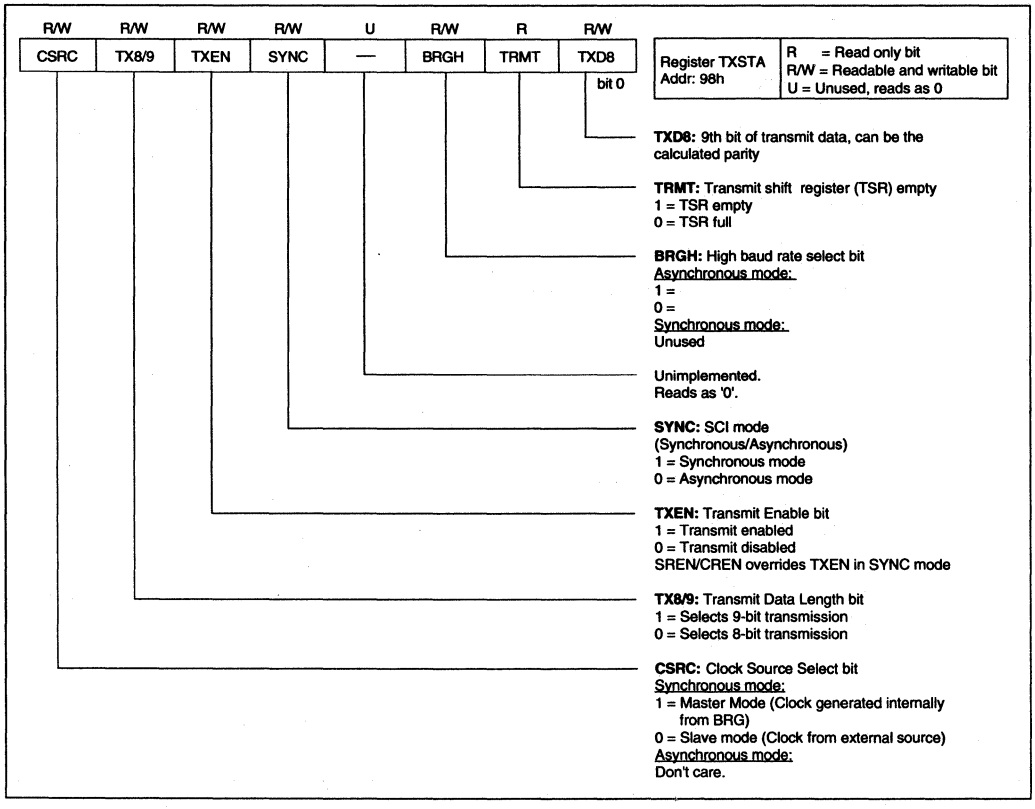
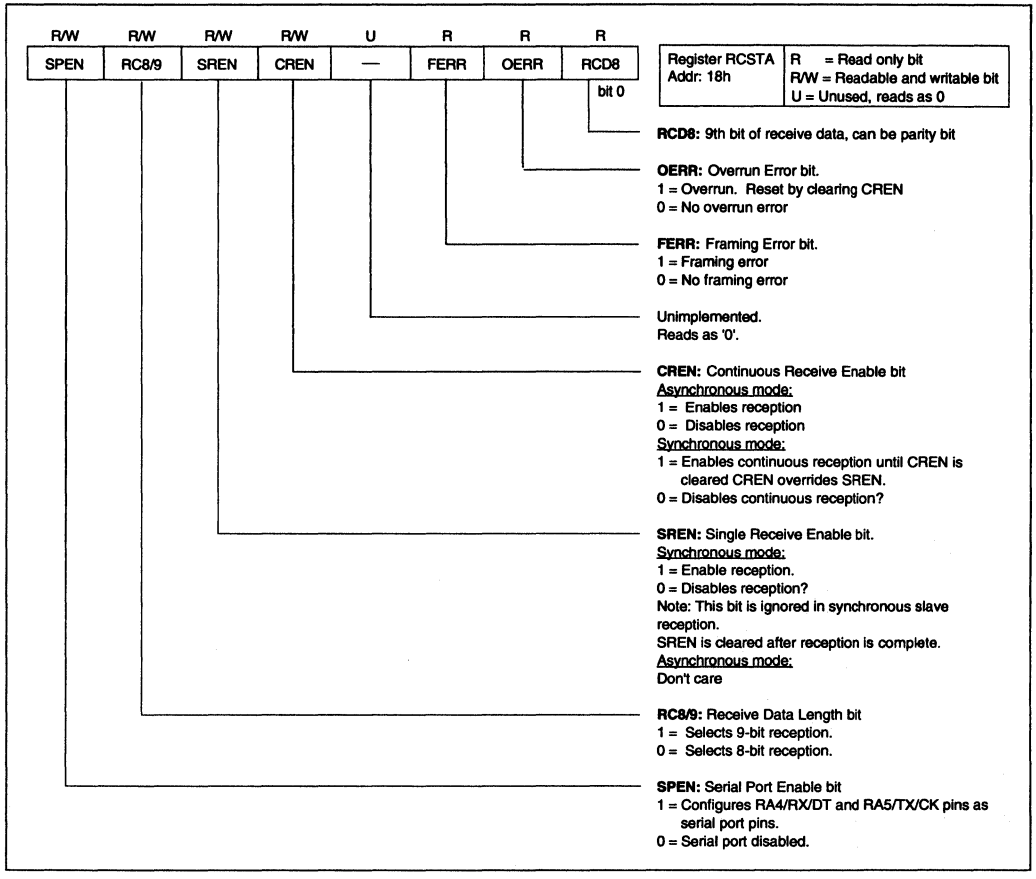


FIGURE 12-2: RCSTA: RECEIVE STATUS AND CONTOL REGISTER



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12.1 SCI BAUD RATE GENERATOR (BRG)

The BRG supports both the Asynchronous and Synchronous modes of the SCI. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In asynchronous mode the BRGH (TXSTA<2>) also controls the baud rate. In synchronous mode BRGH is ignored. Table 12-1 shows the formula for computation of the baud rate for different SCI modes.

Given the desired baud rate, and Fosc, the nearest integer value between 0 and 255 can be calculated using the formula below. The error in baud rate can then be determined.

TABLE 12-1: BAUD RATE FORMULA

SYNC	BRGH=0	BRGH=1
0	Baud Rate=Fosc/64(X+1)	Baud Rate=Fosc/16(X+1)
1	Baud Rate = Fosc/4(X+1)	NA

X = value in SPBRG (0 to 255)

Example 12-1 shows the calcualtion of the baud rate error for the following conditions:

Fosc = 16 MHz
Desired Baud Rate = 9600
BRGH = 0
SYNC = 0

EXAMPLE 12-1: CALCULATING BAUD RATE ERROR

Desired Baud rate = Fosc / (64 (X + 1))

9600 = 16000000 / 64 (X + 1)

X = 25.042 = 25

New Baud Rate = 16000000 / (64 (25 + 1))

= 9615

$$\text{Error} = \frac{\text{(New Baud Rate - Desired Baud Rate)}}{\text{Desired Baud Rate}}$$

= (9615 - 9600) / 9600

= 0.16%

It may be advantageous to use the high baud rate (BRGH = 1) even for slower baud clocks. This is because the FOSC/4(x + 1) equation can reduce the baud rate error in some cases.

Writing a new value to the SPREG, causes the BRG timer to be reset (or cleared), this guarantees that the BRG does not wait for a timer overflow before outputting the new baud rate.

TABLE 12-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x98	TXSTA	CSRC	TX8/9	TXEN	SYNC	—	BRGH	TRMT	TXD8
0x99	SPBRG	Baud Rate Register							

TABLE 12-3: BAUD RATES FOR SYNCHRONOUS MODE

BAUD RATE (K)	fosc = 20MHZ		SPBRG value (decimal)	16MHZ		SPBRG value (decimal)	10MHZ		SPBRG value (decimal)	7.15909MHZ		SPBRG value (decimal)
	KBAUD	%ERROR		KBAUD	%ERROR		KBAUD	%ERROR		KBAUD	%ERROR	
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	NA	-	-	NA	-	-	NA	-	-	NA	-	-
2.4	NA	-	-	NA	-	-	NA	-	-	NA	-	-
9.6	NA	-	-	NA	-	-	9.766	+1.73	255	9.622	+0.23	185
19.2	19.53	+1.73	255	19.23	+0.16	207	19.23	+0.16	129	19.24	+0.23	92
76.8	76.92	+0.16	64	76.92	+0.16	51	75.76	-1.36	32	77.82	+1.32	22
96	96.15	+0.16	51	95.24	-0.79	41	96.15	+0.16	25	94.20	-1.88	18
300	294.1	-1.96	16	307.69	+2.56	12	312.5	+4.17	7	298.3	-0.57	5
500	500	0	9	500	0	7	500	0	4	NA	-	-
HIGH	5000	-	0	4000	-	0	2500	-	0	1789.8	-	0
LOW	19.53	-	255	15.625	-	255	9.766	-	255	6.991	-	255

BAUD RATE (K)	fosc = 5.0688MHZ		SPBRG value (decimal)	3.579545MHZ		SPBRG value (decimal)	1MHZ		SPBRG value (decimal)	32.768KHZ		SPBRG value (decimal)
	KBAUD	%ERROR		KBAUD	%ERROR		KBAUD	%ERROR		KBAUD	%ERROR	
0.3	NA	-	-	NA	-	-	NA	-	-	0.303	+1.14	26
1.2	NA	-	-	NA	-	-	1.202	+0.16	207	1.170	-2.48	6
2.4	NA	-	-	NA	-	-	2.404	+0.16	103	NA	-	-
9.6	9.6	0	131	9.622	+0.23	92	9.615	+0.16	25	NA	-	-
19.2	19.2	0	65	19.04	-0.83	46	19.24	+0.16	12	NA	-	-
76.8	79.2	+3.13	15	74.57	-2.90	11	83.34	+8.51	2	NA	-	-
96	97.48	+1.54	12	99.43	+3.57	8	NA	-	-	NA	-	-
300	316.8	+5.60	3	298.3	-0.57	2	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	1267	-	0	894.9	-	0	250	-	0	8.192	-	0
LOW	4.950	-	255	3.496	-	255	0.9766	-	255	0.032	-	255

TABLE 12-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH=0)

BAUD RATE (K)	fosc = 20MHZ KBAUD	%ERROR	SPBRG value (decimal)	16MHZ KBAUD	%ERROR	SPBRG value (decimal)	10MHZ KBAUD	%ERROR	SPBRG value (decimal)	7.15909MHZ KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	1.221	+1.73	255	1.202	+0.16	207	1.202	+0.16	129	1.203	+0.23	92
2.4	2.404	+0.16	129	2.404	+0.16	103	2.404	+0.16	64	2.380	-0.83	46
9.6	9.469	-1.36	32	9.615	+0.16	25	9.766	+1.73	15	9.322	-2.90	11
19.2	19.53	+1.73	15	19.23	+0.16	12	19.53	+1.73	7	18.64	-2.90	5
76.8	78.13	+1.73	3	83.33	+8.51	2	78.13	+1.73	1	NA	-	-
96	104.2	+8.51	2	NA	-	-	NA	-	-	NA	-	-
300	312.5	+4.17	0	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	312.5	-	0	250	-	0	156.3	-	0	111.9	-	0
LOW	1.221	-	255	0.977	-	255	0.6104	-	255	0.437	-	255

BAUD RATE (K)	fosc = 5.0688MHZ KBAUD	%ERROR	SPBRG value (decimal)	3.579545MHZ KBAUD	%ERROR	SPBRG value (decimal)	1MHZ KBAUD	%ERROR	SPBRG value (decimal)	32.768KHZ KBAUD	%ERROR	SPBRG value (decimal)
0.3	0.31	+3.13	255	0.301	+0.23	185	0.300	+0.16	51	0.256	-14.67	1
1.2	1.2	0	65	1.190	-0.83	46	1.202	+0.16	12	NA	-	-
2.4	2.4	0	32	2.432	+1.32	22	2.232	-6.99	6	NA	-	-
9.6	9.9	+3.13	7	9.322	-2.90	5	NA	-	-	NA	-	-
19.2	19.8	+3.13	3	18.64	-2.90	2	NA	-	-	NA	-	-
76.8	79.2	+3.13	0	NA	-	-	NA	-	-	NA	-	-
96	NA	-	-	NA	-	-	NA	-	-	NA	-	-
300	NA	-	-	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	79.2	-	0	55.93	-	0	15.63	-	0	0.512	-	0
LOW	0.3094	-	255	0.2185	-	255	0.0610	-	255	0.0020	-	255

TABLE 12-5: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH=1)

BAUD RATE (K)	fosc = 20MHZ KBAUD	%ERROR	SPBRG value (decimal)	16MHZ KBAUD	%ERROR	SPBRG value (decimal)	10MHZ KBAUD	%ERROR	SPBRG value (decimal)	7.16MHZ KBAUD	%ERROR	SPBRG value (decimal)
9600	9615.34	+0.16	129	9615.34	+0.16	103	9615.39	+0.16	64	9520.07	-0.83	46
19200	19230.77	+0.16	64	19230.77	+0.16	51	18939.39	-1.36	32	19454.05	+1.32	22
38400	37878.79	-1.36	32	38461.54	+0.16	25	39062.5	+1.7	15	37286.93	-2.90	11
57600	56818.18	-1.36	21	58823.53	+2.12	16	56818.18	-1.36	10	55930.39	-2.90	7
115200	113636.4	-1.36	10	111111.1	-3.55	8	125000	+8.51	4	111860.8	-2.90	3
250000	250000	0	4	250000	0	3	NA	-	-	NA	-	-
625000	625000	0	1	NA	-	-	625000	0	0	NA	-	-
1250000	1250000	0	0	NA	-	-	NA	-	-	NA	-	-

BAUD RATE (K)	fosc = 5.068MHZ KBAUD	%ERROR	SPBRG value (decimal)	3.579MHZ KBAUD	%ERROR	SPBRG value (decimal)	1MHZ KBAUD	%ERROR	SPBRG value (decimal)	32.768KHZ KBAUD	%ERROR	SPBRG value (decimal)
9600	9600	0	32	9727.02	+1.32	22	8928.57	-6.99	6	NA	-	-
19200	18645.29	-2.94	16	18643.46	-2.90	11	20833.33	+8.51	2	NA	-	-
38400	39600	+3.12	7	37286.93	-2.90	5	31250	-18.61	1	NA	-	-
57600	52800	-8.33	5	55930.39	-2.90	3	62500	+8.51	0	NA	-	-
115200	105600	-8.33	2	111860.8	-2.90	1	NA	-	-	NA	-	-
250000	NA	-	-	223721.6	-10.51	0	NA	-	-	NA	-	-
625000	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1250000	NA	-	-	NA	-	-	NA	-	-	NA	-	-

12.1.1 SAMPLING

The data on the RX pin is sampled three times by a majority detect circuit to determine if a 1- or a 0-level is present at the RX pin. If BRGH is clear (i.e., at the low baud rates), the sampling is done on the seventh, eighth and ninth edge of a 16x clock (see Figure 12-2). If BRGH is set (i.e., at the high baud rates), the sampling is done on the 3 clocks preceding the second rising edge after the first falling edge of a 4x clock (see Figures 12-4 and 12-5).

FIGURE 12.3 - RX PIN SAMPLING SCHEME (BRGH=0)

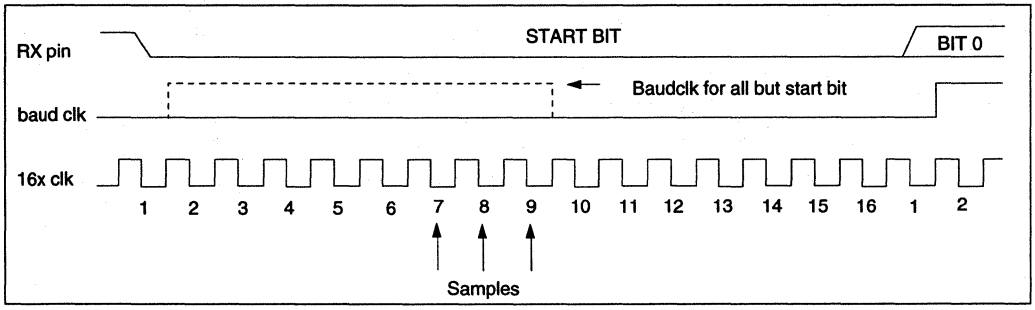


FIGURE 12.4 - RX PIN SAMPLING SCHEME (BRGH=1)

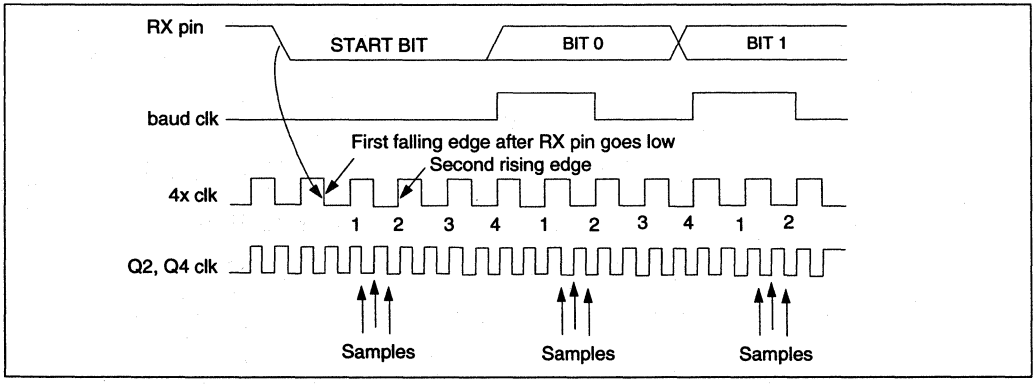
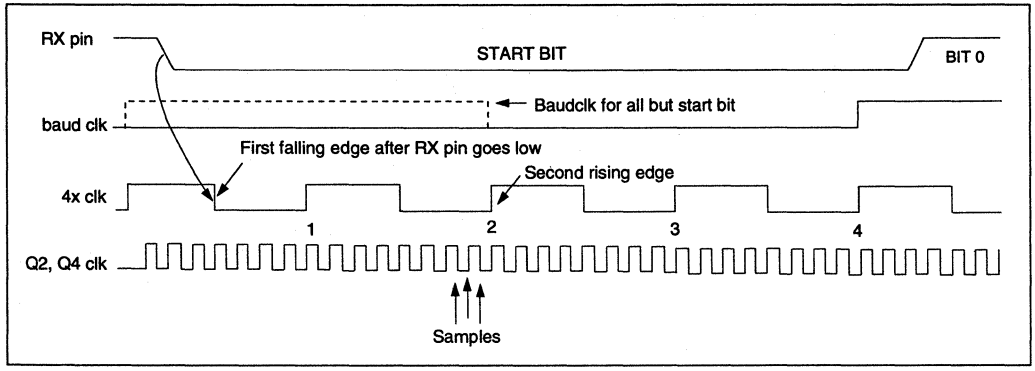


FIGURE 12.5 - RX PIN SAMPLING SCHEME (BRGH=1)



12.2 SCI Asynchronous Mode

In this mode, the SCI used standard nonreturn-to-zero (NRZ) format (one start bit, eight or nine data bits and one stop bit). The most common data format is 8-bits. An on-chip dedicated 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The SCI's transmitter and receiver are functionally independent but use the same data format and baud rate. The baud rate generator produces a clock either 16x or 64x of the bit shift rate, depending on the BRGH (TXSTA<2>) bit. Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

The asynchronous mode is selected by resetting the SYNC bit (TXSTA<4>).

The SCI Asynchronous module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

12.2.2 SCI ASYNCHRONOUS TRANSMITTER

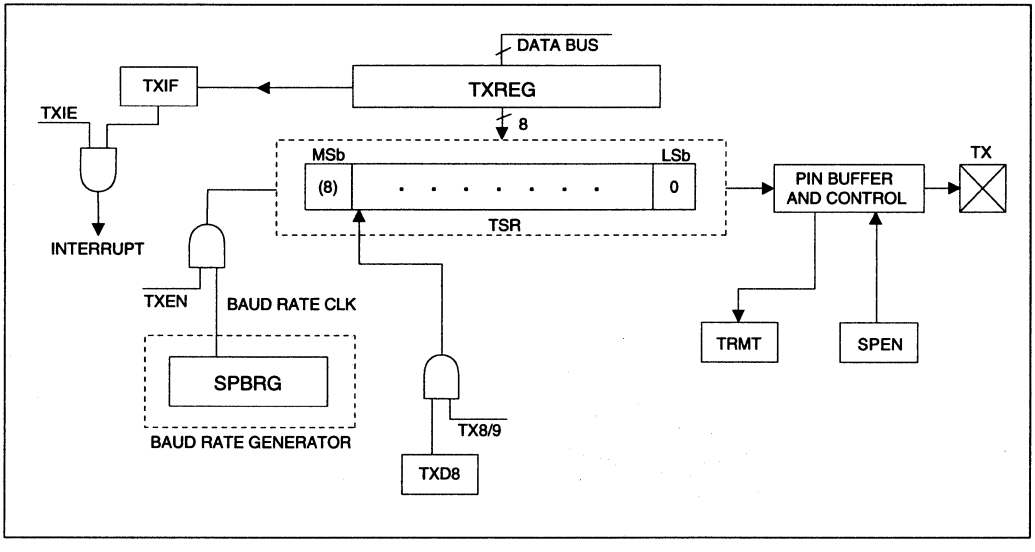
The SCI transmitter block diagram is shown in Figure 12-6. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer (TXREG). The TXREG is loaded with data in software. The TSR is not loaded until the stop bit has been transmitted from the previous load. As soon as the stop bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG transfers the data to the TSR(occurs in one Tcy), the TXREG is empty and a interrupt bit, TXIF (PIR1<4>) is set. This interrupt can be enabled or disabled by the TXIE bit (PIE1<4>). TXIF will be set regardless of TXIE and cannot be reset in software. It will reset only when new data is loaded into the TXREG. While TXIF indicated the status of the TXREG, another bit TRMT(TXSTA<1>) shows the status of the TSR. TRMT is a read only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR is empty.

Note: The TSR is not mapped in data memory so it is not available to the user.

Transmission is enabled by setting the TXEN (TXSTA<5>) bit. The actual transmission will not occur until the TXREG has been loaded with data and the baud rate generator (BRG) has produced a shift clock (Figure 12-6). The transmission can also be started by first loading the TXREG and then setting TXEN. Normally when transmission is first started, the TSR is empty, so a transfer to TXREG will result in an immediate transfer to TSR resulting in an empty TXREG. A back-to-back transfer is thus possible (Figure 12-8). Clearing TXEN during a transmission, will cause the transmission to be aborted and will reset the transmitter as a result the TX pin will revert to hi-impedance.

In order to select 9-bit transmission, the TX8/9 (TXSTA<6>) bit should be set and the ninth bit should be written to the TXD8(TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG. This is because a data write to the TXREG can result in an immediate transfer of the data to the TSR (if the TSR is empty). In such a case, an incorrect ninth data bit maybe loaded in the TSR.

FIGURE 12-6: BLOCK DIAGRAM FOR SCI TRANSMIT



Steps to follow when setting up a Asynchronous Transmission:

- Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set BRGH to 1. See Section 12.1 for details.
- Enable the asynchronous serial port by configuring the bits SYNC = 0 and SPEN = 1.
- Make sure CREN=SREN=0 (these bits override transmission when set to 1).
- If interrupts are desired, then the TXIE bit should be set.
- If 9-bit transmission is desired, then TX8/9 bit should be set.
- Enable the transmission by setting TXEN.
- If 9-bit transmission is selected, the ninth bit should be loaded in TXD8.
- Load data to the TXREG (starts transmission).

FIGURE 12-7: ASYNCHRONOUS MASTER TRANSMISSION

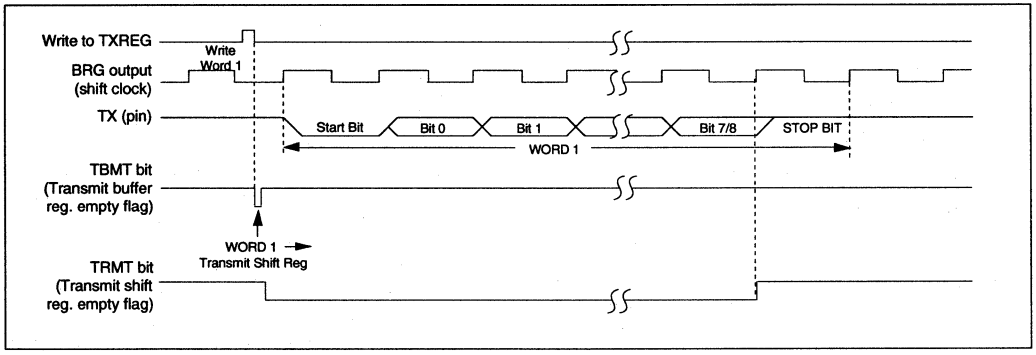
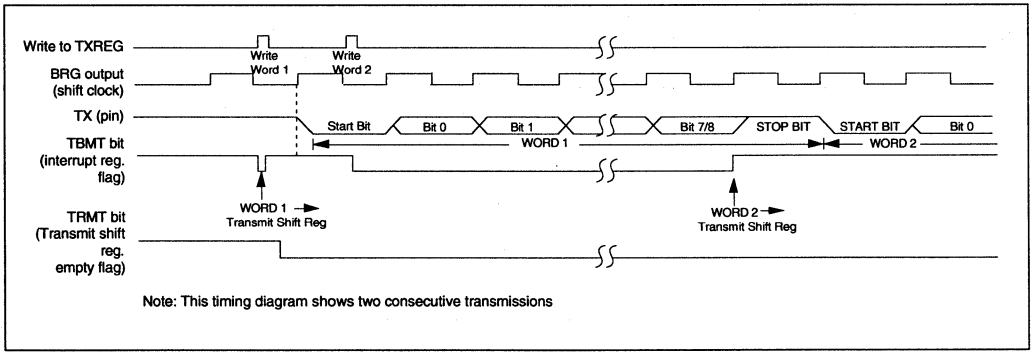


FIGURE 12-8: ASYNCHRONOUS MASTER TRANSMISSION (BACK TO BACK)



Note: This timing diagram shows two consecutive transmissions

TABLE 12-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION:

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
0x18	RCSTA	SPEN	RC8/9	SREN	CREN	—	FERR	OERR	RCD8
0x19	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0
0x8C	PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
0x98	TXSTA	CSRC	TX8/9	TXEN	SYNC	—	BRGH	TRMT	TXD8
0x99	SPBRG	Baud Rate Register							

12.2.2 SCI ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 12-9. The data comes in the RX pin and drives the data recovery block. The data recovery block is actually a high speed shifter operating at 16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at Fosc.

Once the asynchronous mode is selected, reception is enabled by setting the CREN(RCSTA<4> to 1.

The heart of the receiver is the receive (serial) shift register (RSR). After sampling the stop bit, the received data in the RSR is transferred to the RCREG (if it is empty). If the transfer is complete, the interrupt bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled or disabled by the RCIE(PIE1<5>) bit. The RCIF is a read only bit which is reset by the hardware. In this case it is cleared when the RCREG has been read and is empty.

The RCREG is a double buffered register, i.e. it is a two deep FIFO. It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte begin shifting to the RSR. On the detection of the stop bit of the third byte, if the RCREG is still full then the overrun error bit, OERR (RCSTA<1>) will be set. The word in the RSR will be lost. The RCREG can be read twice to retrieve the two bytes in the FIFO. The OERR bit has to be cleared in software and this is done by resetting the receive logic (CREN is set). If the OERR is set, transfers from the RSR to the RCREG are inhibited, so it is essential to OERR is set. The framing error bit FERR(RCSTA<2>) is set if a stop bit is detected as a 0. The FERR and the 9th receive bit are buffered the same way as the receive data. Reading the RCREG, will load the RCD8 and the FERR with new values, therefore it is essential for the user to read the RCSTA register before reading RCREG in order not to lose the old FERR and RCD8 information.

2

FIGURE 12-9: BLOCK DIAGRAM FOR SCI RECEIVE

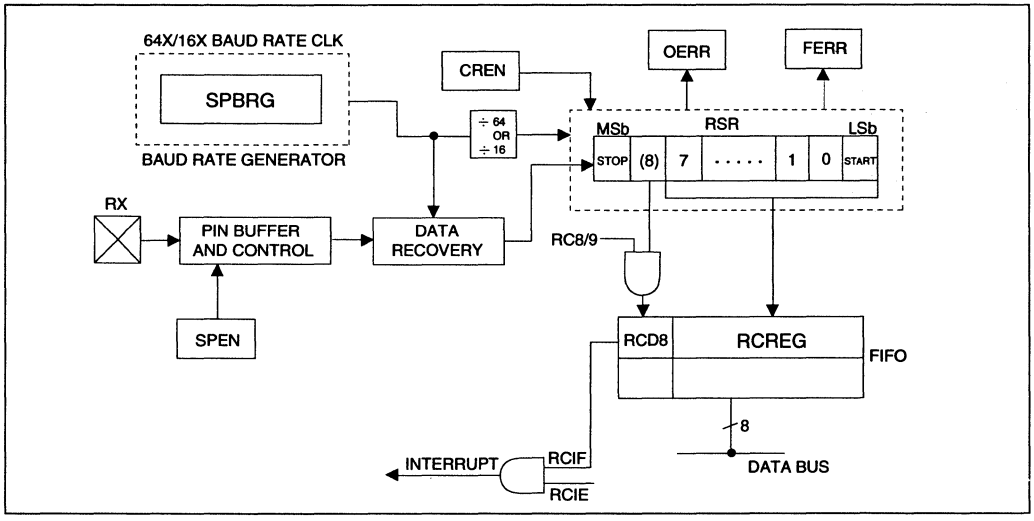
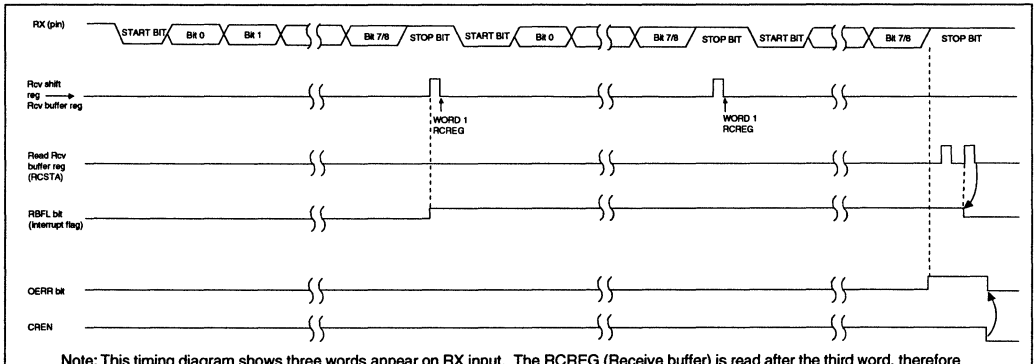


FIGURE 12-10: ASYNCHRONOUS RECEPTION



Note: This timing diagram shows three words appear on RX input. The RCREG (Receive buffer) is read after the third word, therefore causing the OERR (overrun) bit to set.

Steps to follow when setting up a Asynchronous Reception:

- Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set BRGH. See Section 12.1 for details.
- Enable the asynchronous serial port by configuring the SYNC = 0 and SPEN = 1.
- If interrupts are desired, then the RXIE bit should be set.
- If 9-bit reception is desired, then RX8/9-bit should be set.
- Enable the reception by setting CREN.
- The RCIF bit will be set when reception is complete and an interrupt will be generated if the RCIE bit were set.
- Read the RCSTA to get the ninth bit(if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG.
- If any error occurred, clear the error by clearing CREN.

TABLE 12-7: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
0x18	RCSTA	SPEN	RC8/9	SREN	CREN	—	FERR	OERR	RCD8
0x19	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0
0x8C	PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
0x98	TXSTA	CSRC	TX8/9	TXEN	SYNC	—	BRGH	TRMT	TXD8
0x99	SPBRG	Baud Rate Register							

12.3 SCI Synchronous Master Mode

In Master Synchronous mode the data is transmitted in a half-duplex manner i.e. transmission and reception do not occur at the same time, when transmitting data, the reception is inhibited and visa versa. The synchronous mode is entered by setting the SYNC(TXSTA<4>) bit. In addition the SPEN(RCSTA<7>) bit is set in order to configure the RC6 and RC7 I/O ports to CK(clock) and DT(data) lines respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting the CSRC(TXSTA<7>) bit.

12.3.1 SCI SYNCHRONOUS MASTER TRANSMISSION

The SCI transmitter block diagram is shown in Figure 12-6. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer TXREG. The TXREG is loaded with data in software. The TSR is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG transfers the data to the TSR(occurs in one Tcycle), the TXREG is empty and a interrupt bit, TXIF (PIR1<4>) is set. This interrupt can be enabled or disabled by the TXIE bit (PIE1<4>). TXIF will be set regardless of TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG. While TXIF indicated the status of the TXREG, another bit TRMT(TXSTA<1>) shows the status of the TSR. TRMT is a read only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR is empty. The TSR is not mapped in data memory so it is not available to the user.

Transmission is enabled by setting the TXEN (TXSTA<5>) bit. The actual transmission will not occur until the TXREG has been loaded with data. The first data bit will be shifted out on the next available rising edge of the clock on CK. Data out is stable around the falling edge of the synchronous clock (Figure 12-1). The transmission can also be started by first loading the TXREG and then setting TXEN. This is advantageous when slow baud rates are selected, since the BRG is kept in reset when TXEN=CREN=SREN = 0. Setting the TXEN bit will start the BRG, creating a shift clock immediately. Normally when transmission is first started, the TSR is empty, so a transfer to TXREG will result in an immediate transfer to TSR resulting in an empty TXREG. Back-to-back transfers are possible.

Clearing TXEN during a transmission, will cause the transmission to be aborted and will reset the transmitter. The DT and CK pins will revert to hi-impedance. If either CREN or SREN are set, during a transmission, the transmission is aborted and the DT pin reverts to a hi-impedance state (for a reception). The CK pin will remain an output if CSRC=1(internal clock). The transmitter logic however is not reset although it is disconnected from the pins. In order to reset the transmitter, the user has to clear TXEN. If the SREN bit is set (to interrupt an on going transmission and receive a single word), then after the single word is received, the SREN will = 0 and the serial port will revert back to transmitting since the TXEN bit is still set. The DT line will immediately switch from hi-impedance receive mode to transmit and start driving. To avoid this, TXEN should be cleared.

In order to select 9-bit transmission, the TX8/9 (TXSTA<6>) bit should be set and the ninth bit should be written to the TXD8(TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG. This is because a data write to the TXREG can result in an immediate transfer of the data to the TSR (if the TSR is empty). If the TSR was empty and the TXREG was written before writing the "new" TXD8, the "present" value of TXD8 is loaded.

Steps to follow when setting up a Synchronous Master Transmission:

- Initialize the SPBRG register for the appropriate baud rate (see Section 12.1 for details)
- Enable the synchronous master serial port by configuring the bits SYNC = 1, SPEN = 1 and CSRC = 1.
- If interrupts are desired, then the TXIE bit should be set.
- If 9-bit transmission is desired, then TX8/9-bit should be set.
- Enable the transmission by setting TXEN to 1.
- If 9-bit transmission is selected, the ninth bit should be loaded in TXD8.
- Start transmission by loading data to the TXREG.

TABLE 12-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION:

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
0x18	RCSTA	SPEN	RC8/9	SREN	CREN	—	FERR	OERR	RCD8
0x19	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	T X0
0x8C	PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
0x98	TXSTA	CSRC	TX8/9	TXEN	SYNC	—	BRGH	TRMT	TXD8
0x99	SPBRG	Baud Rate Register							

FIGURE 12-11: SYNCHRONOUS TRANSMISSION

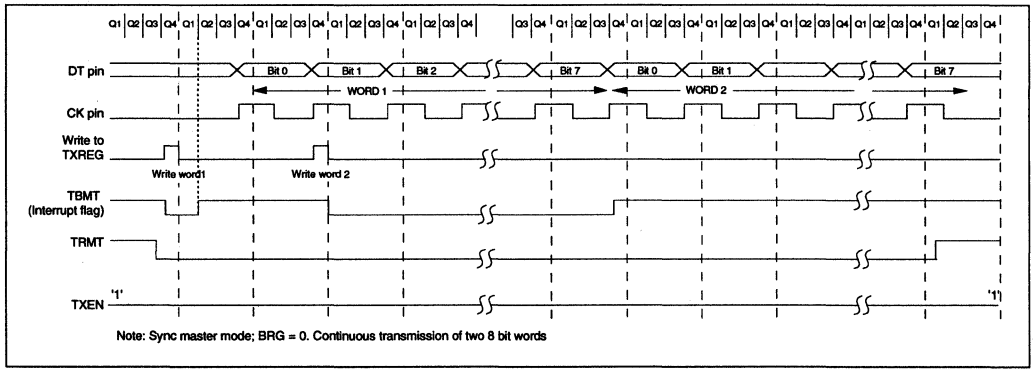
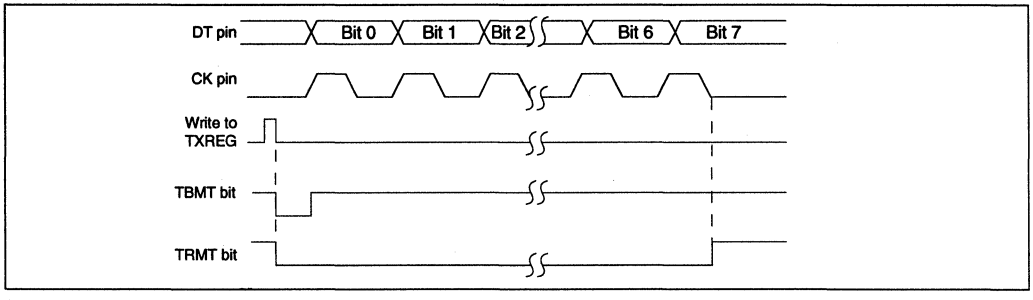


FIGURE 12-12: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



12.3.2 SCI SYNCHRONOUS MASTER RECEPTION

Once the synchronous mode is selected, reception is enabled by setting either the SREN(RCSTA<5>) bit or the CREN(RCSTA<4>). Data is sampled on the DT pin on the falling edge of the clock. If SREN is set, then only a single word is received, if CREN is set, the reception is continuous until CREN is reset. If both the bit are set then CREN takes precedence. After clocking the last bit, the received data in the Receive Shift Register(RSR) is transferred to the RCREG (if it is empty). If the transfer is complete, the interrupt bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled or disabled by the RCIE(PIE1<5>) bit. The RCIF is a read only bit which is reset by the hardware. In this case it is reset when the RCREG has been read and is empty. The RCREG is a double buffered register, i.e. it is a two deep FIFO. It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte begin shifting to the RSR. On the clocking of the last bit of the third byte, if the RCREG is still full then the overrun error bit, OERR (RCSTA<1>) is set. The word in the RSR will be lost. The RCREG can be read twice to retrieve the two bytes in the FIFO. The OERR bit has to be cleared in software and this is done by clearing CREN. If the OERR is set, transfers from the RSR to the RCREG are inhibited, so it is essential to clear the OERR if set. The 9th receive bit is buffered the same way as the receive data. Reading the RCREG, will load the RCD8 with a new value, therefore it is essential for the user to read the RCSTA register before reading RCREG in order not to lose the old RCD8 information.

Steps to follow when setting up a Synchronous Master Reception:

- Initialize the SPBRG register for the appropriate baud rate. See section 12.1 for details.
- Enable the synchronous master serial port by configuring the bits SYNC = 1, SPEN = 1 and CSRC = 1.
- If interrupts are desired, then the RXIE bit should be set.
- If 9-bit reception is desired, then RX8/9-bit should be set.
- If a single reception is required, set SREN. For continuous reception set CREN.
- The RCIF bit will be set when reception is complete and an interrupt will be generated if the RCIE bit were set.
- Read the RCSTA to get the ninth bit(if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG.
- If any error occurred, clear the error by clearing CREN.

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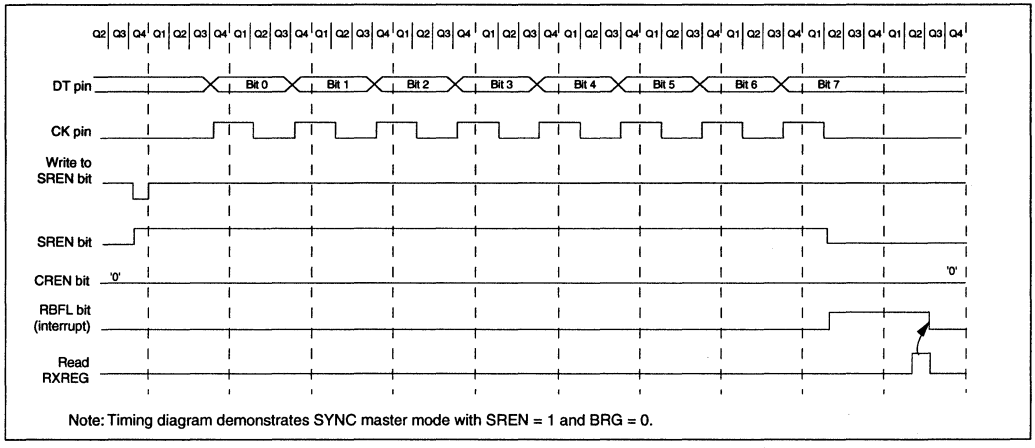
TABLE 12-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION:

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
0x18	RCSTA	SPEN	RC8/9	SREN	CREN	—	FERR	OERR	RCD8
0x19	PCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0
0x8C	PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
0x98	TXSTA	CSRC	TX8/9	TXEN	SYNC	—	BRGH	TRMT	TXD8
0x99	SPBRG	Baud Rate Register							

FIGURE 12-13: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates SYNC master mode with SREN = 1 and BRG = 0.

12.4 SCI Synchronous Slave Mode

The synchronous slave mode differs from the master mode in the fact that the shift clock is supplied externally at the CK pin (instead of being supplied internally in the master mode). This allows the device to transfer or receive data in the SLEEP mode. The slave mode is entered by clearing the CSRC(TXSTA<7>) bit.

12.4.1 SCI SYNCHRONOUS SLAVE TRANSMIT

The operation of the sync master and slave modes are identical except in the case of the SLEEP mode.

If two words are written to the TXREG and then the SLEEP instruction executed, the following will occur. The first word will immediately transfer to the TSR and transmit. The second word will remain in TXREG. The TXIF will not be set. When the first word has been shifted out of TSR, the TXREG will transfer the second word to the TSR and the TXIF flag will now be set. If the TXIE is enabled, the interrupt will wake the chip from SLEEP and if the global interrupt is enabled, then the program will branch to the interrupt vector (0004h).

Steps to follow when setting up a Synchronous Slave Transmission:

- Enable the synchronous slave serial port by configuring the bits SYNC = 1, SPEN = 1 and CSRC = 0.
- Make CREN = 0
- If interrupts are desired, then the TXIE bit should be set.
- If 9-bit transmission is desired, then TX8/9-bit should be set.
- Enable the transmission by setting TXEN to 1.
- If 9-bit transmission is selected, the ninth bit should be loaded in TXD8.
- Start transmission by loading data to the TXREG.

12.4.2 SCI SYNCHRONOUS SLAVE RECEPTION

The operation of the synchronous master and slave modes is identical except in the case of the SLEEP mode. Also, SREN is a don't care in slave mode.

If receive is enabled (CREN) prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR will transfer the data to the RCREG and if the RCIE bit is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up a Synchronous Slave Reception:

- Enable the synchronous master serial port by configuring the bits SYNC = 1, SPEN = 1 and CSRC = 0.
- If interrupts are desired, then the RCIE bit should be set.
- If 9-bit reception is desired, then RX8/9-bit should be set.
- To enable reception, set CREN = 1.
- The RCIF bit will be set when reception is complete and an interrupt will be generated if the RCIE bit were set.
- Read the RCSTA to get the ninth bit(if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG.
- If any error occurred, clear the error by clearing CREN.

TABLE 12-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
0x18	RCSTA	SPEN	RC8/9	SREN	CREN	—	FERR	OERR	RCD8
0x19	TXREG	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0
0x8C	PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
0x98	TXSTA	CSRC	TX8/9	TXEN	SYNC	—	BRGH	TRMT	TXD8
0x99	SPBRG	Baud Rate Register							

TABLE 12-11: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
0x18	RCSTA	SPEN	RC8/9	SREN	CREN	—	FERR	OERR	RCD8
0x19	RCREG	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0
0x8C	PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
0x98	TXSTA	CSRC	TX8/9	TXEN	SYNC	—	BRGH	TRMT	TXD8
0x99	SPBRG	Baud Rate Register							

13.0 ANALOG TO DIGITAL CONVERTER MODULE (A/D)

Analog-to-Digital Converter (A/D) Module

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a corresponding 8-bit digital number. The A/D module has eight analog inputs, which are multiplexed into one sample and hold. The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (V_{DD}) or the voltage level on the RA3/AN3/VREF pin. The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode.

The A/D module has three registers. These registers are:

- A/D result register (ADRES)
- A/D control register 0 (ADCON0)
- A/D control register 1 (ADCON1)

The ADCON0 register, shown in Figure 13-1, controls the operation of the A/D module. The ADCON1 register, shown in Figure 13-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be a voltage reference) or as digital I/O.

2

FIGURE 13-1: A/D CONTROL REGISTER 0 (ADCON0)

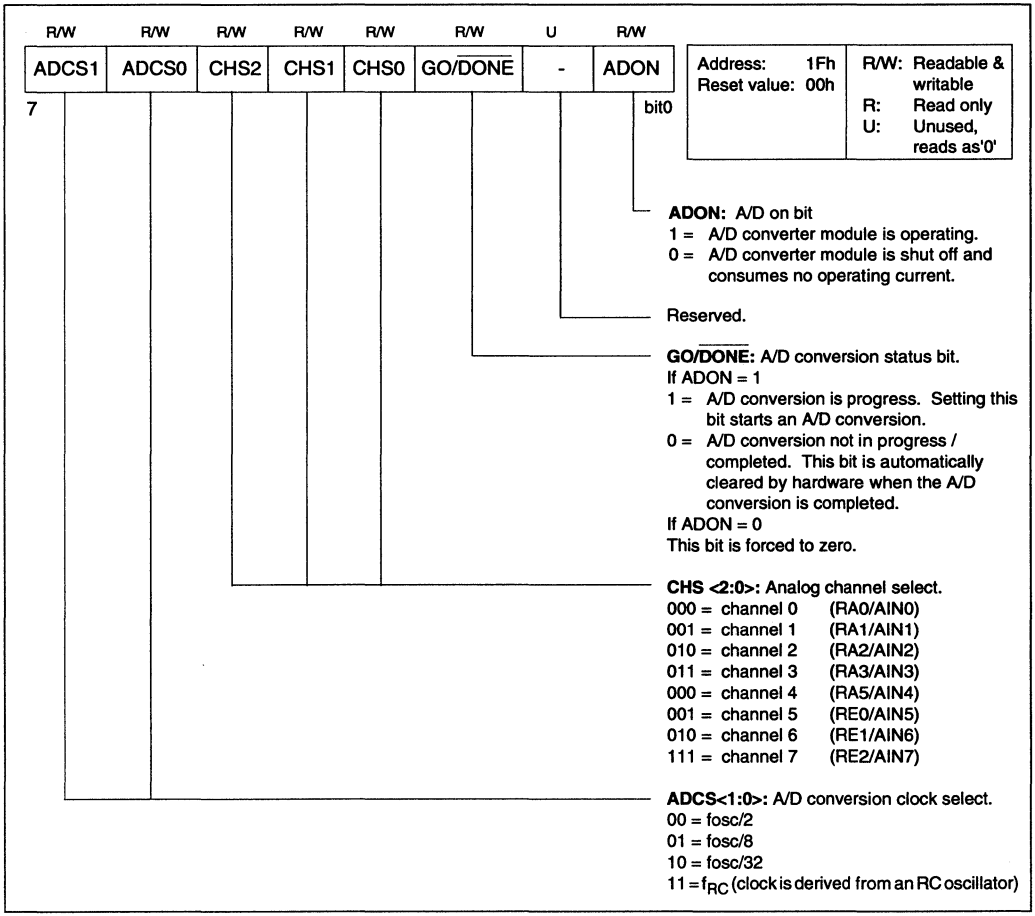


FIGURE 13-2: A/D CONTROL REGISTER 1 (ADCON1)

U	U	U	U	U	R/W	R/W	R/W
-	-	-	-	-	PCFG2	PCFG1	PCFG0
							bit0

Address: 9Fh
Reset value: 00h

R/W: Readable & writable
R: Read only
U: Unused, reads as'0'

PCFG<2:0>: A/D port configuration bits. These bits configure the analog port pins to the various modes of operation.

PCFG <2:0>	RA0	RA1	RA2	RA5	RA3	RE0	RE1	RE2	Ref
000	A	A	A	A	A	A	A	A	VDD
001	A	A	A	A	VREF	A	A	A	RA3
010	A	A	A	A	A	D	D	D	VDD
011	A	A	A	A	VREF	D	D	D	RA3
100	A	A	D	D	A	D	D	D	VDD
101	A	A	D	D	VREF	D	D	D	RA3
11X	D	D	D	D	D	D	D	D	-

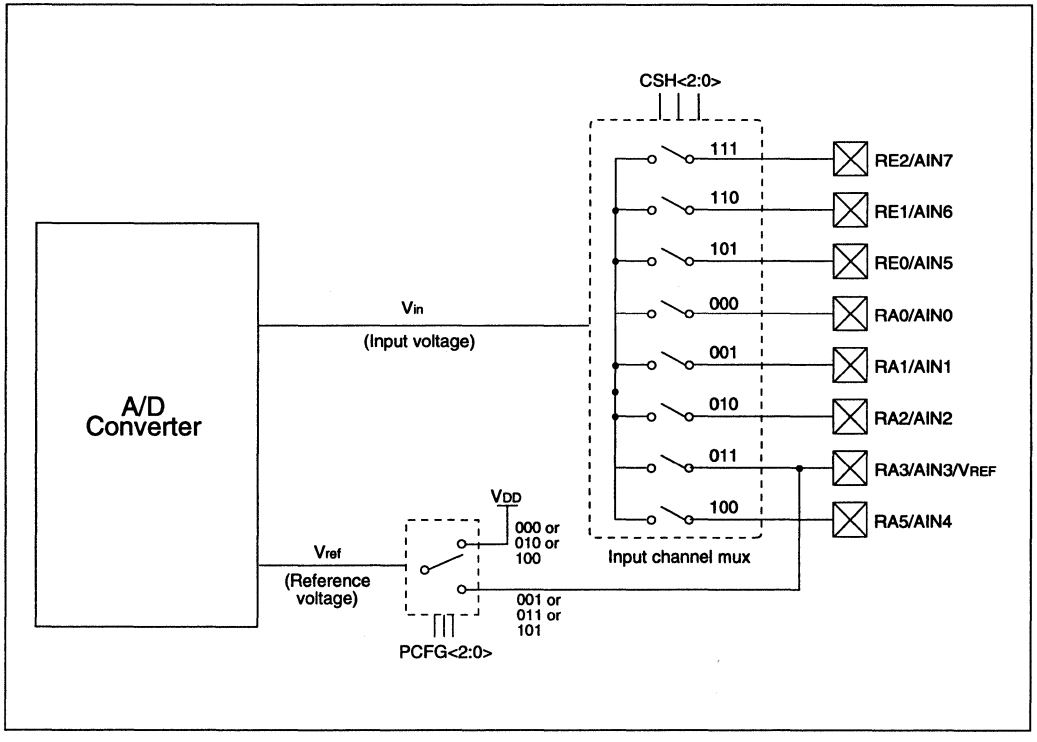
A = Analog input
D = Digital input/output depending on corresponding TRIS bit

The ADRES register contains the result of the A/D conversion. When the A/D conversion is completed, the result is loaded into the ADRES, the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) is cleared, and the A/D interrupt flag (ADIF) is set. The block diagram of the A/D module is shown in Figure 13-3.

After the A/D module has been configured as desired, the selected channel must be sampled before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. The A/D bit sample time is defined as T_{ad}. To determine sample time see Section 13.1. After this sample time has elapsed the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

1. Configure the A/D module
   - Configure analog pins / voltage reference / and digital I/O (ADCON1<2:0>)
   - Select A/D input channel (ADCON0<5:3>)
   - Select A/D conversion clock (ADCON<7:6>)
   - Turn on A/D module (ADCON<0>)
2. Configure A/D interrupt (if required)
   - Clear ADIF bit (PIR1<6>)
   - Set ADIE bit (PIE1<6>)
   - Set GIE bit (INTCON<7>
3. Ensure required sampling time
4. Start conversion
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0<2>)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared
   - Waiting for the A/D interrupt
6. Read A/D Result register (ADRES), clear ADIF if required.
7. For next conversion, go to step 1 or step 2 as required. A minimum wait of $2T_{ad}$ is required before next sampling starts.

FIGURE 13-3: A/D BLOCK DIAGRAM



13.1 Sampling Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (C_{hold}) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 13-4. The source impedance (R_S) and the internal sampling switch (R_{ss}) impedence directly affect the time required to charge the capacitor C_{hold}. The sampling switch (R_{ss}) impedence varies over the device voltage (Vdd), see Figure 13-4. **The maximum recommended impedance for analog sources is 10-KΩ.** After the analog input channel is selected (changed) this sampling time must be done before the conversion is started.

To calculate the minimum sampling time, Equation 13-1 may be used. This equation assumes that 1/2 lsb error is used (512 steps for the A/D). The 1/2 lsb error is the maximum error allowed for the A/D to meet its specified resolution.

EQUATION 13-1: A/D SAMPLING TIME EQUATION

$$V_{REF} = (V_{REF} - V_{REF}/512) \bullet (1 - e^{(-t/C_{hold}(R_{IC} + R_{SS} + R_S)})$$

or

$$t = -51.2\ pF\ (2\text{-}K\Omega + R_S)\ \ln(1/511)$$

Example 13-1 shows the calculation of the minimum required sample time. This calculation is based on the following system assumptions:

R_S = 10-KΩ
1/2 LSB error
Vdd = 5-V ⇒ Rss = 7-KΩ
Temp (system Max.) = 50°C

Note:
1. The reference voltage (V_{REF}) has no effect on the equation, since it cancels itself out.
2. The charge holding capacitor (C_{hold}) is not discharged after each conversion.
3. The maximum recommended impedance for analog sources is 10-KΩ. This is required to meet the pin leakage specification.
4. After a conversion has completed, 2 T_{ad} time must be waited before sampling can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

EXAMPLE 13-1: CALCULATING THE MINIMUM REQUIRED SAMPLE TIME

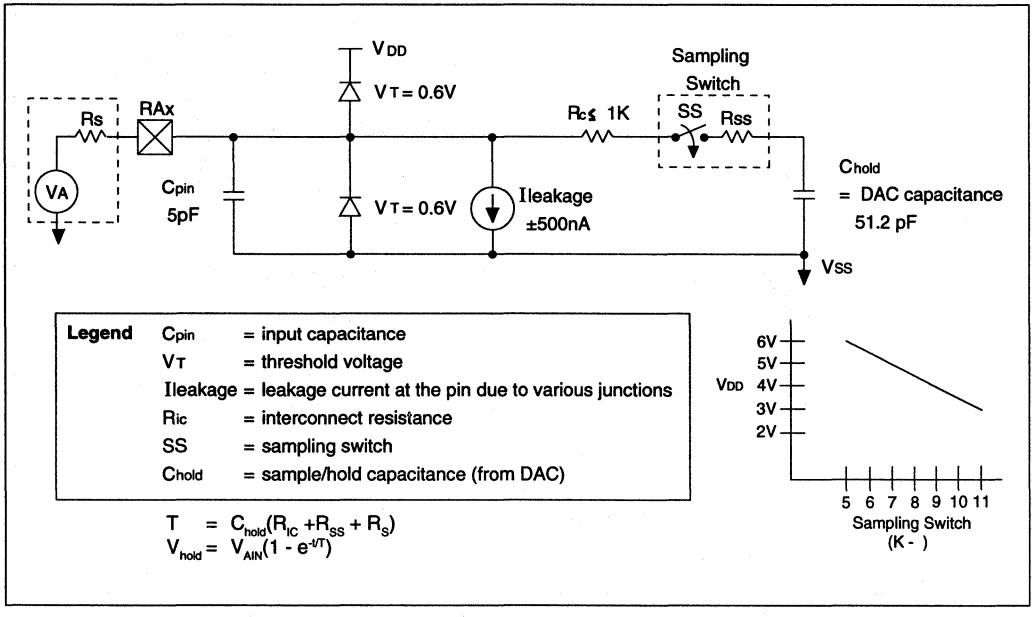
Sampling Time = Amplifier Settling Time
+ Holding Capacitor Charging Time
+ Temperature Coefficient †
= 5µs + t + [(Temp - 25°C) (0.05µs/°C)]†

t = $-C_{hold}(R_{IC} + R_{SS} + R_S)\ \ln(1/511)$
-51.2 pF (8-KΩ + 10-KΩ) ln (0.0020)
-51.2 pF (18-KΩ) ln (-0.0020)
-0.921µs (-6.2364)
5.724µs

Sampling Time = 5µs + 5.724µs + [(50°C - 25°C) (0.05µs / °C)]
= 10.724µs + 1.25µs
= 11.974µs

† The temperature coefficient is only required for temperatures > 25°C.

FIGURE 13.4: ANALOG INPUT MODEL



$$T = C_{hold}(R_{IC} + R_{SS} + R_S)$$
$$V_{hold} = V_{AIN}(1 - e^{-t/T})$$

13.2 Selecting the Conversion Clock

The A/D conversion requires 10 T_{ad}. The source of the A/D conversion clock is software selected. The four possible options for T_{ad} are:

- 2 T_{OSC}
- 8 T_{OSC}
- 32 T_{OSC}
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (T_{ad}) must be selected to ensure a minimum T_{ad} time of 1.6 us. Table 13-1 shows the resultant T_{ad} times derived from the device operating frequencies and the A/D clock source selected.

13.3 Configuring Analog Port Pins

The use of the ADCON1, TRISA, and TRISE registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be the converted.

The A/D operation is independent of the state of the CS<2:0> bits and the TRIS bits.

Note: 1. When reading the PORT register, all pins configured as analog input channel will read as cleared (a low level). Pins configured as digital inputs, will convert an analog in put. Analog levels on a digitally configured input will not affect the conversion accuracy.

2. Analog levels on any pin that is defined as a digital input (including the AIN7-0 pins), may cause the input buffer to consume current that is out of the devices specification.

2

TABLE 13-1: T_{AD} VS. DEVICE OPERATING FREQUENCIES

AD Clock Source (T_{ad})		Device Frequency			
Operation	ADCS1:ADCS0	20 MHz	5MHz	1.25 MHz	333.33 KHz
2 Tosc	00	100 ns §	400 ns §	1.6 µs	6µs
8 Tosc	01	400 ns §	1.6 µs	6.4 µs	24 µs ♠
32 Tosc	10	1.6 µs	6.4 µs	25.6 µs ♠	96 µs ♠
RC	11	2 - 6 µs*	2 -6 µs*	2 - 6 µs*	2 -6 µs*

* The RC source has a typical T_{ad} time of 4 us.

§ These values violate the minimum required T_{ad} time.

♠ For faster conversion times, the selection of another clock source is recommended.

13.4 A/D Conversions

Example 13-2 shows how to perform an A/D conversion. The RA0, RA1, and RA3 pins are configured as analog inputs. The analog reference (V_{REF}) is the device V_{DD}. The RA2, RA5, RE<2:0> pins are configured as digital I/O. The A/D interrupt is enabled, and the A/D conversion clock is T_{RC}. The conversion is performed on the RA0 channel.

EXAMPLE 13-2: DOING AN A/D CONVERSION

```
   BSF     STATUS, RP0    ; Select Page 1
   MOVLW   0x04           ; Configure A/D Inputs
   MOVWF   ADCON1         ;
   BSF     PIE1, ADIE     ; Enable A/D interrupts
   BCF     STATUS, RP0    ; Select Page 0
   MOVLW   0xC1           ; RC clock, A/D is on,
                          ; Ch 0 is selected
   MOVWF   ADCON0         ;
   BCF     PIR1, ADIF     ; Clear A/D Int Flag
   BSF     INTCON, PEIE   ; Enable Peripheral
                          ; Interrupts
   BSF     INTCON, GIE    ; Enable All Interrupts
;
; Ensure that the required sampling time for the
; selected input channel has lasped. Then the
; conversion may be started.
   BSF     ADCON0, GO     ; Start A/D Conversion
           :                The ADIF bit will be
           :                set and theGO/DONE bit
           :                cleared upon comple-
                            tion of the A/D con-
                            version.
```

Note: The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The ADRES will NOT be updated with the partially completed A/D conversion sample. That is the ADRES will continue to contain the value of the last completed conversion (or the last value written to the ADRES register). After the A/D conversion is aborted, the $2T_{ad}$ wait is required before the next sampling is started. After this $2T_{ad}$ wait, sampling is automatically started on the selected channel.

13.4.1 FASTER CONVERSION - LOWER RESOLUTION TRADEOFF

Not all applications require a result with 8-bits of resolution, but may instead require a faster conversion time. The A/D module allows users to make the trade off of conversion speed to resolution. Regardless of the resolution required, the sampling time is the same. To speed up the conversion, the clock source of the A/D module may be switched so that the T_{ad} time violates the minimum specified time (see specification # 120). Once the T_{ad} time violates the minimum specified time, all the following A/D result bits are not valid (see A/D Conversion Timing in the Electrical Specifications section.) The clock sources may only be switched between the three oscillator versions (cannot be switched from/to RC). The equation to determine the time before the oscillator can be switched is as follows:

$$\text{Conversion time} = 2T_{ad} + N\,T_{ad} + (8 - N)(2\,T_{OSC})$$

Where: N = number of bits of resolution required

Since the T_{ad} is based from the device oscillator, the user must use some method (a timer, software loop, etc) to determine when the A/D oscillator may be changed. Example 13-2 shows a comparison of time required for a conversion with 4-bits of resolution, verses the 8-bit resolution conversion. The example is for a device operating at 20 MHz (The A/D clock is programmed for 32 TOSC), and assumes that immediately after 6 T_{ad}, the A/D clock is programmed for $2T_{OSC}$.

The 2 TOSC violates the T_{ad} time of 1.6 µs, since the last 4-bits will not be converted to correct values.

EXAMPLE 13-2: 4-BIT VS. 8-BIT CONVERSION TIMES (AT 20 MHz).

	Resolution	
	4-bit	8-bit
Tad	1.6 µs	1.6 µs
TOSC	50 ns	50 ns
2Tad+NTad+(8-N)(2TOSC)	10 µs	16 µs

13.5 Use of the CCP2 Trigger

An A/D conversion can be started by the "special event trigger" of the CCP2 module. This requires that the CCP2M<3:0> bits (CCP2CON<3:0>) be programmed as 1011b and that the A/D module is enabled (ADON is set). When the trigger occurs, the GO/DONE bit will be set to start the A/D conversion and the Timer 1 counter will be reset to zero. Timer 1 is reset to automatically repeat the A/D sampling period, with minimal software overhead (moving the ADRES to the desired location). The appropriate analog input channel must be selected and the minimum sampling done before the "special event trigger" sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), then the "special event trigger" will be ignored by the A/D module, but will still reset the Timer 1 counter.

13.6 Operation During Sleep

The A/D module can operate during SLEEP mode. This requires that the A/D clock source be set to RC (ADCS<1:0> = 11b). When the RC clock source is selected the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise from the conversion. When the conversion is completed the GO/DONE bit will be cleared, and the result loaded into the ADRES register. If the A/D interrupt is enabled, the device will wake-up from SLEEP. If the A/D interrupt is not enabled, the A/D module will remain be turned off, though the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note: For the A/D module to operate in SLEEP, the A/D clock source must be set to RC (ADCS<1:0>=11b).

13.7 A/D Accuracy/Error

The overall accuracy of the A/D is less than ± 1 LSB for V_{DD} = 5 V ± 10% and the analog $V_{REF} = V_{DD}$. This overall accuracy includes offset error, full scale error, and integral error. The A/D converter is guaranteed to be monotonic. The resolution and accuracy may be less when either the analog reference (V_{DD}) is less then 5.0V or when the analog reference (V_{REF}) is less then V_{DD}.

The maximum pin leakage current is ± 5 µa.

In systems where the device frequency is low, use of the A/D clock derived from the device oscillator is preferred. This is because T_{ad}, when derived from T_{OSC} is kept away from on-chip phase clock transitions. This reduces, to a large extent, the effects of digital switching noise. This is not possible with the RC derived clock. The loss of accuracy due to digital switching noise can be significant if many I/O pins are active.

In systems where the device will enter SLEEP mode after the start of the A/D conversion, the RC clock source selection is required. In this mode, the digital noise from the modules in SLEEP are stopped. This method gives the highest accuracy.

13.8 Effects of a RESET

A device reset forces all register to their reset state. This forces the A/D module to be turned off, and any conversion is aborted. The value that is in the ADRES register is not modified for a power-on reset. The ADRES register will contain unknown data after a power-up reset.

13.9 Connection Considerations

Since the analog inputs employ ESD protection, they have reversed biased diodes to V_{DD} and V_{SS}. This requires that the analog input must be between V_{DD} and V_{SS}. If the input voltage exceeds this range by greater than 0.6V (either direction), one of the diodes is forward biased and it may damage the device if the input current specification is exceeded.

An external RC filter is sometimes added for anti-aliasing of the input signal. The R component should be selected to ensure that the total source impedance is kept under the 10 K recommended specification. Any external components connected (via high impedance) to an analog input pin (capacitor, zener diode, etc.) should have very little leakage current at the pin.

13.10 Transfer Function

The ideal transfer function of the A/D converter is as follows: The first transition occurs when the analog input voltage (V_{AIN}) is 1 LSB (or Analog V_{REF} / 256). This is shown in Figure 13-5.

FIGURE 13.5 - A/D TRANSFER FUNCTION

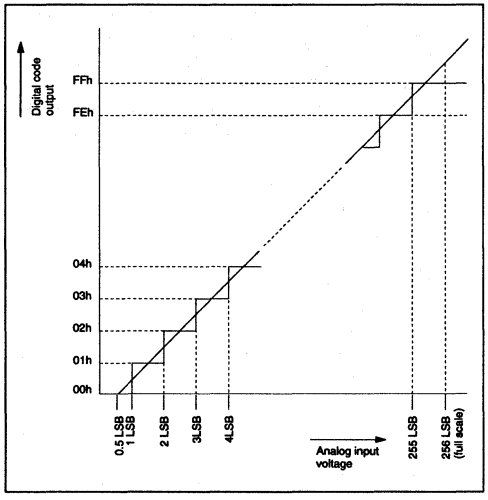


FIGURE 13.6 - FLOWCHART OF A/D OPERATION

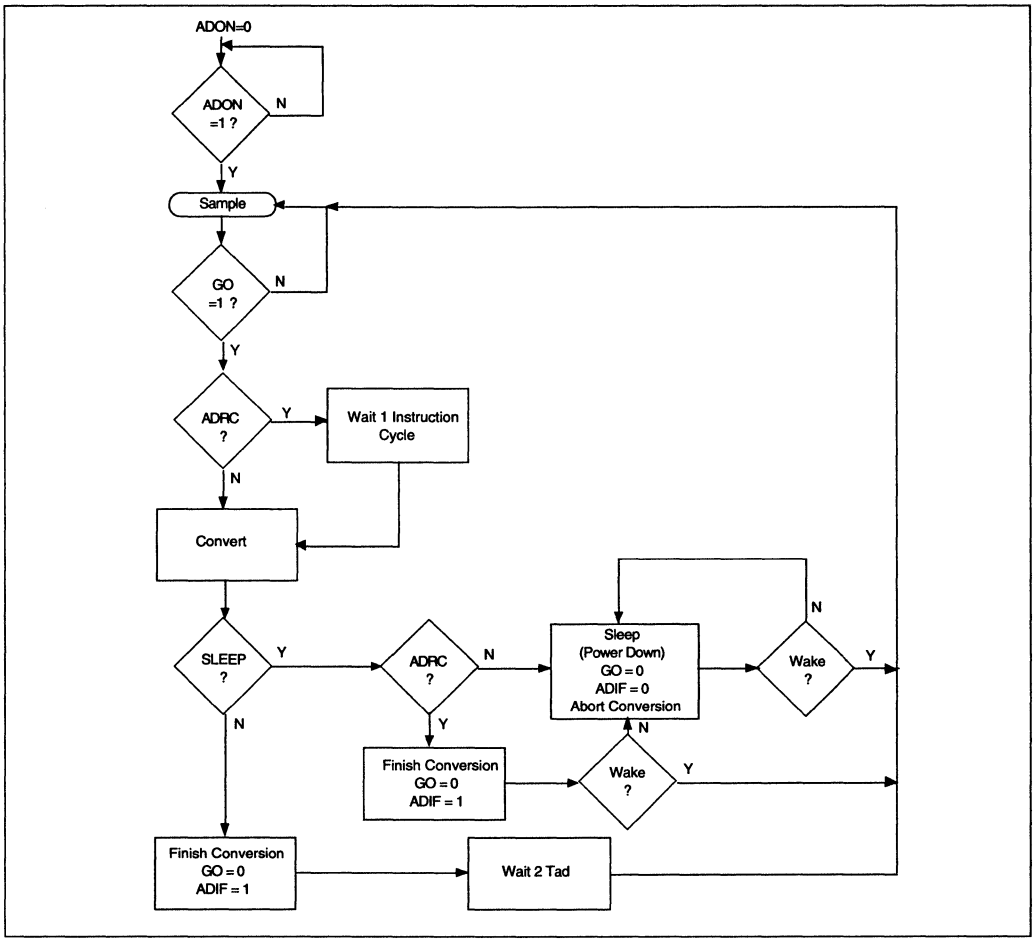


FIGURE 13.7 - SUMMARY OF A/D REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B / 8B	INTCON	GIE	PEIE	RTIE	INTE	RBIE	RTIF	INTF	RBIF
0C	PIR1	PSPIF	ADIF	RXIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
8C	PIE1	PSPIE	ADIE	RXIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
OD	PIR2	–	–	–	–	–	–	–	CCP2IF
8D	PIE2	–	–	–	–	–	–	–	CCP2IE
1E	ADRES	A/D Result Register							
1F	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	–	ADON
8F	ADCON1	–	–	–	–	–	PCFG2	PCFG1	PCFG0
05	PORTA	PortA Data Latch when written to, PortA when read							
85	TRISA	PortA Data Direction latch							
09	PORTE	PortE Data Latch when written to, PortA when read							
89	TRISE	PortE Data Direction latch							

14.0 SPECIAL FEATURES OF THE CPU

What sets apart a microcontroller from other processors are special circuits to deal with the needs of real time applications. The PIC16CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

1. OSC selection
2. Reset
   - Power-On Reset (POR)
   - Power-Up Timer (PWRT)
   - Oscillator Start-Up Timer (OST)
3. Interrupts
4. Watchdog Timer (WDT)
5. SLEEP
6. Code protection
7. In-circuit serial programming

The PIC16CXX has a watchdog timer which can be shut off only through EPROM fuses. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the oscillator start-up timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the power-up timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

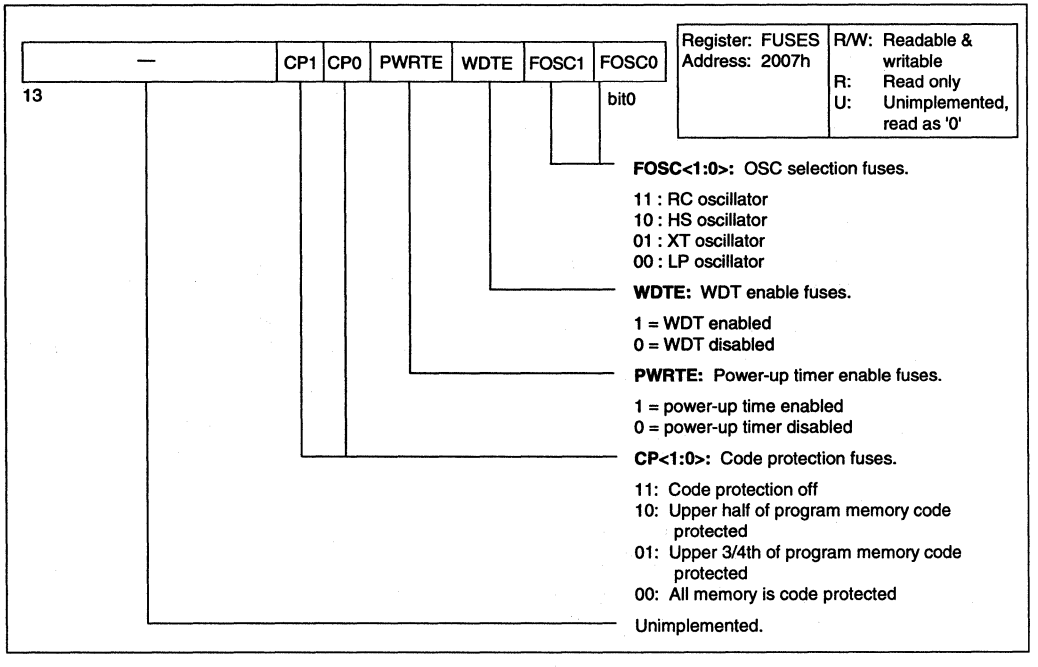
The SLEEP mode is designed to offer a very low current power-down mode. The user can wake up from SLEEP through external reset, watchdog timer time-out or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of EPROM configuration bits (fuses) are used to select various options.

14.1 Configuration Fuses

The PIC16CXX has six configuration fuses which are EPROM bits. These fuses can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed during programming.

FIGURE 14-1: CONFIGURATION WORD



14.2 Oscillator Configurations

14.2.1 OSCILLATOR TYPES

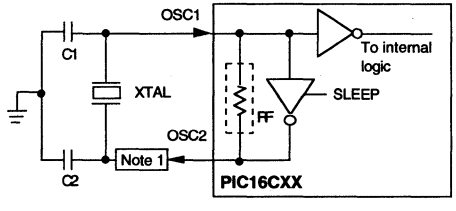
The PIC16CXX can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal
- HS High Speed Crystal
- RC Resistor/Capacitor

14.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 14-2). The PIC16CXX Oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin. This is shown in Figure 14-3.

FIGURE 14-2: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Tables 14-1 and 14-2 for recommended values of C1 and C2.

Note 1: A series resistor may be required for AT strip cut crystals.

FIGURE 14-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP OSC CONFIGURATION)

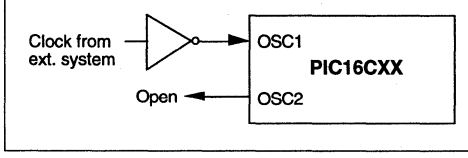


TABLE 14-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	150 - 330 pF
	2.0 MHz	20 - 330 pF
	4.0 MHz	20 - 330 pF
HS	8.0 MHz	20 - 200 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 14-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz§	15 pF	15 pF
	100 KHz	15 pF	15 pF
	200 KHz	0 - 15 pF	0 - 15 pF
XT	100 KHz	15 - 30 pF	200 - 300 pF
	200 KHz	15 - 30 pF	100 - 200 pF
	455 KHz	15 - 30 pF	15 - 100 pF
	1 MHz	15 - 30 pF	15 - 30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

§ For V_{DD} > 4.5V, C1 = C2 ≃ 30pf is recommended.

14.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance, or one with parallel resonance.

Figure 14-4 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 14-4: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

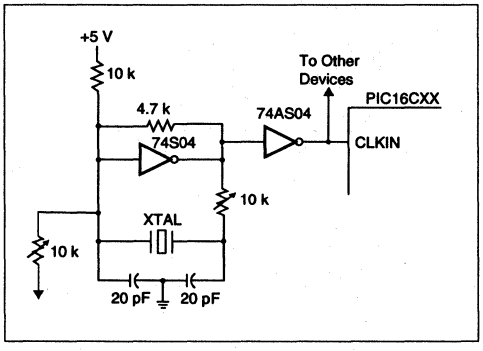
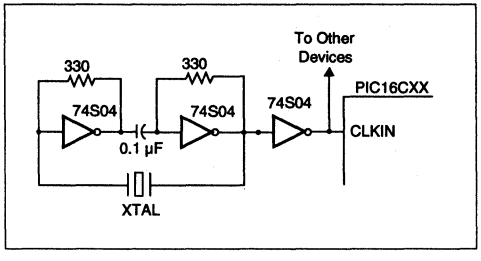


Figure 14-5 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330-Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 14-5 : EXTERNALSERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



14.2.4 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 14-6 shows how the R/C combination is connected to the PIC16CXX. For Rext values below 2.2 kOhm, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 kOhm and 100 kOhm.

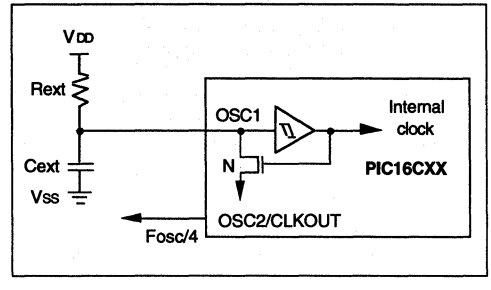
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 17.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 17.0 for variation of oscillator frequency due to V_{DD} for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and V_{DD} values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-2 for waveform).

FIGURE 14-6: RC OSCILLATOR MODE



14.3 Reset

The PIC16CXX differentiates between various kinds of reset:

a) Power-on reset (POR)
b) $\overline{MCLR}$ Reset during normal operation
c) $\overline{MCLR}$ reset during SLEEP
d) WDT time-out reset during normal operation
e) WDT time-out reset during SLEEP

Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on power-on reset (POR), on $\overline{MCLR}$ or WDT reset during normal operation and on $\overline{MCLR}$ reset during SLEEP. They are not affected by a WDT reset during SLEEP, since this reset is viewed as the resumption of normal operation. $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations as indicated in Table 14-4. These bits are used in software to determine the nature of reset. See Table 14-6 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 14-7.

14.4 Power-On Reset (POR), Power-Up-Timer (PWRT) and Oscillator Start-up Timer (OST)

14.4.1 Power-On Reset (POR)

A Power-On Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.6V - 1.8V). To take advantage of the POR, just tie $\overline{MCLR}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-On Reset. A minimum rise time for VDD is required. See Electrical Specifications for details.

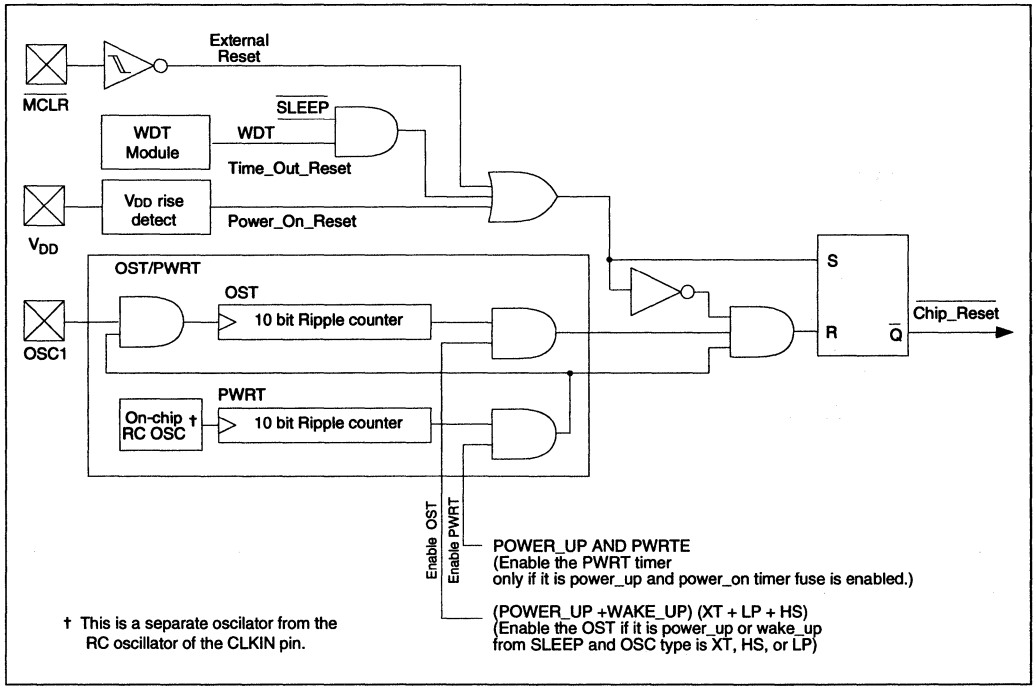
The POR circuit does not produce internal reset when VDD declines.

14.4.2 POWER-UP TIMER (PWRT)

The Power-Up Timer provides a fixed 72ms time-out on power-up only, from POR. The power-up timer operates on an internal RC oscillator. The chip is kept in reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration fuse, PWRTE can enable (if set) or disable (if cleared or programmed) the power-up timer.

The Power-Up Time delay will vary from chip to chip and due to VDD and temperature. See DC parameters for details.

FIGURE 14-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



14.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-Up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This guarantees that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on power-on reset or wake-up from SLEEP.

14.4.4 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and PWRTE fuse status. For example, in RC mode with PWRTE fuse cleared (PWRT disabled), there will be no time-out at all. Figures 14-8 to 14-10 depict time-out sequences.

TABLE 14-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power up		Wake up from SLEEP
	PWRTE = 1	PWRTE = 0	
XT, HS, LP	72 ms + 1024 tosc	1024 tosc	1024 tosc
RC	72 ms	–	–

Since the time-outs occur from POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately (see Figure 14-9). This is useful for testing purposes or to synchronize more than one PIC16CXX device operating in parallel.

Table 14-5 shows the reset conditions for some special registers, while Table 14-6 shows the reset conditions for all the registers.

14.4.1 POWER CONTROL/STATUS REGISTER (PCON)

The power control/status register, PCON (address 8Eh) has only one bit.

Bit1 is $\overline{POR}$ (Power-on-reset). It is cleared on power-on-reset and unaffected otherwise. The user must set this bit following power-on-reset. On a subsequent reset if $\overline{POR}$ is cleared, it will indicate that a Power-On Reset must have occured (V_{DD} may have gone too low).

TABLE 14-4: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{TO}$	$\overline{PD}$	
0	1	1	Power-on-reset
0	0	X	Illegal, $\overline{TO}$ is set on POR
0	X	0	Illegal, $\overline{PD}$ is set on POR
1	0	1	WDT reset during normal operation
1	0	0	WDT timeout wakeup from SLEEP
1	1	1	$\overline{MCLR}$ reset during normal operation
1	1	0	$\overline{MCLR}$ reset during SLEEP or interrupt wake-up from SLEEP

TABLE 14-5: RESET CONDITION FOR SPECIAL REGISTERS

	PCL Addr: 02h	STATUS Addr: 03h	PCON Addr: 8Eh
Power-On Reset	000h	0001 1xxx	---- --0-
$\overline{MCLR}$ reset during normal operation	000h	0001 1uuu	---- --u-
$\overline{MCLR}$ reset during SLEEP	000h	0001 0uuu	---- --u-
WDT reset during normal operation	000h	0000 1uuu	---- --u-
WDT during SLEEP	PC + 1	uuu0 0uuu	---- --u-
Interrupt wake-up from SLEEP	PC + 1 (1)	uuu1 0uuu	---- --u-

Legend: u = unchanged
x = unknown
- = unimplemented bit, reads as '0'

Notes: 1. When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 14-6: RESET CONDITION FOR REGISTERS

Register	Address	• Power-on Reset	• $\overline{MCLR}$ Reset during: - normal operation - SLEEP • WDT timeout during normal operation	• Wake up from SLEEP through interrupt • Wake up from SLEEP through WDT timeout
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	-	-	-
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	02h	0000h	0000h	PC + 1 (2)
STATUS	03h	0001 1xxx	000? ?uuu (3)	uuu? ?uuu (3)
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--xx xxxx	--uu uuuu	--uu uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTE	09h	---- -xxx	---- -uuu	---- -uuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu(1)
PIR1	0Ch	0000 0000	0000 0000	uuuu uuuu(1)
PIR2	0Dh	---- ---0	---- ---0	---- ---u(2)
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	--00 0000	--uu uuuu	--uu uuuu
TMR2	11h	xxxx xxxx	uuuu uuuu	uuuu uuuu
T2CON	12h	-000 0000	-000 0000	-uuu uuuu
SSPBUF	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	14h	0000 0000	0000 0000	uuuu uuuu
CCPR1L	15h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	17h	--00 0000	--00 0000	--uu uuuu
RCSTA	18h	0000 0000	0000 0000	uuuu uuuu
TXREG	19h	xxxx xxxx	uuuu uuuu	uuuu uuuu
RCREG	1Ah	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR2L	1Bh	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR2H	1Ch	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP2CON	1Dh	0000 0000	0000 0000	uuuu uuuu
ADRES	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	1Fh	0000 0000	0000 0000	uuuu uuuu

(Cont.)

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', ? = value depends on condition

Notes:
1. One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).
2. When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
3. See Table 12-5 for reset value for specific condition.

TABLE 14-6: RESET CONDITION FOR REGISTERS (Continued)

Register	Address	• Power-on Reset	• $\overline{MCLR}$ Reset during: - normal operation - SLEEP • WDT timeout during normal operation	• Wake up from SLEEP through interrupt • Wake up from SLEEP through WDT timeout
INDF	80h	-	-	-
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
PC	82h	0000h	0000h	PC + 1
STATUS	83h	0001 1xxx	000? ?uuu (3)	uuu? ?uuu (3)
FSR	84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
TRISC	87h	1111 1111	1111 1111	uuuu uuuu
TRISD	88h	1111 1111	1111 1111	uuuu uuuu
TRISE	89h	0000 -111	0000 -111	uuuu -uuu
PCLATH	8Ah	---0 0000	---0 0000	---u uuuu
INTCON	8Bh	0000 000x	0000 000u	uuuu uuuu(1)
PIE1	8Ch	0000 0000	0000 0000	uuuu uuuu
PIE2	8Dh	---- ---0	---- ---0	---- ---u
PCON	8Eh	---- --0-	---- --u-	---- --u-
PR2	92h	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPADD	93h	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	94h	--00 0000	--00 0000	--uu uuuu
TXSTA	98h	0000 0000	0000 0000	uuuu uuuu
SPBRG	99h	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1	9Fh	---- -000	---- -000	---- -uuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', ? = value depends on condition

Notes:
1. One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).
2. When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
3. See Table 12-5 for reset value for specific condition.

FIGURE 14-8 : TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD): Case 1

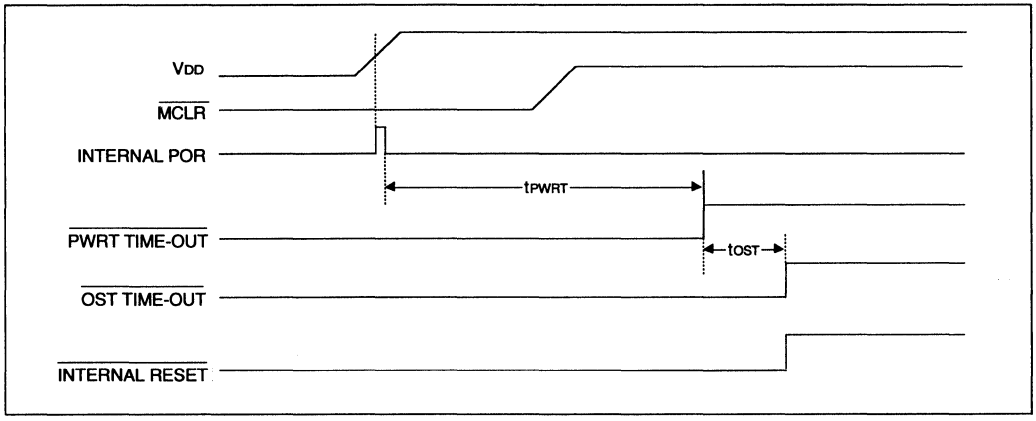


FIGURE 14-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD): Case 2

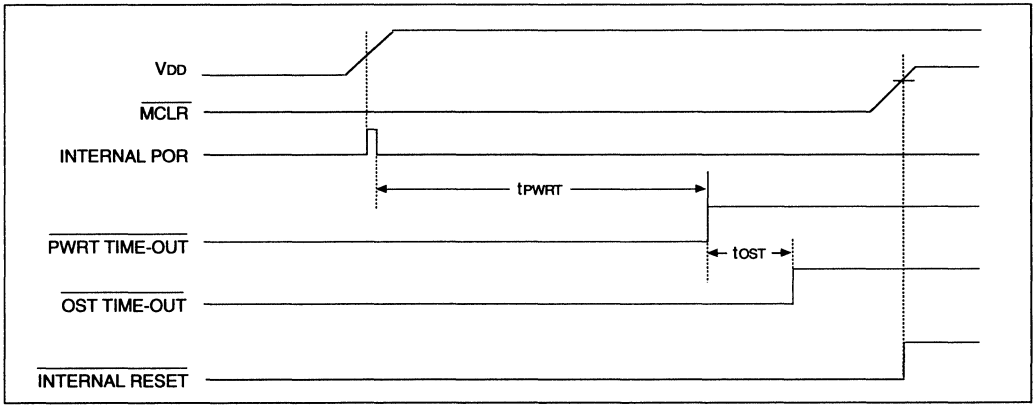


FIGURE 14-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD)

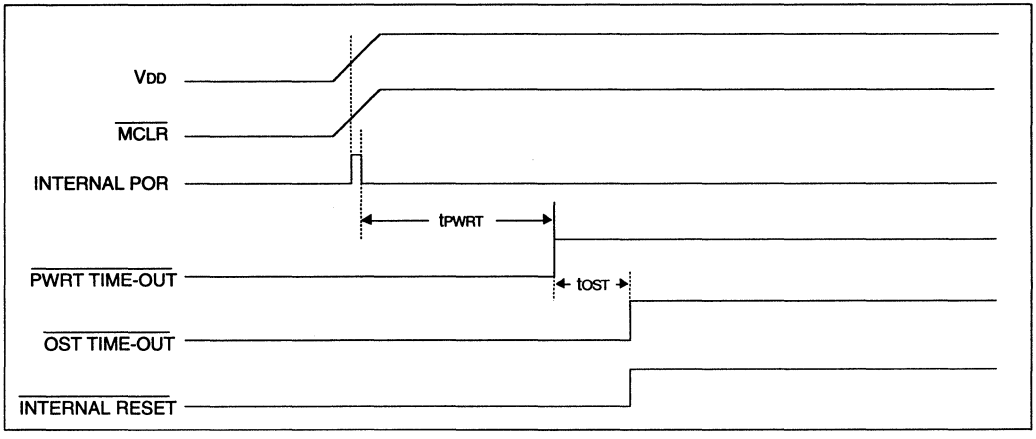
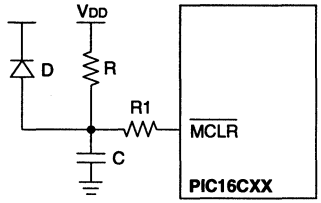
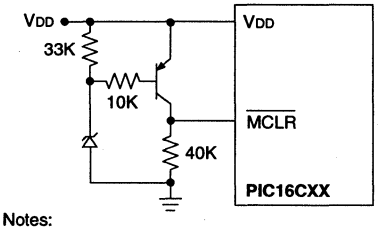


FIGURE 14-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



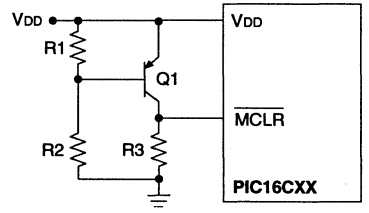
Notes:
1. External power-on reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40KΩ is recommended to make sure that voltage drop across R does not exceed 0.2V (max leakage current spec on $\overline{MCLR}$ pin is 5μA). A larger voltage drop will degrade VIH level on $\overline{MCLR}$ pin.
3. R1 = 100Ω to 1KΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$ pin breakdown due to ESD or EOS.

FIGURE 14-12: BROWN-OUT PROTECTION CIRCUIT 1



Notes:
1. This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

FIGURE 14-13: BROWN-OUT PROTECTION CIRCUIT 2



Notes:
1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V.$$

14.5 Interrupts

The PIC16C74 has 12 sources of interrupt:

- External interrupt RB0/INT
- RTCC timer/counter overflow interrupt
- PortB change interrupts (pins RB<7:4>)
- Timer1 overflow interrupt
- Timer2 interrupt
- CCP1 interrupt
- CCP2 interrupt
- SCI asynchronous transmit and receive
- Sync serial port interrupt
- SCI interrupt
- A/D interrupt
- Microprocessor port read/write interrupt

The interrupt control register (INTCON, addr 0Bh) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. GIE is cleared on reset.

The `RETFIE` instruction allows user to return from interrupt and enable interrupt at the same time.

The INT pin interrupt, the RB port change interrupt and the RTCC overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the special register PIR1 (0Ch). The corresponding interrupt enable bits are contained in special registers PIE1 (8Ch).

When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

Note 1: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

Note 2: If an interrupt occurs while the Global Interrupt Enable (GIE) bit is being cleared, the GIE bit may unintentionally be re-enabled by the user's Interrupt Service Routine (the `RETFIE` instruction). The events that would cause this to occur are:

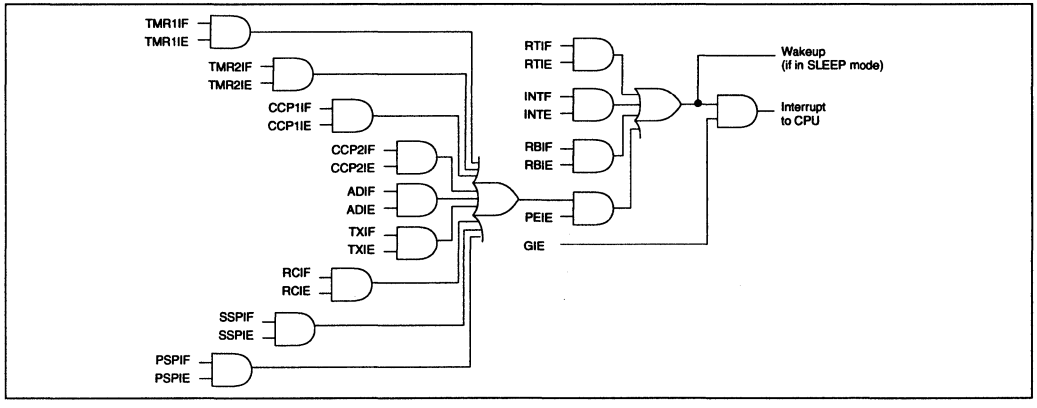
1. An instruction clears the GIE bit while an interrupt is acknowledged
2. The program branches to the interrupt vector and executes the Interrupt Service Routine.
3. The Interrupt Service Routine completes with the execution of the `RETFIE` instruction. This causes the GIE bit to be set (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.

The method to ensure that interrupts are globally disabled is:

1. Ensure that the GIE bit was cleared by the instruction, as shown in the following code:

```
LOOP  BCF    INTCON, GIE ; Disable Global
                         ;  Interrupts
      BTFSC  INTCON, GIE ; Global Inter-
rupts                    ;  Disabled?
      GOTO   LOOP        ; NO, try again
      :                  ; Yes, continue
                         ;  with program
                         ;  flow
```

FIGURE 14-14: INTERRUPT LOGIC



14.5.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake up the processor from SLEEP, if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 14.8 for details on SLEEP and Figure 14-16 for timing of wake-up from SLEEP through INT interrupt.

14.5.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the TMR0 module, see Section 7.0.

14.5.3 PORT RB INTERRUPT

An input change on PortB <7:4> sets the RBIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the RBIE (INTCON<4>) bit. For operation of PortB, see Section 5.2.

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not be set.

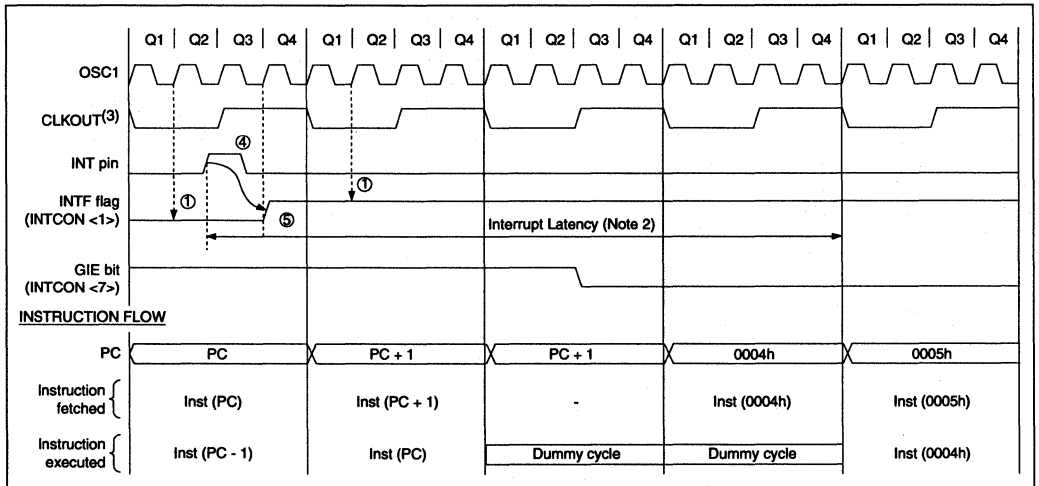
14.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt e.g. W register and status register. This will have to be implemented in software.

EXAMPLE 14-1: SAVING W REGISTER AND STATUS IN RAM:

```
push:  movwf   temp_w       ;Saving Values
       swapf   STATUS,W     ;
       movwf   temp_stat    ;
       :                    ;Interrupt
       :                    ; Service Routine
pop:   swapf   temp_stat,W  ;Restoring
                            ;  Values
       movwf   STATUS       ;
       swapf   temp_w, F    ;Do not want to
       swapf   temp_w, W    ; affect Z-bit
```

FIGURE 14-15: INT PIN INTERRUPT TIMING



Notes:
1. INTF flag is sampled here (every Q1)
2. Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time.
   Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3. CLKOUT is available only in RC oscillator mode.
4. For minimum width spec of INT pulse, refer to AC specs.
5. INTF is enabled to be set anytime during the Q4-Q1 cycles.

14.7 Watchdog Timer (WDT)

The watchdog timer is realized as a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT timeout generates a device RESET. If the device is in SLEEP mode, a WDT timeout causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration fuse WDTE as a '0' (Section 14.1).

14.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a watchdog timer time-out.

14.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

2

FIGURE 14-16: WATCHDOG TIMER BLOCK DIAGRAM

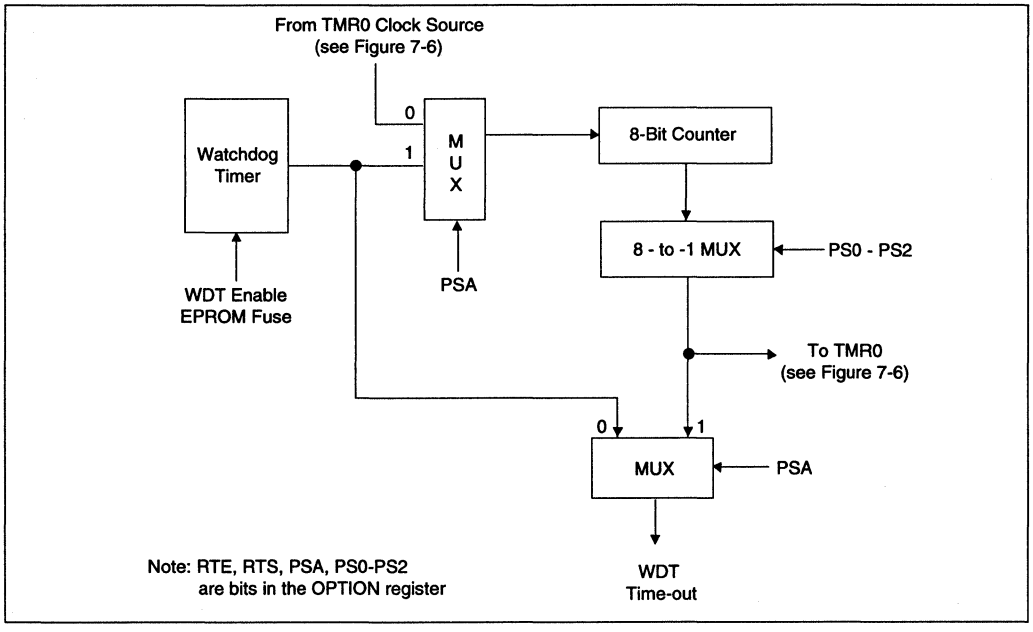


FIGURE 14-17: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007	Config. Fuses	—	—	CPI	CP0	PWRTE	WDTE	FOSC1	FOSC0
81	OPTION	RBPU	INTEDG	RTS	RTE	PSA	PS2	PS1	PS0

14.8 Power-Down Mode (SLEEP)

The Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{PD}$ bit in the STATUS register is cleared, the $\overline{TO}$ bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low, or hi-impedance).

For lowest curent consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are hi-impedence inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC input should also be at VDD or VSS for lowest current consumption. The contribution from on chip pull-ups on PortB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (VIHMC).

It should be noted that a RESET generated by a WDT time-out does not drive $\overline{MCLR}$ pin low.

14.8.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. External reset input on $\overline{MCLR}$ pin
2. Watchdog timer time-out reset (if WDT was enabled)
3. Interrupt from INT pin, RB port change, TMR0 overflow, or some Peripheral Interrupts.

The following peripheral interrupts can wake-up from SLEEP:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. SSP Start/Stop bit detect interrupt.
3. CCP capture mode interrupt.
4. Slave port read or write.

Other peripherals can not generate interrupts since during SLEEP, no on-chip Q clocks are present.

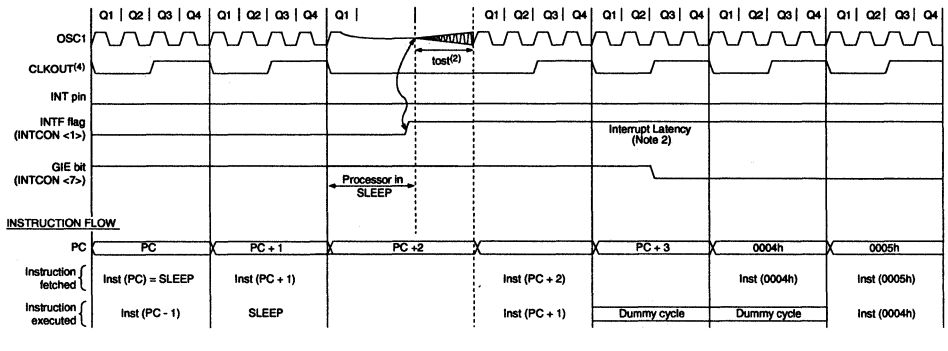
The first event will cause a device reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. $\overline{PD}$ bit, which is set on power-up is cleared when SLEEP is invoked. $\overline{TO}$ bit is cleared if WDT time-out occurred (and caused wake-up).

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and the branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

Note: If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake from sleep.

The WDT is cleared when the device wakes-up from sleep, regardless of the source of wake-up.

FIGURE 14-18: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Notes:
1. XT, HS or LP oscillator mode assumed
2. tost = 1024 tosc (drawing not to scale). This delay will not be there for RC osc mode.
3. GIE = 1 assumed. In this case after wake up processor jumps to interrupt routine. If GIE = 0, execution will continue in line.
4. CLKOUT is not available in these osc modes, but shown here for timing reference.

14.9 Code Protection

The code in the program memory can be protected by blowing the code protect fuses (CP<1:0>).

When code protected, the contents of the program memory cannot be read out in a way that the program code can be reconstructed.

In code-protected mode, the configuration word (2007h) will not be scrambled, allowing reading of all fuses.

14.9.1 CODE PROTECTION FUSES:

The PIC16/17 microcontroller code protection scheme has been enhanced. These enhancements allow the user to selectively code protect portions of the program memory. The two code protect fuses (CP<1:0>) allow the selection of the following code protection mappings:

11 Program memory not code protected
01 Upper 3/4 of program memory code protected (3FF - 0FFFh)
10 Upper 1/2 of program memory code protected (7FF - 0FFFh)
00 Entire program memory code protected

Any word of a protected memory section will read out a scrambled version as shown in Figure 14-19:

FIGURE 14-19: PROTECTED MEMORY READ FORMAT

13				7	6						0
0	0	0	0	0	0	0	b6	b5	b4	b3	b2	b1	b0

where b0 = XNOR of bit0 and bit7 of the program memory location.
b1 = XNOR of bit1 and bit8 of the programmemory location.
•
•
•
b6 = XNOR of bit6 and bit13 of the program.

The configuration word is not code protected, and therefore no scrambling is done. Unprotected segments read normally. Once the program memory location(s) have been code protected, those memory locations can not be further programmed.

14.9.2 VERIFYING A CODE-PROTECTED PART

When code protected, verifying any program memory location will read a scrambled output which looks like "0000000xxxxxxx" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

1. First, program and verify a good device without code protecting it.
2. Next, blow its code protection fuse and then load its contents in a file.
3. Verify any code-protected PIC16C74 against this file.

14.10 In-Circuit Serial Programming

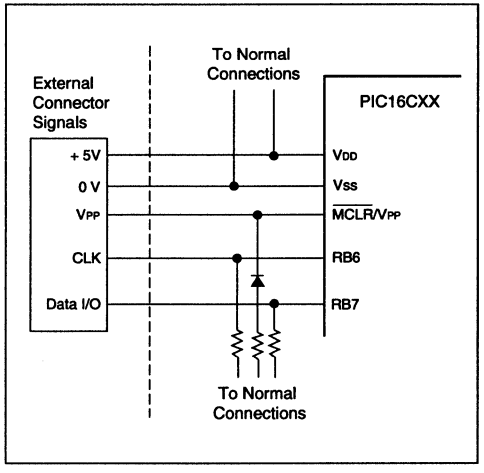
The PIC16CXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and date, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low while raising the MCLR (Vpp) pin from Vil to Vihh. RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are schmidt trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program date are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X Programming Specifications (Literature #DS30228).

A typical in-system serial programming connection is shown in Figure 14-20.

FIGURE 14-20: TYPICAL IN-SYSTEM SERIAL PROGRAMMING CONNECTION



15.0 INSTRUCTION SET SUMMARY

Each PIC16CXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 15-2 lists byte-oriented, bit-oriented, and literal and control operations. Table 15-1 shows the opcode field descriptions.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which file register is to be utilized by the instruction.

The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or eleven bit constant or literal value.

TABLE 15-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8 bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
PCLATH	Program Counter High Latch
GIE	Global Interrupt Enable Bit
WDT	Watchdog Timer Counter
$\overline{TO}$	Time-out Bit
$\overline{PD}$	Power-down Bit
dest	Destination either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term

The instruction set is highly orthogonal and is grouped into three basic categories:

- Byte oriented operations
- Bit oriented operations
- Literal and control operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Table15-2 lists the instructions recognized by the MPASM assembler.

Figure 15-1 shows the three general formats that the instructions can have.

Note: To maintain upward compatibility with future PIC16CXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexidecimal number:

0xhh

where h signifies a hexidecimal digit.

FIGURE 15-1: GENERAL FORMAT FOR INSTRUCTIONS

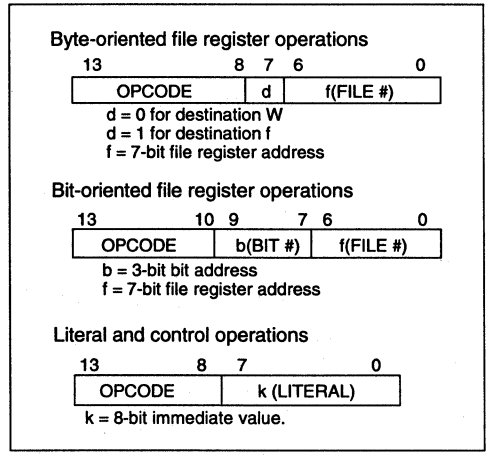


TABLE 15-2: INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode msb	lsb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS							
ADDWF	f, d	Add W and f	1	00	0111 dfff ffff	C, DC, Z	1, 2
ANDWF	f, d	AND W and f	1	00	0101 dfff ffff	Z	1, 2
CLRF	f	Clear f	1	00	0001 1fff ffff	Z	2
CLRW	-	Clear W	1	00	0001 0xxx xxxx	Z	
COMF	f, d	Complement f	1	00	1001 dfff ffff	Z	1, 2
DECF	f, d	Decrement f	1	00	0011 dfff ffff	Z	1, 2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011 dfff ffff		1, 2, 3
INCF	f, d	Increment f	1	00	1010 dfff ffff	Z	1, 2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111 dfff ffff		1, 2, 3
IORWF	f, d	Inclusive OR W and f	1	00	0100 dfff ffff	Z	1, 2
MOVF	f, d	Move f	1	00	1000 dfff ffff	Z	1, 2
MOVWF	f	Move W to f	1	00	0000 1fff ffff		
NOP	-	No Operation	1	00	0000 0xx0 0000		
RLF	f, d	Rotate left f through carry	1	00	1101 dfff ffff	C	1, 2
RRF	f, d	Rotate right f through carry	1	00	1100 dfff ffff	C	1, 2
SUBWF	f, d	Subtract W from f	1	00	0010 dfff ffff	C, DC, Z	1, 2
SWAPF	f, d	Swap halves f	1	00	1110 dfff ffff		1, 2
XORWF	f, d	Exclusive OR W and f	1	00	0110 dfff ffff	Z	1, 2
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF	f, b	Bit Clear f	1	01	00bb bfff ffff		1, 2
BSF	f, b	Bit Set f	1	01	01bb bfff ffff		1, 2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS							
ADDLW	k	Add literal to W	1	11	111x kkkk kkkk	C, DC, Z	
ANDLW	k	AND literal to W	1	11	1001 kkkk kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk kkkk kkkk		
CLRWDT	-	Clear watchdog timer	1	00	0000 0110 0100	$\overline{TO}$, $\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk kkkk kkkk		
IORLW	k	Inclusive OR literal to W	1	11	1000 kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx kkkk kkkk		
RETFIE	-	Return from interrupt	2	00	0000 0000 1001		
RETLW	k	Return with literal in W	2	11	01xx kkkk kkkk		
RETURN	-	Return from subroutine	2	00	0000 0000 1000		
SLEEP	-	Go into standby mode	1	00	0000 0110 0011	$\overline{TO}$, $\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x kkkk kkkk	C, DC, Z	
XORLW	k	Excl. OR literal to W	1	11	1010 kkkk kkkk	Z	

Notes: 1. When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2. If this instruction is executed on the TMR0 register (and, where applicable, d=1), the prescaler will be cleared if assigned to the TMR0.

3. If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

15.1 Instruction Descriptions

ADDLW Add Literal to W

Syntax: [*label*] ADDLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) + k → W

Status Affected: C, DC, Z

Encoding:

11	111X	kkkk	kkkk

Description: The contents of the W register are added to the eight bit literal "k" and the result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ADDLW   0x15
```
Before Instruction
W = 0x10

After Instruction
W = 0x25

ANDLW AND Literal and W

Syntax: [*label*] ANDLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .AND. (k) → W

Status Affected: Z

Encoding:

11	1001	kkkk	kkkk

Description: The contents of W register are AND'ed with the eight bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ANDLW   0x5F
```
Before Instruction
W = 0xA3

After Instruction
W = 0x03

ADDWF ADD W to f

Syntax: [*label*] ADDWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

00	0111	dfff	ffff

Description: Add the contents of the W register to register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
ADDWF   FSR, 0
```
Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0xD9
FSR = 0xC2

ANDWF AND W with f

Syntax: [*label*] ANDWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (W) .AND. (f) → dest

Status Affected: Z

Encoding:

00	0101	dfff	ffff

Description: AND the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
ANDWF   FSR, 1
```
Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0x17
FSR = 0x02

BCF Bit Clear f

Syntax: [*label*] BCF f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: 0 → f<b>

Status Affected: None

Encoding:

01	00bb	bfff	ffff

Description: Bit "b" in register "f" is reset to 0.

Words: 1

Cycles: 1

Example:
```
BCF     FLAG_REG, 7
```
Before Instruction
FLAG_REG = 0xC7

After Instruction
FLAG_REG = 0x47

BSF Bit Set f

Syntax: [*label*] BSF f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: 1 → f<b>

Status Affected: None

Encoding:

01	01bb	bfff	ffff

Description: Bit "b" in register "f" is set to 1.

Words: 1

Cycles: 1

Example:
```
BSF     FLAG_REG, 7
```
Before Instruction
FLAG_REG = 0x0A

After Instruction
FLAG_REG = 0x8A

BTFSC Bit Test, skip if Clear

Syntax: [*label*] BTFSC f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

01	10bb	bfff	ffff

Description: If bit 'b' in register 'f' is '0' then the next instruction is skipped.

If bit 'b' is '0', the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address HERE

After Instruction
if FLAG<1> = 0, PC = address TRUE
if FLAG<1> = 1, PC = address FALSE

BTFSS Bit Test, skip if Set

Syntax: [*label*] BTFSS f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

01	11bb	bfff	ffff

Description: If bit "b" in register "f" is "1" then the next instruction is skipped.

If bit '"b" is "0", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

Words: 1

Cycles: 1 (2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address HERE

After Instruction
if FLAG<1> = 0, PC = address FALSE
if FLAG<1> = 1,PC = address TRUE

CALL — Subroutine Call

Syntax: [*label*] CALL k

Operands: 0 ≤ k ≤ 2048

Operation: (PC) + 1 → TOS,
k → PC<10:0>,
(PCLATH<4:3>) → PC<12:11>;

Status Affected: None

Encoding:

10	0kkk	kkkk	kkkk

Description: Subroutine call. First, return address (PC + 1) is pushed onto the stack. The eleven bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH (f03). CALL is a two cycle instruction.

Words: 1

Cycles: 2

Example:
```
HERE    CALL    THERE
```
Before Instruction
PC = Address HERE

After Instruction
PC = Address THERE
TOS = Address HERE

CLRF — Clear f

Syntax: [*label*] CLRF f

Operands: 0 ≤ f ≤ 127

Operation: 00h → f
1 → Z

Status Affected: Z

Encoding:

00	0001	1fff	ffff

Description: The contents of register "f" are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example:
```
CLRF    FLAG_REG
```
Before Instruction
FLAG_REG = 0x5A

After Instruction
FLAG_REG = 0x00
Z = 1

CLRW — Clear W Register

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W)
1 → Z

Status Affected: Z

Encoding:

00	0001	0XXX	XXXX

Description: W registered is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example:
```
CLRW
```
Before Instruction
W = 0x5A

After Instruction
W = 0x00
Z = 1

CLRWDT — Clear Watchdog Timer

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0100

Description: CLRWDT instruction resets the watchdog timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example:
```
CLRWDT
```
Before Instruction
WDT counter = ?

After Instruction
WDT counter = 0x00
WDT prescale = 0
$\overline{TO}$ = 0
$\overline{PD}$ = 0

COMF Complement f

Syntax: [*label*] COMF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: $\overline{(f)} \rightarrow$ (dest)

Status Affected: Z

Encoding:

00	1001	dfff	ffff

Description: The contents of register "f" are complemented. If "d" is 0 the result is stored in W. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
COMF    REG1, 0
```
Before Instruction
REG1 = 0x13
After Instruction
REG1 = 0x13
W = 0xEC

DECF Decrement f

Syntax: [*label*] DECF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f)-1 → (dest)

Status Affected: Z

Encoding:

00	0011	dfff	ffff

Description: Decrement register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
DECF    CNT, 1
```
Before Instruction
CNT = 0x01
Z = 0
After Instruction
CNT = 0x00
Z = 1

DECFSZ Decrement f, skip if 0

Syntax: [*label*] DECFSZ f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - 1 → d; skip if result = 0

Status Affected: None

Encoding:

00	1011	dfff	ffff

Description: The contents of register "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1 (2)

Example:
```
HERE    DECFSZ    CNT, 1
        GOTO      LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address HERE
After Instruction
CNT = CNT - 1
if CNT = 0, PC = address CONTINUE
if CNT ≠ 0, PC = address HERE + 1

GOTO Unconditional Branch

Syntax: [*label*] GOTO k

Operands: $0 \le k \le 2048$

Operation: k → PC<10:0>,
(PCLATH<4:3>) → PC<12:11>

Status Affected: None

Encoding:

10	1kkk	kkkk	kkkk

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH <4:3>. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Example:
```
GOTO THERE
```
After Instruction
PC = Address of THERE

INCF — Increment f

Syntax: [*label*] INCF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) + 1 → (dest)

Status Affected: Z

Encoding:

00	1010	dfff	ffff

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

Words: 1

Cycles: 1

Example:
```
INCF    CNT, 1
```
Before Instruction
CNT = 0xFF
Z = 0

After Instruction
CNT = 0x00
Z = 1

INCFSZ — Increment f, skip if 0

Syntax: [*label*] INCFSZ f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) + 1 → (dest), skip if result = 0

Status Affected: None

Encoding:

00	1111	dfff	ffff

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1 (2)

Example:
```
HERE    INCFSZ  CNT, 1
        GOTO    LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address HERE

After Instruction
CNT = CNT + 1
if CNT = 0, PC = address CONTINUE
if CNT ≠ 0, PC = address HERE + 1

IORLW — Inclusive OR Literal with W

Syntax: [*label*] IORLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .OR. (k) → (W)

Status Affected: Z

Encoding:

11	1000	kkkk	kkkk

Description: The contents of the W register are OR'ed with the eight bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
IORLW   0x35
```
Before Instruction
W = 0x9A

After Instruction
W = 0xBF

IORWF — Inclusive OR W with f

Syntax: [*label*] IORWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (W) .OR. (f) → (dest)

Status Affected: Z

Encoding:

00	0100	dfff	ffff

Description: Inclusive OR the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
IORWF   RESULT, 0
```
Before Instruction
RESULT = 0x13
W = 0x91

After Instruction
RESULT = 0x13
W = 0x93

MOVLW **Move Literal to W**

Syntax: [*label*] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (W)

Status Affected: None

Encoding:

11	00XX	kkkk	kkkk

Description: The eight bit literal "k" is loaded into W register.

Words: 1

Cycles: 1

Example:
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \le f \le 127$

Operation: (W) → (f)

Status Affected: None

Encoding:

00	0000	1fff	ffff

Description: Move data from W register to register "f".

Words: 1

Cycles: 1

Example:
```
MOVWF   OPTION
```
Before Instruction
OPTION = 0xFF
W = 0x4F

After Instruction
OPTION = 0x4F
W = 0x4F

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Encoding:

00	1000	dfff	ffff

Description: The contents of register f is moved to destination d. If d=0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example:
```
MOVF    FSR, 0
```
After Instruction
W = value in FSR register

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

00	0000	0XX0	0000

Description: No operation

Words: 1

Cycles: 1

Example:
```
NOP
```

OPTION **Load Option Register**

Syntax: [*label*] OPTION

Operands: None

Operation: W → OPTION;

Status Affected: None

Encoding:

00	0000	0110	0010

Description: The contents of the W register is loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.

Words: 1

Cycles: 1

Example:

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

RETFIE **Return from Interrupt**

Syntax: [*label*] RETFIE

Operands: None

Operation: TOS → PC,
1 → GIE;

Status Affected: None

Encoding:

00	0000	0000	1001

Description: Return from Interrupt. Stack is popped and Top of the Stack (TOS) is loaded in PC. Interrupts are enabled by setting the GIE bit. GIE is the global interrupt enable bit (INTCON<7>). This is a two cycle instruction.

Words: 1

Cycles: 2

Example: `RETFIE`

After Interrupt
PC = TOS
GIE = 1

RETLW **Return Literal to W**

Syntax: [*label*] RETLW k

Operands: $0 \le k \le 255$

Operation: k → W; TOS → PC;

Status Affected: None

Encoding:

11	01XX	kkkk	kkkk

Description: The W register is loaded with the eight bit literal "k". The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

Words: 1

Cycles: 2

Example:

```
      CALL  TABLE ; W contains table offset
                  ; value
      •           ; W now has table value
      •
      •
TABLE ADDWF PC    ; W = offset
      RETLW k1    ; Begin table
      RETLW k2    ;
      •
      •
      •
      RETLW kn    ; End of table
```

Before Instruction
W = 0x07

After Instruction
W = value of k7

RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: TOS → PC;

Status Affected: None

Encoding:

00	0000	0000	1000

Description: Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

Words: 1

Cycles: 2

Example: `RETURN`

After Interrupt
PC = TOS

RLF — Rotate Left f through Carry

Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

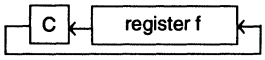
Operation: f<n> → d<n+1>, f<7> → C, C → d<0>;

Status Affected: C

Encoding:

00	1101	dfff	ffff

Description: The contents of register "f" are rotated one bit to the left through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is stored back in register "f".



Words: 1

Cycles: 1

Example:
```
RLF     REG1,0
```
Before Instruction
REG1 = 11100110
C = 0

After Instruction
REG1 = 11100110
W = 11001100
C = 1

RRF — Rotate Right f through Carry

Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

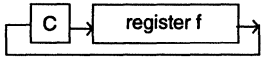
Operation: f<n> → d<n-1>,
f<0> → C,
C → d<7>;

Status Affected: C

Encoding:

00	1100	dfff	ffff

Description: The contents of register "f" are rotated one bit to the right through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".



Words: 1

Cycles: 1

Example:
```
RRF     REG1,0
```
Before Instruction
REG1 = 11100110
C = 0

After Instruction
REG1 = 11100110
W = 01110011
C = 1

SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0011

Description: The power down status bit ($\overline{PD}$) is cleared. Time-out status bit ($\overline{TO}$) is set. Watchdog Timer and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP mode for more details.

Words: 1

Cycles: 1

Example:
```
SLEEP
```

SUBLW — Subtract W from Literal

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Encoding:

11	110X	kkkk	kkkk

Description: The W register is subtracted (2's complement method) from the eight bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example 1:
```
SUBLW     0X02
```
Before Instruction
W = 1
C = ?
After Instruction
W = 1
C = 1 ; result is positive

Example 2: Before Instruction
W = 3
C = ?

After Instruction
W = FF
C = 0 ; result is negative

SUBWF Subtract W from f

Syntax: [*label*] SUBWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f)-(W) → (dest)

Status Affected: C, DC, Z

Encoding:

00	0010	dfff	ffff

Description: Subtract (2's complement method) the W register from register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example 1:
```
SUBWF  REG1,1
```
Before Instruction
REG1 = 0
W = 1
C = ?
After Instruction
REG1 = FF
W = 1
C = 0 ; result is negative

Example 2: Before Instruction
REG1 = FF
W = 0
C = ?
After Instruction
REG1 = FF
W = 0
C = 1 ; result is positive

TRIS Load TRIS Register

Syntax: [*label*] TRIS f

Operands: 5 ≤ f ≤ 7

Operation: W → TRIS register f;

Status Affected: None

Encoding:

00	0000	0110	0fff

Description: This instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.

Words: 1

Cycles: 1

Example:

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

SWAPF Swap f

Syntax: [*label*] SWAPF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: f<0:3> → d<4:7>,
f<4:7> → d<0:3>;

Status Affected: None

Encoding:

00	1110	dfff	ffff

Description: The upper and lower nibbles of register "f" are exchanged. If "d" is 0 the result is placed in W register. If "d" is 1 the result is placed in register "f".

Words: 1

Cycles: 1

Example:
```
SWAPF  REG, 0
```
Before Instruction
REG = 0xA5
After Instruction
REG = 0xA5
W = 0x5A

XORLW Exclusive OR literal with W

Syntax: [*label*] XORLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

11	1010	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the eight bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
XORLW  0xAF
```
Before Instruction
W = 0xB5
After Instruction
W = 0x1A

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 128$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected Z

Encoding:

00	0110	dfff	ffff

Description: Exclusive OR the contents of the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
XORWF  REG, 1
```
Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

2

16.0 DEVELOPMENT SUPPORT

16.1 Development Tools

The PIC16C5X and PIC16CXX microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER™ Real-Time In-Circuit Emulator
- PRO MATE™ Universal Programmer
- PICSTART™ Low-Cost Prototype Programmer
- Assembler
- Software Simulator

16.2 PICMASTER™: High Performance Universal In-Circuit Emulator

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X, PIC16CXX and PIC17CXX families.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16C5X, PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on PC compatible machines ranging from 80286-AT® class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.1 environment, allowing the operator access to a wide range of supporting software and accessories.

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.1 environment was chosen to best make these features available to you, the end user.

The PICMASTER Emulator Universal System consists primarily of four major components:

- Host-Interface Card
- Emulator Control Pod
- Target-Specific Emulator Probe
- PC Host Emulation Control Software

The Windows 3.1 System is a multitasking operating system which will allow the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window.

Dynamic Data Exchange (DDE), a feature of Windows 3.1, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

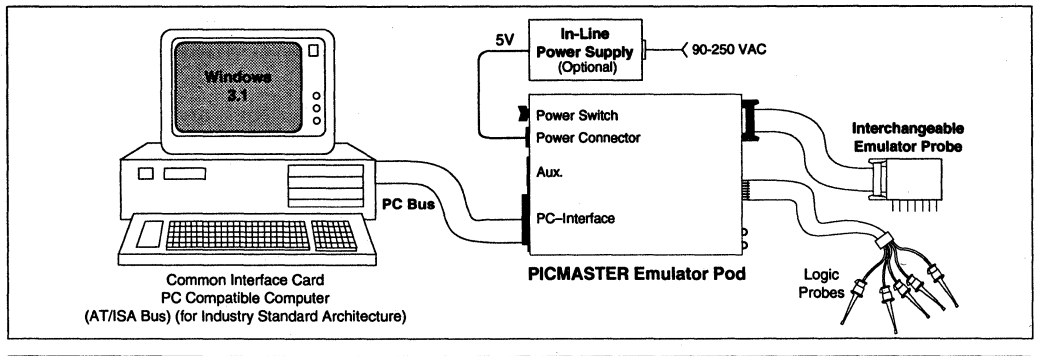
Under Windows 3.1, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16CXX processor and a PIC17CXX processor).

16.3 PRO MATE™: Universal Programmer

The PRO MATE Universal Programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MATE has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability . It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MATE can read, verify or program PIC16C5X, PIC16CXX and PIC17CXX devices. It can also set fuse configuration and code-protect in this mode. Its EEPROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.

FIGURE 16-1: PICMASTER SYSTEM CONFIGURATION



In PC-hosted mode, the PRO MATE connects to the PC via one of the COM (RS232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of VDD min, VDD max and VPP levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different serial number, sequential or random.

The PRO MATE has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. PRO MATE supports all PIC16C5X, PIC16CXX and PIC17CXX processors.

16.4 PICSTART™ Programmer

The PICSTART™ programmer is an easy to use, very low-cost prototype programmer. It connects to the PC via one of the COM (RS232) ports. A PC based user interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based.

16.5 Assembler (MPASM)

Cross Assembler is a PC hosted symbolic assembler. It supports all microcontroller series including the PIC16C5X CMOS, PIC16CXX, and PIC17CXX families.

MPASM offers fully featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from the Microchip Universal Emulator System (PICMASTER).

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro Assembly Capability
- Provides Object, Listing, Symbol and special files required for debugging with one of the Microchip Emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a full feature directive language represented by four basic classes of directives:

- **Data Directives** are those that control the allocation of memory and provide a way to refer to data items symbolically, by meaningful names.
- **Listing Directives** control the MPASM listing dis play. They allow the specification of titles and subtitles, page ejects and other listing control.
- **Control Directives** permit sections of conditionally assembled code.
- **Macro Directives** control the execution and data allocation within macro body definitions.

16.6 Software Simulator (MPSIM)

The Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16C5X and PIC16CXX series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in single step, execute until break or in a trace mode. Two forms of symbolic debugging are available: an internal symbol table for disassembling opcodes and the displaying of source code from a listing file. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

16.7 Development Systems

For convenience, the development tools are packaged into comprehensive systems as listed in Table 16-1:

TABLE 16-1: DEVELOPMENT SYSTEM PACKAGES

Item	Name	System Description
1.	PICMASTER™ System	PICMASTER In-Circuit Emulator with your choice of Target Probe, PRO MATE Programmer, Assembler, Software Simulator and Samples.
2.	PICSTART™ System	PICSTART™ Low-Cost Prototype Programmer, Assembler, Software Simulator and Samples

16.8 Probe Specifications

The PICMASTER probes currently meet the following specifications:

PICMASTER PROBE	Devices Supported	PROBE Maximum Frequency	PROBE Operating Voltage
PROBE - 16F	PIC16C74	10 MHZ	4.5V - 5.5V

18.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to+ 125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss (except VDD and $\overline{MCLR}$) ..... -0.6V to VDD +0.6V
Voltage on VDD with respect toVss ..... 0 to +7.5 V
Voltage on $\overline{MCLR}$ with respect to Vss (Note 2) ..... 0 to +14 V
Total power Dissipation (Note 1) ..... 1.0 W
Maximum Current out of Vss pin 300mA
Maximum Current into VDD pin 250mA
Input clamp current, IIK (VI<0 or VI> VDD) ..... ±20mA
Output clamp current, IOK (V0 <0 or V0>VDD) ..... ±20mA
Maximum Output Current sunk by any I/O pin 25mA
Maximum Output Current sourced by any I/O pin 25mA
Maximum Current sunk by Port A, Port B, and Port E (combined) 200mA
Maximum Current sourced by Port A, Port B, and Port E (combined) 200mA
Maximum Current sunk by Port C and Port D (combined) 200mA
Maximum Current sourced by Port C and Port D (combined) 200mA

Notes: 1. Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ Ioh} + Σ {(VDD-Voh) x Ioh} + Σ(Vol x Iol)

2. Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low' level to the $\overline{MCLR}$ pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

18.1 DC CHARACTERISTICS: PIC16C74-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C74-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ + 125°C for automotive,
-40°C ≤ TA ≤ + 85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD = 4.0V to 6.0V

Characteristic	Sym	Min	Typ †	Max	Units	Conditions
Supply Voltage	VDD	4.0 4.5		6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
RAM Data Retention Voltage (Note 1)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee Power-On Reset	VPOR		VSS		V	See section on power on reset for details
VDD rise rate to guarantee Power-On Reset	SVDD	0.05*			V/ms	See section on power on reset for details
Supply Current (Note 2, 5)	IDD		2.7 52.5 13.5	5 105 30	mA µA mA	FOSC = 4 MHz, VDD = 5.5V (Note 4) LP osc configuration FOSC = 32 KHz, VDD = 4.0V, WDT disabled HS osc configuration FOSC = 20 MHz, VDD = 5.5V (PIC16C74-20)
Power Down Current (Note 3, 5)	IPD		10.5 1.5 1.5 1.5	42 21 24 TBD	µA µA µA µA	VDD = 4.0V, WDT enabled, -40°C to +85°C VDD = 4.0V, WDT disabled, 0°C to +70°C VDD = 4.0V, WDT disabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -40°C to +125°C

* These parameters are characterized but not tested.

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Notes: 1. This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2. The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
   The test conditions for all IDD measurements in active operation mode are:
   OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
3. The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.
4. For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
5. Timer1 oscilator (when enabled) adds approximately xmA to the specification. This value is from characterization and is for design guidance only. This is not tested.

18.2 DC CHARACTERISTICS: PIC16LC74-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ + 125°C for automotive,
-40°C ≤ TA ≤ + 85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD = 2.5V to 6.0V

Characteristic	Sym	Min	Typ †	Max	Units	Conditions
Supply Voltage	VDD	2.5		6.0	V	XT, RC and LP osc configuration
		4.5		5.5	V	HS osc configuration
RAM Data Retention Voltage (Note 1)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee Power-On Reset	VPOR		VSS		V	See section on power on reset for details
VDD rise rate to guarantee Power-On Reset	SVDD	0.05*			V/ms	See section on power on reset for details
Supply Current (Note 2, 5)	IDD		2.7	5	mA	FOSC = 4 MHz, VDD = 5.5V (Note 4)
			22.5	48	µA	FOSC = 32 KHz, VDD = 3.0V, WDT disabled
Power Down Current (Note 3, 5)	IPD		7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
			0.9	13.5	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
			0.9	18	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
			0.9	24	µA	VDD = 3.0V, WDT disabled, -40°C to +125°C

* These parameters are characterized but not tested.

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Notes: 1. This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2. The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3. The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

4. For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5. Timer1 oscilator (when enabled) adds approximately xmA to the specification. This value is from characterization and is for design guidance only. This is not tested.

18.3 DC CHARACTERISTICS: PIC16C74-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C74-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16LC74-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS — **Standard Operating Conditions (unless otherwise stated)**
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40 ≤ TA ≤ +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec tables 14.1 and 14.2

Characteristic	Sym	Min	Typ †	Max	Units	Conditions
Input Low Voltage						
I/O ports	VIL					
- with TTL buffer		VSS		0.8 V	V	
- with Schmitt Trigger buffer		VSS		0.2 VDD	V	
$\overline{MCLR}$, RA4/T0CKI, OSC1 (in RC mode)		VSS		0.2 VDD	V	
OSC1(in XT, HS and LP)		VSS		0.3 VDD	V	Note 1
Input High Voltage						
I/O ports	VIH					
- with TTL buffer		2.0		VDD	V	VDD ≤ 5.5V (Note 4)
- with Schmitt Trigger buffer		0.8 VDD		VDD		For entire VDD range (Note 4)
$\overline{MCLR}$		0.8 VDD		VDD	V	
RA4/T0CKI, RC<7:4>, RD<7.4>, RE<2:0>, OSC1 (XT, HS and LP)		0.7 VDD		VDD	V	Note 1
PortB weak pull-up current	IPURB	50	100	150	µA	VDD = 5V, VPIN = VSS
Input Leakage Current (Notes 2, 3)						
I/O ports	IIL			±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{MCLR}$, RA4/T0CKI				±5	µA	VSS ≤ VPIN ≤ VDD
OSC1				±5	µA	VSS ≤ VPIN ≤ VDD , XT, HS and LP osc configuration
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
				0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
OSC2/CLKOUT				0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
(RC osc configuration)				0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C
Output High Voltage						
I/O Ports (Note 3)	VOH	VDD-0.7			V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
		VDD-0.7			V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
OSC2/CLKOUT		VDD-0.7			V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
(RC osc configuration)		VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
Capacitive Loading Specs on Output Pins						
OSC2 pin	COSC2			15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
All I/O pins and OSC2 (in RC mode)	CIO			50	pF	
SCL, SDA in I²C mode	Cb			400	pF	

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Notes: 1. In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C74 be driven with external clock in RC mode.

2. The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
3. Negative current is defined as coming out of the pin.
4. The user may use better of the two specs.

18.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. Tcc:st (I²C specifications only)
4. Ts (I²C specifications only)

T			
F	Frequency	T	Time

Lowercase subscripts (pp) and their meanings:

pp			
cc	CCP1	os	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Upper case letters and their meanings:

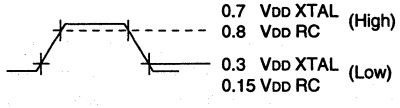
S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedence)	V	Valid
L	Low	Z	High Impedence
I²C only			
AA	output access	High	High
BUF	Bus free	Low	Low

Tcc:st (I²C specifications only)

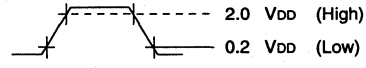
CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

PARAMETER MEASUREMENT INFORMATION

All timings are measured between high and low measurement points as indicated in the figures below.



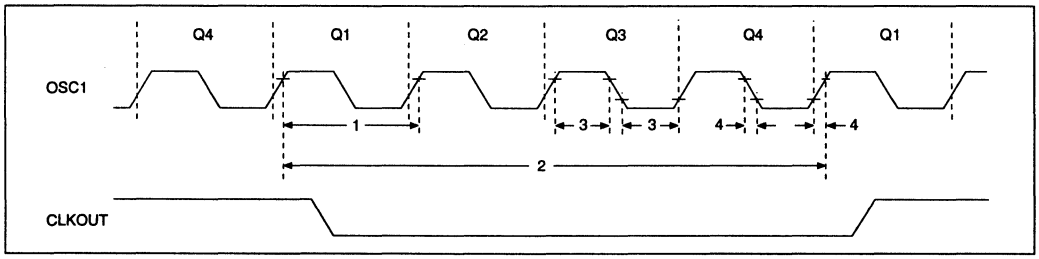
OSC1 MEASUREMENT POINTS



I/O PORT MEASUREMENT POINTS

18.5 Timing Diagrams and Specifications

External Clock Timing



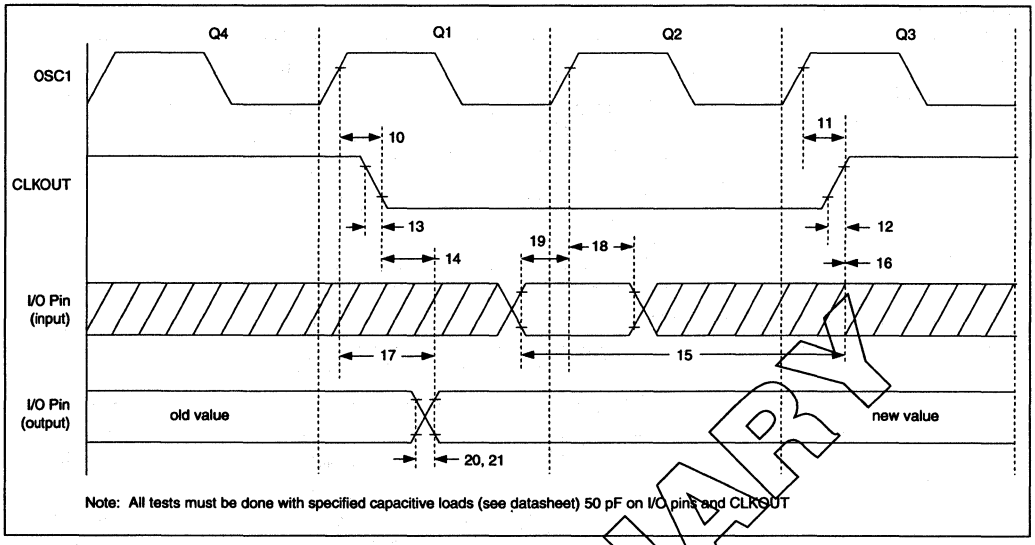
External Clock Timing Requirements

Parameter No.	Sym	Characteristic	Min	Typ †	Max	Units	Conditions
	Fos	**External CLKIN Frequency**	DC		4	MHz	XT and RC osc mode
		(Note 1)	DC		4	MHz	HS osc mode (PIC16C74-04,
				-			PIC16LC64-04)
			DC		20	MHz	HS osc mode (PIC16C74-20)
			DC		200	KHz	LP osc mode
		Oscillator Frequency	DC		4	MHz	RC osc mode
		(Note 1)	0.1		4	MHz	XT osc mode
			1		4	MHz	HS osc mode (PIC16C74-04
				-			PIC16LC64-04)
			1		20	MHz	HS osc mode (PIC16C74-20)
			DC		200	KHz	LP osc mode
1	Tos	**External CLKIN Period**	250		-	ns	XT and RC osc mode
		(Note 1)	250		-	ns	HS osc mode (PIC16C74-04,
				-			PIC16LC64-04)
			50		-	ns	HS osc mode (PIC16C74-20)
			50		-	µs	LP osc mode
		Oscillator Period	250			ns	RC osc mode
		(Note 1)	250		10,000	ns	XT osc mode
			250		1,000	ns	HS osc mode (PIC16C74-04
							PIC16LC64-04)
			50		1,000	ns	HS osc mode (PIC16C74-20)
			5			µs	LP osc mode
2	Tcy	**Instruction Cycle Time (Note 1)**	1.0	$4/F_{os}$	DC	µs	
3	TosL,	Clock in (OSC1) High or Low Time	50	-	-	ns	XT oscillator
	TosH		2.5	-	-	µs	LP oscillator
			20	-	-	ns	HS oscillator
4	TosR,	Clock in (OSC1) Rise or Fall Time	25	-	-	ns	XT oscillator
	TosF		50	-	-	ns	LP oscillator
			25	-	-	ns	HS oscillator

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

CLKOUT and I/O Timing



Note: All tests must be done with specified capacitive loads (see datasheet) 50 pF on I/O pins and CLKOUT

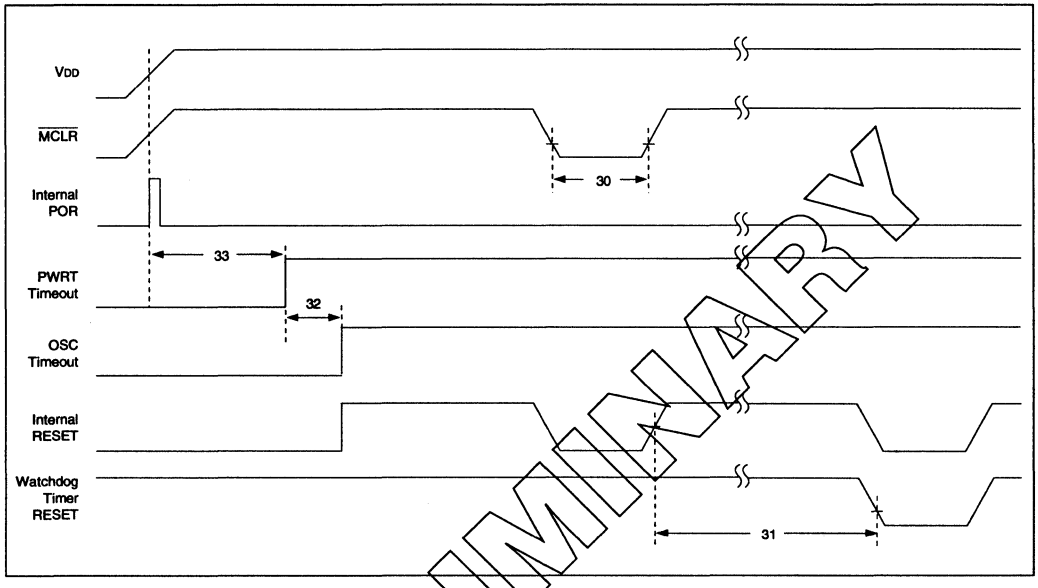
CLKOUT and I/O Timing Requirements

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓ (RC mode)	-	15	30	ns	
11	TosH2ckH	OSC1↑ to CLKOUT↑ (RC mode)	-	15	30	ns	
12	TckR	CLKOUT rise time (RC mode)	-	5	15	ns	
13	TckF	CLKOUT fall time (RC mode)	-	5	15	ns	
14	TckL2ioV	CLKOUT ↓ to Port out valid	-	-	0.5Tcy+20	ns	
15	TioV2ckH	Port in valid before CLKOUT ↑ (RC mode)	0.25 Tcy+25	-	-	ns	
16	TckH2ioI	Port in hold after CLKOUT ↑ (RC mode)	0	-	-	ns	
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	-	-	TBD	ns	
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	-	-	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	-	-	ns	
20	TioR	Port output rise time	-	10	25	ns	
21	TioF	Port output fall time	-	10	25	ns	

* These parameters are characterized but not tested.

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Reset, Watchdog Timer, Oscillator Start-Up Timer and Power-Up Timer Timing



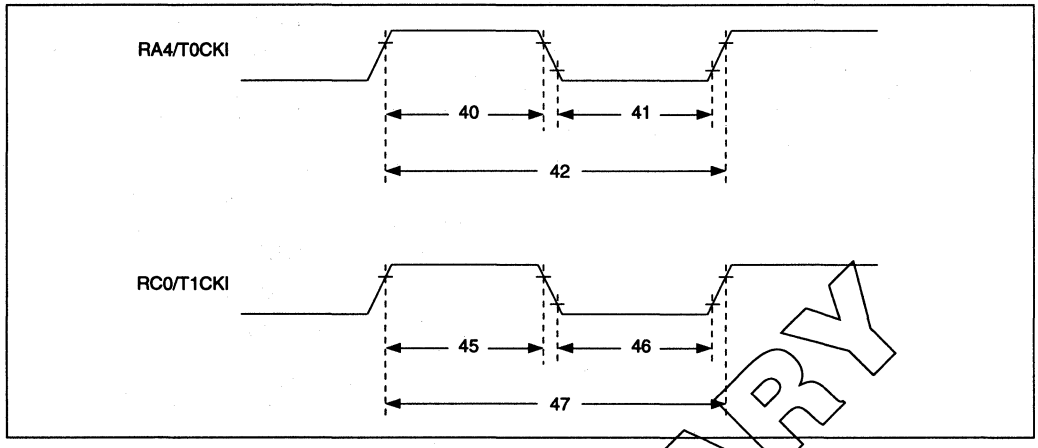
Reset, Watchdog Timer, Oscillator Start-Up Timer and Power-Up Timer Requirements

Parameter No.	Sym	Characteristic	Min	Typ †	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	100	-	-	ns	
31	Twdt	Watchdog Timer Timeout Period (No Prescaler)	7*	18	33*	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period		1024 tosc		ms	tosc = OSC1 period
33	Tpwrt	Power up Timer Period	28*	72	132*	ms	VDD = 5V, -40°C to +125°C

* These parameters are characterized but not tested.

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Timer0 and Timer1 Clock Timings



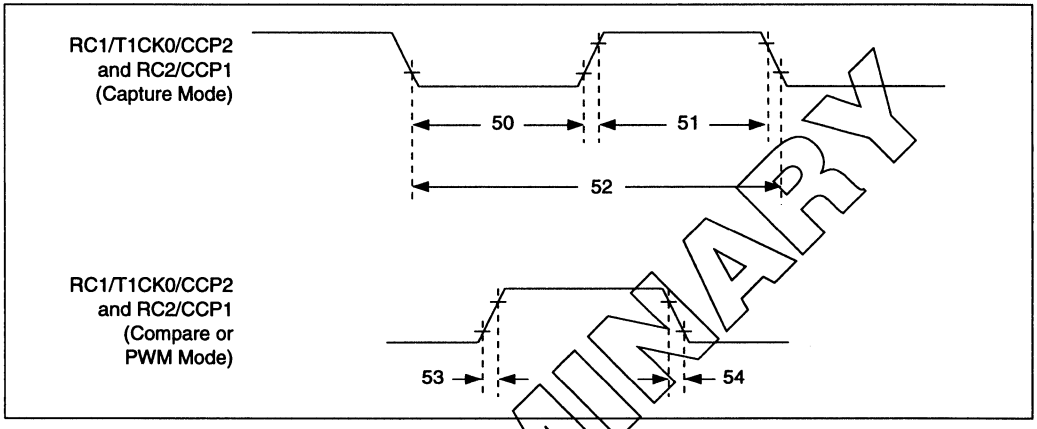
Timer0 and Timer1 Clock Requirements

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	$T_{t0}H$	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20*	-	-	ns	
			With Prescaler	10*	-	-	ns	
41	$T_{t0}L$	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20*	-	-	ns	
			With Prescaler	10*	-	-	ns	
42	$T_{t0}P$	T0CKI Period		$\frac{T_{CY} + 40^*}{N}$	-	-	ns	Where N = prescale value (2, 4, ..., 256)
45	$T_{t1}H$	T1CKI High Time	Synchronous, No Prescaler	0.5Tcy + 20	-	-	ns	
			Synchronous, With Prescaler	10*	-	-	ns	
			Asynchronous	2 Tcy	-	-	ns	
46	$T_{t1}L$	T1CKI Low Time	Synchronous, No Prescaler	0.5Tcy + 20*	-	-	ns	
			Synchronous, With Prescaler	10*	-	-	ns	
			Asynchronous	2 Tcy	-	-	ns	
47	$T_{t1}P$	T1CKI input period	Synchronous	$\frac{T_{CY} + 40^*}{N}$	-	-	ns	N=prescale value (1, 2, 4, 8)
			Asynchronous	4 Tcy	-	-	ns	
	F_{t1}	Timer1 oscillator input frequency range (oscillator enabled by setting the T1OSCEN bit)		DC	-	200	KHz	

* These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Capture/Compare/PWM Timings (CCP1 and CCP2)



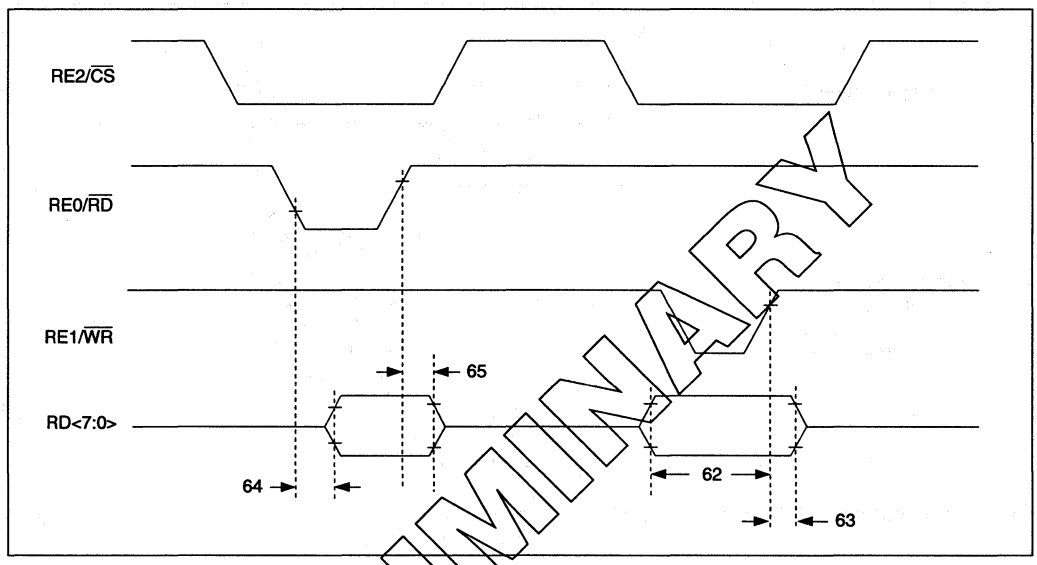
Capture/Compare/PWM Requirements (CCP1 and CCP2)

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
50	TccL	CCP1 and CCP2 input low time	No Prescaler	0.5 Tcy + 20	-	-	ns	
			With Prescaler	10	-	-	ns	
51	TccH	CC1 and CCP2 input high time	No Prescaler	0.5 Tcy + 20	-	-	ns	
			With Prescaler	10	-	-	ns	
52	TccP	CCP1 and CCP2 input period		$\frac{Tcy + 40}{N}$	-	-	ns	N = prescale value (4 or 16)
53	TccR	CCP1 and CCP2 output rise time			-	10	25	ns
54	TccF	CCP1 and CCP2 output fall time			-	10	25	ns

* These parameters are characterized but not tested.

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Parallel Slave Port Timing

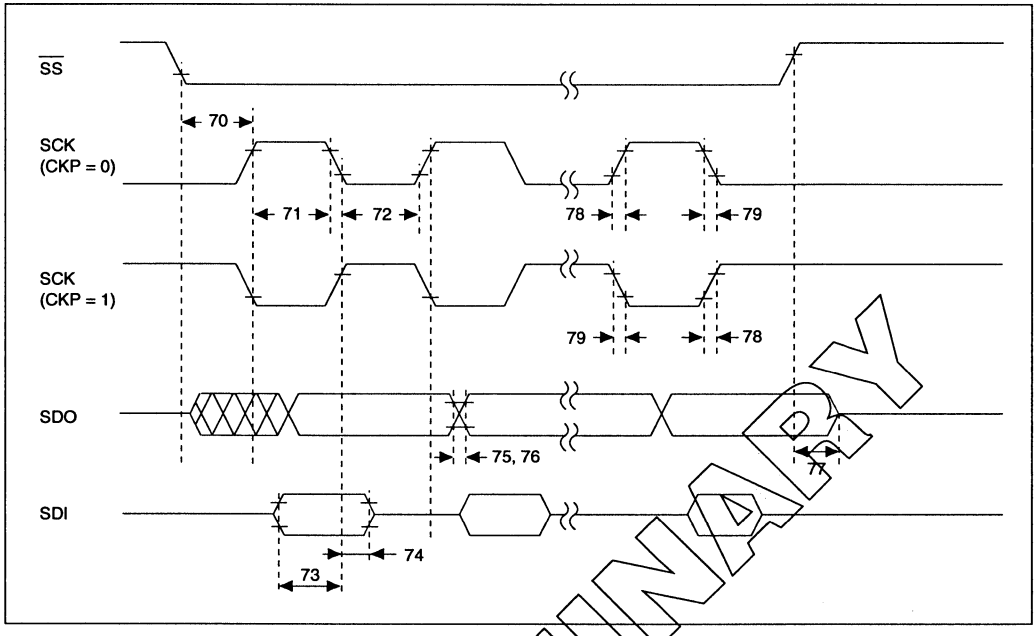


Parallel Slave Port Requirements

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before WR↑ or CS↑ (setup time)	20	-	-	ns	
63	TwrH2dtI	WR↑ or CS↑ to data–in invalid (hold time)	20	-	-	ns	
64	TrdL2dtV	RD↓ and CS↓ to data–out valid	-	-	40	ns	
65	TrdH2dtI	RD↑ or CS↓ to data–out invalid	10	-	30	ns	

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

SPI Mode Timing

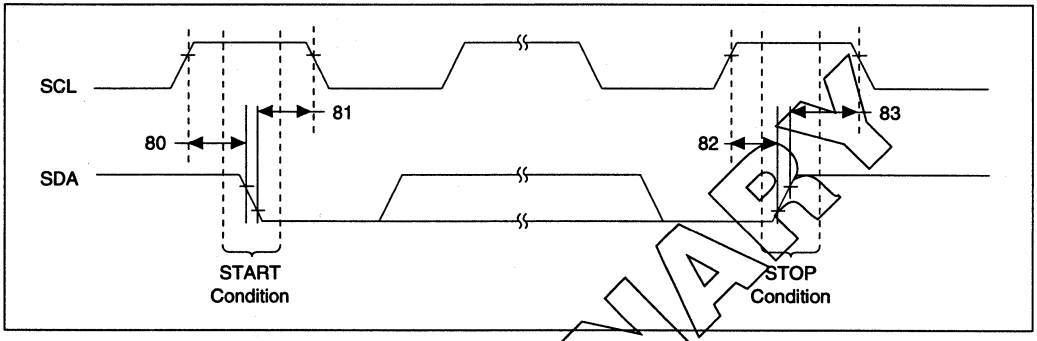


SPI Mode Requirements

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL,	SS↓ to SCK↓ or SCK↑ input	Tcy	-	-	ns	
71	TscH	SCK input high time (slave mode)	Tcy + 20	-	-	ns	
72	TscL	SCK input low time (slave mode)	Tcy + 20	-	-	ns	
73	TdiV2scH, TdiV2scL	SDI data input valid before SCK edge	Tcy	-	-	ns	
74	TscH2dil, TscL2dil,	SDI data input invalid after SCK edge	0.5Tcy	-	-	ns	
75	TdoR	SDO data output rise time	-	10	25	ns	
76	TdoF	SDO data output fall time	-	10	25	ns	
77	TssH2doZ	SS↓ to SDO output hi-impedence	10	-	50	ns	
78	TscR	SCK output rise time (master mode)	-	10	25	ns	
79	TscF	SCK output fall time (master mode)	-	10	25	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

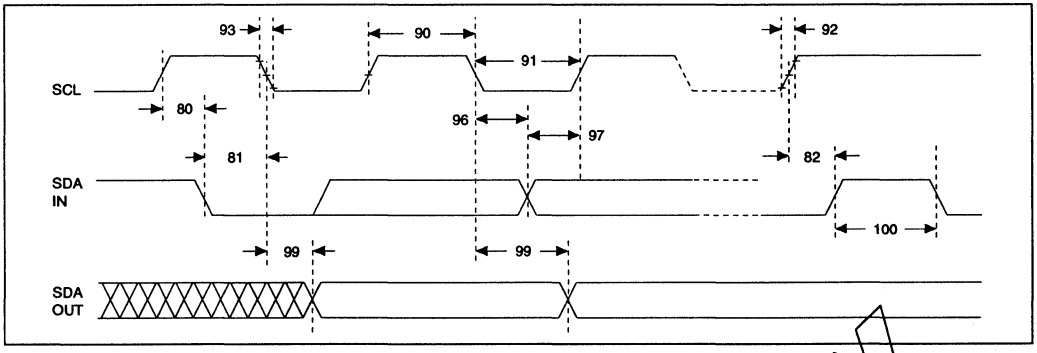
I²C Bus Start/Stop Bits Timing



I²C Bus Start/Stop Bits Requirements

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
80	TSU:STA	START condition	100 KHZ mode	4700	-	-	ns	Only relevant for repeated
		Setup time	400 KHz mode	600	-	-		START condition
81	THD:STA	START condition	100 KHz mode	4000	-	-	ns	After this period the
		Hold time	400 KHz mode	600	-	-		first clock pulse is generated
82	TSU:STO	STOP condition	100 KHZ mode	4700	-	-	ns	
		Setup time	400 KHz mode	600	-	-		
83	THD:STO	STOP condition	100 KHz mode	4000	-	-	ns	
		Hold time	400 KHz mode	600	-	-		

I²C Bus Data Timing



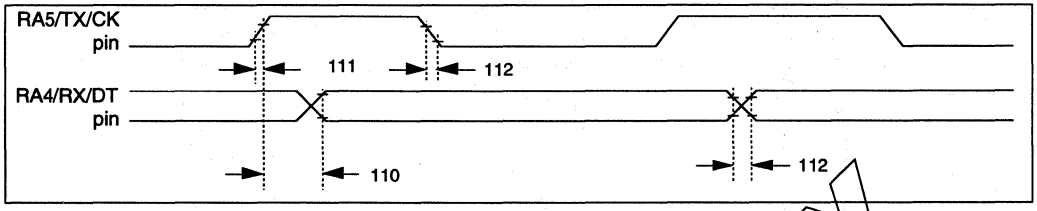
I²C Bus Data Requirements

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
90	THIGH	Clock high time	100 KHz mode	4.0	-	µs	PIC16C74 must operate at a minimum of 1.5 MHz
			400 KHz mode	0.6	-	µs	PIC16C74 must operate at a minimum of 10 MHz
			SSP Module	1.5 Tcy	-		
91	TLOW	Clock low time	100 KHz mode	4.7	-	µs	PIC16C74 must operate at a minimum of 1.5 MHz
			400 KHz mode	1.3		µs	PIC16C74 must operate at a minimum of 10 MHz
			SSP Module	1.5 Tcy	-		
92	TR	SDA and SCL rise time	100 KHz mode	-	1000	ns	
			400 KHz mode	20+0.1 Cb	300	ns	Cb is specified to be from 10-400 pF
93	TF	SDA and SCL fall time	100 KHz mode	-	300	ns	
			400 KHz mode	20+0.1 Cb	300	ns	Cb is specified to be from 10-400 pF
80	TSU:STA	START condition setup time	100 KHz mode	4.7	-	µs	Only relevant for repeated START condition
			400 KHz mode	0.6	-	µs	
81	THD:STA	START condition hold time	100 KHz mode	4.0	-	µs	After this period the first clock pulse is generated
			400 KHz mode	0.6	-	µs	
96	THD:DAT	Data input hold time	100 KHz mode	0	-	ns	
			400 KHz mode	0	0.9	µs	
97	TSU:DAT	Data input setup time	100 KHz mode	250	-	ns	
			400 KHz mode	100	-	ns	Note 2
82	TSU:STO	STOP condition setup time	100 KHz mode	4.7	-	µs	
			400 KHz mode	0.6	-	µs	
99	TAA	Output valid from clock	100 KHz mode	-	3500	ns	Note 1
			400 KHz mode	-	-	-	
100	TBUF	Bus free time	100 KHz mode	4.7	-	µs	Time the bus must be free before a new transmission can start
			400 KHz mode	1.3	-	µs	
	Cb	Bus capacitive loading		-	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement tsu;DAT≥250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max.+tsu;DAT=1000+250=1250ns (according to the standard-mode I²C bus specification) before the SCL line is released.

SCI Module: Synchronous Transmission (Master/Slave) Timing

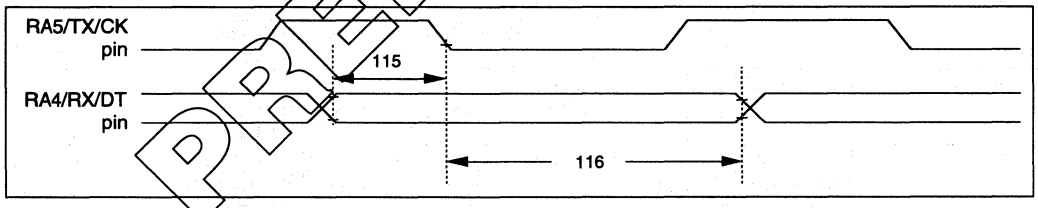


Serial Port Synchronous Transmission Requirements

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
		SYNC XMIT (MASTER & SLAVE)					
110	tckH2dtV	Clock high to data out valid	-	-	50	ns	
111	tckrf	Clock out rise time and fall time (Master Mode)	-	-	25	ns	
112	tdtrf	Data out rise time and fall time	-	-	25	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

SCI Module: Synchronous Receive (Master/Slave) Timing



Serial Port Synchronous Receive Requirements

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
		SYNC RCV (MASTER & SLAVE)					
115	tdtV2ckL	Data hold before CK ↓ (DT setup time)	15	-	-	ns	
116	tckL2dtl	Data hold after CK ↓ (DT hold time)	15	-	-	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

18.6 A/D CONVERTER CHARACTERISTICS:

PIC16C6X/7X-04 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)
PIC16C6X/7X-20 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)
PIC16LC6X/7X-04 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	-	-	8 bits	-	VREF = VDD = 512V, VSS ≤ Ain ≤ VREF
	NINT	Integral error	-	-	less than ±1 LSB	-	VREF = VDD = 512V, VSS ≤ Ain ≤ VREF
	NDIF	Differential error	-	-	less than ±1 LSB	-	VREF = VDD = 512V, VSS ≤ Ain ≤ VREF
	NFS	Full scale error	-	-	less than ±1 LSB	-	VREF = VDD = 512V, VSS ≤ Ain ≤ VREF
	NOFF	Offset error	-	-	less than ±1 LSB	-	VREF = VDD = 512V, VSS ≤ Ain ≤ VREF
	-	Monotonicity	-	guaranteed	-	-	VSS ≤ Ain ≤ VREF
	VREF	Reference voltage	3.0V	-	VDD + 0.3	V	
	VAIN	Analog input voltage	VSS-0.3	-	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	-	-	10.0	KΩ	
	Iad	A/D conversion current (VDD)	-	180	-	µa	Average current consumption when A/D is on. (Note 2)
	IREF	VREF input current (Note 3)		-	1 10	mA µA	During sampling All other times

* These parameters are characterized but not tested.

† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Sampling time may be less (or more) if source impedance is smaller (or higher). Also note that sampling begins after 2tad delay after a conversion is completed.

Note 2: When A/D is off, it will not consume any current other than minor leakage current. The power down current spec includes any such leakage from the A/D module.

Note 3: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

18.7 A/D CONVERTER CHARACTERISTICS: PIC16LC6X/7X-04 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	-	-	8 bits	-	VREF = VDD = 3.0V (Note 1)
	NINT	Integral error	-	-	less than ±1 LSB	-	VREF = VDD = 3.0V (Note 1)
	NDIF	Differential error	-	-	less than ±1 LSB	-	VREF = VDD = 3.0V (Note 1)
	NFS	Full scale error	-	-	less than ±1 LSB	-	VREF = VDD = 3.0V (Note 1)
	NOFF	Offset error	-	-	less than ±1 LSB		VREF = VDD = 3.0V (Note 1)
	-	Monotonicity	-	guaranteed	-	-	VSS ≤ Ain ≤ VREF
	VREF	Reference voltage	3.0V	-	VDD + 0.3	V	
	VAIN	Analog input voltage	Vss-0.3	-	VREF + 0.3	V	
	ZAIN	Recommended impedance of analog voltage source	-	-	10.0	KΩ	
	Iad	A/D conversion current (VDD)	-	90		µa	Average current consumption when A/D is on. (Note 2)
	IREF	VREF input current (Note 4)	-	-	1 10	mA µA	During sampling All other times

* These parameters are characterized but not tested.

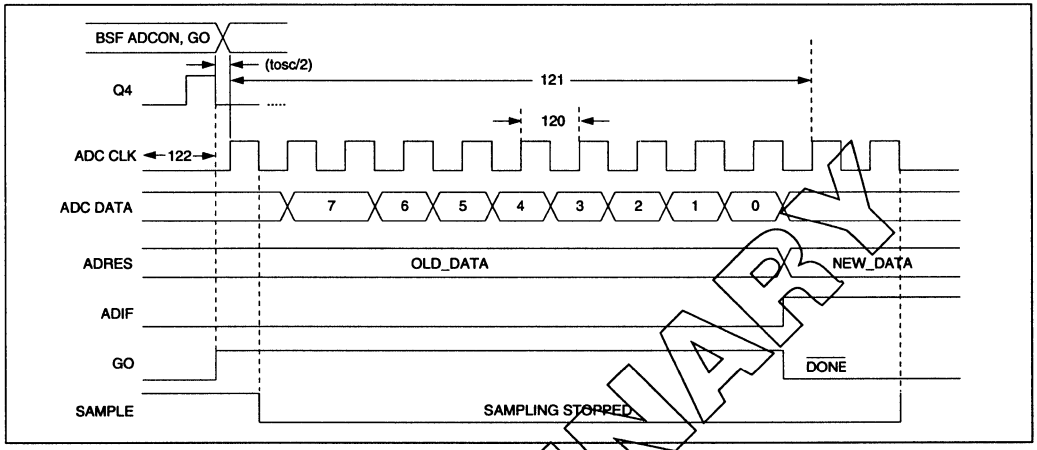
† : Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Sampling time may be less (or more) if source impedance is smaller (or higher). Also note that sampling begins after 2tad delay after a conversion is completed.

Note 2: When A/D is off, it will not consume any current other than minor leakage current. The power down current spec includes any such leakage from the A/D module.

Note 3: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

A/D Conversion Timing



A/D Conversion Requirements

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
120	tad	A/D clock period	-	2tosc	-	-	ADCS1,0 = 00 (for tosc ≥ 1 µs)
			-	8tosc	-	-	ADCS1,0 = 01 (for tosc ≥ 0.25 µs)
			-	32tosc	-	-	ADSC1,0 = 10 (for tosc ≥ 50 ns)
							ADSC1,0 = 11 (RC oscillator source)
			3.0	6.0	9.0	µs	PIC16LC74
			2.0	4.0	6.0	µs	PIC16C74
121	TCNV	Conversion time (not including S/H time)	-	10tad	-	-	-
122	TSMP	Sampling time	5	-	-	µs	The minimum time is the amplifier settling time. This may be used of the "new" input voltage has not changed by more than 1 Lsb (i.e. 20mV @ 5.12V) from the last sampled voltage (as stated on C_{HOLD}).

* These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

19.0 DC AND AC CHARACTERISTICS (GRAPHS/TABLES)

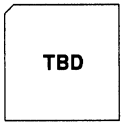
NOT AVAILABLE AT THIS TIME

20.0 PACKAGING INFORMATION

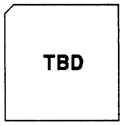
See Section 11 in the Data Book (pages ?).

20.1 Package Marking Information

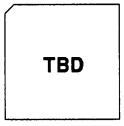
44L PLCC



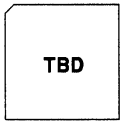
Example



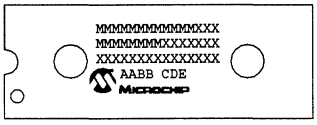
44L PQFP



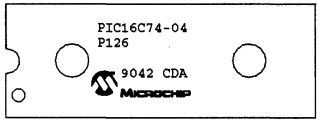
Example



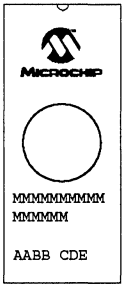
40L PDIP (.600 mil)



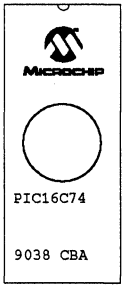
Example



40L Cerdip



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country or origin in which part was assmebled

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

APPENDIX A

The following are the list of modifications over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bit. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and register file (128 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from status register.
3. Data memory paging is redefined slightly. Status register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.

   Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5x.
5. OPTION and TRIS registers are made addressible.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers oscillator start-up timer (OST) and power-up timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PortB has weak pull-ups and interrupt on change feature.
13. RTCC pin is also a port pin (RA4) now.
14. FSR is made a full eight bit register.
15. "In system programming" is made possible. The user can program PIC16CXX devices using only five pins: V_{DD}, V_{SS}, $\overline{MCLR}/V_{PP}$, RB6 (clock) and RB7 (data in/out).
16. PCON status register is added with a Power-on-Reset (POR) status bit.
17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.

APPENDIX B

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

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CONNECTING TO MICROCHIP BBS

Connect world wide to the Microchip BBS using the CompuSserve communications network. In most cases a local call is your only expense. The Microchip BBS connection does not use CompuServe membership services, therefore **you do not need CompuServe membership to join Microchip's BBS.**

The procedure to connect will vary slightly from country to country. Please check with your local CompuServe agent for details if you have a problem. CompuServe services allows multiple users at baud rates up to 9600.

To connect:

1. Set your modem to 8 bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.

2. Dial your local CompuServe phone number.

3. Depress **<ENTER>** and a garbage string will appear because CompuServe is expecting a 7E1 setting.

4. Type **+ <ENTER>** and `Host Name:` will appear.

5. Type **MCHIPBBS<ENTER>** and you will be connected to the Microchip BBS.

In the United States, to find CompuServe's phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600 baud connection. After the system responds with `Host Name:`, type

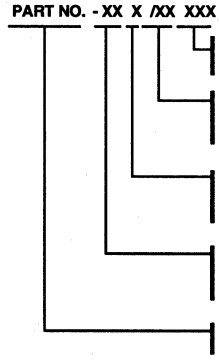
NETWORK<ENTER> and follow CompuServe's directions.

For voice information (or calling from overseas), you may call (614) 457-1550 for your local CompuServe number.

NOTES:

PIC16C74 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Pattern:	3-Digit Pattern Code for QTP/SQTP (factory specified) (blank for OTP and Windowed Parts)	
Package:	P = PDIP (600 mil) L = PLCC PQ = MQFP (Metric PQFP) JW = CerDIP (600 mil)	
Temperature Range:	- = 0°C to +70°C (T for tape/reel) I = -40°C to +85°C (S for tape/reel) E = -40°C to +125°C	
Frequency Range:	04 = 4 MHz 20 = 20 MHz	
Device:	PIC16C74 : Standard V_{DD} range PIC16LC74 : Extended V_{DD} range	

Examples:

a) PIC16C74 - 04/P
= Commercial temp., DIP (600 mil) package, 4 MHz, standard V_{DD} limits, OTP part

b) PIC16C74 - 04I/PQ462
= Industrial temp., MQFP package, 4 MHz, standard V_{DD} limits, pattern #462 (QTP or SQTP parts)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local Compuserve number.

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

PIC16C84

8-Bit CMOS EEPROM Microcontroller

FEATURES

High Performance RISC-like CPU

- Only 35 single word instructions to learn
- All instructions single cycle (400ns) except for program branches which are two-cycle
- Operating speed: DC - 10 MHz clock input
  DC - 400ns instruction cycle
- 14-bit wide instructions
- 8-bit wide data path
- 1024 x 14 on-chip EEPROM program memory
- 36 x 8 general purpose registers (SRAM)
- 15 special function hardware registers
- 64 x 8 EEPROM data memory
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
  - External INT pin
  - TMR0 timer overflow
  - PORTB<7:4> interrupt on change
  - Data EEPROM write complete
- 1,000,000 ERASE/WRITE cycles (Typical)
- Data Retention >40 years

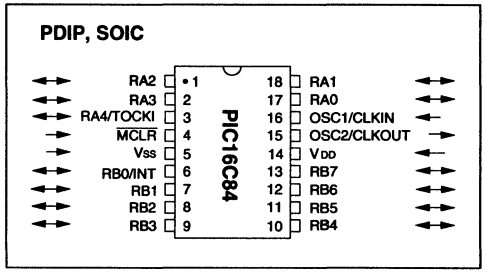
Peripheral Features

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25mA sink max. per pin
  - 20mA source max. per pin
- TMR0: 8-bit real time clock/counter with 8-bit programmable prescaler

Special Microcontroller Features

- Power-On Reset
- Power-up Timer
- Oscillator Start-up Timer
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security EEPROM fuse for code-protection
- Power saving SLEEP mode
- User selectable oscillator options:
  - RC oscillator: RC
  - Crystal/resonator: XT
  - High-speed crystal/resonator: HS
  - Power-saving, low-frequency crystal: LP
- Serial, In-System Programming (ISP) of EEPROM program and data memory using only two pins

FIGURE A - PIN CONFIGURATION



CMOS Technology

- Low-power, high-speed CMOS EEPROM technology
- Fully static design
- Wide-operating voltage range:
  - Commercial: 2.0V to 6.0V
  - Industrial: 2.0V to 6.0V
  - Automotive: 2.0V to 6.0V
- Low-power consumption
  - < 2mA @ 5V, 4 MHz
  - 15μA typical @ 2V, 32 KHz
  - < 1μA typical standby current @ 2V

INTRODUCTION

The PIC16C84 is a high-performance, low-cost, CMOS, fully-static 8-bit microcontroller with 1K x 14 EEPROM program memory and 64 bytes of EEPROM data memory. It is the second member of an enhanced family of PIC16CXX microcontrollers (customers familiar with the PIC16C5X products may refer to Appendix A for a list of enhancements).

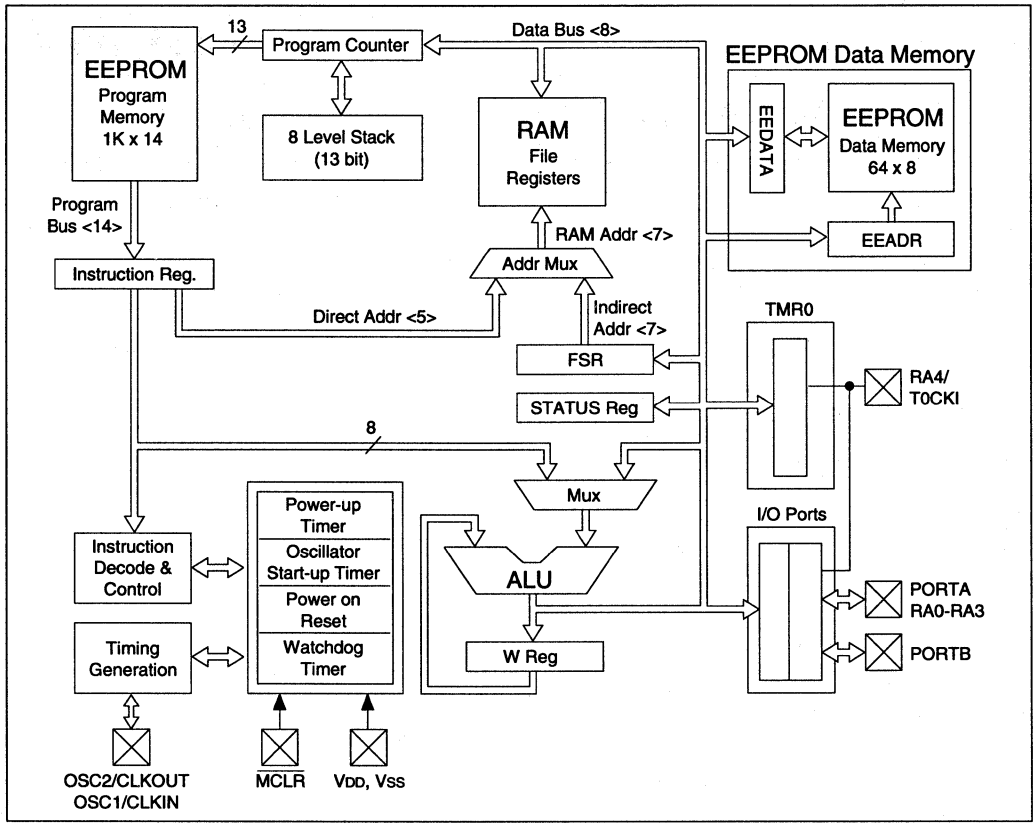
Its high performance is due to instructions that are all single word (14-bit wide), which execute in single cycle (400ns at 10 MHz clock) except for program-branches which take two cycles (800ns).

The PIC16C84 has four interrupt sources and an eight-level hardware stack.

The peripherals include an 8-bit timer/counter with an 8-bit prescaler (effectively a 16-bit timer) and 13 bi-directional I/O pins. The high current drive (25mA max. sink, 20mA max source) of the I/O pins help reduce external drivers and therefore, system cost.

The PIC16C84 product is supported by an assembler, an in-circuit emulator and a production quality programmer. These tools are supported on IBM PC® and compatible machines.

FIGURE B - PIC16C84 BLOCK DIAGRAM



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1.0 GENERAL DESCRIPTION

The PIC16C84 is a low-cost, high-performance, CMOS, fully static, EEPROM-based 8-bit microcontroller. The EEPROM program memory is intended to be used for code development as well as One-Time-Programmable memory for full production. The program memory can not be updated during code execution. However, a special "in-system-programming" capability using only two pins to serially input and output data allows users to update program code of the PIC16C84 embedded in a system. The EEPROM data memory (64-bytes) is readable and writable during normal execution at full VDD range (2.0V - 6.0V).

The PIC16C84 employs an advanced RISC-like architecture. A reduced set of 35 instructions, single word instructions (14-bit wide), single cycle instructions except for two-cycle program branches, instruction pipelining, large register set and separate instruction and data memory (Harvard architecture) schemes are some of the architectural innovation used to achieve very high performance. The PIC16C84 typically achieves a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in its class.

The PIC16C84 is equipped with special features to reduce external components and thus reduce cost, enhance system reliability and reduce power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low cost solution and the LP oscillator minimizes power consumption. The SLEEP (power down) mode offers power saving. The user can wake up the chip from SLEEP through external interrupts and reset.

A highly reliable watchdog timer with its own on-chip RC oscillator provides protection against software malfunction.

1.1 Compatibility with PIC16C5X

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an improved version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of modifications. Code written for PIC16C5X can be easily ported to the PIC16C84 (see Appendix B).

1.2 Applications

The PIC16C84 fits perfectly in applications ranging from high speed automotive and appliance control to low-power remote sensors, electronic locks and security devices. The PIC16C84 is also ideal for smart cards and RF tags. The EEPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages for through hole or surface mounting make this microcontroller series perfect for all applications with space limitations.

Low-cost, low-power, high-performance, ease of use and I/O flexibility makes the PIC16C84 very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

Additionally, the In System Programmability of the PIC16C84 (using only two pins for data transfer) offers flexibility to customize a product after complete assembly and test.

This feature can be used to serialize a product, store calibration data available only after final test or to upgrade the firmware on finished goods.

2.0 PIC16C84 DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information and tables in this section. When placing orders, please use the "PIC16C84 Product Identification System" on the back page of this data sheet to specify the correct part number.

2.1 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. All EEPROM program memory locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.2 Serialized Quick-Turnaround-Production (SQTP) Devices

Microchip offers the unique programming service where few locations in each device is programmed with a different serial number. The serial number may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as entry-code, pass-word or ID number.

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C84 can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C84 uses a Harvard architecture, in which, program and data are accessed from separate memories. This improves bandwidth over traditional Von-Neuman architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. In PIC16C84, op-codes are 14-bit wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single cycle except for program branches.

The PIC16C84 address 1K x 14 program memory space, all on-chip. Program execution is internal only (microcontroller mode).

The PIC16C84 can directly or indirectly address its 48 register files or data memory. All special function registers including the program counter are mapped in the data memory. The instruction set is fairly orthogonal (symmetrical) which makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C84 simple yet efficient. In addition, the learning curve is reduced significantly.

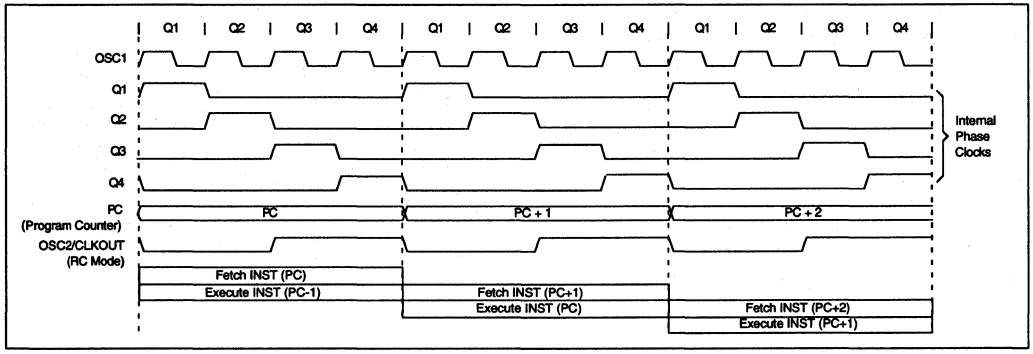
2

3.1 - PIC16C84 PINOUT DESCRIPTION

Pin name	Pin Type	Pin function	
		Normal operation	Serial In-System Programming (ISP) Mode
VDD	P	Power	Power
VSS	P	Ground	Ground
OSC1/CLKIN	I	Clock input/oscillator connection	-
OSC2/CLKOUT	I/O	Oscillator connection/CLKOUT output. It is CLKOUT in RC oscillator mode and oscillator connection in all other modes.	-
$\overline{MCLR}$/VPP	I/P	Master clear (external reset) input. Active low.	Master clear. Apply high voltage (VPP) to enter programming mode.
RA4/T0CKI	I	Open-drain output/input pin. It is also the clock input to TMR0 timer/counter: Schmitt trigger input buffer	-
RA0	I/O	Bidirectional I/O pin. TTL input levels	-
RA1	I/O	Bidirectional I/O pin. TTL input levels	-
RA2	I/O	Bidirectional I/O pin. TTL input levels	-
RA3	I/O	Bidirectional I/O pin. TTL input levels	-
RB0/INT	I/O	Bidirectional I/O pin/External interrupt input. TTL input levels	-
RB1	I/O	Bidirectional I/O pin. TTL input levels	-
RB2	I/O	Bidirectional I/O pin. TTL input levels	-
RB3	I/O	Bidirectional I/O pin. TTL input levels	-
RB4	I/O	Bidirectional I/O pin. TTL input levels	-
RB5	I/O	Bidirectional I/O pin. TTL input levels	-
RB6	I/O	Bidirectional I/O pin. TTL input levels	Clock input
RB7	I/O	Bidirectional I/O pin. TTL input levels	Data input/output

Legend: I = input, O = output, I/O = input/output, P = power. - = Not used.

FIGURE 3.2.1 - CLOCK/INSTRUCTION CYCLE



3.2 Clocking Scheme/Instruction Cycle

The clock input (from pin OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1, an instruction is fetched from the program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3.2.1.

3.3 Instruction Flow/Pipelining

An "Instruction Cycle" consists of Q1, Q2, Q3 and Q4 cycles. The Instruction fetch and execute cycles are pipelined such that fetch takes one instruction cycle while the decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction.

A fetch cycle begins with the program counter (PC) incrementing in Q1.

The fetched instruction is latched into the "Instruction Register (IR)" which is decoded and executed during Q2, Q3 and Q4. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

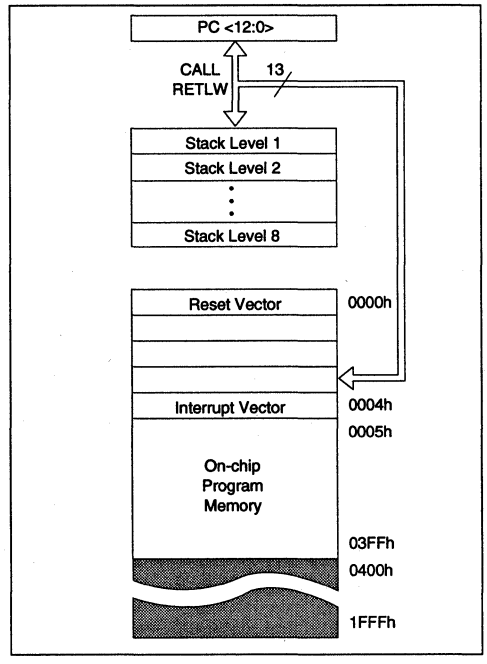
3.4 Program Memory Organization

The PIC16C84 has a 13-bit wide program counter (Figure 3.4.1) capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h - 03FFh) are physically implemented. Accessing a location above 3FFh will cause a wrap-around within the first 1K x 14 space. The reset vector is at 0000h and the interrupt vector is at 0004h.

The EEPROM program memory of the PIC16C84 is rated for limited Erase/write cycles. To program the program memory, the part must be put into a special mode by raising MCLR pin to high voltage (see section 11.5 for programming specification). Also, VDD must be 4.5V to 5.5V during programming. The PIC16C84 is not suitable for applications where program memory is updated in the user application frequently.

The program memory can be programmed serially using two data/clock pins (see Section 11) which makes in-system programming (ISP) possible. This allows the user to customize the system during final testing or upgrade a system in the field.

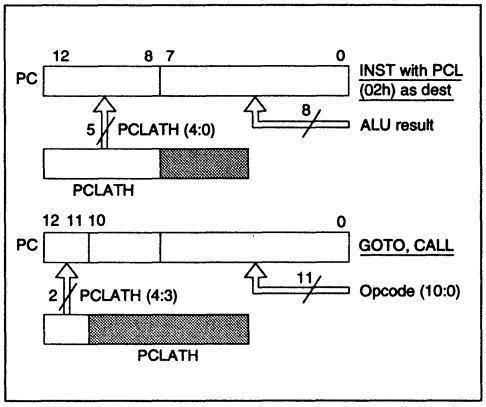
FIGURE 3.4.1 - PROGRAM MEMORY MAP AND STACK



3.5 Program Counter Module

The program counter (PC) is 13-bits wide. The low byte, PCL is a readable and writable register. The high byte of the PC, PCH, is not directly readable or writable. The high byte of the PC can be written through the PCLATH register (0Ah). When the PC is loaded with a new value during a CALL, GOTO or a write to PCL, the high bits of PC are loaded from PCLATH as shown in Figure 3.5.1.

FIGURE 3.5.1 - LOADING OF PC IN DIFFERENT SITUATIONS



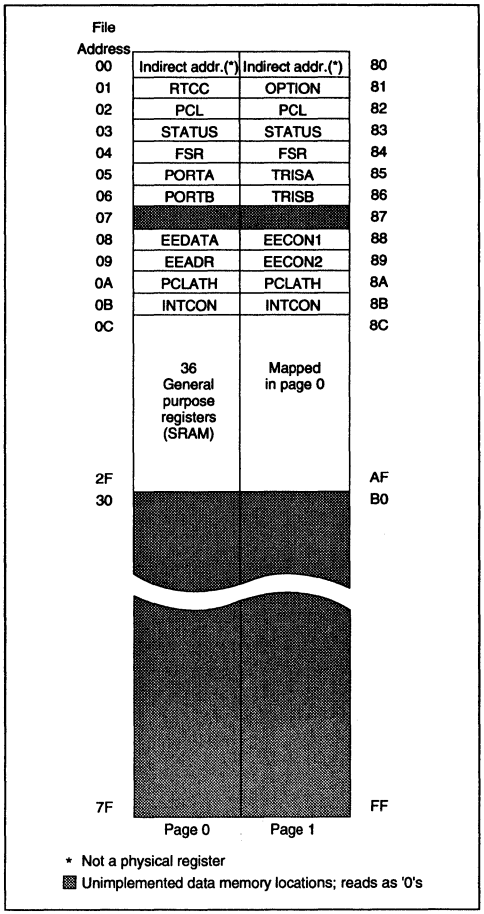
3.6 Stack

The PIC16C84 has an 8-deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is pushed on the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is popped in the event of a RETURN, RETLW or RETFIE instruction execution. PCLATH (0Ah) is not affected by a PUSH or a POP operation.

3.7 Register File Organization

The register file is organized as 128 x 8. It is accessed either directly or indirectly through the file select register FSR. It is also referred to as the data memory. There are several register file page select bits in the STATUS register allowing up to four pages. However, data memory extends only up to 2Fh. The first 12 locations are used to map special function registers. Locations 0Ch - 2Fh are general purpose registers implemented as static RAM. Some special function registers are mapped in page 1. When in page 1, accessing locations 8Ch - AFh will access the RAM in page 0 (Figure 3.7.1).

FIGURE 3.7.1 - REGISTER FILE MAP



3.7.1 REGISTER FILE ADDRESSING MODES

The register file can be addressed directly or indirectly. In both modes, up to 512 register locations can be addressed.

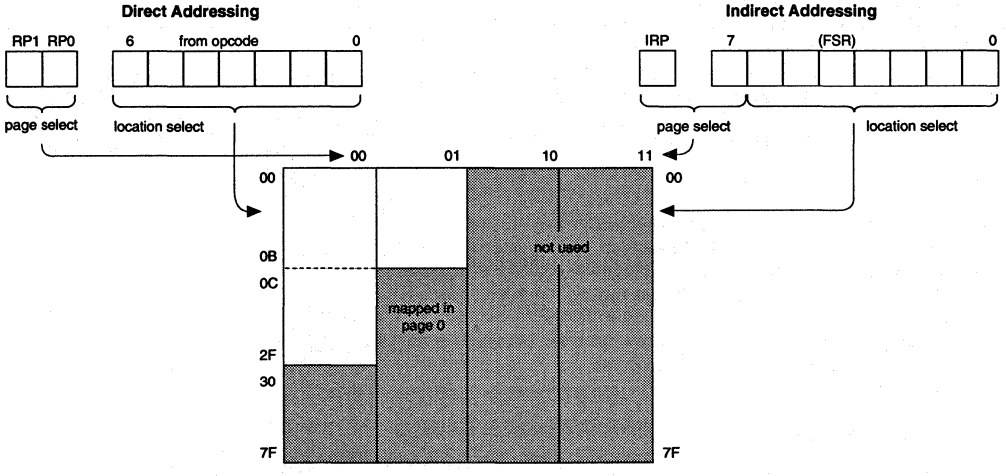
Direct addressing mode: An effective 9-bit direct address is obtained by concantenating 7-bits of direct address from the opcode and two bits (RP1, RP0) from the status register as shown in figure 3.7.1.1.

Indirect addressing mode: Indirect addressing is possible by using file address 00h (INDF). Any instruction using INDF as file register actually accesses data pointed to by the file select register, FSR. Reading INDF itself indirectly will produce 00h. Writing to INDF indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concantenating the 8-bit FSR register and the IRP bit from the status register as shown in Figure 3.7.1.1.

Please note that some special function registers are mapped in page 1. It will be necessary to set RP0 bit to address them. Both RP1 and IRP bits are essentially not used.

For convenience, the general purpose registers are mapped both in page 0 and page 1.

FIGURE 3.7.1.1 - DIRECT/INDIRECT ADDRESSING



Note: For memory map detail, see figure 3.7.1

FIGURE 3.7.2 - REGISTER FILE SUMMARY (PIC16C84)

Filename		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0	Value on power on reset
Page 0:										
00	INDO	Uses contents of FSR to address data memory (not a physical register)								00000000
01	TMR0	8 Bit Real Time clock counter								xxxxxxxx
02	PCL	Low order 8 bits of PC								00000000
03	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	00011xxx
04	FSR	Indirect data memory, address pointer 0								xxxxxxxx
05	PORTA	-	-	-	RA4/RT	RA3	RA2	RA1	RA0	
06	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	
07										
08	EEDATA	EEPROM Data Register								xxxxxxxx
09	EEADR	EEPROM Address Register								xxxxxxxx
0A	PCLATH	Holding register for high byte of PC (Note 1)								---00000
0B	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000000x
Page 1:										
80	INDO	MAPPED IN PAGE 0								
81	OPTION	$\overline{RBPU}$	INTEDG	RTS	RTE	PSA	PS2	PS1	PS0	11111111
82	PCL	Mapped in page 0								
83	STATUS	Mapped in page 0								
84	FSR	Mapped in page 0								
85	TRISA	PORTA (f05) data direction register								---11111
86	TRISB	PORTB (f06) data direction register								11111111
		Not implemented								
88	EECON1	-	-	-	EEIF	WRERR	WREN	WR	RD	0000X000
89	EECON2	Not a physical register								
8A	PCLATH	Mapped in page 0								
8B	INTCON	Mapped in page 0								

Notes: 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<15:8> whose contents are updated from or transfered to the upper byte of the program counter.

x = unknown
u = unchanged

3.8 Indirect Addressing Register

It is not a physical register. Addressing INDF will cause indirect addressing. See Section 3.7.1.1 for details.

3.8.1 TMR0

8-bit real time clock counter. See Section 6.4 for details.

3.8.2 PCL

Low order 8-bits of the PC. See Section 3.5 for details.

3.9 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for data memory.

The STATUS register can be the destination for any instruction like any other register. However, the status bits are set following the write operation (Q4). Furthermore, $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with STATUS register as destination may be different than intended. For example, CLRF STATUS will clear all bits except for $\overline{TO}$ and $\overline{PD}$ and then set the Z bit and leave STATUS register as 000UU100 (where U = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the STATUS registers because these instructions do not affect any status bit.

For other instructions, affecting any status bits, see the section "Instruction Set Summary" (see Section 4.0).

3.9.1 CARRY/$\overline{BORROW}$ AND DIGIT CARRY/ $\overline{BORROW}$ BITS

The carry bit (C) is a carry out in addition operations (ADDWF, ADDLW) and a $\overline{borrow}$ out in subtract operations (SUBWF, SUBLW). The following examples explain operation of carry/$\overline{borrow}$ bit:

```
;SUBLW Example #1
;
MOVLW   0x01    ;wreg=1
SUBLW   0x02    ;wreg= 2-wreg = 2-1=1
                ;Carry=1: result is positive
;
;SUBLW Example #2
;
MOVLW   0x02    ;wreg=2
SUBLW   0x01    ;wreg=1-wreg=1-2=FFh
                ;Carry=0: Result is negative
;
;SUBWF Example #1
;
clrf    0x20    ;f(20h)=0
movlw   1       ;wreg=1
subwf   0x20    ;f(20h)=f(20h)-wreg=0-1=FFh
                ;Carry=0:Result is negative
;
;SUBWF Example #2
movlw   0xFF    ;
movwf   0x20    ;f(20h)=FFh
clrw            ;wreg=0
subwf   0x20    ;f(20h)=f(20h)-wreg=FFh-0=FFh
                ;Carry=1: Result is positive
;
```

The digit carry operates in the same way as the carry bit, i.e.: it is a $\overline{borrow}$ in subtract operations.

3.9.2 TIME OUT AND POWER DOWN STATUS BITS ($\overline{TO}$, $\overline{PD}$)

The $\overline{TO}$ and $\overline{PD}$ bits in the status register can be tested to determine if a RESET condition has been caused by a Watchdog Timer time-out, a power-up condition or a wake-up from SLEEP by the Watchdog Timer or $\overline{MCLR}$ pin.

These status bits are only affected by events listed in Table 3.9.2.1.

TABLE 3.9.2.1 - EVENTS AFFECTING $\overline{PD}$/ $\overline{TO}$ STATUS BITS

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
WDT Timeout	0	U	No effect on $\overline{PD}$
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

U: unchanged

Note: A WDT timeout will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{PD}$ bit. Table 3.9.2.2 reflects the status of $\overline{PD}$ and $\overline{TO}$ after the corresponding event.

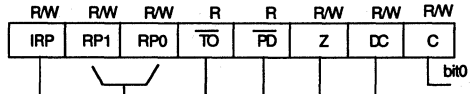
TABLE 3.9.2.2 - $\overline{PD}$/$\overline{TO}$ STATUS AFTER RESET

$\overline{TO}$	$\overline{PD}$	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT time-out (not during SLEEP)
U	0	$\overline{MCLR}$ wake-up from SLEEP
1	1	Power-up
U	U	$\overline{MCLR}$ reset during normal operation

U: unchanged

Note: The $\overline{PD}$ and $\overline{TO}$ bit maintain their status until an event of Table 3.9.2.1 occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{PD}$ and $\overline{TO}$ status bits.

FIGURE 3.9.1 - STATUS REGISTER



ADDRESS:	03h
RESET CONDITION:	000??XXX
TO, PD are set or reset as shown in Table 3.9.2.1	

CARRY/BORROW BIT:
For ADDWF, SUBWF , ADDLW and SUBLW instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
Note that a subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

DIGIT CARRY/BORROW BIT:
For ADDWF, SUBWF , ADDLW and SUBLW instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

ZERO BIT:
Set if the result of an arithmetic or logic operation is zero.
Reset otherwise. Additionally, MOVF instruction will affect the Z bit.

POWER DOWN BIT:
Set to "1" during power up or by a CLRWDT command. This bit is cleared to "0" by a SLEEP instruction.

TIME-OUT BIT:
Set to "1" during power up and by the CLRWDT and SLEEP command. This bit is cleared to "0" by a watchdog timer time out.

REGISTER PAGE SELECT BITS FOR DIRECT ADDRESSING:

RP1,0:
00 : page 0 (00h - 7Fh)
01 : page 1 (80h - FFh)
10 : page 2 (100h - 17Fh)
11 : page 3 (180h - 1FFh)

Each page is 128 bytes.
Only RP0 is useful in PIC16C84. Bit RP1 can be used as a general purpose read/write bit. However, this may affect upward compatibility with future products.

REGISTER PAGE SELECT BITS FOR INDIRECT ADDRESSING:
IRP0: 0 : page 0,1 (00h - FFh)
1 : page 2,3 (100h - 1FFh)
This bit is effectively not used in the PIC16C84.
It may be used as a general purpose read/write bit. However, this may affect upward compatibility with future product.

3.10 Arithmetic and Logic Unit (ALU)

The ALU is 8-bit wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register) or the accumulator. The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

3.11 W Register

The W register is an 8-bit working register (or accumulator) used for ALU operations. It is not in the data memory.

3.12 Interrupts

The PIC16C84 has four sources of interrupt:

- external interrupt from RB0/INT pin
- TMR0 timer/counter overflow interrupt
- end of data EEPROM write
- interrupt on change on RB<7:4> pins

The interrupt control register (INTCON, addr 0Bh) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

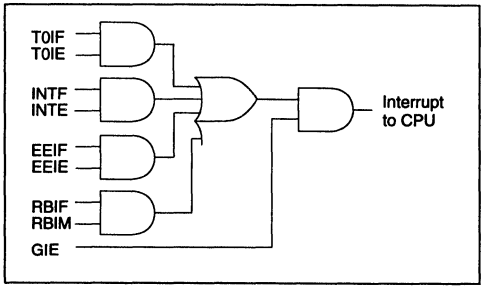
A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. GIE is cleared on reset.

The `RETFIE` instruction allows user to return from interrupt and enable interrupt at the same time.

The INT pin interrupt, the RB port change interrupt and the RTCC overflow interrupt flags are contained in the INTCON register.

When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

FIGURE 3.12.1 - INTERRUPT LOGIC



Note 1: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

Note 2: If an interrupt occurs while the Global Interrupt Enable (GIE) bit is being cleared, the GIE bit may unintentionally be re-enabled by the user's Interrupt Service Routine (the `RETFIE` instruction). The events that would cause this to occur are:

1. An instruction clears the GIE bit while an interrupt is acknowledged.
2. The program branches to the Interrupt vector and executes the Interrupt Service Routine.
3. The Interrupt Service Routine completes with the execution of the `RETFIE` instruction. This causes the GIE bit to be set (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.

The method to ensure that interrupts are globally disabled is:

1. Ensure that the GIE bit was cleared by the instruction, as shown in the following code:

```
LOOP   BCF   INTCON, GIE  ; Disable Global
                          ;   Interrupts
       BTFSC INTCON, GIE  ; Global Interrupts
                          ;   Disabled?
       GOTO  LOOP         ; NO, try again
       :                  ; Yes, continue with
                          ;   program flow
```

3.12.1 INT INTERRUPTS

External interrupt on RB0/INT pin is edge triggered: either rising (if INTEDG = 1, OPTION<6>) or falling (if INTEDG = 0). When a valid edge appears on INT pin, INTF bit is set (INTCON <1>). This interrupt can be disabled by clearing INTE control bit INTCON<4>. The INTF bit (INTCON<1>) must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake up the processor from SLEEP if INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 5.5 for details on SLEEP and Figure 5.5.1 for timing of wake-up from SLEEP through INT interrupt.

3.12.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. See Section 6.4 for details.

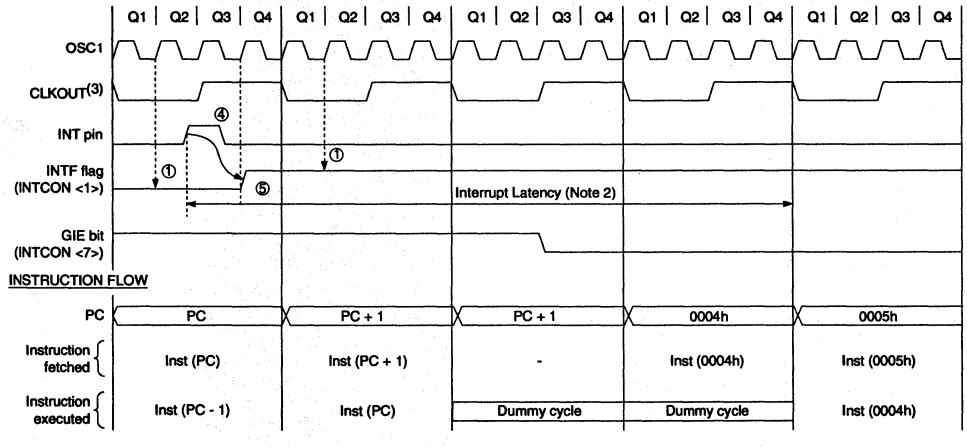
3.12.3 PORT RB INTERRUPT

An input change on PORTB <7:4> will set the RBIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing RBIE (INTCON<4>) bit.

3.12.4 EEPROM WRITE INTERRUPT

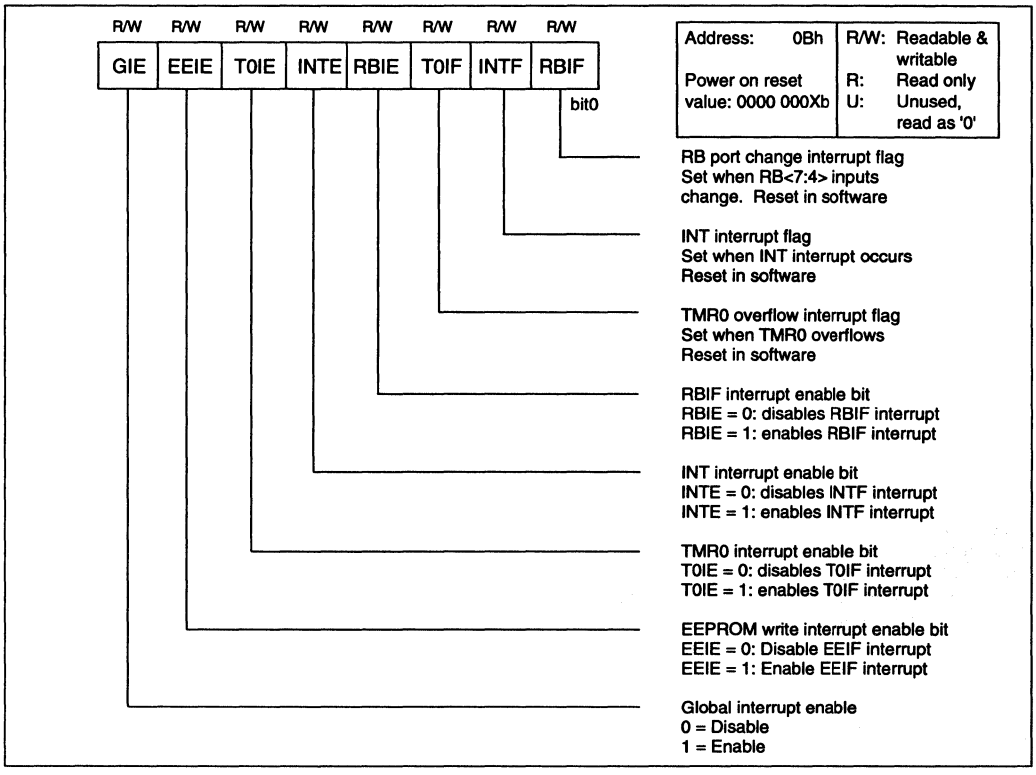
The EEPROM write interrupt flag, EEIF (EECON1<4>) when a data EEPROM write is complete. The interrupt can be masked by clearing the EEIE bit (INTCON<6>). See Section 6.1 for details on EEPROM write interrupt.

FIGURE 3.12.1.1 - INT PIN INTERRUPT TIMING



Notes:
1. INTF flag is sampled here (every Q1)
2. Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time.
   Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3. CLKOUT is available only in RC oscillator mode.
4. For minimum width spec of INT pulse, refer to AC specs.
5. INTF is enabled to be set anytime during the Q4-Q1 cycles.

FIGURE 3.12.2 - INTCON REGISTER



2

4.0 SPECIAL FEATURES OF THE CPU

What sets apart a microcontroller from other processors are special circuits to deal with the needs of real time applications. The PIC16C84 has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

The on-chip Watchdog Timer can only be shut off through an EEPROM fuse. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the power-up timer (PWRT), which provides a fixed delay of 72ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake up from SLEEP through external reset, watchdog timer time-out or interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of EEPROM configuration bits (fuses) are used to select various options (Section 5.6).

4.1 RESET

The PIC16C84 differentiates between various kinds of reset:

a) Power on reset (POR)

b) $\overline{MCLR}$ Reset during normal operation

c) $\overline{MCLR}$ reset during SLEEP

d) WDT time-out reset during normal operation

e) WDT time-out reset during SLEEP

Some registers are not reset; they are unknown on POR and unchanged in any other reset. Most other registers are reset to "reset state" on Power-On Reset (POR), on $\overline{MCLR}$ or WDT reset during normal operation and on $\overline{MCLR}$ reset during SLEEP. They are not affected by a WDT reset during SLEEP, since this reset is viewed as the resumption of normal operation. There are a few exceptions to this. The $\overline{PC}$ is always reset to all 0's (0000h). Finally, $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different reset situations as indicated in Section 3.9.1. These bits are used in software to determine the nature of reset. See Table 5.1.1 for a full description of reset states of all registers.

4.2 Power-On Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)

Power-On Reset (POR): A Power-On Reset pulse is generated on-chip when V_{DD} rise is detected (in the range of 1.2V to 1.8V). To take advantage of the POR, just tie $\overline{MCLR}$ pin directly (or through a resistor) to V_{DD}. This will eliminate external RC components usually needed to create Power-On Reset.

FIGURE 4.0.1 - SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

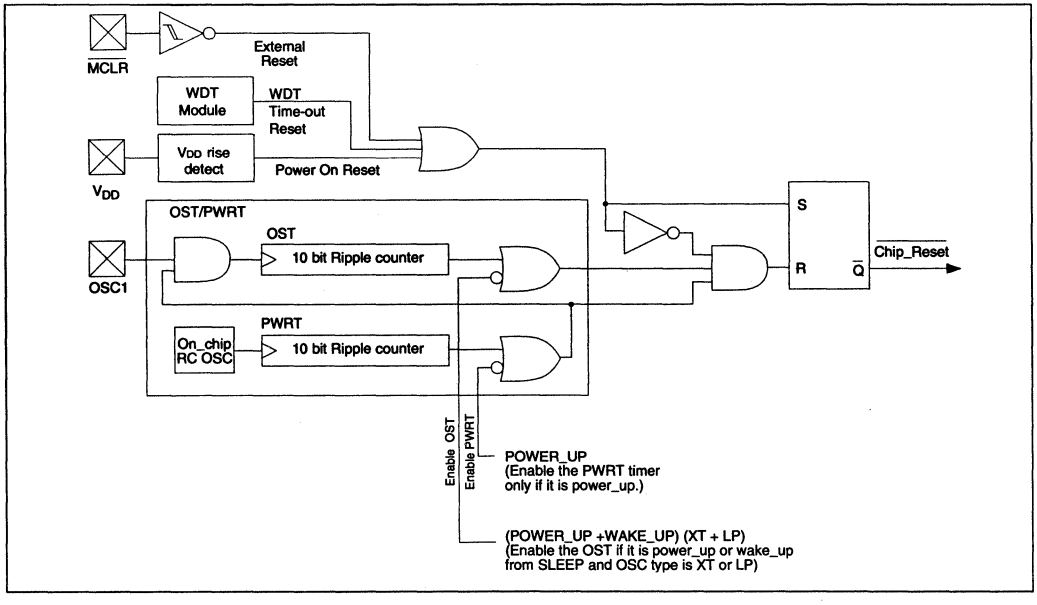


TABLE 4.1.1 - RESET CONDITIONS FOR REGISTERS

Register	Address	Power-on reset (POR)	WDT time-out reset during normal operation	WDT time-out reset during SLEEP	$\overline{MCLR}$ reset during normal operation	$\overline{MCLR}$ reset during SLEEP	Wake-up through interrupt
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
INDIR	00h	-	-	-	-	-	-
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PC	02h	0000h	0000h	PC + 1	0000h	0000h	PC + 1
STATUS	03h	0001 1xxx	0000 1uuu	uuu0 0uuu	000u uuuu	0001 0uuu	uuu1 0uuu
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PORT A	05h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TRIS A	85h	---1 1111	---1 1111	---u uuuu	---1 1111	---1 1111	---u uuuu
TRIS B	86h	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111	uuuu uuuu
OPTION	81h	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111	uuuu uuuu
EEDATA	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
EEADR	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
EECON1	88h	---0 0000	---0 ?000†	---u uuuu	---0 ?000†	---0 ?000†	---u uuuu
EECON2	89h	-	-	-	-	-	-
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu	0000 000u	0000 0000	uuuuuuuu*

Legend: - = unimplemented, reads as '0' u = unchanged x = unknown

* In the event of wake-up through interrupt, one or more of the interrupt flags will be set. Other bits in INTCON will remain unchanged.

† WRERR (bit3) will be set if reset occurred during EEPROM write.

The POR circuit does not produce internal reset when VDD declines (or goes through a brown-out).

Power-up Timer (PWRT): The power-up timer provides a fixed 72ms time-out on power-up only, from POR. The power-up timer operates on an internal RC oscillator. The chip is kept in reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration fuse, PWRTE can enable (if = 1) or disable (if = 0 or programmed) the Power-up Timer (Section 5.6).

The power-up time delay will vary from chip to chip and due to VDD and temperature. See DC parameters for details.

Oscillator Start-up Timer (OST): The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This guarantees that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-On Reset or wake-up from SLEEP.

Time-out Sequence: On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then TOST is activated. The total time-out will vary based on oscillator configuration and PWRTE fuse status. For example, in RC mode with PWRTE set to '0' (PWRT disabled), there will be no time-out at all. Figures 5.2.1, 5.2.2 and 5.2.3 depict time-out sequences. Table 5.2.1 shows time outs on power-up versus wake-up from SLEEP.

Since the time-outs occur from POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately. This is useful for testing purposes or to synchronize more than one PIC16C84 operating in conjunction.

TABLE 4.2.1 - TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Wake up from SLEEP
	PWRTE = 1	PWRTE = 0	
XT, HS, LP	72 ms + 1024 tosc	1024 tosc	1024 tosc
RC	72 ms	-	-

FIGURE 4.2.1 - TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): Case 1

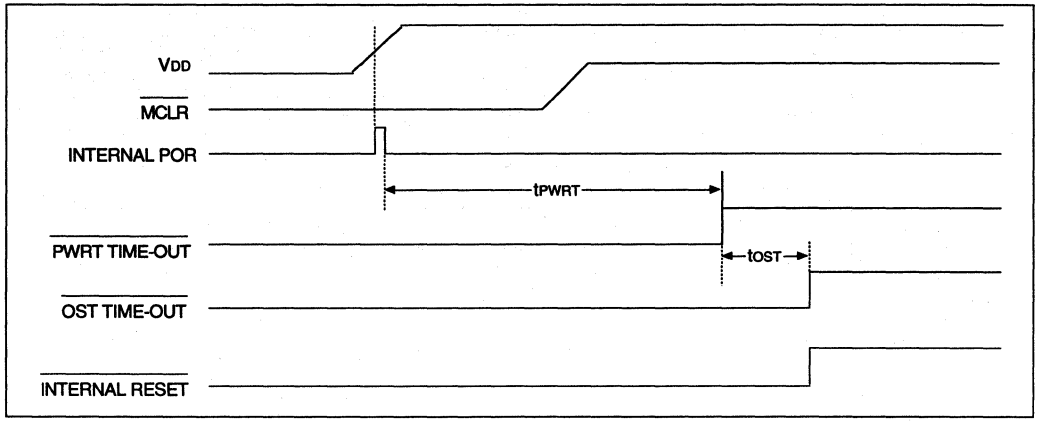


FIGURE 4.2.2 - TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): Case 2

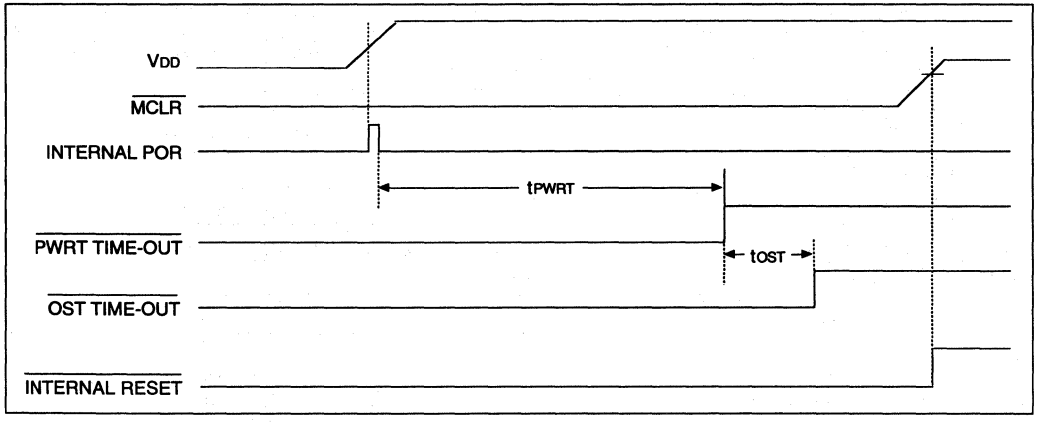


FIGURE 4.2.3 - TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

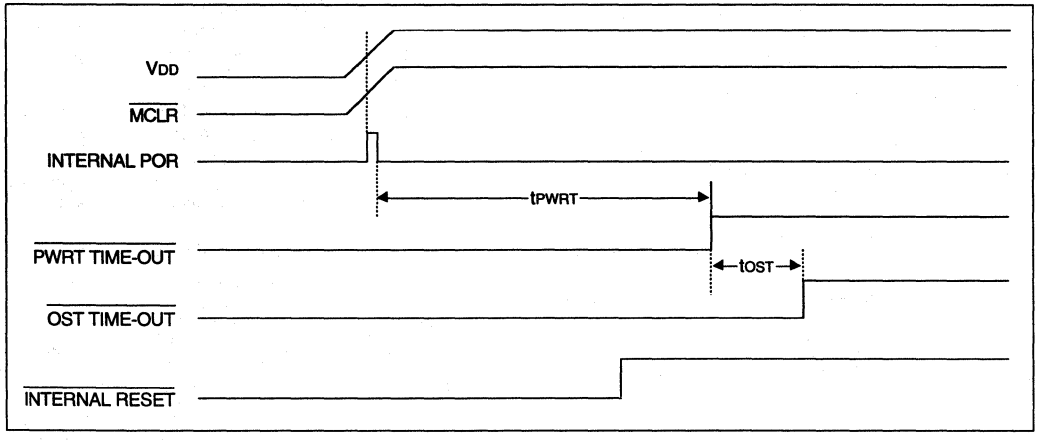
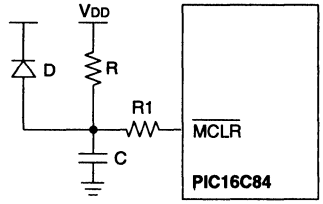
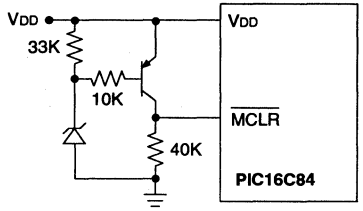


FIGURE 4.2.4 - EXTERNAL POWER ON RESET CIRCUIT



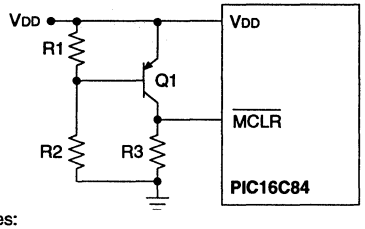
Notes:
1. External power on reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40KΩ is recommended to make sure that voltage drop across R does not exceed 0.2V (max leakage current spec on MCLR pin is 5μA). A larger voltage drop will degrade VIH level on MCLR pin.
3. R1 = 100Ω to 1KΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to ESD or EOS.

FIGURE 4.2.5 - BROWN OUT PROTECTION CIRCUIT 1



Notes:
1. This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

FIGURE 4.2.6 - BROWN OUT PROTECTION CIRCUIT 2



Notes:
1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7\ V.$$

4.3 Watchdog Timer (WDT)

The watchdog timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by programming the configuration fuse WDTE as a '0' (Section 5.6).

4.3.1 WDT PERIOD

The WDT has a nominal time-out period of 18ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The "CLRWDT" and "SLEEP" instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit $\overline{TO}$ in STATUS register will be cleared upon a Watchdog Timer timeout.

4.3.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

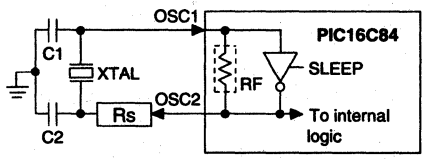
2

4.4 Oscillator Configurations

4.4.1 OSCILLATOR TYPES

The PIC16C84 can be operated in four different oscillator options. The user can program two configuration fuses (FOSC1 and FOSC0) to select one of these four modes.

FIGURE 4.4.1 - CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



Rs may be necessary in HS mode or in XT mode for AT strip-cut crystals. See Tables 5.4.1 and 5.4.2 for recommended values of C1, C2 and Rs.

TABLE 4.4.1 - CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	150 - 330 pF
	2.0 MHz	20 - 330 pF
	4.0 MHz	20 - 330 pF
HS	10.0 MHz	20 - 200 pF

Note: Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

4.4.2 CRYSTAL OSCILLATOR

In XT, HS, or LP modes a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 5.4.1).

FIGURE 4.4.2 - EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP OSC CONFIGURATION)

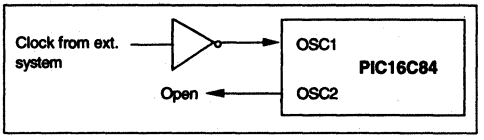


TABLE 4.4.2 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	30 pF	30-50 pF
	100 KHz	15 pF	15 pF
	200 KHz	0 - 15 pF	0 - 15 pF
XT	100 KHz	15 - 30 pF	200 - 300 pF
	200 KHz	15 - 30 pF	100 - 200 pF
	455 KHz	15 - 30 pF	15 - 100 pF
	1 MHz	15 - 30 pF	15 - 30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	10 MHz	15 pF	15 pF

Note: Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

4.4.3 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation to due tolerance of external R and C components used. Figure 4.4.3 shows how the R/C combination is connected to the PIC16C84. For Rext values below 2.2 kOhm, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 3 kOhm and 100 kOhm.

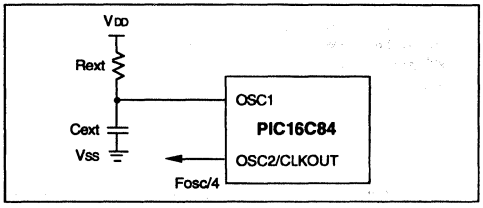
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 8.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See the characteristics in Section 8.0 for variation of oscillator frequency due to V_{DD} for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C and V_{DD} values.

In RC mode, the oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3.2.1 for timing).
The WDT is cleared when the device wakes up from SLEEP, regardless of the source of wake-up.

FIGURE 5.4.3 - RC OSCILLATOR (RC TYPE ONLY)



4.5 Power Down Mode (Sleep)

The power down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the bit $\overline{PD}$ in the STATUS register is cleared, the $\overline{TO}$ bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low or hi-impedance).

For lowest curent consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are in the High-Z mode should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC input should also be at VDD or VSS for lowest current consumption. The contribution from on chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (VIHMC).

It should be noted that a RESET generated by a WDT time out does not drive $\overline{MCLR}$ pin low.

4.5.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

a. External reset input on $\overline{MCLR}$ pin

b. Watchdog Timer time-out reset (if WDT was enabled)

c. Interrupt from INT pin, RB port change or data EEPROM write completion.

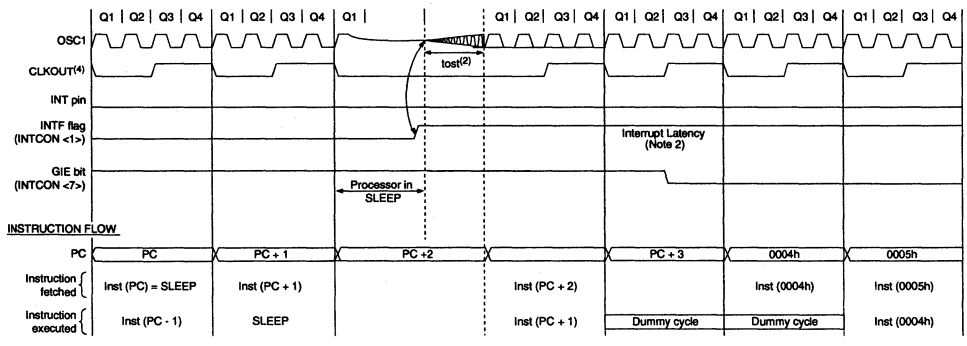
The first event will cause a device reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. $\overline{PD}$ bit, which is set on power-up is cleared when SLEEP is invoked. $\overline{TO}$ bit is cleared if WDT time-out occurred (and caused wake-up).

When the `SLEEP` instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the GIE bit is set (enabled), the device executes the instruction after the `SLEEP` instruction and the branches to the interrupt address (0004h). In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

Note: If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake from sleep.

The WDT is cleared when the device wakes-up from sleep, regardless of the source of wake-up.

FIGURE 4.5.1.1 - WAKE UP FROM SLEEP THROUGH INTERRUPT



Notes:
1. XT, HS or LP oscillator mode assumed
2. tost = 1024 tosc (drawing not to scale). This delay will not be there for RC osc mode.
3. GIE = 1 assumed. In this case after wake up processor jumps to interrupt routine. If GIE = 0, execution will continue in line.
4. CLKOUT is not available in these osc modes, but shown here for timing reference.

4.6 Configuration Fuses

The PIC16C84 has five configuration fuses which are EEPROM bits. These fuses can be programmed (reads '0') or left unprogrammed (reads '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh). However, through a special mode, this location can be accessed during programming.

See the description of fuses in Figure 4.6.1.

4.7 ID Locations

The PIC16C84 has four ID locations (2000h - 2003h) mapped in the test program memory for storing code revision number, manufacturing information or other useful information. As with the configuration word, these locations are readable and writable through a programmer. They are not accessible during normal code execution.

If the chip is code protected, it is recommended that the user uses only the lower seven bits of the ID locations and program the higher seven bits as '0'. This way the ID locations will be readable even after code protection.

4.8 Code Protection

The code in the program memory can be protected by blowing the code protect fuse (CP).

When code protected, the contents of the program memory cannot be read out in a way that the program code can be reconstructed. In addition, all memory locations are protected against programming.

The code protected data EEPROM can be read and updated by the CPU in normal operation. All EEPROM data memory locations can not be programmed nor can they be read out in normal operation (ie, programming modes, test modes).

Once code protected, the CP fuse can be erased only through a chip erase. A chip erase will erase EEPROM program and data memory before erasing the code-protect fuse. Refer to PIC16C84 programming specification for details.

4.8.1 VERIFYING A CODE-PROTECTED PART

When code protected verifying any program memory location will read a scrambled output which looks like "0000000xxxxxxx" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

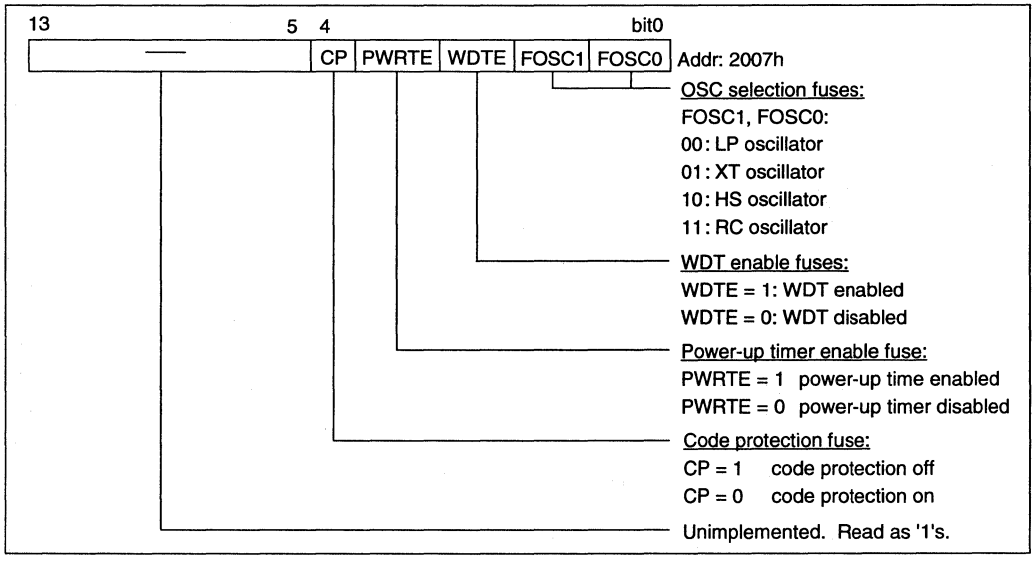
a. First, program and verify a good device without code protecting it.

b. Next, blow its code protection fuse and then load its contents in a file.

c. Verify any code-protected PIC16C84 against this file.

EEPROM data memory can not be verified after code protection. The user can embed code for self testing the data memory in the program.

FIGURE 4.6.1 - CONFIGURATION WORD



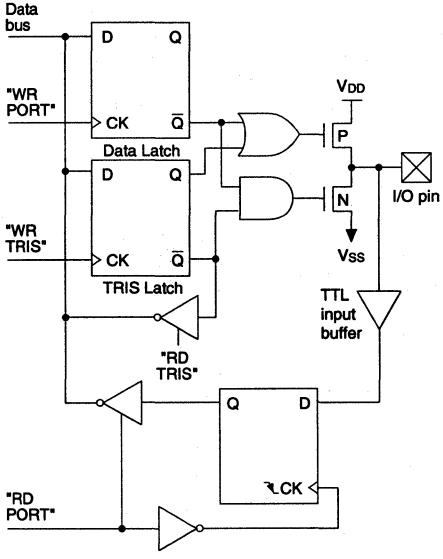
5.0 OVERVIEW OF PERIPHERALS

The PIC16C84 has 13 I/O pins organized as two I/O ports, PORTA (5 bit) and PORTB (8-bit). There is one general purpose timer/counter, TMR0 which 8-bit wide with 8-bit programmable prescaler. It is separate from the Watchdog Timer. The PIC16C84 also has a 64 x 8 EEPROM data memory accessible through an 8-bit data register and address register.

5.1 PORTA

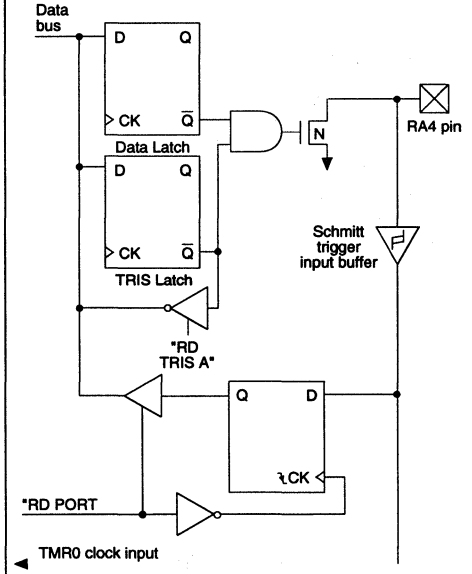
PORTA is a 5-bit wide port with pins RA<4:0>. Port pins RA<3:0> are bidirectional whereas RA4 has a open-collector output. PortA is file register 05h. Its corresponding direction control register TRISA is mapped in page 1 of register file at address 85h. TRISA is a five-bit wide register with bits <4:0> physically implemented. Refer to Figures 5.1.1 and 5.1.2 for block diagrams of PORTA pins.

FIGURE 5.1.1 - BLOCK DIAGRAM OF RA0 - RA3 PINS



Note 1: I/O pins have protection diodes to VDD and VSS.

FIGURE 5.1.2 - BLOCK DIAGRAM OF RA4 PIN



Note 1: I/O pins have protection diodes to VSS.

TABLE 5.1.1 - PORTA FUNCTIONS

Port Pin	Bit	Pin Function	Alternate Function
RA0	bit0	Input/output port. TTL input levels	-
RA1	bit1	Input/output port. TTL input levels	-
RA2	bit2	Input/output port. TTL input levels	-
RA3	bit3	Input/output port. TTL input levels	-
RA4/T0CKI	bit4	Input/output port. Output is open collector type. Input is Schmitt trigger type.	External clock input for TMR0 timer/counter

TABLE 5.1.2 - SUMMARY OF PORTA REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTA	PORTA pins when read PORTA latch when written	05h	---x xxxx
TRISA	PORTA data direction register	85h	---1 1111

Notes: 1: x = unknown, - = unimplemented, reads as a '0'.
2: For reset values of registers in other reset situations refer to table 5.1.1.

5.2 PORTB

PORTB is an 8-bit wide bidirectional port (file register address 06h). The corresponding data direction register is TRISB (address 86h). A '1' in TRISB sets the corresponding port pin as an input. Reading PORTB register reads the status of the pins whereas writing to it will write to the port latch. See Figures 5.2.1 and 5.2.2 for block diagrams of the PORTB pins.

Each of the PORTB pins has a weak internal pull-up (~100 µA typical). The weak pull-up is automatically turned off if the port pin is configured as an output. Furthermore, a single control bit RBPU (OPTION<7>) can turn off (RBPU is set) all the pull-ups. The pull-ups are disabled on Power-On Reset.

PORTB has an interrupt on change feature on four of its pins, RB<7:4>. When configured as input, the inputs on these pins are sampled and latched on the Q1 cycle of a read. The new input is compared with the old latched value in every instruction cycle. An active high output is generated on mismatch between the pin and the latch. The "mismatch" outputs of RB4, RB5, RB6 and RB7 are OR'ed together to generate the RBIF interrupt (latched in INTCON<0>. Any pin configured as output is excluded from the comparison. This interrupt can wake the chip up from SLEEP. The user, in interrupt service routine can clear the interrupt in one of two ways:

a) Disable the interrupt by clearing RBIE INTCON<3> bit.

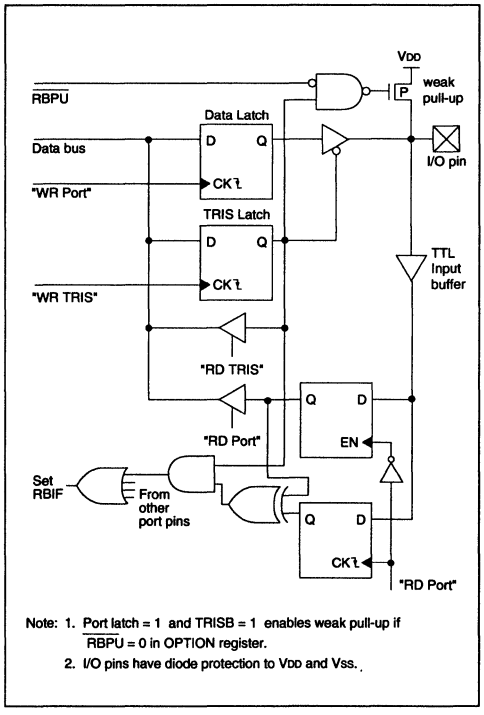
b) Read PORTB. This will end mismatch condition, then clear RBIF bit.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression.

Finally, port pin RB0 is multiplexed with external interrupt input INT.

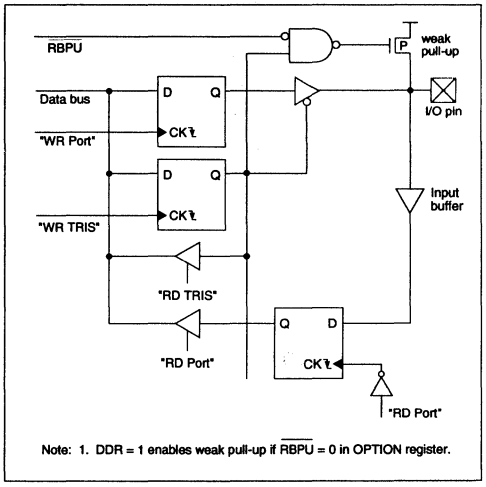
2

FIGURE 5.2.1 - BLOCK DIAGRAM OF PORT PINS RB<7:4>



Note: 1. Port latch = 1 and TRISB = 1 enables weak pull-up if $\overline{RBPU}$ = 0 in OPTION register.
2. I/O pins have diode protection to VDD and VSS.

FIGURE 5.2.2 - BLOCK DIAGRAM OF PORT PINS RB<3:0>



Note: 1. DDR = 1 enables weak pull-up if $\overline{RBPU}$ = 0 in OPTION register.

TABLE 5.2.1 - PORTB FUNCTIONS

Port Pin	Bit	Pin Function	Alternate Function
RB0/INT	bit0	Input/output port pin. TTL input levels and internal software programmable weak pull-up	External interrupt input
RB1	bit1	Input/output port pin. TTL input levels and internal software programmable weak pull-up	-
RB2	bit2	Input/output port pin. TTL input levels and internal software programmable weak pull-up	-
RB3	bit3	Input/output port pin. TTL input levels and internal software programmable weak pull-up	-
RB4	bit4	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change
RB5	bit5	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change
RB6	bit6	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change
RB7	bit7	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change

TABLE 5.2.2 - SUMMARY OF PORTB REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTB	PORTB pins when read PORTB latch when written	06h	xxxx xxxx
TRISB	PORTB data direction register	86h	1111 1111
OPTION	Weak pull-up on/off control ($\overline{RBPU}$ bit)	88h	1111 1111

5.3 I/O Programming Considerations

5.3.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit 5 and PORTB is re-output to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

Reading the PORT register, reads the values of the PORT pins. Writing to the PORT register writes the value to the PORT latch. When using read modify write instructions (ex. BCF, BSF, etc.) on a PORT, the value of the PORT pins is read, the desired operation is done to this value, and this value is then written to the PORT latch.

Example 5-1 shows the effect of two sequential read modify write instructions (ex. BCF, BSF, etc.) on an I/O PORT.

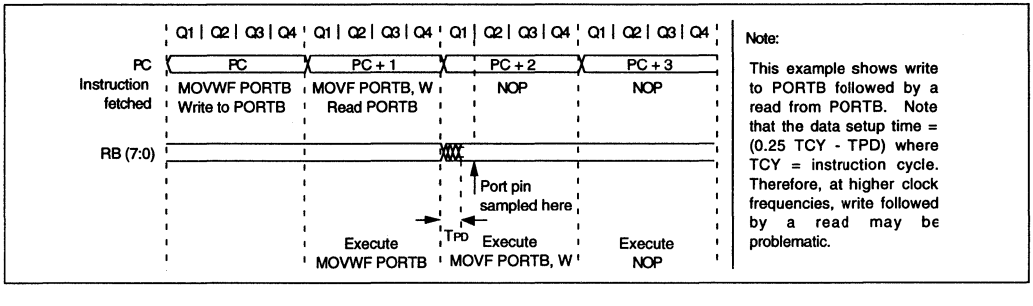
EXAMPLE 5-1: READ MODIFY WRITE INSTRUCTIONS ON AN I/O PORT

```
; Initial PORT settings:  PORTB<7:4> Inputs
;                         PORTB<3:0> Outputs
; PORTB<7:6> have external pull-up and are not
; connected to other circuitry.
;
;                           PORT latch   PORT pins
;                           ----------   ----------
      BCF     PORTB, 7    ; 01pp pppp    11pp pppp
      BCF     PORTB, 6    ; 10pp pppp    11pp pppp
      BSF     STATUS, RP0 ;
      BCF     TRISB, 7    ; 10pp pppp    11pp pppp
      BCF     TRISB, 6    ; 10pp pppp    10pp pppp
;
; Note that the user may have expected the pin
; values to be 00pp pppp. The 2nd BCF caused RB7
; to be latched as the pin value (High).
```

5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see Figure 4.5.2.1). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

FIGURE 5.3.1 - SUCCESSIVE I/O OPERATION



5.4 TIMER0 (TMR0) Module

The TMR0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable (file address 01h)
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

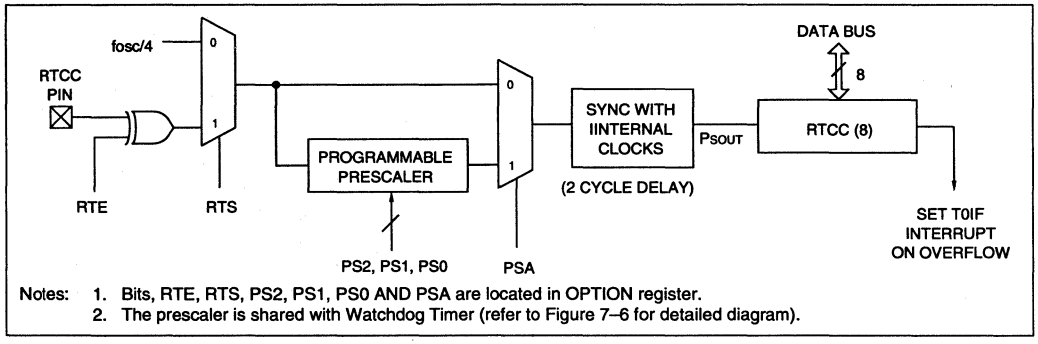
Figure 5.4.1 is a simplified block diagram of the TMR0 module.

Timer mode is selected by clearing the RTS bit (OPTION<5>). In timer mode, the TMR0 module will increment every instruction cycle (without prescaler). If TMR0 is written, increment is inhibited for the following two cycles (see Figures 5.4.2 and 5.4.3). The user can work around this by writing an adjusted value to the TMR0 module.

Counter mode is selected by setting the RTS bit (OPTION<5>). In this mode TMR0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by control bit RTE (OPTION<4>). Clearing the RTE bit selects the rising edge. Restrictions on the external clock input is discussed in detail in Section 5.4.2.

The prescaler is shared between the TMR0 module and the watchdog timer. The prescaler assignment is controlled in software by control bit, PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to TMR0. The prescaler is not readable or writable. When the prescaler is assigned to the TMR0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 5.4.3 details the operation of the prescaler.

FIGURE 5.4.1: TIMER0 (TMR0) BLOCK DIAGRAM



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 AND PSA are located in OPTION register.
2. The prescaler is shared with Watchdog Timer (refer to Figure 7–6 for detailed diagram).

FIGURE 5.4.2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALE

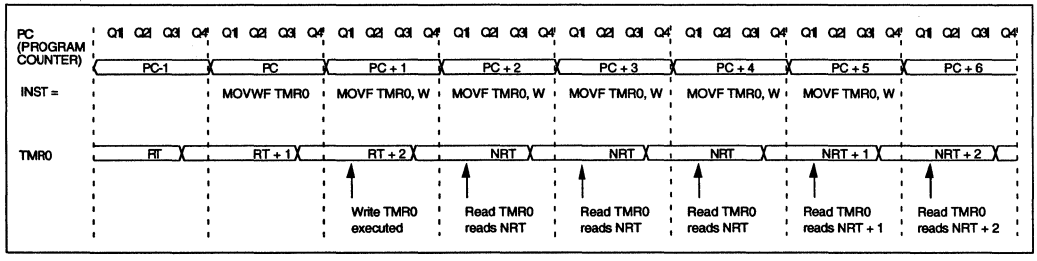
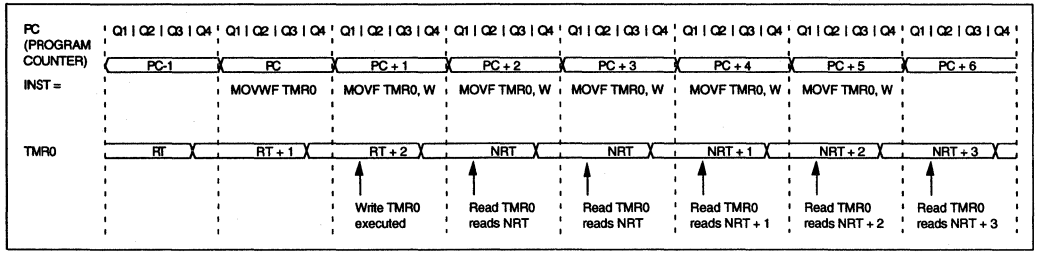


FIGURE 5.4.3: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/PRESCALE 1:2



5.4.1 TIMER0 (TMR0) INTERRUPT

TMR0 interrupt is generated when the TMR0 module timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the TMR0 module interrupt service routine before re-enabling this interrupt. The TMR0 module interrupt can not wake the processor from SLEEP since the timer is shut off during SLEEP. See Figure 5.4.4 for TMR0 interrupt timing.

5.4.2 USING TMR0 WITH EXTERNAL CLOCK

When external clock input is used for TMR0, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements.

Also, there is some delay from the occurance of the external clock edge to the actual incrementing of TMR0. Referring to Figure 5.4.5, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where:

tosc = oscillator time period.

When no prescaler is used, PSOUT (Prescaler output, see Figure 4.2.1) is the same as TMR0 clock input and therefore the requirements are:

T_{RTH} = TMR0 high time ≥ 2tosc + ΔT (See parameter #40)

T_{RTL} = TMR0 low time ≥ 2tosc + ΔT (See parameter #41)

When prescaler is used, the TMR0 module input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.

Then:

$$P_{SOUT}\text{ high time} = P_{SOUT}\text{ low time} = \frac{N \bullet T_{RT}}{2}$$

where

T_{RT} = TMR0 input period

N = prescale value (2, 4, ..., 256).

The requirement is, therefore:

$$\frac{N \bullet T_{RT}}{2} \geq 2\,tosc + \Delta T, \text{ or } T_{RT} \geq \frac{4\,tosc + 2\,\Delta T}{N}$$

where

ΔT = small RC delay (see Timing Specifications).

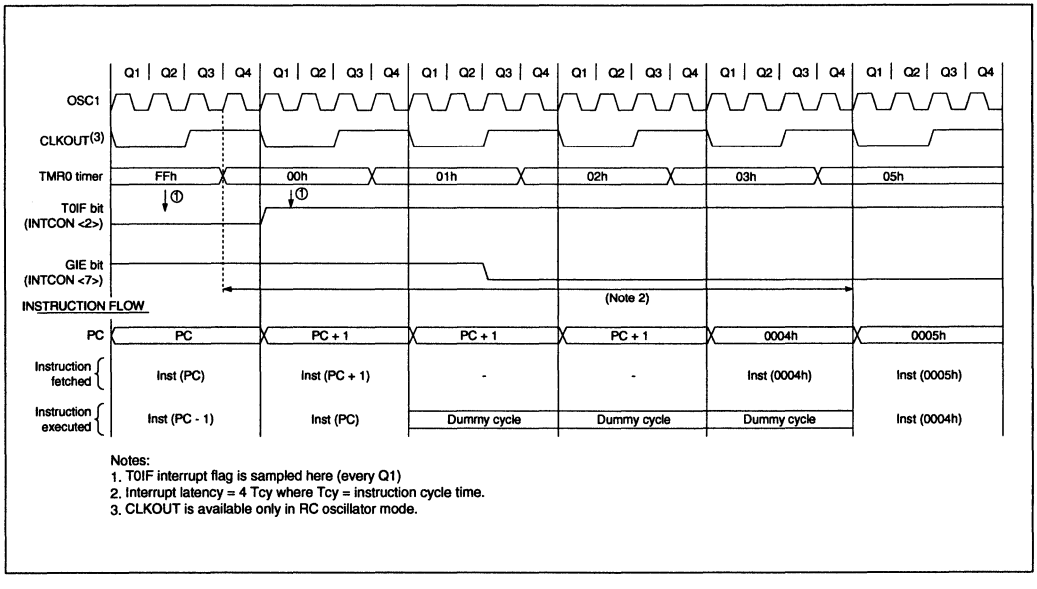
The user will notice that no requirement on TMR0 high time or low time is specified. However, if the high time or low time on TMR0 is too small then the pulse may not be detected, hence a minimum high or low time of 10 ns is required. In summary, the TMR0 module input requirements are:

T_{RT} = TMR0 period ≥ (4 tosc + 2 ΔT)/N

T_{RTH} = TMR0 high time ≥ ΔT

T_{RTL} = TMR0 low time ≥ ΔT

FIGURE 5.4.4: TIMER0 (TMR0) INTERRUPT TIMING



Notes:
1. T0IF interrupt flag is sampled here (every Q1)
2. Interrupt latency = 4 Tcy where Tcy = instruction cycle time.
3. CLKOUT is available only in RC oscillator mode.

Delay from external clock edge: Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 module is actually incremented. Referring to Figure 5.4.5, the reader can see that this delay is between 3 tosc and 7 tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±200ns @ 20 MHz).

5.4.3 PRESCALER

An 8-bit counter is available as a prescaler for the TMR0 module, or as a post-scaler for the Watchdog Timer, respectively (see Figure 5.4.6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the TMR0 module and the Watchdog Timer. Thus, a prescaler assignment for the TMR0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2-PS0 bits (OPTION<3:0>) determine the prescaler assignment and pre-scale ratio.

When assigned to the TMR0 module, all instructions writing to the TMR0 module (e.g. `CLRF TMR0`, `MOVWF TMR0`, `BSF TMR0,x` ....etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 5.4.5: TIMER0 TIMING WITH EXTERNAL CLOCK

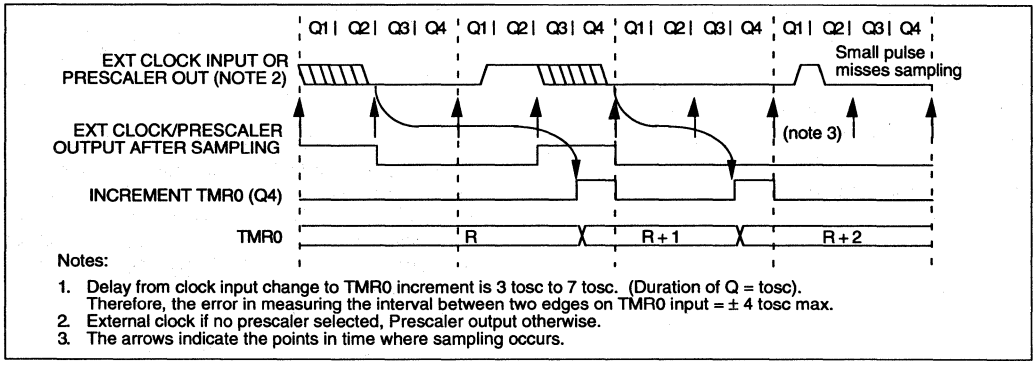
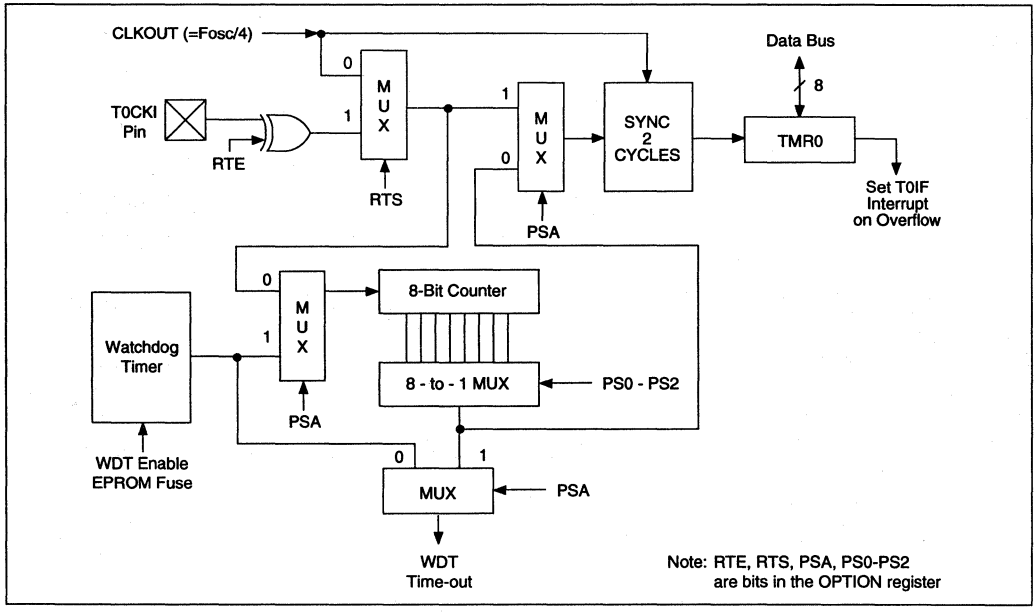


FIGURE 5.4.6: BLOCK DIAGRAM OF THE TMR0/WDT PRESCALER



5.4.4 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence (shown in Example 5-2) must be executed when changing the prescaler assignment from TMR0 to WDT. Depending on the selected prescaler value (lines 1 and 2) determines if lines 7 and 8 are required:

EXAMPLE 5-2: CHANGING PRESCALER (TMR0→WDT)

```
1. BCF     STATUS, RP0   ;Bank 0
2. CLRF    TMR0          ;Clear TMR0
3. BSF     STATUS, RP0   ;Bank 1
4. CLRWDT                ;Clears WDT and
                         ;   prescale
5. MOVLW   B'xxxx1xxx'   ;Select new prescale
6. MOVWF   OPTION        ;   value
7. BCF     STATUS, RP0   ;Bank 0
```

Steps 1 and 2 are only required if an external TMR0 source is used. Steps 7 and 8 are necessary only if the desired prescale value is '000' or '001'.

To change prescaler from the WDT to the TMR0 module use the sequence shown in Example 7-3. This precaution must be taken even if the WDT is disabled.

EXAMPLE 5-3: CHANGING PRESCALER (WDT→TMR0)

```
1. CLRWDT                ;Clear WDT and
                         ;prescaler
2. MOVLW B'xxxx0xxx'     ;Select TMR0, new
                         ;prescale value and
                         ;clock source
3. MOVWF OPTION          ;
```

2

TABLE 5.4.1: SUMMARY OF TMR0 REGISTERS

Register Name	Function	Address	Power-on Reset Value
TMR0	Timer/counter register	01h	XXXX XXXX
OPTION	Configuration and prescaler assignment bits for TMR0. See Figure 4-4	81h	1111 1111
INTCON	TMR0 overflow interrupt flag and mask bits See Figure 4-5	0Bh	0000 000X

TABLE 5.4.2: REGISTERS ASSOCIATED WITH TMR0

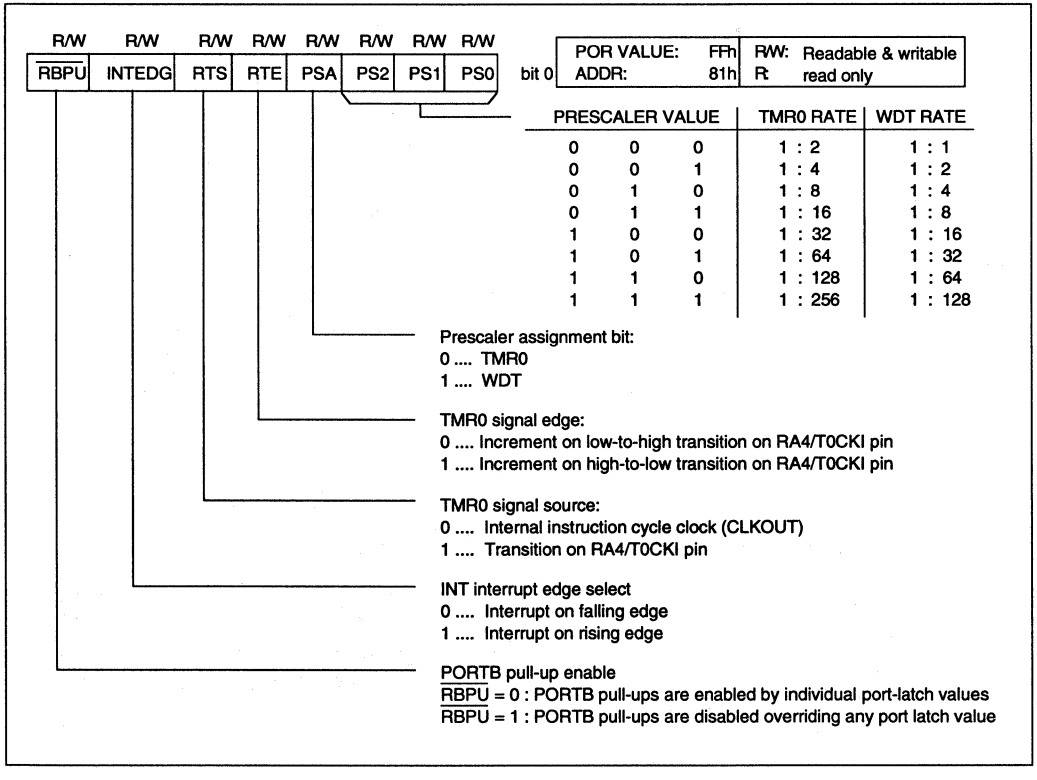
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01	TMR0	TIMER0							
0B/8B	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
81	OPTION	RBPU	INTEDG	RTS	RTE	PSA	PS2	PS1	PS0
85	TRISA	—	—	TRISA 5	TRISA 4	TRISA 3	TRISA 2	TRISA 1	TRISA 0

Legend — = Unimplemented locations, Read as '0'
Shaded boxes are not used by TMR0 module.

5.5 OPTION Register

The OPTION register (address 81h) is a readable and writable register which contains various control bits to configure the prescaler, the external INT interrupt edge select, the TMR0 and the weak pull-ups on PORTB.

FIGURE 5.5.1 - OPTION REGISTER



5.6 EEPROM Data Memory

The PIC16C84 has 64x8 EEPROM data memory which is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead it is accessed through two registers: EEDATA<08h> which holds the 8-bit data for read/write, EEADR<09h> which holds the address of the EEPROM location being accessed. The 64 bytes are in the address range 0h - 63h. Additionally, there are two control registers: EECON1<88h> and EECON2<89h>.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is nominally 10 ms, and is controlled by an on-chip timer. The actual write-time will vary with voltage and temperature as well as from chip to chip. Please refer to AC specifications for exact limits.

5.6.1 EECON1 AND EECON2 REGISTERS

EECON1 (address 88h) is the control register with five low order bits physically implemented. The upper-three bits are non-existent and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits can only be set in software. They are reset in hardware at completion of read or write operation. Inability to clear WR bit in software prevents accidental termination of a write operation prematurely.

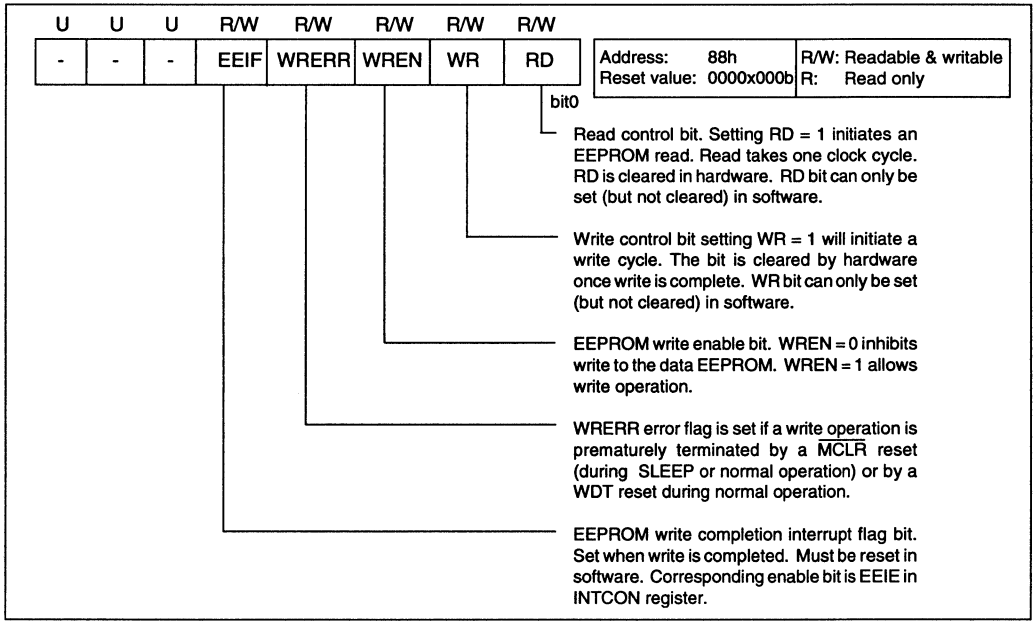
WREN bit, when set will allow a write operation. On power-up WREN = 0. WRERR bit is set when a write operation is interrupted by MCLR reset or a WDT time-out reset during normal operation. In these situations, following reset the user can check for WRERR bit and rewrite the location. The data and address will be unchanged in EEDATA and EEADR registers.

EEIF bit is the interrupt flag set when write is complete. It must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read '0's.

2

FIGURE 5.6.3.1 - EECON1 REGISTER



5.6.2 READING THE EEPROM DATA MEMORY

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>). The data is available in the very next cycle in the EEDATA register; therefore it can be read in the next instruction. EEDATA will hold this value until another read or until it is written to by the user (during a write operation).

5.6.3 WRITING TO THE EEPROM DATA MEMORY

To write an EEPROM data location, the user must first write the address to EEADR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate write:

```
movlw  55h
movwf  EECON2
movlw  AAh
movwf  EECON2
bsf    EECON1,WR  ;set WR bit
                  ;begin write
```

Write will not initiate if this sequence (write 55h to EECON2, write AAh to EECON2, then set WR bit) is not followed with exact timing. The user must disable interrupts during this code segment.

Additionally WREN bit in EECON1 must be set to enable write. This mechanism is to prevent accidental writes to data EEPROM due to errant (unexpected) code execution i.e. lost programs. The user is recommended to keep WREN off at all times except when updating EEPROM. Furthermore, the code segments that enables WREN and initiates write should be kept at separate locations to prevent accidental execution of both of them in the event of a software malfunction.

At the end of the write, the WR bit is cleared in hardware and the EE write complete interrupt flag is set (bit EEIF). The user can either enable this interrupt or poll this bit. EEIF must be cleared in software.

5.6.4 PROTECTION AGAINST SPURIOUS WRITE

Various mechanisms are built in to prevent spurious EEPROM write. On power-up WREN is cleared. Also, the power-up timer (72ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during brown-out or power glitch or software malfunction.

TABLE 5.6.2 - SUMMARY OF EEPROM REGISTERS

Register Name	Function	Address	Power-on-Reset Value
EEDATA	EEPROM data register	08h	XXXX XXXX
EEADR	EEPROM address register	09h	XXXX XXXX
EECON1	EEPROM control register1	88h	0000 X000
EECON2	EEPROM control register2	89h	-

6.0 PROGRAMMING THE PIC16C84

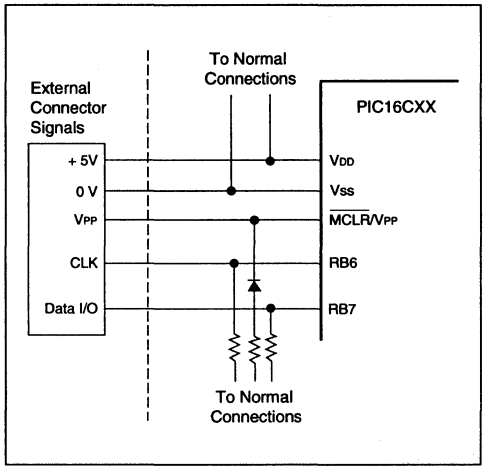
The PIC16CXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and date and three other lines for power, ground and programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low while raising the MCLR (vpp) pin from Vil to Vihh. RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are schmidt trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program date are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16CXX Programming Specifications (Literature #DS30189).

A typical in-system serial programming connection is shown in Figure 6-1.

FIGURE 6.1: TYPICAL IN-SYSTEM SERIAL PROGRAMMING CONNECTION



7.0 INSTRUCTION SET SUMMARY

Each PIC16CXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 7-2 lists byte-oriented, bit-oriented, and literal and control operations. Table 7-1 shows the opcode field descriptions.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which file register is to be utilized by the instruction.

The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an 8- or 11-bit constant or literal value.

TABLE 7.1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8 bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
PCLATH	Program Counter High Latch
GIE	Global Interrupt Enable Bit
WDT	Watchdog Timer Counter
$\overline{TO}$	Time-out Bit
$\overline{PD}$	Power-down Bit
dest	Destination either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term

The instruction set is highly orthogonal and is grouped into three basic categories:

- Byte oriented operations
- Bit oriented operations
- Literal and control operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Table 7-2 lists the instructions recognized by the MPASM assembler.

Figure 7-1 shows the three general formats that the instructions can have.

Note: To maintain upward compatibility with future PIC16CXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexidecimal number:

0xhh

where h signifies a hexidecimal digit.

FIGURE 7.1: GENERAL FORMAT FOR INSTRUCTIONS

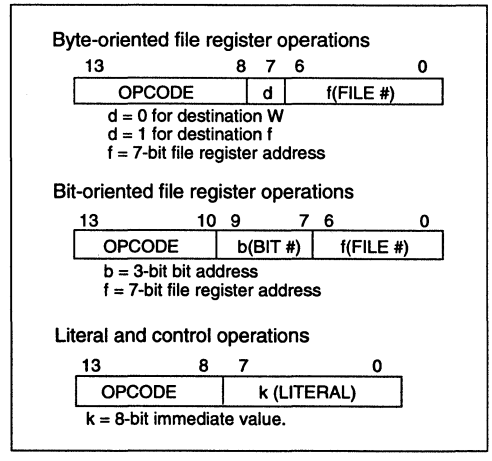


TABLE 7.2: INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode msb	lsb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS							
ADDWF	**f, d**	Add W and f	1	00 0111	dfff ffff	C, DC, Z	1, 2
ANDWF	**f, d**	AND W and f	1	00 0101	dfff ffff	Z	1, 2
CLRF	**f**	Clear f	1	00 0001	1fff ffff	Z	2
CLRW	**-**	Clear W	1	00 0001	0xxx xxxx	Z	
COMF	**f, d**	Complement f	1	00 1001	dfff ffff	Z	1, 2
DECF	**f, d**	Decrement f	1	00 0011	dfff ffff	Z	1, 2
DECFSZ	**f, d**	Decrement f, Skip if 0	1 (2)	00 1011	dfff ffff		1, 2, 3
INCF	**f, d**	Increment f	1	00 1010	dfff ffff	Z	1, 2
INCFSZ	**f, d**	Increment f, Skip if 0	1 (2)	00 1111	dfff ffff		1, 2, 3
IORWF	**f, d**	Inclusive OR W and f	1	00 0100	dfff ffff	Z	1, 2
MOVF	**f, d**	Move f	1	00 1000	dfff ffff	Z	1, 2
MOVWF	**f**	Move W to f	1	00 0000	1fff ffff		
NOP	**-**	No Operation	1	00 0000	0xx0 0000		
RLF	**f, d**	Rotate left f through carry	1	00 1101	dfff ffff	C	1, 2
RRF	**f, d**	Rotate right f through carry	1	00 1100	dfff ffff	C	1, 2
SUBWF	**f, d**	Subtract W from f	1	00 0010	dfff ffff	C, DC, Z	1, 2
SWAPF	**f, d**	Swap halves f	1	00 1110	dfff ffff		1, 2
XORWF	**f, d**	Exclusive OR W and f	1	00 0110	dfff ffff	Z	1, 2
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF	**f, b**	Bit Clear f	1	01 00bb	bfff ffff		1, 2
BSF	**f, b**	Bit Set f	1	01 01bb	bfff ffff		1, 2
BTFSC	**f, b**	Bit Test f, Skip if Clear	1 (2)	01 10bb	bfff ffff		3
BTFSS	**f, b**	Bit Test f, Skip if Set	1 (2)	01 11bb	bfff ffff		3
LITERAL AND CONTROL OPERATIONS							
ADDLW	**k**	Add literal to W	1	11 111x	kkkk kkkk	C, DC, Z	
ANDLW	**k**	AND literal to W	1	11 1001	kkkk kkkk	Z	
CALL	**k**	Call subroutine	2	10 0kkk	kkkk kkkk		
CLRWDT	**-**	Clear watchdog timer	1	00 0000	0110 0100	$\overline{TO}$, $\overline{PD}$	
GOTO	**k**	Go to address	2	10 1kkk	kkkk kkkk		
IORLW	**k**	Inclusive OR literal to W	1	11 1000	kkkk kkkk	Z	
MOVLW	**k**	Move literal to W	1	11 00xx	kkkk kkkk		
RETFIE	**-**	Return from interrupt	2	00 0000	0000 1001		
RETLW	**k**	Return with literal in W	2	11 01xx	kkkk kkkk		
RETURN	**-**	Return from subroutine	2	00 0000	0000 1000		
SLEEP	**-**	Go into standby mode	1	00 0000	0110 0011	$\overline{TO}$, $\overline{PD}$	
SUBLW	**k**	Subtract W from literal	1	11 110x	kkkk kkkk	C, DC, Z	
XORLW	**k**	Excl. OR literal to W	1	11 1010	kkkk kkkk	Z	

Notes: 1. When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2. If this instruction is executed on the TMR0 register (and, where applicable, d=1), the prescaler will be cleared if assigned to the TMR0.

3. If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

7.1 Instruction Descriptions

ADDLW Add Literal to W

Syntax: [*label*] ADDLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) + k → W

Status Affected: C, DC, Z

Encoding:

11	111X	kkkk	kkkk

Description: The contents of the W register are added to the 8-bit literal "k" and the result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ADDLW   0x15
```
Before Instruction
W = 0x10

After Instruction
W = 0x25

ANDLW AND Literal and W

Syntax: [*label*] ANDLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .AND. (k) → W

Status Affected: Z

Encoding:

11	1001	kkkk	kkkk

Description: The contents of W register are AND'ed with the 8-bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ANDLW   0x5F
```
Before Instruction
W = 0xA3

After Instruction
W = 0x03

ADDWF ADD W to f

Syntax: [*label*] ADDWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

00	0111	dfff	ffff

Description: Add the contents of the W register to register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
ADDWF   FSR, 0
```
Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0xD9
FSR = 0xC2

ANDWF AND W with f

Syntax: [*label*] ANDWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (W) .AND. (f) → dest

Status Affected: Z

Encoding:

00	0101	dfff	ffff

Description: AND the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
ANDWF   FSR, 1
```
Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0x17
FSR = 0x02

BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: 0 → f<b>

Status Affected: None

Encoding:

01	00bb	bfff	ffff

Description: Bit "b" in register "f" is reset to 0.

Words: 1

Cycles: 1

Example:
```
BCF     FLAG_REG, 7
```
Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47

BSF **Bit Set f**

Syntax: [*label*] BSF f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: 1 → f<b>

Status Affected: None

Encoding:

01	01bb	bfff	ffff

Description: Bit "b" in register "f" is set to 1.

Words: 1

Cycles: 1

Example:
```
BSF     FLAG_REG, 7
```
Before Instruction
FLAG_REG = 0x0A
After Instruction
FLAG_REG = 0x8A

BTFSC **Bit Test, skip if Clear**

Syntax: [*label*] BTFSC f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

01	10bb	bfff	ffff

Description: If bit 'b' in register 'f' is '0' then the next instruction is skipped.

If bit 'b' is '0', the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address HERE
After Instruction
if FLAG<1> = 0, PC = address TRUE
if FLAG<1> = 1, PC = address FALSE

BTFSS **Bit Test, skip if Set**

Syntax: [*label*] BTFSS f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

01	11bb	bfff	ffff

Description: If bit "b" in register "f" is "1" then the next instruction is skipped.

If bit '"b" is "0", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address HERE
After Instruction
if FLAG<1> = 0, PC = address FALSE
if FLAG<1> = 1,PC = address TRUE

CALL — Subroutine Call

Syntax: [*label*] CALL k

Operands: 0 ≤ k ≤ 2048

Operation: (PC) + 1 → TOS,
k → PC<10:0>,
(PCLATH<4:3>) → PC<12:11>;

Status Affected: None

Encoding:

10	0kkk	kkkk	kkkk

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The 11-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH (f03). CALL is a two-cycle instruction.

Words: 1

Cycles: 2

Example:
```
HERE    CALL    THERE
```
Before Instruction
PC = Address HERE
After Instruction
PC = Address THERE
TOS = Address HERE

CLRF — Clear f

Syntax: [*label*] CLRF f

Operands: 0 ≤ f ≤ 127

Operation: 00h → f
1 → Z

Status Affected: Z

Encoding:

00	0001	1fff	ffff

Description: The contents of register "f" are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example:
```
CLRF    FLAG_REG
```
Before Instruction
FLAG_REG = 0x5A
After Instruction
FLAG_REG = 0x00
Z = 1

CLRW — Clear W Register

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W)
1 → Z

Status Affected: Z

Encoding:

00	0001	0XXX	XXXX

Description: W registered is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example:
```
CLRW
```
Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

CLRWDT — Clear Watchdog Timer

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0100

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example:
```
CLRWDT
```
Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescale = 0
$\overline{TO}$ = 0
$\overline{PD}$ = 0

COMF Complement f

Syntax: [*label*] COMF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: $\overline{(f)} \rightarrow$ (dest)

Status Affected: Z

Encoding:

00	1001	dfff	ffff

Description: The contents of register "f" are complemented. If "d" is 0 the result is stored in W. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
COMF    REG1, 0
```
Before Instruction
REG1 = 0x13

After Instruction
REG1 = 0x13
W = 0xEC

DECF Decrement f

Syntax: [*label*] DECF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f)-1 → (dest)

Status Affected: Z

Encoding:

00	0011	dfff	ffff

Description: Decrement register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
DECF    CNT, 1
```
Before Instruction
CNT = 0x01
Z = 0

After Instruction
CNT = 0x00
Z = 1

DECFSZ Decrement f, skip if 0

Syntax: [*label*] DECFSZ f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - 1 → d; skip if result = 0

Status Affected: None

Encoding:

00	1011	dfff	ffff

Description: The contents of register "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Example:
```
HERE    DECFSZ    CNT, 1
          GOTO      LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address HERE

After Instruction
CNT = CNT - 1
if CNT = 0, PC = address CONTINUE
if CNT ≠ 0, PC = address HERE + 1

GOTO Unconditional Branch

Syntax: [*label*] GOTO k

Operands: $0 \le k \le 2048$

Operation: k → PC<10:0>,
(PCLATH<4:3>) → PC<12:11>

Status Affected: None

Encoding:

10	1kkk	kkkk	kkkk

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH <4:3>. GOTO is a two-cycle instruction.

Words: 1

Cycles: 2

Example:
```
GOTO THERE
```
After Instruction
PC = Address of THERE

INCF — Increment f

Syntax: [*label*] INCF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (dest)

Status Affected: Z

Encoding:

00	1010	dfff	ffff

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

Words: 1

Cycles: 1

Example:
```
INCF    CNT, 1
```
Before Instruction
CNT = 0xFF
Z = 0

After Instruction
CNT = 0x00
Z = 1

INCFSZ — Increment f, skip if 0

Syntax: [*label*] INCFSZ f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (dest), skip if result = 0

Status Affected: None

Encoding:

00	1111	dfff	ffff

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Example:
```
HERE    INCFSZ  CNT, 1
        GOTO    LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address HERE

After Instruction
CNT = CNT + 1
if CNT = 0, PC = address CONTINUE
if CNT ≠ 0, PC = address HERE + 1

IORLW — Inclusive OR Literal with W

Syntax: [*label*] IORLW k

Operands: $0 \le k \le 255$

Operation: (W) .OR. (k) → (W)

Status Affected: Z

Encoding:

11	1000	kkkk	kkkk

Description: The contents of the W register are OR'ed with the 8-bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
IORLW   0x35
```
Before Instruction
W = 0x9A

After Instruction
W = 0xBF

IORWF — Inclusive OR W with f

Syntax: [*label*] IORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .OR. (f) → (dest)

Status Affected: Z

Encoding:

00	0100	dfff	ffff

Description: Inclusive OR the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:
```
IORWF   RESULT, 0
```
Before Instruction
RESULT = 0x13
W = 0x91

After Instruction
RESULT = 0x13
W = 0x93

MOVLW **Move Literal to W**

Syntax: [*label*] MOVLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W)

Status Affected: None

Encoding:

11	00XX	kkkk	kkkk

Description: The 8-bit literal "k" is loaded into W register.

Words: 1

Cycles: 1

Example:
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: 0 ≤ f ≤ 127

Operation: (W) → (f)

Status Affected: None

Encoding:

00	0000	1fff	ffff

Description: Move data from W register to register "f".

Words: 1

Cycles: 1

Example:
```
MOVWF   OPTION
```
Before Instruction
OPTION = 0xFF
W = 0x4F

After Instruction
OPTION = 0x4F
W = 0x4F

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) → (dest)

Status Affected: Z

Encoding:

00	1000	dfff	ffff

Description: The contents of register f is moved to destination d. If d=0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example:
```
MOVF    FSR, 0
```
After Instruction
W = value in FSR register

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

00	0000	0XX0	0000

Description: No operation

Words: 1

Cycles: 1

Example:
```
NOP
```

OPTION **Load Option Register**

Syntax: [*label*] OPTION

Operands: None

Operation: W → OPTION;

Status Affected: None

Encoding:

00	0000	0110	0010

Description: The contents of the W register is loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.

Words: 1

Cycles: 1

Example:

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

RETFIE **Return from Interrupt**

Syntax: [*label*] RETFIE

Operands: None

Operation: TOS → PC,
1 → GIE;

Status Affected: None

Encoding:

00	0000	0000	1001

Description: Return from Interrupt. Stack is popped and Top of the Stack (TOS) is loaded in PC. Interrupts are enabled by setting the GIE bit. GIE is the global interrupt enable bit (INTCON<7>). This is a two-cycle instruction.

Words: 1

Cycles: 2

Example: `RETFIE`

After Interrupt
PC = TOS
GIE = 1

RETLW **Return Literal to W**

Syntax: [*label*] RETLW k

Operands: 0 ≤ k ≤ 255

Operation: k → W; TOS → PC;

Status Affected: None

Encoding:

11	01XX	kkkk	kkkk

Description: The W register is loaded with the 8-bit literal "k". The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

Words: 1

Cycles: 2

Example:

```
        CALL   TABLE ; W contains table offset
                     ; value
        •            ; W now has table value
        •
        •
TABLE   ADDWF  PC    ; W = offset
        RETLW  k1    ; Begin table
        RETLW  k2    ;
        •
        •
        •
        RETLW  kn    ; End of table
```

Before Instruction
W = 0x07

After Instruction
W = value of k7

RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: TOS → PC;

Status Affected: None

Encoding:

00	0000	0000	1000

Description: Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

Words: 1

Cycles: 2

Example: `RETURN`

After Interrupt
PC = TOS

RLF — Rotate Left f through Carry

Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

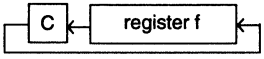
Operation: f<n> → d<n+1>, f<7> → C, C → d<0>;

Status Affected: C

Encoding:

00	1101	dfff	ffff

Description: The contents of register "f" are rotated 1-bit to the left through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is stored back in register "f".



Words: 1

Cycles: 1

Example:
```
RLF    REG1,0
```
Before Instruction
REG1 = 11100110
C = 0

After Instruction
REG1 = 11100110
W = 11001100
C = 1

RRF — Rotate Right f through Carry

Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

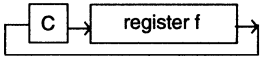
Operation: f<n> → d<n-1>,
f<0> → C,
C → d<7>;

Status Affected: C

Encoding:

00	1100	dfff	ffff

Description: The contents of register "f" are rotated 1-bit to the right through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".



Words: 1

Cycles: 1

Example:
```
RRF    REG1,0
```
Before Instruction
REG1 = 11100110
C = 0

After Instruction
REG1 = 11100110
W = 01110011
C = 1

SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0011

Description: The power down status bit ($\overline{PD}$) is cleared. Time-out status bit ($\overline{TO}$) is set. Watchdog Timer and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP mode for more details.

Words: 1

Cycles: 1

Example:
```
SLEEP
```

SUBLW — Subtract W from Literal

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Encoding:

11	110X	kkkk	kkkk

Description: The W register is subtracted (two's complement method) from the 8-bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example 1:
```
SUBLW    0X02
```
Before Instruction
W = 1
C = ?
After Instruction
W = 1
C = 1 ; result is positive

Example 2: Before Instruction
W = 3
C = ?

After Instruction
W = FF
C = 0 ; result is negative

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f)-(W) → (dest)

Status Affected: C, DC, Z

Encoding:

00	0010	dfff	ffff

Description: Subtract (two's complement method) the W register from register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example 1:
```
SUBWF  REG1,1
```
Before Instruction
REG1 = 0
W = 1
C = ?
After Instruction
REG1 = FF
W = 1
C = 0 ; result is negative

Example 2: Before Instruction
REG1 = FF
W = 0
C = ?
After Instruction
REG1 = FF
W = 0
C = 1 ; result is positive

TRIS **Load TRIS Register**

Syntax: [*label*] TRIS f

Operands: 5 ≤ f ≤ 7

Operation: W → TRIS register f;

Status Affected: None

Encoding:

00	0000	0110	0fff

Description: This instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.

Words: 1

Cycles: 1

Example:

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

SWAPF **Swap f**

Syntax: [*label*] SWAPF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: f<0:3> → d<4:7>,
f<4:7> → d<0:3>;

Status Affected: None

Encoding:

00	1110	dfff	ffff

Description: The upper and lower nibbles of register "f" are exchanged. If "d" is 0 the result is placed in W register. If "d" is 1 the result is placed in register "f".

Words: 1

Cycles: 1

Example:
```
SWAPF  REG, 0
```
Before Instruction
REG = 0xA5
After Instruction
REG = 0xA5
W = 0x5A

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

11	1010	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the 8-bit literal "k". The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
XORLW  0xAF
```
Before Instruction
W = 0xB5
After Instruction
W = 0x1A

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 128$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected Z

Encoding:

00	0110	dfff	ffff

Description: Exclusive OR the contents of the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

Words: 1

Cycles: 1

Example:

```
XORWF  REG, 1
```

Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

2

8.0 DEVELOPMENT SUPPORT

8.1 Development Tools

The PIC16C5X and PIC16CXX microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER™ Real-Time In-Circuit Emulator
- PRO MATE™ Universal Programmer
- PICSTART™ Low-Cost Prototype Programmer
- Assembler
- Software Simulator

8.2 PICMASTER™: High Performance Universal In-Circuit Emulator

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X, PIC16CXX and PIC17CXX families.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16C5X, PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on PC compatible machines ranging from 80286-AT™ class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.1 environment, allowing the operator access to a wide range of supporting software and accessories.

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.1 environment was chosen to best make these features available to you, the end user.

The PICMASTER Emulator Universal System consists primarily of four major components:

- Host-Interface Card
- Emulator Control Pod
- Target-Specific Emulator Probe
- PC Host Emulation Control Software

The Windows 3.1 System is a multitasking operating system which will allow the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window.

Dynamic Data Exchange (DDE), a feature of Windows 3.1, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

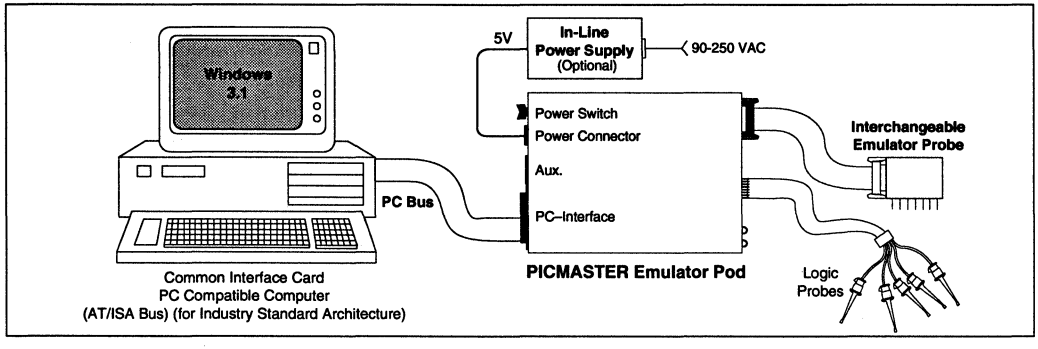
Under Windows 3.1, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16CXX processor and a PIC17CXX processor).

8.3 PRO MATE™: Universal Programmer

The PRO MATE Universal Programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MATE has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability . It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MATE can read, verify or program PIC16C5X, PIC16CXX and PIC17CXX devices. It can also set fuse configuration and code-protect in this mode. Its EEPROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.

FIGURE 8-1: PICMASTER SYSTEM CONFIGURATION



In PC-hosted mode, the PRO MATE connects to the PC via one of the COM (RS232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of V_{DD} min, V_{DD} max and V_{PP} levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different serial number, sequential or random.

The PRO MATE has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. PRO MATE supports all PIC16C5X, PIC16CXX and PIC17CXX processors.

8.4 PICSTART™ Programmer

The PICSTART™ programmer is an easy to use, very low-cost prototype programmer. It connects to the PC via one of the COM (RS232) ports. A PC based user interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based.

8.5 Assembler (MPASM)

Cross Assembler is a PC hosted symbolic assembler. It supports all microcontroller series including the PIC16C5X CMOS, PIC16CXX, and PIC17CXX families.

MPASM offers fully featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from the Microchip Universal Emulator System (PICMASTER).

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro Assembly Capability
- Provides Object, Listing, Symbol and special files required for debugging with one of the Microchip Emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a full feature directive language represented by four basic classes of directives:

- **Data Directives** are those that control the allocation of memory and provide a way to refer to data items symbolically, by meaningful names.
- **Listing Directives** control the MPASM listing dis play. They allow the specification of titles and subtitles, page ejects and other listing control.
- **Control Directives** permit sections of conditionally assembled code.
- **Macro Directives** control the execution and data allocation within macro body definitions.

8.6 Software Simulator (MPSIM)

The Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16C5X and PIC16CXX series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in single step, execute until break or in a trace mode. Two forms of symbolic debugging are available: an internal symbol table for disassembling opcodes and the displaying of source code from a listing file. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

9.7 Development Systems

For convenience, the development tools are packaged into comprehensive systems as listed in Table 9-1:

TABLE 8-1: DEVELOPMENT SYSTEM PACKAGES

Item	Name	System Description
1.	PICMASTER™ System	PICMASTER In-Circuit Emulator with your choice of Target Probe, PRO MATE Programmer, Assembler, Software Simulator and Samples.
2.	PICSTART™ System	PICSTART™ Low-Cost Prototype Programmer, Assembler, Software Simulator and Samples

9.8 Probe Specifications

The PICMASTER probes currently meet the following specifications:

PICMASTER PROBE	Devices Supported	PROBE Maximum Frequency	PROBE Operating Voltage
PROBE - 16C	PIC16C84	10 MHZ	4.5V - 5.5V

9.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Ambient temperature under bias ..... -55 to+ 125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss
(except VDD and MCLR) ..... -0.6V to VDD +0.6V
Voltage on VDD with respect to Vss ..... 0 to +7.5 V
Voltage on MCLR with respect to Vss
(Note 2) ..... 0 to +14 V
Total power Dissipation (Note 1) 800mW
Max. Current out of Vss pin 150mA
Max. Current into VDD pin 100mA
Input clamp current, IIK (VI<0 or VI> VDD) ..... ±20mA
Output clamp current, IOK (V0<0 or V0> VDD) ..... ±20mA
Max. Output Current sunk by any I/O pin 25mA
Max. Output Current sourced by any I/O pin 20mA
Max. Output Current sunk by I/O PORTA 80mA
Max. Output Current sunk by I/O PORTB 150mA
Max. Output Current sourced by I/O PORTA 50mA
Max. Output Current sourced by I/O PORTB 100mA

Notes:
1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
   $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{oh}\} + \sum \{(V_{DD}-V_{oh}) \times I_{oh}\} + \sum(V_{ol} \times I_{ol})$
2. Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low' level to the MCLR pin rather than pulling this pin directly to Vss.

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or compliance to AC and DC parametric specifications at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

9.1 DC CHARACTERISTICS: PIC16C84-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C84-10 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ + 125°C for automotive,
-40°C ≤ TA ≤ + 85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD = 4.0V to 6.0V

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Supply Voltage						
	VDD	4.0		6.0	V	XT, RC and LP osc configuration
		4.5		5.5	V	HS osc configuration
RAM Data Retention Voltage (Note 2)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See Section 5.2 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See Section 5.2 for details on power on reset
Supply Current (Note 3)						
	IDD		1.8	4.5	mA	FOSC = 4 MHz, VDD = 5.5V (Note 5)
			35	70	µA	FOSC = 32 KHz, VDD = 4.0V, WDT disabled, LP osc configuration
			5	10	mA	FOSC = 10 MHz, VDD = 5.5V, HS osc configuration (PIC16C84-10 only)
Power Down Current (Note 4)						
	IPD		7	28	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
			1.0	14	µA	VDD = 4.0V, WDT disabled, 0°C to +70°C
			1.0	16	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
			1.0	TBD	µA	VDD = 4.0V, WDT disabled, -40°C to +125°C

* These parameters are characterized but not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: For RC osc configuration, current through Rext (external pull-up resistor) is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

9.2 DC CHARACTERISTICS: PIC16LC84-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ + 125°C for automotive,
-40°C ≤ TA ≤ + 85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD = 2.0V to 6.0V

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Supply Voltage	VDD	2.0 4.5		6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
RAM Data Retention Voltage (Note 2)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 5.2 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 5.2 for details on power on reset
Supply Current (Note 3)	IDD		1.8 15	4.5 32	mA µA	FOSC = 4 MHz, VDD = 5.5V (Note 5) FOSC = 32 KHz, VDD = 2.0V, WDT disabled, LP osc configuration
Power Down Current (Note 4)	IPD		3 0.4 0.4 0.4	16 7 9 TBD	µA µA µA µA	VDD = 2.0V, WDT enabled, -40°C to +85°C VDD = 2.0V, WDT disabled, 0°C to +70°C VDD = 2.0V, WDT disabled, -40°C to +85°C VDD = 2.0V, WDT disabled, -40°C to +125°C

* These parameters are characterized but not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: For RC osc configuration, current through Rext (external pull-up resistor) is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

Notes to Table 9.3

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C84 be driven with external clock in RC mode.

Note 3 : The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5: The user may use better of the two specifications.

9.3 DC CHARACTERISTICS: PIC16C84-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C84-10 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16LC84-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40 ≤ TA ≤ +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Tables 9.1 and 9.2

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Input Low Voltage						
I/O ports	VIL	VSS		0.2 VDD	V	
MCLR, T0CKI		VSS		0.2 VDD	V	
OSC1 (in RC configuration)		VSS		0.1 VDD		Note 2
OSC1 (in XT, HS and LP configuration)		VSS		0.3 VDD	V	
Input High Voltage						
I/O ports	VIH	2.0		VDD	V	VDD ≤ 5.5V (note 5)
		0.7 VDD				For entire VDD range (note 5)
MCLR, T0CKI, OSC1 (in RC configuration)		0.85 VDD		VDD	V	Note 2
OSC1 (XT, HS and LP configuration)		0.7 VDD		VDD	V	
Input Leakage Current (Notes 3, 4)						
I/O ports RA, RB	IIL			±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR, T0CKI				±5	µA	VSS ≤ VPIN ≤ VDD
OSC1				±5	µA	VSS ≤ VPIN ≤ VDD , XT, HS and LP osc configuration
PortB Weak Pull-up Current	IPU	50	100	150	µA	VPIN = VSS, VDD = 5.0V
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.5mA, VDD = 4.5V, -40°C to +85°C
				0.6	V	IOL = 6.0mA, VDD = 4.5V, -40°C to +125°C
OSC2/CLKOUT				0.6	V	IOL = 1.6mA, VDD = 4.5V, -40°C to +85°C
(RC osc configuration)				0.6	V	IOL = 1.2mA, VDD = 4.5V, -40°C to +125°C
Output High Voltage						
I/O Ports (Note 4)	VOH	VDD-0.7			V	IOH = -3.0mA, VDD = 4.5V, -40°C to +85°C
		VDD-0.7			V	IOH = -2.5mA, VDD = 4.5V, -40°C to +125°C
OSC2/CLKOUT		VDD-0.7			V	IOH = -1.3mA, VDD = 4.5V, -40°C to +85°C
(RC osc configuration)		VDD-0.7			V	IOH = -1.0mA, VDD = 4.5V, -40°C to +125°C
Data EEPROM						
Endurance	Ed	100,000	1,000,000		E/W cycles	
VDD for read/write	Vdrw		Full VDD range			
Erase/write cycle time	tdew			10	ms	
Program EEPROM Memory						See section 11 for more details on programming
Endurance	Ep	100	1000		E/W cycles	
Erase/write cycle time	tpew			10	ms	
VDD for read	Vpr		Full VDD range			
VDD for erase/write	Vpw	4.5		5.5	V	

Notes on previous page.

9.4 AC CHARACTERISTICS: PIC16C84-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C84-10 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16LC84-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

AC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40 ≤ TA ≤ +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Tables 9.1 and 9.2

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
External CLOCKIN Frequency (Note 2)	FOSC	DC		2	MHz	XT, RC osc mode. 2V ≥ VDD ≥ 6V
		DC		4	MHz	XT, RC osc mode. 3V ≥ VDD ≥ 6V
		DC		10	MHz	HS osc mode (PIC16C84-10)
		DC		200	KHz	LP osc mode
Oscillator Frequency (Note 2)	FOSC	DC		2	MHz	RC OSC mode. 2V ≥ VDD ≥ 6V
		DC		4	MHz	RC osc mode. 2V ≥ VDD ≥6V
		0.1		2	MHz	XT osc mode. 3V ≥ VDD ≥ 6V
		0.1		4	MHz	XT osc mode. 3V ≥ VDD ≥6V
		1		10	MHz	HS osc mode (PIC16C84-10)
		DC		200	KHz	LP osc mode
Instruction Cycle Time (Note 2)	TCY	0.4	4/Fosc	DC	µs	
External Clock in Timing (Note 4)						
Clock in (OSC1) High or Low Time						
XT oscillator type	TCKHLXT	60			ns	
LP oscillator type	TCKHLLP	2			µs	
HS oscillator type	TCKHLHS	50			ns	
Clock in (OSC1) Rise or Fall Time						
XT oscillator type	TCKRFXT	25			ns	
LP oscillator type	TCKRFLP	50			ns	
HS oscillator type	TCKRFHS	25			ns	
OSC1 high to CLKOUT low	TOSH2CKL				ns	Note 6
OSC1 high to CLKOUT high	TOSH2CKH				ns	Note 6
CLKOUT output rise time	TCKR				ns	Note 6
CLKOUT output fall time	TCKF				ns	Note 6
RESET Timing						
MCLR Pulse Width (low)	TMCL	150			ns	
TMR0 Input Timing, No Prescaler						
TMR0 High Pulse Width	TRTH	0.5 TCY+ 20*			ns	Note 3
TMR0 Low Pulse Width	TRTL	0.5 TCY+ 20*			ns	Note 3
TOCKI Input Timing, With Prescaler						
TOCKI High Pulse Width	TRTH	50			ns	Note 3
TOCKI Low Pulse Width	TRTL	50			ns	Note 3
TOCKI Period	TRTP				ns	Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Timeout Period (No Prescaler)	TWDT	$\frac{TCY + 40}{7^* \quad N}$*	18*	33*	ms	VDD = 5V, -40°C to +125°C
OST/PWRT Timings						
Oscillation Start-up Timer Period	TOST		1024 tosc		ms	tosc = OSC1 period
Power-up timer period	TPWRT	28*	72*	132*	ms	VDD = 5V, -40°C to +125°C

* These parameters are characterized, but not tested.

(Cont. on next page)

9.4 AC CHARACTERISTICS: PIC16C84-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C84-10 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16LC84-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

AC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40 ≤ TA ≤ +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec Tables 9.1 and 9.2

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
I/O Timing						
I/O Pin Input Valid Before CLKOUT↑	TioV2ckH	0.30 TCY+ 30			ns	Note 6
I/O Pin Input Hold After CLKOUT↑	TckH2ioI	0			ns	Note 6
I/O Pin Output Valid After CLKOUT↓	TioV2ckL			120	ns	Note 6
I/O Pin Input Valid Before OSC↑ (I/O Setup Time)	TioV2osH	TBD			ns	
OSC1↑ to I/O pin input invalid (I/O hold time)	TosH2ioL	TBD			ns	
OSC1↑ to I/O pin output valid	TosH2ioV			TBD	ns	
I/O pin output rise time	TioR			TBD	ns	
I/O pin output fall time	TioF			TBD	ns	
Interrupt Timing						
INT pin high or low time	TinP	20			ns	
RB <7:4> input change time for interrupt to be recognized	TrbP	20			ns	
Capacitive Loading Specs on Output Pins						
OSC2 pin	COSC2			15	pF	In XT, HS or LP modes when external clock is used to drive OSC1
All I/O pins and OSC2 (in RC mode)	CIO			50	pF	

* These parameters are characterized, but not tested.

NOTES TO TABLE 9.4

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: Instruction cycle period (Tcy) equals four times the input oscillator time base period.
All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Note 3: For a detailed explanation of TMR0 input clock requirements see Section 6.4.1.

Note 4: Clock-in high-time is the duration for which clock input is at VIHOSC or higher. Clock-in low-time is the duration for which clock input is at VIHOSC or lower.

Note 5: All AC parameters are tested or characterized with these capacitive loads.

Note 6: CLKOUT is available only in RC oscillator mode.

9.5 Electrical Structure of Pins

FIGURE 9.5.1 - ELECTRICAL STRUCTURE OF I/O PINS (RA, RB)

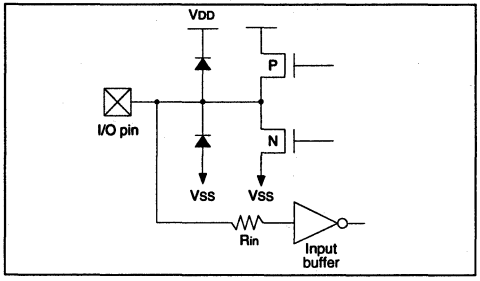
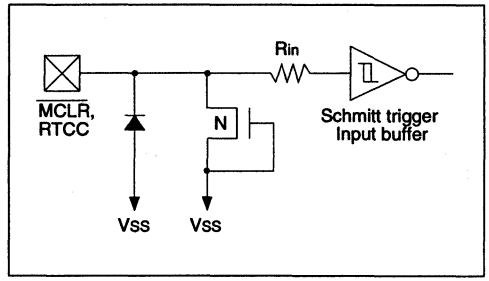


FIGURE 9.5.2 - ELECTRICAL STRUCTURE OF MCLR AND T0CKI PINS



Notes to Figures 9.5.1 and 9.5.2: The diodes and the grounded gate (or output driver) NMOS device are carefully designed to protect against ESD (Electrostatic discharge) and EOS (Electrical overstress). Rin is a small resistance to further protect the input buffer from ESD.

10.0 TIMING DIAGRAMS

FIGURE 10.0.1 - TOCKI TIMING

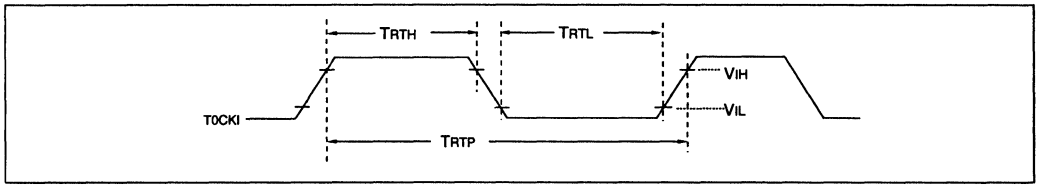
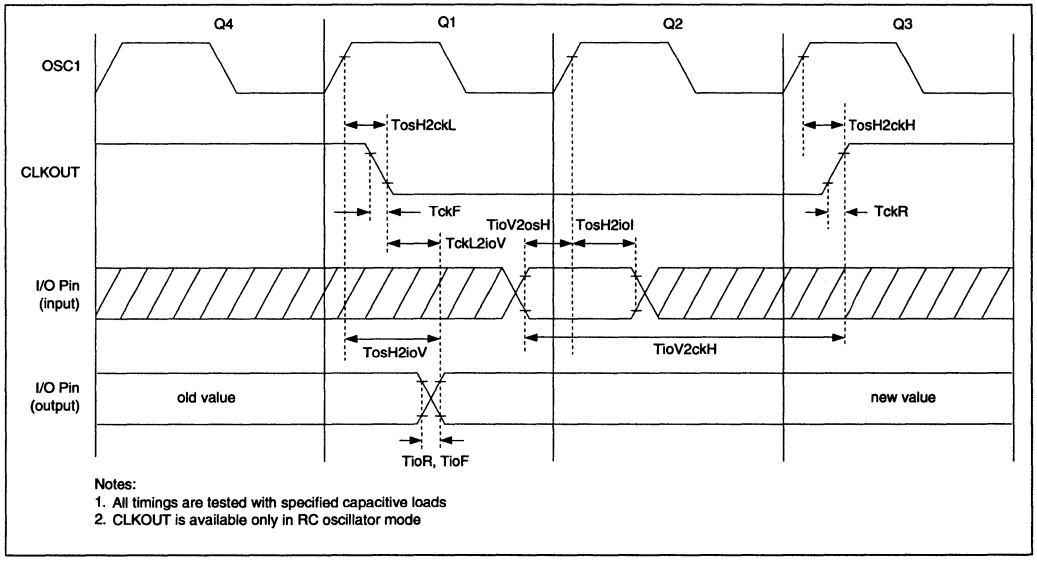


FIGURE 10.0.2 - INPUT/OUTPUT TIMING FOR I/O PORTS



Notes:
1. All timings are tested with specified capacitive loads
2. CLKOUT is available only in RC oscillator mode

11.0 DC & AC CHARACTERISTICS GRAPHS/TABLES

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. **In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.**

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

FIGURE 11.0.1 - TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

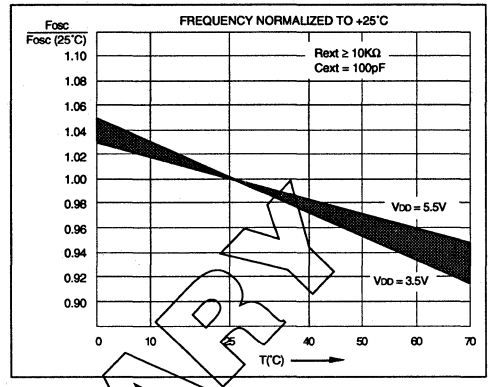
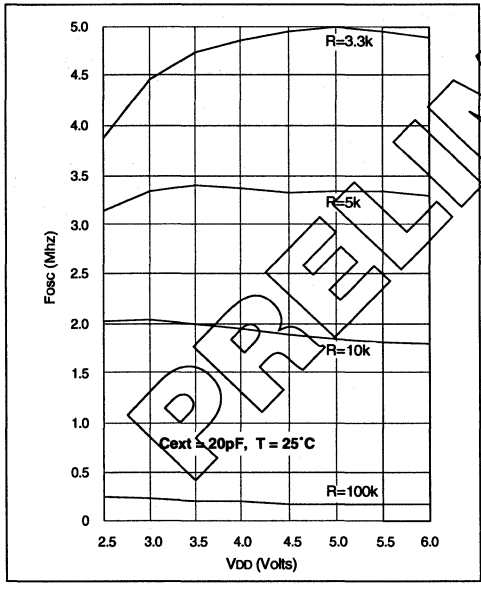
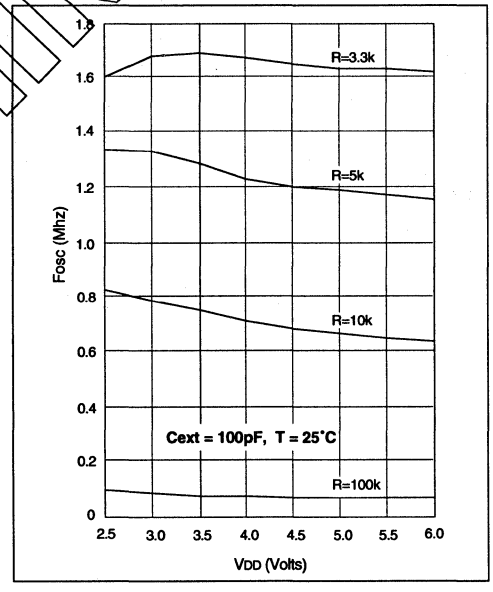


FIGURE 11.0.2 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD*



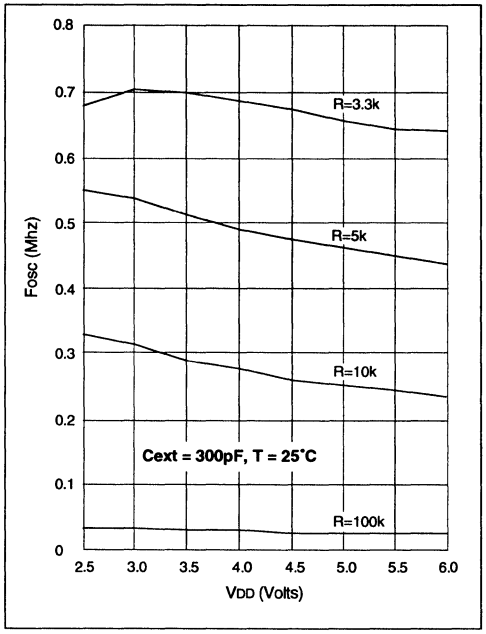
*Measured in PDIP Packages.

FIGURE 11.0.3 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD*



*Measured in PDIP Packages.

FIGURE 11.0.4 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD*



*Measured in PDIP Packages.

TABLE 11.0.1 - RC OSCILLATOR FREQUENCIES*

Cext	Rext	Average Fosc @ 5V, 25°C	
20pf	3.3k	4.71 MHz	± 28%
	5k	3.31 MHz	± 25%
	10k	1.91 MHz	± 24%
	100k	207.76 KHz	± 39%
100pf	3.3k	1.65 MHz	± 18%
	5k	1.23 MHz	± 21%
	10k	711.54 KHz	± 18%
	100k	75.62 KHz	± 28%
300pf	3.3k	672.78 KHz	± 14%
	5k	489.49 KHz	± 13%
	10k	275.73 KHz	± 13%
	100k	28.12 KHz	± 23%

*Measured in PDIP Packages.

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value.

FIGURE 11.0.5 - TYPICAL Ipd vs VDD WATCHDOG DISABLED 25°C

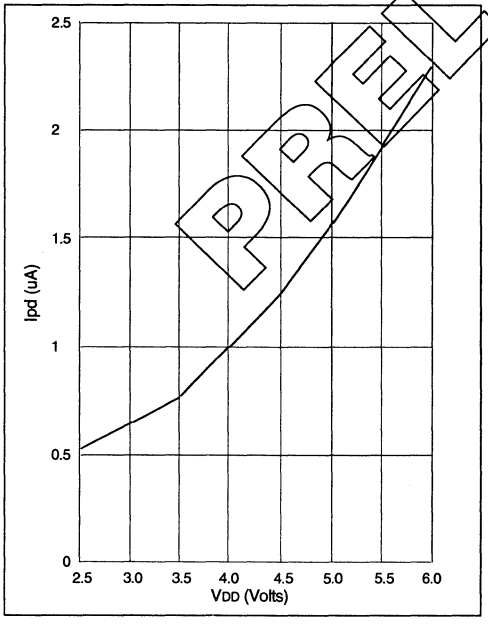


FIGURE 11.0.6 - TYPICAL Ipd vs VDD WATCHDOG ENABLED 25°C

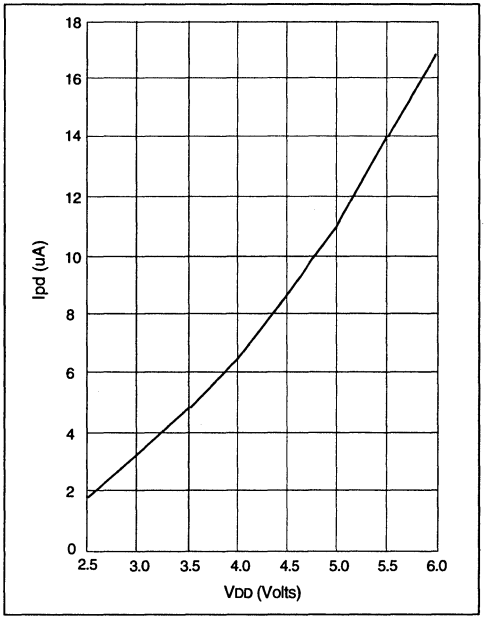


FIGURE 112.0.7 - MAXIMUM Ipd vs VDD WATCHDOG DISABLED

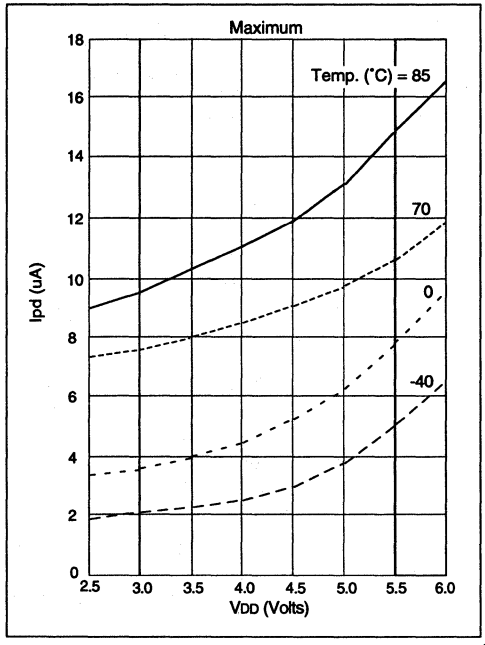
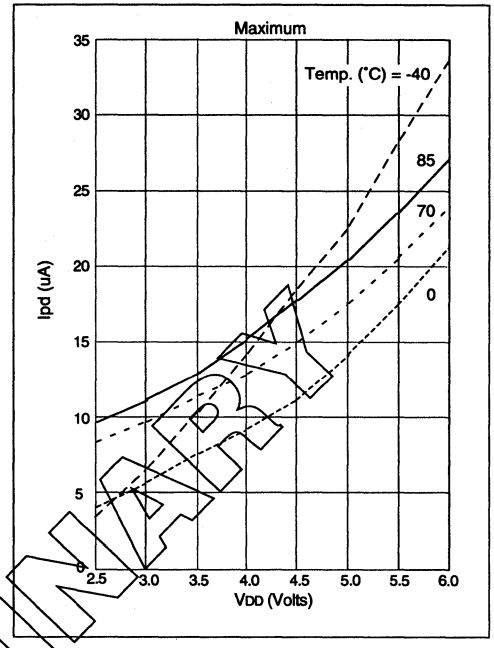


FIGURE 11.0.8 - MAXIMUM Ipd vs VDD WATCHDOG ENABLED*



* IPD, with watchdog timer enabled, has two components: The leakage current which increases with higher temperature and the operating current of the watchdog timer logic which increases with lower temperature. At -40°C, the latter dominates explaining the apparently anomalous behavior.

FIGURE 11.0.9 - VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs VDD

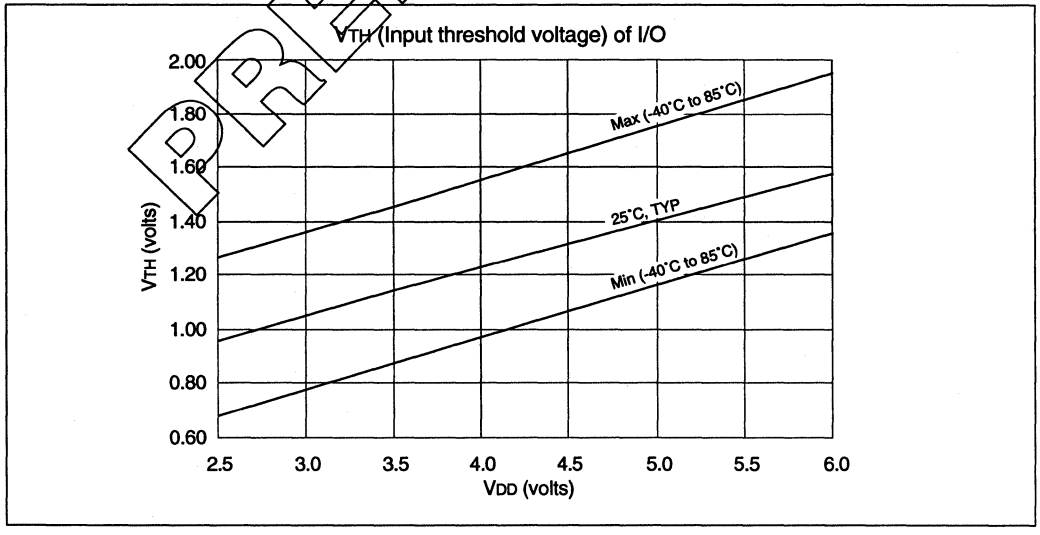
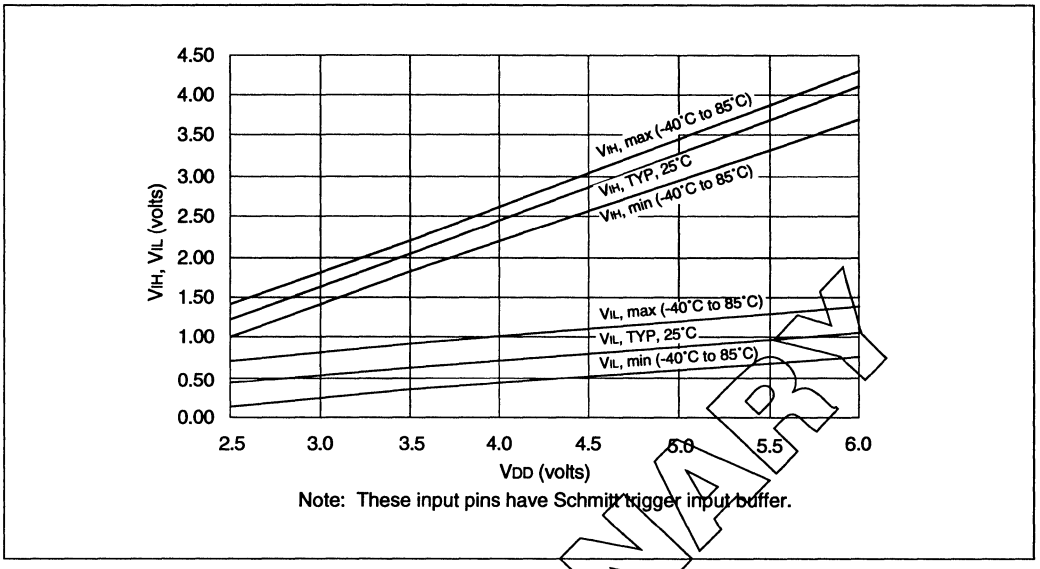


FIGURE 11.0.10 - VIH, VIL OF $\overline{MCLR}$, T0CKI AND OSC1 (IN RC MODE) vs VDD



Note: These input pins have Schmitt trigger input buffer.

FIGURE 11.0.11 - VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs VDD

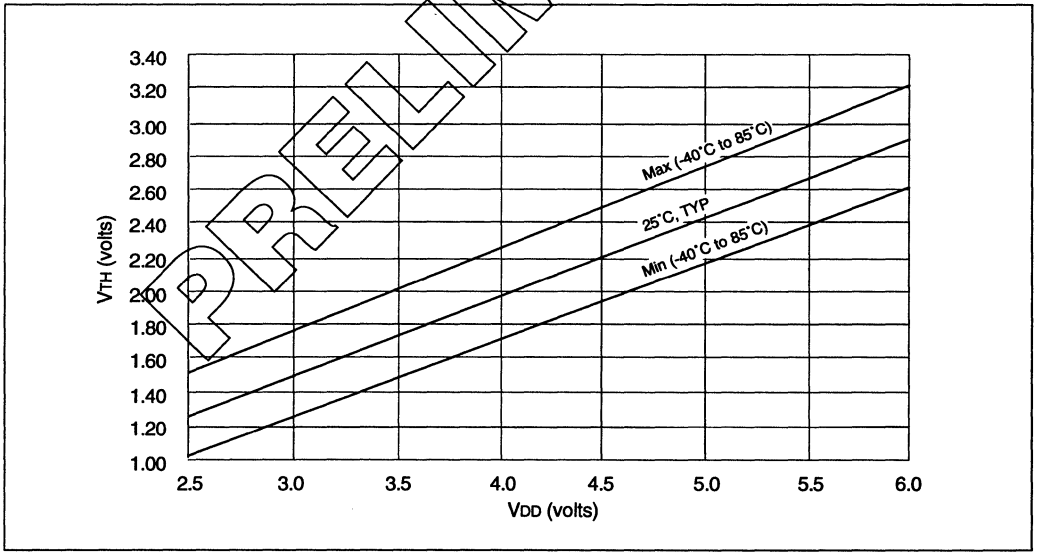


FIGURE 11.0.12 - TYPICAL IDD vs FREQ (EXT CLOCK, 25°C)

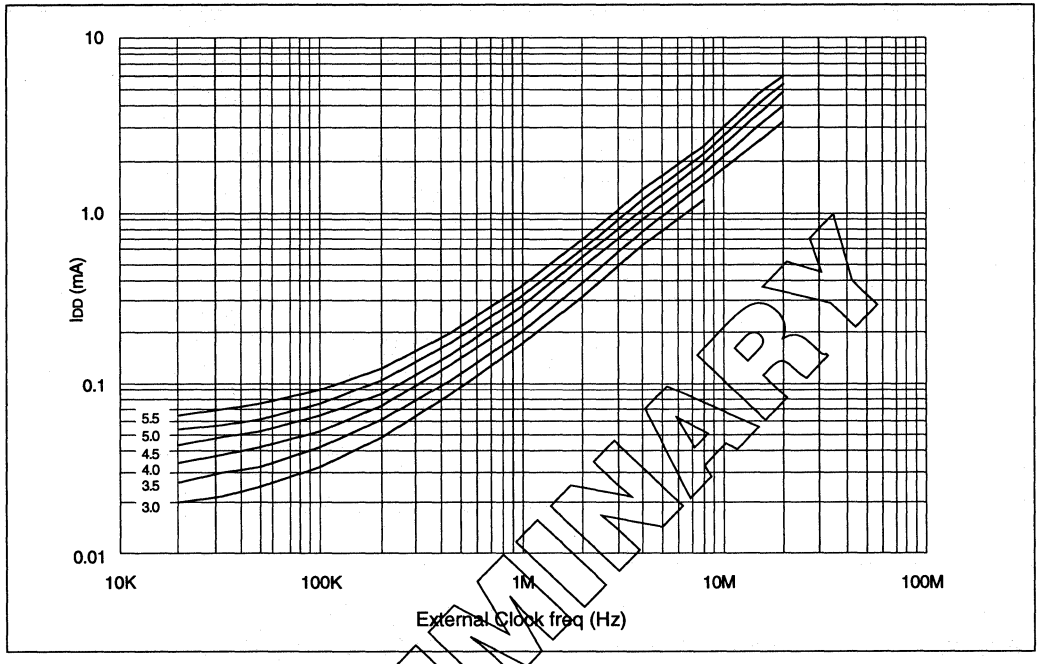


FIGURE 11.0.13 - MAXIMUM IDD vs FREQ (EXT CLOCK, -40° to +85°C)

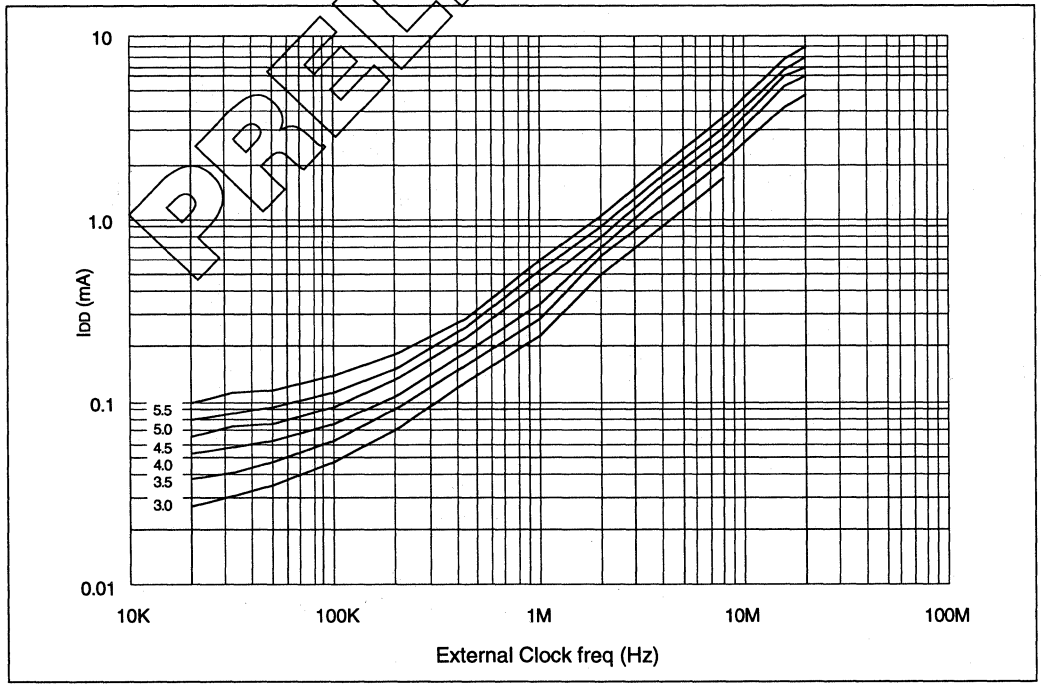


FIGURE 11.0.14 - WDT Timer Time-out Period vs VDD

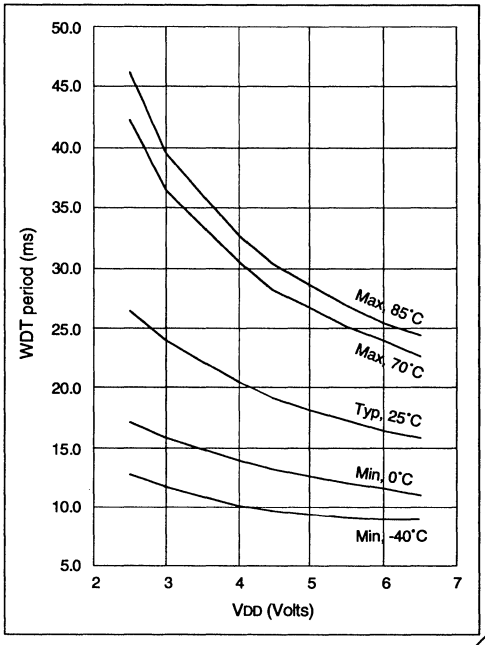


FIGURE 11.0.15 - Transconductance (gm) of HS Oscillator vs VDD

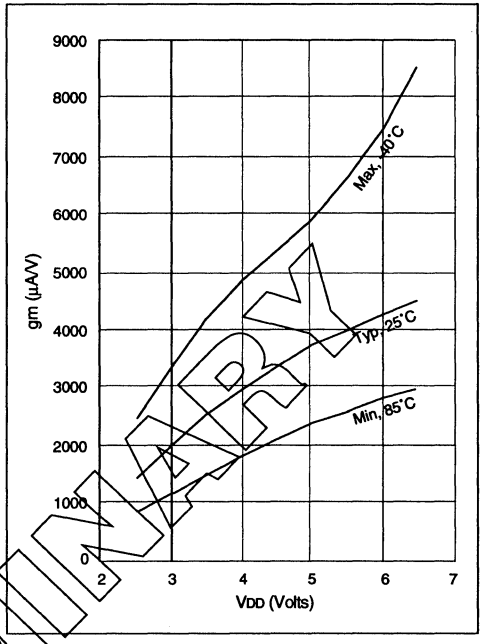


FIGURE 11.0.16 - Transconductance (gm) of LP Oscillator vs VDD

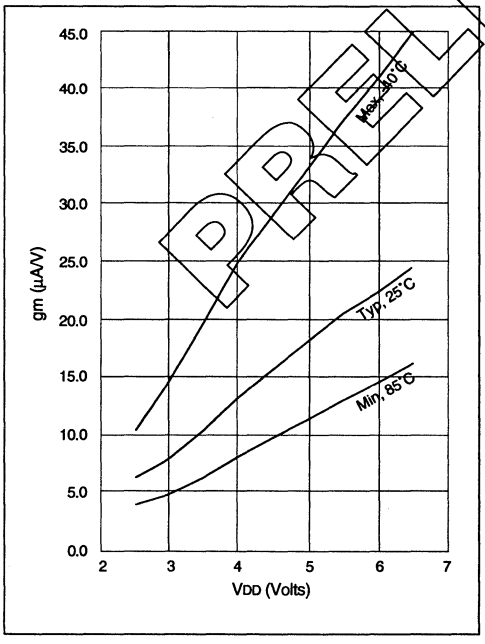


FIGURE 11.0.17 - Transconductance (gm) of XT Oscillator vs VDD

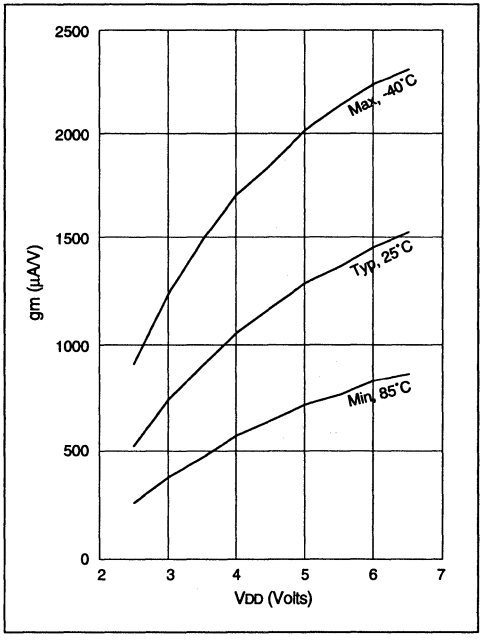


FIGURE 11.0.18 - IOH vs VOH, VDD = 3V

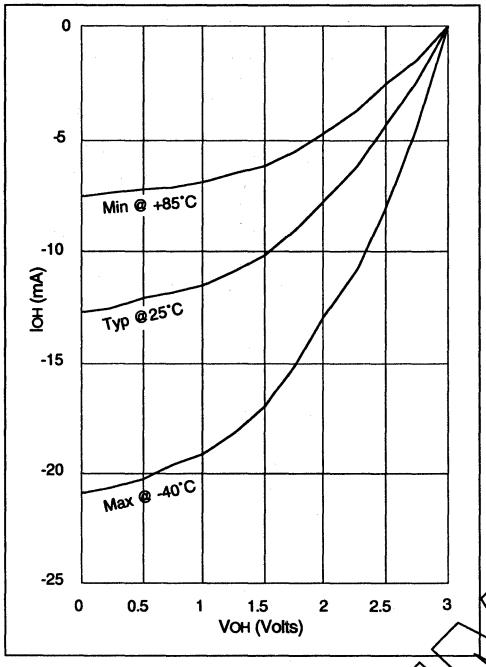


FIGURE 11.0.19 - IOH vs VOH, VDD = 5V

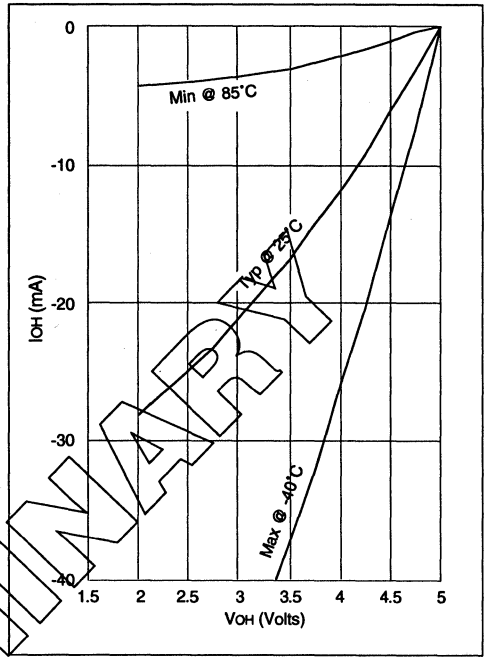


FIGURE 11.0.20 - IOL vs VOL, VDD = 3V

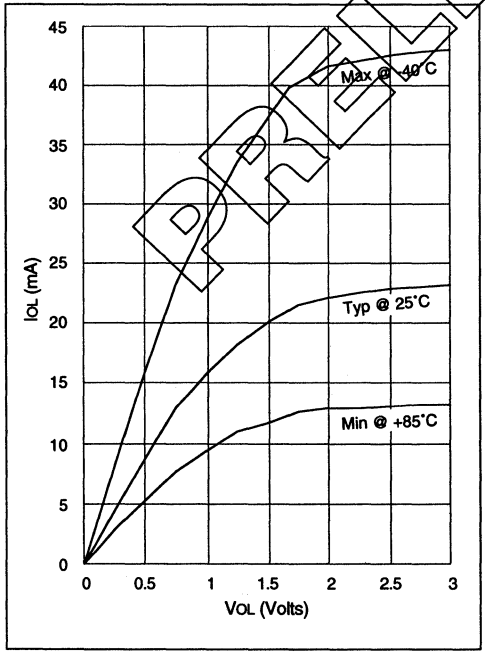


FIGURE 11.0.21 - IOL vs VOL, VDD = 5V

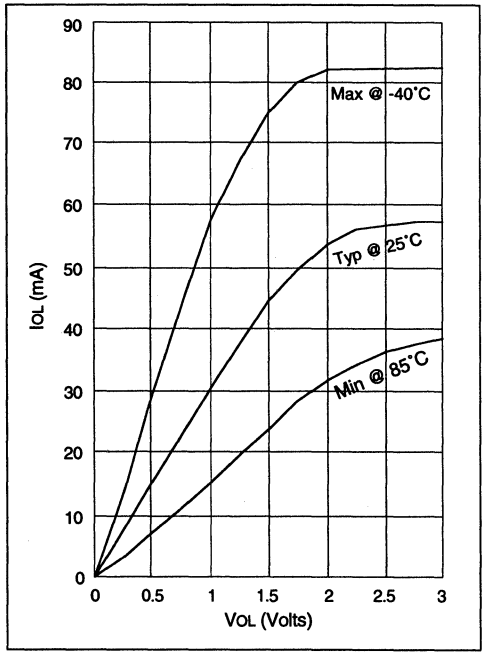


TABLE 11.0.2 - INPUT CAPACITANCE *

Pin Name	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
RTCC	3.2	2.8

* All capacitance values are typical at 25°C. A part to part variation of ±25% (three standard deviations) should be taken into account.

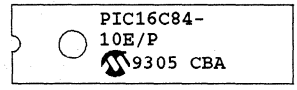
12.0 PACKAGING DIAGRAMS AND DIMENSIONS

See Section 11 of the Data Book.

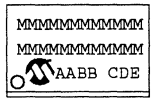
12.1 Package Marking Information

18L PDIP

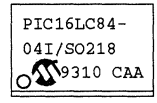
Example



18L SOIC



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

APPENDIX A

The following are the list of modifications over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14-bit. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and register file (128 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from status register.
3. Data memory paging is redefined slightly. Status register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.

   Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressible.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to eight deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change feature.
13. RTCC pin is also a port pin (RA4) now.
14. Location 07h (PortC) is unimplemented and not a general purpose register.
15. FSR is made a full 8-bit register.
16. "In system programming" is made possible. The user can program the PIC16C84 using only five pins: VDD, VSS, MCLR/VPP, RB6 (clock) and RB7 (data in/out).

APPENDIX B

To convert code written for PIC16C5X to PIC16C84, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.
6. Note that location 07h is an unimplemented data memory location.

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CONNECTING TO MICROCHIP BBS

Connect world wide to the Microchip BBS using the Compuserve communications network. In most cases a local call is your only expense. The Microchip BBS connection does not use Compuserve membership services, therefore **you do not need Compuserve membership to join Microchip's BBS.**

The procedure to connect will vary slightly from country to country. Please check with your local Compuserve agent for details if you have a problem. Compuserve services allows multiple users at baud rates up to 9600.

To connect:

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal Compuserve setting which is 7E1.

2. Dial your local Compuserve phone number.

3. Depress **<ENTER>** and a garbage string will appear because Compuserve is expecting a 7E1 setting.

4. Type **+ <ENTER>** and `Host Name:` will appear.

5. Type **MCHIPBBS<ENTER>** and you will be connected to the Microchip BBS.

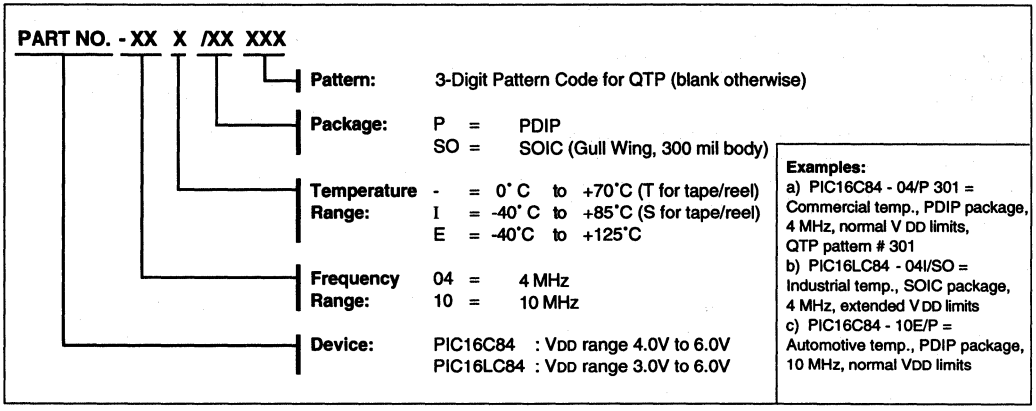
In the United States, to find Compuserve's phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600 baud connection. After the system responds with `Host Name:`, type

NETWORK<ENTER> and follow Compuserve's directions.

For voice information (or calling from overseas), you may call (614) 457-1550 for your local Compuserve number.

PIC16C84 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local Compuserve number.

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

PIC17C42

High-Performance 8-Bit CMOS EPROM Microcontroller

FEATURES

Powerful CPU

- Fully static design
- 8-bit wide data path
- 16-bit wide instructions
- All instructions are single word
- Most instructions are single cycle, a few are two cycle
- 160ns cycle time (at 25 MHz).
- 64K x 16 of addressable program memory space
- Direct, indirect (with auto increment and decrement), immediate and relative addressing
- Four modes of operation
  - Microcontroller mode
  - Secure microcontroller mode
  - Extended microcontroller mode (both internal and external program memory access)
  - Microprocessor mode (external only program memory access)

High-level of Integration

- 2K x 16 on chip EPROM program memory
- 232 x 8 general purpose registers (SRAM)
- 48 special function registers
- 16 x 16 hardware stack
- 11 external/internal interrupts
- Up to 33 I/O pins
- Three 16-bit timer/counters
- Two 16-bit capture registers
- Two high-speed PWM outputs (10-bit, 15.6 KHz)
- Full-featured serial port (USART) with baud rate generator

Special microcontroller features

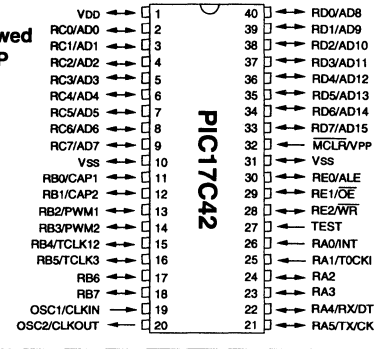
- Watchdog Timer with its own on-chip RC oscillator for reliable operation
- Power saving SLEEP mode
- On-chip Power-up Timer and Power-On Reset saves external circuitry
- On-chip Oscillator Start-up Timer
- Fuse selectable oscillator options: standard crystal oscillator, low frequency crystal oscillator, RC oscillator or external clocking
- Code protection feature to protect on-chip EPROM program memory

Package Options

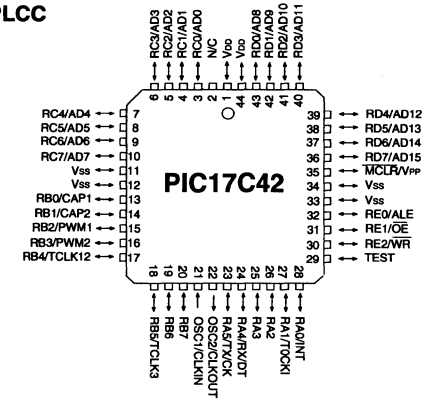
- 40L PDIP, 44L PLCC and 44L PQFP

PACKAGE TYPES

PDIP, Windowed CERDIP



PLCC



PQFP

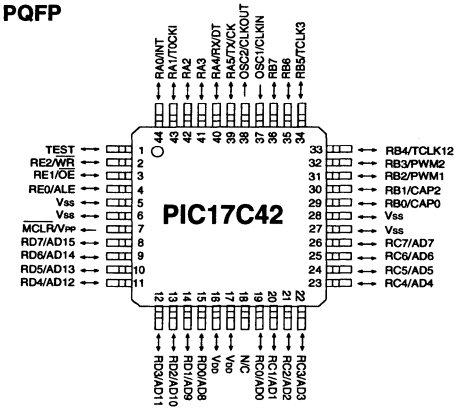
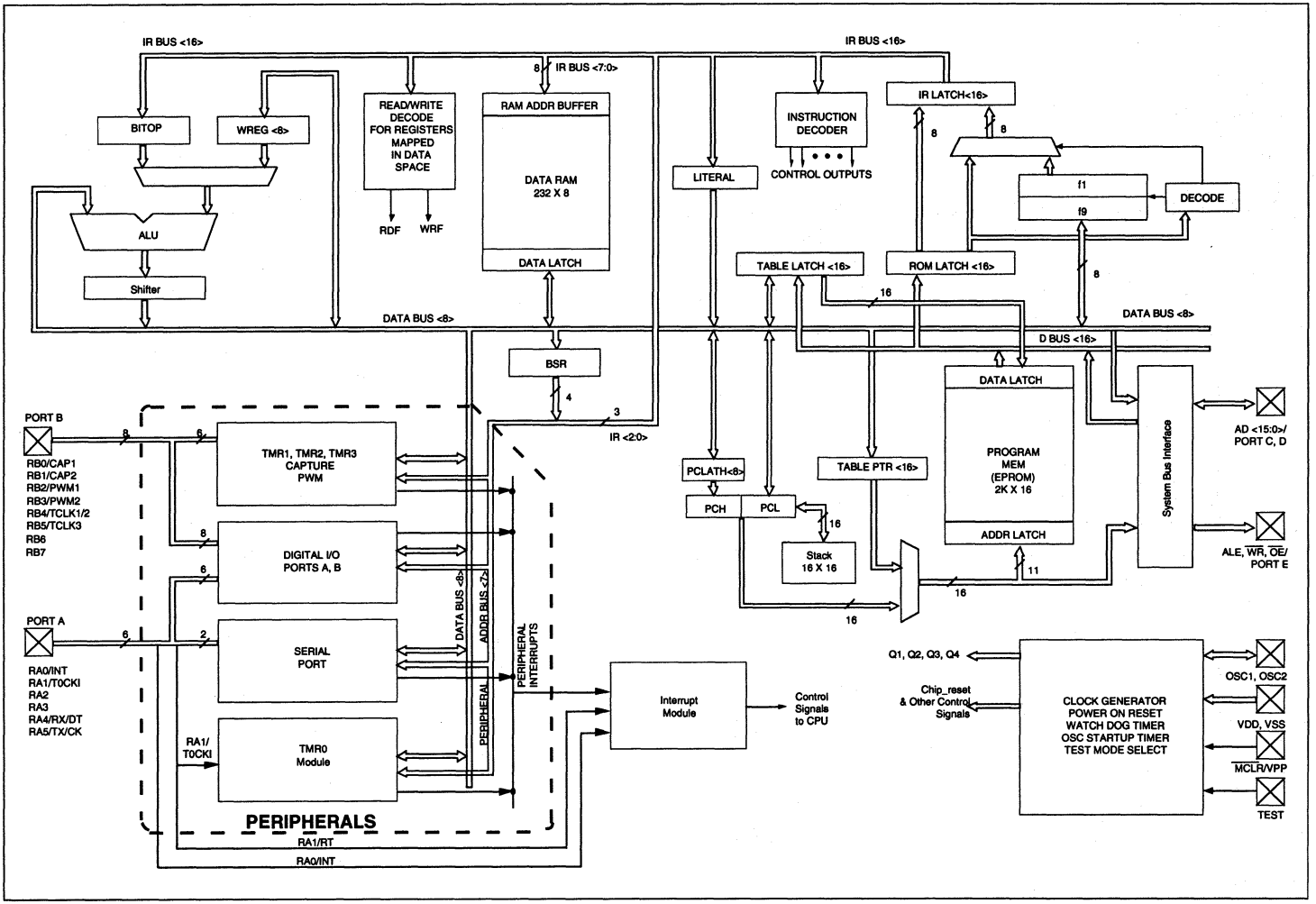


FIGURE B - PIC17C42 BLOCK DIAGRAM



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PIC17C42 OVERVIEW

PIC17C42 is the first member of a high-performance EPROM based 8-bit CMOS microcontroller family. The PIC17C42 integrates a powerful CPU (160ns instruction cycle) with an array of peripheral resources making it ideal for complex real-time control applications.

Microchip's EPROM technology allows the user to test and develop code on windowed cerdip package version and move into production with the cost effective One Time Programmable (OTP) plastic DIP package version.

The PIC17C42 is fully supported by a host of software and hardware development tools. These include an assembler/linker; a low-cost in-circuit emulator; a high performance, in-circuit emulator; a programmer; and a programmer/development board. A C compiler is planned. All tools are supported by PC AT® and compatible platforms.

1.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC17C42 can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC17C42 uses a modified Harvard architecture, in which, program and data are accessed from separate memories. This improves bandwidth over traditional Von-Neuman architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. In PIC17C42, op-codes are 16-bit wide making it possible to have all single word instructions. Full 16-bit wide program memory access bus fetches a 16-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (55 in all) execute in a single cycle (160ns @ 25MHz) except for program branches and two special instructions that transfer data between program and data memory.

The PIC17C42 can address 64K x 16 program memory space. It integrates 2K x 16 EPROM program memory on-chip. Program execution can be internal only (microcontroller mode), external only (microprocessor mode) or both (extended microcontroller mode).

The PIC17C42 can directly or indirectly address 256 data memory locations (file registers). All special function registers including the program counter are mapped in the data memory. The PIC17C42 has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC17C42 simple yet efficient. In addition, the learning curve is reduced significantly.

1.1 PIC17C42 Pinout Description

Pin Name	Pin Type	Number of Pins	Pin Function
$\overline{MCLR}$/VPP	I/P	1	Master clear (reset) input. This is the active low reset input to the chip. During Programming mode, it is the programming voltage (VPP) input.
OSC1/CLKIN	I	1	Oscillator input in crystal/resonator or RC oscillator mode. External clock input in external clock mode.
OSC2/CLKOUT	O	1	Oscillator output. Connects to crystal or resonator in crystal oscillator mode. In RC oscillator or external clock modes OSC2 pin outputs CLKOUT which has one fourth the frequency of OSC1 and denotes the instruction cycle rate.
RA0/INT	I	1	Input only port pin (bit 0 of Port A) and also external interrupt input. Interrupt can be configured to be on positive or negative edge.
RA1/T0CKI	I	1	Input only port pin (bit 1 of Port A) and also an external interrupt input. Interrupt can be configured to be on rising or falling edge. It is also the external clock input for the TMR0 timer/counter.
RA2,RA3	I/O	2	High voltage, high current open drain input/output port pins.
RA4/RX/DT	I/O	1	Input only port pin (bit 4 of Port A). If the serial port is enabled, in full duplex asynchronous serial communication mode this is the receive pin. In half duplex synchronous serial communication mode it is data input (during receive) or data output (during transmit).
RA5/TX/CK	I/O	1	Input only port pin (bit 5 of Port A). If the serial port is enabled, in full duplex asynchronous serial communication mode it is the transmit pin. In half duplex synchronous communication mode, it is shift clock input (slave mode) or clock output (master mode).

(cont.)

Pin Name	Pin Type	Number of Pins	Pin Function
RB0/CAP1	I/O	1	Port pin configurable as input or output in software, with Schmitt trigger input (bit 2 of Port B). It is also the PWM1 input pin.
RB1/CAP2	I/O	1	Port pin configurable as input or output in software, with Schmitt trigger input (bit 3 of Port B). It is also the PWM2 input pin.
RB2/PWM1	I/O	1	Port pin configurable as input or output in software, with Schmitt trigger input (bit 2 of Port B). It is also the PWM1 output pin.
RB3/PWM2	I/O	1	Port pin configurable as input or output in software, with Schmitt trigger input (bit 3 of Port B). It is also the PWM2 output pin.
RB4/TCLK12	I/O	1	Port pin configurable as input or output in software, with Schmitt trigger input (bit 4 of Port B). It is also the external clock input to timer1 and timer2.
RB5/TCLK3	I/O	1	Port pin configurable as input or output in software, with Schmitt trigger input (bit 5, of Port B). It is also the external clock input to timer3.
RB6,RB7	I/O	2	Port pins configurable as input or output in software, with Schmitt trigger input (bits 6 and 7 of Port B).
RC7/AD7- RC0/AD0	I/O	8	Eight bit wide Port C with each pin software configurable as input or output. Input is TTL compatible (and not CMOS Schmitt trigger type). This is also the lower half of the 16 bit wide system bus in microprocessor mode or extended microcontroller mode. In multiplexed system bus configuration, these pins are address output as well as data input or output.
RD7/AD15- RD0/AD8	I/O	8	Eight bit wide Port D with each pin software configurable as input or output. Input is TTL compatible (and not CMOS Schmitt trigger type). This is also the upper byte of the 16 bit system bus in microprocessor mode or extended microprocessor mode or extended microcontroller mode. In multiplexed system bus configuration these pins are address output as well as data input or output.
RE0/ALE	I/O	1	Port pin configurable as input or output in software, with TTL compatible input (bit 0 of Port E). In microprocessor mode or extended microcomputer mode, it is the Address Latch Enable (ALE) output. Address should be latched on the falling edge of ALE output.
RE1/$\overline{OE}$	I/O	1	Port pin configurable as input or output in software, with TTL compatible input (bit 1 of Port E). In microprocessor or extended microcontroller mode, it is the Output Enable ($\overline{OE}$) control output (active low).
RE2/$\overline{WR}$	I/O	1	Port pin configurable as input or output in software, with TTL compatible input (bit 2 of Port E). In microprocessor or extended microcontroller mode, it is the Write Enable ($\overline{WR}$) control output (active low).
TEST	I	1	Test mode selection control input. Always tie to Vss for normal operation.
VDD	P	1	Power
Vss	P	2	Ground. Both pins must be connected to system ground.

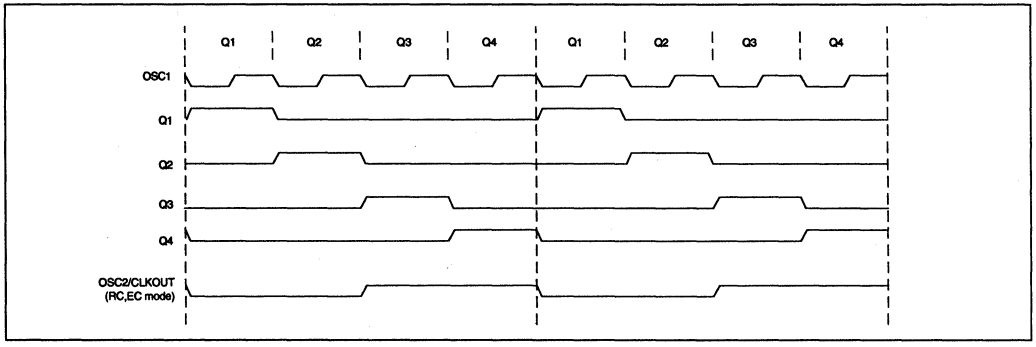
Legend: I = Input only; O = Output only; I/O = Input/output; P = Power.

1.2 Internal Clocking Scheme

Internally, the clock input to OSC1 pin is divided by four to generate four phases (Q1, Q2, Q3 and Q4) each with a frequency equal to fosc /4 and duty cycle of 25%. If EC (external clock) or RC oscillator mode is selected, the OSC2 pin provides a clock output, CLKOUT, which is high during Q3, Q4 and low during Q1, Q2.

As long as internal chip reset is active, the clock generator holds the chip in Q1 state. The CLKOUT pin is driven low (EC, RC mode).

FIGURE 1.2.1 - INTERNAL CLOCKS



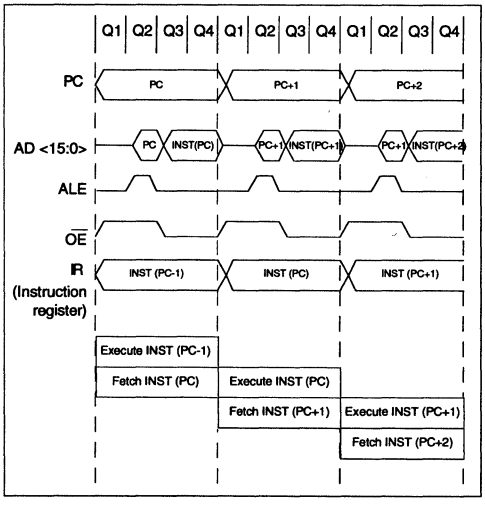
1.3 Instruction Flow/Pipelining

An "Instruction Cycle" in PIC17C42 consists of Q1, Q2, Q3 and Q4. Instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO), then two cycles are required to complete the instruction. Additionally, there are two instructions, TABLRD and TABLWT, which take two or more cycles to complete. These are explained in more details 'Instruction Set' description.

A fetch cycle begins with the program counter (PC) incrementing in Q1. In external execution, the address is presented on pins AD15 - AD0 during Q2. The instruction is latched on the falling edge of Q4.

The fetched instruction is latched into the "Instruction Register (IR)", which is decoded in Q1 and executed during Q2, Q3 and Q4. Data memory is read during Q2 (operand read), ALU operations are done in Q3 and result is written back during Q4 (destination write).

FIGURE 1.3.1 - INSTRUCTION FETCH/ EXECUTE PIPELINE



1.4 Memory Organization

The PIC17C42 employs a Harvard architecture, i.e. it has separate program and data memory space. In addition, there is a hardware stack separate from both data and program space. The data space is 256 bytes in size. Most of the data space is implemented as static RAM (address 18h to FFh). Special function registers, implemented as individual hardware registers make up the rest of the data space. Refer to Section 1.6 for more details. Data memory "address" and "data" buses are not brought outside the chip. So the data memory can not be expanded externally. The user can, however, create data segments in external program memory, use TABLWT and TABLRD instructions to move data between external program memory and the register file.

The program memory is 16-bits wide. It is addressed by the 16-bit program counter for instruction fetch. It is also addressed by the table pointer register (TBLPTR, also 16-bits wide) for data move to and from data space. Addressable program memory is 64K x 16. The PIC17C42 incorporates 2K x 16 EPROM program memory on-chip.

1.5 Different Program Memory Organization

The PIC17C42 operates in on of four possible program memory configurations which are:

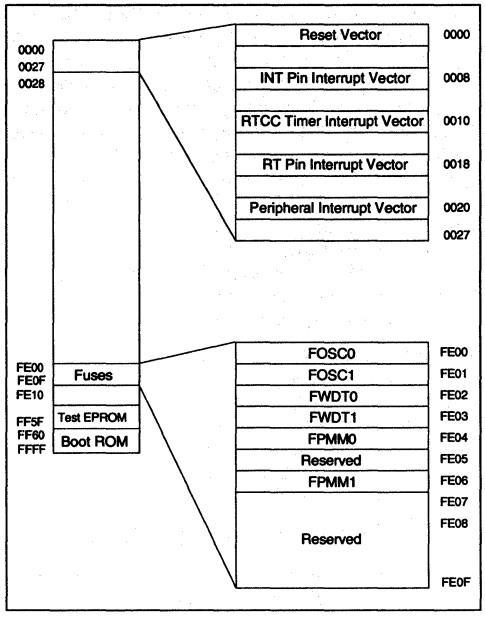
Microcontroller Mode: In this mode, only internal execution is allowed and therefore, only the on-chip 2K program memory is available. Any access to program memory beyond 2K reads 0000h (which is NOP). In addition to program memory, fuses, test memory, and boot memory (FE00h to FFFFh) are accessible.

Protected Microcontroller Mode: It is the same as microcontroller mode except that code protection is enabled. Refer to Section 4.7 for details on code protection.

Extended Microcontroller Mode: In this mode, on chip program memory (0-2K) as well as external memory (2K - 64K) are available. Execution automatically switches to external if program memory address is greater than 07FFh. The fuses, test memory and the boot memory are not accessible in this mode.

Microprocessor Mode: In this mode the on-chip program memory is not used. The entire 64K program memory is mapped externally. The fuses, test memory and the boot memory are not accessible in this mode.

FIGURE 1.5.1 - PROGRAM MEMORY MAP



The different modes are selected by fuses FPMM0 and FPMM1. These fuses are mapped in the following program memory locations:

FPMM0: FE04h

FPMM1: FE06h

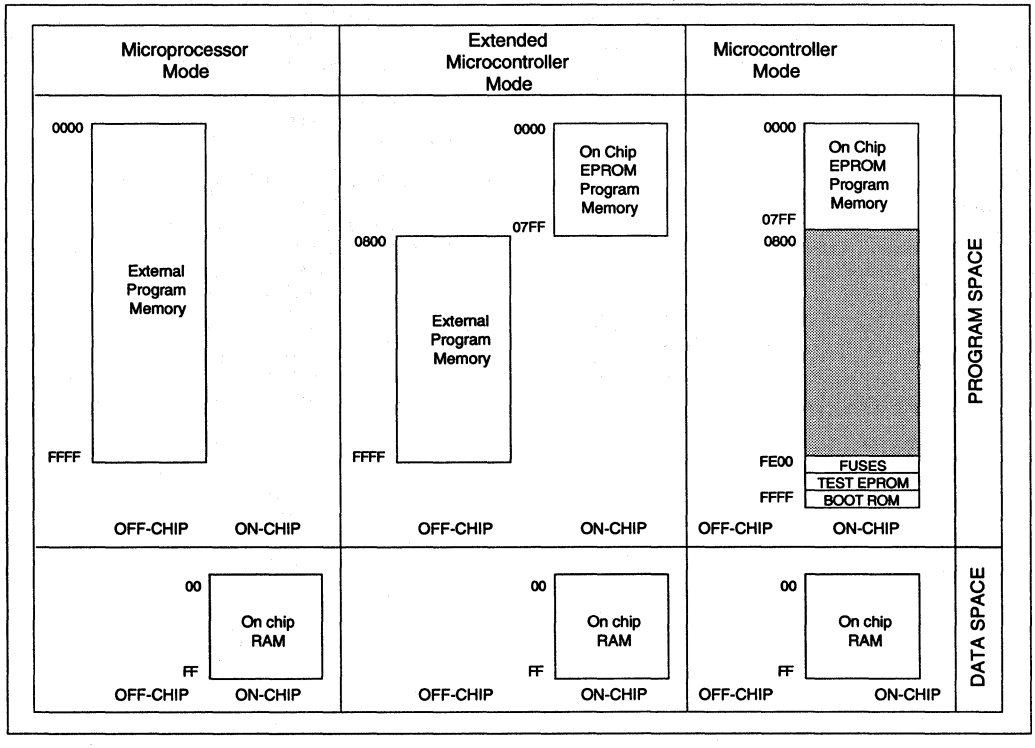
FPMM0	FPMM1	Mode
0	0	Microcontroller Mode (Code Protected)
0	1	Microcontroller Mode (Unprotected)
1	0	Extended Microcontroller Mode
1	1	Microprocessor Mode

Note: * 1 = fuse unprogrammed or erased,
0 = fuse programmed.

Refer to Section 4.7 for information on code protection.

Test Memory, Boot Memory and Fuse Locations: Test memory space is used by the factory for testing purposes. The 'boot ROM' area holds programs used for programming and verification. The user need not be concerned about either of these. The fuse locations map configuration fuses used to select from various operating modes. The fuses are explained in detail in Section 3.8.

FIGURE 1.5.2 - MEMORY MAP IN DIFFERENT MODES



1.5.1 EXTERNAL PROGRAM MEMORY INTERFACE

If external execution is selected, ports C, D and E are configured as a system bus for external program memory access. Ports D and C, together, constitute a 16-bit wide multiplexed address and data bus. The three bit E port outputs control signals ALE (Address Latch Enable), $\overline{OE}$ (Output Enable) and $\overline{WR}$ (Write Enable). An external memory access cycle is comprised of four oscillator cycles (from Q1 rising edge to Q1 rising edge). During Q2, a 16-bit address is presented on ports C and D (RD7 = MSB, RC0 = LSB) and ALE is asserted. The address output should be latched by the falling edge of ALE. In an instruction fetch or data read cycle, the $\overline{OE}$ is asserted during Q3 and Q4. The data is latched on the rising edge of OE. One oscillator cycle separation between OE ↑ and address output guarantees adequate time for external memories to shut off their output drivers before address is driven on to the bus.

In a data write cycle (only during TABLWT instruction), following address output during Q2, data is driven onto the bus during Q3 and Q4. $\overline{WR}$ is asserted during Q4 and the data output is valid both on its falling and rising edge.

Figure 1.5.1.1 depicts read and write cycles and Table 1.5.1.1 shows access time required of the external memory components. For complete timing information on the system bus, refer to the AC Characteristics Section.

FIGURE 1.5.1.1 - EXTERNAL PROGRAM MEMORY READ AND WRITE TIMINGS

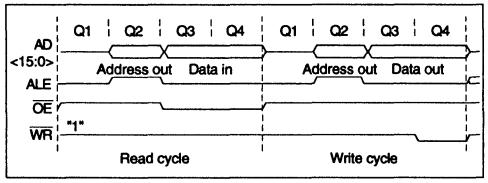
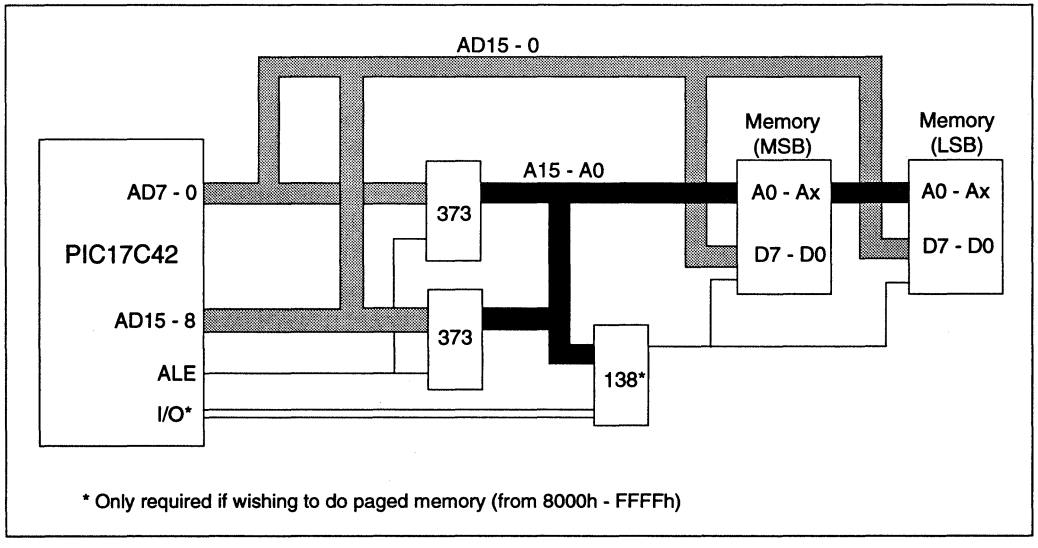


TABLE 1.5.1.2 - ACCESS TIME REQUIREMENTS FOR EXTERNAL MEMORY

Osc frequency	Instruction cycle time (Tcy)	tacc	toe
8 MHz	500ns	345ns	190ns
16 MHz	250ns	157.5ns	65ns
20 MHz	200ns	120ns	40ns
25 MHz	160ns	90ns	20ns

Note: Estimated access time requirements. Exact number will be available after full characterization.

FIGURE 1.5.1.2 - TYPICAL MICROPROCESSOR MODE MEMORY CONNECTION DIAGRAM



1.6 Data Memory Organization

Data memory in the PIC17C42 is organized as 256 x 8. It is accessed via an internal 8-bit data bus and an 8 bit data-memory-address-bus (derived from the instruction register). Data memory can be addressed via direct addressing mode or through indirect addressing mode using file select registers FSR0 or FSR1 as pointer registers.

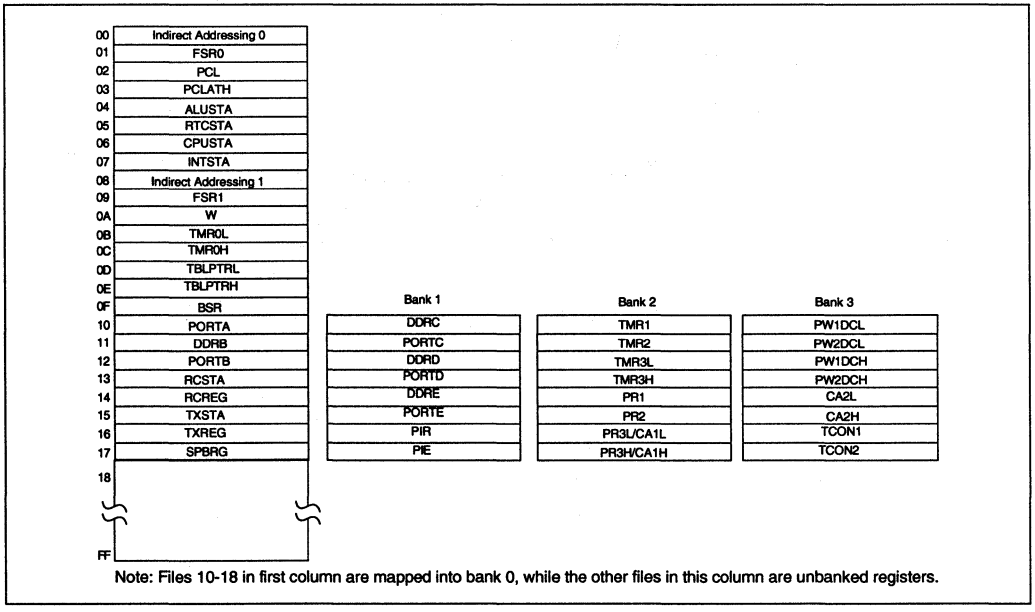
All special function registers (e.g. W, TMR0, Program Counter, Ports) are mapped in the data memory. The rest of the data memory is implemented as static RAM. A few special function registers such as Table Latches (TBLATH, TBLATL) are not mapped in data memory or any other memory space. Also not addressable are the watchdog timer and the stack pointer.

1.6.1 ORGANIZATION OF SPECIAL FUNCTION REGISTERS

Figure 1.6.1 shows the data memory space in detail:

a. Address 00h:0Fh are mostly special function registers related to the CPU.
b. Address 10h:17h are 'peripheral registers' such as timer register or port data latch. Since there are many more peripheral registers than can be mapped into eight address locations, a banking scheme is used. A bank select register, BSR (address 0Fh) is used to select one of many banks. Only the lower 4 bits of BSR are implemented in the PIC17C42, making it possible to address up to 16 banks.
c. Address locations 18h:1Fh are general purpose file registers implemented as part of the static RAM. However, these locations have the added privilege of being source or destination of a MOVPF or MOVFP instruction respectively.
d. Locations 20h:FFh are general purpose file registers implemented as static RAM.

FIGURE 1.6.1 - DATA MEMORY MAP



Note: Files 10-18 in first column are mapped into bank 0, while the other files in this column are unbanked registers.

FIGURE 1.6.2 - REGISTER FILE SUMMARY (PIC17C42)

Filename		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0	Value on power on reset	Value on all other reset (note3)	
UNBANKED:												
00	INDF0	Uses contents of F1 to address data memory (not a physical register)								00000000	00000000	
01	FSR0	Indirect data memory address pointer 0								xxxxxxxx	uuuuuuuu	
02	PCL	Low order 8 bits of PC								00000000	00000000	
03	PCLATH	Holding register for upper 8 bits of PC (Note 1)								xxxxxxxx	uuuuuuuu	Note 1
04	ALUSTA	FS3	FS2	FS1	FS0	OV	Z	DC	C	1111xxxx	1111uuuu	
05	RTCSTA	INTEDG	RTEDG	T/C	RTPS3	RTPS2	RTPS1	RTPS0	-	00000000	00000000	
06	CPUSTA	-	-	STKAV	GLINTD	TO	PD	-	-	00111100	0011??00	Note 2
07	INTSTA	PEIR	RTXIR	T0IR	INTIR	PEIE	RTXIE	T0IE	INTIE	00000000	00000000	
08	INDF1	Uses contents of F9 to address data memory (not a physical register)								00000000	00000000	
09	FSR1	Indirect data memory address pointer 1								xxxxxxxx	uuuuuuuu	
0A	W	W register								xxxxxxxx	uuuuuuuu	
0B	TMR0L	Timer0 Low byte								xxxxxxxx	uuuuuuuu	
0C	TMR0H	Timer0 High byte								xxxxxxxx	uuuuuuuu	
0D	TBLPTRL	Low byte of program memory table pointer								xxxxxxxx	uuuuuuuu	
0E	TBLPTRH	High byte of program memory table pointer								xxxxxxxx	uuuuuuuu	
0F	BSR	Bank select register								00000000	00000000	
BANK0:												
10	PORTA	PUEB	-	RA5	RA4	RA3	RA2	RA1/RT	RA0/INT	00xxxxxx	00uuuuuu	
11	DDRB	Data Direction Register for PORTB								11111111	11111111	
12	PORTB	PORTB data latch								xxxxxxxx	uuuuuuuu	
13	RCSTA	SPEN	RC8/9	SREN	CREN	-	FERR	OERR	RCD8	0000000x	0000000u	
14	RCREG	Serial Port Receive Register								xxxxxxxx	uuuuuuuu	
15	TXSTA	CSRC	TX8/9	TXEN	SYNC	-	-	TRMT	TXD8	0000001x	0000001u	
16	TXREG	Serial Port Transmit Register								xxxxxxxx	uuuuuuuu	
17	SPBRG	Baud Rate Generator								xxxxxxxx	uuuuuuuu	
BANK1:												
10	DDRC	Data Direction Register for PORTC								11111111	11111111	
11	PORTC	PORTC data latch								xxxxxxxx	uuuuuuuu	
12	DDRD	Data Direction Register for PORTD								11111111	11111111	
13	PORTD	PORTD data latch								xxxxxxxx	uuuuuuuu	
14	DDRE	Data Direction Register for PORTE								00000111	00000uuu	
15	PORTE	PORTE data latch								00000xxx	00000uuu	
16	PIR	IRB	TM3IR	TM2IR	TM1IR	CA2IR	CA1IR	TBMT	RBFL	00000010	00000010	
17	PIE	IEB	TM3IE	TM2IE	TM1IE	CA2IE	CA1IE	TXIE	RCIE	00000000	00000000	
BANK2:												
10	TMR1	Timer1								xxxxxxxx	uuuuuuuu	
11	TMR2	Timer2								xxxxxxxx	uuuuuuuu	
12	TMR3L	Timer3 Low byte								xxxxxxxx	uuuuuuuu	
13	TMR3H	Timer3 High byte								xxxxxxxx	uuuuuuuu	
14	PR1	Timer1 Period Register								xxxxxxxx	uuuuuuuu	
15	PR2	Timer2 Period Register								xxxxxxxx	uuuuuuuu	
16	PR3L/CA1L	Timer3 Period Register, low byte/capture1 register, low byte								xxxxxxxx	uuuuuuuu	
17	PR3H/CA1H	Timer3 Period Register, High byte/capture1 register, high byte								xxxxxxxx	uuuuuuuu	
BANK3:												
10	PW1DCL	DC1	DC0	-	-	-	-	-	-	xx000000	uu000000	
11	PW2DCL	DC1	DC0	TM2PW2	-	-	-	-	-	xx000000	uu000000	
12	PW1DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxxxxxx	uuuuuuuu	
13	PW2DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxxxxxx	uuuuuuuu	
14	CA2L	Capture2 low byte								xxxxxxxx	uuuuuuuu	
15	CA2H	Capture2 high byte								xxxxxxxx	uuuuuuuu	
16	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	16/8	TMR3C	TMR2C	TMR1C	00000000	00000000	
17	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/PR3	TMR3ON	TMR2ON	TMR1ON	00000000	00000000	

x = unknown
u = unchanged

Notes:

1: The upper byte of the program counter is not directly accessible. f03 is a holding register for PC<15:8> whose contents are updated from or transfered to the upper byte of the program counter.

2: The "TO" and PD" status bits in f06h are not affected by a "MCLR" reset. TO bit will be reset in the event of a WDT time-out reset.

3: Other (non power-up) resets include external reset through MCLR pin and Watchdog Timer timeout reset.

2.0 HARDWARE DESCRIPTION OF THE CPU

2.1 Indirect Addressing Registers (INDF0 and INDF1)

These two register locations (not physically implemented) are used to implement indirect addressing of data memory space. An instruction using INDF0 or INDF1 actually accesses the data memory location pointed to by the corresponding FSR registers. If file INDF0 (or INDF1) itself is read indirectly via an FSR, all zeroes are read. Similarly, if INDF0 (or INDF1) is written to indirectly, the operation will be equivalent to a NOP.

Single cycle data transfers within the entire data space are possible with MOVFP and MOVPF instructions, when "p" is specified as INDF0 and "f" as INDF1, or vice versa.

2.2 File Select Registers (FSR0 and FSR1)

These two registers are 8-bit wide indirect address pointers for data memory. They can be auto-incremented, auto-decremented or left unchanged after each access as determined by the four control bits in the STATUS register "ALUSTA" (File 04h bits 7:4). See Figure 2.8.1.

2.3 Table Pointer (TBLPTRL and TBLPTRH)

File registers TBLPTRL and TBLPTRH form a 16-bit pointer to address the 64K program memory space. The table pointer is used by instructions TABLWT and TABLRD.

The TABLRD and the TABLWT instructions allow transfer of data between program and data space. The table pointer serves as the 16-bit address of the data word within the program memory.

3.4 Table Latch (TBLATH, TBLATL)

The table latch (TBLAT) is a 16-bit register, consisting of TBLATH and TBLATL refer to the high and low bytes of the register. It is not mapped into data or program memory. The table latch is used as a temporary holding latch during data transfer between program and data memory (see descriptions of instructions TABLRD, TABLWR, TLRD and TLWR).

2.5 Program Counter Module

The Program Counter (PC) is a 16-bit register. PCL, the low byte of the PC, is mapped in the data memory (file 02h). PCL is readable and writable just as any other register. PCH is the high byte of the PC and is not directly addressable since PCH is not mapped in data or program memory. An 8-bit register PCLATH (PC high latch) is used as a holding latch for the high byte of the PC. PCLATH is mapped into data memory (file 03h). The user can read or write PCH through PCLATH.

The 16-bit wide PC is incremented after each instruction fetch during Q1 unless modified by GOTO, CALL, LCALL, RETURN, RETLW, or RETFIE instruction or interrupt response or due to destination write to PCL by an instruction. "Skip"s are equivalent to incrementing the PC twice.

The operations of the PC and PCLATH for different instructions are as follows:

a) LCALL:

PCLATH → PCH , IR<7:0> → PCL (PCL is loaded with 8-bit destinaton address embedded in the instruction. PCLATH is unchanged.

b) CALL, GOTO:

A 13-bit destination address is provided in the instruction
IR<12:0> → PC <12:0>
PC<15:13> → PCLATH<7:5>

c) Read PCL (Any instruction that reads PCL):

PCL → data bus → ALU or destination
PCH → PCLATH

d) Write PCL (Any instruction that writes to PCL):

8-bit data → data bus → PCL
PCLATH → PCH

e) Read-Modify-Write (Any instruction that does a read-write-modify operation on PCL, such as ADDWF PCL)

Read: PCL → data bus → ALU
Write: 8-bit result → data bus → PCL
PCLATH → PCH

Note that read-modify-write only affects the PCL with the result. PCH is loaded with PCLATH. Thus, ADDWF PCL, for example will result in a jump within the current page. If PC = 03F0h, W = 30h and PCLATH = 03h before instruction, PC = 0320h after the instruction. To accomplish a true 16-bit computed jump, the user needs to compute the 16-bit destination address, write the high byte to PCLATH and then write the low value to PCL.

The following PC related operations do not change PCLATH:

a) LCALL, RETLW, RETURN, RETFIE instructions,
b) Interrupt vector is forced onto the PC,
c) Read-modify-write instructions (e.g. BSF PCL) on PCL.

2.6 Stack

The PIC17C42 has a 16-word x 1- bit hardware stack which is not part of data or program space. The PC is pushed onto the stack if CALL or LCALL instructions are executed or if an interrupt is responded to by branching to the corresponding interrupt vector. The stack is POPed into the PC if a RETURN, RETLW or RETFIE instruction is executed. The top of the stack is not addressable in any other way.

2.6.1 STACK AVAILABLE STATUS BIT (BIT 5, CPUSTA)

STKAVL is a read only status bit that indicates any stack overflow error. STKAVL is set on reset and stays set unless the following situation occurs:

If stack is full: i.e. there are 16 entries in the stack the STKAVL is cleared. If the stack is popped (by RETURN, RETLW or RETFIE instruction) then STKAVL is set again indicating 'stack availability'.

If, however, a push takes place instead (due to CALL, LCALL or interrupt), then stack overflow occurs. In this event, the first entry is lost and STKAVL is permanently cleared . Under this condition, the only way STKAVL will be set is via reset.

STKAVL usage caution: If the stack is empty, a POP (due to RETURN, RETLW or RETFIE) followed by a PUSH, will permanently clear STKAVL.

For a description of CPUSTA register, see Figure 4.5.1.

2.6.2 USING THE STKAVL BIT

One way to use the STKAVL bit is to test it at the beginning of every subroutine or interrupt service routine. If STKAVL is clear, then all stack locations are used (and presumably no error has occurred yet). In such case, interrupts must be disabled in the subroutine. Also, no subroutine calls must be made unless software stack management is invoked.

2.7 Interrupt Logic

The PIC17C42 has 11 interrupt sources that are mapped into 4 interrupt vectors. The interrupt logic is controlled by the INTSTA register and the global interrupt disable bit (GLINTD) in CPUSTA register. See Figure 4.5.1 for a description of CPUSTA register. Four hard-wired vectors allow fast interrupt response time. Worst case latency is three instruction cycles when only one interrupt at a time is being serviced. Interrupt nesting to multiple levels is possible by enabling interrupts within the service routine. When an interrupt occurs, the current PC value is pushed onto the stack and the vector corresponding to the interrupt source is loaded into the PC.

Note 1: Individual interrupt flag bits are set regardless of the status of the corresponding mask bit or the GLINTD bit.

Note 2: If an interrupt occurs while the Global Interrupt Disable (GLINTD) bit is being set, the GLINTD bit may unintentionally be re-enabled by the user's `RETFIE` instruction at the end of the Interrupt Service Routine (the `RETFIE` instruction). The events that would cause this to occur are:

1. An instruction sets the GLINTD bit while an interrupt is acknowledged
2. The program branches to the Interrupt vector and executes the Interrupt Service Routine.
3. The Interrupt Service Routine completes with the execution of the `RETFIE` instruction.
   This causes the GLINTD bit to be cleared (enables interrupts), and the program returns to the instruction after the one which was meant to disable interrupts.

The method to ensure that interrupts are globally disabled is:

1. Ensure that the GLINTD bit was cleared by the instruction, as shown in the following code:

```
LOOP  BSF   CPUSTA, GLINTD ; Disable Global
                           ;   Interrupts
      BTFSS CPUSTA, GLINTD ; Global
                           ;   Interrupts
                           ;   Disabled?
      GOTO  LOOP           ; NO, try again
      :                    ; Yes, continue
                           ;   with program
                           ;   flow
```

2.7.1 INTERRUPT FLAG AND MASK BITS

Each interrupt has a request flag bit and a mask bit associated with it. The registers that hold these bits are INTSTA (file 07h), PIR (Bank 1, file 16h) and PIE (Bank 1, file 17h). See Table 3.7.1 for details.

Interrupt flag bits INTIR, T0IR or RTXIR are cleared automatically in hardware. PEIR is not cleared automatically since it is not a latched bit. PEIR is simply the OR of all the individual peripheral interrupt flag bits such as IRB, TM3IR, etc. Therefore, if PEIR is the source of the interrupt, the user must clear, in software, the actual peripheral interrupt flag bit. The global interrupt disable bit, GLINTD, is set, preventing any further interrupt. To enable interrupts from the service routine the user must clear GLINTD. The user must first clear the current interrupt flag bit to prevent recursive vectoring to the same service routine.

The TABLWT instruction, in a long write situation (i.e. writing to on-chip EPROM location) must be terminated with an interrupt. On completion, TABLWT clears the interrupt flag in the same exact fashion as an interrupt response, i.e. INTIR, RTCIR or RTXIR flag will be cleared if responsible for ending the TABLWT.

2.7.2 PERIPHERAL INTERRUPTS

All peripherals use the same interrupt vector, 0020h. The individual peripheral interrupt request bits are "OR-ed" together. When multiple peripheral interrupt sources are enabled, the priorities have to be determined by software. Each peripheral has its own interrupt enable and request bit(s). In addition, the PEIE (Peripheral Interrupt Enable) bit acts as a global enable bit for all peripheral interrupts. There is a common peripheral interrupt request status bit (PEIR, bit 7, register INTSTA)which is a logical OR of all the individual peripheral interrupt request flags. This is a read only status bit useful for quickly determining if any peripheral request is outstanding.

2.7.3 INTERRUPT AND TABLWT INTERACTION

On the PIC17C42, the TABLWT instruction can be used to either program the on-chip EPROM or to write to an external memory mapped in address space. In order to accomplish a write to internal program memory (i.e. program the EPROM), interrupts are required to time the programming event. If a TABLWT is executed and the table-latch is pointing to an internal memory location, the PIC17C42 goes into a long write (i.e. programming is initiated). The PIC17C42 stays in a long write mode until either an unmasked interrupt occurs or the chip is reset. If an unmasked interrupt occurs the long write is terminated, the interrupt that caused the termination is cleared in hardware (except for peripheral interrupts which are never cleared in hardware). Only the interrupt that caused the termination of the TABLWT instruction is cleared. In the case where an interrupt is pending, the TABLWT is aborted and no programming occurs but the interrupt flag is still cleared. This sequence of events is true for any TABLWT regardless of an internal write or an external write.

A table write to locations off-chip to the PIC17C42 are handled much the same way as internal writes. The major difference is that the table is forced to be a two-cycle only instruction since it will only take one cycle to actually write the external memory locations. The interrupt interaction, however, is the same. If an unmasked interrupt is pending or occurs during an external TABLWT, the interrupt is cleared (except for peripheral interrupts). Since the external TABLWT is already forced to a two-cycle instruction, the external TABLWT is already forced to a two-cycle instruction, the external write still occurs.

If the application is doing an external TABLWT and using hardware clearable interrupts (RT, INT, TMR0), then it is important to mask those interrupts during a TABLWT so the interrupt flag is not cleared as a result of the TABLWT.

2.7.1 - TABLE OF INTERRUPTS

Interrupt flag	Flag location bit, Register	Interrupt mask bit	Mask bit location bit , Register	Interrupt Source	Priority	Vectors to
INTIR	bit 4,INTSTA	INTIE	bit 0, INTSTA	External interrupt on INT pin	Highest priority	0008h
T0IR	bit 5,INTSTA	T0IE	bit 1, INTSTA	TMR0 overflow interrupt	2nd priority	0010h
RTXIR	bit 6, INTSTA	RTXIE	bit 2, INTSTA	External interrupt on RT pin	3rd priority	0018h
PEIR	bit 7, INTSTA	PEIE	bit 3, INTSTA	Any peripheral interrupt	Lowest priority	0020h
IRB	bit 7, PIR	IEB	bit 7, PIE	Port B input change interrupt	lowest priority	0020h
TM3IR	bit 6, PIR	TM3IE	bit 6, PIE	Timer/Counter3 interrupt	(All these	
TM2IR	bit 5, PIR	TM2IE	bit 5, PIE	Timer/Counter2 interrupt	peripheral	
TM1IR	bit 4, PIR	TM1IE	bit 4, PIE	Timer/Counter1 interrupt	interrupts are	
CA2IR	bit 3, PIR	CA2IE	bit 3, PIE	Capture1 interrupt	OR'ed together	
CA1IR	bit 2, PIR	CA1IE	bit 2, PIE	Capture2 interrupt	to generate	
TBMT	bit 1, PIR	TXIE	bit 1, PIE	Serial port transmit interrupt	PEIR)	
RBFL	bit 0, PIR	RCIE	bit 0, PIE	Serial port receive interrupt		

FIGURE 2.7.1.1 - REGISTER INTSTA

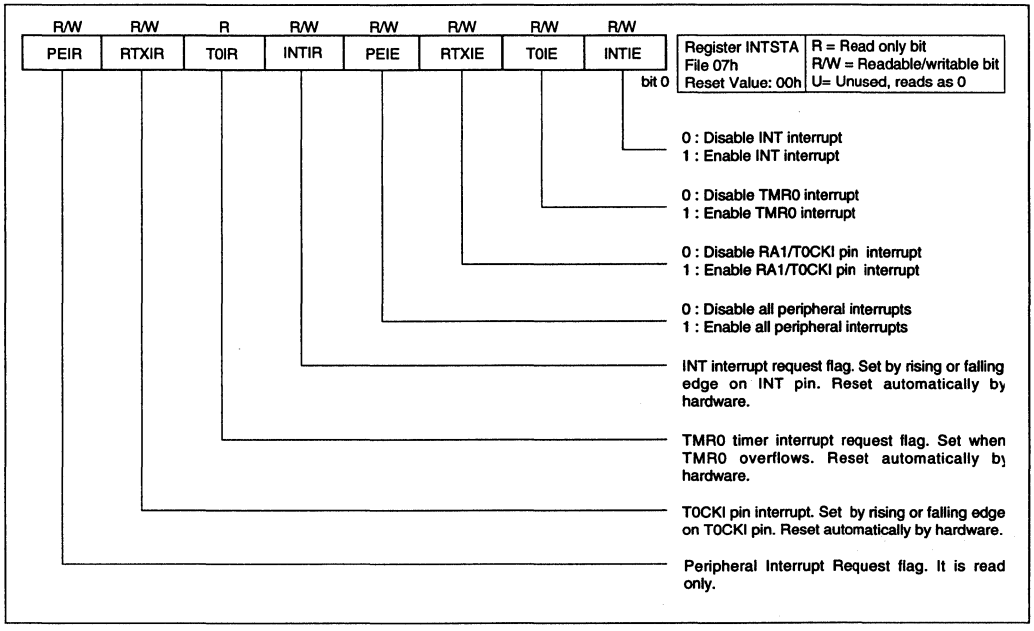


FIGURE 2.7.1.2 - PIR (PERIPHERAL INTERRUPT REQUEST) REGISTER

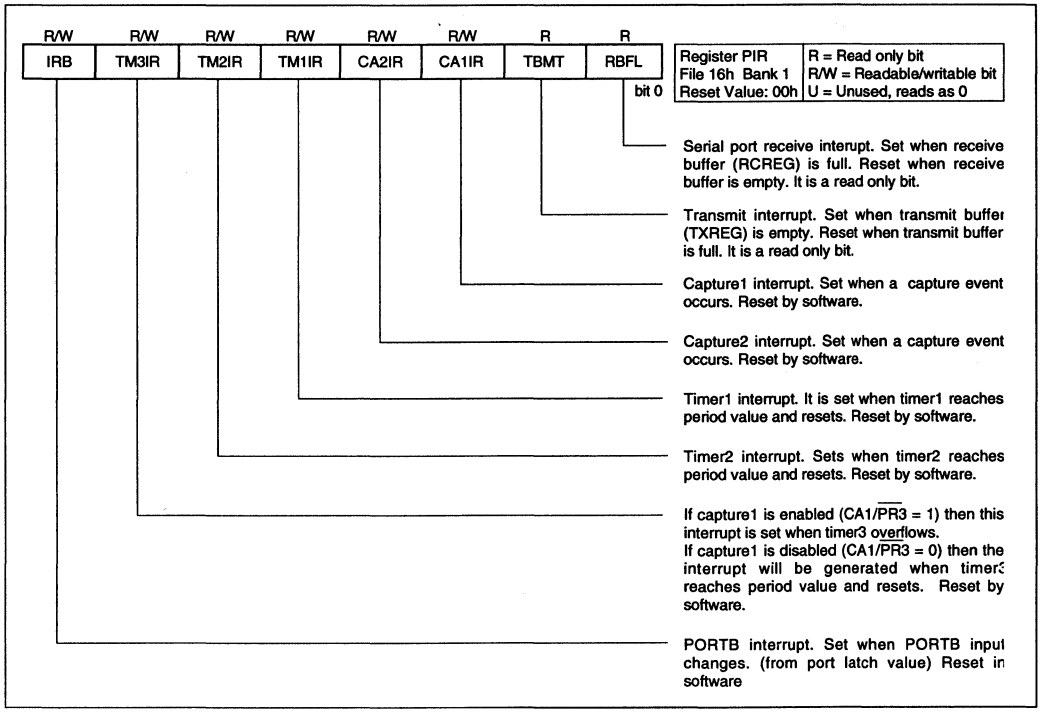
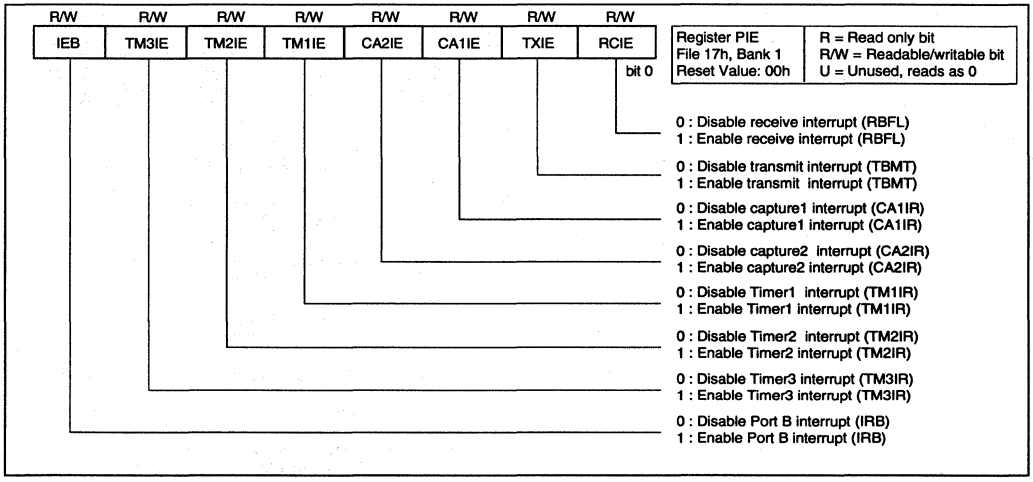


FIGURE 2.7.1.3 - PIE (PERIPHERAL INTERRUPT ENABLE) REGISTER



2.7.4 INT AND RT EXTERNAL INTERRUPTS

INT and RT external interrupts can be positive or negative edge triggered, selectable in software. INT interrupt is generated on falling edge if INTEDG = 0 or on rising edge if INTEDG = '1'. Similarly, setting bit RTEDG = '0' will generate T0CKI pin interrupt on falling edge whereas RTEDG = '1' will trigger RT interrupt on rising edge. The timing requirements on INT and RT inputs are as follows:

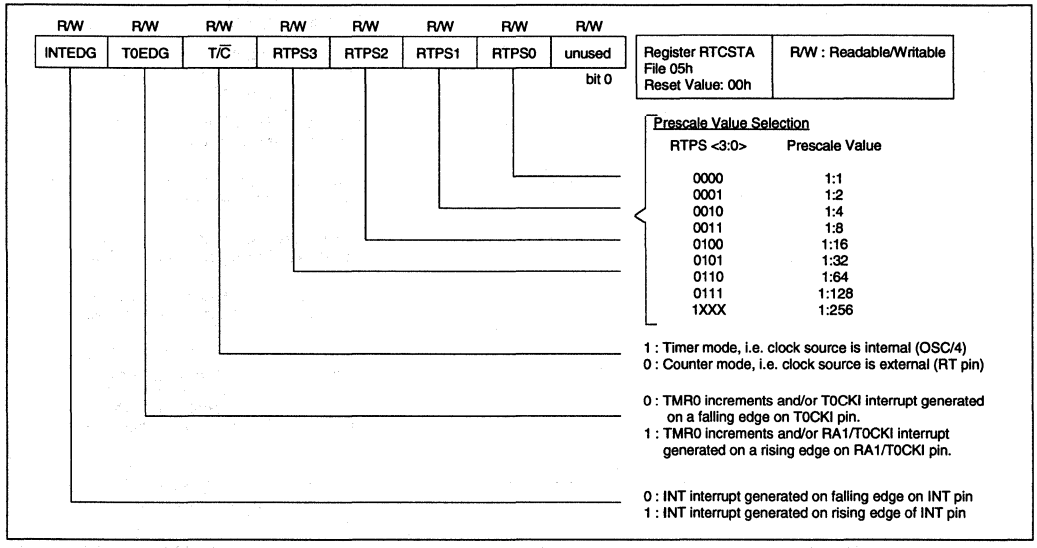
t_{INTH} = t_{RTIH} = INT or RT high time ≥ 25ns

t_{INTL} = t_{RTIL} = INT or RT low time ≥ 25ns

Please note that changing edge selection for INT or RT pin may generate a false interrupt. The user should clear the INTIR or the RTXIR bit after changing edge setting.

See RTCSTA (register file 05h) for bit allocation.

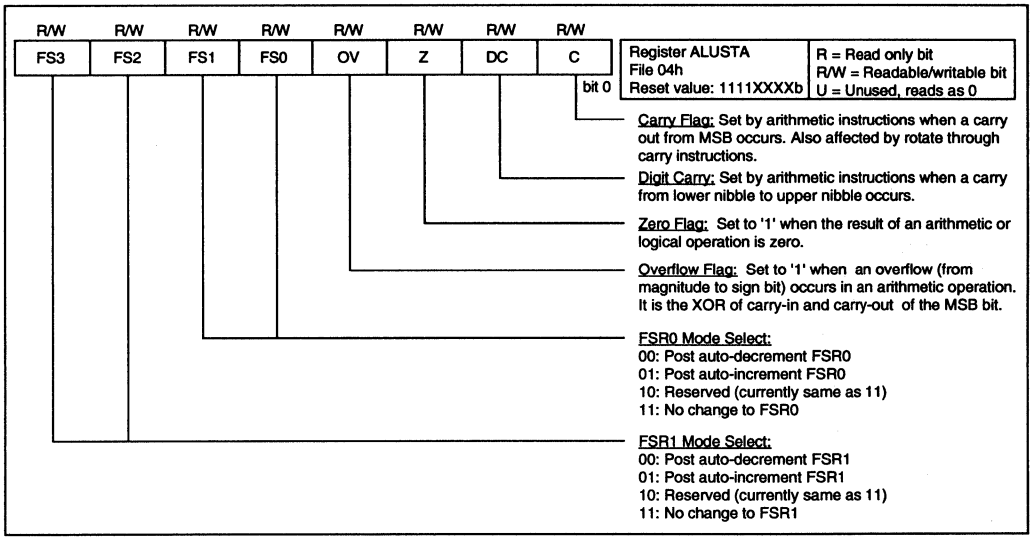
FIGURE 2.7.3.1 - RTCSTA: TMR0 STATUS/CONTROL REGISTER



2.8 ALU

The Arithmetic and Logic Unit of the PIC17C42 is capable of carrying out arithmetic or logical operations on two operands or a single operand. All single operand instructions operate either on the W register or a file register. For two operand instructions, one of the operands is the W register and the other one is either a file register or an 8-bit immediate constant.

FIGURE 2.8.1 - ALUSTA (ALU STATUS) REGISTER



3.0 SPECIAL FEATURES OF THE CPU

What sets apart a microcontroller from other processors the most are special circuits to deal with the needs of real time applications. The PIC17C42 has a host of such features intended to maximize system reliability, minimize cost through elimination of costly external components, provide power saving operating modes and offer code protection.

The PIC17C42 has a Watchdog Timer which can be shut off only through EPROM fuses. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 80ms nominal on power up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on chip, most applications need no external reset circuitry. The SLEEP mode is designed to offer a very low current power-down mode. The user can wake up from SLEEP through external reset, Watchdog Timer timeout or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LF (Low Frequency) crystal/resonator option saves power. A set of EPROM configuration bits (fuses) are used to select various options. Additional EPROM fuses are included for code-security.

3.1 Reset

The reset logic resets the complete PIC17C42 circuitry as follows:

- Oscillator buffer is enabled (i.e. oscillator is restarted if waking up from SLEEP through reset).
- Program Counter is reset to 0000h.
- All registers are reset as described in Table 1.6.2.
- Watchdog timer and its prescaler are cleared.
- Internal phase clock generator is held in Q1 state. If external execution is selected, ALE output is held low while $\overline{OE}$ and $\overline{WR}$ outputs are driven high.
- I/O ports B, C, D and E are configured as inputs. In case of port B, the weak pull-ups are activated. Ports RA2 and RA3 revert to high impedance state.

There are three events which can cause a device reset.

a) Power-On Reset :V_{DD} rise is detected (1.2V - 2.0V range)

b) External reset: "Low" level on the $\overline{MCLR}$ input

c) WDT reset: Watchdog Timer Timeout

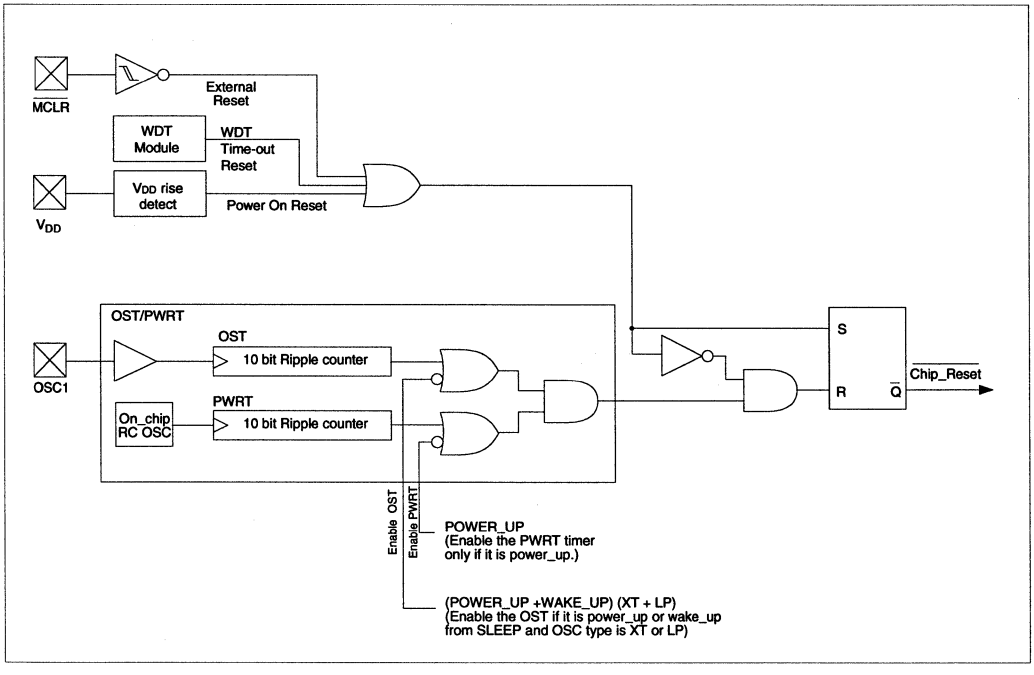
The RESET condition is maintained as long as:

a) The $\overline{MCLR}$ input is "low"

b) $\overline{MCLR}$ has gone high but the Power-up Timer (PWRT) is active, (i.e. has not timed out)

c) $\overline{MCLR}$ has gone high but the Oscillator Start-up Timer (OST) is active (i.e. has not timed out)

FIGURE 3.1.1 - SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



3.2 Oscillator

The PIC17C42 can accept an external clock input on OSC1 pin or will run off external crystal or ceramic resonator connected between OSC1 and OSC2 pins. It also has an RC oscillator mode in which an external R and C combination can be connected to OSC1 pin. The choice is made by EPROM fuses FOSC1 and FOSC0. These fuses are mapped in program memory locations FE01h and FE00h respectively. Refer to section 4.8 for details on the fuses.

TABLE 3.2.1 - OSCILLATOR OPTIONS

Fosc1, Fosc0 Fuses	Mode	OSC1 Pin Function	OSC2 Pin Function	Freq. Range
11	EC: External Clock input	External clock input	CLKOUT output	DC-25Mhz
01	RC: RC oscillator mode	External RC oscillator connection	CLKOUT output	DC-4Mhz
10	XT: Crystal oscillator mode	Crystal connection	Crystal connection	0.2-25Mhz
00	LF: Low frequency crystal oscillator mode	Crystal connection	Crystal connection	32-200Khz

Note: 0 implies a programmed fuse.

3.2.1 EC: EXTERNAL CLOCK INPUT MODE:

The OSC1 input can be driven by CMOS drivers (figure 4.2.1A). In this mode, the OSC1 pin is a high impedance CMOS input. The OSC2 pin outputs CLKOUT (frequency = fosc/4). See Figure 3.2.1 for timing of CLKOUT.

3.2.2 RC: RC OSCILLATOR MODE:

An external R and C combination can be connected to OSC1 pin (Figure 3.2.1B). The RC oscillator mode provides a very cost effective solution. However, the frequency of oscillation will vary with Vcc, temperature and from chip to chip due to process variation. It is, therefore, not the right choice for timing sensitive applications where accurate oscillator frequency is desired. The OSC2 pin, in this mode, outputs CLKOUT (freq. = fosc/4). See Figure 3.2.1 for timing of CLKOUT.

3.2.3 XT: CRYSTAL OSCILLATOR MODE:

In this mode a crystal or a ceramic resonator can be connected across OSC1 and OSC2. (Figure 3.2.1C). The crystal must be of fundamental mode. If an overtone mode crystal is used (which is common above 20 MHz) then a tank circuit must be used to attenuate the gain at fundamental frequency (Figure 3.2.1D)

3.2.4 LF: LOW FREQUENCY CRYSTAL OSCILLATOR MODE:

This is same as the XT mode, (Figure 3.2.1E) except that it is suitable for crystals of frequency range 32 KHz to 200 KHz.

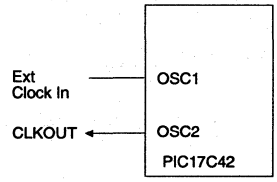
TABLE 3.2.2 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR†

Osc Type	Freq	C1	C2
LF	32KHz	300pF	300pF
	50KHz	15pF	300pF
	100KHz	50pF	200pF
	200KHz	50pF	200pF
XT	1MHz	500pF	500pF
	2MHz	500pF	500pF
	4MHz	300pF	300pF
	8MHz	200pF	200pF
	16MHz	200pF	100pF
	25MHz	TBD	TBD

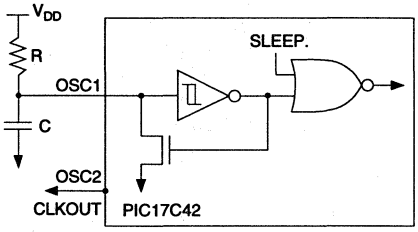
† This table is for design guidance. The values shown here are from a single manufacturer. Other crystal may require different C1 and/or C2 values.

FIGURE 3.2.1 - DIFFERENT OSCILLATOR/ CLOCKIN OPTIONS

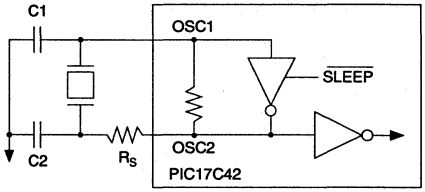
3.2.1A EXTERNAL CLOCK



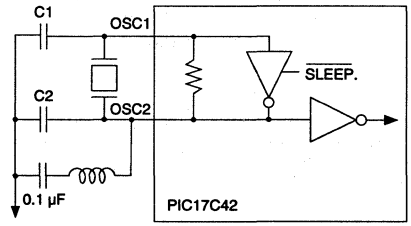
3.2.1B RC OSCILLATOR MODE



3.2.1C XT CRYSTAL OSCILLATOR MODE



3.2.1D XT CRYSTAL OSCILLATOR MODE (OVERTONE CRYSTALS)

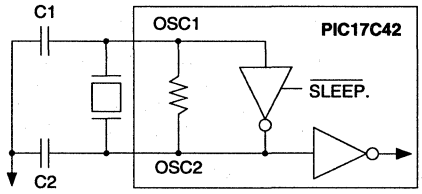


To Filter the fundamental frequency

$$\frac{1}{LC2} = (2\pi f)^2$$

Where f= tank circuit resonant frequency.This should be midway between the fundamental and the 3rd overtone frequencies of the crystal.

3.2.1E LF CRYSTAL OSCILLATOR MODE



3.3 Oscillator Start-up Timer (OST)

The OST provides a 1024 oscillator period delay on power-up and on wake up from SLEEP. This delay is provided by a 10-bit ripple counter. On power-up, the delay begins from the rising edge of MCLR. On wake-up from SLEEP the time-out is counted from the time the wake-up event occurs. Since the OST counts oscillator signal on OSC1 pin, the counter only starts counting when amplitude on OSC1 pin reaches a certain acceptable limit. The OST time-out allows the crystal oscillator (or resonator) to stabilize before the chip is taken out of reset. The circuit will function with crystals of any frequency. This time-out is not invoked in RC oscillator mode or external clock (EC) mode.

3.4 Power-up Timer (PWRT) and Power-on Reset (POR)

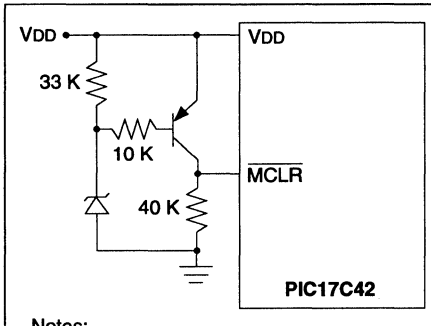
The function of the PWRT timer is to provide a fixed 80 ms (typical) delay only on power-up. This is provided by a 10-bit ripple counter whose input clock comes from an on chip RC oscillator. The time-out is counted from the rising edge of MCLR. The purpose of this time-out is to allow the VDD supply to reach acceptable level before the part is taken out of reset.

An internal Power-on Reset pulse (POR) is generated when a VDD rise is detected during initial power-up of the chip. (when VDD = 1.2V to 2.0V nominally). The POR signal resets internal registers as described in Table 1.6.2. The user should note that the on-chip circuitry does not generate an internal reset when VDD goes down, i.e., it does not provide brown out protection. Figures 3.4.1 and 3.4.2 shows possible external brown-out protection circuits. Also VDD must come up from VSS (nominal) for a POR signal to be generated. The PWRT timer and OST timer guarantee proper power-on reset without external components. This is done by simply tying the MCLR pin to VDD (Figure 3.4.4). As VDD comes up, POR is generated and MCLR is sensed as '1' inside the chip, both OST and PWRT timers begin time-out. The 80ms (nominal) delay of the PWRT allows VDD to rise above VDD min. spec. If the rise time of VDD is much slower such that at the end of the time-out VDD has not reached an acceptable level (as in Figure 3.4.6), then external RC delay must be added on MCLR pin.

The following table shows the time-outs for different oscillator types.

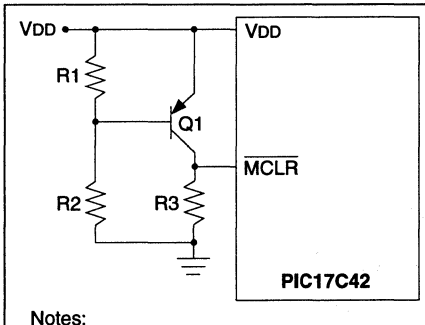
Oscillator Type	Power-up	Wake-up from SLEEP
EC	80 ms	—
RC	80 ms	—
XT	Greater of 80 ms and 1024 tosc	1024 tosc
LP	Greater of 80 ms and 1024 tosc	1024 tosc

FIGURE 3.4.1 - BROWN OUT PROTECTION CIRCUIT



Notes:
1. This circuit will activate reset when VDD goes below (VZ + 0.7 V) where VZ = Zener voltage.

FIGURE 3.4.2 - BROWN OUT PROTECTION CIRCUIT



Notes:
1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7\ V$$

FIGURE 3.4.3 - EXTERNAL RESET PULSE

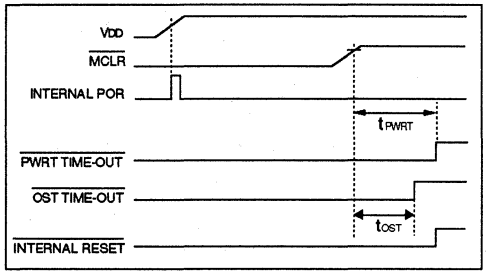


FIGURE 3.4.4 - USING ON-CHIP POR

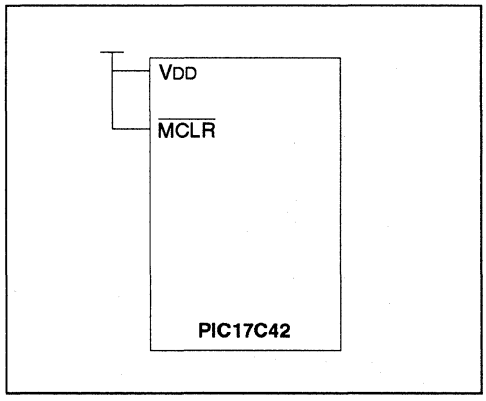
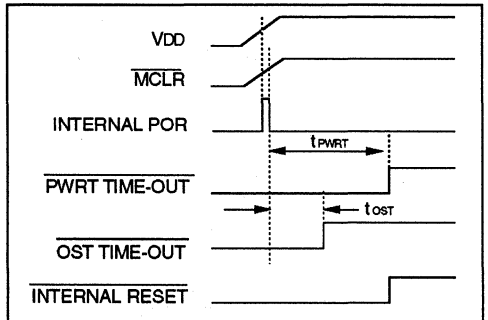
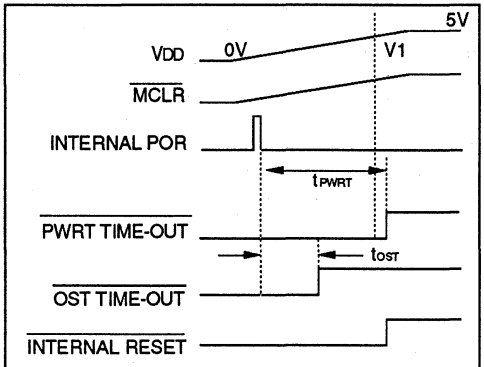


FIGURE 3.4.5 - INTERNAL RESET (VDD AND MCLR TIED TOGETHER)



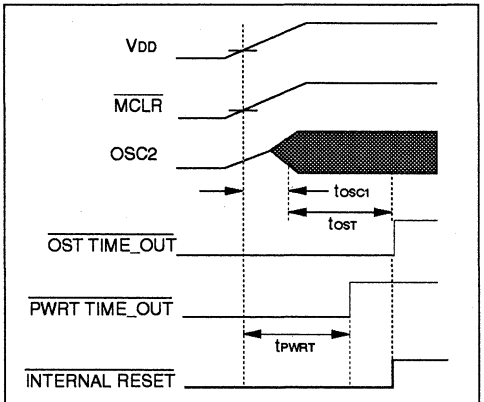
Note: In this example t PWRT> t OSTas would be the case in higher frequency crystals. For lowe frequency crystals (i.e. 32 Khz) tOST will be greater.

FIGURE 3.4.6 - INTERNAL RESET (VDD AND MCLR TIED TOGETHER): SLOW VDD RISE TIME



Note: In this example tPWRT > tOST, as would be the case in higher frequency crystals. For lower frequency crystals, (i.e. 32 Khz) tOST will be greater.

FIGURE 3.4.7 - OST START UP TIMING DETAILS



This figure shows in greater detail the timings involved with the oscillator start-up timer. In this example the low frequency crystal start-up time is larger than power-up time (tPWRT).

tOSC1 = time for the crystal oscillator to reach oscillation level detectable by the oscillator start-up timer (OST)

tOST = 1024 tosc

3.5 Sleep Mode

The full static design of the PIC17C42 makes it possible to put the part in a power saving SLEEP (or power down) mode in which all on chip clocks are stopped.

The SLEEP mode, entered by executing a SLEEP instruction, shuts down the oscillator, sets $\overline{TO}$ (bit3, CPUSTA), clears $\overline{PD}$ (bit2, CPUSTA) the Watchdog Timer and its prescaler. In XT or LP mode, both OSC1 and OSC2 are placed into high-impedance state. In EC and RC modes, OSC1 pin is placed in high-impedance state while OSC2 is driven low. No clocks are presented to the internal logic even when an external clock is present on the OSC1 pin. The chip will remain in a completely static condition with the following exceptions:

a) If the Watchdog Timer is enabled, it will keep running and will consequently wake up the chip on time-out.
b) Signal edges on the T0CKI pin (rising or falling whichever is defined to be the active edge by the RTEDG control bit) will increment the TMR0 prescaler (an asynchronous ripple counter) if an external clock source is selected for TMR0. The TMR0 itself will not increment.
c) Any external interrupt event, such as RT, INT, capture1 or capture2 interrupt will wake the processor provided the corresponding interrupt mask bit was enabled when entering SLEEP mode. If global interrupt disable is off (GLINTD=0) then the chip will jump to corresponding interrupt vector on wake-up. Otherwise the chip will wake up and resume executing without responding to the interrupt (i.e. will not branch to interrupt vector).
d) Any peripheral operating independent of the internal processor clock can change its status due to external events. Specifically, the serial port receive shift register will shift in data in synchronous slave (external clock) mode.

Besides the on-chip oscillator, any circuitry that consumes current is turned off in SLEEP mode. This includes the entire EPROM and, in particular, the EPROM fuses. The only fuses that will remain active are the WDT fuses (FWDT0, FWDT1). If minimal SLEEP current is desired, the user should consider turning off the watchdog timer. Since fuses consume current in '1' state. Turning WDT off not only saves the operating current it requires, but also saves fuse current due to FWDT1 or FWDT0 fuses. All I/O pins maintain their status during SLEEP.

3.5.1 WAKE-UP FROM SLEEP

Once the chip has entered the SLEEP mode it can only be awakened by one of the following events:

a) Bringing V_{DD} down to zero and back up to operational level will induce a power on reset and wake up the chip.
b) Applying a "low" level on $\overline{MCLR}$ pin
c) A Watchdog Timer timeout (WDT must be enabled). $\overline{TO}$ status bit will be cleared in this case.
d) The following interrupts can wake up the processor from SLEEP:
   1. External interrupt on T0CKI pin
   2. External interrupt on INT pin
   3. Capture1 interrupt, due to a capture event on the RB0/CAP1 pin. The prescaler on the capture input will operate during SLEEP. The actual capture of the timer value will occur when execution resumes after wake-up (which is therefore, not meaningful).
   4. Capture2 interrupt.
   5. Input change on PORTB interrupt
   6. Synchronous slave mode transmission interrupt: If synchronous transmission is in progress (using external clock) at the time the processor is put to SLEEP, a TBMT interrupt will be generated at the end of the transmission and wake the chip-up.
   7. Synchronous slave mode reception interrupt: If synchronous reception is enabled (CREN = 1) before the chip goes into SLEEP, then RBFL interrupt will be set at the end of a reception (if a receive word came during SLEEP) which will wake the chip-up.

If GLINTD = 0, the normal interrupt response takes place. If GLINTD = 1, the chip will resume execution starting with the instruction following the SLEEP instruction. It will not vector to interrupt service routine.

If selected oscillator type is XT or LF then the Oscillator Start-up Timer (OST) is activated on wake-up. This will mean that the timer will keep the part in reset for 1024 tosc. The user needs to take this into account when considering interrupt response time coming out of SLEEP.

3.5.2 INTERRUPT/SLEEP INTERACTION

If an interrupt occurs during the very cycle a SLEEP instruction is fetched, it will be recognized in the following cycle (which is the execution cycle of the SLEEP instruction) preventing the processor from going into SLEEP. The SLEEP instruction will effectively execute as a single cycle NOP. The $\overline{PD}$ bit will not be cleared.

3.5.3 MINIMIZING CURRENT CONSUMPTION IN SLEEP MODE

The SLEEP mode is designed to reduce power consumption. To minimize current drawn during SLEEP mode, the user should turn-off output drivers that are sourcing or sinking current, if it is practical. Weak pull-ups on port-pins should be turned off, if possible. All inputs should be either at V_{SS} or at V_{DD} (or as close to rail as possible). An intermediate voltage on an input pin causes the input buffer to draw a significant amount of current.

FIGURE 3.5.1 - CPUSTA REGISTER

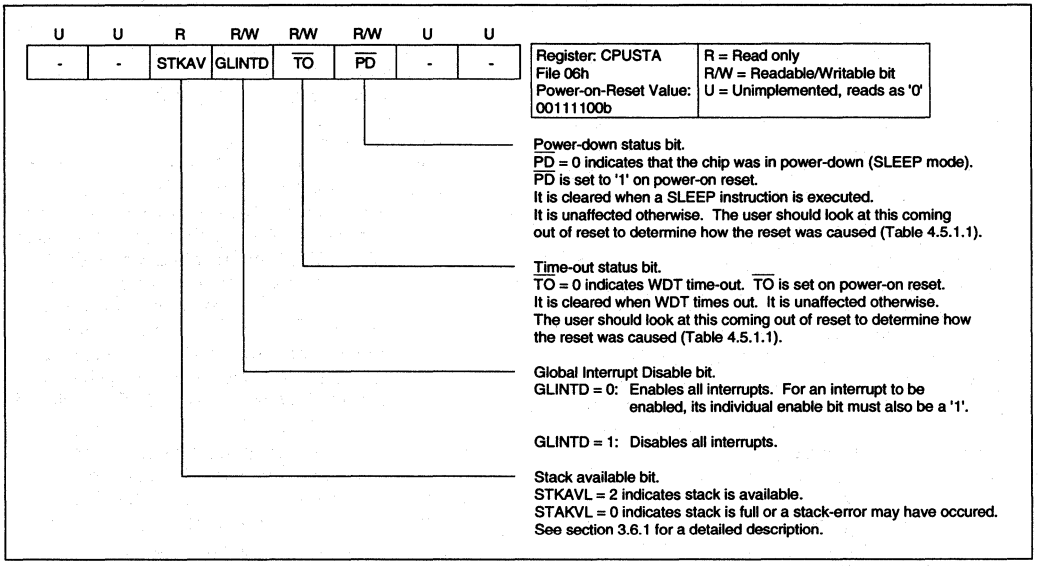


TABLE 3.5.1.1 - WAKE - UP AND RESET FUNCTION TABLE

Event	Chip Status before event	Chip function after event					Notes
		PC	Oscillator Circuit	OST	$\overline{TO}$	$\overline{PD}$	
Power on reset	Don't care	0000	on	yes	1	1	
$\overline{MCLR}$ reset	Normal operation	0000	on	no	u	u	
SLEEP instruction	Normal operation	N+1	off	no	1	0	
$\overline{MCLR}$ wake-up	SLEEP	0000	on	yes(2)	u	u	
WDT time-out	Normal operation	0000	on	no	0	u	
WDT wake-up	SLEEP	0000	on	yes(2)	0	u	
Interrupt	Normal operation	Vector	on	no	u	u	
Interrupt wake-up	SLEEP,GLINTD=0	1. N+1 2.Vector	on	yes(2)	u	u	1
Interrupt wake-up	SLEEP,GLINTD=1	1. N+1 2. N+2	on	yes(2)	u	u	1

Legend

- PC Program Counter contents after the event
- $\overline{TO}$ Time Out status bit after the event
- $\overline{PD}$ Power Down status bit after the event
- N Address of SLEEP instruction
- U No change takes place

Notes

Note 1: The instruction at "N+1" executed, after wake up. Step 2 depends on the status of the GLINTD bit at the time of the event. If GLINTD was "0", the program will vector to the interrupt routine.

Note 2: OST timer is activated only in XT and LP oscillator modes. (Sec. 4.4)

3.6 Watchdog Timer

The PIC17C42 has an on-chip Watchdog Timer whose function is to recover from software malfunction. The Watchdog Timer is an 8-bit asynchronous ripple counter with an 8-bit prescaler (also an asynchronous ripple counter). The watchdog timer always runs off its own internal RC oscillator. The Watchdog Timer is not readable or writable. It is not mapped in data or program memory space. Two EPROM fuses provide four operating options for the Watchdog Timer:

FWDT1, FWDT0	WDT Clock Input Source	WDT Function Input Clock	WDT Period
1 0	RC osc	WDT runs with prescale = 256	3 sec
0 1	RC osc	WDT runs with prescale = 64	0.8 sec
1 1	RC osc	WDT runs with prescale = 1	12 ms
0 0	OSC/4	WDT runs as a regular timer with prescale = 256	65536 Tcy

Note: 0 implies a programmed fuse.

Fuses FWDT1 abd FWDT0 are mapped in program memory locations FE03h and FE02h respectively. See Section 4.8 for details on how to program fuses.

The Watchdog Timer and its prescaler are reset and the timeout bit, $\overline{TO}$ (bit3, CPUSTA) set to '1' if:

a. A CLRWDT instruction is executed.
b. A SLEEP instruction is executed.
c. A power on reset occurs.

Under normal circumstances, the user program is expected to clear the Watchdog Timer on a regular interval. If the program fails to do so, the WDT will overflow and reset the chip. The Watchdog Timer and its prescaler are physically the same as the Power-up Timer (PWRT). They simply perform different roles in and outside reset condition.

3.6.1 WDT AS A REGULAR TIMER

Setting fuses FWDT1 and FWDT0 as 0's will configure the WDT as a simple timer. In this mode the timer increments on internal OSC/4 clock with a prescale of 256 (i.e. increments at OSC freq/1024 rate). On overflow $\overline{TO}$ bit is cleared, but the chip is not reset. In this mode the WDT is stopped during SLEEP. The $\overline{TO}$ bit is set when a CLRWDT instruction is executed.

3.7 Code Protection and Write Protection

The code in the user EPROM may be protected from piracy by selecting "code protected Microcontroller mode." This is done by blowing fuses FPMM1 and FPMM0 to "0". A TABLRD instruction, executed from the test EPROM attempting to read user EPROM will read encrypted data. However, if the instruction is executed from an address less than 2K (i.e. from user EPROM), it will read un-encrypted data.

Further, any TABLWT instruction executed from the test EPROM and attempting to write to the user EPROM, will not result in programming of the destination. However, the instruction will still need to be terminated by an interrupt condition and the table latches will still be written. A TABLWT instruction, executed from an address less than 2K can program any user EPROM location regardless of code protection.

The above measures essentially prevent read, verify or programming of any user EPROM location from outside.

3.8 Configuration fuses

Configuration fuses are EPROM bits that can be programmed (reads '0') or left unprogrammed (reads '1') to select between options (e.g. operating modes). For simplicity of programming they are mapped into program memory. This also makes it possible to read the fuse values (only in microcontroller modes). Each fuse is assigned one program memory location. In erased condition a fuse will read as a '1'. To program (or "blow") a fuse, the user needs to write to the fuse address using a TABLWT instruction. Regardless of the data, a TABLWT to a fuse location will bow the fuse. The fuses and their addresses are shown in Table 4.8.1.

Reading configuration fuses: Reading any fuse location in the address range FE00:FE07h will read all eight fuse values in the lower byte and all 1's in the upper byte. Fuse located at FE00h will show up in bit 0 and so on. The fuse locations are accessible only in microcontroller and secure microcontroller modes. In microprocessor and extended microcontroller modes, this section of the program memory is mapped external (see Figure 1.5.2) making the fuse locations inaccessible.

TABLE 3.8.1 - CONFIGURATION FUSES

Fuse	Address	Function
FOSC0	FE00h	FOSC1, FOSC0 :
FOSC1	FE01h	00 : LF oscillator mode 01 : RC oscillator mode 10 : XT oscillator mode 11 : EC (external clock mode)
FWDT0	FE02h	FWDT1, FWDT0 :
FWDT1	FE03h	10 : WDT prescale is 256 01 : WDT prescale is 64 11 : WDT prescale is 1 00 : WDT is a normal timer
FPMM0	FE04h	FPMM1, FPMM0 :
FPMM1	FE06h	00 : Microcontroller mode (code protected) 10 : Microcontroller mode 01 : Extended microcontroller mode 11 : Microprocessor mode

FIGURE 3.8.1 - READING FUSE LOCATION

Address FE00:FE07h

1	1	1	1	1	1	1	1
bit15							bit8

0	FPMM1	0	FPMM0	FWDT1	FWDT0	FOSC1	FOSC0
bit7							bit0

4.0 OVERVIEW OF PERIPHERALS

An array of sophisticated, high-speed peripherals are incorporated on chip to meet the demands of real-time applications. All peripherals are highly intelligent and have their own interrupts and error handling to free up the CPU as much as possible. There are three 16-bit timer/counters one of which can be split into two 8-bit timers creating up to four timer/counter resources. Two high-speed captures are provided for efficient interface to shaft encoders and other high-speed pulse train sources. Two high-speed pulse-width-modulation (PWM) outputs with up to 10-bit resolution make it possible to control a motor through power drivers. There are two external and several internal interrupt sources. The capture pins can be used as interrupt pins making it possible to have up to four external interrupts. Finally, there are 33 I/O pins most of which can be configured as inputs or outputs in software. A number of the I/O pins are multiplexed with peripheral functions or the system bus. In microcontroller mode 23 I/O pin are un-multiplexed.

4.1 The Bank Select Register (BSR)

All the peripheral registers are mapped into the data memory space. In order to accommodate the large number of registers in the 256 byte data memory space without taking away from the general purpose data RAM, a banking scheme has been used. A segment of the data memory, from address 10h to address 17h, is banked. A bank select register (BSR, address 0Fh) selects the currently active "peripheral bank". Effort has been made to group the peripheral registers of related functionality in one bank. However, it will still be necessary to switch from bank to bank in order to address all peripherals related to a single task. To alleviate this problem, a single cycle instruction, MOVLB (move literal value to BSR) is incorporated in the instruction set. In the PIC17C42 only the low four bits of the BSR are physically implemented, making it possible to address up to sixteen banks. Only four banks are actually used (see data memory map in Figure 1.6.1).

5.0 DIGITAL I/O PORTS

The PIC17C42 has five ports A, B, C, D and E. Together these add up to 33 port pins. Most port pins have an associated data direction bit which configures it as input (DDR bit='1') or output (DDR bit='0'). When a port pin is read as an input, the value on the pin (and not the data latch) is read.

Most port pins are multiplexed with the system bus or peripheral functions. These pins are configured as port pins or peripheral inputs/outputs by control bits in corresponding peripheral registers. Once a port pin is selected for an alternate function, its direction will be determined by the peripheral logic which will force the DDR bit to the required state.

Ports A, B, C, D and E and their associated DDR registers are mapped into the data-memory. Ports C, D and E multiplex with the system bus (AD <15:0>, ALE, WR and OE).

Reading the PORT register, reads the values of the PORT pins. Writing to the PORT register writes the value to the PORT latch. When using read modify write instructions (ex. BCF, BSF, etc.) on a PORT, the value of the PORT pins is read, the desired operation is done to this value, and this value is then written to the PORT latch.

Example 5-1 shows the effect of two sequential read modify write instructions (ex. BCF, BSF, etc.) on an I/O PORT.

EXAMPLE 5-1: READ MODIFY WRITE INSTRUCTIONS ON AN I/O PORT

```
; Initial PORT settings:  PORTB<7:4> Inputs
;                         PORTB<3:0> Outputs
; PORTB<7:6> have external pull-up and are not
; connected to other circuitry.
;
;                           PORT latch    PORT pins
;                           ----------    ---------
--
      BCF     PORTB, 7    ; 01pp pppp     11pp pppp
      BCF     PORTB, 6    ; 10pp pppp     11pp pppp
      BSF     STATUS, RP0 ;
      BCF     TRISB, 7    ; 10pp pppp     11pp pppp
      BCF     TRISB, 6    ; 10pp pppp     10pp pppp
;
; Note that the user may have expected the pin
```

TABLE 5.1.1 - PORT A FUNCTIONS

Port Pin	Bit	Pin function	Alternate function
RA0/INT	bit 0	Input only (Schmitt Trigger) port pin	INT external interrupt input
RA1/T0CKI	bit 1	Input only (Schmitt Trigger) port pin	T0CKI external interrupt input. It is also the external clock input for the TMR0 timer/counter.
RA2, RA3	bit 2,3	Input/output pins with Schmitt Trigger input and open-drain output. To use either of these two pins as an input, the user must write a '1' to the port data latch. If used as an output, external pull-up resistor must be provided. These pins can be pulled up to voltages higher than Vcc. Also, these two port pins provide higher current sink capability (See DC specs for details).	None
RA4/RX/DT	bit 4	Input only (Schmitt Trigger) port pin	If the SPEN bit (bit 7, RCSTA) is a '1' then this pin is configured by the serial port. In SYNC mode: It is data input or output (DT). In ASYNC mode: It is receive data input (RX).
RA5/TX/CK	bit 5	Input only (Schmitt Trigger) port pin	If the SPEN (bit 7, RCSTA) bit is a '1' then this pin is controlled by the serial port. In SYNC mode: It is either clock input (slave mode) or the clock output (master mode) in ASYNC mode: It is the transmit data output (TX).
	bit 6	This bit is unimplemented and reads as '0'	
	bit 7	No pin associated	This is a control bit ($\overline{PUEB}$) for Port B. No port pin is associated with this bit. $\overline{PUEB}$=0 enables weak pull-ups on Port B.

5.1.1 USING RA2, RA3 PINS AS OUTPUT

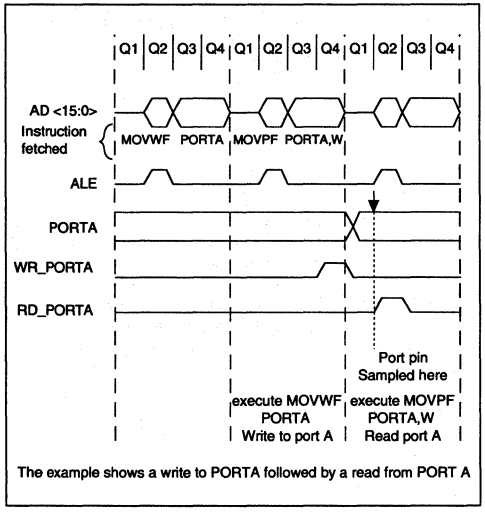
PORTA does not have an associated data direction register. When using them as outputs, read-modify-write instructions (such as BCF, BSF, BTF) are not recommended on PORTA, since a read will read the port pins but a write will write to the port data latch. Such an operation may inadvertantly cause RA2, RA3 to switch from output to input or vice-versa.

```
; values to be 00pp pppp. The 2nd BCF caused RB7
; to be latched as the pin value (High).
```

5.1 PORTA

File 10h in Bank 0 is PORTA, a 6-bit port. There is no Data Direction Register associated with this port. PORTA is multiplexed with peripheral functions as described in Table 5.1.1. See Figure 5.1.1 for block diagram of PORTA and 5.0.1 for read/write timing.

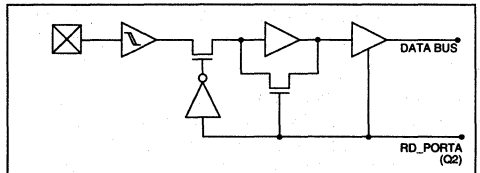
FIGURE 5.0.1 - I/O PORT READ AND WRITE TIMING



The example shows a write to PORTA followed by a read from PORT A

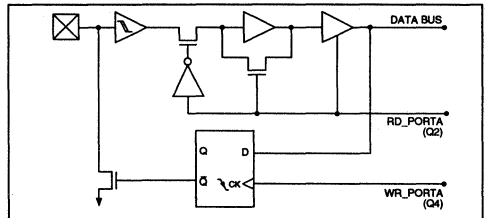
FIGURE 5.1.1 - PORT A BLOCK DIAGRAMS

FIGURE 5.1.1A - RA0 AND RA1



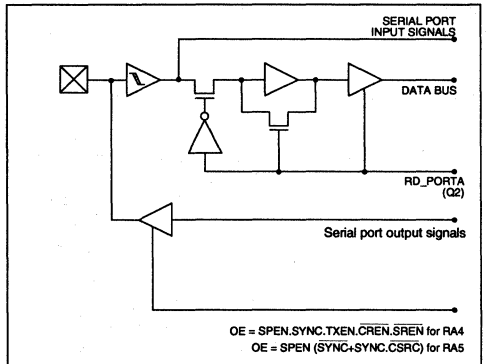
NOTE: I/O pins have protection diodes to VDD and Vss.

FIGURE 5.1.1B - RA2 AND RA3



NOTE: I/O pins have protection diodes to Vss.

FIGURE 5.1.1C - RA4 AND RA5



NOTE: I/O pins have protection diodes to VDD and Vss.

5.1.2 SUMMARY OF PORT A REGISTERS

Register Name	Function	Address	Reset Value
PORTA	Port A pins when read, Port A latch when written (RA2/RA3 only)	Bank 0, File10h	00XXXXXb
RTCSTA	RTCC status/control register (configures RA0/INT & RA1/T0CKI pins)	File 05h	0000000b
RCSTA	Serial port receive status/control register (configures RA4/RX/DT and RA5/TX/CK pins)	Bank0, File 13h	000000Xb

5.2 PORTB

PORTB is an 8-bit wide bidirectional port. It is mapped in Bank0, File 12h. Writing to this address writes to the port latch while reading it will read the port pins. An 8-bit data direction register (DDRB, Bank 0, File 11h) configures each port pin as an input or output. A '0' in the 'DDR' register configures the port as an output. Each port pin also has a software configurable weak pull-up (~100 µA typical). A control bit $\overline{\text{PUEB}}$ (bit 7, Bank 0, File 10h, Register PORTA) can enable ($\overline{\text{PUEB}}$ = '0') or disable ($\overline{\text{PUEB}}$ = '1') the pull-ups. The weak pull-up is turned off for any pin configured as output.

Most of the pins of PORTB are multiplexed with peripheral functions. Table 5.2.1 describes their alternate functions. When a pin is redefined to be a port pin from a peripheral pin, its data direction bit may be left in an unknown state. The user will need to re-initialize the DDR bit properly. See Figures 5.2.1 and 5.2.2 for block diagrams of PORTB and Figure 5.0.1 for read/write timing.

PORTB also has an "interrupt on change" feature. When configured as input, its output data latch can be used as a compare latch. An active high output is generated on mismatch between the pin and the latch. The "mismatch" outputs of all the input pins are OR-ed together to generate the IRB interrupt. All the output pins are excluded from the comparison. Thus, an interrupt is generated when the port input changes. This interrupt can wake the chip up from SLEEP mode.

The interrupt is latched in the IRB bit (bit-7, Register PIR, Bank1, File 16h). IRB is readable and writable by the CPU. The user, in the interrupt service routine, can clear the interrupt in one of two ways:

a) Disable the interrupt by clearing the corresponding interrupt enable bit, IEB.

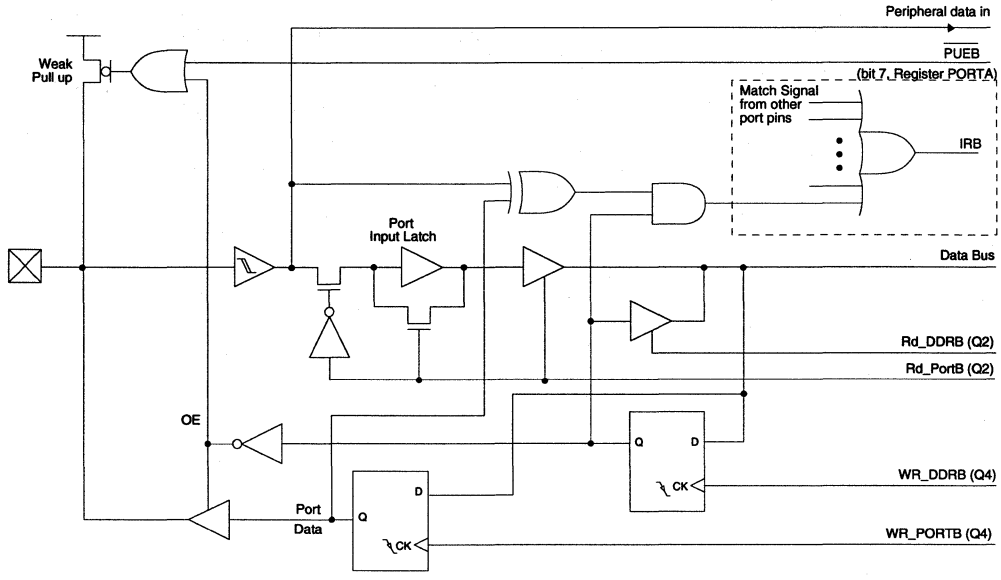
b) Read PORTB and write back the pin value to the data latch. This will end mismatch condition and therefore the mismatch output. Next, the user must clear bit IRB.

2

TABLE 5.2.1 - PORTB FUNCTIONS

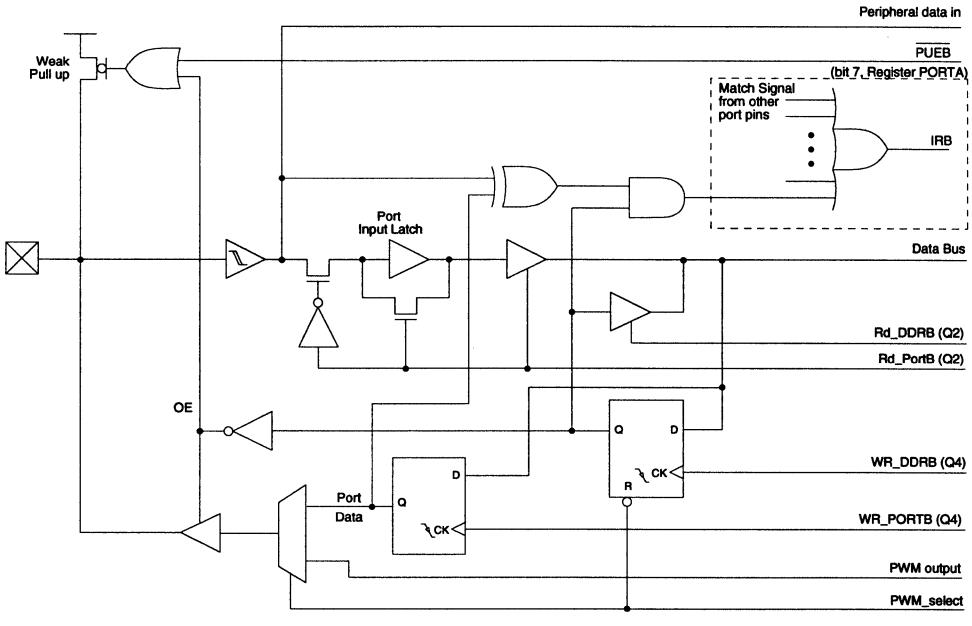
Port Pin	Bit	Pin Function	Alternate Function
RB0/CAP1	bit 0	Input/Output port pin with Schmitt Trigger input	CAP1: Capture1 input
RB1/CAP2	bit 1	Input/Output port pin with Schmitt Trigger input	CAP2: Capture2 input
RB2/PWM1	bit 2	Input/Output port pin with Schmitt Trigger input	PWM1 output. This pin is configured as the PWM1 output if the control bit PWM1ON (bit 4, Register TCON2, Bank 3, File 17h) is set to '1'.
RB3/PWM2	bit 3	Input/Output port pin with Schmitt Trigger input	PWM2 output. This pin is configured as the PWM2 output if the control bit PWM2ON (bit 5, Register TCON2, Bank 3, File 17h) is '1'
RB4/TCLK12	bit 4	Input/Output port pin with Schmitt Trigger input	TCLK12: external clock input for timer1 and timer2
RB5/TCLK3	bit 5	Input/Output port pin with Schmitt Trigger input	TCLK3: external clock input for timer3
RB6	bit 6	Input/Output port pin with Schmitt Trigger input	
RB7	bit 7	Input/Output port pin with Schmitt Trigger input	

FIGURE 5.2.1 - BLOCK DIAGRAM OF PORT PINS RB0, RB1, RB4 - RB7



NOTE: I/O pins have protection diodes to VDD and Vss.

FIGURE 5.2.2 - BLOCK DIAGRAM OF PORT PINS RB<3:2>



NOTE: I/O pins have protection diodes to VDD and Vss.

2

5.2.1 SUMMARY OF PORTB REGISTERS

Register Name	Function	Address	Reset Value
PORTB	PORTB pins when read PORTB latch when written	Bank 0, File 12h	XXXXXXXXb
DDRB	PORTB data direction register	Bank 0, File 11h	11111111b
PORTA (bit $\overline{PUEB}$)	PORTA data/ $\overline{PUEB}$ bit	Bank 0, File 10h	00XXXXXXb
PIR (bit IRB)	Peripheral interrupt register	Bank 1, File 16h	00000010b
PIE (bit IEB)	Peripheral interrupt enable register	Bank 1, File 17h	00000000b
INTSTA (bit PEIE)	Interrupt status register	File 07h	00000000b
CPUSTA (bit GLINTD)	CPU status register	File 06h	0011XX00b
TCON2	Timer/PWM/capture control registers	Bank 3, File 17h	00000000b

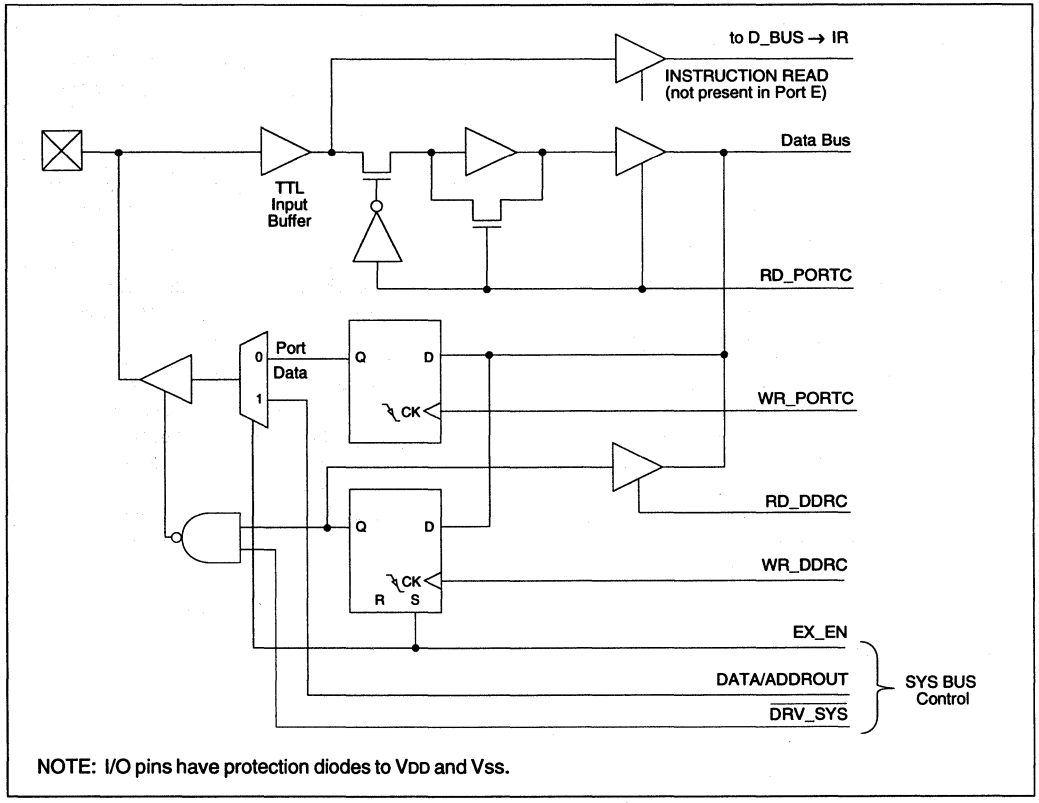
5.3 PORTC

PORTC is an 8-bit wide bidirection port mapped in File 11h, Bank 1. The corresponding data direction register DDRC (file 10h, Bank 1) can configure each pin as an input (if DDRC bit is '1') or output (if DDRC bit is '0'). This port is multiplexed with AD<7:0>, the lower byte of the Address/Data bus. Bit 0 of PORTC is AD<0>. See Figure 5.3.1 for block diagram of PORTC and Figure 5.0.1 for read/write timing.

5.3.1 SUMMARY OF PORT C REGISTERS

Register Name	Function	Address	Reset Value
PORTC	PORTC pins when read PORTC latch when written	Bank 1, File 11h	XXXXXXXXb
DDRC	PORTC data direction register	Bank 1, File 10h	11111111b
INTSTA (bit PEIE)	Interrupt status register	File 07h	00000000b
CPUSTA (bit GLINTD)	CPU status register	File 06h	0011XX00b

FIGURE 5.3.1 - BLOCK DIAGRAM OF PORTS C, D AND E



NOTE: I/O pins have protection diodes to VDD and Vss.

5.4 PORTD

PORTD is an 8-bit wide bidirection port mapped in File 13h, Bank 1. The corresponding data direction register DDRD (file 12h, Bank 1) can configure each pin as an input (if DDRD bit is '1') or output (if DDRD bit is '0'). This port is multiplexed with AD<15.8>, the higher byte of the Address/Data bus. Bit 0 of PORTD is AD<8>. See Figure 5.3.1 for block diagram of PORTC and Figure 5.0.1 for read/write timing.

5.5 PORTE

PORTE is a 3-bit wide bidirectional port mapped in data memory (file 15h, Bank1). The corresponding Data Direction Register, DDRE, is mapped at file 14h, Bank 1. Each port pin can be configured as an input (DDRE bit = '1') or an output (DDRE bit = '0'). Only the three lowest significant bits are physically implemented in 17C42. The unimplemented bits read as '0'. See Figure 5.3.1 for block diagram of PORTE and Figure 5.0.1 for read/write timing. PORTE is multiplexed with control outputs ALE, $\overline{WR}$ and $\overline{OE}$ in external execution mode.

5.4.1 - SUMMARY OF PORTD REGISTERS

Register Name	Function	Address	Reset Value
PORTD	PORTtD pins when read PORTD latch when written	Bank 1, File 13h	xxxxxxxxb
DDRD	PORTD data direction register	Bank 1, File 12h	11111111b

5.5.1 SUMMARY OF PORT E REGISTERS

Register Name	Function	Address	Reset Value
PORT E	PORTE pins when read PORTE latch when written	Bank 1, File15h	00000XXXb
DDRE	PORTE data direction register	Bank 1, File14h	00000111b

TABLE 5.5.1 - PORTE FUNCTIONS

Port Pin	Bit	Pin Function	System Bus Function (External execution)
RE0/ALE	bit 0	Input/output port. TTL input buffer.	ALE output
RE1/$\overline{OE}$	bit 1	Input/output port. TTL input buffer.	$\overline{OE}$ output
RE2/$\overline{WR}$	bit 2	Input/output port. TTL input buffer.	$\overline{WR}$ output

6.0 UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART)

The serial port can operate either a full-duplex asynchronous mode or in a half-duplex clocked synchronous mode. Synchronous mode uses a bi-directional data pin and a bi-directional clock pin. In synchronous mode, the clock can be either internal (master mode) or external (slave mode). In asynchronous mode, the clock is always derived internally. A dedicated 8-bit Baud Rate Generator (BRG) is used for internal clock generation. In both modes, receiver and transmitter are double buffered, eight or nine data bits are supported and separate transmit and receive interrupts are available.

6.1 Asynchronous Mode

The asynchronous mode is selected by clearing the SYNC bit in the TXSTA register. Furthermore, SPEN bit (Serial Port Enable, bit 7, Register RCSTA, Bank 0) has to be set to enable RA4 and RA5 as serial port pins. SPEN=0 will configure these pins as port pins. In asynchronous mode the RX pin receives data and the TX pin transmits data in a full duplex mode. Data is transmitted and received least significant bit first. Both receive and transmit operate on the same internally generated clock which is derived from the Baud Rate Generator (Register SPBRG, Bank 0, File 17h). Data on the RX pin is sampled on the seventh, eighth and ninth pulses of a 16X (16 times the baud clock) internal clock. A majority of these three bits decide whether a one or a zero was received. In addition to the eight or nine data bits, one start bit and one stop bit are sent. Parity is not supported directly in hardware, but can easily be implemented in software. Asynchronous mode operation is stopped during SLEEP.

6.1.1 ASYNCHRONOUS MODE TRANSMISSION

Once asynchronous mode is selected (SYNC=0, bit 4 Register TXSTA) and serial port outputs are enabled (SPEN=1, bit 7, Register RCSTA) transmission can be enabled by setting TXEN bit (bit 5,TXSTA register). Actual transmission will begin when a word is written to the transmit buffer register (TXREG, bank0, file 16h) and the Baud Rate Generator produces a shift clock (figure 7.1.1.1). A start bit is sent out first (logic '0'), followed by eight or nine data bits and a stop bit (logic '1'). Transmitted data appears on RA5/TX/CK pin. Transmission can also be started by first writing a word to the TXREG and then setting TXEN.

The transmit register (TXREG) is double buffered. As the user writes to TXREG, the data is transferred from the buffer to the transmit shift register (TSR), thus freeing up the buffer register. An interrupt is pending as long as TXREG is empty. Indicating that the transmit buffer register (TXREG) is free to accept another word. This interrupt request is bit 1 (TBMT) of PIR (peripheral interrupt request register; Bank 1, file 16h) register. This interrupt can be enabled or disabled by bit 1 (TXIE) of PIE (peripheral interrupt enable; Bank 1, file 17h) register. TXIE=1 enables the interrupt. Regardless of TXIE, the TBMT bit will always show the status of the TXREG buffer (can not be affected in software) and can be used as a status bit. The interrupt request bit (TBMT) is read only. Therefore, to avoid unwanted interrupts (say, at the end of a transmission) the user will need to mask off this interrupt.

In addition to TXIE bit, two other bits will affect the transmit interrupt. They are: PEIE (bit3, INTSTA register, file 07h) that enables (if='1') or disables (if='0') all peripheral interrupts, and GLINTD (Global Interrupt Disable, bit 4, CPUSTA register, file 06h) bit that disables all interrupts if set.

While TBMT (Transmit Buffer Empty) indicates the status of the transmit buffer register, another bit TRMT (bit1, register TXSTA) indicates the status of the transmit shift register. It is a read only bit. TRMT=1 implies transmit shift register is empty. The user can determine exactly when transmission is completed by polling this bit. TRMT is set after stop bit is sent out.

CREN or SREN bits do not affect asynchronous transmission. Clearing TXEN during transmission aborts transmission, reverts TX pin to hi-impedance and resets the transmitter.

FIGURE 6.1.1.1 - ASYNCHRONOUS TRANSMISSION

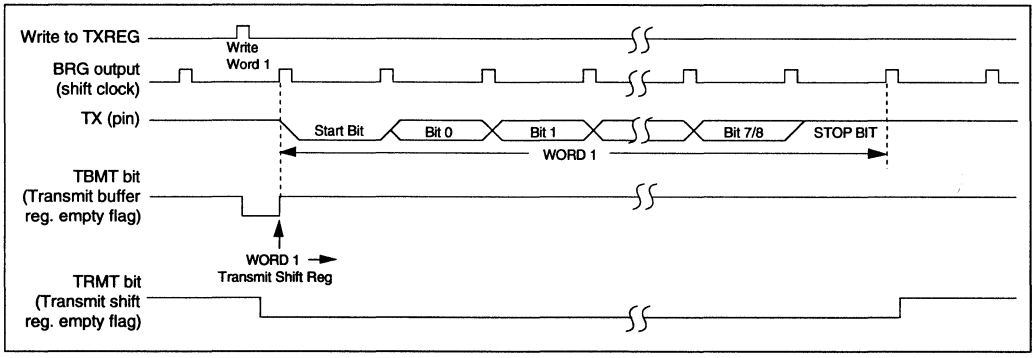
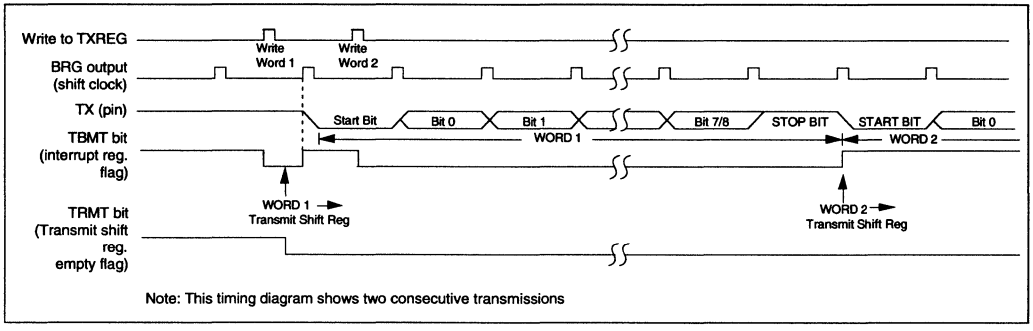


FIGURE 6.1.1.2 - ASYNCHRONOUS TRANSMISSION (BACK TO BACK)



Note: This timing diagram shows two consecutive transmissions

If 9-bit transmission is selected (TX8/9=1, bit 6, register TXSTA) the 9th bit should be written to TXD8 (bit0, TXSTA). This bit is double buffered as well. The 9th bit must be written before writing the data word to TXREG, since the latter triggers the transfer of the entire word to the transmit shift register.

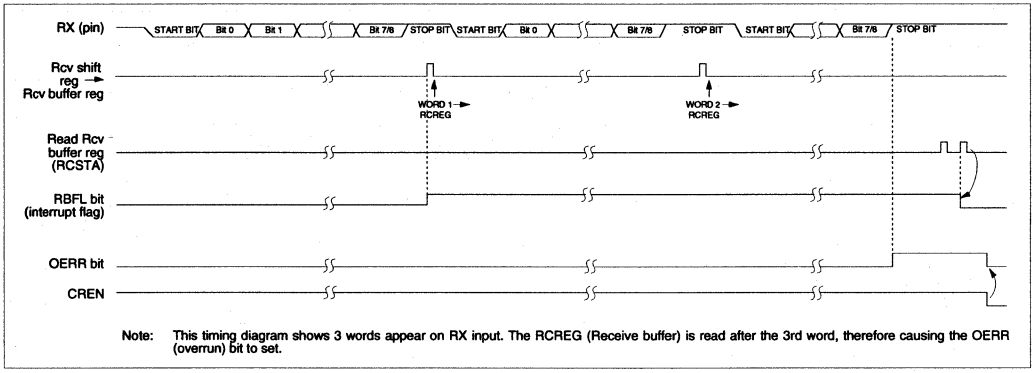
6.1.2 ASYNCHRONOUS MODE RECEPTION

Data is received on RA4/RX/DT pin. Reception is enabled by setting the CREN bit (bit4, register RCSTA). The SREN bit (bit5, RCSTA) has no function in asynchronous mode. Reception begins when a start-bit is detected on RX pin. The Baud Rate Generator internally generates a 16x clock. Every incoming bit is sampled on the seventh, eighth and the ninth time slot and a majority detection is done to determine the value of the bit. After sampling the stop bit (i.e. halfway through stop bit), the received data is transferred to the receive buffer register (RCREG) if the buffer register is empty. The RCREG is actually a two word deep FIFO. Therefore, it is possible to receive two words, transfer them to RCREG and begin receiving the 3rd word in the receive shift register (RSR). If at the time of reception of the last bit of the third word, the RCREG has still not been read (and therefore is holding two words) then the receiver control logic will set the overrun error bit, OERR (bit1, register RCREG). In case of overrun, the word in the shift register is lost (i.e. it can not be read). The RCREG can be read twice to retrieve the first two words. The user will need to clear OERR by resetting the receiver (by clearing CREN). Clearing OERR is essential since once the overflow flag is set, the receiver simply stops transferring RSR to RCREG.

The framing error bit, FERR (bit 2, Register RCSTA) and the ninth receive bit, RCD8 (bit 0, RCSTA) are buffered the same way as the receive data. Reading RCREG will load the RCD8 and FERR bits with new values. The user, therefore, must read the RCSTA register before reading the received data (RCREG) in order to obtain FERR and ninth data bit information. If the RCREG is read first, then the status register RCSTA will be loaded with new status information and the old information will be lost. The framing error bit, FERR, is set if the stop bit is detected to be a '0'.

A receive interrupt flag RBFL, is set (bit0, register PIR) when the receive shift register content is shifted to the receive buffer register. This interrupt can be enabled or disabled via the RCIE (Receive interrupt enable) bit (bit0, register PIE). RCIE=1 will enable the interrupt. The RBFL (receive buffer full interrupt flag) bit is a read only bit and is cleared when the receive buffer is read. However, if the receive shift register is full, it will transfer its contents to the receive buffer register and the RBFL

FIGURE 6.1.2.1 - ASYNCHRONOUS RECEPTION



Note: This timing diagram shows 3 words appear on RX input. The RCREG (Receive buffer) is read after the 3rd word, therefore causing the OERR (overrun) bit to set.

bit will be set again. To enable receive interrupt, the Peripheral Interrupt Enable bit, PEIE (bit3, INTSTA register). must be set and the Global Interrupt Disable bit, GLINTD (bit4, CPUSTA register), must be cleared.

6.2 Synchronous Mode

The synchronous mode is selected by setting the SYNC bit (bit4, TXSTA register). In addition, the SPEN bit (bit7, RCSTA register) must be set to configure the RA5/TX/CK and RA4/RX/DT pins as CK (synchronous clock) and DT (sync data) pins respectively. Synchronous mode is half duplex with the DT pin as data input during reception and data output during transmission. The CK pin is clock output if internal clock option (master mode) is selected by setting the CSRC (bit7, TXSTA register) bit. If CSRC='0' then the CK pin is clock input (synchronous slave mode).

As in asynchronous mode, eight or nine data bits are transmitted or received. No start or stop bits are sent or received.

6.2.1 SYNCHRONOUS MODE TRANSMISSION

Once the sync mode is selected (SYNC='1') and the serial port is enabled (SPEN='1', register RCSTA), transmission is enabled by setting the TXEN (transmit enable, bit5, TXSTA register) bit. This will configure the TX pin as an output. Actual transmission will begin when a word is written to the transmit buffer register (TXREG). The transmitter is double buffered. If the transmit shift register (TSR) is empty then the word will be transferred from TXREG to TSR. The first data bit will be shifted out at the next available rising edge of the clock. Data out is stable around the falling edge of the sync clock. Transmission can also be started by first writing a data word to TXREG and then setting TXEN='1'. This method may be advantageous when slow baud rates are selected, since the Baud Rate Generator is kept under reset when TXEN=CREN=SREN=0. Setting the TXEN bit will start the BRG, creating a shift clock immediately.

The TBMT interrupt (bit1, PIR register) is pending whenever the transmit buffer is empty and ready to accept another word. The interrupt has a corresponding mask bit (TXIE, bit1, Register PIE). TXIE='1' enables the transmit interrupt while TXIE='0' disables it. Regardless of TXIE, TBMT will always show the status of the TXREG (not affected by software) and can be used as a status bit. To enable the transmit interrupt, Peripheral Interrupt Enable, PEIE (bit3, INTSTA register, file 07h) bit must be set and Global Interrupt Disable, GLINTD (bit4, CPUSTA register, file 06h) bit must be cleared.

While TBMT (Transmit Buffer Empty) indicates the status of the transmit buffer register, another bit TRMT (bit1, register TXSTA), indicates the status of the transmit shift register. It is a read only status bit. TRMT=1 implies that the transmit shift register is empty. The user can determine exactly when transmission is over by polling this bit. TRMT is set after the last bit is sent out.

If 9-bit transmission is selected, the ninth bit should be written to bit TXD8 (bit0, TXSTA). This bit is also double buffered. The ninth bit must be written prior to writing the data word to TXREG, since a write to the TXREG triggers the transfer of the entire word to the transmit shift register.

In sync master mode, the CK pin will output clocks only during actual transmission (see Figure 7.2.1.1). In sync slave mode clock input may be present on the pin at all times.

If TXEN is cleared during transmission of a word, transmission will be aborted and the DT and CK pins will revert to hi-impedance. If either the CREN or the SREN bit is set, transmission is also aborted and the DT pin will go into hi-impedance state (for reception). The CK pin will remain an output if CSRC=1 (internal clock). The transmitter logic, although disconnected from the pins, is not reset. The user must clear the TXEN bit to reset the transmitter. This is particularly important if the SREN was set to interrupt an ongoing transmission. In this case, after reception of a single word, the SREN bit will reset and the serial port will revert back to transmit mode (since TXEN is still set). This means the DT pin will turn around and start driving. To avoid this, TXEN should be cleared.

FIGURE 6.2.1.1 - SYNCHRONOUS TRANSMISSION

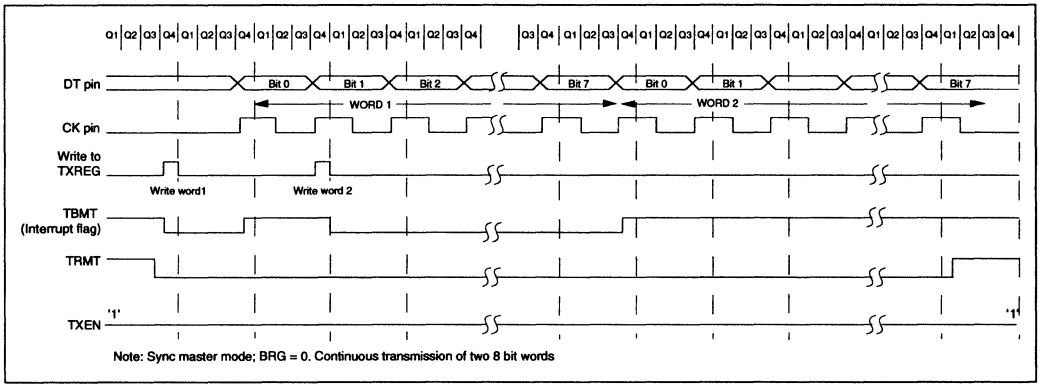


FIGURE 6.2.1.2 - SYNCHRONOUS TRANSMISSION (THROUGH TXEN)

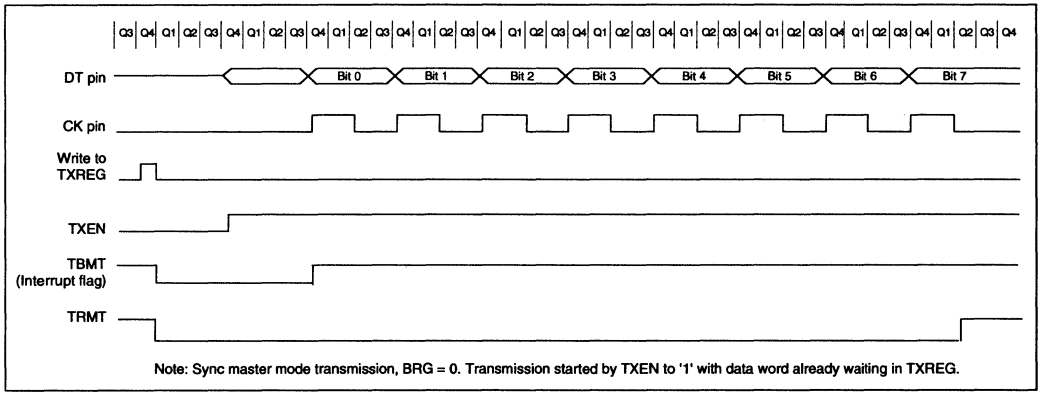
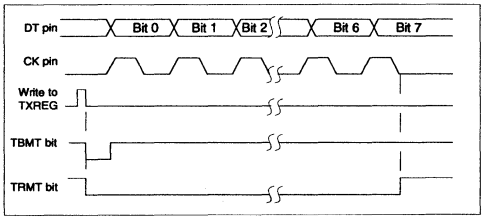


FIGURE 6.2.1.3 - SYNCHRONOUS TRANSMISSION (SLAVE)



6.2.2 SYNCHRONOUS MODE RECEPTION

Data is sampled on the DT pin on the falling edge of the clock. Reception is enabled by either setting the SREN bit (Single Receive Enable, bit5, RCSTA register) or the CREN bit (Continuous Receive Enable, bit4, RCSTA register). If SREN is set, one word is received after which SREN is reset in hardware. If the CREN bit is set, words are received continuously (and read off by the CPU presumably) until CREN is reset by software. If both CREN and SREN are set, then CREN will take precedence.

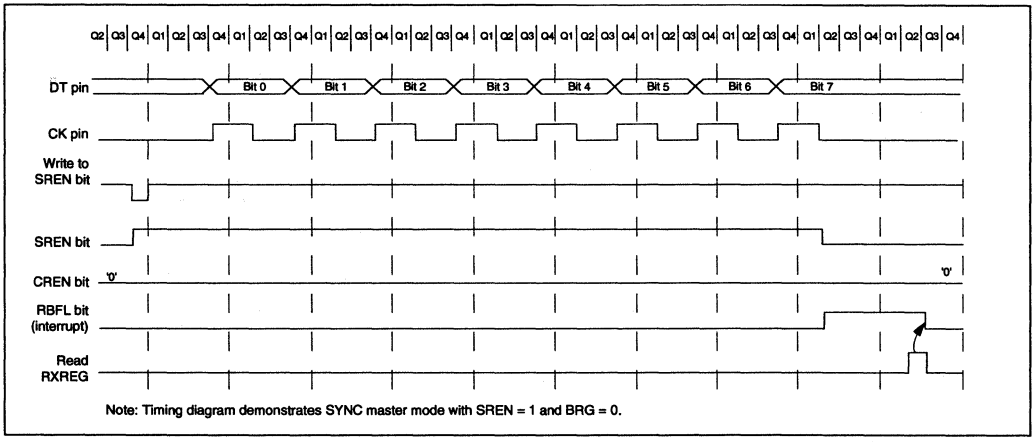
After a word is received completely, it is transferred from the receive shift register (RSR) to the receive buffer register (RCREG) thus freeing up the RSR to receive the next word. With CREN=1, it is possible to receive consecutive data words without any discontinuity in between. This makes it possible to receive data words of larger size, e.g. 16-bit. In synchronous slave mode the SREN bit is a don't care.

The RCREG is actually a two-word deep FIFO. Therefore, it is possible to receive two words, transfer them to RCREG and begin receiving the third word in the receive shift register (RSR). If, at the time of reception of the last bit of the third word, the RCREG has still not been read (and therefore is holding two words) then the receiver control logic will set the overrun error bit, OERR (bit1, register RCSTA). In case of an overrun, the word in the shift register is lost (i.e. it can not be read). The RCREG can be read twice to retrieve the first two words. The user will need to clear OERR by resetting the receiver (by clearing CREN). Clearing OERR is essential since once overflow flag is set the receiver simply stops transferring RSR to RCREG.

An interrupt is issued when RSR transfers a data word to receive buffer register, RCREG, indicating that RCREG is full. The interrupt flag (RBFL, bit0, register PIR) can be masked by interrupt mask bit RCIE (Receive interrupt enable, bit0, register PIE). RCIE=1 enables the receive interrupt.

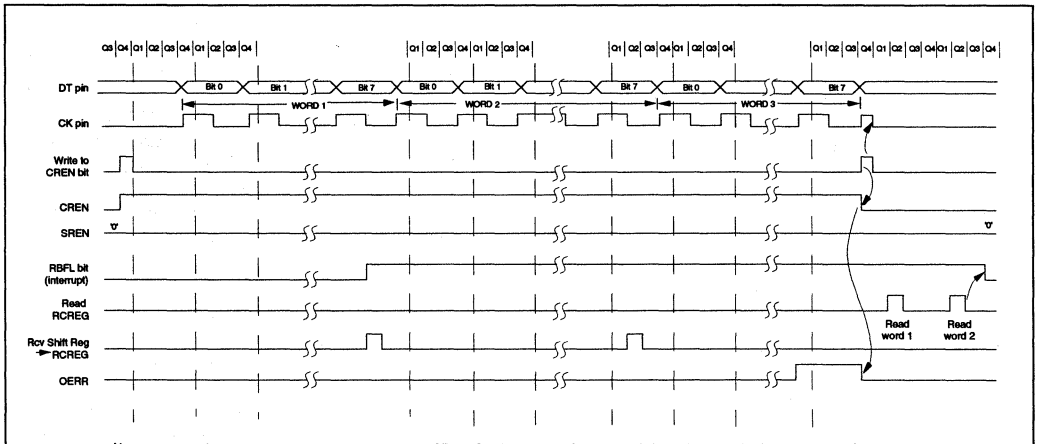
The ninth bit of the received word is loaded into RCD8 (bit0, RCSTA). This bit is buffered the same way as the receive data. Reading the RCREG register will load the new ninth bit. Therefore, the user must read the RCSTA register before reading the received data word from RCREG.

FIGURE 6.2.2.1 - SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates SYNC master mode with SREN = 1 and BRG = 0.

FIGURE 6.2.2.2 - SYNCHRONOUS RECEPTION (MASTER MODE, CREN)



Note : Synchronous master mode reception with CREN. Overflow occurs after two words have been received and reception of the 3rd word is almost complete. Resetting CREN resets the receiver, including the OERR bit. The two words are read which then clears the RBFL flag. The 3rd word is lost.

6.2.3 SYNCHRONOUS SLAVE MODE/SLEEP MODE INTERACTION:

When the part is put into SLEEP mode, all on chip phase clocks are stopped (part is held in Q1 state; see SLEEP section for details). In SLEEP, synchronous slave mode operation is possible because this mode uses external clock.

SLEEP/sync slave receive: If receive is enabled (SREN = '1') prior to invoking SLEEP mode, then a word may be received during SLEEP and at the completion of such reception the RSR will be transferred to RCREG (assuming it is empty). Simultaneously, a receive interrupt will be generated which will wake the chip up, provided this interrupt was enabled (by setting RCIE = PEIE = '1'). If GLINTD = '0', then additionally the interrupt will be responded to by jumping to interrupt vector 0020h. If the receive interrupt is disabled, prior to invoking SLEEP mode, then words are received during SLEEP without waking up the processor. Overflow bit will be set if three words are received.

SLEEP/sync slave transmit: If two words are written to TXREG and then the chip is put into SLEEP the following sequence of events will occur. The first word will immediately transfer to the TSR. The second word will remain in TXREG. Transmit interrupt (TBMT) will stay inactive (low). As the first word is shifted out, the second word will transfer from TXREG to TSR and the transmit interrupt (TBMT) will be raised again. This will wake up the chip provided the interrupt was not masked (i.e. TXIE = PEIE = '1'). If GLINTD = 0, then branch to interrupt vector 0020h will take place as well.

6.3 Baud Rate Generator

The serial port is equipped with a dedicated 8-bit Baud Rate Generator (SPBRG, bank0, file 17h). The SPBRG register is readable and writable. The SPBRG register controls the period of a free running 8-bit timer. In synchronous mode the baud rate is fosc/4(x+1) where fosc = oscillator or clock-in frequency and x = value written to SPBRG register. In asynchronous mode the baud rate is fosc/64(x+1). Tables 6.3.1 and 6.3.2 show baud rate values for different SPBRG value and clock-in frequency. SPBRG is unknown following Power-On Reset.

Writing a value to the SPBRG clears the timer. This guarantees that the timer does not go through an overflow cycle, before outputting the appropriate baud rate.

6.4 Summary of Serial Port Pins

The serial port uses two pins, RA4/RX/DT and RA5/TX/CK. If SPEN bit (bit 7, RCSTA) is set then these pins are controlled by the serial port. If SPEN=0, then they are configured as input only port pins. **(Both pins have Schmitt Trigger input buffer.)**

Pin Name	SPEN = 0	SPEN = 1		
		SYNC Master Mode	SYNC Slave Mode	ASYNC Mode
RA4/RX/DT	input only port pin	DT: Data in/out Data output if TXEN=1 and CREN=0 and SREN=0, Hi-impedance input otherwise		RX: Receive input, Always hi-impedance input.
RA5/TX/CK	input only port pin	CK: clock output Always a driven output	CK: clock input Always hi-impedance input	TX: Transmit Driven output if TXEN=1. Hi-impedance input if TXEN=0

TABLE 6.3.1 - BAUD RATES FOR SYNCHRONOUS MODE

BAUD RATE (K)	tosc = 25MHz KBAUD	%ERROR	SPBRG value (decimal)	fosc = 20MHZ KBAUD	%ERROR	SPBRG value (decimal)	16MHZ KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-
1.2	NA	-	-	NA	-	-	NA	-	-
2.4	NA	-	-	NA	-	-	NA	-	-
9.6	NA	-	-	NA	-	-	NA	-	-
19.2	NA	-	-	19.53	+1.73	255	19.23	+0.16	207
76.8	77.16	+0.47	80	76.92	+0.16	64	76.92	+0.16	51
96	96.15	+0.16	64	96.15	+0.16	51	95.24	-0.79	41
300	297.62	-0.79	20	294.1	-1.96	16	307.69	+2.56	12
500	480.77	-3.85	12	500	0	9	500	0	7
HIGH	6250	-	0	5000	-	0	4000	-	0
LOW	24.41	-	255	19.53	-	255	15.625	-	255

BAUD RATE (K)	10MHz KBAUD	%ERROR	SPBRG value (decimal)	7.15909MHZ KBAUD	%ERROR	SPBRG value (decimal)	fosc =5.0688MHZ KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-
1.2	NA	-	-	NA	-	-	NA	-	-
2.4	NA	-	-	NA	-	-	NA	-	-
9.6	9.766	+1.73	255	9.622	+0.23	185	9.6	0	131
19.2	19.23	+0.16	129	19.24	+0.23	92	19.2	0	65
76.8	75.76	-1.36	32	77.82	+1.32	22	79.2	+3.13	15
96	96.15	+0.16	25	94.20	-1.88	18	97.48	+1.54	12
300	312.5	+4.17	7	298.3	-0.57	5	316.8	+5.60	3
500	500	0	4	NA	-	-	NA	-	-
HIGH	2500	-	0	1789.8	-	0	1267	-	0
LOW	9.766	-	255	6.991	-	255	4.950	-	255

BAUD RATE (K)	3.579545MHz KBAUD	%ERROR	SPBRG value (decimal)	1MHZ KBAUD	%ERROR	SPBRG value (decimal)	32.768KHZ KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	0.303	+1.14	26
1.2	NA	-	-	1.202	+0.16	207	1.170	-2.48	6
2.4	NA	-	-	2.404	+0.16	103	NA	-	-
9.6	9.622	+0.23	92	9.615	+0.16	25	NA	-	-
19.2	19.04	-0.83	46	19.24	+0.16	12	NA	-	-
76.8	74.57	-2.90	11	83.34	+8.51	2	NA	-	-
96	99.43	+3.57	8	NA	-	-	NA	-	-
300	298.3	-0.57	2	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-
HIGH	894.9	-	0	250	-	0	8.192	-	0
LOW	3.496	-	255	0.9766	-	255	0.032	-	255

TABLE 6.3.2 - BAUD RATES FOR ASYNCHRONOUS MODE

BAUD RATE (K)	fosc = 25MHz KBAUD	%ERROR	SPBRG value (decimal)	20MHZ KBAUD	%ERROR	SPBRG value (decimal)	16MHZ KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-
1.2	NA	-	-	1.221	+1.73	255	1.202	+0.16	207
2.4	2.396	0.14	162	2.404	+0.16	129	2.404	+0.16	103
9.6	9.53	-0.76	40	9.469	-1.36	32	9.615	+0.16	25
19.2	19.53	+1.73	19	19.53	+1.73	15	19.23	+0.16	12
76.8	78.13	+1.73	4	78.13	+1.73	3	83.33	+8.51	2
96	97.65	+1.73	3	104.2	+8.51	2	NA	-	-
300	390.63	+30.21	0	312.5	+4.17	0	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-
HIGH	390.6	-	0	312.5	-	0	250	-	0
LOW	1.53	-	255	1.221	-	255	0.977	-	255

BAUD RATE (K)	10MHz KBAUD	%ERROR	SPBRG value (decimal)	7.15909MHZ KBAUD	%ERROR	SPBRG value (decimal)	fosc =5.0688MHZ KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	0.31	+3.13	255
1.2	1.202	+0.16	129	1.203	+0.23	92	1.2	0	65
2.4	2.404	+0.16	64	2.380	-0.83	46	2.4	0	32
9.6	9.766	+1.73	15	9.322	-2.90	11	9.9	+3.13	7
19.2	19.53	+1.73	7	18.64	-2.90	5	19.8	+3.13	3
76.8	78.13	+1.73	1	NA	-	-	79.2	+3.13	0
96	NA	-	-	NA	-	-	NA	-	-
300	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-
HIGH	156.3	-	0	111.9	-	0	79.2	-	0
LOW	0.6104	-	255	0.437	-	255	0.3094	-	255

BAUD RATE (K)	3.579545MHz KBAUD	%ERROR	SPBRG value (decimal)	1MHZ KBAUD	%ERROR	SPBRG value (decimal)	32.768KHZ KBAUD	%ERROR	SPBRG value (decimal)
0.3	0.301	+0.23	185	0.300	+0.16	51	0.256	-14.67	1
1.2	1.190	-0.83	46	1.202	+0.16	12	NA	-	-
2.4	2.432	+1.32	22	2.232	-6.99	6	NA	-	-
9.6	9.322	-2.90	5	NA	-	-	NA	-	-
19.2	18.64	-2.90	2	NA	-	-	NA	-	-
76.8	NA	-	-	NA	-	-	NA	-	-
96	NA	-	-	NA	-	-	NA	-	-
300	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-
HIGH	55.93	-	0	15.63	-	0	0.512	-	0
LOW	0.2185	-	255	0.0610	-	255	0.0020	-	255

6.4 Serial Port Registers

6.4.1 SUMMARY OF SERIAL PORT REGISTERS

Register Name	Function	Address	Reset Value
RCSTA	Receive status/control register	Bank 0, File 13h	0000000Xb
RCREG	Receive buffer register	Bank 0, File 14h	XXXXXXXXb
TXSTA	Transmit status/control register	Bank 0, File 15h	0000001Xb
TXREG	Transmit buffer register	Bank 0, File 16h	XXXXXXXXb
SPBRG	Baud Rate Generator	Bank 0, File 17h	XXXXXXXXb
PIR	Peripheral interrupt flag register	Bank 1, File 16h	00000010b
PIE	Peripheral interrupt enable register	Bank 1, File 17h	00000000b
INTSTA	Interrupt status register	File 07h	00000000b
CPUSTA	CPU status register	File 06h	0011XX00b

FIGURE 6.4.1.1 - RCSTA: RECEIVE STATUS & CONTROL REGISTER

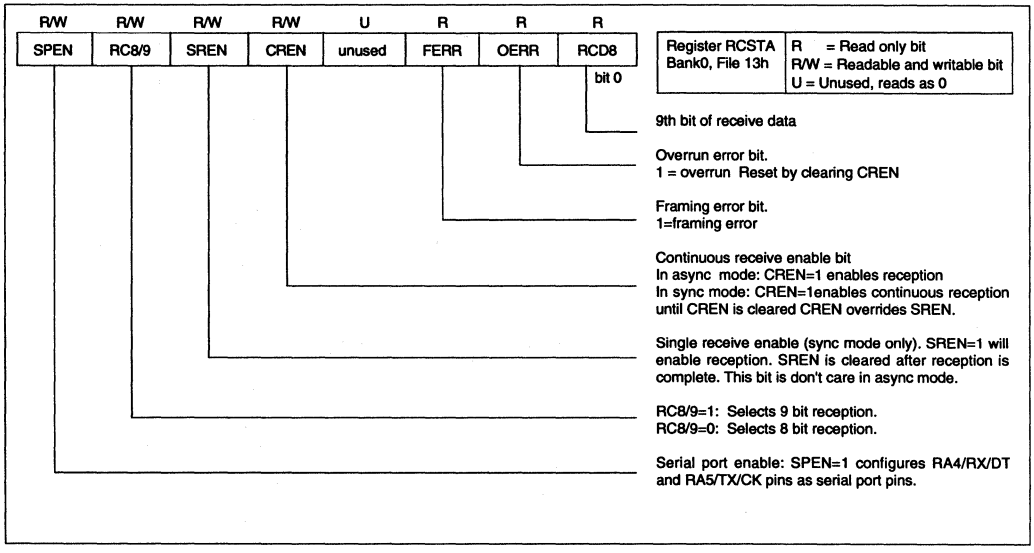
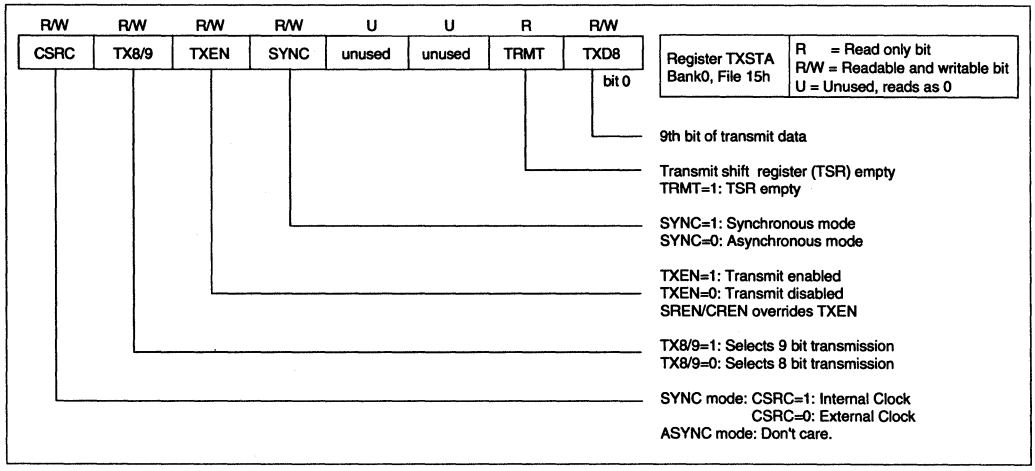


FIGURE 6.4.1.2 - TXSTA: TRANSMIT STATUS & CONTROL REGISTER



7.0 TIMER/COUNTERS: OVERVIEW

The PIC17C42 has a rich set of timer/counters: Two 8-bit timer counters (also configurable as one 16-bit timer/counter) and two 16-bit timer/counters. These can be configured as:

-Two 16-bit + two 8-bittimer/counters

-Three 16-bit timer/counters

A brief overview of these timer/counters is as follows:

TMR0: TMR0 is a 16-bit timer/counter consisting of two 8-bit sections (TMR0H, TMR0L). It has a programmable 8-bit prescaler. TMR0 can increment off internal clock (OSC/4) or external clock input on the RA1/T0CKI pin. TMR0 generates an interrupt on overflow.

TMR1, TMR2: These are two 8-bit timer/counters. They each have an 8-bit period register (PR1 and PR2 respectively) and an interrupt. In counter mode, their clock comes from pin TCLK12 (shared between the two timer/counters). They can be configured as a 16-bit timer/counter with interrupt and a 16-bit period register.

TMR3: Timer3 is a 16-bit timer/counter consisting of two 8-bit sections TMR3H and TMR3L. It has a 16-bit period register (PR3H, PR3L), an interrupt and an external clock source (pin TCLK3) in counter mode.

7.1 Role of the Timer/Counters

The timer/counters are general purpose. However, they have special usage. TMR0 is physically part of the 'core'. It is planned that future variations of the PIC17CXX family will include this timer. Therefore, time dependent code, e.g. real time operating system or clock/calender type software can be written using RTCC and ported to future PIC17CXX family members.

TMR3 is also used for 16-bit capture function as is described in capture section. Timers TMR1 and TMR2 can be used as time bases for PWM1 and PWM2 outputs respectively. Alternately, TMR1 can run both PWM outputs and thus free up TMR2 to be a general purpose timer.

These timers are not needed to do the following functions: Watchdog Timer (it's a separate timer); Baud Rate generation for serial communication (serial port has its own 8-bit Baud Rate Generator).

7.2 TMR0 Module

The TMR0 module consists of a 16-bit timer/counter, TMR0 (high byte TMR0H, file 0Ch and low byte TMR0L, file 0Bh), an 8-bit prescaler, and the RA1/T0CKI pin as the source of external clock signal. The control bits for this module are in register RTCSTA.

FIGURE 7.2.1.1 - TMR0 MODULE BLOCK DIAGRAM

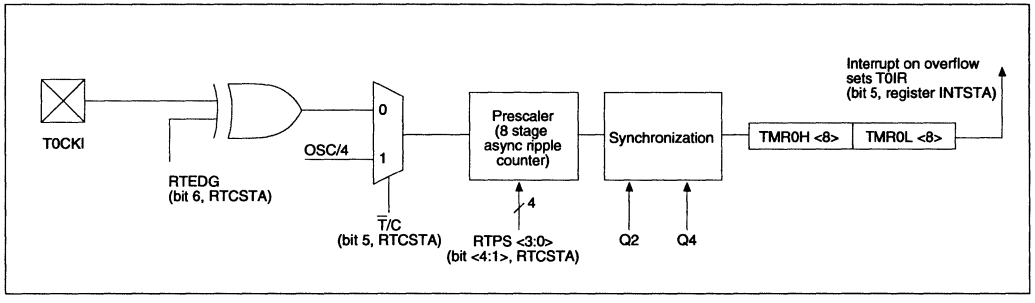
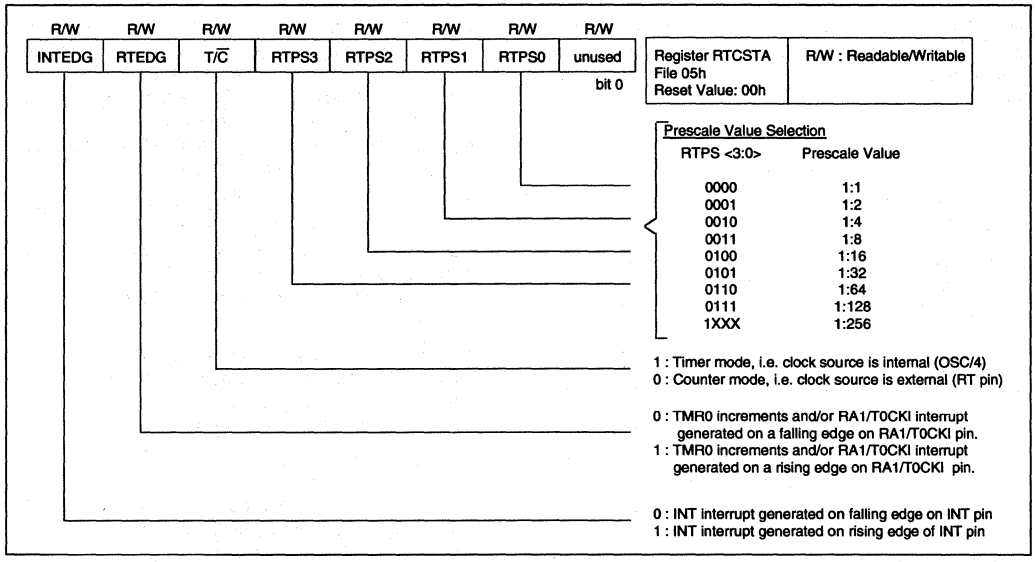


FIGURE 7.2.1.2 - RTCSTA: TMR0 STATUS/CONTROL REGISTER



7.2.1 TMR0 OPERATION

TMR0 increments either on internal clock, OSC/4 (if T/C = '1' in RTCSTA) or on external clock (counter mode) on T0CKI pin (if bit T/C = '0' in RTCSTA). If external clock is chosen, increment can occur on either the rising edge (RTEDG = '1' is RTCSTA register) or the falling edge (RTEDG = '0' is RTCSTA register). The prescaler can be programmed to introduce a prescale of 1:1 to 1:256 in either timer or counter mode. The timers increment from 0000h to FFFFh and roll over to 0000h. On overflow, the TMR0 interrupt request flag, T0IR (bit 5, register INTSTA), is set. The TMR0 interrupt can be masked off by clearing the corresponding interrupt mask bit, T0IE (bit 1, INTSTA). The interrupt request flag, T0IR, must be cleared in software.

7.2.2 READ/WRITE CONSIDERATION FOR TMR0

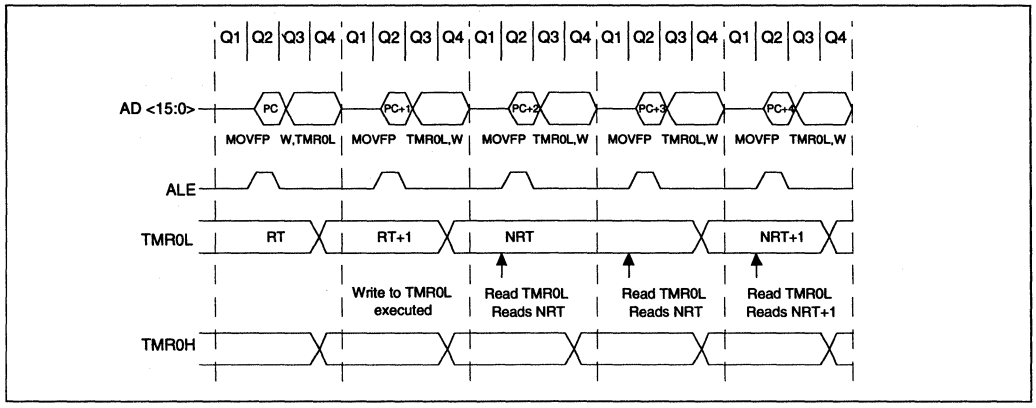
Although the TMR0 is a 16-bit timer/counter, only 8-bits at a time can be read or written. This could create a problem unless care is taken.

Reading 16-bit value: One problem in reading the entire 16-bit value is that after reading the low (or high) byte it may change from FFh to 00h. This can be handled in software as follows:

```
movpf   tmr0l, tmplo   ;read lo tmr0
movpf   tmr0h, tmphi   ;read hi tmr0
movfp   tmplo, wreg    ;tmplo → wreg
cpfslt  tmr0l, wreg    ;tmr0l < wreg?
retfie                 ;no then return
movpf   tmr0l, tmplo   ;read lo tmr0
movpf   tmr0h, tmphi   ;read hi tmr0
retfie                 ;return
```

Interrupts must be disabled during this subroutine.

FIGURE 7.2.2.1 - TMR0 TIMING: WRITE HIGH OR LOW BYTE



Writing a 16-bit value to the TMR0: Since writing to either TMR0L or TMR0H will effectively inhibit increment of that half of the TMR0 in the next cycle (following write), but not inhibit increment of the other half, the user must write to TMR0L first and TMR0H next in two consecutive instructions, as shown below:

```
BSF     CPUSTA, GLINTD      ; Disable interrupt
MOVFP   RAM_L, TMR0L        ;
MOVFP   RAM_H, TMR0H        ;
BCF     CPUSTA, GLINTD      ; Done, enable interrupt
```

Interrupt must be disabled. The user should note that a write to TMR0L or TMR0H will reset the prescaler.

7.2.3 EXTERNAL CLOCK CONSIDERATIONS

When the external clock input is used for TMR0, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements. Also, there is some delay from the occurrence of the external clock edge to the incrementing of TMR0. Referring to Figure 7.2.3.1, the synchronization is done after the prescaler. The output of the prescaler (PSOUT) is sampled twice in every instruction cycle to detect a rising or a falling edge. Therefore, it is necessary for PSOUT to be high for at least 2tosc or low for at least 2tosc where tosc= oscillator time period.

When no prescaler is used (i.e. prescale is 1:1) : PSOUT is the same as the TMR0 clock input and therefore the requirements are:

T_{RTH} = RA1/T0CKI high time ≥ 2tosc + 20ns

T_{RTL} = RA1/T0CKI low time ≥ 2 tosc + 20ns

When prescaler is used: the RA1/T0CKI input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical. The requirements are then:

PSOUT high time = PSOUT low time = $\frac{N \bullet T_{RT}}{2}$

where T_{RT} = RA1/T0CKI input period and

N = prescale value (2, 4, ..., 256).

Therefore $\frac{N \bullet T_{RT}}{2} \geq$ 2tosc + 20 ns, or $T_{RT} \geq \frac{4\,tosc + 40ns}{N}$

The user will notice that no requirement on TMR0 high time or low time is specified. However, if the high time or low time on the TMR0 input is too small then the pulse may not be detected, hence a minimum high or low time of 10ns is required, In summary, the TMR0 input requirements are:

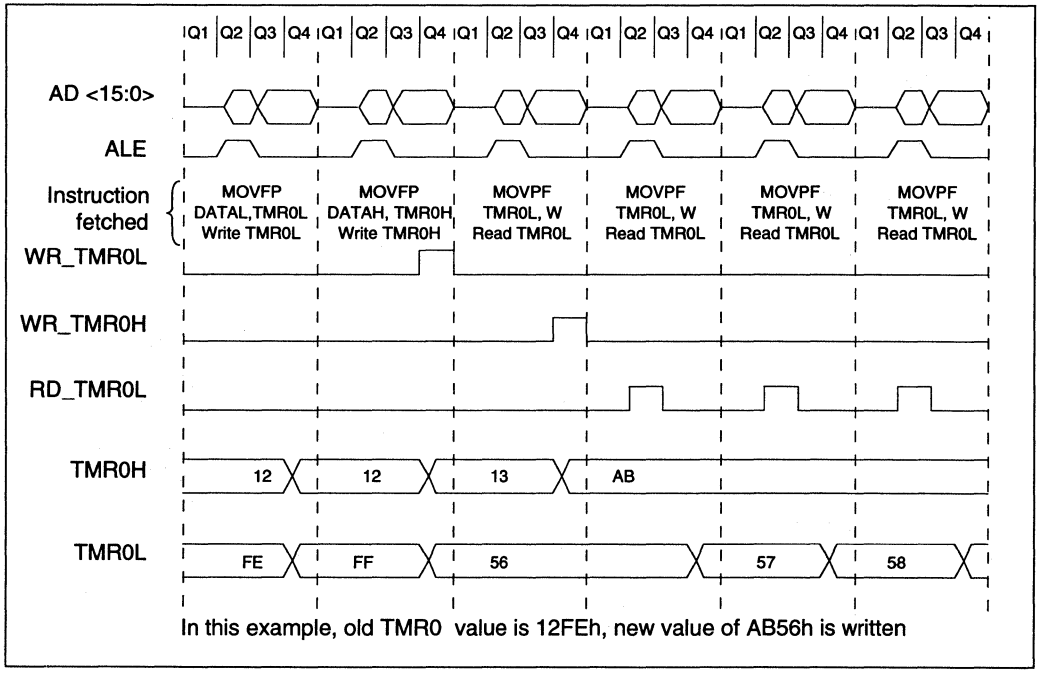
T_{RT} = RA1/T0CKI period ≥ (4tosc + 40 ns)/N

T_{RTH} = RA1/T0CKI high time ≥ 10ns

T_{RTL} = T0CKI low time ≥ 10ns

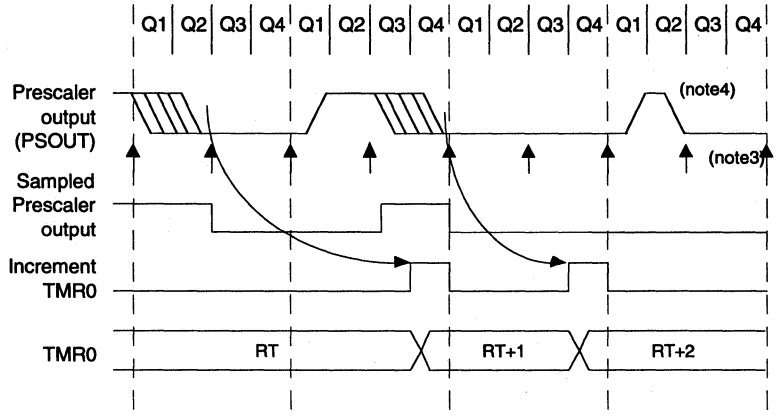
Delay from external clock edge: since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 is actually incremented. Referring to Figure 7.2.3.1, the reader can see that this delay is between 3tosc and 7tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ± 4tosc (± 160ns @ 25 MHz).

FIGURE 7.2.2.2 - RTCC READ/WRITE IN TIMER MODE



In this example, old TMR0 value is 12FEh, new value of AB56h is written

FIGURE 7.2.3.1 - TMR0 TIMING WITH EXTERNAL CLOCK



Note1: The TMR0 increments on falling edges in this example
Note2: The delay from the T0CKI edge to the TMR0 increment is 3tosc-7tosc. Therefore, error in measuring the interval between two edges is ± 4tosc.
Note3: ↑ = PSOUT is sampled here.
Note4: The PSOUT high time is too small and is missed by the sampling circuit.

7.2.4 SUMMARY OF RTCC REGISTERS

Register Name	Function	Address	Reset Value
TMR0L	TMR0 Timer/Counter low byte	File 0Bh	xxxxxxxxb
TMR0H	TMR0 Timer/Counter high byte	File 0Ch	xxxxxxxxb
RTCSTA	TMR0 Status/Control	File 05h	00000000b
INTSTA	Interrupt Status Register	File 07h	00000000b
CPUSTA	CPU Status Register	File 06h	0011xx00b

7.3 Timer1 & Timer2

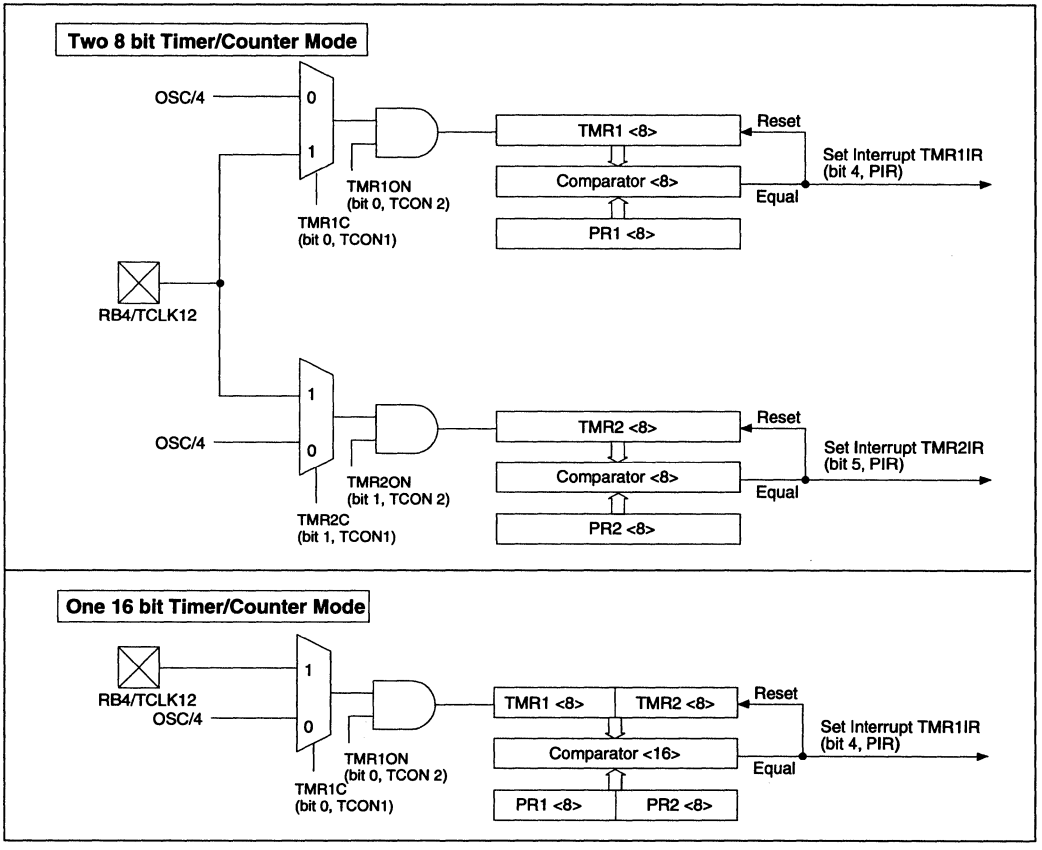
Timer1 (TMR1, Bank 2) and Timer2 (TMR2, Bank 2) are two 8-bit incrementing timer/counters, each with a period register (PR1, Bank 2 and PR2, Bank 2, respectively) and separate overflow interrupt. They can operate as timers (increment on internal OSC/4 clock) or as counters (increment on falling edge of external clock on pin TCLK12). They can operate as two 8-bit timer/counters or as a single 16-bit timer counter. TMR1 and TMR2 are also used as the time base for the PWM (pulse width modulation) module.

7.3.1 TIMER1, TIMER2 IN 8-BIT MODE

8-bit mode is selected by setting 16/8 (bit 3, register TCON1) to '0'. In this mode, TMR1 will be configured as a timer if control bit TMR1C (bit 0, register TCON1) is '0' and increment once every instruction cycle (OSC/4). Setting bit TMR1C = '1' will configure TMR1 as a counter. As a counter, TMR1 will increment on every negative edge on pin TCLK12. Since TCLK12 input is synchronized with internal phase clocks, it has to satisfy certain requirements. TCLK12 must be high for at least (0.5Tcy + 20)ns and low for at least (0.5Tcy + 20)ns where Tcy = 4tosc. TMR1 increments from 00h until it is equal to PR1 and then resets to 00h at the next increment cycle. An interrupt is generated when reset occurs which is latched in bit TM1IR (TMR1 Interrupt Request Flag, bit 4, PIR). This bit can be masked off by setting bit TM1IE (TMR1 Interrupt Enable) to '0'. In order for the TM1IR interrupt to be recognized, the Peripheral Interrupt Enable bit (PEIE, bit 3, register INTSTA) must be set to a '1' and the Global Interrupt Disable bit, GLINTD, must be '0'. TMR1 must be enabled by setting bit TMR1ON (bit 0, register TCON2) to a '1' and can be stopped any time by clearing bit TMR1ON to '0'. TMR1 and PR1 are both readable and writable registers.

TMR2, in 8-bit mode is identical in functionality as TMR1. The corresponding control bits for TMR2 are TMR2C (bit 1, TCON1), TM2IR (Timer2 Interrupt-Request Flag, bit 5, PIR), TM2IE (Timer2 Interrupt Enable Flag, bit 5, PIE) and TMR2ON (bit 1, TCON2). In counter mode, TMR2 also increments on falling edge on TCLK12 pin.

FIGURE 7.3.1.1 - TIMER1/TIMER2 BLOCK DIAGRAM



7.3.2 TIMER1 & TIMER2 IN 16-BIT MODE

16-bit mode is selected by setting bit 16/$\overline{8}$ (bit 3, register TCON1) to '1'. In this mode TMR1 and TMR2 concatenate to form one 16-bit timer/counter (TMR2 = high byte). Timer mode is selected by setting TMR1C (bit0, register TCON1) to '0' where it increments once every instruction cycle (OSC/4). Counter mode is selected if TMR1C bit = '1' and it increments on every negative edge on pin TCLK12. Input clock on TCLK12 must have a high time ≥ (0.5Tcy + 20)ns and a low time ≥ (0.5Tcy + 20)ns where Tcy = 4tosc. The 16-bit timer increments until it matches the 16-bit value in PR1, PR2 (PR2 = high byte) and then resets back to 0000h. An interrupt is generated at this time which is latched into the TM1IR bit (bit 4, PIR). In 16-bit mode, control bit TMR1C controls the entire 16-bit timer and bit TMR2C is a don't care. The TMR2ON bit must be always set to '1' in 16 bit mode. TMR1ON bit controls the entire 16-bit timer.

7.3.3 EXTERNAL CLOCK INPUT FOR TIMER1, TIMER2

When configured as a counter, TMR1 or TMR2 increments on the falling edge of clock input TCLK12. However, this input is sampled and synchronized by the internal phase clocks twice every instruction cycle. Therefore, the external clock must meet the following requirements:

TCLK12 high time ≥ 0.5 Tcy + 20ns
TCLK12 low time ≥ 0.5 Tcy + 20ns

There is a delay from the time a falling edge appears on TCLK12 to the time TMR1 or TMR2 is actually incremented. The delay is between 2tosc and 6tosc, where tosc = oscillator period. See Figure 7.3.3.1 for a timing diagram.

FIGURE 7.3.1.2 - TMR1, TMR2, TMR3 TIMING IN TIMER MODE

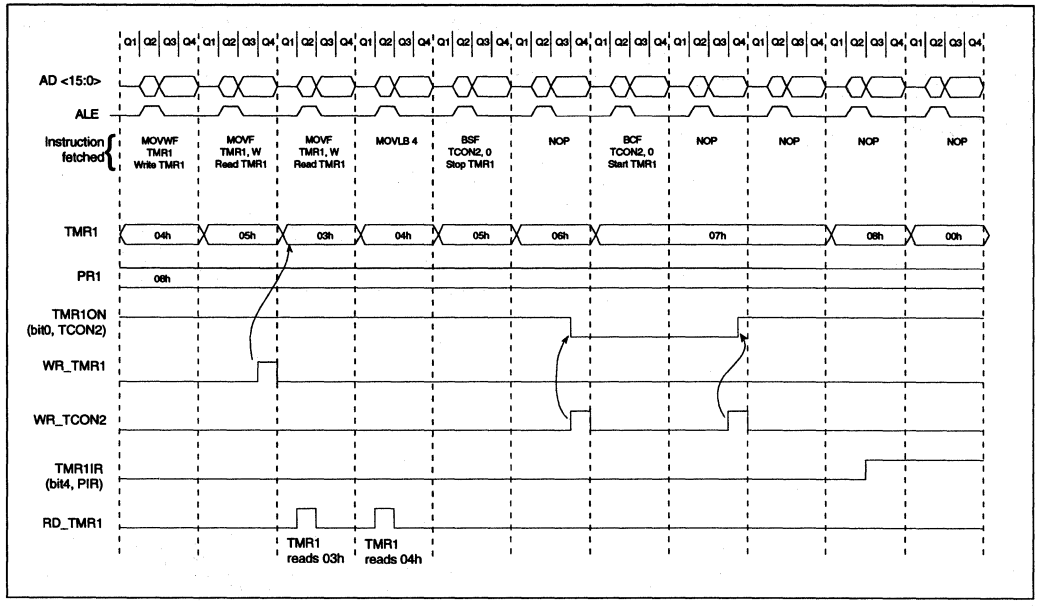
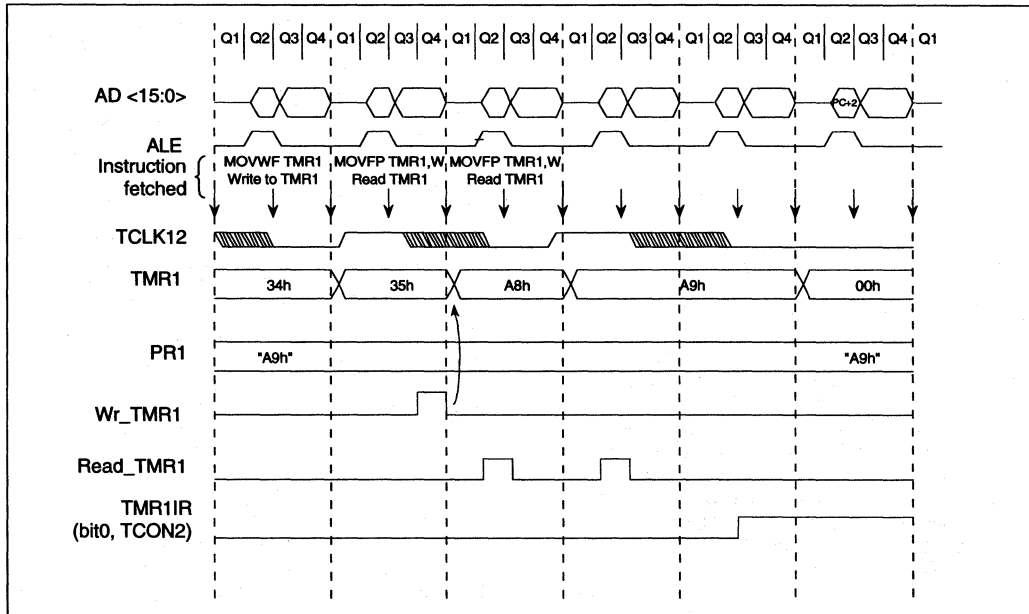


FIGURE 7.3.3.1 - TMR1, TMR2 AND TMR3 IN EXTERNAL CLOCK MODE



Notes: TCLK12 is sampled in Q2 and Q4. ↓ indicates a sampling point.
The latency from TCLK12 ↓ to timer increment is between 2 tosc and 6 tosc.

FIGURE 7.3.1.3 - TIMER/CAPTURE/PWM CONTROL REGISTER 1 (TCON1)

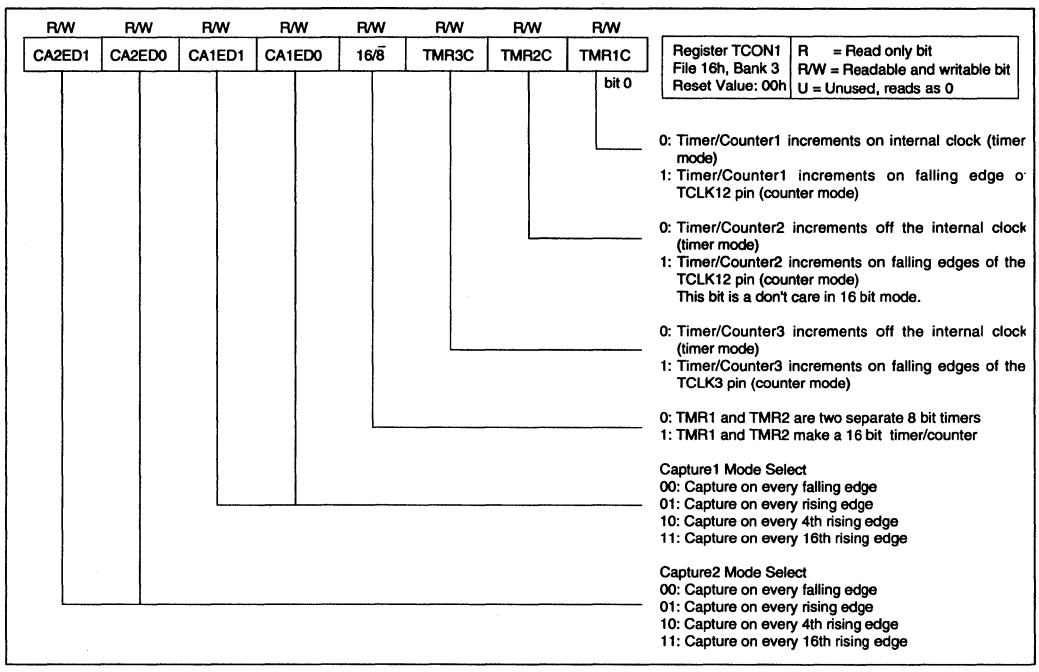
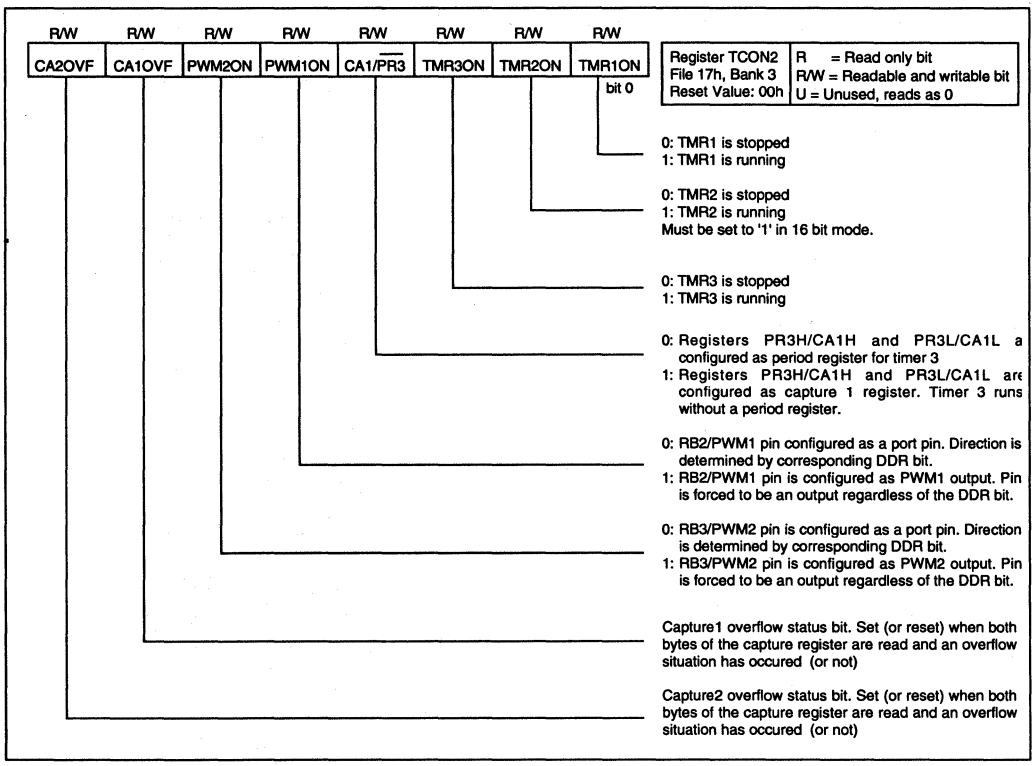


FIGURE 7.3.3.2 - TIMER/CAPTURE/PWM CONTROL REGISTER 2 (TCON2)



7.3.4 SUMMARY OF TIMER1, TIMER2 REGISTERS

Register Name	Function	Address	Reset Value
TMR1	Timer/Counter1	Bank 2, File 10h	xxxxxxxxb
TMR2	Timer/Counter2	Bank 2, File 11h	xxxxxxxxb
PR1	Period Register1	Bank 2, File 14h	xxxxxxxxb
PR2	Period Register2	Bank 2, File 15h	xxxxxxxxb
TCON1	Timer Control Register1	Bank 3, File 16h	00000000b
TCON2	Timer Control Register2	Bank 3, File 17h	00000000b
PIR	Peripheral Interrupt Register	Bank 1, File 16h	00000010b
PIE	Peripheral Interrupt Enable	Bank 1, File 17h	00000000b
INTSTA (bit PEIE)	Interrupt Status Register	File 07h	00000000b
CPUSTA (bit GLINTD)	CPU Status Register	File 06h	0011XX00b

7.4 Timer/Counter 3

TMR3 is a 16-bit timer/counter consisting of TMR3L (file 12, Bank 2) as the low byte of the timer and TMR3H (file 13, Bank 2) as the high byte of the timer. It has an associated 16-bit period register consisting of PR3L/CA1L (file 16, Bank 2), the low byte, and PR3H/CA1H (file 17, Bank 2), the high byte. Timer3 is a timer if TMR3C = 0 (bit 2, Register TCON1) in which case it increments every instruction cycle (OSC/4). If TMR3C = 1, the timer 3 acts as a counter and increments on every falling edge of TCLK3 pin input. In either mode, TMR3 increments if TMR3ON = 1 (bit 2, Register TCON2) and stops if TMR3ON = 0. TMR3 has two modes of operation: depending on bit CA1/$\overline{PR3}$ (bit 3, Register TCON2) the period register can be configured as a period or a capture register (Refer to Section 8.0 for details on capture operation).

Period register mode, CA1/$\overline{PR3}$ = 0: In this mode registers PR3H/CA1H and PR3L/CA1L constitute a 16-bit period register. The timer increments until it equals the period register and then resets to 0000h. Timer3 interrupt (TM3IR, bit 6, Register PIR) request flag is set at this point. This interrupt can be disabled by setting timer3 mask bit (TM3IE, bit 6, Register PIE) to '0'. TM3IR must be cleared in software.

Capture1 register mode, CA1/$\overline{PR3}$ = 1: In this mode the PR3H/CA1H and PR3L/CA1L constitute a 16-bit capture register. The timer operates without a period register and increments from 0000h to FFFFh and rolls over to 0000h. A timer3 interrupt (TM3IR, bit 6, Register PIR) is generated on overflow. The TM3IR interrupt flag must be cleared in software.

7.4.1 EXTERNAL CLOCK INPUT FOR TIMER3

Timer3 increments on the falling edges of the clock input on TCLK3 pin. However, this input is sampled and synchronized by the internal phases, twice every instruction cycle. Therefore, the external clock input must meet the following requirements:

TCLK3 high time ≥ 0.5Tcy + 20 ns

TCLK3 low time ≥ 0.5Tcy + 20 ns

There is a delay from the time an edge occurs on TCLK3 to the time the timer3 is actually incremented. This delay is between 2 tosc and 6tosc, where tosc = oscillator period. See Figure 7.3.3.1 for a timing diagram.

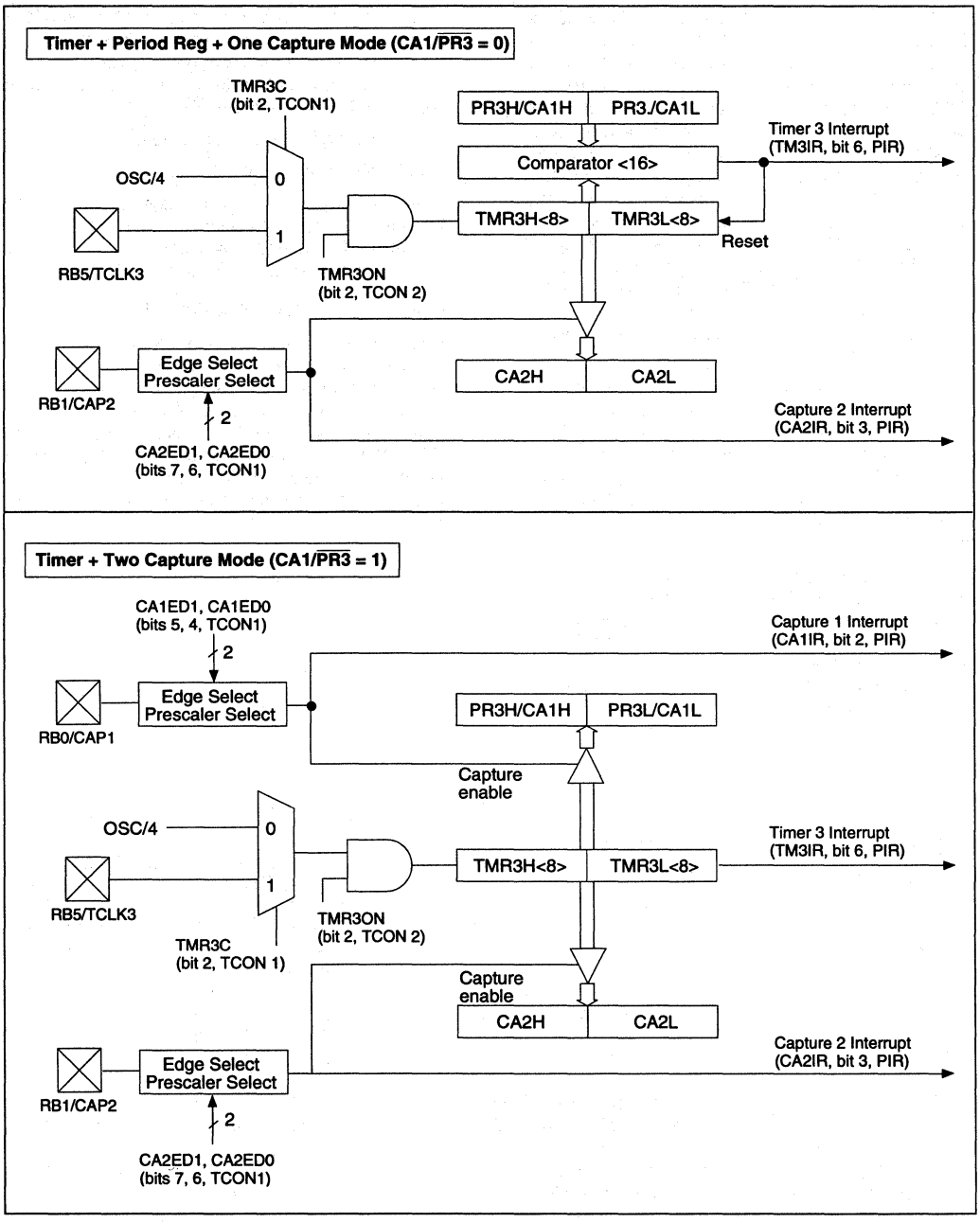
7.4.2 READING/WRITING TIMER3

Since timer3 is a 16-bit timer and only 8-bits at a time can be read or written, the user should be careful about reading and writing when the timer is running. The safe and easy thing to do is to stop the timer, perform any read or write operation, and then restart timer3 (using the TMR3ON bit). If, however, it is necessary to keep timer3 free-running then certain suggested methods must be followed for reading and writing the timer. See Section 7.2.3 for details.

7.4.3 SUMMARY OF TIMER3 REGISTERS

Register Name	Function	Address	Reset Value
TMR3L	Timer/Counter3 low byte	Bank 2, File 12h	xxxxxxxxb
TMR3H	Timer/Counter3 high byte	Bank 2, File 13h	xxxxxxxxb
CA2L	Capture2 low byte	Bank 3, File 14h	xxxxxxxxb
CA2H	Capture2 high byte	Bank 3, File 15h	xxxxxxxxb
PR3L/CA1L	Period Register3 low/capture 1 low	Bank 2, File 16h	xxxxxxxxb
PR3H/CA1H	Period Register3 high/capture 1 high	Bank 2, File 17h	xxxxxxxxb
TCON1	Timer Control Register1	Bank 3, File 16h	00000000b
TCON2	Timer Control Register2	Bank 3, File 17h	00000000b
PIR	Peripheral Interrupt Register	Bank 1, File 16h	00000010b
PIE	Peripheral Interrupt Enable	Bank 1, File 17h	00000000b
INTSTA (bit PEIE)	Interrupt Status Register	File 07h	00000000b
CPUSTA (bit GLINTD)	CPU Status Register	File 06h	0011XX00b

FIGURE 7.4.1.1 - TIMER3/CAPTURE MODULE BLOCK DIAGRAM



8.0 CAPTURE MODULE

The PIC17C42 has two 16-bit capture registers that capture the 16-bit value of timer/counter3 (TMR3) when events are detected on capture pins. There are two capture pins (RB0/CAP1 and RB1/CAP2), one for each capture register. The capture pins are multiplexed with PORTB pins. An event can be a rising edge, a falling edge, 4 rising edges or 16 rising edges on the pin. Each capture register has an interrupt request flag associated with it which is set when a capture is made. The capture module is truly part of the timer/counter3/capture block. Refer to Figure 7.4.1.1 for a block diagram. The capture module can operate in one of two modes described below.

8.1 One Capture + Timer/Counter3 + Period Register Mode

This mode is selected if control bit CA1/$\overline{PR3}$ = 0 (bit 3, register TCON2). In this mode, the capture1 register, consisting of high byte (PR3H/CA1H, File 17, Bank 2) and low byte (PR3L/CA1L, File 16, Bank 2), is configured as the period control register for TMR3. Capture1 is disabled in this mode, and the corresponding interrupt bit CA1IR (bit 2, PIR) is never set. Timer/counter3 increments until it equals the value in the period register and then resets to 0000h. See Section 8.4 for details of TMR3 operation in this mode.

Capture2 is active in this mode. Control bits CA2ED1 and CA2ED0 (bits 7 and 6, Register TCON1) determine the event on which capture will occur. CA2ED1, CA2ED0 = 00 enables capture on every falling edge, 01 = capture on every rising edge, 10 = capture every 4th rising edge and 11 = capture every 16th rising edge. When a capture takes place, an interrupt is latched into CA2IR (capture 2 interrupt flag, bit 3, PIR). This interrupt can be enabled by setting the corresponding mask bit CA2IE (bit 3, PIE). Also, peripheral interrupt enable bit PEIE (bit 3, INSTA) must be set and the Global Interrupt Disable bit (GLINTD, bit 4, CPUSTA), should be cleared for the interrupt to be acknowledged. The CA2IR interrupt flag needs to be cleared in software.

When the capture prescale select is changed, the prescaler is not reset. Therefore, the first capture after such a change will be ambiguous. It, however, sets the basis for the next capture. The prescaler is reset upon chip reset.

The capture pin RB1/CAP2 is a multiplexed pin. When used as a port pin, capture2 is not disabled. However, the user can simply disable the capture2 interrupt by clearing CA2IE. If RB1/CAP2 is used as an output pin, some interesting possibilities arise. The user can activate a capture by writing to the port pin which may be useful during development phase to emulate a capture interrupt.

The input on capture pin, RB1/CAP2, is synchronized internally to internal phase clocks. This imposes certain restrictions on the input waveform. The minimum high time (T_{CPH}) and the minimum low time (T_{CPL}) on the capture input needs to be greater or equal to 10ns. The period (T_{CAP}) must be >2Tcy/N where N = prescale value (1, 4, 16) and where Tcy = one instruction cycle time (= 4tosc).

Capture2 Overflow

The overflow status flag bit is double buffered. The master bit is set if one captured word is already residing in the capture2 register and another 'event' has occurred on RB1/CA2 pin. The new event will not transfer the timer3 value to the capture register, protecting the previous unread capture value. When the user reads both the high and the low bytes (in any order) of the capture2 register, the master overflow bit is transferred to the slave overflow bit (CA2OVF, bit 7, TCON2) and then the master bit is reset. The user can then read TCON2 to determine the value of CA2OVF.

The recommended sequence to read capture registers and overflow is as follows:

```
MOVLB  3                  ; Select Bank 3
MOVPF  CA2L, LO_BYTE      ; Read capture2 low byte,
                          ; store in LO_BYTE
MOVPF  CA2H, HI_BYTE      ; Read capture2 high byte,
                          ; store in HI_BYTE
MOVPF  TCON2, STAT_VAL    ; Read TCON2 into file
                          ; STAT_VAL
```

8.2 Two Capture + Timer/Counter3 Mode

This mode is selected by setting CA1/$\overline{PR3}$ (bit 3, register TCON2). In this mode, the timer (TMR3) runs without a period register and increments from 0000h to FFFFh and rolls over to 0000h. For details on TMR3 operation, see Section 8.4. Registers PR3H/CA1H (file 17h, Bank 2) and PR2L/CA1L (file 16h, Bank 2) make a 16-bit capture register (Capture1). It captures events on pin RB0/CAP1. Capture mode is set by control bits CA1ED1 and CA1ED0 (bit 5 and 4, Register TCON1). A capture1 interrupt is latched into the CA1IR (bit 2, PIR). The corresponding interrupt mask bit is CA1IE (bit 2, PIE). The capture1 overflow status bit is CA1OVF (bit 6, TCON2). Otherwise, capture1 operates identically to capture2. Capture2 operation is same as in the previous mode.

8.3 Summary of Capture Registers

Register Name	Function	Address	Reset Value
PR3L/CA1L	Period Register 3 low/capture 1 low	Bank 2, File 16h	xxxxxxxxb
PR3H/CA1H	Period Register 3 high/capture 1 low	Bank 2, File 17h	xxxxxxxxb
CA2L	Capture2 register low	Bank 3, File 14h	xxxxxxxxb
CA2H	Capture2 register high	Bank 3, File 15h	xxxxxxxxb
TMR3L	Timer/Counter 3 low	Bank 2, File 12h	xxxxxxxxb
TMR3H	Timer/Counter 3 high	Bank 2, File 13h	xxxxxxxxb
TCON1	Timer Control Register 1	Bank 3, File 16h	00000000b
TCON2	Timer Control Register 2	Bank 3, File 17h	00000000b
PIR	Peripheral Interrupt Register	Bank 1, File 16h	00000010b
PIE	Peripheral Interrupt Enable	Bank 1, File17h	00000000b
INTSTA (bit PEIE)	Interrupt Status Register	File 07h	00000000b
CPUSTA (bit GLINTD)	CPU Status Register	File 06h	0011XX00b

9.0 PULSE WIDTH MODULATION (PWM) OUTPUTS

The PIC17C42 provides two high speed pulse-width modulation outputs on pins RB2/PWM1 and RB3/PWM2. Each PWM output has a maximum resolution of 10-bits. At 10 bit resolution, the PWM output frequency is 24.4 KHz (@ 25 MHz clock) and at 8-bit resolution the PWM output frequency is 97.7 KHz.

The user needs to set the PWM1ON control bit (bit 4, register TCON2) to enable the PWM1 output. Once the PWM1ON bit = '1', the RB2/PWM1 pin is configured as PWM1 output and forced as an output irrespective of the data direction bit. If PWM1ON = '0', then the pin behaves as a port pin and its direction is controlled by its data direction bit (bit2, DDRB). Similarly, the PWM2ON bit controls the configuration of the RB3/PWM2 pin.

The period of the PWM1 output is determined by timer1 (TMR1) and its period register (PR1). The period of the PWM2 output is determined by timer1 if control bit TM2PW2 = '0' (bit 5, register PW2DCL) or by timer2 if TM2PW2 = '1'.

Thus the PWM periods are:

t_{PWM1P} = period of PWM1 = [(PR1) + 1] x 4 tosc

t_{PWM2P} = period of PWM2 = [(PR1) + 1] x 4 tosc

or [(PR2) + 1] x 4 tosc

The duty cycle of PWM1 is determined by the 10 bit value DC1<9:0>. The upper 8 bits are from register PW1DCH (file 12, Bank 3) and the lower 2 bits are in register PW1DCL<1:0> (file 10, Bank 3). The PWM1 high time is as follows:

t_{PWM1H} = PWM1 high time = (DC1) x tosc

where DC1 represents the 10 bit value from PW1DCH, PW1DCL concatenated.

If DC1 = 0, then the duty cycle is zero. If t_{PWM1H} is equal to or higher than t_{PWM1P} then the duty cycle is 100%.

Similarly, PWM2 high time, t_{PWM2H} = (DC2) x tosc.

The duty cycle registers for both PWM outputs are double buffered. When the user writes to these registers they are stored in master latches. When TMR1 (or TMR2) overflows, and a new PWM period begins the master latch values are transferred to the slave latches.

Using external clock for PWM will also cause jitter in the 'duty cycle' as well as the 'period' of the PWM output. This is because external TCLK12 input is synchronized internally (sampled once per instruction cycle). Therefore, from the time TCLK12 changes to the time timer increments will vary by as much as Tcy (one instruction cycle). Therefore, both the high time and the period of the PWM output will have a jitter of ±Tcy, unless the external clock is in sync with the processor clock. The latter is the case when TCLK12 input itself is generated by the PIC17C42 (e.g. one PWM output is feedback as TCLK12).

In general therefore, when using external clock reference for PWM, its frequency should be much smaller compared to fosc.

PWM interrupts: The PWM module makes use of timer1 or timer2 interrupts. A timer interrupt is generated when TMR1 or TMR2 equals its period register and is reset to zero. This interrupt also marks the beginning of a PWM cycle. The user can write new duty cycle values before the next interrupt. The timer1 interrupt is latched into the TM1IR bit (bit4, PIR) and the timer2 interrupt is latched into the TM2IR bit (bit 5, PIR). These flags need to be cleared in software.

Using External clock: Timer1 or timer2, when used as the PWM time base, may be run off external clock only if the PWM output is being generated with 8-bit resolution or less. In this case, the PW1DCL and the PW2DCL registers must be kept at '0'. Any other value will distort the PWM output. Internal clock can be used for all resolutions. The user should also note that the maximum attainable frequency is lower. Since the maximum possible external clock input frequency for a timer is 1/(Tc + 40)ns, (see AC specs) the PWM frequency at 8-bit resolution can be, at most, 19.53 KHz (@ 25 MHz osc clock).

Timer selection for PWM2: While PWM1 always runs based on TMR1, PWM2 can run off timer1 (if bit TM2PW2 = 0, bit 5, Register PW2DCL) or timer2 (if TM2PW2 = 1). Running two different PWM outputs on two different timers allow different PWM period.

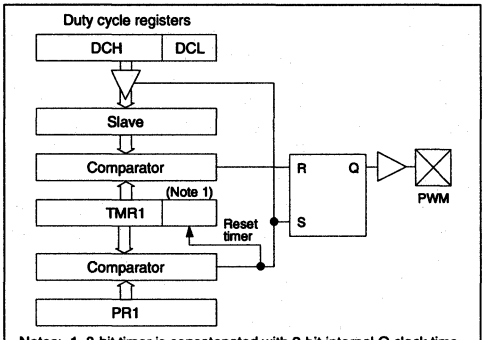
Running both PWMs off timer1 allows the best utilization of resources. If frees timer2 to operate as an 8-bit timer/counter. Timer1 and timer2 can not be used as a 16-bit timer if either PWM is being used.

Figure 9.0.1 shows a simplified block diagram of the PWM module. The duty cycle register is double buffered for a glitch free operation. Figure 10.0.2 shows how a glitch could occur if duty cycle registers are not double buffered.

Operating on duty cycle registers: For PW1DCH, PW1DCL, PW2DCH and PW2DCL registers, a write operation writes to the "master latches" while a read operation reads the "slave latches". As a result, the user may not read back what was just written to the duty cycle registers.

The user should also avoid any "read-modify-write" operations on these registers, such as: ADDWF PW1DCH, may not work as intended.

FIGURE 90.1 - SIMPLIFIED PWM BLOCK DIAGRAM

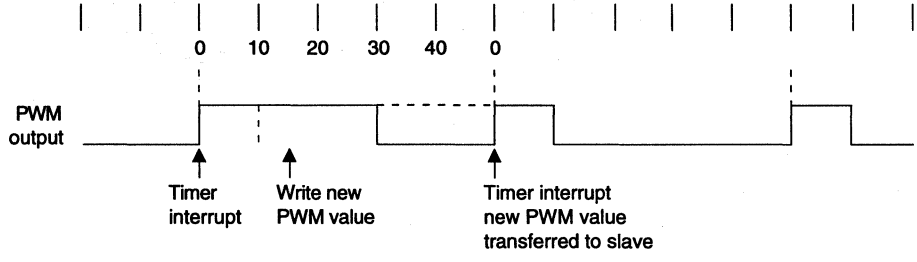


Notes: 1. 8-bit timer is concatenated with 2-bit internal Q clock time to create 10-bit time base.
2. Timer1 is used in this example.

9.1 Summary of PWM Registers

Register Name	Function	Address	Reset Value
TMR1	Timer/Counter 1	Bank 2, File 10h	xxxxxxxxb
TMR2	Timer/Counter 2	Bank 2, File 11h	xxxxxxxxb
PR1	Period Register 1	Bank 2, File 14h	xxxxxxxxb
PR2	Period Register 2	Bank 2, File 15h	xxxxxxxxb
TCON1	Timer/Capture/PWM Control Register 1	Bank 3, File 16h	00000000b
TCON2	Timer/Capture/PWM Control Register 2	Bank 3, File 17h	00000000b
PW1DCL	PWM1 duty cycle, lower 2 bits	Bank 3, File 10h	xx000000b
PW1DCH	PWM1 duty cycle, upper 8 bits	Bank 3, File 12h	xxxxxxxxb
PW2DCL	PWM2 duty cycle, lower 2 bits	Bank 3, File 11h	xx000000b
PW2DCH	PWM2 duty cycle, upper 8 bits	Bank 3, File 13h	xxxxxxxxb
PIR	Peripheral Interrupt Register	Bank 1, File 16h	00000010b
PIE	Peripheral Interrupt Enable	Bank 1, File 17h	00000000b
INTSTA (bit PEIE)	Interrupt Status Register	File 07h	00000000b
CPUSTA (bit GLINTD)	CPU Status Register	File 06h	0011xx00b

FIGURE 9.0.2 - PWM OUTPUT



Notes: 1. The dotted line shows PWM output if duty cycle registers are not double buffered. If the new duty cycle value is written after the timer has passed that value, then the PWM does not reset at all during the current cycle causing a "glitch".

2. In this example, PWM period = 50. Old duty cycle value is 30. New duty cycle value is 10.

10.0 INSTRUCTION SET

The PIC17C42 instruction set consists of 55 instructions, each single word and 16-bit wide. Most instructions operate on a file register f and the working register W (accumulator). Depending on the instruction, the result may be directed to the file register, or the working register (W) or to both.

All instructions are executed in a single instruction cycle unless otherwise noted.

Any unused op-code is executed as a NOP.

The instruction set is highly orthogonal and is grouped into

- Data Move Operations
- Arithmetic and Logical Operations
- Bit Manipulation Operations
- Program Control Operations
- Special Control Operations

Data Move Instructions

Instruction Code Binary	Hex	mnemonic		Description	Function	Status bits Affected	Notes
011p pppp ffff ffff	6pff	MOVFP	f,p	Move f to p	f → p	None	4
1011 1000 kkkk kkkk	B8kk	MOVLB	k	Move literal to BSR	k → BSR	None	
010p pppp ffff ffff	4pff	MOVPF	p,f	Move p to f	p → f	Z	4
0000 0001 ffff ffff	01ff	MOVWF	f	Move W to f	W → f	None	
1010 10ti ffff ffff	A8ff	TABLRD	t,i,f	Read data from table latch into file f, then update table latch with 16-bit contents of memory location addressed by the table pointer.	TBLATH → f if t =1, TBLATL → f if t =0; Prog Mem (TBLPTR) → TBLAT; TBLPTR + 1 → TBLPTR if i =1;	None	8,10
1010 11ti ffff ffff	ACff	TABLWT	t,i,f	Write data from file f to table latch and then Write 16-bit table latch to program memory location addressed by table pointer. It also intitiates programming if on-chip EPROM program memory is addressed.	f → TBLATH if t =1, f →TBLATL if t =0; TBLAT → Prog Mem (TBLPTR); TBLPTR + 1 → TBLPTR if i =1	None	6
1010 00tx ffff ffff	A0ff	TLRD	t,f	Read data from table latch into file f (table latch unchanged).	TBLATH → f if t =1, TBLATL → f if t =0	None	
1010 01tx ffff ffff	A4ff	TLWT	t,f	Write data from file f into table latch.	f → TBLATH if t =1, f →TBLATL if t =0	None	

Arithmetic and Logical Instructions

Instruction Code Binary	Hex	mnemonic		Description	Function	Status bits Affected	Notes
1011 0001 kkkk kkkk	B1kk	ADDLW	k	Add literal to W	(W+k) → W	OV C DC Z	
0000 111d ffff ffff	0Eff	ADDWF	f,d	ADD W to f	(W+f) → d	OV C DC Z	
0001 000d ffff ffff	10ff	ADDWFC	f,d	ADD W and Carry to f	(W+f+C) → d	OV C DC Z	
1011 0101 kkkk kkkk	B5kk	ANDLW	k	AND literal and W	(W.AND.k) → W	Z	
0000 101d ffff ffff	0Aff	ANDWF	f,d	AND W with f	(W.AND.f) → d	Z	
0010 100d ffff ffff	28ff	CLRF	f,d	Clear f and Clear d	"00h" → f, "00h" → d	None	3
0001 001d ffff ffff	12ff	COMF	f,d	Complement f	$\overline{f}$ → d	Z	
0010 111d ffff ffff	2Eff	DAW	f,d	Dec. adjust W, store in f,d	W adjusted → f and d	C	3
0000 011d ffff ffff	06ff	DECF	f,d	Decrement f	(f-1)→ d	OV C DC Z	
0001 010d ffff ffff	14ff	INCF	f,d	Increment f	(f+1) → d	OV C DC Z	
1011 0011 kkkk kkkk	B3kk	IORLW	k	Inclusive OR literal with W	(W.OR.k) → W	Z	
0000 100d ffff ffff	08ff	IORWF	f,d	Inclusive OR W with f	(W.OR.f) → d	Z	
1011 0000 kkkk kkkk	B0kk	MOVLW	k	Move literal to W	k → W	None	
0010 110d ffff ffff	2Cff	NEGW	f,d	Negate W, store in f and d	$(\overline{W}+1)$ → f, $(\overline{W}+1)$ → d	OV C DC Z	1,3
0001 101d ffff ffff	1Aff	RLCF	f,d	Rotate left through Carry	f<n>→d<n+1>, f<7>→C, C→d<0>	C	
0010 001d ffff ffff	22ff	RLNCF	f,d	Rotate left (no Carry)	f<n>→ d<n+1>, f<7>→ d<0>	None	
0001 100d ffff ffff	18ff	RRCF	f,d	Rotate right through Carry	f<n>→d<n-1>, f<0>→C, C→d<7>	C	
0010 000d ffff ffff	20ff	RRNCF	f,d	Rotate right (no Carry)	f<n>→ d<n-1>, f<0>→ d<7>	None	
0010 101d ffff ffff	2Aff	SETF	f,d	Set f and Set d	"FFh" → f, "FFh"→ d	None	3
1011 0010 kkkk kkkk	B2kk	SUBLW	k	Subtract W from literal	(k-W) → W	OV C DC Z	
0000 010d ffff ffff	04ff	SUBWF	f,d	Subtract W from f	(f-W) → d	OV C DC Z	1
0000 001d ffff ffff	02ff	SUBWFB	f,d	Subtract W from f with borrow	(f-W-c)→ d	OV C DC Z	1
0001 110d ffff ffff	1Cff	SWAPF	f,d	Swap f	f<0:3> → d<4:7>, f<4:7> → d <0:3>	None	
1011 0100 kkkk kkkk	B4kk	XORLW	k	Exclusive OR literal with W	(W.XOR.k) → W	Z	
0000 110d ffff ffff	0Cff	XORWF	f,d	Exclusive OR W with f	(W.XOR.f) → d	Z	

Program Control Instructions

Instruction Code Binary	Hex	mnemonic		Description	Function	Status bits Affected	Notes
111k kkkk kkkk kkkk	Ekkk	CALL	k	Subroutine call (within 8K page boundary)	PC+1 → TOS, k → PC<12:0>; k<12:8> → f3<4:0>, PC<15:13> → f3<7:5>	None	8
0011 0001 ffff ffff	31ff	CPFSEQ	f	Compare f/W skip if f=W	f - W, skip if f = W	None	7
0011 0010 ffff ffff	32ff	CPFSGT	f	Compare f/W skip if f>W	f - W, skip if f > W	None	2,7
0011 0000 ffff ffff	30ff	CPFSLT	f	Compare f/W skip if f<W	f - W, skip if f < W	None	2,7
0001 011d ffff ffff	16ff	DECFSZ	f,d	Decrement f, skip if 0	(f-1) → d, skip if result =0	None	7
0010 011d ffff ffff	26ff	DCFSNZ	f,d	Decrement f skip if not 0	(f-1) → d, skip if not 0	None	7
110k kkkk kkkk kkkk	Ckkk	GOTO	k	Unconditional branch (within 8K page boundary)	k → PC<12:0>, k<12:8> → f3<4:0>, PC<15:13> → f3 <7:5>	None	8
0001 111d ffff ffff	1Eff	INCFSZ	f,d	Increment f skip if 0	(f+1) → d, skip if result 0	None	7
0010 010d ffff ffff	24ff	INFSNZ	f,d	Increment f skip if not 0	(f+1) → d, skip if not 0	None	7
1011 0111 kkkk kkkk	B7kk	LCALL	k	Long Call (anywhere in 64K range)	(PC+1) → TOS; (f3) → PCH; k → PCL	None	5,8
0000 0000 0000 0101	0005	RETFIE		Return from interrupt and enable interrupt	TOS → PC (f3 unchanged) "0" → GLINTD	GLINTD	8
1011 0110 kkkk kkkk	B6kk	RETLW	k	Return literal to W	k → W, TOS → PC, f3 unchanged	None	8
0000 0000 0000 0010	0002	RETURN		Return from subroutine	TOS→ PC (f3 unchanged)	None	8
0011 0011 ffff ffff	33ff	TSTFSZ	f	Test f skip if 0	skip if f = 0	None	7

Bit Handling Instructions

Instruction Code Binary	Hex	mnemonic		Description	Function	Status bits Affected	Notes
1000 1bbb ffff ffff	8bff	BCF	f,b	Bit clear f	0 → f(b)	None	4
1000 0bbb ffff ffff	8bff	BSF	f,b	Bit set f	1 → f(b)	None	4
1001 1bbb ffff ffff	9bff	BTFSC	f,b	Bit test, skip if clear	skip if f(b) = 0	None	4,7
1001 0bbb ffff ffff	9bff	BTFSS	f,b	Bit test, skip if set	skip if f(b) = 1	None	4,7
0011 1bbb ffff ffff	3bff	BTG	f,b	Bit Toggle f	$\overline{f(b)}$ → f(b)	None	4

Special control instructions

Instruction Code Binary	Hex	mnemonic	Description	Function	Status bits Affected	Notes
0000 0000 0000 0100	0004	CLRWDT	Clear Watchdog Timer	0 → WDT, 0 → WDT prescaler, 1 → $\overline{PD}$, 1 → $\overline{TO}$	$\overline{PD}$, $\overline{TO}$	
0000 0000 0000 0000	0000	NOP	No operation	None	None	
0000 0000 0000 0011	0003	SLEEP	Enter "sleep" mode	Stop oscillator,"power down" 0 → WDT, 0 → WDT prescaler, 1 → $\overline{TO}$, 1 → $\overline{PD}$	$\overline{PD}$, $\overline{TO}$	

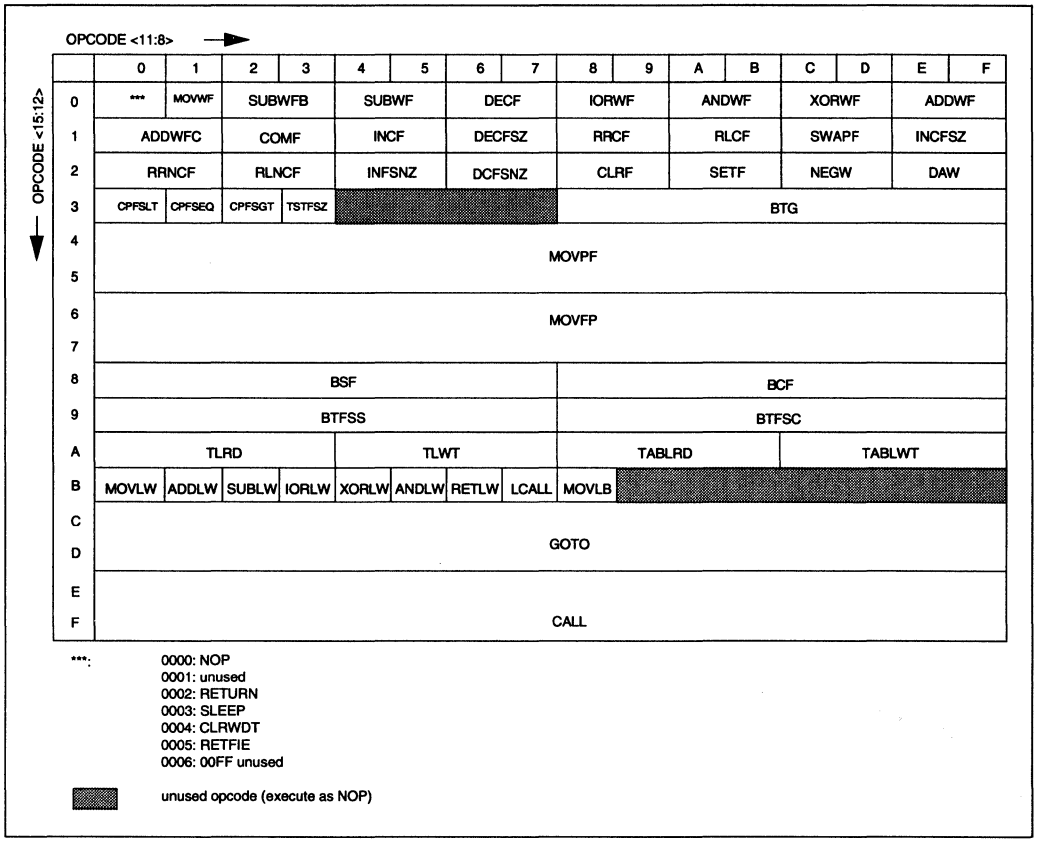
Legend:

f	register file address (00h to FFh)
p	peripheral register file address (00h to 1Fh)
b	bit address with in 8 bit file register
i	table pointer control i = 0: do not change i = 1: increment after instruction execution
t	table byte select t = 0: perform operation on lower byte t = 1: perform operation on upper byte
k	literal field (constant data)
x	don't care
d	destination select; d=0 store result in W (f0A) d=1 store result in file register 'f'
C,DC,Z,OV	ALU status bits Carry, Digit Carry, Zero, Overflow
$\overline{TO}$, $\overline{PD}$	CPU status bits Time-out and Power-down
GLINTD	GLobal Interrupt Disable bit (bit 4, CPUSTA)
W	W-register
PC	Program counter
TBLPTR	Table Pointer (16 bit)
TBLAT	Table Latch (16 bit) consists of high byte (TBLATH) and low byte (TBLATL)
TBLATL	Table latch low byte
TBLATH	Table latch high byte
WDT	Watchdog timer
BSR	Bank Select Register
TOS	Top of Stack

Notes:

1) 2's Complement method.
2) Unsigned arithmetic
3) If d=1, only the file is affected; If d=0, both W and the file are affected; If only W is required to be affected, then f=0Ah (File 0Ah) must be defined.
4) The HEX representation is not accurate. The value of the bit to be modified has to be incorporated into the third digit.
5) During an LCALL, the contents of file 03h are loaded into the MSB of the PC and kkkk kkkk is loaded into file 02h the LSB of the PC.
6) Multiple cycle instruction for EPROM programming when table pointer selects internal EPROM. The instruction is terminated by an interrupt event.
   When writing to external program memory, it is a two cycle instruction.
7) Two cycle instructions when condition is true, else single cycle instruction.
8) Two cycle instruction except for TABLRD to f02h (Program Counter low byte) in which case it takes 3 cycles.
9) A 'skip' means that instruction fetched during execution of current instruction is not executed. Instead a 'NOP' is executed.
10) Any instruction that writes to PCL (f02) is a two cycle instruction, execpt for TABLRD to f02 is a 3 cycle instruction.

FIGURE 10.0.1 - INSTRUCTION DECODE MAP



10.1 Special Function Registers as Source/ Destination

PIC17C42's orthogonal instruction set allows read and write of all file registers, including special function registers such as PC and status registers. There are some special situations the user should be aware of:

ALUSTA as destination (file 04h): If an instruction writes to ALUSTA, the Z, C, DC and OV bits may be set or reset as a result of the instruction and overwrite the original data bits written. For example, executing CLRF 04 will clear register 04, and then set Z bit leaving 00000100b first in the register.

PCL as source or destination (file 02h): Read, write or read-modify-write on PCL (f02) have the following results:

Read PCL (f02):	PCH → PCLATH; PCL → d
Write PCL (f02):	PCLATH → PCH; 8 bit destination value → PCL
Read-Modify-Write:	PCL → ALU operand PCLATH → PCH; 8 bit result → PCL

Where PCH = program counter high byte (not a addressable register), PCLATH = Program counter high holding latch (file f03), d = destination, W or f.

Bit Manipulation

All bit manipulation instructions are done by first reading the entire register, operating on the selected bit and writing the result back (read-modify-write). The user should keep this in mind when operating on special function registers, such as ports.

10.2 Instruction Description

ADDLW Add literal to W

Syntax: ADDLW k

Encoding:	1011	0001	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W + k) → W

Status bits: OV, C, DC, Z

Description: The contents of the W register are added to the 8-bit literal "k" and the result is placed in the W register.

ADDWF ADD W to f

Syntax: ADDWF f,d

Encoding:	0000	111d	ffff	ffff

Words: 1

Cycles: 1

Operation: (W + f) → d

Status bits: OV, C, DC, Z

Description: Add the contents of the W register to data memory location "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored in data memory location "f".

ADDWFC ADD W and Carry to f

Syntax: ADDWFC f,d

Encoding:	0001	000d	ffff	ffff

Words: 1

Cycles: 1

Operation: (W + f + C) → d

Status bits: OV, C, DC, Z

Description: Add the W register and the Carry Flag to data memory location "f". If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed in data memory location "f".

ANDLW AND literal and W

Syntax: ANDLW k

Encoding:	1011	0101	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .AND. k) → W

Status bits: Z

Description: The contents of W register are AND'ed with the 8-bit literal "k". The result is placed in the W register.

ANDWF AND W with f

Syntax: ANDWF f,d

Encoding:	0000	101d	ffff	ffff

Words: 1

Cycles: 1

Operation: (W .AND. f) → d

Status bits: Z

Description: AND the W register with data memory location "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored in data memory location "f".

BCF Bit Clear f

Syntax: BCF f,b

Encoding:	1000	1bbb	ffff	ffff

Words: 1

Cycles: 1

Operation: 0 → f(b)

Status bits: None

Description: Bit "b" in data memory location "f" is reset to 0.

BSF Bit Set f

Syntax: BSF f,b

Encoding:	1000	0bbb	ffff	ffff

Words: 1

Cycles: 1

Operation: 1 → f(b)

Status bits: None

Description: Bit "b" in data memory location "f" is set to 1.

BTFSC Bit test, skip if clear

Syntax: BTFSC f,b

Encoding:	1001	1bbb	ffff	ffff

Words: 1

Cycles: 1(2)

Operation: skip if f(b) = 0

Status bits: None

Description: If bit "b" in data memory location "f" is "0" then the next instruction is skipped.

If bit "b" is "0", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a two-cycle instruction.

BTFSS Bit test, skip if set

Syntax: BTFSS f,b

Encoding:	1001	0bbb	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: skip if f(b) = 1

Status bits: None

Description: If bit "b" in data memory location "f" is "1" then the next instruction is skipped.

If bit "b" is "0", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a two-cycle instruction.

BTG Bit Toggle f

Syntax: BTG f,b

Encoding:	0011	1bbb	ffff	ffff

Words: 1

Cycles: 1

Operation: f(b) → f(b)

Status bits: None

Description: Bit "b" in data memory location "f" is inverted.

CALL Subroutine Call

Syntax: CALL k

Encoding:	111k	kkkk	kkkk	kkkk

Words: 1

Cycles: 2

Operation: PC + 1 → TOS, k → PC<12:0>, k<12:8> → PCLATH<4:0>; PC<15:13> →PCLATH<7:5>

Status bits: None

Description: Subroutine call within 8K page. First, return address (PC + 1) is pushed into the stack. The thirteen bit value is loaded into PC bits <12:0>. Then the upper-eight bits of the PC are copied into PCLATH (f03). CALL is a two-cycle instruction.

CLRF Clear f and Clear d

Syntax: CLRF f,d

Encoding:	0010	100d	ffff	ffff

Words: 1

Cycles: 1

Operation: 00h → f, 00h → d

Status bits: None

Description: The contents of data memory location "f" are set to 0. If "d" is 0 the contents of both data memory location "f" and W register are set to 0. If "d" is 1 the only contents of data memory location "f" are set to 0.

CLRWDT Clear Watchdog Timer

Syntax: CLRWDT

Encoding:	0000	0000	0000	1000

Words: 1

Cycles: 1

Operation: 00h →$\overline{\text{WDT}}$, 0 → $\overline{\text{WDT}}$ prescaler,

Status bits: 1 → $\overline{\text{TO}}$, 1 → $\overline{\text{PD}}$

Description: CLRWDT instruction resets the watchdog timer.It also resets the prescaler of the WDT. Status bits $\overline{\text{TO}}$ and $\overline{\text{PD}}$ are set.

COMF Complement f

Syntax: COMF f,d

Encoding:	0001	001d	ffff	ffff

Words: 1

Cycles: 1

Operation: f → d

Status bits: Z

Description: The contents of data memory location "f" are complemented.If "d" is 0 the result is stored in W. If "d" is 1 the result is stored in data memory location "f".

2

CPFSEQ Compare f with W, skip if f = W

Syntax: CPFSEQ f

Encoding:

0011	0001	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: f - W, skip if f = W

Status bits: None

Description: If the contents of data memory location "f" are equal to the contents of the W register, the next instruction is skipped.

If f = W then the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a two-cycle instruction.

CPFSGT Compare f with W, skip if f > W

Syntax: CPFSGT f

Encoding:

0011	0010	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: f - W, skip if f > W (unsigned comparison)

Status bits: None

Description: If the contents of data memory location "f" are greater than the contents of the W register, the next instruction, is skipped. The subtraction is unsigned.

If f > W then the next instruction, fetched during the current instruction execution, is discarded. A NOP is executed instead making this a two-cycle instruction.

CPFSLT Compare f with W, skip if f< W

Syntax: CPFSLT f

Encoding:

0011	0000	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: f - W, skip if f < W (unsigned)

Status bits: None

Description: If the contents of data memory location "f" are less than the contents of the W register, the next instruction is skipped. The subtraction is unsigned.

If f < W then the next instruction, fetched during the current instruction execution, is discarded. A NOP is executed instead making this a two-cycle instruction.

DAW Decimal Adjust W Register

Syntax: DAW f,d

Encoding:

0010	111d	ffff	ffff

Words: 1

Cycles: 1

Operation: if [W<3:0> >9] .OR. [DC = 1]
then W<3:0> + 6 → f<3:0>, d<3:0>;
if [W<7:4> >9] .OR. [C = 1] then
W<7:4> + 6 → f<7:4>, d<7:4>;

Status bits: C

Description: DAW adjusts the eight bit value in the W register resulting from the earlier addition of two variables (each in packed BCD format) and produces a correct packed BCD result. If "d" is 0 the result is placed in the W register and data memory location "f". If "d" is 1 the result is placed only in data memory location "f".

The Decimal Adjust Algorithm is as follows:

Step 1: If the lower nibble of W is greater than nine, or if the DC flag (Digit Carry) is set from previous operations, then 06h is added to W.

Step 2: If upper nibble is greater than nine, or if C flag (Carry) is set following Step 1 operation, 60h is added to W.

The Carry flag may be set as a result of Step 1 or Step 2 operation.

DECF Decrement f

Syntax: DECF f,d

Encoding:

0000	011d	ffff	ffff

Words: 1

Cycles: 1

Operation: (f-1) → d

Status bits: OV, C, DC, Z

Description: Decrement data memory location "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored in data memory location "f".

DECFSZ Decrement f, skip if 0

Syntax: DECFSZ f,d

Encoding:

0001	011d	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: (f - 1) → d; skip if result = 0

Status bits: None

Description: The contents of data memory location "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed in data memory location "f". If the result is 0 the next instruction is skipped.

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

DCFSNZ Decrement f, skip if not 0

Syntax: DCFSNZ f,d

Encoding:

0010	011d	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: (f-1) → d, skip if not 0

Status bits: None

Description: The contents of data memory location "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed in data memory location "f".

If the result is not 0, the next instruction, fetched during the current instruction execution is discarded. A NOP is executed instead making this a two-cycle instruction.

GOTO Unconditional Branch

Syntax: GOTO k

Encoding:

110k	kkkk	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → PC<12:0>; k<12:8> → f3<4:0>, PC<15:13> → f3<7:5>

Status bits: None

Description: GOTO allows an unconditional branch anywhere within an 8K page boundary. The thirteen bit immediate value is loaded into PC bits <12:0>. Then the upper eight bits of PC are loaded into PCLATH (file 3). GOTO is always a two-cycle instruction.

INCF Increment f

Syntax: INCF f,d

Encoding:

0001	010d	ffff	ffff

Words: 1

Cycles: 1

Operation: (f + 1) → d

Status bits: OV, C, DC, Z

Description: The contents of data memory location "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is place in data memory location "f".

INCFSZ Increment f, skip if 0

Syntax: INCFSZ f,d

Encoding:

0001	111d	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: (f+1) → d, skip if result = 0

Status bits: None

Description: The contents of data memory location "f" are incremented. If "d" is 0 the result is placed in the W register.

If "d" is 1 the result is placed in data memory location "f". If the result is 0 the next instruction is skipped. If the result is 0 the next instruction, fetched during the current instruction execution, is discarded. A NOP is executed instead making this the two-cycle case.

INFSNZ Increment f, skip if not 0

Syntax: INFSNZ f,d

Encoding:

0010	010d	ffff	ffff

Words: 1

Cycles: 1(2)

Operation: (f+1) → d, skip if not 0

Status bits: None

Description: The contents of data memory location "f" are incremented. If "d" is 0 the result is placed in the W register.

If "d" is 1 the result is placed in data memory location "f". If the result is not 0 the next instruction, fetched during the current instruction execution, is discarded. A NOP is executed instead making this a two-cycle instruction.

2

IORLW Inclusive OR literal with W

Syntax: IORLW k

Encoding:	1011	0011	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .OR. k) → W

Status bits: Z

Description: The contents of the W register are inclusively OR'ed with the eight bit literal "k". The result is placed in the W register.

IORWF Inclusive OR W with f

Syntax: IORWF f,d

Encoding:	0000	100d	ffff	ffff

Words: 1

Cycles: 1

Operation: (W .OR. f) → d

Status bits: Z

Description: Inclusive OR the W register with data memory location "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored in data memory location "f".

LCALL Long Call

Syntax: LCALL k

Encoding:	1011	0111	kkkk	kkkk

Words: 1

Cycles: 2

Operation: PC+1 → TOS;
k → PCL, (PCLATH) → PCH

Status bits: None

Description: LCALL allows unconditional subroutine call to anywhere within the 64k program memory space. First, the return address (PC+1) is pushed onto the stack. A 16-bit destination address is then loaded into the program counter. The lower 8-bits of the destination address is embedded in the instruction. The upper 8-bits of PC is loaded from PC high holding latch, PCLATH. LCALL is a two-cycle instruction.

Example:
```
MOVLW   56h         ; W = 56h
MOVPF   W,PCLATH    ; PCLATH = 56h
LCALL   3Ah         ; CALL 563Ah
```

MOVFP Move f to p

Syntax: MOVFP f,p

Encoding:	011p	pppp	ffff	ffff

Words: 1

Cycles: 1

Operation: f → p

Status bits: None

Description: Move data from data memory location "f" to data memory location "p". Location "f" can be anywhere in the 256 word data space (00h to FFh) while "p" can be 00h to 1Fh.

Either "p" or "f" can be the W register (a useful special situation).

MOVFP is particularly useful to transfer a data memory location to a peripheral register (such as the transmit buffer or an I/O port). Both "f" and "p" can be indirectly addressed.

MOVLB Move Literal to BSR

Syntax: MOVLB k

Encoding:	1011	1000	kkkk	kkkk

Words: 1

Cycles: 1

Operation: k → BSR

Status bits: None

Description: The constant is loaded in Bank Select Register (BSR, 0Fh). Only the low 4 bits of the Bank Select Register are physically implemented.

MOVLW Move Literal to W

Syntax: MOVLW k

Encoding:

1011	0000	kkkk	kkkk

Words: 1

Cycles: 1

Operation: k → W

Status bits: None

Description: The eight bit literal "k" is loaded into W register.

MOVPF Move p to f

Syntax: MOVPF p,f

Encoding:

010p	pppp	ffff	ffff

Words: 1

Cycles: 1

Operation: p → f

Status bits: Z

Description: Move data from data memory location "p" to data memory location "f". Location "f" can be anywhere in the 256 byte data space (00h to FFh) while "p" can be 00h to 1Fh.

Either "p" or "f" can be the W register (an useful special situation)

MOVPF is particularly useful for transferring a peripheral register (e.g. the timer or an I/O port) to a data memory location.

MOVWF Move W to f

Syntax: MOVWF f

Encoding:

0000	0001	ffff	ffff

Words: 1

Cycles: 1

Operation: $\overline{W}$ → f

Status bits: None

Description: Move data from W register to data memory location "f". Location "f" can be anywhere in the 256 word data space.

NEGW Negate W

Syntax: NEGW f,d

Encoding:

0010	110d	ffff	ffff

Words: 1

Cycles: 1

Operation: $\overline{W}$ + 1 → f; $\overline{W}$ + 1 → d

Status bit: OV, C, DC, Z

Description: The contents of the W register are negated using two's complement. If "d" is 0 the result is placed in W register and data memory location "f". If "d" is 1 the result is placed only in data memory location "f".

NOP No Operation

Syntax: NOP

Encoding:

0000	0000	0000	0000

Words: 1

Cycles: 1

Operation: No operation

Status bits: None

Description: No operation

RETFIE Return from Interrupt

Syntax: RETFIE

Encoding:

0000	0000	0000	0101

Words: 1

Cycles: 2

Operation: TOS → PC, 0 → GLINTD; PCLATH (f3) is unchanged

Status bits: GLINTD

Description: Return from Interrupt. Stack is popped and Top of the Stack (TOS) is loaded in PC. Interrupts are enabled by clearing GLINTD bit. GLINTD is global interrupt disable bit (bit 4, register CPUSTA). This is a two cycle instruction.

RETLW Return Literal to W

Syntax: RETLW k

Encoding:	1011	0110	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → W; TOS → PC;
PCLATH (f03) is unchanged

Status bits: None

Description: The W register is loaded with the eight bit literal "k". The program counter is loaded from the top of the stack (the return address). The high address latch (PCLATH) remains unchanged. This is a two-cycle instruction.

RETURN Return from Subroutine

Syntax: RETURN

Encoding:	0000	0000	0000	0010

Words: 1

Cycles: 2

Operation: TOS → PC;
PCLATH (f3) is unchanged

Description: Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

RLCF Rotate Left f through Carry

Syntax: RLCF f,d

Encoding:	0001	101d	ffff	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n+1>; f<7> → C; C → d<0>

Status bits: C

Description: The contents of data memory location "f" are rotated one bit to the left through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is stored back in data memory location "f".

RLNCF Rotate Left f (no carry)

Syntax: RLNCF f,d

Encoding:	0010	001d	ffff	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n+1>; f<7> → d<0>

Status bits: None

Description: The contents of data memory location "f" are rotated one bit to the left. If "d" is 0 the result is placed in the W register . If "d" is 1 the result is stored back in data memory location "f".

RRCF Rotate Right f through Carry

Syntax: RRCF f,d

Encoding:	0001	100d	ffff	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n-1>; f<0> → C; C → d<7>

Status bits: C

Description: The contents of data memory location "f" are rotated one bit to the right through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed in data memory location "f".

RRNCF Rotate Right f (no carry)

Syntax: RRNCF f,d

Encoding:	0010	000d	ffff	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n-1>; f<0> → d<7>

Status bits: None

Description: The contents of data memory location "f" are rotated one bit to the right. If "d"is 0 the result is placed in the W register. If "d" is 1 the result is placed in data memory location "f".

SETF Set f and Set d

Syntax: SETF f,d

Encoding:

0010	101d	ffff	ffff

Words: 1

Cycles: 1

Operation: FFh → f, FFh → d

Status bits: None

Description: If "d" is 0 both the data memory location "f" and W register are set to FFh. If "d" is 1 the only the data memory location "f" is set to FFh.

SLEEP

Syntax: SLEEP

Encoding:

0000	0000	0000	0011

Words: 1

Cycles: 1

Operation: 0 → $\overline{PD}$; 1 → $\overline{TO}$
00h → WDT; 0 → WDT prescaler

Status bits: $\overline{TO}$, $\overline{PD}$

Description: The power down status bit ($\overline{PD}$) is cleared. Time-out status bit ($\overline{TO}$) is set. Watchdog Timer and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP mode for more details.

SUBLW Subtract W from literal

Syntax: SUBLW k

Encoding:

1011	0010	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (k - W) → W

Status bits: OV, C, DC, Z

Description: The contents of the W register are subtracted from the 8-bit literal "k". The result is placed in the W register.

SUBWF Subtract W from f

Syntax: SUBWF f,d

Encoding:

0000	010d	ffff	ffff

Words: 1

Cycles: 1

Operation: (f-W) → d

Status bits: OV,C, DC, Z

Description: Subtract (2's complement method) the W register from data memory location "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in data memory location "f".

SUBWFB Subtract W from f with Borrow

Syntax: SUBWFB f,d

Encoding:

0000	001d	ffff	ffff

Words: 1

Cycles: 1

Operation: (f-W-C) → d

Status bits: OV, C, DC, Z

Description: Subtract (2's complement method) the W register and the carry flag (borrow) from data memory location "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored in data memory location "f".

SWAPF Swap f

Syntax: SWAPF f,d

Encoding:

0001	110d	ffff	ffff

Words: 1

Cycles: 1

Operation: f<0:3> → d<4:7>, f<4:7> → d<0:3>

Status bits: None

Description: The upper and lower nibbles of data memory location "f" are exchanged. If "d" is 0 the result is placed in W register. If "d" is 1 the result is place in data memory location "f".

TABLRD Table Read

Syntax: TABLRD t,i,f

Encoding:

1010	10ti	ffff	ffff

Words: 1

Cycles: 2 (3 cycle if f = 02h [PC])

Operation: If t = 1 then TBLATH → f
else if t = 0 TBLATL → f;
Prog Mem (TBLPTR) → TBLAT;
if i = 1 then TBLPTR + 1 → TBLPTR

Status bits: None

Description: First, either the low byte (if t = 0) or the high byte (if t = 1) of the table latch (TBLAT) is moved to register file "f".

Then the contents of the program memory location pointed to by the 16-bit Table Pointer (TBLPTR) is loaded into the 1-bit Table Latch (TBLAT). Finally table pointer is incremented if i = 1.

Example:

```
MOVLW   12h          ;
MOVPF   W, TBLPTRH   ;
MOVLW   34h          ;
MOVPF   W,TBLPTRL    ; TBLPTR = 1234h
TABLRD  0, 1, 50h    ; TBLAT = Prog Mem
                     ; (1234h)
                     ; TBLPTR = 1235h
TLRD    0, 50h       ; low byte → 50h
TABLRD  1,1, 51h     ; high byte → 51h
                     ; TBLAT = Prog Mem
                     ; (1235h)
                     ; TB1.PTR = 1236h
TLRD    0, 52h       ; low byte → 52h
TLRD    1, 53h       ; high byte → 53h
```

TABLWT Table write

Syntax: TABLWT t, i, f

Encoding:

1010	11ti	ffff	ffff

Words: 1

Cycles: 2 (Many if write is to on-chip EPROM program memory)

Operation: if t = 0 then f → TBLATL
else if t = 1 then f → TBLATH;
TBLAT → Prog Mem (TBLPTR);
if i = 1 then TBLPTR + 1 → TBLPTR;

Description: First, contents of file register f is loaded in the low byte (if t = 0) or high byte (if t = 1) of Table Latch, TBLAT.

If TBLPTR points to external program memory location then the contents of TBLAT is written to it and the instruction takes 2 cycles.

If TBLPTR points to an internal EPROM location, then an EPROM write (program) sequence is initiated. It is terminated when an interrupt is received.

If the Global Interrupt Disable bit (GLINTD) is set, the interrupt will complete the TABLWT, but no interrupt sequence will be invoked. If GLINTD = 0, then interrupt will be acknowledged following the TABLWT.

For an interrupt to end programming, its corresponding mask bit must enable the interrupt. If the terminating interrupt is INTIR, RTCIR or RTXIR, the flag bit is automatically cleared. The clearing takes place for both short and long table writes. The user can protect against accidental clearing of an interrupt flag due to a TABLWT instruction by masking off the above mentioned interrupts before doing table write operations.

$\overline{\text{MCLR}}/V_{PP}$ pin must be at programming voltage for successful programming. If $\overline{\text{MCLR}}/V_{PP} = V_{CC}$ then the programming sequence will be executed, but will not be successful (although the location may be disturbed).

TLRD Table Latch Read

Syntax: TLRD t,f

Encoding:

1010	00tx	ffff	ffff

x= don't care

Words: 1

Cycles: 1

Operation: if (t = 0) thenTBLATL → f else if (t = 1) then TBLATH → f

Status bits: None

Description: Read data from high byte (t = 1) or low byte (t = 0) of 16-bit Table Latch into file register "f". Table Latch is unaffected.

This instruction is used in conjunction with TABLRD to transfer data from program memory to data memory.

TLWT Table Latch Write

Syntax: TLWT t,f

Encoding:

1010	01tx	ffff	ffff

x= don't care

Words: 1

Cycles: 1

Operation: if (t=0) then f → TBLATL else if (t=1) then f → TBLATH

Status bits: None

Description: Data from file register f is written into the low byte (t = 0) or thehigh byte(t = 1) of the 16-bit Table Latch.

This instruction is used in conjunction with TABLWT, to transfer data from data memory to program memory.

TSTFSZ Test f, skip if 0

Syntax: TSTFSZ f

Encoding:

0011	0011	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: skip if f = 0

Status bits: None

Description: If the contents of data memory location "f" are 0, then the next instruction is skipped.

If "f" = 0, the next instruction, fetched during the current instruction execution, is discarded. A NOP is executed instead making this a two-cycle instruction.

XORLW Exclusive OR literal with W

Syntax: XORLW k

Encoding:

1011	0100	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .XOR. k) → W

Status bits: Z

Description: The contents of the W register are XOR'ed with the 8-bit literal "k". The result is placed in the W register.

XORWF Exclusive OR W with f

Syntax: XORWF f,d

Encoding:

0000	110d	ffff	ffff

Words: 1

Cycles: 1

Operation: (W .XOR. f) → d

Status bits: Z

Description: Exclusive OR the contents of the W register with data memory location "f". If "d" is 0, the result is stored in the W register. If "d" is 1, the result is stored in data memory location "f".

2

11.0 DEVELOPMENT SUPPORT

11.1 Development Tools

The PIC16C5X and PIC16CXX microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER™ Real-Time In-Circuit Emulator
- PRO MATE™ Universal Programmer
- PICSTART™ Low-Cost Prototype Programmer
- Assembler
- Software Simulator

11.2 PICMASTER™: High Performance Universal In-Circuit Emulator

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X, PIC16CXX and PIC17CXX families.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16C5X, PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on PC compatible machines ranging from 80286-AT® class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.1 environment, allowing the operator access to a wide range of supporting software and accessories.

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.1 environment was chosen to best make these features available to you, the end user.

The PICMASTER Emulator Universal System consists primarily of four major components:

- Host-Interface Card
- Emulator Control Pod
- Target-Specific Emulator Probe
- PC Host Emulation Control Software

The Windows 3.1 System is a multitasking operating system which will allow the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window.

Dynamic Data Exchange (DDE), a feature of Windows 3.1, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

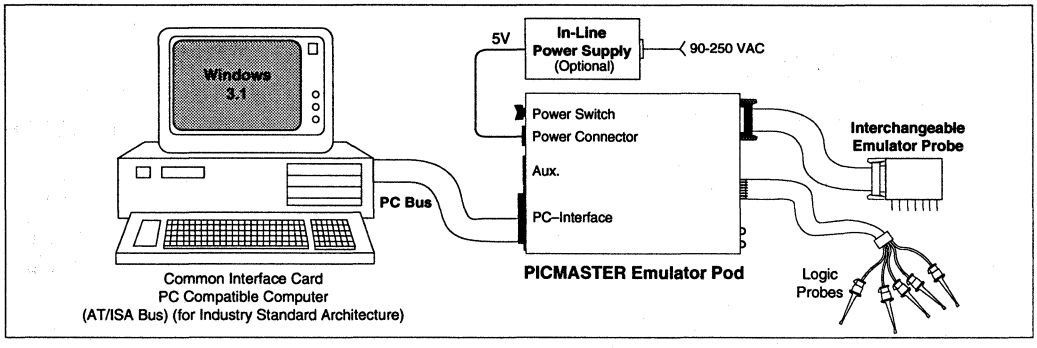
Under Windows 3.1, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16CXX processor and a PIC17CXX processor).

11.3 PRO MATE™: Universal Programmer

The PRO MATE Universal Programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MATE has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability . It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MATE can read, verify or program PIC16C5X, PIC16CXX and PIC17CXX devices. It can also set fuse configuration and code-protect in this mode. Its EEPROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.

FIGURE 11-1: PICMASTER SYSTEM CONFIGURATION



In PC-hosted mode, the PRO MATE connects to the PC via one of the COM (RS232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of V_{DD} min, V_{DD} max and V_{PP} levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different serial number, sequential or random.

The PRO MATE has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. PRO MATE supports all PIC16C5X, PIC16CXX and PIC17CXX processors.

11.4 Assembler (MPASM)

Cross Assembler is a PC hosted symbolic assembler. It supports all microcontroller series including the PIC16C5X CMOS, PIC16CXX and PIC17CXX families.

MPASM offers fully featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from the Microchip Universal Emulator System (PICMASTER).

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro Assembly Capability
- Provides Object, Listing, Symbol and special files required for debugging with one of the Microchip Emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a full feature directive language represented by four basic classes of directives:

- **Data Directives** are those that control the allocation of memory and provide a way to refer to data items symbolically, by meaningful names.
- **Listing Directives** control the MPASM listing dis play. They allow the specification of titles and subtitles, page ejects and other listing control.
- **Control Directives** permit sections of conditionally assembled code.
- **Macro Directives** control the execution and data allocation within macro body definitions.

11.5 Software Simulator (MPSIM)

The Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16C5X and PIC16CXX series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in single step, execute until break or in a trace mode. Two forms of symbolic debugging are available: an internal symbol table for disassembling opcodes and the displaying of source code from a listing file. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

11.6 Development Systems

For convenience, the development tools are packaged into comprehensive systems as listed in Table 11-1:

TABLE 11-1: DEVELOPMENT SYSTEM PACKAGES

Item	Name	System Description
1.	PICMASTER™ System	PICMASTER In-Circuit Emulator with your choice of Target Probe, PRO MATE Programmer, Assembler, Software Simulator and Samples.

20.7 Probe Specifications

The PICMASTER probes currently meet the following specifications:

PICMASTER PROBE	Devices Supported	PROBE Maximum Frequency	PROBE Operating Voltage
PROBE - 17	PIC17C42	16 MHZ	4.5V - 5.5V

12.0 ELECTRICAL CHARACTERISTICS

12.1 Absolute Maximum Ratings†

Ambient temperature under bias ..... –55°C to 125°C
Storage temperature ..... –65°C to 150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0V to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} ..... –0.6V to 12V
Voltage on RA2 and RA3 with respect to V_{SS} ..... –0.6V to 12V
Voltage on any pin with respect to V_{SS} (except V_{DD}, $\overline{MCLR}$, RA2, RA3) ..... –0.6V to V_{DD} +0.6
Maximum current into V_{DD} pin(s) total 150mA
Maximum current out of all V_{SS} pins total 150mA
Maximum current sunk by any I/O pin (except RA2, RA3) 35mA
Maximum current sunk by either RA2 or RA3 pins 60mA
Maximum current sourced by any I/O pin 20mA
Input clamp current, I_{IK} (V_I<0 or V_I>V_{DD}) ..... ±20mA
Output clamp current, I_{OK} (V0<0 or V0>V_{DD}) ..... ±20mA
Total power dissipation 1W

Notes: 1. Total power dissipation should not exceed 1 W for the package. Power dissipation is calculated as follows:

$$Pdis = V_{DD} \times \{I_{DD} - \Sigma\ Ioh\} + \Sigma\ \{(V_{DD}-Voh) \times Ioh\} + \Sigma(Vol \times Iol)$$

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. **This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied.** Exposure to maximum rating conditions for extended periods may affect device reliability.

12.2 DC CHARACTERISTICS

Operating Conditions: 4.5V ≤VDD ≤5.5V, -40°C ≤TA ≤85°C unless otherwise stated.

Characteristic	Symbol	Min	Typ†	Max	Unit	Conditions
Supply voltages and currents						
Supply Voltage	VDD	4.5	5.0	5.5	V	
Supply Current (note 1)	IDD	-	95	-	uA	VDD=4.5V,freq=32KHz
		-	3	6	mA	VDD=5.5V,freq=4MHz
		-	6	12	mA	VDD=5.5V,freq=8MHz
		-	11	24	mA	VDD=5.5V,freq=16MHz
		-	19	38	mA	VDD=5.5V,freq=25MHz
Power Down Current (notes 2,3)	IPD	-	-	20	uA	VDD=4.5V,WDT on
		-	-	20	uA	VDD=5.5V,WDT on
		-	-	5	uA	VDD=4.5V, WDT off
		-	-	5	uA	VDD=5.5V,WDT off
Programming voltage	VPP	12.5	13.0	13.5	V	
Input voltage levels & hysterisis						
All inputs except C, D and E	Vil1	-	-	0.2 VDD	V	
ports (Schmitt trigger inputs)	Vih1	0.8 VDD	-	-	V	
including OSC1 (EC, RC modes)	Vhys1	0.15 VDD*	-	-	V	
Ports C, D and E (TTL input)	Vil2	-	-	0.8	V	
	Vih2	2.0	-	-	V	
OSC1 (XT, LF modes)	Vil3	-	-	0.2VDD		
	Vih3	0.8 VDD	-	-		
Input leakage current						
All pins except MCLR,RA2,RA3	Iil1	-	-	±1	uA	VSS ≤ VPIN ≤VDD (note 4)
MCLR pin	Iil2	-	-	±2	uA	VSS≤VMCLR≤VDD
RA2,RA3 pin	Iil3	-	-	±2	uA	VSS ≤ VRA2, VRA3≤12V
MCLR pin	Iil4	-	-	10	uA	VMCLR = VPP(note 5)
Pin capacitance						
All pins except MCLR, VDD, VSS	Cin	-	10*	-	pF	
MCLR	Cmclr	-	20*	-	pF	
Output voltage levels						
RA2,RA3 (open collector)	Voh1	-	-	12.0	V	(note 6)
	Vol1	-	-	3.0	V	Iol1= 60 mA, VDD = 5.5V
PORT C, D & E (TTL)	Voh2	2.4	-	-	V	Ioh2 = -6 mA, VDD = 4.5V
	Vol2	-	-	0.4	V	Iol2 = 6 mA, VDD = 4.5V
OSC2/CLKOUT (RC & EC modes)	Voh3	2.4	-	-	V	Ioh3 = -5 mA, VDD = 4.5V
	Vol3	-	-	0.4	V	Iol3 = 3 mA, VDD = 4.5V
All Outputs except OSC2	Voh4	0.9 VDD	-	-	V	Ioh4 = -2 mA
(including C, D and E ports)	Vol4	-	-	0.1 VDD	V	Iol4 = 4 mA
Weak pull-up current (PortB)	Ipu	60	100	250	uA	Pull-up active, VPIN = VSS
RAM retention voltage	Vram	1.5*	-	-	V	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
*: Guaranteed by characterization and not tested.
**: Guaranteed by Design.

NOTE 1: Supply current is measured with PIC17C42 executing code (from internal test EPROM which is same as microcomputer mode) with all port pins configured as input and forced to VDD or VSS. External clock (rail to rail) is used. The user should note the following:
a) The code executed from test memory attempts to exercise the chip to make more realistic measurements of IDD (rather than in reset). However, depending on user's code, the current will vary.
b) The user needs to add the current consumed by output drivers driving external capacitive or resistive load. For capacitive loads, this can be estimated for an individual output pin as: (C_L VDD) f where C_L = total capacitive load, f = average frequency with which the pin switches.

The current due to external capacitance load switching is most significant during external execution.

c) The current consumed by the oscillator circuit needs to be considered as well. This will be especially significant for RC oscillator, where the current through the external pull up resistor can be estimated as: VDD/(2 R)

NOTE 2: Standby current is measured under the following conditions: Part in SLEEP, MCLR = VDD. OSC1 and OSC2 pins driven or left floating (makes no difference). All port pins configured as input and tied to VSS or VDD. Standby current is not affected by oscillator type.

NOTE 3: WDT off implies fuses FWDT1 = FWDT0 = 0 which configures the WDT as a normal timer that shuts off during SLEEP. WDT on implies that the WDT is configured as a watchdog timer (FWDT1, FWDT0 = 01, 10 or 11) which continues to run during SLEEP.

NOTE 4: With any weak pull-up disabled.

NOTE 5: When not programming

12.3 AC CHARACTERISTICS

12.3.1 AC Characteristics: OSC/Reset/System bus

Operating Conditions: 4.5V ≤VDD ≤5.5V, -40°C ≤TA ≤85°C unless otherwise stated.

Characteristic	Symbol	Min	Typ†	Max	Unit	Comments
Input clock and oscillator frequencies						
Oscillator frequency	Fosclf	DC	-	200	KHz	LF osc mode
	Foscxt	0.2	-	25	MHz	XT osc mode
RC mode frequency	Foscrc	DC	-	4	MHz	RC osc mode
Recommended limits:	R	2	-	50	Kohm	
	C	20	-	1000	pF	
External clock in frequency	Fextck	DC	-	25	MHz	EC mode (external clock)
Instruction cycle time	Tcy	-	4/Fosc	-	ns	Fosc = osc/clock-in frequency
Clock-in (OSC1) high or low time	TckHL	15*			ns	For external clock input in XT, LF or EC mode.
Clock-in (OSC1) rise or fall time	TckRF			15*	ns	For external clock input in XT, LF or EC mode.
Reset timing						
$\overline{MCLR}$ pulse width	tmcL	100*	-	-	ns	
$\overline{MCLR}$ ↓ to AD<15:0> high impedance	tmcL2adZ	-	-	100	ns	
WDT, OST, PWRT and POR timings						
WDT period	twdt	5	12	25	ms	Prescale = 1
Power up timer period	tPWRT	40	96	200	ms	
Oscillator start-up timer (OST) period	tOST	-	1024 tOSC*	-	ns	tosc = oscillator period
VDD rise time for POR to function properly	tVDDR	-	-	80*	ms	Time for VDD to rise from 0V to 4.5V (Note 1)
VDD start voltage to guarantee power on reset	VPOR	-	VSS*	-	V	See section 4.4 for details
System bus timings						
Address out valid to ALE ↓ (address setup time)	tadV2alL	0.25 Tcy-30	-	-	ns	with 100 pF load on all address/data and control (ALE,$\overline{OE}$,$\overline{WR}$) pins.
ALE ↓ to address out invalid (address hold time)	talL2adI	0	-	-	ns	
AD <15:0> high impedance to $\overline{OE}$↓	tadZ2oeL	10	-	-	ns	
$\overline{OE}$↑ to AD<15:0> driven	toeH2adD	0.25 Tcy-15	-	-	ns	
Data in valid before $\overline{OE}$↑ (data setup time)	tadV2oeH	35	-	-	ns	
$\overline{OE}$↑ to data in invalid (data hold time)	toeH2adI	0	-	-	ns	
Data out valid to $\overline{WR}$↓ (data setup time)	tadV2wrL	0.25 Tcy-40	-	-	ns	
$\overline{WR}$↑ to data out invalid (data hold time)	twrH2adI	-	0.25 Tcy**	-	ns	
ALE pulse width	talH	-	0.25 Tcy**	-	ns	
OE pulse width	toeL	0.5 Tcy-35**	-	-	ns	
$\overline{WR}$ pulse width	twrL	-	0.25 Tcy**	-	ns	
$\overline{ALE}$ ↑ to ALE ↑ (cycle time)	talH2alH	-	Tcy**	-	ns	
Capacitive load on output pins						
OSC2	COSC2	-	-	25	pF	(note 2)
ALE, $\overline{WR}$, $\overline{OE}$ and AD<15:0>	CAD	-	-	100	pF	(note 3)
All other pins, including C, D, E ports (when used as port)	CIO	-	-	50	pF	(note 3)

See footnotes on next page.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
*: Guaranteed by characterization
**: Guaranteed by design
NOTE 1: VDD must start from 0V for Power on reset to function properly. VDD rise time can be longer but then external POR circuitry will be required.
NOTE 2: In EC and RC oscillator modes when OSC2 pin is outputting CLKOUT, or in XT or LP mode when external clock is driven into OSC1 pin.
NOTE 3: All AC specs are valid for these capacitive loadings

12.3.2 AC Characteristics: Serial Port

Operating Conditions: 4.5V ≤VDD ≤5.5V, -40°C ≤TA ≤85°C unless otherwise stated.

Characteristic	Symbol	Min	Typ†	Max	Unit	Comments
SYNC XMIT (MASTER & SLAVE)						
Clock high to data out valid	tckH2dtV	-	-	65	ns	
Clock out rise time and fall time (Master Mode)	tckrf	-	-	35	ns	
Data out rise time and fall time	tdtrf	-	-	35	ns	
SYNC RCV (MASTER & SLAVE)						
Data in valid before CK ↓ (DT setup time)	tdtV2ckL	15	-	-	ns	
Data in invalid after CD ↓ (DT hold time)	tckL2dtI	15	-	-	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

12.3.3 AC Characteristics: I/O Port

Operating Conditions: 4.5V ≤VDD ≤5.5V, -40°C ≤TA ≤85°C unless otherwise stated.

Characteristic	Symbol	Min	Typ†	Max	Unit	Comments
CLKOUT ↑ to Port out valid	tckH2rxV	-	-	0.5Tcy+20	ns	note 1
Port A, B, C, D, E in valid before CLKOUT ↑ (RC and EC mode)	trxV2ckH	0.25 Tcy+25	-	-	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
NOTE 1: Timings are valid for a maximum of 50pF total capacitive load on the port pins, and CLKOUT pin.

12.3.4 AC Characteristics: TMR0 & INT

Operating Conditions: 4.5V ≤VDD ≤5.5V, -40°C ≤TA ≤85°C unless otherwise stated.

Characteristic	Symbol	Min	Typ†	Max	Unit	Comments
TMR0 in ext clock, prescale = 1						
T0CKI clock input high time	trtH1	0.5 Tcy+20**	-	-	ns	
T0CKI clock input low time	trtL1	0.5 Tcy+20**	-	-	ns	
TMR0 in ext clock, prescale > 1						
T0CKI clock input high time	trtH2	10*	-	-	ns	
T0CKI clock input low time	trtH2	10*	-	-	ns	
T0CKI clock input period	trtP	-	$\frac{Tcy+40^{**}}{N}$	-	ns	N = prescale value (2,4,8,....,256)
RA1/T0CKI pin and RA0/INT pin interrupt input						
RA1/T0CKI pin and RA0/INT pin input high time	triH	25*	-	-	ns	
RA1/T0CKI pin and RA0/INT pin input low time	triL	25*	-	-	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

* Guaranteed by characterization

** Guaranteed by design and characterization

12.3.5 AC Characteristics: Timer1, Timer2, Timer3, Capture and PWM

Operating Conditions: 4.5V ≤VDD ≤5.5V, -40°C ≤TA ≤85°C unless otherwise stated.

Characteristic	Symbol	Min	Typ†	Max	Unit	Comments
Timer1, Timer2, Timer3						
Input clock high time on pins TCLK12, TCLK3	tcH	0.5Tcy+20**	-	-	ns	
Input clock low time on pins TCLK12, TCLK3	tcL	0.5Tcy+20**	-	-	ns	
Capture1, Capture2						
Input high time on RB0/CAP1, RB1/CAP2	tcpH	10*	-	-	ns	
Input low time on RB0/CAP1, RB1/CAP2	tcpL	10*	-	-	ns	
Input period on RB0/CAP1, RB1/CAP2	tcpL	$\frac{2\ Tcy\ **}{N}$	-	-	ns	where N=capture prescale (1, 4, 16)

12.3.6 AC TEST LOAD AND TIMING CONDITIONS

FIGURE 12.3.6.1 - INPUT LEVEL CONDITIONS

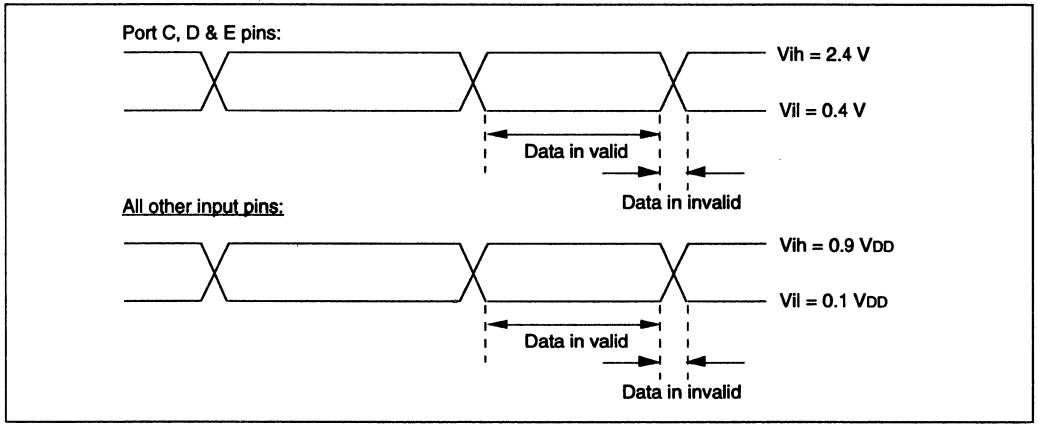


FIGURE 12.3.6.2 - OUTPUT LEVEL CONDITIONS

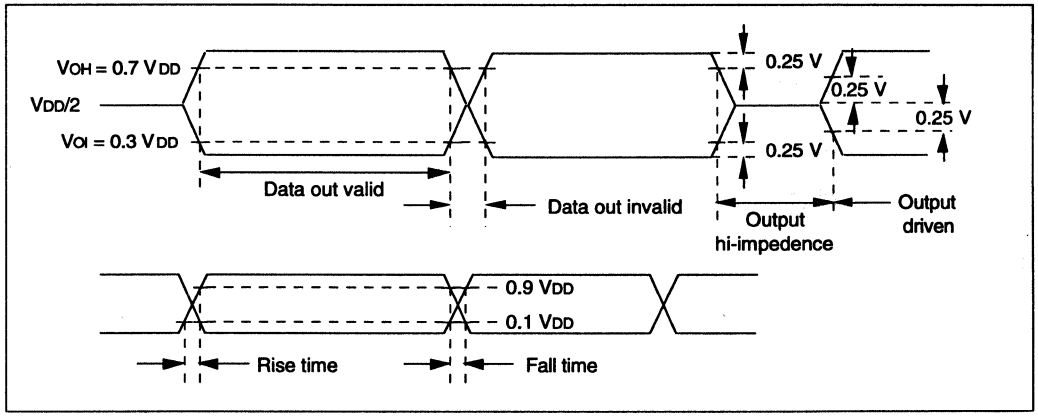
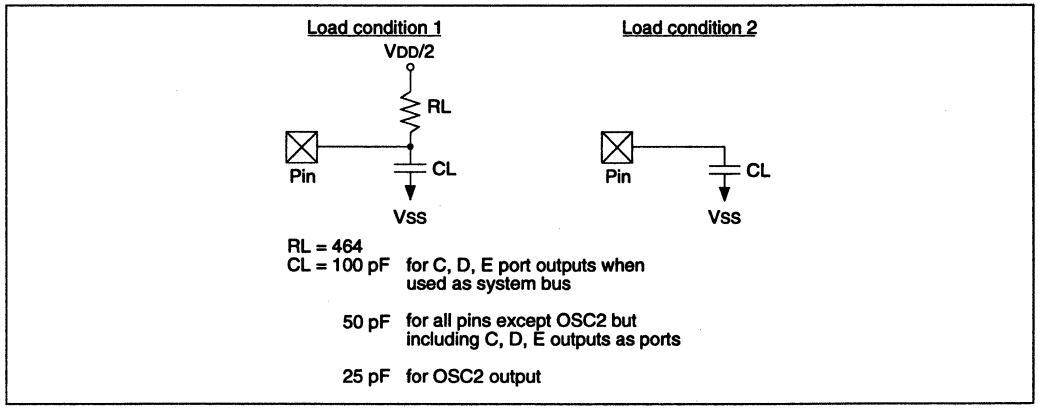
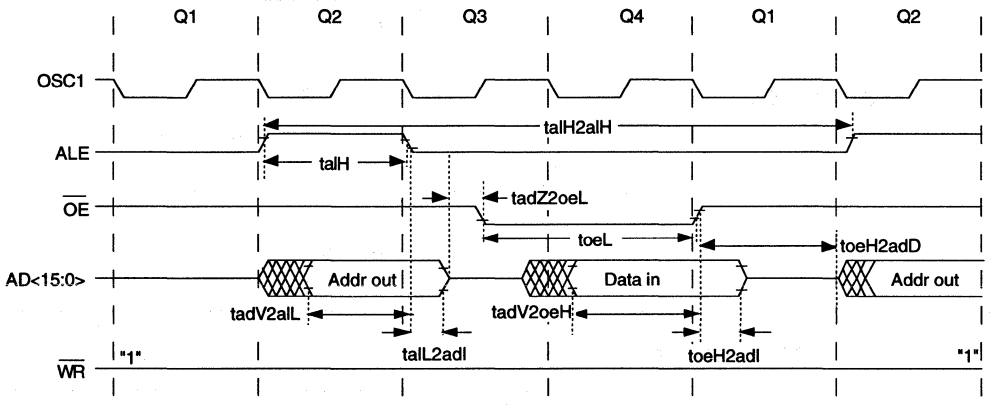


FIGURE 12.3.6.3 - LOAD CONDITIONS



12.4 TIMING DIAGRAMS

FIGURE 12.4.1 - TIMING DIAGRAM - EXTERNAL PROGRAM MEMORY READ



tadV2alL	= AD <15:0> (address) valid to ALE ↓; address setup time
talL2adl	= ALE ↓ to AD<15:0> (address) invalid; address hold time
tadZ2oeL	= AD <15:0> high impedance to $\overline{OE}$ ↓
toeH2adD	= $\overline{OE}$ ↑ to AD <15:0> driven (address out)
tadV2oeH	= AD <15:0> (data) valid to $\overline{OE}$ ↑; data setup time
toeH2adl	= $\overline{OE}$ ↑ to AD <15:0> (data) invalid; data hold time
talH	= ALE pulse width
toeL	= $\overline{OE}$ pulse width
talH2alH	= ALE ↑ to ALE ↑; bus cycle period

FIGURE 12.4.2 - TIMING DIAGRAM - EXTERNAL PROGRAM MEMORY WRITE

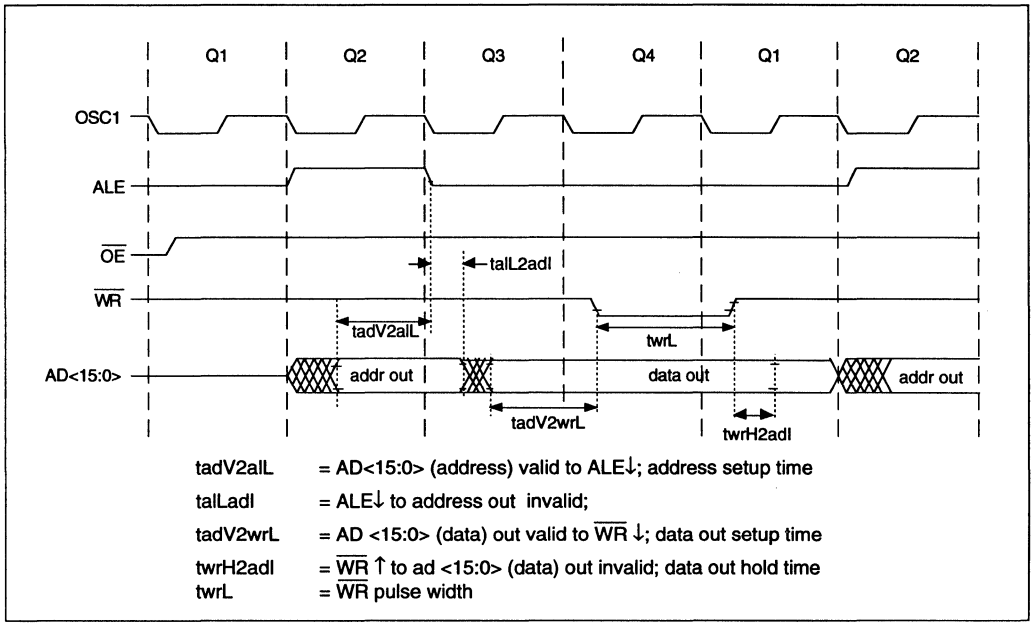


FIGURE 12.4.3 - TIMING DIAGRAM - INTERRUPT TIMING

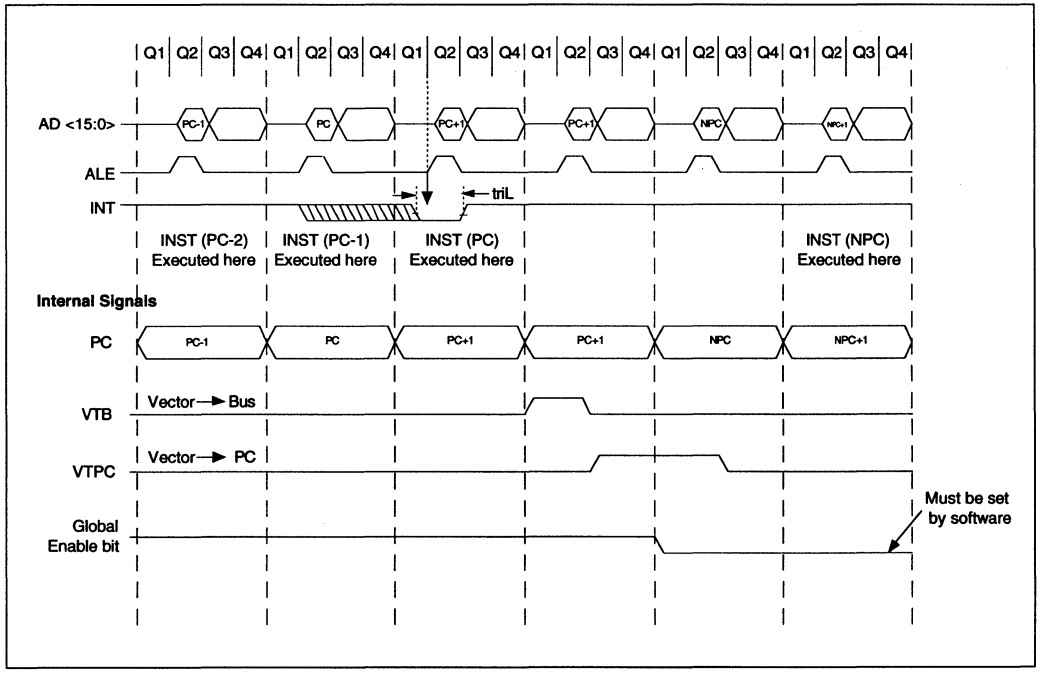


FIGURE 12.4.4 - RESET TIMING

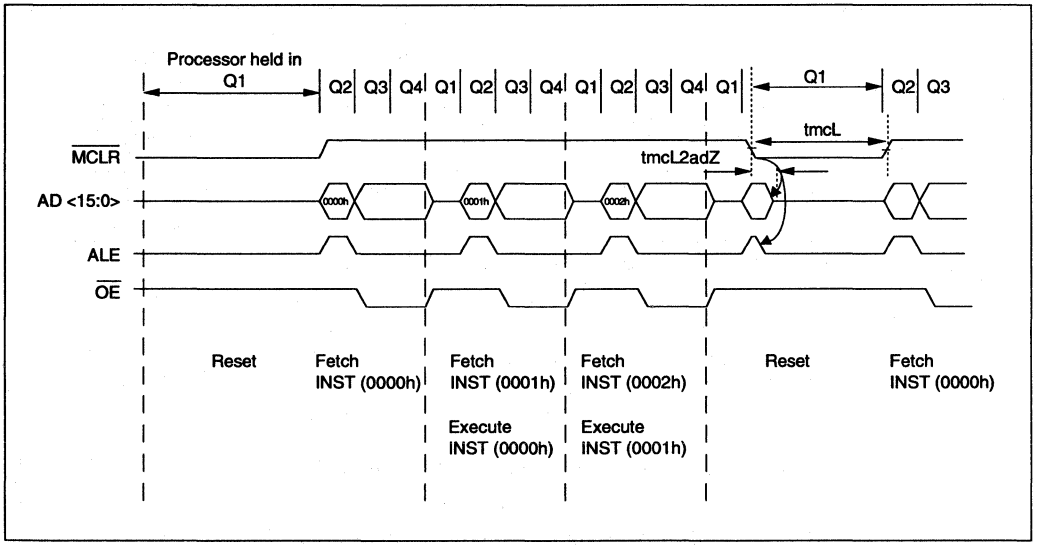


FIGURE 12.4.5 - TABLRD TIMING

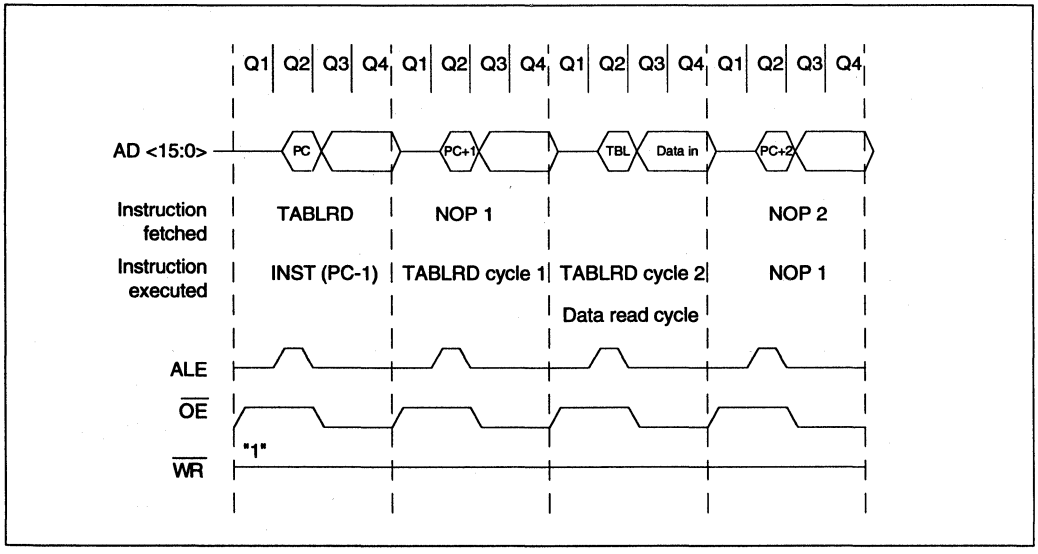


FIGURE 12.4.6 - TABLRD TIMING (CONSECUTIVE TABLRD INSTRUCTIONS)

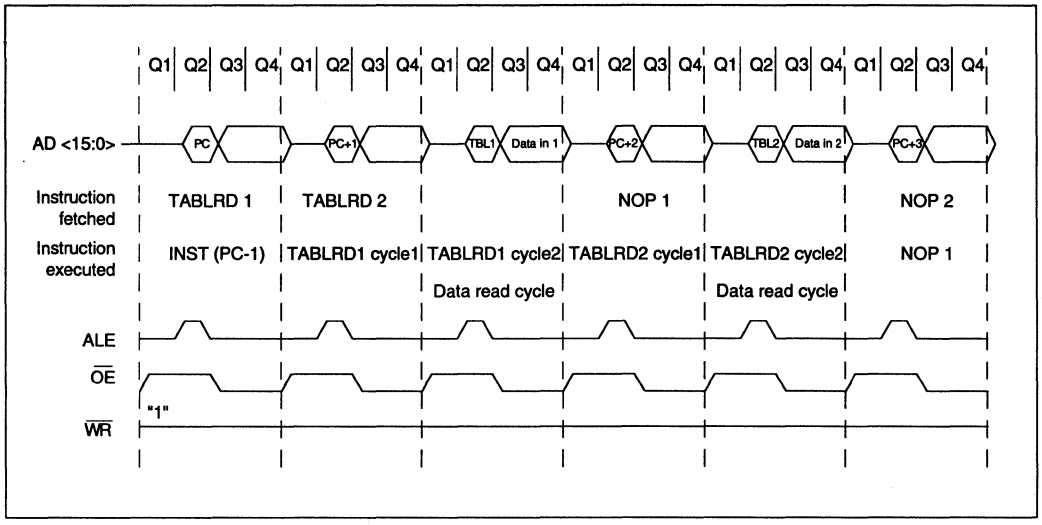


FIGURE 12.4.7 - TABLWT TIMING

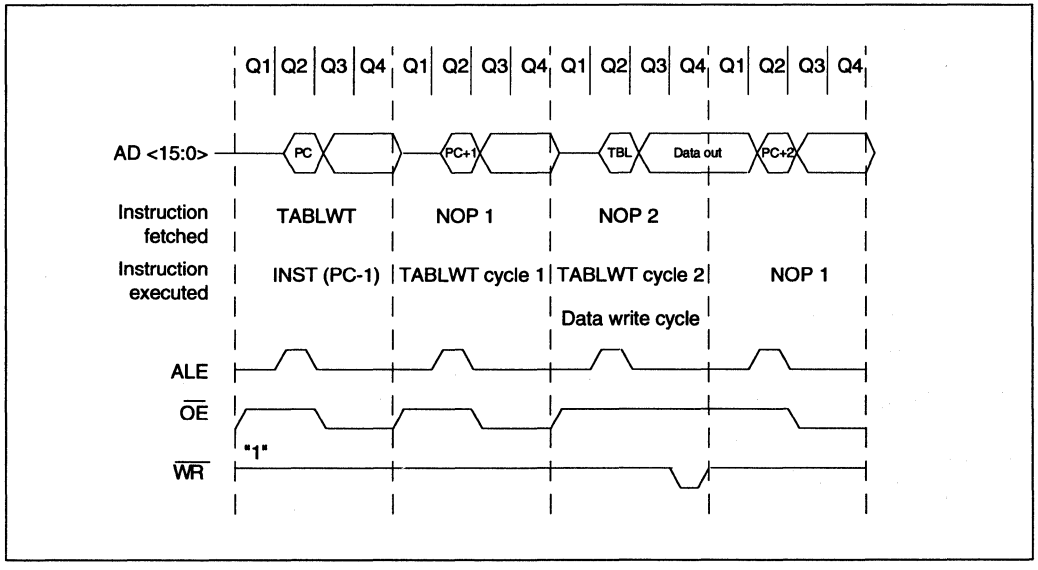


FIGURE 12.4.8 - TABLWT TIMING (CONSECUTIVE TABLWT INSTRUCTIONS)

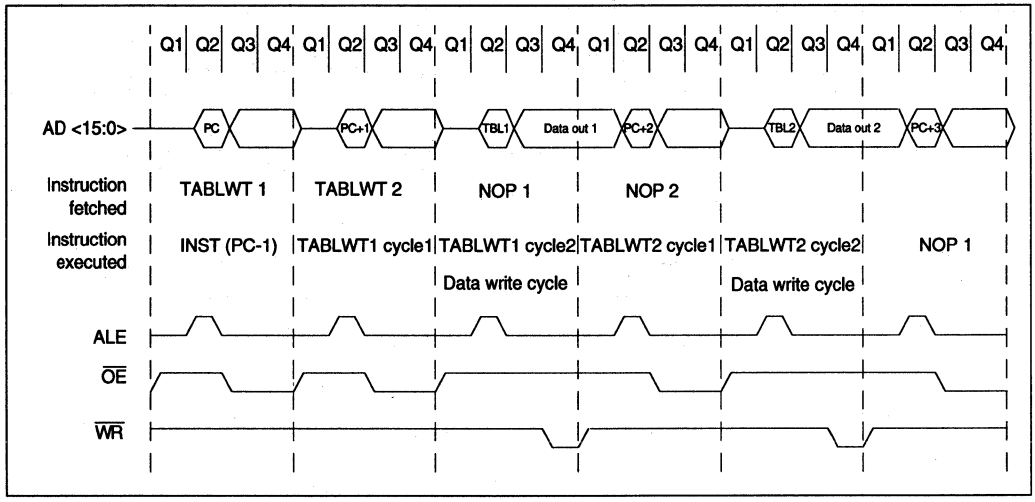
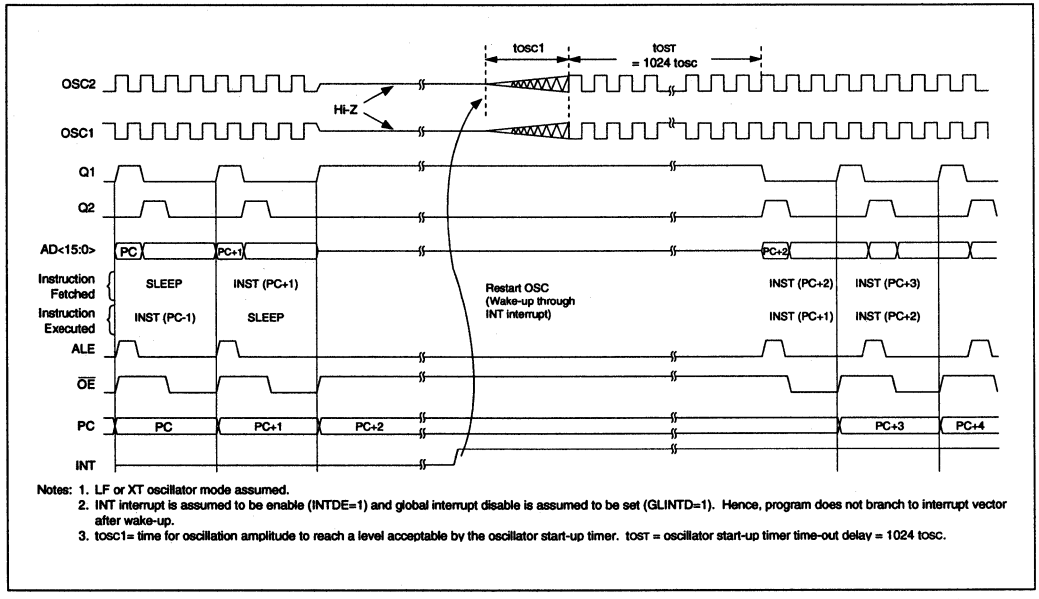
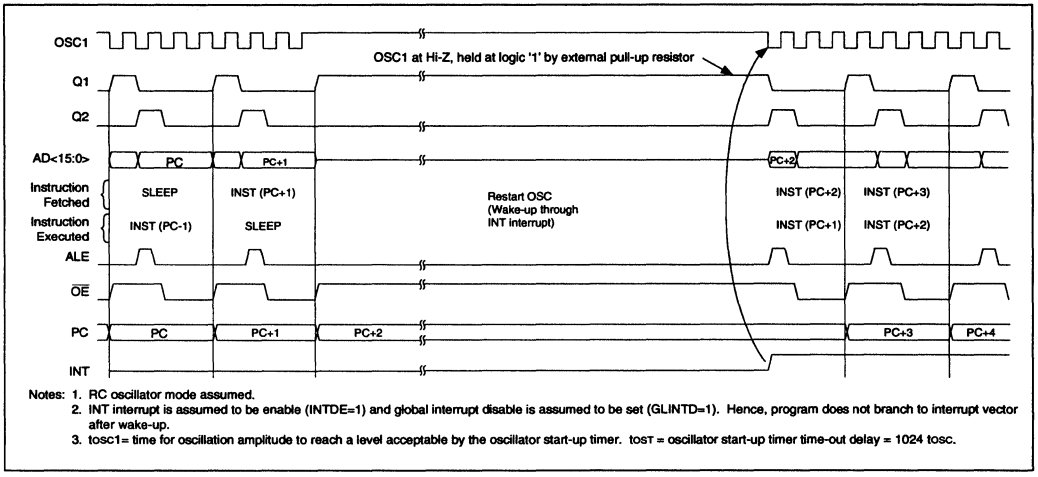


FIGURE 12.4.9 - SLEEP/WAKE-UP THROUGH INT (LF, XT MODES)



Notes: 1. LF or XT oscillator mode assumed.
2. INT interrupt is assumed to be enable (INTDE=1) and global interrupt disable is assumed to be set (GLINTD=1). Hence, program does not branch to interrupt vector after wake-up.
3. tosc1= time for oscillation amplitude to reach a level acceptable by the oscillator start-up timer. tOST = oscillator start-up timer time-out delay = 1024 tosc.

FIGURE 12.4.10 - SLEEP/WAKE-UP THROUGH INT (RC MODE)



Notes: 1. RC oscillator mode assumed.
2. INT interrupt is assumed to be enable (INTDE=1) and global interrupt disable is assumed to be set (GLINTD=1). Hence, program does not branch to interrupt vector after wake-up.
3. tosc1= time for oscillation amplitude to reach a level acceptable by the oscillator start-up timer. tost = oscillator start-up timer time-out delay = 1024 tosc.

FIGURE 12.4.11 - SYNCHRONOUS TRANSMISSION (MASTER/SLAVE)

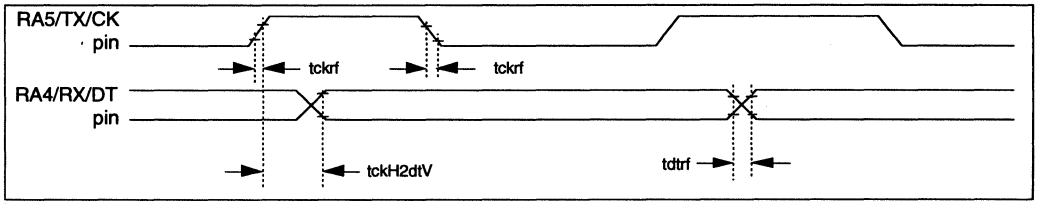


FIGURE 12.4.12 - SYNCHRONOUS RECEIVE (MASTER/SLAVE)

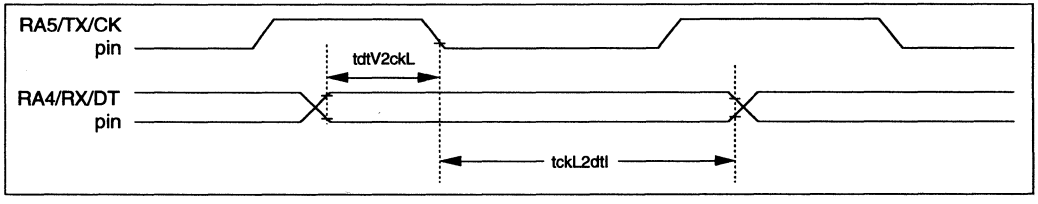
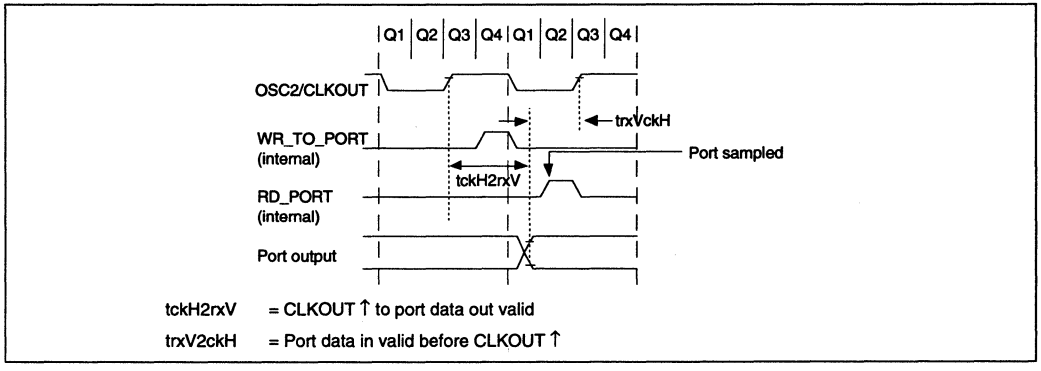


FIGURE 12.4.13 - I/O PORT INPUT/OUTPUT TIMING (PORTA, PORTB)



tckH2rxV = CLKOUT ↑ to port data out valid
trxV2ckH = Port data in valid before CLKOUT ↑

13.0 PACKAGING INFORMATION

See Section 11 of the Data Book.

CONNECTING TO MICROCHIP BBS

Connect world wide to the Microchip BBS using the Compuserve communications network. In most cases a local call is your only expense. The Microchip BBS connection does not use Compuserve membership services, therefore **you do not need Compuserve membership to join Microchip's BBS.**
The procedure to connect will vary slightly from country to country. Please check with your local Compuserve agent for details if you have a problem. Compuserve services allows multiple users at baud rates up to 9600.

To connect:

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal Compuserve setting which is 7E1.

2. Dial your local Compuserve phone number.

3. Depress **<ENTER>** and a garbage string will appear because Compuserve is expecting a 7E1 setting.

4. Type **+ <ENTER>** and Host Name: will appear.

5. Type **MCHIPBBS<ENTER>** and you will be connected to the Microchip BBS.

In the United States, to find Compuserve's phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600 baud connection. After the system responds with Host Name:, type **NETWORK<ENTER>** and follow Compuserve's directions.

For voice information (or calling from overseas), you may call (614) 457-1550 for your local Compuserve number.

PIC17C42 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

PART NO - XXX/X XXX

	PATTERN:	3-Digit Pattern code for QTP (blank for OTP and windowed parts)
	PACKAGE:	P = PDIP JW = Cerdip window L = PLCC PQ = MQFP (Metric PQFP)
	TEMPERATURE RANGE:	Blank = 0°C to + 70°C I = -40°C to + 85°C
	SPEED:	16 = 16 MHz 25 = 25 MHZ
	DEVICE:	PIC17C42

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local Compuserve number.

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

SECTION 3
8-BIT MICROCONTROLLER PROGRAMMING SPECIFICATIONS

PIC16C5X EPROM Memory Programming Specification

1.0 INTRODUCTION

1.1 Overview

The PIC16C5X Series is a family of single-chip CMOS microcontrollers with on-chip EPROM for program storage.

Due to the special architecture of these microcontrollers (12-bit wide instruction word) and the low pin counts (starting at 18 pins), the EPROM programming methodology is different from that of standard (byte-wide) EPROMs (e.g., 27C256, etc.) or other EPROM-based microcontrollers.

The PIC16C5X Series can be programmed by applying the 12-bit wide data word to the 12 available I/O pins while the address is generated by the on-chip Program Counter. The $\overline{MCLR}$ pin provides the programming supply voltage (V_{PP}) and serves also as a general test mode enable pin. Programming/verify chip enable is controlled by the RTCC pin while the OSC1 pin controls the Program Counter.

This document describes all the programming details of the PIC16C5X Series and the requirements for programming equipment to be used from programming prototypes in the engineering lab up to high volume programming on the factory floor.

FIGURE 1.1.1 - PIN CONFIGURATIONS

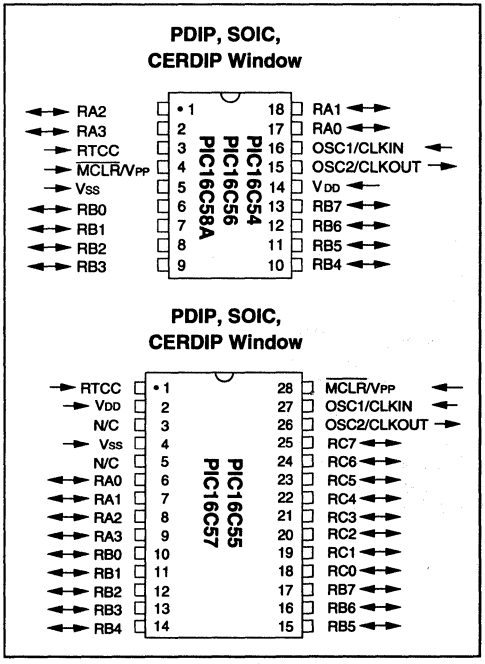


TABLE 1.1.2 - PIN DESCRIPTIONS (DURING PROGRAMMING): PIC16C54/56, PIC16C55/57

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
RTCC	$\overline{PROG}/\overline{VER}$	I	Program pulse input/verify pulse input
RA0 - RA3	D0 - D3	I/O	Data input/output
RB0 - RB7	D4 - D11	I/O	Data input/output
OSC1	INCPC	I	Increment Program Counter input
$\overline{MCLR}$	V_{PP}	P	Programming power
V_{DD}	V_{DD}	P	Power supply
V_{SS}	V_{SS}	P	Ground

Legend: I = Input, O = Output, P = Power

2.0 PROGRAM/VERIFY MODES

The PIC16C5X Series uses the internal Program Counter (PC) to generate the EPROM address. VPP is supplied through the MCLR pin.

The RTCC pin acts as chip enable, alternating between programming and verifying.

The OSC1 pin is used for verifying and incrementing the PC.

Data is applied to, or can be read on PORTA and PORTB (MSB on RB7, LSB on RA0).

The programming/verify mode is entered by raising the level on the MCLR pin from VIL to VHH (= VPP) while the RTCC pin is held at VIH and the OSC1 pin is held at VIL.

The Program Counter has now the value "FFFh", because MCLR was at VIL before. This condition selects the configuration EPROM as the very first EPROM location to be accessed after entering the program/verify mode.

Since the MCLR pin was initially at VIL, the device is in the reset state (the I/O pins are in the reset state).

Incrementing the PC once (by pulsing the OSC1 pin) selects location "000h" of the regular program memory. Afterwards all other memory locations from 001h through 1FFh can be addressed by incrementing the PC .

If the Program Counter has reached the last address of the normal memory area (e.g. "1FFh" for the PIC16C54/55), and is incremented again, the on-chip TEST EPROM will be addressed. (See Figure 2.3.2 to determine where the TEST EPROM is located for the various PIC16C5X devices).

2.1 Program/Verify without PC Increment

After entering the program/verify mode, pulsing the RTCC pin LOW programs the data present on PORTA and PORTB into the memory location selected by the Program Counter. The duration of the RTCC LOW time determines the length of the programming pulse.

Pulsing the RTCC pin LOW again without changing the signals on MCLR and OSC1 puts the contents of the selected memory location out on Port A and Port B for verification of a successful programming cycle. This verification pulse on RTCC can be much shorter than the programming pulse. If the programming was not successful, RTCC can be pulsed LOW again to apply another programming pulse, followed again by a shorter RTCC LOW pulse for another verification cycle.

This sequence can be repeated as many times as required until the programming Is successful.

2.2 Verify with PC Increment

If a verification cycle shows that programming was successful, the Program Counter can be incremented by keeping the RTCC input at a HIGH level while pulsing the OSC1 input HIGH. When both, RTCC and OSC1, are HIGH, the contents of the selected memory location is put out on Ports A and B (= Verify). The falling edge of OSC1 will increment the Program Counter.

A fast VERIFY- ONLY with automatic increment of the PC can be performed by entering the program/verify mode as described above and then clocking the OSC1 input. If OSC1 is HIGH, the selected memory location is output on Ports A and B, while the falling edge of OSC1 will increment the Program Counter. Thus, the first memory location to be verified after entering the program/verify mode, is the configuration EPROM. The next location is 000h followed by 001h and so on. The program memory location "N" can be reached by generating "N + 1" falling edges on OSC1. When OSC1 is brought HIGH again, the contents of address "N" are output on Ports A and B as long as OSC1 stays HIGH.

2.3 Programming/Verifying Configuration Fuse

The configuration word, logically mapped at program memory location "FFFh", is physically separate from the user and TEST EPROM. The PC points to the configuration word after MCLR pin goes from LOW to VHH (HIGH). The configuration word can be programmed or verified using the techniques described in Sections 2.1 and 2.2.

If PC is incremented, the next location it will point to is "000h" in user memory. Incrementing PC 4096 times will not allow the user to point to the configuration word. The only way to point to it again is to reset and re-enter program test mode.

2.4 Programming Method

The programming technique is described in the following section. It is designed to guarantee good programming margins. It does, however, require a variable power supply for VCC.

2.4.1 PROGRAMMING METHOD DETAILS

Essentially, this technique includes the following steps:

Step 1: Perform blank check at VDD = VDD min. Report failure as an erase problem. The device may not be properly erased.

Step 2: Program location with pulses (100 µs typically) and verify after each pulse at VDD = VDDP: where VDDP = VDD range required during programming (4.5 V - 5.5 V).

A. Programming condition:

VPP = 13.0 V to 13.25 V

VDD = VDDP = 4.5 V to 5.5 V

VPP must be ≥ VDD + 7.5 V to keep "programming mode" active.

B. Verify condition:

$V_{DD} = V_{DDP}$ = 4.5 V to 5.5 V

$V_{PP} \geq V_{DD}$ + 7.5 V

If location fails to program after "N" pulses, (suggested maximum program pulses of 25) then report error as a programming failure.

Step 3: Once location passes "Step 2", apply 3X overprogramming, i.e., apply three times the number of pulses that were required to program the location. This will guarantee a solid margin. The overprogramming should be made "software programmable" for easy updates.

Step 4: Program all locations.

Step 5: Verify all locations (using speed verify mode) at $V_{DD} = V_{DD}$ min.

Step 6: Verify all locations at $V_{DD} = V_{DD}$ max.

V_{DD} min. is the minimum operating voltage spec. for the part. V_{DD} max. is the maximum operating voltage spec. for the part.

2.4.2 SYSTEM REQUIREMENTS

Clearly to implement this technique, the most stringent requirements will be that of the power supplies:

V_{PP}: V_{PP} can be a fixed 13.0 V to 13.25 V supply. It must not exceed 14.0 V to avoid damage to the pin and should be current limited to approximately 30 mA. **To avoid latchup on the $\overline{MCLR}/V_{PP}$ pin, the V_{PP} power supply must have 50 Ω to 100 Ω impedance. If not, an external resistance is recommended.**

V_{DD}: 2.0 V to 6.5 V with 0.25 V granularity. Since this method calls for verification at different V_{DD} values, a programmable V_{DD} power supply is needed.

Current Requirement: 40 mA maximum

Microchip may release PIC16CXXs in the future with different V_{DD} ranges which make it necessary to have a programmable V_{DD}.

It is important to verify an EPROM at the voltages specified in this method to remain consistent with Microchip's test screening. For example, a PIC16C5X specified for 4.5 V to 5.5 V should be tested for proper programming from 4.5 V to 5.5 V. **Any programmer not meeting the programmable V_{DD} requirement and the verify at V_{DD} max and V_{DD} min requirement may only be classified as "prototype" or "development" programmer but not a production programmer.**

2.4.3 SOFTWARE REQUIREMENTS

Certain parameters should be programmable (and therefore easily modified) for easy upgrade.

A. Pulse width, current value 100µs.

B. Maximum number of pulses, current limit 25.

C. Number of over-programming pulses: should be = (A • N) + B, where N = number of pulses required in regular programming. In our current algorithm A = 3, B = 0.

2.5 Programming Pulse Width

Normal EPROM Cells

When programming one word of EPROM (program memory and TEST EPROM) a programming pulse width (TPW) of 100 microseconds is recommended.

The maximum number of programming attempts can be limited to 25 per word.

After the first successful verify, the same location should be over-programmed with 3X over-programming.

Configuration Fuses

The configuration fuses for oscillator selection, WDT (watchdog timer) disable and code protection, require a programming pulse width (T_{PWF}) of 10 milliseconds. A series of 100µs pulses is preferred over a single 10 ms pulse.

2.6 Special Memory Locations

On top of the normal EPROM section for program storage is a special EPROM area available, called the TEST EPROM. Depending on the PIC16C5X device type, this TEST EPROM can be of different size and located at different start locations. Please refer to Figure 2.3.2 for information about the TEST EPROM start address for a particular device.

For the PIC16C54/55, the TEST EPROM consists of 64 extra words (12-bit wide) which reside on top of the 512 word program memory, starting at address location 200h and ending at location 23Fh.

For the PIC16C56, the TEST EPROM is 64 words as well, starting at location 400h to 43Fh.

For the PIC16C57/C58A, the 64 TEST EPROM locations are between addresses 800h and 83Fh.

The TEST EPROM is only enabled if the device is in a test or programming/verify mode. Thus, in normal operation mode only the memory location 000h to NNNh will be accessed and the Program Counter will just roll over from address NNNh to 000h when incremented.

FIGURE 2.3.1 - PROGRAMMING METHOD

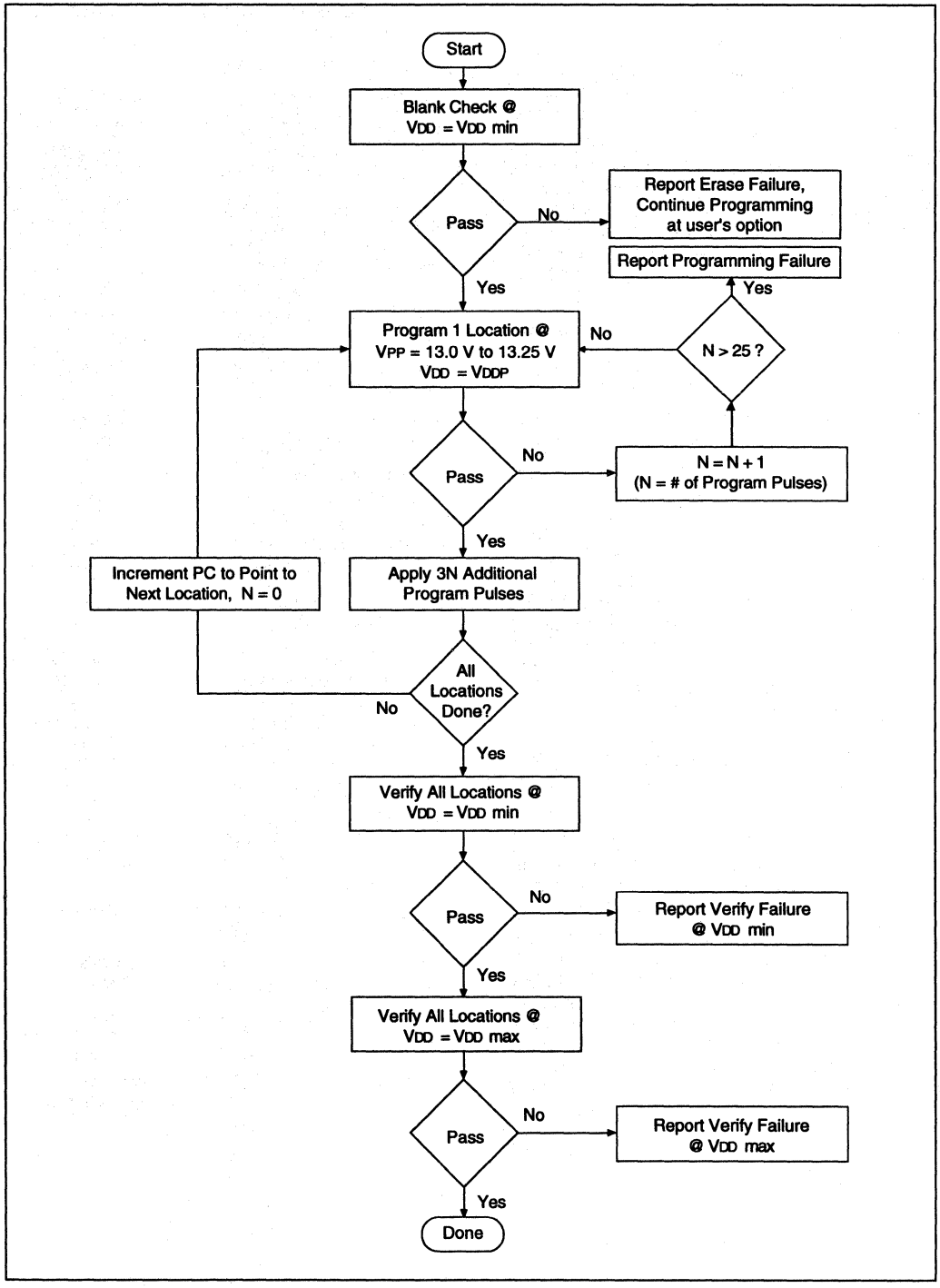
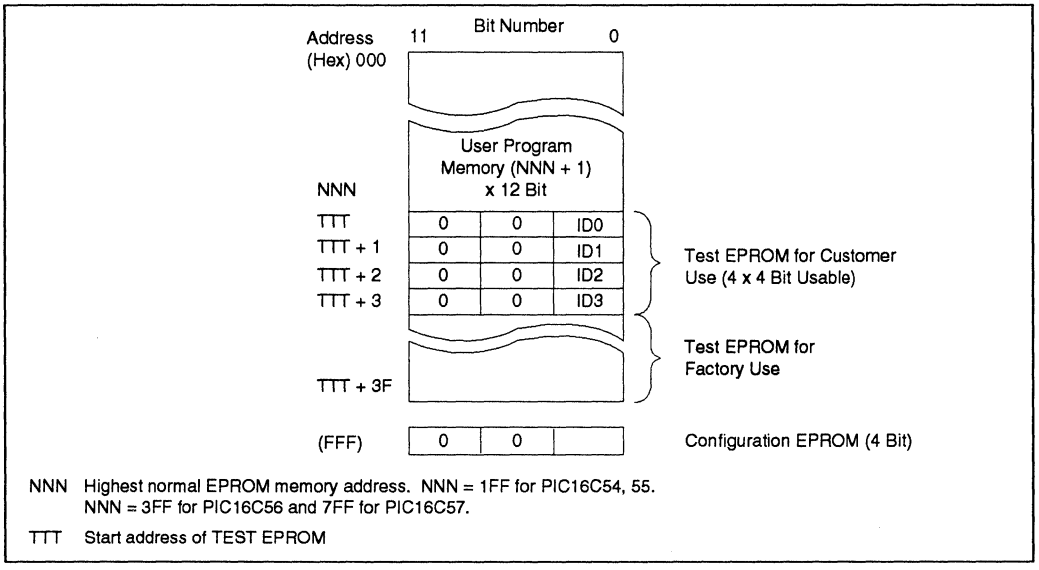


FIGURE 2.6.2 - PIC16C5X SERIES PROGRAM MEMORY MAP IN PROGRAM/VERIFY MODE



The configuration EPROM can only be accessed immediately after $\overline{MCLR}$ going from V_{IL} to V_{HH}. The Program Counter will be set to all "1s" upon $\overline{MCLR} = V_{IL}$. Thus, it has the value "FFFh" when accessing the configuration EPROM. Incrementing the Program Counter once by pulsing OSC1 causes the Program Counter to roll over to all "0s". Incrementing the Program Counter 4K times after reset ($\overline{MCLR} = V_{IL}$) does not allow access to the configuration EPROM.

2.6.1 CUSTOMER ID CODE LOCATIONS

Per definition, the first four words of the TEST EPROM (address TTT to TTT + 3) are reserved for customer use. Although all words in the TEST EPROM are 12-bits wide, it is recommended that the customer uses only the four lower order bits (bits 0 through 3) of each word and fills the eight higher order bits with "0s". This guarantees that these locations can be read correctly even when the code protection logic is activated (see Section 2.6 for details).

2.6.2 CONFIGURATION FUSES

The configuration word is the very first memory location which is accessed after entering the program/verify mode of the PIC16C5X. It contains the two fuses for the selection of the oscillator type, the watchdog timer enable fuse, and the code protection fuse. All other bits (4 through 11) are read as "1s" during a verify if the code protection fuse is not blown. If the code protection logic is activated, all bits 4 through 11 of the configuration EPROM are read as "0s" (see Section 3.4 for details).

FIGURE 2.6.2.1 - CONFIGURATION FUSE BIT MAP

Bit Number:	11	10	9	8	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	X	X	CP	WDTE	OT1	OT0
	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	RA3	RA2	RA1	RA0

Note: I/O port assignment for programming and testing (the bits marked "X" are read as "1s" if CP = 1 and are read as "0s" if CP = 0).

FIGURE 2.6.2.2 - FUSE BITS FUNCTIONALITY

RA3 CP	RA2 WDTE	RA1 OT1	RA0 OT2	Function	Remarks
1	X	X	X	Memory Unprotected	Default
0	X	X	X	Memory Protected	Note
X	1	X	X	Watchdog Timer Enabled	Default
X	0	X	X	Watchdog Timer Disabled	Note
X	X	1	1	RC Oscillator	Default
X	X	1	0	HS - High Speed Crystal	
X	X	0	1	XT - Standard Crystal	
X	X	0	0	LP - Low Frequency Crystal	

Legend: 1 Erased (apply HIGH Level to I/O pin during program).
0 Written (blown) (apply LOW Level to I/O pin during program).
X Don't care.

One-Time-Programmable (OTP) devices may have the oscillator fuses "OT0" and "OT1" set by the factory and are tested accordingly. The packages are marked "PIC16C5XHS", "PIC16C5XXT", "PIC16C5XLP", or "PIC16C5XRC". Therefore, it is essential that the inputs RA0 and RA1 are held at "1s" when programming the "WDTE" and/or the "CP" bit of the configuration EPROM. Otherwise, the factory tested and selected oscillator configuration could be overwritten and the functionality of the device is not guaranteed any more.

2.7 Code Protection

The program code written into the EPROM can be protected by blowing the code protection fuse (bit "CP" in the configuration EPROM). If the code protection logic is activated, the contents of the program EPROM cannot be read out in a way that the program code can be reconstructed. A location when read out will read as: 0000 0000 xxxx where xxxx is the XOR of the three nibbles. In addition, all memory locations starting at 040h and above are protected against programming. It is still possible to program locations 000h through 03Fh, the TEST EPROM (ID locations), and the configuration fuses. However, performing a verify (see Section 3.1) with activated code protection logic puts a 4-bit wide "checksum" out on PORTA while the 8-bits of PORTB are read as "0s". This "checksum" is computed in the following way:

The four high order bits of an instruction word are "XOR-ed" with the four middle and the four low order bits, and the result is transferred to PORTA. All memory locations including the configuration and TEST EPROM are affected (see Notes 1 and 2).

This data scrambling scheme makes it impossible to reconstruct the program stored in the EPROM. However, a verify generates an unique sequence of "checksums" on PORTA which allows a program identification for the authorized user.

The upper-eight bits of the configuration EPROM are read as "0s" if the code protection bit is blown. Thus, the "checksum" will be identical to actual settings of the four configuration EPROM fuses.

A user may want to store an identification code (ID) in the TEST EPROM and still to be able to read this code after the code protection bit was blown. This is possible if the ID code is only four bits long per memory location, is located on a nibble boundary of the 12-bit word, and the remaining eight bits are all "0s".

Example: The Customer ID code "D1E2h" should be stored in the TEST EPROM locations 200-203 like this:

200: 0000 0000 1101
201: 0000 0000 0001
202: 0000 0000 1110
203: 0000 0000 0010

Reading these four memory locations with the code protection bit blown would still output on Port A the bit sequence "1101", "0001", "1110", "0010" which is "D1E2h".

2.7.1 PROGRAMMING LOCATIONS 0000H TO 003FH AFTER CODE PROTECTION

In a code protected part, these locations will program but will read back scrambled data. Therefore to program these locations correctly, the programmer must program one nibble at a time and verify the result. Remember that the scrambled data read out is:

0000 0000 xxxx

where xxxx is the XOR of the three nibbles.

2.8 Embedding Configuration Fuse and ID Information in the Hex File

To allow portability of code, a PIC16C5X programmer is required to read the fuse and ID locations from the hex file when loading the hex file. If fuse information was not present in the hex file then a simple warning message may be issued. Similarly, while saving a hex file, all fuse and ID information must be included. Fuse information should have the address of FFFh. ID locations are mapped at addresses described in section 2.6.1. An option to not include this information may be provided.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

3.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

3.1 DC Program Characteristics

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TABLE 4 - DC CHARACTERISTICS (TA = +25°C)

Characteristics	Symbol	Min	Typ	Max	Units	Conditions
Supply Voltage during programming	VDDP	4.75	5.0	5.25	V	
Supply Current (from VDD)	IDDP			25.0	mA	VDD = 5.0 V, FOSC1 = 5 MHz,
Supply Voltage during verify	VDDV	VDD min		VDD max		Note 1
Voltage on $\overline{MCLR}$ to stay in Program/Verify Modes	VHH1	VDD		VDD + 7.25	V	
Voltage on $\overline{MCLR}$ during programming	VHH2	12.5		13.5	V	
Supply current from programming voltage source	IHH			100	mA	
Current into $\overline{MCLR}$ pin during Programming (RTCC = 0)	IHH2		10.0	25.0	mA	VHH = 13.5 V, VDD = 6.0 V
Input Low Voltage	VILmc	VSS		0.15 VDD	V	Note 2
Input High Voltage	VIHrt	0.85 VDD	5.0	VDD	V	

Note 1: Device must be verified at minimum and maximum specified operating voltages.
Note 2: The programming voltage source (connected to $\overline{MCLR}$ pin) should have a minimum of 5Ω impedance.

3.2 AC Program and Test Mode Characteristics

TABLE 5 - AC CHARACTERISTICS (TA = +10°C to +40°C, VDD = 5.0 V)

Characteristics	Symbol	Min	Typ	Max	Units	Conditions
$\overline{MCLR}$ Rise Time	TR	0.15	1.0	5	µs	Note
$\overline{MCLR}$ Fall Time	TF	0.5	2.0	5	µs	Note
Program Mode Setup Time	TPS	1.0			µs	
Data Access Time	TACC			250	ns	
Data Setup Time	TDS	1.0			µs	
Data Hold Time	TDH	1.0			µs	
Output Enable Time	TOE	0		100	ns	
Output Disable Time	TOZ	0		100	ns	
Programming Pulse Width	TPW	10.0	100	1000	µs	Standard and TEST EPROM
Programming Pulse Width	TPWF		10000		µs	Configuration Fuses Only
Recovery Time	TRC	10.0			µs	
Frequency on OSC1	FOSC	DC		5	MHz	For Incrementing of the PC

3.3 Timing Diagrams

FIGURE 3.3.1 - PROGRAMMING AND VERIFY TIMING WAVEFORM

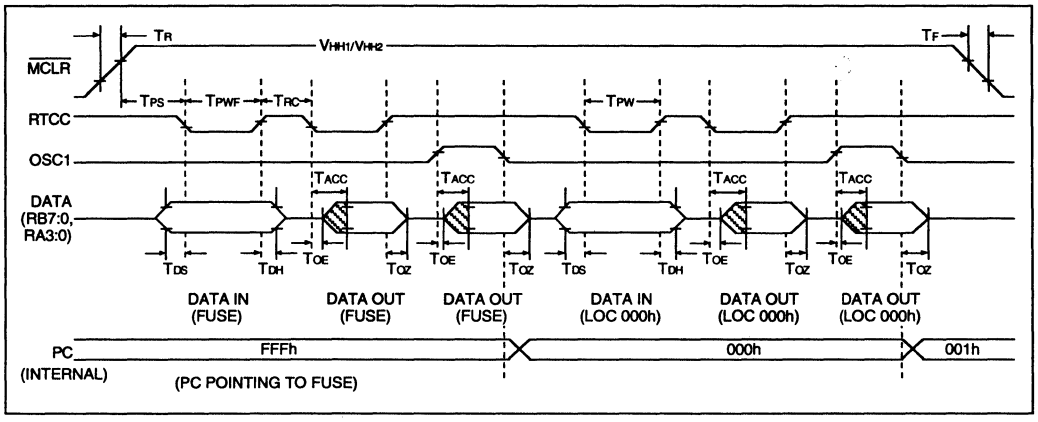
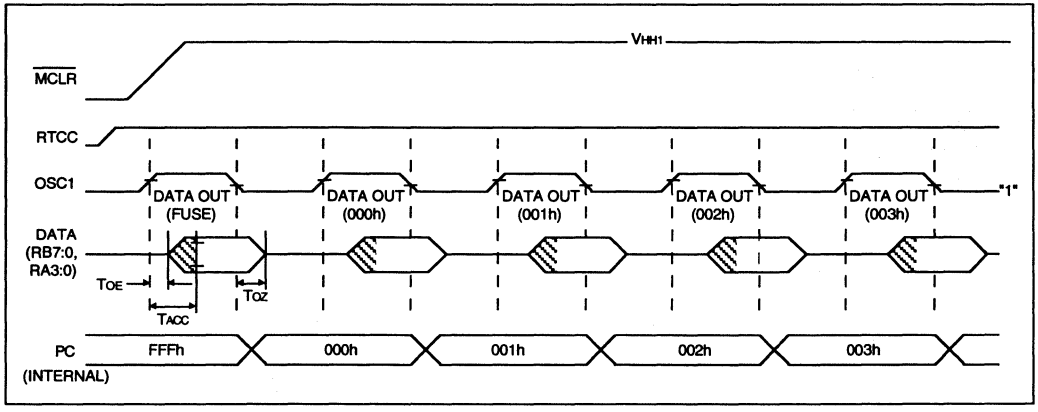


FIGURE 3.3.2 - SPEED VERIFY TIMING WAVEFORM



4.0 CHECKSUM COMPUTATION

4.1 Checksum

Read PIC16C5X memory and compute a checksum by simply adding up all memory locations from 000h to the maximum user address (e.g., 1FFh for the PIC16C54/C55). Checksum computation should not include the TEST EPROM and ID locations. The addition takes place "byte-wide". That is, the low byte of a 12- bit wide memory location is added to the high byte (with the upper four bits always "0"). Any carry bits exceeding 16-bits are neglected.

The configuration fuses must be included in the calculation using the following format:

xxxx xxxx cwoo

x 1 if device is not protected

x 0 if device is code protected

c Code protection bit

w Watchdog timer fuse

o Oscillator selection fuse

Note that the TEST EPROM and ID locations must not be included in the calculation.

The value of "x" is automatically determined by the PIC16C5X device depending on the code protection bit.

Two "checksum" functions must be available:

A. Compute checksum and display only.

B. Compute checksum and program into PIC16C5X's Customer ID locations. If the checksum is, for example, "1234h", the ID locations have to be programmed:

ID0 = 001h

ID1 = 002h

ID2 = 003h

ID3 = 004h

5.0 PIC16C5X HEX DATA FORMATS

Assemblers for the PIC16C5X can produce PIC16C5X object files in various formats. A PIC16C5X programmer must be able to accept and send data in at least one of following formats. The 8-bit merged (INHX8M) format is preferred.

5.1 8-Bit Split Intellec Hex Format (INHX8S)

This format will be output by the assembler if the INHX8S option is used with the LIST F directive or with the 'f' option on the command line.

This format produces two 8-bit Hex files. One file will contain the address/data pairs for the high order 8-bits and the other file will contain the low order 8-bits. File extensions for the object code will be '.obl' and '.obh' for low and high order files respectively.

Example:

<filename>. OBL:

:0A0000000000000000000000000000F6

:0A0000000000000000000000000000F6

:100019000028406 8A8E8C82868A989EA28086ABFAA

:10002900E0E82868BFE8C8080808034303E8E8FFDO

:03003900FFFF19AD

:00000001FF

Example:

<filename>. OBH:

:0A0000000000000000000000000000F6

:0A0000000000000000000000000000F6

:1000190000000000000000010101010102020202CA

:1000290002020303030303040404040506070708 83

:0300390008080AAA

:00000001FF

5.2 8-Bit Merged Intellec Hex Format (INHX8M)

This format will be output by the assembler if the INHX8M option is used with the LIST F directive or with the 'f' option on the command line.

This format produces one 8-bit Hex file with a low byte/high byte combination. Since each address can only contain 8 bits in this format, all addresses will be doubled. File extensions for the object code will be '.obj'.

This format is useful for transferring PIC16C5X series object code to third party EPROM programmers.

Example:

:0400100000000000EC

:100000000000000000000000000000000000000000F0

:0400100000000000EC

:10003200000028004000680OA800E800C80028016D

:100042006801A9018901EA01280208026A02BF02C5

:10005200E002E80228036803BF03E803C8030804B8

:1000620008040804030443050306E807E807FF0839

:06007200FF08FF08190A57

:00000001FF

5.3 16-Bit Hex Format

This format will be output by the assembler if the INHX16 option is used with the "LIST F" directive or with the 'f' option on the command line.

This format produces one 16-bit Hex file. File extension for the object code will be '.obj'.

This format is particularly useful to send PIC16C5X Series object code to Microchip's proprietary PICPRO™ EPROM programmer.

Example:

:0200080000000000F6

:080000000000000000000000000000000000000000F8

:0200080000000000F6

:0800190000000028004000680OA800E800C801288E

:08002100016801A9018901EA02280208026A02BFEE

:0800290002E002E80328036803BF03E803C80408E9

:0800310004080408040305430600307E807E808FF72

:0300390008FF08FF0A1993

:00000001FF

5.4 8-Bit Word Format

Each data record begins with a nine character prefix and ends with a two character checksum. Each record has the following format:

:BBAAAATTHHHH....HHHCC

Where:

BB Two-digit hexadecimal byte count representing the number of data words that will appear on the line.

AAAA Four-digit hexadecimal address representing the starting address for the data record.

TT Two-digit record type that will always be '00' except for the end-of-file record which is set to '01'.

HH Two-digit hexadecimal data word.

CC Two-digit hexadecimal checksum that is the two's compliment of the sum of all preceding bytes in the record including the prefix.

5.5 16-Bit Word Format

The 16-bit word format is basically the same as the 8-bit word format. The only difference is that the hexadecimal data word is extended to four digits.

:BBAAAATTHHHHHHHH....HHHHCC

Where:

BB Two-digit hexadecimal byte count representing the number of data words that will appear on the line. MPALC is limiting "BB" to "08" (Hex) to be compatible with PICPRO.

AAAA Four-digit hexadecimal address representing the starting address for the data record.

TT Two-digit record type that will always be "00" except for the end-of-file record which is set to "01".

HHHH Four-digit hexadecimal data word. For the PIC16C5X, the first Hex digit is always "0".

cc Two-digit hexadecimal checksum that is the two's compliment of the sum of all preceding bytes in the record including the prefix. Note that the four digit data word is treated as two bytes.

The format of each record (line) in the file is as follows:

{3,F}<count><symbol><value><marking>...<checksum>

Where:

The first digit is always '3' except for the last line which is 'F'. <count> is the number of symbols in the record (one digit).

<symbol> is the name of the symbol (six digits).

<value> is the hexadecimal value of the symbol (three digits). <marking> is a one character marking based on the symbols use:

F = file

K = literal

L = label

B = bit

U = unused

<checksum> is the hexadecimal checksum (three digits).

3

NOTES:

PIC16C6X/7X

PIC16C6X/7X EPROM Memory Programming Specification

PROGRAMMING THE PIC16C6X/7X

The PIC16C6X/7X can be programmed using one of two methods, serial or parallel. In serial mode the PIC16C6X/7X can be programmed while in the users system. This allows for increased design flexability. The parallel mode will provide faster programming as the data is loaded into the PIC16C6X/7X with a greater throughput. Either mode may be selected at the start of the programming process.

Hardware Requirements

The PIC16C6X/7X requires two programmable power supplies, one for VDD (2.0V to 6.5V recommended) and one for VPP (12V to 14V). Both supplies should have a minimum resolution of 0.25V.

Programming Mode

The programming mode for the PIC16C6X/7X allows programming of user program memory, special locations used for ID (PIC16C71 only), and the configuration fuses for the PIC16C6X/7X.

1.0 PROGRAM MODE ENTRY

1.1 User Program Memory Map

The user memory space extends from 0000h to 1FFFh (8K). Table 1-2 shows actual implementation of program memory in the PIC16C6X/7X family.

TABLE 1-2: IMPLEMENTATION OF PROGRAM MEMORY IN THE PIC16C6X/7X FAMILY

Device	Actual Implementation of Program Memory	Access to Program Memory
16C64	0000h - 07FFh (2K)	PC<10:0>
16C71	0000h - 03FFh (1K)	PC<9:0>

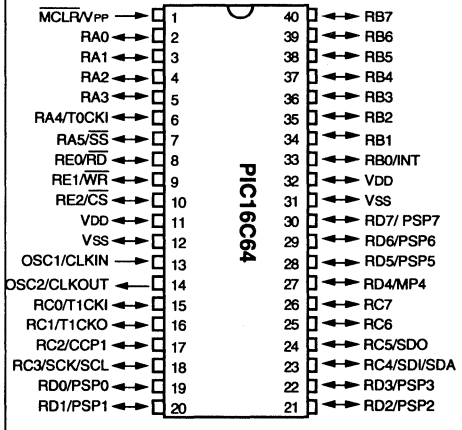
When the PC reaches the last location of the implemented program memory, it will wrap around and address a location within the physically implemented memory (see Figure 1-1).

In programming mode the program memory space extends from 0000h to 3FFFh, with the first half (0000h-1FFFh) being user program memory and the second half (2000h-3FFFh) being configuration memory. The PC will increment from 0000h to 1FFFh to 2000h to 3FFFh and wrap around to 2000h (not to 0000h). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and reenter program/verify mode (TMOD1), as described in Section 1.2.

In the configuration memory space, 2000h-207Fh or 2000h-20FFh are utilized. When in configuration memory, as in the user memory, the 2000h-2xFFh segment is repeatedly accessed as PC exceeds 2xFFh (see Figure 1-1).

FIGURE A - PIN CONFIGURATION

PDIP, CERDIP Window



PDIP, SOIC, CERDIP Window

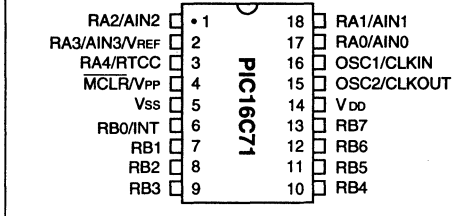
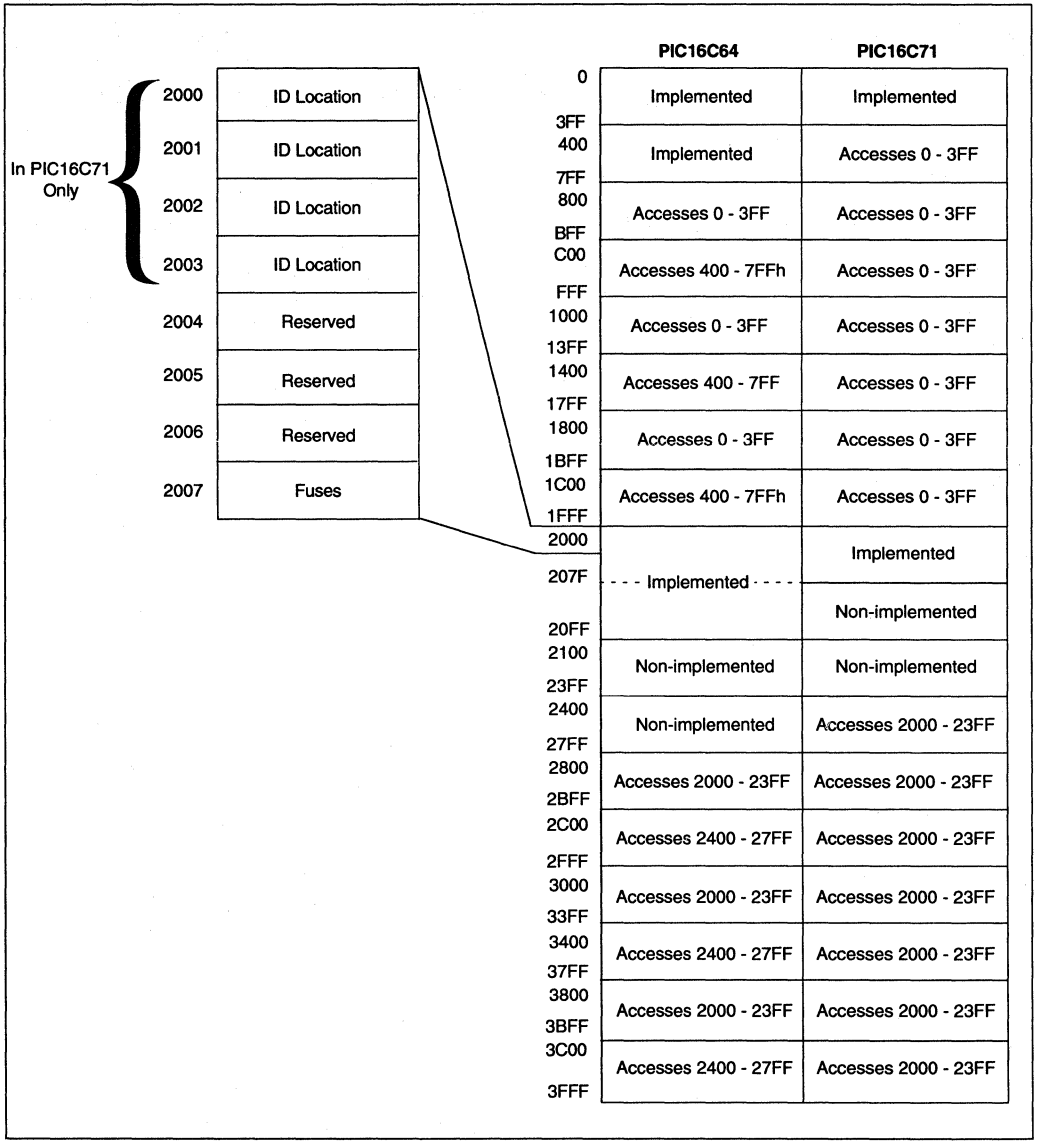


FIGURE 1-1: PROGRAM MEMORY MAPPING



1.2 Program/Verify Mode

The program/verify mode is entered by holding pins RB6 and RB7 low while raising MCLR pin from Vil to ViHH (high voltage). Once in this mode the user program memory and the configuration memory can be accessed and programmed in either a serial or parallel fashion. The initial mode of operation is serial, and the memory that is accessed is the user program memory. RB6 is a Schmitt trigger input in this mode.

The sequence that enters the device into the programming/verify mode places all other logic into the reset state (the MCLR pin was initially at VIL). This means that all I/O are in the reset state (High impedance inputs).

1.2.1 SERIAL PROGRAM/VERIFY OPERATION

The RB6 pin is used as a clock input pin, and the RB7 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RB6) is cycled six times. Each command bit is latched on the falling edge of the clock with the least significant bit (lsb) of the command being input first. The data on pin RB7 is required to have a minimum setup and hold time (see AC/DC specs) with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of us between the command and the data. After this delay the clock pin is cycled 16 times with the first cycle being a start bit and the last cycle being a stop bit. Data is also input and output lsb first. Therefore, during a read operation the lsb will be transmitted onto pin RB7 on the rising edge of the second cycle, and during a load operation the lsb will be latched on the falling edge of the second cycle. A minimum us delay is also specified between consecutive commands.

All commands are transmitted lsb first. Data words are also transmitted lsb first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1us is required between a command and a data word (or another command).

The commands that are available are:

1.2.1.1 Load Configuration

After receiving this command, the program counter (PC) will be set to 2000 hex. By then applying 16 cycles to the clock pin, the chip will load 14-bits in as the "data word", as described above, to be programmed into the configuration memory. A description of the memory mapping schemes for normal operation and configuration mode operation is shown in Figure 1-1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the program/verify test mode by taking MCLR low (Vil).

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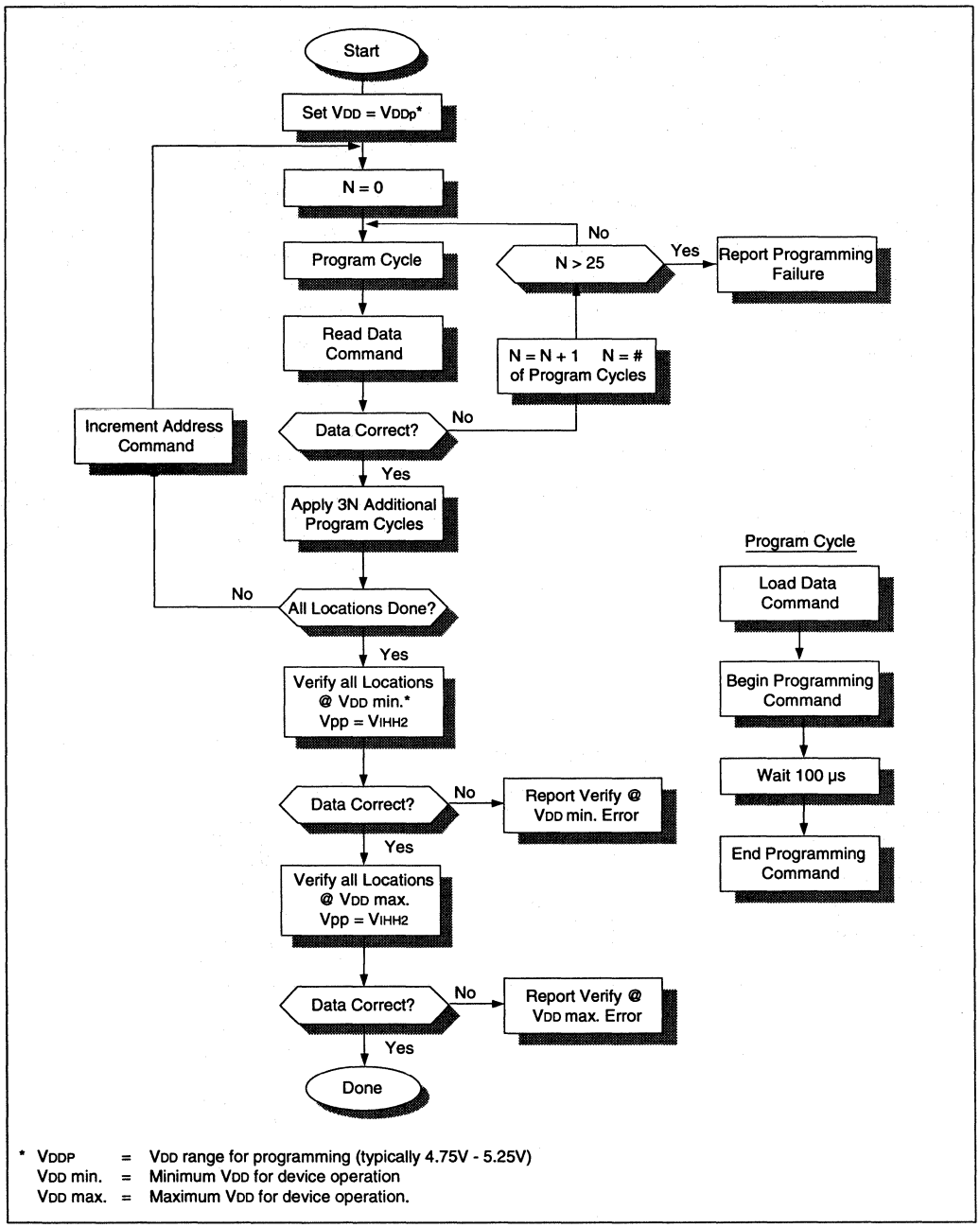
TABLE 1-3: COMMAND MAPPING (SERIAL OPERATION)

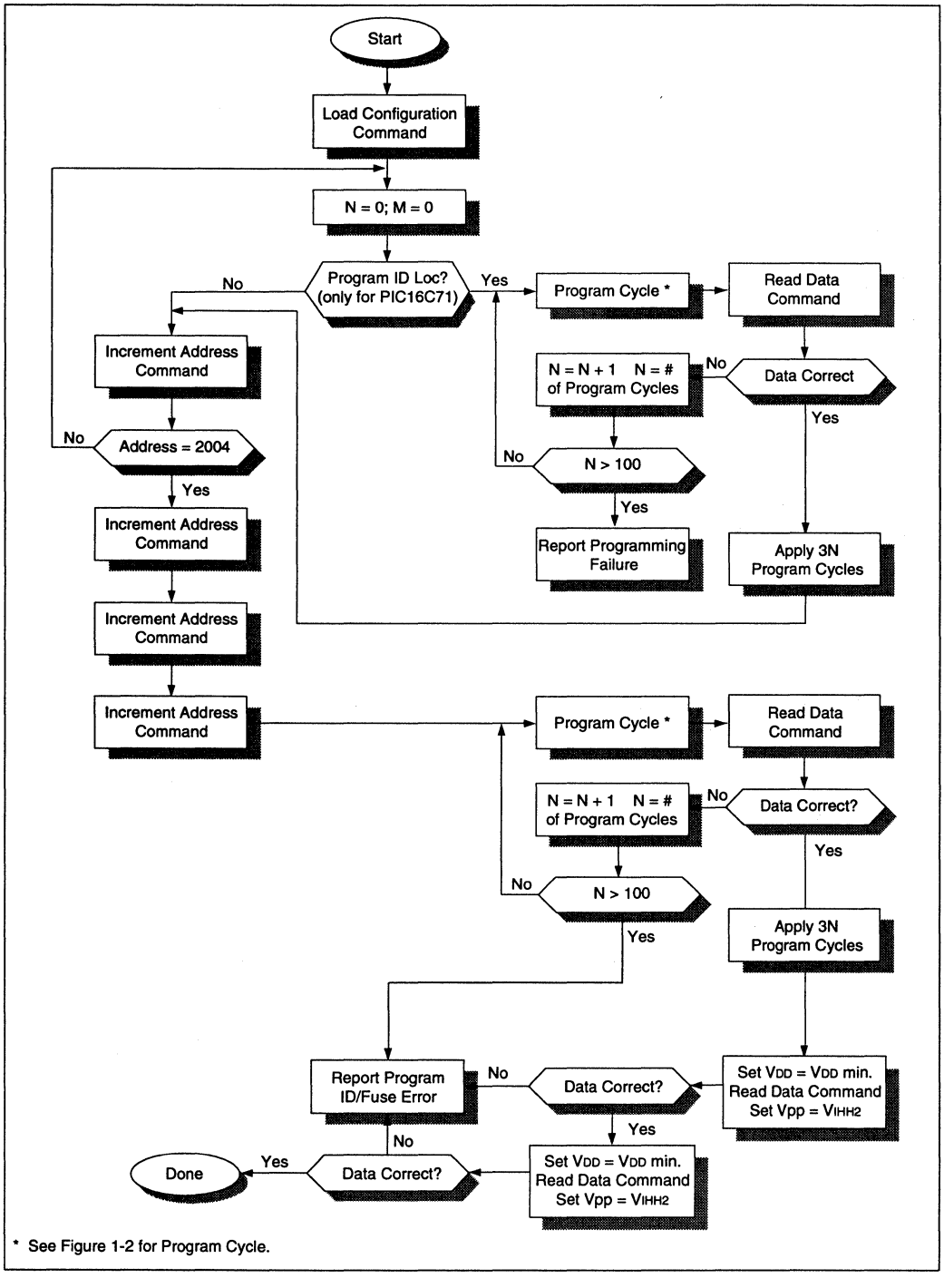
Command	Mapping (msb ... lsb)	Data
Load Configuration	0 0 0 0 0 0	0, data(14), 0
Load Data	0 0 0 0 1 0	0, data(14), 0
Read Data	0 0 0 1 0 0	0, data(14), 0
Increment Address	0 0 0 1 1 0	
Begin programming	0 0 1 0 0 0	
Enter Parallel Mode	0 0 1 0 1 0	
End Programming	0 0 1 1 1 0	

FIGURE 1-2: PROGRAM FLOW CHART - PIC16C6X/7X PROGRAM MEMORY



* VDDP = VDD range for programming (typically 4.75V - 5.25V)
VDD min. = Minimum VDD for device operation
VDD max. = Maximum VDD for device operation.

FIGURE 1-3: PROGRAM FLOW CHART - PIC16C6X/7X CONFIGURATION MEMORY



* See Figure 1-2 for Program Cycle.

1.2.1.2 Load Data

After receiving this command, the chip will load in 14-bits as a "data word" when 16 cycles are applied, as described previously. A timing diagram for the load data command is shown in Figure 1-4.

1.2.1.3 Read Data

After receiving this command, the chip will transmit data bits out of the memory currently accessed starting with the second rising edge of the clock input. The RB7 pin will go into output mode on the second rising clock edge, and it will revert back to input mode (hi-impedence) after the 16th rising edge. A timing diagram of this command is shown in Figure 1-5.

1.2.1.4 Increment Address

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 1-6.

FIGURE 1-4: LOAD DATA COMMAND (SERIAL PROGRAM/VERIFY)

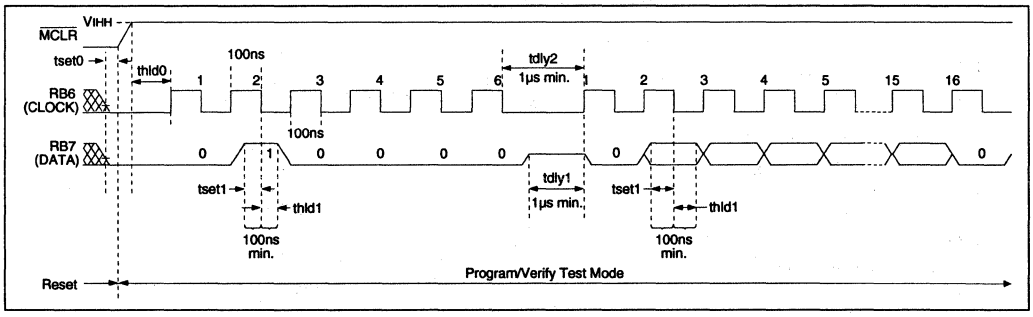


FIGURE 1-5: READ DATA COMMAND (SERIAL PROGRAM/VERIFY)

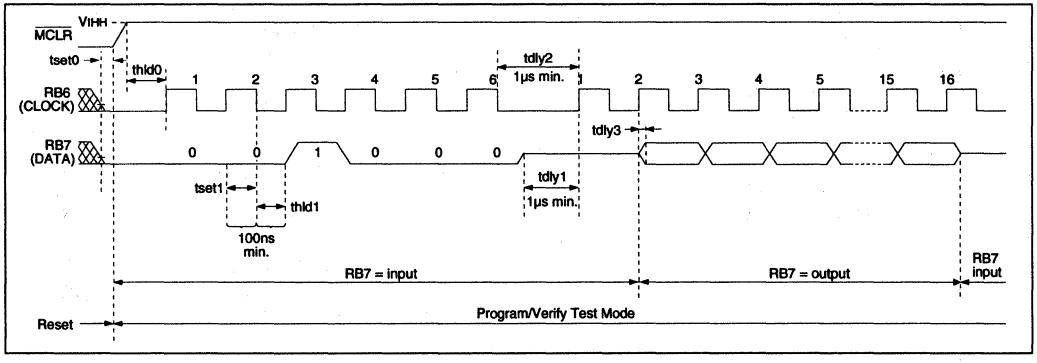
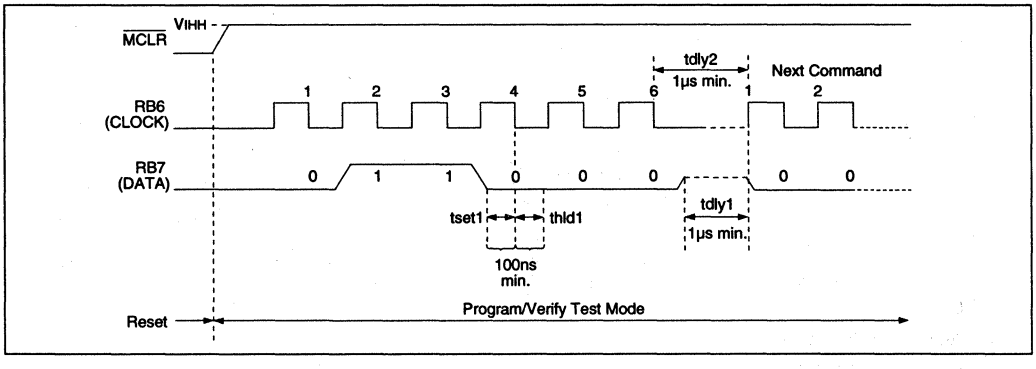


FIGURE 1-6: INCREMENT ADDRESS COMMAND (SERIAL PROGRAM/VERIFY)



1.2.1.5 Begin Programming

A load command (load configuration or load data) **must** be given before every begin programming command. Programming of the appropriate memory (test program memory or user program memory) will begin after this command is received and decoded. Programming should be performed with a series of 100µs programming pulses. A programming pulse is defined as the time between the begin programming command and the end programming command.

1.2.1.6 Enter Parallel Mode

After receiving this command, the chip will accept commands and supply data in a parallel fashion. After parallel mode has been entered, serial operation can only be achieved by fully exiting the program/verify mode and re-entering. See Figure 1-8 for details.

1.2.1.7 End Programming

After receiving this command, the chip stops programming the memory (configuration program memory or user program memory) that it was programming at the time.

1.2.2 PARALLEL OPERATING

After receiving the command 'Enter Parallel Mode', the circuitry will function in a parallel fashion. The function of pins RB6 and RB7 change during parallel operation, and it is also necessary to control several more pins to achieve the desired results. Since the memories in this device are 14 bits wide and there are only 12 I/O pins, it is necessary to transfer data into and out of the chip in two data words. These high and low data words are selected based upon the value of pin RB6 (RB6 = '1': high data word). In parallel mode, both the high and low segments of data input/output are 10-bit wide, making it possible to handle up to 20-bit data words. The need for 20-bit capability is because future versions of PIC16C6X/7X may need to read/program data words larger than 14-bit.

For each 10-bit data-segment (high or low), RB0 is the lsb and RA3 is the msb. In PIC16C6X/7X, the lower 14 bits of the total 20-bit word is actually used. The upper six bits are don't care (see Figure 1-7). The pin RB7 also has a new function in parallel operation and that is to indicate whether a command is being input or data is being transferred (RB7 = '1' - data transfer). Commands are input on pins RB<3:1> with the lsb applied to pin RB1. The clock pin during parallel operation is the RT pin. Data is again transmitted on the rising edge and latched on the falling edge of the clock. A minimum setup and hold time of 100ns with respect to the falling edge of the clock is again required. When entering a command RB7 must be held low for a minimum of 100ns after the falling edge of the clock.
The commands which are available during parallel operation are shown in Table 1-3.

A very important point to note in "parallel program/verify" operation is the function of the DATA/COMMAND pin (RB7). RB7 = 0 during RT pin pulsing indicates a command input, whereas RB7 = 1 indicates a data input. After every command, the RB7 pin must go high (for >100ns) to initiate execution of that command. This is necessary even if back to back commands are being executed without any data word in between.

TABLE 1-3: COMMAND MAPPING (PARALLEL OPERATION)

Command	Mapping (RB<3:1>)	Data
Load Configuration	0 0 0	Yes
Load Data	0 0 1	Yes
Read Data	0 1 0	Yes
Increment Address	0 1 1	No
Begin Programming	1 0 0	No
Enter Program-Compare Mode	1 1 0	No
End Programming	1 1 1	No

1.2.2.1 Load Configuration

After receiving this command, the program counter (PC) will be set to 2000h pointing to the first location in the configuration memory. By then setting pin RB7 high and pin RB6 high, the upper 4 bits of the complete data word will be latched in on the falling edge of the RT pin. Setting pin RB6 low allows the lower 10-bits to be latched in, and then the entire data word can be programmed into the configuration memory.

Note: The data must be loaded high byte first and then low byte.

A description of the memory mapping schemes for normal operation and programming mode operation is shown in Figure 1-1. After the configuration memory is entered, the only way to get back to the user program memory is by exiting the program/verify mode.

1.2.2.2 Load Data

After receiving this command, the RB7 pin is set high, and the data can then be latched into the chip. A timing diagram for the load data command is shown in Figure 1-8.

1.2.2.3 Read Data

After receiving this command, the chip will transmit data bits out of the memory currently accessed on the second rising edge of the clock input after pin RB7 has been set high. When the clock is taken high for the second time after RB7 is set high, the clock must remain high until all of the data has been read out. The high or low data words can be accessed while the clock is high by setting RB6 high or low, respectively. The pins RA<3:0>, and RB<5:0> go into output mode on the second rising clock edge, and they will revert back to input mode (hi-impedence) when the clock is set low. A timing diagram of this command is shown in Figure 1-9.

1.2.2.4 Increment Address

The PC is incremented when this command is received.

1.2.2.5 Begin Programming

A load command (load configuration or load data) must be given before every begin programming command. Programming of the appropriate memory (configuration memory or user program memory) will begin after this command is received and decoded. The programming pulse is defined by RB7, and RB7 must remain high for the duration of the programming pulse time.

1.2.2.6 Enter Program-Compare Mode

After receiving this command, the data that has been latched into the shift register by a load command can be alternatively programmed into the memory and compared to the contents of the memory location currently accessed by pulsing the RT pin high. When in this mode, the RT pin ceases to act as a clock. A single bit compare output is provided to indicate whether the data has been successfully programmed into the memory ('1' - successful), and this value is output on pin OSC2. The comparison bit is transmitted on the rising edge and latched on the falling edge of every other RT pulse starting with the second RT pulse. In order to exit this mode, it is necessary to pulse the OSC1 pin high, and this also increments the program counter. It is required to have a 1us delay time before another command is entered to allow the high voltages time to decay. A timing diagram of this command is shown in Figure 1-10.

1.2.2.7 End Programming

After receiving this command, the chip stops programming the memory (test program memory or user program memory) that it was programming at the time. It is required to have a 1us delay time before another command is entered to allow the high voltages time to decay.

FIGURE 1-7: DATA IN/OUT FORMAT

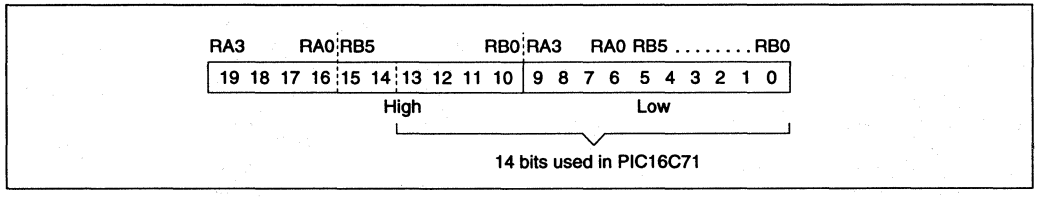


FIGURE 1-8: LOAD DATA COMMAND (PARALLEL PROGRAM/VERIFY)

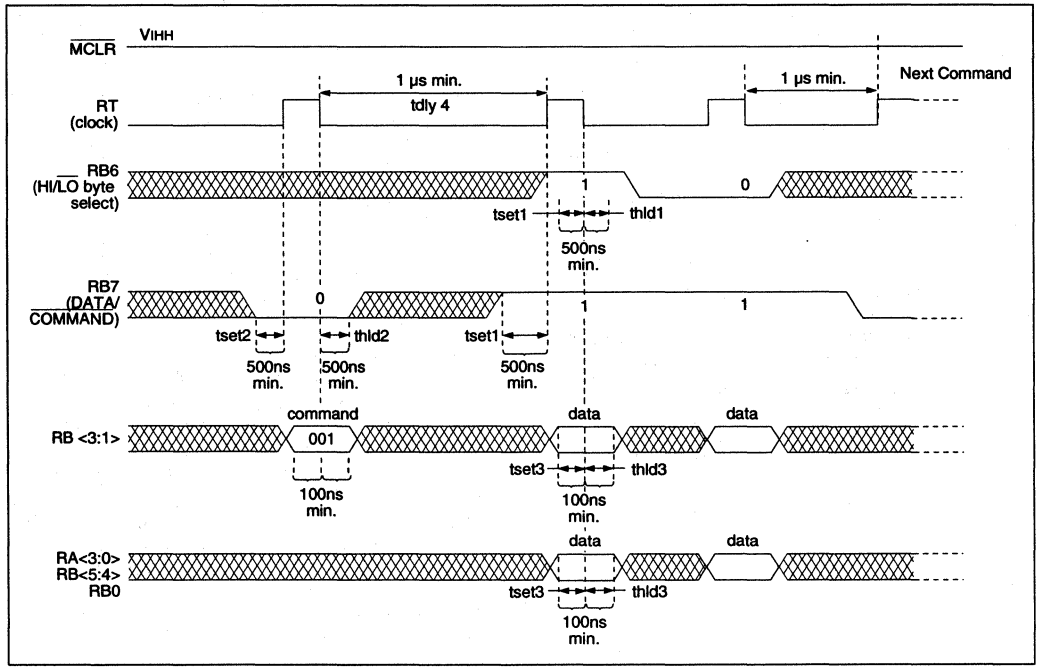


FIGURE 1-9: READ DATA COMMAND (PARALLEL PROGRAM/VERIFY)

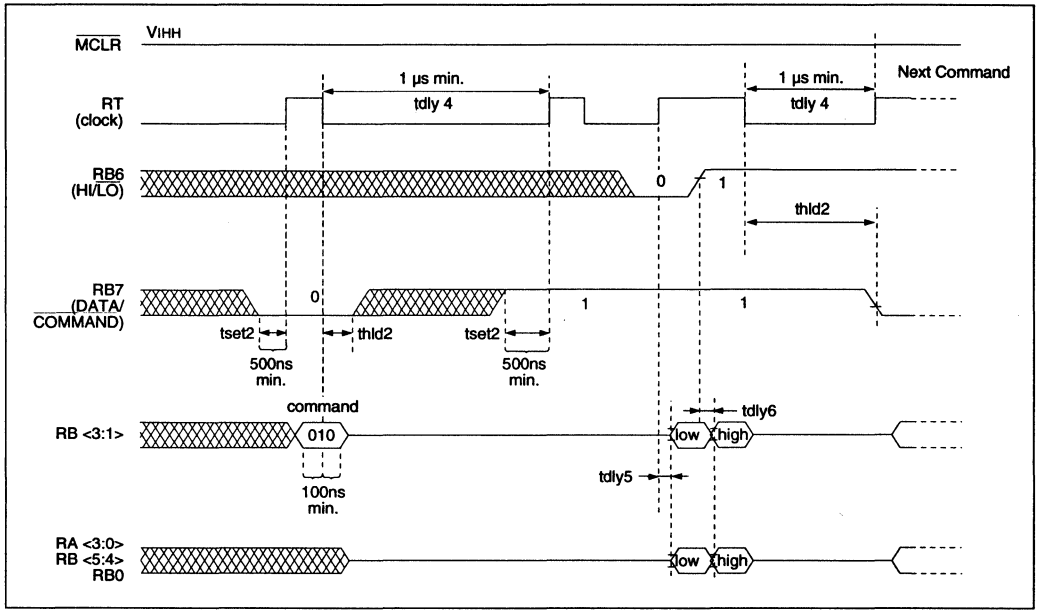
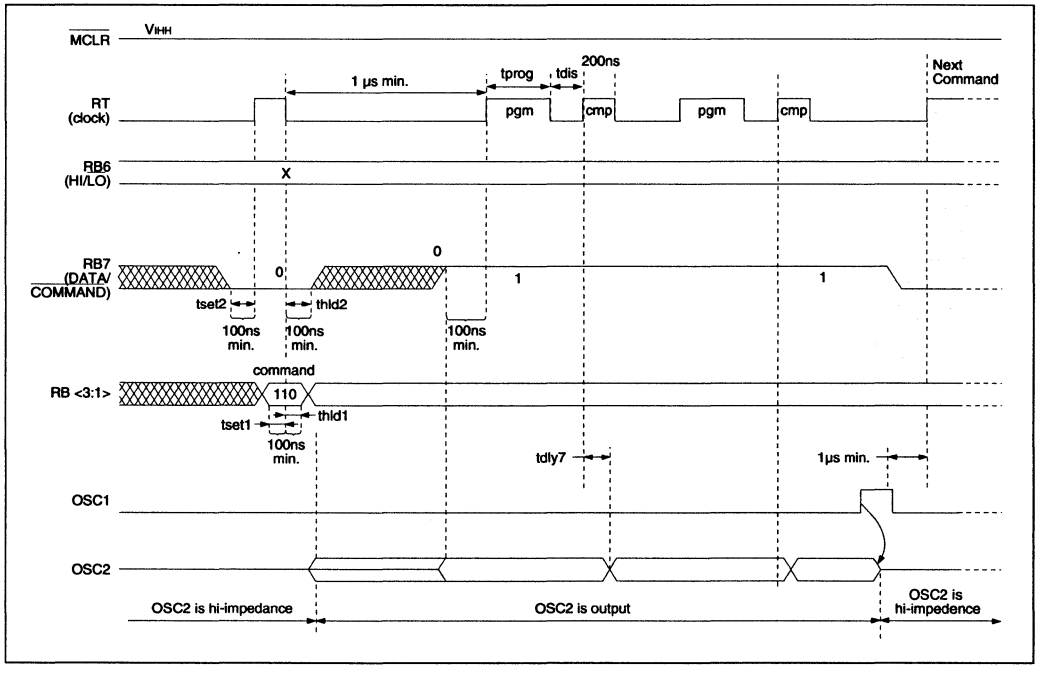


FIGURE 1-10: ENTER PROGRAM - COMPARE MODE



1.4 AC/DC Timing Requirements for Program/Verify Mode

AC/DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions Operating temperature +10°C ≤ TA ≤ +40°C, unless otherwise stated Operating voltage 4.5V ≤ VDD ≤ 5.5V, unless otherwise stated					
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
General						
Supply voltage during programming	VDDP	4.75	5.0	5.25	V	
Supply voltage during verify	VDDV	VDD min.		VDD max.	V	Note 1
Supply current (from VDD) during programming	IDDP			20	mA	
Programming supply current (from VPP)	IPP			50	mA	
Voltage on $\overline{MCLR}$ during programming	VIHH	12.5		13.5	V	
Voltage on MCLR during verify	VIHH2	VDD + 4.0		13.5		
$\overline{MCLR}$ rise time (VSS to VHH) for test mode entry	tVHHR			1.0	µs	
(RB6, RB7) input high level	VIH1	0.8 VDD			V	Schmitt trigger input
(RB6, RB7) input low level	VIL1	0.2 VDD			V	Schmitt trigger input
RB<7:2> setup time before $\overline{MCLR}$↑ (test mode selection pattern setup time)	tset0	100			ns	
RB<7:2> hold time after $\overline{MCLR}$↑ (test mode selection pattern hold time)	thld0	2			µs	
Serial Program/Verify						
Data in setup time before clock↓	tset1	100			ns	
Data in hold time after clock↓	thld1	100			ns	
Data input not driven to next clock input (delay required between command/data or command/command)	tdly1	1.0			µs	
Delay between clock↓ to clock↑ of next command or data	tdly2	1.0			µs	
Clock↑ to date out valid (during read data)	tdly3	80			ns	
Parallel Program/Verify						
Data in setup time before clock↓	tset3	100			ns	
Data in hold time after clock↓	thld3	100			ns	
RB6 and RB7 setup time before clock↓	tset1	500			ns	
RB6 and RB7 hold time after clock↓	thld1	500			ns	
RT (clock)↓ to RT (clock)↑	tdly4	1.0			µs	
RB7 (data/command select input) setup before RT (clock)↑	tset2	500			ns	
RB7 (data/command select input) hold time after RT (clock)↓	thld2	500			ns	
RT (clock)↑ to data out valid	tdly5	100			ns	
RB6 (hi/lo select) valid to data out valid	tdly6	100			ns	
Programming pulse width Time delay from program to compare (HV discharge time)	tprog tdis	1.0 0.5	100	1000	µs µs	
RT↑ to OSC2 out (compare output) valid	tdly7			100	ns	

Note 1: Program must be verified at the minimum and maximum VDD limits for the part.
Note 2: VIHH must be greater than VDD + 4.5V to stay in programming/verify mode.

2.0 CONFIGURATION FUSES

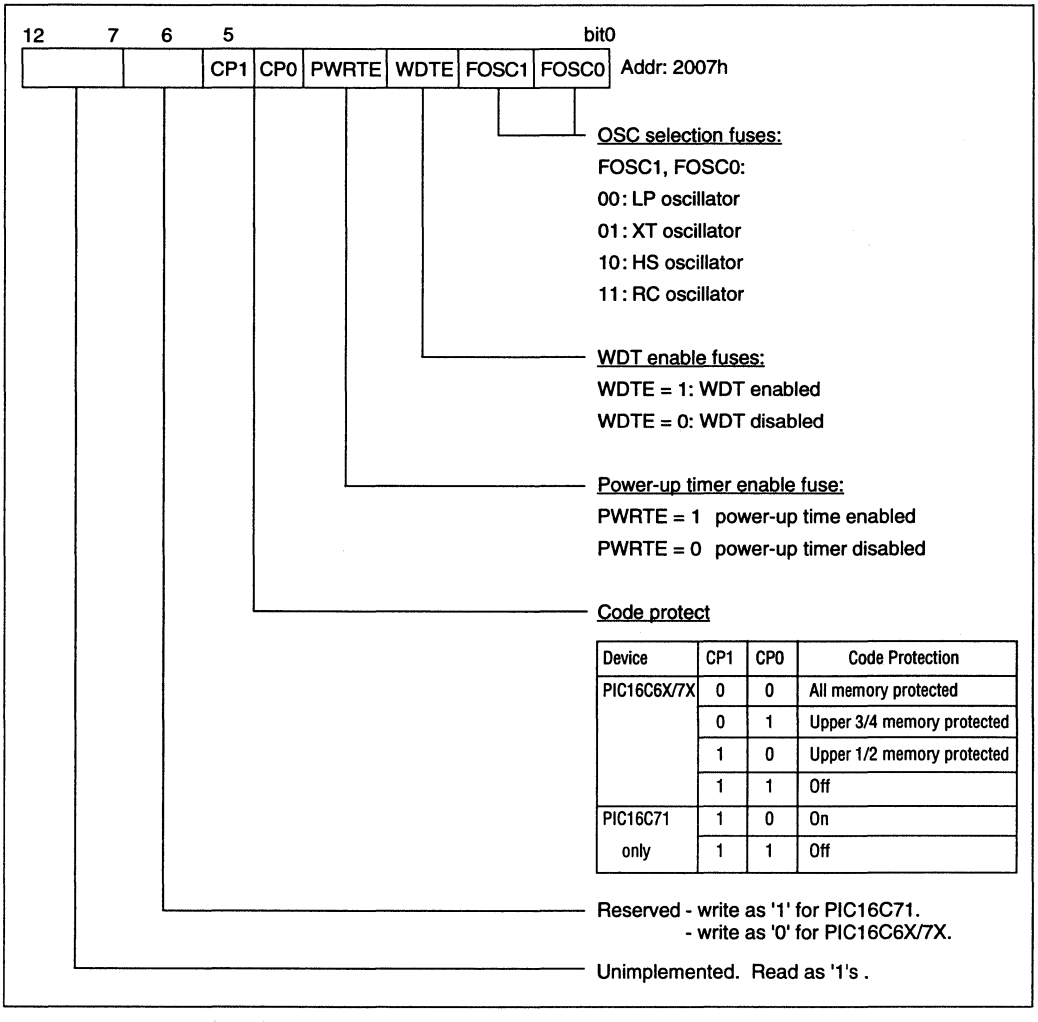
The PIC16C6X/7X has seven configuration fuses, which are EPROM bits. These fuses can be programmed (reads '0') or left unprogrammed (reads '1') to select various device configurations.

2.1 Embedding Configuration Fuse and ID Information in the Hex File

To allow portability of code, the programmer is required to read the fuse and ID locations from the hex file when loading the hex file. If fuse information was not present in the hex file then a simple warning message may be issued. Similarly, while saving a hex file, all fuse and ID information must be included. An option to not include this information may be provided.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

FIGURE 2.0.1 - CONFIGURATION WORD



Device	CP1	CP0	Code Protection
PIC16C6X/7X	0	0	All memory protected
	0	1	Upper 3/4 memory protected
	1	0	Upper 1/2 memory protected
	1	1	Off
PIC16C71	1	0	On
only	1	1	Off

2.2 Code Protection

The code in the program memory can be protected by blowing the code protect fuse (CP).

When code protected, the contents of the program memory cannot be read out in a way that the program code can be reconstructed. In addition, all memory locations starting at 0040h and above are protected against programming.

In the PIC16C71 it is still possible to program locations 0000 - 003F, the ID locations and the configuration fuses.

2.2.1 PROGRAMMING LOCATIONS 0000H TO 003FH AFTER CODE PROTECTION

These locations can be programmed but will read back scrambled data. To successfully program these locations the programmer must program the high and low 7-bits separately:

1. First program 11 1111 1bbb bbbb into the location and verify for 00 0000 0bbb bbbb.
2. Next program bb bbbb b111 1111 into the location and verify for 00 0000 0xxx xxxx, where xxxxxxx is XNOR of the high 7 bits and the low 7 bits.

2.2.2 VERIFYING A CODE-PROTECTED PIC16C6X/7X

When code protected verifying any program memory location will read a scrambled output which looks like "0000000xxxxxxx" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

a. First, program and verify a good device without code protecting it.

b. Next, blow its code protection fuse and then load its contents in a file.

c. Verify any code-protected PIC16C6X/7X against this file.

2.3 ID Locations (PIC16C71 Only):

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code - identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

It is recommended that the user use only the lower 7-bits of the ID locations and always program the upper 7-bits as '1's.

3.0 PROGRAMMING ALGORITHM REQUIRES VARIABLE VDD

The PIC16C6X/7X uses an intelligent algorithm. The algorithm calls for program verification at VDD (min.) as well as VDD (max.). Verification at VDD (min.) guarantees good "erase margin". Verification at VDD (max) guarantees good "program margin".

The actual programming must be done with VDD in the VDDP range (4.75 - 5.25V).

VDDP = VCC range required during programming.
VDD min. = minimum operating VDD spec for the part.
VDD max. = maximum operating VDD spec for the part.

Programmers must verify the PIC16C6X/7X at its specified VDD max. and VDD min. levels. Since Microchip may introduce future versions of the PIC16C6X/7X with a broader VDD range, it is best that these levels are user selectable (defaults are ok). **Any programmer not meeting these requirements may only be classified as "prototype" or "development" programmer but not a "production" quality programmer.**

MICROCHIP

PIC16C84

PIC16C84 EEPROM Memory Programming Specification

PROGRAMMING THE PIC16C84

The PIC16C84 is programmed using one of two methods, serial or parallel. The serial mode will allow the PIC16C84 to be programmed while in the users system. This allows for increased design flexability. The parallel mode will provide faster programming as the data is loaded into the PIC16C84 with a greater throughput. Either mode may be selected at the start of the programming process.

Hardware Requirements

The PIC16C84 requires two programmable power supplies, one for VDD (4.5V to 5.5V) and one for VPP (12V to 14V). Both supplies should have a minimum resolution of 0.25V.

Programming Mode

The programming mode for the PIC16C84 allows programming of user program memory, data memory, special locations used for ID, and the configuration fuses for the PIC16C84.

1.0 PROGRAM MODE ENTRY

TABLE 1.0 - TEST MODE SELECTION

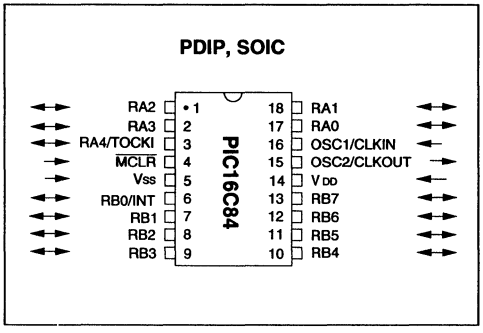
RB7	RB6	RB5	RB4	Mode	Function
0	0	X	X	TMOD1	Program/verify

1.1 User Program Memory Map

The user memory space extends from 0000h to 1FFFh (8K), of which 1K (0000h - 03FFh) is physically implemented. In actual implementation the on-chip user program memory is accessed by the lower 10-bits of the PC, with the upper 3-bits of the PC ignored. Therefore if the PC is greater than 3FFh, it will wrap around and address a location within the physically implemented memory. (See Figure 1.1.1).

In programming mode the program memory space extends from 0000h to 3FFFh, with the first half (0000h-1FFFh) being user program memory and the second half (2000h-3FFFh) being configuration memory. The PC will increment from 0000h to 1FFFh to 2000h to 3FFFh and wrap around to 2000h (not to 0000h). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and reenter program/verify mode (TMOD1) as described in Section 1.2.

FIGURE A - PIN CONFIGURATION



In the configuration memory space, 2000h-200Fh are physically implemented. Locations beyond 200Fh will physically access user memory. (See figure 1.1.1).

1.2 TMOD1: Program/Verify Mode

The program/verify mode is entered by holding pins RB6 and RB7 low while raising MCLR pin from Vil to ViHH (high voltage). RB5 and RB4 pins are don't care. Once in this mode the user program memory and the configuration memory can be accessed and programmed in either a serial or parallel fashion. The initial mode of operation is serial, and the memory that is accessed is the user program memory. RB6 and RB7 are schmitt trigger inputs in this mode.

The sequence that enters the device into the programming/verify mode places all other logic into the reset state (the MCLR pin was initially at VIL). This means that all I/O are in the reset state (High impedance inputs).

1.2.1 SERIAL PROGRAM/VERIFY OPERATION

The RB6 pin is used as a clock input pin, and the RB7 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RB6) is cycled six times. Each command bit is latched on the falling edge of the clock with the least significant bit (lsb) of the command being input first. The data on pin RB7 is required to have a minimum setup and hold time (see AC/DC specifications) with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of us between the command and the data. After this delay, the clock pin is cycled 16 times with the first cycle being a start bit and the last cycle being a stop bit. Data is also input and output lsb first.

FIGURE 1.1.1 - PROGRAM MEMORY MAPPING

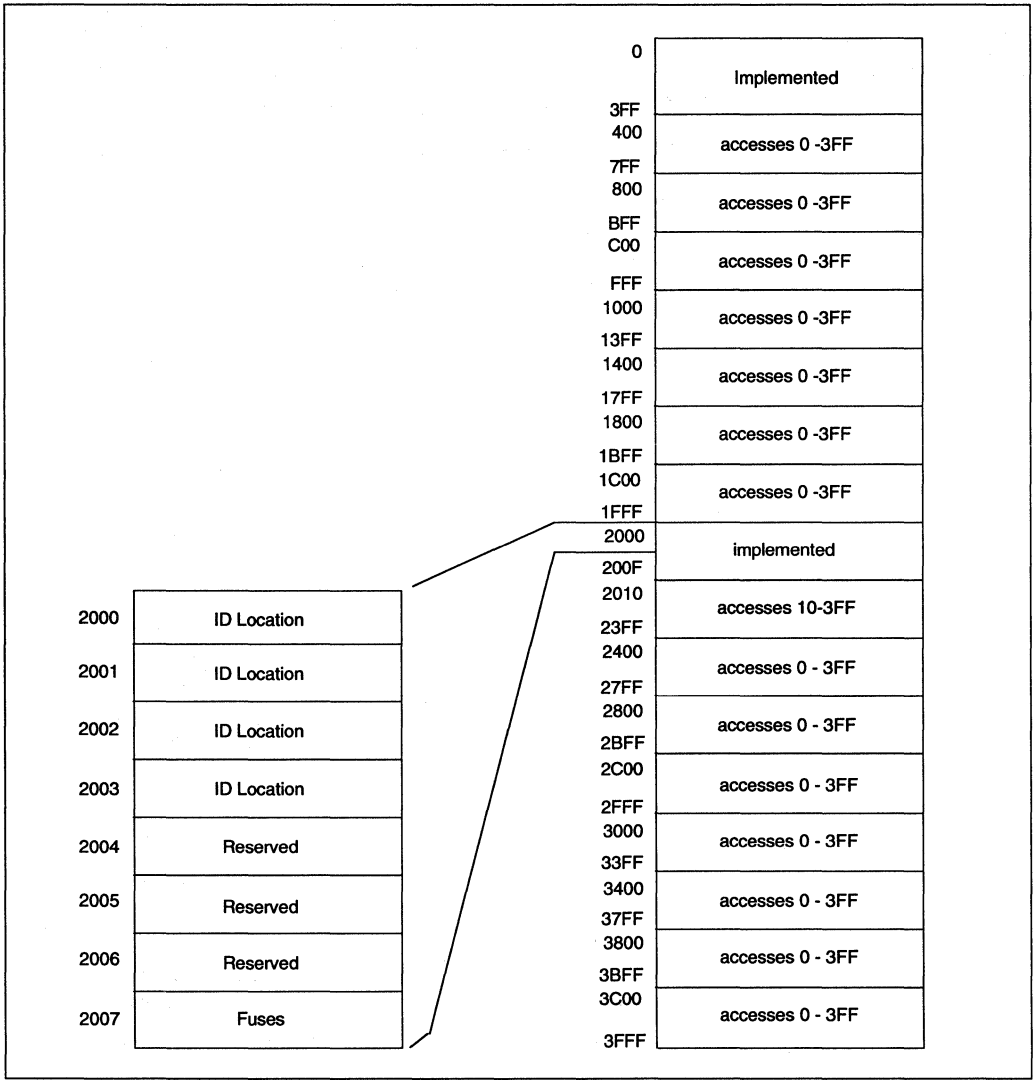
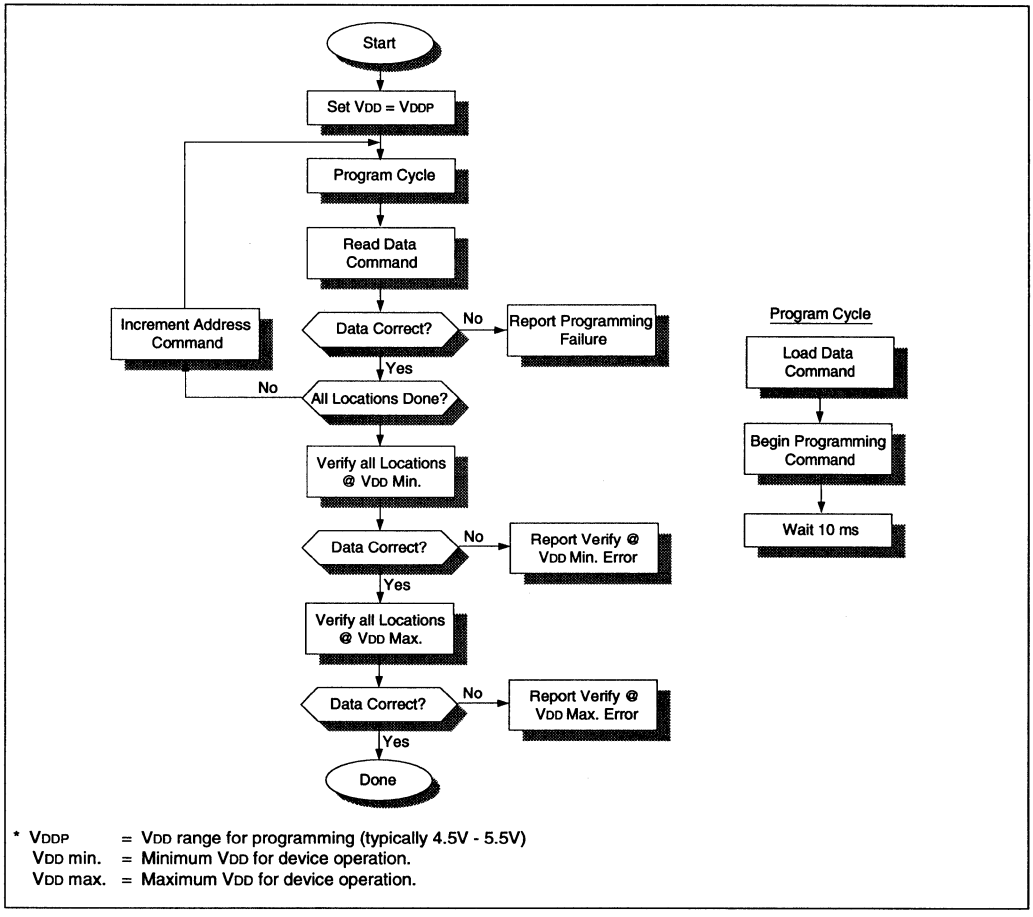


TABLE 1.2.1.1 - COMMAND MAPPING (SERIAL OPERATION)

Command	Mapping (msb ... lsb)						Data
Load Configuration	0	0	0	0	0	0	0, data (14), 0
Load Data for Program Memory	0	0	0	0	1	0	0, data (14), 0
Read Data from Program Memory	0	0	0	1	0	0	0, data (14), 0
Increment Address	0	0	0	1	1	0	
Begin Programming (Note 1)	0	0	1	0	0	0	
Enter Parallel Mode	0	0	1	0	1	0	
Load Data for Data Memory	0	0	0	0	1	1	0, data (14), 0
Read Data from Data Memory	0	0	0	1	0	1	0, data (14), 0

Notes: 1. Programming is self-timed, hence no end programming command.

FIGURE 1.2.1.1 - PROGRAM FLOW CHART - PIC16C84 PROGRAM MEMORY



* VDDP = VDD range for programming (typically 4.5V - 5.5V)
VDD min. = Minimum VDD for device operation.
VDD max. = Maximum VDD for device operation.

Therefore, during a read operation the lsb will be transmitted onto pin RB7 on the rising edge of the second cycle, and during a load operation the lsb will be latched on the falling edge of the second cycle. A minimum 1us delay is also specified between consecutive commands.

All commands are transmitted lsb first. Data words are also transmitted lsb first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least us is required between a command and a data word (or another command).

The commands that are available are:

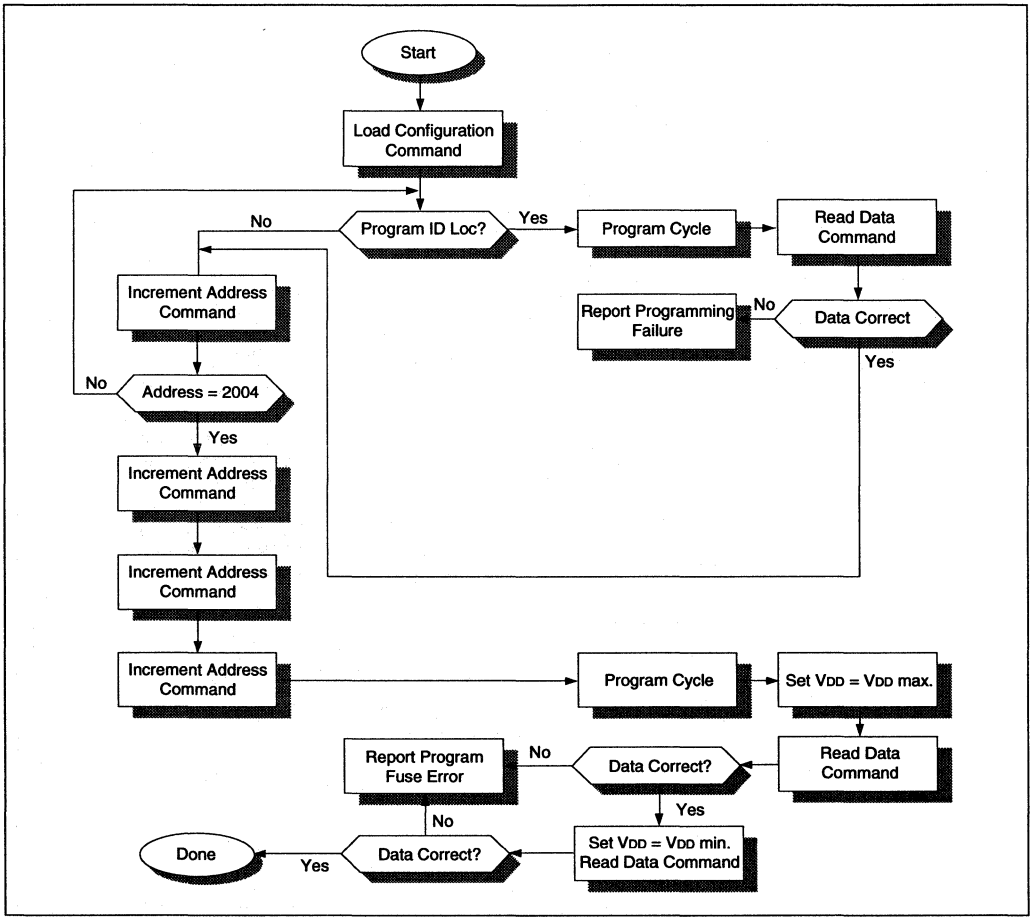
1.2.1.1 Load Configuration

After receiving this command, the program counter (PC) will be set to 2000 hex. By then applying 16 cycles to the clock pin, the chip will load 14-bits in as the "data word", as described above, to be programmed into the configuration memory. A description of the memory mapping schemes of the program memory for normal operation and configuration mode operation is shown in figure 1.0. After the configuration memory is entered, the only way to get back to the user program memory is to exit the program/verify test mode by taking $\overline{MCLR}$ low (Vil).

1.2.1.2 Load Data for Program Memory

After receiving this command, the chip will load in 14-bits as a "data word" when 16 cycles are applied, as described previously. A timing diagram for the load data command is shown in Figure 1.2.1.3.

FIGURE 1.2.1.2 - PROGRAM FLOW CHART - PIC16C84 CONFIGURATION MEMORY



1.2.1.3 Load Data for Data Memory

After receiving this command, the chip will load in 14-bits as a "data word" when 16 cycles are applied. However, the data memory is only 8-bits wide, and thus only the first 8-bits of data after the start bit will be programmed into the data memory. It is still necessary to cycle the clock the full 16 cycles in order to allow the internal circuitry to reset properly. The data memory contains 64 words. Only the lower 8-bits of the PC are decoded by the data memory, and therefore if the PC is greater than 3Fh, it will wrap around and address a location within the physically implemented memory.

1.2.1.4 Read Data from Program Memory

After receiving this command, the chip will transmit data bits out of the program memory (user or configuration) currently accessed starting with the second rising edge of the clock input. The RB7 pin will go into output mode on the second rising clock edge, and it will revert back to input mode (hi-impedence) after the 16th rising edge. A timing diagram of this command is shown in Figure 1.2.1.4.

1.2.1.5 Read Data from Data Memory

After receiving this command, the chip will transmit data bits out of the data memory starting with the second rising edge of the clock input. The RB7 pin will go into output mode on the second rising edge, and it will revert back to input mode (hi-impedence) after the 16th rising edge. As previously stated, the data memory is 8-bits wide, and therefore, only the first 8-bits that are output are actual data.

1.2.1.6 Increment Address

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 1.2.1.5.

FIGURE 1.2.1.3 - LOAD DATA FOR PROGRAM MEMORY COMMAND (SERIAL PROGRAM/VERIFY)

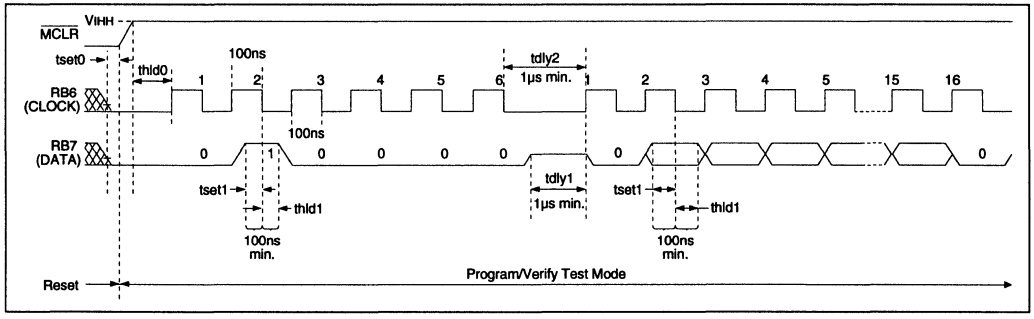


FIGURE 1.2.1.4 - READ DATA FROM PROGRAM MEMORY COMMAND (SERIAL PROGRAM/VERIFY)

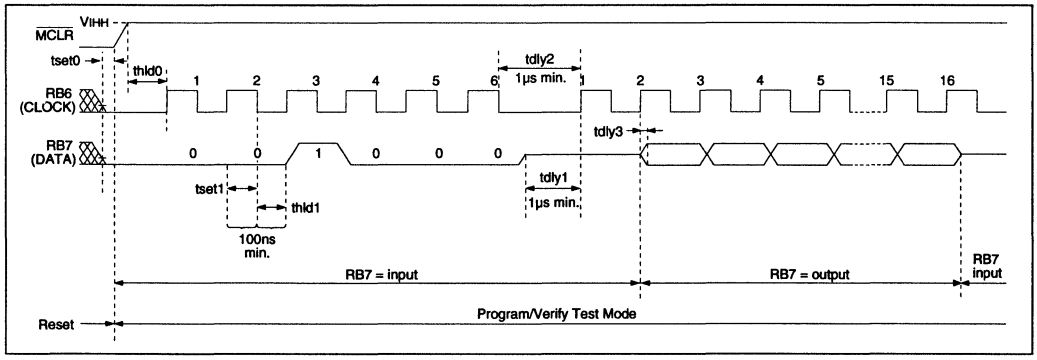
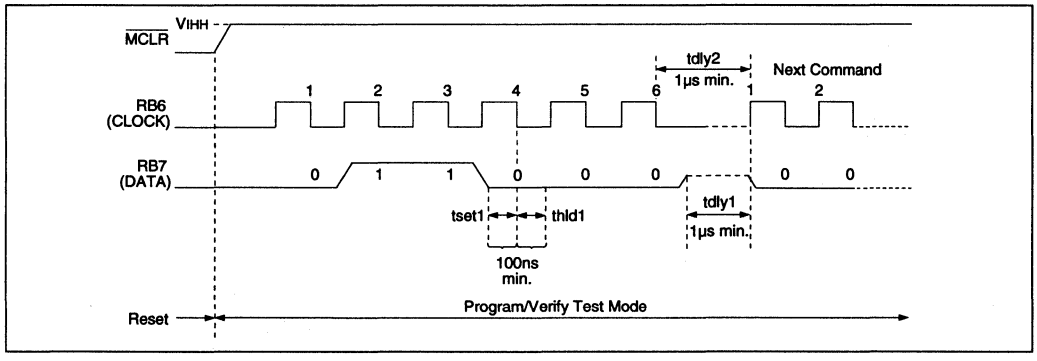


FIGURE 1.2.1.5 - INCREMENT ADDRESS COMMAND (SERIAL PROGRAM/VERIFY)



1.2.1.7 Begin Programming

A load command must be given before every begin programming command. Programming of the appropriate memory (test program memory, user program memory or data memory) will begin after this command is received and decoded. An internal timing mechanism executes an erase before write. The user must allow 10ms for programming to complete. No "end programming" command is required.

1.2.1.8 Enter Parallel Mode

After receiving this command, the chip will accept commands and supply data in a parallel fashion. After parallel mode has been entered, serial operation can only be achieved by fully exiting the program/verify mode and re-entering. See Section 1.2.2 for details.

1.2.2 PARALLEL OPERATION

After receiving the command 'Enter Parallel Mode', the circuitry will function in a parallel fashion. The function of pins RB6 and RB7 change during parallel operation, and it is also necessary to control several more pins to achieve the desired results. Since the program memory in this device is 14-bits wide and there are only 12 I/O pins, it is necessary to transfer data into and out of the chip in two data words. These high and low data words are selected based upon the value of pin RB6 (RB6 = '1': high data word). In parallel mode, both the high and low segments of data input/output are 10-bits wide, making it possible to handle up to 20-bit data words. The need for 20-bit capability is because future versions of PIC16C84 may need to read/program data words larger than 14-bit.

For each 10-bit data-segment (high or low), RB0 is the lsb and RA3 is the msb. In PIC16C84, the lower 14 bits of the total 20-bit word is actually used. The upper-six bits are don't care (see Figure 1.2.2.1). The pin RB7 also has a new function in parallel operation and that is to indicate whether a command is being input or data is being transferred (RB7 = '1' - data transfer). Commands are input on pins RB<3:0> with the lsb applied to pin RB0. The clock pin during parallel operation is the RT pin. Data is again transmitted on the rising edge and latched on the falling edge of the clock. A minimum setup and hold time of 100ns with respect to the falling edge of the clock is again required. When entering a command RB7 must be held low for a minimum of 100ns after the falling edge of the clock. The commands which are available during parallel operation are shown in Table 1.2.2.1.

Note: In "parallel program/verify" operation is the function of the DATA/COMMAND pin (RB7). RB7 = 0 during RT pin pulsing indicates a command input, whereas RB7 = 1 indicates a data input. After every command, the RB7 pin must go high (for >100ns) to initiate execution of that command. This is necessary even if back to back commands are being executed without any data word inbetween them.

TABLE 1.2.2.1 - COMMAND MAPPING (PARALLEL OPERATION)

Command	Mapping (RB<3:0>)	Data
Load Configuration	0 0 0 0	Yes
Load Data for Program Memory	0 0 1 0	Yes
Read Data from Program Memory	0 1 0 0	Yes
Increment Address	0 1 1 0	No
Begin Programming	1 0 0 0	No
Read Data from Data Memory	0 1 0 1	Yes
Load Data from Data Memory	0 0 1 1	Yes
Bulk Erase Program Memory	1 0 0 1	No
Bulk Erase Data Memory	1 0 1 1	No

1.2.2.1 Load Configuration

After receiving this command, the program counter (PC) will be set to 2000h pointing to the first location in the configuration memory. By then setting pin RB7 high and pin RB6 high, the upper 4-bits of the complete data word will be latched in on the falling edge of the RT pin. Setting pin RB6 low allows the lower 10-bits to be latched in, and then the entire data word can be programmed into the configuration memory.

Note: The data must be loaded high byte first and then low byte.

A description of the memory mapping schemes for normal operation and programming mode operation is shown in Figure 1.0. After the configuration memory is entered, the only way to get back to the user program memory is by exiting the program/verify mode.

1.2.2.2 Load Data for Program Memory

After receiving this command, the RB7 pin is set high, and the data can then be latched into the chip. A timing diagram for the load data command is shown in Figure 1.2.2.2.

1.2.2.3 Load Data for Data Memory

After receiving this command, the RB7 pin is set high, and the data can then be latched into the chip. When a 'Begin Programming' command is issued following this command, the data will be programmed into the data memory.

1.2.2.4 Read Data from Program Memory

After receiving this command, the chip will transmit data bits out of the program memory currently accessed (user or configuration) on the second rising edge of the clock input after pin RB7 has been set high. When the clock is taken high for the second time after RB7 is set high, the clock must remain high until all of the data has been read out. The high or low data words can be accessed while the clock is high by setting RB6 high or low, respectively. The pins RA<3:0>, and RB<5:0> go into output mode on the second rising clock edge, and they will revert back to input mode (hi-impedence) when the clock is set low. A timing diagram of this command is shown in Figure 1.2.2.3.

1.2.2.5 Read Data from Data Memory

After receiving this command, the chip will transmit data bits out of the currently accessed data memory location in a fashion identical to that of the read command for program memory.

1.2.2.6 Increment Address

The PC is incremented when this command is received.

FIGURE 1.2.2.1 - DATA IN/OUT FORMAT

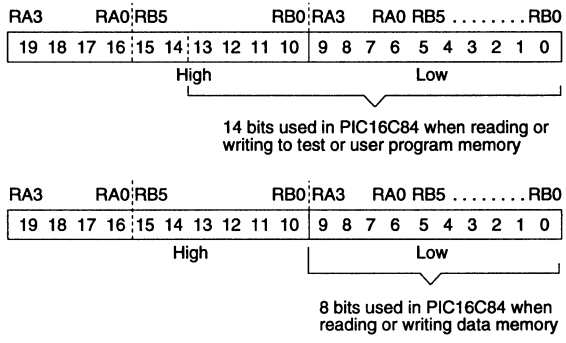


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FIGURE 1.2.2.2 - LOAD DATA FOR PROGRAM MEMORY COMMAND (PARALLEL PROGRAM/ VERIFY)

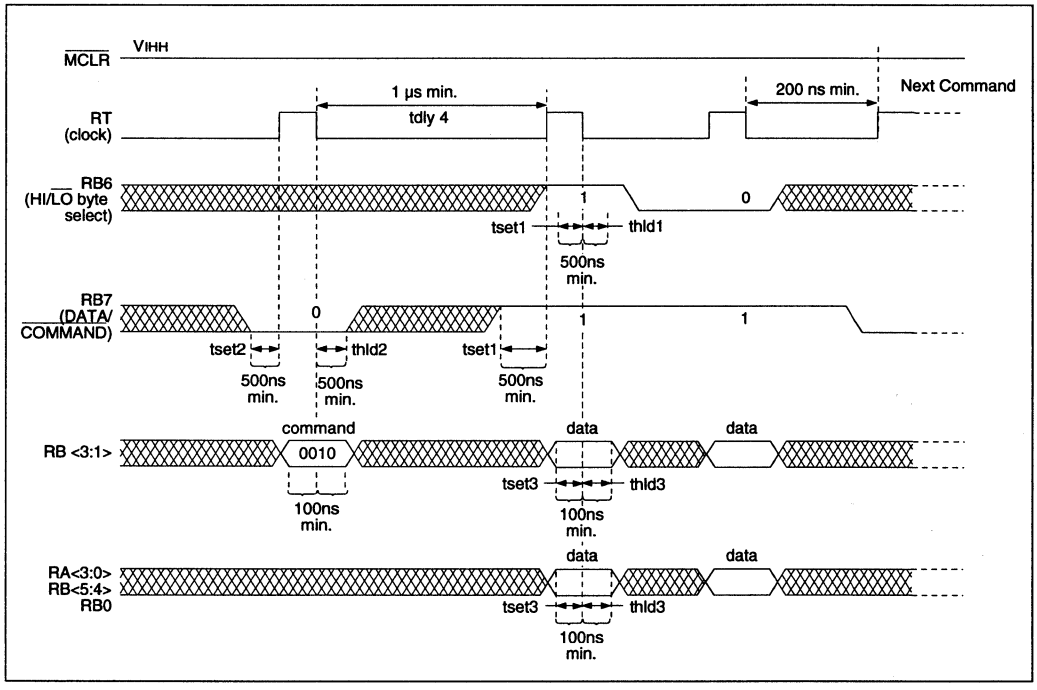
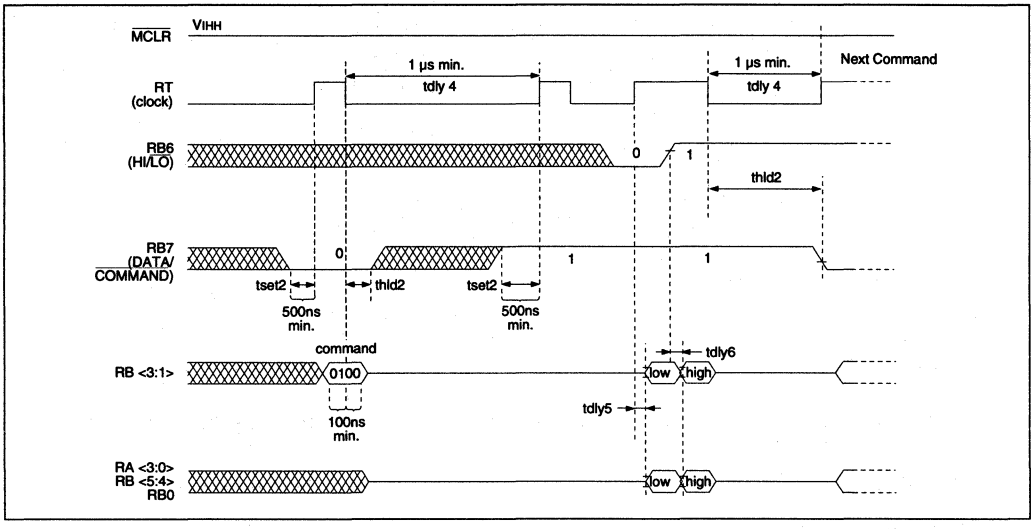


FIGURE 1.2.2.3 - READ DATA FROM PROGRAM MEMORY COMMAND (PARALLEL PROGRAM/VERIFY)



1.2.2.7 Begin Programming

A load command must be given before every begin programming command. Programming of the selected memory (configuration memory, user program memory or data memory) will begin after this command is received and decoded. The programming time is specified to be 10ms. The OSC2 pin will go high when the programming is completed (only in parallel mode).

1.2.2.8 Bulk Erase Program Memory

After this command is performed, the next program command will erase the entire program memory. The erase time is specified to be 10ms.

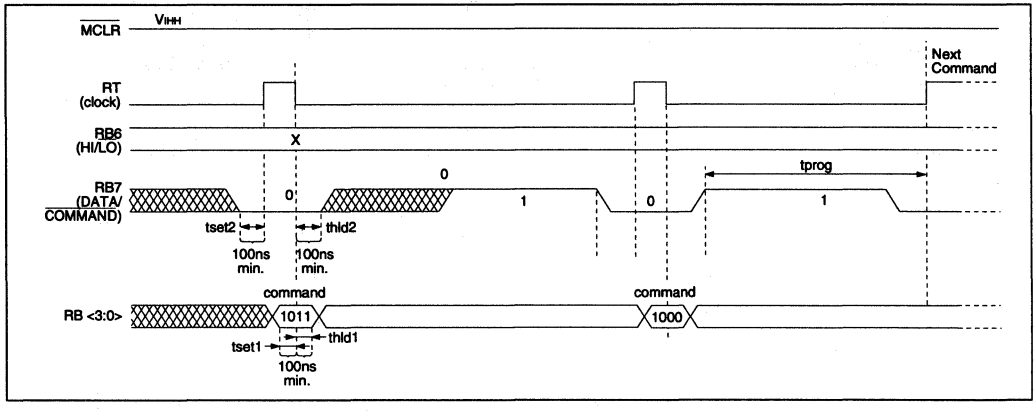
If the address is pointing to user memory, only the user memory will be erased.

If the address is pointing to the test program memory (2000h - 200Fh), then both the user memory and the test memory will be erased. The configuration word will not be erased, even if the address is pointing to location 2007h.

1.2.2.9 Bulk Erase Data Memory

After this command is performed, the next program command will erase the entire data memory. The erase time is specified to be 10ms. A description of the sequence of these two commands is shown in Figure 1.2.2.4.

FIGURE 1.2.2.4 - BULK ERASE DATA MEMORY AND BEGIN PROGRAMMING COMMANDS



1.3.1 AC/DC TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

AC/DC CHARACTERISTICS, POWER SUPPLY PINS	**Standard Operating Conditions** Operating temperature $0 \le T_A \le +70°C$, unless otherwise stated Operating voltage $4.5V \le V_{DD} \le 5.5V$, unless otherwise stated					
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions/Comments**
General						
Supply voltage during programming	V_{DDP}	4.5	5.0	5.5	V	
Supply voltage during verify	V_{DDV}	V_{DD} min.		V_{DD} max.	V	Note 1
High voltage on $\overline{MCLR}$ and RT for test-mode entry	V_{IHH}	12		14.0	V	Note 2
Supply current (from V_{DD}) during program/verify	I_{DDP}			50	mA	
Supply current from V_{IHH} (on $\overline{MCLR}$)	I_{HH}			1	mA	
$\overline{MCLR}$ rise time (V_{SS} to V_{HH}) for test mode entry	tVHHR			1.0	µs	
(RB6, RB7) input high level	V_{IH1}	0.8 V_{DD}			V	Schmitt trigger input
(RB6, RB7) input low level	V_{IL1}	0.2 V_{DD}			V	Schmitt trigger input
RB<7:4> setup time before $\overline{MCLR}\uparrow$ (test mode selection pattern setup time)	tset0	100			ns	
RB<7:4> hold time after $\overline{MCLR}\uparrow$ (test mode selection pattern hold time)	thld0	100			ns	
Serial Program/Verify						
Data in setup time before clock↓	tset1	100			ns	
Data in hold time after clock↓	thld1	100			ns	
Data input not driven to next clock input (delay required between command/data or command/command)	tdly1	1.0			µs	
Delay between clock↓ to clock↑ of next command or data	tdly2	1.0			µs	
Clock↑ to data out valid (during read data	tdly3	80			ns	
Parallel Program/Verify						
Data in setup time before clock↓	tset3	1			µs	
Data in hold time after clock↓	thld3	1			µs	
RB6 and RB7 setup time before clock↓	tset1	1			µs	
RB6 and RB7 hold time after clock↓	thld1	1			µs	
RT (clock)↓ to RT (clock)↑	tdly4	2			µs	
RB7 (data/command select input) setup before RT (clock)↑	tset2	1			µs	
RB7 (data/command select input) hold time after RT (clock)↓	thld2	1			µs	
RT (clock)↑ to data out valid	tdly5	1			µs	

(cont.)

1.3.1 AC/DC TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE (Cont.)

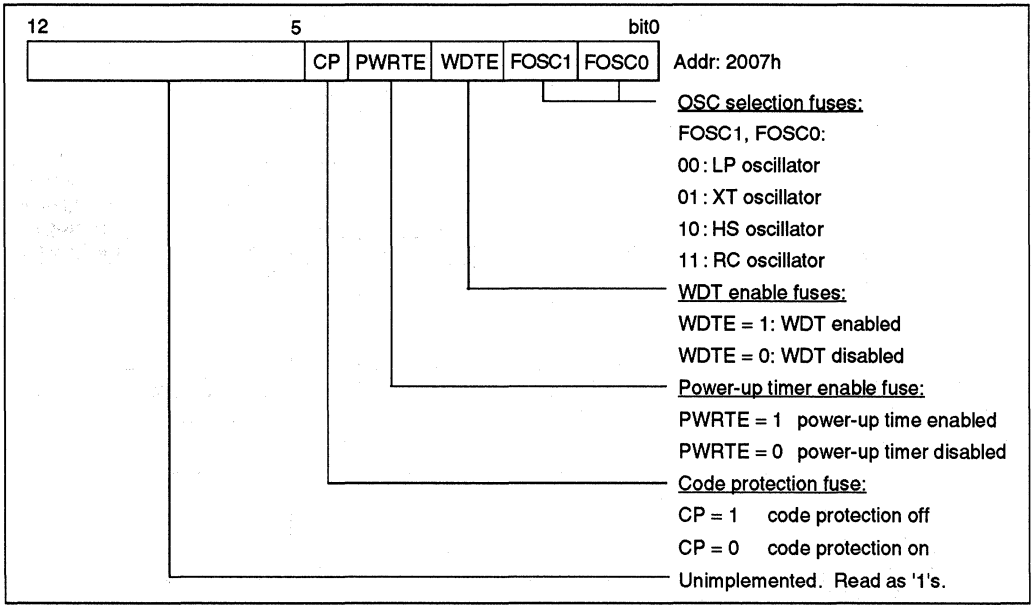
AC/DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions Operating temperature 0 ≤ TA ≤ +70°C, unless otherwise stated Operating voltage 4.5V ≤ VDD ≤ 5.5V, unless otherwise stated					
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions/Comments**
Parallel Program/Verify (cont.)						
RB6 (hi/lo select) valid to data out valid	tdly6	100			ns	
Programming pulse width	tprog	10			ms	
Time delay from program to compare (HV discharge time)	tdis	0.5			µs	

Note 1: Program must be verified at the minimum and maximum VDD limits for the part.
Note 2: VIHH must be higher than VDD + 4.5V to stay in programming/verify mode.

2.0 CONFIGURATION FUSES

The PIC16C84 has five configuration fuses, which are EEPROM bits. These fuses can be programmed (reads '0') or left unprogrammed (reads '1') to select various device configurations.

FIGURE 2.0.1 - CONFIGURATION WORD



2.1 Embedding Configuration Fuse and ID Information In the Hex File

To allow portability of code, the programmer is required to read the fuse and ID locations from the hex file when loading the hex file. If fuse information was not present in the hex file then a simple warning message may be issued. Similarly, while saving a hex file, all fuse and ID information must be included. An option to not include this information may be provided.

Specifically for the PIC16C84, the EEPROM data memory should also be embedded in the hex file (see Section 3.0).

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

2.2 Code Protection

The code in the program memory and data in the data memory can be protected by programming the code protect fuse (CP).

When code protected, the contents of the program memory cannot be read out in a way that the program code can be reconstructed. It is also not possible to read out the contents of the data memory. In addition, it is not possible to program any memory locations (data or program) while code protection is on.

2.2.1 VERIFYING A CODE-PROTECTED PIC16C84

When code protected verifying any program memory location will read a scrambled output which looks like "0000000xxxxxxx" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

a. First, program and verify a good device without code protecting it.

b. Next, blow its code protection fuse and then load its contents in a file.

c. Verify any code-protected PIC16C84 against this file.

Date memory can not be verified after code protection.

2.3 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code - identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

It is recommended that the user use only the lower 7-bits of the ID locations and always program the upper 7-bits as '1's.

2.2.2 DISABLING CODE-PROTECTION

It is recommended that the following procedure be performed before any other programming is attempted. It is also possible to turn code protection off (code protect fuse = 1) using this procedure; however, all data within the program memory and the data memory will be erased when this procedure is executed, and thus, the security of the data or code is not compromised.

Procedure to disable code protect:

a. Execute load configuration (with a '1' in bit 4, code protect).

b. Increment to fuse location (2007h)

c. Execute command (0001 - RB<3-0>)

d. Execute command (0111 - RB<3-0>)

e. Execute 'Begin Programming'

f. Wait 10ms

g. Execute command (0001 - RB<3-0>)

h. Execute command (0111 - RB<3-0>)

3.0 EMBEDDING DATA EEPROM CONTENTS IN HEX FILE

The programmer should be able to read data EEPROM information from a hex file and conversely (as an option) write data EEPROM contents to a hex file along with program memory information and fuse information.
The 64 data memory locations are logically mapped starting at address 2100h.

4.0 PROGRAMMING ALGORITHM REQUIRES VARIABLE VDD

The PIC16C84 uses an intelligent algorithm. The algorithm calls for program verification at VDD (min.) as well as VDD (max.). Verification at VDD (min.) guarantees good "erase margin". Verification at VDD (max) guarantees good "program margin".

The actual programming must be done with VDD in the VDDP range (4.5 - 5.5V).

VDDP = VCC range required during programming.
VDD min. = minimum operating VDD spec for the part.
VDD max. = maximum operating VDD spec for the part.

Programmers must verify the PIC16C84 at its specified VDD max. and VDD min. levels. Since Microchip may introduce future versions of the PIC16C84 with a broader VDD range, it is best that these levels are user selectable (defaults are ok). **Any programmer not meeting these requirements may only be classified as "prototype" or "development" programmer but not a "production" quality programmer.**

3

NOTES:

PIC17CXX EPROM Memory Programming Specification

1.0 PROGRAMMING THE PIC17CXX

The PIC17CXX is fundamentally programmed using the TABLWT instruction with the table pointer pointing to an internal EPROM location. Therefore, a user can program an EPROM location while executing code (even from internal EPROM).

For the convenience of a programmer developer, a "program & verify" routine is provided in the on-chip test program memory space, the program resides in ROM and not EPROM. Therefore, it is not erasable. The "program/verify" routine allows the user to load any address, program a location, verify a location or increment to the next location. It allows variable programming pulse width.

1.1 Hardware Requirements

Since the PIC17CXX under programming is actually executing code from "boot ROM", clock must be provided to the part. Furthermore, the PIC17CXX under programming may have any oscillator configuration (EC, XT, LF or RC). Therefore, the external clock driver must be able to overdrive pulldown in RC mode. CMOS drivers are required since the OSC1 input has a Schmitt trigger input with levels (typically) of 0.2 VDD and 0.8 VDD. See the PIC17C42 datasheet (DS30073) for exact specifications.

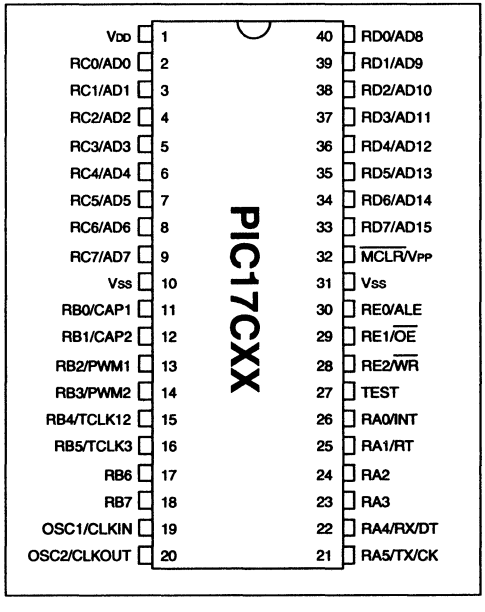
The PIC17C42 requires two programmable power supplies, one for VDD (2.0V to 6.5V recommended) and one for VPP (12V to 14V). Both supplies should have a minimum resolution of 0.25V.

2.0 HOW TO ENTER PROGRAMMING MODE

To execute the programming routine, the user must hold TEST pin high, RA2, RA3 must be low and RA4 must be high (after power-up) while keeping $\overline{MCLR}$ low and then raise $\overline{MCLR}$ pin from VIL to VIHH (VDD or VPP). This will force FFE0h in the program counter and execution will begin at that location following reset. Execution is forced to Internal mode by overriding fuse configuration. The code protect fuse is not overwritten. The program immediately polls port RB<7:0> to determine a branch address. Presenting E1h on port RB will cause the program to jump to and execute the "program/verify" routine.

The sequence that enters the device into the programming/verify mode places all other logic into the reset state (the MCLR pin was initially at VIL). This means that all I/O are in the reset state (High impedance inputs).

FIGURE A - 40L PDIP, CERDIP WINDOW PINOUT



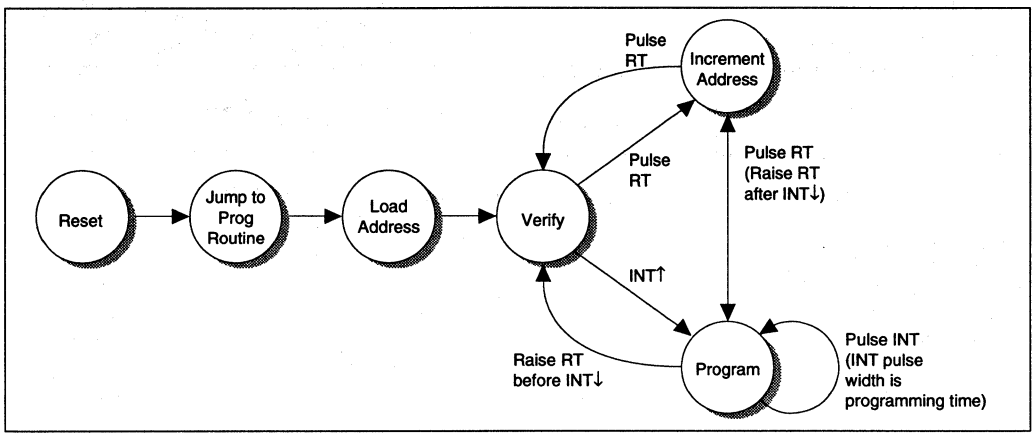
PORTB (RB) has internal weak pull-ups which are active during the programming mode. When TEST pin is high, Power-On Reset and Oscillator Start-up Timers are disabled.

2.1 PROGRAM/VERIFY MODE

The program/verify mode is intended for full-feature programmers. This mode offers the following capabilities:

a. Load any arbitrary 16-bit address to start program and/or verify at that location.
b. Increment address to program/verify the next location.
c. Allows arbitrary length programming pulse width.
d. Following a "verify" allows option to program the same location or increment and verify the next location.
e. Following a "program" allows options to program the same location again, verify the same location or to increment and verify the next location.

FIGURE 2.1.1 - PROGRAMMING/VERIFY STATE DIAGRAM



2.1.1 LOADING NEW ADDRESS

The program allows new address to be loaded right out of reset. A 16-bit address is presented on ports RB (high byte) and RC (low byte) and the RT is pulsed (0 → 1, then 1 → 0). The address is latched on the rising edge of RT. See timing diagrams for details. After loading address the program automatically goes into a "verify cycle". To load a new address at any time, the PIC17C42 must be reset and this programming mode re-entered.

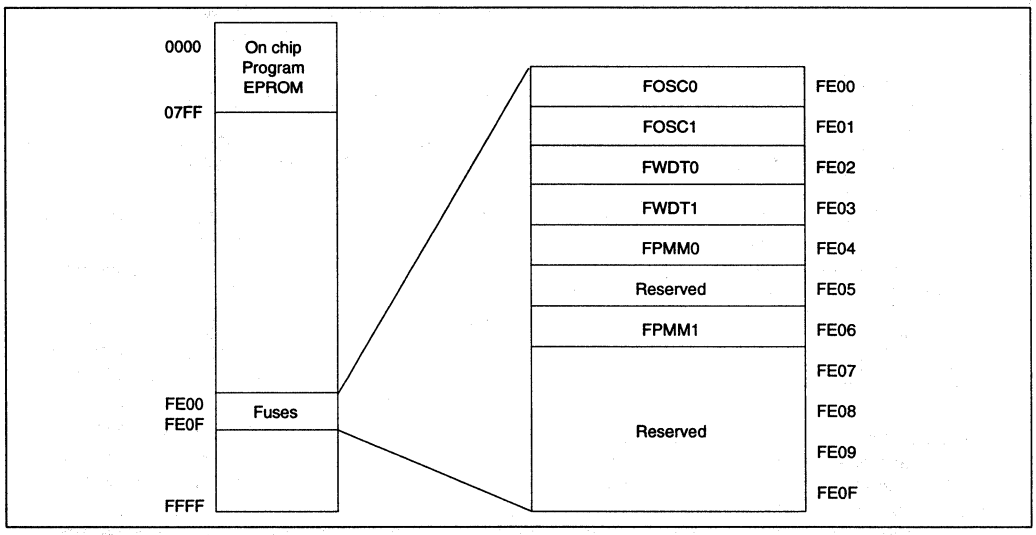
2.1.2 VERIFY (OR READ) MODE

"Verify mode" can be entered from "Load address" mode, "program mode" or "verify mode". In verify mode pulsing RT will turn on ports RB and RC output drivers and output the 16-bit value from the current location. Pulsing RT again will increment location count and be ready for the next verify cycle. Pulsing INT will begin a program cycle.

2.1.3 PROGRAM CYCLE

"Program cycle" is entered from "verify cycle" or program cycle" itself. After a verify, pulsing INT will begin a program cycle. 16-bit data must be presented on ports RB (high byte) and RC (low byte) before INT is raised.

FIGURE 2.1.2 - PIC17C42 PROGRAM MEMORY MAP



The data is sampled 3 Tcy after the rising edge of INT. Programming continues for the duration of INT pulse.

At the end of programming the user can choose one of three different routes. If RT is kept low and INT is pulsed again, the same location will be programmed again. This is useful for applying over programming pulses. If RT is raised before INT falling edge, then a verify cycle is started without address increment. Raising RT after INT goes low will increment address and begin verify cycle on the next address.

3.0 CONFIGURATION FUSES

Configuration fuses are programmable EPROM bits that can be programmed (reads '0') or left unprogrammed (reads '1') to select between options (e.g. operating modes). For simplicity of programming they are mapped into program memory. Each fuse is assigned one program memory location. In erased condition a fuse will read as '1'. To program (or "blow") a fuse, the user needs to write to the fuse address. The data is immaterial; the very act of writing will blow the fuse. The fuses and their address are shown in the table below. **The programmer should not program (i.e. not write a '0') the reserved locations to avoid unpredicatable results and to be compatible with future variations of the PIC17C42.**

TABLE 3.0.1 - MAPPING OF CONFIGURATION FUSES

Fuse	Address	Function
FOSC0	FE00h	FOSC1, FOSC0 = 00 : LF oscillator mode
FOSC1	FE01h	01 : RC oscillator mode
		10 : XT oscillator mode
		11 : EC (external clock mode)
FWDT0	FE02h	FWDT1, FWDT0 = 10 : WDT prescale is 256
FWDT1	FE03h	01 : WDT prescale is 64
		11 : WDT prescale is 1
		00 : WDT is off (normal timer)
FPMM0	FE04h	FPMM1, FPMM0 = 00 : Microcontroller mode (code protected)
FPMM1	FE06h	10 : Microcontroller mode
		01 : Extended micrcontroller mode
		11 : Microprocessor mode

3.1 Reading Configuration Fuses

For simplicity, reading any fuse in address range FE00: FE07h will read all eight fuse values in the lower byte and all 1's in the upper byte. Fuse located at FE00h will show up in bit 0 and so on.

1 1 1 1	1 1 1 1	reserved	FPMM1	reserved	FPMM0	FWDT1	FWDT0	FOSC1	FOSC0
									bit0

When code protected, reading any program memory location will read out a scrambled output "0000 0000 xxxx xxxx" (binary) where x = 0 or 1. To verify a device after code protection follow this procedure:

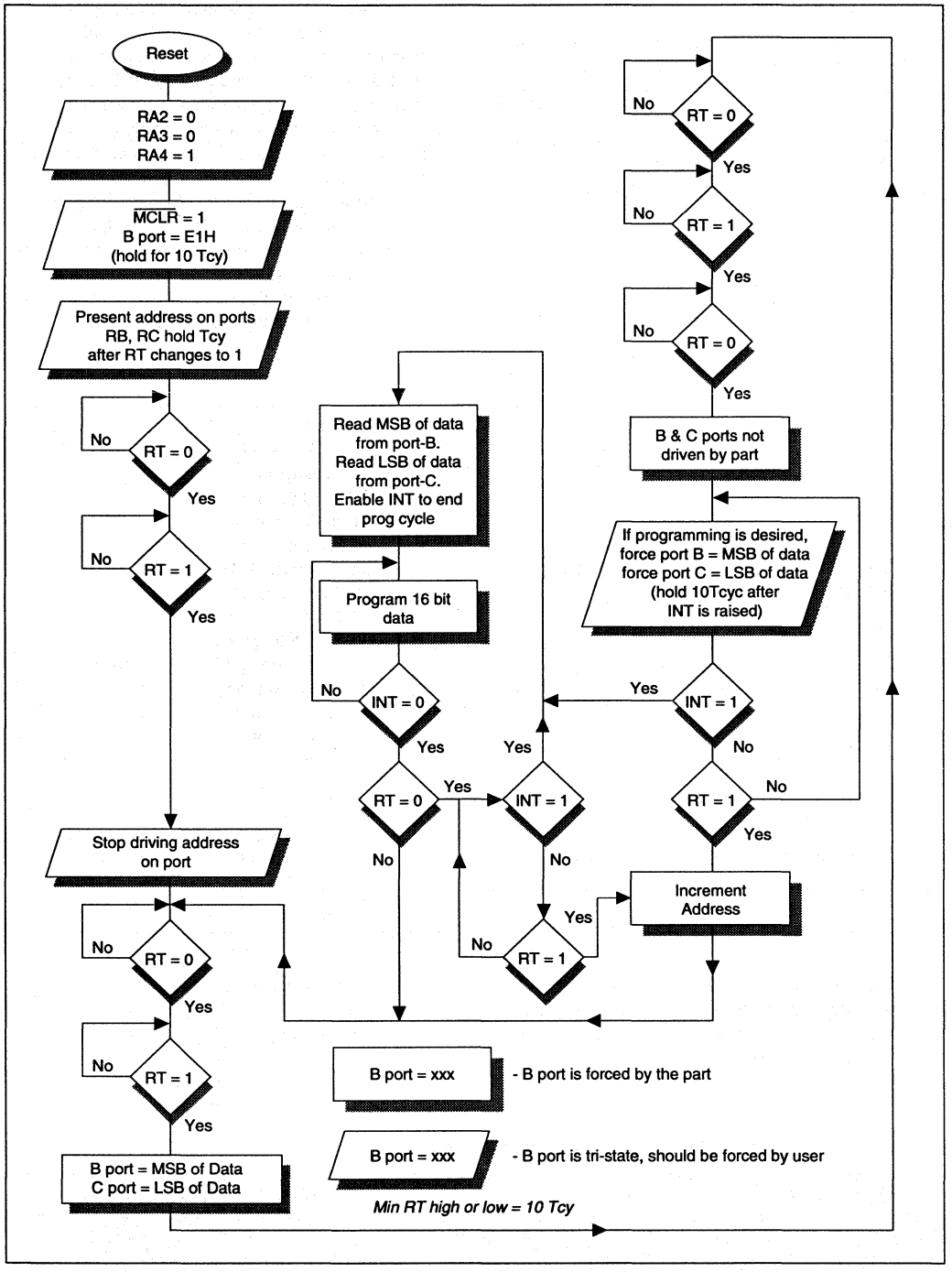
a. First, program and verify a device without code protection.
b. Next, blow its code protection fuse(s) and read it into a file.
c. Verify any code protected PIC17C42 against this this file.

3.2 Embedding Configuration Fuse Information in the Hex File

To allow portability of code, a PIC17C42 programmer is required to read the fuse locations from the hex file when loading the hex file. If fuse information was not present in the hex file then a simple warning message may be issued. Similarly, while saving a hex file, all fuse information must be included. An option to not include the fuse information may be provided. When embedding fuse information in the hex file, it should be to address FE00H.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

FIGURE 4.0.1 - PROGRAMMING ROUTINE FLOWCHART



5.0 PROGRAMMING SPECIFICATIONS

FIGURE 5.0.1 - PROGRAMMING AND VERIFY TIMINGS I

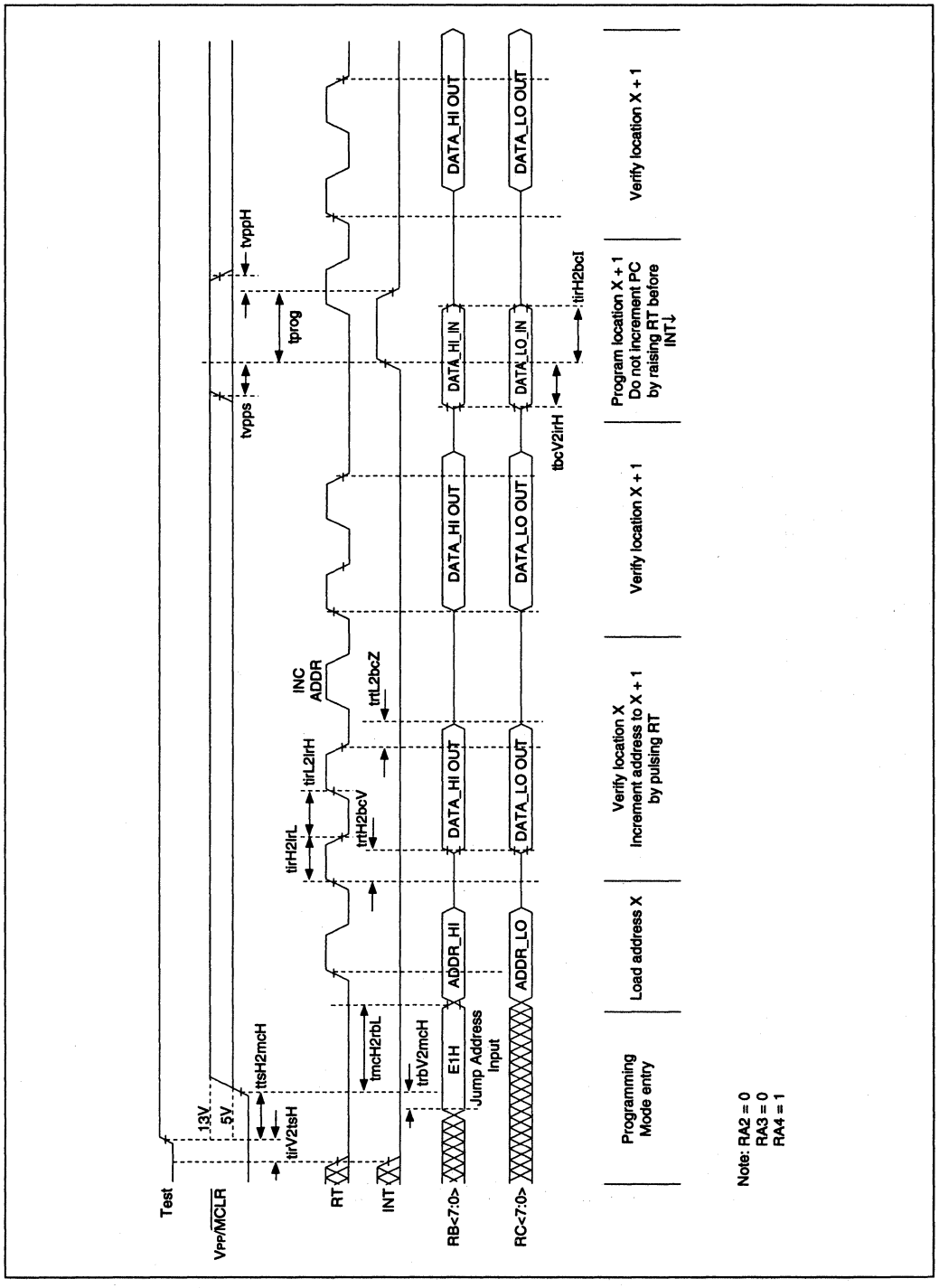


FIGURE 5.0.2 - PROGRAMMING AND VERIFY TIMINGS II

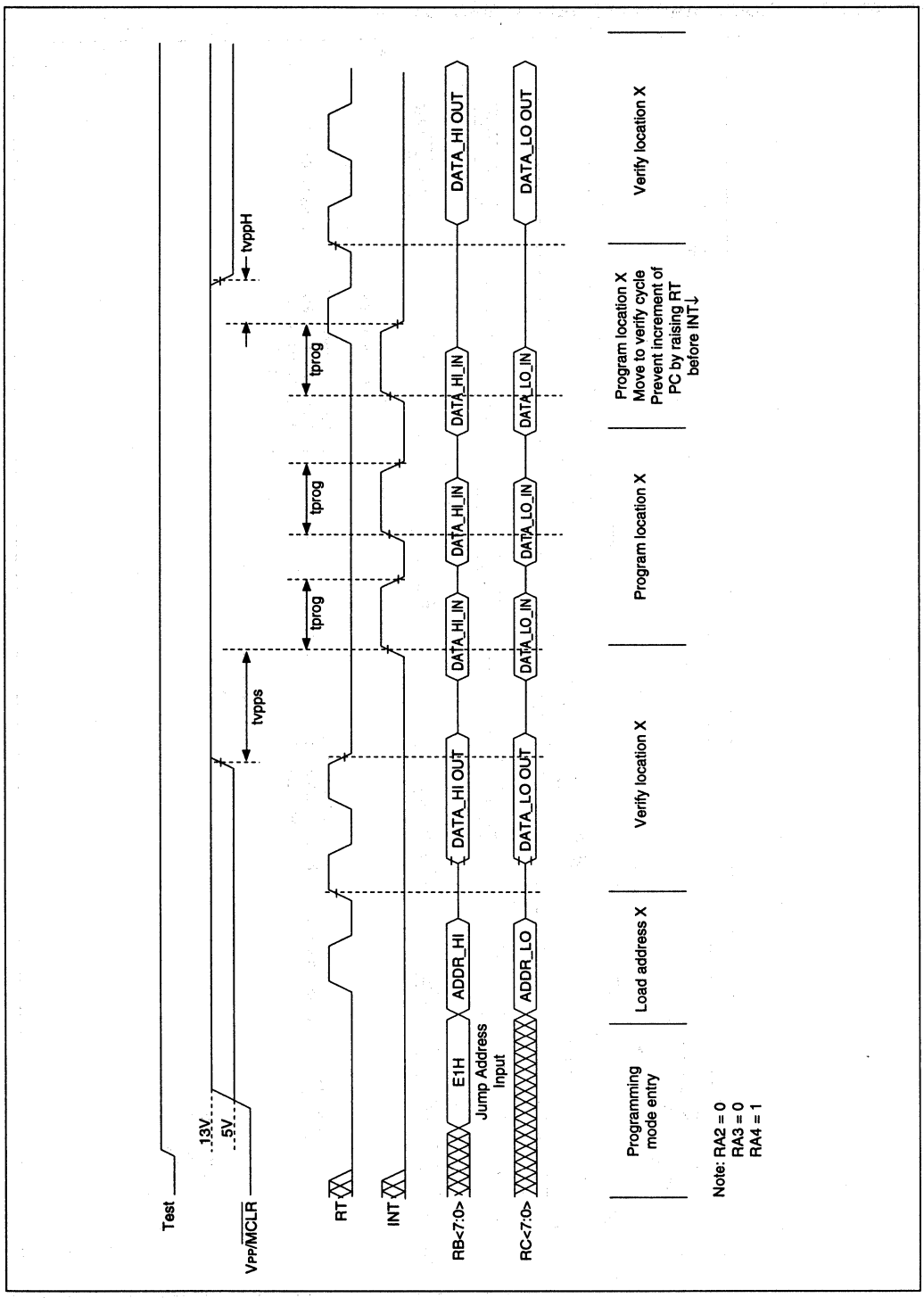


FIGURE 5.0.3 - PROGRAMMING AND VERIFY TIMINGS III

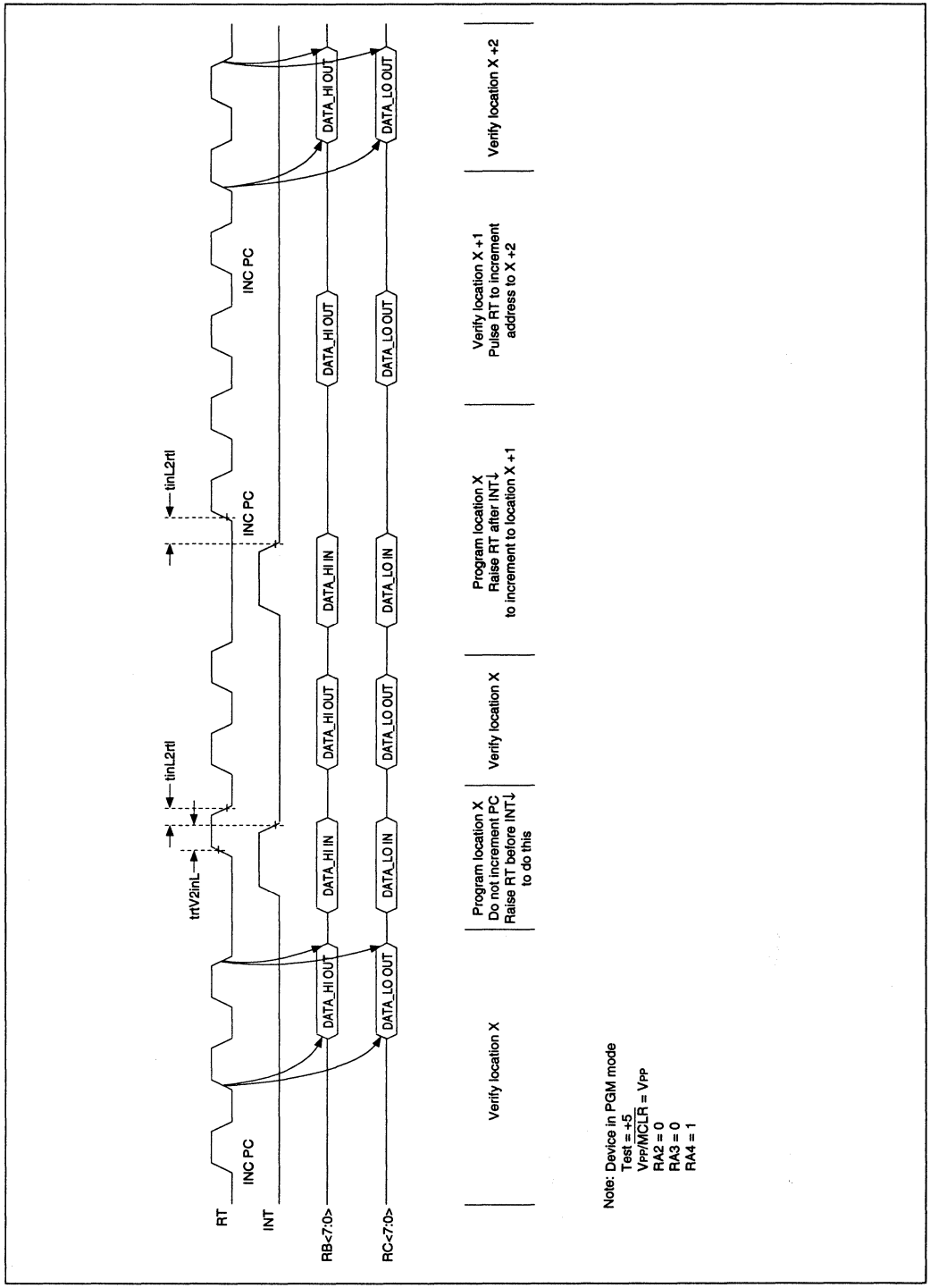
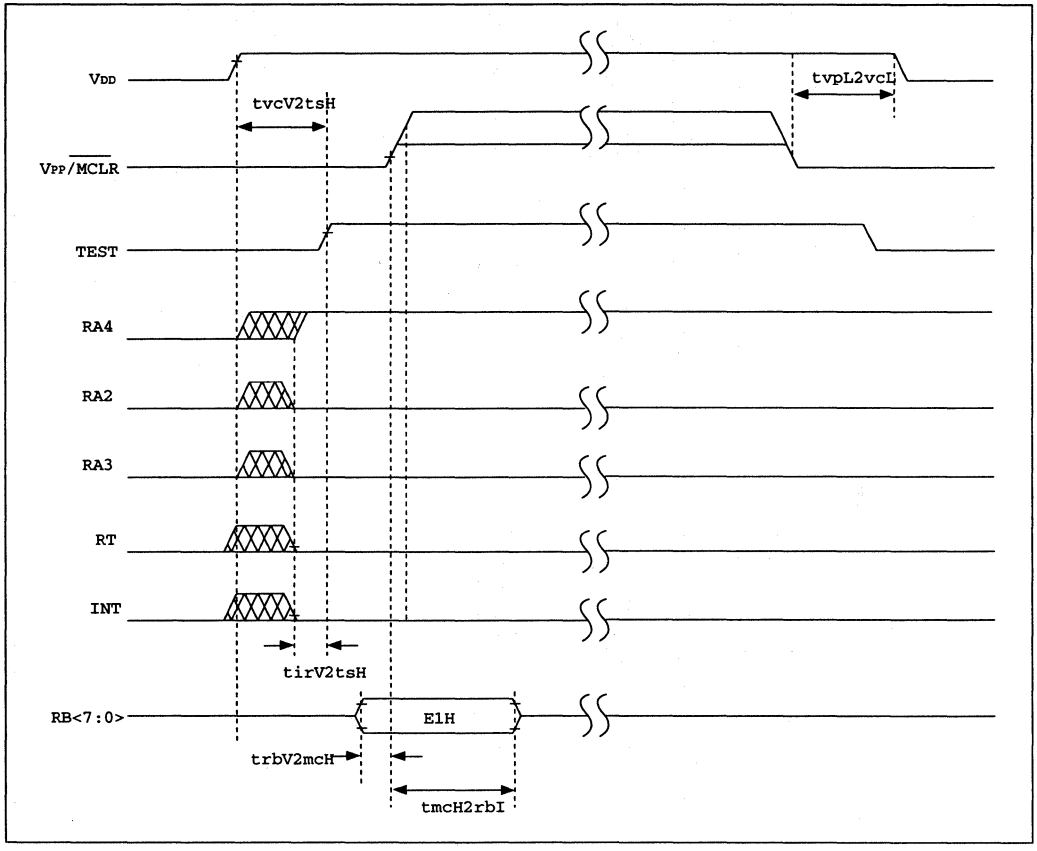


FIGURE 5.0.4 - POWER-UP/DOWN SEQUENCE FOR PROGRAMMING



6.0 AC/DC SPECIFICATIONS FOR PROGRAMMING

		Standard Operating Conditions (unless otherwise stated) Operating temperature 10°C ≤ TA ≤+40°C Operating voltage 4.5V <VCC <5.5V				
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Programming voltage on VPP/$\overline{MCLR}$ pin	VPP	12.5		13.5	V	Note 1
Programming current on VPP/$\overline{MCLR}$ pin	IPP		25	50	mA	
Supply voltage during programming	VDDP	4.5	5.0	5.5	V	
Osc/clockin frequency during programming	FOSCP	4		10	MHz	
Instruction cycle	TCY	1		0.4	µs	TCY = 4/FOSCP
Supply current during programming	IDDP			30	mA	Freq = 10 MHz, VDD = 5.5V
Supply voltage during verify	VDDV	VDD min.		VDD max.	V	Note 2
INT, RT, RA2, RA3, RA4 setup before TEST↑	tirV2tsH	1			µs	
TEST↑ to $\overline{MCLR}$↑	ttsH2mcH	1			µs	
RC<7:0>, RB<7:0>valid to RT or INT↑ :Address/ Data input setup time	tbcV2irH	0			µs	
RT or INT↑ to RB<7:0>, RC<7:0> invalid; Address datahold time	tirH2bcI	10 Tcy			µs	
RT↓ to RB<7:0>, RC<7:0> high impedance	trtL2rbcZ			8 Tcy		
RT↑ to data out valid	trtH2bcV			10 Tcy		
Programming pulse width	tprog	10	100	1000	µs	
INT, RT high pulse width	tirH2irL	10 Tcy			µs	
INT, RT low pulse width	tirL2irH	10 Tcy			µs	
RT↑ before INT↓ (to go from prog cycle to verify w/o increment)	trtV2inL	0			µs	
RT valid after INT (to select increment or no increment going from program to verify cycle	tinL2rtI	10 Tcy			µs	
VPP setup time before INT↑	tvpps	100			µs	Note 1
VPP hold time after INT↓	tvpph	0			µs	Note 1
VDD stable to TEST↑	tvdV2tsH	10			ms	
RB input (E1h) valid to VPP/$\overline{MCLR}$↑	trbV2mcH	0			µs	
RB input (E1h) hold after VPP/$\overline{MCLR}$↑	tmcH2rbI	10 Tcy			ns	
VDD power down after VPP power down	tvpL2vdL	10			ms	

Note 1: VPP/$\overline{MCLR}$ pin can be kept at VPP level (12.5V - 13.5V) at times other than programming.
Note 2: Program must be verified at the minimum and maximum VDD limits for the part.

7.0 PROGRAMMING ALGORITHM REQUIRES VARIABLE VDD

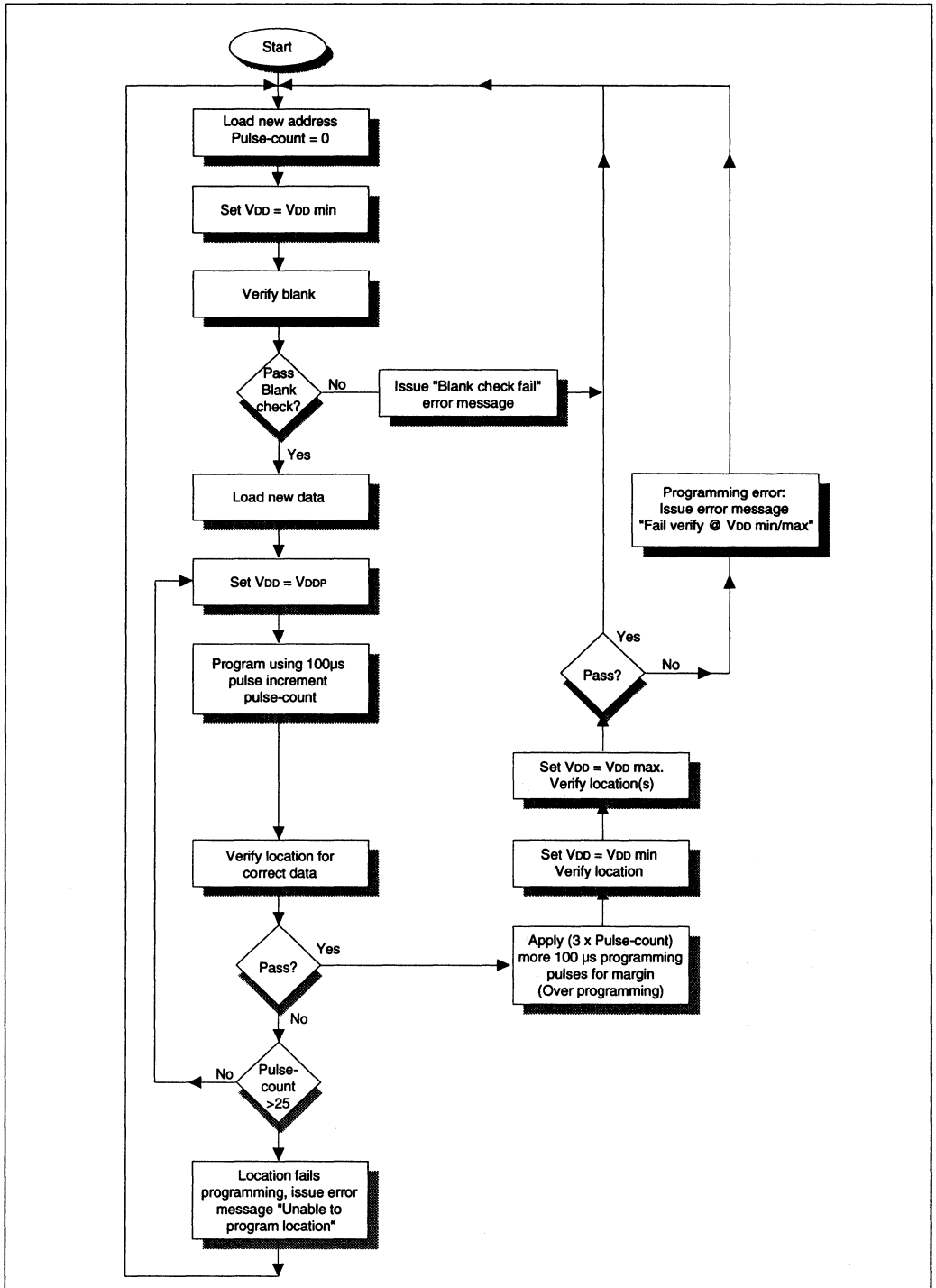
The PIC17CXX uses an intelligent algorithm. The algorithm calls for program verification at VDD (min.) as well as VDD (max.). Verification at VDD (min.) guarantees good "erase margin". Verification at VDD (max) guarantees good "program margin". Three times (3X) additional pulses will increase program margin then beyond VDD (max.) and insure safe operation in user system.

The actual programming must be done with VDD in the VDDP range (4.5 - 5.5V).

VDDP = VDD range required during programming.
VDD min. = minimum operating VDD spec for the part.
VDD max. = maximum operating VCC spec for the part.

Programmers must verify the PIC17CXX at its specified VDD max. and VDD min. levels. Since Microchip may introduce future versions of the PIC17CXX with a broader VDD range, it is best that these levels are user selectable (defaults are ok). Any programmer not meeting these requirements may only be classified as "prototype" or "development" programmer but not a "production" quality programmer.

FIGURE 7.2 - RECOMMENDED PROGRAMMING ALGORITHM



NOTES:

MICROCHIP

SQTP Specification for PIC16C5X

SQTP™ (Serialized Quick Turn Programming) Specification for PIC16C5X

OVERVIEW

Serialization is a method of programming PIC16C5X microcontrollers whereby each chip is programmed with a slightly different code. Typically, all locations are programmed with the same basic code except for a few continuous bytes which are programmed with a different number (referred to as 'key' or 'ID number' or 'serial number') in each member. Typical applications of such programming are remote transmitters for car alarms or garage door openers where each unit must have a different access code.

Microchip offers a flexible SQTP program, whereby a customer can simply specify the nature of serialization. The 'serial number' generation and programming will be taken care of by the factory.

1.0 DEVICES CURRENTLY SUPPORTED

PIC16C54 osc type=XT, RC, LP, HS Packages=PDIP, SOIC
PIC16C55 osc type=XT, RC, LP, HS Packages=PDIP, SOIC
PIC16C56 osc type=XT, RC, LP, HS Packages=PDIP, SOIC
PIC16C57 osc type=XT, RC, LP, HS Packages=PDIP, SOIC

Other device types are being added. Please consult a Microchip representative or Microchip sales person.

2.0 SERIALIZATION SCHEME SUPPORTED

2.1 Locations:

The serial number must reside in continuous locations with up to eight locations used. Furthermore these locations must be coded as 8NN (RETLW NN, where NN=8-bit random code) in the finished product. For details on how the RETLW instruction is typically used for serialization purposes, please see Appendix A. The customer code must be supplied without the serial code in these locations. These locations must be 8FFh in the customer code provided to Microchip. Microchip will insert the serial code at these locations during programming. Hex files must be in Intel hex 8-bit merged format. See Appendix B for details.

2.2 Numbering Schemes:

Random: Truly random numbers are generated. However, there is no guarantee that the numbers will be non-repeating although the probability of such an occurrence will be infinitesimally small for a reasonably large field.

Pseudo-Random*: Pseudo-random sequences of requested length (e.g. 32-bit long if four locations are used) starting with a 'seed value' selected by the factory. The customer may optionally specify the starting value. Pseudo-random sequences, by definition are non-repeating. See Appendix C for polynomials used to generate the numbers.

Sequential: Sequential numbers are generated. User specifies the "starting number" and an increment value. In sequential numbering, the least significant digit is in the lowest memory location. The increment value must be between 1 and 255.

Numbers are always in hex and not in BCD or any other format.

3.0 PROGRAMMING SEQUENCE

The factory will program the "basic code" first, then program the serial number and finally program the code-protection fuse. Program memory will be verified at each stage except after code protection. Optionally, the factory may choose to program the "basic code" and the "serial number" at the same time. The customer may specify an ID number (four hex digits) to be programmed in the ID locations or elect to leave them unprogrammed.

4.0 SAMPLES

Three (3) verification samples will be provided. These will be programmed with factory selected random or sequential codes in the serialization locations. The three parts will be programmed with three different serial codes. If order entry has been completed, then the samples will reflect the first three codes. If code protection is requested, then one of the three samples will be code protected.

5.0 THE FOLLOWING LIMITATIONS APPLY TO THE SQTP PROGRAM

1. During shipment of serialized parts, no particular sequence can be guaranteed.
2. In sequential or pseudo-random numbering scheme, there may be missing serial numbers (e.g. due to QC sampling).
3. A list of serial numbers programmed can not be provided, nor will such a list be generated or maintained by Microchip.
4. For sequential and pseudo-random numbering schemes, Microchip will maintain last number used in last shipment and use the next number as the starting number for the next shipment. The customer should be prepared to provide a "new starting number" in the event the flow is disrupted due to unforeseen events.

APPENDIX A

Implementing a table in the program memory of PIC16C5X:

The PIC16C5X uses Harvard architecture, in which the program memory is separate from data memory. All instructions operate on data that is fetched from the register file or data memory. Since there are no instructions to read from or write to the program memory, simply storing data words in program memory is of no use. There is, however, a simple and elegant way to implement constant tables in the program memory by using the RETLW instruction. This instruction returns from a subroutine as well as loads an 8-bit constant into the W register. The following example shows how to get a byte of "serial information" from the table stored at location 000h in PIC16C54:

```
          ORG    0          ;store serial
numbers
          RETLW  0FFh
          RETLW  0FFh
          RETLW  0FFh
          RETLW  0FFh
          RETLW  0FFh
          RETLW  0FFh
          RETLW  0FFh
          RETLW  0FFh       ;end of serial
                            ;numbers
          o
          o
main_prog ORG    XYZ        ;This is main
program
          o
          o
          MOVLW  byte_num   ;byte_num = 0 for
1st                                 ;byte
          CALL   get_1byte      ;
          o
          o
get_1byte MOVWF  PC         ;write W to program
                            ;counter
                            ;W = offset = 0 for
                            ;1st byte
                            ;end of get_1byte sub
                            ;routine
          o
          o
          o
          END
```

The next example shows how a serial number may reside at location other than 000h.

```
main_prog ORG    XYZ        ;This is main
program
          o
          o
          MOVLW  byte_num   ;byte_num = 0 for
1st                                 ;byte
          CALL   get_1byte      ;
          o
          o
get_1byte ADDWF  PC         ;W = offset
          RETLW  0ffh       ;
          RETLW  0ffh       ;
          RETLW  0ffh       ;
          RETLW  0ffh       ;
          RETLW  0ffh       ;
          RETLW  0ffh       ;
          RETLW  0ffh       ;
          RETLW  0ffh       ;end of serial
                            ;numbers
          o
          o
          END
```

APPENDIX B

Standard hex file format for serial programming:

The hex file containing the 'serial numbers' will be in Intel hex 8-bit format. Since the PIC16C5X has 12-bit data words, all addresses are doubled in this hex format. Each line of the hex file will be for a new part. Each line can contain only up to 16 bytes (i.e. eight PIC16C5X instruction words). The format is as follows:

:NNAAAATTHHHHHH.....HHCC

where:

NN = byte count on current line (max 10h allowed)

AAAA = address in four hex digits

TT = record type, always 00 except 01 for EOF

HH = Two digit hex data byte

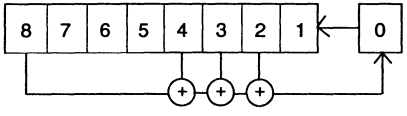
CC = Two digit hex checksum

APPENDIX C

Pseudo-random numbers are generated using modulo-2 primitive polynomials. This method guarantees to produce a sequence of maximal length, i.e., cycle through all possible sequence of n bits before it repeats. By providing a seed value as the initial bit pattern (the only combination not used is all 0's), one can get 2^n-1 random bits before the sequence repeats itself. Microchip will only support pseudo-random serial numbers for bit lengths 8, 16, 24, 32, 40, 48, 56 and 64 (i.e., 1-8 locations). The polynomials used are:

8 bit:	$x^8 + x^4 + x^3 + x^2 + 1$
16 bit:	$x^{16} + x^5 + x^3 + x^2 + 1$
24 bit:	$x^{24} + x^4 + x^3 + x + 1$
32 bit:	$x^{32} + x^7 + x^5 + x^3 + x^2 + x + 1$
40 bit:	$x^{40} + x^5 + x^4 + x^3 + 1$
48 bit:	$x^{48} + x^7 + x^5 + x^4 + x^2 + x + 1$
56 bit:	$x^{56} + x^7 + x^4 + x^2 + 1$
64 bit:	$x^{64} + x^4 + x^3 + x + 1$

To implement the 8-bit polynomial requires XORing the non-zero bits of the polynomial (shown as a shift register below) and shift on the resetting bit back into the shift register.



NOTES:

SECTION 4
ASSP PRODUCT SPECIFICATIONS

MICROCHIP

MTA11200

TRUEGAUGE™ Intelligent Battery Management I.C.

FEATURES

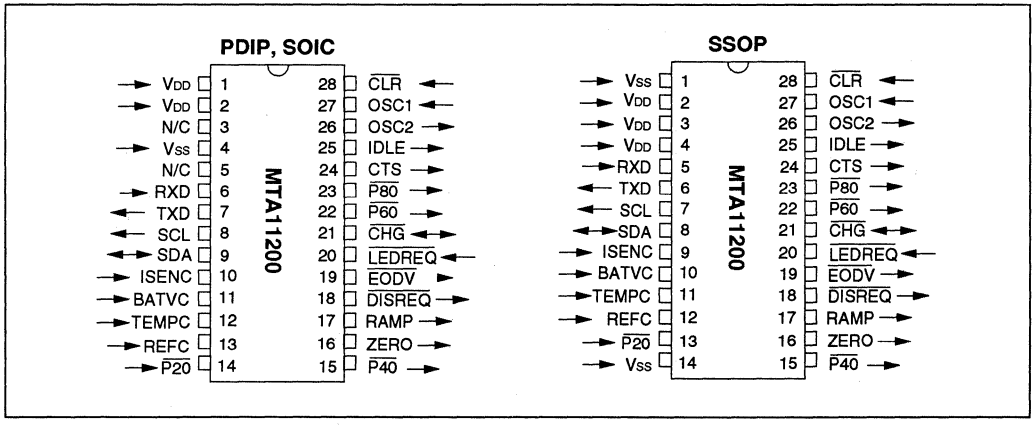
- Digitally integrates battery charge and discharge current to provide an accurate state of charge indication
- Operates with NiCd, NiMH, or Lead Acid battery packs containing as few as three cells
- Provides real-time battery data via a single-wire interface
  - Remaining capacity in percentage
  - Total Capacity in mA-Hr
  - Battery Voltage
  - Battery Temperature
  - Battery Current
- -ΔV, ΔT/dt, or maximum voltage fast charge termination
- Provides three overcharge protection mechanisms:
  - Elapsed time fast charge termination
  - Over and Under Temperature protection
  - Over-Voltage protection
- Automatically measures and updates the total capacity of the battery
- Automatic battery conditioning requests at regular intervals based on usage

BENEFITS

- Provides accurate, real-time battery capacity information
- Extends battery life through automatic, regular conditioning cycles
- Permits use of an inexpensive current source for battery charging
- Allows rapid and reliable battery recharging with multiple backup safety mechanisms
- Avoids errors due to battery noise, variations in load current, and deep discharge situations
- Provides total capacity data to help detect imminent battery failure
- Assists in efficient power management

4

FIGURE A - PIN CONFIGURATIONS



TrueGauge name and logo are trademarks of Microchip Technology Inc.

DESCRIPTION

The MTA11200 is the heart of a simple, low-cost, yet fully featured solution to battery monitoring and charging. It is designed to operate with either nickel cadmium, nickel-metal hydride, or lead acid battery packs.

By digitally integrating battery charge and discharge current the MTA11200 accurately determines the battery's state of charge. The battery's total capacity is automatically measured and factored into the state of charge calculation. Thus, an accurate indication of percentage of battery capacity remaining is determined.

Automatic total capacity measurement occurs during battery conditioning cycles when the battery is cycled from full charge to full discharge. The MTA11200 requests conditioning cycles at regular intervals based on battery usage to extend battery life. Additionally, the MTA11200 continually monitors battery condition and can output the following battery parameters via RS-232 1-wire interface or optional 3-wire bi-directional serial link: remaining capacity, total capacity, voltage, current, temperature, error flag, etc.

The MTA11200 is a 28-pin low power CMOS integrated circuit. Combined with a few simple external components, a complete battery maintenance system can be realized.

APPLICATIONS

The MTA11200 is ideally suited for use in portable computers, portable video equipment, cellular phones, and other products relying on rechargeable battery technology. The MTA11200 excels in applications where an accurate "fuel gauge" is desired to prevent interruption in use or data loss due to insufficient battery power.

1.0 PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
TXD	Output	RS-232 transmit data 9600,N,8,1. The MTA11200 transmits command responses and measured battery data to a host via this pin
RXD	Input	RS-232 receive data 9600,N,8,1. The MTA11200 receives commands and data from a host via this pin. This pin can be a no-connect if the MTA11200 is operating in the transmit only (broadcast) mode
CTS	Output	RS-232 clear to send output. The MTA11200 signals that it is ready to receive a command from the host via this pin. This pin can be a no-connect if the MTA11200 is operating in the transmit only mode
SCL	OC-Output	I²C™ format serial clock to an external Serial EEPROM
SDA	Input/Output	I²C format serial data to and from external Serial EEPROM
REFC	Input	Reference voltage comparator sense input
BATVC	Input	Battery Voltage comparator sense input
TEMPC	Input	Temperature comparator sense input
ISENC	Input	Charge and Discharge Current comparator sense input
ZERO	Output	Comparator offset compensation control
RAMP	Output	A/D voltage ramp control
$\overline{\text{DISREQ}}$	OC-Output	Discharge request output for external charger/discharger control. Active low when battery discharge cycle is requested. Inactive tristated
$\overline{\text{EODV}}$	OC-Output	Battery at End Of Discharge Voltage output, active low, inactive tristated
$\overline{\text{CHG}}$	Input/Output	Charge request output and host or charger present input. When in output mode, fast charge request is active low when capacity is less than value stored in EEPROM. Inactive tristate. In input mode charger present is indicated when input is high. A 100K pull down is required. Externally pulled high to command ON (as opposed to STANDBY) mode
$\overline{\text{LEDREQ}}$	Input	LED request switch input for momentary contact switch. Enables LED outputs for ~1.75 seconds when input goes low
$\overline{\text{P20}}$	OC-Output	Battery >20% full, LED drive, active low, inactive tristated
$\overline{\text{P40}}$	OC-Output	Battery >40% full, LED drive, active low, inactive tristated
$\overline{\text{P60}}$	OC-Output	Battery >60% full, LED drive, active low, inactive tristated
$\overline{\text{P80}}$	OC-Output	Battery >80% full, LED drive, active low, inactive tristated
IDLE	Output	Standby mode output, shuts down external circuits, active high
OSC2	Output	4.0 MHz ceramic or crystal oscillator output
OSC1	Input	4.0 MHz ceramic or crystal oscillator input
$\overline{\text{CLR}}$	Input	Power on reset input
V_{DD}	Pwr	
Vss	Gnd	

I²C is a trademark of Philips Corporation.

2.0 OVERVIEW

The MTA11200 determines the state of charge of a battery by integrating all the current going into and out of a NiCd, NiMH, or Lead Acid rechargeable battery pack. Compensation factors that adjust for battery non-linearity and environmental conditions are continuously applied to the state of charge calculation. The MTA11200 also performs the charge controller function of a battery charging system. It can directly control a "dumb" current source charging supply to provide both a high current fast charge and a long term maintenance (trickle) charge. The battery's state of charge is communicated by the MTA11200's four LED outputs and by a 9600 baud RS-232 serial link. Additionally, battery voltage, current, temperature, measured total capacity, and history information are available via the RS-232 link.

System control parameters that are stored in an external EEPROM allow the operation of the MTA11200 to be customized for use with a wide variety of battery types and sizes. There are approximately 35 programmable system parameters stored in 128 bytes of external EEPROM. These parameters are listed alphabetically and described in detail in Section 5.0.

2.1 STANDBY State

The MTA11200 has two states of operation: the ON state and a low power STANDBY state. The MTA11200 enters the STANDBY state when it senses that the battery is not connected to any external equipment (via the CHG pin) and therefore is not in use. In this low power state, the battery voltage, temperature, and current flow are measured at 138 second intervals. The MTA11200 compensates for battery self-discharge by adjusting the state of charge indication based upon the temperature and the battery's available charge. The self-discharge compensation factors are highly programmable and allow the MTA11200 to accurately compute the decay in the battery's available charge for a wide variety of different battery types. In this STANDBY state, the battery's charge state can be communicated via the four LED outputs. The MTA11200's RS-232 link is disabled when in the STANDBY state to conserve power.

2.2 ON State

Exiting the STANDBY state and entering the "ON" state occurs when a connection to external equipment is detected. This indicates that the battery is in use or is being charged. The ON state is entered when the $\overline{CHG}$ pin is sampled at a high level. The $\overline{CHG}$ pin is sampled at a 1.75 second rate and the MTA11200 can be easily forced into the "ON" mode when the battery's host equipment is powered up or when the battery is connected to a charger. Battery voltage, temperature, and current flow are sampled at 1.75 second intervals in this state.

2.3 Monitoring and Charging System

The MTA11200 is designed as the main controller I.C. in a battery monitoring and charging system. Additionally, a few other components are required to implement an entire system. A Serial EEPROM that uses standard I^2C interface is required. Control parameters that customize the MTA11200 for a particular battery type and application are stored in the Serial EEPROM. Additionally, the actual battery capacity that is measured by the MTA11200 is routinely updated and stored in the EEPROM. The analog-to-digital conversion technique used by the MTA11200 is a timed voltage ramp system that uses an external quad comparator. This combination provides highly accurate conversions across a wide dynamic range of input levels. For example, the current measurement range is typically 5000:1 for charge or discharge current.

3.0. FUNCTIONAL DESCRIPTION

3.1 Charge State Indicator

The MTA11200 indicates the present state of charge in percentage relative to a full (100%) charge. The total capacity of the battery pack is measured and used as the reference value for calculating the present state of charge. The total capacity is obtained by numerically integrating discharge current only, over a complete discharge cycle. A separate numerical integration is performed using both charge and discharge currents. The result of this integration in relation to the measured capacity determines the present state of charge of the battery.

3.1.1 Measured Battery Capacity

Total battery capacity is automatically determined by measuring and integrating the total discharge current delivered by the battery during any uninterrupted (by charge current) and complete discharge cycle. This helps maintain the accuracy of the charge state indication over the life of the battery.

An automatic capacity measurement cycle begins when the battery is charged to its 100% capacity point. This occurs when fast charging is terminated by the MTA11200's internal charge controller. Additionally, if the MTA11200 receives a Start Capacity Measurement command, it allows the discharge measurement cycle to begin by defining the present state of the battery as the 100% capacity point.

Now, integration of the discharge current begins when measurable discharge current flows from the battery. The MTA11200 may enter the STANDBY state and not cause the measurement cycle to abort. However, a complete and uninterrupted discharge cycle must occur following the start of discharge. If, after the start of discharge, the battery discharge current is reduced to zero, or if charge current is detected, the measurement cycle will be aborted.

If the discharge cycle continues until the battery reaches the programmed (in EEPROM) End Of Discharge Voltage (EODV), the capacity measurement cycle is completed. This measured battery capacity replaces the value previously stored in EEPROM at location MEACAP and becomes the new basis for the charge state calculation. From this point forward the MTA11200 will integrate all charge and discharge current and calculate battery self-discharge rates in relation to the stored measured capacity.

Long term accuracy of the state of charge calculation is maintained by regularly referencing known battery capacity points. When the fast charge termination point is detected, the state of charge indicator will be adjusted to indicate 100% capacity remaining. When the battery voltage reaches the end of discharge voltage point during discharge, the state of charge indicator will be adjusted to 0% if necessary. Additionally, the indicated battery capacity is restricted to a 0% to 100% range.

3.1.2 Nominal Battery Capacity

The MTA11200 reserves storage space for the battery's nominal (rated) capacity in the EEPROM at address NOMCAP. The MTA11200 does not use this value for any calculations. It is included so that a smart host may query the MTA11200 for the measured battery capacity and the nominal battery capacity. The host can then alert the user of impending battery "wear out" or failure.

3.1.3 Compensation Factors

The MTA11200 applies several compensation factors to the state of charge calculation. Compensation is required to maintain an accurate state of charge indication due to battery non-linearity and changing environmental conditions. These compensation factors are stored as lookup tables in the EEPROM.

When the battery is being charged, the charge current is integrated and the state of charge indication is calculated. However, since battery charging is not a 100% efficient operation, compensation is applied to the state of charge calculation. Charge efficiency is adjusted based upon the battery's present state of charge and it's temperature. Since most charging sources charge at a fixed rate, a separate compensation table for charge rate versus charge efficiency is not included. The compensation required for this rate is usually factored into the programmable temperature compensation versus charge efficiency table in EEPROM.

Self-discharge compensation occurs when the MTA11200 is in the STANDBY state. The MTA11200 measures the temperature once every 138 seconds and applies self-discharge compensation based on the temperature and the battery's state of charge. The self-discharge compensation factors are stored in a lookup table SDFT(31-0) in EEPROM.

Accuracy is improved by not applying compensation factors to the state of charge calculation when the battery is discharging. The MTA11200 maintains accuracy by avoiding the cumulative application of compensation factors to both the measured capacity discharge cycle and subsequent discharges. Since the measured capacity is based upon an actual measured discharge cycle that typically occurs during actual use in the host equipment, the discharge rate is automatically factored into the state of charge calculation.

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3.2 Charge Controller

The MTA11200 can control the complete charging regimen for several popular types of rechargeable batteries. Nickel Metal Hydride (NiMH), Nickel Cadmium (NiCd), and Lead Acid (Pb) batteries are all supported. The internal charge controller is designed to interface via a single wire to a "dumb" constant current source, thus forming a complete charging system. Two modes of charging are provided, a high current fast charge mode and a low current maintenance (or trickle) charge mode. Several "fail-safe" backup mechanisms are provided to ensure that the fast charge mode is not allowed to continue indefinitely. Fail-safe mechanisms for maintenance charge mode are also included to allow termination of all charging if the battery voltage or temperature is out of range.

3.2.1 Fast Charge

The fast charge mode is designed to allow high current rapid charging of a battery pack. Several techniques for fast charge termination are supported. They are: negative delta voltage (-ΔV), rate of change in temperature with respect to time (dT/dt) and absolute voltage. Typically, -ΔV termination is used with NiCd batteries, dT/dt is used with NiMH batteries, and voltage detection is used with lead acid (Pb) batteries. The MTA11200 uses one of these principal fast charge termination methods based upon the data in EEPROM location BATINFO. BATINFO is read immediately following a power on reset or during execution of a reset command. The MTA11200 will request fast charging via the $\overline{CHG}$ pin when the battery's state of charge is less than the percentage value programmed in EEPROM location TONCHG. Once fast charging begins, TONCHG has no effect. Fast charging will continue until the programmable limit for the selected principal fast charge method is reached or exceeded. Fast charging can also terminate if any one of the fast charge fail-safe limits are exceeded. Maintenance charge mode will always be entered after the fast charge mode terminates. Additionally, the LED outputs P20, P40, P60 and P80 are always enabled and indicating the battery state of charge when the MTA11200 is requesting fast charge and the battery is receiving fast charge current, regardless of the state of the LEDREQ input pin.

3.2.2 Fail-Safe Mechanisms

The MTA11200 provides several programmable fail-safe mechanisms. Temperature limits for both over-temperature and under-temperature are stored in EEPROM locations MAXTFC and MINTFC respectively. Fast charging will not be allowed if the battery temperature exceeds the over-temperature limit or is less than the under-temperature limit. Fast charging will begin or resume when the temperature falls within these limits.

Overvoltage and under-voltage protection is also provided by the MTA11200. The charge request is terminated if the battery voltage exceeds the value stored in EEPROM address MAXTV. Fast charge is prevented when battery voltage is less than the value stored in EEPROM location EODV.

A fast charge timer provides additional protection by limiting the amount of time that the fast charge mode may be active during any one charging cycle. This timer runs anytime fast charge mode is active. If the timer value exceeds the maximum fast charge time limit programmed in EEPROM at address OVTIM, the state of charge indication is set to 100%, the timer is turned off and is reset, and fast charge mode is terminated.

3.2.3 Maintenance Charge Mode

The maintenance charge mode allows the battery to continue charging and remain at or near a 100% state of charge during periods of discharge inactivity. The amount of current provided to the battery is determined by the external "dumb" current source. Fail-safe limits for battery over-temperature (MAXTMC) and under-temperature (MINTMC), as well as battery overvoltage (MAXTV), can all suspend maintenance mode charging. Maintenance charging can resume when battery conditions fall back within the fail-safe limits.

3.2.4 External Charge Current Source Control

The charge rate is controlled by the $\overline{CHG}$ pin. The $\overline{CHG}$ pin is driven high when the MTA11200 is requesting maintenance (trickle) charge current. When driven low fast charge current is requested.

The $\overline{CHG}$ pin is also used to force the MTA11200 into the ON state. This pin is sampled (i.e. becomes an input) once every 1.75 seconds. If the $\overline{CHG}$ pin is sampled high, then the MTA11200 is forced into the ON state. If it is sampled low, then no action is taken and the MTA11200 enters the standby state.

3.2.5 ΔV Fast Charge Termination

The MTA11200's proprietary -ΔV algorithm makes extensive use of filtering, signal processing techniques, and heuristics to avoid premature charge termination and to retain high sensitivity. The -ΔV termination threshold is programmable and is stored in EEPROM at location NDV.

3.2.6 dT/dt Fast Charge Termination

The MTA11200's dT/dt algorithm is designed to use an external thermistor to detect the rapid rise in temperature that rechargeable batteries exhibit when full charge is reached. The MTA11200 measures the battery temperature and calculates the rate temperature rise with respect to time and compares this value to the programmed DTDT threshold stored in EEPROM. When fast charging begins the measured dT/dt rate is allowed to exceed the programmed DTDT threshold for three minutes without causing a fast charge termination. Thereafter, the MTA11200 will terminate fast charge mode if the measured dT/dt rate meets or exceeds DTDT and the dT/dt rate is increasing.

3.2.7 Voltage Detection Fast Charge Termination

When programmed for voltage detection fast charge termination, which is typically used with lead acid batteries, the MTA11200 will terminate fast charge mode when the battery voltage meets or exceeds the limit programmed in EEPROM location LAFCV. This should not be confused with the MTA11200 fail-safe overvoltage mechanism that will remove all charge current requests if a maximum voltage limit (MAXTV) is exceeded. The MAXTV limit is a backup mechanism for fast charge termination and is always enabled. The LAFCV is a primary charge termination limit and is only active when voltage detection fast charge termination is enabled.

3.3 A/D Conversion

The MTA11200 uses a highly accurate timing system to control a timed voltage ramp analog-to-digital converter. Battery current, voltage and temperature are sampled every 1.75 seconds when the battery is in use.

Each measurement cycle begins by performing a comparator offset correction procedure. First the ZERO pin is driven high. Approximately 200 ms later an internal timer begins counting and the RAMP pin is driven from a low to a tristated condition. Next, the MTA11200 monitors the ISENC, and REFC inputs for a state change from low to high. The elapsed time until the state change occurs is recorded for both inputs. The total duration of this offset correction measurement is constant and takes approximately 650 ms

The measurement cycle continues and the A/D conversion starts when the ZERO pin is driven to a low state. An internal timer begins counting and the RAMP pin is driven from a low to a tristated condition. Next, the MTA11200 monitors the BATVC, ISENC, TEMPC, and REFC inputs for a state change from low to high. The elapsed time until the state change occurs is recorded for each input. The duration of this measurement cycle is constant and takes approximately 650 ms These elapsed time measurements form the basis for the A/D conversions. Figure 3.3 illustrates this form of analog-to-digital conversion.

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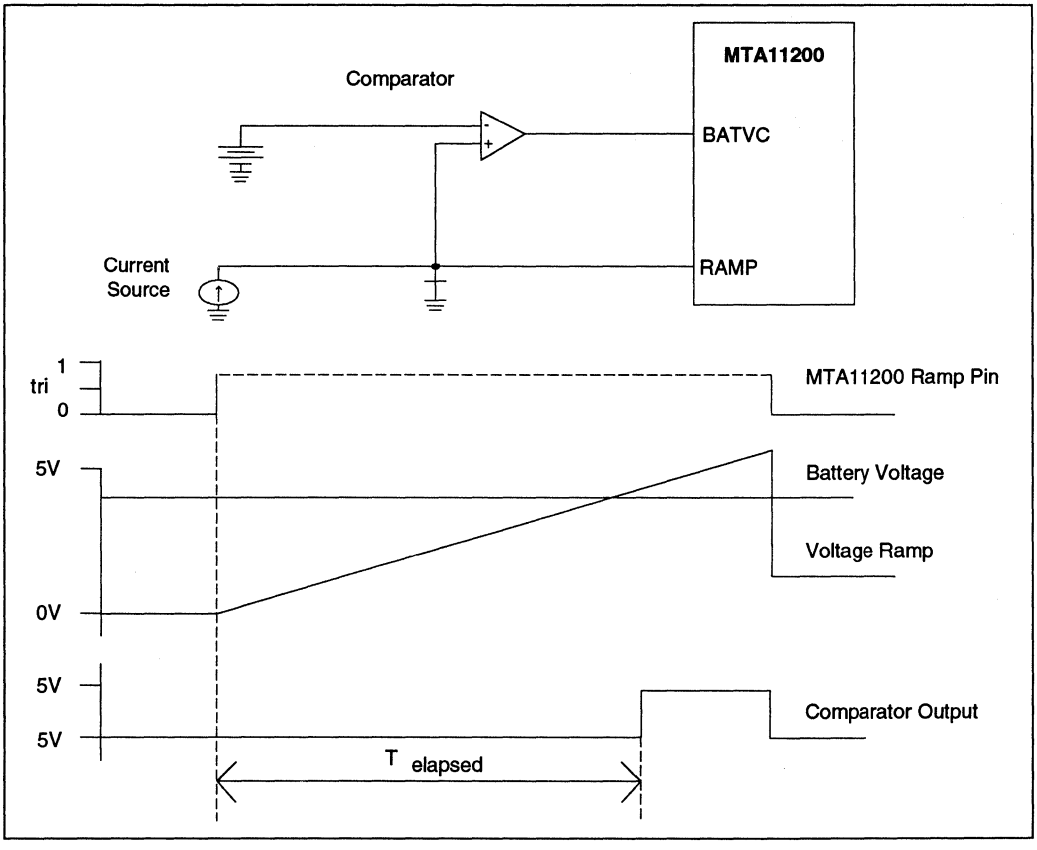
FIGURE 3.3 - A/D CONVERSION PRINCIPLE



3.3.1 A/D Calibration

Calibration factors for each A/D input are stored in the Serial EEPROM. These factors compensate for component tolerances and drift for the external circuits. Typically, the calibration factors are determined and programmed into the Serial EEPROM once the external circuits are connected to the MTA11200 (i.e. at board assembly). After calibration, the MTA11200 based system is ready for use. Normally, it is then mated to a battery pack.

An "A/D Reference Point" is set during the calibration process. It allows the MTA11200 to adjust for variations in the external voltage ramp over time and temperature. The elapsed time value for the REFC input is stored in the EEPROM when the Set A/D Reference Point command is received. Typically, this command is only used once in the life of the TrueGauge system and usually occurs as the first step in the calibration process. During normal operation, the elapsed time values for the BATVC. ISENC, and TEMPC inputs are compensated for the difference in the present value of REFC and the stored "A/D Reference Point" value for REFC. Note, since the REFC input is used for drift compensation of the external voltage ramp, the other input of the comparator is kept at a constant voltage potential.

Gain values for battery current, voltage, and temperature inputs are stored in the EEPROM.

Offset correction factors are also stored for the BATVC and TEMPC inputs. The offset measurement that occurs when the ZERO pin is driven high determines the "zero" point for the ISENC input and eliminates the need for an offset correction factor for this input.

Typically, the voltage, current, and temperature gain factors in EEPROM are set equal to one prior to performing a calibration procedure. Also, the offset factors for voltage and temperature calculations are usually set to zero. Next, two known values of current (usually 0 mA and -1000 mA) are applied and the measured values reported by the MTA11200 are recorded. A current gain correction factor is then calculated from the known values of current versus the reported values. This correction factor is then written into the EEPROM.

Correction factors for voltage and temperature measurement are determined in a similar manner. Additionally, offset factors for voltage and temperature are required to ensure that the zero temperature point and the zero voltage point are correct.

During normal operation the MTA11200 uses all of these calibration factors to accurately compute the physical quantities of voltage, current, and temperature from the elapsed time measurements.

3.4 Communication

The MTA11200 communicates battery status information via a 9600 baud RS-232 serial link. It can operate as a transmit only device via a single wire connected to the TXD pin and a ground return. Or, bidirectional communication can occur via a three wire interface that uses the TXD, RXD, and CTS pins. Utilizing the three wire bidirectional mode during initial system calibration, and then switching to the single wire transmit only mode when the device is mated to a battery pack provides both a flexible and low cost battery monitoring solution.

A data broadcast mode is provided that is especially useful when a single wire interface is desired. The MTA11200 will transmit battery status data spontaneously when broadcast mode is enabled by setting the system parameter BRDINTVL to a nonzero value. BRDINTVL sets the interval between these data broadcasts. The amount of data that is sent during the broadcast can either be a single byte that indicates the battery's state of charge in percent, or a 16 byte data packet that gives complete information about the battery. The system parameter REPMODE controls the amount of data that is broadcast.

Alternately, the three wire interface method uses a CTS handshake protocol that allows a host device to poll the MTA11200 for battery status data. Additionally, several commands are available that can be sent to the MTA11200 that allow the host to access the system control parameters stored in the EEPROM and perform other control functions.

3.4.1 Data Format

The following data format is broadcast by the MTA11200 when transmitting data to the host. This 9600 baud 8,N,1 RS-232 serial data format utilizes a 10-bit data frame that consists of 8 bits of message data and two control bits. All data to and from the MTA11200 is binary coded.

Data Frame Format:

Bit	Description
1	Start Bit (always 1)
2	Message Data Bit 0 , lsb
3	Message Data Bit 1
4	Message Data Bit 2
5	Message Data Bit 3
6	Message Data Bit 4
7	Message Data Bit 5
8	Message Data Bit 6
9	Message Data Bit 7, msb
10	Stop Bit (always 0)

3.4.2 Battery Parameter Data Packet

When transmitting the complete set of battery status information, the MTA11200 transmits the following 16-byte data packet:

Byte (1) = Battery Voltage in mV (lsb)

Byte (2) = Battery Voltage in mV (msb)

Byte (3) = Battery Temperature in °C (lsb)

Byte (4) = Battery Temperature in °C (msb) (signed)

Byte (5) = Battery Current magnitude in mA (lsb)

Byte (6) = Battery Current magnitude in mA (msb)

Byte (7) = Battery State of Charge in %

Byte (8) = Battery Error Byte

Byte (9) = Battery Capacity in mA-hr (lsb)

Byte (10) = Battery Capacity in mA-hr (msb)

Byte (11) = Reserved

Byte (12) = Reserved

Byte (13) = Battery Status Byte

Byte (14) = Measured dT/dt rate*

Byte (15) = Reserved

Byte (16) = Reserved

To translate the battery data into physical quantities apply the following equations and decodes.

Battery Voltage in volts =
(Byte(2) * 256) + Byte(1)) / 1000

Battery Temperature in °C =
(Byte(3) / 256) + Byte(4)

Battery Current in Amps =
(Byte(5) + (256 * Byte(6))) / 1000

Battery Capacity in Amp-hours =
(Byte 9 + (256 *Byte(10))) / 1000

Measured dT/dt rate in degrees Celsius per minute = Byte (14) / 32

* Note: Byte 14 of the data packet is only valid when the MTA11200 is configured to use dT/dt fast charge termination, otherwise this byte is undefined (refer to Section 5.1)

Battery Error Byte:

Bit	Description
0	Fast Charge Time Out Error, 1 = true, 0 = false
1	Low Temperature Error, 1 = true, 0 = false
2	High Temperature Error, 1 = true, 0 = false
3	Reserved
4	Overvoltage Error, 1 = true, 0 = false
7,6,5	0,0,1 = SOC below Low Battery Alarm (Low BAT) Limit (refer to Section 5.13)
7,6,5	0,1,0 = SOC below Critical Battery Alarm (CRITBAT) Limit (refer to Section 5.5)
7,6,5	0,1,1 = SOC below Battery Shutdown Alarm (SHUTDN) Limit (refer to Section 5.29)
7,6,5	1,0,0 = SOC below EODV Limit (refer to Section 5.7)
	SOC = Indicated Battery State of Charge in percent

Battery Status Byte:

Bit	Description
0	Sign of Current, 1= Charging, 0 = Discharging
1	Reserved
2	Reserved
3	Reserved
4	Charge Current Request, 1 = turn on current, 0 = turn off current
5	Capacity Measurement Request, 1 = true, 0 = false
6	Capacity Measurement in Progress, 1 = true, 0 = false
7	Fast Charge Request, 1 = Fast charge, 0 = maintenance charge

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4.0 COMMANDS

TABLE 1 - COMMAND SUMMARY

Command	Code, Data	Units
Read EEPROM byte	F0,XX	XX= Address
Write EEPROM byte	F1,XX,YY	XX= Address YY= Data
Send State of Charge (SOC)	F2	Percentage
Send Firmware Revision	F3	Rev. Number (Hex)
Send Battery Data	F4	16 bytes, mixed data types (see text)
reserved	F5	n/a
reserved	F6	n/a
Execute Self-test	F7	n/a
Start Capacity Measurement Cycle	F8	n/a
Clear Battery Errors	F9	n/a
Initialize EEPROM	FA,XX,...,XX	128 bytes
Reset	FB	n/a
Set A/D Reference Point	FC	n/a
Toggle EEPROM Lock	FD	n/a
High Speed Read EEPROM	FE	128 bytes
Force Capacity to 100%	FF	n/a

4.1 Read EEPROM Code: F0h,XXh

This command reads one Serial EEPROM byte at the specified address. Upon receiving this command, the MTA11200 issues a read command to the Serial EEPROM via the I²C bus. The Serial EEPROM responds with the data at the specified address. The MTA11200 receives the serial EEPROM's response and in turn transmits this data in RS-232 format on the TXD pin.

4.2 Write EEPROM Code: F0h,XXh

This command writes one byte of data to the Serial EEPROM at the specified address. Then a read of the EEPROM address is performed and the read data is transmitted back to the host. This adds additional security to the write operation by allowing the host to quickly verify that the data was written correctly.

When the WRITE EEPROM command is received the MTA11200 issues a write command to the Serial EEPROM on its I²C bus port (SCL and SDA). The MTA11200 then issues a read command to the Serial EEPROM via the I²C bus. When the Serial EEPROM responds with the data at the specified address the MTA11200 forwards the serial EEPROM's response to the host by transmitting this data in RS-232 format on the TXD pin.

4.3 Send State Of Charge Code: F2h

The MTA11200 will transmit a single byte that indicates the battery's internal state of charge in response to the Send State of Charge command. This byte is limited to the range from 0 to 64h inclusive and indicates from 0% to 100% state of charge.

4.4 Send Firmware Revision Code: F3h

In response to this command the MTA11200 will transmit a single byte that indicates the internal firmware version and revision. The most significant four bits of this byte represent the version number and the least significant four bits indicate the revision status.

Note: There is no predefined correlation between the firmware version and the MTA11200 revision status as physically marked on the I.C.

4.5 Send Battery Data Code — Code: F4h

The MTA11200 transmits a 16-byte data packet in response to this command. This data provides complete information about the present status of the battery. The data packet is defined as follows:

Byte (n)	Battery Data
1	Voltage LSB
2	Voltage MSB
3	Temperature LSB
4	Temperature MSB
5	Current LSB
6	Current MSB
7	State of Charge
8	Error Byte
9	Measured Total Capacity Byte 1
10	Measured Total Capacity Byte 2
11	Reserved
12	Reserved
13	Flag Byte
14	Measured dT/dt
15	Reserved
16	Reserved

4.6 Start Capacity Measurement Cycle — Code: F8h

This command forces the initiation of a battery capacity measurement sequence in the MTA11200 controller. First the internal discharge count register is cleared. Next, the MTA11200 will total all discharge current until the programmed End Of Discharge Voltage (EODV) is reached or the discharge is aborted (i.e. charge current is detected or current goes to zero). If the discharge is aborted then this capacity measurement cycle is abandoned. Otherwise, the measured total capacity is copied to the internal total capacity register and is also written to system parameter MEACAP in the EEPROM.

4.7 Clear Battery Errors — Code: F9h

This command clears the error bits in the Battery Error Byte. The Time-out Error, Under-temperature Error, Over-temperature Error, and Overvoltage bits are all reset to zero. Additionally, if an error bit was set prior to receipt of the Clear Battery Errors command the associated error counter in EEPROM will be incremented when the error bit is reset. For example, if a Clear Battery Errors command is executed when the Over-temperature error bit in the Battery Error Byte is set then the Over-temperature error bit in the Battery Error byte will be reset and the error counter HITERRS in EEPROM will be incremented.

4.8 Initialize EEPROM — Code: FAh

This command is used to initialize the MTA11200 system parameters in external EEPROM. The MTA11200 accepts 128 bytes of data that will be written sequentially into the EEPROM starting at location 0. The MTA11200 suspends all operations while receiving this data and writing it to the EEPROM. This allows the EEPROM data to be initialized at a much faster rate than using the single-byte **Write EEPROM** command.

4.9 Reset — Code: FBh

This command initiates a power up reset sequence in the MTA11200 controller. First, all internal registers and operating parameters are cleared. Next, the present state of charge is reset to zero percent and the total battery capacity is read from location MEACAP in EEPROM and normal operation begins. This command has the effect of driving the CLR pin from low to high.

4.10 Set A/D Reference — Code: FCh

This Set A/D Reference command causes the MTA11200 to measure and record a reference point for the A/D converter. The MTA11200 maintains the A/D's high accuracy by using this reference point to compensate for drift in the A/D circuits over time and temperature. This command is usually issued only once during the normal operating life of the battery monitoring system. It is normally issued as the first step of the A/D calibration process.

The MTA11200 measures the amount of time that elapses from when it tristates the RAMP pin until the REFC pin goes to a high state. When the Set A/D command is issued this value is then stored as the A/D reference point in EEPROM at location REFVAL. Subsequently, during each conversion cycle the stored value is compared with the measured amount of time and all A/D measurements are compensated accordingly.

4.11 Reserved Commands — Code:(Fxh)

Command codes F5h and F6h are reserved and should not be sent to the MTA11200. Unpredictable operation may result if the MTA11200 receives one or more reserved command codes.

4.12 Unspecified Commands

Command codes not in the range of F0h to FFh are unspecified. The MTA11200 will completely ignore command codes that are not within the range F0h to FFh.

4.13 High Speed EEPROM Read — Code: FEh

This command reads 128 Serial EEPROM bytes starting with address 0. Upon receiving this command the MTA11200 enters a loop that reads a byte from the Serial EEPROM and transmits this data in RS-232 format on the TRANSMIT pin. The loop continues until all 128 bytes have been read and transmitted. Note that in response to this command the data is transmitted spontaneously and cannot delayed or interrupted.

4.14 Toggle EEPROM Lock Code: FDh

This command toggles the MTA11200's internal EEPROM Lock bit. The MTA11200 responds by transmitting the new state of the EEPROM Lock where 00 indicates locked and AA indicates unlocked. When locked all writes to the EEPROM are disabled except for writes to EEPROM addresses 20h through 2Fh.

4.15 Force 100% Capacity Indication Code: FFh

This command forces the percent capacity indication to be set to 100% to force the MTA11200 to behave as if the battery is fully charged.

This command is provided to aid manufacturing testability of end products.

4.16 Perform Self-test Code: F7h

This command causes the MTA11200 to initiate a self-test sequence. Upon completion of the self-test sequence a single byte will be transmitted to indicate a test pass (AAh) or fail (any non-AAh data). Two checks of external circuits are included in the self test sequence. The state of RAMP pin is tested at 1 ms and 500 ms after the RAMP pin is driven from a low to tristate by the MTA11200. The RAMP pin must be low at the 1 ms sample point and high at the 500 ms sample point for this test to pass. If these conditions are not satisfied the MTA11200 will return a 01H code indicating an A/D ramp failure.

Next, the LED outputs $\overline{P20}$, $\overline{P40}$, $\overline{P60}$, and $\overline{P80}$ are individually driven low in sequence starting with $\overline{P20}$ for a period of 125 ms each.

5.0 CONFIGURATION PARAMETERS

The MTA11200 is designed to work in conjunction with an external Serial EEPROM that stores configuration parameters for the MTA11200. The MTA11200 communicates with the Serial EEPROM via the SCL and SDA pins. Standard I²C bus communication protocol is used.

The parameters that are stored in Serial EEPROM are variables that control the MTA11200's mode of operation and variables that describe the characteristics of the battery that the TrueGauge is monitoring. These system parameters range from single-byte values to four-byte values. All multi-byte system parameters are stored in little endian (low byte first) format.

All bytes and bits declared as reserved must be programmed to a value of zero (0).

TABLE 2 - SYSTEM PARAMETER STORAGE MAP FOR SERIAL EEPROM

Addr (hex)	Parameter	Addr (hex)	Parameter	Addr (hex)	Parameter	Addr (hex)	Parameter
0	REVID	20	TCC -lb	40	CESC(0)	60	SDFT(0) lb
1	BATINFO	21	TCC-hb	41	CESC(1)	61	SDFT(0) hb
2	NOMCAP- lb	22	TOERRS	42	CESC(2)	62	SDFT(1) lb
3	NOMCAP - lmb	23	LOTERRS	43	CESC(3)	63	SDFT(1) hb
4	NOMCAP - hmb	24	HITERRS	44	CESC(4)	64	SDFT(2) b
5	NOMCAP - hb	25	HIVERRS	45	CESC(5)	65	SDFT(2) hb
6	reserved	26	reserved	46	CESC(6)	66	SDFT(3) b
7	reserved	27	reserved	47	CESC(7)	67	SDFT(3) hb
8	MAXTFC	28	reserved	48	CESC(8)	68	SDFT(4) b
9	MINTFC	29	reserved	49	CESC(9)	69	SDFT(4) hb
0A	MAXTMC	2A	reserved	4A	CESC(10)	6A	SDFT(5) b
0B	MINTMC	2B	reserved	4B	CESC(11)	6B	SDFT(5) hb
0C	reserved	2C	MEACAP - lb	4C	CESC(12)	6C	SDFT(6) b
0D	MAXTV	2D	MEACAP - lmb	4D	CESC(13)	6D	SDFT(6) hb
0E	reserved	2E	MEACAP - hmb	4E	CESC(14)	6E	SDFT(7) b
0F	reserved	2F	MEACAP - hb	4F	CESC(15)	6F	SDFT(7) hb
10	TONCHG	30	REFVAL - lb	50	CEFT(0)	70	SDFT(8) b
11	CCCR	31	REFVAL - hb	51	CEFT(1)	71	SDFT(8) hb
12	USER	32	VSC -lb	52	CEFT(2)	72	SDFT(9) b
13	USER	33	VSC - hb	53	CEFT(3)	73	SDFT(9) hb
14	USER	34	VOC - lb	54	CEFT(4)	74	SDFT(10) b
15	USER	35	VOC - hb	55	CEFT(5)	75	SDFT(10) hb
16	DTDT	36	ISC - lb	56	CEFT(6)	76	SDFT(11) b
17	OVTIM - lb	37	ISC - hb	57	CEFT(7)	77	SDFT(11) hb
18	OVTIM - hb	38	TSC - lb	58	CEFT(8)	78	SDFT(12) b
19	EODV	39	TSC - hb	59	CEFT(9)	79	SDFT(12) hb
1A	NDV	3A	TOC - lb	5A	CEFT(10)	7A	SDFT(13) b
1B	LOWBAT	3B	TOC - hb	5B	CEFT(11)	7B	SDFT(13) hb
1C	CRITBAT	3C	reserved	5C	CEFT(12)	7C	SDFT(14) hb
1D	SHUTDN	3D	reserved	5D	CEFT(13)	7D	SDFT(14) hb
1E	REPMODE	3E	LAFCV-lb	5E	CEFT(14)	7E	SDFT(15) hb
1F	REPINTRVL	3F	LAFCV-hb	5F	CEFT(15)	7F	SDFT(15) hb

5.0 CONFIGURATION PARAMETERS (LISTED IN ALPHABETICAL ORDER)

5.1 BATINFO

Battery Information Byte

EEPROM Address	1h
Allowable Range	Number of cells = 0 to 15
Typical Value	N/A
Stored Value	(See below)

The battery information byte specifies the number of series connected cells in the battery pack and the fast charge termination technique being used. Parallel connected cells should only be counted as one cell.

Stored Value:

Bits 7-4: Number of cells in the battery pack (0-15)

Bits 3-2: Reserved (unused)

Bit 1: Voltage Limit Fast Charge Termination, 1 = enabled, 0 = disabled

Bit 0: Fast Charge Termination Technique, 1= dT/dt, 0 = -ΔV

Bits 0 and 1 are mutually exclusive. If voltage limit fast charge termination is enabled then bit 0 is ignored and -ΔV or dT/dt termination is disabled.

5.2 CCCR

Charge Cycles between Capacity Measurement Requests

EEPROM Address	11h
Allowable Range	0 to 255
Typical Value	5 to 25
Stored Value	Number of Charge Cycles

The charge cycles between capacity measurement requests parameter specifies the number of full or partial charge cycles that occur before the MTA11200 will issue a request for a battery capacity measurement cycle.

This request is indicated in the flag byte of the battery parameter's data packet. An internal counter is incremented each time fast charge mode is terminated by exceeding any of the following limits: dT/dt, -ΔV or absolute voltage. If a capacity measurement cycle successfully completes, then this internal charge cycle counter will be reset to zero.

5.3 CESC(0 15)

Charge Efficiency vs. State of Charge

EEPROM Addresses	40h through 4Fh
Allowable Range	0 to 99.6%
Typical Value	N/A
Stored Value	(% Efficiency) * 25.6

The charge efficiency versus state of charge table is a sixteen-byte lookup table. These compensation parameters adjust for the less than 100% charge acceptance efficiency that batteries display when charging. This table contains charge efficiency factors for the ranges of percent capacity from 0% to 3% and 90% to 100%, in 1% increments. The capacity range from 4% to 89% is compensated with a single factor. Each entry in the table specifies charge efficiency as a fraction of 256. A value of 128 (07Fh) indicates 50% charge efficiency whereas a value of (0ECh) indicates 92.2% charge efficiency.

TABLE 3 - CHARGE EFFICIENCY VS STATE OF CHARGE COMPENSATION

Addr	Parameter	Definition
40h	CESC(0)	Chg eff. for chg state 0%
41h	CESC(1)	Chg eff. for chg state 1%
42h	CESC(2)	Chg eff. for chg state 2%
43h	CESC(3)	Chg eff. for chg state 3%
44h	CESC(4)	Chg eff. for chg state 4% to 89%
45h	CESC(5)	Chg eff. for chg state 90%
46h	CESC(6)	Chg eff. for chg state 91%
47h	CESC(7)	Chg eff. for chg state 92%
48h	CESC(8)	Chg eff. for chg state 93%
49h	CESC(9)	Chg eff. for chg state 94%
4Ah	CESC(10)	Chg eff. for chg state 95%
4Bh	CESC(11)	Chg eff. for chg state 96%
4Ch	CESC(12)	Chg eff. for chg state 97%
4Dh	CESC(13)	Chg eff. for chg state 98%
4Eh	CESC(14)	Chg eff. for chg state 99%
4Fh	CESC(15)	Chg eff. for chg state 100%

5.4 CEFT(0-15)

Charge Efficiency versus Temperature

EEPROM Addresses	50h through 5Fh
Allowable Range	0 to 100%
Typical Value	N/A
Stored Value	(% Efficiency) * 2.56

The charge efficiency versus temperature table is a sixteen-byte lookup table. These compensation parameters adjust for the decrease in charge acceptance efficiency that batteries typically exhibit as their temperature increases. This table stores compensation factors for a temperature range of 0°C to 60°C, in 4°C increments. Each entry in the table specifies charge efficiency as a fraction of 256, which indicates 100% charge efficiency. For example, a value of 128 (07Fh) indicates 50% charge efficiency and a value of 253 (0FDh) indicates 98.8% charge efficiency.

TABLE 4 - CHARGE EFFICIENCY VS CHARGE STATE COMPENSATION TABLE

Addr	Parameter	Definition
50h	CEFT(0)	Chg eff. for temperature 0 °C
51h	CEFT(1)	Chg eff. for temperature 4 °C
52h	CEFT(2)	Chg eff. for temperature 8 °C
53h	CEFT(3)	Chg eff. for temperature 12 °C
54h	CEFT(4)	Chg eff. for temperature 16 °C
55h	CEFT(5)	Chg eff. for temperature 20 °C
56h	CEFT(6)	Chg eff. for temperature 24 °C
57h	CEFT(7)	Chg eff. for temperature 28 °C
58h	CEFT(8)	Chg eff. for temperature 32 °C
59h	CEFT(9)	Chg eff. for temperature 36 °C
5Ah	CEFT(10)	Chg eff. for temperature 40 °C
5Bh	CEFT(11)	Chg eff. for temperature 44 °C
5Ch	CEFT(12)	Chg eff. for temperature 48 °C
5Dh	CEFT(13)	Chg eff. for temperature 52 °C
5Eh	CEFT(14)	Chg eff. for temperature 56 °C
5Fh	CEFT(15)	Chg eff. for temperature 60 °C

5.5 CRITBAT

Critical Battery Level

EEPROM Address	1Ch
Allowable Range	SHUTDN < CRITBAT < LOWBAT
Typical Value	3%
Stored Value	Integer limit in %

A bit in the FLAGBYTE portion of the battery parameter data packet is set when the battery state of charge is less than the CRITBAT limit. The MTA11200 will indicate a critical battery level and mask off a low battery level indication in response to state of charge falling below this limit. Conversely, the critical level indication will be cleared and the low battery level alarm will be unmasked when the state of charge exceeds the CRITBAT limit. The programmed value of this parameter must be between the limits set for the SHUTDN and LOWBAT parameters.

5.6 DTDT

Delta Temperature Delta Time

EEPROM Address	16h
Allowable Range	0 to 7.97 °C/minute
Typical Value	0.5 to 1.0 °C/minute
Stored Value	(°C/minute) * 32

This parameter specifies the rate of change in temperature in degrees Celsius over a one minute interval that will terminate a fast charge request. For example, to set a 0.625 °C/minute rate termination limit the DTDT stored value would be .625 *32 = 20.

5.7 EODV

End of Discharge Voltage

EEPROM Address	19h
Allowable Range	0 to 65.28 Volts
Typical Value	NiCd (1.0V to 1.1V) * (# of cells) NiMH (1.0V to 1.1V) * (# of cells) Pb (1.7V to 1.8V) * (# of cells)
Stored Value	(Limit in Volts) / 0.256

The End Of Discharge Voltage parameter specifies the battery voltage when the battery is at 0% capacity. It is the value indicated by EODV is multiplied by 256mV to obtain the specified end of discharge voltage for the battery. This parameter establishes an end point for the battery state of charge calculation. It also prevents the MTA11200 from requesting fast charge when the battery voltage is less than EODV. A typical value for both NiCd and NiMH battery packs is calculated by multiplying 1.05V times the number of cells in the battery pack. This formula assumes that the cells are electrically connected in a series fashion.

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5.8 HITERRS

Over Temperature Errors

EEPROM Address	24h
Allowable Range	0 to 255
Typical Value	0
Stored Value	Number of Errors

This parameter is incremented each time an Over Temperature Error, as defined by the MAXTFC or MAXTMC parameters, occurs and is acknowledged by a host via the RS-232 link. This error counter will be incremented immediately after the host issues a clear battery errors command if an over temperature error has occurred.

5.9 HIVERRS

Over Voltage Errors

EEPROM Address	25h
Allowable Range	0 to 255
Typical Value	0
Stored Value	Number of Errors

This parameter is incremented each time an Over Voltage Error, as defined by the MAXTV parameter, occurs and is acknowledged by the host. This error counter will be incremented immediately after the host issues a clear battery errors command if an over voltage error has occurred.

5.10 ISC

Current Slope Correction

EEPROM Address	36h (lsb) and 37h (msb)
Allowable Range	0 to 65535
Typical Value	256 (100h)
Stored Value	Current Gain * 256

The Current Slope Correction factor provides a fixed gain that is applied to the A/D conversion calculation of the battery current. Gain factors from 1/256 to 255 are available. This factor is normally determined when the A/D converter is calibrated. A value of 100h corresponds to a gain of 1.0.

5.11 LAFCV

Lead Acid Fast Charge Cutoff Voltage

EEPROM Address	3Eh (lsb) and 3Fh (msb)
Allowable Range	0 to 65.28V
Typical Value	Pb (2.5V to 2.7V) * number of cells
Stored Value	Volts / 1000

The Lead Acid Fast Charge Cutoff Voltage applies when voltage limit fast charge termination is specified by parameter BATINFO. This is a sixteen-bit (two-byte) value that indicates the termination voltage in 1mV increments. A value of 13450 (348A HEX) specifies a 13.340V termination limit.

Voltage limit termination is generally the preferred method of fast charge termination used with lead acid batteries.

5.12 LOTERRS

Under Temperature Errors

EEPROM Address	23h
Allowable Range	0 to 255
Typical Value	0
Stored Value	Numbers of Errors

This parameter is incremented each time an Under Temperature Error, as defined by the MINTFC or MINTMC parameters, occurs and is acknowledged by the host. This error counter will be incremented immediately after the host issues a clear battery errors command if an under-temperature error occurs.

5.13 LOWBAT

Low Battery Warning Level

EEPROM Address	1Bh
Allowable Range	CRITBAT < LOWBAT < 100%
Typical Value	5%
Stored Value	Integer limit in %

A bit in the ERRORBYTE portion of the battery parameter data packet is set when the battery state of charge is less than the LOWBAT limit. This alarm sets the appropriate bit in ERRORBYTE. No other action by the MTA11200 is taken in response to the alarm. The value of this parameter must be greater than the CRITBAT limit and less than 100%.

5.14 MAXTFC

Maximum Temperature for Fast Charge

EEPROM Address	8h
Allowable Range	0 to 255 °C
Typical Value	40 °C to 50 °C
Stored Value	Integer limit in °C

Maximum Temperature for Fast Charge specifies the maximum temperature limit for fast charging. If the temperature exceeds this limit fast charging will be terminated. MAXTFC is an 8-bit (1-byte) value that indicates the temperature limit value in 1°C increments. For example, a value of 40 (28h) equals a 40 °C over temperature fast charge termination limit.

5.15 MAXTMC

Maximum Temperature for Maintenance Charge

EEPROM Address	0Ah
Allowable Range	0 to 255 °C
Typical Value	50 °C to 60 °C
Stored Value	Integer limit in °C

Maximum Temperature for Maintenance Charge specifies the maximum temperature limit for maintenance charging. If the temperature exceeds this limit all charging will be terminated. MAXTFC is an 8 bit (1 byte) value that indicates the temperature limit value in 1 °C increments. For example, a value of 50 (32h) equals a 50 °C over temperature charge termination limit.

5.16 MAXTV

Maximum Terminal Voltage

EEPROM Address	0Dh
Allowable Range	0 to 65.28 Volts
Typical Value	NiCd (1.5V to 1.7V) * (number of cells) NiMH (1.5V to 1.7V) * (number of cells) Pb (2.8V to 3.0V) * (number of cells)
Stored Value	(Limit in Volts) / 0.256

Maximum Terminal Voltage specifies the maximum voltage allowed during charging. If the battery voltage exceeds this value then all charge requests, both fast and maintenance charging will be terminated and the $\overline{CHG}$ pin will be driven low.

The actual terminal voltage is obtained by multiplying the value stored in MAXTV by 256mV.

5.17 MEACAP

Measured Battery Capacity

EEPROM Address	2Ch(lsb) through 2Fh(msb)
Allowable Range	0 to 2,087,831 mA-hr
Typical Value	Nominal Battery Capacity
Stored Value	(Capacity in mA-hr) *(2057.14)

This parameter is updated with the measured capacity of the battery each time a manual or automatic battery capacity calibration is performed by the MTA11200. A four-byte value is stored that indicates the measured capacity in mA-Sec /1.75.

5.18 MINTFC

Minimum Temperature for Fast Charge

EEPROM Address	9h
Allowable Range	0 to 255 °C
Typical Value	10°C
Stored Value	Integer limit in °C

Minimum Temperature for Fast Charge specifies the minimum temperature limit for fast charging. If the temperature is below this limit fast charging will be terminated. MINTFC is an 8-bit (1-byte) value that indicates the temperature limit value in 1°C increments. For example, a value of 10 (0Ah) equals a 10°C under temperature fast charge termination limit.

5.19 MINTMC

Minimum Temperature for Maintenance Charge

EEPROM Address	0Bh
Allowable Range	0 to 255 °C
Typical Value	0 °C
Stored Value	Integer limit in °C

Minimum Temperature for Maintenance Charge specifies the minimum temperature limit for maintenance charging. If the temperature is below this limit all charge requests will be terminated. MINTMC is an 8-bit (1-byte) value that indicates the temperature limit value in 1 °C increments. For example, a value of 5 equals a 5 °C under temperature charge termination limit.

5.20 NDV

Negative Delta Voltage Threshold

EEPROM Address	1Ah
Allowable Range	0 to 255 mV
Typical Value	NiCd (2mV to 4mV) * (number of cells) NiMH (1mV to 2mV) * (number of cells) Pb n/a
Stored Value	Limit in mV

The Negative Delta Voltage Threshold specifies the amount of voltage decay that is required for termination of a fast charge cycle. This voltage decay is referenced from the peak voltage obtained during the fast charge cycle. ΔV termination must be enabled in the BATINFO parameter for this threshold voltage to control fast charge termination.

5.21 NOMCAP

Nominal Battery Capacity

EEPROM Address	2h(lsb) through 5h(msb)
Allowable Range	0 to 2,087,831 mA-hr
Typical Value	Nominal Battery Capacity
Stored Value	(Capacity in mA-hr) *(2057.14)

This parameter is a storage location for saving the rated capacity of the battery pack. With this information a smart host can determine if the battery has reached end of life or is malfunctioning by comparing the rated capacity with the measured capacity. A four-byte value is stored that indicates the rated capacity in mA-Sec / 1.75. This value is not used by the MTA11200 for any capacity calculations or error detection.

5.22 OVTIM

Override Timer

EEPROM Address	17h(lsb) and 18h(msb)
Allowable Range	0 to 114686 seconds
Typical Value	1.5 * ((Nom. capacity mA-hr) *3600sec/hr)/(Fast chg rate mA))
Stored Value	(Limit in seconds) / 1.75

The override timer specifies the maximum amount of time that a fast charge cycle is allowed to be active. If a fast charge cycle exceeds this time limit a time-out error is logged. The time limit is calculated by multiplying the value of OVTIM by 1.75 seconds.

5.23 REFVAL

A/D Reference Value

EEPROM Address	30h(lsb) and 31h(msb)
Allowable Range	0 to 64535
Typical Value	N/A
Stored Value	Reference level

This location is where the MTA11200 stores the A/D reference value that is set during the A/D calibration procedure.

5.24 REPMODE

Reporting Mode

EEPROM Address	1Eh
Allowable Range	N/A
Typical Value	N/A
Stored Value	(See below)

Reporting Mode defines the amount of data broadcast by the MTA11200 when broadcasting is enabled as well as the type of data output on the LED drive pins P20, P40, P60, and P80. REPMODE is defined as follows:

Bits 7 Broadcast data select, 1 = send entire 16-byte battery parameter packet. 0 = send only the single byte percent capacity indication.

Bit 6-1: Reserved (program to 0)

Bit 0 LED mode select, 1 = LED outputs are BCD code 0 through 10 that represents 0 percent to 100 percent remaining battery capacity in 10% increments, 0 = LED outputs represent discrete >20%, >40%, >60%, and >80% levels.

5.25 REPINTRVL

Report Interval

EEPROM Address	1Fh
Allowable Range	0 to 222.25 seconds
Typical Value	5.25 to 31.5 sec
Stored Value	(Interval in seconds) / 1.75

The report interval byte specifies the interval between battery data broadcasts on the RS-232 link. The time between data broadcasts from the MTA11200 will be 1.75 seconds times the value contained in REPINTRVL. If a polling scheme of communication is desired then REPINTRVL can be set to zero and will battery data broadcasting will be disabled.

5.26 Reserved

Reserved Locations

EEPROM Address	Various
Allowable Range	0
Typical Value	0
Stored Value	0

All location listed as RESERVED are not presently used by the MTA11200. They are however reserved for future versions or revisions of the TrueGauge family. These locations must be initially programmed to a value of zero. EEPROM locations defined as USER are provided for general purpose data storage.

5.27 REVID

EEPROM Revision Identification

EEPROM Address	0h
Allowable Range	0 to 255
Typical Value	N/A
Stored Value	Revision

This location allows a revision identifier to accompany the system parameter EEPROM data set. When a set of system parameters are defined for use with a particular battery and/or system an identifier can be allocated and stored at location REVID. This allows unique data sets to be identified. This REVID location is provided as a convenience feature only and not used by the MTA11200 for any control or monitoring functions.

5.28 SDFT(0-15)

Self-discharge as a Function of Temperature

EEPROM Address	60h through 7Fh
Allowable Range	0 65535
Typical Value	N/A
Stored Value	K

The self-discharge versus temperature lookup table provides the factor K, that is used in the self-discharge compensation calculation:

Compensated SOC = SOC - (SOC * (K / 2^{24})

SOC (State Of Charge)

The battery state of charge is decreased once every 138 seconds when battery is idle and this calculation is applied. The compensation factors cover the temperature range of 0 °C up to 60 °C in 4 °C increments. For temperatures in excess of 60 °C, the 60 °C compensation factor is applied. Similarly, for temperatures below 0 °C the 0 °C factor is used.

TABLE 5 - SELF-DISCHARGE VS TEMPERATURE COMPENSATION TABLE

Addr	Parameter	Definition
61h, 60h	SDFT(0)	Self-dischg const. for 0°C
63h, 62h	SDFT(1)	Self-dischg const. for 4 °C
65h, 64h	SDFT(2)	Self-dischg const. for 8 °C
67h, 66h	SDFT(3)	Self-dischg const. for 12 °C
69h, 68h	SDFT(4)	Self-dischg const. for 16 °C
6Bh, 6Ah	SDFT(5)	Self-dischg const. for 20 °C
6Dh, 6Ch	SDFT(6)	Self-dischg const. for 24 °C
6Fh, 6Eh	SDFT(7)	Self-dischg const. for 28 °C
71h, 70h	SDFT(8)	Self-dischg const. for 32 °C
73h, 72h	SDFT(9)	Self-dischg const. for 36 °C
75h, 74h	SDFT(10)	Self-dischg const. for 40 °C
77h, 76h	SDFT(11)	Self-dischg const. for 44 °C
79h, 78h	SDFT(12)	Self-dischg const. for 48 °C
7Bh, 7Ah	SDFT(13)	Self-dischg const. for 52 °C
7Dh, 7Ch	SDFT(14)	Self-dischg const. for 54 °C
7Fh, 7Eh	SDFT(15)	Self-dischg const. for 60 °C

5.29 SHUTDN

Shutdown Alarm Limit

EEPROM Address	1Dh
Allowable Range	0 < SHUTDN < CRITBAT
Typical Value	1%
Stored Value	Integer limit in %

A bit in the FLAGBYTE portion of the battery parameter data packet is set when the battery state of charge is less than the SHUTDN limit. This alarm sets the appropriate bit in FLAGBYTE. The MTA11200 will mask off a battery critical level indication in response to this alarm. The alarm will be cleared and the critical level alarm will be unmasked when the state of charge exceeds the SHUTDN level. The value of this parameter must be between 0 and the CRITBAT limit.

5.30 TCC

Total Charge Cycle Counter

EEPROM Address	20h (lsb) and 21h (msb)
Allowable Range	0 to 65535
Typical Value	0 (initial)
Stored Value	Number of charge cycles

This parameter is incremented each time a charge cycle is terminated by exceeding a dT/dt, -ΔV or absolute voltage limit threshold.

5.31 TOC

Temperature Offset Correction Factor

EEPROM Address	3Ah (lsb) and 3Bh (msb)
Allowable Range	-32766 (80h) to 32767 (7Fh)
Typical Value	0
Stored Value	Voltage offset in °C / 256

The Temperature Offset Correction factor provides a fixed value that is added to the A/D conversion calculation of the Temperature. Offset factors from (-32766/256) to (32767/256) °C are available. This factor is normally determined when the A/D converter is calibrated.

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5.32 TOERRS

Time-out Errors Counter

EEPROM Address	22h
Allowable Range	0 to 255
Typical Value	0
Stored Value	Number of Errors

This parameter is incremented each time a Time Out Error, as defined by the OVTIM parameter, occurs. This error counter will be incremented when the error is acknowledged when the host issues a Clear Battery Errors Command.

5.33 TONCHG

Fast Charge Turn On Threshold

EEPROM Address	10h
Allowable Range	0 to 100
Typical Value	90% to 96%
Stored Value	Threshold in %

This parameter controls the point at which the charge controller will enter fast charge mode.

5.34 TSC

Temperature Slope Correction

EEPROM Address	38h (lsb) and 39h (msb)
Allowable Range	0 to 65535
Typical Value	256 (100h)
Stored Value	Temperature Gain * 256

The Temperature Slope Correction factor provides a fixed gain that is applied to the A/D conversion calculation of the battery temperature. Gain factors from 1/256 to (255+255/256) are available. This factor is normally determined when the A/D converter is calibrated.

5.35 USER

User Storage

EEPROM Address	12h through 15h
Allowable Range	N/A
Typical Value	N/A
Stored Value	N/A

These locations are not used by the MTA11200 and will not be used by future versions. They are available to the user for general purpose data storage.

5.36 VOC

Voltage Offset Correction

EEPROM Address	34h (lsb) and 35h (msb)
Allowable Range	-32768 (80h) to 32767 (7Fh)
Typical Value	0
Stored Value	Voltage offset in mV

The Voltage Offset Correction factor provides a fixed value that is added to the A/D conversion calculation of the battery voltage. Offset factors from -32768mV to 32767mV are available. This factor is normally determined when the A/D converter is calibrated.

5.37 VSC

Voltage Slope Correction

EEPROM Address	32h (lsb) and 33h (msb)
Allowable Range	0 to 65535
Typical Value	256 (100h)
Stored Value	Voltage Gain * 256

The Voltage Slope Correction factor provides a fixed gain that is applied to the A/D conversion calculation of the battery voltage. Gain factors from 1/256 to (255+255/256) are available. This factor is normally determined when the A/D converter is calibrated.

6.0 POWER ON RESET

The MTA11200 incorporates an on-chip Power On Reset Timer which provides internal chip reset. An internal timer begins counting when a logic high level is detected on $\overline{CLR}$. The MTA11200 remains in the reset state while this timer is running or anytime $\overline{CLR}$ is low. The timer expires 18mS (typical) after $\overline{CLR}$ goes high. Then the MTA11200 emerges from the reset condition and the remaining battery capacity is set to 0%.

In order to ensure proper power-on reset when a battery provides the V_{DD} power source, an external voltage level detector or "brown-out" circuit is recommended. This prevents $\overline{CLR}$ from reaching a valid logic high level when V_{DD} less than V_{DD} minimum, which can occur while the battery is in storage for long periods and its voltage is very slowly decaying to zero.

The voltage level detector or brown out circuit should ensure that $\overline{CLR}$ is held low anytime V_{DD} is less than the minimum operational V_{DD} level for the MTA11200 and any external I.C.'s. This will prevent erroneous operation and inaccurate capacity gauging.

7.0 APPLICATION EXAMPLE

An example of a MTA11200-based battery monitoring and charging system is shown in the following schematic (Document number 11200DTS).

This example system provides battery state of charge information via the TXD output and the display LEDs. In normal operation, only three connections are required between the host and the battery subsystem. LOAD+ provides the charge and discharge current path and LOAD- is the system ground. TXD allows the host to receive battery status data in real time and connects to a receiver in the host. If the battery charging source is included in the host system then an additional connection, to $\overline{CHG}$, can be used.

To connect to an external charging source (e.g. stand alone charger) only 3 connections between the charger and the battery system are required.

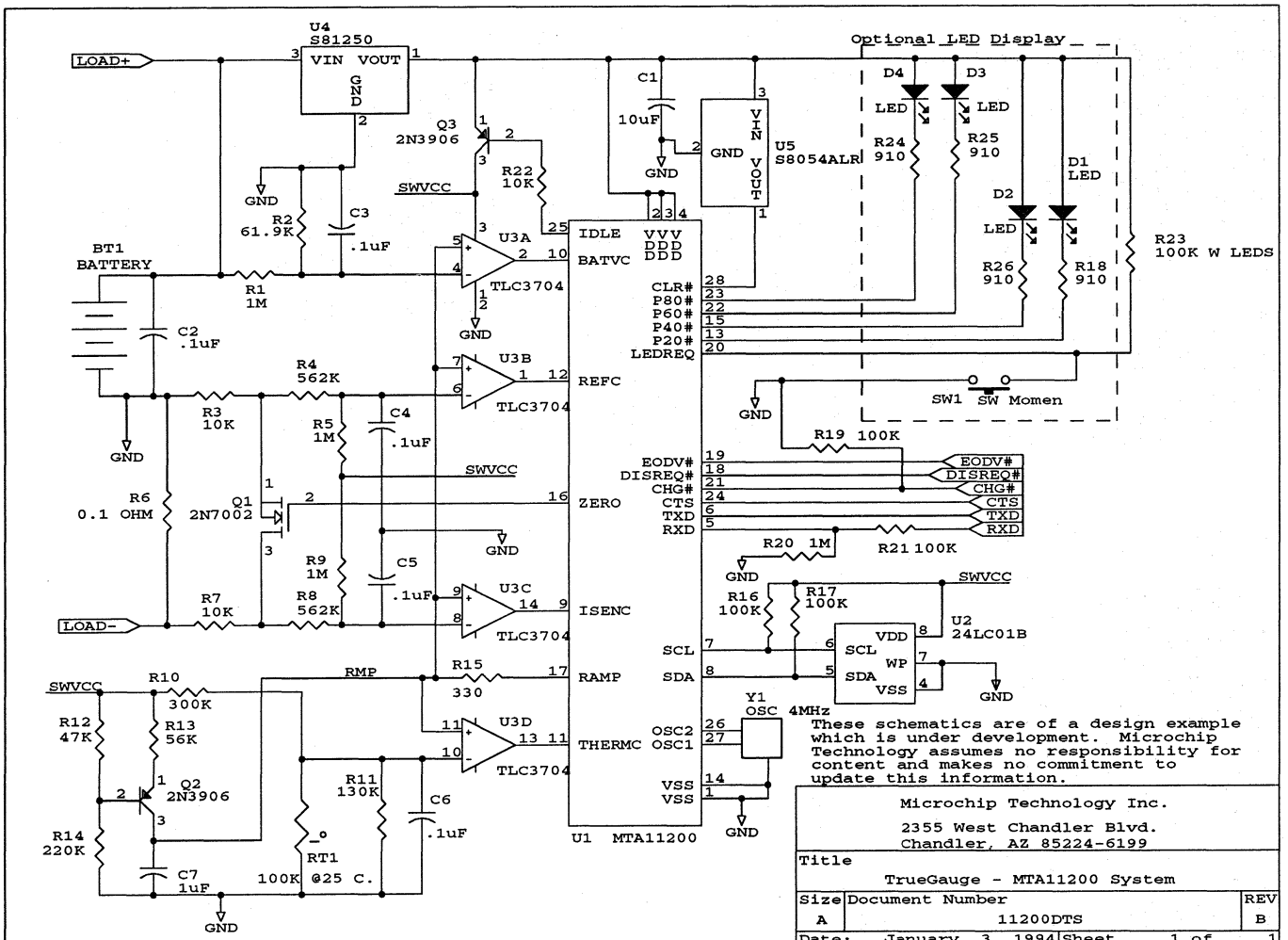
In this case the connection to the $\overline{CHG}$ is needed and the TXD connection usually is not needed. Again, LOAD+ provides the charge and discharge current path and LOAD- is the system ground.

Additionally, the $\overline{DISREQ}$ output can control a discharge circuit within the charger (or host for that matter) to instruct the charger to fully discharge (to EODV) the battery.

The external A/D components and the Serial EEPROM are routinely powered down to reduce power consumption when the MTA11200 is in the STANDBY state. The IDLE pin controls a transistor that switches the power bus to these circuits. The Serial EEPROM, comparators, current source, and their associated pull-up resistors and bias resistors are powered by this secondary power bus.

The MTA11200, voltage regulator (U4), and dropout voltage detector are always powered up as long as there is sufficient battery power. The voltage regulator protects the entire system from the battery voltage. It also provides the voltage that the A/D is referenced to.

The voltage detector forces the entire battery monitor system to shut down if the battery voltage falls below the operational limits of the I.C.'s in the system. This is added insurance against data corruption for both transmitted and stored data.



7.1 Component Selection

7.1.1 Current Sense Resistor

The MTA11200's programmable features accommodate a wide variety of battery types and load currents. The current slope correction factor stored in EEPROM defines the gain factor that the MTA11200 applies to the current measurement. By calibrating this gain factor and selecting the current sense resistor (R6) maximum sensitivity and dynamic range in the current measurements can be achieved.

The maximum discharging current and the maximum charging current expected in normal operation are the parameters that determine the required value of the current sense resistor. The resistor for the example circuit is selected based on the following formula:

Rsense <= 0.5V / Imax

The 0.5V maximum voltage drop limits the power dissipated by the resistor to an acceptable value. It also results in good measurement resolution.

7.1.2 Thermistor

A wide variety of linear thermistors can be used in a MTA11200-based system. The programmable gain and offset factors for thermistor input can be adjusted to obtain accurate temperature readings. The thermistor and it's associated bias resistors should be selected to ensure that voltage swing at the A/D comparator always remains within the range of the voltage ramp.

7.1.3 Serial EEPROM

The MTA11200 communicates with a 1Kbit Serial EEPROM organized as 128 bytes x 8 bits via standard I^2C protocol.

8.0 DEVELOPMENT SYSTEM

FEATURES

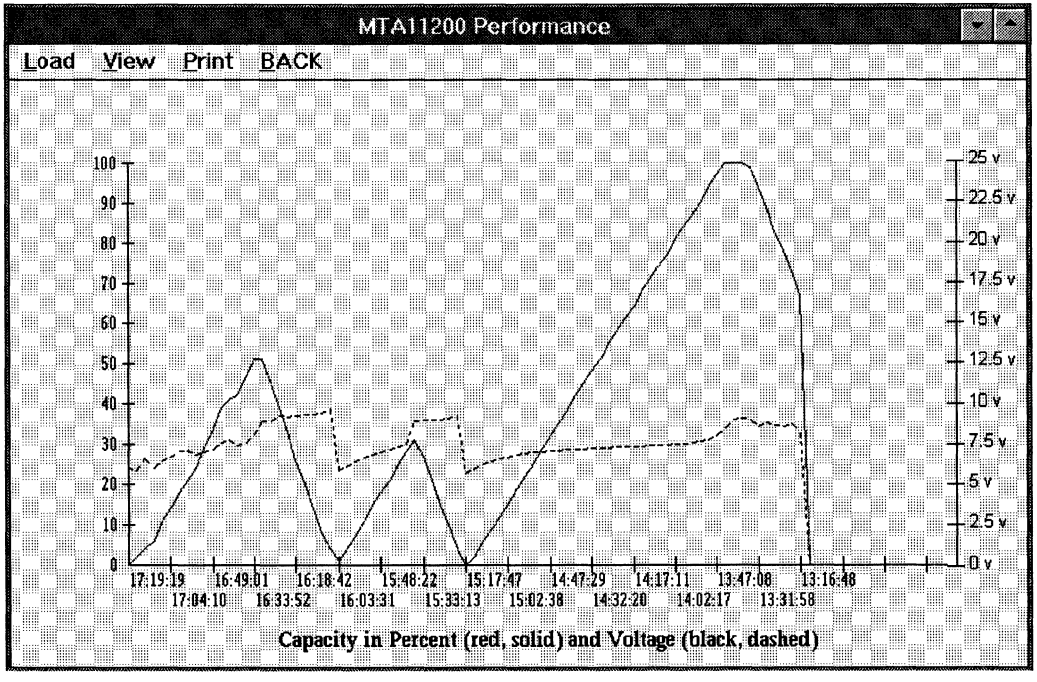
The MTA11200 development system is a full featured design environment to allow the system designer to design, validate and release full production products. The system includes:

- NiCd and NiMH battery packs, complete with MTA11200 intelligent battery management systems attached.
- Stand alone MTA11200 intelligent battery management system ready for customization.
- Charger/discharger control board with PC RS-232 cable and battery interface cable.
- MTA11200 *TrueGauge*™ design software package for Windows™ 3.1 operating system.
- International power supply
- Complete documentation

FUNCTION

The MTA11200 development system part number DV114001 has been designed to allow the user to collect real time data from the TrueGauge system and display it in a graphical format. In addition the software can log the data to disk for multiple design comparison or to archive current results for study at a later time. The data displayed can be one of four parameters: Voltage, Capacity, Temperature or Current. Voltage and Capacity are displayed concurrently as shown in Figure 8.1. The vertical scale shows capacity in percent between 0.0 (0%) and 1.0 (100%). The voltage per cell is shown on the scale above 1.0 and is in volts. Note that time increases to the left. Temperature is displayed in Figure 8.2 and current is displayed in Figure 8.3. The graphs read like a strip chart recorder with time increasing to the left.

FIGURE 8.1 - TRUEGAUGE VOLTAGE AND CAPACITY VS TIME



TrueGauge is a trademark of Microchip Technology Inc.
Windows is a trademark of Microsoft Corporation

FIGURE 8.2 - TEMPERATURE VS. TIME

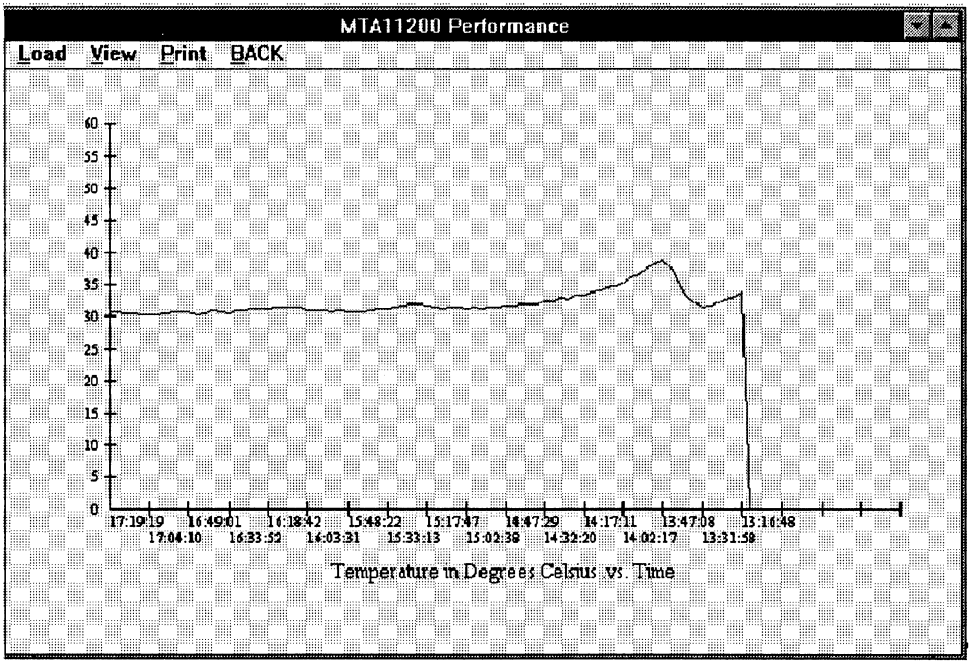
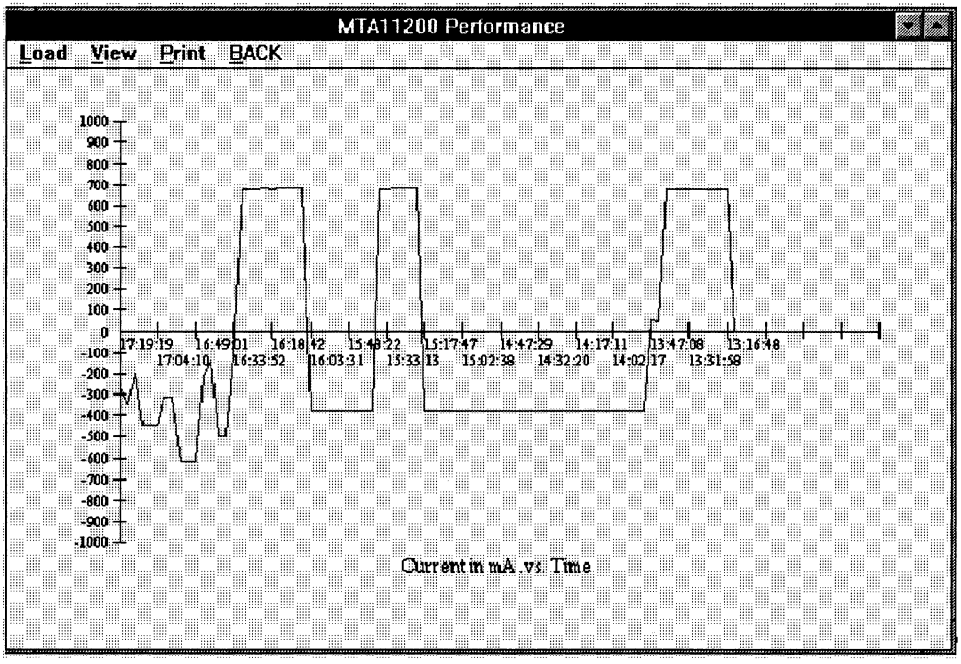
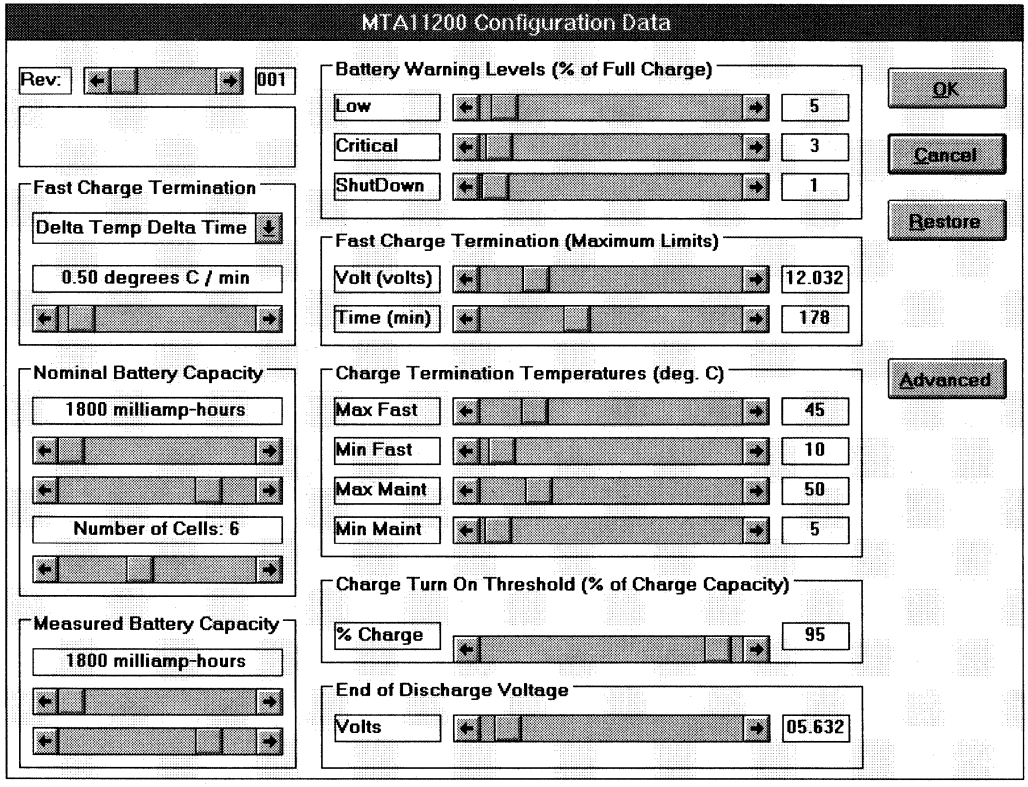


FIGURE 8.3 - CURRENT VS. TIME



In addition to the display and recording of data the software allows the user to easily configure the system EEPROM. The data contained within the EEPROM is all of the system parameters that control how the MTA11200 operates. To ease in the setup and archiving of this data, the TrueGauge development software has a user friendly configuration panel. This allows the user to easily configure the system for use with their specific battery packs. An example of the control panel to support this operation is shown below in Figure 8.4.

FIGURE 8.4 - CONFIGURATION CONTROL PANEL



9.0 ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings †

Ambient temperature under	-55°C to +125°C bias
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to Vss (except VDD and $\overline{CLR}$)	-0.6V to (VDD +0.6V)
Voltage on $\overline{CLR}$ pin with respect to Vss	0V to +14.0V
Voltage on VDD with respect to Vss	0V to +9.5V
Total power dissipation (Note 2)	800 mW
Maximum current out of Vss pin	150 mA
Maximum current into VDD pin	50 mA
Maximum current into input pin	± 500 uA
Maximum output current sinked by any I/O or output pin	25 mA
Maximum output current sourced by any I/O or output pin	20 mA

Notes:

1. Voltage spikes below Vss at the $\overline{CLR}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to this pin, rather than connecting this pin directly to Vss.
2. Total power dissipation should not exceed 800 mW for the package. The total power dissipation is calculated as follows: $P_{dis} = V_{DD} \times (I_{DD} - \sum I_{OH}) + \sum\{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$.

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

10.0 DC CHARACTERISTICS

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated). Operating Temperature 0°C < TA < 70°C for commercial. Operating voltage VDD = 3.0V to 5.5V unless otherwise stated.				
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply Voltage	VDD	3.0		6.25	V	FOSC = DC to 4 MHz
Vnn start voltage to guarantee power-on reset	VPOR		VSS		V	
Vnn rise rate to guarantee power-on reset	SVDD	0.05(1)			V/mS	
Supply Current	IDD ISTBY(2)		1.8 12	3.3 18	mA µA	FOSC = 4 MHz , VDD = 5.5V STANDBY Mode, FOSC= MHz, VDD = 5.0V
Input Low Voltage						
$\overline{CLR}$ (Schmitt trigger)	VILMC			.15 VDD	V	
OSC1 (Schmitt trigger)	VILOSC			.3 VDD	V	
All other Inputs	VIL			.2 VDD	V	
Input High Voltage						
$\overline{CLR}$ (Schmitt trigger)	VIHMC	.85 VDD		VDD	V	
OSC1 (Schmitt trigger)	VIHOSC	.7 VDD		VDD	V	
All other Inputs	VIH	.45 VDD		VDD	V	
Input Leakage Current						
$\overline{CLR}$	IILMCL	-5			µA	VPIN = Vss + 0.25V
$\overline{CLR}$	IILMCH		0.5	+5	µA	VPIN = VDD
OSC1 (Schmitt trigger)	IILMCH		0.5	+3	µA	Vss ≤ VPIN ≤ VDD
All other Inputs	IIL	-1	0.5	+1	µA	Vss ≤ VPIN ≤ VDD
Output Low Voltage						
All other Outputs	VOL			0.6V	V	IOL = 1.6 mA, VDD = 4.5V
Output High Voltage						
All other Outputs	VOH	VDD - .7			V	IOH =-1.0 mA, VDD = 4.5V

Note 1: These parameters are based on characterization and are not tested.

Note 2: The supply current in STANDBY mode is measured with all outputs unconnected and inputs tied to VDD or VSS.

10.1 DC Character Graphs

FIGURE 10.1.1 - TYPICAL ISTBY vs VDD AT 25 °C

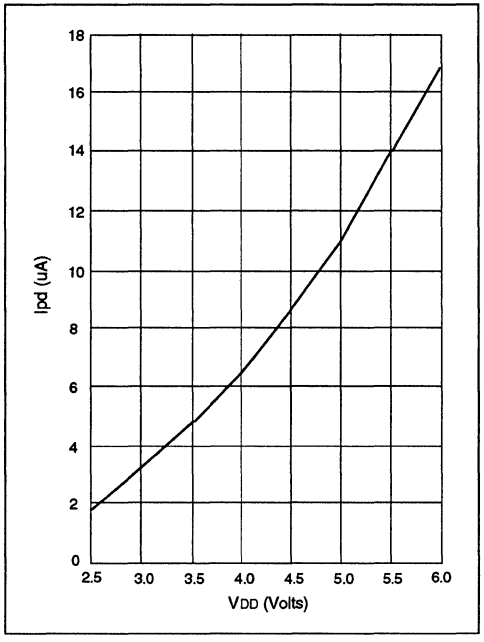


FIGURE 10.1.2 - MAXIMUM ISTBY vs VDD

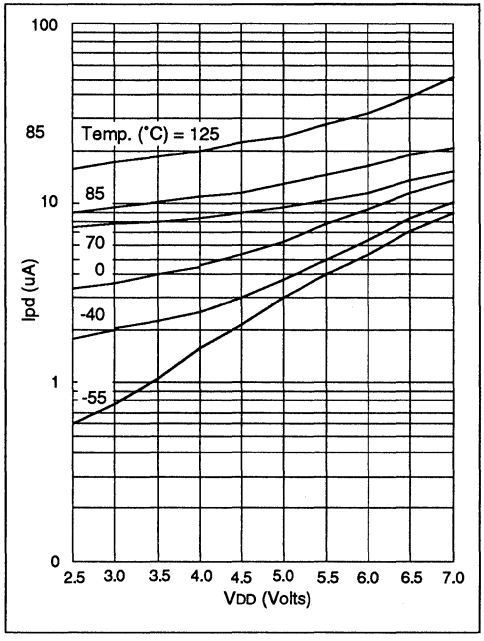


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FIGURE 10.1.3 - VTH (INPUT THRESHOLD VOLTAGE) OF INPUT AND I/O PINS vs VDD

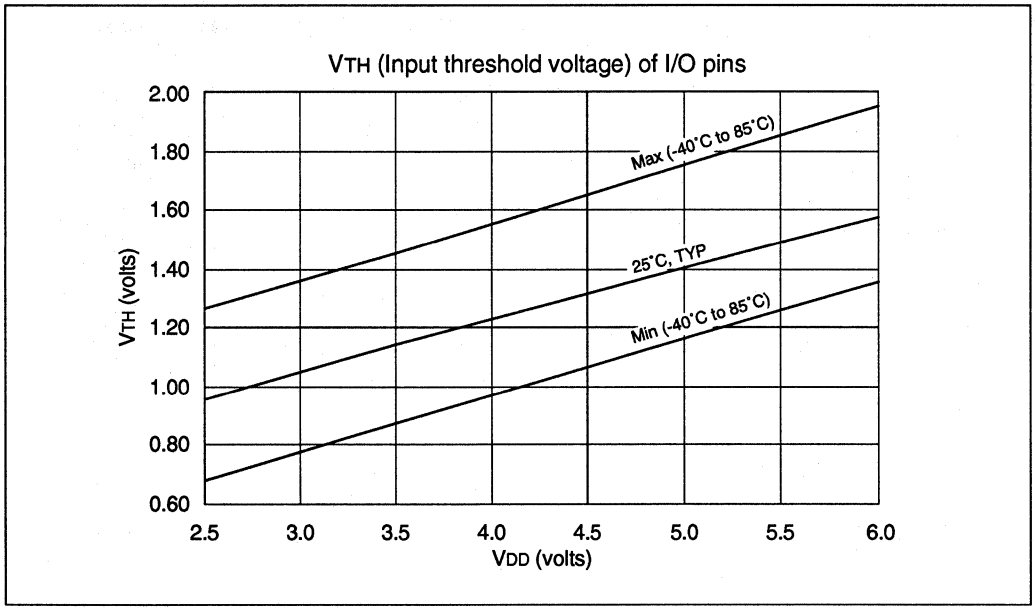
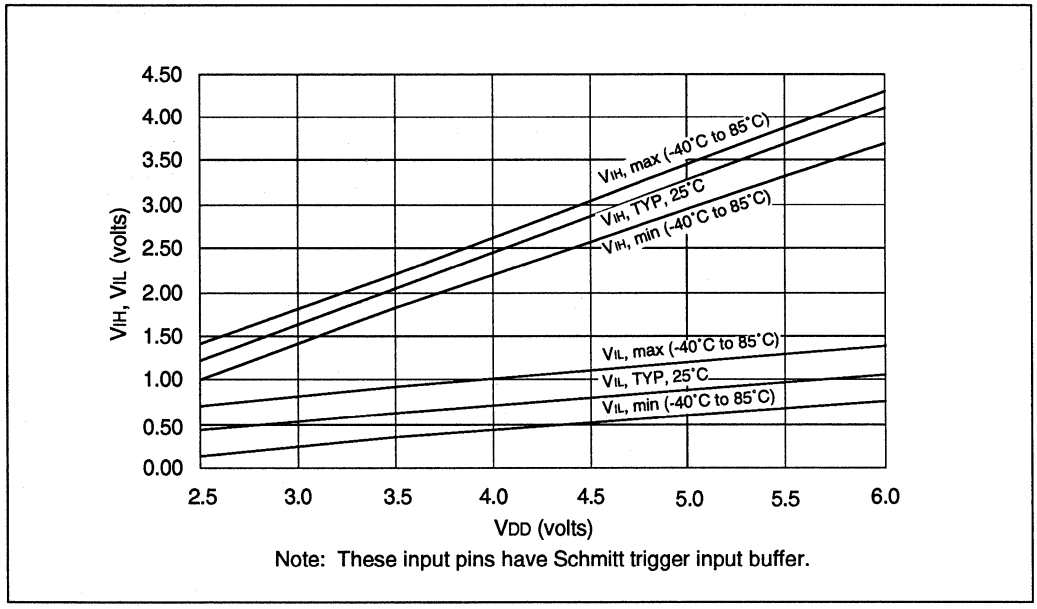


FIGURE 10.1.4 - VTH, VIH OF $\overline{CLR}$ INPUT vs VDD



Note: These input pins have Schmitt trigger input buffer.

FIGURE 10.1.5 - VTH OF $\overline{CLR}$ AND OSC1 INPUT vs VDD

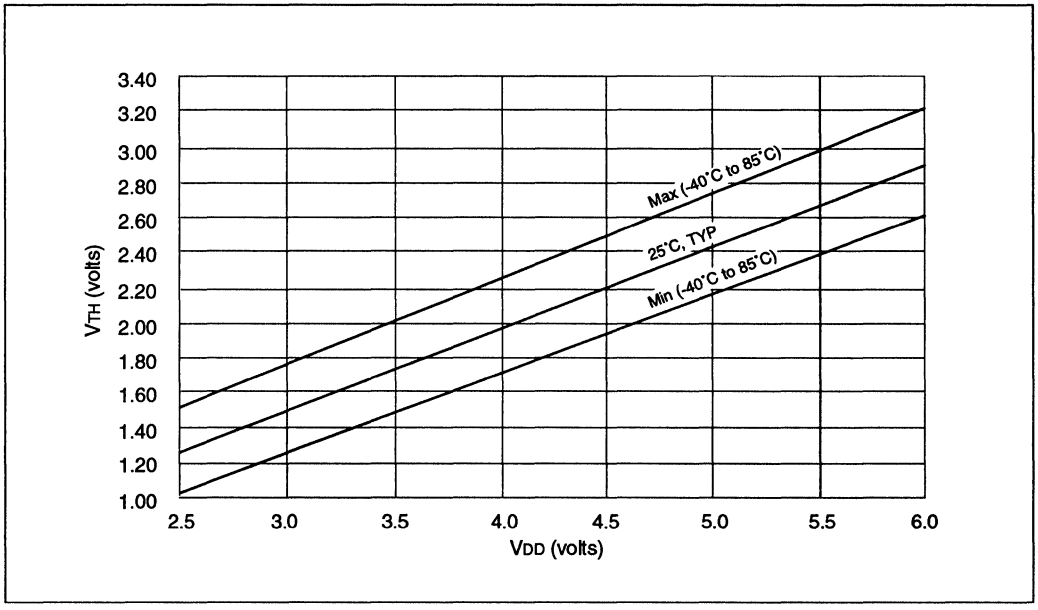


FIGURE 10.1.6 - TRANSCONDUCTANCE (G_M) OF OSCILLATOR vs VDD

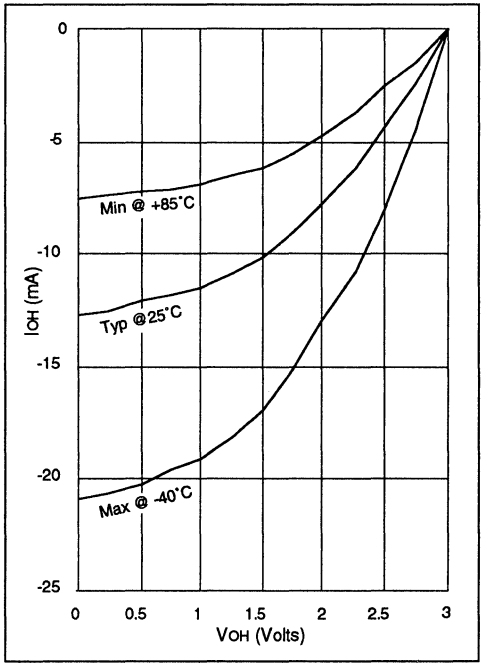


FIGURE 10.1.7 - IOH vs VOH, VDD = 3V

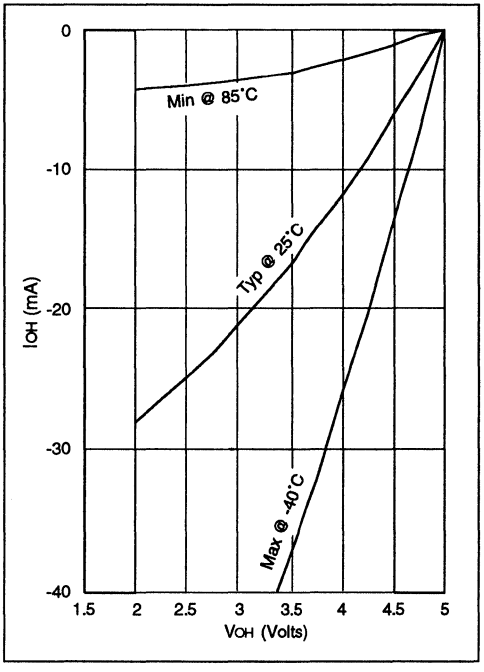


FIGURE 10.1.8 - I_{OH} vs V_{OH}, V_{DD} = 5V

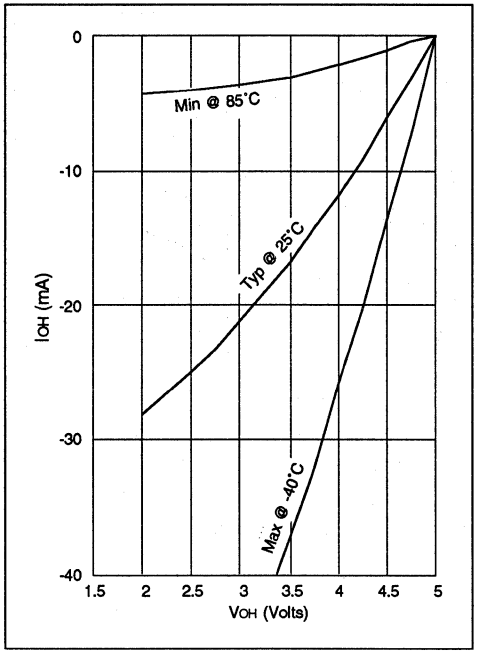


FIGURE 10.1.9 - I_{OL} vs V_{OL}, V_{DD} = 3V

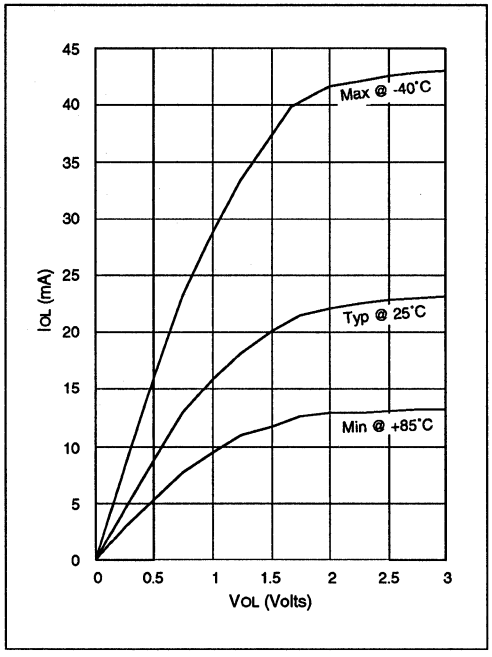


FIGURE 10.1.10 - I_{OL} vs V_{OL}, V_{DD} = 5V

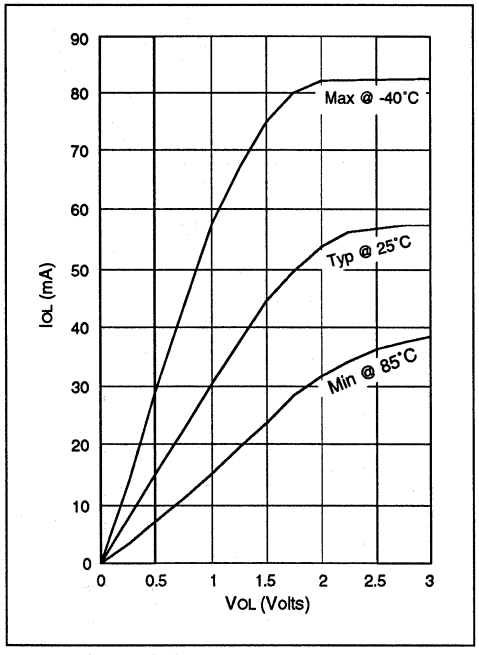


FIGURE 10.1.11 - INPUT CAPACITANCE

	Typical Capacitance (pF)	
Pin Name	**28L PDIP (600 mil)**	**28L SOIC**
INPUTS and I/Os	5	4
$\overline{CLR}$	17	17
OSC1	6	3
OSC2	4	3

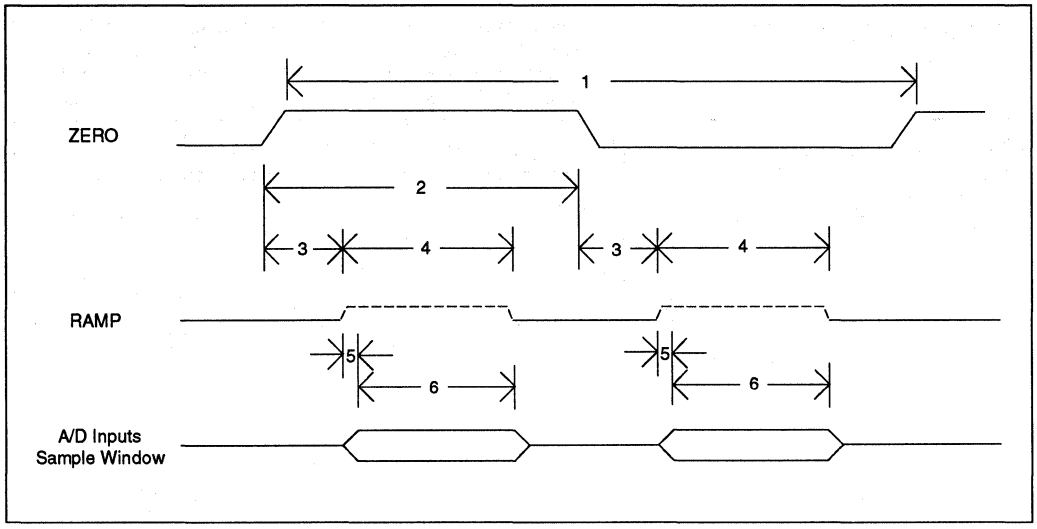
11.0 AC CHARACTERISTICS

AC CHARACTERISTICS						Standard Operating Conditions (unless otherwise stated). Operating Temperature 0°C < TA < 70°C for commercial. Operating Voltage VDD = 3.0V to 5.5V unless otherwise stated. Oscillator Frequency = 4 MHz.
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Oscillator Frequency	FOSC	DC		4	MHz	
RESET Timing						
$\overline{CLR}$ pulse width (low)	TMCL	100			ns	
Oscillator Start-up Timer Period	TOST (Note 1)	9	18	30	ms	VDD = 5.0 V

Note 1: These parameters are based on characterization and are not tested.

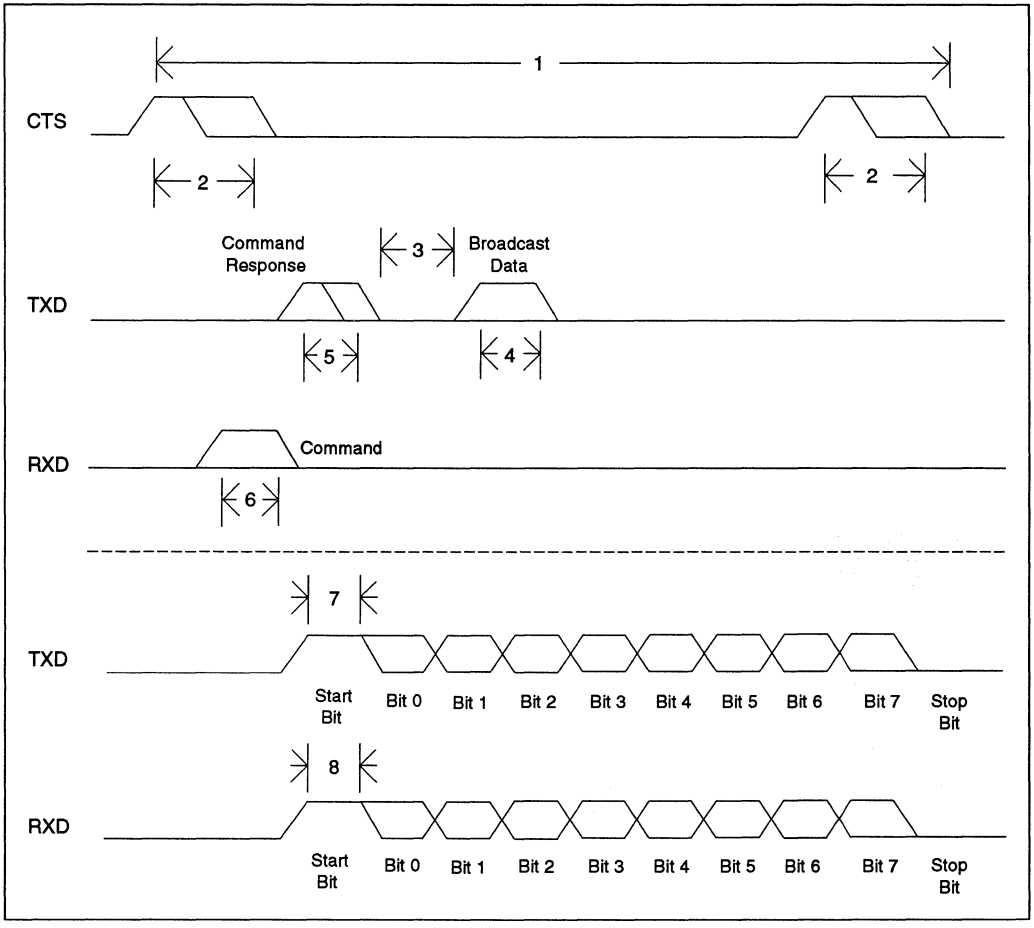
4

11.0.1 A/D Timing Diagram and Specifications



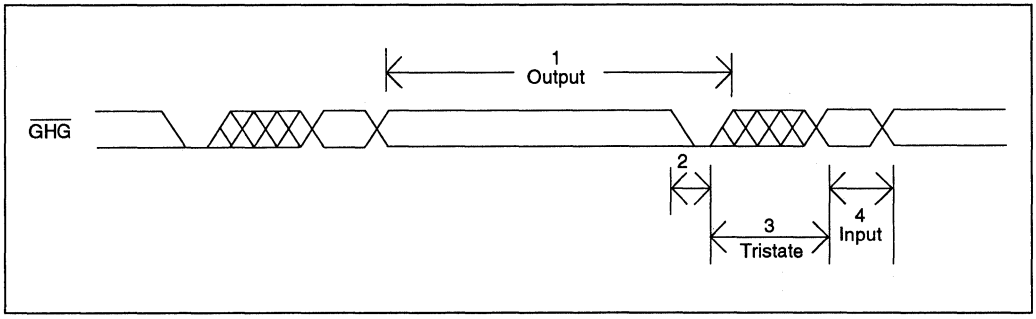
Param. No.	Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions: Standard Conditions unless otherwise stated
1	ZERO Pulse Period		TP:ZRO	1.65	1.75	1.85	S
2	ZERO Pulse Width		TW:ZRO	840	850	860	ms
3	RAMP Output Delay		TD:RMP		200		ms
4	RAMP Pulse Width		TW:RMP	640	650	660	ms
5	BATVC, REFC, ISENC, TEMPC A/D Input Window Delay Time	TD:ADI			20	µs	
6	BATVC, REFC, ISENC, TEMPC A/D Input Window Width		TW:ADI	640			µs

11.0.2 Host Communication Timing Diagram and Specifications



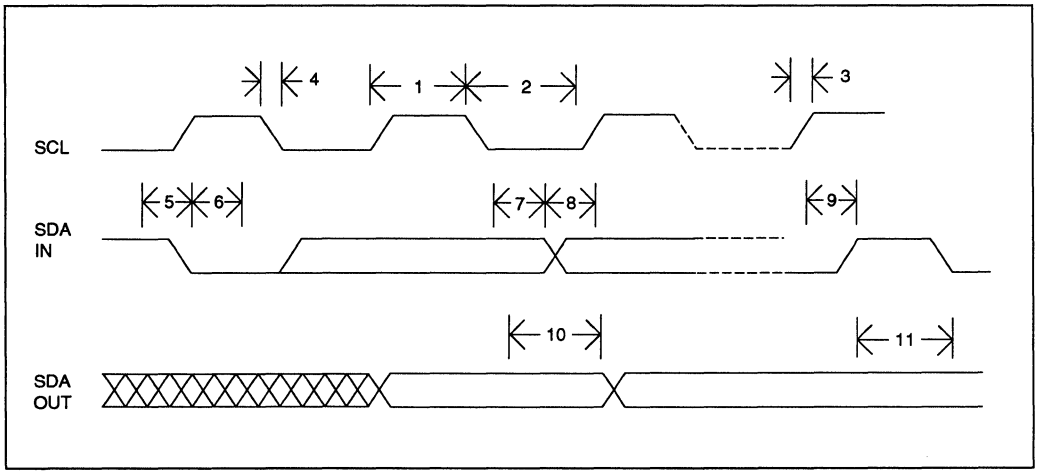
Param. No.	Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions: Standard Conditions unless otherwise stated
1	CTS Pulse Period	TP:CTS	1.65	1.75	1.85		
2	CTS Pulse Width	TW:CTS	2		12	ms	
3	RXD data to TXD (broadcast) Delay	TD:CTS			1	ms	
4	TXD (broadcast) Data Packet Width	TW:TXB	16.5		17.5	ms	
5	TXD (Cmd Resp.) Data Packet Width	TW:TXC			17.5	ms	
6	RXD Data Packet Width	TW:RX	1			µs	
7	TXD Bit Time	TT:TX	90	100	110	µs	9600 Baud
8	RXD Bit Time	TT:RX	60		110	µs	

11.0.3 Charge Control Timing Diagram and Specifications



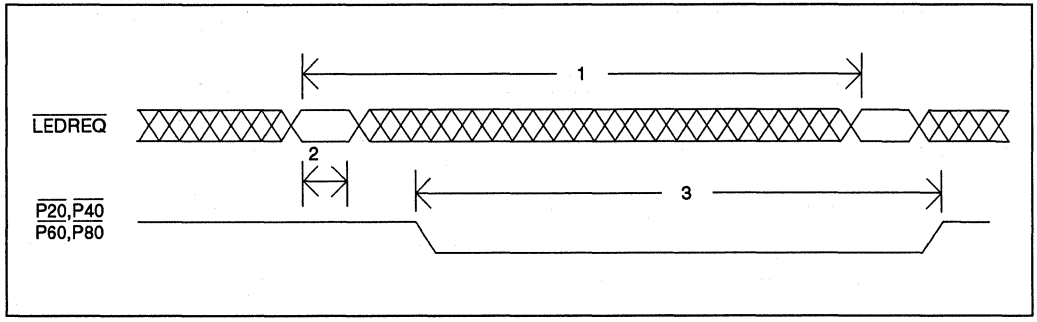
Param. No.	Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions: Standard Conditions unless otherwise stated
1	$\overline{CHG}$ Output Pulse Period	TP:CRG	1.65	1.75	1.85	s	
2	$\overline{CHG}$ Output Low (Input Preconditioning) Time	TOL:CRG	1	2	3	µs	
3	$\overline{CHG}$ Input Setup Time	TIW:CRG	7			µs	
4	$\overline{CHG}$ Input Window Time	TSU:CRG	1		2	µs	

11.0.4 I²C Bus Timing Diagram and Specifications



Param. No.	Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions: Standard Conditions unless otherwise stated
1	Clock high time		THI:SCL	4.0			µs
2	Clock low time		TLO:SCL	4.7			µs
3	SCL and SDA rise time		TR:SCD			300	µs
4	SCL and SDA fall time		TF:SCD			300	µs
5	Start condition setup time	TSU:STA	4.7			µs	
6	Start condition HOLD time	THD:STA	4.0			µs	
7	Data input hold time		THD:DAT	0			µs
8	Data input setup time		TSU:DAT	250			µs
9	Stop condition setup time	TSU:STO	4.7			µs	
10	Output valid from clock		TAA	3.5			µs
11	Bus free time		TBUF	4.7			µs
	Capacitive loading		CB			400	pF

11.0.5 LED Timing Diagram and Specifications



Param. No.	Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions: Standard Conditions unless otherwise stated
1	LEDREQ Input Sample Period	TP:LRQ	1.65	1.75	1.85	S	
2	LEDREQ Input Window		TW:LRQ		1		µS
3	P20, P40, P60, P80 Output Pulse Width		TPW:LED	1.65		1.75	S

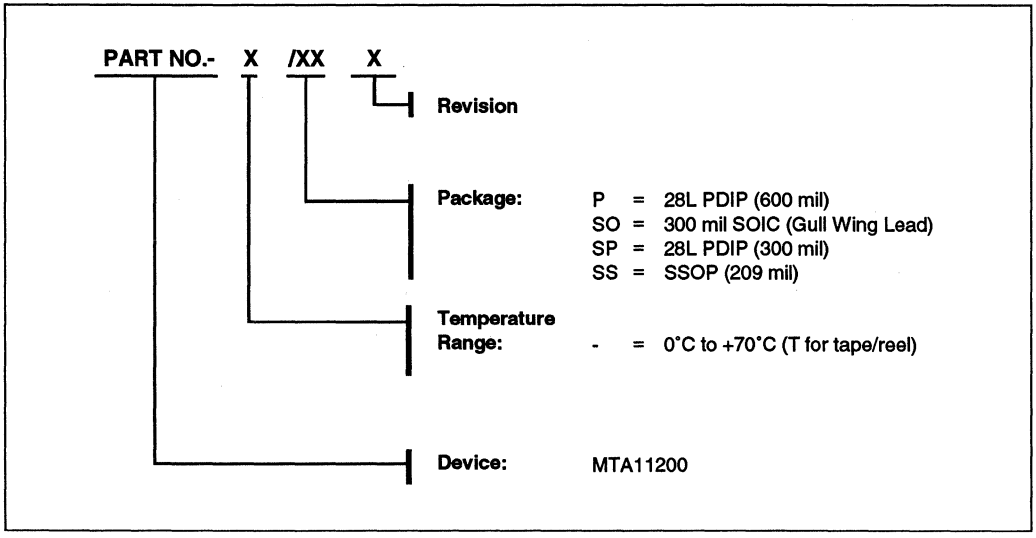
12.0 PACKAGING DIAGRAMS AND DIMENSIONS

See Section 11 of the Data Book.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



MICROCHIP

MTA41110

PS/2® Mouse and Trackball Controller I.C.

FEATURES

- Single-chip two-button mouse or trackball controller
- 10 KHz IBM® PS/2® interface
- IBM PS/2 mouse compliant
- Selectable Mouse or Trackball resolutions
- Strobed motion encoders for reduced system power consumption
- Motion sampling rate of 8700 Samples/second
- Proprietary anti-jitter algorithm simplifies motion encoder interface
- Available In:
  - 18-lead 300 mil PDIP
  - 18-lead 300 mil SOIC
  - 20-lead 209 mil SSOP

DESCRIPTION

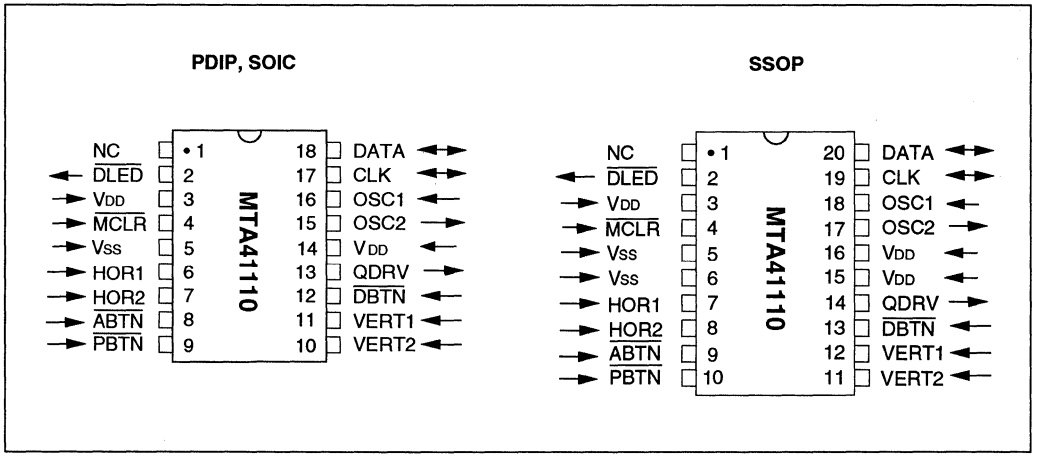
The MTA41110 is the heart of a simple, low-cost, mouse or trackball solution. It can be configured to operate as an IBM PS/2 compliant mouse or trackball controller. The mouse select and drag operation can be accomplished with a trackball by using the optional drag lock input and drag lock LED. This allows for one handed select and drag operation when using a trackball.

MTA41110

The MTA41110 is an 18-lead low-power CMOS integrated circuit. Combined with a few simple external components, a complete mouse or trackball system can be realized.

4

FIGURE A - PIN CONFIGURATIONS



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1.0 PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
NC	No Connect	This pin should be left unconnected
QDRV	Output	Active high strobed encoder drive
HOR1	Input	Horizontal quadrature input #1
HOR2	Input	Horizontal quadrature input #2
$\overline{PBTN}$	Input	Primary mouse button. Active low , 0 = button depressed
$\overline{ABTN}$	Input	Alternate mouse button. Active low, 0 = button depressed
$\overline{DBTN}$	Input	Optional trackball drag lock button. Active low, 0 = button depressed. For mouse operation connect this pin to VDD
VERT1	Input	Vertical quadrature input #1
VERT2	Input	Vertical quadrature input #2
$\overline{DLED}$	Output	Optional trackball drag LED. For mouse operation this pin is a no connect and should be left unconnected
OSC1	Input	4 MHz crystal or ceramic resonator connection
OSC2	Output	4 MHz crystal or ceramic resonator connection
DATA	I/O	Bi-directional data port for PS/2
CLK	Input	PS/2 data clock input
$\overline{MCLR}$	Input	A "low" voltage on this pin causes a reset condition for the MTA41110 controller
VDD	Pwr	+5V
VSS	Pwr	Ground

2.0 OPERATION

Upon power-up, the MTA41110 mouse controller initiates an internal reset sequence. First, all internal registers and communication parameters are cleared. Next, the status registers are set to the default condition. Finally, if the MTA41110 receives a Resend command as the first command after power-up, it will transmit a AAh followed by a 00h in response. This notifies the host that the initialization is complete and that the controller is a standard mouse type. This is to ensure compatibility with some hosts that do not follow the normally recommended behavior of issuing a Reset command as the first command after power-up.

The MTA41110 always confirms reception of a command sent by the host by returning an acknowledge byte (FAh). If the host interrupts the transmission of the acknowledge byte, the MTA41110 discards the complete command. The MTA41110 is then ready to receive and acknowledge the next command. Two exceptions to the acknowledge after command received rule exist. The MTA41110 does not issue an acknowledge upon receipt of either the Set Wrap Mode (EEh) or Resend (FEh) commands.

2.1 PS/2 COMMANDS

Command Summary:

Command	Code, Data
Reset	FFh
Resend	FEh
Set Default	F6h
Disable Reporting	F5h
Enable Reporting	F4h
Set Report Rate	F3h , XXh
Read Device Type	F2h
Set Remote Mode	F0h
Set Wrap Mode	EEh
Reset Wrap Mode	ECh
Read Data	EBh
Set Stream Mode	EAh
Status Request	E9h
Set Resolution	E8h , XXh
Set Scaling	E7h
Reset Scaling	E6h

2.1.1 Reset — Code: FFh

This command initiates a reset sequence in the MTA41110 mouse controller. First, all internal registers and communication parameters are cleared. Next, the status registers are set to the default condition. Finally, the MTA41110 transmits a AAh followed by a 00h, this informs the host that the initialization is complete and that the controller is a standard mouse type.

2.1.2 Resend — Code: FEh

Anytime the MTA41110 controller receives an invalidly formatted command, it will transmit a Resend command to the host. The controller will ignore invalid commands and will continue to operate in its present mode. When any command other than a Resend is received by the controller it will clear its motion and displacement counters.

The host system may send a Resend command to the controller if an error is detected in a transmission from the controller. When the controller receives a Resend command, it will retransmit the last data packet transmitted. If the last packet transmitted was a Resend command, the packet prior to the last packet will be retransmitted.

2.1.3 Set Default — Code: F6h

The Set Default command re-initializes all controller parameters to the power-up state. The controller initializes the following status registers.

Report rate:	100 reports per second
Scaling:	Linear
Mode:	Streaming
Resolution:	Physical Resolution / 2
Reporting:	Disabled

This command does not initiate any self-test diagnostics. The controller remains in the disabled state until another command is received from the host.

2.1.4 Disable Reporting — Code: F5h

The Disable Reporting command prevents data transmission by the controller while it is in the Stream Mode. However, the controller will still respond to other commands. When reporting is disabled, Stream Mode must be disabled prior to the host sending a command that requires a response by the controller.

2.1.5 Enable Reporting — Code: F4h

The Enable Reporting command allows the controller to transmit data when in Stream Mode. This command has no effect while the controller is in Remote Mode.

2.1.6 Set Report Rate — Code: F3h , XXh

This command updates the report rate status register with the data contained in the second byte of the command. However, the physical report rate remains fixed at 40 times per second. This command only exists to ensure compatibility.

2.1.7 Read Device Type — Code: F2h

The controller always transmits a 00h in response to receiving this command. This informs the host that a standard mouse is present.

2.1.8 Set Remote Mode — Code: F0h

Remote Mode is entered when the controller receives this command. In Remote Mode, event packets are transmitted to the host only when a read data command is received by the controller.

2.1.9 Set Wrap Mode — Code: EEh

Wrap Mode is entered when the controller receives this command. In Wrap Mode, the controller will echo all commands that are received back to the host. Note, the Reset and Reset Wrap commands will cancel Wrap Mode and neither of these commands will be echoed back to the host. Wrap Mode can be enabled in either Reporting Mode, Stream Mode or Remote Mode.

2.1.10 Reset Wrap Mode — Code: ECh

This command cancels Wrap Mode. The controller remains in the current Reporting Mode. Note, if the controller enters Wrap Mode while in Stream Mode and then a Reset Wrap Mode command is received, the controller will reenter the Stream Mode with Wrap Mode disabled.

2.1.11 Read Data — Code: EBh

The controller will transmit an event packet to the host after a read data command is received. This command can be issued in either the Remote or Stream Modes. The controller will transmit data even if there has not been any button changes or motion since the last report. The controller clears the motion counters after ever read data command.

2.1.12 Set Stream Mode — Code: EAh

The controller will enter the Stream Mode upon receiving this command. In Stream Mode, event packets are transmitted to the host as they occur.

2.1.13 Status Request Code: E9h

A three byte status report packet will be transmitted in response to this command. These status bytes are defined as follows:

Byte 1:

Bit	Description
0	1 = Secondary Button Depressed
1	Reserved
2	1 = Primary Button Depressed
3	Reserved
4	1 = 2:1 Scaling
5	1 = Enabled
6	1 = Remote Mode
7	Reserved

Byte 2: Current Resolution

Byte 3: Current Sample Rate

2.1.14 Set Resolution Code: E8h , XXh

The controller provides four resolutions selected by the second byte of this command. The effective resolution is the physical device resolution divided by the divisor indicated below.

Second Byte	Description
0	divide by 8
1	divide by 4
2	divide by 2
3	divide by 1

2.1.15 Set Scaling Code: E7h

This command has no effect on resolution and only exists to ensure compatibility.

2.1.16 Reset Scaling Code: E6h

This command resets the scaling to 1:1 (input count equals reported count).

2.2 PS/2 Message Data Format

The following PS/2 compliant data format is used by the MTA41110 when transmitting data to the host and when receiving data from the host. The data format utilizes an 11 bit data frame that utilizes 8 bits for message data and 3 bits for control.

Data Frame Format :

Bit	Description
1	Start Bit (always 0)
2	Message Data Bit 0 , LSB
3	Message Data Bit 1
4	Message Data Bit 2
5	Message Data Bit 3
6	Message Data Bit 4
7	Message Data Bit 5
8	Message Data Bit 6
9	Message Data Bit 7 , MSB
10	Parity Bit (odd parity)
11	Stop bit (always 1)

The MTA41110 mouse controller transmits the following three byte data packet in response to a Read Data (EBh) command or when operating in Stream Mode with reporting enabled.

Status Message Data Byte 1:

Bit	Description
0	1 = Primary Button Depressed
1	1 = Secondary Button Depressed
2	Reserved
3	Reserved
4	X data sign, 1 = negative
5	Y data sign, 1 = negative
6	X data overflow, 1 = overflow
7	Y data overflow, 1 = overflow

Status Message Data Byte 2:

Delta X motion

Status Message Data Byte 3:

Delta Y motion

3.0 MOTION ENCODER INTERFACE

The MTA41110 is designed to interface to both optical encoders that utilize LED and photo transistor pairs with a chopper wheel or mechanical encoders that utilize a commutator with wiper contacts.

Power consumption is reduced by strobing the motion encoder power each time the encoders are sampled. The MTA41110 will drive the QDRV output high 8 µS (with 4 MHz input clock) prior to sampling the HOR and VERT inputs to give the encoders time to stabilize. The QDRV output will be driven back low 2 µs after the sample is taken. If power consumption is not a concern, then the QDRV output can be left unconnected and encoders can be powered directly from a constant supply (e.g. +5V power).

An anti-jitter algorithm is employed to eliminate false motion counting when the mouse or trackball is not moving. This is especially useful in designs employing optical encoders since the output of an optical detector is an analog signal. The anti-jitter algorithm eliminates false counting when a voltage that is not a well defined logic low or logic high is applied to either the HOR or VERT inputs.

The HOR and VERT inputs detect positive and negative delta motion. Motion direction is defined in the following state table along with Figures 3.1 and 3.2.

Positive Motion:

Hor1,Hor2 / Vert1,Vert2	Description
0,0	
0,1	
1,1	Positive Direction Sequence
1,0	
0,0	
etc.	

Negative Motion:

Hor1,Hor2 / Vert1,Vert2	Description
0,0	
1,0	
1,1	Negative Direction Sequence
0,1	
0,0	
etc.	

The HOR and VERT inputs are sampled at ~8700 samples per second with a 4 MHz input clock. The sample rate will decrease slightly when communication traffic to or from the host is occurring. The sample rate is directly proportional to the clock frequency on the OSC1 and OSC2 pins.

4

FIGURE 3.1 - POSITIVE MOTION SEQUENCE

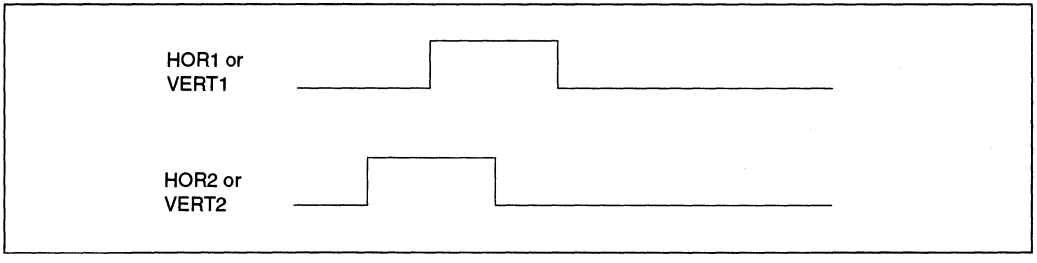
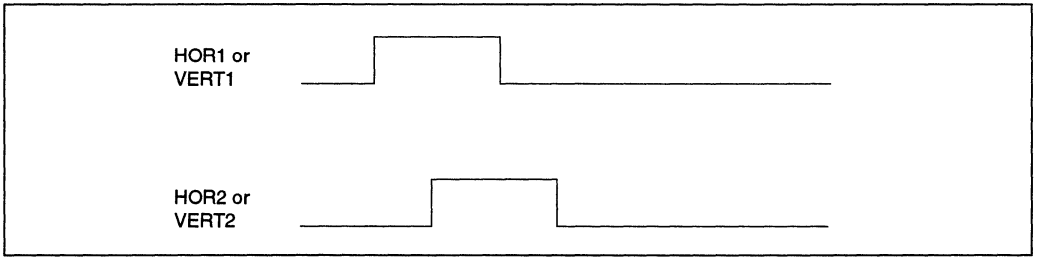


FIGURE 3.2 - NEGATIVE MOTION SEQUENCE



4.0 PUSH-BUTTON INPUTS

The MTA41110 push-button inputs are defined to be active when the input pin is in the low state. The appropriate message data bit will be set equal to one when a low is sampled at a switch input. When a switch input is sampled in the high state, the appropriate message data bit will be set equal to zero.

5.0 TRACKBALL OPTION

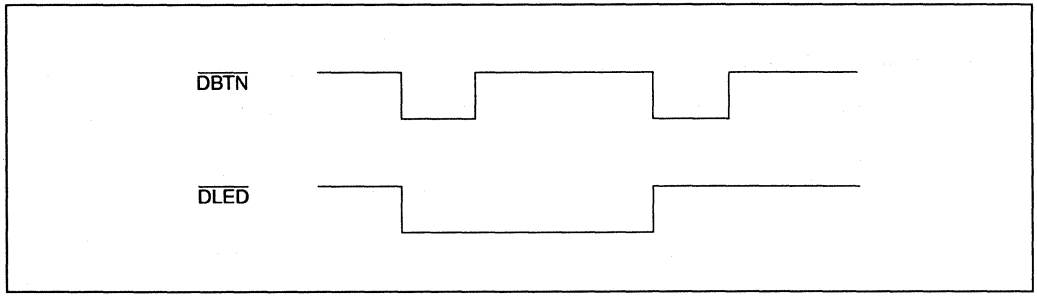
The MTA41110 can also function as a trackball controller. A trackball drag lock switch can be connected to the $\overline{DBTN}$ input and an LED indicator connected to the $\overline{DLED}$ output to aid in one-handed trackball operation.

When using a mouse, a select and drag operation is performed by clicking on an object and holding the primary mouse button down. Moving the mouse then drags the object to the desired location. When the primary button is released the object is placed at the desired location. However, when the same select and drag operation is performed using a trackball, it may be difficult to hold the button depressed and guide the trackball with the same hand.

The MTA41110's "drag lock" feature allows this function to be accomplished with one hand. The drag lock is set to the "locked" state by momentarily applying a low to the $\overline{DBTN}$ input. This "locked" state is equivalent to depressing and holding the primary mouse button. The user then guides the object to the desired location without having to hold a button depressed and simultaneously guide the trackball. The object is placed and the "lock" is released when a low (e.g. button depressed) is momentarily applied to any button input.

The $\overline{DLED}$ output is latched in the low state (0V) when the $\overline{DBTN}$ input is sampled low (refer to Figure 5.1). The $\overline{DLED}$ output will remain low ("locked") until the $\overline{DBTN}$ input is sampled high and then sampled low again. Exiting the locked state also occurs if the $\overline{PBTN}$ input or $\overline{SBTN}$ input is sampled low when the $\overline{DLED}$ output is low. When the $\overline{DLED}$ output is in low "locked" state, the Primary Button depressed bit in the status message is set high.

FIGURE 5.1 - TRACKBALL DRAG LOCK OPERATION



6.0 ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS †

Ambient temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$)	-0.6V to (V_{DD} +0.6V)
Voltage on $\overline{MCLR}$ pin with respect to V_{SS}	0V to +14.0V
Voltage on V_{DD} with respect to V_{SS}	0V to +9.5V
Total power dissipation (Note 2)	800 mW
Maximum current out of V_{SS} pin	150 mA
Maximum current into V_{DD} pin	50 mA
Maximum current into input pin	±500 µA
Maximum output current sinked by any I/O or output pin	25 mA
Maximum output current sourced by any I/O or output pin	20 mA

Notes:

1. Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to this pin, rather than connecting this pin directly to V_{SS}.
2. Total power dissipation should not exceed 800 mW for the package. The total power dissipation is calculated as follows:

   $P_{DIS} = V_{DD} \times (I_{DD} - \sum I_{OH}) + \sum\{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

4

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

6.2 DC CHARACTERISTICS MTA41110 (COMMERCIAL)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated). Operating Temperature 0°C < TA < 70°C for commercial. Operating voltage VDD = 3.0V to 5.5V unless otherwise stated.				
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply Voltage	VDD	3.0		6.25	V	FOSC = DC to 4 MHz
VDD start voltage to guarantee power-on reset	VPOR		VSS		V	
VDD rise rate to guarantee power-on reset	SVDD	0.05*			V/mS	
Supply Current	IDD		1.8	3.3	mA	FOSC = 4 MHz , VDD = 5.5V
Input Low Voltage						
$\overline{MCLR}$ (Schmitt trigger)	VILMC			.15 VDD	V	
OSC1 (Schmitt trigger)	VILOSC			.3 VDD	V	
All other Inputs	VIL			.2 VDD	V	
Input High Voltage						
$\overline{MCLR}$ (Schmitt trigger)	VIHMC	.85 VDD		VDD	V	
OSC1 (Schmitt trigger)	VIHOSC	.7 VDD		VDD	V	
All other Inputs	VIH	.45 VDD		VDD	V	
		2V		VDD		4.0V < VDD ≤ 5.5V
Input Leakage Current						
$\overline{MCLR}$	IILMCL	-5			µA	VPIN = VDD + 0.25V
$\overline{MCLR}$	IILMCH		0.5	+5	µA	VPIN = VDD
OSC1 (Schmitt trigger)	IILMCH		0.5	+3	µA	VDD ≤ VPIN ≤ VDD
All other Inputs	IIL	-1	0.5	+1	µA	VDD ≤ VPIN ≤ VDD
Output Low Voltage						
OSC2	VOL			0.6	V	IOL = 1.6 mA, VDD = 4.5V
All other Outputs	VOL			0.6	V	IOL = 8.7 mA, VDD = 4.5V
Output High Voltage						
OSC2	VOH	VDD - .7			V	IOH = -1.0 mA, VDD = 4.5V
All Outputs	VOH	VDD - .7			V	IOH = -5.4 mA, VDD = 4.5V

*These parameters are based on characterization and are not tested.

FIGURE 6.2.1 - INPUT THRESHOLD VOLTAGE (V_{TH}) OF ALL INPUT AND I/O PINS EXCEPT $\overline{MCLR}$ AND OSC1

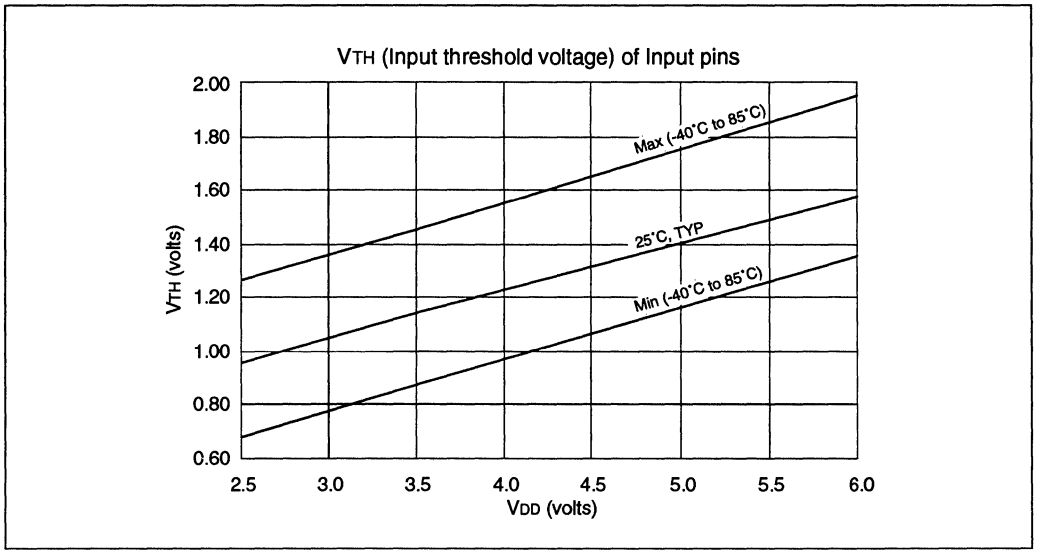
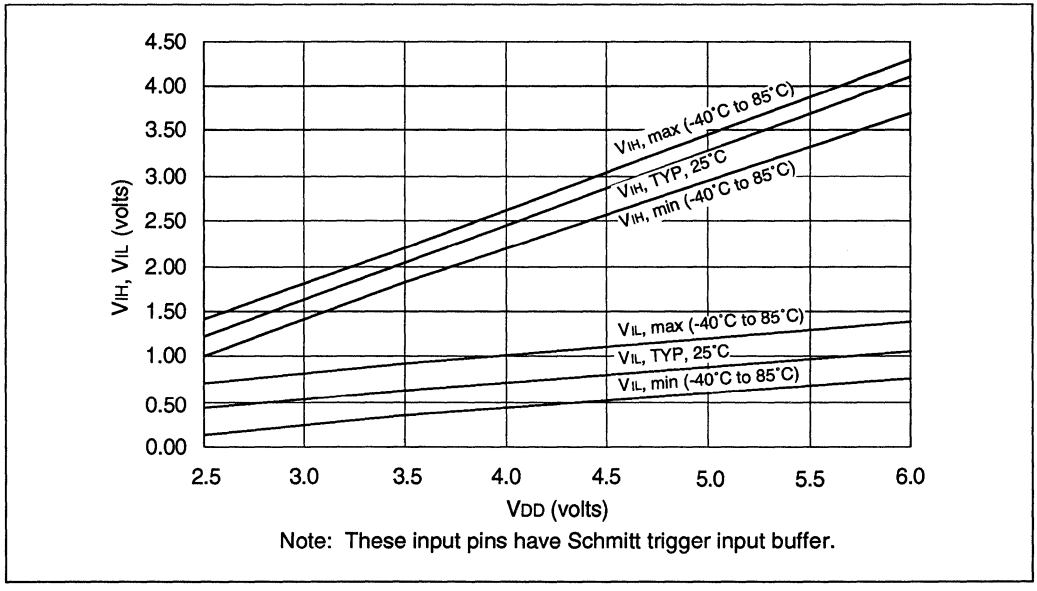


FIGURE 6.2.2 - V_{IH}, V_{IL} OF $\overline{MCLR}$ vs V_{DD}



Note: These input pins have Schmitt trigger input buffer.

FIGURE 6.2.3 - INPUT THRESHOLD VOLTAGE (V_{TH}) OF OSC1 INPUT

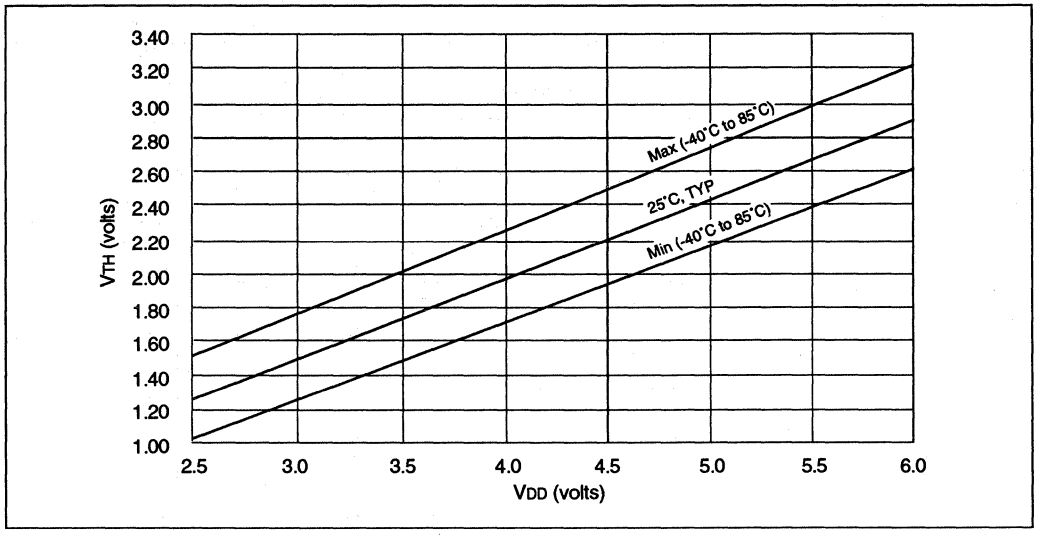


FIGURE 6.2.4 - I_{OH} vs V_{OH}, V_{DD} = 3V

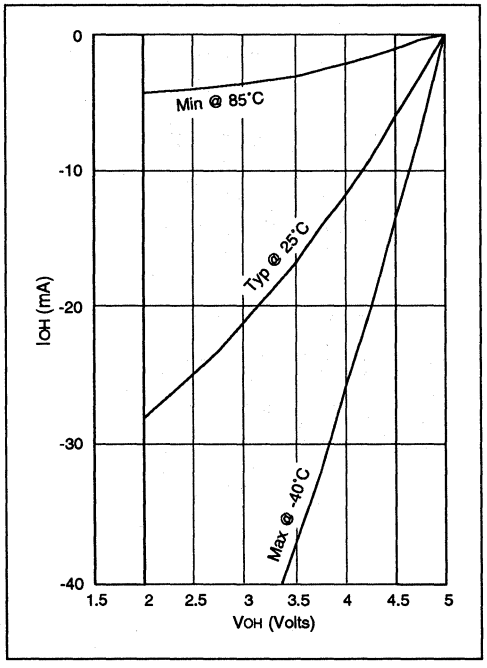


FIGURE 6.2.5 - I_{OH} vs V_{OH}, V_{DD} = 5V

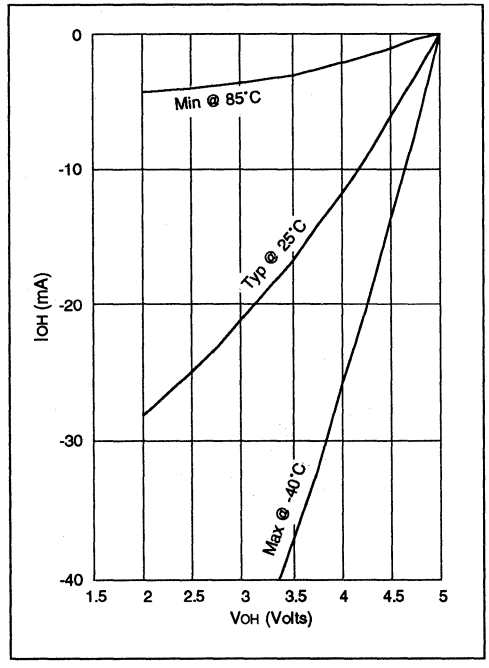


FIGURE 6.2.6 - IOL vs VOL, VDD = 3V

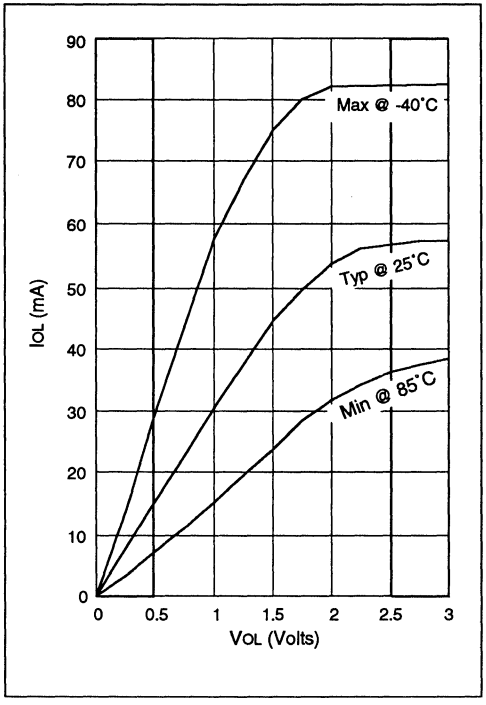
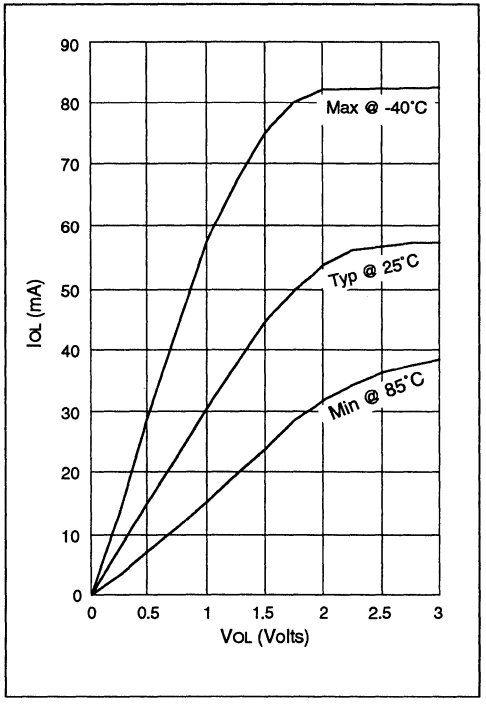


FIGURE 6.2.7 - IOL vs VOL, VDD = 5V



4

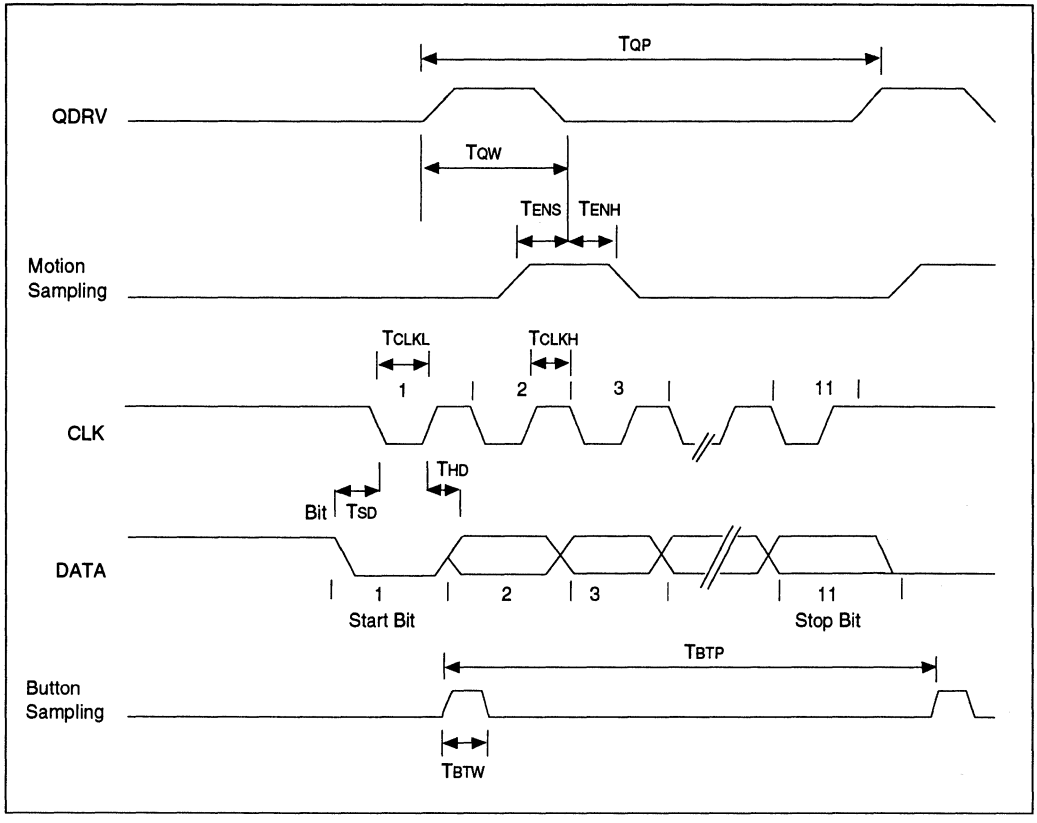
6.3 AC CHARACTERISTICS MTA41110 (COMMERCIAL)

AC CHARACTERISTICS						Standard Operating Conditions (unless otherwise stated). Operating Temperature 0°C < TA < 70°C for commercial. Operating Voltage VDD = 3.0V to 5.5V unless otherwise stated. Oscillator Frequency = 4 MHz.
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Oscillator Frequency	FOSC	DC		4	MHz	
Motion Encoder Timing						
QDRV						
Pulse Period	TQP (Note 2)		115		µS	
Pulse Width	TQW	8	10	12	µS	
HOR1,HOR2,VERT1,VERT2						
Input Sample Setup Time	TENS	3			µS	Before QDRV falling edge.
Input Sample Hold	TENH			0	nS	After QDRV falling edge.
I/O Timing						
CLK High time	TCLKH	30		50	µS	
CLK Low time	TCLKL	30		50	µS	
DATA setup time to CLK falling	TSD	5		25	µS	
DATA hold time to CLK rising	THD	5		45		
Button Input Timing						
$\overline{PBTN}$, $\overline{SBTN}$, $\overline{DBTN}$						
Input Sample Period	TBTP (Note 2)			50	ms	
Input Sample Window width	TBTW			280	ns	
RESET Timing						
$\overline{MCLR}$ pulse width (low)	TMCL	100			ns	
Oscillator Start-up Timer Period	TOST (Note 1)	9	18	30	ms	VDD = 5.0V

Notes:

1. These parameters are based on characterization and are not tested.
2. Sampling can be suspended if device is receiving data from host or transmission to host is inhibited by host (CLK held low)

FIGURE 6.3.1 - TIMING DIAGRAMS



7.0 APPLICATION EXAMPLE

The MTA41110 controller can be configured as either a mouse or trackball controller. Trackball systems require the addition of the components labeled as trackball only. These components allow support of a drag lock switch and indicator. A pull-up resistor for the drag lock switch must be included in trackball systems. For a mouse, the $\overline{DBTN}$ input is simply connected to V_{DD}.

Three examples of motion encoders are shown in the schematics (Document Number 41XXXEN). Two types of optical encoders and a mechanical type are shown. Since the MTA41110 employs an anti-jitter algorithm, the "basic" style of optical encoder or the mechanical encoder are both recommended for use with the MTA41110. Use of the "improved" style of optical encoder that employs comparators may only be necessary in high noise environments.

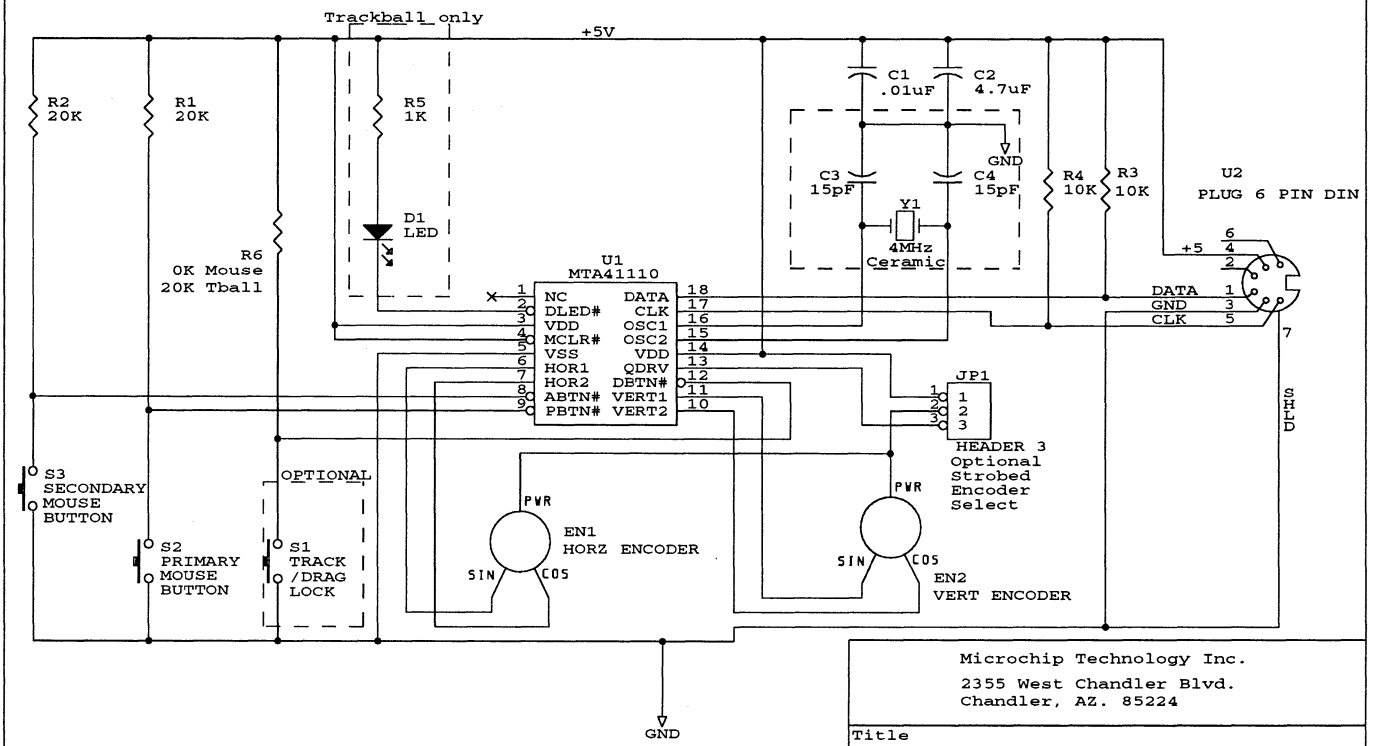
All button switches should be of the momentary contact type, including the drag lock switch.

7.1 Host System Device Drivers

The MTA41110 is compatible with standard IBM PS/2 device drivers. Additionally, host system software device drivers for use with the MTA41110 are available from third party vendors. Contact your local sales office for a list of vendors currently offering device drivers that support the MTA41110.

Microchip Technology Inc.

MTA41110 Based PS/2 Mouse or Trackball



These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

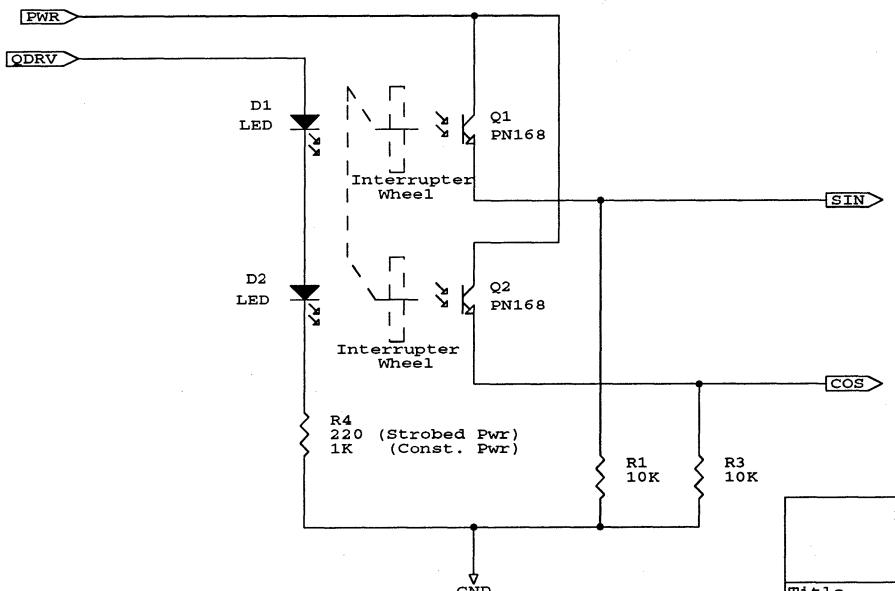
Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ. 85224

Title: MTA41110 Full Featured PS2 Mse/Tball Cntrlr		
Size: A	Document Number: 41110PSa	REV: B
Date: June 11, 1993	Sheet: 1 of 1	

4

Microchip Technology Inc.

Basic Mouse/Trackball Optical Motion Encoder



LINK
OPTO2.SCH
MECH.SCH

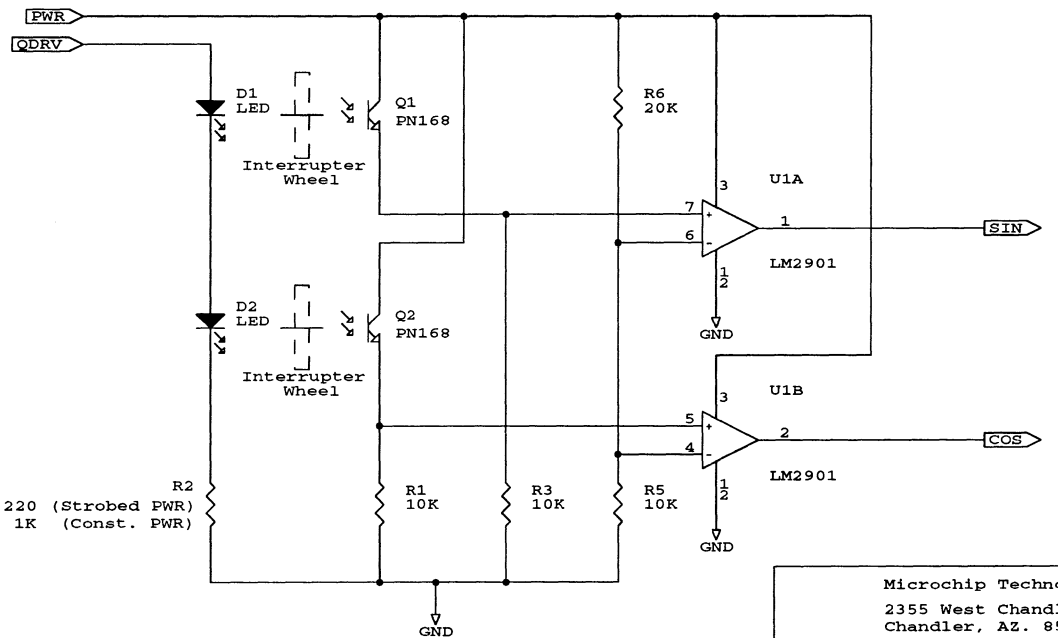
These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ. 85224

Title		
Typical Optical Motion Encoder		
Size: A	Document Number: 41XXXEN	REV: C
Date: August 24, 1993	Sheet: 1 of 3	

Microchip Technology Inc.

Improved Mouse/Trackball Optical Motion Encoder



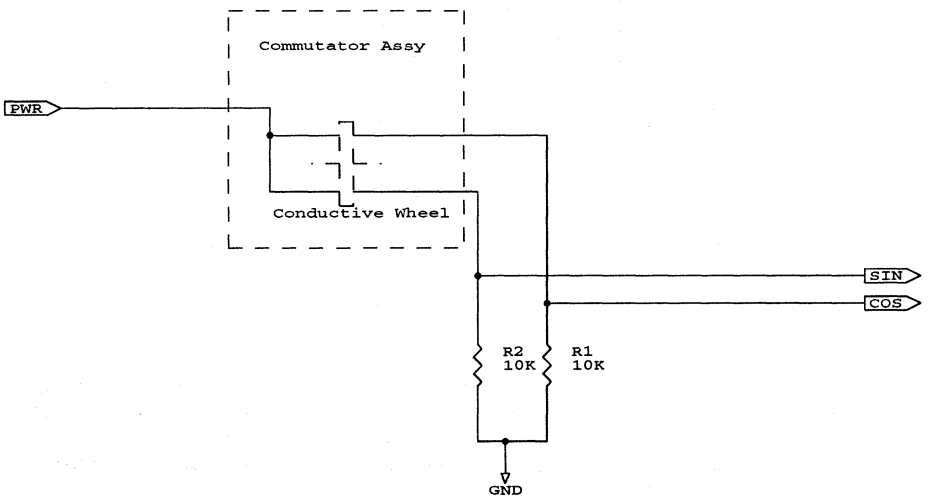
These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

Microchip Technology Inc. 2355 West Chandler Blvd. Chandler, AZ. 85224		
Title: Improved Optical Motion Encoder		
Size: A	Document Number: 41XXXEN	REV: C
Date: August 24, 1993	Sheet: 2 of 3	

4

Microchip Technology Inc.

Mouse/Trackball Mechanical Motion Encoder



These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

Microchip Technology Inc. 2355 West Chandler Blvd. Chandler, AZ. 85224	
Title Typical Mechanical Motion Encoder	
Size A	Document Number 41XXXEN REV C
Date: August 20, 1993	Sheet 3 of 3

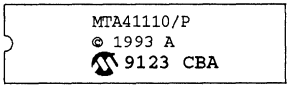
8.0 PACKAGING DIAGRAMS AND DIMENSIONS

See Section 11 of the Data Book.

9.0 PACKAGE MARKING INFORMATION

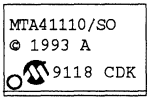
18L PDIP

Example

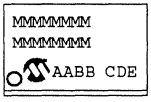


18L SOIC

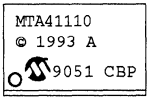
Example



20L SSOP



Example



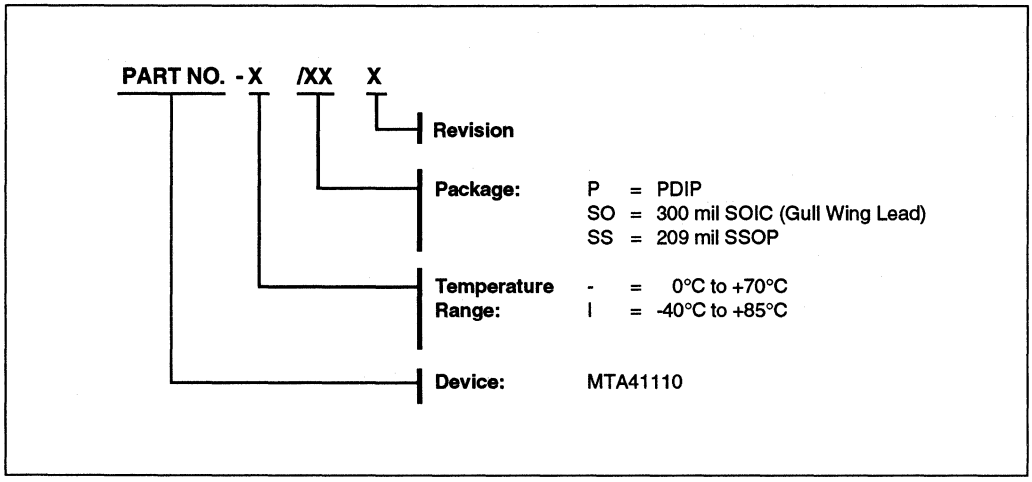
Legend:	MM...M	Microchip part number information
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line.

4

SALES AND SUPPORT

To order or to obtain information, e.g. on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



MTA41111

Velocity Scaling Mouse and Trackball Controller I.C.

FEATURES

- Single-chip two-button mouse or trackball controller that supports velocity scaling
- 10 KHz IBM® PS/2® interface
- IBM PS/2 mouse compliant
- Selectable Mouse or Trackball resolutions
- Strobed motion encoders for reduced system power consumption
- Motion sampling rate of 8700 Samples/second
- Proprietary anti-jitter algorithm simplifies motion encoder interface
- Available In:
  - 18-lead 300 mil PDIP
  - 18-lead 300 mil SOIC
  - 20-lead 209 mil SSOP

DESCRIPTION

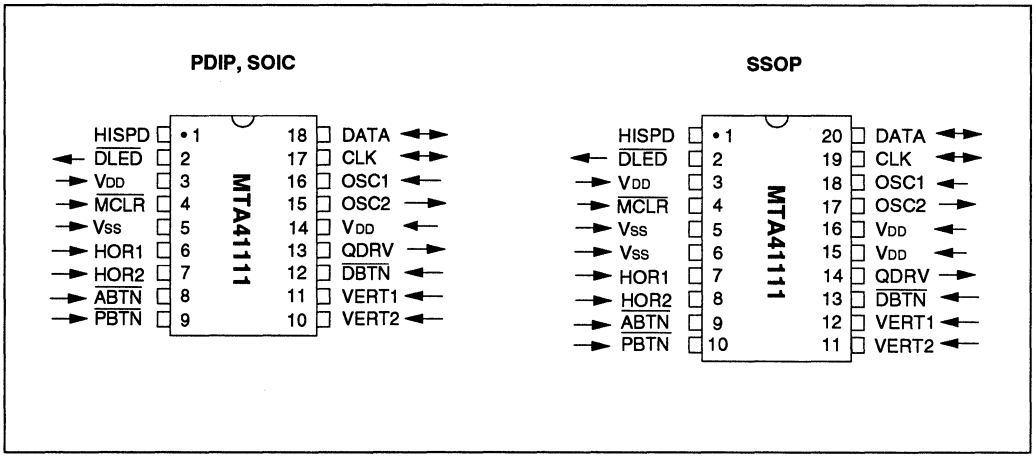
The MTA41111 is the heart of a simple, low-cost, mouse or trackball solution. It can be configured to operate as an IBM PS/2 compliant mouse or trackball controller. The mouse select and drag operation can be accomplished with a trackball by using the optional drag lock input and drag lock LED. This allows for one handed select and drag operation when using a trackball.

MTA41111

The MTA41111 is an 18-lead low-power CMOS integrated circuit. Combined with a few simple external components, a complete mouse or trackball system can be realized.

4

FIGURE A - PIN CONFIGURATIONS



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1.0 PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
HISPD	Input	Active high, velocity gain activated
QDRV	Output	Active high strobed encoder drive
HOR1	Input	Horizontal quadrature input #1
HOR2	Input	Horizontal quadrature input #2
$\overline{PBTN}$	Input	Primary mouse button. Active low , 0 = button depressed
$\overline{ABTN}$	Input	Alternate mouse button. Active low, 0 = button depressed
$\overline{DBTN}$	Input	Optional trackball drag lock button. Active low, 0 = button depressed. For mouse operation connect this pin to VDD
VERT1	Input	Vertical quadrature input #1
VERT2	Input	Vertical quadrature input #2
$\overline{DLED}$	Output	Optional trackball drag LED. For mouse operation this pin is a no connect and should be left unconnected
OSC1	Input	4 MHz crystal or ceramic resonator connection
OSC2	Output	4 MHz crystal or ceramic resonator connection
DATA	I/O	Bi-directional data port for PS/2
CLK	Input	PS/2 data clock input
$\overline{MCLR}$	Input	A "low" voltage on this pin causes a reset condition for the MTA41111 controller
VDD	Pwr	+5V
VSS	Pwr	Ground

2.0 OPERATION

Upon power-up, the MTA41111 mouse controller initiates an internal reset sequence. First, all internal registers and communication parameters are cleared. Next, the status registers are set to the default condition. Finally, if the MTA41111 receives a Resend command as the first command after power-up, it will transmit a AAh followed by a 00h in response. This notifies the host that the initialization is complete and that the controller is a standard mouse type. This is to ensure compatibility with some hosts that do not follow the normally recommended behavior of issuing a Reset command as the first command after power-up.

The MTA41111 always confirms reception of a command sent by the host by returning an acknowledge byte (FAh). If the host interrupts the transmission of the acknowledge byte, the MTA41111 discards the complete command. The MTA41111 is then ready to receive and acknowledge the next command. Two exceptions to the acknowledge after command received rule exist. The MTA41111 does not issue an acknowledge upon receipt of either the Set Wrap Mode (EEh) or Resend (FEh) commands.

The MTA41111 supports velocity scaling. When activated, it allows the cursor to travel faster based on the speed of the mouse or trackball movement.

2.1 PS/2 COMMANDS

Command Summary:

Command	Code, Data
Reset	FFh
Resend	FEh
Set Default	F6h
Disable Reporting	F5h
Enable Reporting	F4h
Set Report Rate	F3h , XXh
Read Device Type	F2h
Set Remote Mode	F0h
Set Wrap Mode	EEh
Reset Wrap Mode	ECh
Read Data	EBh
Set Stream Mode	EAh
Status Request	E9h
Set Resolution	E8h , XXh
Set Scaling	E7h
Reset Scaling	E6h

2.1.1 Reset Code: FFh

This command initiates a reset sequence in the MTA41111 mouse controller. First, all internal registers and communication parameters are cleared. Next, the status registers are set to the default condition. Finally, the MTA41111 transmits a AAh followed by a 00h, this informs the host that the initialization is complete and that the controller is a standard mouse type.

2.1.2 Resend Code: FEh

Anytime the MTA41111 controller receives an invalidly formatted command, it will transmit a Resend command to the host. The controller will ignore invalid commands and will continue to operate in its present mode. When any command other than a Resend is received by the controller it will clear its motion and displacement counters.

The host system may send a Resend command to the controller if an error is detected in a transmission from the controller. When the controller receives a Resend command, it will retransmit the last data packet transmitted. If the last packet transmitted was a Resend command, the packet prior to the last packet will be retransmitted.

2.1.3 Set Default Code: F6h

The Set Default command re-initializes all controller parameters to the power-up state. The controller initializes the following status registers.

Report rate:	100 reports per second
Scaling:	Linear
Mode:	Streaming
Resolution:	Physical Resolution / 2
Reporting:	Disabled

This command does not initiate any self-test diagnostics. The controller remains in the disabled state until another command is received from the host.

2.1.4 Disable Reporting Code: F5h

The Disable Reporting command prevents data transmission by the controller while it is in the Stream Mode. However, the controller will still respond to other commands. When reporting is disabled, Stream Mode must be disabled prior to the host sending a command that requires a response by the controller.

2.1.5 Enable Reporting Code: F4h

The Enable Reporting command allows the controller to transmit data when in Stream Mode. This command has no effect while the controller is in Remote Mode.

2.1.6 Set Report Rate Code: F3h , XXh

This command updates the report rate status register with the data contained in the second byte of the command. However, the physical report rate remains fixed at 40 times per second. This command only exists to ensure compatibility.

2.1.7 Read Device Type Code: F2h

The controller always transmits a 00h in response to receiving this command. This informs the host that a standard mouse is present.

2.1.8 Set Remote Mode Code: F0h

Remote Mode is entered when the controller receives this command. In Remote Mode, event packets are transmitted to the host only when a read data command is received by the controller.

2.1.9 Set Wrap Mode Code: EEh

Wrap Mode is entered when the controller receives this command. In Wrap Mode, the controller will echo all commands that are received back to the host. Note, the Reset and Reset Wrap commands will cancel Wrap Mode and neither of these commands will be echoed back to the host. Wrap Mode can be enabled in either Reporting Mode, Stream Mode or Remote Mode.

2.1.10 Reset Wrap Mode Code: ECh

This command cancels Wrap Mode. The controller remains in the current Reporting Mode. Note, if the controller enters Wrap Mode while in Stream Mode and then a Reset Wrap Mode command is received, the controller will reenter the Stream Mode with Wrap Mode disabled.

2.1.11 Read Data Code: EBh

The controller will transmit an event packet to the host after a read data command is received. This command can be issued in either the Remote or Stream Modes. The controller will transmit data even if there has not been any button changes or motion since the last report. The controller clears the motion counters after ever read data command.

2.1.12 Set Stream Mode Code: EAh

The controller will enter the Stream Mode upon receiving this command. In Stream Mode, event packets are transmitted to the host as they occur.

2.1.13 Status Request Code: E9h

A three byte status report packet will be transmitted in response to this command. These status bytes are defined as follows:

Byte 1:

Bit	Description
0	1 = Secondary Button Depressed
1	Reserved
2	1 = Primary Button Depressed
3	Reserved
4	1 = 2:1 Scaling
5	1 = Enabled
6	1 = Remote Mode
7	Reserved

Byte 2: Current Resolution

Byte 3: Current Sample Rate

2.1.14 Set Resolution Code: E8h , XXh

The controller provides four resolutions selected by the second byte of this command. The effective resolution is the physical device resolution divided by the divisor indicated below.

Second Byte	Description
0	divide by 8
1	divide by 4
2	divide by 2
3	divide by 1

2.1.15 Set Scaling Code: E7h

This command has no effect on resolution and only exists to ensure compatibility.

2.1.16 Reset Scaling Code: E6h

This command resets the scaling to 1:1 (input count equals reported count).

2.2 PS/2 Message Data Format

The following PS/2 compliant data format is used by the MTA41111 when transmitting data to the host and when receiving data from the host. The data format utilizes an 11 bit data frame that utilizes 8 bits for message data and 3 bits for control.

Data Frame Format :

Bit	Description
1	Start Bit (always 0)
2	Message Data Bit 0 , LSB
3	Message Data Bit 1
4	Message Data Bit 2
5	Message Data Bit 3
6	Message Data Bit 4
7	Message Data Bit 5
8	Message Data Bit 6
9	Message Data Bit 7 , MSB
10	Parity Bit (odd parity)
11	Stop bit (always 1)

The MTA41111 mouse controller transmits the following three byte data packet in response to a Read Data (EBh) command or when operating in Stream Mode with reporting enabled.

Status Message Data Byte 1:

Bit	Description
0	1 = Primary Button Depressed
1	1 = Secondary Button Depressed
2	Reserved
3	Reserved
4	X data sign, 1 = negative
5	Y data sign, 1 = negative
6	X data overflow, 1 = overflow
7	Y data overflow, 1 = overflow

Status Message Data Byte 2:

Delta X motion

Status Message Data Byte 3:

Delta Y motion

3.0 MOTION ENCODER INTERFACE

The MTA41111 is designed to interface to both optical encoders that utilize LED and photo transistor pairs with a chopper wheel or mechanical encoders that utilize a commutator with wiper contacts.

Power consumption is reduced by strobing the motion encoder power each time the encoders are sampled. The MTA41111 will drive the QDRV output high 8 µS (with 4 MHz input clock) prior to sampling the HOR and VERT inputs to give the encoders time to stabilize. The QDRV output will be driven back low 2 µs after the sample is taken. If power consumption is not a concern, then the QDRV output can be left unconnected and encoders can be powered directly from a constant supply (e.g. +5V power).

An anti-jitter algorithm is employed to eliminate false motion counting when the mouse or trackball is not moving. This is especially useful in designs employing optical encoders since the output of an optical detector is an analog signal. The anti-jitter algorithm eliminates false counting when a voltage that is not a well defined logic low or logic high is applied to either the HOR or VERT inputs.

The HOR and VERT inputs detect positive and negative delta motion. Motion direction is defined in the following state table along with Figures 3.1 and 3.2.

Positive Motion:

Hor1,Hor2 / Vert1,Vert2	Description
0,0	
0,1	
1,1	Positive Direction Sequence
1,0	
0,0	
etc.	

Negative Motion:

Hor1,Hor2 / Vert1,Vert2	Description
0,0	
1,0	
1,1	Negative Direction Sequence
0,1	
0,0	
etc.	

The HOR and VERT inputs are sampled at ~8700 samples per second with a 4 MHz input clock. The sample rate will decrease slightly when communication traffic to or from the host is occurring. The sample rate is directly proportional to the clock frequency on the OSC1 and OSC2 pins.

4

FIGURE 3.1 - POSITIVE MOTION SEQUENCE

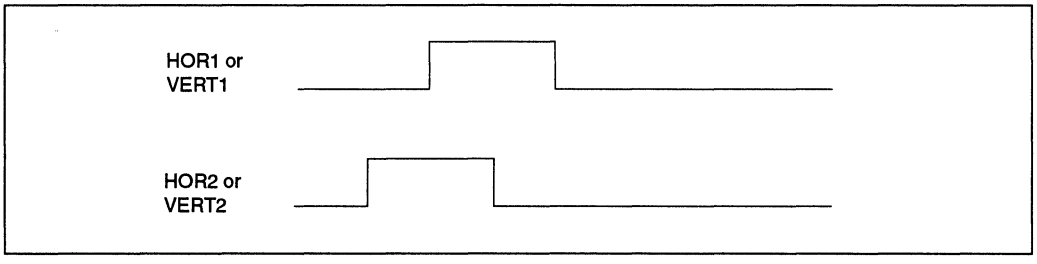
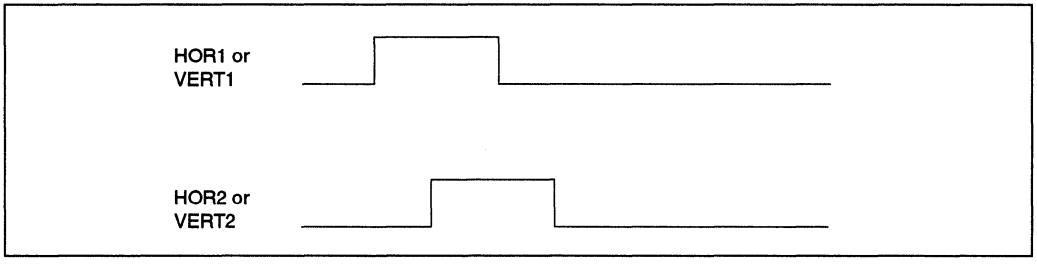


FIGURE 3.2 - NEGATIVE MOTION SEQUENCE



4.0 PUSH-BUTTON INPUTS

The MTA41111 push-button inputs are defined to be active when the input pin is in the low state. The appropriate message data bit will be set equal to one when a low is sampled at a switch input. When a switch input is sampled in the high state, the appropriate message data bit will be set equal to zero.

5.0 TRACKBALL OPTION

The MTA41111 can also function as a trackball controller. A trackball drag lock switch can be connected to the $\overline{DBTN}$ input and an LED indicator connected to the $\overline{DLED}$ output to aid in one-handed trackball operation.

When using a mouse, a select and drag operation is performed by clicking on an object and holding the primary mouse button down. Moving the mouse then drags the object to the desired location. When the primary button is released the object is placed at the desired location. However, when the same select and drag operation is performed using a trackball, it may be difficult to hold the button depressed and guide the trackball with the same hand.

The MTA41111's "drag lock" feature allows this function to be accomplished with one hand. The drag lock is set to the "locked" state by momentarily applying a low to the $\overline{DBTN}$ input. This "locked" state is equivalent to depressing and holding the primary mouse button. The user then guides the object to the desired location without having to hold a button depressed and simultaneously guide the trackball. The object is placed and the "lock" is released when a low (e.g. button depressed) is momentarily applied to any button input.

The $\overline{DLED}$ output is latched in the low state (0V) when the $\overline{DBTN}$ input is sampled low (refer to Figure 5.1). The $\overline{DLED}$ output will remain low ("locked") until the $\overline{DBTN}$ input is sampled high and then sampled low again. Exiting the locked state also occurs if the $\overline{PBTN}$ input or $\overline{SBTN}$ input is sampled low when the $\overline{DLED}$ output is low. When the $\overline{DLED}$ output is in low "locked" state, the Primary Button depressed bit in the status message is set high.

5.1 Velocity Scaling

When HISPD is enabled, velocity scaling is activated. The velocity scaling is defined in Table 5.1 and illustrated in Figure 5.2.

TABLE 5.1 - BALLISTIC GAIN

Physical Counts (per sample period)	Output Counts
0	0
1	1
2	2
3	4
4	7
5	10
6	13
7	16
8	19
9	22
10	26
11	30
12	34
13	38
14	42
15	46
16	50
17	54
18	58
19	62
20	67
21	72
22	77
23	82
24	87
25	92
26	97
27	103
28	109
29	115
30	121
31	127

FIGURE 5.1 - TRACKBALL DRAG LOCK OPERATION

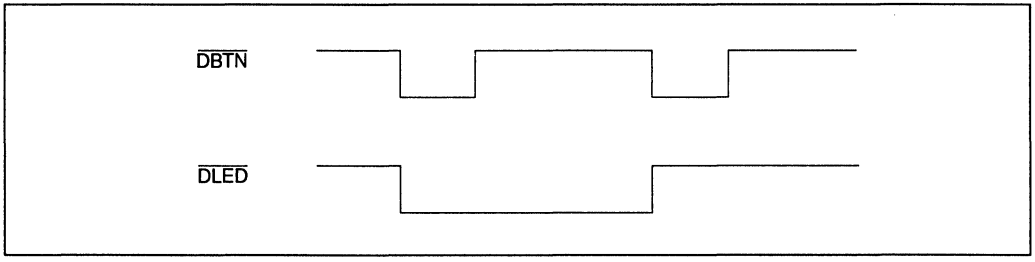
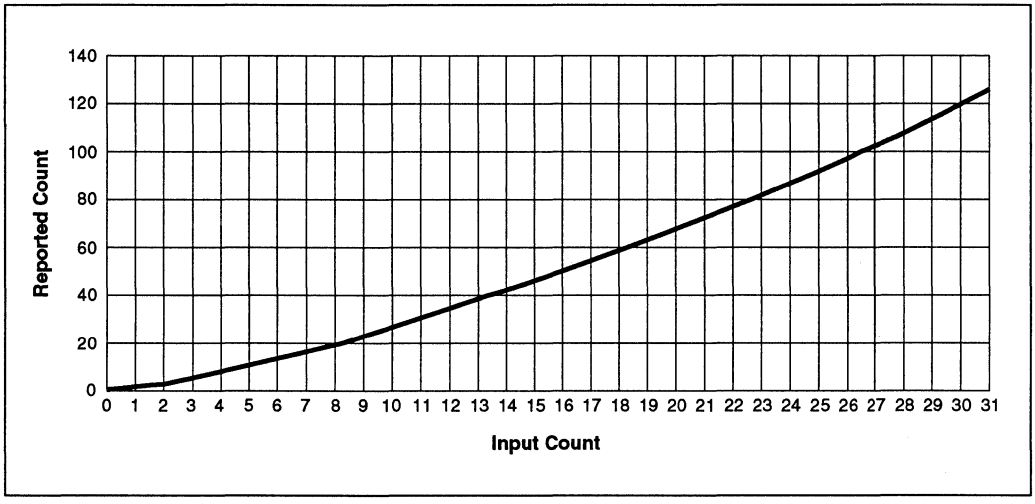


FIGURE 5.2 - MTA41111 BALLISTIC GAIN



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6.0 ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS †

Ambient temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to Vss (except VDD and $\overline{MCLR}$)	-0.6V to (VDD +0.6V)
Voltage on $\overline{MCLR}$ pin with respect to Vss	0V to +14.0V
Voltage on VDD with respect to Vss	0V to +9.5V
Total power dissipation (Note 2)	800 mW
Maximum current out of Vss pin	150 mA
Maximum current into VDD pin	50 mA
Maximum current into input pin	±500 µA
Maximum output current sinked by any I/O or output pin	25 mA
Maximum output current sourced by any I/O or output pin	20 mA

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes:

1. Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to this pin, rather than connecting this pin directly to Vss.
2. Total power dissipation should not exceed 800 mW for the package. The total power dissipation is calculated as follows:

   $P_{DIS} = V_{DD} \times (I_{DD} - \sum I_{OH}) + \sum\{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

6.2 DC CHARACTERISTICS MTA41111 (COMMERCIAL)

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated).
Operating Temperature 0°C < TA < 70°C for commercial.
Operating voltage V_{DD} = 3.0V to 5.5V unless otherwise stated.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	3.0		6.25	V	F_{OSC} = DC to 4 MHz
V_{DD} start voltage to guarantee power-on reset	V_{POR}		V_{SS}		V	
V_{DD} rise rate to guarantee power-on reset	SV_{DD}	0.05*			V/mS	
Supply Current	I_{DD}		1.8	3.3	mA	F_{OSC} = 4 MHz , V_{DD} = 5.5V
Input Low Voltage						
$\overline{MCLR}$ (Schmitt trigger)	V_{ILMC}			.15 V_{DD}	V	
OSC1 (Schmitt trigger)	V_{ILOSC}			.3 V_{DD}	V	
All other Inputs	V_{IL}			.2 V_{DD}	V	
Input High Voltage						
$\overline{MCLR}$ (Schmitt trigger)	V_{IHMC}	.85 V_{DD}		V_{DD}	V	
OSC1 (Schmitt trigger)	V_{IHOSC}	.7 V_{DD}		V_{DD}	V	
All other Inputs	V_{IH}	.45 V_{DD}		V_{DD}	V	
		2V		V_{DD}		4.0V < V_{DD} ≤ 5.5V
Input Leakage Current						
$\overline{MCLR}$	I_{ILMCL}	-5			µA	V_{PIN} = V_{DD} + 0.25V
$\overline{MCLR}$	I_{ILMCH}		0.5	+5	µA	V_{PIN} = V_{DD}
OSC1 (Schmitt trigger)	I_{ILMCH}		0.5	+3	µA	V_{DD} ≤ V_{PIN} ≤ V_{DD}
All other Inputs	I_{IL}	-1	0.5	+1	µA	V_{DD} ≤ V_{PIN} ≤ V_{DD}
Output Low Voltage						
OSC2	V_{OL}			0.6V	V	I_{OL} = 1.6 mA, V_{DD} = 4.5V
All other Outputs	V_{OL}			0.6V	V	I_{OL} = 8.7 mA, V_{DD} = 4.5V
Output High Voltage						
OSC2	V_{OH}	V_{DD} - .7			V	I_{OH} = -1.0 mA, V_{DD} = 4.5V
All Outputs	V_{OH}	V_{DD} - .7			V	I_{OH} = -5.4 mA, V_{DD} = 4.5V

*These parameters are based on characterization and are not tested.

FIGURE 6.2.1 - INPUT THRESHOLD VOLTAGE (V_{TH}) OF ALL INPUT AND I/O PINS EXCEPT $\overline{MCLR}$ AND OSC1

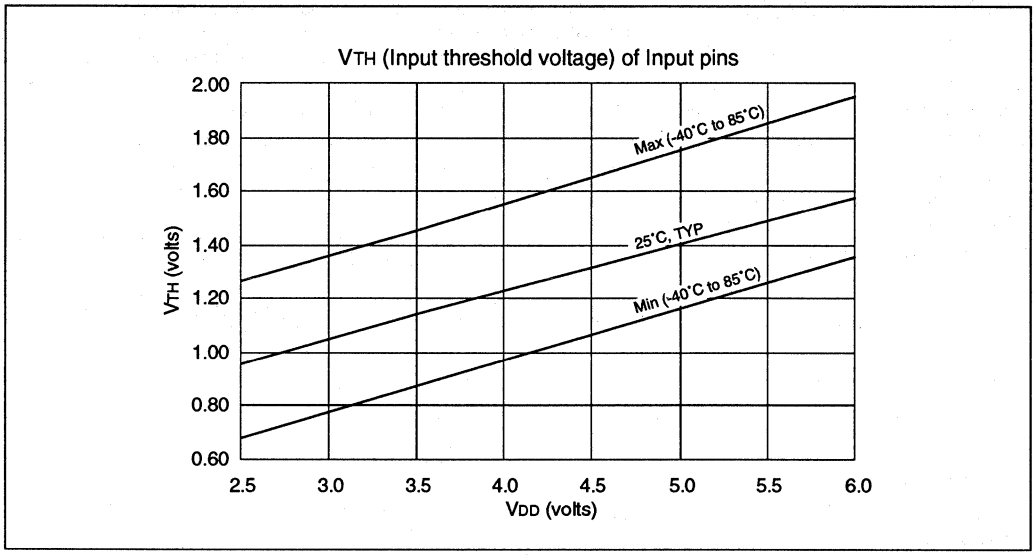
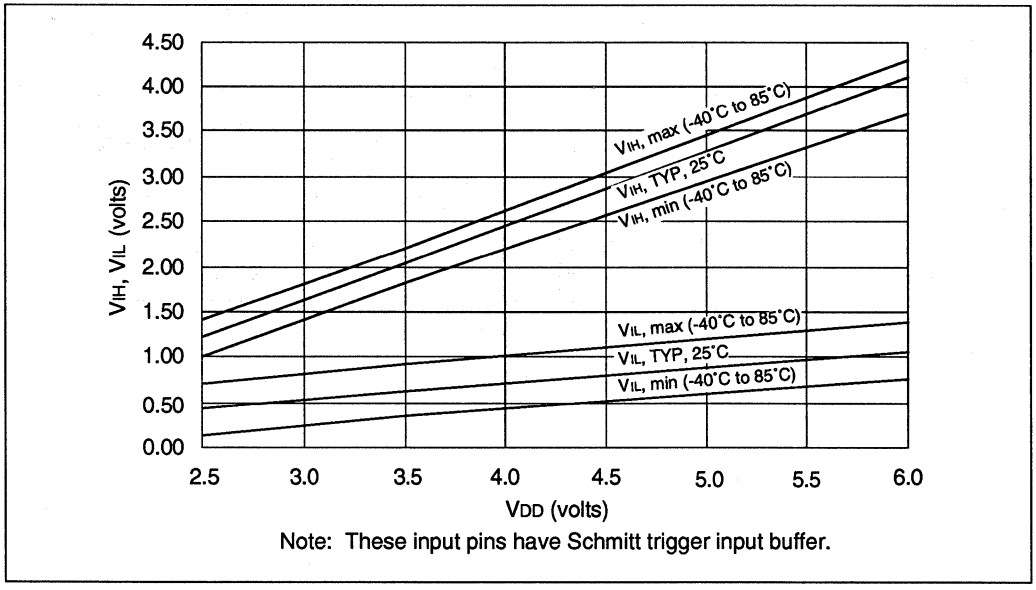


FIGURE 6.2.2 - V_{IH}, V_{IL} OF $\overline{MCLR}$ vs V_{DD}



Note: These input pins have Schmitt trigger input buffer.

FIGURE 6.2.3 - INPUT THRESHOLD VOLTAGE (V_{TH}) OF OSC1 INPUT

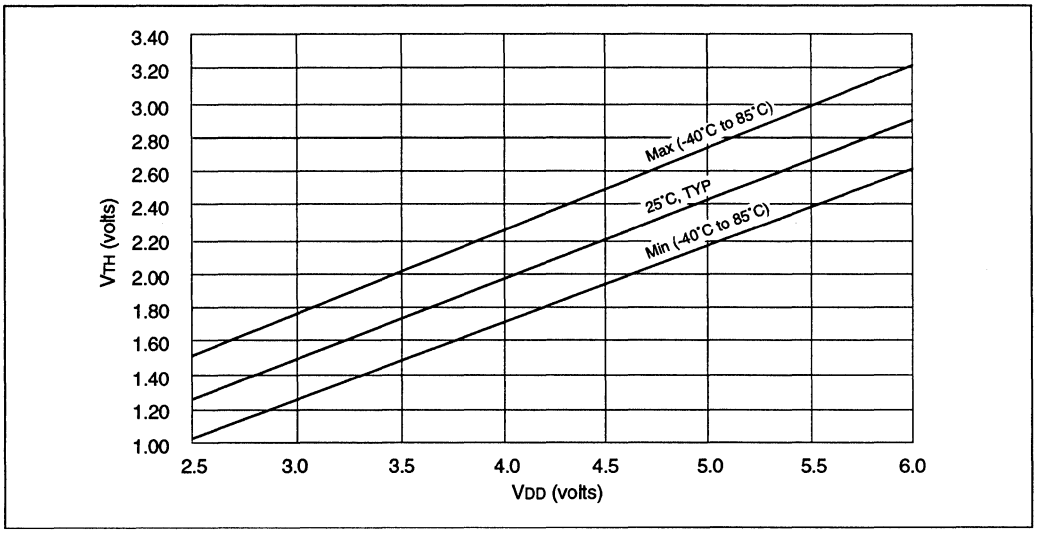


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FIGURE 6.2.4 - I_{OH} vs V_{OH}, V_{DD} = 3V

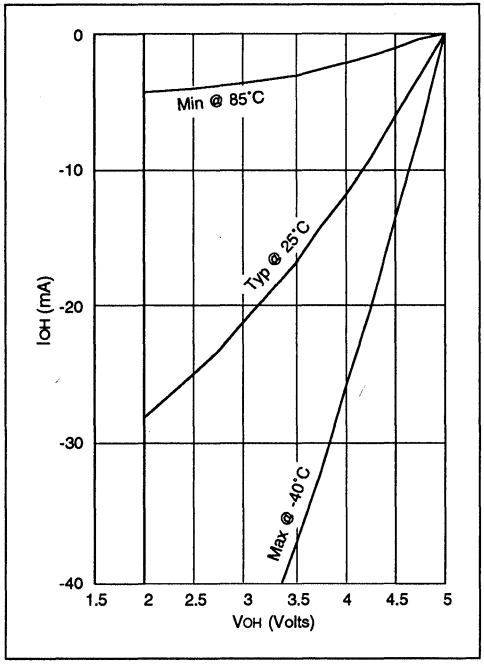


FIGURE 6.2.5 - I_{OH} vs V_{OH}, V_{DD} = 5V

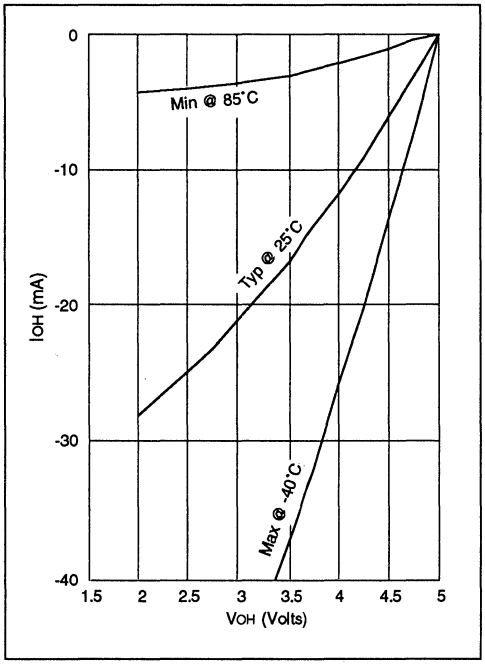


FIGURE 6.2.6 - I_{OL} vs V_{OL}, V_{DD} = 3V

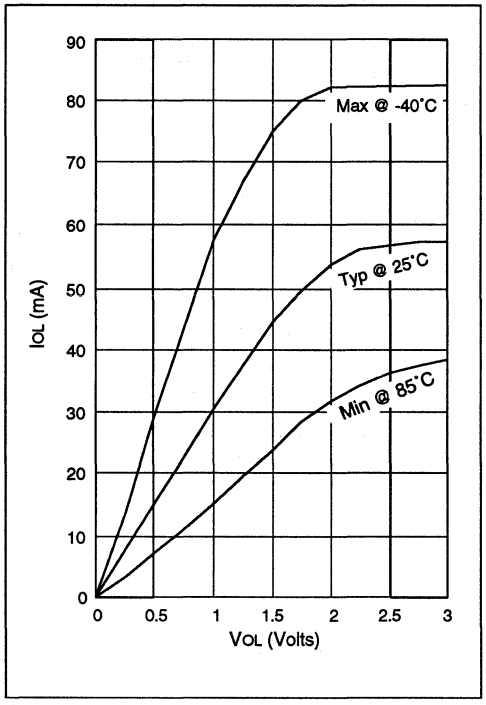
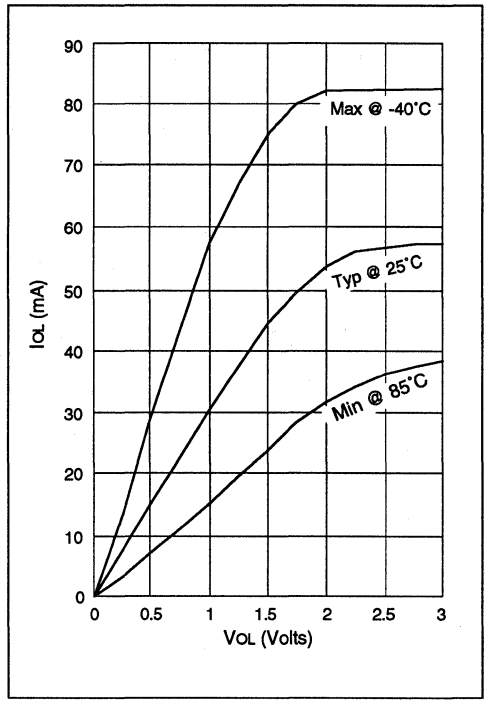


FIGURE 6.2.7 - I_{OL} vs V_{OL}, V_{DD} = 5V



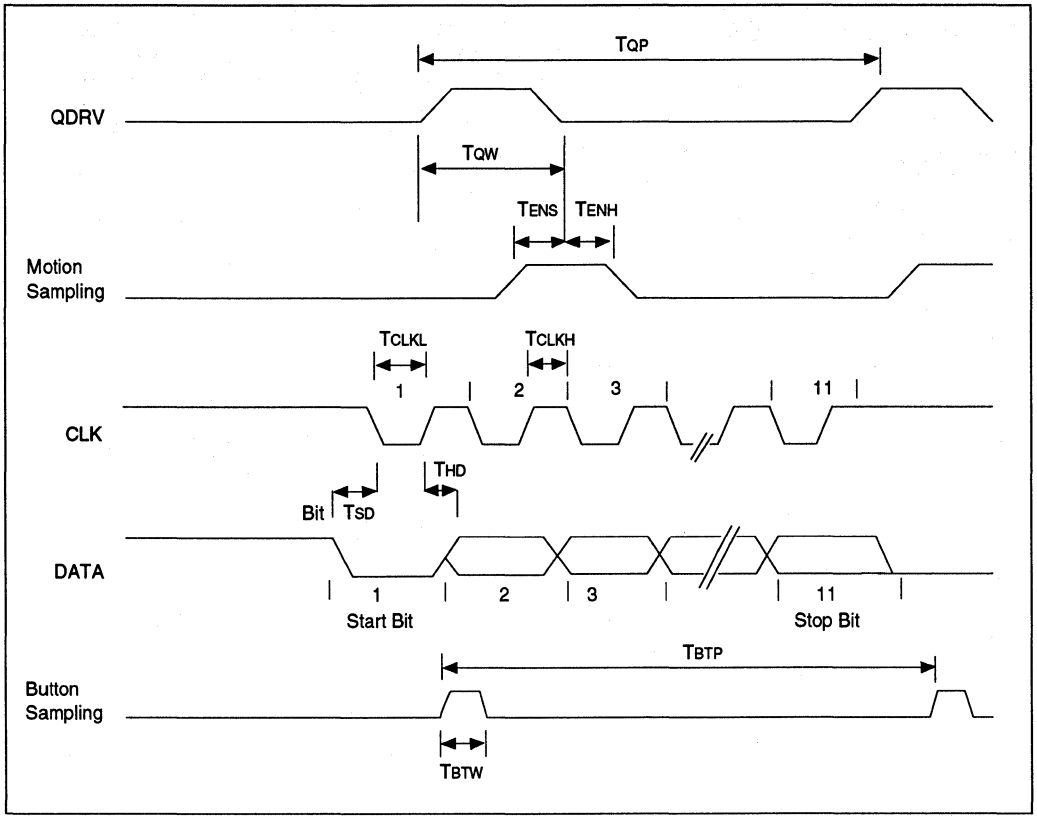
6.3 AC CHARACTERISTICS MTA41111 (COMMERCIAL)

AC CHARACTERISTICS						Standard Operating Conditions (unless otherwise stated). Operating Temperature 0°C < TA < 70°C for commercial. Operating Voltage VDD = 3.0V to 5.5V unless otherwise stated. Oscillator Frequency = 4 MHz.
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Oscillator Frequency	FOSC	DC		4	MHz	
Motion Encoder Timing						
QDRV						
Pulse Period	TQP (Note 2)		115		µS	
Pulse Width	TQW	8	10	12	µS	
HOR1,HOR2,VERT1,VERT2						
Input Sample Setup Time	TENS	3			µS	Before QDRV falling edge.
Input Sample Hold	TENH			0	nS	After QDRV falling edge.
I/O Timing						
CLK High time	TCLKH	30		50	µS	
CLK Low time	TCLKL	30		50	µS	
DATA setup time to CLK falling	TSD	5		25	µS	
DATA hold time to CLK rising	THD	5		45		
Button Input Timing						
$\overline{PBTN}$, $\overline{SBTN}$, $\overline{DBTN}$, HISPD						
Input Sample Period	TBTP (Note 2)			50	ms	
Input Sample Window width	TBTW			280	ns	
RESET Timing						
$\overline{MCLR}$ pulse width (low)	TMCL	100			ns	
Oscillator Start-up Timer Period	TOST (Note 1)	9	18	30	ms	VDD = 5.0V

Notes:

1. These parameters are based on characterization and are not tested.
2. Sampling can be suspended if device is receiving data from host or transmission to host is inhibited by host (CLK held low)

FIGURE 6.3.1 - TIMING DIAGRAMS



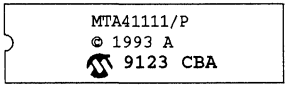
7.0 PACKAGING DIAGRAMS AND DIMENSIONS

See Section 11 of the Data Book.

8.0 PACKAGE MARKING INFORMATION

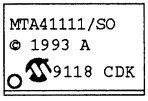
18L PDIP

Example

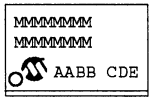


18L SOIC

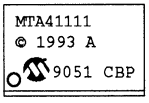
Example



20L SSOP



Example

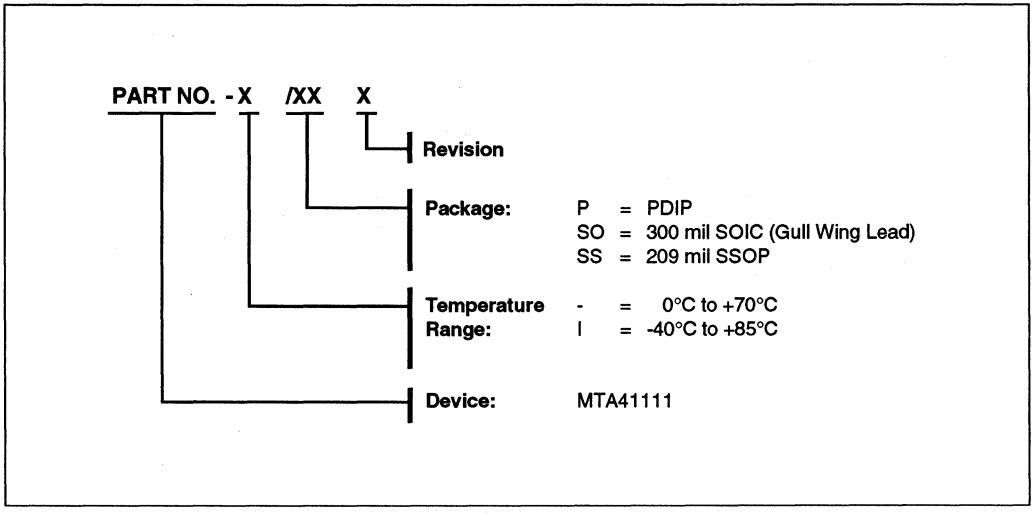


Legend:	MM...M	Microchip part number information
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line.

SALES AND SUPPORT

To order or to obtain information, e.g. on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



MICROCHIP

MTA41120

ADB™ Mouse/Trackball Controller I.C.*

FEATURES

- Single-chip two-button mouse or trackball controller
- Built in collision detection so that multiple devices may be connected to the host interface without conflict
- Strobed motion encoders for reduced system power consumption
- Proprietary anti-jitter algorithm simplifies motion encoder interface
- Motion sampling rate of 6000 samples/second
- Available In:
  - 18-lead 300 mil PDIP
  - 18-lead 300 mil SOIC
  - 20-lead 209 mil SSOP

DESCRIPTION

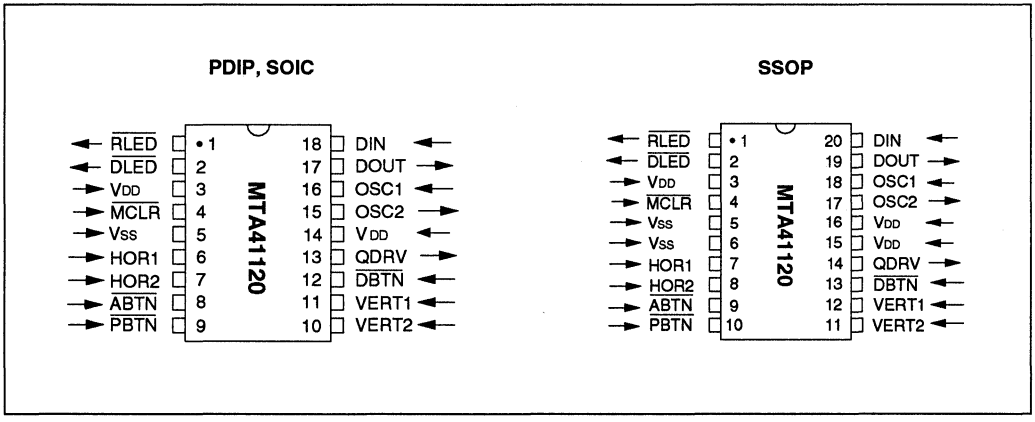
The MTA41120 is the heart of a simple, low-cost, mouse or trackball solution. It can be configured to operate as either an Apple Macintosh compatible mouse or trackball controller. The mouse select and drag operation can be performed with a trackball by using the optional drag lock input and drag lock LED. This allows for one handed select and drag operation when using a trackball. The MTA41120 does not require special host system device drivers.

MTA41120

The MTA41120 is an 18-lead low-power CMOS integrated circuit. Combined with a few simple external components, a complete mouse or trackball system can be realized.

4

FIGURE A - PIN CONFIGURATIONS



*Apple Macintosh Compatible Host Interface

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Apple Desktop Bus (ADB) is a trademark of Apple Corp.

1.0 PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
QDRV	Output	Active high strobed encoder drive
HOR1	Input	Horizontal quadrature Input #1
HOR2	Input	Horizontal quadrature Input #2
$\overline{\text{PBTN}}$	Input	Primary mouse button. Active low , 0 = button depressed
$\overline{\text{ABTN}}$	Input	Alternate mouse button. Active low, 0 = button depressed
$\overline{\text{DBTN}}$	Input	Optional trackball drag lock button. Active low, 0 = button depressed. For mouse operation connect this pin to VDD
VERT1	Input	Vertical quadrature input #1
VERT2	Input	Vertical quadrature input #2
$\overline{\text{RLED}}$	Output	Optional high resolution LED. Indicates mouse or trackball is in high resolution mode. If high resolution LED is not required then this pin is a no connect and should be left unconnected
$\overline{\text{DLED}}$	Output	Optional trackball drag LED. For mouse operation this pin is a no connect and should be left unconnected
OSC1	Input	4 MHz crystal or ceramic resonator connection
OSC2	Output	4 MHz crystal or ceramic resonator connection
DIN	Input	Input data port for host communication
DOUT	OC-Output	Open Collector output for data communication with host
$\overline{\text{MCLR}}$	Input	A "low" voltage on this pin causes a reset condition for the MTA41120 controller
VDD	Pwr	+5V
VSS	Pwr	Ground

2.0 OVERVIEW

The MTA41120 mouse and trackball controller is compliant with all specifications that apply to the Host Interface. Its collision detection and recovery algorithms allow it to be used in systems where one or more devices may be connected to the host interface.

The drag lock button input allows the MTA41120 to be used as either a trackball controller or a mouse controller.

The MTA41120 supports two LED indicators that indicate operation in high resolution mode and when a drag lock operation is occurring. High Resolution mode is entered in response to a command from a host and is indicated by the $\overline{\text{RLED}}$ pin being driven low.

3.0 MOTION ENCODER INTERFACE

The MTA41120 is designed to interface to both optical encoders that utilized LED and photo transistor pairs with a chopper wheel or mechanical encoders utilizing a commutator with wiper contacts.

The HOR and VERT inputs are sampled at ~6000 samples per second with a 4 MHz input clock. The sample rate may decrease slightly when communication traffic to or from the host is occurring. The sample rate is directly proportional to the clock frequency on the OSC1 and OSC2 pins.

Power consumption is reduced by strobing the motion encoder power each time the encoders are sampled. The MTA41120 will drive the QDRV output high 10 uS (with 4 MHz input clock) prior to sampling the HOR and VERT inputs to give the encoders time to stabilize. The QDRV output will be driven back low 2 us after the sample is taken. If power consumption is not a concern then the QDRV output can be left unconnected and encoders can be powered directly from a constant supply (e.g. +5V power).

An anti-jitter algorithm is employed to eliminate false motion counting when the mouse or trackball is not moving. This is especially useful in designs employing optical encoders since the output of an optical detector is an analog signal. The anti-jitter algorithm eliminates false counting when a voltage that is not a well defined logic low or logic high is applied to either the HOR or VERT inputs.

The HOR and VERT inputs detect positive and negative delta motion. Motion direction is defined in the following state table and is illustrated in Figures 3.1 and 3.2.

Positive Motion:

Hor1, Hor2 / Vert1, Vert2	Description
0,0	
0,1	
1,1	Positive Direction Sequence
1,0	
0,0	
etc.	

Negative Motion:

Hor1, Hor2 / Vert1, Vert2	Description
0,0	
1,0	
1,1	Negative Direction Sequence
0,1	
0,0	
etc.	

4

FIGURE 3.1 - POSITIVE MOTION SEQUENCE

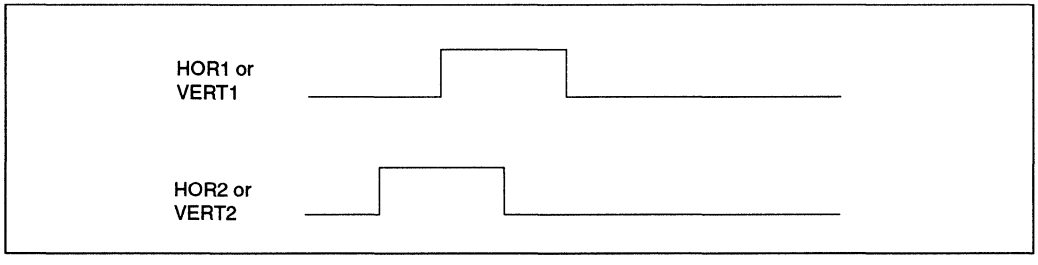
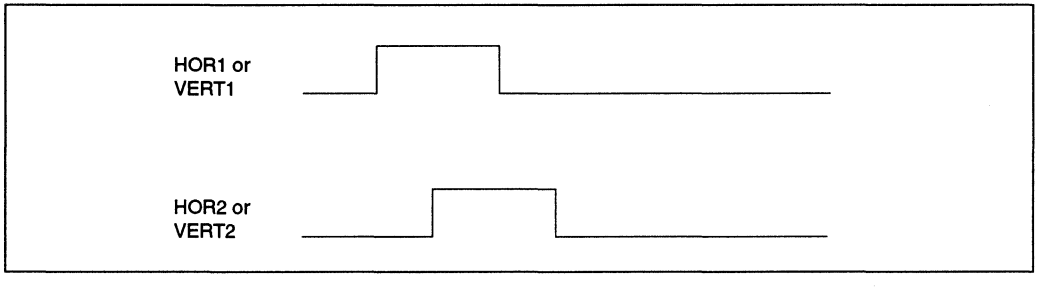


FIGURE 3.2 - NEGATIVE MOTION SEQUENCE



4.0 PUSH-BUTTON INPUTS

The MTA41120 push-button inputs are defined to be active when the input pin is in the low state. The appropriate message data bit will be set equal to one when a low is sampled at a switch input. When a switch input is sampled in the high state the appropriate message data bit will be set equal to zero. The push-button inputs are internally debounced to eliminate "false" button status reporting.

5.0 TRACKBALL OPTION

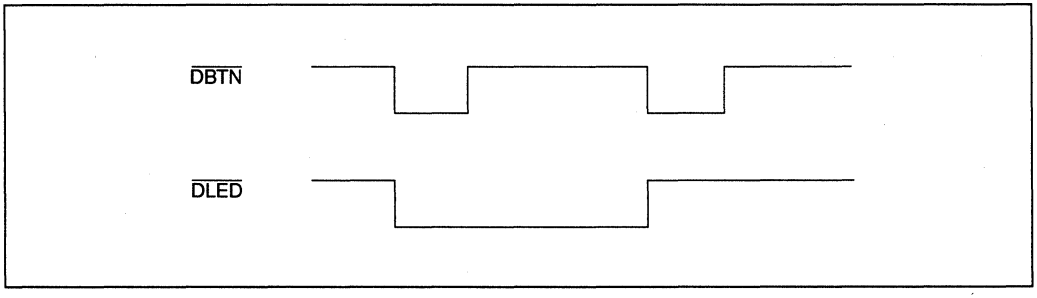
The MTA41120 can also function as a trackball controller. A trackball drag lock switch can be connected to the $\overline{\text{DBTN}}$ input and an LED indicator connected to the $\overline{\text{DLED}}$ output to aid in one-handed trackball operation.

When using a mouse a select and drag operation is performed by clicking on an object and holding the primary mouse button down. Moving the mouse then drags the object to the desired location. When the primary button is released the object is placed at the desired location. However, when the same select and drag operation is performed using a trackball, it may be difficult to hold the button depressed and guide the trackball with the same hand.

The MTA41120's "drag lock" feature allows this function to be accomplished with one hand. The drag lock is set to the "locked" state by momentarily applying a low to the $\overline{\text{DBTN}}$ input. This "locked" state is equivalent to depressing and holding the primary mouse button. The user then guides the object to the desired location without having to hold a button depressed and simultaneously guide the trackball. The object is placed and the "lock" is released when a low (e.g. button depressed) is momentarily applied to any button input.

The $\overline{\text{DLED}}$ output is latched in the low state (0V) when the $\overline{\text{DBTN}}$ input is sampled low (refer to Figure 5.1). The $\overline{\text{DLED}}$ output will remain low ("locked") until the $\overline{\text{DBTN}}$ input is sampled high and then sampled low again. Exiting the locked state also occurs if the $\overline{\text{PBTN}}$ input or $\overline{\text{SBTN}}$ input is sampled low when the $\overline{\text{DLED}}$ output is low.

FIGURE 5.1 - TRACKBALL DRAG LOCK OPERATION



6.0 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings †

Ambient temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to Vss (except VDD and $\overline{MCLR}$)	-0.6V to (VDD +0.6V)
Voltage on $\overline{MCLR}$ pin with respect to Vss	0V to +14.0V
Voltage on VDD with respect to Vss.	0V to +9.5V
Total power dissipation (Note 2)	800 mW
Maximum current out of Vss pin	150 mA
Maximum current into VDD pin	50 mA
Maximum current into input pin	±500 µA
Maximum output current sinked by any I/O or output pin	25 mA
Maximum output current sourced by any I/O or output pin	20 mA

Notes:

1. Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to this pin, rather than connecting this pin directly to Vss.
2. Total power dissipation should not exceed 800 mW for the package. The total power dissipation is calculated as follows:

   $Pdis = V_{DD} \times (I_{DD} - \Sigma Ioh) + \Sigma\{(V_{DD} - Voh) \times Ioh\} + \Sigma(Vol \times Iol)$

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

6.2 DC CHARACTERISTICS MTA41120 (COMMERCIAL)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated). Operating Temperature 0°C < TA < 70°C for commercial. Operating voltage VDD = 3.0V to 5.5V unless otherwise stated.				
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply Voltage	VDD	3.0		6.25	V	FOSC = DC to 4 MHz
VDD start voltage to guarantee power-on reset	VPOR		VSS		V	
VDD rise rate to guarantee power-on reset	SVDD	0.05*			V/mS	
Supply Current	IDD		1.8	3.3	mA	FOSC = 4 MHz , VDD = 5.5V
Input Low Voltage						
$\overline{\text{MCLR}}$ (Schmitt trigger)	VILMC			.15 VDD	V	
OSC1 (Schmitt trigger)	VILOSC			.3 VDD	V	
All other Inputs	VIL			.2 VDD	V	
Input High Voltage						
$\overline{\text{MCLR}}$ (Schmitt trigger)	VIHMC	.85 VDD		VDD	V	
OSC1 (Schmitt trigger)	VIHOSC	.7 VDD		VDD	V	
All other Inputs	VIH	2.0		VDD	V	4.45V ≤ VSS ≤ 5.5V
		.45 VDD		VDD		VDD < 4.45V
		.36 VDD		VDD		VDD > 5.5V
Input Leakage Current						
$\overline{\text{MCLR}}$	IILMCL	-5			µA	VPIN = Vss + 0.25V
$\overline{\text{MCLR}}$	IILMCH		0.5	+5	µA	VPIN = VDD
OSC1 (Schmitt trigger)	IILMCH	-3	0.5	+3	µA	Vss ≤ VPIN ≤ VDD
All other Inputs	IIL	-1	0.5	+1	µA	Vss ≤ VPIN ≤ VDD
Output Low Voltage						
OSC2	VOL			0.6V	V	IOL = 1.6 mA, VDD = 4.5V
All other Outputs	VOL			0.6V	V	IOL = 8.7 mA, VDD = 4.5V
Output High Voltage						
OSC2	VOH	VDD - .7			V	IOH =-1.0 mA, VDD = 4.5V
All other Outputs	VOH	VDD - .7			V	IOH =-5.4 mA, VDD = 4.5V

*These parameters are based on characterization and are not tested.

FIGURE 6.2.1 - INPUT THRESHOLD VOLTAGE (VTH) OF ALL INPUT AND I/O PINS EXCEPT MCLR AND OSC1

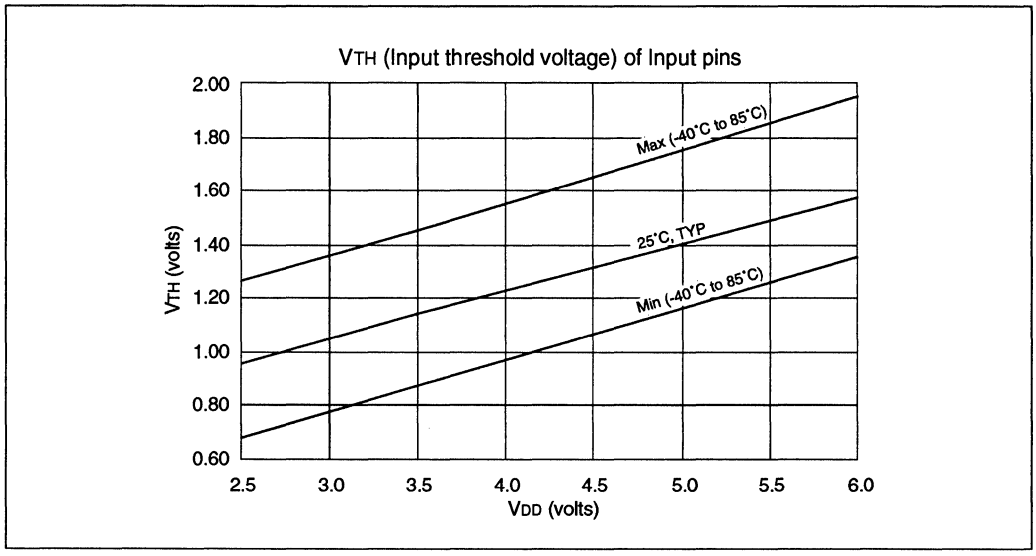
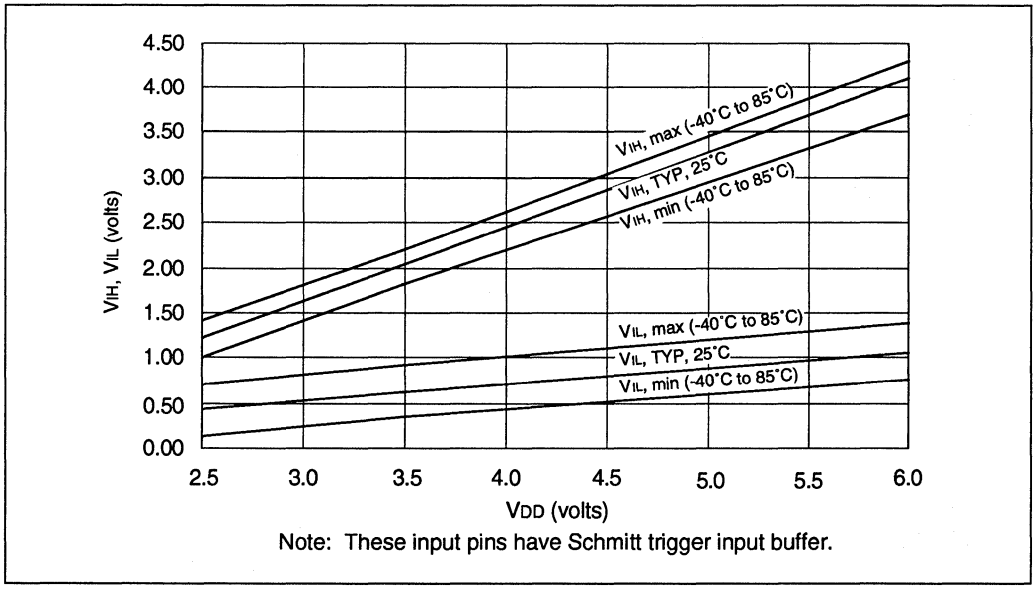


FIGURE 6.2.2 - VIH, VIL OF $\overline{\text{MCLR}}$ vs VDD



Note: These input pins have Schmitt trigger input buffer.

FIGURE 6.2.3 - INPUT THRESHOLD VOLTAGE (V_{TH}) OF OSC1 INPUT

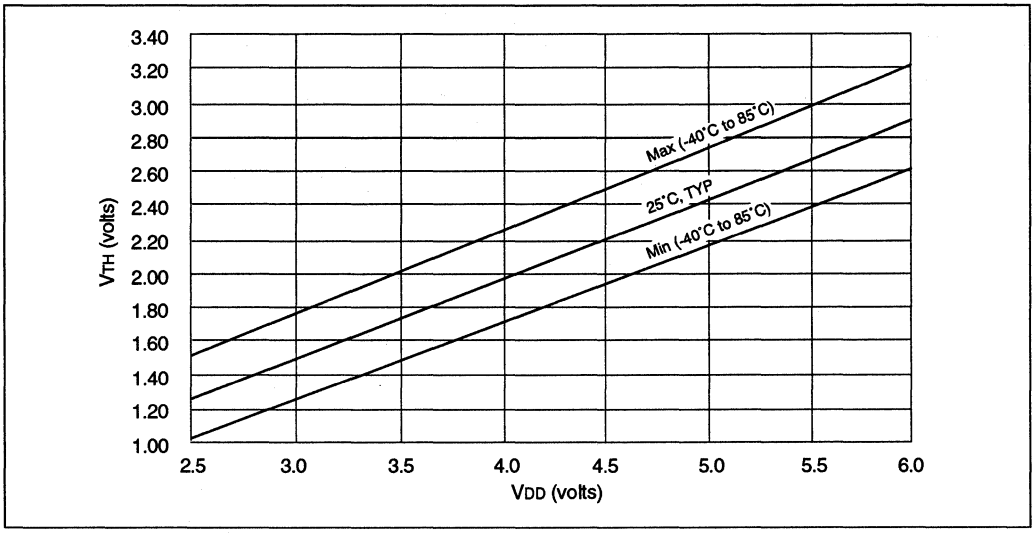


FIGURE 6.2.4 - I_{OH} vs V_{OH}, V_{DD} = 3V

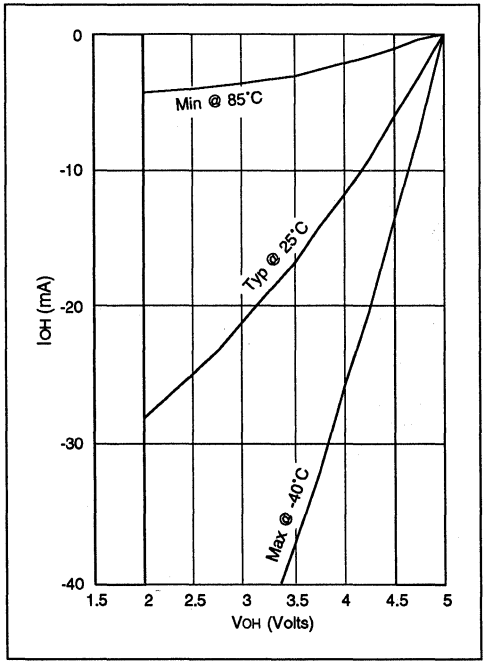


FIGURE 6.2.5 - I_{OH} vs V_{OH}, V_{DD} = 5V

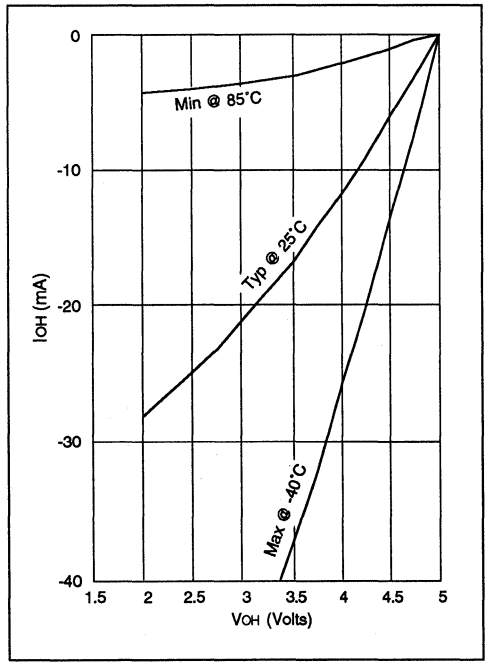


FIGURE 6.2.6 - IOL vs VOL, VDD = 3V

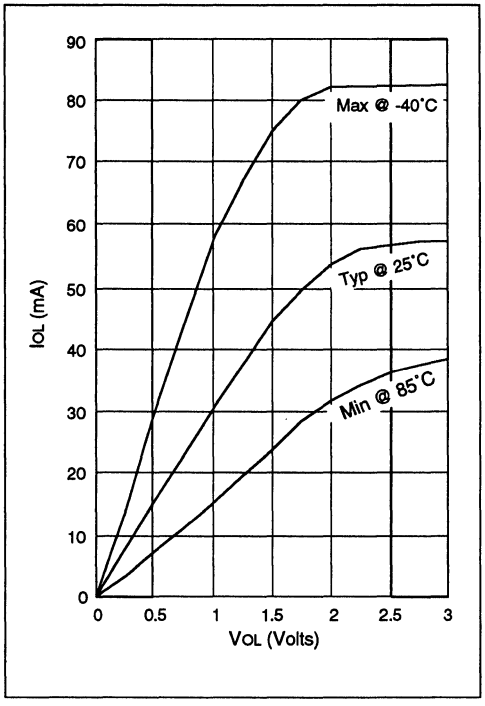
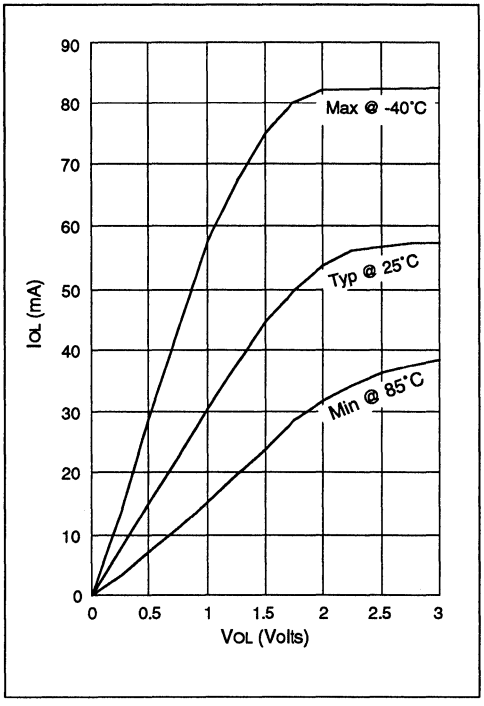


FIGURE 6.2.7 - IOL vs VOL, VDD = 5V



4

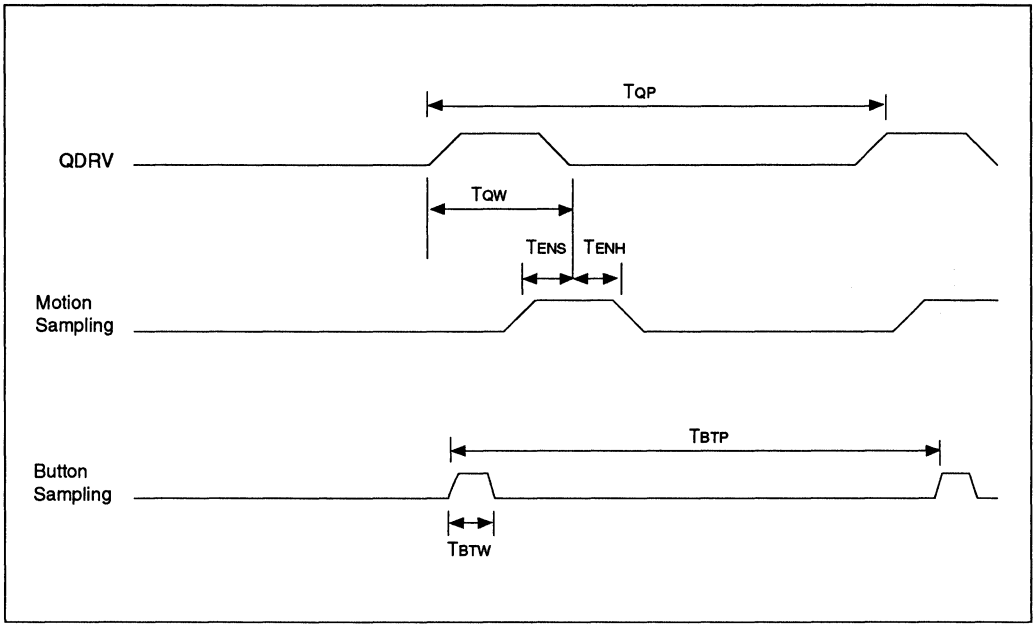
6.3 AC CHARACTERISTICS MTA41120 (COMMERCIAL)

AC CHARACTERISTICS						Standard Operating Conditions (unless otherwise stated). Operating Temperature 0°C < TA < 70°C for commercial. Operating Voltage VDD = 3.0V to 5.5V unless otherwise stated. Oscillator Frequency = 4 MHz.
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Oscillator Frequency	FOSC	DC		4	MHz	
Motion Encoder Timing						
QDRV						
Pulse Period	TQP (Note 2)		166		µS	
Pulse Width	TQW	11	12	13	µS	
HOR1,HOR2,VERT1,VERT2						
Input Sample Setup Time	TENS	2			µS	Before QDRV falling edge.
Input Sample Hold	TENH			0	nS	After QDRV falling edge.
Button Input Timing						
$\overline{PBTN}$, $\overline{SBTN}$, $\overline{DBTN}$						
Input Sample Period	TBP (Note 2)			10	ms	
Input Sample Window width	TBTU			280	ns	
RESET Timing						
$\overline{MCLR}$ Pulse Width (low)	TMCL	100			ns	
Oscillator Start-up Timer Period	TOST (Note 1)	9	18	30	ms	VDD = 5.0V

Notes:

1. These parameters are based on characterization and are not tested.
2. Sampling period can increase if device is receiving data from host or when transmitting to host.

FIGURE 6.3.1 - TIMING DIAGRAMS



7.0 APPLICATION EXAMPLE

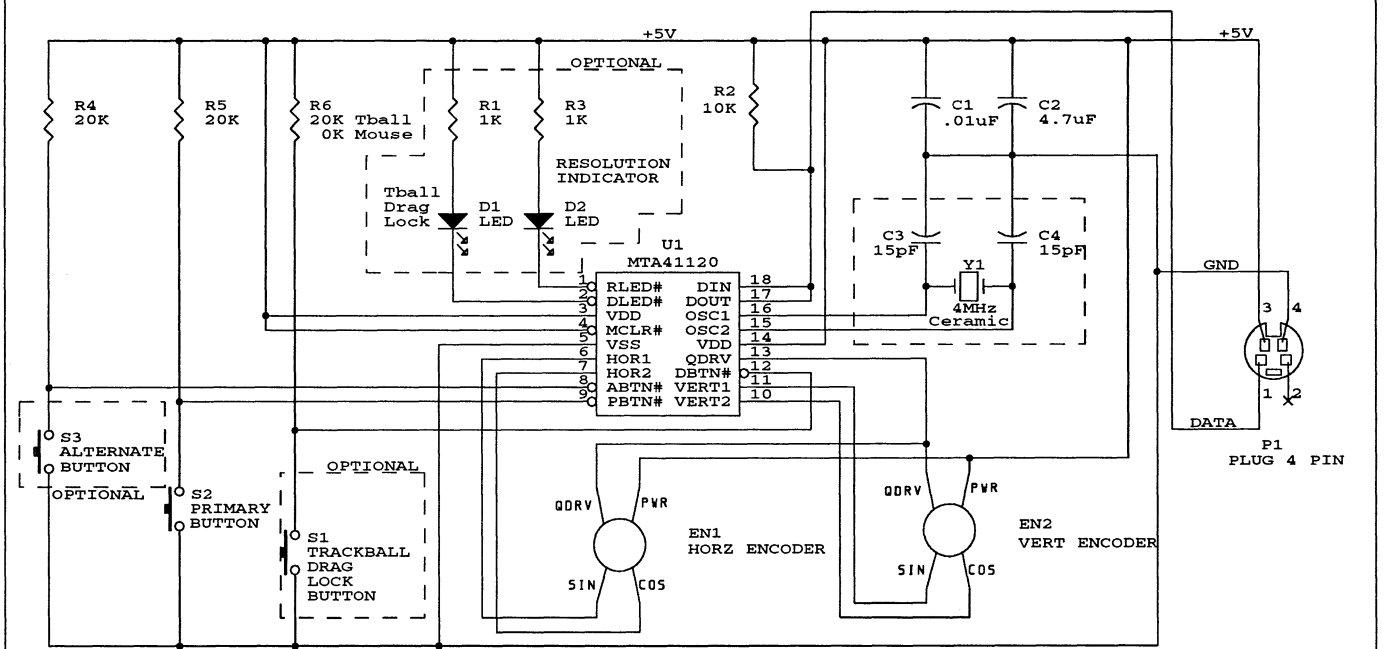
The MTA41120 controller can be configured as either a mouse or trackball controller. Trackball systems require the addition of the components labeled as trackball only. These components allow support of a drag lock switch and indicator. A pull-up resistor for the drag lock switch must be included in trackball systems. For a mouse the $\overline{DBTN}$ input is simply connected to V_{DD}.

Three examples of motion encoders are shown in the schematics (Document number 41XXXEN). Two types of optical encoders and a mechanical type are shown. Since the MTA41120 employs an anti-jitter algorithm, the "basic" style of optical encoder or the mechanical encoder are both recommended for use with the MTA41120. Use of the "improved" style of optical encoder that employs comparators, may only be necessary in high noise environments.

All button switches should be of the momentary contact type, including the drag lock switch.

Microchip Technology Inc.

MTA41120 Based Mouse or Trackball (note 1)



Note 1: System shown is for an Apple Macintosh compatable pointing device

Apple and Macintosh are registered trademarks of Apple Computer Inc.

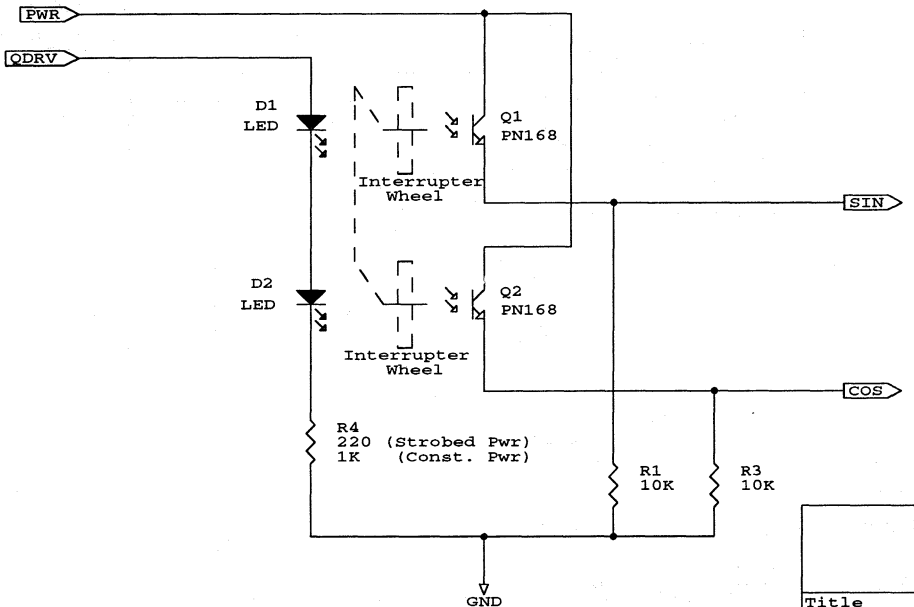
These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

Microchip Technology Inc. 2355 West Chandler Blvd. Chandler, AZ. 85224	
Title: MTA41120 Mouse or Trackball	
Size: A	Document Number: 41120ADa — REV: C
Date: December 16, 1993	Sheet 1 of 1

4

Microchip Technology Inc.

Basic Mouse/Trackball Optical Motion Encoder



LINK
OPTO2.SCH
MECH.SCH

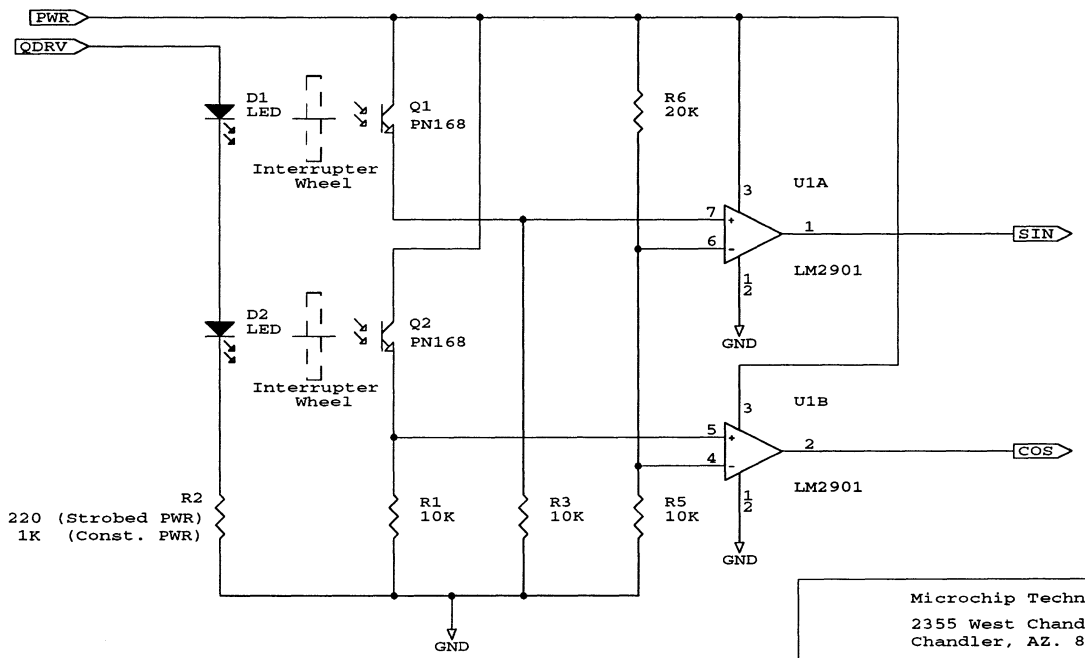
These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ. 85224

Title		
Typical Optical Motion Encoder		
Size	Document Number	REV
A	41XXXEN	C
Date: August 24, 1993	Sheet 1 of 3	

Microchip Technology Inc.

Improved Mouse/Trackball Optical Motion Encoder

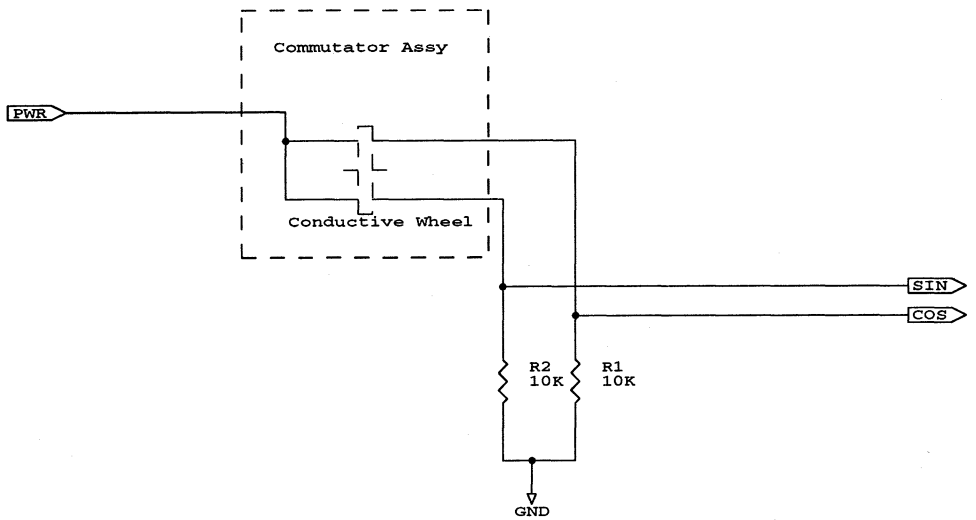


These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

Microchip Technology Inc. 2355 West Chandler Blvd. Chandler, AZ. 85224		
Title Improved Optical Motion Encoder		
Size A	Document Number 41XXXEN	REV C
Date: August 24, 1993	Sheet 2 of 3	

Microchip Technology Inc.

Mouse/Trackball Mechanical Motion Encoder



These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

Microchip Technology Inc. 2355 West Chandler Blvd. Chandler, AZ. 85224		
Title Typical Mechanical Motion Encoder		
Size A	Document Number 41XXXEN	REV C
Date: August 20, 1993	Sheet 3 of 3	

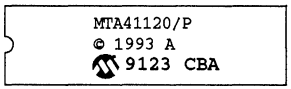
8.0 PACKAGING DIAGRAMS AND DIMENSIONS

See Section 11 of the Data Book.

9.0 PACKAGE MARKING INFORMATION

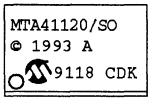
18L PDIP

Example

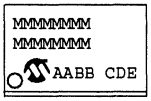


18L SOIC

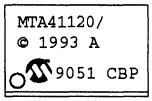
Example



20L SSOP



Example



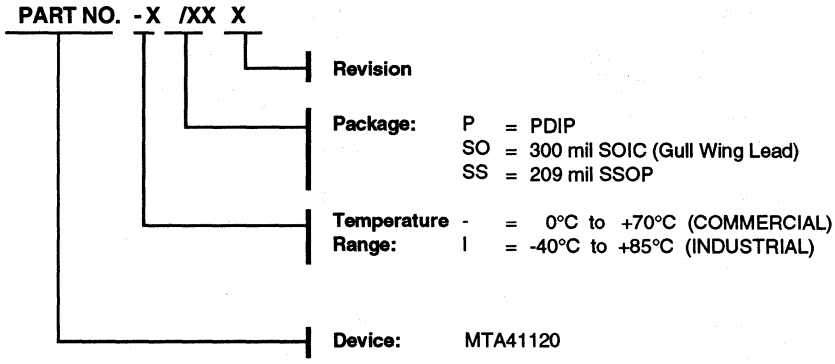
Legend:	MM...M	Microchip part number information
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line.

SALES AND SUPPORT

To order or to obtain information, e.g. on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



MTA41300

PS/2® and Serial Mouse and Trackball Controller I.C.

FEATURES

- Mouse and trackball controller IC
- Selectable RS-232 Serial or IBM® PS/2® interfaces
- Microsoft® serial interface format and IBM PS/2 mouse compliant
- Single-chip, two-button mouse or trackball controller
- 1200,N,7,1 - RS-232 serial communication format
- 10 KHz PS/2 interface
- Fixed mouse and trackball resolution
- Motion sampling rate of 12000 samples/second in PS/2 Mode and 15000 samples/second in RS-232 Mode
- Available in:
  - — 18-lead 300 mil PDIP
  - — 18-lead 300 mil SOIC
  - — 20-lead 209 mil SSOP

DESCRIPTION

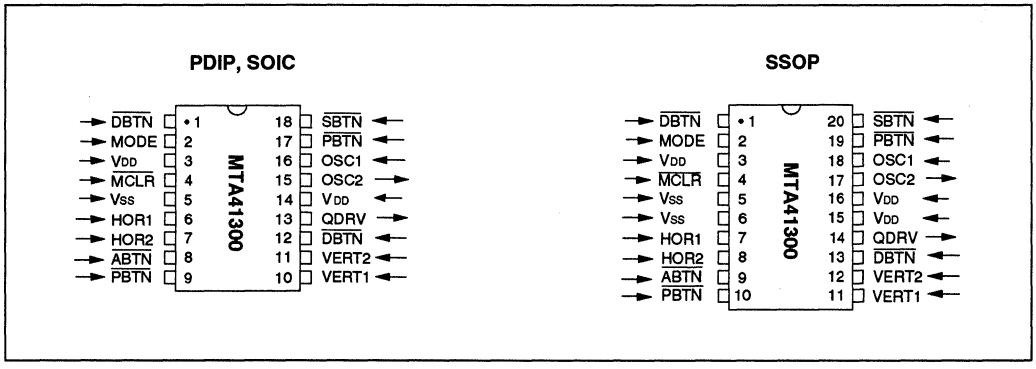
The MTA41300 is the heart of a simple, low-cost, mouse or trackball solution. It can be configured to operate as either an IBM PS/2 compliant mouse or as a serial mouse that is Microsoft serial format compatible. Both interface options are also available when the MTA41300 is used as a trackball controller. The mouse select and drag operation can be performed with a trackball by using the optional drag lock input and drag lock LED. This allows for one-handed select and drag when using a trackball.

MTA41300

The MTA41300 is an 18-lead low-power CMOS integrated circuit. Combined with a few simple external components, a complete mouse or trackball system can be realized.

4

FIGURE A - PIN CONFIGURATIONS



1.0 PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
$\overline{TXD}$	Output	Data port for RS-232 serial data. Active low. For IBM PS/2 Mode, this pin is a no connect and should be left open
MODE	Input	Mode select 1 = PS/2, 0 = RS-232 serial
HOR1	Input	Horizontal quadrature Input #1
HOR2	Input	Horizontal quadrature Input #2
$\overline{PBTN}$	Input	Primary mouse button. Active low, 0 = button depressed
$\overline{SBTN}$	Input	Secondary mouse button. Active low, 0 = button depressed
$\overline{DBTN}$	Input	Optional trackball drag lock button. Active low, 0 = button depressed. For mouse only operation, connect this pin to V_{DD}
VERT1	Input	Vertical quadrature input #1
VERT2	Input	Vertical quadrature input #2
$\overline{DLED}$	Output	Optional trackball drag LED. For mouse only operation, this pin is a no connect and should be left open
OSC1	Input	4 MHz crystal or ceramic resonator connection
OSC2	Output	4 MHz crystal or ceramic resonator connection
DATA	I/O	Bidirectional data port for PS/2. For Serial Mouse Mode, this pin is a no connect and should be left open
CLK	I/O	PS/2 data clock input. For Serial Mouse Mode, this pin is a no connect and should be left open
$\overline{MCLR}$	Input	A "low" voltage on this pin causes a reset condition for the MTA41300 controller
V_{DD}	Pwr	+5V
V_{SS}	Pwr	Ground

2.0 SERIAL MOUSE MODE OPERATION

When operating in serial mouse mode the MTA41300 mouse controller is a transmit only device. The MTA41300 transmits a fixed format data packet at 1200 baud to the host when a button press or mouse motion is detected.

2.1 Reset Initialization

The MTA41300 will transmit a "M" character immediately after power-up or when a reset is initiated by the host. This character notifies the host that the message format is Microsoft serial format compliant. The MTA41300 is placed in the reset state when the $\overline{MCLR}$ pin is driven low.

2.2 Serial Mode Message Format

The following Microsoft serial interface compliant data format is broadcast by the MTA41300 when transmitting data to the host. The 1200 baud data format utilizes a 9-bit data frame that consists of 7 bits of message data and 2 control bits.

Data Frame Format :

Bit	Description
1	Start Bit (always 0)
2	Message Data Bit 0, LSB
3	Message Data Bit 1
4	Message Data Bit 2
5	Message Data Bit 3
6	Message Data Bit 4
7	Message Data Bit 5
8	Message Data Bit 6, MSB
9	Stop bit (always 1)

The MTA41300 mouse controller transmits the following three byte Microsoft serial interface compliant data packet in response to a mouse event.

Message Data Byte 1:

Bit	Description
6	Always = 1 (message sync bit)
5	1 = Primary Button Depressed
4	1 = Secondary Button Depressed
3	Vertical Motion bit 7 (MSB)
2	Vertical Motion bit 6
1	Horizontal Motion bit 7 (MSB)
0	Horizontal Motion bit 6

Message Data Byte 2:

Bit	Description
6	Always = 0
5	Horizontal Motion bit 5
4	Horizontal Motion bit 4
3	Horizontal Motion bit 3
2	Horizontal Motion bit 2
1	Horizontal Motion bit 1
0	Horizontal Motion bit 0

Message Data Byte 3:

Bit	Description
6	Always = 0
5	Vertical Motion bit 5
4	Vertical Motion bit 4
3	Vertical Motion bit 3
2	Vertical Motion bit 2
1	Vertical Motion bit 1
0	Vertical Motion bit 0

3.0 IBM PS/2 MODE OPERATION

Upon power-up the MTA41300 mouse controller initiates an internal reset sequence. First, all internal registers and communication parameters are cleared. Next, the status registers are set to the default condition. Finally, if the MTA41300 receives a Resend command as the first command after power-up, it will transmit a AAh followed by a 00h in response. This notifies the host that the initialization is complete and that the controller is a standard mouse type. This is to ensure compatibility with some hosts that do not follow the normally recommended behavior of issuing a Reset command as the first command after power-up.

The MTA41300 always confirms reception of a command sent by the host by returning an acknowledge byte (FAh). If the host interrupts the transmission of the acknowledge byte, the MTA41300 discards the complete command. The MTA41300 is then ready to receive and acknowledge the next command. Two exceptions to the acknowledge after command received rule exist. The MTA41300 does not issue an acknowledge upon receipt of either the Set Wrap Mode (EEh) or Resend (FEh) commands.

3.1 PS/2 Mode Commands

Command Summary:

Command	Code
Reset	FFh
Resend	FEh
Set Default	F6h
Disable Reporting	F5h
Enable Reporting	F4h
Set Report Rate	F3h, XXh
Read Device Type	F2h
Set Remote Mode	F0h
Set Wrap Mode	EEh
Reset Wrap Mode	ECh
Read Data	EBh
Set Stream Mode	EAh
Status Request	E9h
Set Resolution	E8h, XXh
Set Scaling	E7h
Reset Scaling	E6h

3.1.1 Reset Code: FFh

This command initiates a reset sequence in the MTA41300 mouse controller. First, all internal registers and communication parameters are cleared. Next, the status registers are set to the default condition. Finally, the MTA41300 transmits a AAh followed by a 00h, this notifies the host that the initialization is complete and that the controller is a standard mouse type.

3.1.2 Resend Code: FEh

Anytime the MTA41300 controller receives an invalidly formatted command, it will transmit a Resend command to the host. The controller will ignore invalid commands and will continue to operate in its present mode. When any command other than a resend is received by the controller, it will clear its motion and displacement counters.

The host system may send a Resend command to the controller if an error is detected in a transmission from the controller. When the controller receives a Resend command, it will retransmit the last data packet transmitted. If the last packet transmit was a resend command, the packet prior to the last packet will be retransmitted.

3.1.3 Set Default Code: FEh

The Set Default command re-initializes all controller parameters to the power-up state. The controller initializes the following status registers, which only exist to ensure compatibility.

Report rate:	100 reports per second
Scaling:	Linear
Mode:	Streaming
Resolution:	Physical resolution
Reporting:	Disabled

This command does not initiate self test diagnostics. The controller remains in the disabled state until another command is received from the host.

3.1.4 Disable Reporting Code: F5h

The Disable Reporting command prevents data transmission by the controller while it is in the Stream Mode. However, the controller will still respond to other commands. When reporting is disabled, Stream Mode must be disabled prior to the host sending a command that requires a response by the controller.

3.1.5 Enable Reporting Code: F4h

The Enable Reporting command allows the controller to transmit data when in Stream Mode. This command has no effect while the controller is in Remote Mode.

3.1.6 Set Report Rate Code: F3h, XXh

This command updates the report rate status register with the data contained in the second byte of the command. However, the actual report rate remains fixed at 40 times per second. This command only exists to ensure compatibility.

3.1.7 Read Device Type Code: F2h

The controller always transmits a 00h in response to receiving this command. This informs the host that a standard mouse is present.

3.1.8 Set Remote Mode Code: F0h

Remote Mode is entered when the controller receives this command. In Remote Mode, event packets are transmitted to the host only when a read data command is received by the controller.

3.1.9 Set Wrap Mode Code: EEh

Wrap Mode is entered when the controller receives this command. In Wrap Mode, the controller will echo all commands that are received back to the host. Note, the Reset and Reset Wrap commands will cancel wrap mode and neither of these commands will be echoed back to the host. Wrap Mode can be enabled in either Reporting, Stream or Remote Mode.

3.1.10 Reset Wrap Mode Code: ECh

This command cancels Wrap Mode. The controller remains in the current Reporting Mode. Note, if the controller enters Wrap Mode while in Stream Mode and then a Reset Wrap Mode command is received, the controller will reenter the Stream Mode with Wrap Mode disabled.

3.1.11 Read Data Code: EBh

The controller will transmit an event packet to the host after a Read Data command is received. This command can be issued in the Remote or Stream Mode. The controller will transmit data even if there has not been any button changes or motion since the last report. The controller clears the motion counters after every read data command.

3.1.12 Set Stream Mode Code: EAh

The controller will enter the Stream Mode upon receiving this command. In Stream Mode event packets are transmitted to the host as they occur.

3.1.13 Status Request Code: E9h

A three byte status report packet will transmit in response to this command. These status bytes are defined as follows:

Byte 1:

Bit	Description
0	1= Secondary Button Depressed
1	Reserved
2	1= Primary Button Depressed
3	Reserved
4	1= 2:1 scaling
5	1= Enabled
6	1= Remote Mode
7	Reserved

Byte 2: Current Resolution

Byte 3: Current Sample Rate

3.1.14 Set Resolution Code: E8h, XXh

This command has no effect and only exists to ensure compatibility. The physical device resolution is always the resolution of the mouse or trackball.

3.1.15 Set Scaling Code: E7h

This command has no effect on resolution and only exists to ensure compatibility. The scaling will always be 1:1.

3.1.16 Reset Scaling Code: E6h

This command has no effect on resolution and only exists to ensure compatibility. The scaling will always be 1:1.

3.2 PS/2 Message Data Format

The following PS/2 compliant data format is used by the MTA41300 when transmitting data to the host and when receiving data from the host. The data format utilizes an 1-bit data frame that utilizes 8 bits for message data and 3 bits for control.

PS/2 Data Frame Format :

Bit	Description
1	Start Bit (always 0)
2	Message Data Bit 0, LSB
3	Message Data Bit 1
4	Message Data Bit 2
5	Message Data Bit 3
6	Message Data Bit 4
7	Message Data Bit 5
8	Message Data Bit 6
9	Message Data Bit 7, MSB
10	Parity Bit (odd parity)
11	Stop bit (always 1)

The MTA41300 mouse controller transmits the following three-byte data packet in response to a Read Data (EBh) command or when operating in stream mode with reporting enabled.

Status Message Data Byte 1:

Bit	Description
0	1= Primary Button Depressed
1	1= Secondary Button Depressed
2	Reserved
3	Reserved
4	X data sign, 1 = negative
5	Y data sign, 1 = negative
6	X data overflow, 1 = overflow
7	Y data overflow, 1 = overflow

Status Message Data Byte 2: Delta X motion

Status Message Data Byte 3: Delta Y motion

4.0 MOTION ENCODER INPUTS

The MTA41300 is designed to interface with either optical encoders that utilized LED and phototransistor pairs with a chopper wheel, or mechanical encoders utilizing a commutator with wiper contacts. The HOR and VERT inputs detect positive and negative delta motion. Motion direction is defined in the following state table. Refer to Figures 4.1 and 4.2.

Positive Motion:

Hor1, Hor2/ Vert1,Vert2	Description
0,0	
0,1	
1,1	Positive Direction
1,0	Sequence
0,0	
etc.	

Negative Motion:

Hor1, Hor2/ Vert1,Vert2	Description
0,0	
1,0	
1,1	Negative Direction
0,1	Sequence
0,0	
etc.	

The HOR and VERT inputs are sampled at approximately 12000 samples per second with a 4 MHz input clock. The sample rate will decrease when communication traffic to or from the host is occurring. There is a one

FIGURE 4.1 - POSITIVE MOTION INPUT

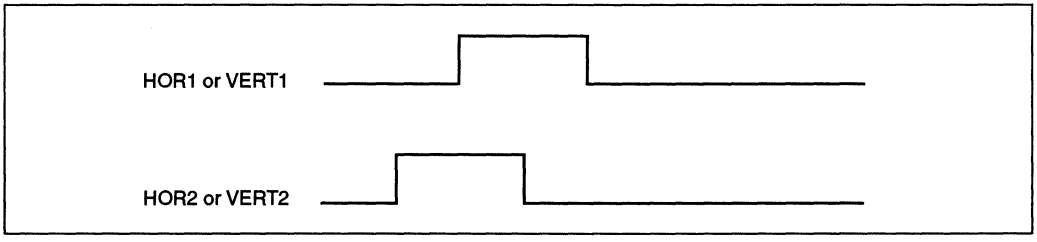
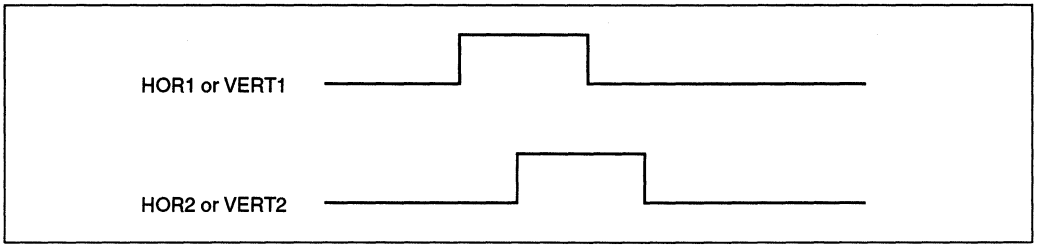


FIGURE 4.2 - NEGATIVE MOTION INPUT



to one correlation between encoder transitions and the motion data that is transmitted to the host. For example, a transition of 0,1 to 1,1 on the horizontal encoder inputs (HOR1, HOR2) will result in one bit of horizontal motion as broadcast to the host. The sample rate, along with all other timed events related to the controller, is directly proportional to the clock frequency on the OSC1 and OSC2 pins.

An anti-jitter algorithm is employed to eliminate false motion counting when the mouse or trackball is not moving. This is especially useful in designs employing optical encoders since the output of an optical detector is an analog signal. The anti-jitter algorithm eliminates false counting when a voltage that is not a well defined logic low or logic high is applied to either the HOR or VERT inputs.

5.0 PUSHBUTTON INPUTS

The MTA41300 pushbutton inputs are defined to be active when the input pin is in the low state. The appropriate message data bit will be set equal to one when a low is sampled at a switch input. When a switch input is sampled in the high state the appropriate message data bit will be set equal to zero.

6.0 TRACKBALL OPTION

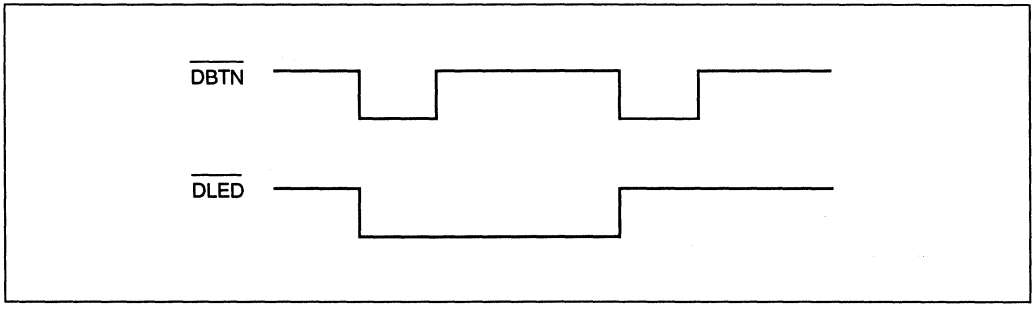
The MTA41300 can also function as a trackball controller. A trackball drag lock switch can be connected to the $\overline{\text{DBTN}}$ input and an LED indicator connected to the $\overline{\text{DLED}}$ output to aid in one-handed trackball operation.

When using a mouse, a select and drag operation is accomplished by clicking on an object and holding the primary mouse button down. Moving the mouse then drags the object to the desired location. When the primary button is released, the object is placed at the desired location. However, when the same select and drag operation is performed using a trackball it may be difficult to hold the button depressed and guide the trackball with the same hand.

The MTA41300's "drag lock" feature allows this function to be accomplished with one hand. The drag lock is set to the "locked" state by momentarily applying a low to the $\overline{\text{DBTN}}$ input. This "locked" state is equivalent to depressing and holding the primary button when using a mouse. The user then guides the object to the desired location without having to hold a button depressed and simultaneously guide the trackball. The object is placed and the "lock" is released when a low (e.g. button depressed) is momentarily applied to any button input.

The $\overline{\text{DLED}}$ output is latched in the low state (0V) when the $\overline{\text{DBTN}}$ input is sampled low (refer to Figure 6.1). The $\overline{\text{DLED}}$ output will remain low ("locked") until the $\overline{\text{DBTN}}$ input is sampled high and then sampled low again. Exiting the locked state also occurs if either the $\overline{\text{PBTN}}$ or $\overline{\text{SBTN}}$ inputs are sampled low when the $\overline{\text{DLED}}$ output is low. When the $\overline{\text{DLED}}$ output is in low "locked" state, the Primary Button depressed bit in the status message is set high.

FIGURE 6.1 - TRACKBALL DRAG LOCK OPERATION



7.0 ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS †

Ambient temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to Vss (except VDD and $\overline{MCLR}$) .-0.6V to (VDD +0.6V)

Voltage on $\overline{MCLR}$ pin with respect to Vss ..... 0V to +14.0V

Voltage on VDD with respect to Vss ..... 0V to +9.5V

Total power dissipation (Note 2) ..... 800 mW

Maximum current out of Vss pin ..... 150 mA

Maximum current into VDD pin ..... 50 mA

Maximum current into input pin ..... ±500 µA

Maximum output current sinked by any I/O or output pin ..... 25 mA

Maximum output current sourced by any I/O or output pin ..... 20 mA

Notes:

1. Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to this pin, rather than connecting this pin directly to Vss.
2. Total power dissipation should not exceed 800 mW for the package. The total power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times (I_{DD} - \sum I_{OH}) + \sum\{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$.

4

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

7.2 DC CHARACTERISTICS MTA41300 (COMMERCIAL)

DC CHARACTERISTICS						Standard Operating Conditions (unless otherwise stated). Operating Temperature 0°C < TA < 70°C for commercial. Operating voltage VDD = 3.0V to 5.5V unless otherwise stated.
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply Voltage	VDD	3.0		6.25	V	FOSC = DC to 4 MHz
VDD start voltage to guarantee power on reset	VPOR		VSS		V	
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/mS	
Supply Current	IDD		1.8	3.3	mA	FOSC = 4 MHz , VDD = 5.5V
Input Low Voltage						
$\overline{MCLR}$ (Schmitt trigger)	VILMC			.15VDD	V	
OSC1 (Schmitt trigger)	VILOSC			.3VDD	V	
All other Inputs	VIL			.2VDD	V	
Input High Voltage						
$\overline{MCLR}$ (Schmitt trigger)	VIHMC	.85 VDD		VDD	V	
OSC1 (Schmitt trigger)	VIHOSC	.7 VDD		VDD	V	
All other Inputs	VIH	.45 VDD		VDD	V	
		2 V		VDD	V	4.0V < VDD ≤ 5.5V
Input Leakage Current						
$\overline{MCLR}$	IILMCL	-5			µA	VPIN = VDD + 0.25V
$\overline{MCLR}$	IILMCH		0.5	+5	µA	VPIN = VDD
OSC1 (Schmitt trigger)	IILMCH		0.5	+3	µA	VDD ≤ VPIN ≤ VDD
All other Inputs	IIL	-1	0.5	+1	µA	VDD ≤ VPIN ≤ VDD
Output Low Voltage						
OSC2	VOL			0.6V	V	IOL = 1.6mA, VDD = 4.5V
All other Outputs	VOL	VDD - .7		0.6V	V	IOL = 8.7mA, VDD = 4.5V
Output High Voltage						
OSC2						IOH =-1.0mA, VDD = 4.5V
All other Outputs	VOH				V	IOH =-5.4mA, VDD = 4.5V

*These parameters are based on characterization and are not tested.

FIGURE 7.2.1 - INPUT THRESHOLD VOLTAGE (V_{TH}) OF ALL INPUT AND I/O PINS EXCEPT MCLR AND OSC1

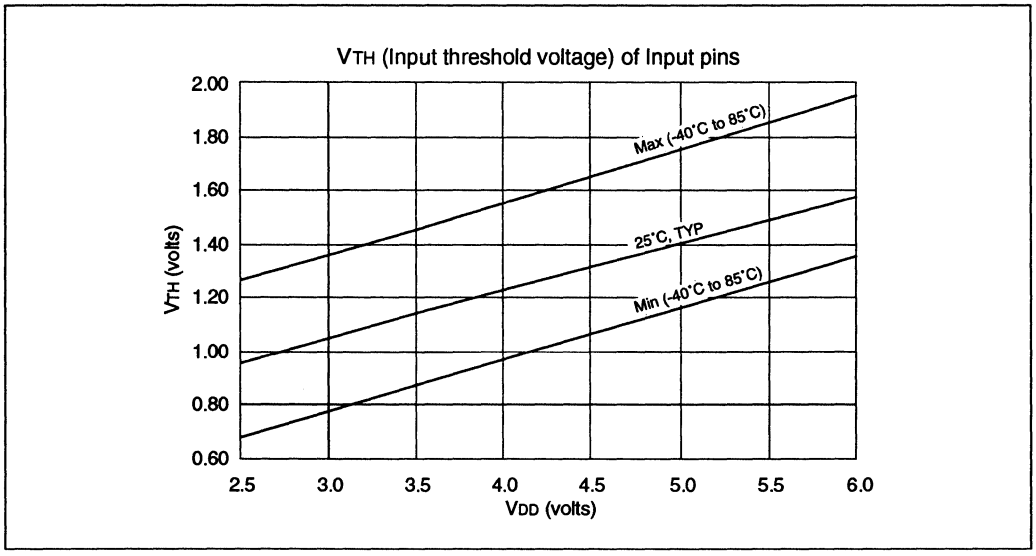
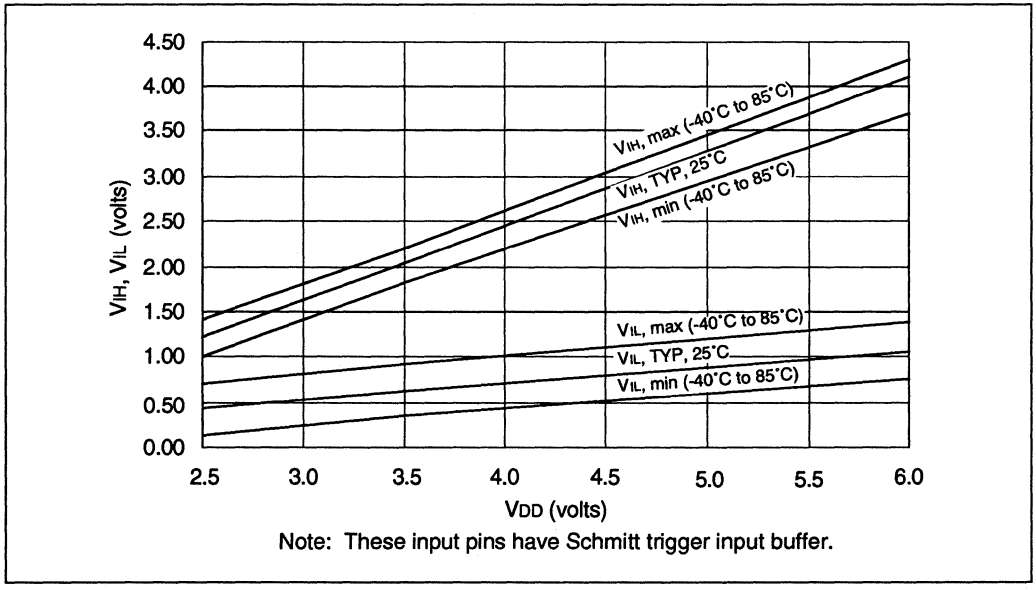


FIGURE 7.2.2 - V_{IH}, V_{IL} OF $\overline{MCLR}$ vs V_{DD}



Note: These input pins have Schmitt trigger input buffer.

FIGURE 7.2.3 - INPUT THRESHOLD VOLTAGE (V_{TH}) OF OSC1 INPUT

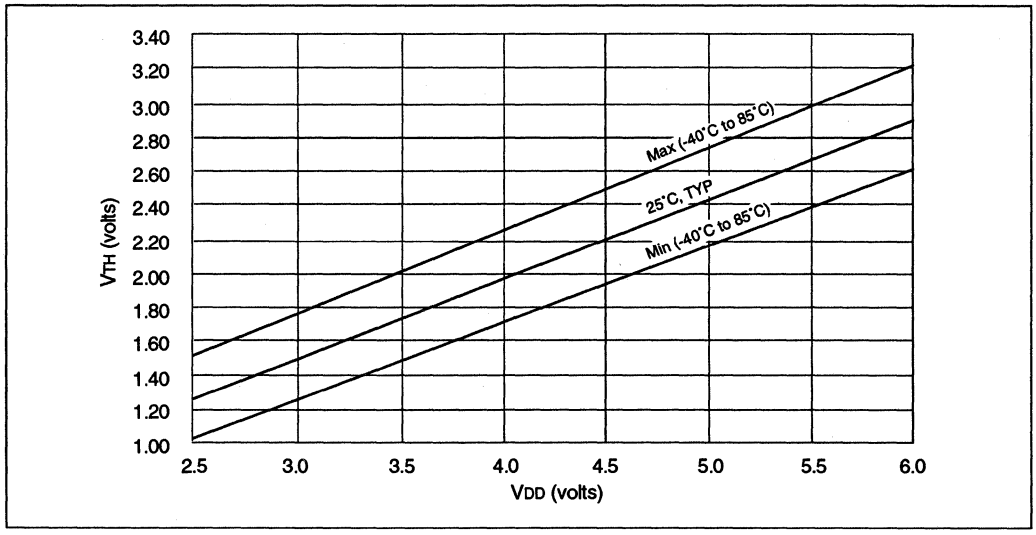


FIGURE 7.2.4 - I_{OH} vs V_{OH}, V_{DD} = 3V

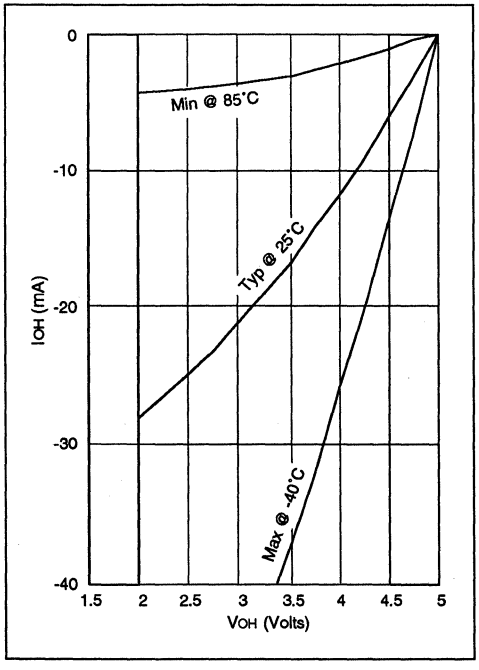


FIGURE 7.2.5 - I_{OH} vs V_{OH}, V_{DD} = 5V

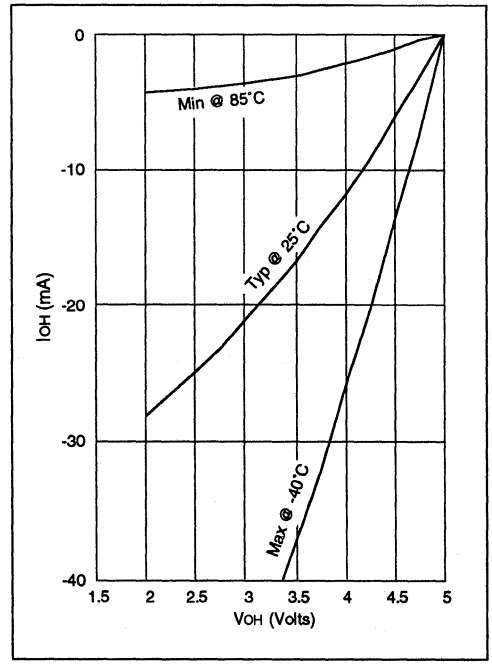


FIGURE 7.2.6 - IOL vs VOL, VDD = 3V

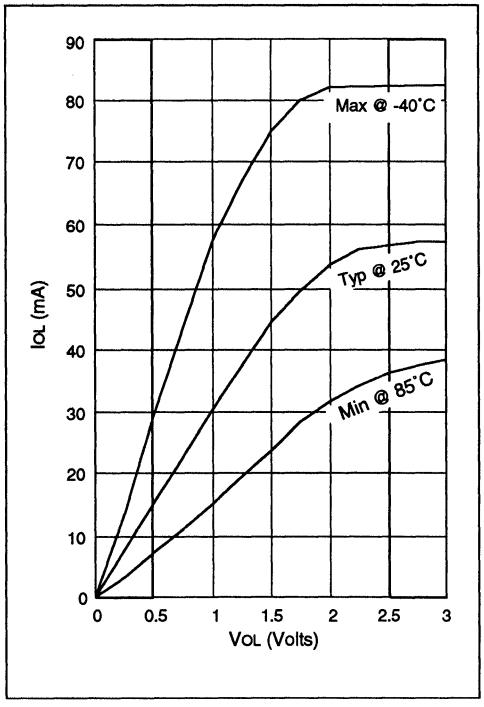
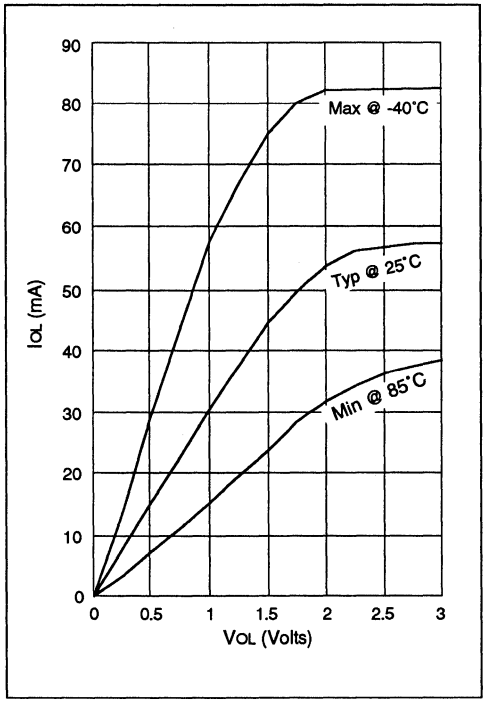


FIGURE 7.2.7 - IOL vs VOL, VDD = 5V



4

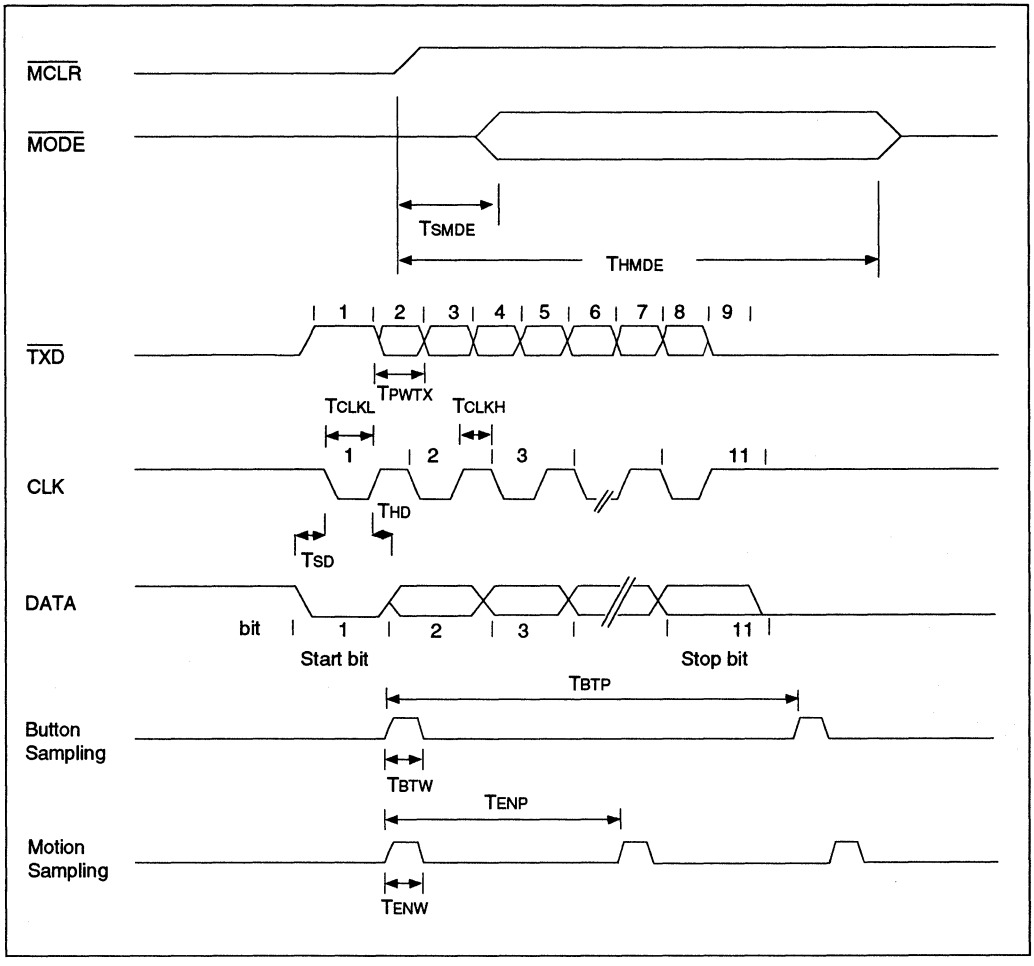
7.3 AC CHARACTERISTICS MTA41300 (COMMERCIAL)

AC CHARACTERISTICS						Standard Operating Conditions (unless otherwise stated). Operating Temperature 0°C < TA < 70°C for commercial. Operating Voltage VDD = 3.0V to 5.5V unless otherwise stated. Oscillator Frequency = 4 MHz.
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Oscillator Frequency	FOSC	DC		4	MHz	
Serial Mode Output Timing						
TXD output pulse width (per bit)	TPWTX	800	833	866	µS	1200 baud @ FOSC = 4 MHz
PS/2 Mode I/O Timing						
CLK High time	TCLKH	30		50	µS	
CLK Low time	TCLKL	30		50	µS	
DATA setup time to CLK falling	TSD	5		25	µS	
DATA hold time to CLK rising	THD	5		45		
Input Timing:						
$\overline{PBTN}$, $\overline{SBTN}$, $\overline{DBTN}$						
Input Sample Period	TBTP			50	ms	
Input Sample Window width	TBTW			280	ns	
HOR1,HOR2,VERT1,VERT2						
Input Sample Period (PS/2 Mode)	TENP2		83[1]		µS	
Input Sample Period (RS-232 Mode)	TENPS		66		µS	
Input Sample Window width	TENW			280	ns	
RESET Timing						
$\overline{MCLR}$ pulse width (low)	TMCL	100			ns	
Oscillator Start-up Timer Period	TOST	9[2]	18[2]	30[2]	ms	VDD = 5.0V
MODE Timing						
Setup time	TSMDE	-5			ms	from $\overline{MCLR}$ high
Hold time	THMDE	50			ms	from $\overline{MCLR}$ high

Notes: 1. Sampling can be suspended if device is receiving data from host or if transmission to host is inhibited by host (CLK held low).

2. These parameters are based on characterization and are not tested.

FIGURE 7.3 - TIMING DIAGRAMS



4

8.0 APPLICATION EXAMPLES

Three distinct types of mice or trackball systems can be created using the MTA41300 controller. These systems are distinguished on the type of host interface they use. The three types are: RS-232 serial, IBM PS/2, or a "combo" interface that can operate in either RS-232 or PS/2.

Also, three example types of motion encoders are shown in the schematics (document number 41XXXEN). Two types of optical encoders and a mechanical type are shown.

All system types use momentary contact type switches for the button inputs including the drag lock input.

8.1 RS-232 Serial Interface Mouse or Trackball

To operate the MTA41300 controller in the RS-232 Serial Mode only, the MODE pin is simply connected to Vss. The example schematic (document number 41300RSa), shows the MTA41300 configured as a RS-232 serial mouse or trackball.

Trackball systems require the addition of the components labeled as trackball only. These components allow support of a drag lock switch and indicator. A pull-up resistor for the drag lock switch must be included for trackball systems. For a mouse the $\overline{DBTN}$ input is simply connected to VDD.

Since the MTA41300 operates from a single supply a discrete transistor is used as a level shifter to insure that a low output on the RS-232 data line is below the -3V RS-232 threshold.

8.2 PS/2 Interface Mouse or Trackball

To operate the MTA41300 controller in the PS/2 Mode only, the MODE pin is simply connected to VDD. The example schematic, document number 41300PSa, shows the MTA41300 configured as a PS/2 mouse or trackball.

8.3 RS-232 and PS/2 "Combo" Mouse or Trackball

The "combo" mouse system is designed to change its host interface to the desired protocol depending on the type of host system it is connected to. The schematic (document number 41300SPa) shows a typical "combo" mouse or trackball. In this system, the MODE select is wired to the host connector and is not connected directly to either VDD or Vss.

For RS-232 operation, the RTS line is driven by the host to -12V. A protection diode limits the maximum negative voltage applied to the MODE pin to -.6V. This logical low on power-up places the MTA41300 in the RS-232 Serial Interface Mode.

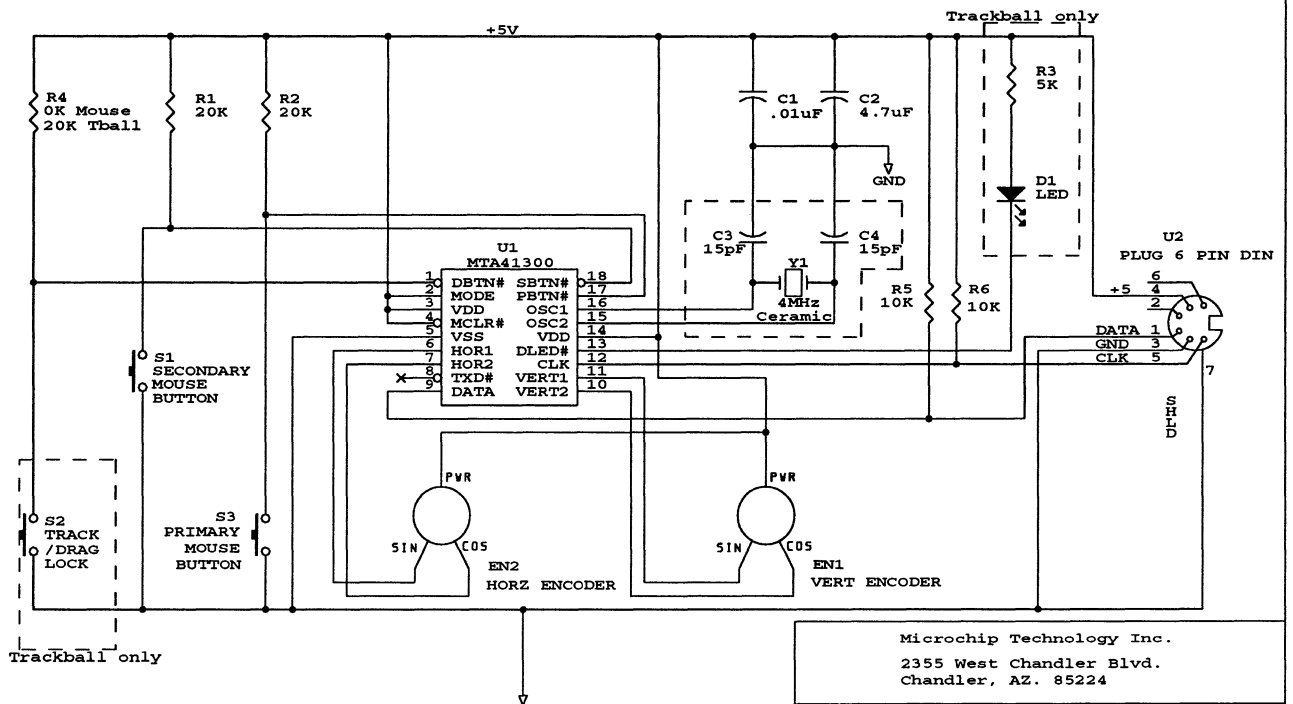
For PS/2 operation, a special adapter plug (document number 41300SPa, page 2) can be used to change the RS-232 DB-9 connector to the mini-DIN type used by PS/2 systems. The adapter plug also connects the MODE pin to +5V thus automatically configuring the MTA41300 for the PS/2 interface.

8.4 Host System Device Drivers

The MTA41300 is compatible with standard IBM PS/2 drivers and Microsoft device drivers. Additionally, host system device drivers for use with the MTA41300 are available from third party vendors. Contact your local Microchip Technology Inc. sales office for a list of vendors currently offering device drivers for use with the MTA41300.

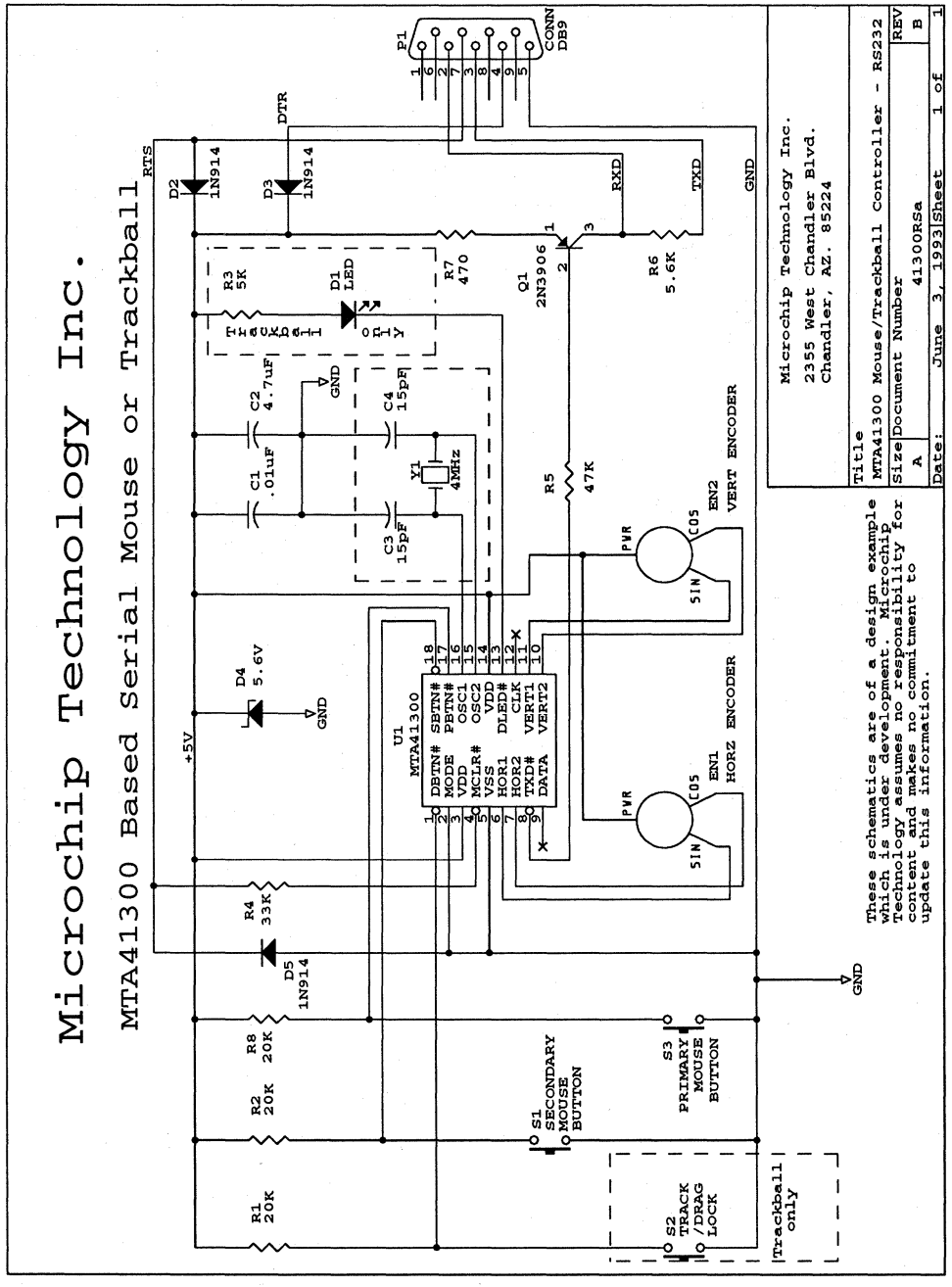
Microchip Technology Inc.

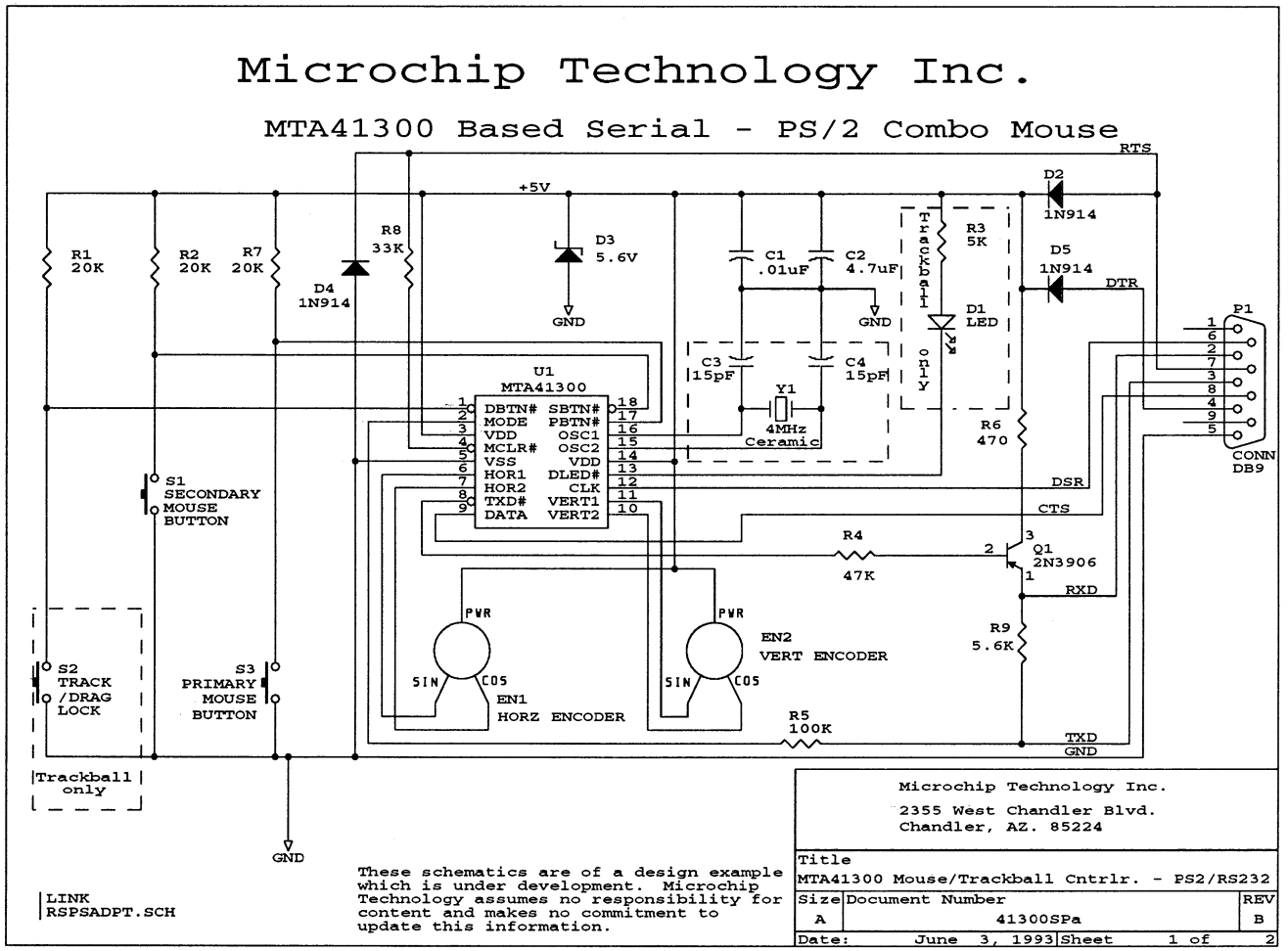
MTA41300 Based PS/2 Mouse or Trackball



These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

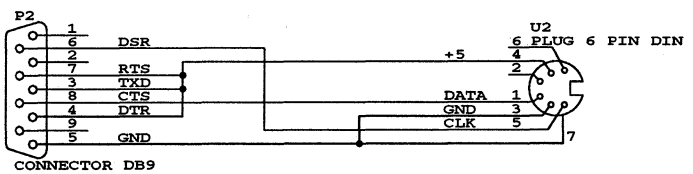
Microchip Technology Inc. 2355 West Chandler Blvd. Chandler, AZ. 85224	
Title: MTA41300 Mouse/Trackball Controller - PS/2	
Size: A	Document Number: 41300PSa — REV: B
Date: June 3, 1993	Sheet 1 of 1





Microchip Technology Inc.

RS232 TO PS/2 ADAPTER PLUG WIRING FOR MTA41300

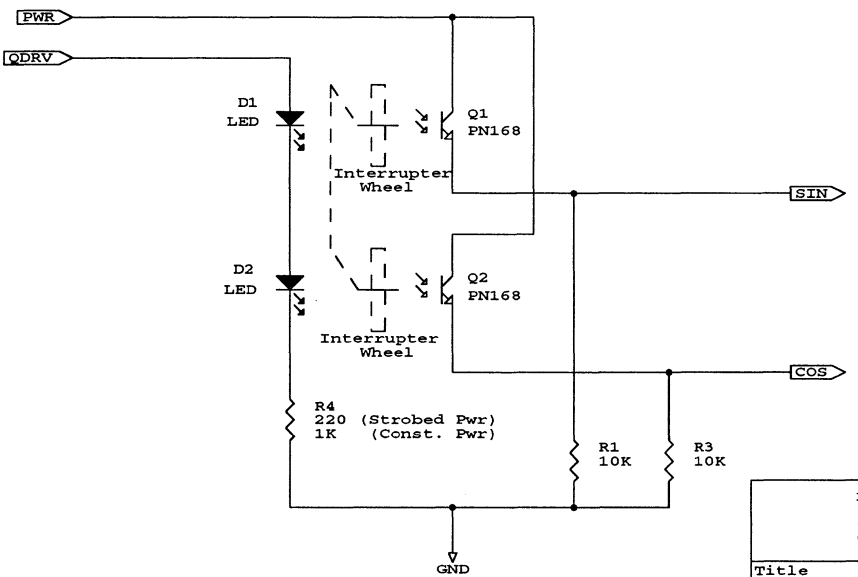


These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

Microchip Technology Inc. 2355 West Chandler Blvd. Chandler, AZ. 85224		
Title RS232/PS2 Adapter Plug		
Size A	Document Number 41300SPa	REV B
Date: June 3, 1993	Sheet 2 of 2	

Microchip Technology Inc.

Basic Mouse/Trackball Optical Motion Encoder



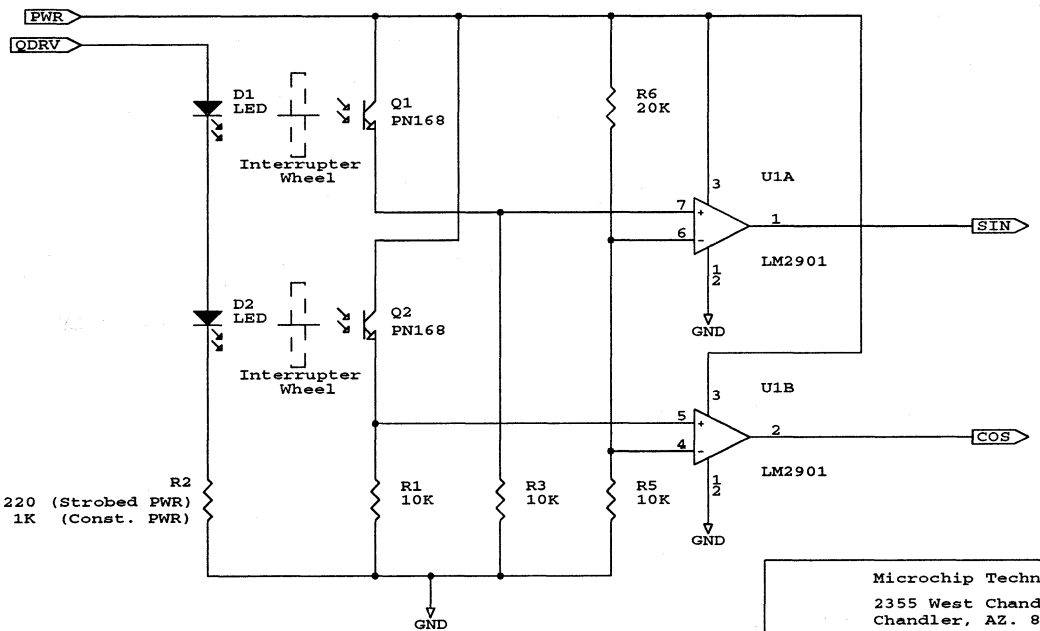
LINK
OPTO2.SCH
MECH.SCH

These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

Microchip Technology Inc. 2355 West Chandler Blvd. Chandler, AZ. 85224	
Title: Typical Optical Motion Encoder	
Size: A	Document Number: 41XXXEN — REV: C
Date: August 24, 1993	Sheet: 1 of 3

Microchip Technology Inc.

Improved Mouse/Trackball Optical Motion Encoder

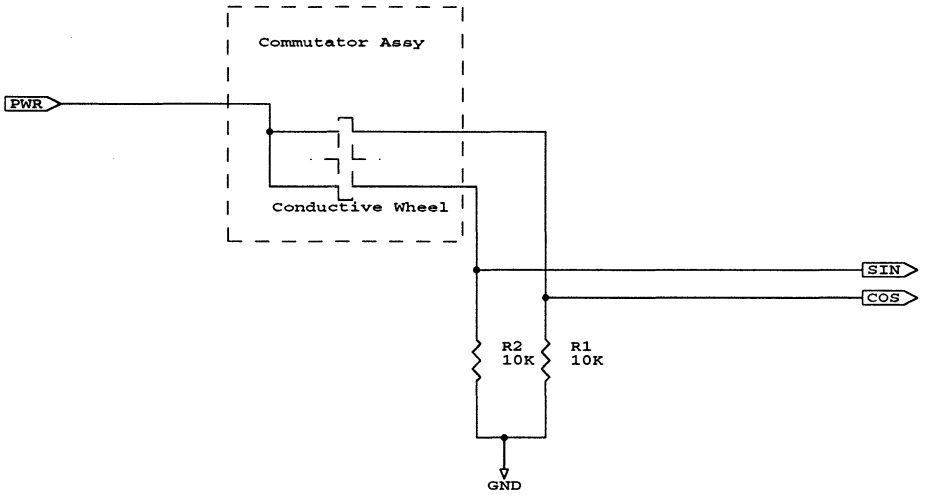


These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

Microchip Technology Inc. 2355 West Chandler Blvd. Chandler, AZ. 85224	
Title: Improved Optical Motion Encoder	
Size: A	Document Number: 41XXXEN — REV: C
Date: August 24, 1993	Sheet 2 of 3

Microchip Technology Inc.

Mouse/Trackball Mechanical Motion Encoder



These schematics are of a design example which is under development. Microchip Technology assumes no responsibility for content and makes no commitment to update this information.

Microchip Technology Inc. 2355 West Chandler Blvd. Chandler, AZ. 85224		
Title Typical Mechanical Motion Encoder		
Size A	Document Number 41XXXEN	REV C
Date: August 20, 1993	Sheet 3 of	3

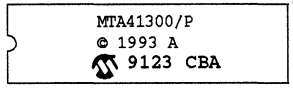
9.0 PACKAGING DIAGRAMS AND DIMENSIONS

See Section 11 of the Data Book.

10.0 PACKAGE MARKING INFORMATION

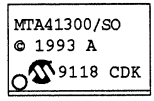
18L PDIP

Example

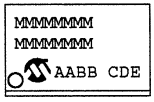


18L SOIC

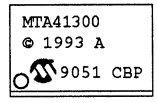
Example



20L SSOP



Example



Legend:	MM...M	Microchip part number information
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

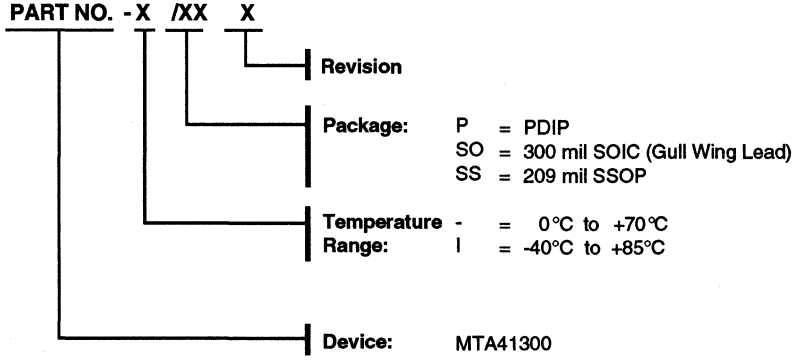
Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



MICROCHIP

MTA41600

UniMouse™ Mouse and Trackball Controller I.C.

FEATURES

- Selectable for most popular communication formats
- Microsoft® serial interface format compatible
- Mouse Systems® serial interface format compatible
- IBM PS/2® mouse compatible host interface
- Apple® Macintosh® compatible host interface
- Single chip one, two or three-button mouse controller
- Motion sampling rate of 6000 Samples/second
- Available In:

  18-lead 300 mil PDIP

  18-lead 300 mil SOIC

  20-lead 209 mil SSOP

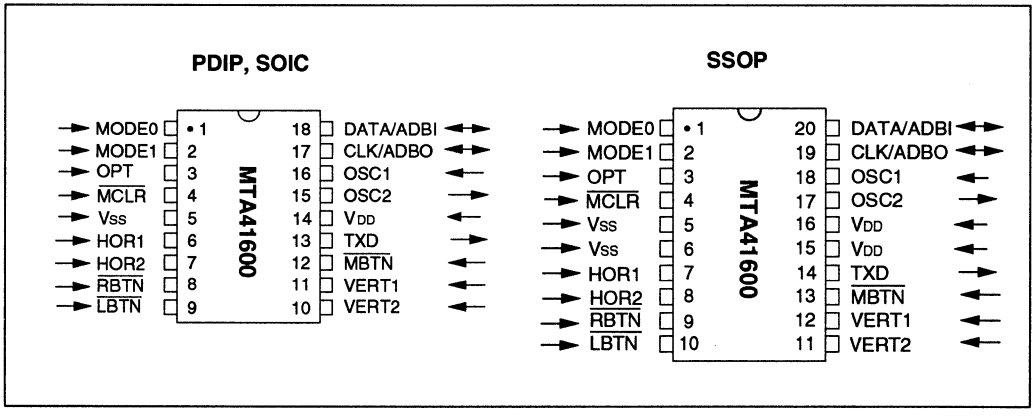
DESCRIPTION

The MTA41600 is the heart of a simple, low-cost, universal mouse solution. By combining the four most popular interface formats in a single controller, one pointing device can function with a wide variety of host machines. It can be configured to operate as either an IBM PS/2 compatible mouse, an Apple Macintosh compatible mouse, a serial mouse that is Microsoft serial format compliant, or a serial mouse that is Mouse Systems serial format compatible.

The MTA41600 is an 18-lead low-power CMOS integrated circuit. Combined with a few simple external components, a complete universal mouse solution can be realized.

4

FIGURE A - PIN CONFIGURATIONS



MICROCHIP

MTA81010

PICSEE™ 28-Pin MCU with Serial EEPROM Multi-Chip Module

FEATURES

- Multi-chip module
- PIC16C54 Microcontroller and 24LC01B Serial EEPROM in a single package
- 512 x 12 EPROM program memory
- 128 x 8 Serial EEPROM data memory
- Separate VDD inputs for Microcontroller and Serial EEPROM
- ESD protection > 4,000 V

MICROCONTROLLER FEATURES

High Performance RISC-like CPU

- Only 33 single word instructions to learn
- All single-cycle instructions except for program branches which are two-cycle
- Operating speed: DC - 4 MHz clock input
  DC - 1 µs instruction cycle
- 12-bit wide instructions
- 8-bit wide data path
- 25 x 8 general purpose registers (SRAM)
- 7 special function hardware registers
- 2 level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features

- 12 I/O pins with individual direction control
- 8 bit real time clock/counter (RTCC) with 8-bit programmable prescaler
- Power on reset
- Oscillator start-up timer
- Watchdog timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security EPROM fuse for code-protection
- Power saving SLEEP mode
- EPROM fuse selectable oscillator options:
  - Low cost RC oscillator: RC
  - Standard crystal/resonator: XT
  - Power saving low frequency crystal: LP

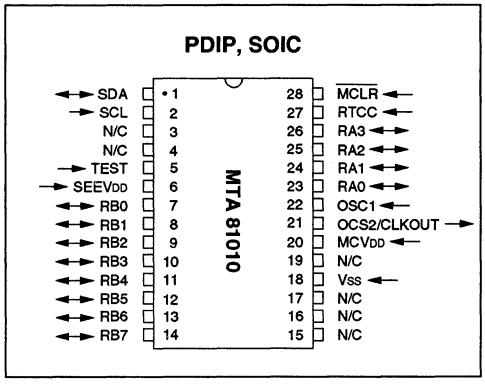
CMOS Technology

- Low-power, high-speed CMOS EPROM technology
- Factory programming (QTP) available for EPROM
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.5V to 6.25V
  - Industrial: 2.5V to 6.25V
- Low power consumption
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 KHz
  - < 3 µA typical standby current @ 3V, 0°C to 70°C

SERIAL EEPROM FEATURES

- Single supply with operation down to 2.5 volts
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as a single block of 128 bytes (128 x 8)
- Two-wire serial interface bus
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 KHz and 400 KHz compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years

FIGURE A - PIN CONFIGURATIONS



PICSEE is a trademark of Microchip Technology Inc.

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1.0 GENERAL DESCRIPTION

The MTA81010 from Microchip Technology offers the unique combination of a EPROM-based microcontroller and a Serial EEPROM in a single package. It is a multi-chip module that combines a PIC16C54, low cost, high performance, 8-bit, fully static, EPROM-based CMOS microcontroller with a 24LC01B, a 1K bit Serial Electrically Erasable PROM. Combining these two popular chips into a single package reduces system cost, board area, and inventory.

The microcontroller and EEPROM are electrically independent, sharing only a common ground (Vss). Independent power sources are valuable in power-conscious applications where it may be desirable to power down the EEPROM when it is not being accessed. One of the microcontroller's output pins can supply power directly to the internal EEPROM's power pin thus avoiding the use of external power switching components.

The microcontroller and serial EEPROM are exactly equivalent to their respective individual chips, the PIC16C54 and 24LC01B.

1.1 APPLICATIONS

The MTA81010 is ideally suited to a wide variety of applications including but not limited to; keyless entry, remote control, smart cards, and automotive controllers. The EPROM program memory makes customization of application programs fast and convenient. The EEPROM data memory is ideal for storing configuration information, access codes, serial numbers, and adaptive lookup tables. The small footprint packages available for through hole or surface mounting make MTA81010 perfect for applications with physical space limitations. Low-cost, low-power, high-performance, ease of use, I/O flexibility, and nonvolatile EEPROM memory makes the MTA81010 the microcontroller of choice for a wide variety of systems.

1.2 MTA81010 SERIES OVERVIEW

Depending on application and production requirements the proper device option can be selected using the table in this section. When placing orders, please use the "MTA81010 Product Identification System" on the back page of this data sheet to specify the correct part number.

1.2.1 ONE-TIME-PROGRAMMABLE (OTP) DEVICES

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates. OTP devices have the oscillator type pre-configured by the factory, and they are tested only for this special configuration (including voltage and frequency ranges, current consumption).

The program EPROM is erased, allowing the user to write the application code into it. In addition, the watchdog timer can be disabled, and/or the code protection logic can be activated by programming special EPROM fuses. The sixteen special EPROM bits for ID code storage are also user programmable.

1.2.2 QUICK-TURNAROUND-PRODUCTION (QTP) DEVICES

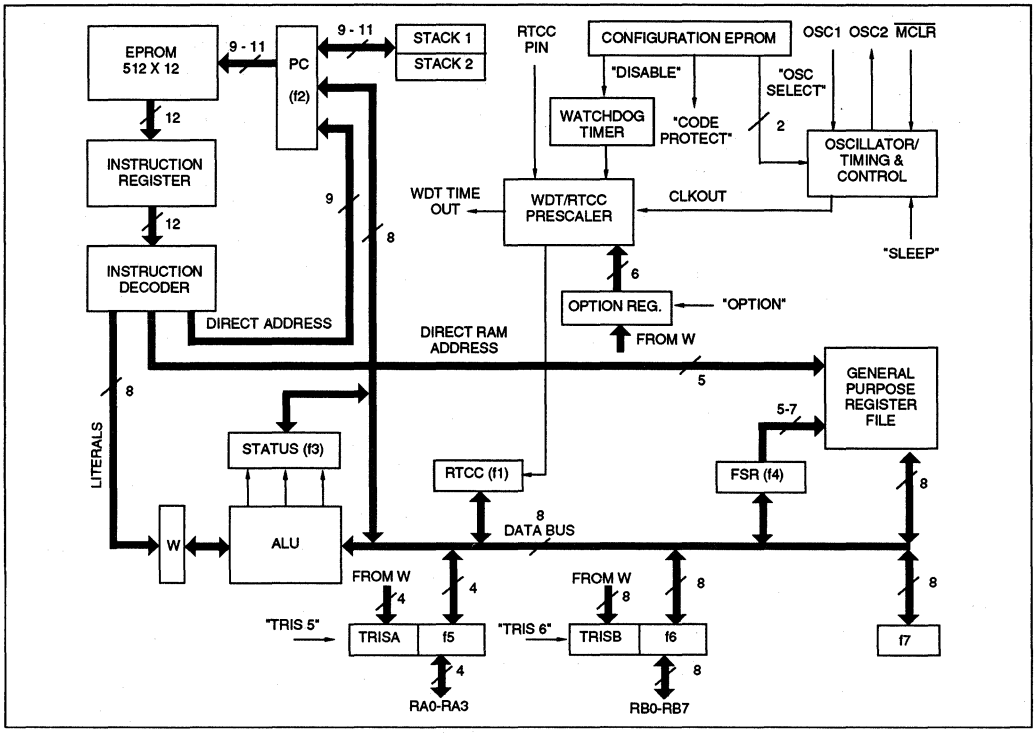
Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

TABLE 1.0.1 - OVERVIEW

Part #	EPROM	EEPROM	RAM*	I/O†	Package Options
MTA81010	512 x 12	128 x 8	32 x 8	13	28L PDIP (600 mil), 28L SOIC (300 mil)

* Including special function registers
† Includes RTCC pin.

FIGURE 2.1.1 - MTA81010 MICROCONTROLLER CHIP BLOCK DIAGRAM



2.0 MICROCONTROLLER SECTION

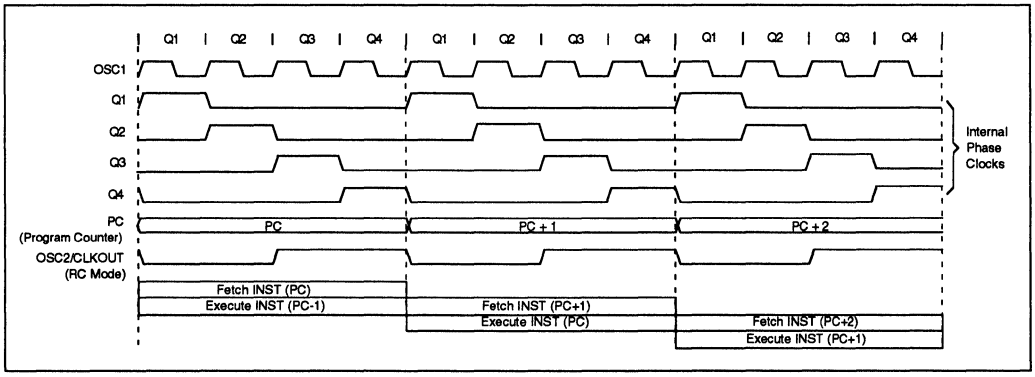
The MTA81010 from Microchip Technology contains low-cost, high-performance, 8-bit, fully static, EPROM-based CMOS microcontroller. It employs a RISC-like architecture with only 33 single word/single cycle instructions to learn. All instructions are single cycle except for program branches which take two cycles. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The MTA81010 product is equipped with special features that reduce system cost and power requirements. The power on reset and oscillator start up timer eliminate the need for external reset circuitry. There are three oscillator configurations to choose from, including power saving LP (Low Power) oscillator, standard XT oscillator and cost saving RC oscillator. Power saving SLEEP mode, watchdog timer and code protection features improves system cost, power and reliability.

TABLE 2.1.1 - MICROCONTROLLER PIN FUNCTIONS

Name	Function
RA0 - RA3	I/O PORT A
RB0 - RB7	I/O PORT B
RTCC	Real Time Clock/Counter
MCLR	Master Clear
OSC1	Oscillator (input)
OSC2/CLKOUT	Oscillator (output)
MCVDD	Power supply
VSS	Ground
N/C	No (internal) Connection

FIGURE 2.2.1 - CLOCKS/INSTRUCTION CYCLE



2.1 MICROCONTROLLER ARCHITECTURAL DESCRIPTION

2.1.1 HARVARD ARCHITECTURE

The MTA81XXX family microcomputers contain a, high-speed, fully static CMOS CPU with EPROM, RAM, and I/O on a single die.

The architecture is based on a register file concept with separate bus and memories for data and instructions (Harvard architecture). The data bus and memory (RAM) are 8 bits wide while the program bus and program memory (EPROM) have a width of 12 bits. This concept allows a simple yet powerful instruction set designed to emphasize bit, byte and register operations under high speed with overlapping instruction fetch and execution cycles. That means that, while one instruction is executed, the following instruction is already being read from the program memory. A block diagram of the microcontroller core is given in Figure 2.1.1.

2.1.2 CLOCKING SCHEME/INSTRUCTION CYCLE

The clock input (from pin OSC1) is internally divided by four to generate four non overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, PC is incremented every Q1, instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 2.2.1.

2.1.3 DATA REGISTER FILE

The 8-bit data bus connects two basic functional elements together: the Register File composed of 32 addressable 8-bit registers including the I/O Ports, and an 8-bit wide Arithmetic Logic Unit. The 32 bytes of RAM are directly addressable (Figure 3.2.1). Data can be addressed direct or indirect using the file select register (f4). Immediate data addressing is supported by special "literal" instructions which load data from program memory into the W register.

The register file is divided into two functional groups: operational registers and general purpose registers. The operational registers include the Real Time Clock Counter (RTCC) register, the Program Counter (PC), the Status Register, the I/O registers (PORTs), and the File Select Register. The general purpose registers are used for data and control information under command of the instructions.

In addition, special purpose registers are used to control the I/O port configuration, and the prescaler options.

2.1.4 ARITHMETIC/LOGIC UNIT (ALU)

The 8-bit wide ALU contains one temporary working register (W Register). It performs arithmetic and Boolean functions between data held in the W Register and any file register. It also does single operand operations on either the W register or any file register.

2.1.5 PROGRAM MEMORY

512 words of 12-bit wide on-chip program memory (EPROM) can be directly addressed (Figure 3.3.1). Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations, supporting direct, indirect, relative addressing modes, can be performed by Bit Test and Skip instructions, Call instructions, Jump instructions or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting.

3.0 OPERATIONAL REGISTER FILES

3.1 F0 INDIRECT DATA ADDRESSING

This is not a physically implemented register. Addressing f0 calls for the contents of the File Select Register to be used to select a file register. f0 is useful as an indirect address pointer. For example, in the instruction ADDWF f0, W will add the contents of the register pointed to by the FSR (f4) to the content of the W Register and place the result in W.

If f0 itself is read through indirect addressing (i.e. FSR = 0h), then 00h is read. If f0 is written to via indirect addressing, the result will be a NOP.

3.2 F1 REAL TIME CLOCK/COUNTER REGISTER (RTCC)

This register can be loaded and read by the program as any other register. In addition, its contents can be incremented by an external signal edge applied to the RTCC pin, or by the internal instruction cycle clock (CLKOUT=fosc/4). Figure 3.1.1 is a simplified block diagram of RTCC.

An 8-bit prescaler can be assigned to the RTCC by writing the proper values to the PSA bit and the PS bits in the OPTION register. OPTION register is a special register (not mapped in data memory) addressable using the 'OPTION' instruction. See Section 6.4 for details. If the prescaler is assigned to the RTCC, instructions writing to f1 (e.g. CLRF 1, or BSF1, 5, ...etc.) clear the prescaler.

The bit "RTS" (RTCC signal Source) in the OPTION register determines, if f1 is incremented internally or externally.

RTS=1: The clock source for the RTCC or the prescaler, if assigned to it, is the signal on the RTCC pin. Bit 4 of the OPTION register (RTE) determines if an increment occurs on the falling (RTE=1) or rising (RTE=0) edge of the signal presented to the RTCC pin.

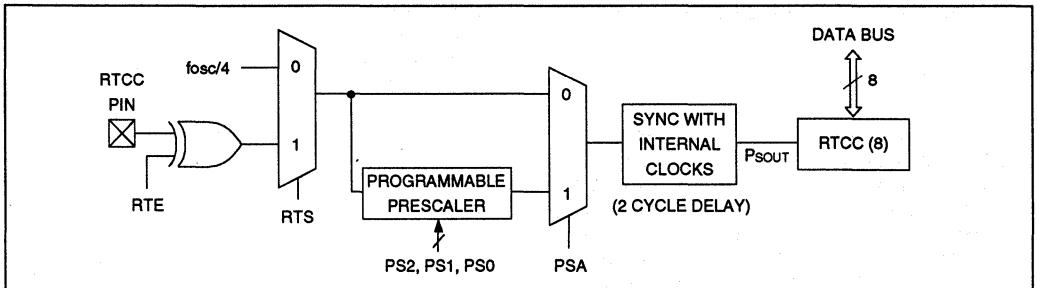
RTS=0: The RTCC register or its prescaler, respectively, will be incremented with the internal instruction clock (= Fosc/4). The "RTE" bit in the OPTION register and the RTCC pin are "don't care" in this case. However, the RTCC pin must be tied to VDD or VSS, whatever is convenient, to prevent unintended entering of test modes and to reduce the current consumption in low power applications.

As long as clocks are applied to the RTCC (from internal or external source, with or without prescaler), f1 keeps incrementing and just rolls over when the value "FFh" is reached. All increment pulses for f1 are delayed by two instruction cycles. After writing to f1, for example, no increment takes place for the following two instruction cycles. This is independent if internal or external clock source is selected. If a prescaler is assigned to the RTCC, the output of the prescaler will be delayed by two cycles before f1 is incremented. This is true for instructions that either write to or read-modify-write RTCC (e.g. MOVF f1, CLRF f1). For applications where RTCC needs to be tested for zero without affecting its count, use of MOVF f1, W instruction is recommended. Timing diagrams in Figure 3.2.2 show RTCC read, write and increment timing.

3.2.1 Using RTCC With External Clock

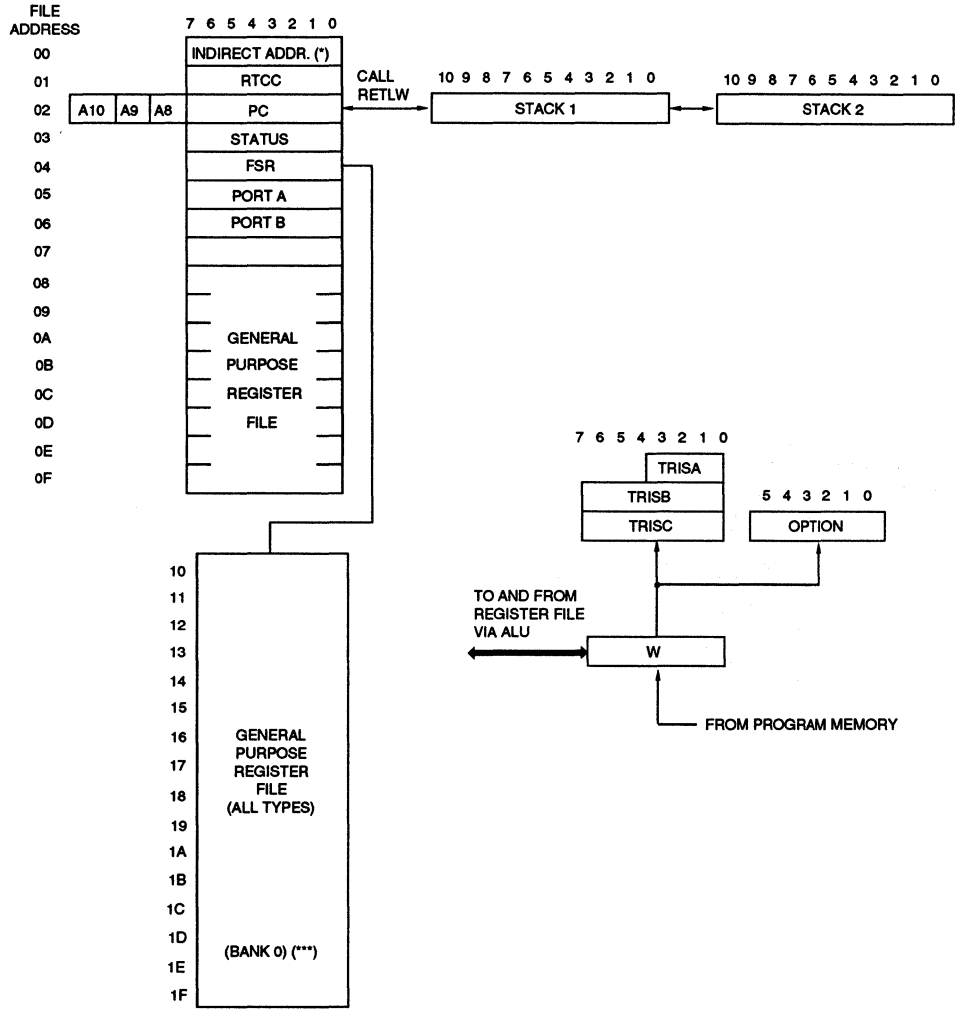
When external clock input is used for RTCC, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements. Also there is some delay from the occurrence of the external clock edge to the actual incrementing of RTCC. Referring to Figure 3.1.1, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where tosc = oscillator time period.

FIGURE 3.1.1 - RTCC BLOCK DIAGRAM (SIMPLIFIED)



Notes: 1. Bits RTE, RTS, PS2, PS1, PS0 are located in option register.
2. The prescaler is shared with Watchdog Timer (see Figure 8.0.1).

FIGURE 3.2.1 - MTA81010 MICROCONTROLLER DATA MEMORY MAP



(*) Not a physically implemented register. See Section 4.0 for details

4

When no prescaler is used, PSOUT (Prescaler output, see Figure 5) is the same as RTCC clock input and therefore the requirements are:

T_{RTH} = RTCC high time ≥ 2tosc + 20 ns

T_{RTL} = RTCC low time ≥ 2tosc + 20 ns

When prescaler is used, the RTCC input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.

Then: PSOUT high time = PSOUT low time = $\frac{N.T_{RT}}{2}$

where T_{RT} = RTCC input period and N = prescale value (2, 4, ..., 256). The requirement is, therefore $\frac{N.T_{RT}}{2} \geq$ 2 tosc + 20 ns, or $T_{RT} \geq \frac{4\ tosc + 40\ ns}{N}$.

The user will notice that no requirement on RTCC high time or low time is specified. However, if the high time or low time on RTCC is too small then the pulse may not be detected, hence a minimum high or low time of 10 ns is required. In summary, the RTCC input requirements are:

T_{RT} = RTCC period ≥ (4 tosc + 40 ns)/N

T_{RTH} = RTCC high time ≥ 10 ns

T_{RTL} = RTCC low time ≥ 10 ns

Delay from external clock edge: Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the RTCC is actually incremented. Referring to Figure 3.2.3, the reader can see that this delay is between 3 tosc and 7 tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±1 µs @ 4 MHz).

3.3 f2 PROGRAM COUNTER

The program counter generates the addresses for 512 x 12 on-chip EPROM cells containing the program instruction words (Figure 3.3.1).

The program counter and its associated two-level hardware stack is 9-bits wide.

The program counter is set to all "1"s upon a RESET condition. During program execution it is auto incremented with each instruction unless the result of that instruction changes the PC itself:

a) "GOTO" instructions allow the direct loading of the lower 9 program counter bits (PC <8:0>).

b) "CALL" instructions load the lower 8-bit of the PC directly while the ninth bit is cleared to "0". The PC value, incremented by one, will be pushed into the stack.

c) "RETLW" instructions load the program counter with the top of stack contents.

d) If PC is the destination in any instruction (e.g. MOVWF 2, ADDWF 2, or BSF 2,5) then the computed 8-bit result will be loaded into the low 8-bits of program counter. The ninth bit of PC will be cleared.

It should be noted that because bit 8 (ninth bit) of PC is cleared in CALL instruction or any instruction which writes to the PC (e.g. MOVWF 2), all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 3.2.2A - RTCC TIMING: INT CLOCK/NO PRESCALE

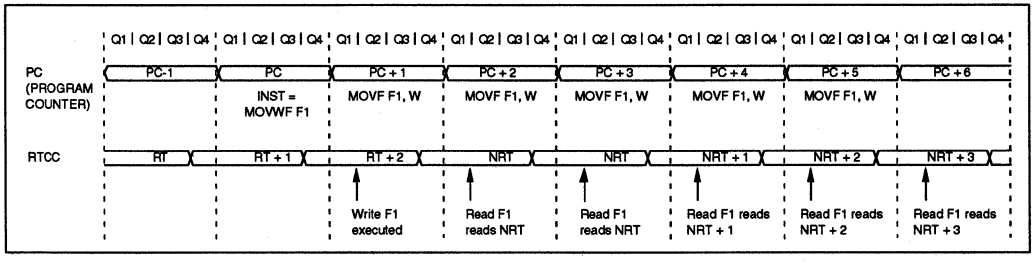
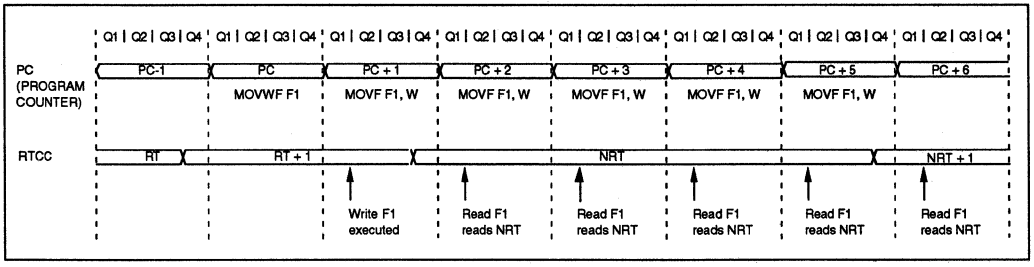


FIGURE 3.2.2B - RTCC TIMING: INT CLOCK/PRESCALE 1:2



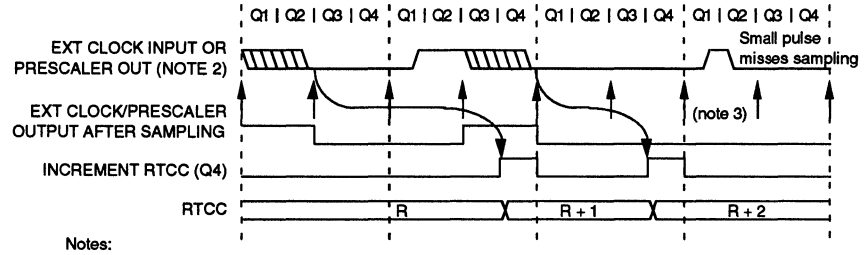
3.4 STACK

The MTA81010 series employs a two level hardware push/pop stack (Figure 3.3.1).

CALL instructions push the current program counter value, incremented by "1", into stack level 1. Stack level 1 is automatically pushed to level 2. If more than 2 subsequent "CALL"s are executed, only the most recent two return addresses are stored.

RETLW instructions load the contents of stack level 1 into the program counter while stack level 2 gets copied into level 1. If more than 2 subsequent "RETLW"s are executed, the stack will be filled with the address previously stored in level 2.

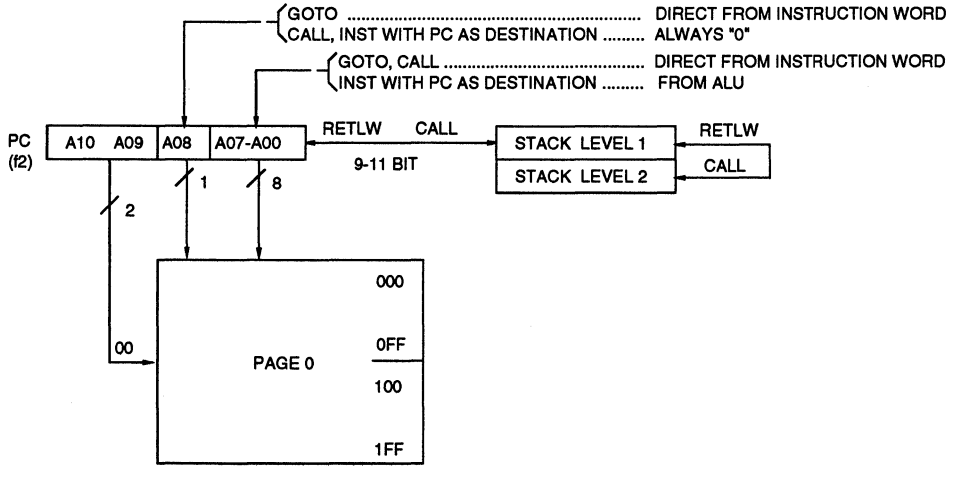
FIGURE 3.2.3 - RTCC TIMING WITH EXTERNAL CLOCK



Notes:

1. Delay from clock input change to RTCC increment is 3 tosc to 7 tosc. (Duration of Q = tosc). Therefore, the error in measuring the interval between two edges on RTCC input = ± 4 tosc max.
2. External clock if no prescaler selected, Prescaler output otherwise.
3. The arrows indicate the points in time where sampling occurs.

FIGURE 3.3.1 - PROGRAM MEMORY ORGANIZATION



3.5 f3 STATUS WORD REGISTER

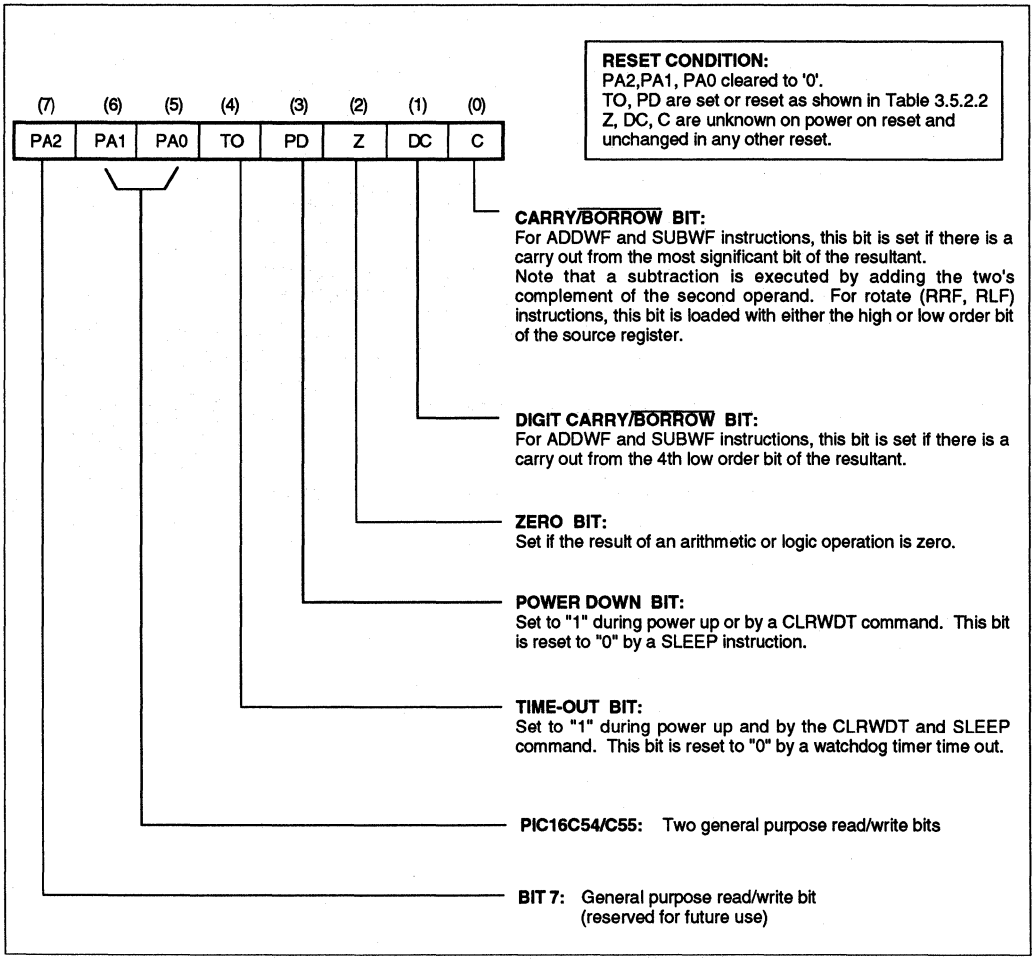
This register contains the arithmetic status of the ALU, the RESET status.

The status register (f3) can be destination for any instruction like any other register. However, the status bits are set after the following write. Furthermore, TO and PD bits are not writable. Therefore, the result of an instruction with status register as destination may be different than intended. For example, CLRF f3 will clear all bits except for TO and PD and then set the Z bit and leave status register as 000UU100 (where U = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the status registers because these instructions do not affect any status bit.

For other instructions, affecting any status bits, see section "Instruction Set Summary" (Table 9.0.1).

FIGURE 3.5.1 - STATUS WORD REGISTER f3



3.5.1 Carry/Borrow and Digit Carry/ Borrow Bits

The Carry bit (C) is a carry out in addition operation (ADDWF) and a borrow out in subtract operation (SUBWF).

It is also affected by RRF and RLF instructions. The following examples explain carry/borrow bit operation:

```
;SUBWF Example #1
;
clrf    0x20    ;f(20h)=0
movlw   1       ;wreg=1
subwf   0x20    ;f(20h)=f(20h)-wreg=0-1=FFh
                ;Carry=0: Result is negative
;
;SUBWF Example #2
movlw   0xFF    ;
movwf   0x20    ;f(20h)=FFh
clrw            ;wreg=0
subwf   0x20    ;f(20h)=f(20h)-wreg=FFh-0=FFh
                ;Carry=1: Result is positive
;
```

The digit carry operates in the same way as the carry bit, i.e. it is a borrow in subtract operation.

3.5.2 Time Out and Power Down Status Bits (TO, PD)

The "TO" and "PD" bits in the status register f3 can be tested to determine if a RESET condition has been caused by a watchdog timer time-out, a power-up condition, or a wake-up from SLEEP by the watchdog timer or MCLR pin.

These status bits are only affected by events listed in Table 3.5.2.1.

3.6 f4 FILE SELECT REGISTER (FSR)

Bits 0-4 select one of the 32 available file registers in the indirect addressing mode (that is, calling for file f0 in any of the file oriented instructions).

Bits 5-7 of the FSR are read-only and are always read as "one"s.

If no indirect addressing is used, the FSR can be used as a 5-bit wide general purpose register.

TABLE 3.5.2.1 - EVENTS AFFECTING PD/ TO STATUS BITS

Event	TO	PD	Remarks
Power-up	1	1	
WDT Time-out	0	X	No effect on PD
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Note: A WDT time-out will occur regardless of the status of the TO bit. A SLEEP instruction will be executed, regardless of the status of the PD bit. Table 3.5.2.2 reflects the status of PD and TO after the corresponding event.

TABLE 3.5.2.2 - PD/TO STATUS AFTER RESET

TO	PD	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT time-out (not during SLEEP)
1	0	MCLR wake-up from SLEEP
1	1	Power-up
X	X	= Low pulse on MCLR input

Note: The PD and TO bit maintain their status (X) until an event of Table 3.5.2.1 occurs. A low-pulse on the MCLR input does not change the PD and TO status bits.

4.0 I/O REGISTERS (PORTS)

The I/O registers can be written and read under program control like any other register of the register file. However, "read" instructions (e.g. MOVF 6,W) always read the I/O pins, regardless if a pin is defined as "input" or "output." Upon a RESET condition, all I/O ports are defined as "input" (= high impedance mode) as the I/O control registers (TRISA, TRISB) are all set to "ones."

The execution of a "TRIS f" instruction with corresponding "zeros" in the W-register is necessary to define any of the I/O pins as output.

4.1 f5 (PORT A)

4-bit I/O register. Low order 4 bits only are used (RA0 - RA3). Bit 4-7 are unimplemented and read as "zeros."

4.2 f6 (PORT B)

8-bit I/O register.

4.3 F7

General purpose register.

4.4 I/O INTERFACING

The equivalent circuit for an I/O port bit is shown in Figure 4.4.1. All ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g. MOVF 6, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB) must be set to zero. For use as an input, the corresponding TRIS bit must be "one". Any I/O pin can be programmed individually as input or output.

4.5 I/O PROGRAMMING CONSIDERATIONS

4.5.1 Bidirectional I/O Ports

a) Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of f6 (Port B) will cause all eight bits of f6 to be read into the CPU. Then the BSF operation takes place on bit 5 and f6 is re-output to the output latches. If another bit of f6 is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

b) A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

   For "wired-or" outputs (assuming negative logic), it is recommended to use external pull-up resistors on the corresponding pins. The pin should be left in high-impedance mode, unless a "0" has to be output. Thus, external devices can drive this pin "0" as well. "Wired-and" outputs can be realized in the same way, but with external pull-down resistors and only actively driving the "1" level from the PIC16C54. The resistor values are user selectable, but should not force output currents above the specified limits (see DC Characteristics).

4.5.2 Successive Operations on I/O Ports

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see Figure 4.5.2.1). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

4.5.3 Operation in Noisy Environment

In noisy application environments, such as keyboards which are exposed to ESD (Electro Static Discharge), register contents can get corrupted due to noise spikes.

The on-chip watchdog timer will take care of all situations involving program sequence "lockups." However, if an I/O control register gets corrupted, the program sequence may still be executed properly although an input pin may have switched unintentionally to an output. In this case, the program would always read the same value on this pin. This may result, for example, in a keyboard "lockup" situation without leading to a watchdog timer timeout. Thus, it is recommended to redefine all I/O pins in regular time intervals (inputs as well as outputs). The optimal strategy is to update the I/O control register every time before reading input data or writing output data.

FIGURE 4.4.1 - EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN

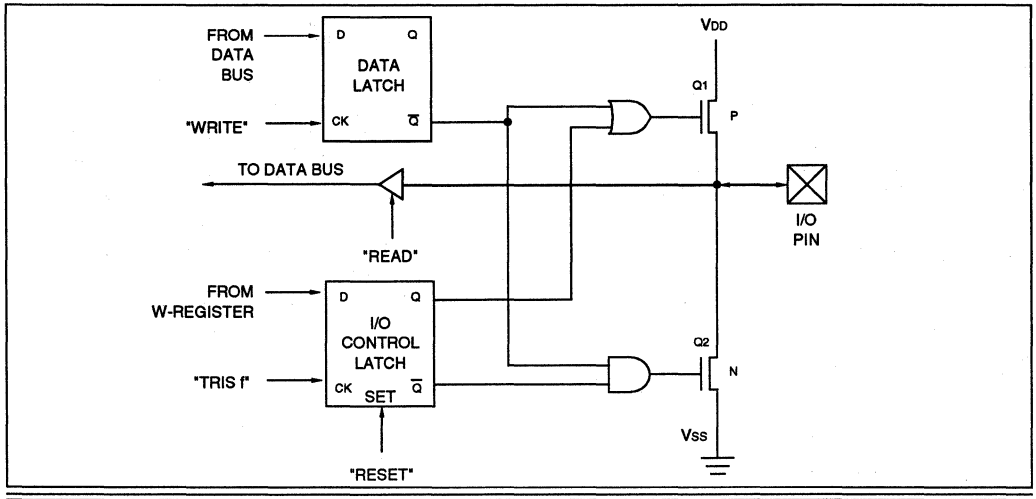
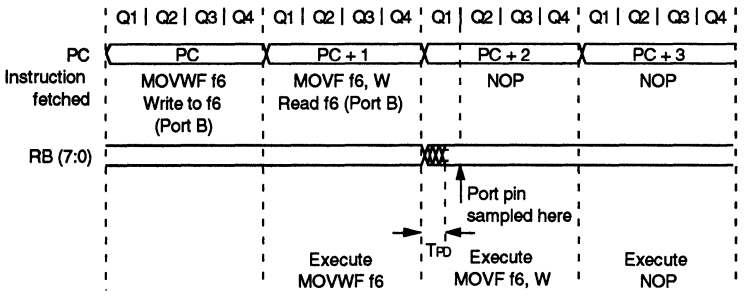


FIGURE 4.5.2.1 - I/O PORT READ/WRITE TIMING



Note:

This example shows write to port B followed by a read from port B. Note that the data setup time = (0.25 TCY - TPD) where TCY = instruction cycle. Therefore, at higher clock frequencies, write followed by a read may be problematic.

5.0 GENERAL PURPOSE REGISTERS

f08h - f1Fh: are general purpose register files.

6.0 SPECIAL PURPOSE REGISTERS

6.1 W WORKING REGISTER

Holds second operand in two operand instructions and/or supports the internal data transfer.

6.2 TRISA I/O CONTROL REGISTER FOR PORT A (F5)

Only bits 0-3 are available. The corresponding I/O port (f5) is only 4-bit wide.

6.3 TRISB I/O CONTROL REGISTER FOR PORT B (f6)

The I/O control registers will be loaded with the content of the W register by execution of the TRIS f instruction. A "1" in the I/O control register puts the corresponding I/O pin into a high impedance mode. A "0" puts the contents of file register f5 or f6, respectively, out on the selected I/O pins.

These registers are "write-only" and are set to all "ones" upon a RESET condition.

6.4 OPTION PRESCALER/RTCC OPTION REGISTER

Defines prescaler assignment (RTCC or WDT), prescaler value, signal source and signal edge for the RTCC. The OPTION register is "write-only" and is 6 bit wide.

By executing the "OPTION" instruction, the contents of the "W" register will be transferred to the option register. Upon a RESET condition, the option register is set to all "ones."

7.0 RESET CONDITION

A RESET condition can be caused by applying power to the chip (power-up), pulling the MCLR input "low", or by a Watchdog timer time-out. The device will stay in RESET as long as the oscillator start-up timer (OST) is active or the MCLR input is "low."

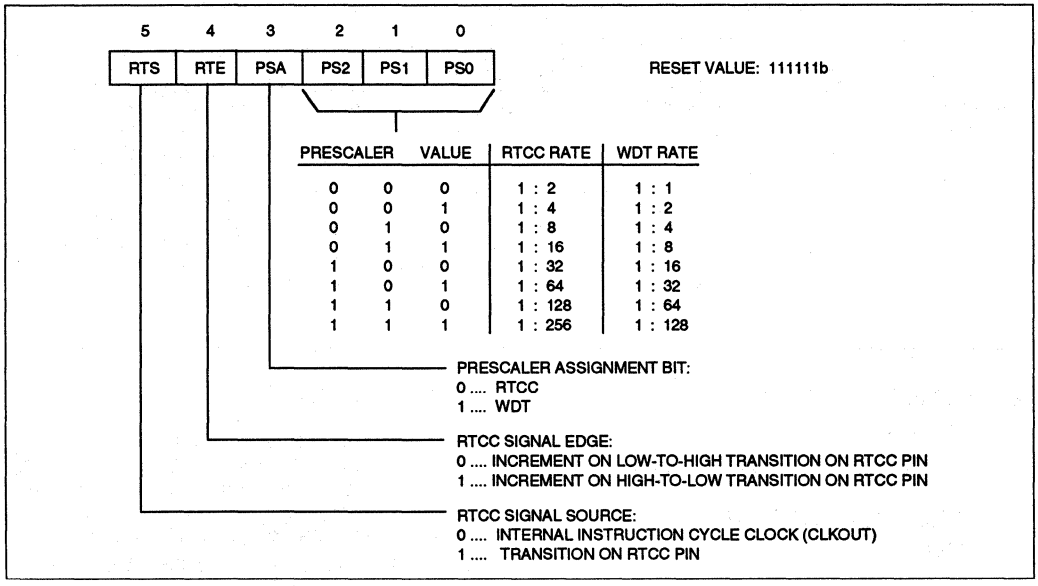
The oscillator start-up timer is activated as soon as MCLR input is sensed to be high. This implies that in case of power on reset with MCLR tied to VDD the OST starts from power-up. In case of WDT time-out, it will start at the end of the time-out (since MCLR is high). In case of MCLR reset, the OST will start when MCLR goes high. The nominal OST time-out period is 18 ms. See Section 12.0 for detailed information on OST and power on reset.

During a RESET condition the state of the PIC16C54 is defined as :

- The oscillator is running, or will be started (power-up or wake-up from SLEEP).
- All I/O port pins (RA0 - RA3, RB0 - RB7) are put into the high-impedance state by setting the "TRIS" registers to all "ones" (= input mode).
- The Program Counter is set to all "ones".
- The OPTION register is set to all "ones".
- The Watchdog Timer and its prescaler are cleared.
- The upper three bits (page select bits) in the Status Register (f3) are cleared to "zero."
- "RC" devices only: The "CLKOUT" signal on the OSC2 pin is held at a "low" level.

4

FIGURE 6.5.1 - OPTION REGISTER



8.0 PRESCALER

An 8-bit counter is available as a prescaler for the RTCC, or as a post-scaler for the watchdog timer, respectively (Figure 8.0.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the RTCC and the watchdog timer. Thus, a prescaler assignment for the RTCC means that there is no prescaler for the watchdog timer, and vice versa.

The PSA and PS0-PS2 bits in the OPTION register determine the prescaler assignment and pre-scale ratio.

When assigned to the RTCC, all instructions writing to the RTCC (e.g. CLRF 1, MOVWF 1, BSF 1,x ....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the watchdog timer.

8.1 SWITCHING PRESCALER ASSIGNMENT

CHANGING PRESCALER FROM RTCC TO WDT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence must be executed when changing the prescaler assignment from RTCC to WDT:

```
1. MOVLW  B'xx0x0xxx'   ; Select internal clock and select new
2. OPTION               ; prescaler value. If new prescale value
                        ; is = '000' or '001', then select any other
                        ; prescale value temporarily.

3. CLRF 1               ; Clear RTCC and prescaler.
4. MOVLW  B'xxxx1xxx'   ; Select WDT, do not change prescale
                        ; value.
5. OPTION               ;
6. CLRWDT               ; Clears WDT and prescaler.
7. MOVLW  B'xxxx1xxx'   ; Select new prescale value.
8. OPTION               ;
```

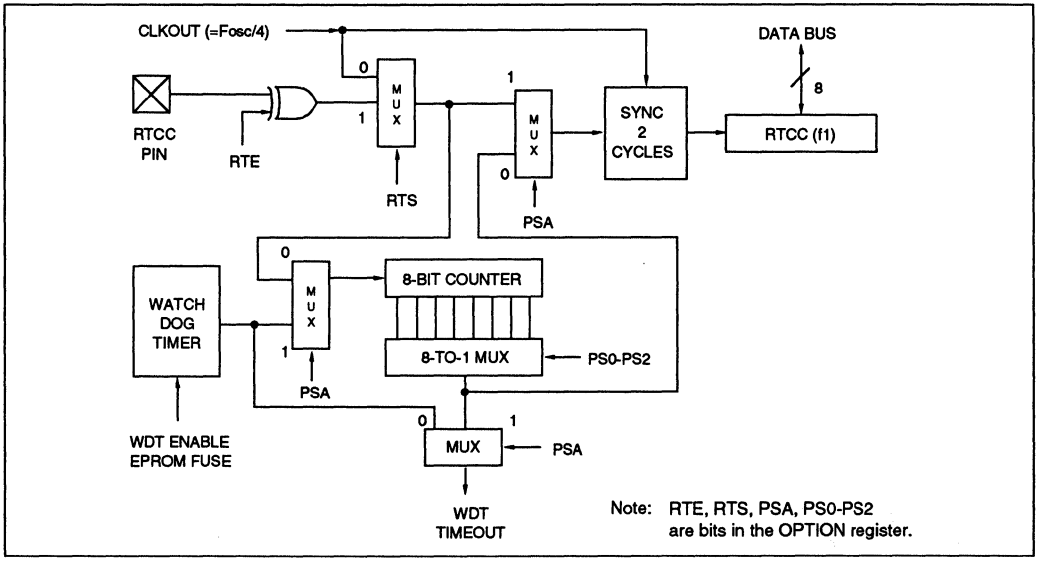
Steps 1 and 2 are only required if an external RTCC source is used. Steps 7 and 8 are necessary only if the desired prescale value is '000' or '001'.

CHANGING PRESCALER FROM WDT TO RTCC

To change prescaler from WDT to RTCC use the following sequence:

```
1. CLRWDT               ; Clear WDT and prescaler
2. MOVLW  B'xxxx0xxx'   ; Select RTCC, new prescale value
                        ; and clock source
3. OPTION               ;
```

FIGURE 8.0.1 - BLOCK DIAGRAM RTCC/WDT PRESCALER



9.0 BASIC INSTRUCTION SET SUMMARY

Each PIC16C54 instruction is a 12-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C54 instruction set summary in Table 9.0.1 lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the thirty-two PIC16C54 file registers is to be utilized by the instruction.

The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µs.

Notes to Table 9.0.1

Note 1: The 9th bit of the program counter will be forced to a "zero" by any instruction that writes to the PC (f2) except for GOTO (e.g. CALL, MOVWF 2 etc.). See Section 3.3 on page 8 for details.

Note 2: When an I/O register is modified as a function of itself (e.g. MOVF 6,1), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as output and is driven low by an external device, the data will be written back with a '0'.

Note 3: The instruction "TRIS f" , where f = 5 or 6 causes the contents of the W register to be written to the tristate latches of the specified file (port). A "one" forces the pin to a high impedance state and disables the output buffers.

Note 4: If this instruction is executed on file register f1 (and, where applicable, d=1), the prescaler will be cleared if assigned to the RTCC.

TABLE 9.0.1 - INSTRUCTION SET SUMMARY

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4 - 0)
OPCODE	d	f(FILE #)

d = 0 for destination W
d = 1 for destination f

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0001 11df ffff 1Cf	Add W and f	**ADDWF**	f, d	W + f → d	C,DC,Z	1,2,4
0001 01df ffff 14f	AND W and f	**ANDWF**	f, d	W & f → d	Z	2,4
0000 011f ffff 06f	Clear f	**CLRF**	f	0 → f	Z	4
0000 0100 0000 040	Clear W	**CLRW**	-	0 → W	Z	
0010 01df ffff 24f	Complement f	**COMF**	f, d	$\bar{f}$ → d	Z	2,4
0000 11df ffff 0Cf	Decrement f	**DECF**	f, d	f -1 → d	Z	2,4
0010 11df ffff 2Cf	Decrement f, Skip if Zero	**DECFSZ**	f, d	f - 1 → d, skip if zero	None	2,4
0010 10df ffff 28f	Increment f	**INCF**	f, d	f + 1 → d	Z	2,4
0011 11df ffff 3Cf	Increment f, Skip if zero	**INCFSZ**	f, d	f + 1 → d, skip if zero	None	2,4
0001 00df ffff 10f	Inclusive OR W and f	**IORWF**	f, d	W v f → d	Z	2,4
0010 00df ffff 20f	Move f	**MOVF**	f, d	f → d	Z	2,4
0000 001f ffff 02f	Move W to f	**MOVWF**	f	W → f	None	1,4
0000 0000 0000 000	No Operation	**NOP**	-	-	None	
0011 01df ffff 34f	Rotate left f	**RLF**	f, d	f(n) → d(n+1), C → d(0), f(7) → C	C	2,4
0011 00df ffff 30f	Rotate right f	**RRF**	f, d	f(n) → d(n-1), C → d(7), f(0) → C	C	2,4
0000 10df ffff 08f	Subtract W from f	**SUBWF**	f, d	f - W → d [f + $\overline{W}$ + 1 → d]	C,DC,Z	1,2,4
0011 10df ffff 38f	Swap halves f	**SWAPF**	f, d	f(0-3) ↔ f(4-7) → d	None	2,4
0001 10df ffff 18f	Exclusive OR W and f	**XORWF**	f, d	W ⊕ f → d	Z	2,4

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4 - 0)
OPCODE	b(BIT #)	f(FILE #)

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0100 bbbf ffff 4bf	Bit Clear f	**BCF**	f, b	0 → f(b)	None	2,4
0101 bbbf ffff 5bf	Bit Set f	**BSF**	f, b	1 → f(b)	None	2,4
0110 bbbf ffff 6bf	Bit Test f, Skip if Clear	**BTFSC**	f, b	Test bit (b) in file (f): Skip if clear	None	
0111 bbbf ffff 7bf	Bit Test f, Skip if Set	**BTFSS**	f, b	Test bit (b) in file (f): Skip if set	None	

LITERAL AND CONTROL OPERATIONS

(11-8)	(7 - 0)
OPCODE	k (LITERAL)

Instruction-Binary (Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
1110 kkkk kkkk Ekk	AND Literal and W	**ANDLW**	k	k & W→ W	Z	
1001 kkkk kkkk 9kk	Call subroutine	**CALL**	k	PC + 1 → Stack, k → PC	None	1
0000 0000 0100 004	Clear Watchdog timer	**CLRWDT**	-	0 → WDT (and prescaler, if assigned)	TO, PD	
101k kkkk kkkk Akk	Go To address (k is 9 bit)	**GOTO**	k	k → PC (9 bits)	None	
1101 kkkk kkkk Dkk	Incl. OR Literal and W	**IORLW**	k	k v W → W	Z	
1100 kkkk kkkk Ckk	Move Literal to W	**MOVLW**	k	k → W	None	
0000 0000 0010 002	Load OPTION register	**OPTION**	-	W → OPTION register	None	
1000 kkkk kkkk 8kk	Return, place Literal in W	**RETLW**	k	k → W, Stack → PC	None	
0000 0000 0011 003	Go into standby mode	**SLEEP**	-	0 → WDT, stop oscillator	TO, PD	
0000 0000 0fff 00f	Tristate port f	**TRIS**	f	W→ I/O control register f	None	3
1111 kkkk kkkk Fkk	Excl. OR Literal and W	**XORLW**	k	k ⊕ W → W	Z	

Notes: See previous page

9.1 INSTRUCTION DESCRIPTION

ADDWF ADD W to f

Syntax: ADDWF f,d

Encoding:

0001	11df	ffff

Words: 1

Cycles: 1

Operation: (W + f) → d

Status bits: C, DC, Z

Description: Add the contents of the W register to register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

ANDLW AND Literal and W

Syntax: ANDLW k

Encoding:

1110	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .AND. k) → W

Status bits: Z

Description: The contents of W register are AND'ed with the eight bit literal "k". The result is placed in the W register.

ANDWF AND W with f

Syntax: ANDWF f,d

Encoding:

0001	01df	ffff

Words: 1

Cycles: 1

Operation: (W .AND. f) → d

Status bits: Z

Description: AND the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

BCF Bit Clear f

Syntax: BCF f,b

Encoding:

0100	bbbf	ffff

Words: 1

Cycles: 1

Operation: 0 → f(b)

Status bits: None

Description: Bit "b" in register "f" is reset to 0.

BSF Bit Set f

Syntax: BSF f,b

Encoding:

0101	bbbf	ffff

Words: 1

Cycles: 1

Operation: 1 → f(b)

Status bits: None

Description: Bit "b" in register "f" is set to 1.

BTFSC Bit Test, skip if Clear

Syntax: BTFSC f,b

Encoding:

0110	bbbf	ffff

Words: 1

Cycles: 1(2)

Operation: skip if f(b) = 0

Status bits: None

Description: If bit "b" in register "f" is "0" then the next instruction is skipped.

If bit "b" is "0", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

BTFSS Bit Test, skip if Set

Syntax: BTFSS f,b

Encoding:

0111	bbbf	ffff

Words: 1

Cycles: 1 (2)

Operation: skip if f(b) = 1

Status bits: None

Description: If bit "b" in register "f" is "1" then the next instruction is skipped.

If bit "b" is "1", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

CALL Subroutine Call

Syntax: CALL k

Encoding:

1001	kkkk	kkkk

Words: 1

Cycles: 2

Operation: PC + 1 → TOS; k → PC<7:0>, '0' → PC<8>, PA2, PA1, PA0 → PC<11:9>;

Status bits: None

4

Description: Subroutine call. First, return address (PC + 1) is pushed into the stack. The eight bit value is loaded into PC bits <7:0>. PC bit 9 is cleared. PC<2:0> bits are loaded into PC <11:9>. CALL is a two cycle instruction.

CLRF Clear f and Clear d

Syntax: CLRF f,d

Encoding:	0000	011f	ffff

Words: 1

Cycles: 1

Operation: 00h → f, 00h → d

Status bits: None

Description: The contents of register "f" are set to 0. If "d" is 0 the contents of both data memory location "f" and W register are set to 0. If "d" is 1 the only contents of register "f" are set to 0.

CLRW Clear W Register

Syntax: CLRW

Encoding:	0000	0100	0000

Words: 1

Cycles: 1

Operation: 00h →W

Status bits: Z

Description: W registered is cleared. Zero bit (Z) is set.

CLRWDT Clear Watchdog Timer

Syntax: CLRWDT

Encoding:	0000	0000	0100

Words: 1

Cycles: 1

Operation: 00h →WDT, 0 → WDT prescaler,

Status bits: 1 → TO, 1 → PD

Description: CLRWDT instruction resets the watchdog timer. It also resets the prescaler of the WDT. Status bits TO and PD are set.

COMF Complement f

Syntax: COMF f,d

Encoding:	0010	01df	ffff

Words: 1

Cycles: 1

Operation: $\overline{f}$ → d

Status bits: Z

Description: The contents of register "f" are complemented. If "d" is 0 the result is stored in W. If "d" is 1 the result is stored back in register "f".

DECF Decrement f

Syntax: DECF f,d

Encoding:	0000	11df	ffff

Words: 1

Cycles: 1

Operation: (f-1) → d

Status bits: C, DC, Z

Description: Decrement register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

DECFSZ Decrement f, skip if 0

Syntax: DECFSZ f,d

Encoding:	0010	11df	ffff

Words: 1

Cycles: 1 (2)

Operation: (f - 1) → d; skip if result = 0

Status bits: None

Description: The contents of register "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f". If the result is 0 the next instruction is skipped.

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

GOTO Unconditional Branch

Syntax: GOTO k

Encoding:	101k	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → PC<8:0>, PA2, PA1, PA0

→ PC<11:9>;

Status bits: None

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH <4:3>. GOTO is a two cycle instruction.

INCF Increment f

Syntax: INCF f,d

Encoding:	0010	10df	ffff

Words: 1

Cycles: 1

Operation: (f + 1) → d

Status bits: C, DC, Z

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

INCFSZ Increment f, skip if 0

Syntax: INCFSZ f,d

Encoding:

0011	11df	ffff

Words: 1

Cycles: 1 (2)

Operation: (f + 1) → d, skip if result = 0

Status bits: None

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f". If the result is 0 the next instruction is skipped.

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

IORLW Inclusive OR Literal with W

Syntax: IORLW k

Encoding:

1101	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .OR. k) → W

Status bits: Z

Description: The contents of the W register are OR'ed with the eight bit literal "k". The result is placed in the W register.

IORWF Inclusive OR W with f

Syntax: IORWF f,d

Encoding:

0001	00df	ffff

Words: 1

Cycles: 1

Operation: (W .OR. f) → d

Status bits: Z

Description: Inclusive OR the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

MOVF Move f

Syntax: MOVF f,d

Encoding:

0010	00df	ffff

Words: 1

Cycles: 1

Operation: (f) → d

Status bits: Z

Description: The contents of register "f" are moved. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

MOVLW Move Literal to W

Syntax: MOVLW k

Encoding:

1100	kkkk	kkkk

Words: 1

Cycles: 1

Operation: k → W

Status bits: None

Description: The eight bit literal "k" is loaded into W register.

MOVWF Move W to f

Syntax: MOVWF f

Encoding:

0000	001f	ffff

Words: 1

Cycles: 1

Operation: W → f

Status bits: None

Description: Move data from W register to register "f".

NOP No Operation

Syntax: NOP

Encoding:

0000	0000	0000

Words: 1

Cycles: 1

Operation: No operation

Status bits: None

Description: No operation

OPTION Load Option Register

Syntax: OPTION

Encoding:

0000	0000	0010

Words: 1

Cycles: 1

Operation: W → OPTION;

Status bits: None

Description: The contents of the W register is loaded in the OPTION register.

RETLW Return Literal to W

Syntax: RETLW k

Encoding:	1000	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → W; TOS → PC;

Status bits: None

Description: The W register is loaded with the eight bit literal "k". The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

RLF Rotate Left f through Carry

Syntax: RLF f,d

Encoding:	0011	01df	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n+1>, f<7> → C, C → d<0>;

Status bits: C

Description: The contents of register "f" are rotated one bit to the left through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is stored back in register "f".

RRF Rotate Right f through Carry

Syntax: RRF f,d

Encoding:	0011	00df	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n-1>, f<0> → C, C → d<7>;

Status bits: C

Description: The contents of register "f" are rotated one bit to the right through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

SLEEP

Syntax: SLEEP

Encoding:	0000	0000	0011

Words: 1

Cycles: 1

Operation: 0 → PD, 1 → TO;
00h → WDT, 0 → WDT prescaler;

Status bits: TO, PD

Description: The power down status bit (PD) is cleared. Time-out status bit (TO) is set. Watchdog Timer and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP mode for more details.

SUBWF Subtract W from f

Syntax: SUBWF f,d

Encoding:	0000	10df	ffff

Words: 1

Cycles: 1

Operation: (f-W) → d

Status bits: C, DC, Z

```
;SUBWF Example #1
;
clrf   0x20   ;f(20h)=0
movlw  1      ;wreg=1
subwf  0x20   ;f(20h)=f(20h)-wreg=0-1=FFh
              ;Carry=0; Result is negative
;
;SUBWF Example #2
;
movlw 0xFF    ;
movwf 0x20    ;f(20h)=FFh
clrw          ;wreg=0
subwf 0x20    ;f(20h)=f(20h)-wreg=FFh-
0=FFh
              ;Carry=1:Result is positive
;
```

Description: Subtract (2's complement method) the W register from register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

SWAPF Swap f

Syntax: SWAPF f,d

Encoding:	0011	10df	ffff

Words: 1

Cycles: 1

Operation: f<0:3> → d<4:7>, f<4:7> → d<0:3>;

Status bits: None

Description: The upper and lower nibbles of register "f" are exchanged. If "d" is 0 the result is placed in W register. If "d" is 1 the result is placed in register "f".

TRIS Load TRIS Register

Syntax: TRIS f

Encoding:	0000	0000	0fff

Words: 1

Cycles: 1

Operation: W → TRIS register f;

Status bits: None

Description: TRIS register f (f = 5, 6 or 7) is loaded with the contents of the W register.

XORLW Exclusive OR literal with W

Syntax: XORLW k

Encoding:

1111	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .XOR. k) → W

Status bits: Z

Description: The contents of the W register are XOR'ed with the eight bit literal "k". The result is placed in the W register.

XORWF Exclusive OR W with f

Syntax: XORWF f,d

Encoding:

0001	10df	ffff

Words: 1

Cycles: 1

Operation: (W .XOR. f) → d

Status bits: Z

Description: Exclusive OR the contents of the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

10.0 WATCHDOG TIMER (WDT)

The watchdog timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1/OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by programming a "zero" into a special EPROM fuse which is not part of the normal program memory EPROM. The development tools provide special commands to program this fuse.

10.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.5 seconds can be realized.

The "CLRWDT" and "SLEEP" instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit "TO" in file register f3 will be cleared upon a watchdog timer timeout.

The WDT period is a function of the supply voltage, operating temperature, and will also vary from unit to unit due to variations in the manufacturing process. Please refer to the graphs in Section 17.0 and DC specs for more details.

10.2 WDT PROGRAMMING CONSIDERATIONS

In a noisy application environment the OPTION register can get corrupted. The OPTION register should be updated at regular intervals.

It should also be taken in account that under worst case conditions (VDD = Minimum, Temperature = Maximum, maximum WDT prescaler) it may take several seconds before a WDT timeout occurs.

11.0 OSCILLATOR CIRCUITS

11.1 OSCILLATOR TYPES

The MTA81010 series is available with three different oscillator options. On OTP and QTP devices, the oscillator configuration is programmed by the factory and the parts are tested only to the according specifications.

11.2 CRYSTAL OSCILLATOR

The MTA81010, -XT, or LP needs a crystal or ceramic resonator connected to the OSC1 and OSC2 pins to establish oscillation (Figure 11.2.1). XT = Standard crystal oscillator, LP = low power crystal oscillator. The series resistor Rs may be required in XT mode with AT strip-cut type crystals to avoid overdriving.

11.3 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 11.3.1 shows how the R/C combination is connected to the MTA81010. For Rext values below 2.2 kOhm, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 5 kOhm and 100 kOhm.

Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

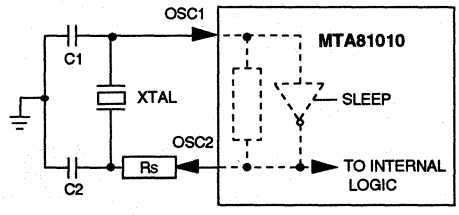
4

See Table 17.0.1 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characteristics in Section 17.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 2.2.1 for timing).

FIGURE 11.2.1 - CRYSTAL OPERATION (OR CERAMIC RESONATOR) XT OR LP TYPES ONLY)



Rs may be required in XT mode for AT strip-cut crystals to avoid overdriving. See Tables 11.2.1 and 11.2.2 for recommended values of C1, C2 per oscillator type and frequency.

TABLE 11.2.1 - CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	150 - 330 pF
	2.0 MHz	20 - 330 pF
	4.0 MHz	20 - 330 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

FIGURE 11.2.2 - EXTERNAL CLOCK INPUT OPERATION (XT OR LP TYPES ONLY)

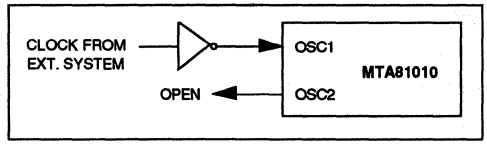


TABLE 11.2.2 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	15 pF	15 pF
XT	100 KHz	15 - 30 pF	200 - 300 pF
	200 KHz	15 - 30 pF	100 - 200 pF
	455 KHz	15 - 30 pF	15 - 100 pF
	1 MHz	15 - 30 pF	15 - 30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

FIGURE 11.3.1 - RC OSCILLATOR (RC TYPE ONLY)

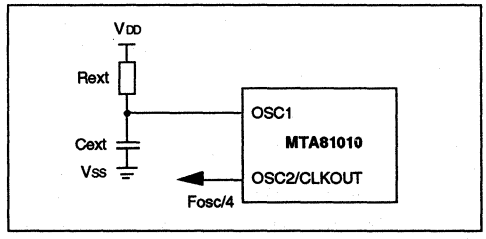
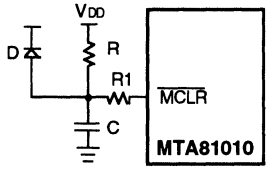


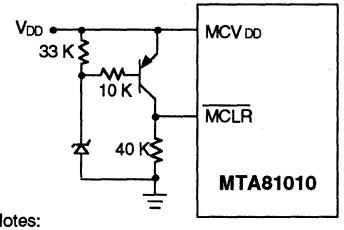
FIGURE 12.1.1 - EXTERNAL POWER ON RESET CIRCUIT



Notes:

1. External power on reset circuit is required only if VDD power-up slope is too slow or if a low frequency crystal oscillator is being used that need a long start-up time. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40 KΩ must be observed to make sure that voltage drop across R does not exceed 0.2 V (maximum leakage current specification on MCLR pin is 5 μA). A larger voltage drop will degrade VIH level on MCLR pin.
3. R1= 100Ω to 1KΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to ESD or EOS.

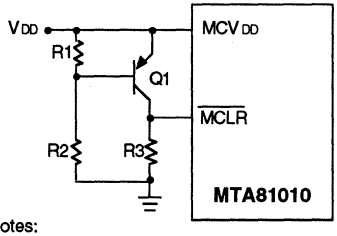
FIGURE 12.1.2 - BROWN OUT PROTECTION CIRCUIT



Notes:

1. This circuit will activate reset when VDD goes below (VZ + 0.7 V) where VZ = Zener voltage.

FIGURE 12.1.3 - BROWN OUT PROTECTION CIRCUIT



Notes:

1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$VDD \bullet \frac{R1}{R1 + R2} = 0.7\ V.$$

12.0 OSCILLATOR START-UP TIMER (OST)

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. An on-chip oscillator start-up timer is provided which keeps the device in a RESET condition for approximately 18 ms after the voltage on the MCLR pin has reached a logic high (VIHMC) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The OST will also be triggered upon a watchdog timer timeout. This is particularly important for applications using the WDT to awake the MTA81010 from SLEEP mode automatically.

The OST is not adequate for low frequency crystals which require much longer than 18 ms to start up and stabilize.

12.1 POWER ON RESET (POR)

The MTA81010 incorporates an on chip Power On Reset (POR) circuitry which provides internal chip reset for most power-up situations. To use this feature the user merely needs to tie MCLR pin to MCVDD. A simplified block diagram of the on-chip power on reset circuit is shown in Figure 12.1.4. The power on reset circuit and the oscillator start-up timer circuit are closely related. On power-up the reset latch is set and the start-up timer (see Figure 12.1.4) is reset. The start-up timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will reset the reset-latch and thus end the on-chip reset signal.

Figures 12.1.5 and 12.1.6 are two power-up situations with relatively fast rise time on MCVDD. In Figure 12.1.5, MCVDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset TOST ms after MCLR goes high. In Figure 12.1.6, the on chip power-on reset feature is being utilized (MCLR and MCVDD are tied together). The MCVDD is stable before the start-up timer times out and there is no problem in getting a proper reset. Figure 12.1.7 depicts a potentially problematic situation where MCVDD rises too slowly. In this situation, when the start-up timer times out, MCVDD has not reached the MCVDD (minimum) value and the chip is therefore not guaranteed to function correctly.

To summarize, the on chip power-on reset is guaranteed to work if the rate of rise of MCVDD is no slower than 0.05 V/ms. It is also necessary that the MCVDD starts from 0V. The on chip power on reset is also not adequate for low frequency crystals which require much longer than 18 ms to start up and stabilize. For such situations, we recommend that external RC circuits are used for longer power on reset.

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FIGURE 12.1.4 - SIMPLIFIED POWER ON RESET BLOCK DIAGRAM

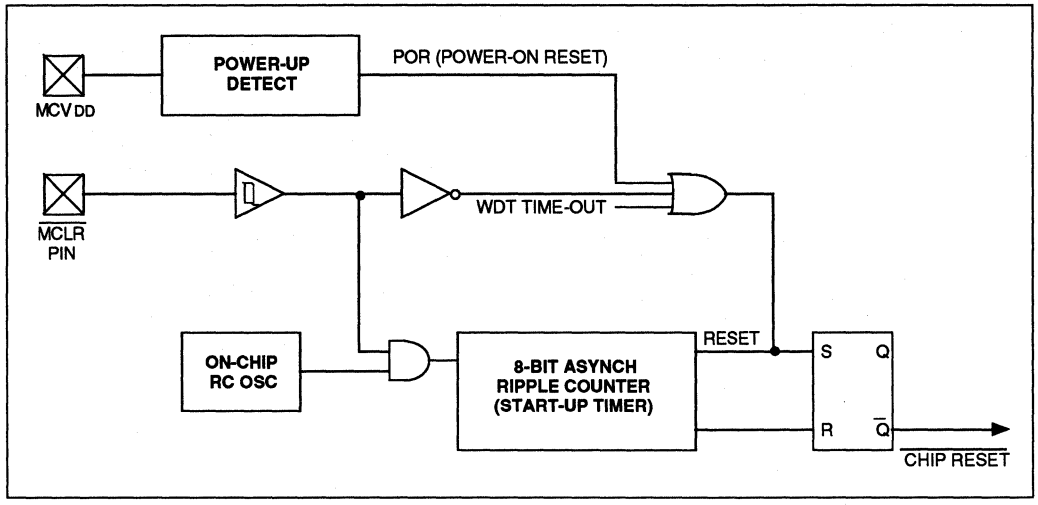
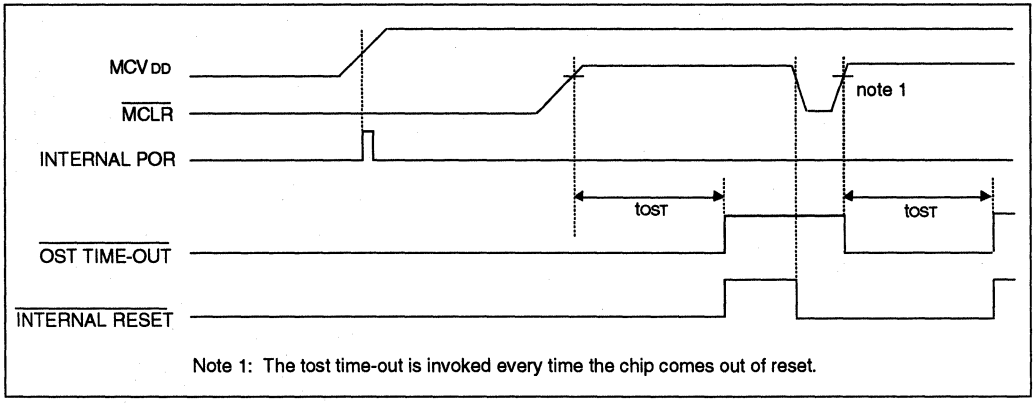


FIGURE 12.1.5 - USING EXTERNAL RESET INPUT



Note 1: The tost time-out is invoked every time the chip comes out of reset.

FIGURE 12.1.6 - USING ON-CHIP POR (FAST VDD RISE TIME)

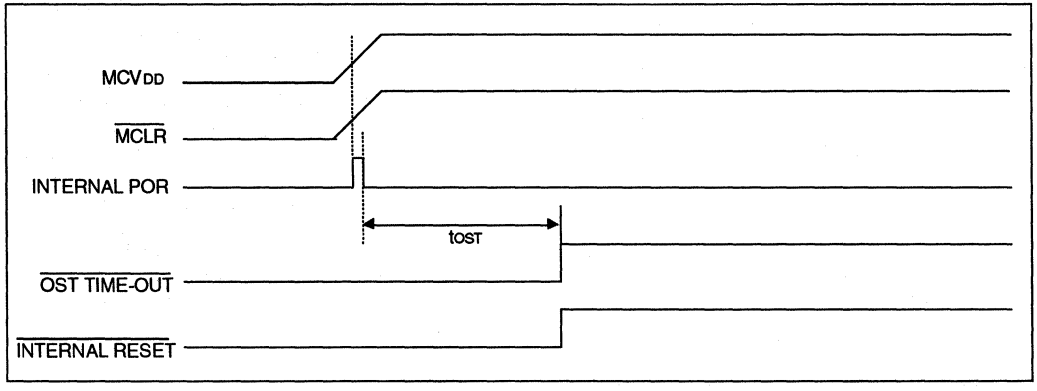
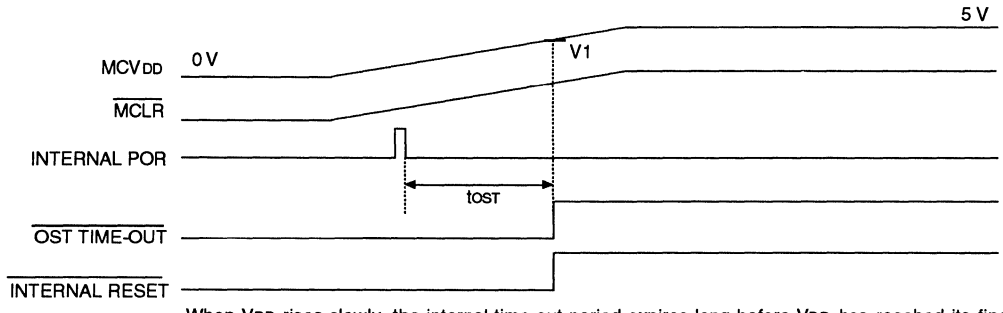


FIGURE 12.1.7 - USING ON-CHIP POR (SLOW VDD RISE TIME)



When VDD rises slowly, the internal time-out period expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1≥ VDDMIN.

13.0 POWER DOWN MODE (SLEEP)

The power down mode is entered by executing a SLEEP instruction.

If enabled, the watchdog timer will be cleared but keeps running, the bit "PD" in the status register (f3) is cleared, the "TO" bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are in the High-Z mode should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC input should also be at VDD or VSS for lowest current consumption.

The MCLR pin must be at VIHMC.

13.1 WAKE-UP

The device can be awakened by a watchdog timer timeout (if it is enabled) or an externally applied "low" pulse at the MCLR pin. In both cases the PIC16C54 will stay in RESET mode for one oscillator start-up timer period (triggered from rising edge on MCLR or WDT timeout) before normal program execution resumes.

The "PD" bit in the STATUS register, which is set to one during power on, but cleared by the "SLEEP" command, can be used to determine if the processor was powered up or awakened from the power down mode (Table 3.5.1.2). The TO bit in the Status register can be used to determine if the "wake up" was caused by an external MCLR signal or a watchdog timer time out.

NOTE: Some applications may require external R/C networks on the MCLR pin in order to allow for oscillator start-up times longer than one OST period. In this case, a WDT wake up from power down mode is not recommended, because a RESET generated by a WDT time out does not discharge the external capacitor, and the PIC16C54 will be in RESET only for the oscillator start-up timer period.

14.0 CONFIGURATION FUSES

The configuration EPROM consists of four EPROM fuses which are not part of the normal EPROM for program storage.

Two are for the selection of the oscillator type, one is the watchdog timer enable fuse, and one is the code protection fuse.

OTP or QTP devices have the oscillator configuration programmed by the factory and the parts are tested accordingly. The packages are marked with the suffixes "XT", "RC" or "LP" following the part number to identify the oscillator type and operating range.

14.1 CUSTOMER ID CODE

The MTA81010 series has 16 special EPROM bits which are not part of the normal program memory. These bits are available to the user to store an identifier (ID) code, checksum, or other informative data. They cannot be accessed during normal program execution. Programmers designed for the MTA81010 provide special commands to read or write these ID bits.

14.2 CODE PROTECTION

The program code written into the EPROM can be protected by programming the code protection fuse with "0".

When code protected, the contents of the program EPROM cannot be read out in a way that the program code can be reconstructed. In addition, all memory locations starting at 040h and above are protected against programming.

It is still possible to program locations 000h - 03Fh, the ID locations and the configuration fuses.

Note that the configuration fuses and the ID bits can still be read, even if the code protection logic is active.

14.2.1 Verifying a Code-protected PIC16C54

When code protected verifying any program memory location will read a scrambled output which looks like "00000000XXXX" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

a. First, program and verify a good device without code protecting it.

b. Next, blow its code protection fuse and then load its contents in a file.

c. Verify any code-protected PIC16C54 against this file.

15.0 MICROCONTROLLER ELECTRICAL CHARACTERISTICS

15.1 ABSOLUTE MAXIMUM RATINGS*

Ambient temperature under bias .. .-55°C to +125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss (except VDD and $\overline{MCLR}$) ..... -0.6V to VDD +0.6V
Voltage on VDD with respect to Vss ..... 0 to +9.5V
Voltage on $\overline{MCLR}$ with respect to Vss (Note 2) ..... 0 to +14V
Total power Dissipation (Note 1) ..... 800 mW
Maximum Current out of Vss pin ..... 150 mA
Maximum Current into VDD pin ..... 50 mA
Maximum Current into an input pin .....±500 µA
Maximum Output Current sinked by any I/O pin ..... 25 mA
Maximum Output Current sourced by any I/O pin ..... 20 mA
Maximum Output Current sourced by a single I/O port (Port A or B) ..... 40 mA
Maximum Output Current sinked by a single I/O port (Port A or B) ..... 50 mA

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes:

1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:

   $Pdis = V_{DD} \times \{I_{DD} - \sum I_{oh}\} + \sum \{(V_{DD}-V_{oh}) \times I_{oh}\} + \sum(V_{ol} \times I_{ol})$

2. Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low' level to the $\overline{MCLR}$ pin rather than pulling this pin directly to Vss.

TABLE 15.2 - MICROCONTROLLER PIN DESCRIPTIONS

Name	Function	Observation
RA0 - RA3	I/O PORT A	4 input/output lines
RB0 - RB7	I/O PORT B	8 input/output lines
RTCC	Real Time Clock/Counter	Schmitt Trigger Input
		Clock input to RTCC register. Must be tied to Vss or VDD if not in use to avoid unintended entering of test modes and to reduce current consumption
$\overline{MCLR}$	Master Clear	Schmitt Trigger Input
		A "Low" voltage on this input generates a RESET condition for the MTA81010 microcontroller
		A rising voltage triggers the on-chip oscillator start-up timer which keeps the chip in RESET mode for about 18ms. This input must be tied directly, or via a pull-up resistor, to VDD
OSC1	Oscillator (input)	"XT" and "LP" devices: Input terminal for crystal, ceramic resonator, or external clock generator
		"RC" devices: Driver terminal for external RC combination to establish oscillation
OSC2/CLKOUT	Oscillator (output)	For "XT" and "LP" devices: Output terminal for crystal and ceramic resonator. Do not connect any other load to this output. Leave open if external clock generator is used
		For "RC" devices : A "CLKOUT" signal with a frequency of 1/4 Fosc1 is put out on this pin
MCVDD	Power supply	
Vss	Ground	
N/C	No (internal) Connection	

15.3 MICROCONTROLLER DC CHARACTERISTICS: MTA81010-RC, XT, LP (COMMERCIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions Operating temperature 0 ≤ TA ≤ +70°C, unless otherwise stated Operating voltage VDD = 3.0V to 5.5V unless otherwise stated					
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage						
MTA81010-XT	VDDxt	3.0		6.25	V	Fosc = DC to 4 MHz
MTA81010-RC	VDDrc	3.0		6.25	V	Fosc = DC to 4 MHz
MTA81010-LP	VDDlp	2.5		6.25	V	Fosc = DC to 40 KHz
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See Section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See Section 13.1 for details on power on
Supply Current (Note 2)						
MTA81010-XT	IDDxt		1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
MTA81010-RC (Note 5)	IDDrc		1.8	3.3	mA	Fosc = 4 MHz , VDD = 5.5V
MTA81010-LP	IDDlp		15	32	µA	Fosc = 32 KHz, VDD=3.0V, WDT disabled
Power Down Current (Note 4)						
MTA81010	IPD1		4	12	µA	VDD = 3.0V, WDT enabled
	IPD2		0.6	9	µA	VDD = 3.0V, WDT disabled

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

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15.4 MICROCONTROLLER DC CHARACTERISTICS: MTA81010I-RC, XT, LP (INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS		Standard Operating Conditions Operating temperature -40 ≤ TA ≤ +85°C, unless otherwise stated Operating voltage VDD = 3.5V to 5.5V unless otherwise stated				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage						
MTA81010-XT	VDDxt	3.0		6.25	V	Fosc = DC to 4 MHz
MTA81010-RC	VDDrc	3.0		6.25	V	Fosc = DC to 4 MHz
MTA81010-LP	VDDlp	2.5		6.25	V	Fosc = DC to 40 KHz
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See Section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See Section 13.1 for details on power on reset
Supply Current (Note 2)						
MTA81010-XT	IDDxt		1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
MTA81010-RC (Note 5)	IDDrc		1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
MTA81010-LP	IDDlp		19	40	µA	Fosc = 32 KHz, VDD = 3.0V, WDT disabled
Power Down Current (Note 4)						
MTA81010	IPD1		5	14	µA	VDD = 3.0V, WDT enabled
	IPD2		0.8	12	µA	VDD = 3.0V, WDT disabled

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1= external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

15.5 MICROCONTROLLER DC CHARACTERISTICS: MTA81010-RC, XT, LP (COMMERCIAL) MTA81010I-RC, XT, LP (INDUSTRIAL)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40 < TA < +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC specification
Tables 16.3 and 16.4

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Input Low Voltage						
I/O ports	VIL	VSS		0.2 VDD	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt trigger)	VILMC	VSS		0.15 VDD	V	
RTCC (Schmitt trigger)	VILRT	VSS		0.15 VDD	V	
OSC1 (Schmitt trigger)	VILOSC	VSS		0.15 VDD	V	MTA81010RC only (Note 5)
OSC1	VILOSC	VSS		0.3 VDD	V	MTA81010-XT, LP
Input High Voltage						
I/O ports	VIH	0.45 VDD		VDD	V	For all VDD (Note 6)
	VIH	2.0		VDD	V	4.0 V < VDD ≤ 5.5 V (Note 6)
	VIH	0.36 VDD		VDD	V	VDD > 5.5 V
$\overline{MCLR}$ (Schmitt trigger)	VIHMC	0.85 VDD		VDD	V	
RTCC (Schmitt trigger)	VIHRT	0.85 VDD		VDD	V	
OSC1 (Schmitt trigger)	VIHOSC	0.85 VDD		VDD	V	MTA81010-RC only (Note 5)
OSC1	VIHOSC	0.7 VDD		VDD	V	MTA81010-XT, LP
Input Leakage Current (Notes 3, 4)						**For VDD ≤ 5.5V**
I/O ports	IIL	-1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{MCLR}$	IILMCL	-5			µA	VPIN = VSS + 0.25V
$\overline{MCLR}$	IILMCH		0.5	+5	µA	VPIN = VDD
RTCC	IILRT	-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1	IILOSC1	-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD , MTA81010-XT, LP
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT (MTA81010-RC)	VOL			0.6	V	IOL = 1.6 mA, VDD = 4.5V
Output High Voltage						
I/O Ports (Note 4)	VOH	VDD-0.7			V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT (MTA81010-RC)	VOH	VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 °C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : For MTA81010RC devices, the OSC1 pin is a Schmitt trigger input. It is not recommended that the MTA81010 be driven with external clock in RC mode.

Note 6: The user may use better of the two specifications.

15.6 MICROCONTROLLER AC CHARACTERISTICS: MTA81010-RC, XT, LP (COMMERCIAL) MTA81010I-RC, XT, LP (INDUSTRIAL)

AC CHARACTERISTICS **Standard Operating Conditions (unless otherwise stated)**
Operating temperature T_A = -40°C to +85°C (industrial),
and 0°C ≤ T_A ≤ +70°C (commercial)
Operating voltage V_{DD} range as described in DC specification
Tables 16.3 and 16.4

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
External CLOCKIN						
Frequency (Note 2)	FOSCRC	DC		4	MHz	RC mode
	FOSCXT	DC		4	MHz	XT mode
	FOSCLP	DC		40	KHz	LP mode
Oscillator Frequency						
(Note 2)	FOSCRC	DC		4	MHz	RC mode
	FOSCXT	0.1		4	MHz	XT mode
	FOSCLP	DC		40	KHz	LP mode
Instruction Cycle Time						
(Note 2)	TCYRC	1.0	4/FOSCRC	DC	µs	RC mode
	TCYXT	1.0	4/FOSCXT	DC	µs	XT mode
	TCYLP	100	4/FOSCLP	DC	µs	LP mode
External Clock in Timing						
(Note 4)						
Clock in (OSC1) High or Low Time						
XT oscillator type	TCKHLXT	50*			ns	
LP oscillator type	TCKHLLP	2*			µs	
Clock in (OSC1) Rise or Fall Time						
XT oscillator type	TCKRFXT	25*			ns	
LP oscillator type	TCKRFLP	50*			ns	
RESET Timing						
$\overline{\text{MCLR}}$ Pulse Width (low)	TMCL	100*			ns	
RTCC Input Timing, No Prescaler						
RTCC High Pulse Width	TRTH	0.5 TCY + 20*			ns	Note 3
RTCC Low Pulse Width	TRTL	0.5 TCY + 20*			ns	Note 3
RTCC Input Timing, With Prescaler						
RTCC High Pulse Width	TRTH	10*			ns	Note 3
RTCC Low Pulse Width	TRTL	10*			ns	Note 3
RTCC Period	TRTP	$\frac{T_{CY} + 40^*}{N}$			ns	Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Timeout Period						
(No Prescaler)	TWDT	9*	18*	30*	ms	VDD = 5.0V
Oscillation Start-up Timer Period	TOST	9*	18*	30*	ms	VDD = 5.0V
I/O Timing						
I/O Pin Input Valid Before						
CLKOUT≠ (RC Mode)	TDS	0.25 TCY+ 30*			ns	
I/O Pin Input Hold After						
CLKOUT≠ (RC Mode)	TDH	0*			ns	
I/O Pin Output Valid After						
CLKOUTØ (RC Mode)	TPD			40*	ns	

* Guaranteed by characterization, but not tested.

(Notes on next page)

NOTES TO AC CHARACTERISTICS:
MTA81010-RC, XT, LP (COMMERCIAL)
MTA81010I-RC, XT, LP (INDUSTRIAL)

1. Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.
2. Instruction cycle period (Tcy) equals four times the input oscillator time base period.

   All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "minimum" values with an external clock applied to the OSC1 pin.

   When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.
3. For a detailed explanation of RTCC input clock requirements see Section 3.2.1.
4. Clock-in high-time is the duration for which clock input is at VIHOSC or higher.

   Clock-in low-time is the duration for which clock input is at VILOSC or lower.

15.7 ELECTRICAL STRUCTURE OF PINS

FIGURE 15.7.1 - ELECTRICAL STRUCTURE OF I/O PINS (RA, RB, RC)

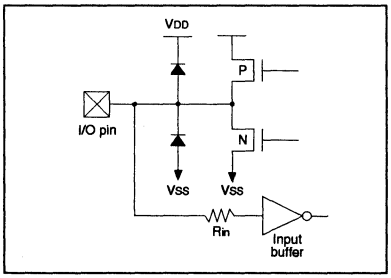
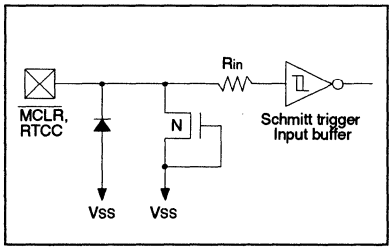


FIGURE 15.7.2 - ELECTRICAL STRUCTURE OF MCLR AND RTCC PINS



16.0 MICROCONTROLLER TIMING DIAGRAMS

FIGURE 16.0.1 - RTCC TIMING

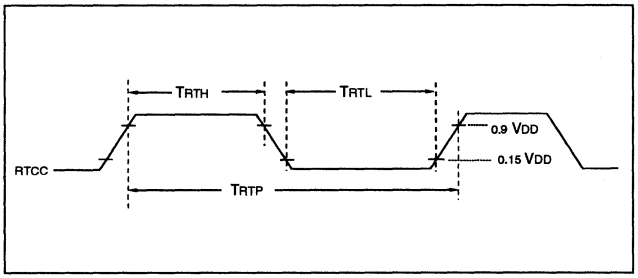
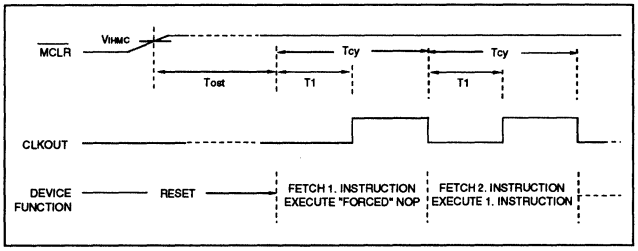
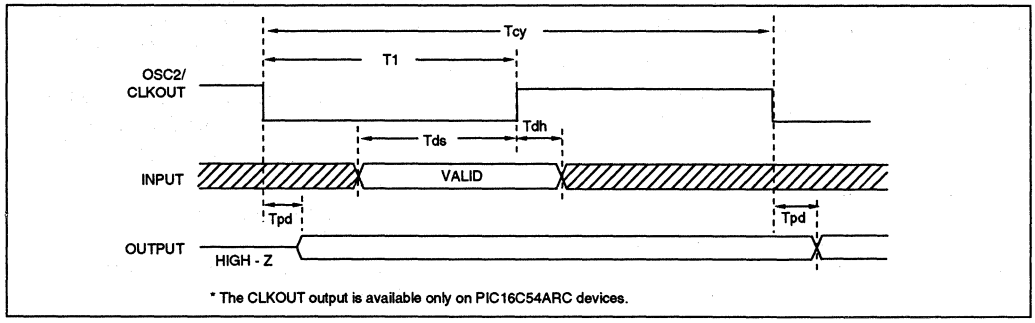


FIGURE 16.0.2 - OSCILLATOR START-UP TIMING (MTA81010RC)



Notes to Figures 15.7.1 and 15.7.2: The diodes and the grounded gate (or output driver) NMOS device are carefully designed to protect against ESD (Electrostatic discharge) and EOS (Electrical overstress). Rin is a small resistance to further protect the input buffer from ESD.

FIGURE 16.0.3 - INPUT/OUTPUT TIMING FOR I/O PORTS (MTA81010RC*)



* The CLKOUT output is available only on PIC16C54ARC devices.

17.0 MICROCONTROLLER DC & AC CHARACTERISTICS GRAPHS/ TABLES:

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. 'Typical' represents the mean of the distribution while 'maximum' or 'minimum' represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

FIGURE 17.0.1 - TYPICAL RC OSCILLATOR FREQUENCY vs TEMPERATURE

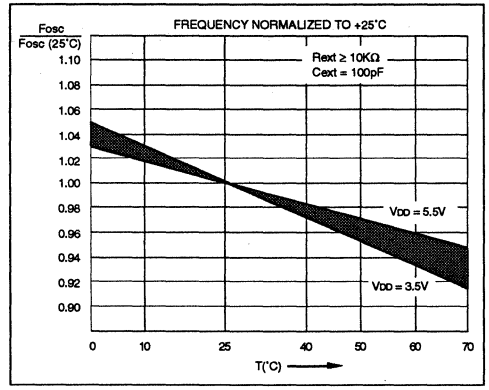


FIGURE 17.0.2 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

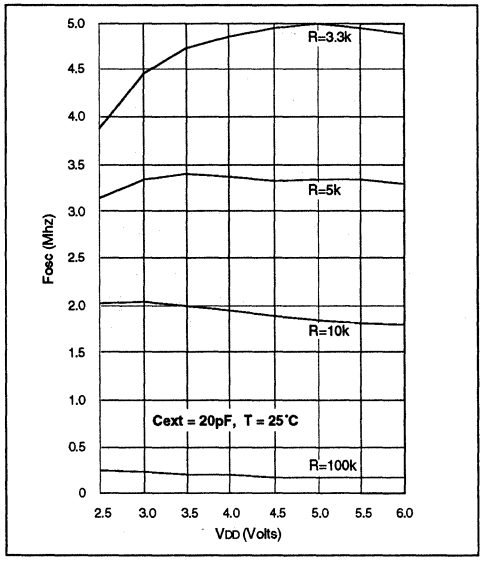


FIGURE 17.0.3 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

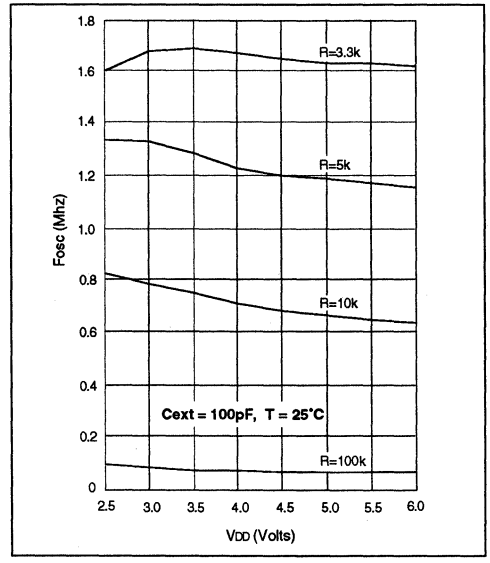


FIGURE 17.0.4 - TYPICAL RC OSCILLATOR FREQUENCY VS VDD

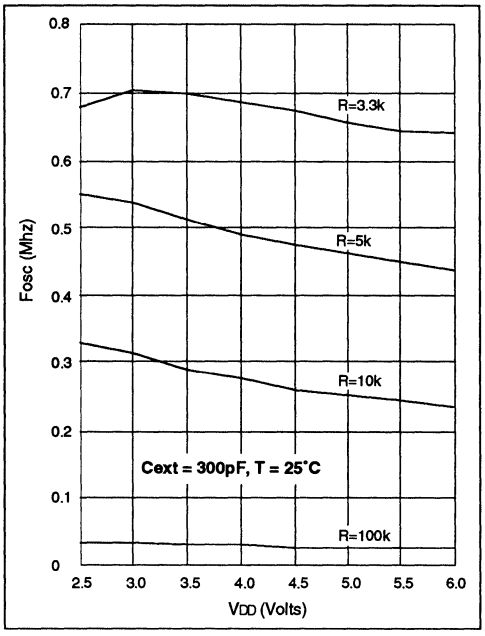


TABLE 17.0.1 - RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
20pf	3.3k	4.71 MHz	± 28%
	5k	3.31 MHz	± 25%
	10k	1.91 MHz	± 24%
	100k	207.76 KHz	± 39%
100pf	3.3k	1.65 MHz	± 18%
	5k	1.23 MHz	± 21%
	10k	711.54 KHz	± 18%
	100k	75.62 KHz	± 28%
300pf	3.3k	672.78 KHz	± 14%
	5k	489.49 KHz	± 13%
	10k	275.73 KHz	± 13%
	100k	28.12 KHz	± 23%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for full VDD range.

FIGURE 17.0.5 - TYPICAL IPD VS VDD WATCHDOG DISABLED 25°C

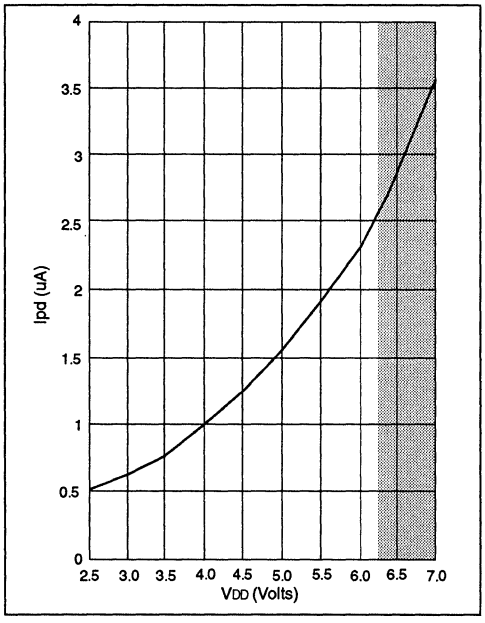
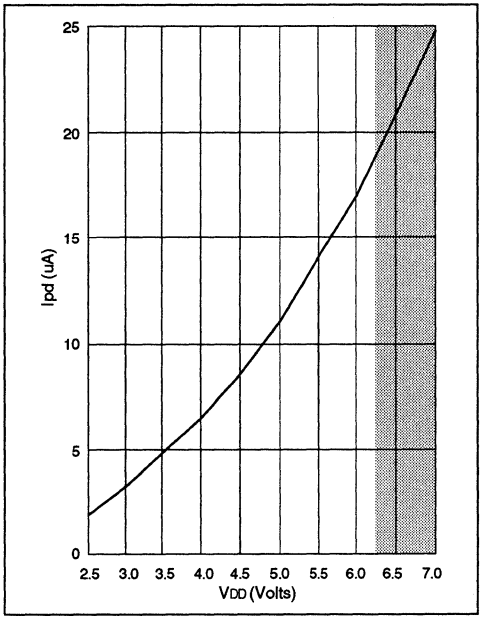


FIGURE 17.0.6 - TYPICAL IPD VS VDD WATCHDOG ENABLED 25°C



Note: The gray shaded regions are outside the normal PIC16C54 operating range. Do not operate in these regions.

FIGURE 17.0.7 - MAXIMUM IPD VS VDD WATCHDOG DISABLED

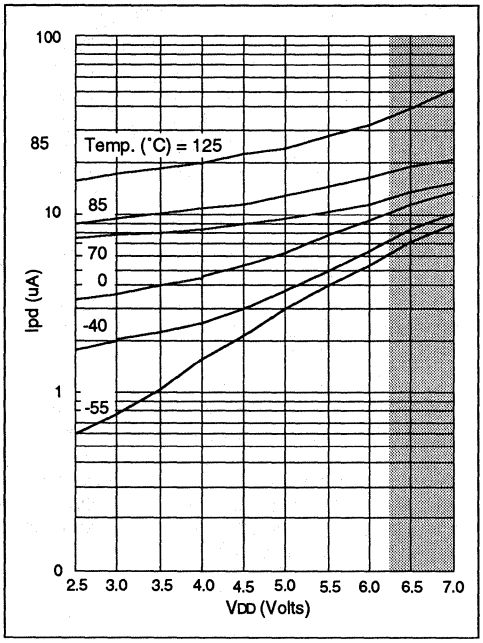
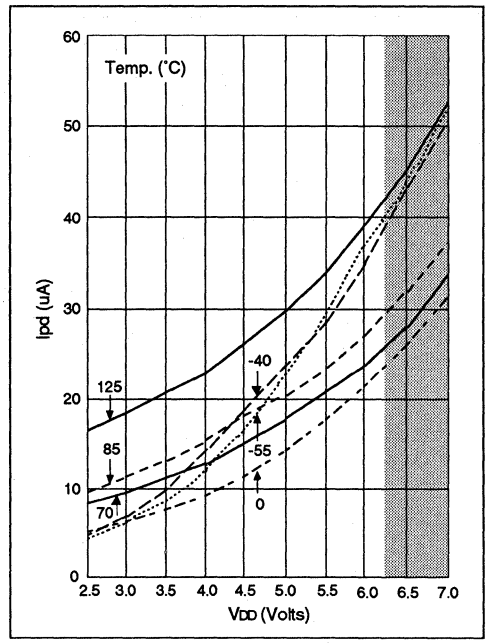


FIGURE 17.0.8 - MAXIMUM IPD VS VDD WATCHDOG ENABLED*



* IPD, with watchdog timer enabled, has two components: The leakage current which increases with higher temperature and the operating current of the watchdog timer logic which increases with lower temperature. At -40°C, the latter dominates explaining the apparently anomalous behavior.

Note: The gray shaded regions are outside the normal PIC16C54 operating range. Do not operate in these regions.

FIGURE 17.0.9 - VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS VS VDD

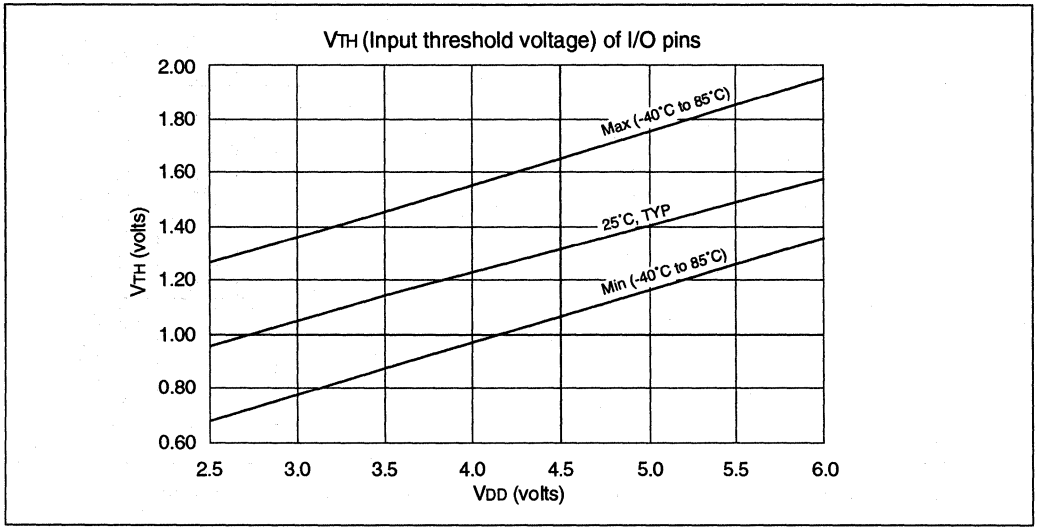
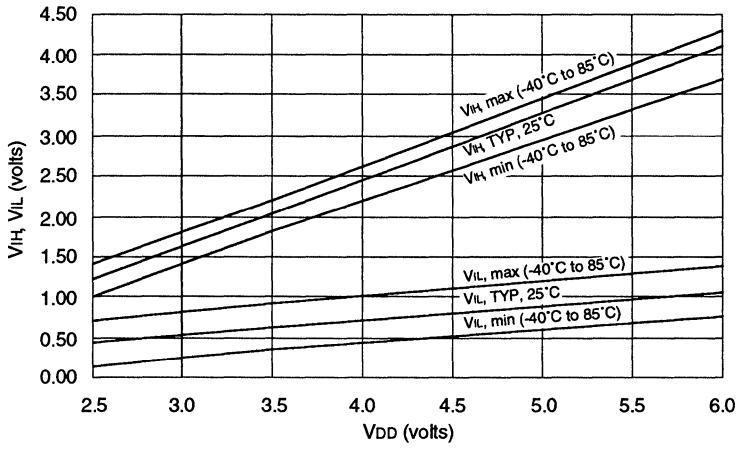


FIGURE 17.0.10 - V_{IH}, V_{IL} OF $\overline{MCLR}$, RTCC AND OSC1 (IN RC MODE) vs V_{DD}



Note: These input pins have Schmitt trigger input buffer.

4

FIGURE 17.0.11 - V_{TH} (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT AND LP MODES) vs V_{DD}

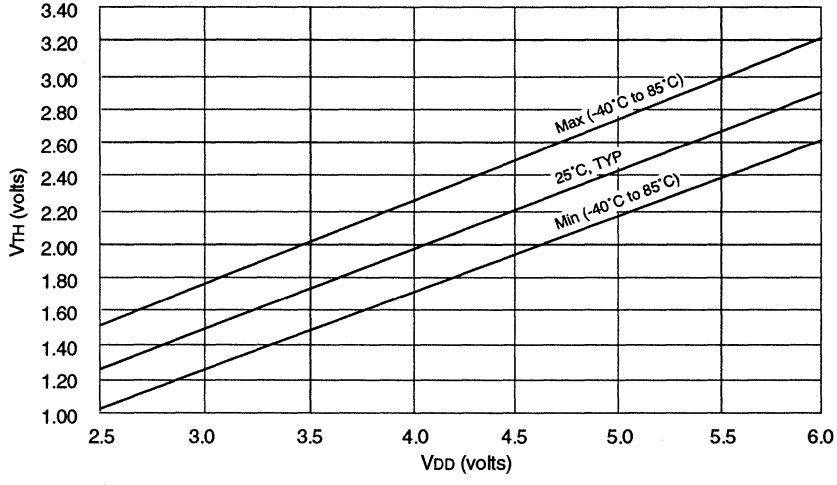


FIGURE 17.0.12 - TYPICAL IDD VS FREQ (EXT CLOCK, 25°C)

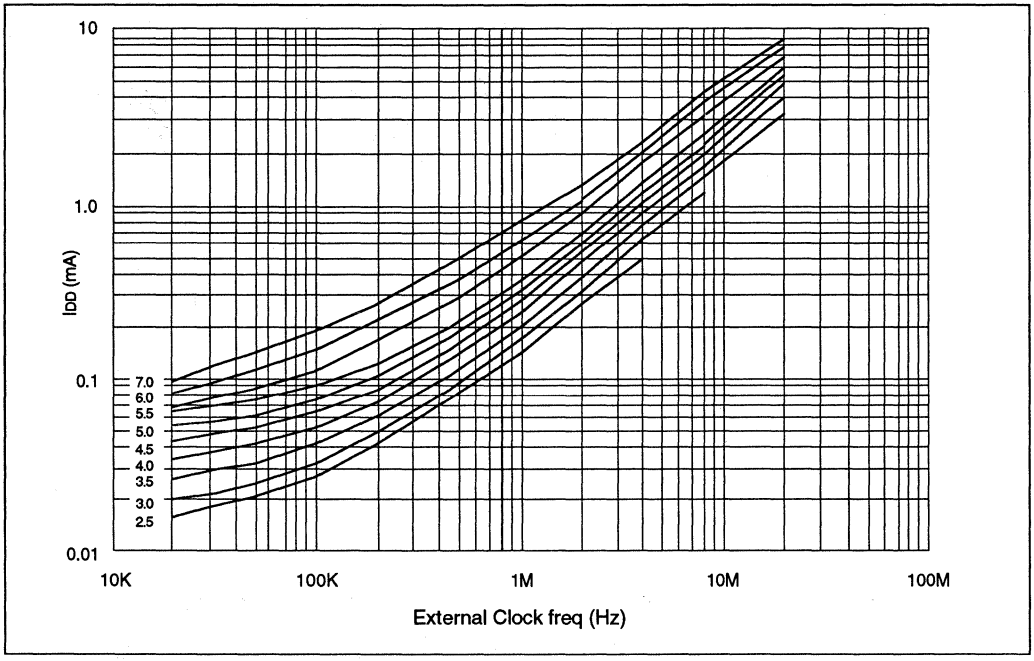


FIGURE 17.0.13 - MAXIMUM IDD VS FREQ (EXT CLOCK, -40° TO +85°C)

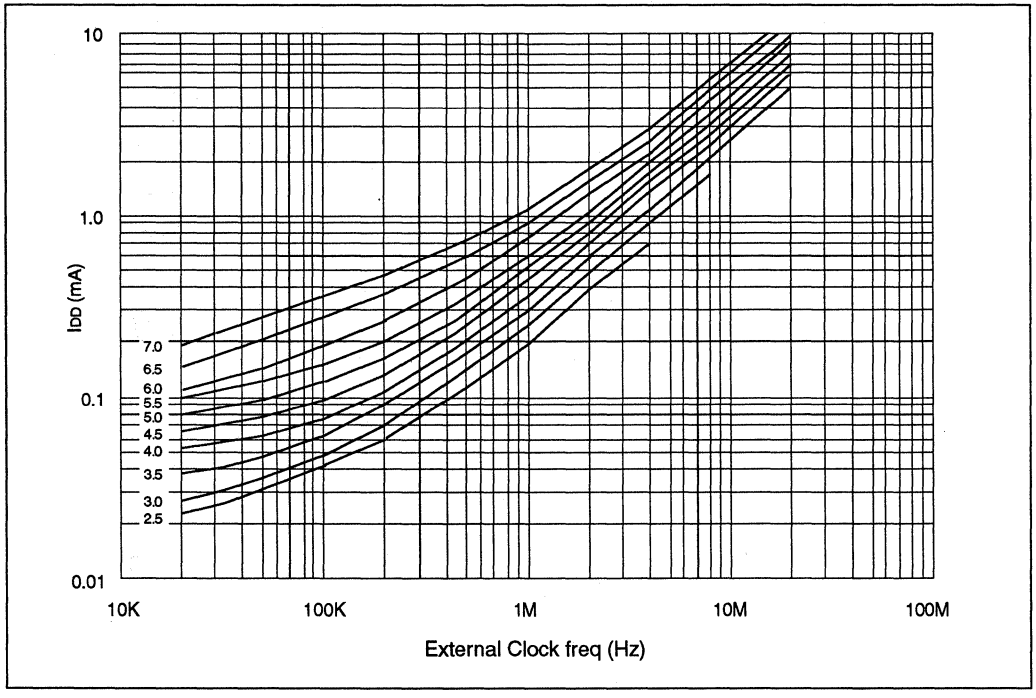


FIGURE 17.0.14 - MAXIMUM IDD VS FREQ (EXT CLOCK, -55° TO +125°C)

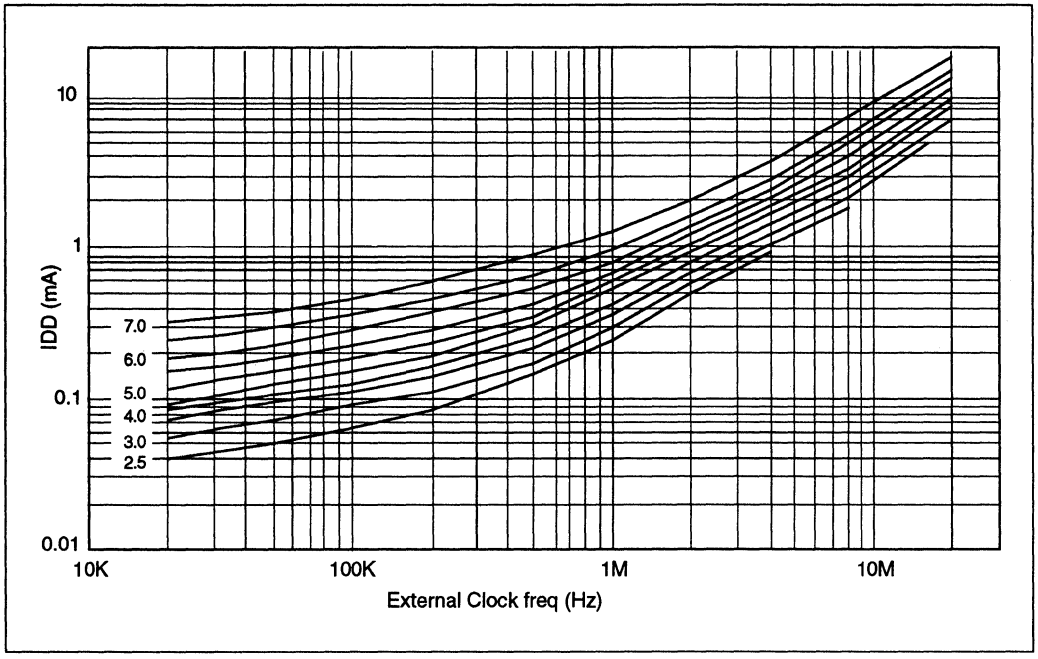


FIGURE 17.0.15 - WDT TIMER TIME-OUT PERIOD VS VDD

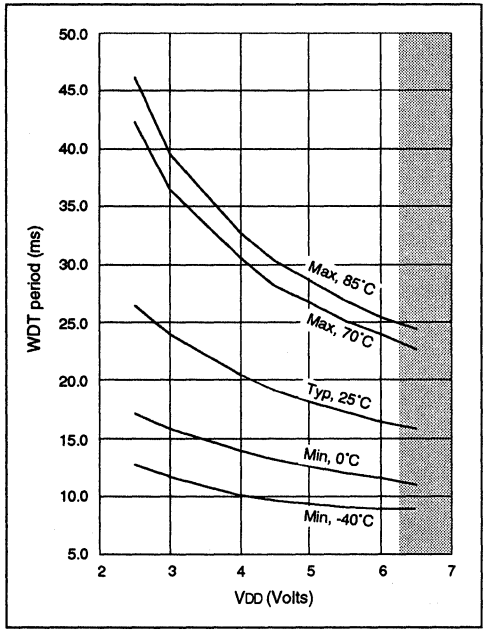
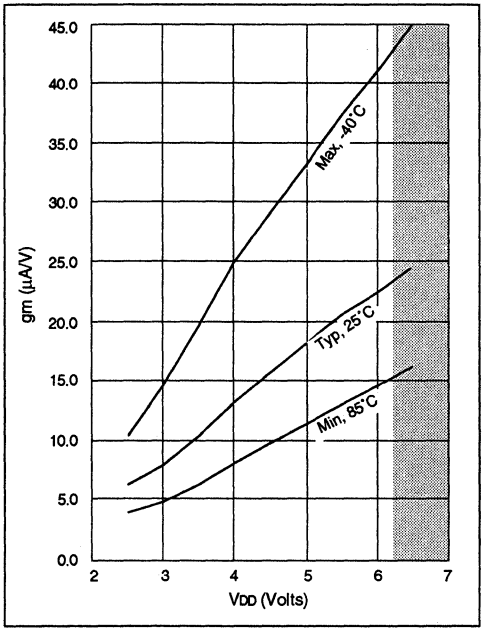


FIGURE 17.0.16 - TRANSCONDUCTANCE (gm) OF LP OSCILLATOR VS VDD



Note: The gray shaded regions are outside the normal PIC16C54 operating range. Do not operate in these regions.

FIGURE 17.0.17 - TRANSCONDUCTANCE (gm) OF XT OSCILLATOR VS VDD

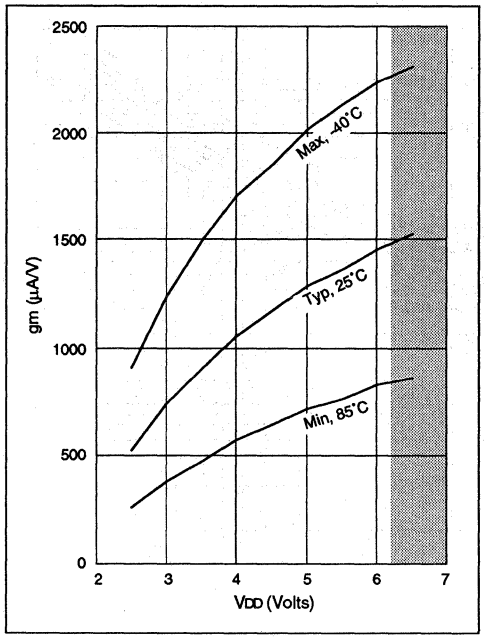
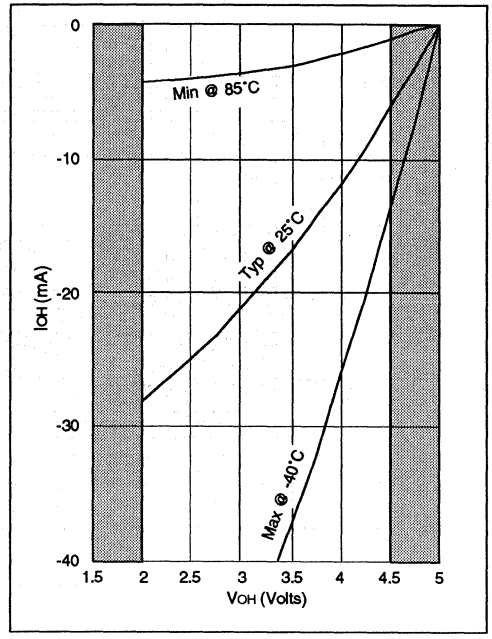


FIGURE 17.0.18 - IOH VS VOH, VDD = 3V



Note: The gray shaded regions are outside the normal PIC16C54 operating range. Do not operate in these regions.

FIGURE 17.0.19 - IOH VS VOH, VDD = 5V

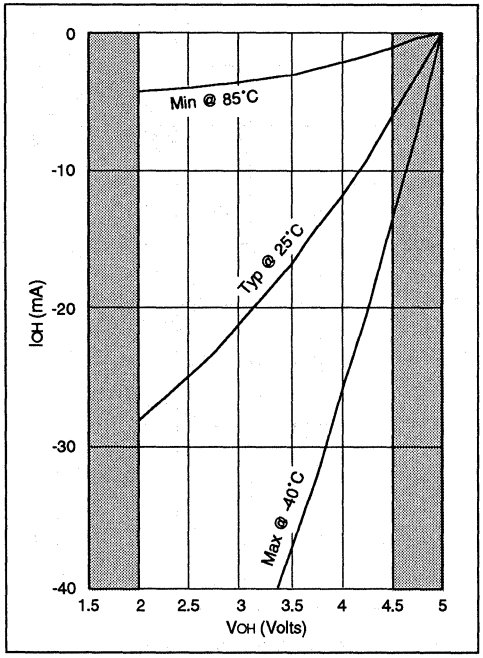


FIGURE 17.0.20 - IOL VS VOL, VDD = 3V

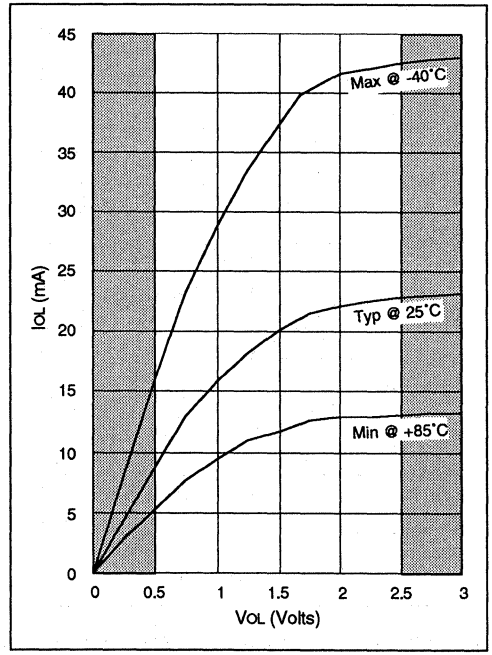
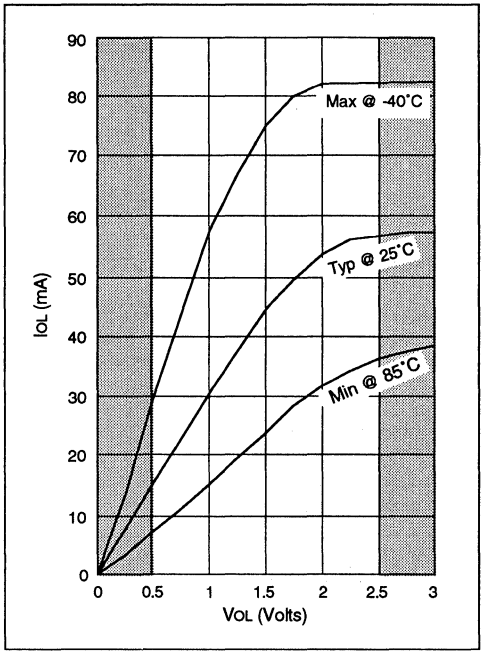


FIGURE 17.0.21 - IOL VS VOL, VDD = 5V



Note: The gray shaded regions are outside the normal PIC16C54 operating range. Do not operate in these regions.

TABLE 17.0.2 - INPUT CAPACITANCE FOR MTA81010 *

Pin Name	Typical Capacitance (pF)	
	28L PDIP (600 mil)	28L SOIC
RA port	5.2	4.8
RB port	5.6	4.7
MCLR	17.0	17.0
OSC1	6.6	3.5
OSC2/CLKOUT	4.6	3.5
RTCC	4.5	3.5

* All capacitance values are typical at 25°C and measured at 1 MHz. A part to part variation of ±25% (three standard deviations) should be taken into account.

4

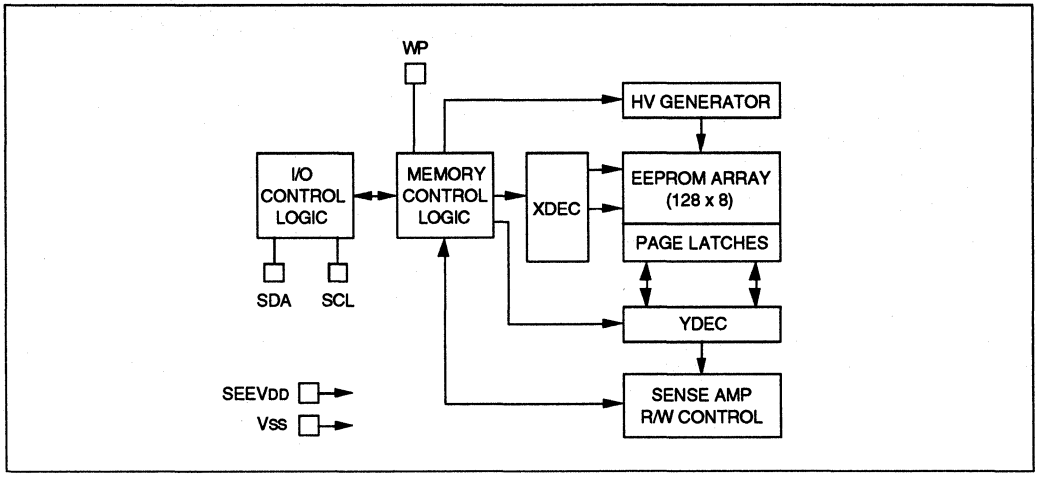
18.0 SERIAL EEPROM SECTION

The Microchip Technology Inc. MTA81010 contains a 24LC01B 1K bit Electrically Erasable PROM. The SEEPROM is organized as a single block of 128 x 8 bit memory with a two-wire serial interface. Low voltage design permits operation down to 2.5 volts with a standby and active currents of only 5 µA and 1 mA respectively. The 24LC01B has page-write capability for up to 8 bytes of data.

TABLE 18.1.1 - SEEPROM PIN FUNCTION

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
SEEVDD	+2.5V to 5.5V Power Supply
NC	No Connection

FIGURE 18.1.1 - SERIAL EEPROM BLOCK DIAGRAM



19.0 SERIAL EEPROM FUNCTIONAL DESCRIPTION

The 24LC01B supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC01B works as slave. The internal 24LC01B in the MTA81010 is hardwire configured with a device address of 0. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

20.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 20.1.1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC01B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Slave Address

The chip address of the internal 24LC01B in the MTA81010 is hardwire configured with a device address of XXX.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit control code (1010) for the 24LC01B, followed by three don't care bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24LC01B. (See Figure 20.1.2).

The 24LC01B monitors the bus for its corresponding control code all the time. It generates an acknowledge bit if the control code was true and it is not in a programming mode.

External devices (e.g. Serial EEPROMs) with the same control code as the internal 24LC01B must not be connected to the same serial bus or a conflict will occur. Devices with different control codes may be connected to the serial bus without risk of conflict.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXX	1
Write	1010	XXX	0

FIGURE 20.1.2 - CONTROL BYTE ALLOCATION

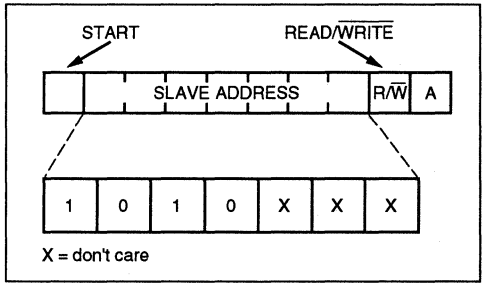
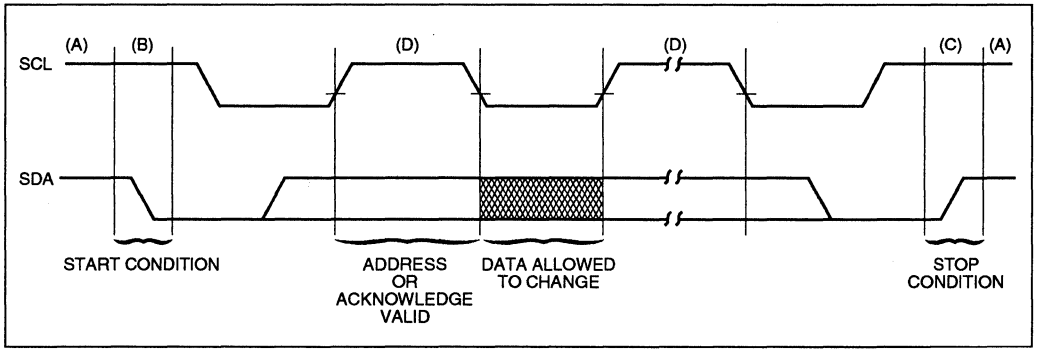


FIGURE 20.1.1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



Byte Write

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC01B. After receiving another acknowledge signal from the 24LC01B the master device will transmit the data word to be written into the addressed memory location. The 24LC01B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC01B will not generate acknowledge signals. (See Figure 20.1.3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC01B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LC01B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin. (See Figure 20.1.4).

FIGURE 20.1.3 - BYTE WRITE

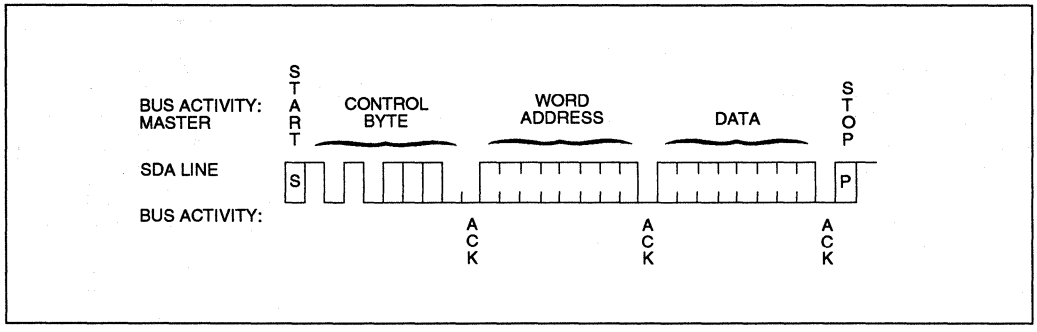


FIGURE 20.1.4 - PAGE WRITE

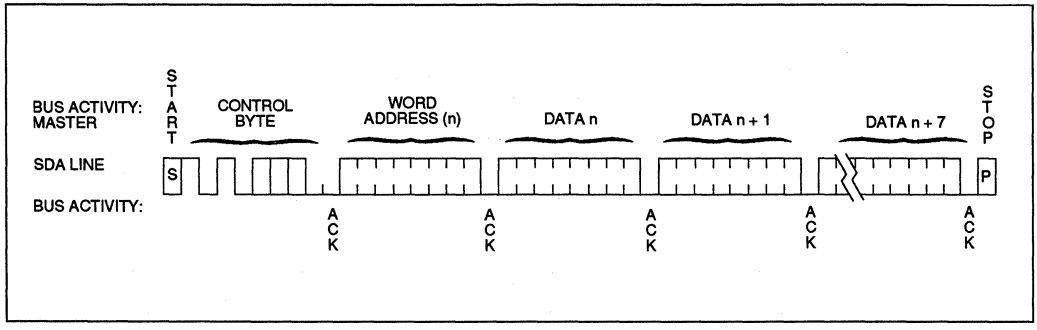


FIGURE 20.1.5 - CURRENT ADDRESS READ

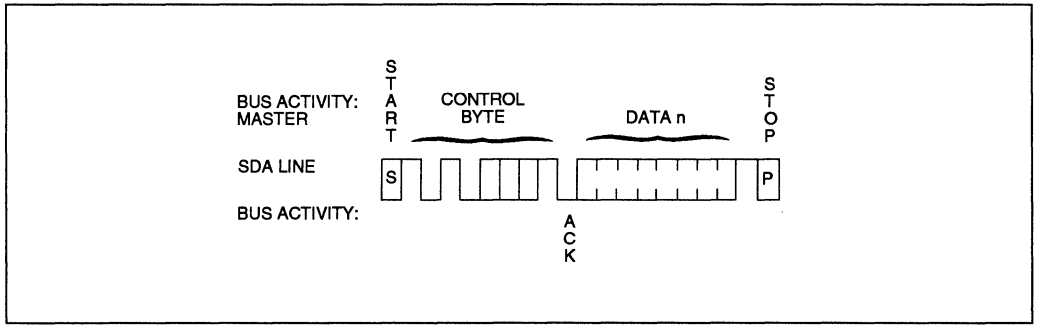


FIGURE 20.1.6 - RANDOM READ

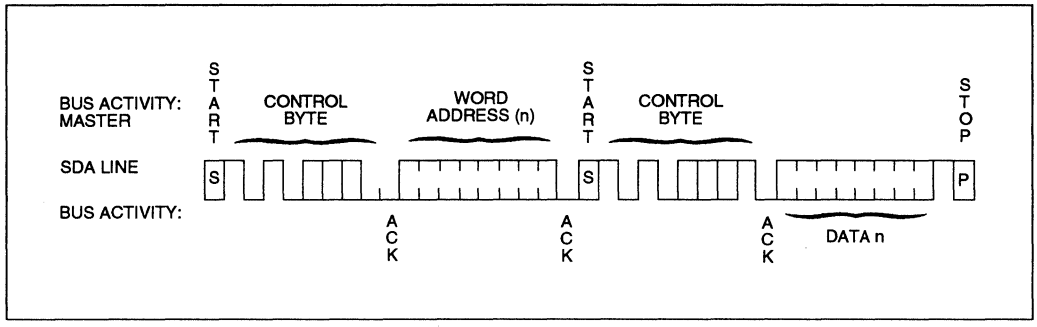
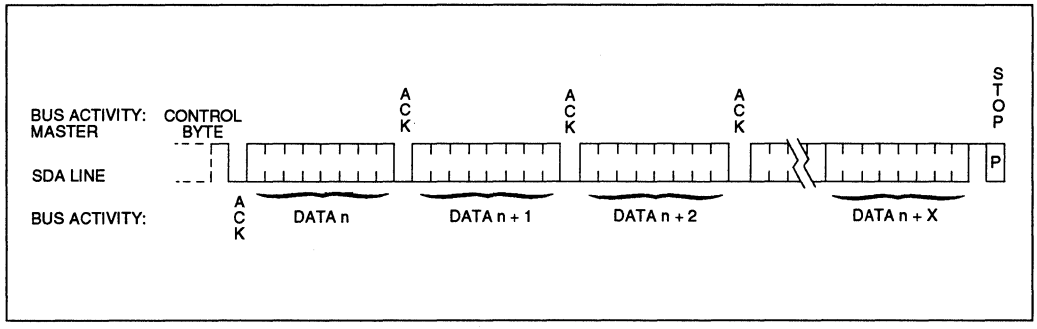


FIGURE 20.1.7 - SEQUENTIAL READ



WRITE PROTECTION

The 24LC01B can be used as a serial ROM when the WP pin is connected to SEEVDD. Programming will be inhibited and the entire memory will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24LC01B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC01B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC01B discontinues transmission (see Figure 20.1.5).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC01B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC01B will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC01B discontinues transmission (see Figure 20.1.6).

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC01B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC01B to transmit the next sequentially addressed 8 bit word (see Figure 20.1.7).

To provide sequential reads the 24LC01B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The 24LC01B employs a VDD threshold detector circuit which disables the internal erase/write logic if the VDD is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

21.0 PIN DESCRIPTIONS

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP

This pin must be connected to either VSS or SEEVDD.

If tied to VSS, normal memory operation is enabled (read/write the entire memory 00-7F or 00-FF).

If tied to SEEVDD, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC01B as a serial ROM when WP is enabled (tied to SEEVDD).

22.0 SERIAL EEPROM ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3V to +6.25V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied .... -65°C to +125°C
Soldering temperature of leads (10 seconds) . +300°C
ESD protection on all pins ..... ≥ 4 kV

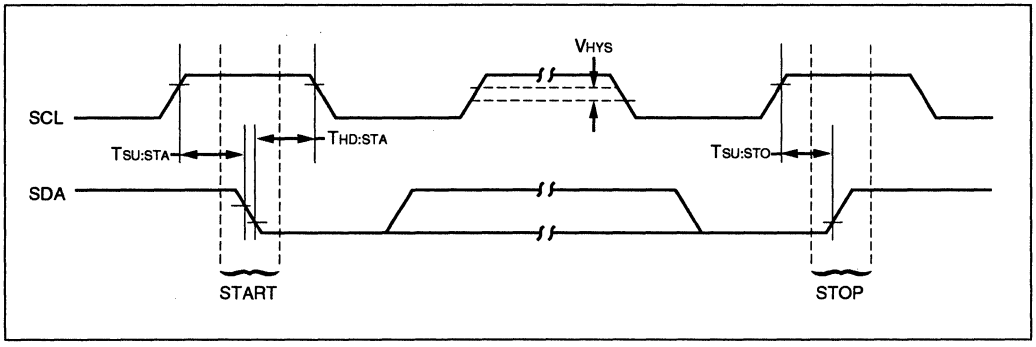
*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

22.1 SERIAL EEPROM DC CHARACTERISTICS

DC CHARACTERISTICS					V_{DD} = +2.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins: High level input voltage	V_{IH}	.7 V_{DD}	—	V	
Low level input voltage	V_{IL}	—	.3 V_{DD}	V	
Hysteresis of Schmitt trigger inputs	V_{HYS}	0.05 V_{DD}	—	V	Note 1
Low level output voltage	V_{OL}	—	.40	V	I_{OL} = 3.0 mA, V_{DD} = 2.5V
Input leakage current	I_{LI}	-10	10	µA	V_{IN} = .1V to V_{DD}
Output leakage current	I_{LO}	-10	10	µA	V_{OUT} = .1V to V_{DD}
Internal capacitance (all inputs/outputs)	C_{INT}	—	10	pF	V_{CC} = 5.0V (Note 1) Tamb = 25°C, F_{CLK} = 1 MHz
Operating current	I_{DDO}	—	3	mA	V_{DD} = 5.5V SCL = 400 KHz
Standby current	I_{DDS}	—	30	µA	V_{DD} = 3.0V SDA = SCL = V_{DD}
		—	100	µA	V_{DD} = 5.5V SDA = SCL = V_{DD}

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 22.1.1 - BUS TIMING START/STOP



22.2 SERIAL EEPROM AC CHARACTERISTICS

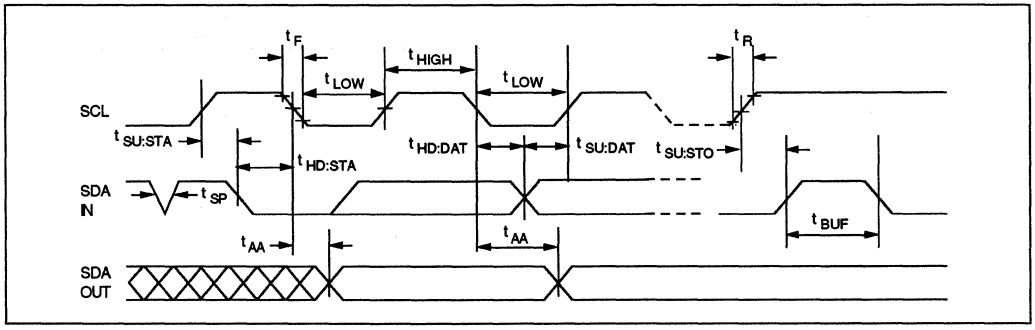
AC CHARACTERISTICS		STANDARD MODE		VDD = 4.5-5.5V FAST MODE			
Parameter	Symbol	Min	Max	Min	Max	Units	Remarks
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	20 +0.1 CB	300	ns	Note 2
SDA and SCL fall time	TF	—	300	20 +0.1 CB	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	100,000	—	100,000	—	E/W Cycles	

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

FIGURE 22.2.1 - BUS TIMING DATA

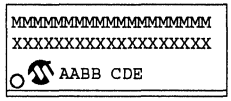


23.0 PACKAGING DIAGRAMS AND DIMENSIONS

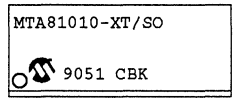
See Section 11 of the Data Book.

23.1 PACKAGE MARKING INFORMATION

28L SOIC



Example

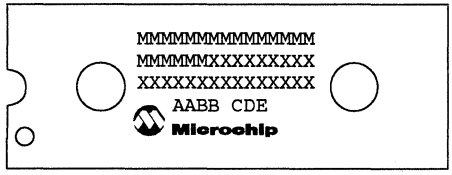


Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.
Note:	In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

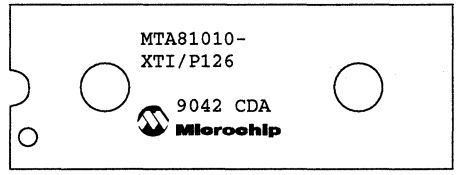
*Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are incuded in QTP price.

PACKAGE MARKING INFORMATION (CONT.)

28L PDIP (.600 mil)



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

Index

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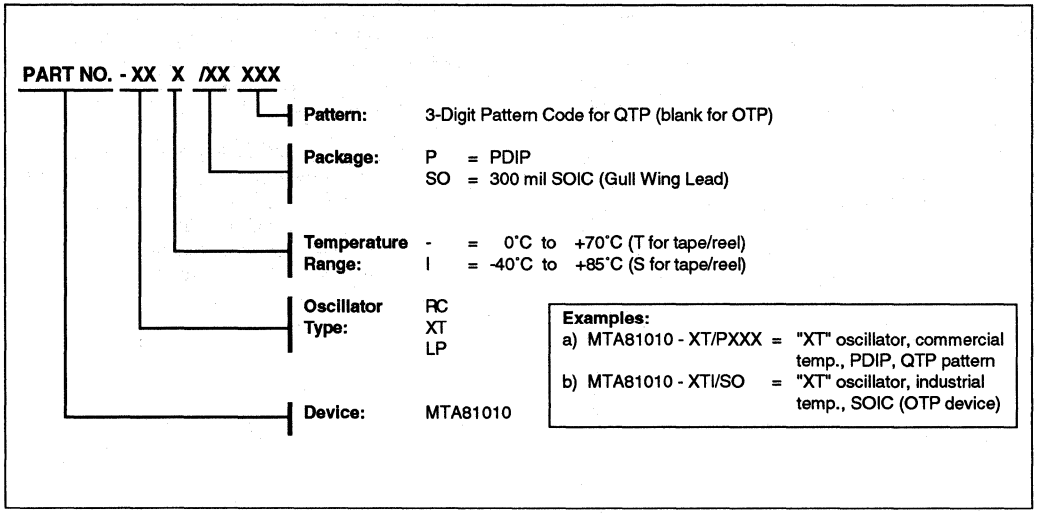
Trademarks:

IBM PC is a trademark of IBM Corporation.

MS DOS and Microsoft Windows are registered trademarks of Microsoft Corporation.

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



MICROCHIP

MTA85XXX

PICSEE™ 20-Pin MCU with Serial EEPROM Multi-Chip Module

FEATURES

- Multi-chip module
- PIC16C54A or PIC16C58A Microcontrollers with 24LC01B or 24LC02B Serial EEPROMs (SEEs) in a single package
- Wide operating voltage range: VDD = 3.0V to 6.25V
- Microcontroller control of SEE power for low standby current: MTA85X1X series

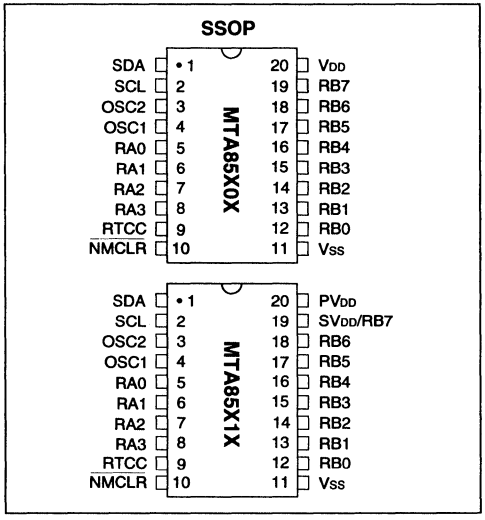
High Performance RISC-like CPU

- Only 33 single-word instructions to learn
- All instructions are single-cycle except for program branches, which are two
- Operating speed: DC - 20 MHz clock
  DC - 200 ns cycle
- 12-bit wide instructions
- 8-bit wide data path
- 512 or 2048 x 12 on-chip EPROM program memory
- 25 or 72 x 8 general purpose registers (SRAM)
- 7 special function hardware registers
- 2 level deep hardware stack
- Direct, Indirect, and relative addressing modes for data and instructions

Peripheral Features

- 12 I/O pins with individual direction control (RB7 dedicated for SEE VDD in MTA85X1X devices)
- 8-bit real time clock/counter (RTCC) with 8-bit programmable prescaler
- Power on reset
- Oscillator start-up timer
- Watchdog timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security EPROM bit for code-protection
- Power saving SLEEP mode
- EPROM selectable oscillator options:
  - Low cost RC oscillator: RC
  - Standard crystal/resonator: XT
  - High speed crystal/resonator: HS
  - Power saving low speed crystal: LP

FIGURE A - PIN CONFIGURATIONS



Serial EEPROM Features

- 1K or 2K of EEPROM memory, organized as one block (128 x 8) or (256 x 8)
- Two-wire serial interface bus
- 100 KHz and 400 KHz compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2ms typical cycle times for page-write
- 1,000,000 ERASE/WRITE cycles typical
- Data retention > 40 years

CMOS Technology

- Low-power, high-speed CMOS EPROM and EEPROM technologies, in a single package
- Fully static Microcontroller
- Low power consumption:
  - < 3.5 mA typical, @ 5V, 4 MHz, EEPROM write
  - < 2.5 mA typical, @ 5V, 4 MHz, EEPROM read
  - < 7 µA typical standby current @ 3V, MTA85X0X series
  - < 3 µA typical standby current @ 3V, MTA85X1X series (WDT disabled, 0°C to 70°C)

PICSEE and PRO MATE are trademarks of Microchip Technology Inc.

1.0 GENERAL DESCRIPTION

The MTA85XXX devices from Microchip Technology Inc. are a family of multi-chip products which offer a unique combination of EPROM-based Microcontrollers and Serial EEPROM data memory in a single package. The MTA85XXX line features the PIC16C5XA family of Microcontrollers combined with Microchip's 24LC0XB family of Serial EEPROMs.

Two unique pinouts are available in this family of devices, regardless of which combination of component chips are used. The first pinout (MTA85X0X series) features shared power and ground pins for the Microcontroller and SEE. All other Microcontroller and SEE pins are electrically independent. The second available pinout (MTA85X1X series) features Microcontroller control of the SEE VDD. This allows the SEE to be powered down when going into a standby mode. This is often desirable in power conscious applications to reduce current when the SEE is not being accessed. In this configuration the Microcontroller pin RB7 is used to supply power to the SEE. It is the user's responsibility to ensure that RB7 is driving a '1' while the SEE is being used.

The Microcontroller and Serial EEPROM portions of these multi-chip devices are equivalent to their respective individual components chips, except for the electrical specifications on shared pins. Please refer to the datasheets of the component die for information on each device's architecture, functionality, and other important user information.

1.1 APPLICATIONS

The MTA85XXX family is ideally suited to a wide variety of applications including, but not limited to: keyless entry, remote control, smart cards and automotive controllers. The EPROM program memory makes customization of application programs fast and convenient. The EEPROM data memory is ideal for storing configuration information, access codes, serial numbers, and adaptive look-up tables. The small footprint package makes the MTA85XXX devices perfect for applications with physical space limitations. This small size coupled with the low-cost, low-power, wide voltage range, and high performance of this flexible family of devices makes the MTA85XXX the microcontroller of choice for a wide variety of applications which utilize EEPROM memory.

1.2 MTA85XXX SERIES OVERVIEW

A variety of EPROM sizes, EEPROM sizes and frequency ranges are available. Depending on the application and production requirements, the proper device option can be selected using the information in Table 1.2.1 below. When placing orders, please use the "MTA85XXX Product Identification System" on the back page of this data sheet to specify the correct part.

1.2.1 ONE-TIME-PROGRAMMABLE (OTP) DEVICES

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

With OTP devices the program EPROM is erased, allowing the user to write the application code into it. Additionally the watchdog timer can be disabled, and/or the code protection logic can be activated by programming special EPROM fuses. Sixteen non-dedicated EPROM bits are available for the customer ID or other customer information and are also user programmable.

1.2.2 QUICK-TURN-PRODUCTION (QTP) DEVICES

Microchip offers a QTP Programming Service for factory production orders. This service is made available for volume users with stable code, who choose not to program the devices themselves. A QTP device is identical to an OTP device, except that the program memory and special EPROM fuses are programmed at the factory, with the customer's code. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology Inc. sales office for more details.

TABLE 1.2.1 - FAMILY OVERVIEW

Part Number	Microcontroller	SEE	PGM EPROM	EEPROM	RAM	I/O
MTA85401	PIC16C54A	24LC01B	512 X 12	128 X 8	32 X 8	12
MTA85402	PIC16C54A	24LC02B	512 X 12	256 X 8	32 X 8	12
MTA85411	PIC16C54A	24LC01B	512 X 12	128 X 8	32 X 8	12 note 1
MTA85412	PIC16C54A	24LC02B	512 X 12	256 X 8	32 X 8	12 note 1
MTA85801	PIC16C58A	24LC01B	2048 X 12	128 X 8	79 X 8	12
MTA85802	PIC16C58A	24LC02B	2048 X 12	256 X 8	79 X 8	12
MTA85811	PIC16C58A	24LC01B	2048 X 12	128 X 8	79 X 8	12 note 1
MTA85812	PIC16C58A	24LC02B	2048 X 12	256 X 8	79 X 8	12 note 1

Note 1: RB7 dedicated to SEE VDD

2.0 DEVELOPMENT SUPPORT

2.1 Development Tools

The PIC16C5X and PIC16CXX microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER™ Real-Time In-Circuit Emulator
- PRO MATE™ Universal Programmer
- PICSTART™ Low-Cost Prototype Programmer
- Assembler
- Software Simulator

2.2 PICMASTER™: High Performance Universal In-Circuit Emulator

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all devices utilizing microcontrollers in the PIC16C5X, PIC16CXX and PIC17CXX families.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new products based on PIC16C5X, PIC16CXX and PIC17CXX microcontrollers.

SSOP to DIP socket adaptors for the MTA85XXX products allow the user to operate the application with a surface mount device, after the emulation has been completed.

The Emulator System is designed to operate on low-cost PC compatible machines ranging from 80286-AT class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows™ 3.X environment, allowing the operator access to a wide range of supporting software and accessories.

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.X environment was chosen to best make these features available to the end user.

The PICMASTER Emulator Universal System consists primarily of four major components:

- Host-Interface Card
- Emulator Control Pod
- Target-Specific Emulator Probe, with MTA85XXX interface board
- PC Host Emulation Control Software

The Windows 3.X System is a multitasking operating system which will allow the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window. Dynamic Data Exchange (DDE), a feature of Windows 3.X, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

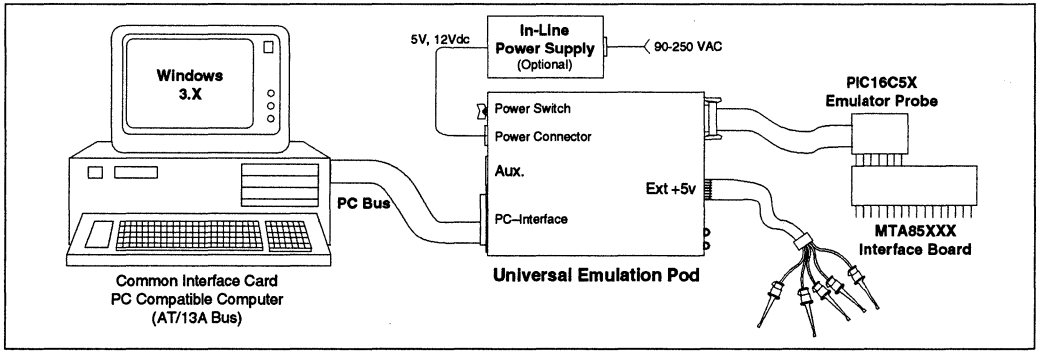
Under Windows 3.X, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible.

2.3 PRO MATE™: Universal Programmer

The PRO MATE Universal Programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MATE has programmable V_{DD} and V_{PP} supplies which allows it to verify programmed memory at V_{DD} minimum and V_{DD} maximum for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MATE can read, verify or program products based on PIC16C5X, PIC16CXX and PIC17CXX devices. It can also set fuse configuration and code-protect in this mode. Its EEPROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.

FIGURE 2.1 - PICMASTER SYSTEM CONFIGURATION



In PC-hosted mode, the PRO MATE connects to the PC via one of the COM (RS-232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of VDD minimum, VDD maximum and VPP levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, and blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different serial number, sequential or random.

The PRO MATE has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. PRO MATE supports all products based on PIC16C5X, PIC16CXX and PIC17CXX processors.

MTA85XXX customers can use their existing PIC16C5X PRO MATE socket module with an adaptor socket, or use the PRO MATE socket module designed specifically for the MTA85XXX products.

2.4 PICSTART™ Programmer

The PICSTART programmer is an easy to use, very low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. A PC-based user interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based.

The same MTA85XXX adaptor socket which is available for use with the PRO MATE will allow the user to convert the MTA85XXX SSOP footprint to the DIP footprint used by PICSTART. This same socket will also allow the user to program the EEPROM portion of the MTA85XXX in a standard EEPROM programmer.

2.5 Assembler

The Assembler is a PC-hosted software development tool supporting the PIC16C5X and PIC16CXX series microcontrollers. It offers a full featured Macro and Conditional assembly capability. It can also generate various object code formats including several Hex formats to support Microchip's proprietary development tools as well as third party tools. Also supports Hex (default), Decimal and Octal Source and listing formats. An assembler users manual is available for detailed support.

2.6 Software Simulator

The Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16C5X and PIC16CXX series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in single step, execute until break or in a trace mode. Two forms of symbolic debugging are available: an internal symbol table for disassembling opcodes and the displaying of source code from a listing file. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

2.7 Development Systems

For convenience, the development tools are packaged into comprehensive systems as listed below:

Item	Name	System Description
1.	PICMASTER System	PICMASTER In-Circuit Emulator with your choice of Target Probe, PRO MATE Programmer, Assembler, Software Simulator and Samples.
2.	PICSTART System	PICSTART Low-Cost Prototype Programmer, Assembler, Software Simulator and Samples

3.0 ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum Ratings*

Ambient temperature under bias ..... -55°C to +125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss
(except VDD and MCLR) ..... -0.6V to VDD +0.6V
Voltage on VDD with respect to Vss ..... 0 to +7.5V
Voltage on MCLR with respect to Vss
(Note 2) ..... 0 to +14V
Total power Dissipation (Note 1) ..... 800 mW
Maximum Current out of Vss pin ..... 150 mA
Maximum Current into VDD pin ..... 50 mA
Maximum Current into an input pin ..... ±500 µA
Maximum Output Current sinked by any I/O pin 25 mA
Maximum Output Current sourced
by any I/O pin ..... 20 mA
Maximum Output Current sourced by a single
I/O port (Port A or B) ..... 40 mA
Maximum Output Current sinked by a single
I/O port (Port A or B) 50mA

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
$Pdis = VDD \times \{IDD - \Sigma Ioh\} + \Sigma\{(VDD-Voh) \times Ioh\} + \Sigma(Vol \times Iol)$

2. Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to Vss.

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3.2 Pin Descriptions

Name	Function	Description
RA0 - RA3	I/O PORT A	4 input/output lines.
RB0 - RB7	I/O PORT B	8 input/output lines.
SVDD/RB7	Shared VDD-I/O pin	Input/Output pin dedicated to EEPROM VDD. No external connection needed. MTA85X1X only.
RTCC	Real Time Clock/Counter	Schmitt Trigger Input. Clock input to RTCC register. Must be tied to Vss or VDD if not in use to avoid unintended entering of test modes and to reduce current consumption.
$\overline{MCLR}$	Master Clear	Schmitt Trigger Input. A "Low" voltage on this input generates a RESET condition for the microcontroller. A rising voltage triggers the on-chip oscillator start-up timer which keeps the chip in RESET mode for about 18ms. This input must be tied directly, or via a pull-up resistor, to VDD.
OSC1	Oscillator (input)	"XT", "HS" and "LP" devices: Input terminal for crystal, ceramic resonator, or external clock generator. "RC" devices : Driver terminal for external RC combination to establish oscillation.
OSC2/CLKOUT	Oscillator (output)	For "XT", "HS" and "LP" devices: Output terminal for crystal and ceramic resonator. Do not connect any other load to this output. Leave open if external clock generator is used. For "RC" devices : A "CLKOUT" signal with a frequency of 1/4 Fosc1 is put out on this pin.
SDA	Serial EEPROM Data	EEPROM data line.
SCL	Serial EEPROM Clock	EEPROM clock line.
VDD	Power supply	
Vss	Ground	

3.3 DC Characteristics: MTA85X0X-04 (COMMERCIAL, INDUSTRIAL) MTA85X0X-10 (COMMERCIAL, INDUSTRIAL) MTA85X0X-20 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS			Standard Operating Conditions Operating temperature -40°C ≤ TA ≤ +125°C for automotive, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial			
Characteristic	**Sym**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	3.0 4.5		6.25 5.5	V V	XT, RC and LP options HS option
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See POR section in microcontroller datasheet for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See POR section in microcontroller datasheet for details on power on reset
Supply Current (Note 2)	IDD					XT and RC options
			2.8	6.0	mA	FOSC = 4 MHz, VDD = 5.5V
						HS option
			5.8	13	mA	FOSC = 10 MHz , VDD = 5.5V
			10	23	mA	FOSC = 20 MHz, VDD = 5.5V
						LP option, Commercial
			25	60	µA	FOSC = 32 KHz, VDD = 3.0V, WDT disabled
						LP option, Industrial
			30	70	µA	FOSC = 32 KHz, VDD = 3.0V, WDT disabled
Power Down Current (Note 4)						
WDT enabled	IPD		4	12	µA	VDD = 3.0V, Commercial
			5	14	µA	VDD = 3.0V, Industrial
WDT disabled			0.6	9	µA	VDD = 3.0V, Commercial
			0.8	12	µA	VDD = 3.0V, Industrial

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified; EEPROM in write condition.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode and SDA and SCL are tied to VSS.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS; SDA and SCL tied to VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

3.4 DC Characteristics: MTA85X1X-04 (COMMERCIAL, INDUSTRIAL) MTA85X1X-10 (COMMERCIAL, INDUSTRIAL) MTA85X1X-20 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS

Standard Operating Conditions
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ *	Max	Units	Conditions
Supply Voltage	VDD	3.0		6.25	V	XT, RC and LP options
		4.5		5.5	V	HS option
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See POR section in microcontroller datasheet for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See POR section in microcontroller datasheet for details on power on reset
Supply Current (Note 2)	IDD					XT and RC options
			2.8	6.0	mA	FOSC = 4 MHz, VDD = 5.5V
						HS option
			5.8	13	mA	FOSC = 4 MHz, VDD = 5.5V
			10	23	mA	FOSC = 20 MHz, VDD = 5.5V
			15	32	µA	LP option, Commercial
						FOSC = 32 KHz, VDD = 3.0V, WDT disabled
						LP option, Industrial
			19	40	µA	FOSC = 32 KHz, VDD = 3.0V, WDT disabled
Power Down Current (Note 4)						
WDT enabled	IPD		4	40	µA	VDD = 2.5V, Commercial
			5	14	µA	VDD = 2.5V, Industrial
WDT disabled			0.6	9	µA	VDD = 2.5V, Commercial
			0.8	12	µA	VDD = 2.5V, Industrial

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, except RB7 driving '1' for SEE VDD. RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified; EEPROM in write condition.
b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode and SDA and SCL are tied to VSS.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS; SDA and SCI tied to VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

3.5 DC Characteristics: MTA85XXX-04 (COMMERCIAL, INDUSTRIAL)
MTA85XXX-10 (COMMERCIAL, INDUSTRIAL)
MTA85XXX-20 (COMMERCIAL, INDUSTRIAL)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY

Standard Operating Conditions
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Input Low Voltage						
I/O ports	VIL	VSS		0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt trigger)		VSS		0.15 VDD	V	
RTCC (Schmitt trigger)		VSS		0.15 VDD	V	
OSC1 (Schmitt trigger)		VSS		0.15 VDD	V	RC option only (Note 5)
OSC1		VSS		0.3 VDD	V	XT, HS and LP options
Input High Voltage						
I/O ports	VIH	0.45 VDD		VDD	V	For all VDD (Note 6)
		2.0		VDD	V	4.0V < VDD ≤ 5.5V (Note 6)
		0.36 VDD		VDD	V	VDD > 5.5V
MCLR (Schmitt trigger)		0.85 VDD		VDD	V	
RTCC (Schmitt trigger)		0.85 VDD		VDD	V	
OSC1 (Schmitt trigger)		0.85 VDD		VDD	V	RC option only (Note 5)
OSC1		0.7 VDD		VDD	V	XT, HS and LP options
Input Leakage Current (Note 4)						**For VDD ≤ 5.5V**
I/O ports	IIL	-1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		-5			µA	VPIN = VSS + 0.25V (Note 3)
MCLR			0.5	+5	µA	VPIN = VDD (Note 3)
RTCC		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD ,
SDA, SCL		-10		10	µA	XT, HS and LP options
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT (RC option only)				0.6	V	IOL = 1.6 mA, VDD = 4.5V
SDA				0.4	V	IOL = 3.0 mA, VDD = 3.0V
Output High Voltage						
I/O Ports (Note 4)	VOH	VDD-0.7			V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT (RC option only)		VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : In RC oscillator mode, the OSC1 pin is a Schmitt trigger input. It is not recommended that the microcontroller be driven with external clock in RC mode.

Note 6: The user may use better of the two specifications.

3.6 AC Characteristics: MTA85XXX-04 (COMMERCIAL, INDUSTRIAL) MTA85XXX-10 (COMMERCIAL, INDUSTRIAL) MTA85XXX-20 (COMMERCIAL, INDUSTRIAL)

AC CHARACTERISTICS **Standard Operating Conditions**
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
External CLOCKIN Frequency (Note 2)	Fosc	DC		4	MHz	RC mode
		DC		4	MHz	XT mode
		DC		20	MHz	HS mode (Com/Ind) (Note 5)
		DC		40	KHz	LP mode
Oscillator Frequency (Note 2)	Fosc	DC		4	MHz	RC mode
		0.1		4	MHz	XT mode
		4		20	MHz	HS mode (Com/Ind) (Note 5)
		DC		40	KHz	LP mode
Instruction Cycle Time (Note 2)	TCY	1.0		DC	µs	RC mode
		1.0	4/Fosc	DC	µs	XT mode
		0.2		DC	µs	HS mode (Note 5)
		100		DC	µs	LP mode
External Clock in Timing (Note 4)						
Clock in (OSC1) High or Low Time						
XT oscillator type	TCKHLXT	50*			ns	
LP oscillator type	TCKHLLP	2*			µs	
HS oscillator type	TCKHLHS	20*			ns	
Clock in (OSC1) Rise or Fall Time						
XT oscillator type	TCKRFXT	25*			ns	
LP oscillator type	TCKRFLP	50*			ns	
HS oscillator type	TCKRFHS	25*			ns	
RESET Timing						
$\overline{MCLR}$ Pulse Width (low)	TMCL	100*			ns	
RTCC Input Timing, No Prescaler						
RTCC High Pulse Width	TRTH	0.5 TCY+ 20*			ns	Note 3
RTCC Low Pulse Width	TRTL	0.5 TCY+ 20*			ns	Note 3
RTCC Input Timing, With Prescaler						
RTCC High Pulse Width	TRTH	10*			ns	Note 3
RTCC Low Pulse Width	TRTL	10*			ns	Note 3
RTCC Period	TRTP	$\frac{TCY + 4C}{N}$ *			ns	Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Time-out Period (No Prescaler)	TWDT	9*	18*	30*	ms	VDD = 5.0V
Oscillation Start-up Timer Period	TOST	9*	18*	30*	ms	VDD = 5.0V
I/O Timing						
I/O Pin Input Valid Before CLKOUT↑ (RC Mode)	TDS	0.25 TCY+ 30*			ns	
I/O Pin Input Hold After CLKOUT↑ (RC Mode)	TDH	0*			ns	
I/O Pin Output Valid After CLKOUT↓ (RC Mode)	TPD			40*	ns	

* Guaranteed by characterization, but not tested.

(Cont. on next page)

3.6 AC Characteristics: MTA85XXX-04 (COMMERCIAL, INDUSTRIAL) MTA85XXX-10 (COMMERCIAL, INDUSTRIAL) MTA85XXX-20 (COMMERCIAL, INDUSTRIAL)

AC CHARACTERISTICS **Standard Operating Conditions**
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
I/O Timing (cont.)						
I/O pin input valid before OSC↑ (I/O setup time)	TioV2osH	TBD			ns	
OSC1↑ to I/O pin input invalid (I/O hold time)	TosH2ioL	TBD			ns	
OSC1↑ to I/O pin output valid	TosH2ioV			TBD	ns	
I/O pin output rise time	TioR			TBD	ns	
I/O pin output fall time	TioF			TBD	ns	
Capacitive Loading Specs on Output Pins						
OSC2 pin	Cosc2			15	pF	In XT, HS or LP modes when external clock is used to drive OSC1
All I/O pins	Cio			50	pF	Excludes RB7 on MTA85X1X devices

* Guaranteed by characterization, but not tested.

Note 1. Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2. Instruction cycle period (Tcy) equals four times the input oscillator time base period.
All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "minimum" values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.

Note 3. For a detailed explanation of RTCC input clock requirements see microcontroller datasheet Section 4.2.1.

Note 4. Clock-in high-time is the duration for which clock input is at VIHOSC or higher.
Clock-in low-time is the duration for which clock input is at VILOSC or lower.

Note 5. This HS specification is only for the -20 device. The -10 device has a maximum of 10 MHz and the -04 device has a maximum of 4 MHz.

FIGURE 3.6.1 - EEPROM BUS START/STOP TIMING

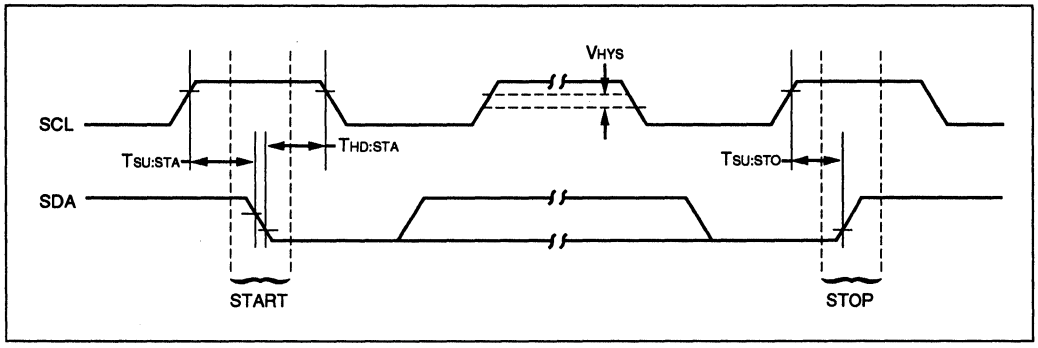

FIGURE 3.6.2 - BUS TIMING DEFINITIONS

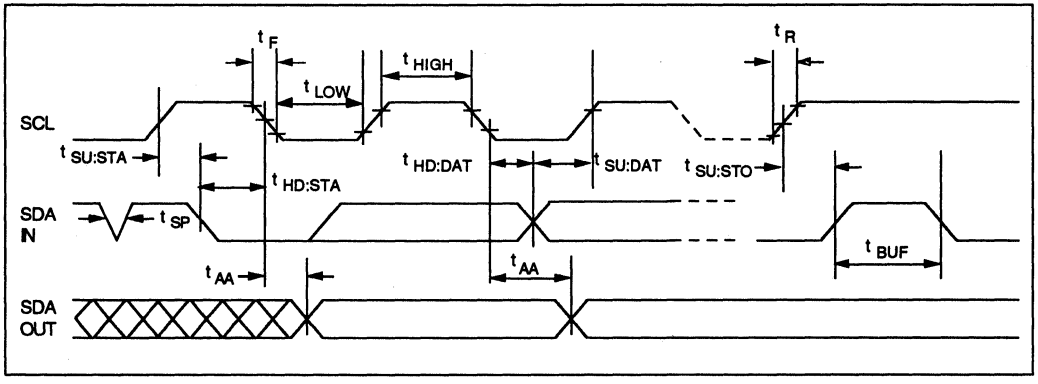

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TABLE 3.6.2 - AC CHARACTERISTICS OF EEPROM

AC CHARACTERISTICS		STANDARD MODE		Vcc = 4.5-5.5V FAST MODE			
Parameter	Symbol	Min	Max	Min	Max	Units	Remarks
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	UF	300	ns	Note 2
SDA and SCL fall time	TF	—	300	UF	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	Note 1
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	100,000	—	100,000	—	E/W Cycles	

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

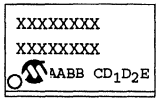
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4.0 PACKAGE OUTLINES

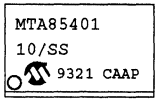
See Section 11 of the Data Book.

5.0 PACKAGE MARKING INFORMATION

20L SSOP



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D_1	Mask revision number for microcontroller
	D_2	Mask revision number for EEPROM
	E	Assembly code of the plant or country of origin in which part was assembled.
Note:	In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask revision number, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are incuded in QTP price.

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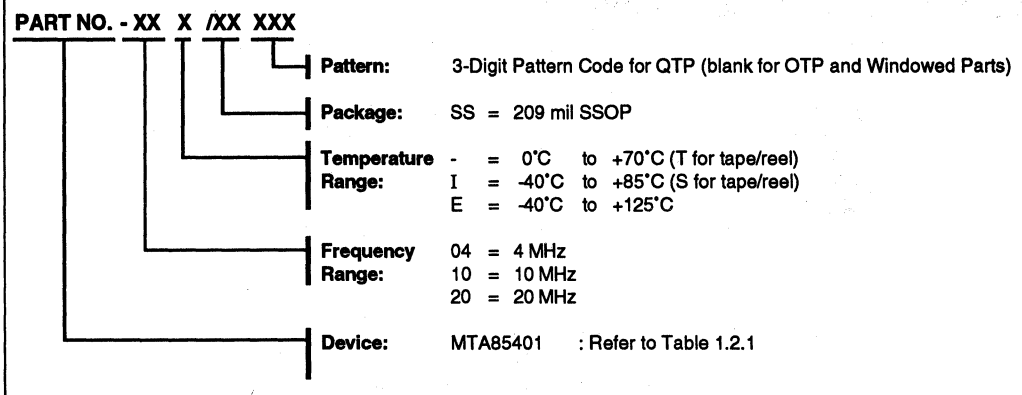
SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices. Refer to Table 1.2.1.



Examples:
a) MTA85402 - 04/SS 301 = Commercial temperature, SSOP package, 4 MHz, QTP pattern # 301
b) MTA85811 - 10I/SS = Industrial temperature, SSOP package, 10 MHz

MICROCHIP

SECTION 5
SERIAL EEPROM PRODUCT SPECIFICATIONS

5

MICROCHIP

Serial EEPROMs

Serial EEPROM Selection Guide

CMOS Serial EEPROMs

2-Wire Bus Protocol

Device	Compat-ibility	Density/ Organization	Page Buffer	Write Speed	Max Clock Freq.	Endur-ance (min.)*	Temp Range	# Pins	Package Types	Operating Voltage
24C01A	Industry	1K bits (128 x 8)	2 bytes	1 ms/byte	100 KHz	100K	C, I, E	8	P,SN,SM	4.5V - 5.5V
24C02A	Industry	2K bits (256 x 8)	2 bytes	1 ms/byte	100 KHz	100K	C, I, E	8	P,SN,SM	4.5V - 5.5V
24C04A	Industry	4K bits (512 x 8)	8 bytes	1 ms/byte	100 KHz	100K	C, I, E	8, 14	P,SN,SM,SL	4.5V - 5.5V
85C72	Philips	1K bits (128 x 8)	2 bytes	1 ms/byte	100 KHz	100K	C, I, E	8	P,SM	4.5V - 5.5V
85C82	Philips	2K bits (256 x 8)	2 bytes	1 ms/byte	100 KHz	100K	C, I, E	8	P,SM	4.5V - 5.5V
85C92	Philips	4K bits (512 x 8)	8 bytes	1 ms/byte	100 KHz	100K	C, I, E	8, 14	P,J,SM,SL	4.5V - 5.5V
24LC01B	Industry	1K bits (128 x 8)	8 bytes	10 ms	400 KHz	100K	C, I	8	P,SN,SM	2.5V - 5.5V
24AA01	Industry	1K bits (128 x 8)	8 bytes	10 ms	400 KHz	100K	C	8	P,SN,SM	1.8V - 5.5V
24LC02B	Industry	2K bits (256 x 8)	8 bytes	10 ms	400 KHz	100K	C, I	8	P,SN,SM	2.5V - 5.5V
24AA02	Industry	2K bits (256 x 8)	8 bytes	10 ms	400 KHz	100K	C	8	P,SN,SM	1.8V - 5.5V
24LC04B	Industry	4K bits (512 x 8)	16 bytes	10 ms	400 KHz	100K	C, I	8, 14	P,SN,SM,SL	2.5V - 5.5V
24AA04	Industry	4K bits (512 x 8)	16 bytes	10 ms	400 KHz	100K	C	8, 14	P,SN,SM,SL	1.8V - 5.5V
24LC08B	Industry	8K bits (1K x 8)	16 bytes	10 ms	400 KHz	100K	C, I	8, 14	P,SN,SM,SL	2.5V - 5.5V
24AA08	Industry	8K bits (1K x 8)	16 bytes	10 ms	400 KHz	100K	C	8, 14	P,SN,SM,SL	1.8V - 5.5V
24LC16B	Industry	16K bits (2K x 8)	16 bytes	10 ms	400 KHz	100K	C, I	8, 14	P,SN,SL	2.5V - 5.5V
24AA16	Industry	16K bits (2K x 8)	16 bytes	10 ms	400 KHz	100K	C	8, 14	P,SN,SL	1.8V - 5.5V
24LC164	Atmel, Xicor	16K bits (2K x 8)	16 bytes	10 ms	400 KHz	100K	C, I	8	P, SN	2.5V - 5.5V
24AA164	Atmel, Xicor	16K bits (2K x 8)	16 bytes	10 ms	400 KHz	100K	C	8	P, SN	1.8V - 5.5V
24LC174	Sole Source	16K bits (2K x 8) + 16 bytes	16 bytes	10 ms	400 KHz	100K	C, I	8	P, SN	2.5V - 5.5V
24AA174	Sole Source	16K bits (2K x 8) +16 bytes	16 bytes	10 ms	400 KHz	100K	C	8	P, SN	1.8V - 5.5V
24C32	Sole Source	32K bits (4K x 8)	64 bytes	5 ms/pg	400 KHz	100K/10K	C,I	8	P,SM	4.5V - 5.0V
24LC32	Sole Source	32K bits (4K x 8)	64 bytes	5 ms/pg	400 KHz	100K/10K	C,I	8	P,SM	2.5V - 6.0V
24C65	Sole Source	64K bits (8K x 8)	64 bytes	5 ms/pg	400 KHz	100K/5K	C,I	8	P,SM	4.5V - 5.5V
24LC65	Sole Source	64K bits (8K x 8)	64 bytes	5 ms/pg	400 KHz	100K/5K	C,I	8	P,SM	2.5V - 6.0V
24AA65	Sole Source	64K bits (8K x 8)	64 bytes	5 ms/pg	100 KHz	100K/5K	C	8	P,SM	1.8V - 6.0V

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CMOS Serial EEPROMs (Cont.)

3-Wire/4-Wire Bus Protocol

Device	Compat-ibility	Density/ Organization	Page Buffer	Write Speed	Max Clock Freq.	Endur-ance (min.)*	Temp Range	# Pins	Package Types	Operating Voltage
5911	Industry	1K bits (x8 or x16)	N/A	1 ms/byte	1 MHz	100K	C, I, E	8	P,SN,SM	4.5V - 5.5V
93C06	Industry	256 bits (16 x 16)	N/A	1 ms/byte	1 MHz	100K	C, I, E	8	P,SN,SM	4.5V - 5.5V
93C46	Industry	1K bits (64 x 16)	N/A	1 ms/byte	1 MHz	100K	C, I, E	8	P,SN,SM	4.5V - 5.5V
93C56	Industry	2K bits (x8 or x16)	N/A	1ms/byte	2 MHz	100K	C, I, E	8, 14	P,SN, SM,SL	4.5V - 5.5V
93C66	Industry	4K bits (x8 or x16)	N/A	1ms/byte	2 MHz	100K	C, I, E	8, 14	P,SN,SM,SL	4.5V - 5.5V
93LC46	Industry	1K bits (x8 or x16)	N/A	10 ms	2 MHz	100K	C, I	8	P,SN,SM	2.0V - 6.0V
93LC56	Industry	2K bits (x8 or x16)	N/A	10 ms	2 MHz	100K	C, I	8, 14	P,SN,SM,SL	2.0V - 6.0V
93LC66	Industry	4K bits (x8 or x16)	N/A	10 ms	2 MHz	100K	C, I	8, 14	P,SN,SM,SL	2.0V - 6.0V

3-Wire Bus Protocol

Device	Compat-ibility	Density/ Organization	Page Buffer	Write Speed	Max Clock Freq.	Endur-ance (min.)*	Temp Range	# Pins	Package Types	Operating Voltage
93AA46	Atmel	1K bits (x8 or x16)	N/A	10 ms	2 MHz	100K	C	8	P,SN,SM	1.8V - 5.5V
93AA56	Atmel	2K bits (x8 or x16)	N/A	10 ms	2 MHz	100K	C	8	P,SN,SM	1.8V - 5.5V
93AA66	Atmel	4K bits (x8 or x16)	N/A	10 ms	2 MHz	100K	C	8	P,SN,SM	1.8V - 5.5V
93LC46B	National	1K bits (64 x 16)	N/A	10 ms	2 MHz	100K	C, I	8	P,SN,SM	2.0 - 6.0V
93LC56B	National	2K bits (128 x 16)	N/A	10 ms	2 MHz	100K	C, I	8	P,SN,SM	2.0 - 6.0V
93LC66B	National	4K bits (256 x 16)	N/A	10 ms	2 MHz	100K	C, I	8	P,SN,SM	2.0 - 6.0V
93LCS56	National	2K bits (128 x 16)	N/A	10 ms	2 MHz	100K	C, I	8, 14	P,SN,SM,SL	2.5V - 6.0V
93LCS66	National	4K bits (256 x 16)	N/A	10 ms	2 MHz	100K	C, I	8, 14	P,SN,SM,SL	2.5V - 6.0V

PACKAGES

P = Plastic DIP
SN = .150" 8ld SOIC
S = Dice in Wafflepack
J = Ceramic DIP
SM = .207" 8ld SOIC
L = PLCC
SL = .150" 14ld SOIC
W = Dice in Wafer Form
VS = 28ld VSOP (8x13.4mm)
K = Ceramic LCC
SO = .300" 28ld SOIC
TS = 28ld TSOP (8x20mm)

* Endurance is guaranteed to 10K cycles at extended (-40°C to +125°C) temperature.

NOTE: NOT ALL COMBINATIONS OF SPEED/TEMPERATURE RANGE/PACKAGE/ETC. ARE AVAILABLE. CONSULT FACTORY FOR SPECIFIC PART INFORMATION.

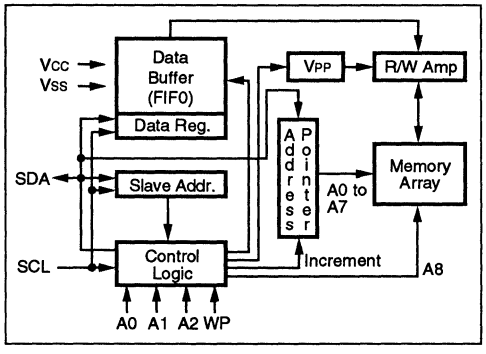
24C01A/02A/04A

1K/2K/4K 5V CMOS Serial EEPROMs

FEATURES

- Low power CMOS technology
- Hardware write protect
- Two wire serial interface bus, I²C™ compatible
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer
- 1ms write cycle time for single byte
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention >40 years
- 8-pin DIP/SOIC packages
- Available for extended temperature ranges:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C
  —Automotive: -40°C to +125°C

BLOCK DIAGRAM



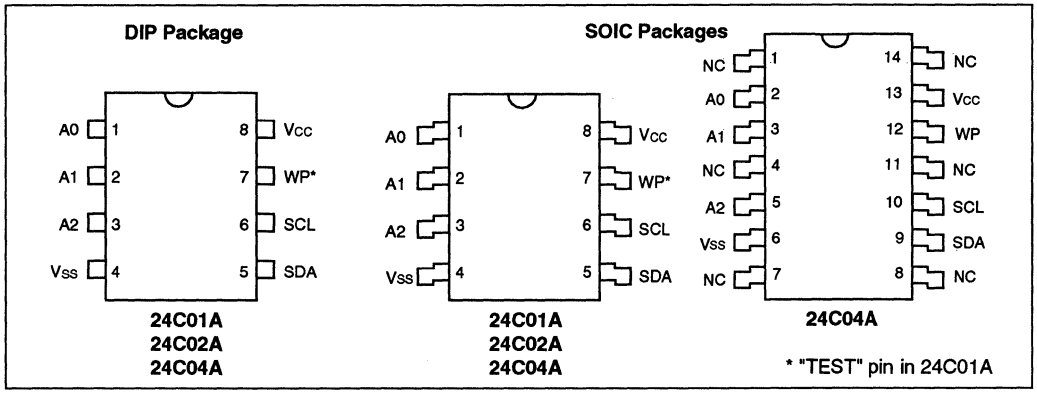
DESCRIPTION

The Microchip Technology Inc. 24C01A/02A/04A is a 1K/2K/4K bit Electrically Erasable PROM. The device is organized as shown, with a standard two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature provides hardware write protection for the upper 256 byte block. The 24C01A/02A/04A also has a page-write capability for up to 8 bytes of data (see chart). Up to four 24C01A/02A/04As may be connected to the two wire bus. The 24C01A/02A/04A is available in the standard 8-pin DIP and 8-pin surface mount SOIC package.

This device offers fast (1ms) byte write and extended (-40°C to 125°C) temperature operation. It is recommended that all other applications use Microchip's 24LCXXB.

	24C01A	24C02A	24C04A
Organization	128 x 8	256 x 8	2 x 256 x 8
Write Protect	None	080-0FF	100-1FF
Page Write Buffer	2 Bytes	2 Bytes	8 Bytes

PIN CONFIGURATIONS



I²c is a trademark of Philips Corporation

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0	No Function for 24C04A only, Must be connected to VCC or VSS
A0, A1, A2	Chip Address Inputs
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
TEST	(24C01A only) VCC or VSS
WP	Write Protect Input
VCC	+5V Power Supply

DC CHARACTERISTICS

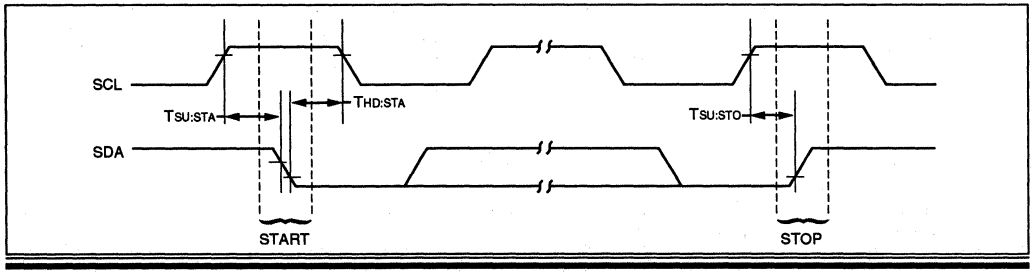
VCC = +5V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C (Note 2)

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	VCC x 0.7	VCC + 1	V	
Low level input voltage	VIL	-0.3	VCC x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A1 & A2 pins:					
High level input voltage	VIH	VCC - 0.5	VCC + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI	—	10	µA	VIN = 0V to VCC
Output leakage current	ILO	—	10	µA	VOUT = 0V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	7.0	pF	VIN/VOUT = 0V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICC write	—	3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, VCC = 5V, Tamb = 0°C to +70°C
	ICC write	—	4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, VCC = 5V, Tamb = (I) and (E)
	ICC read	—	750	µA	VCC = 5V, Tamb= (C), (I) and (E)
Standby current	ICCS	—	100	µA	SDA = SCL = VCC = 5V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles

BUS TIMING START/STOP

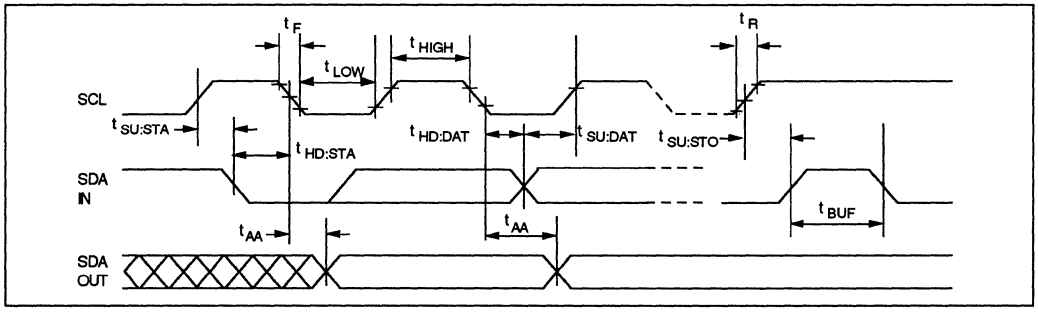


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK	—	—	100	kHz	
Clock high time	THIGH	4000	—	—	ns	
Clock low time	TLOW	4700	—	—	ns	
SDA and SCL rise time	TR	—	—	1000	ns	
SDA and SCL fall time	TF	—	—	300	ns	
START condition hold time	THD:STA	4000	—	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	—	ns	
Data input setup time	TSU:DAT	250	—	—	ns	
Data output delay time	TPD	300	—	3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700	—	—	ns	
Bus free time	TBUF	4700	—	—	ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI	—	—	100	ns	
Program cycle time	TWC	—	.4 .4N	1 N	ms ms	Byte Mode Page Mode, N = # of bytes
Endurance	—	100,000	—	—	E/W Cycles	

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

FIGURE 2 - BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C01A/02A/04A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C01A/02A/04A works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to four 24C01A/02A/04As can be connected to the bus, selected by the A1 and A2 chip address inputs. A0 must be tied to Vcc or Vss. Other devices can be connected to the bus but require different device codes than the 24C01A/02A/04A (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

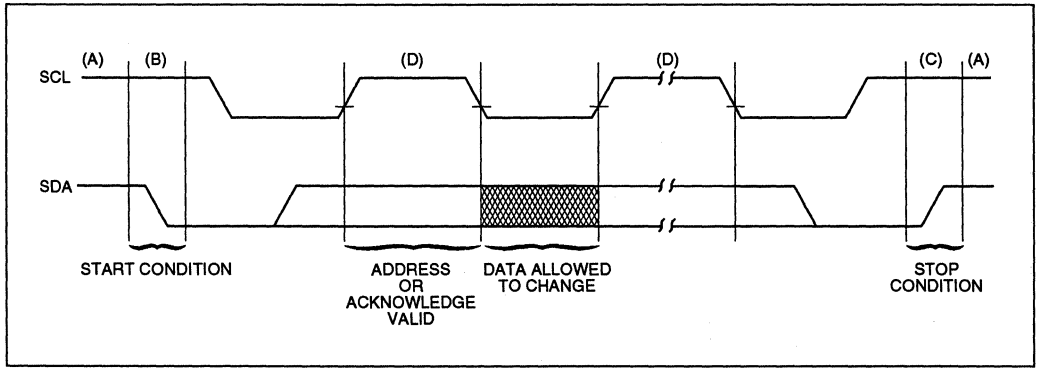
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C01A/02A/04A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

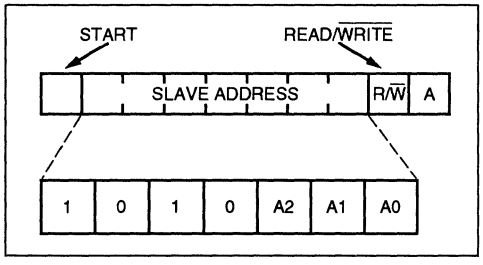
The chip address inputs A1 and A2 of each 24C01A/02A/04A must be externally connected to either Vcc or ground (Vss), assigning to each 24C01A/02A/04A a unique 2-bit address. Up to four 24C01A/02A/04As may be connected to the bus. Chip selection is then accomplished through software by setting the bits A1 and A2 of the slave address to the corresponding hard-wired logic levels of the selected 24C01A/02A/04A. A0 is not used and must be connected to either Vcc or Vss.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C01A/02A/04A, followed by the chip address bits A1 and A2. In the 24C04A, the seventh bit of that byte (BA) is used to select the upper block (addresses 100—1FF) or the lower block (addresses 000—0FF) of the array.

The eighth bit of slave address determines if the master device wants to read or write to the 24C01A/02A/04A (see Figure 2).

The 24C01A/02A/04A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 24C01A/02A/04A.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C01A/02A/04A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C01A/02A/04A. After receiving the acknowledge of the 24C01A/02A/04A, the master device transmits the data word to be written into the addressed memory location. The 24C01A/02A/04A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 24C01A/02A/04A (see Figure 3).

PAGE PROGRAM MODE

To program the 24C01A/02A/04A, the master sends addresses and data to the 24C01A/02A/04A which is the slave (see Figure 3 and 4). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C01A/02A/04A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (The BA bit transmitted with the slave address is the ninth bit of the address pointer). The 24C01A/02A/04A will generate an acknowledge after every 8-bits received and store them consecutively in a 2-byte or 8-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 8 bytes (2 bytes in 24C01A/02A) are transmitted by the master, the 24C01A/02A/04A will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address registers bottom 3 bits to increment while the upper 5 bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received data bytes in the page buffer will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 8 for 24C04A, 2 for 24C01A/02A).

FIGURE 3 - BYTE WRITE

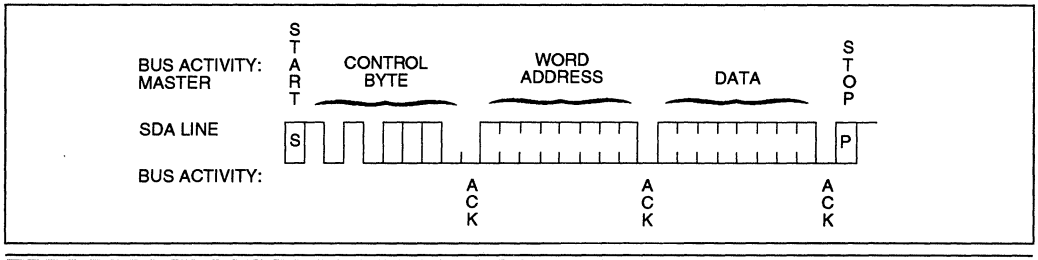
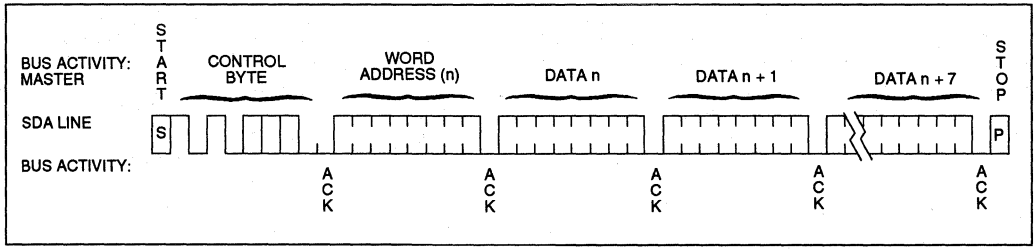


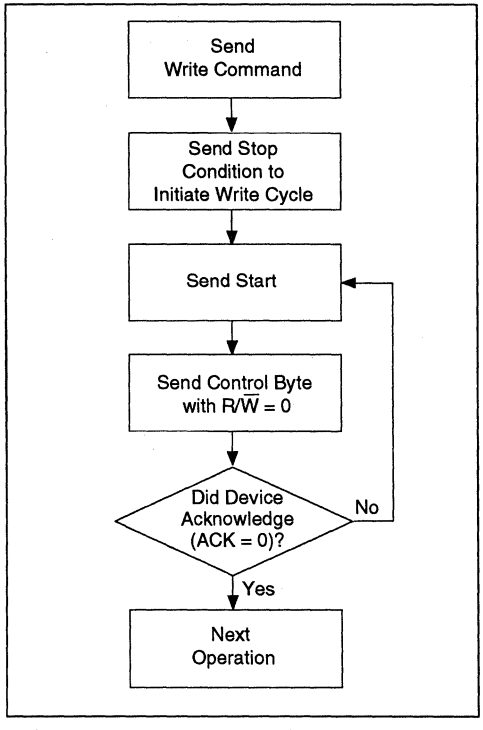
FIGURE 4 - PAGE WRITE



ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5 for flow diagram.

FIGURE 5 - ACKNOWLEDGE POLLING FLOW



WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the 24C02A or 24C04A is connected to Vcc (+5V). The device will accept slave and word addresses but if the memory accessed is write protected by the WP pin, the 24C02A/04A will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the STOP condition is asserted. Polarity of the WP pin has no effect on the 24C01A.

READ MODE

This mode illustrates master device reading data from the 24C01A/02A/04A.

As can be seen from Figures 7 and 8, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to). During this period the 24C01A/02A/04A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This auto-increment sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at the current address (see Figure 6) and save time transmitting the slave and word addresses.

Note: In all modes, the address pointer will not increment through a block (256 byte) boundary, but will rotate back to the first location in that block.

FIGURE 6 - CURRENT ADDRESS READ

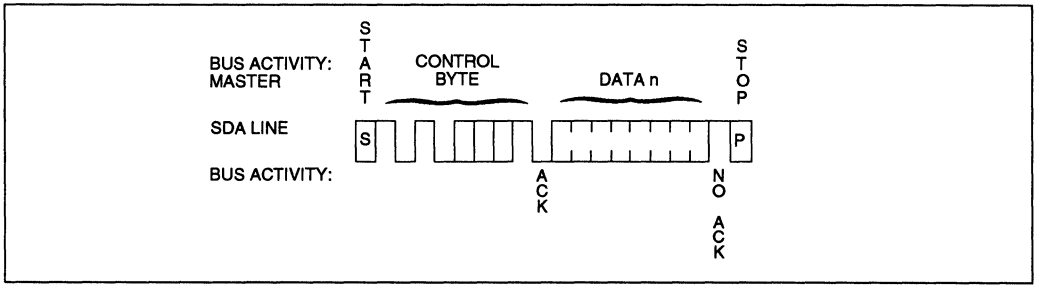


FIGURE 7 - RANDOM READ

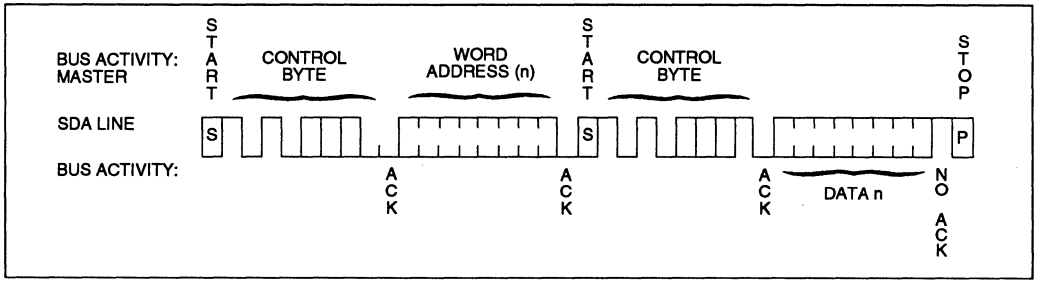
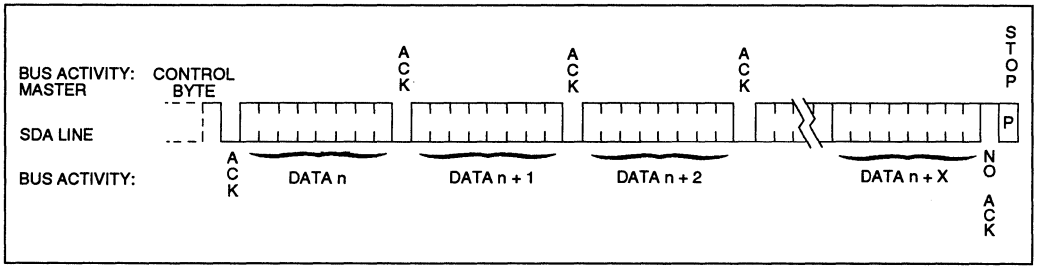


FIGURE 8 - SEQUENTIAL READ



PIN DESCRIPTION

A0, A1, A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true. For 24C04 A0 is no function.

Up to eight 24C01A/02A's or up to four 24C04A's can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10KΩ).

For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP Write Protection

This pin must be connected to either Vcc or Vss for 24C02A or 24C04A. It has no effect on 24C01A.

If tied to Vcc, PROGRAM operations onto the upper memory block will not be executed. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Notes:

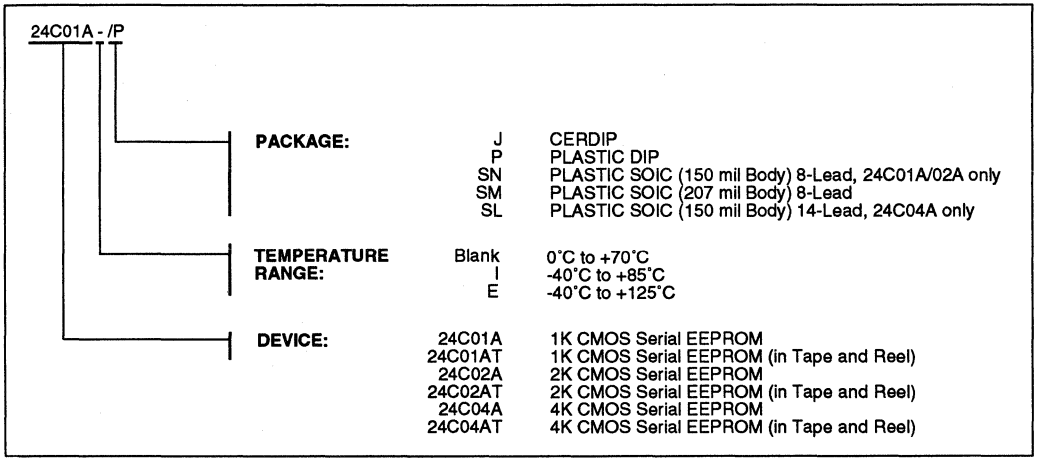
1. A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 24C04A page is 8 bytes long; the 24C01A/02A page is 2 bytes long.
2. A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 24C01A/02A/04A has two blocks, 256 bytes each. The 24C01A and 24C02A each have only one block.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



MICROCHIP

24LC01B/02B

1K/2K 2.5V CMOS Serial EEPROMs

FEATURES

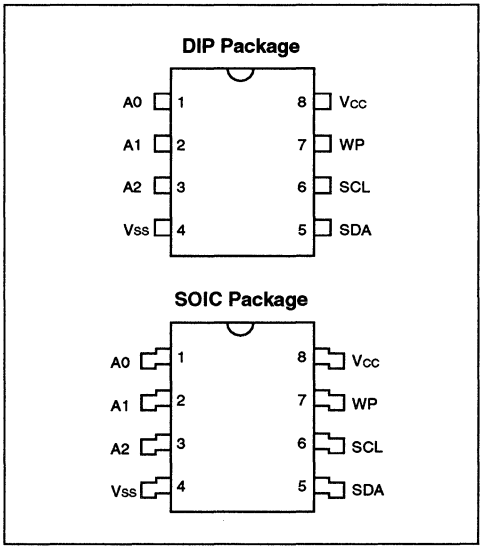
- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as a single block of 128 bytes (128 x 8) or 256 bytes (256 x 8)
- Two wire serial interface bus, I²C™ compatible
- 100KHz (2.5V) and 400KHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 3,000V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP or SOIC package
- Available for extended temperature ranges
  - Commercial: 0°C to + 70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

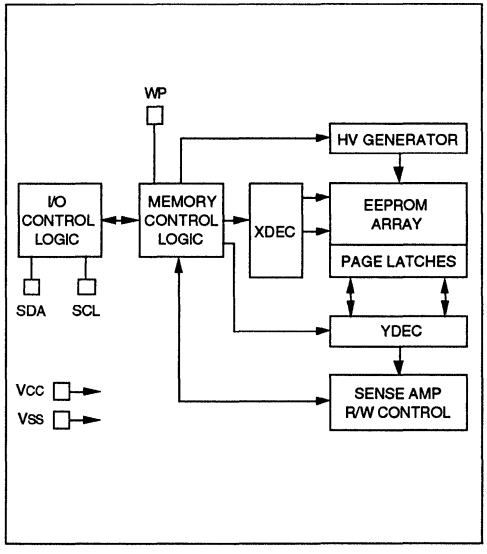
The Microchip Technology Inc. 24LC01B and 24LC02B are 1K bit and 2K bit Electrically Erasable PROMs. The devices are organized as a single block of 128 x 8 bit or 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 2.5 volts with a standby and active currents of only 5 µA and 1 mA respectively. The 24LC01B and 24LC02B also have page-write capability for up to 8 bytes of data. The 24LC01B and 24LC02B are available in the standard 8-pin DIP and an 8-pin surface mount SOIC package.

5

PIN CONFIGURATION



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+2.5V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

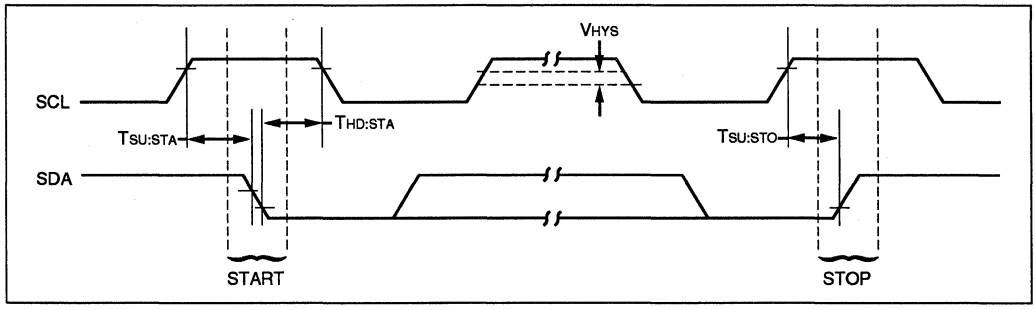
DC CHARACTERISTICS

VCC = +2.5V to +5.5V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min	Max	Units	Conditions
WP, SCL and SDA pins: High level input voltage	VIH	.7 VCC		V	
Low level input voltage	VIL		.3 VCC	V	
Hysteresis of Schmidt trigger inputs	VHYS	0.05 VDD	—	V	Note 1
Low level output voltage	VOL		.40	V	IOL = 3.0 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to 5.5V
Output leakage current	ILO	-10	10	µA	VOUT = .1V to 5.5V
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC write	—	3	mA	VCC = 5.5V SCL = 400 KHz
	ICC read	—	1	mA	
Standby current	ICCS	—	30	µA	VCC = 3.0V SDA = SCL = VCC
			100	µA	VCC = 5.5V SDA = SCL = VCC

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP



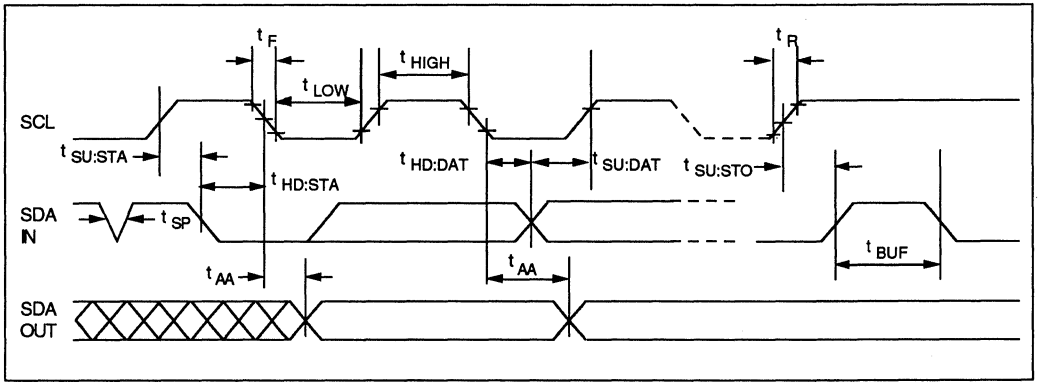
AC CHARACTERISTICS		STANDARD MODE		Vcc = 4.5-5.5V FAST MODE			
Parameter	Symbol	Min	Max	Min	Max	Units	Remarks
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	Note 1
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	100,000	—	100,000	—	E/W Cycles	

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24LC01B/02B supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC01B/02B works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

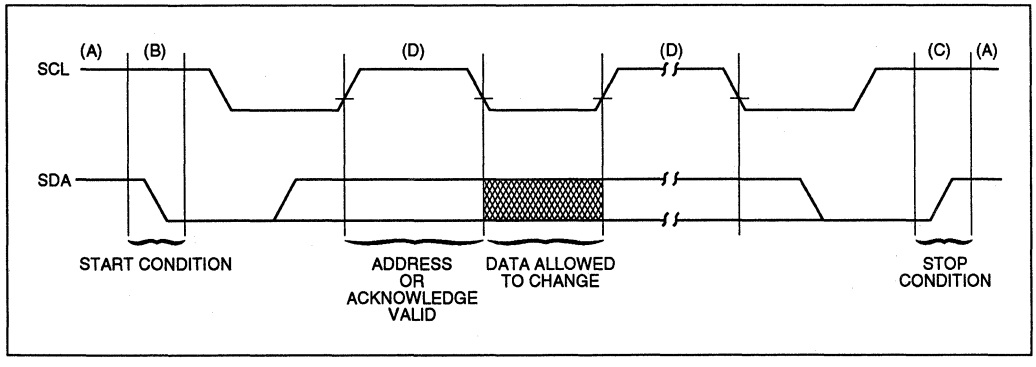
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC01B/02B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

Slave Address

The 24LC01B/02B are software-compatible with older devices such as 24C01A, 24C02A, 24LC01, and 24LC02. A single 24LC02B can be used in place of two 24LC01's, for example, without any modifications to software. The "chip select" portion of the control byte becomes a don't care.

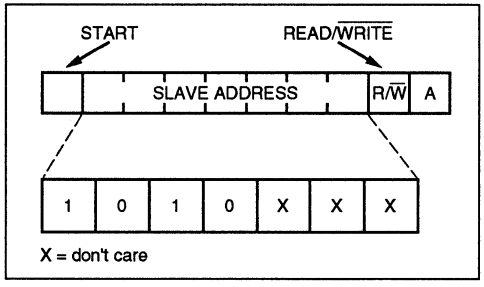
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24LC01B/02B, followed by three don't care bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24LC01B/02B (see Figure 2).

The 24LC01B/02B monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXX	1
Write	1010	XXX	0

FIGURE 2 - CONTROL BYTE ALLOCATION



WRITE OPERATION

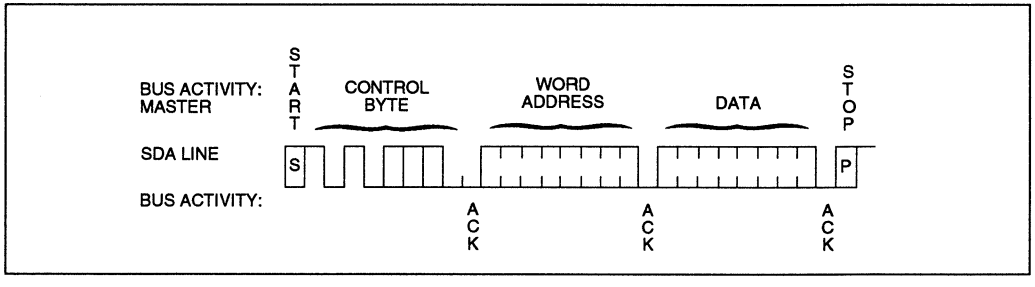
Byte Write

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC01B/02B. After receiving another acknowledge signal from the 24LC01B/02B the master device will transmit the data word to be written into the addressed memory location. The 24LC01B/02B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC01B/02B will not generate acknowledge signals (see Figure 3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC01B/02B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LC01B/02B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 5).

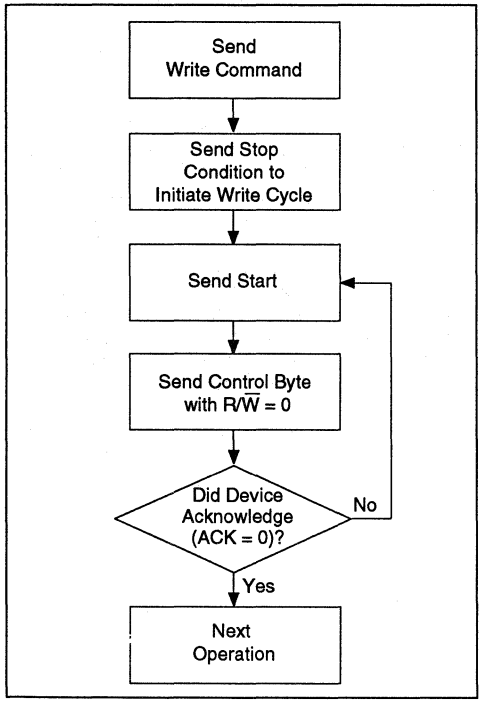
FIGURE 3 - BYTE WRITE



ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 4 for flow diagram.

FIGURE 4 - ACKNOWLEDGE POLLING FLOW



WRITE PROTECTION

The 24LC01B/02B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24LC01B/02B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC01B/02B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC01B/02B discontinues transmission (see Figure 6).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC01B/02B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC01B/02B will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC01B/02B discontinues transmission (see Figure 7).

FIGURE 5 - PAGE WRITE

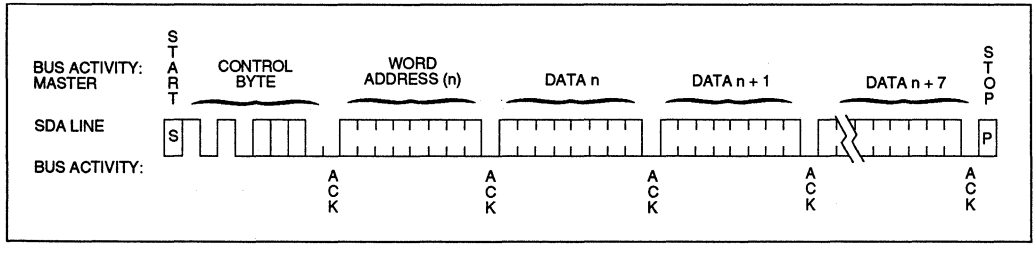


FIGURE 6 - CURRENT ADDRESS READ

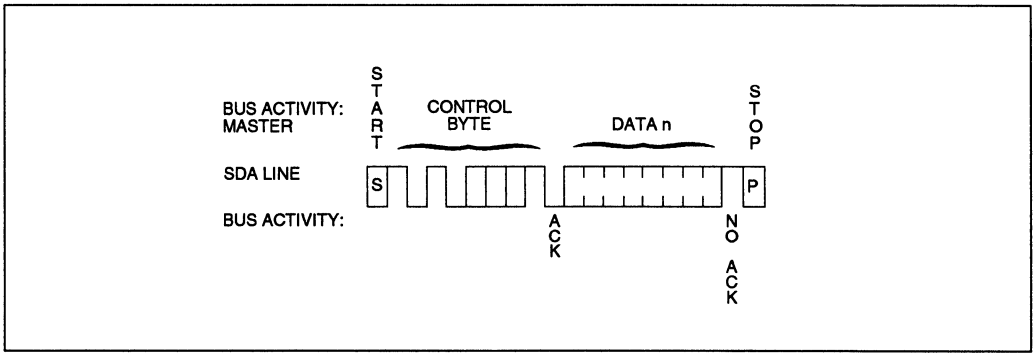
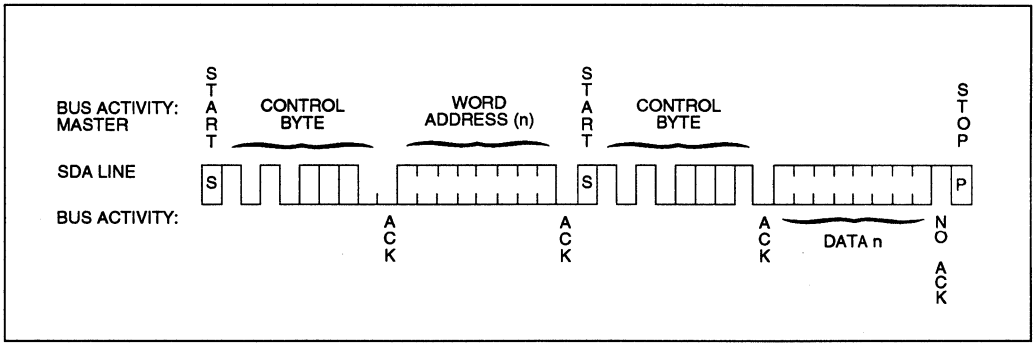


FIGURE 7 - RANDOM READ



5

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC01B/02B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC01B/02B to transmit the next sequentially addressed 8 bit word (see Figure 8).

To provide sequential reads the 24LC01B/02B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The 24LC01B/02B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

PIN DESCRIPTIONS

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 KHz, 1KΩ for 400 KHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

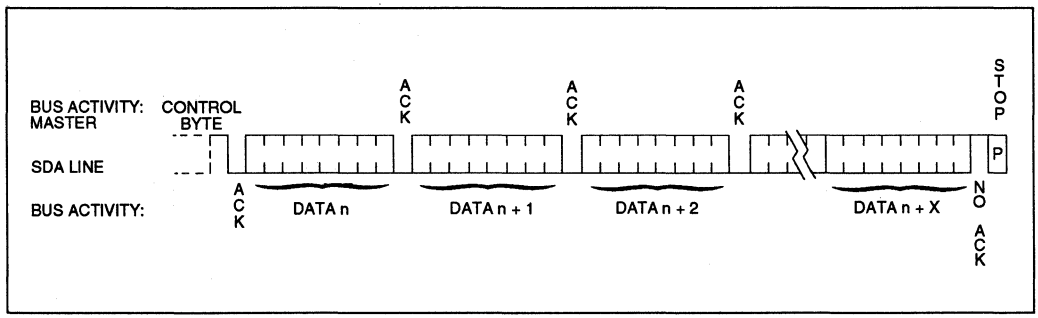
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC01B/02B as a serial ROM when WP is enabled (tied to Vcc).

A0, A1, A2

These pins are not used by the 24LC01B/02B. They may be left floating or tied to either Vss or Vcc.

FIGURE 8 - SEQUENTIAL READ



NOTES

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the sales offices below or contact corporate headquarters for the representative or distributor in your area.

PART NUMBERS

24LC01B - /P

PACKAGE:		P	PLASTIC DIP
		SN	PLASTIC SOIC (150 mil Body)
		SM	PLASTIC SOIC (207 mil Body)
TEMPERATURE RANGE:		Blank	0° C to +70° C
		I	-40° C to +85° C
DEVICE:		24LC01B	1K CMOS Serial EEPROM
		24LC01BT	1K CMOS Serial EEPROM (in Tape and Reel form)
		24LC02B	2K CMOS Serial EEPROM
		24LC02BT	2K CMOS Serial EEPROM (in Tape and Reel form)

MICROCHIP

24AA01/02

1K/2K 1.8V CMOS Serial EEPROMs

FEATURES

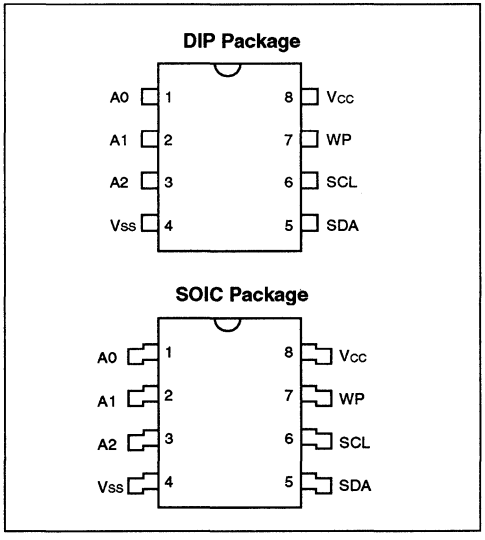
- Single supply with operation down to 1.8V
- Low power CMOS technology
  - — 1 mA active current typical
  - — 10 µA standby current typical at 5.5V
  - — 3 µA standby current typical at 1.8V
- Organized as a single block of 128 bytes (128 x 8) or 256 bytes (256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 KHz (1.8V) and 400 KHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 3,000V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges
  - — Commercial: 0°C to +70°C

DESCRIPTION

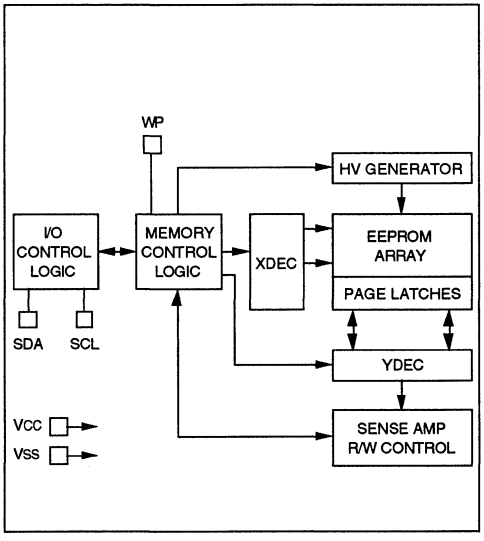
The Microchip Technology Inc. 24AA01 and 24AA02 are 1K bit and 2K bit Electrically Erasable PROMs. The devices are organized as a single block of 128 x 8 bit or 256 x 8 bit memory with a two wire serial interface. Low-voltage design permits operation down to 1.8 volts with standby and active currents of only 3 µA and 1 mA, respectively. The 24AA01 and 24AA02 also have page-write capability for up to 8 bytes of data. The 24AA01 and 24AA02 are available in the standard 8-pin DIP and 8-pin surface mount SOIC packages.

5

PIN CONFIGURATION



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+1.8V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

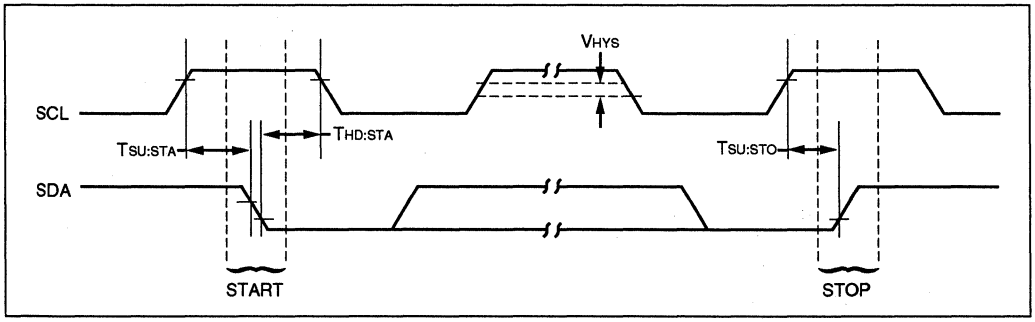
DC CHARACTERISTICS

Vcc = +1.8V to +5.5V
Commercial (C): Tamb = 0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
WP, SCL and SDA pins: High level input voltage	VIH	.7 Vcc	—	—	V	
Low level input voltage	VIL	—	—	.3 Vcc	V	
Hysteresis of Schmitt trigger inputs	VHYS	0.05 VDD	—	—	V	Note 1
Low level output voltage	VOL	—	—	.40	V	IOL = 3.0 mA, Vcc = 1.8V
Input leakage current	ILI	-10	—	10	µA	VIN = .1V to 5.5V
Output leakage current	ILO	-10	—	10	µA	VOUT = .1V to 5.5V
Internal capacitance (all inputs/outputs)	CINT	—	—	10	pF	Vcc = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	—	3	mA	Vcc = 5.5V, SCL = 400 KHz
		—	0.5	—	mA	Vcc = 1.8V, SCL = 100 KHz
	ICC Read	—	—	1	mA	Vcc = 5.5V, SCL = 400 KHz
		—	0.05	—	mA	Vcc = 1.8V, SCL = 100 KHz
Standby current	ICCS	—	—	100	µA	Vcc = 5.5 V, SDA = SCL = Vcc
		—	—	30	µA	Vcc = 3.0 V, SDA = SCL = Vcc
		—	3	—	µA	Vcc = 1.8 V, SDA = SCL = Vcc

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP



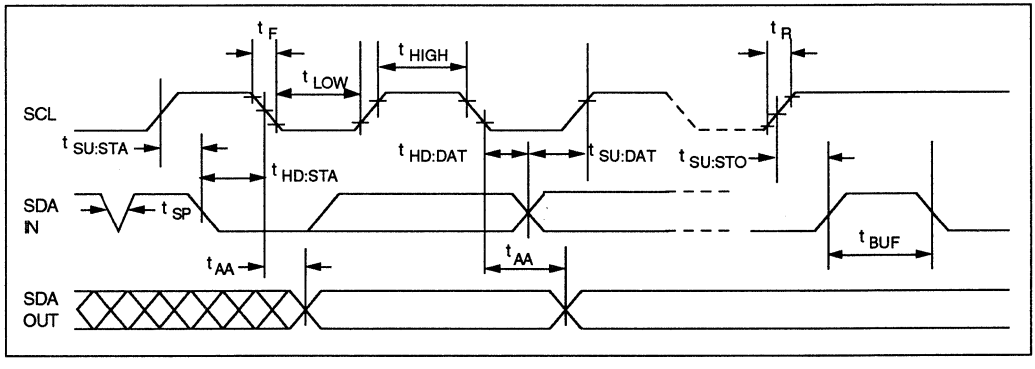
AC CHARACTERISTICS		STANDARD MODE		Vcc = 4.5-5.5V FAST MODE			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**	**Remarks**
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	Note 1
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3.
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	100,000	—	100,000	—	E/W Cycles	1,000,000 typical

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24AA01/02 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA01/02 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

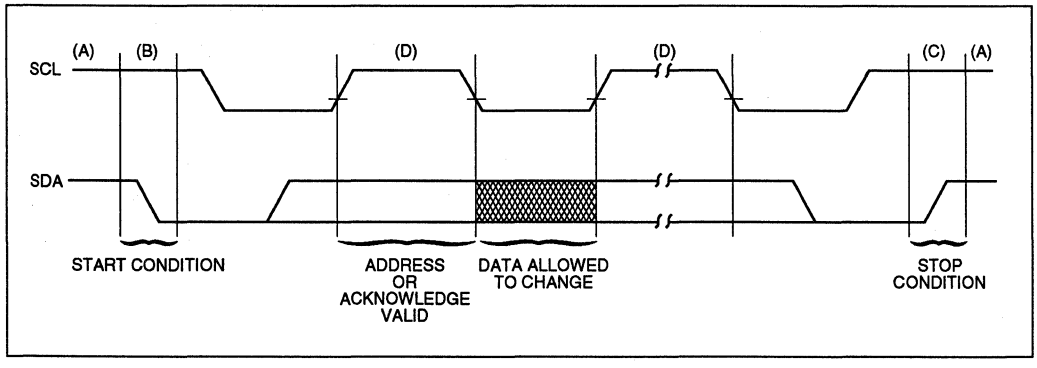
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA01/02 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

Slave Address

The 24AA01/02 are software-compatible with older devices such as 24C01A, 24C02A, 24LC01, and 24LC02. A single 24AA02 can be used in place of two 24LC01's, for example, without any modifications to software. The "chip select" portion of the control byte becomes a don't care.

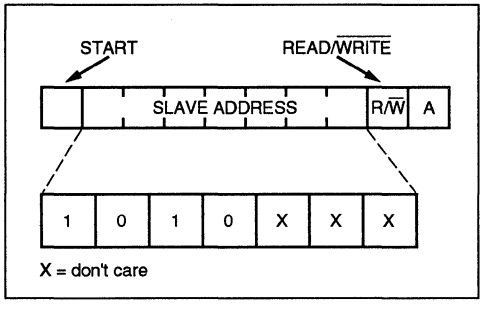
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24AA01/02, followed by three don't care bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24AA01/02 (see Figure 2).

The 24AA01/02 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXX	1
Write	1010	XXX	0

FIGURE 2 - CONTROL BYTE ALLOCATION



WRITE OPERATION

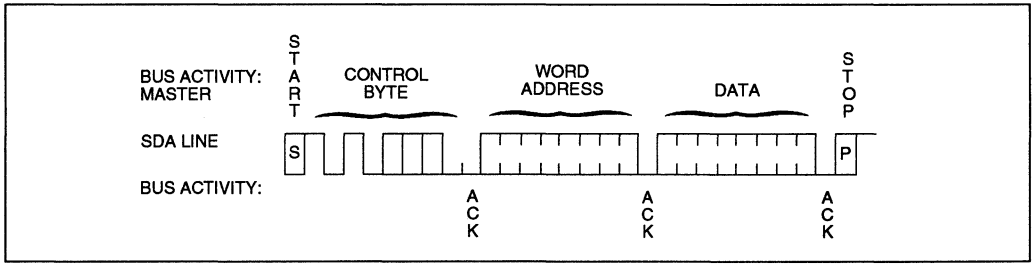
Byte Write

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA01/02. After receiving another acknowledge signal from the 24AA01/02 the master device will transmit the data word to be written into the addressed memory location. The 24AA01/02 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA01/02 will not generate acknowledge signals (see Figure 3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA01/02 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24AA01/02 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 5).

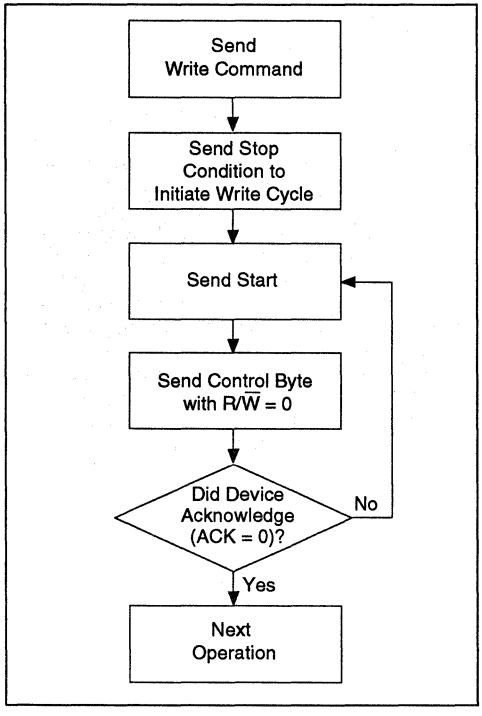
FIGURE 3 - BYTE WRITE



ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 4 for flow diagram.

FIGURE 4 - ACKNOWLEDGE POLLING FLOW



WRITE PROTECTION

The 24AA01/02 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24AA01/02 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA01/02 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA01/02 discontinues transmission (see Figure 6).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA01/02 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA01/02 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA01/02 discontinues transmission (see Figure 7).

FIGURE 5 - PAGE WRITE

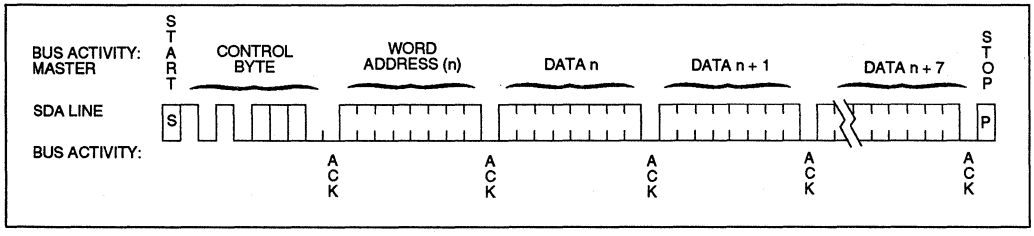


FIGURE 6 - CURRENT ADDRESS READ

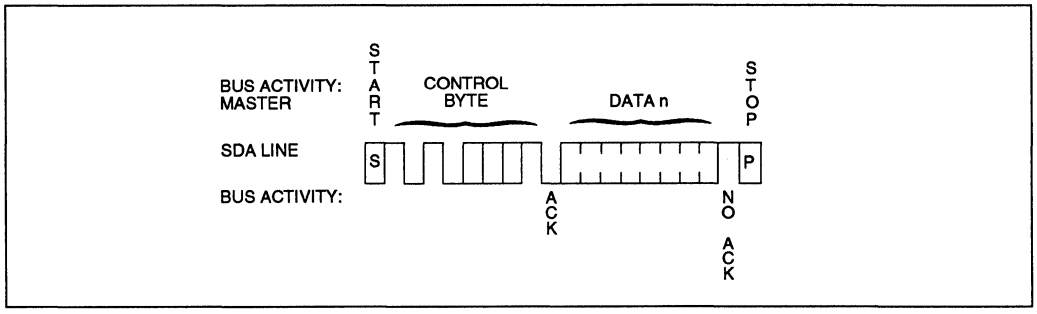
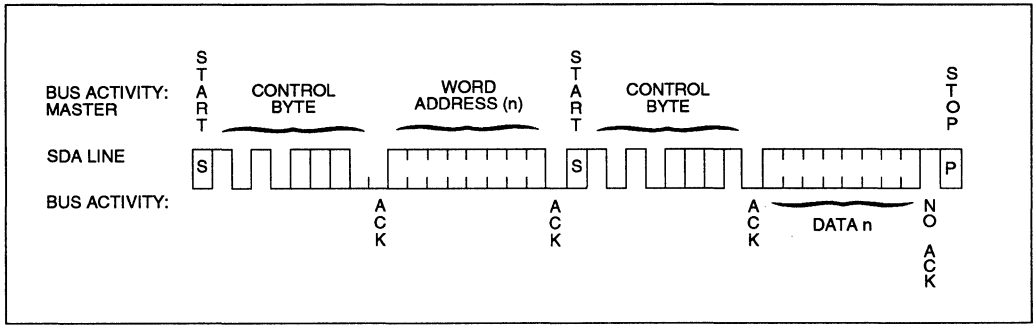


FIGURE 7 - RANDOM READ



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Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA01/02 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA01/02 to transmit the next sequentially addressed 8 bit word (see Figure 8).

To provide sequential reads the 24AA01/02 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The 24AA01/02 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

PIN DESCRIPTIONS

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 KHz, 1K for 400 KHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

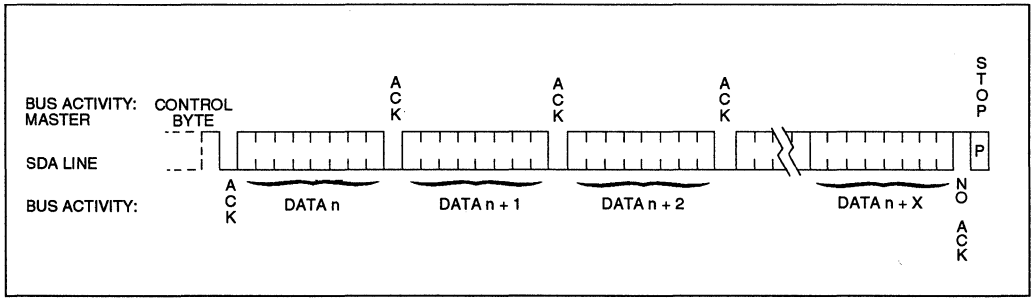
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24AA01/02 as a serial ROM when WP is enabled (tied to Vcc).

A0, A1, A2

These pins are not used by the 24AA01/02. They may be left floating or tied to either Vss or Vcc.

FIGURE 8 - SEQUENTIAL READ

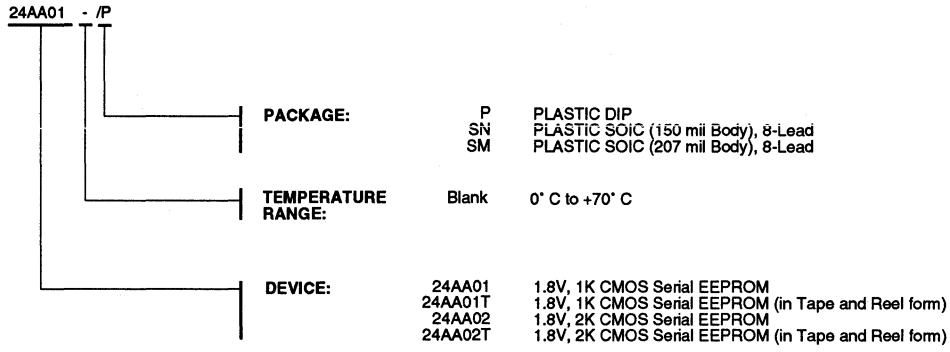


NOTES

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the listed sales offices below or contact corporate headquarters for the representative or distributor in your area.

PART NUMBERS



24LC04B/08B

4K/8K 2.5V CMOS Serial EEPROMs

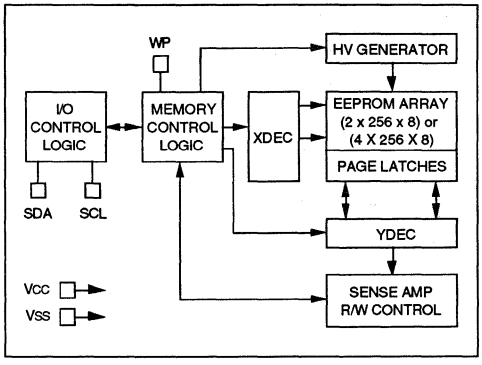
FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as two or four blocks of 256 bytes (2 x 256 x 8) and (4 x 256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 KHz (2.5V) and 400 KHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8-pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

The Microchip Technology Inc. 24LC04B/08B is a 4K- or 8K-bit Electrically Erasable PROM. The device is organized as two or four blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 2.5 volts with standby and active currents of only 5 µA and 1 mA respectively. The 24LC04B/08B also has a page-write capability for up to 16 bytes of data. The 24LC04B/08B is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

BLOCK DIAGRAM



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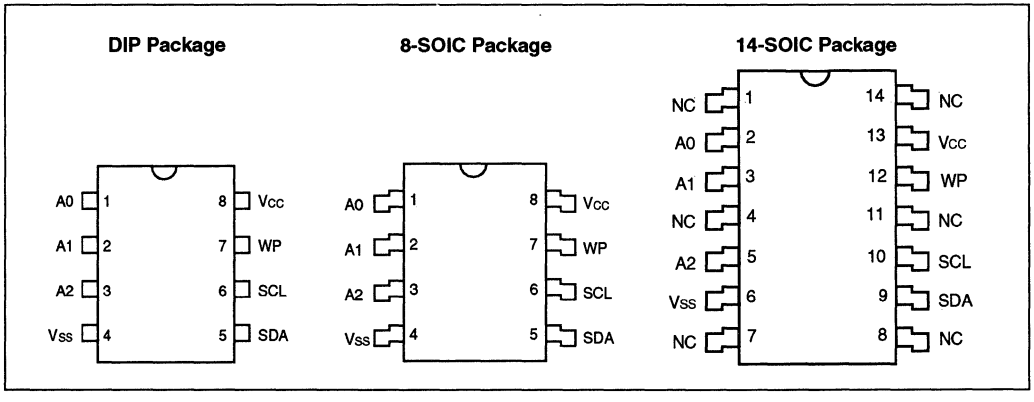
PIN CONFIGURATION



I²C is a trademark of Philips Corporation

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ... -0.3V to VCC + 1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+2.5V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

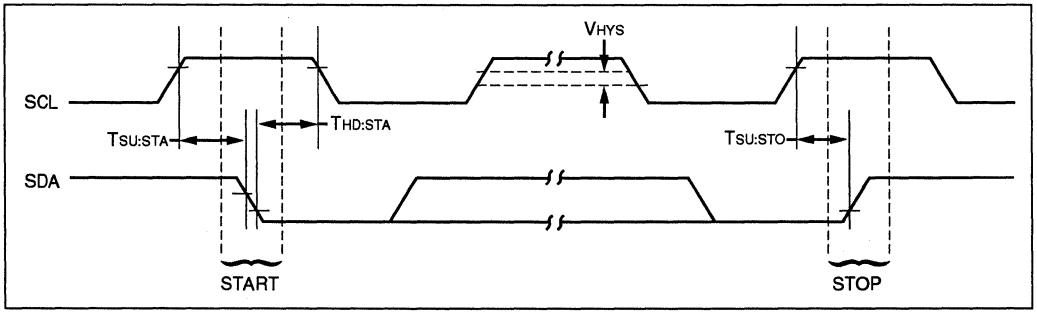
DC CHARACTERISTICS

VCC = +2.5V to +5.5V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min	Max	Units	Conditions
WP, SCL and SDA pins: High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	0.05 VCC	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC WRITE	—	3	mA	VCC = 5.5V SCL = 400 KHz
	ICC READ	—	1	mA	
Standby current	ICCS	—	30	µA	VCC = 3.0V SDA = SCL = VCC
		—	100	µA	VCC = 5.5V SDA = SCL = VCC

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP



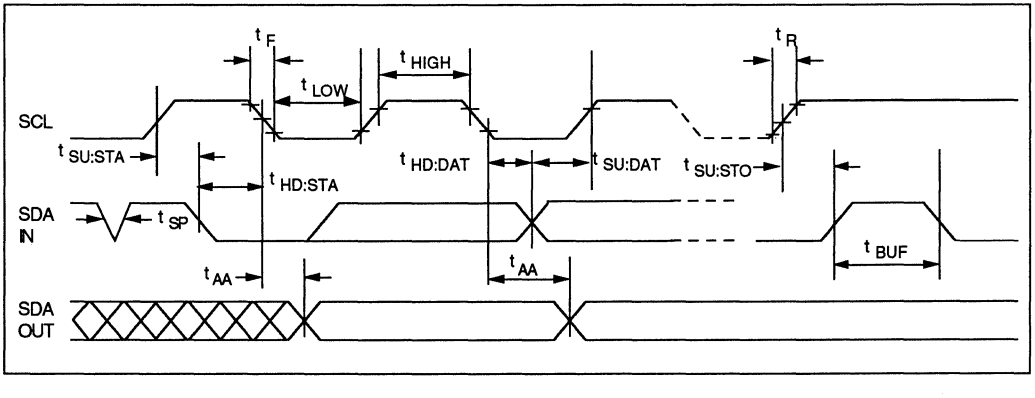
AC CHARACTERISTICS		STANDARD MODE		Vcc = 4.5-5.5V FAST MODE			
Parameter	Symbol	Min	Max	Min	Max	Units	Remarks
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	100,000	—	100,000	—	E/W Cycles	1,000,000 typical

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24LC04B/08B supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC04B/08B works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

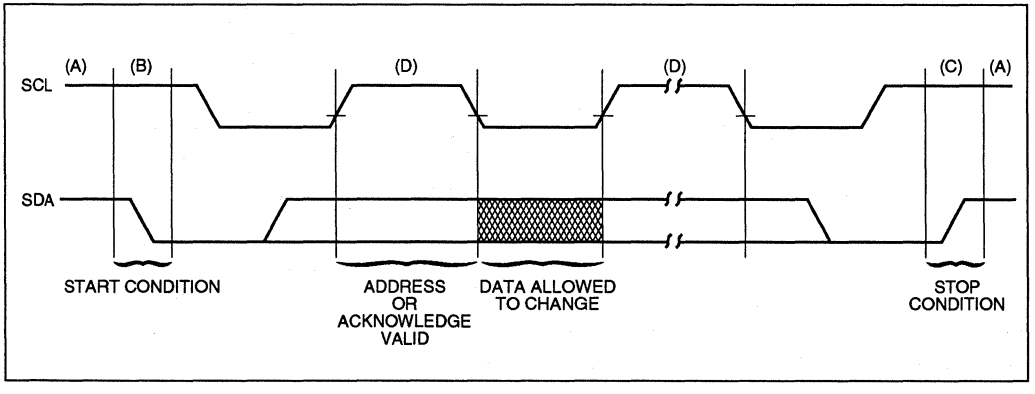
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC04B/08B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

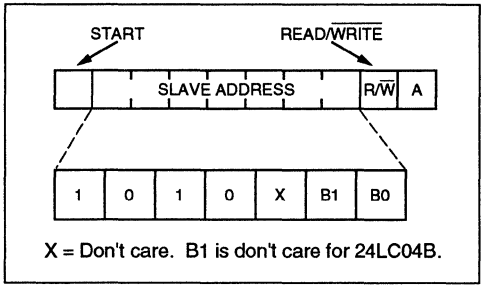
Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24LC04B/08B this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). B2 is a don't care for both the 24LC04B and 24LC08B; B1 is a don't care for the 24LC04B. They are used by the master device to select which of the two or four 256 word blocks of memory are to be accessed. These bits are in effect the most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC04B/08B monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC04B/08B will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 2 - CONTROL BYTE ALLOCATION



X = Don't care. B1 is don't care for 24LC04B.

WRITE OPERATION

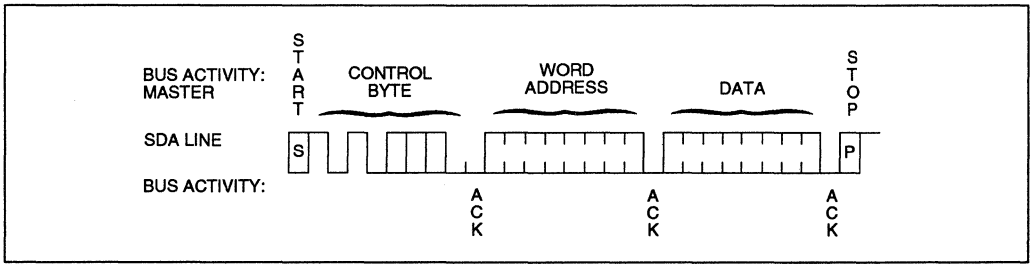
Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC04B/08B. After receiving another acknowledge signal from the 24LC04B/08B the master device will transmit the data word to be written into the addressed memory location. The 24LC04B/08B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC04B/08B will not generate acknowledge signals (see Figure 3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC04B/08B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24LC04B/08B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 5).

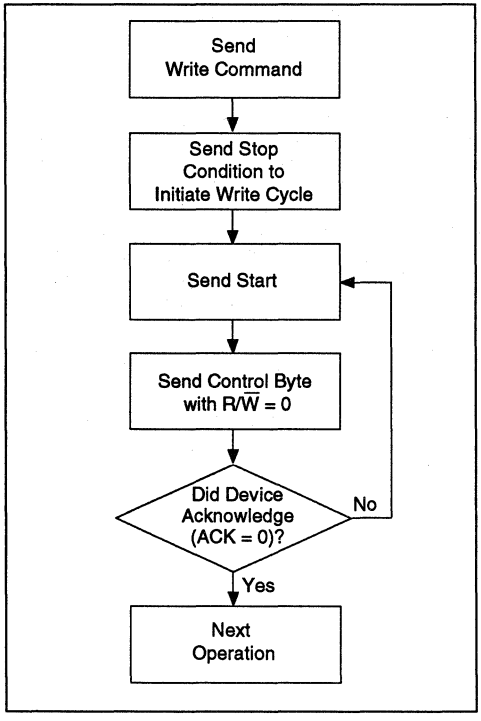
FIGURE 3 - BYTE WRITE



ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 4 for flow diagram.

FIGURE 4 - ACKNOWLEDGE POLLING FLOW



WRITE PROTECTION

The 24LC04B/08B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24LC04B/08B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC04B/08B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC04B/08B discontinues transmission (see Figure 6).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC04B/08B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC04B/08B will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC04B/08B discontinues transmission (see Figure 7).

FIGURE 5 - PAGE WRITE

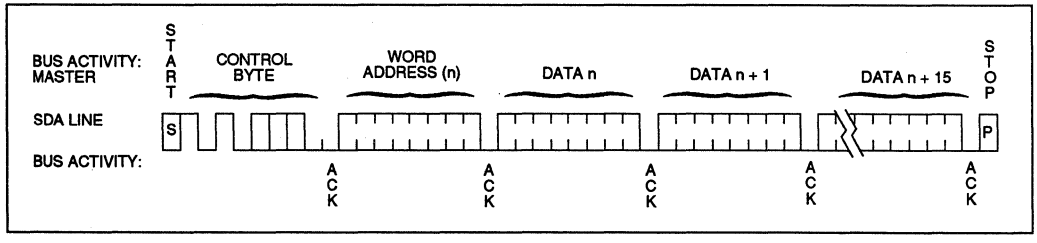


FIGURE 6 - CURRENT ADDRESS READ

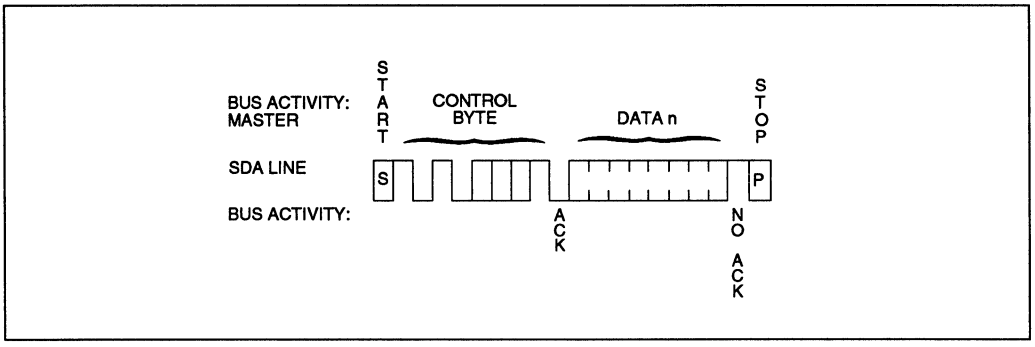
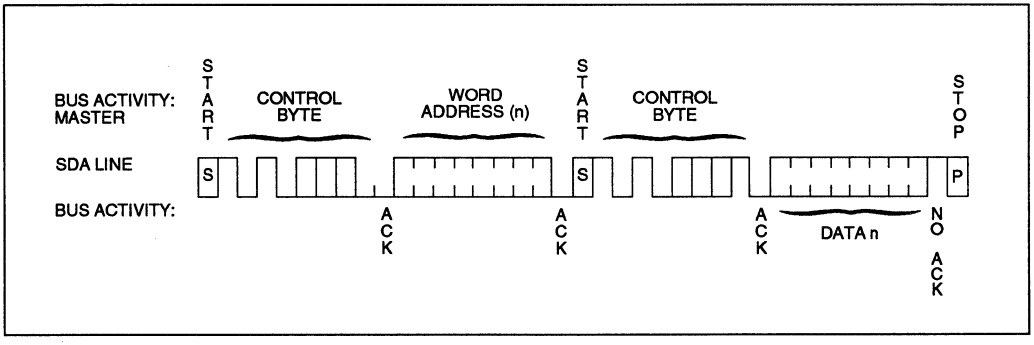


FIGURE 7 - RANDOM READ



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Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC04B/08B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC04B/08B to transmit the next sequentially addressed 8 bit word (see Figure 8).

To provide sequential reads the 24LC04B/08B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The 24LC04B/08B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

PIN DESCRIPTIONS

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 KHz, 1KΩ for 400 KHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

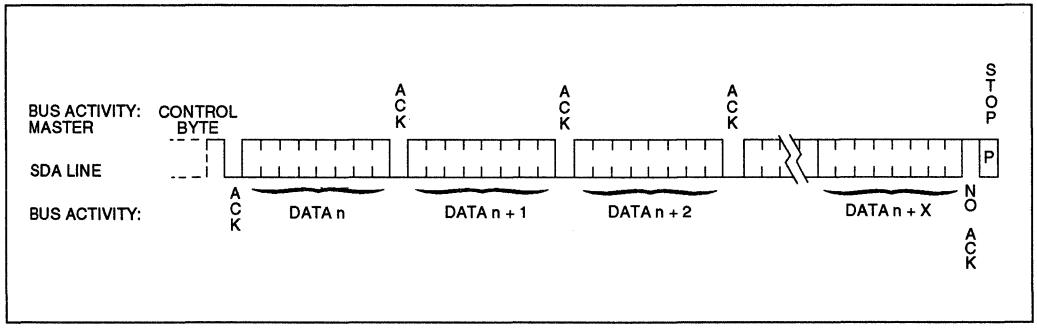
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC04B/08B as a serial ROM when WP is enabled (tied to Vcc).

A0, A1, A2

These pins are not used by the 24LC04B/08B. They may be left floating or tied to either Vss or Vcc.

FIGURE 8 - SEQUENTIAL READ



NOTES

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

24LC04B - / P

PACKAGE:	P	PLASTIC DIP
	SL	PLASTIC SOIC (150 mil Body), 14-Lead
	SN	PLASTIC SOIC (150 mil Body), 8-Lead
	SM	PLASTIC SOIC (207 mil Body), 8-Lead
TEMPERATURE RANGE:	Blank	0°C to +70°C
	I	-40°C to +85°C
DEVICE:	24LC04B	4K CMOS Serial EEPROM
	24LC04BT	4K CMOS Serial EEPROM (in Tape and Reel Form)
	24LC08B	8K CMOS Serial EEPROM
	24LC08BT	8K CMOS Serial EEPROM (in Tape and Reel Form)

24AA04/08

4K/8K 1.8V CMOS Serial EEPROMs

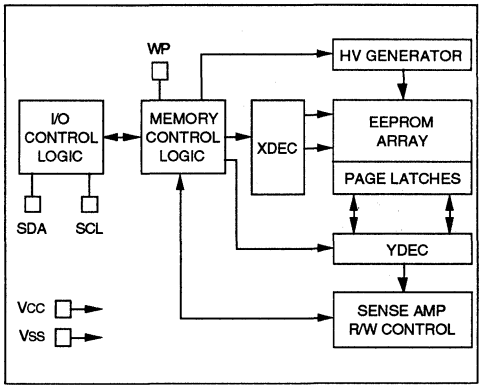
FEATURES

- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 3 µA standby current typical at 1.8V
- Organized as 2 or 4 blocks of 256 bytes (2 x 256 x 8) or (4 x 256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 KHz (1.8V) and 400 KHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8-pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C

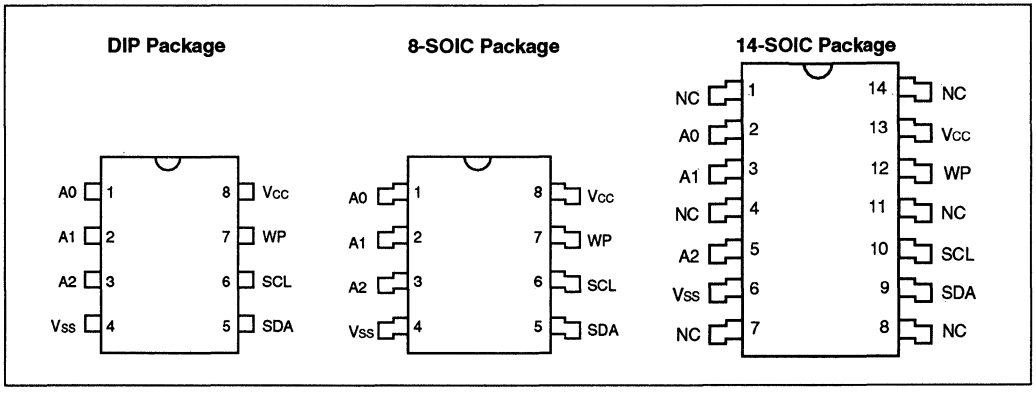
DESCRIPTION

The Microchip Technology Inc. 24AA04/08 is a 4K bit or 8K bit Electrically Erasable PROM. The device is organized as 2 or 4 blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 1.8 volts with standby and active currents of only 3 µA and 1 mA respectively. The 24AA04/08 also has a page-write capability for up to 16 bytes of data. The 24AA04/08 is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

BLOCK DIAGRAM



PIN CONFIGURATION



I²C is a trademark of Philips Corporation

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+1.8V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

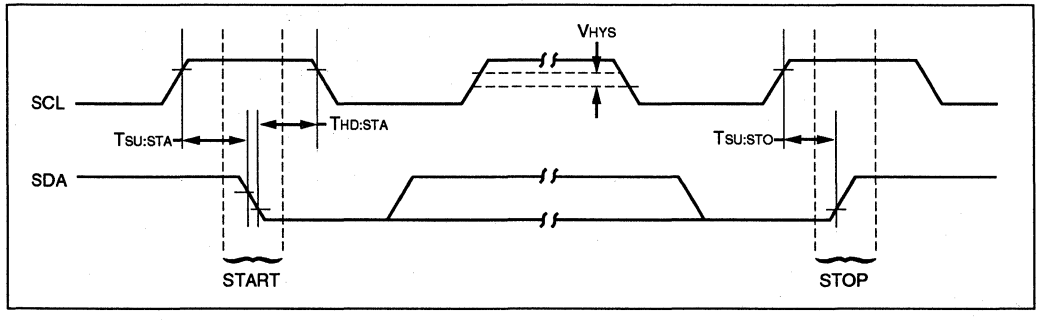
DC CHARACTERISTICS

VCC = +1.8V to +5.5V
Commercial (C): Tamb = 0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
WP, SCL and SDA pins: High level input voltage	VIH	.7 VCC	—	—	V	
Low level input voltage	VIL	—	—	.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	0.05 VCC	—	—	V	Note 1
Low level output voltage	VOL	—	—	.40	V	IOL = 3.0 mA, VCC = 1.8V
Input leakage current	ILI	-10	—	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	—	10	µA	VOUT = .1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC WRITE	—	—	3	mA	VCC = 5.5V, SCL = 400 KHz
		—	.05	—	mA	VCC = 1.8V, SCL = 100 KHz
	ICC READ	—	—	1	mA	VCC = 5.5V, SCL = 400 KHz
		—	0.05	—	mA	VCC = 1.8V, SCL = 100 KHz
Standby current	ICCS	—	—	100	µA	VCC = 5.5V, SDA=SCL=VCC
		—	—	30	µA	VCC = 3.0V, SDA=SCL=VCC
		—	3	—	µA	VCC = 1.8V, SDA=SCL=VCC

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP



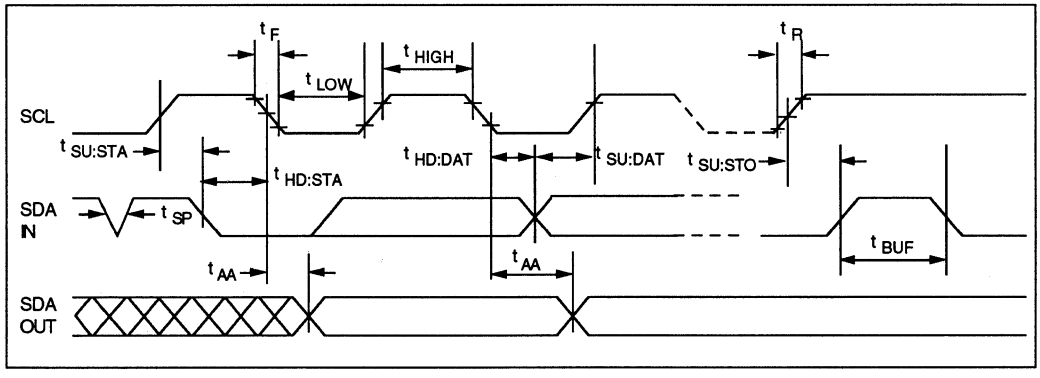
AC CHARACTERISTICS		STANDARD MODE		Vcc = 4.5-5.5V FAST MODE			
Parameter	Symbol	Min	Max	Min	Max	Units	Remarks
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	100,000	—	100,000	—	E/W Cycles	1,000,000 typical

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24AA04/08 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA04/08 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

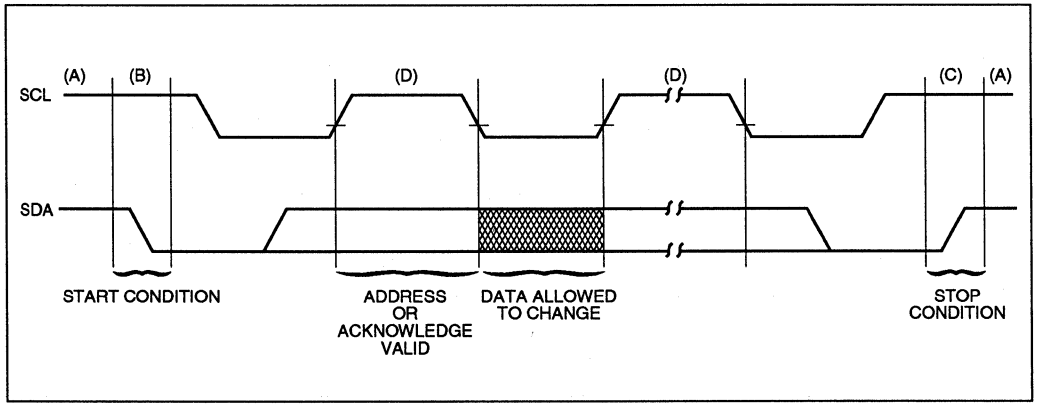
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA04/08 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

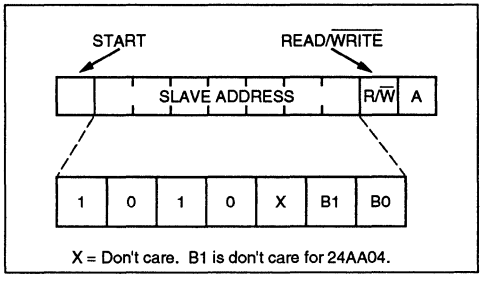
Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24AA04/08 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). B2 is a don't care for both the 24AA04 and 24AA08; B1 is a don't care for the 24AA04. They are used by the master device to select which of the two or four 256 word blocks of memory are to be accessed. These bits are in effect the most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24AA04/08 monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA04/08 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 2 - CONTROL BYTE ALLOCATION



WRITE OPERATION

Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA04/08. After receiving another acknowledge signal from the 24AA04/08 the master device will transmit the data word to be written into the addressed memory location. The 24AA04/08 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA04/08 will not generate acknowledge signals (see Figure 3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA04/08 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24AA04/08 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 5).

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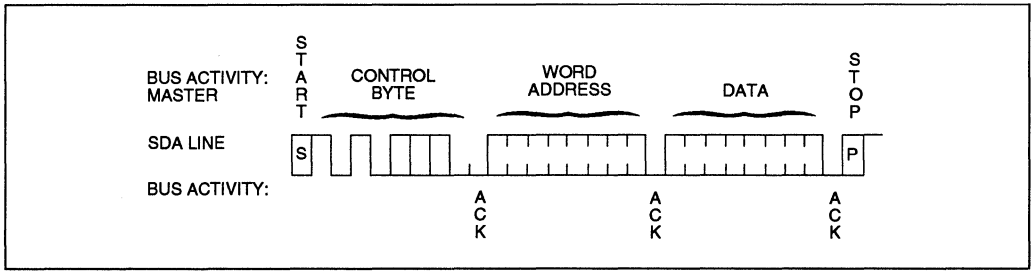
FIGURE 3 - BYTE WRITE



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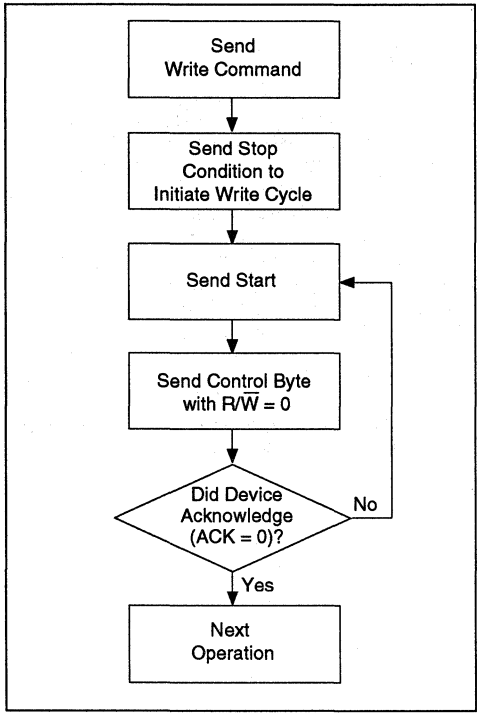

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Read operations are initiated in the same way as write operations with the exception that the $R/\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24AA04/08 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with $R/\overline{W}$ bit set to one, the 24AA04/08 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA04/08 discontinues transmission (see Figure 6).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA04/08 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the $R/\overline{W}$ bit set to a one. The 24AA04/08 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA04/08 discontinues transmission (see Figure 7).

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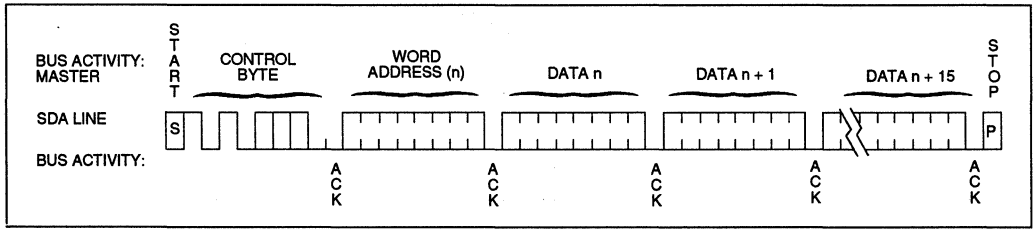


FIGURE 6 - CURRENT ADDRESS READ

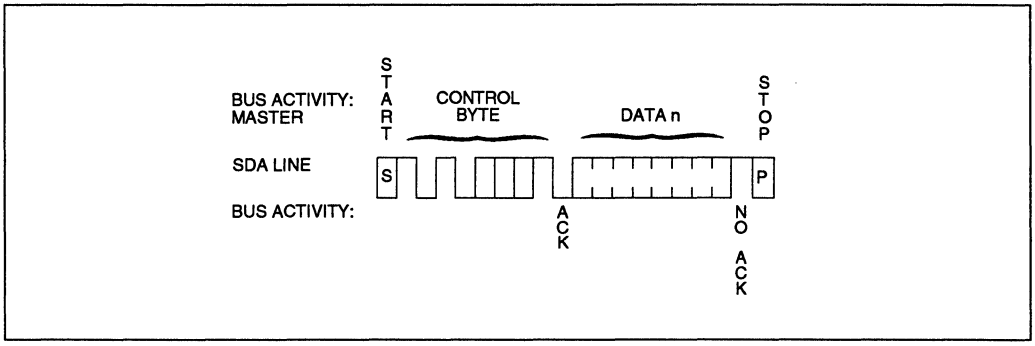
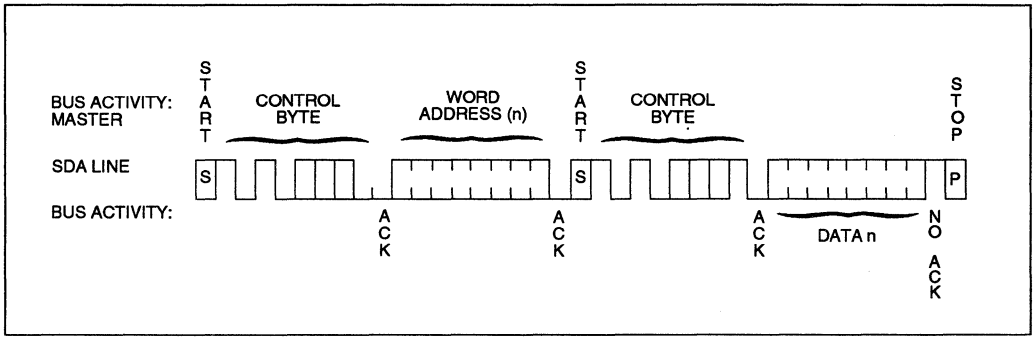


FIGURE 7 - RANDOM READ



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The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

PIN DESCRIPTIONS

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 KHz, 1KΩ for 400 KHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

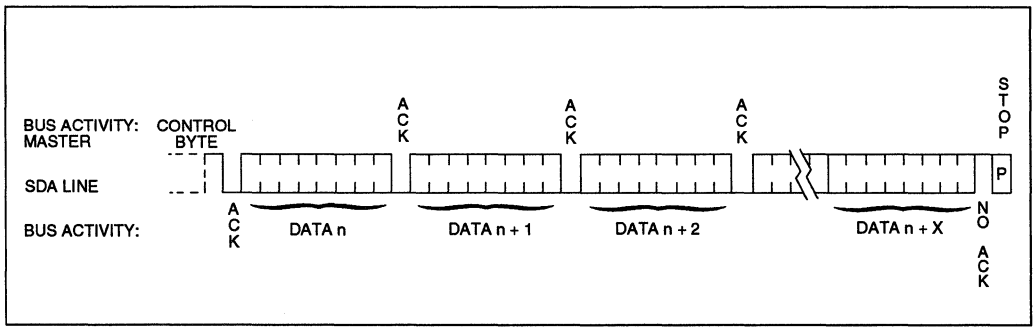
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24AA04/08 as a serial ROM when WP is enabled (tied to Vcc).

A0, A1, A2

These pins are not used by the 24AA04/08. They may be left floating or tied to either Vss or Vcc.

FIGURE 8 - SEQUENTIAL READ



NOTES

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

24AA04 - / P

PACKAGE:	P	PLASTIC DIP
	SL	PLASTIC SOIC (150 mil Body), 14-Lead
	SN	PLASTIC SOIC (150 mil Body), 8-Lead
	SM	PLASTIC SOIC (207 mil Body), 8-Lead
TEMPERATURE RANGE:	Blank	0°C to +70°C
DEVICE:	24AA04	1.8V, 4K CMOS Serial EEPROM
	24AA04T	1.8V, 4K CMOS Serial EEPROM (in Tape and Reel Form)
	24AA08	1.8V, 8K CMOS Serial EEPROM
	24AA08T	1.8V, 8K CMOS Serial EEPROM (in Tape and Reel Form)

24LC16B

16K 2.5V CMOS Serial EEPROM

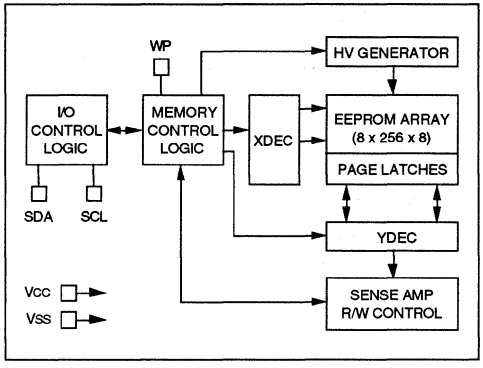
FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 KHz (2.5V) and 400 KHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

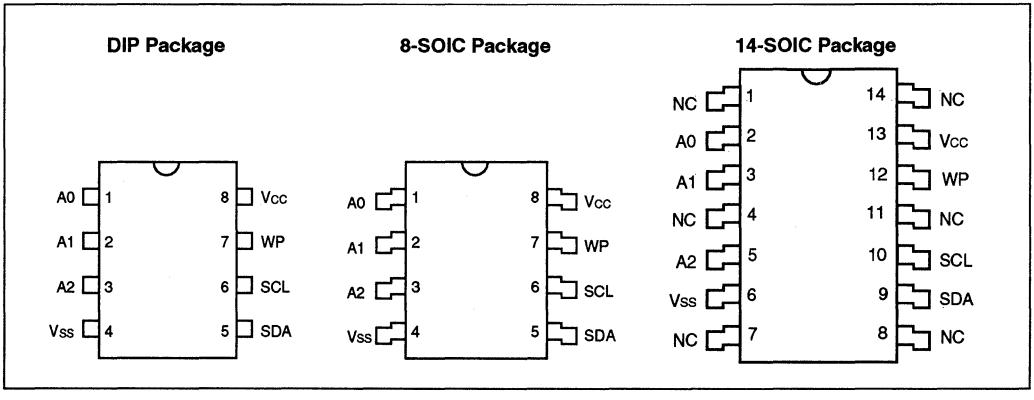
DESCRIPTION

The Microchip Technology Inc. 24LC16B is a 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 2.5 volts with standby and active currents of only 5 µA and 1 mA respectively. The 24LC16B also has a page-write capability for up to 16 bytes of data. The 24LC16B is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

BLOCK DIAGRAM



PIN CONFIGURATION



I²C is a trademark of Philips Corporation

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.3V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+2.5V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

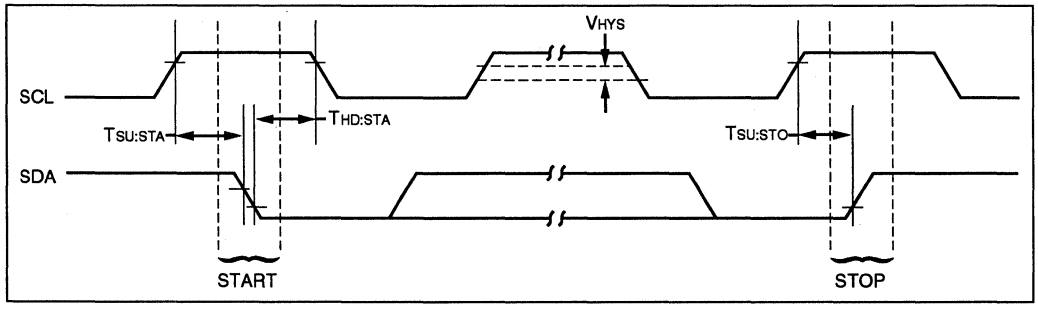
DC CHARACTERISTICS

VCC = +2.5V to +5.5V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I) : Tamb = -40°C to +85°C

Parameter	Symbol	Min	Max	Units	Conditions
WP, SCL and SDA pins: High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	0.05 VCC	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC write	—	3	mA	VCC = 5.5V SCL = 400 KHz
	ICC read	—	1	mA	
Standby current	ICCS	—	30	µA	VCC = 3.0V SDA = SCL = VCC
		—	100	µA	VCC = 5.5V SDA = SCL = VCC

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP



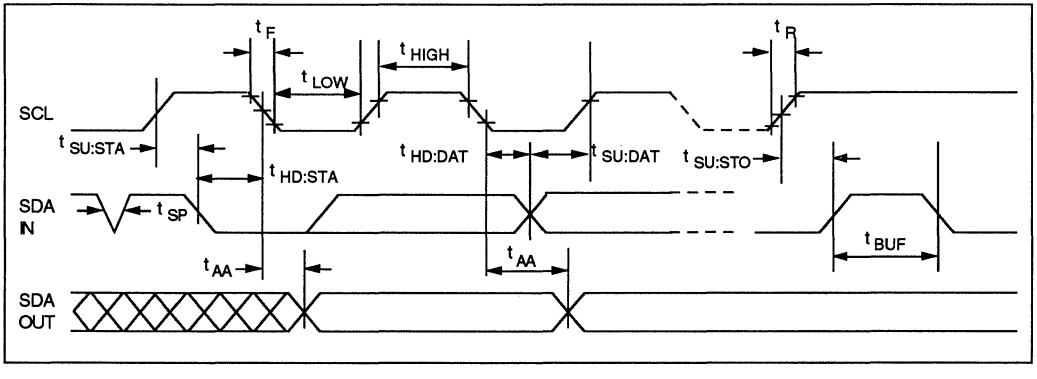
AC CHARACTERISTICS		STANDARD MODE		Vcc = 4.5-5.5V FAST MODE			
Parameter	Symbol	Min	Max	Min	Max	Units	Remarks
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	100,000	—	100,000	—	E/W Cycles	

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24LC16B supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC16B works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

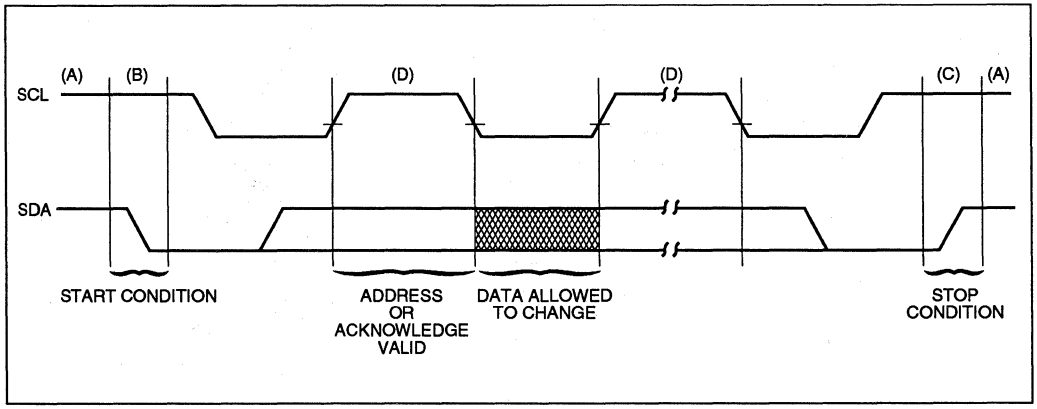
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC16B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC16B) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

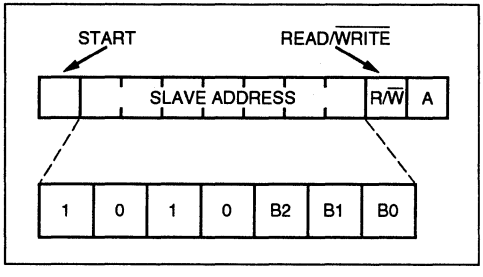
Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24LC16B this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore the protocol can support only one 24LC16B per system.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC16B monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC16B will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 2 - CONTROL BYTE ALLOCATION



WRITE OPERATION

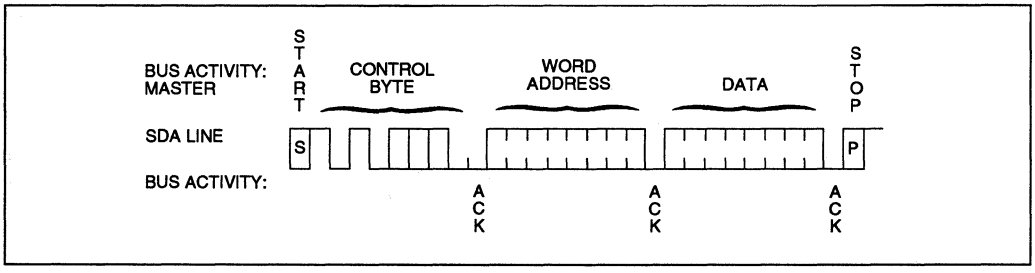
Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC16B. After receiving another acknowledge signal from the 24LC16B the master device will transmit the data word to be written into the addressed memory location. The 24LC16B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC16B will not generate acknowledge signals (see Figure 3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC16B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24LC16B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 5).

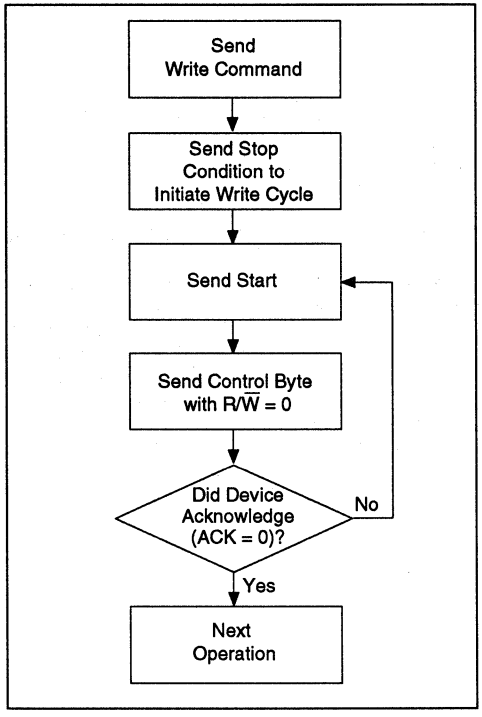
FIGURE 3 - BYTE WRITE



ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 4 for flow diagram.

FIGURE 4 - ACKNOWLEDGE POLLING FLOW



WRITE PROTECTION

The 24LC16B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24LC16B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC16B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC16B discontinues transmission (see Figure 6).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC16B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC16B will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC16B discontinues transmission (see Figure 7).

FIGURE 5 - PAGE WRITE

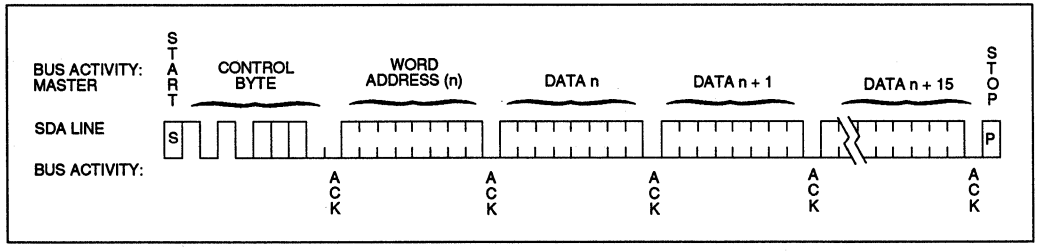


FIGURE 6 - CURRENT ADDRESS READ

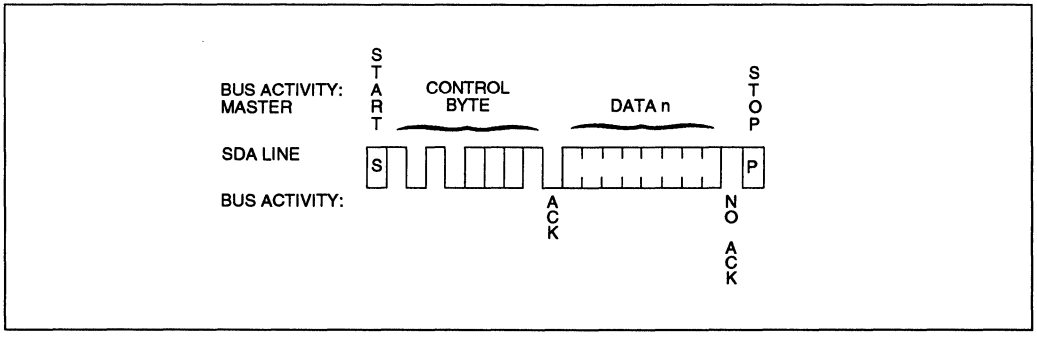
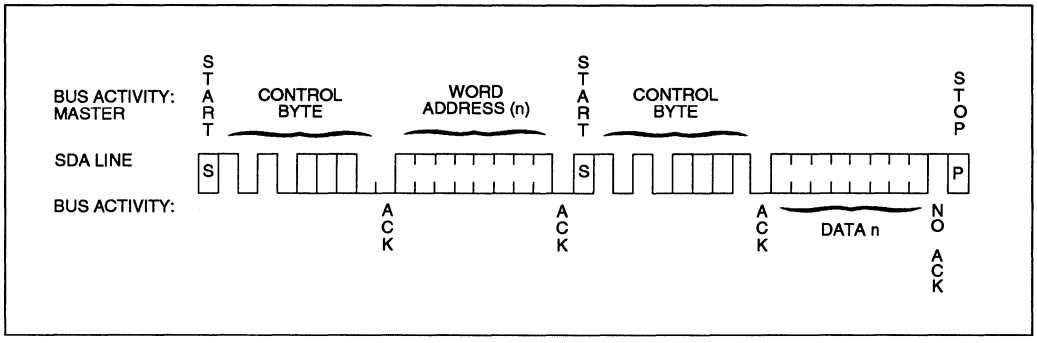


FIGURE 7 - RANDOM READ



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Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC16B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC16B to transmit the next sequentially addressed 8 bit word (see Figure 8).

To provide sequential reads the 24LC16B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The 24LC16B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

PIN DESCRIPTIONS

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 KHz, 1KΩ for 400 KHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

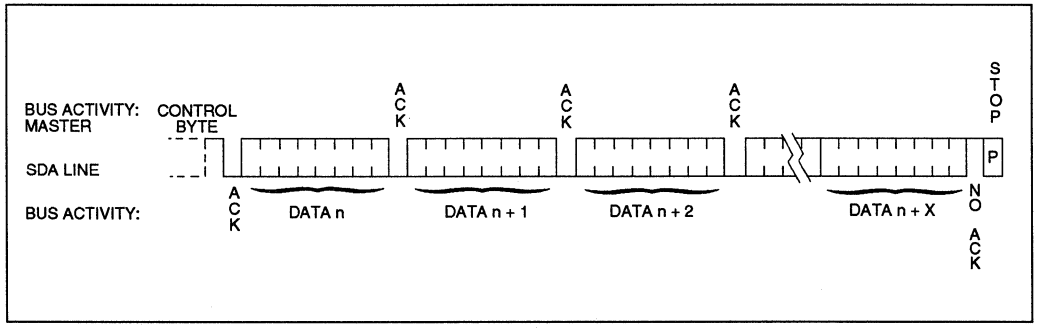
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC16B as a serial ROM when WP is enabled (tied to Vcc).

A0, A1, A2

These pins are not used by the 24LC16B. They may be left floating or tied to either Vss or Vcc.

FIGURE 8 - SEQUENTIAL READ



NOTES

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

24LC16B - / P

PACKAGE:	P	PLASTIC DIP
	SL	PLASTIC SOIC (150 mil Body), 14-Lead
	SN	PLASTIC SOIC (150 mil Body), 8-Lead
	SM	PLASTIC SOIC (207 mil Body), 8-Lead
TEMPERATURE RANGE:	Blank	0°C to +70°C
	I	-40°C to +85°C
DEVICE:	24LC16B	16K CMOS Serial EEPROM
	24LC16BT	16K CMOS Serial EEPROM (in Tape and Reel Form)

MICROCHIP

24C08B/16B

8K/16K 5V E-Temperature Serial EEPROMs

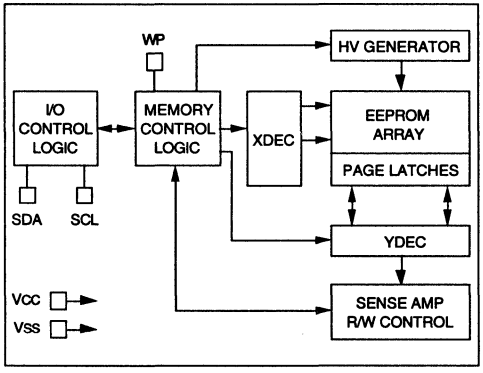
FEATURES

- Single supply with operation from 4.5-5.5V
- Low power CMOS technology
  - — 1 mA active current typical
  - — 10 μA standby current typical at 5.5V
- Organized as 4 or 8 blocks of 256 bytes (4 x 256 x 8) or (8 x 256 x 8)
- Two wire serial interface bus, I²C compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 KHz compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 100K ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature range
  - — Automotive: -40°C to +125°C

DESCRIPTION

The Microchip Technology Inc. 24C08B/16B is an 8K/16K bit Electrically Erasable PROM intended for use in extended/automotive temperature ranges. The device is organized as 4 or 8 blocks of 256 x 8 bit memory with a two wire serial interface. The 24C08B/16B also has a page-write capability for up to 16 bytes of data. The 24C08B/16B is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

BLOCK DIAGRAM



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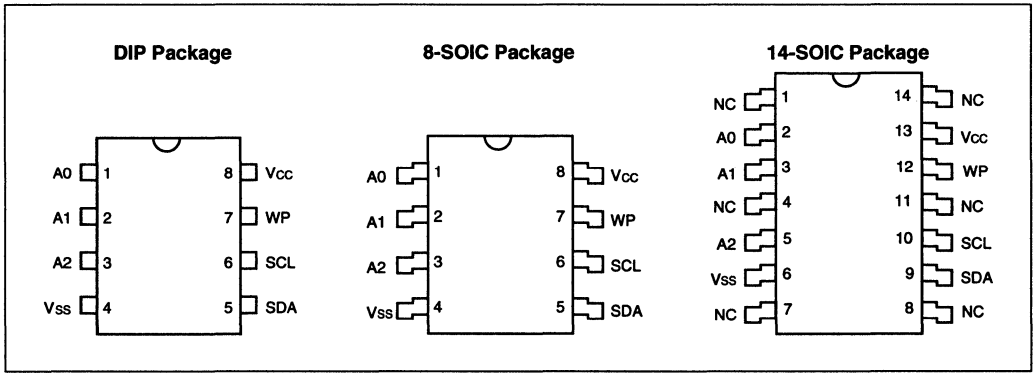
PIN CONFIGURATION



I²C is a trademark of Philips Corporation

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+4.5V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

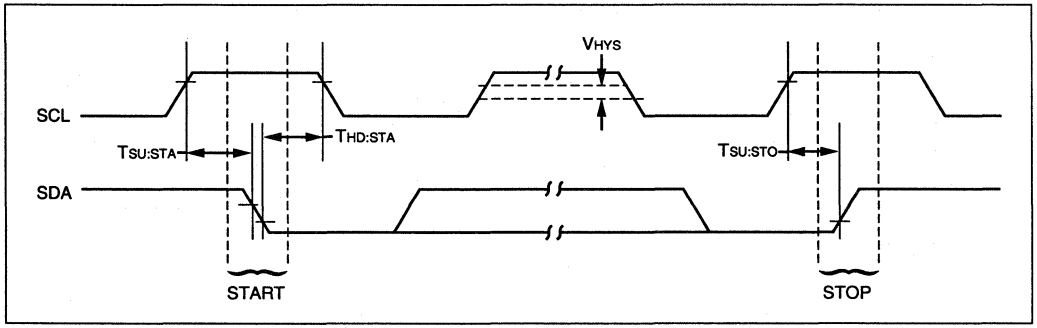
DC CHARACTERISTICS

Vcc = +4.5V to +5.5V
Automotive (I): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
WP, SCL and SDA pins: High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt trigger inputs	VHYS	0.05 Vcc	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, Vcc = 4.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	Vcc = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	Icc write	—	3	mA	Vcc = 5.5V SCL = 400 KHz
	Icc read	—	1	mA	
Standby current	Iccs	—	100	µA	Vcc = 5.5V SDA = SCL = Vcc

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP



AC CHARACTERISTICS

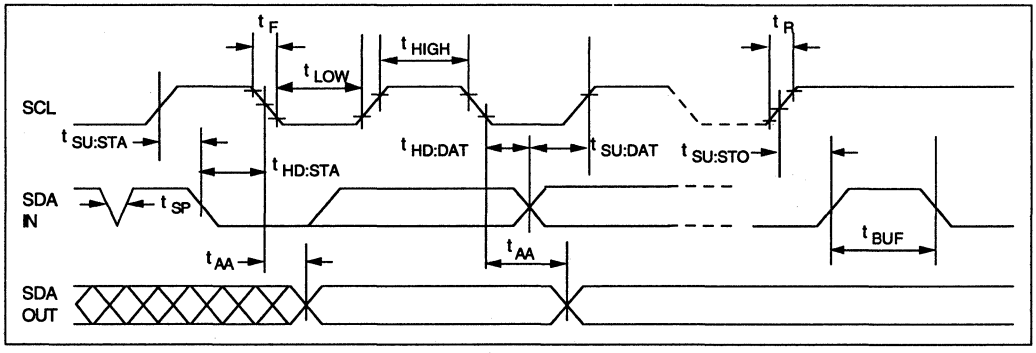
Parameter	Symbol	Min	Max	Units	Remarks
Clock frequency	FCLK	0	100	kHz	
Clock high time	THIGH	4000	—	ns	
Clock low time	TLOW	4700	—	ns	
SDA and SCL rise time	TR	—	1000	ns	Note 2
SDA and SCL fall time	TF	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	ns	
Data input setup time	TSU:DAT	250	—	ns	
STOP condition setup time	TSU:STO	4000	—	ns	
Output valid from clock	TAA	—	3500	ns	Note 1
Bus free time	TBUF	4700	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	ns	Note 3
Write cycle time	TWR	—	10	ms	Byte or Page mode
Endurance	—	10,000	—	E/W Cycles	

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C08B/16B supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C08B/16B works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

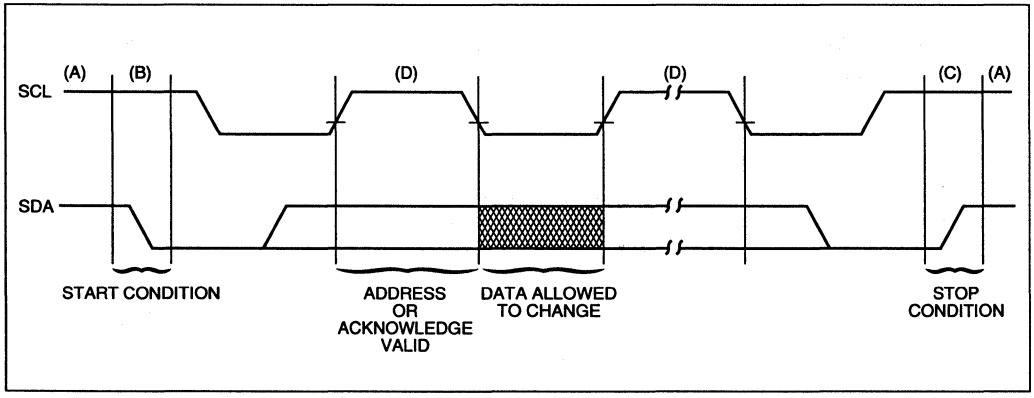
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C08B/16B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24C08B/16B) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

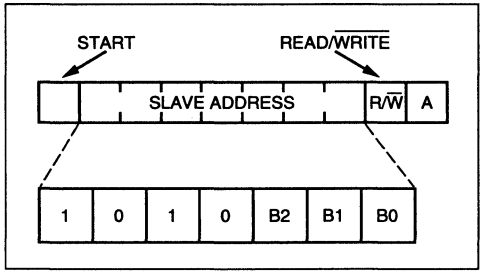
Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24C08B/16B this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24C08B/16B monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24C08B/16B will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 2 - CONTROL BYTE ALLOCATION



WRITE OPERATION

Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C08B/16B. After receiving another acknowledge signal from the 24C08B/16B the master device will transmit the data word to be written into the addressed memory location. The 24C08B/16B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C08B/16B will not generate acknowledge signals (see Figure 3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24C08B/16B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24C08B/16B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 5).

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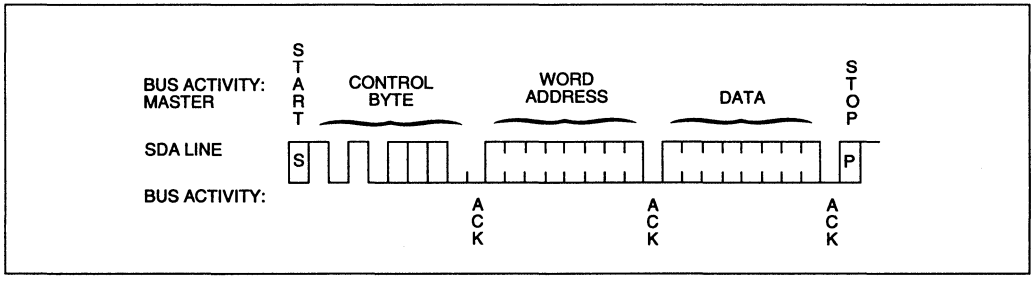
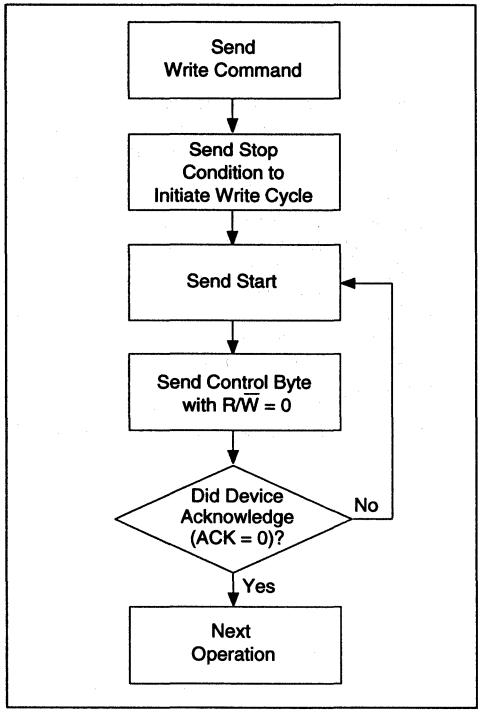
FIGURE 3 - BYTE WRITE



ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 4 for flow diagram.

FIGURE 4 - ACKNOWLEDGE POLLING FLOW



WRITE PROTECTION

The 24C08B/16B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24C08B/16B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24C08B/16B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C08B/16B discontinues transmission (see Figure 6).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C08B/16B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C08B/16B will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C08B/16B discontinues transmission (see Figure 7).

FIGURE 5 - PAGE WRITE

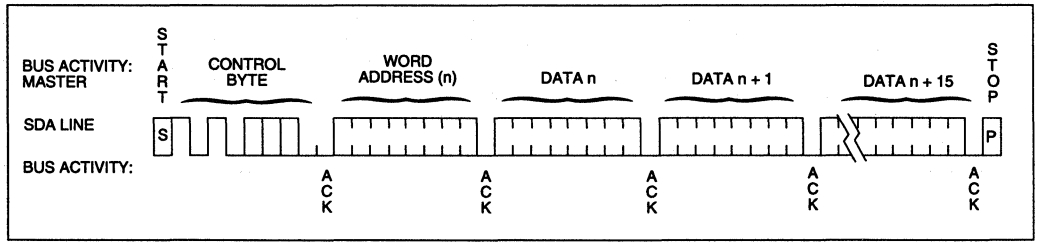


FIGURE 6 - CURRENT ADDRESS READ

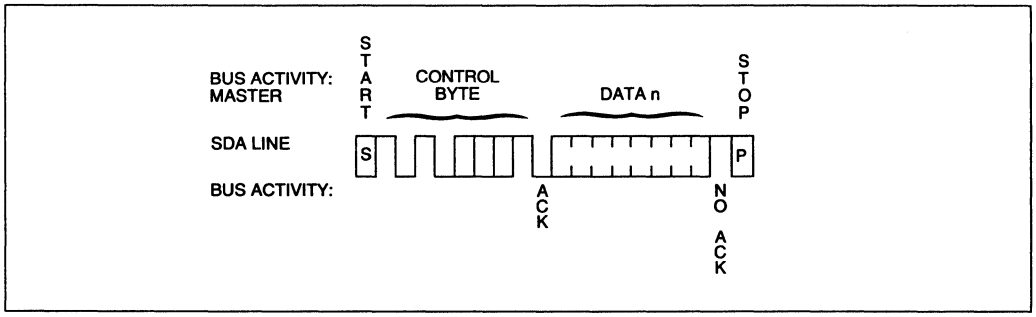
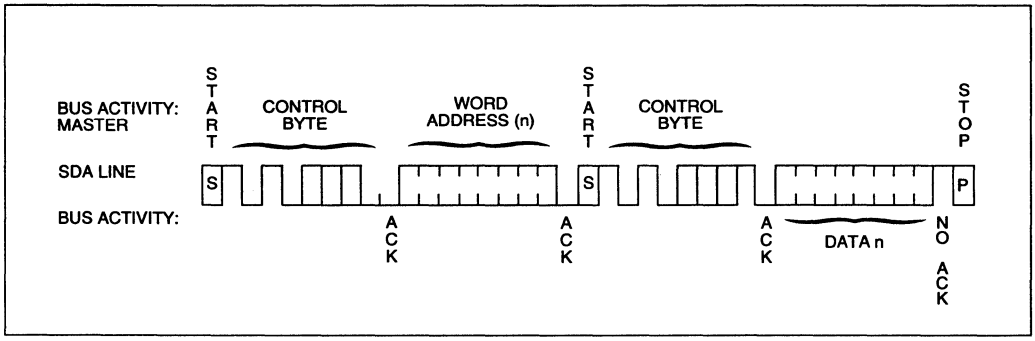


FIGURE 7 - RANDOM READ



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Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C08B/16B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24C08B/16B to transmit the next sequentially addressed 8 bit word (see Figure 8).

To provide sequential reads the 24C08B/16B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The 24C08B/16B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

PIN DESCRIPTIONS

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

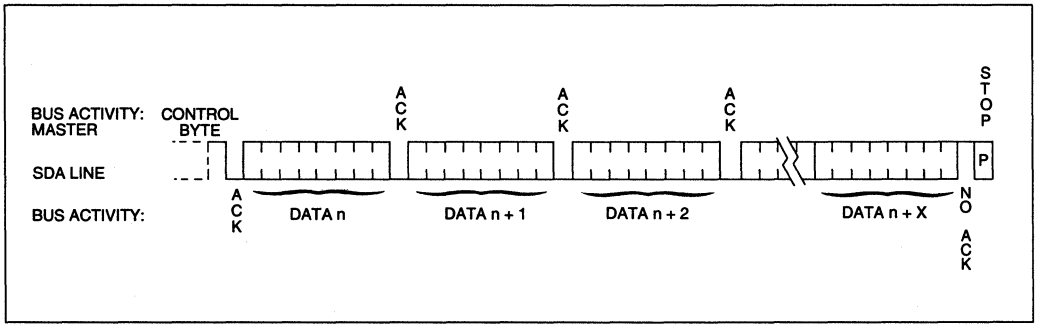
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24C08B/16B as a serial ROM when WP is enabled (tied to Vcc).

A0, A1, A2

These pins are not used by the 24C08B/16B. They may be left floating or tied to either Vss or Vcc.

FIGURE 8 - SEQUENTIAL READ

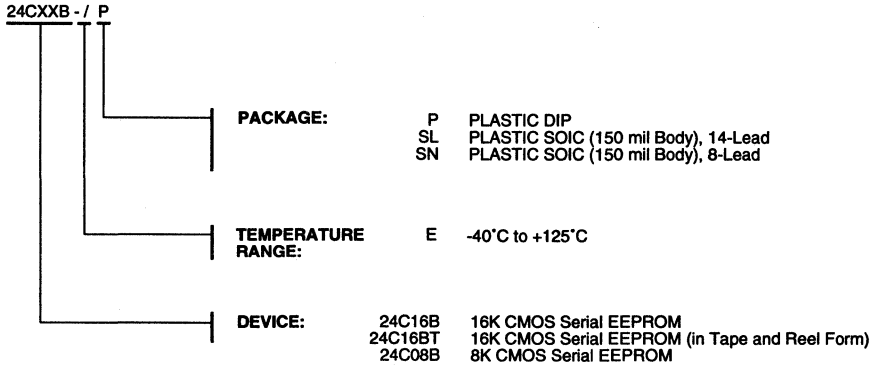


NOTES

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



MICROCHIP

24AA16

16K 1.8V CMOS Serial EEPROM

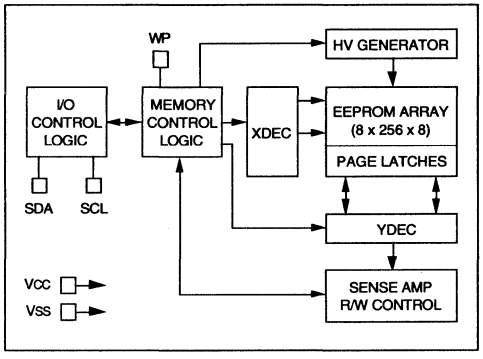
FEATURES

- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 3 µA standby current typical at 1.8V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 KHz (1.8V) and 400 KHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C

DESCRIPTION

The Microchip Technology Inc. 24AA16 is a 1.8 volt 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 1.8 volts with standby and active currents of only 3 µA and 1 mA, respectively. The 24AA16 also has a page-write capability for up to 16 bytes of data. The 24AA16 is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

BLOCK DIAGRAM



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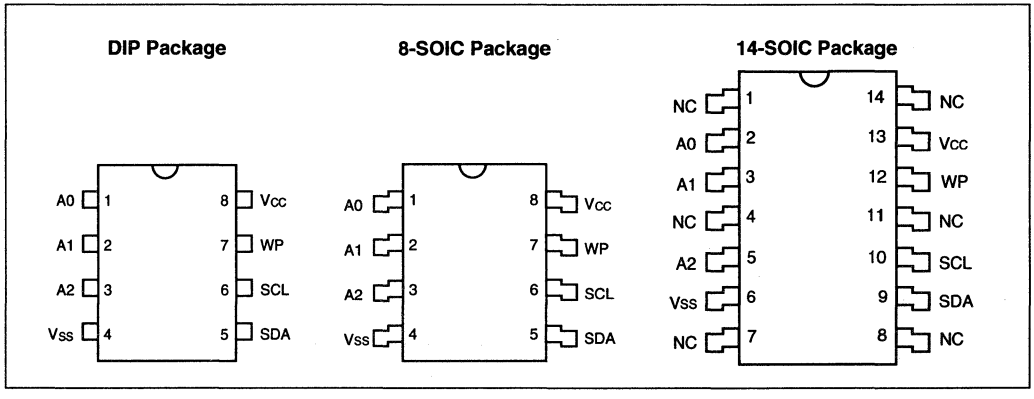
PIN CONFIGURATION



I²C is a trademark of Philips Corporation

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+1.8V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

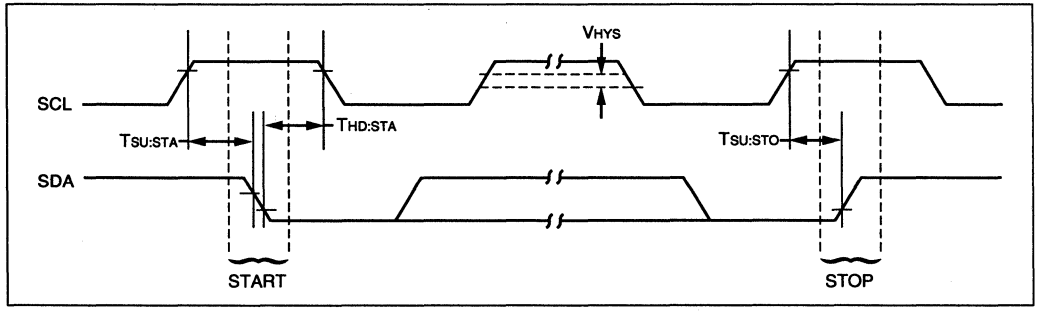
DC CHARACTERISTICS

VCC = +1.8V to +5.5V
Commercial (C): Tamb = 0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
WP, SCL and SDA pins: High level input voltage	VIH	.7 VCC		—	V	
Low level input voltage	VIL	—		.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	0.05 VCC		—	V	Note 1
Low level output voltage	VOL	—		.40	V	IOL = 3.0 mA, VCC = 1.8V
Input leakage current	ILI	-10		10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10		10	µA	VOUT = .1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—		10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC WRITE	—	—	3	mA	VCC = 5.5V, SCL = 400 KHz
		—	.05	—	mA	VCC = 1.8V, SCL = 100 KHz
	ICC READ	—	—	1	mA	VCC = 5.5V, SCL = 400 KHz
		—	0.05	—	mA	VCC = 1.8V, SCL = 100 KHz
Standby current	ICCS	—	—	100	µA	VCC = 5.5V, SDA=SCL=VCC
		—	—	30	µA	VCC = 3.0V, SDA=SCL=VCC
		—	3	—	µA	VCC = 1.8V, SDA=SCL=VCC

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP



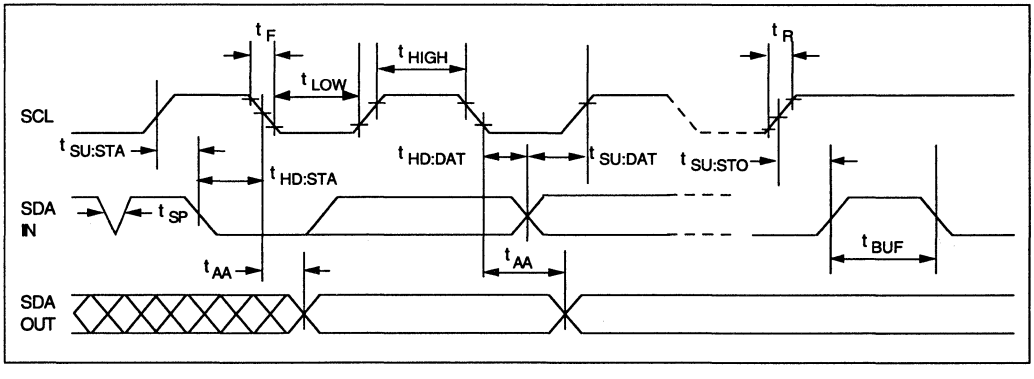
AC CHARACTERISTICS		STANDARD MODE		Vcc = 4.5-5.5V FAST MODE			
Parameter	Symbol	Min	Max	Min	Max	Units	Remarks
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	100,000	—	100,000	—	E/W Cycles	1,000,000 typical

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24AA16 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA16 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

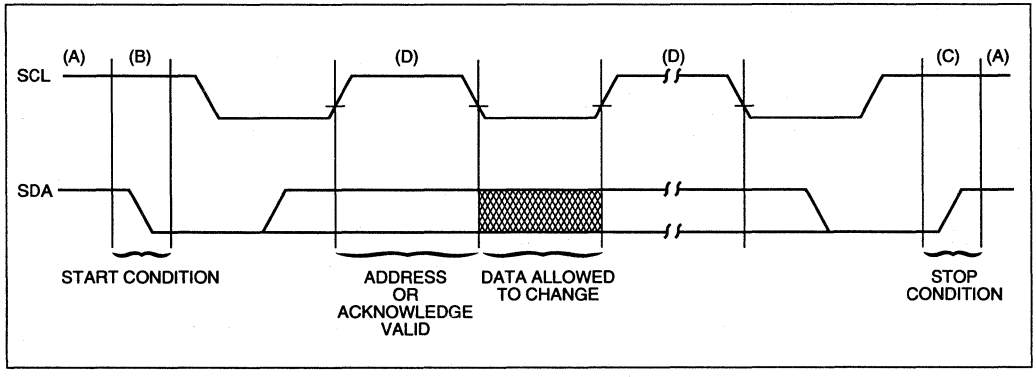
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA16 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

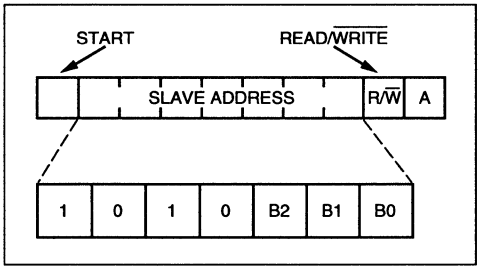
Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24AA16 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore the protocol can support only one 24AA16 per system.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24AA16 monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA16 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 2 - CONTROL BYTE ALLOCATION



WRITE OPERATION

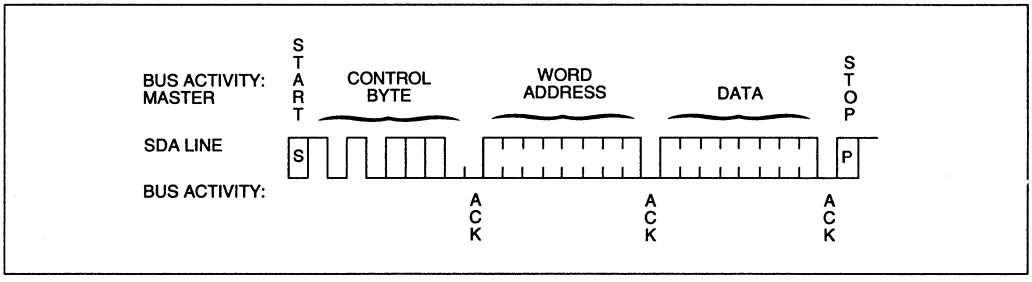
Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA16. After receiving another acknowledge signal from the 24AA16 the master device will transmit the data word to be written into the addressed memory location. The 24AA16 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA16 will not generate acknowledge signals (see Figure 3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA16 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24AA16 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 5).

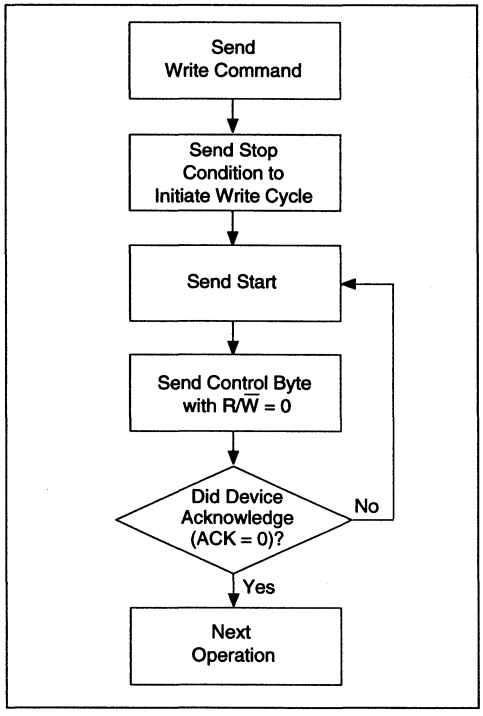
FIGURE 3 - BYTE WRITE



ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 4 for flow diagram.

FIGURE 4 - ACKNOWLEDGE POLLING FLOW



WRITE PROTECTION

The 24AA16 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the $R/\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24AA16 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with $R/\overline{W}$ bit set to one, the 24AA16 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA16 discontinues transmission (see Figure 6).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA16 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the $R/\overline{W}$ bit set to a one. The 24AA16 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA16 discontinues transmission (see Figure 7).

FIGURE 5 - PAGE WRITE

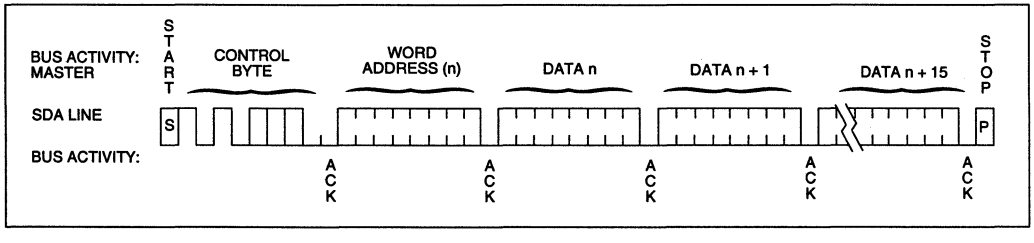


FIGURE 6 - CURRENT ADDRESS READ

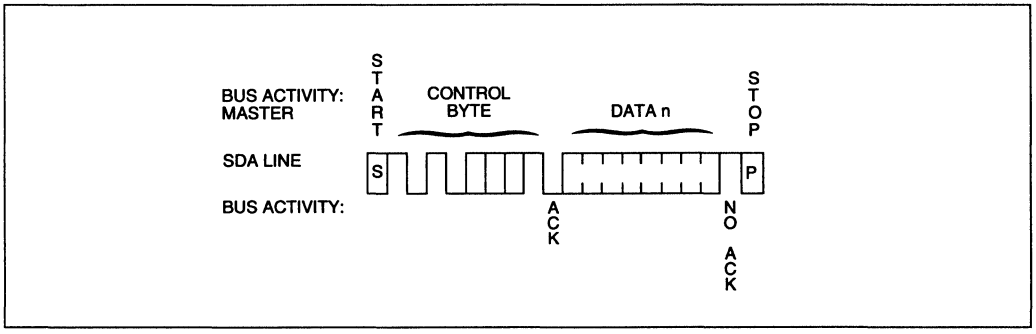
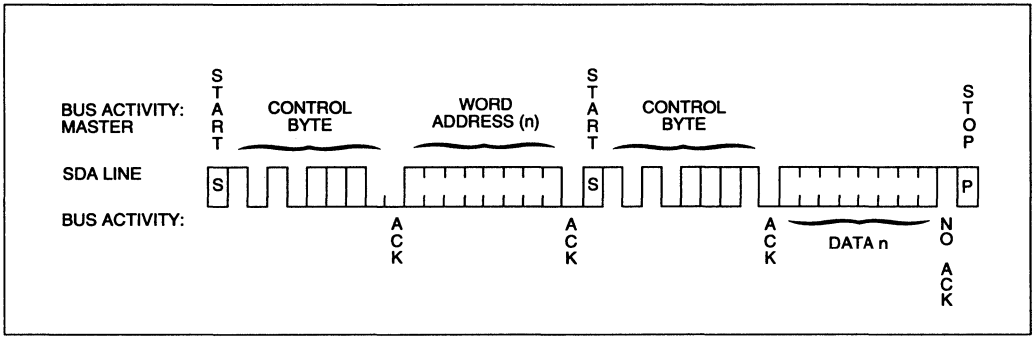


FIGURE 7 - RANDOM READ



5

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA16 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA16 to transmit the next sequentially addressed 8 bit word (see Figure 8).

To provide sequential reads the 24AA16 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The 24AA16 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

PIN DESCRIPTIONS

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 KHz, 1KΩ for 400 KHz) from 24LC04B/08B.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

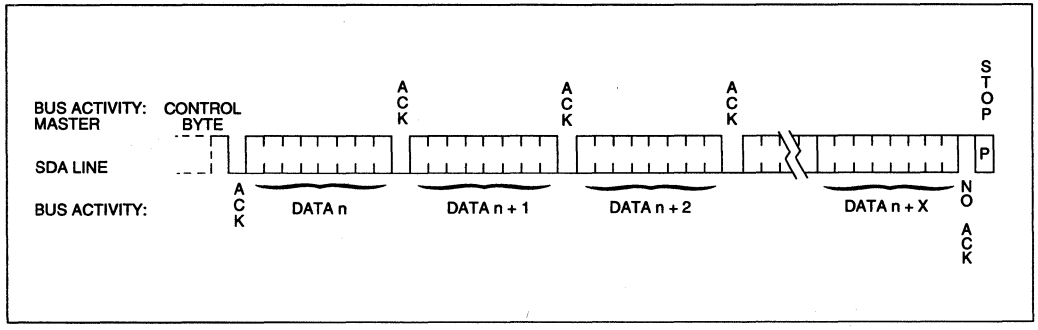
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24AA16 as a serial ROM when WP is enabled (tied to Vcc).

A0, A1, A2

These pins are not used by the 24AA16. They may be left floating or tied to either Vss or Vcc.

FIGURE 8 - SEQUENTIAL READ



NOTES

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

24AA16 - / P

PACKAGE:	P	PLASTIC DIP
	SL	PLASTIC SOIC (150 mil Body), 14-Lead
	SN	PLASTIC SOIC (150 mil Body), 8-Lead
TEMPERATURE RANGE:	Blank	0°C to +70°C
DEVICE:	24AA16	1.8 V, 16K CMOS Serial EEPROM
	24AA16T	1.8 V, 16K CMOS Serial EEPROM (in Tape and Reel Form)

MICROCHIP

24LC164

16K 2.5V Cascadable CMOS Serial EEPROM

FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 5 μA standby current typical at 3.0V
- Functional device select lines A0, A1, A2 for up to eight devices on the same bus
- Two wire serial interface bus, I²C compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 KHz (2.5V) and 400 KHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write-protect for the entire memory
- Can be operated as serial ROM
- ESD protection > 4,000V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP, 8-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to + 70°C
  - Industrial: -40°C to + 85°C

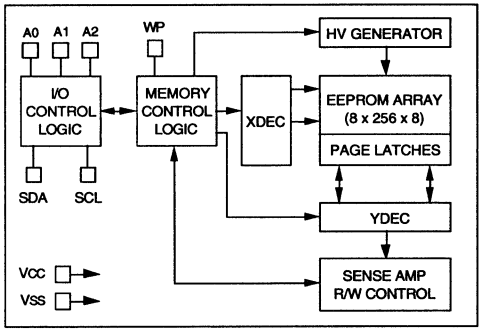
DESCRIPTION

The Microchip Technology Inc. 24LC164 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 2.5 volts with typical standby and active currents of only 5 μA and 1 mA respectively. The 24LC164 also has a page-write capability for up to 16 bytes of data. The 24LC164 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

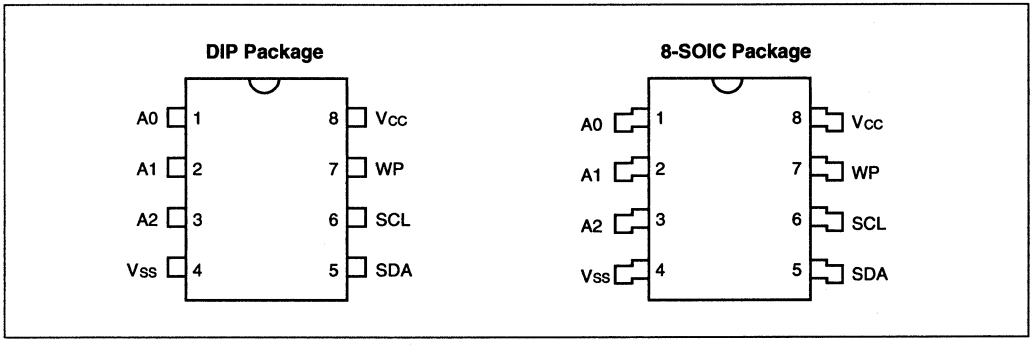
The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

5

BLOCK DIAGRAM



24LC164 PIN CONFIGURATION



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the sales offices below or contact corporate headquarters for the representative or distributor in your area.

PART NUMBERS

24LC164 - /P

PACKAGE:		P	PLASTIC DIP
		SN	PLASTIC SOIC (150 mil Body), 8-Lead
TEMPERATURE RANGE:		Blank	0°C to +70°C
		I	-40°C to +85°C
DEVICE:		24LC164	16K CMOS Serial EEPROM
		24LC164T	16K CMOS Serial EEPROM (in Tape and Reel form)

MICROCHIP

24AA164

16K 1.8V Cascadable CMOS Serial EEPROM

FEATURES

- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 5 µA standby current typical at 3.0V
  - 3 µA standby current typical at 1.8V
- Functional device select lines A0, A1, A2 for up to eight devices on the same bus
- Two wire serial interface bus, I²C compatible
- Schmitt trigger filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 KHz and 400 KHz compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write-protect for the entire memory
- Can be operated as a serial ROM
- ESD protection > 4,000V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP, 8-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to + 70°C

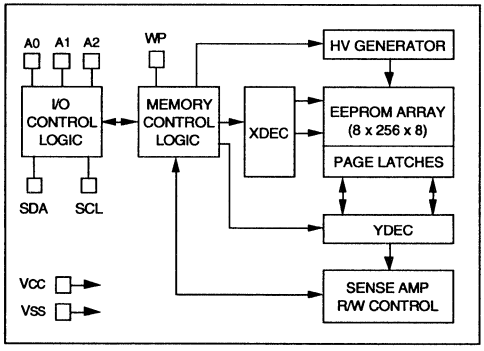
DESCRIPTION

The Microchip Technology Inc. 24AA164 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 1.8 volts with typical standby and active currents of only 3 µA and 1 mA respectively. The 24AA164 also has a page-write capability for up to 16 bytes of data. The 24AA164 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

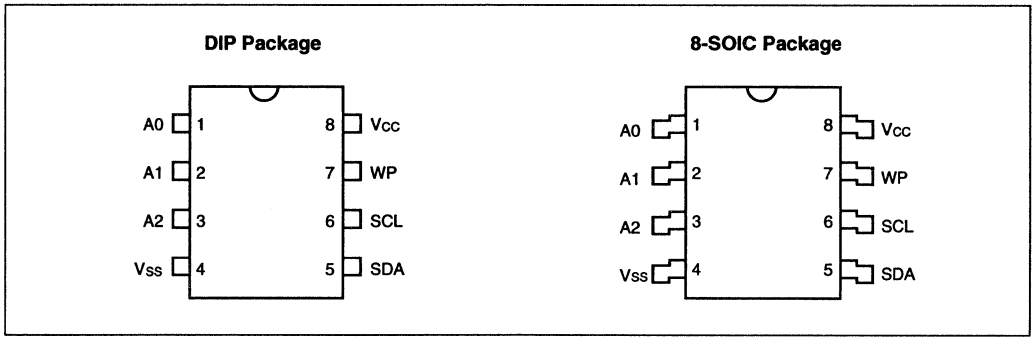
The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

5

BLOCK DIAGRAM



24AA164 PIN CONFIGURATION



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the sales offices below or contact corporate headquarters for the representative or distributor in your area.

PART NUMBERS

24AA164 - /P

PACKAGE:	P	PLASTIC DIP
	SN	PLASTIC SOIC (150 mil Body), 8-Lead
TEMPERATURE RANGE:	Blank	0°C to +70°C
DEVICE:	24AA164	16K CMOS Serial EEPROM
	24AA164T	16K CMOS Serial EEPROM (in Tape and Reel form)

MICROCHIP

24LC174

16K 2.5V CMOS Serial EEPROM with OTP Security Page

FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 5 µA standby current typical at 3.0V
- Functional device select lines A0, A1, A2 for up to 8 devices on the same bus
- 16 byte OTP security page
- Two wire serial interface bus
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 KHz and 400 KHz compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write-protect for the entire memory
- Can be operated as a serial ROM
- ESD protection > 4,000V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP, 8-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to + 70°C
  - Industrial: -40°C to + 85°C

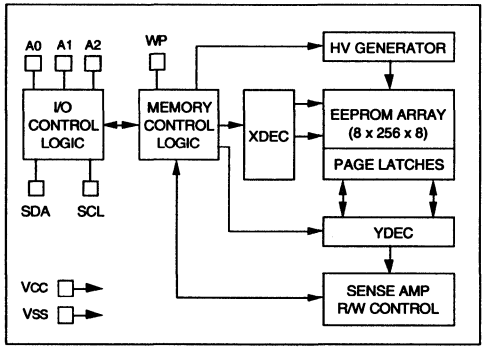
DESCRIPTION

The Microchip Technology Inc. 24LC174 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface and provides a specially addressed, OTP (one-time programmable) 16 byte security block. Low voltage design permits operation down to 2.5 volts with typical standby and active currents of only 5 µA and 1 mA respectively. The 24LC174 also has a page-write capability for up to 16 bytes of data. The 24LC174 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

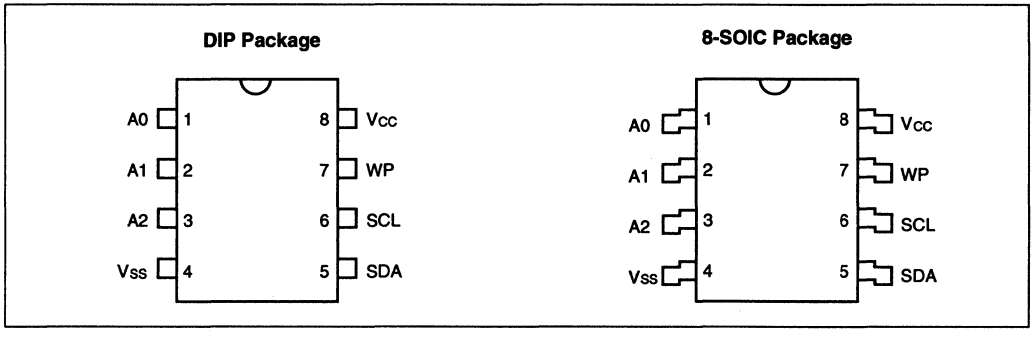
The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

5

BLOCK DIAGRAM



24LC174 PIN CONFIGURATION



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the sales offices below or contact corporate headquarters for the representative or distributor in your area.

PART NUMBERS

24LC174 - /P

PACKAGE:	P	PLASTIC DIP
	SN	PLASTIC SOIC (150 mil Body), 8-Lead
TEMPERATURE RANGE:	Blank	0° C to +70° C
	I	-40° C to +85° C
DEVICE:	24LC174	16K CMOS Serial EEPROM
	24LC174T	16K CMOS Serial EEPROM (in Tape and Reel form)

MICROCHIP

24AA174

16K 1.8V CMOS Serial EEPROM with OTP Security Page

FEATURES

- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 5 µA standby current typical at 3.0V
- Functional device select lines A0, A1, A2 for up to 8 devices on the same bus
- 16 byte OTP security page
- Two wire serial interface bus
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 KHz and 400 KHz compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write-protect for the entire memory
- Can be operated as a serial ROM
- ESD protection > 4,000V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP, 8-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to + 70°C

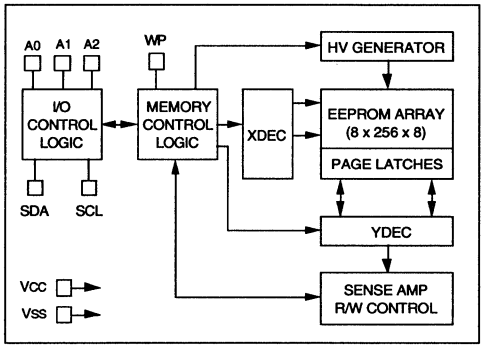
DESCRIPTION

The Microchip Technology Inc. 24AA174 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface and provides 16 byte security block. Low voltage design permits operation down to 1.8 volts with typical standby and active currents of only 3 µA and 1 mA respectively. The 24AA174 also has a page-write capability for up to 16 bytes of data. The 24AA174 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

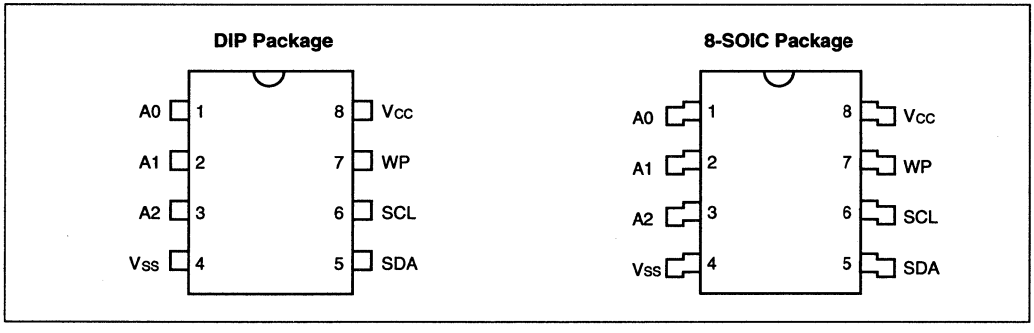
The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

5

BLOCK DIAGRAM



24AA174 PIN CONFIGURATION



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the sales offices below or contact corporate headquarters for the representative or distributor in your area.

PART NUMBERS

24AA174 - /P

PACKAGE:	P	PLASTIC DIP
	SN	PLASTIC SOIC (150 mil Body), 8-Lead
TEMPERATURE RANGE:	Blank	0°C to +70°C
DEVICE:	24AA174	16K CMOS Serial EEPROM
	24AA174T	16K CMOS Serial EEPROM (in Tape and Reel form)

MICROCHIP

24C32

32K 5V CMOS Serial EEPROM

FEATURES

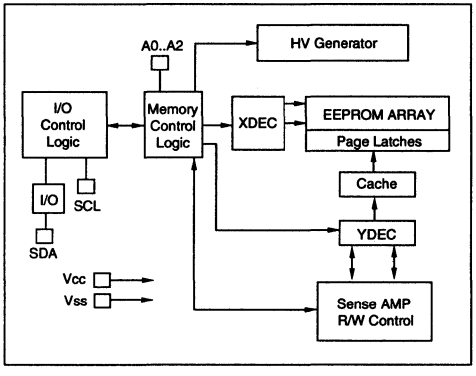
- Voltage operating range: 4.5V to 5.5V
  - Peak write current 3 mA at 5.5V
  - Maximum read current 150 µA at 5.5V
  - Standby current 5 µA typical
- Industry standard two-wire bus protocol, I²C™ compatible
  - Including 100 KHz and 400 KHz modes
- Self-timed write cycle (including auto-erase)
- Power on/off data protection circuitry
- Endurance: - 20K Erase/Write cycles typical (28K block)
  - 1 million E/W cycles typical (4K block)
- 8 byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Factory programming (QTP) available
- Up to 8 chips may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 40 years
- 8-pin PDIP/SOIC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

The Microchip Technology Inc. 24C32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24C32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24C32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to 8 - 24C32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24C32 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

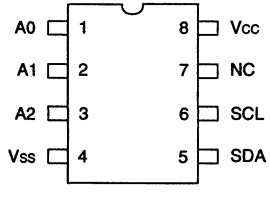
5

BLOCK DIAGRAM

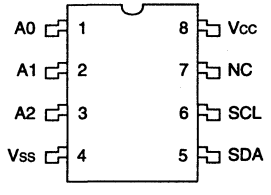


PIN CONFIGURATIONS

PDIP Package



SOIC Package



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ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied .... -65°C to +125°C
Soldering temperature of leads (10 seconds) . +300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1 - PIN FUNCTIONS

Name	Function
A0..A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

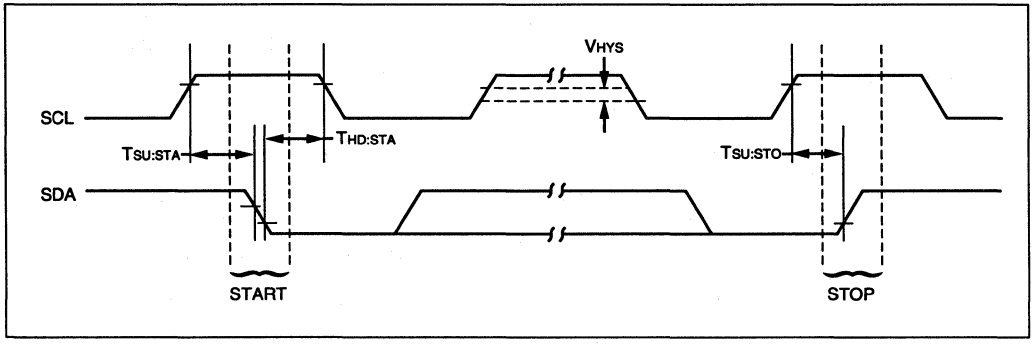
DC CHARACTERISTICS

VCC = +4.5V to 5.5V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min.	Max.	Units	Conditions
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC Write	—	3	mA	VCC = 5.5V, SCL = 400 KHz
	ICC Read	—	150	µA	VCC = 5.5V, SCL = 400 KHz
Standby current	ICCS	—	50	µA	VCC = 5.5V, SCL = SDA = VCC

Note 1: This parameter is periodically sampled and not 100% tested.

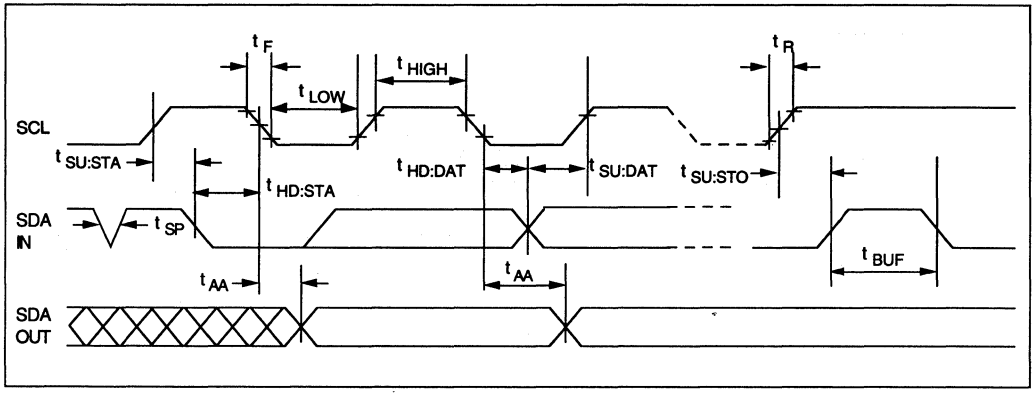
FIGURE 1 - BUS TIMING START/STOP



AC CHARACTERISTICS		Vcc = 4.5-5.5V STD. MODE		Vcc = 4.5-5.5V FAST MODE			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**	**Remarks**
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 1
SDA and SCL fall time	TF	—	300	—	300	ns	Note 1
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 2
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 1, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	5	—	5	ms/page	Note 4

Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.
Note 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.
Note 4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

FIGURE 2 - BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C32 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C32 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3).

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

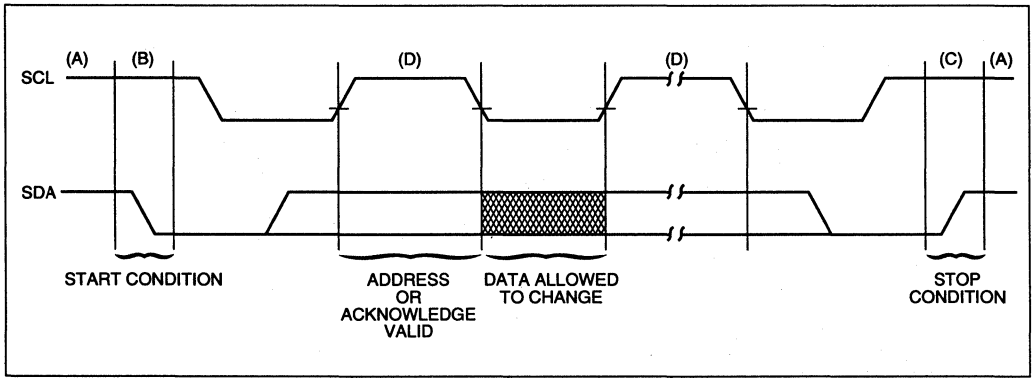
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C32 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24C32) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

Device Addressing and Operation (Figure 4A)

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code; for the 24C32 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte ($R/\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (see Figure 4B). Because only A11..A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first. Following the start condition, the 24C32 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the $R/\overline{W}$ bit, the 24C32 will select a read or write operation.

Operation	Control Code	Device Select	$R/\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 4A - CONTROL BYTE ALLOCATION

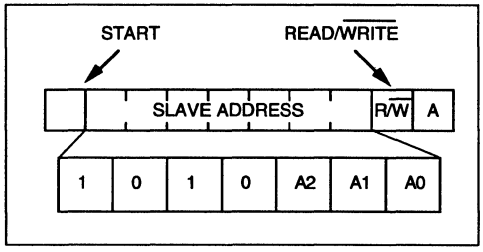


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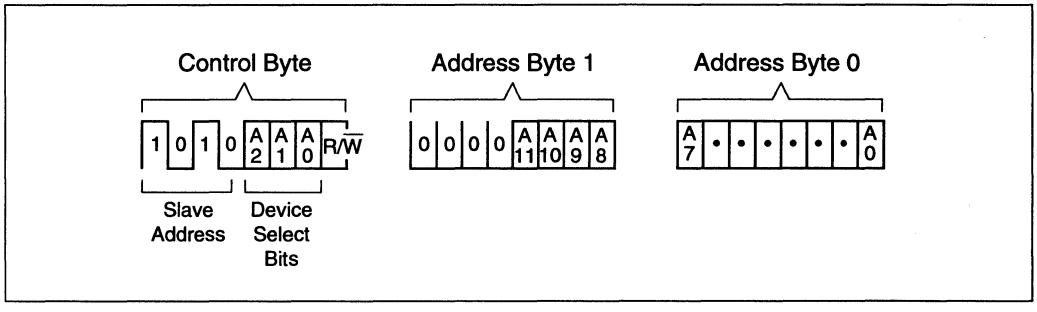
FIGURE 4B - ADDRESS SEQUENCE BIT ASSIGNMENTS



WRITE OPERATION

Split Endurance

The 24C32 is organized as a continuous 32K block of memory. However, the first 4K, starting at address 000, is rated at 1 million E/W cycles typical. The remainder of the array, 28K bits, is rated at 20K E/W cycles typical. This feature is helpful in applications in which some data change frequently, while a majority of the data change infrequently. One example would be a cellular telephone in which last-number redial and microcontroller scratch pad require a high-endurance block, while speed dials and lookup tables change infrequently and so require only a standard endurance rating.

Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24C32. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24C32 the master device will transmit the data word to be written into the addressed memory location. The 24C32 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C32 will not generate acknowledge signals (see Figure 5).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24C32 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24C32. They will be written from cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once a stop condition is received, an internal write cycle will begin. The 64-byte cache will continue to capture data until a stop condition occurs or the operation is aborted (see Figure 6).

FIGURE 5 - BYTE WRITE

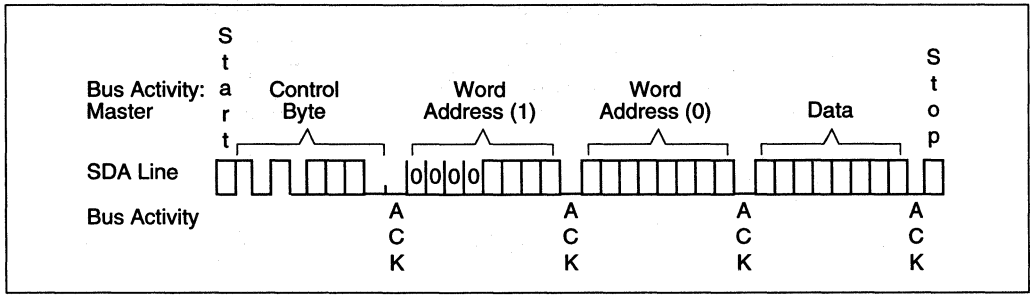
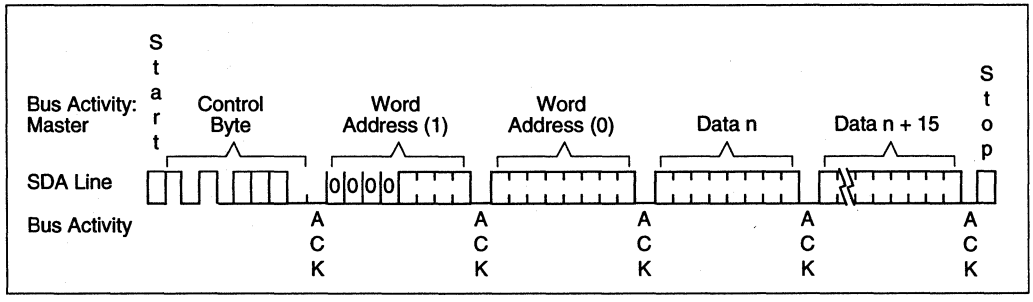


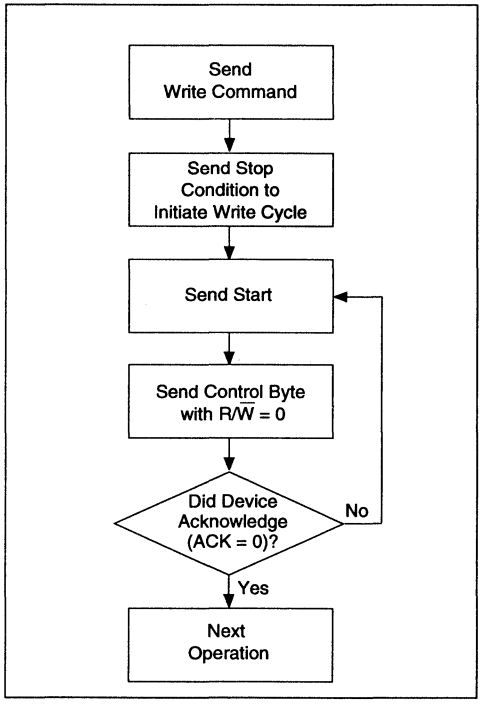
FIGURE 6 - PAGE WRITE (For cache WRITE, see Figure 10)



ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7 for flow diagram.

FIGURE 7 - ACKNOWLEDGE POLLING FLOW



READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24C32 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24C32 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C32 discontinues transmission (see Figure 8).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C32 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C32 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24C32 to discontinue transmission (see Figure 9).

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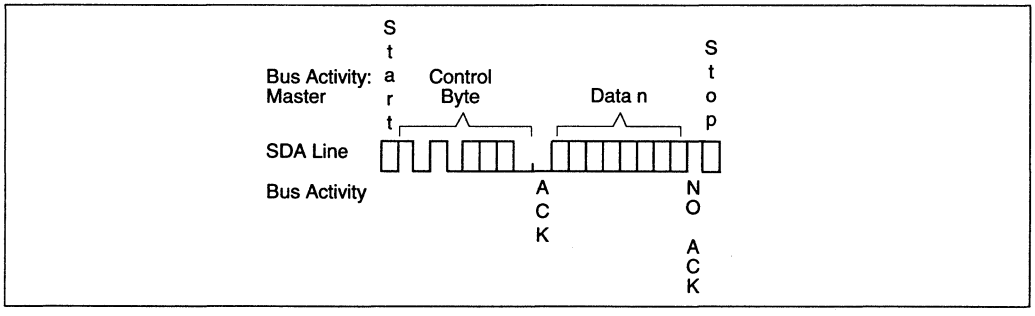
FIGURE 8 - CURRENT ADDRESS READ



Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24C32's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C32 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24C32 to transmit the next sequentially addressed 8 bit word. (See Figure 10). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24C32 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The address pointer, however, will not roll over from address 07FF to address 0000. It will roll from 07FF to unused memory space.

Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to ensure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 KHz (Fast Mode) compatibility.

FIGURE 9 - RANDOM READ

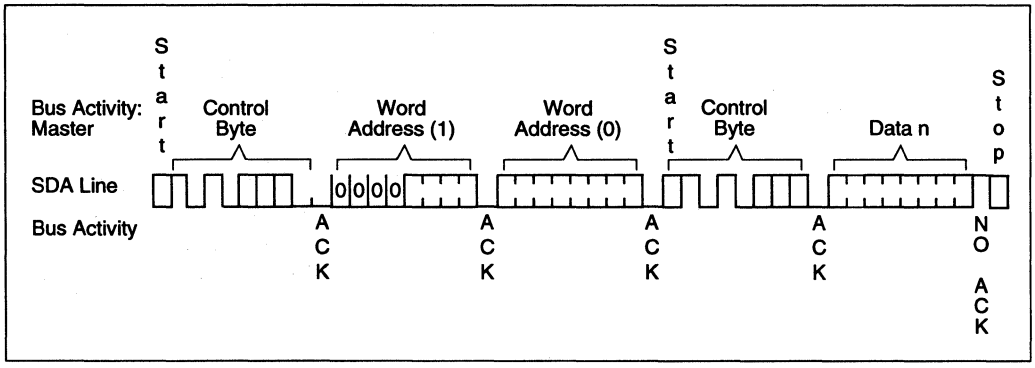
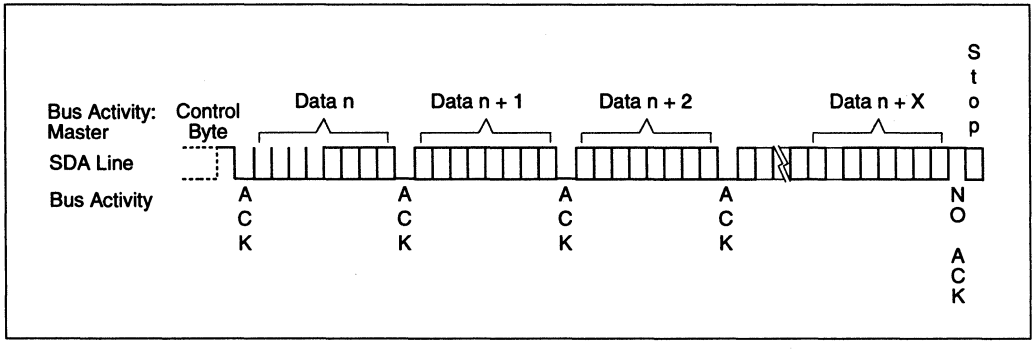


FIGURE 10 - SEQUENTIAL READ



PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 10 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten.

Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (see Figure 11) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown below (see Figure 12), a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

Power Management

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, ie. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates V_{DD} monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The V_{DD} monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

PIN DESCRIPTIONS

A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24C32 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (see Figure 4B).

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 KHz, 1KΩ for 400 KHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

FIGURE 11 - CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

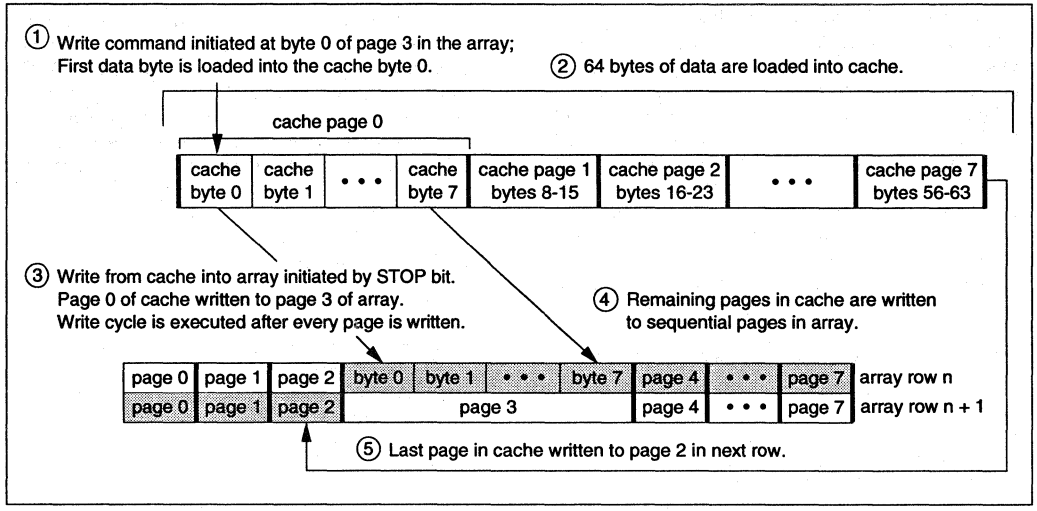
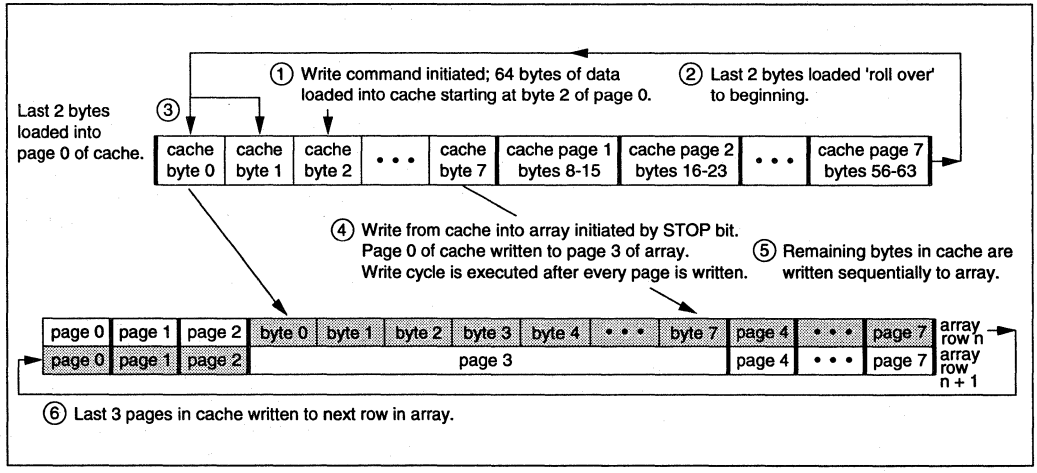


FIGURE 12 - CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY

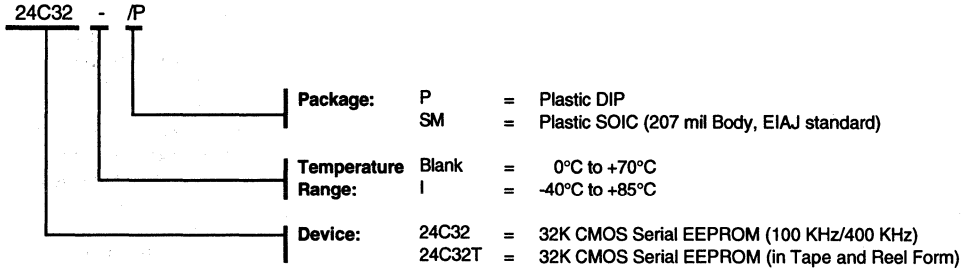


NOTES

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



MICROCHIP

24LC32

32K 2.5V CMOS Serial EEPROM

FEATURES

- Voltage operating range: 2.5V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150 µA at 6.0V
  - Standby current 5 µA typical
- Industry standard two-wire bus protocol, I²C™ compatible
  - Including 100 KHz (2.5V) and 400 KHz (5V) modes
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Endurance: - 20K Erase/Write cycles typical (28K block)
  - 1 million E/W cycles typical (4K block)
- 8 byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Factory programming (QTP) available
- Up to 8 devices may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 40 years
- 8-pin PDIP/SOIC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

The Microchip Technology Inc. 24LC32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (2.5V to 6.0V). This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24LC32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24LC32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to 8 - 24LC32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology and broad voltage range make this device ideal for low-power/low voltage, nonvolatile code and data applications. The 24LC32 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

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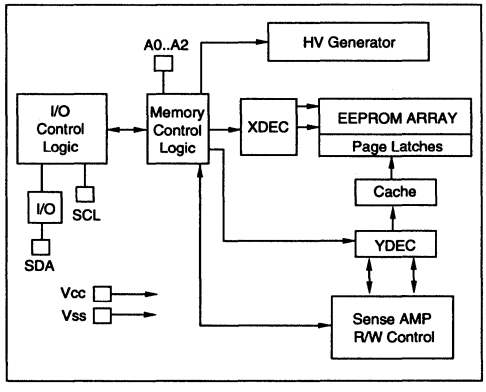
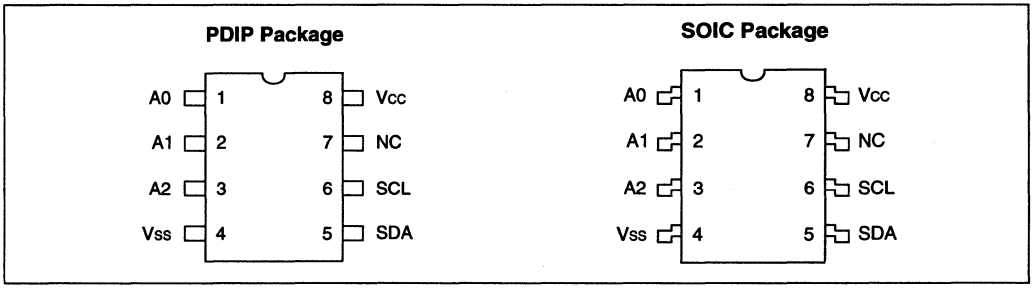
BLOCK DIAGRAM



PIN CONFIGURATIONS



I²C™ is a trademark of Philips Corporation

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to+150°C
Ambient temp. with power applied .... -65°C to +125°C
Soldering temperature of leads (10 seconds) . +300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1 - PIN FUNCTIONS

Name	Function
A0..A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+2.5V to 6.0V Power Supply
NC	**No Internal Connection**

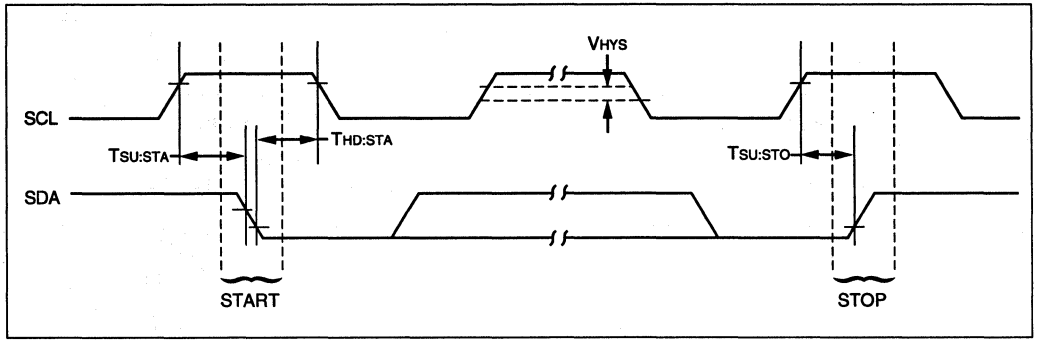
DC CHARACTERISTICS

Vcc = +2.5V to 6.0V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min.	Max.	Units	Conditions
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 Vcc	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	Vcc = 5.0V (Note 1) Tamb = 25°C, Fclk = 1 MHz
Operating current	Icc Write	—	3	mA	Vcc = 6.0V, SCL = 400 KHz
	Icc Read	—	150	µA	Vcc = 6.0V, SCL = 400 KHz
Standby current	Iccs	—	50	µA	Vcc = 6.0V, SCL = SDA = Vcc

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1 - BUS TIMING START/STOP



AC CHARACTERISTICS		Vcc = 2.5V-6.0V STD. MODE		Vcc = 4.5V-6.0V FAST MODE			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**	**Remarks**
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 1
SDA and SCL fall time	TF	—	300	—	300	ns	Note 1
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 2
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 1, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	5	—	5	ms/page	Note 4

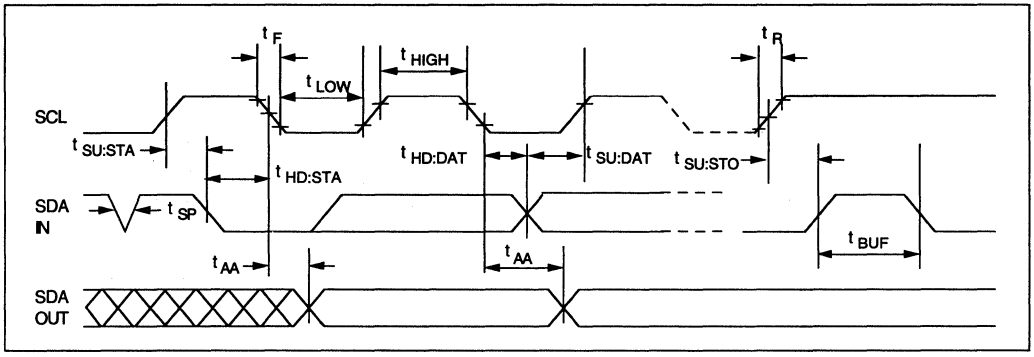
Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.

Note 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

Note 4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

FIGURE 2 - BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24LC32 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC32 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (See Figure 3).

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

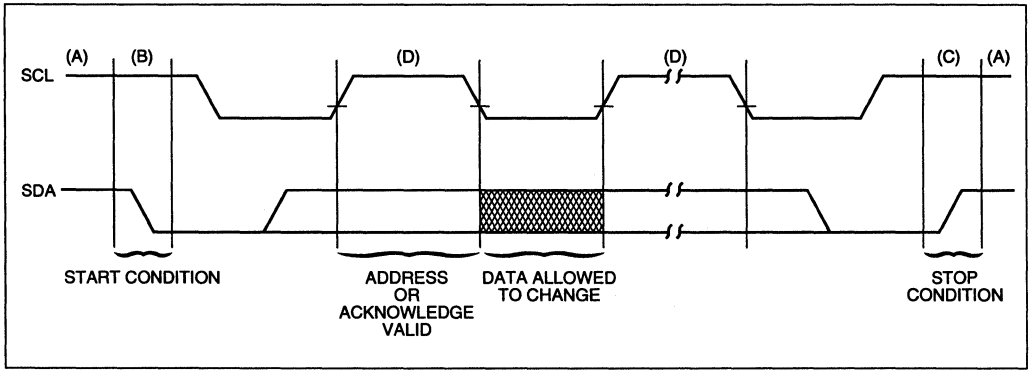
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC32 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC32) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

Device Addressing and Operation (Figure 4A)

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code; for the 24LC32 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (see Figure 4B). Because only A11...A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first. Following the start condition, the 24LC32 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC32 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 4A - CONTROL BYTE ALLOCATION

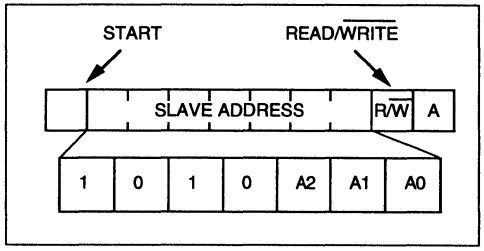
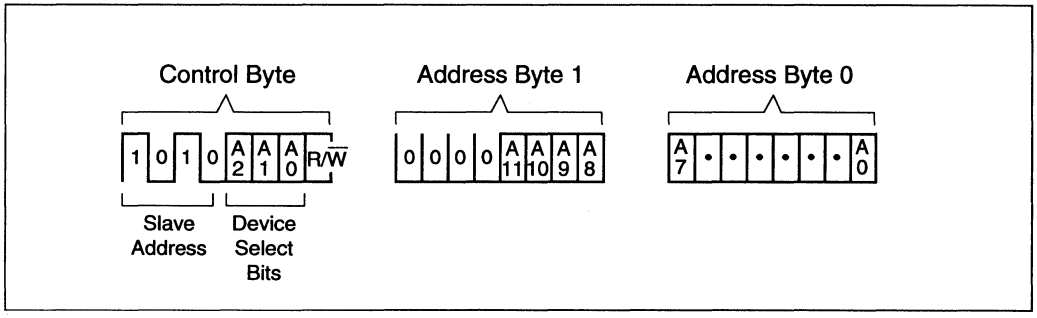


FIGURE 4B - ADDRESS SEQUENCE BIT ASSIGNMENTS



WRITE OPERATION

Split Endurance

The 24C32 is organized as a continuous 32K block of memory. However, the first 4K, starting at address 000, is rated at 1 million E/W cycles typical. The remainder of the array, 28K bits, is rated at 20K E/W cycles typical. This feature is helpful in applications in which some data change frequently, while a majority of the data change infrequently. One example would be a cellular telephone in which last-number redial and microcontroller scratch pad require a high-endurance block, while speed dials and lookup tables change infrequently and so require only a standard endurance rating.

Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/W bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24LC32. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24LC32 the master device will transmit the data word to be written into the addressed memory location. The 24LC32 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC32 will not generate acknowledge signals (see Figure 5).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC32 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24LC32. They will be written from cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once a stop condition is received, an internal write cycle will begin. The 64-byte cache will continue to capture data until a stop condition occurs or the operation is aborted (see Figure 6).

FIGURE 5 - BYTE WRITE

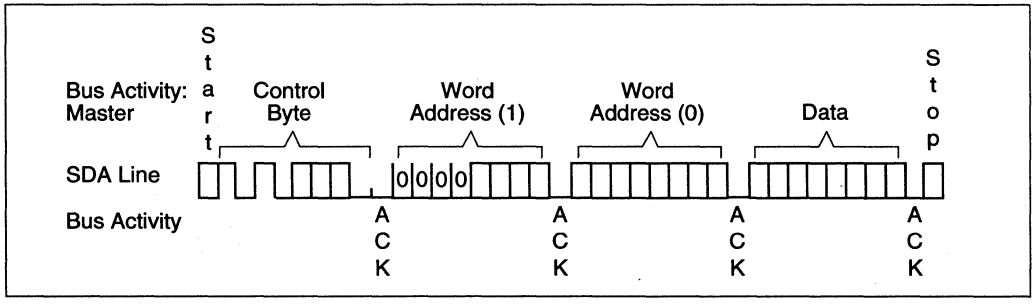
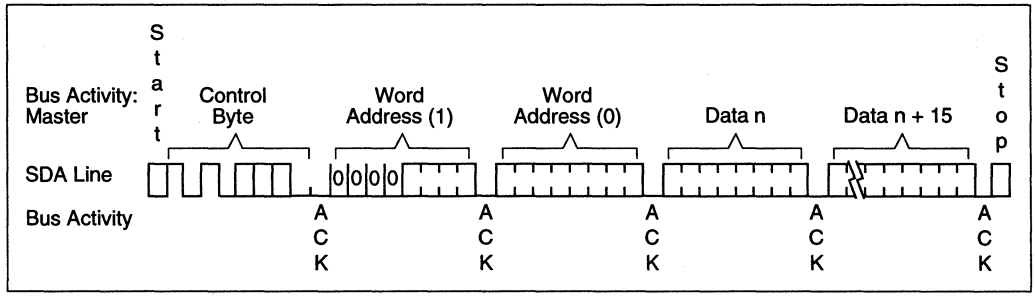


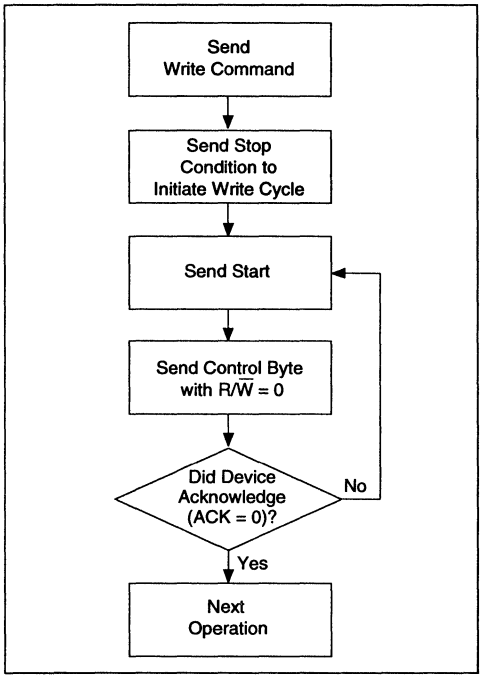
FIGURE 6 - PAGE WRITE (For cache WRITE, see Figure 11)



ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7 for flow diagram.

FIGURE 7 - ACKNOWLEDGE POLLING FLOW



READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

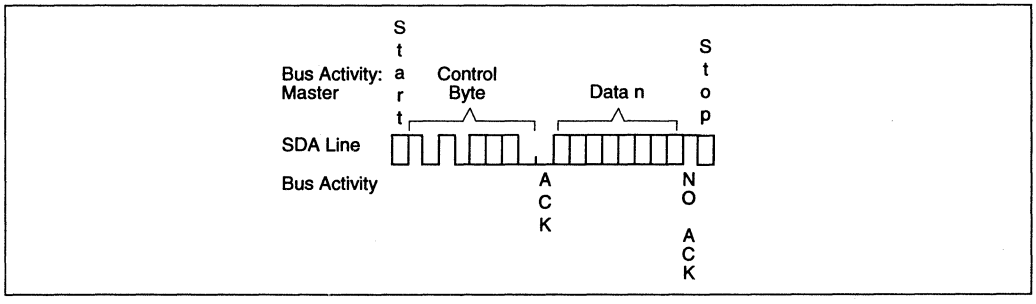
Current Address Read

The 24LC32 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/W bit set to one, the 24LC32 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC32 discontinues transmission (see Figure 8).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC32 as part of a write operation (R/W bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/W bit set to a one. The 24LC32 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24LC32 to discontinue transmission (see Figure 9).

FIGURE 8 - CURRENT ADDRESS READ



Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24LC32's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC32 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24LC32 to transmit the next sequentially addressed 8 bit word (see Figure 10). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24LC32 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The address pointer, however, will not roll over from address 07FF to address 0000. It will roll from 07FF to unused memory space.

Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to ensure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 KHz (Fast Mode) compatibility.

FIGURE 9 - RANDOM READ

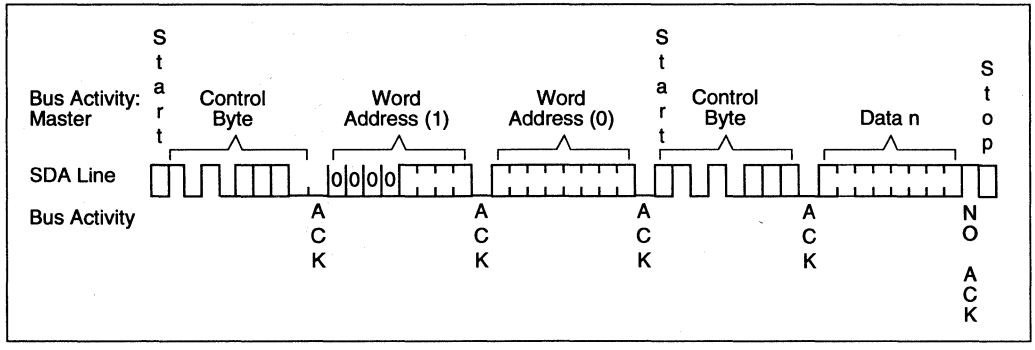
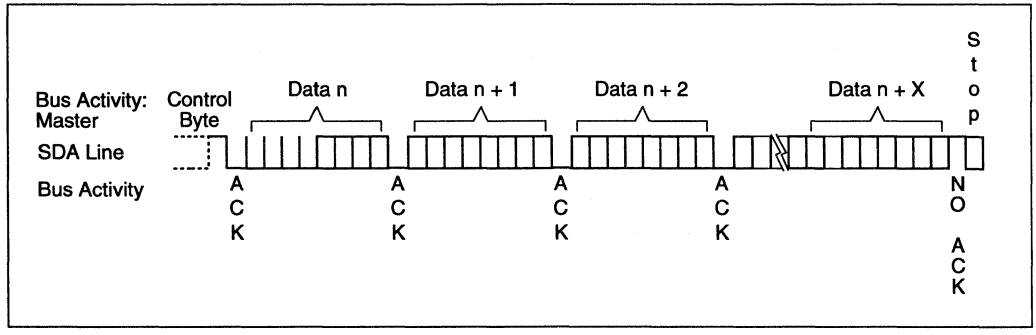


FIGURE 10 - SEQUENTIAL READ



PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 10 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten.

Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (see Figure 11) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown below (see Figure 12), a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

Power Management

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, ie. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

5

PIN DESCRIPTIONS

A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24LC32 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (see Figure 4B).

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 KHz, 1KΩ for 400 KHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

FIGURE 11 - CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

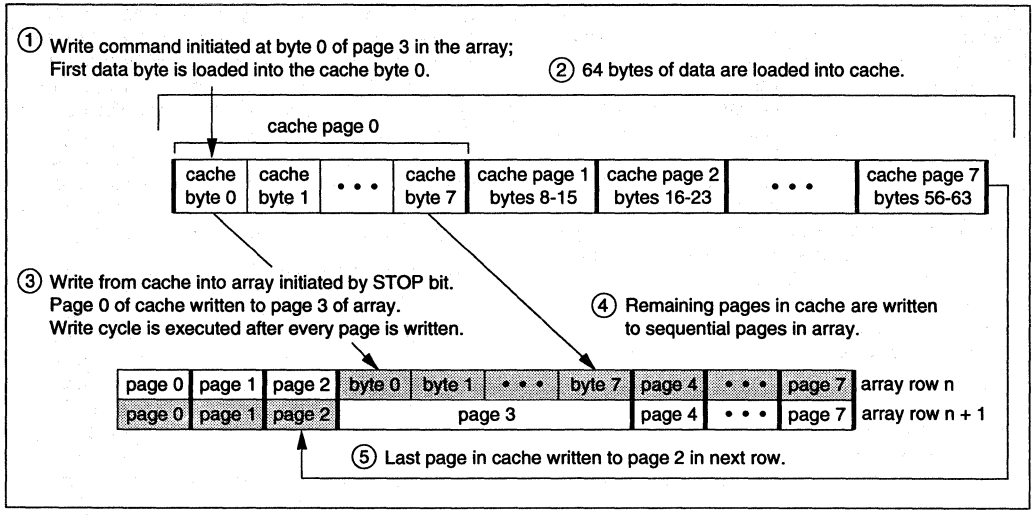
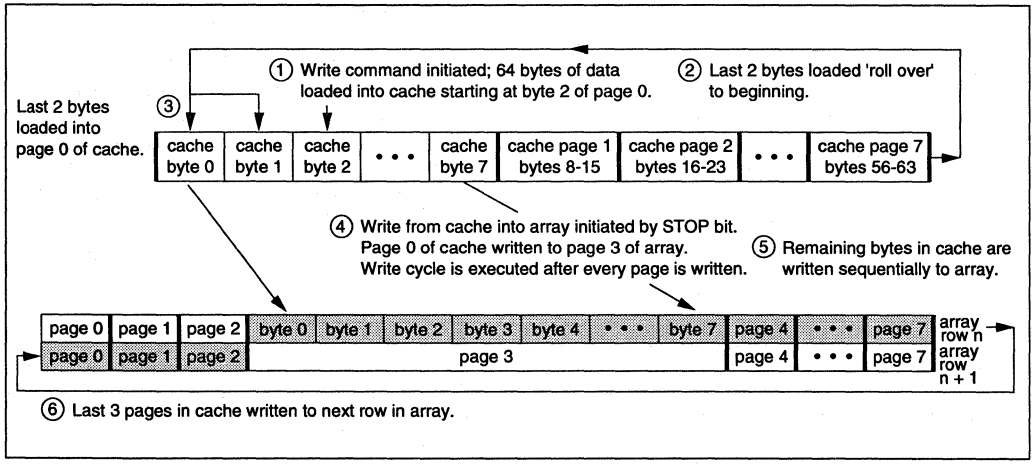


FIGURE 12 - CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY

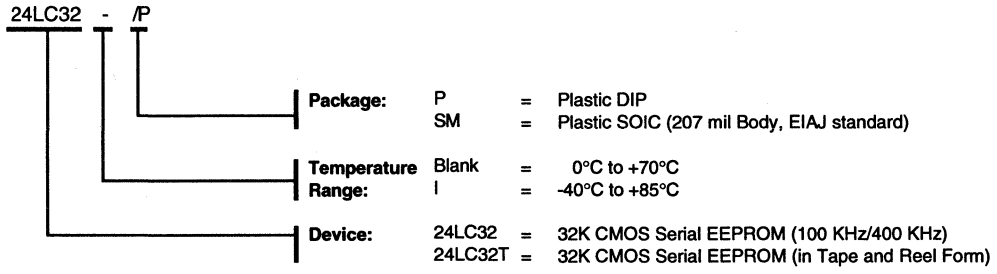


NOTES

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



MICROCHIP

24C65

64K 5V CMOS Smart Serial™ EEPROM

FEATURES

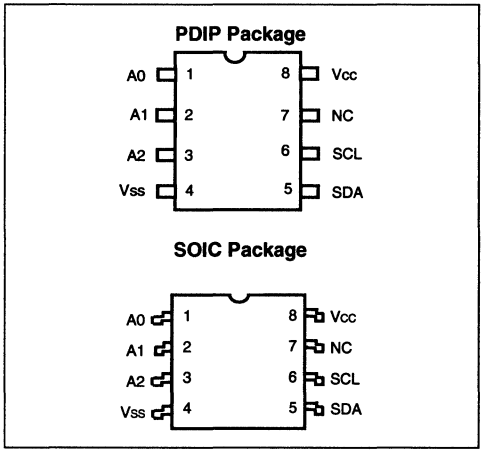
- Voltage operating range: 4.5V to 5.5V
  - Peak write current 3 mA at 5.5V
  - Maximum read current 150 µA at 5.5V
  - Standby current 5 µA typical
- Industry standard two wire bus protocol, I²C™ compatible
  - Including 400 KHz Mode
- Programmable block security options
- Programmable endurance options
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- Self-timed ERASE (E) and WRITE (W) cycles
- Power on/off data protection circuitry
- Endurance: 1 million E/W for a 4K block (typical)
  10,000 E/W for a 60K block (typical)
- 8 byte page, or byte modes available
- 1 page x 8 line input cache for fast write loads
- Electrostatic discharge protection > 4000V
- Data retention > 40 years
- 8-pin PDIP/SOIC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
- 2 ms typical write cycle time, byte or page
- Up to 8 devices may be connected to the same bus for up to 512K bits total memory

DESCRIPTION

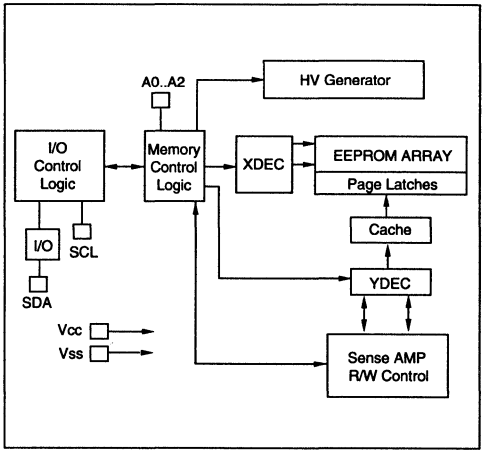
The Microchip Technology Inc. 24C65 is a "smart" 8K x 8 Serial Electrically Erasable PROM (EEPROM). This device has been developed for advanced, low power applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. The 24C65 offers a relocatable 4K bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 10,000 ERASE/WRITE (E/W) cycles typical. The 24C65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to fifteen 4K blocks. Functional address lines allow the connection of up to eight 24C65's on the same bus for up to 512K bits contiguous EEPROM memory. Advanced CMOS technology makes this device ideal for low-power nonvolatile code and data applications. The 24C65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

5

PIN CONFIGURATIONS



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation
Smart Serial is a trademark of Microchip Technology Inc.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V
Storage temperature ..... -65°C to+150°C
Ambient temp. with power applied .... -65°C to +125°C
Soldering temperature of leads (10 seconds) . +300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0..A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

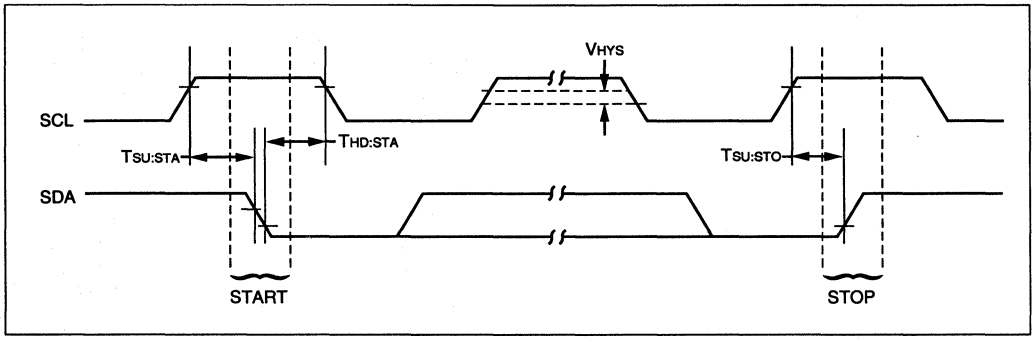
DC CHARACTERISTICS

Vcc = +4.5V to 5.5V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min.	Max.	Units	Conditions
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 Vcc	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	Vcc = 5.0V (Note 1) Tamb = 25°C, Fclk = 1 MHz
Operating current	Icc Write	—	3	mA	Vcc = 5.5V, SCL = 400 KHz
	Icc Read	—	150	µA	Vcc = 5.5V, SCL = 400 KHz
Standby current	Iccs	—	50	µA	Vcc = 5.5V, SCL = SDA = Vcc

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1 - BUS TIMING START/STOP



AC CHARACTERISTICS		Vcc = 2.5V-5.5V STD. MODE		Vcc = 4.5V-5.5V FAST MODE			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**	**Remarks**
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 1
SDA and SCL fall time	TF	—	300	—	300	ns	Note 1
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 2
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 1, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	5	—	5	ms/page	Note 4

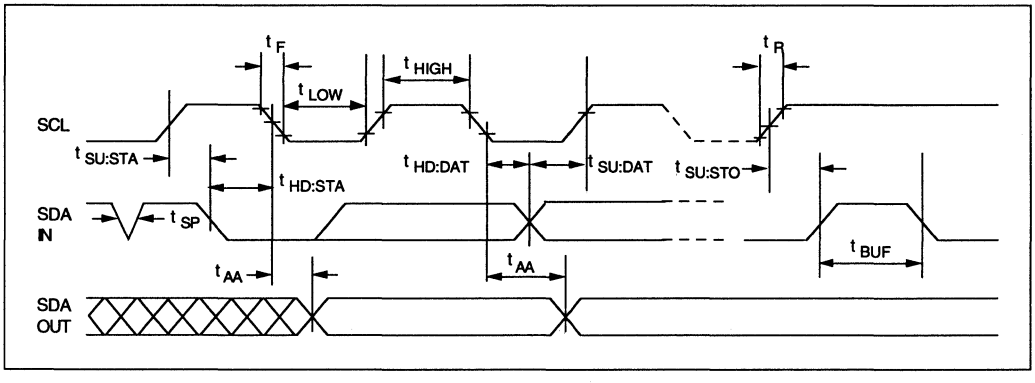
Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.

Note 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

Note 4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

FIGURE 2 - BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C65 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C65 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (See Figure 3).

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

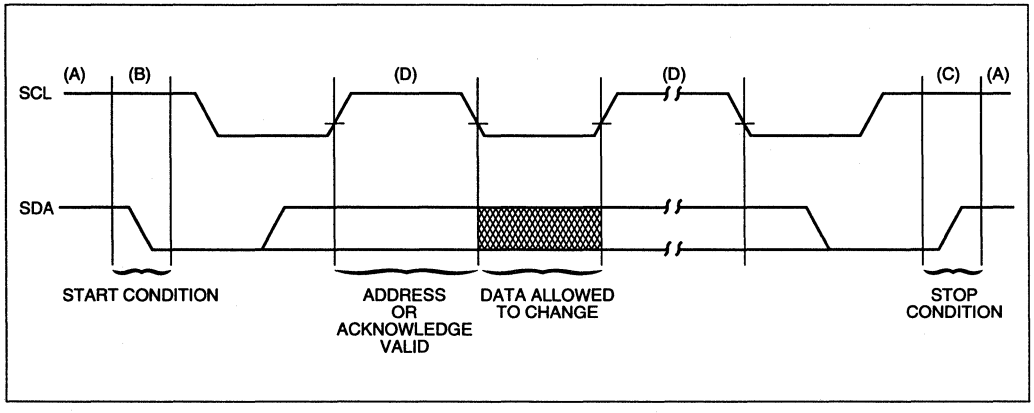
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C65 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24C65) must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



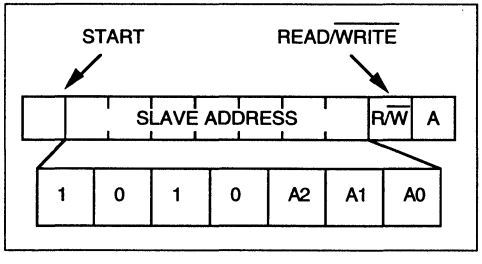
BUS CHARACTERISTICS

Device Addressing and Operation (Figure 4)

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24C65 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte ($R/\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (see Figure 5). Because only A12..A0 are used, the upper three address bits must be zeros. The most significant bit of the most significant byte is transferred first. Following the start condition, the 24C65 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device (24C65) outputs an acknowledge signal on the SDA line. Depending upon the state of the $R/\overline{W}$ bit, the 24C65 will select a read or write operation.

Operation	Control Code	Device Select	$R/\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 4 - CONTROL BYTE ALLOCATION



WRITE OPERATION

Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the $R/\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver (24C65) that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24C65. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24C65 the master device will transmit the data word to be written into the addressed memory location. The 24C65 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C65 will not generate acknowledge signals (see Figure 5).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24C65 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24C65. They will be written from the cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once the stop condition is received an internal write cycle will begin. The 64 byte cache will continue to capture data until a stop condition occurs or the operation is aborted (see Figure 6).

FIGURE 5 - BYTE WRITE

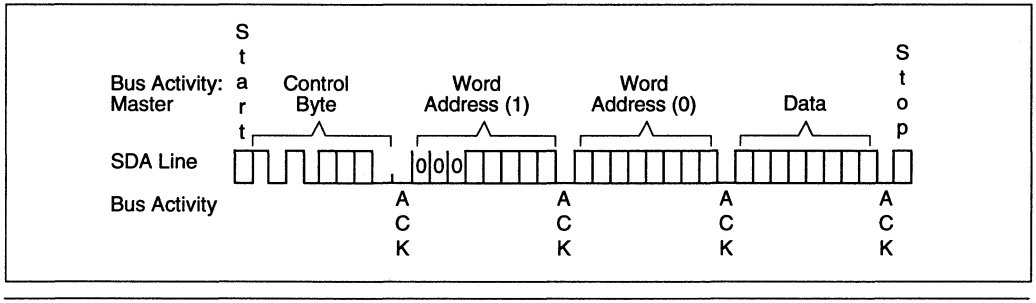


FIGURE 6 - PAGE WRITE (For cache WRITE, see Figure 12)

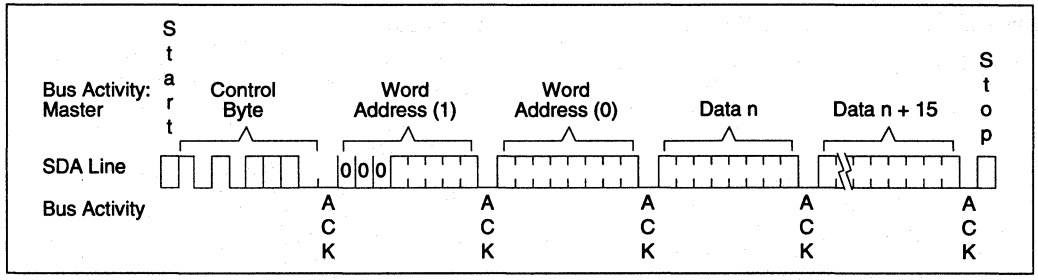


FIGURE 7 - CURRENT ADDRESS READ

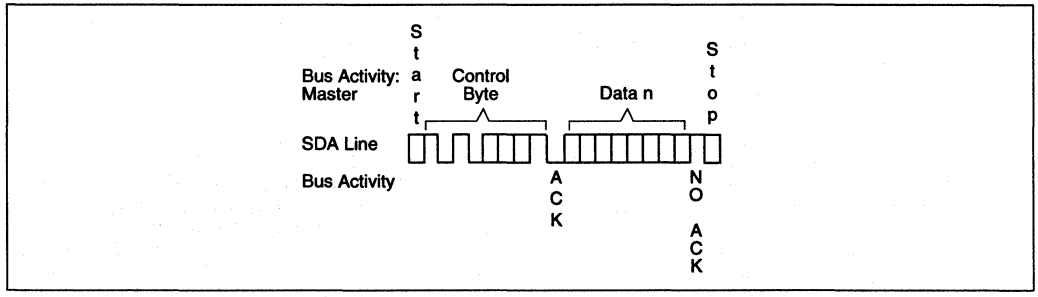


FIGURE 8 - RANDOM READ

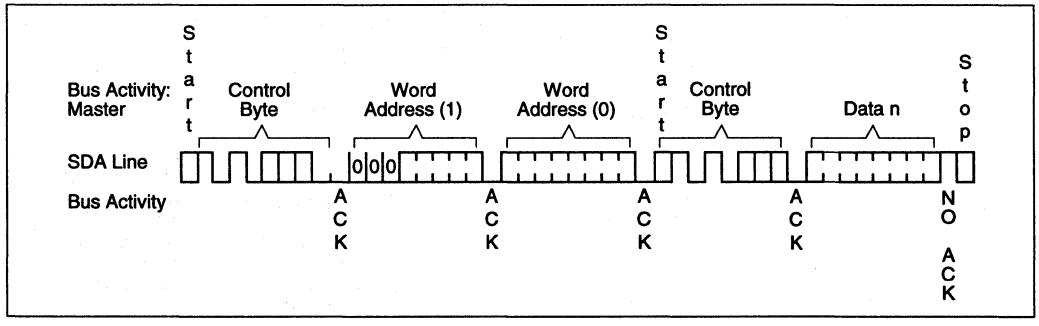
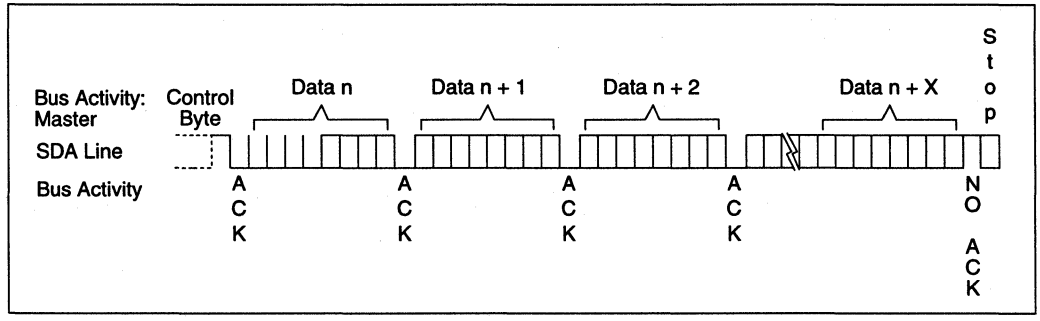


FIGURE 9 - SEQUENTIAL READ



READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24C65 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24C65 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C65 discontinues transmission (see Figure 7).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C65 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C65 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24C65 to discontinue transmission (see Figure 8).

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C65 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24C65 to transmit the next sequentially addressed 8 bit word (see Figure 9). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24C65 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24C65's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15.

Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 KHz (Fast Mode) compatibility.

High Endurance Block

The location of the high-endurance block within the memory map is programmed by setting the leading bit 7 (S/$\overline{HE}$) of the configuration byte to 0. The upper bits of the address loaded in this command will determine which 4K block within the memory map will be set to high endurance (see Figure 11). This block will be capable of one million erase/write cycles typical.

Note: The High Endurance Block cannot be changed after the security option has been set. If the H.E. block is not programmed by the user, the default location is the highest block of memory.

Security Options

The 24C65 has a sophisticated mechanism for write-protecting portions of the array. This write protect function is programmable and allows the user to protect 0-15 contiguous 4K blocks. The user sets the security option by sending to the device the starting block number for the protected region and the number of blocks to be protected. If the security option is invoked with 0 blocks protected, then all portions of the array will be unprotected. All parts will come from the factory in the default configuration with the starting block number set to 15 and the number of protected blocks set to zero. THE SECURITY OPTION CAN BE SET ONLY ONCE.

To invoke the security option, a write command is sent to the device with the leading bit (bit 7) of the first address byte set to a 1 (see Figure 11). Bits 1-4 of the first address byte define the starting block number for the protected region. For example, if the starting block number is to be set to 5, the first address byte would be 1XX0101X. Bits 0, 5 and 6 of the first address byte are disregarded by the device and can be either high or low. The device will acknowledge after the first address byte. A byte of don't care bits is then sent by the master, with the device acknowledging afterwards. The third byte sent to the device has bit 7 (S/$\overline{HE}$) set high and bit 6 (R) set low. Bits 4 and 5 are don't cares and bits 0-3 define the number of blocks to be write protected. For example, if three blocks are to be protected, the third byte would be 10XX0011. After the third byte is sent to the device, it will acknowledge and a STOP bit is then sent by the master to complete the command.

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During a normal write sequence, if an attempt is made to write to a protected address, no data will be written and the device will not report an error or abort the command. If a write command is attempted across a secure boundary, unprotected addresses will be written and protected addresses will not.

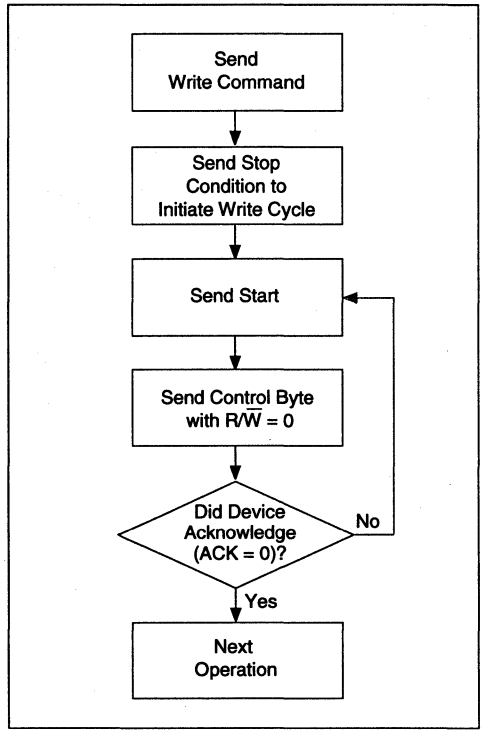
Security Configuration Read

The status of the secure portion of memory can be read by using the same technique as programming this option except the READ bit (bit 6) of the configuration byte is set to a one. After the configuration byte is sent, the device will acknowledge and then send two bytes of data to the master just as in a normal read sequence. The master must acknowledge the first byte and not acknowledge the second, and then send a stop bit to end the sequence. The upper four bits of both of these bytes will always be read as '1's. The lower four bits of the first byte contains the starting secure block. The lower four bits of the second byte contains the number of secure blocks. The default starting secure block is fifteen and the default number of secure blocks is zero (see Figure 11).

ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 10 for flow diagram.

FIGURE 10 - ACKNOWLEDGE POLLING FLOW



PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 10 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten.

Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (see Figure 12) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 13, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

Power Management

The design incorporates a power standby mode when not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates V_{DD} monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The V_{DD} monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

PIN DESCRIPTIONS

A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24C65 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (see Figures 4 and 11).

SDA Serial Address/Data Input/Output

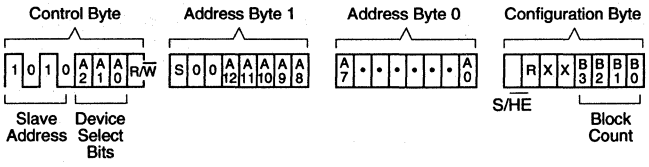
This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to V_{CC} (typical 10KΩ for 100 KHz, 1KΩ for 400 KHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

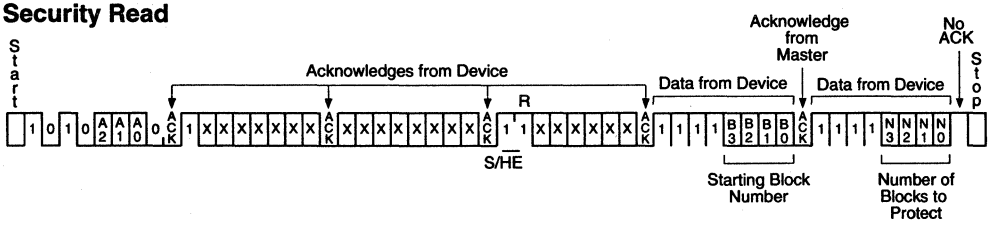
SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

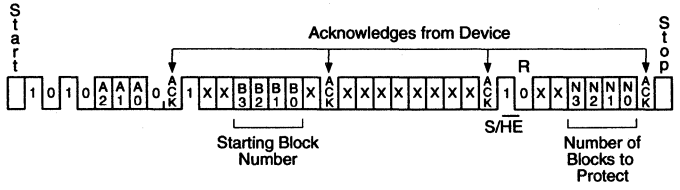
FIGURE 11 - CONTROL SEQUENCE BIT ASSIGNMENTS



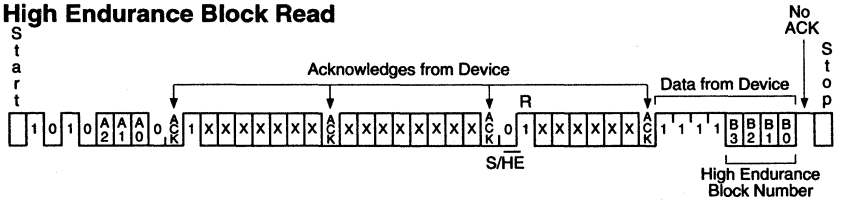
Security Read



Security Write



High Endurance Block Read



High Endurance Block Write

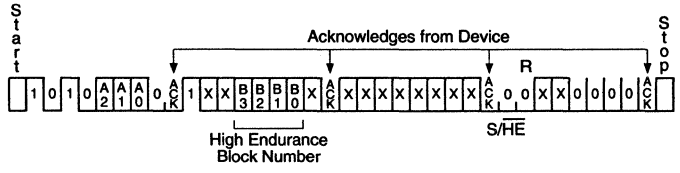


FIGURE 12 - CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

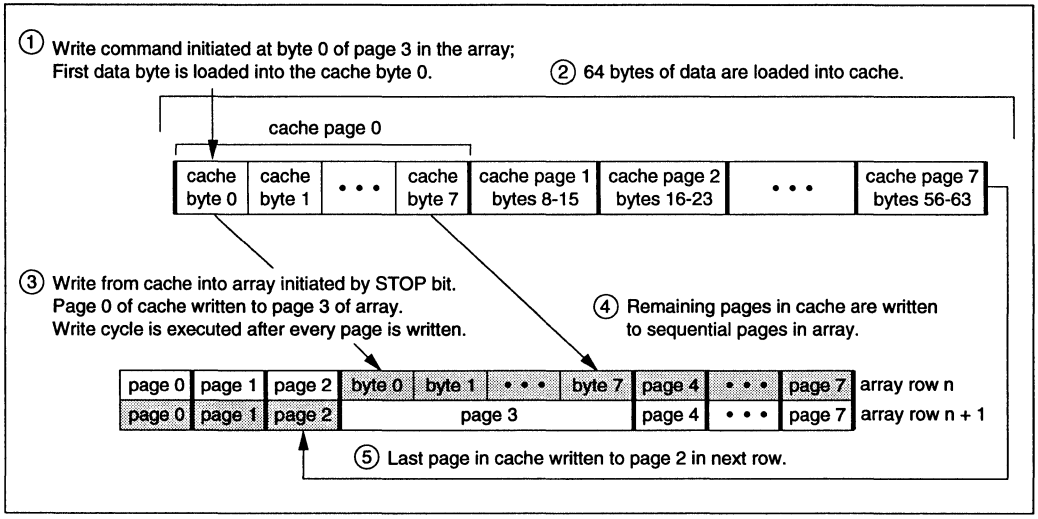
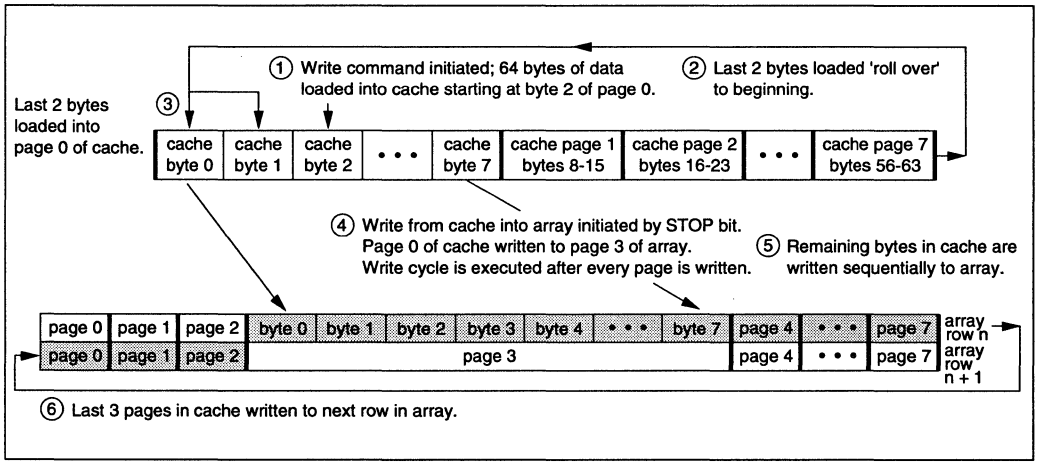


FIGURE 13 - CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



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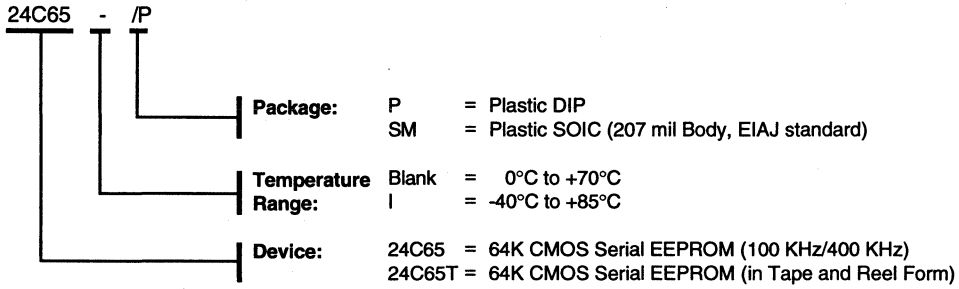
SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



MICROCHIP

24LC65

64K 2.5V CMOS Smart Serial™ EEPROM

FEATURES

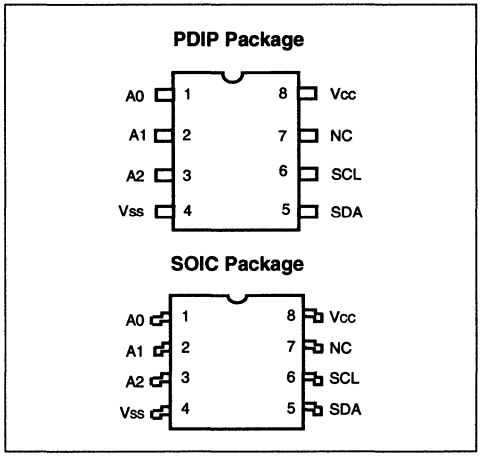
- Voltage operating range: 2.5V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150 µA at 6.0V
  - Standby current 5 µA typical
- Industry standard two wire bus protocol I²C™ compatible
  - Including 100 KHz (2.5V) and 400 KHz (5V) Modes
- Programmable block security options
- Programmable endurance options
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- Self-timed ERASE (E) and WRITE (W) cycles
- Power on/off data protection circuitry
- Endurance: 1 million E/W for a 4K block (typical)
  10,000 E/W for a 60K block (typical)
- 8 byte page, or byte modes available
- 1 page x 8 line input cache for fast write loads
- Electrostatic discharge protection > 4000V
- Data retention > 40 years
- 8-pin PDIP/SOIC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
- 2 ms typical write cycle time, byte or page
- Up to 8 devices may be connected to the same bus for up to 512K bits total memory

DESCRIPTION

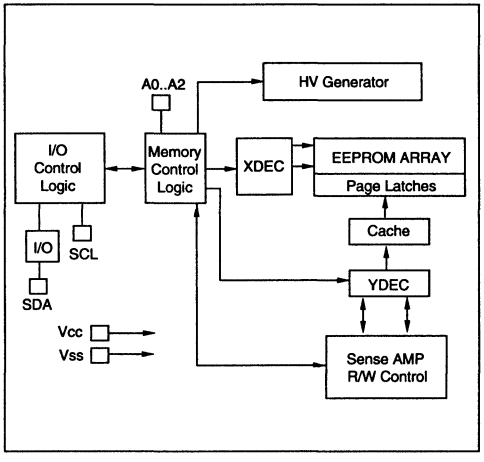
The Microchip Technology Inc. 24LC65 is a "smart" 8K x 8 Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. The 24LC65 offers a relocatable 4K bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 10,000 ERASE/WRITE (E/W) cycles typical. The 24LC65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to fifteen 4K blocks. Functional address lines allow the connection of up to eight 24LC65's on the same bus for up to 512K bits contiguous EEPROM memory. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24LC65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

5

PIN CONFIGURATIONS



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation
Smart Serial is a trademark of Microchip Technology Inc.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature ..... -65°C to+150°C
Ambient temp. with power applied .... -65°C to +125°C
Soldering temperature of leads (10 seconds) . +300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0..A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+2.5V to 6.0V Power Supply
NC	**No Internal Connection**

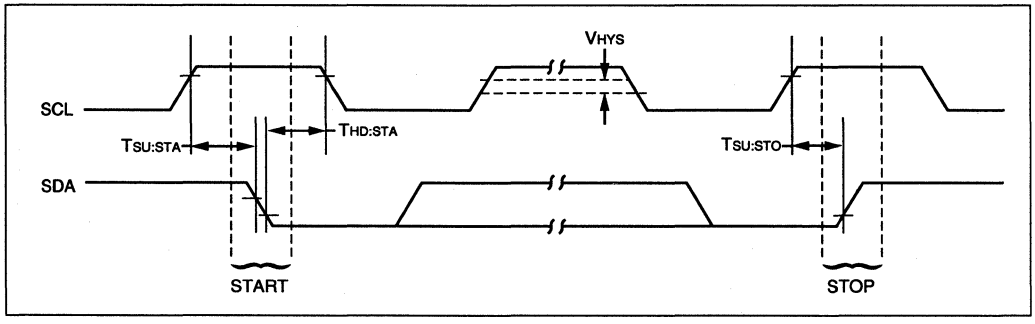
DC CHARACTERISTICS

VCC = +2.5V to 6.0V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min.	Max.	Units	Conditions
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC Write	—	3	mA	VCC = 6.0V, SCL = 400 KHz
	ICC Read	—	150	µA	VCC = 6.0V, SCL = 400 KHz
Standby current	ICCS	—	50	µA	VCC = 6.0V, SCL = SDA = VCC

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1 - BUS TIMING START/STOP



AC CHARACTERISTICS		Vcc = 2.5V-6.0V STD. MODE		Vcc = 4.5V-6.0V FAST MODE			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**	**Remarks**
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 1
SDA and SCL fall time	TF	—	300	—	300	ns	Note 1
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 2
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 1, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	5	—	5	ms/page	Note 4

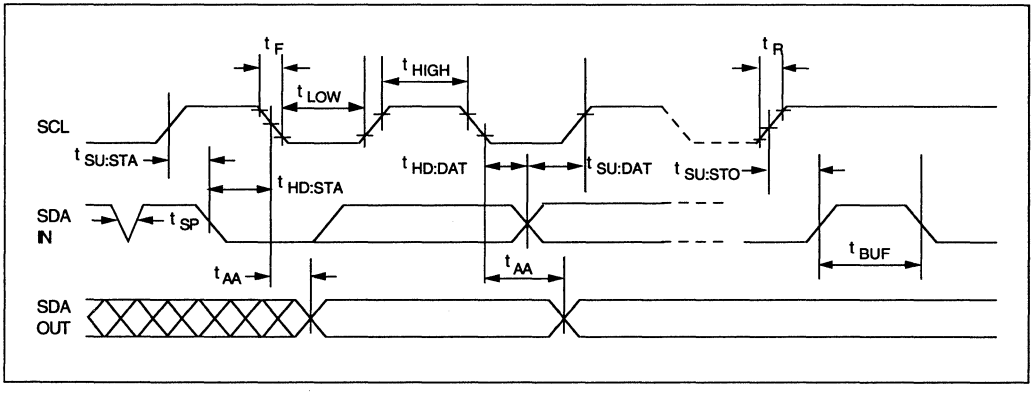
Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.

Note 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

Note 4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

FIGURE 2 - BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24LC65 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC65 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3).

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

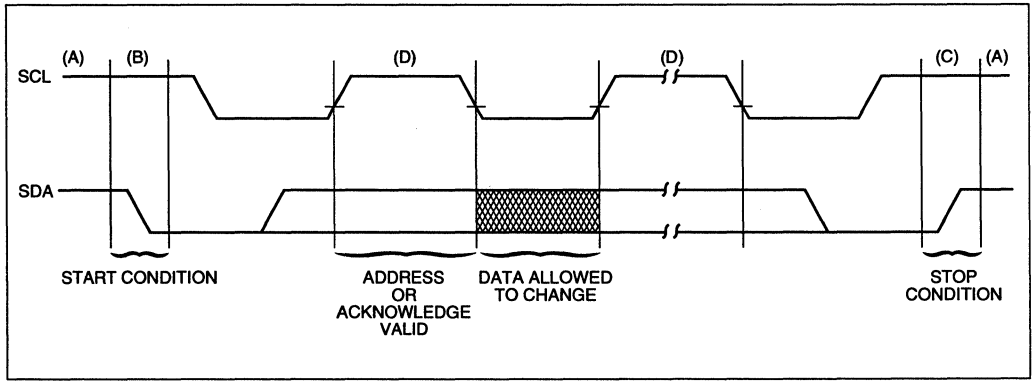
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC65 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC65) must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



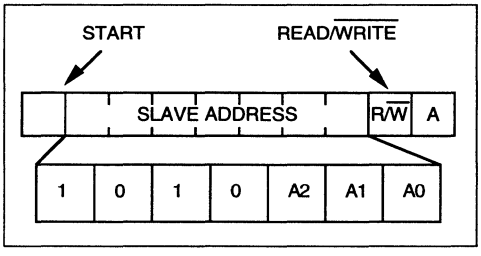
BUS CHARACTERISTICS

Device Addressing and Operation (Figure 4)

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24LC65 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (see Figure 5). Because only A12..A0 are used, the upper three address bits must be zeros. The most significant bit of the most significant byte is transferred first. Following the start condition, the 24LC65 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device (24LC65) outputs an acknowledge signal on the SDA line. Depending upon the state of the R/$\overline{W}$ bit, the 24LC65 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 4 - CONTROL BYTE ALLOCATION



WRITE OPERATION

Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver (24LC65) that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24LC65. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24LC65 the master device will transmit the data word to be written into the addressed memory location. The 24LC65 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC65 will not generate acknowledge signals (see Figure 5).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC65 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24LC65. They will be written from the cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once the stop condition is received an internal write cycle will begin. The 64 byte cache will continue to capture data until a stop condition occurs or the operation is aborted (see Figure 6).

FIGURE 5 - BYTE WRITE

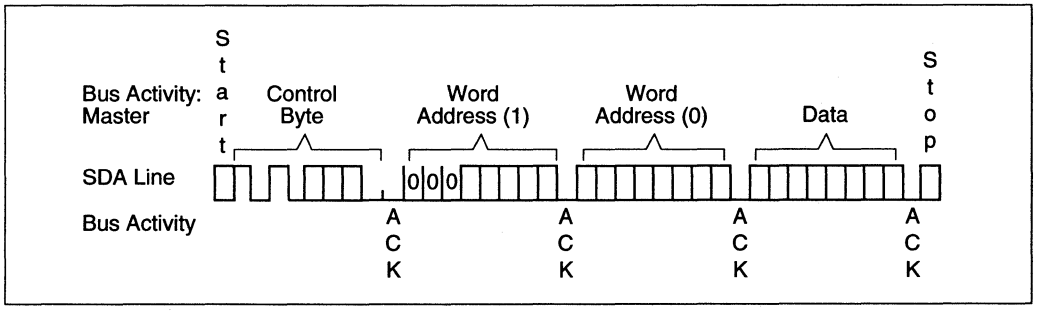


FIGURE 6 - PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 12)

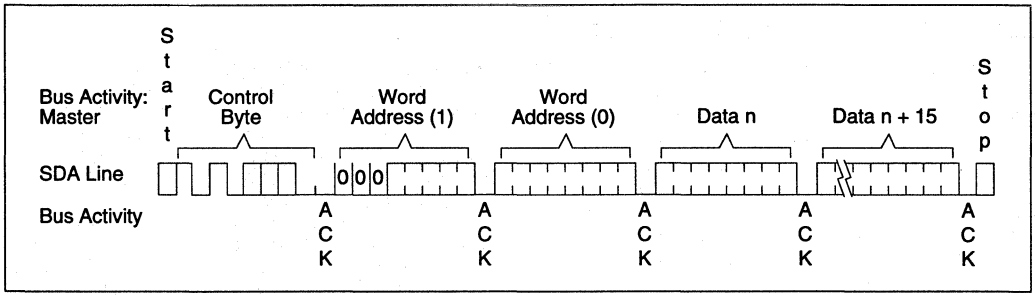


FIGURE 7 - CURRENT ADDRESS READ

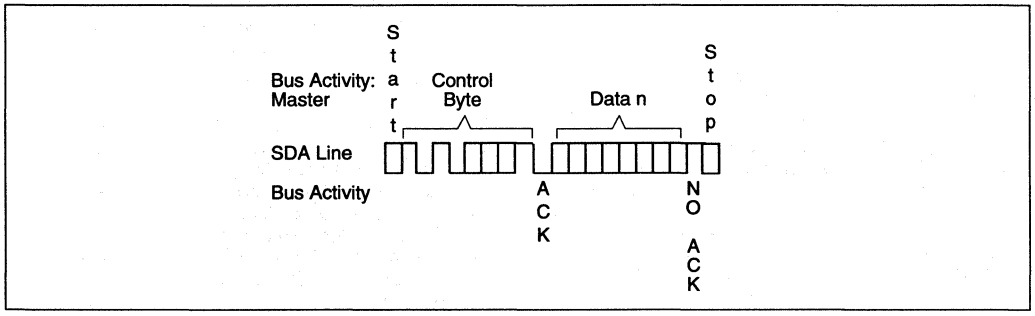


FIGURE 8 - RANDOM READ

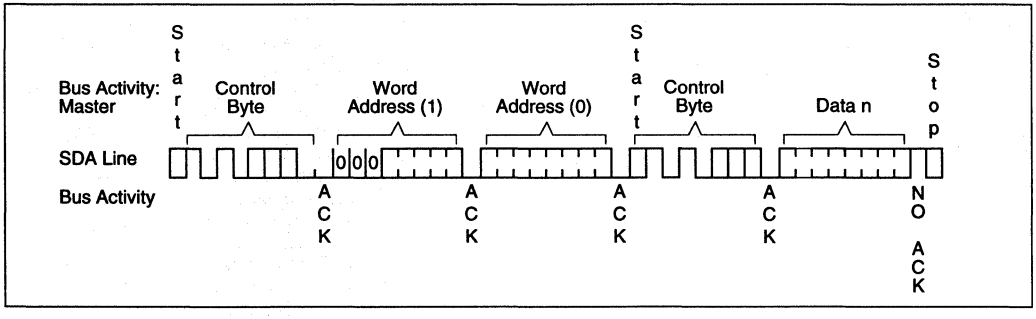
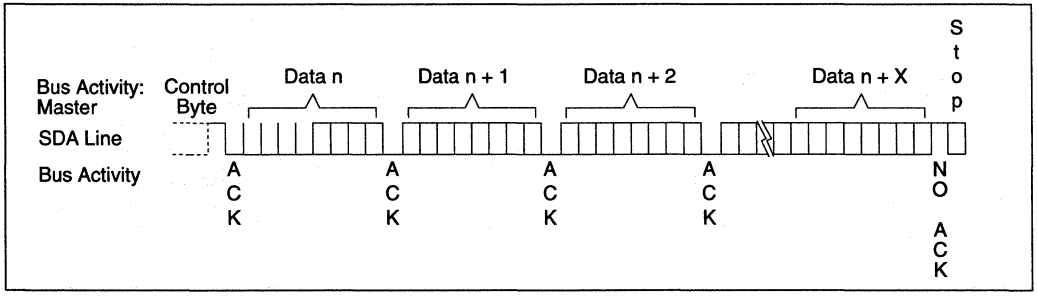


FIGURE 9 - SEQUENTIAL READ



READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24LC65 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC65 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC65 discontinues transmission (see Figure 7).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC65 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC65 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24LC65 to discontinue transmission (see Figure 8).

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC65 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24LC65 to transmit the next sequentially addressed 8 bit word (see Figure 9). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24LC65 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24LC65's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15.

Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 KHz (Fast Mode) compatibility.

High Endurance Block

The location of the high-endurance block within the memory map is programmed by setting the leading bit 7 (S/$\overline{HE}$) of the configuration byte to 0. The upper bits of the address loaded in this command will determine which 4K block within the memory map will be set to high endurance. This block will be capable of one million erase/write cycles typical (see Figure 11).

Note: The High Endurance Block cannot be changed after the security option has been set. If the H.E. block is not programmed by the user, the default location is the highest block of memory.

Security Options

The 24LC65 has a sophisticated mechanism for write-protecting portions of the array. This write protect function is programmable and allows the user to protect 0-15 contiguous 4K blocks. The user sets the security option by sending to the device the starting block number for the protected region and the number of blocks to be protected. If the security option is invoked with 0 blocks protected, then all portions of the array will be unprotected. All parts will come from the factory in the default configuration with the starting block number set to 15 and the number of protected blocks set to zero. THE SECURITY OPTION CAN BE SET ONLY ONCE.

To invoke the security option, a write command is sent to the device with the leading bit (bit 7) of the first address byte set to a 1 (see Figure 11). Bits 1-4 of the first address byte define the starting block number for the protected region. For example, if the starting block number is to be set to 5, the first address byte would be 1XX0101X. Bits 0, 5 and 6 of the first address byte are disregarded by the device and can be either high or low. The device will acknowledge after the first address byte. A byte of don't care bits is then sent by the master, with the device acknowledging afterwards. The third byte sent to the device has bit 7 (S/HE) set high and bit 6 (R) set low. Bits 4 and 5 are don't cares and bits 0-3 define the number of blocks to be write protected. For example, if three blocks are to be protected, the third byte would be 10XX0011. After the third byte is sent to the device, it will acknowledge and a STOP bit is then sent by the master to complete the command.

5

During a normal write sequence, if an attempt is made to write to a protected address, no data will be written and the device will not report an error or abort the command. If a write command is attempted across a secure boundary, unprotected addresses will be written and protected addresses will not.

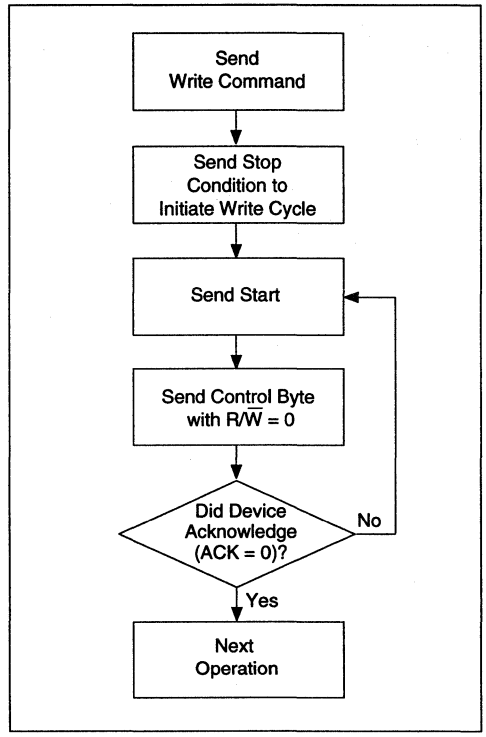
Security Configuration Read

The status of the secure portion of memory can be read by using the same technique as programming this option except the READ bit (bit 6) of the configuration byte is set to a one. After the configuration byte is sent, the device will acknowledge and then send two bytes of data to the master just as in a normal read sequence. The master must acknowledge the first byte and not acknowledge the second, and then send a stop bit to end the sequence. The upper four bits of both of these bytes will always be read as '1's. The lower four bits of the first byte contains the starting secure block. The lower four bits of the second byte contains the number of secure blocks. The default starting secure block is fifteen and the default number of secure blocks is zero (see Figure 11).

ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 10 for flow diagram.

FIGURE 10 - ACKNOWLEDGE POLLING FLOW



PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 10 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten.

Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (see Figure 12) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 13, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

Power Management

The design incorporates a power standby mode when not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates V_{DD} monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The V_{DD} monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

5

PIN DESCRIPTIONS

A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24LC65 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (see Figures 4 and 11).

SDA Serial Address/Data Input/Output

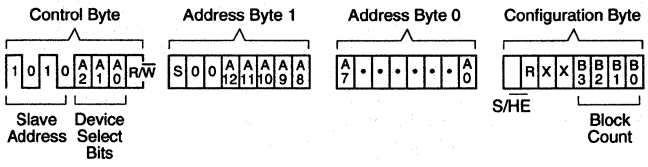
This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to V_{CC} (typical 10KΩ for 100 KHz, 1KΩ for 400 KHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

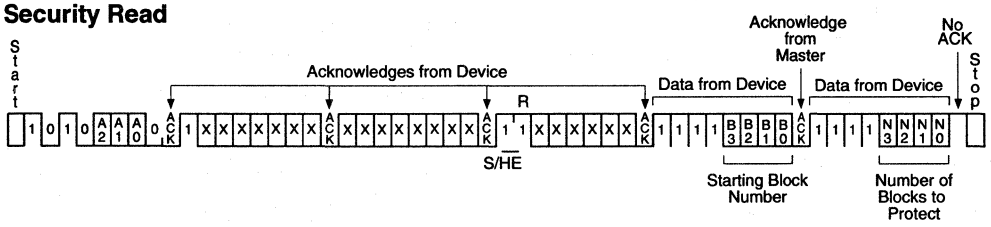
SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

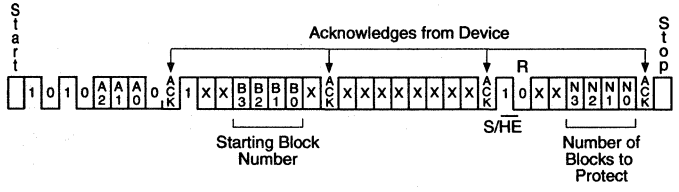
FIGURE 11 - CONTROL SEQUENCE BIT ASSIGNMENTS



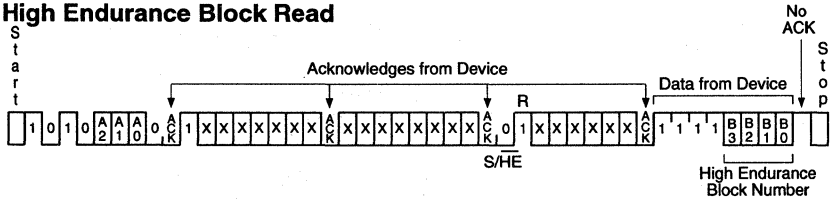
Security Read



Security Write



High Endurance Block Read



High Endurance Block Write

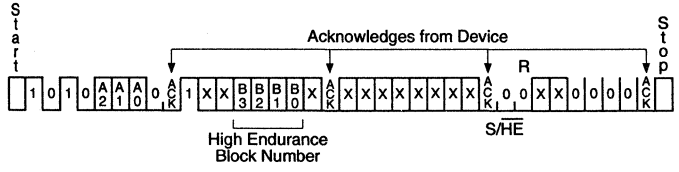


FIGURE 12 - CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

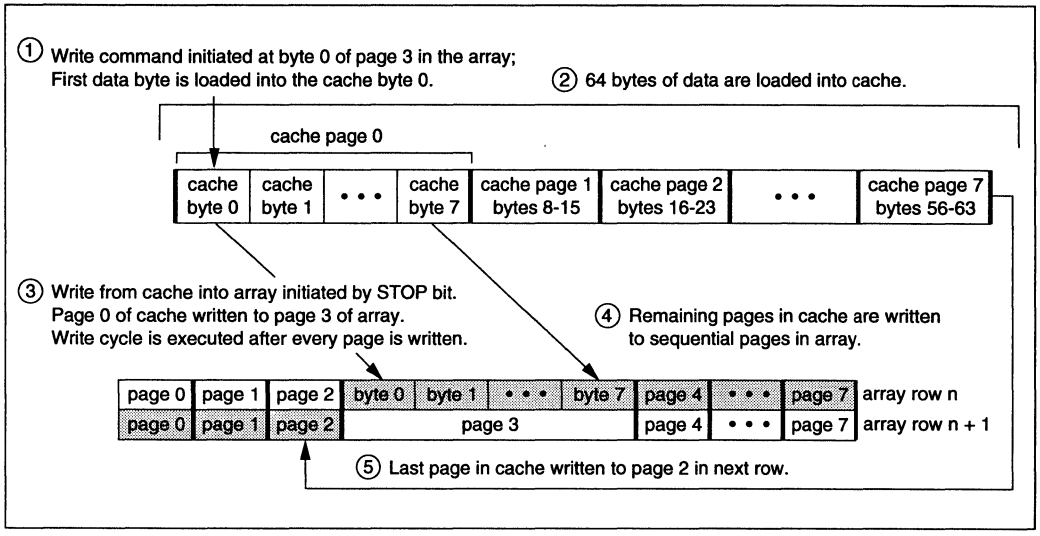
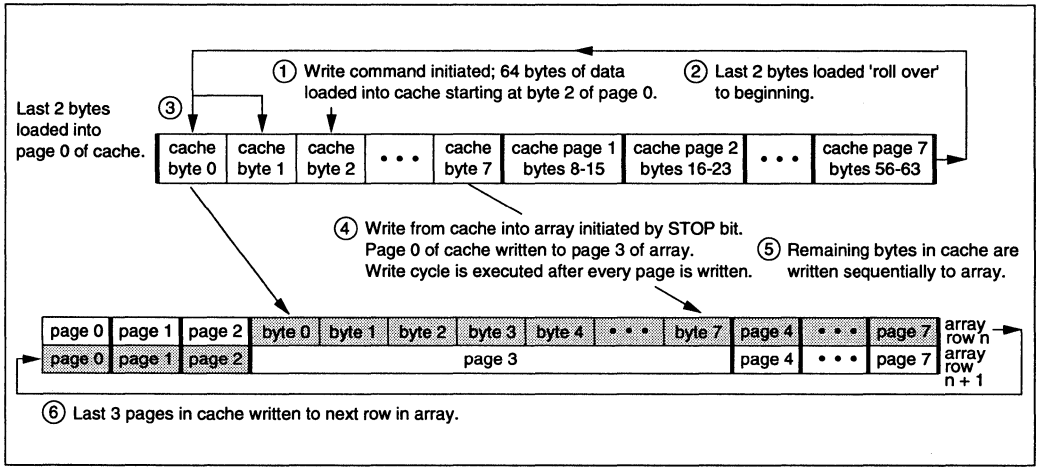


FIGURE 13 - CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

24LC65 - /P

Package:	P	=	Plastic DIP
	SM	=	Plastic SOIC (207 mil Body, EIAJ standard)
Temperature Range:	Blank	=	0°C to +70°C
	I	=	-40°C to +85°C
Device:	24LC65	=	64K CMOS Serial EEPROM (100 KHz/400 KHz)
	24LC65T	=	64K CMOS Serial EEPROM (in Tape and Reel Form)

MICROCHIP

24AA65

64K 1.8V CMOS Smart Serial™ EEPROM

FEATURES

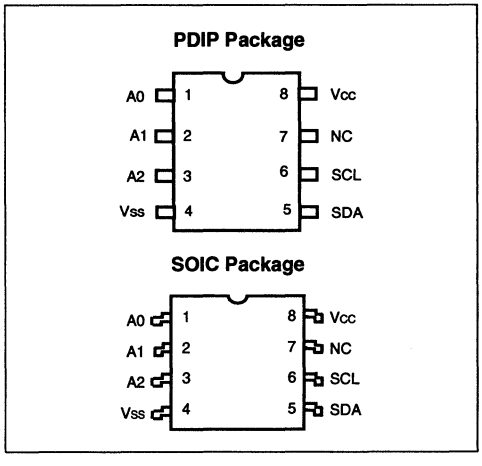
- Voltage operating range: 1.8V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150 µA at 6.0V
  - Standby current 5 µA typical
- Industry standard two wire bus protocol I²C™ compatible
  - Including 100 KHz (1.8V) and 400 KHz (5V) Modes
- Programmable block security options
- Programmable endurance options
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- Self-timed ERASE (E) and WRITE (W) cycles
- Power on/off data protection circuitry
- Endurance: 1 million E/W for a 4K block (typical)
  10,000 E/W for a 60K block (typical)
- 8 byte page, or byte modes available
- 1 page x 8 line input cache for fast write loads
- Electrostatic discharge protection > 4000V
- Data retention > 40 years
- 8-pin PDIP/SOIC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C
- 2 ms typical write cycle time, byte or page
- Up to 8 devices may be connected to the same bus for up to 512K bits total memory

DESCRIPTION

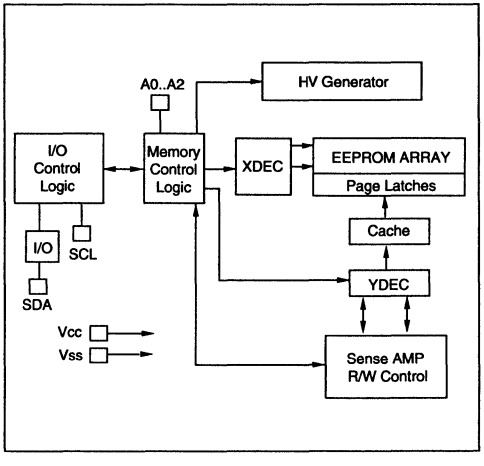
The Microchip Technology Inc. 24AA65 is a "smart" 8K x 8 Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. It is capable of operation down to 1.8V, the end-of-life voltage for 2 "AA" battery cells for most popular battery technologies. The 24AA65 offers a relocatable 4K bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 10,000 ERASE/WRITE (E/W) cycles typical. The 24AA65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to fifteen 4K blocks. Functional address lines allow the connection of up to eight 24LC65's on the same bus for up to 512K bits contiguous EEPROM memory. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24AA65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

5

PIN CONFIGURATIONS



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation
Smart Serial is a trademark of Microchip Technology Inc.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature ..... -65°C to+150°C
Ambient temp. with power applied .... -65°C to +125°C
Soldering temperature of leads (10 seconds) . +300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0..A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+1.8V to 6.0V Power Supply
NC	**No Internal Connection**

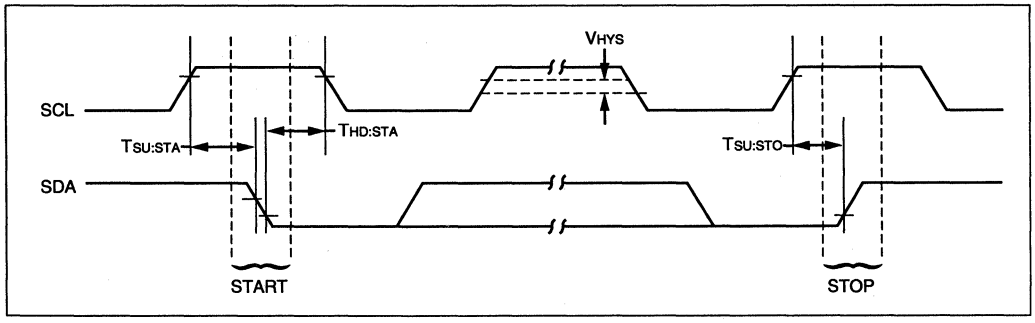
DC CHARACTERISTICS

VCC = +1.8V to 6.0V
Commercial (C): Tamb = 0°C to +70°C

Parameter	Symbol	Min.	Max.	Units	Conditions
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC Write	—	3	mA	VCC = 6.0V, SCL = 400 KHz
	ICC Read	—	150	µA	VCC = 6.0V, SCL = 400 KHz
Standby current		—	50	µA	VCC = 6.0V, SCL = SDA = VCC

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1 - BUS TIMING START/STOP



AC CHARACTERISTICS		Vcc = 1.8V-6.0V STD. MODE		Vcc = 4.5V-6.0V FAST MODE			
Parameter	Symbol	Min	Max	Min	Max	Units	Remarks
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 1
SDA and SCL fall time	TF	—	300	—	300	ns	Note 1
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 2
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 1, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	5	—	5	ms/page	Note 4

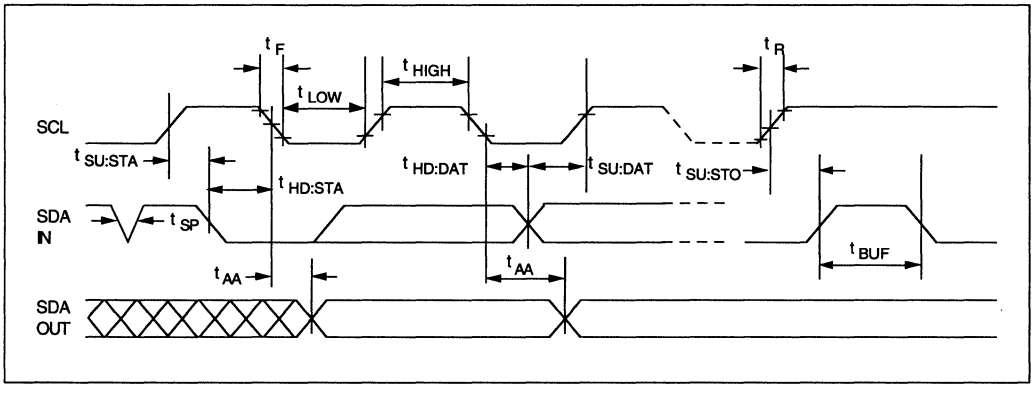
Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.

Note 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

Note 4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

FIGURE 2 - BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24AA65 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA65 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3).

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

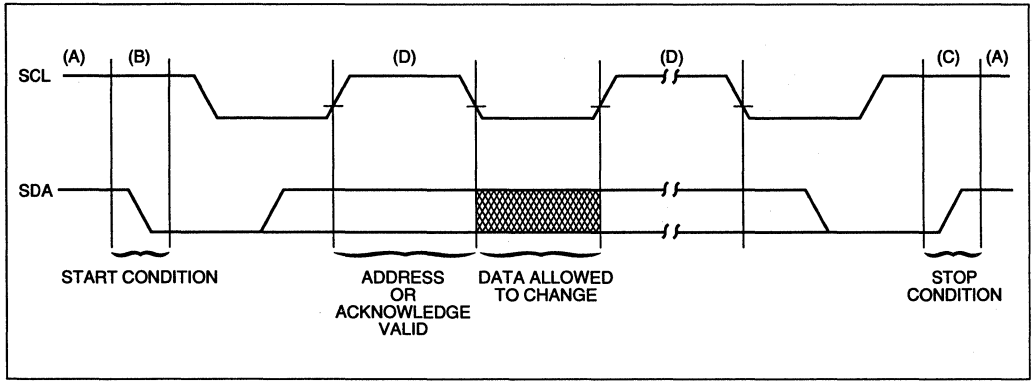
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA65 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24AA65) must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



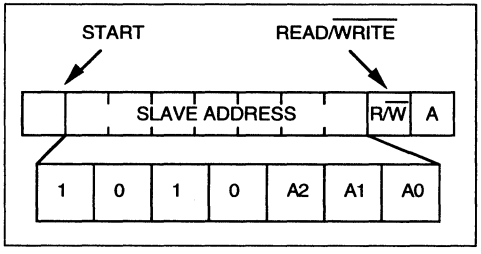
BUS CHARACTERISTICS

Device Addressing and Operation (Figure 4)

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24AA65 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (see Figure 5). Because only A12..A0 are used, the upper three address bits must be zeros. The most significant bit of the most significant byte is transferred first. Following the start condition, the 24AA65 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device (24AA65) outputs an acknowledge signal on the SDA line. Depending upon the state of the R/$\overline{W}$ bit, the 24AA65 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 4 - CONTROL BYTE ALLOCATION



WRITE OPERATION

Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver (24AA65) that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24AA65. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24AA65 the master device will transmit the data word to be written into the addressed memory location. The 24AA65 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA65 will not generate acknowledge signals (see Figure 5).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA65 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24AA65. They will be written from the cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once the stop condition is received an internal write cycle will begin. The 64 byte cache will continue to capture data until a stop condition occurs or the operation is aborted (see Figure 6).

FIGURE 5 - BYTE WRITE

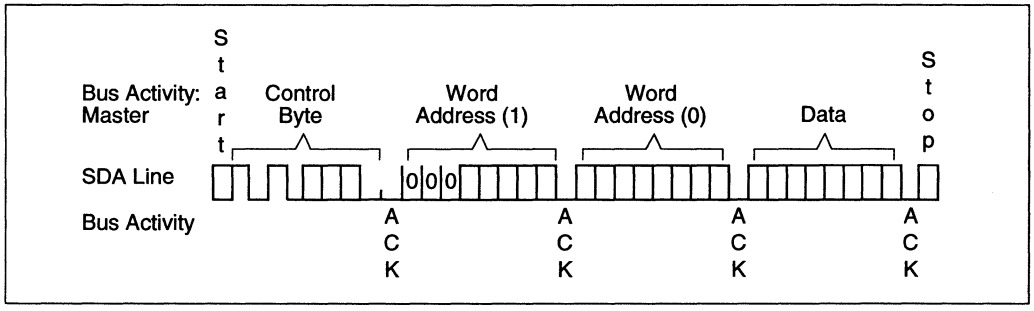


FIGURE 6 - PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 12)

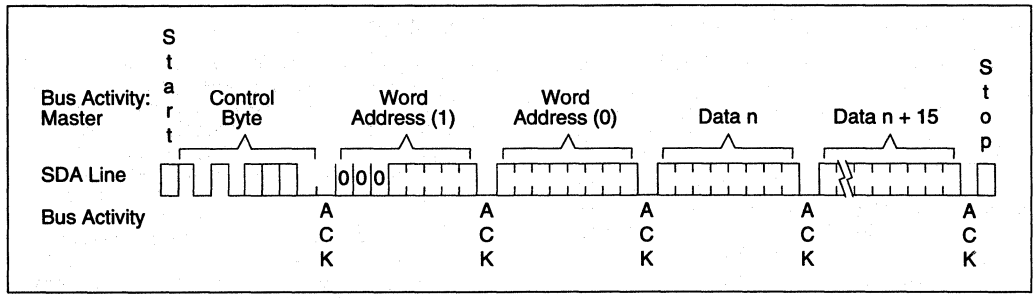


FIGURE 7 - CURRENT ADDRESS READ

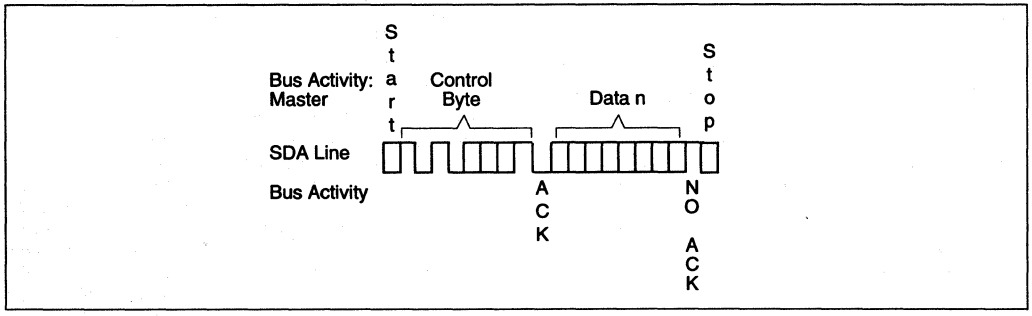


FIGURE 8 - RANDOM READ

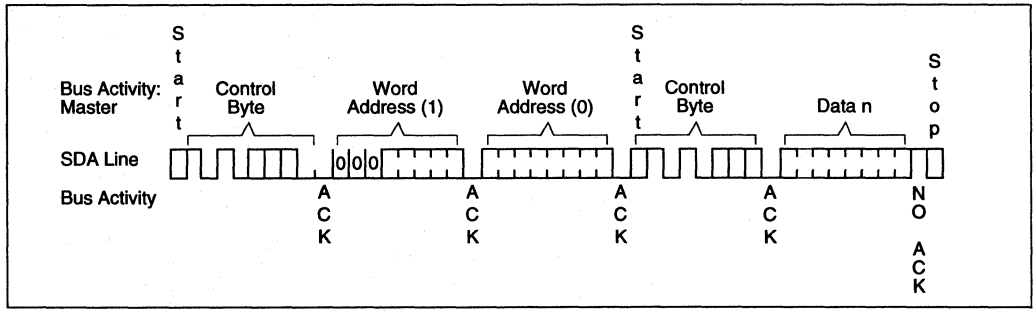
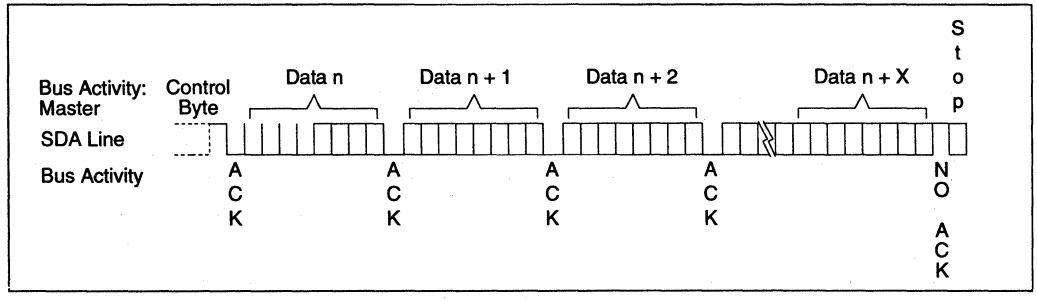


FIGURE 9 - SEQUENTIAL READ



READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24AA65 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA65 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA65 discontinues transmission (see Figure 7).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA65 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA65 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24AA65 to discontinue transmission (see Figure 8).

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA65 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24AA65 to transmit the next sequentially addressed 8 bit word (see Figure 9). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24AA65 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24LC65's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15.

Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 KHz (Fast Mode) compatibility.

High Endurance Block

The location of the high-endurance block within the memory map is programmed by setting the leading bit 7 (S/$\overline{HE}$) of the configuration byte to 0. The upper bits of the address loaded in this command will determine which 4K block within the memory map will be set to high endurance. This block will be capable of one million erase/write cycles typical (see Figure 11).

Note: The High Endurance Block cannot be changed after the security option has been set. If the H.E. block is not programmed by the user, the default location is the highest block of memory.

Security Options

The 24AA65 has a sophisticated mechanism for write-protecting portions of the array. This write protect function is programmable and allows the user to protect 0-15 contiguous 4K blocks. The user sets the security option by sending to the device the starting block number for the protected region and the number of blocks to be protected. If the security option is invoked with 0 blocks protected, then all portions of the array will be unprotected. All parts will come from the factory in the default configuration with the starting block number set to 15 and the number of protected blocks set to zero. THE SECURITY OPTION CAN BE SET ONLY ONCE.

To invoke the security option, a write command is sent to the device with the leading bit (bit 7) of the first address byte set to a 1 (see Figure 11). Bits 1-4 of the first address byte define the starting block number for the protected region. For example, if the starting block number is to be set to 5, the first address byte would be 1XX0101X. Bits 0, 5 and 6 of the first address byte are disregarded by the device and can be either high or low. The device will acknowledge after the first address byte. A byte of don't care bits is then sent by the master, with the device acknowledging afterwards. The third byte sent to the device has bit 7 (S/HE) set high and bit 6 (R) set low. Bits 4 and 5 are don't cares and bits 0-3 define the number of blocks to be write protected. For example, if three blocks are to be protected, the third byte would be 10XX0011. After the third byte is sent to the device, it will acknowledge and a STOP bit is then sent by the master to complete the command.

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During a normal write sequence, if an attempt is made to write to a protected address, no data will be written and the device will not report an error or abort the command. If a write command is attempted across a secure boundary, unprotected addresses will be written and protected addresses will not.

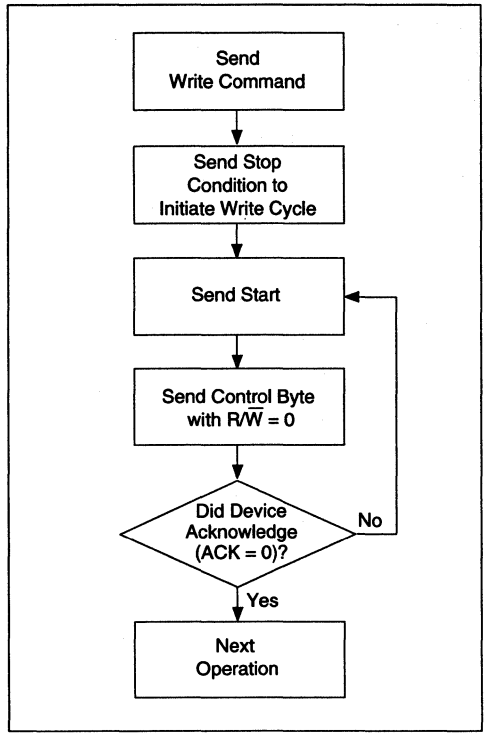
Security Configuration Read

The status of the secure portion of memory can be read by using the same technique as programming this option except the READ bit (bit 6) of the configuration byte is set to a one. After the configuration byte is sent, the device will acknowledge and then send two bytes of data to the master just as in a normal read sequence. The master must acknowledge the first byte and not acknowledge the second, and then send a stop bit to end the sequence. The upper four bits of both of these bytes will always be read as '1's. The lower four bits of the first byte contains the starting secure block. The lower four bits of the second byte contains the number of secure blocks. The default starting secure block is fifteen and the default number of secure blocks is zero (see Figure 11).

ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 10 for flow diagram.

FIGURE 10 - ACKNOWLEDGE POLLING FLOW



PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 10 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten.

Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (see Figure 12) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 13, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

Power Management

The design incorporates a power standby mode when not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

PIN DESCRIPTIONS

A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24AA65 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (see Figures 4 and 11).

SDA Serial Address/Data Input/Output

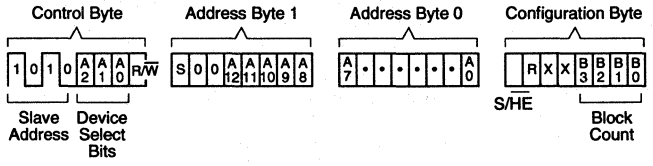
This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 KHz, 1KΩ for 400 KHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

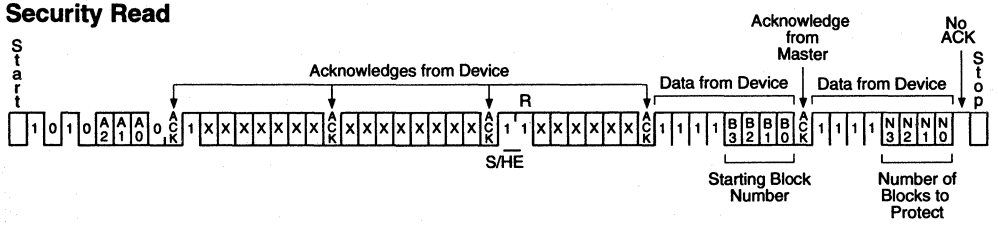
SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

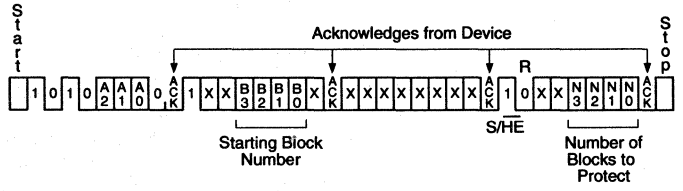
FIGURE 11 - CONTROL SEQUENCE BIT ASSIGNMENTS



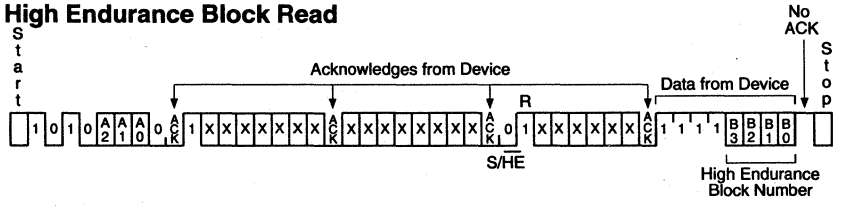
Security Read



Security Write



High Endurance Block Read



High Endurance Block Write

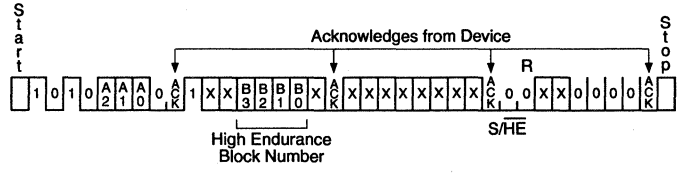


FIGURE 12 - CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

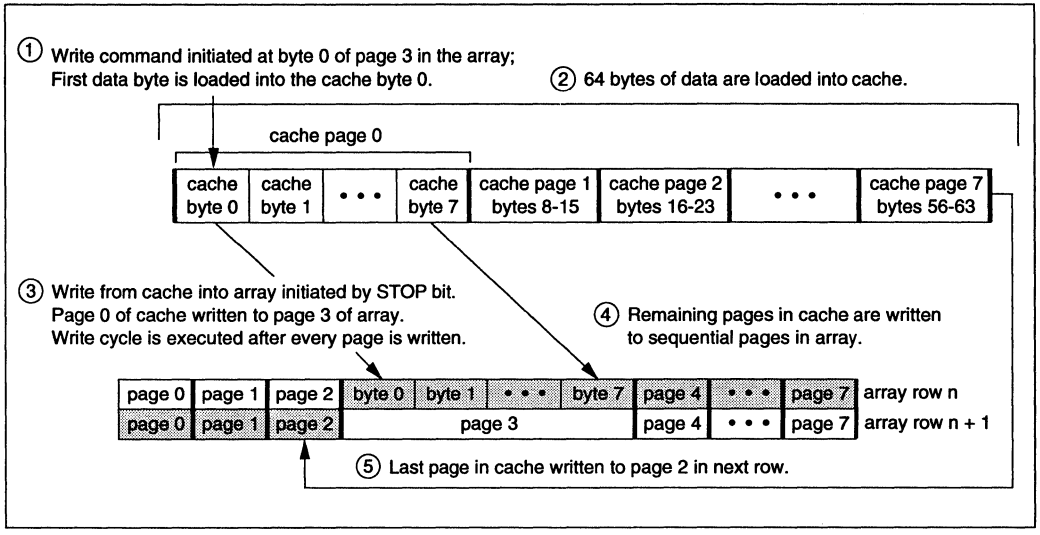


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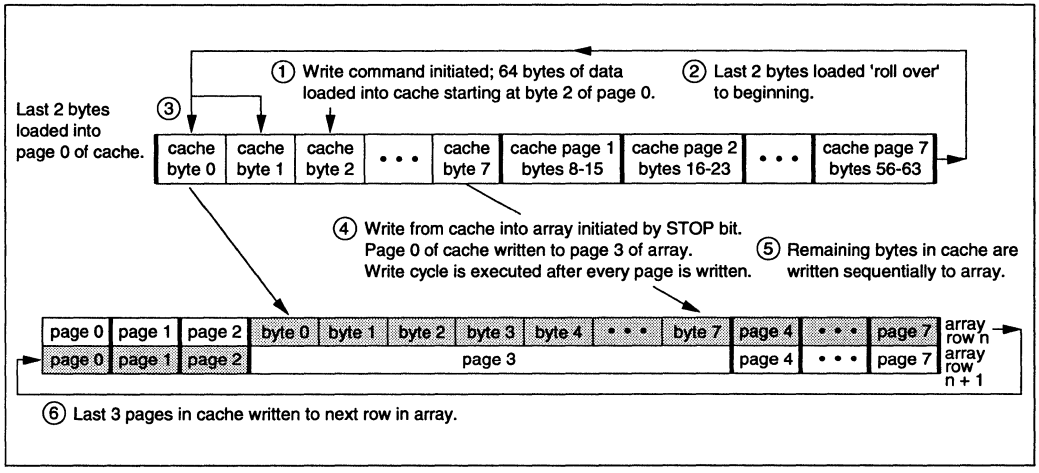
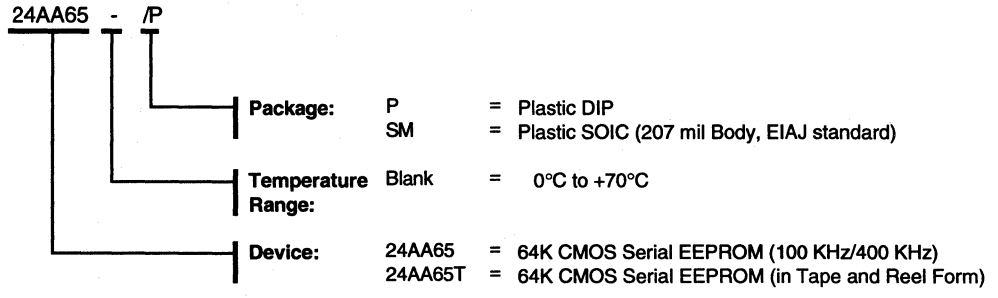
FIGURE 13 - CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



MICROCHIP

59C11

1K 5V CMOS Serial EEPROM

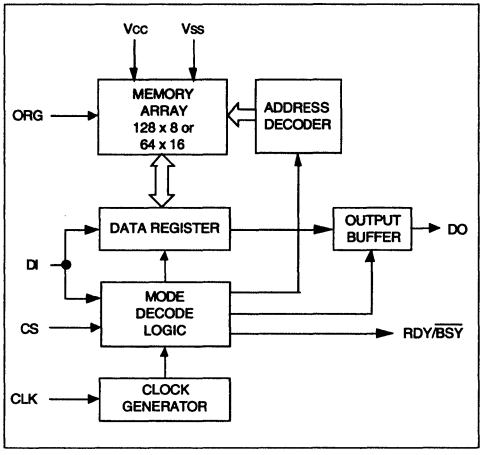
FEATURES

- Low power CMOS technology
- Pin selectable memory organization
  - 128 x 8 or 64 x 16 bit organization
- Single 5 volt only operation
- Self timed WRITE, ERAL and WRAL cycles
- Automatic erase before WRITE
- RDY/$\overline{BSY}$ status information during WRITE
- Power on/off data protection circuitry
- 1,000,000 ERASE/WRITE cycles typical
- Data Retention > 40 Years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

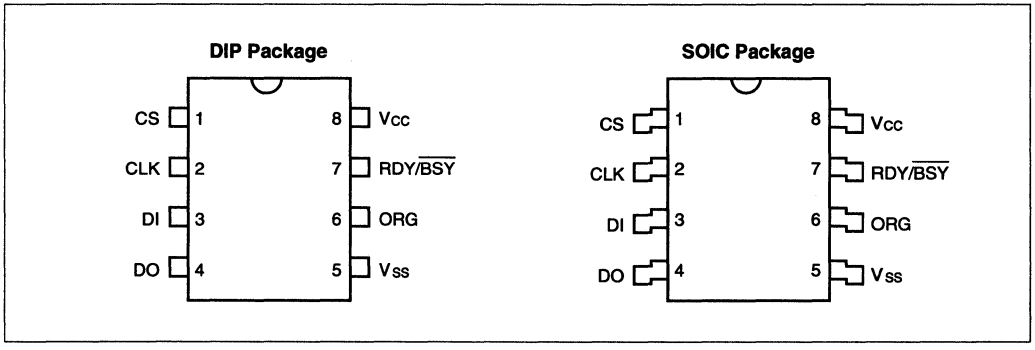
DESCRIPTION

The Microchip Technology Inc. 59C11 is a 1K bit Electrically Erasable PROM. The device is configured as 128 x 8 or 64 x 16, selectable externally by means of the control pin ORG. Advanced CMOS technology makes this device ideal for low power nonvolatile memory applications. The 59C11 is available in the standard 8-pin DIP and a surface mount SOIC package.

BLOCK DIAGRAM



PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temperature with
power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ... +300°C
ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
VSS	Ground
ORG	Memory Array Organization
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Status
VCC	+5V Power Supply

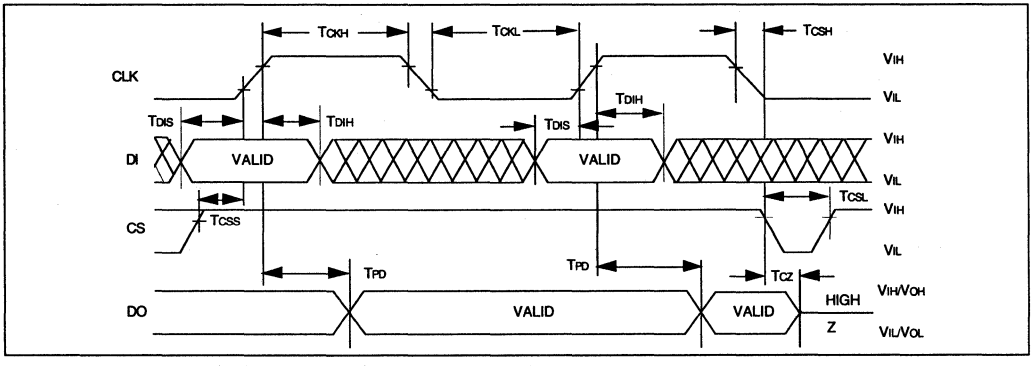
DC CHARACTERISTICS

VCC = +5V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = –40°C to +85°C
Automotive: Tamb = –40°C to +125°C (Note 3)

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	VCC + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4	—	V	IOH = -400 µA
Low level output voltage	VOL	—	0.4	V	IOL = 3.2 mA
Input leakage current	ILI	—	10	µA	VIN = 0V to VCC (Note 1)
Output leakage current	ILO	—	10	µA	VOUT = 0V to VCC (Note 1)
Internal capacitance (all inputs/outputs)	CINT	—	7	pF	VIN/VOUT = 0V (Note 2) Tamb = 25°C, f = 1 MHz
Operating current (all modes)	ICC write	—	4	mA	FCLK = 1 MHz, VCC =5.5V
Standby current	ICCS	—	100	µA	CS = 0V, VCC = 5.5V

Note 1: Internal resister pull-up at Pin 6. Active output at Pin 7.
Note 2: This parameter is periodically sampled and not 100% tested.
Note 3: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

SYNCHRONOUS DATA TIMING



AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500	—	ns	
Clock low time	TCKL	500	—	ns	
Chip select setup time	TCSS	50	—	ns	
Chip select hold time	TCSH	0	—	ns	
Chip select low time	TCS	100	—	ns	
Data input setup time	TDIS	100	—	ns	
Data input hold time	TDIH	100	—	ns	
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time (from CS = low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
RDY/$\overline{\text{BSY}}$ delay time	TRBD	—	400	ns	
Program cycle time (Auto Erase and Write)	TWC	—	1 15	ms ms	for 8-bit mode for ERAL and WRAL in 8/16-bit modes

5

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a WRITE cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a WRITE cycle, the device will go into standby mode as soon as the WRITE cycle is completed.

CS must be LOW for 100 ns (TCSL) minimum between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 59C11. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock high time (TCKH) and clock low time (TCKL)). This gives freedom in preparing opcode, address and data for the controlling master.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but a START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto erase/write) cycle.

After detection of a START condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). When that limit has been reached, CLK and DI become "Don't Care" inputs until CS is brought LOW for at least chip select low time (TCSL) and brought HIGH again and a WRITE cycle (if any) is completed.

Data In (DI)

Data In is used to clock in START bit, opcode, address and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK). This output is in HIGH–Z mode except if data is clocked out as a result of a READ instruction.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is output after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during WRITE cycles.

Organization (ORG)

This input selects the memory array organization. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization. In applications subject to electrical noise, it is recommended that this pin not be left floating, but tied either high or low.

Ready/Busy (RDY/$\overline{\text{BSY}}$)

Pin 7 provides RDY/$\overline{\text{BSY}}$ status information. RDY/BSY is low if the device is performing a WRITE, ERAL, or WRAL operation. When it is HIGH the internal, self-timed WRITE, ERAL or WRAL operation has been completed and the device is ready to receive a new instruction.

DATA PROTECTION

During power-up, all modes of operation are inhibited until Vcc has reached a level of 2.8 V. During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below 2.8 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, EWEN instruction must be performed before any WRITE, ERAL or WRAL instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

INSTRUCTION SET — 64 X 16 MODE, ORG=1

Instruction	Start Bit	Opcode	Address	Data In	Data Out	Number of Req. CLK Cycles
READ	1	1 0 X X	A5 A4 A3 A2 A1 A0	—	D15 – D0	27
WRITE	1	X 1 X X	A5 A4 A3 A2 A1 A0	D15 – D0	High-Z	27
EWEN	1	0 0 1 1	X X X X X X	—	High-Z	11
EWDS	1	0 0 0 0	X X X X X X	—	High-Z	11
ERAL	1	0 0 1 0	X X X X X X	—	High-Z	11
WRAL	1	0 0 0 1	X X X X X X	D15 – D0	High-Z	27

128 X 8 MODE, ORG=0

Instruction	Start Bit	Opcode	Address	Data In	Data Out	Number of Req. CLK Cycles
READ	1	1 0 X X	A6 A5 A4 A3 A2 A1 A0	—	D7 – D0	20
WRITE	1	X 1 X X	A6 A5 A4 A3 A2 A1 A0	D7 – D0	High-Z	20
EWEN	1	0 0 1 1	X X X X X X X	—	High-Z	12
EWDS	1	0 0 0 0	X X X X X X X	—	High-Z	12
ERAL	1	0 0 1 0	X X X X X X X	—	High-Z	12
WRAL	1	0 0 0 1	X X X X X X X	D7 – D0	High-Z	20

FUNCTIONAL DESCRIPTION

START Condition

The START bit is detected by the device if CS and DI are both High with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition) without resulting in any device operation (READ, WRITE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e. clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

Note: CS must go LOW between consecutive instructions.

DI/DO Pins

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

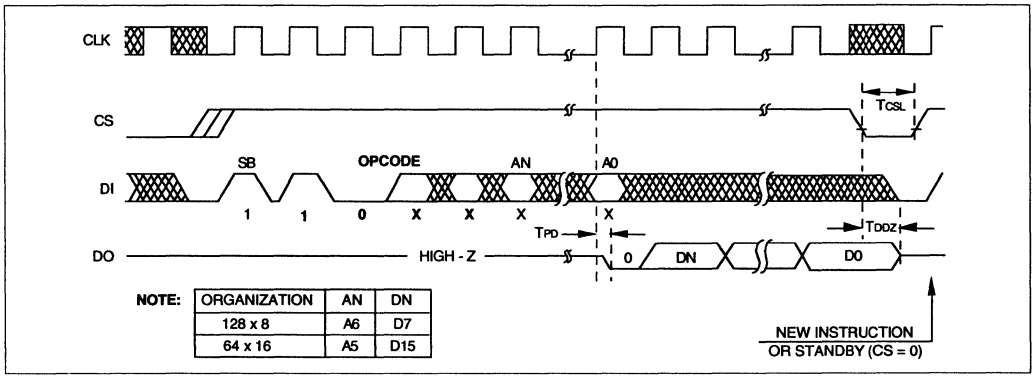
READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 8- or 16-bit output string. The output data changes during the high state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 is a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the negative edge of CS, whichever occurs first. D0 remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

The most significant data bit (D15 or D7) is always output first, followed by the lower significant bits (D14 - D0 or D6 - D0).

READ MODE



NOTE:

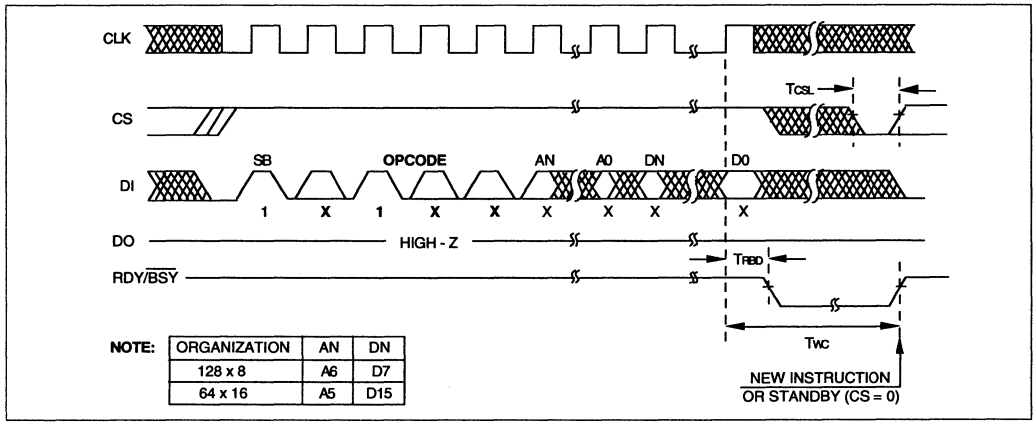
ORGANIZATION	AN	DN
128 x 8	A6	D7
64 x 16	A5	D15

WRITE

The WRITE instruction is followed by 8 or 16 bits of data which are written into the specified address. The most significant data bit (D15 or D7) has to be clocked in first followed by the lower significant data bits (D14 – D0 or D6 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic erase cycle on the specified address before the data are written. The WRITE cycle is completely self timed and commences automatically after the rising edge of the CLK signal for the last data bit (D0).

The WRITE cycle takes 1 ms maximum for 8-bit mode and 2 ms maximum for 16-bit mode.

WRITE MODE



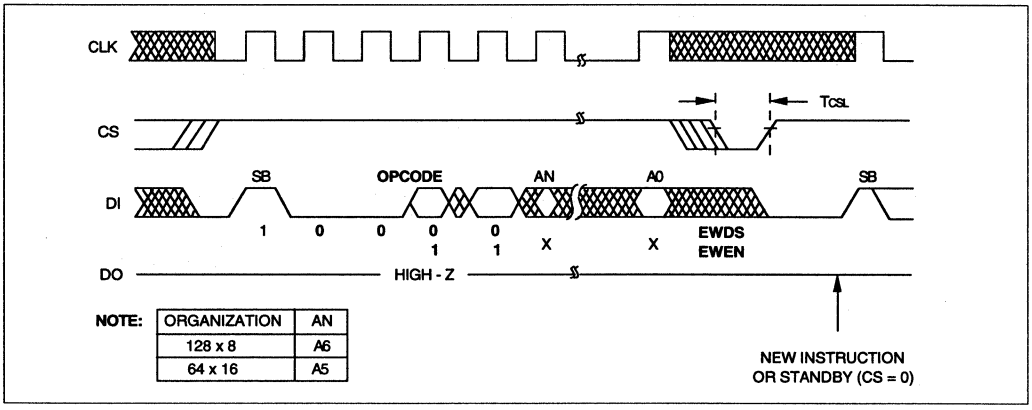
NOTE:

ORGANIZATION	AN	DN
128 x 8	A6	D7
64 x 16	A5	D15

ERASE/WRITE Enable/Disable (EWEN, EWDS)

The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, EWEN instruction has to be performed before any WRITE, ERAL, or WRAL instruction is executed by the device. For added data protection, the device should be put in the ERASE/WRITE Disable mode (EWDS) after programming operations are completed.

ERASE/WRITE ENABLE AND DISABLE



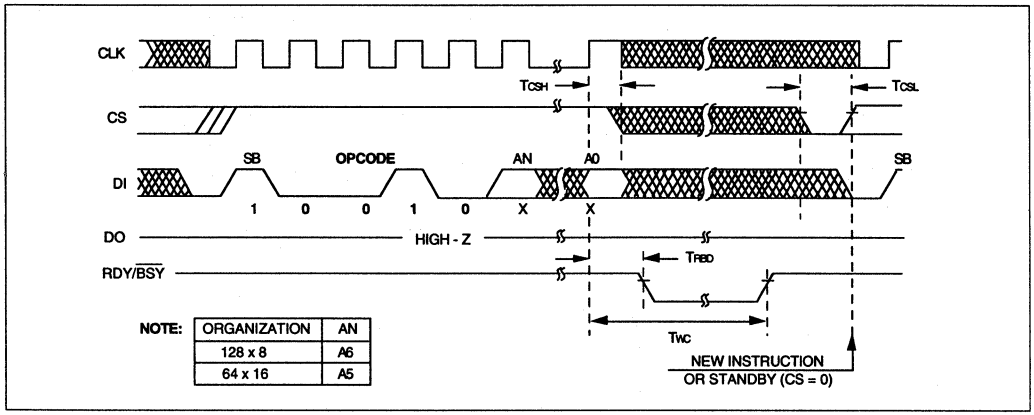
NOTE:

ORGANIZATION	AN
128 x 8	A6
64 x 16	A5

ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the rising edge of the CLK signal for the last dummy address bit. ERAL takes 15 ms maximum.

ERASE ALL (CHIP ERASE)



NOTE:

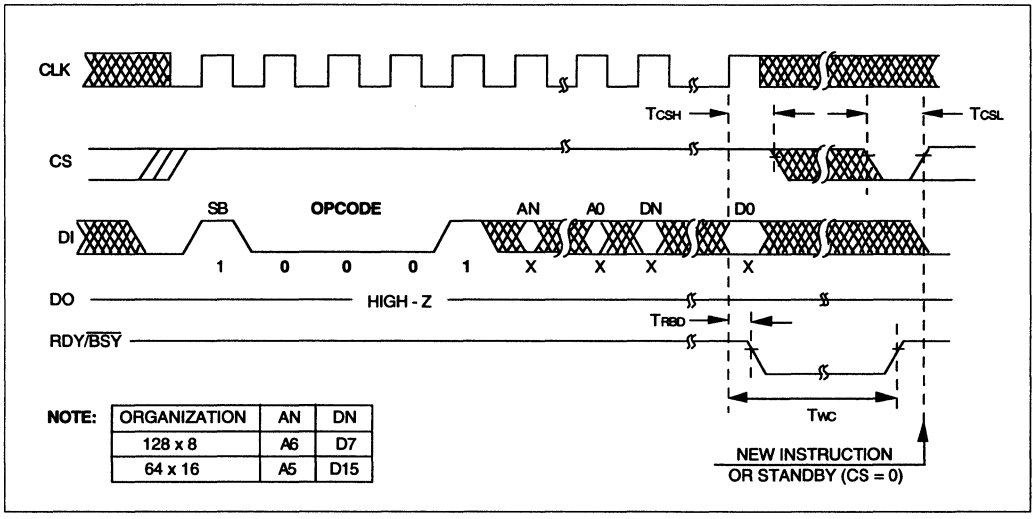
ORGANIZATION	AN
128 x 8	A6
64 x 16	A5

WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the last data bit (D0) has been clocked in. WRAL takes 15 ms maximum.

Note: The WRAL does not include an automatic ERASE cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases. The WRAL instruction is used for testing and/or device initialization.

WRITE ALL



NOTE:

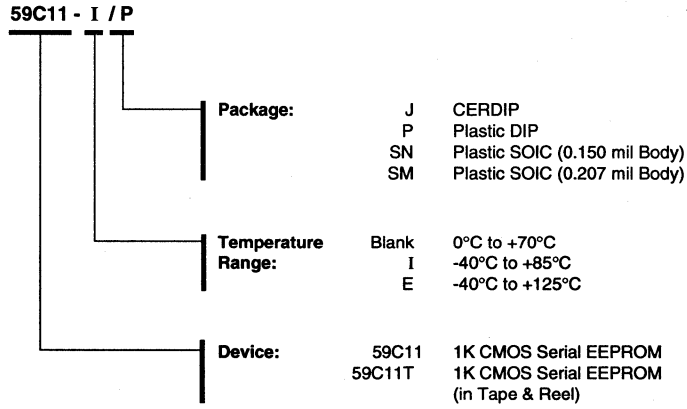
ORGANIZATION	AN	DN
128 x 8	A6	D7
64 x 16	A5	D15

5

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



85C72/82/92

1K/2K/4K 5V CMOS Serial EEPROM

FEATURES

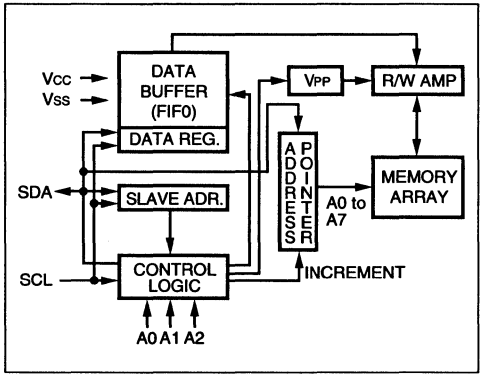
- Low power CMOS technology
- Two wire serial interface bus, I²C™ compatible
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer
- 1ms write cycle time for single byte
- 100,000 erase/write cycles
- Data retention >40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C
  —Automotive: -40°C to +125°C

	85C72	85C82	85C92
Organization	128 x 8	256 x 8	2 x 256 x 8
Page Write Buffer	2 Bytes	2 Bytes	8 Bytes

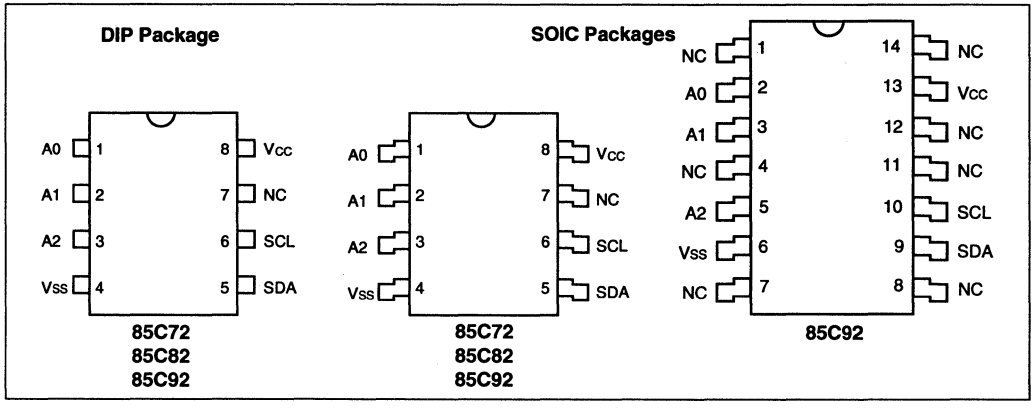
DESCRIPTION

The Microchip Technology Inc. 85C72/82/92 is a 1K/2K/4K bit Electrically Erasable PROM. The device is organized as shown with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. The 85C72/82/92 also has a page-write capability for up to 8 bytes of data (see chart). Up to eight 85C72/82/92s may be connected to the two wire bus. The 85C72/82/92 is available in standard 8-pin DIP and surface mount SOIC packages.

BLOCK DIAGRAM



PIN CONFIGURATIONS



I²C is a trademark of Philips Corporation

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied .... -65°C to +125°C
Soldering temperature of leads (10 seconds) . +300°C
ESD protection on all pins ..... 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data Input/Output
SCL	Serial Clock
NC	No Connect
Vcc	+5V Power Supply

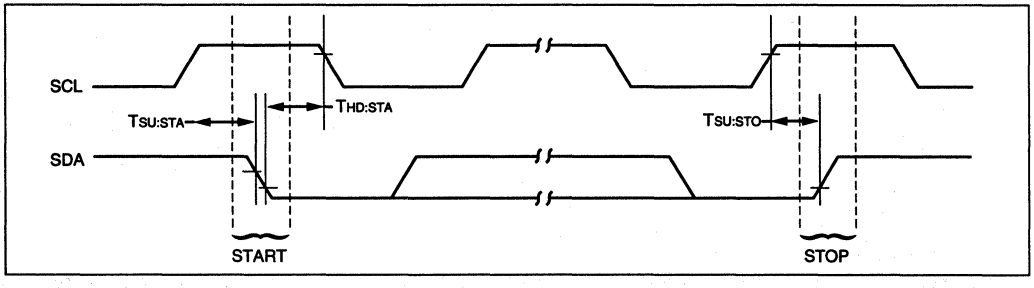
DC CHARACTERISTICS

Vcc = +5V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C (Note 2)

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL	-0.3	Vcc x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI	—	10	µA	VIN = 0V to Vcc
Output leakage current	ILO	—	10	µA	VOUT = 0V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	7.0	pF	VIN/VOUT = 0V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO	—	3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5V, Tamb = 0°C to +70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5V, Tamb = (I) and (E)
read cycle	ICCR	—	750	µA	Vcc = 5V, Tamb = (C), (I) and (E)
Standby current	ICCS	—	100	µA	SDA = SCL = Vcc = 5V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles

BUS TIMING START/STOP

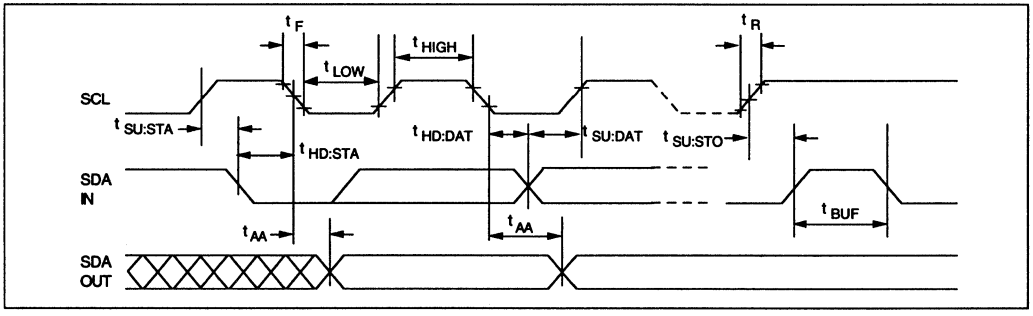


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK	—	—	100	kHz	
Clock high time	THIGH	4000	—	—	ns	
Clock low time	TLOW	4700	—	—	ns	
SDA and SCL rise time	TR	—	—	1000	ns	
SDA and SCL fall time	TF	—	—	300	ns	
START condition hold time	THD:STA	4000	—	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	—	ns	
Data input setup time	TSU:DAT	250	—	—	ns	
Data output delay time	TPD	300	—	3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700	—	—	ns	
Bus free time	TBUF	4700	—	—	ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI	—	—	100	ns	
Program cycle time	TWC	—	.4 .4N	1 N	ms ms	Byte Mode Page Mode, N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 85C72/82/92 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 85C72/82/92 works as slave. Both, master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Up to eight 85C72/82/92s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus, but require different device codes than the 85C72/82/92 (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

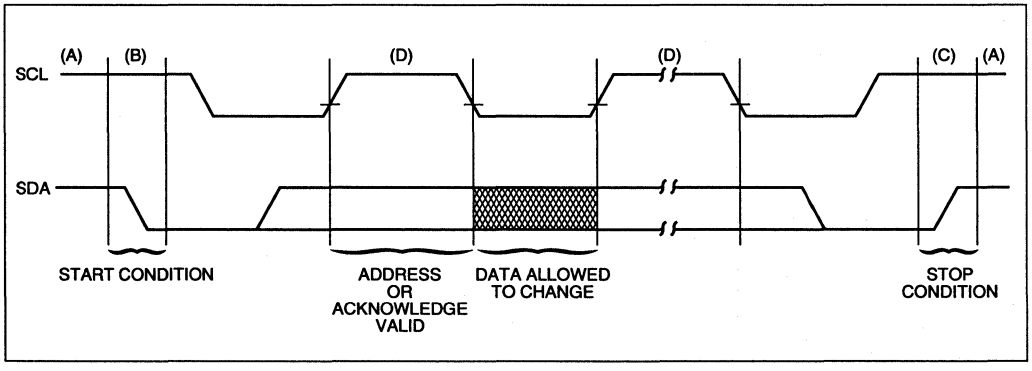
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 85C72/82/92 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

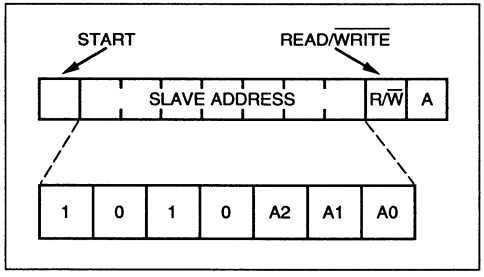
The chip address inputs A0, A1 and A2 of each 85C72/82/92 must be externally connected to either Vcc or ground (Vss), assigning to each 85C72/82/92 a unique 3-bit address. Up to eight 85C72/82/92s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the transmitted slave address to the corresponding hardwired logic levels of the selected 85C72/82/92.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 85C72/82/92, followed by the chip address bits A0, A1 and A2. In the 85C92 the seventh bit of that byte (BA) is used to select the upper block (addresses 100 - 1FF) or the lower block (000 - FFF) of the array.

The eighth bit of slave address determines if the master device wants to read or write to the 85C72/82/92 (see Figure 2).

The 85C72/82/92 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode the master sends addresses and one data byte to the 85C72/82/92.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 85C72/82/92 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 85C72/82/92. After receiving the acknowledge of the 85C72/82/92, the master device transmits the data word to be written into the addressed memory location. The 85C72/82/92 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 85C72/82/92 (see Figure 3).

PAGE PROGRAM MODE

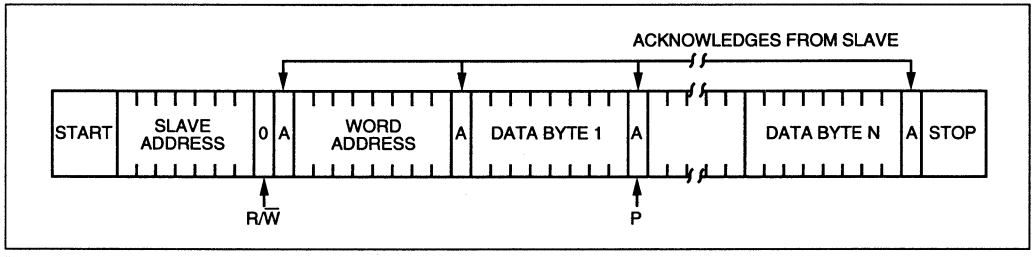
To program the 85C72/82/92, the master sends addresses and data to the 85C72/82/92 which is the slave (see Figure 3). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 85C72/82/92, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. The 85C72/82/92 will generate an acknowledge after every 8 bits received and store them consecutively in a 2-byte RAM until a stop condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 85C72/82/92 will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to two) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

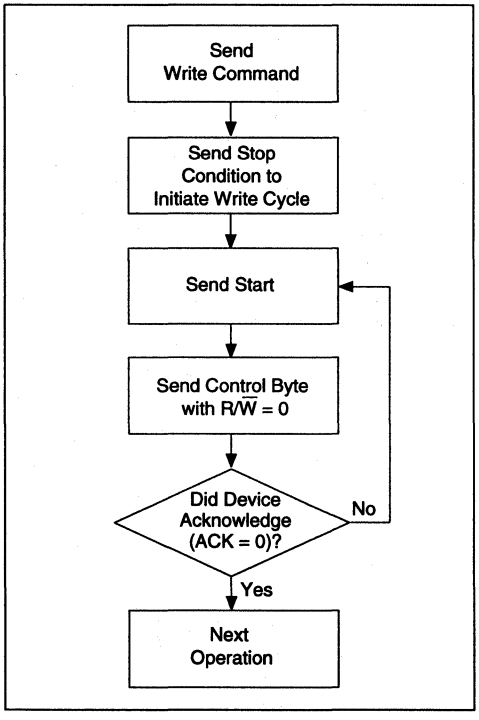
FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 4 for flow diagram.

FIGURE 4 - ACKNOWLEDGE POLLING FLOW



READ MODE

This mode illustrates master device reading data from the 85C72/82/92.

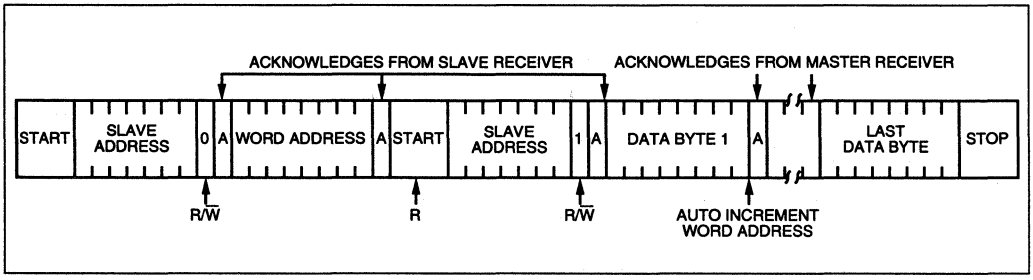
As can be seen from Figure 5, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to.) During this period the 85C72/82/92 generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 5 and save time transmitting the slave and word addresses.

Note: In all modes, the address pointer will automatically increment from the end of the memory block (256 byte) back to the first location in that block.

FIGURE 5 - READ MODE



PIN DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true. For 85C92, A0 is no function.

Up to eight 85C72/82s or four 85C92s can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ). For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

NC No Connect

This pin can be left open or used as a tie point.

Notes:

1. A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 85C72/82 page is 2 bytes long and the 85C92 page is 8 bytes long.
2. A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 85C72/82 has only one block (256 bytes), while the 85C92 has two blocks of 256 bytes each.

5

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

85C82 - /P

PACKAGE:	J	CERDIP
	P	Plastic DIP
	SM	Plastic SOIC (207 mil Body) 8-Lead
	SL	Plastic SOIC 14-Lead (85C92 only)
TEMPERATURE RANGE:	Blank	0°C to +70°C
	I	-40°C to +85°C
	E	-40°C to +125°C
DEVICE:	85C72	1K CMOS Serial EEPROM
	85C72T	1K CMOS Serial EEPROM (in Tape & Reel)
	85C82	2K CMOS Serial EEPROM
	85C82T	2K CMOS Serial EEPROM (in Tape & Reel)
	85C92	4K CMOS Serial EEPROM
	85C92T	4K CMOS Serial EEPROM (in Tape & Reel)

93C06/46

256 Bit/1K 5V CMOS Serial EEPROM

FEATURES

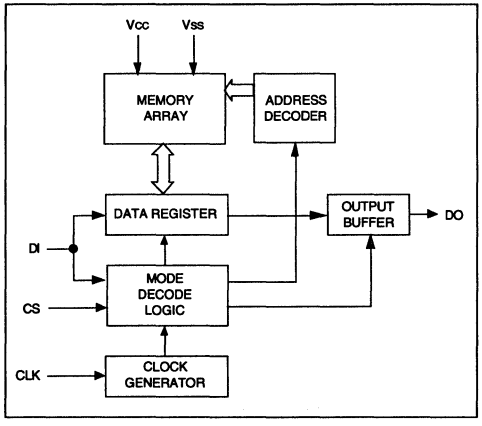
- Low power CMOS technology
- 16 bit memory organization
  - — 16 x 16 bit organization (93C06)
  - — 64 x 16 bit organization (93C46)
- Single 5 volt only operation
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- 1,000,000 ERASE/WRITE cycles (typical)
- Data Retention > 40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - — Commercial: 0°C to +70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C
- 2 ms program cycle time

DESCRIPTION

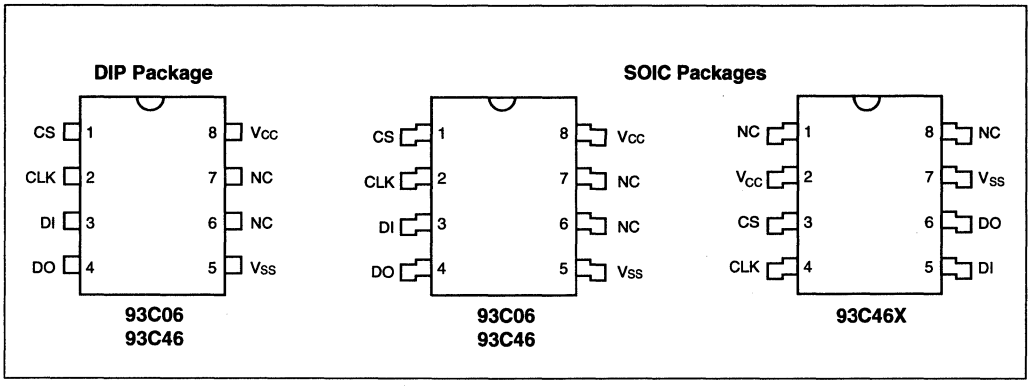
The Microchip Technology Inc. 93C06/46 family of Serial Electrically Erasable PROMs are configured in a x16 organization. Advanced CMOS technology makes these devices ideal for low-power non-volatile memory applications. The 93C06/46 is available in the standard 8-pin DIP and surface mount SOIC packages. The 93C46X comes as SOIC only.

These devices offer fast (1 ms) byte write and extended (-40°C to 125°C) temperature operation. It is recommended that all other applications use Microchip's 93LC46.

BLOCK DIAGRAM



PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temperature with
power applied ..... -65°C to +125C
Soldering termperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
Vss	Ground
NC	No Connect; No Internal Connection
Vcc	+5V Power Supply

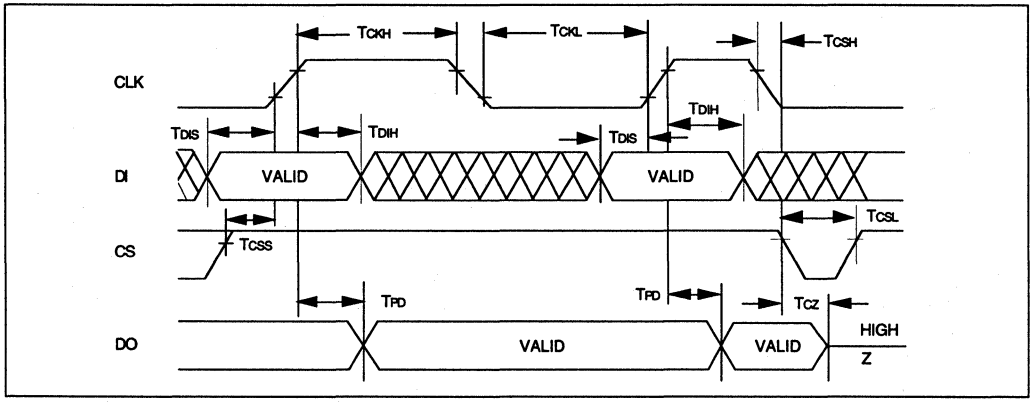
DC CHARACTERISTICS

Vcc = +5V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = –40°C to +85°C
Automotive: Tamb = –40°C to +125°C (Note 3)

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	Vcc + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4	—	V	IOH = -400 µA
Low level output voltage	VOL	—	0.4	V	IOL = 3.2 mA
Input leakage current	ILI	—	10	µA	VIN = 0V to Vcc (Note 1)
Output leakage current	ILO	—	10	µA	VOUT = 0V to Vcc (Note 1)
Internal capacitance (all inputs/outputs)	CINT	—	7	pF	VIN/VOUT = 0V (Note 2) Tamb = +25°C, f = 1 MHz
Operating current (all modes)	Icc write	—	4	mA	FCLK = 1 MHz, Vcc = 5.5V
Standby current	Iccs	—	100	µA	CS = 0V, Vcc = 5.5V

Note 1: Internal resistor pull-up at Pin 6.
Note 2: This parameter is periodically sampled and not 100% tested.
Note 3: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

SYNCHRONOUS DATA TIMING



AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500	—	ns	
Clock low time	TCKL	500	—	ns	
Chip select setup time	TCSS	50	—	ns	
Chip select hold time	TCSH	0	—	ns	
Chip select low time	TCSL	100	—	ns	
Data input setup time	TDIS	100	—	ns	
Data input hold time	TDIH	100	—	ns	
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time (from CS = low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
Status valid time	TSV	—	100	ns	CL = 100 pF
Program cycle time (Auto Erase and Write)	TWC	—	2 15	ms ms	for ERAL and WRAL
Erase cycle time	TEC	—	1	ms	
Endurance	—	100,000	—	E/W Cycles	

5

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C06/46. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but STARTcondition has not been detected, any number of clock cycles can be received by the device without changing its status. (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition, the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become "Don't Care" inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) from the falling edge of the CLK which clocked in the last DI bit (D0 for WRITE, A0 for ERASE) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is outputted after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during Erase and Write cycles if the READY/BUSY status information is outputted by the 93C06/46.

INSTRUCTION SET - 93C06

Instruction	Start BIT	Opcode OP1	Opcode OP2	Address						Number of Data In	Data Out	Req. CLK Cycles
READ	1	1	0	0	0	A3	A2	A1	A0	—	D15 – D0	25
WRITE	1	0	1	0	0	A3	A2	A1	A0	D15 – D0	(RDY/$\overline{BSY}$)	25
ERASE	1	1	1	0	0	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	9
EWEN	1	0	0	1	1	X	X	X	X	—	High-Z	9
EWDS	1	0	0	0	0	X	X	X	X	—	High-Z	9
ERAL	1	0	0	1	0	X	X	X	X	—	(RDY/$\overline{BSY}$)	9
WRAL	1	0	0	0	1	X	X	X	X	D15 – D0	(RDY/$\overline{BSY}$)	25

INSTRUCTION SET - 93C46

Instruction	Start BIT	Opcode OP1	Opcode OP2	Address						Number of Data In	Data Out	Req. CLK Cycles
READ	1	1	0	A5	A4	A3	A2	A1	A0	—	D15 – D0	25
WRITE	1	0	1	A5	A4	A3	A2	A1	A0	D15 – D0	(RDY/$\overline{BSY}$)	25
ERASE	1	1	1	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	9
EWEN	1	0	0	1	1	X	X	X	X	—	High-Z	9
EWDS	1	0	0	0	0	X	X	X	X	—	High-Z	9
ERAL	1	0	0	1	0	X	X	X	X	—	(RDY/$\overline{BSY}$)	9
WRAL	1	0	0	0	1	X	X	X	X	D15 – D0	(RDY/$\overline{BSY}$)	25

FUNCTIONAL DESCRIPTION

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all modes of operation are inhibited until Vcc has reached 2.8V. During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below 2.8V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 16-bit output string. The output data changes during the HIGH state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 has been a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the low going edge of CS, which ever occurs first.

DO remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

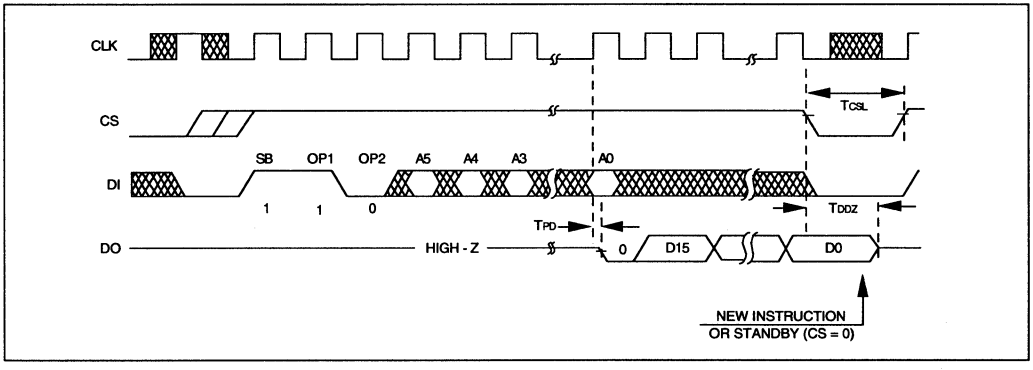
The most significant data bit (D15) is always output first, followed by the lower significant bits (D14 - D0).

WRITE Mode

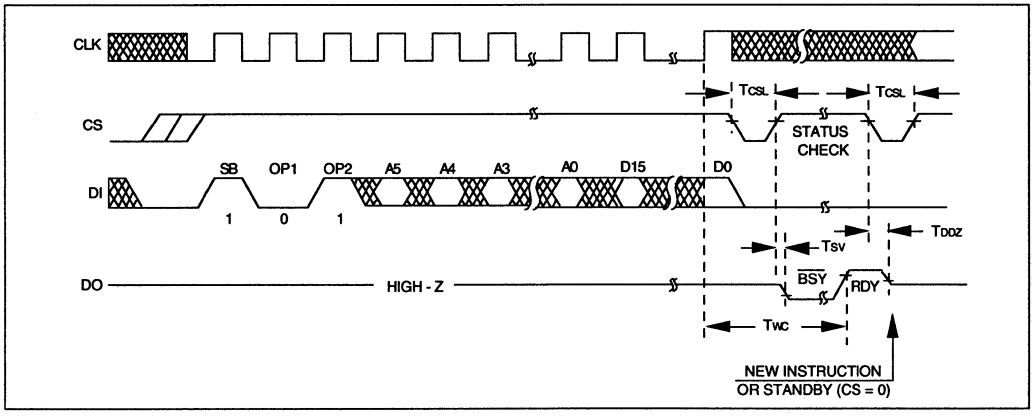
The WRITE instruction is followed by 16 bits of data which are written into the specified address. The most significant data bit (D15) has to be clocked in first, followed by the lower significant data bits (D14 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic ERASE cycle on the specified address before the data are written. The WRITE cycle is completely self-timed and commences automatically after the rising edge of the CLK for the last data bit (D0).

The WRITE cycle takes 2 ms maximum.

READ MODE



WRITE MODE

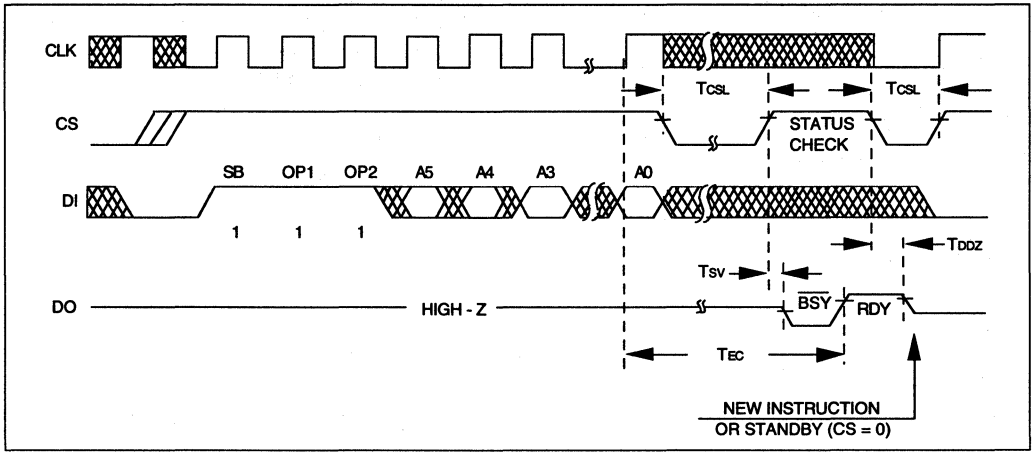


ERASE Mode

The ERASE instruction forces all the data bits of the specified address to logical "1s". The ERASE cycle is completely self-timed and commences automatically after the last address bit has been clocked in.

The ERASE cycle takes 1 ms maximum.

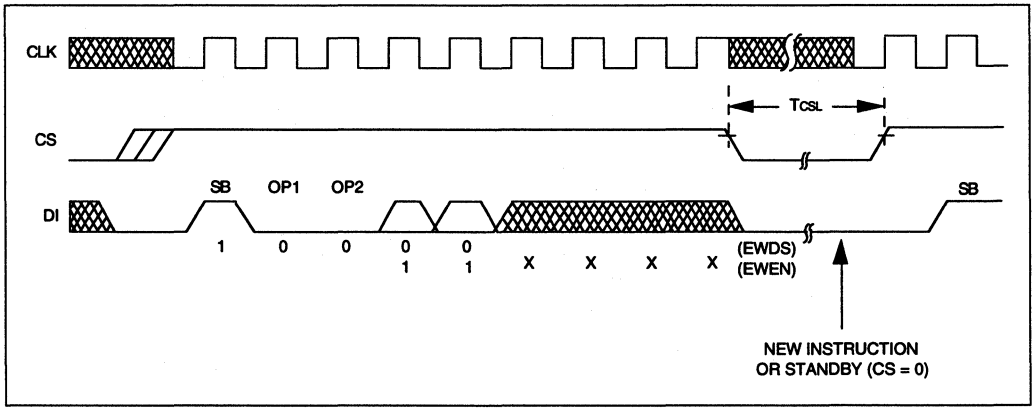
ERASE MODE



ERASE/WRITE Enable/Disable (EWEN, EWDS)

The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, an EWEN instruction has to be performed before any ERASE, WRITE, ERAL, WRAL instruction is executed by the device. For added data protection, the device should be put in the ERASE/WRITE Disable mode (EWDS) after programming operations are completed.

ERASE/WRITE ENABLE/DISABLE

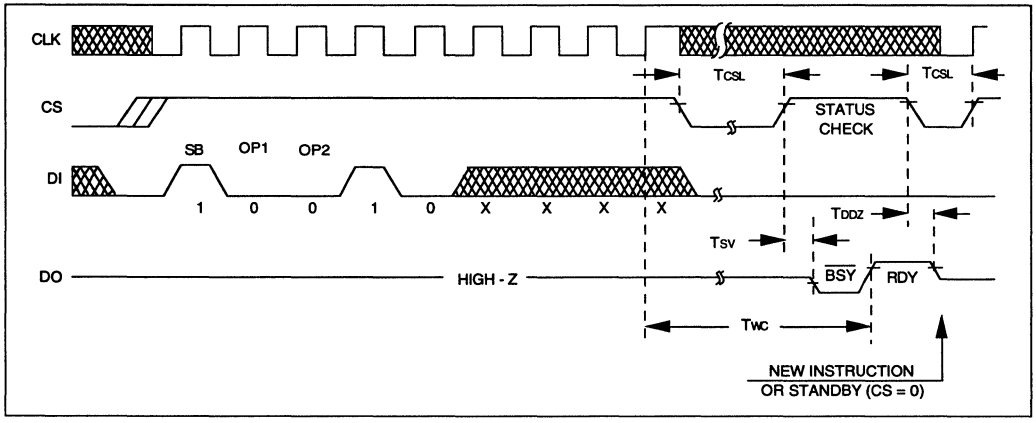


ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the last dummy address bit has been clocked in.

ERAL takes 15 ms maximum.

ERASE ALL



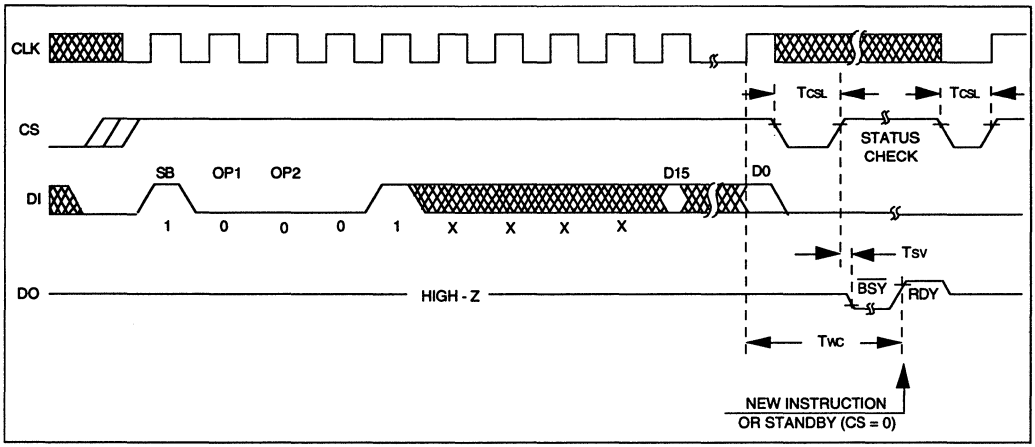
WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the rising edge of the CLK for the last data bit (DO). WRAL takes 15 ms maximum.

Note: The WRAL does not include an automatic ERASE cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The WRAL instruction is used for testing and/or device initialization.

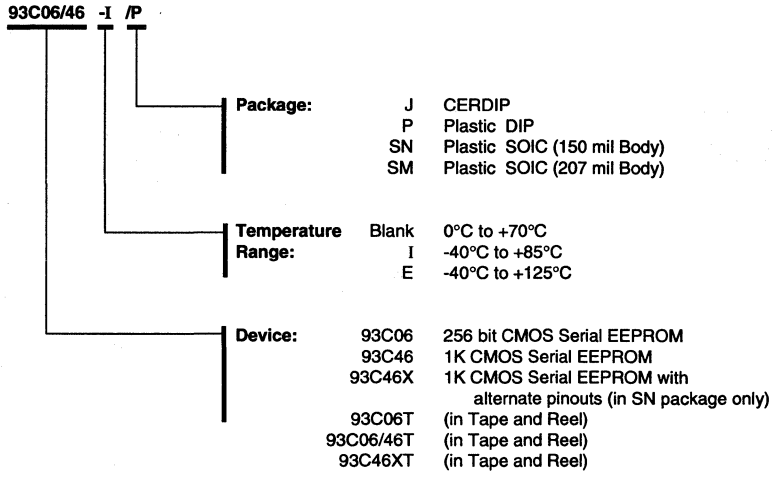
WRITE ALL



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



MICROCHIP

93C56/66

2K/4K 5V CMOS Serial EEPROM

FEATURES

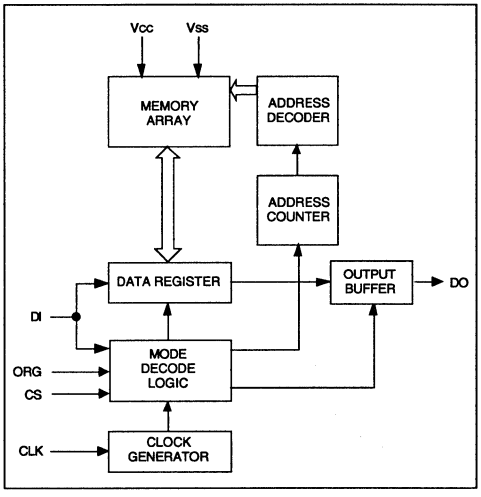
- Low power CMOS technology
- ORG pin selectable memory organization
  - — 256 x 8 or 128 x 16 bit organization (93C56)
  - — 512 x 8 or 256 x 16 bit organization (93C66)
- Single 5 volts only operation
- Max clock at 2 MHz
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8-pin PDIP/SOIC packages (SOIC in JEDEC and EIAJ standards)
- Available for extended temperature ranges:
  - — Commercial: 0°C to + 70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C
- 1 ms byte write time

DESCRIPTION

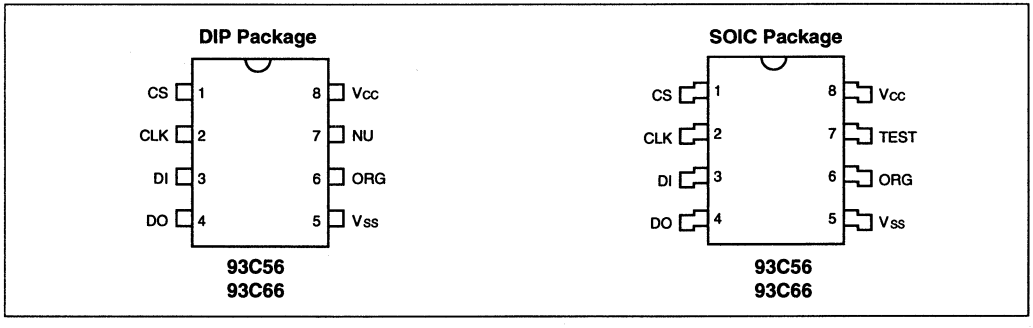
The Microchip Technology Inc. 93C56/66 family of Serial EEPROMs are configurable to either x16 or x8 organization. The ORG pin is used to select the desired configuration. Advanced CMOS technology makes this device ideal for low-power non-volatile memory applications. The 93C56/66 are available in the standard 8-pin DIP and 8-pin surface mount SOIC package.

This device offers fast (1 ms) byte write and extended (-40°C to 125°C) temperature operation. It is recommended that all other applications use Microchip's 93LC56/93LC66.

BLOCK DIAGRAM



PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied .... -65°C to +125°C
Soldering temperature of leads (10 seconds) . +300°C
ESD protection on all pins ..... 3 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
ORG	Memory Array Organization
Test	Connect to Vss or Vcc
Vcc	Power Supply +5V

DC AND AC ELECTRICAL CHARACTERISTICS

Commercial (C): Tamb = 0°C to +70°C Vcc = +5V (±10%)
Industrial (I): Tamb = -40°C to +85°C Vcc = +5V (±10%)
(Note 2) Automotive (E): Tamb = -40°C to +125°C Vcc = +5V (±10%)

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.3	4.5	V	
High level input voltage	VIH	2.0	Vcc + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL	—	0.4	V	IOL = 2.1 mA
Input leakage current	ILI	—	10	µA	VIN = 0V to Vcc
Output leakage current	ILO	—	10	µA	VOUT = 0V to Vcc
Output capacitance	COUT	—	7	pF	VIN/VOUT = 0V; Note 1
Input capacitance	CIN	—	7	pF	VIN/VOUT = 0V; Note 1
Operating current (all modes)	ICC write	—	4	mA	FCLK = 2 MHz; Vcc = 5.5V
Standby current	ICCS	—	130	µA	CS = 0V; Vcc = 5.5V; x 8 org
	—	—	100	µA	CS = 0V; Vcc = 5.5V; x 16 org
Endurance	—	100,000	—	E/W Cycles	
Clock frequency	FCLK		2	MHz	
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	100	—	ns	
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time	TCZ	—	100	ns	CL = 100 pF
Status valid time	TSV	—	100	ns	CL = 100 pF
Program cycle time	TWC	—	1	ms	(x 8 organization)
(auto ERASE and WRITE)		—	2	ms	(x 16 organization)
	TEC	—	15	ms	ERAL & WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz. It is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

INSTRUCTION SET FOR 93C56

ORG = 1 (x 16 organization)						
Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

ORG = 0 (x 8 organization)						
Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

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INSTRUCTION SET FOR 93C66

ORG = 1 (x 16 organization)						
Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

ORG = 0 (x 8 organization)						
Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

FUNCTIONAL DESCRIPTION

The 93C56/66 family can be organized x16 or x8. When the ORG pin is connected to Vcc, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the (x16) organization. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the ready/busy status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CLK.

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all modes of operation are inhibited until Vcc has reached 2.3 V. During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below 2.3 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

ERASE/WRITE ENABLE AND DISABLE

The 93C56/66 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data changes, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 1 ms per byte maximum.

WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/BUSY status of the device if CS is brought high after a minimum of 100 ns (T_{CSL}). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 1 ms per byte maximum.

ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1". The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (T_{CSL}).

The ERAL cycle takes 15 ms maximum.

WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does not include an automatic ERASE cycle for the device. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (T_{CSL}).

The WRAL cycle takes 15 ms maximum.

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (T_{CSL}) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C56/66. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (T_{CKH}) and clock LOW time (T_{CKL}). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (T_{PD} after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/BUSY status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (T_{CSL}) and an ERASE or WRITE operation has been initiated.

Organization (ORG)

When ORG is connected to V_{CC}, the (x16) memory organization is selected. When ORG is tied to V_{SS}, the (x8) memory organization is selected. When ORG is left floating, an internal pullup device will select the device in (x16) organization.

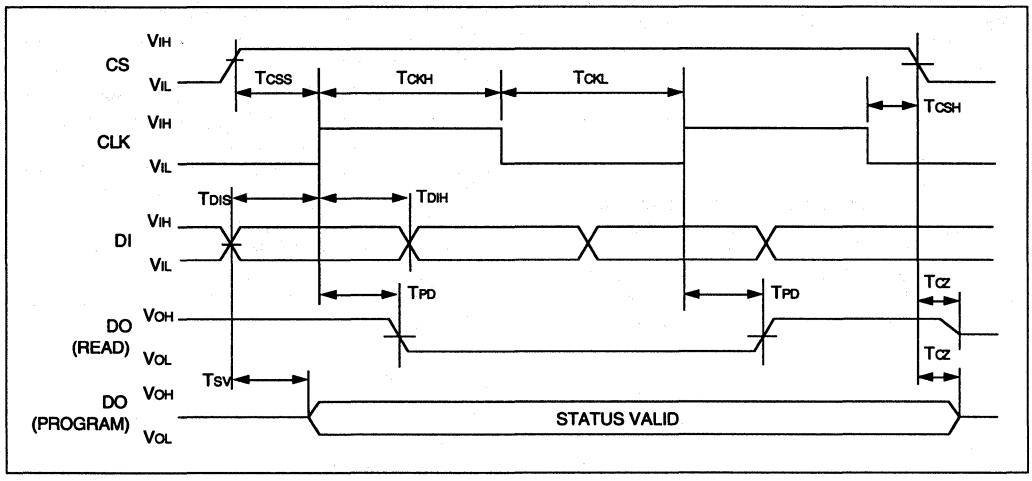
Test

This pin is used for test mode only. It is recommended to connect to V_{CC} or V_{SS} for normal operation.

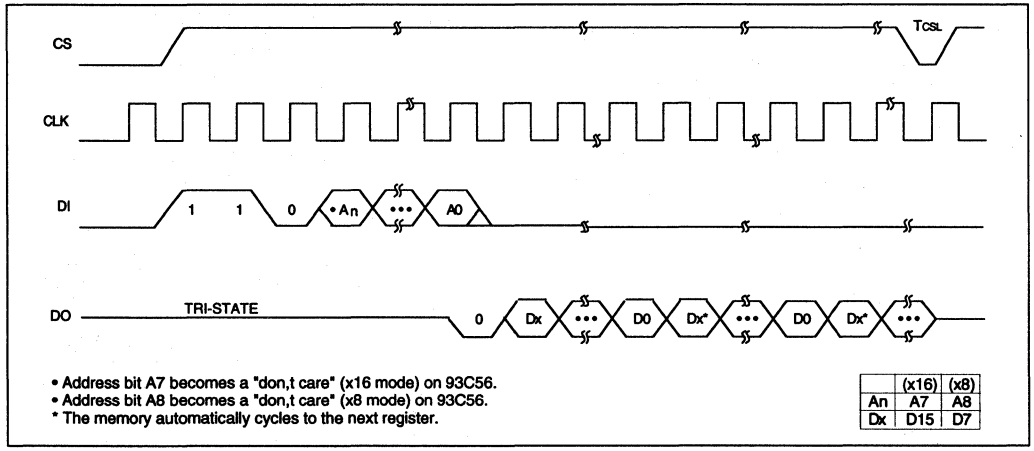
5

TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



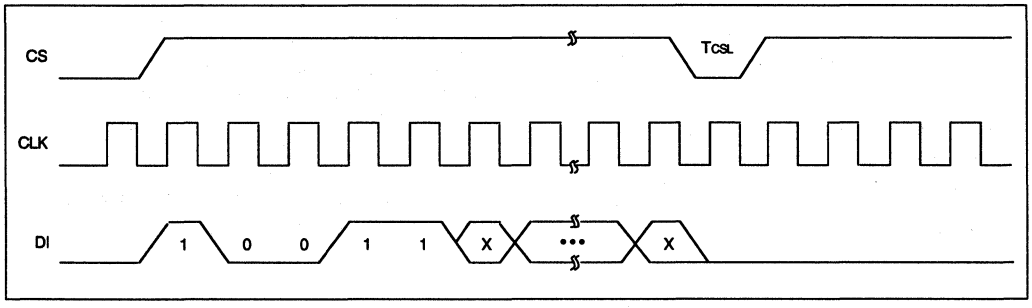
READ



• Address bit A7 becomes a "don,t care" (x16 mode) on 93C56.
• Address bit A8 becomes a "don,t care" (x8 mode) on 93C56.
* The memory automatically cycles to the next register.

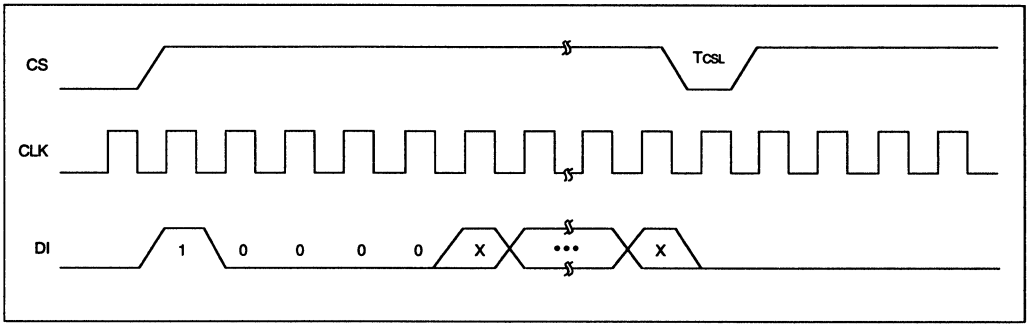
	(x16)	(x8)
An	A7	A8
Dx	D15	D7

EWEN

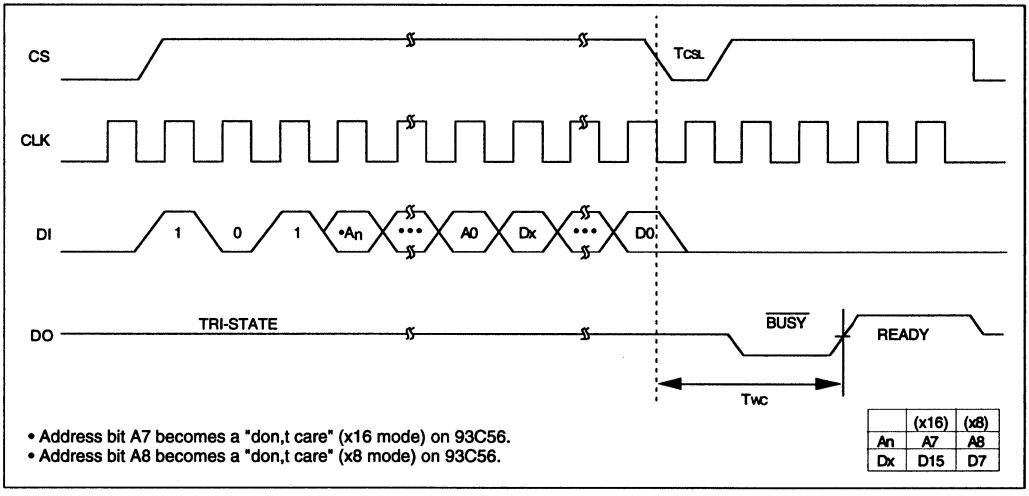


TIMING DIAGRAMS (Cont.)

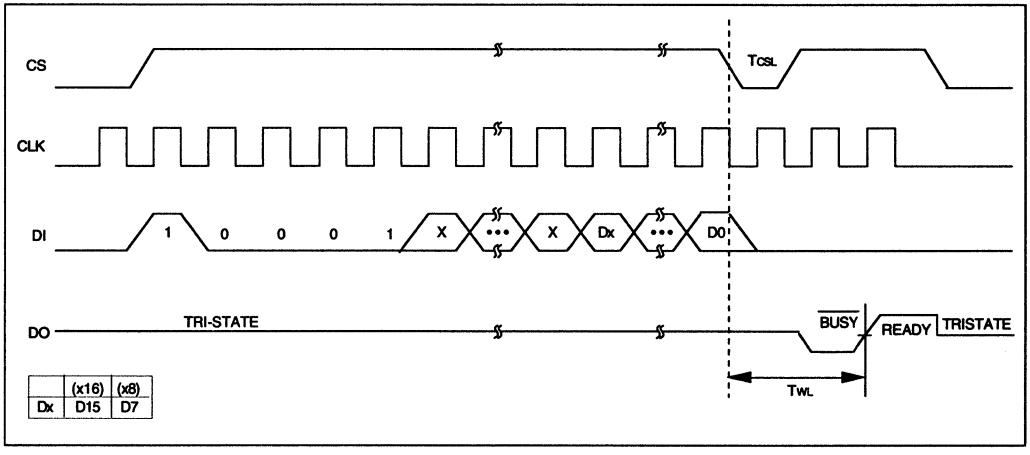
EWDS



WRITE

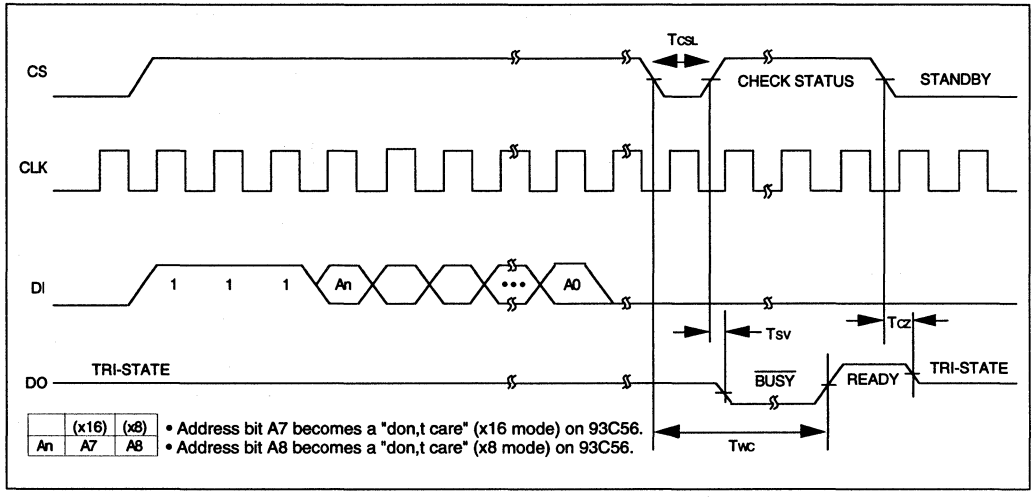


WRAL

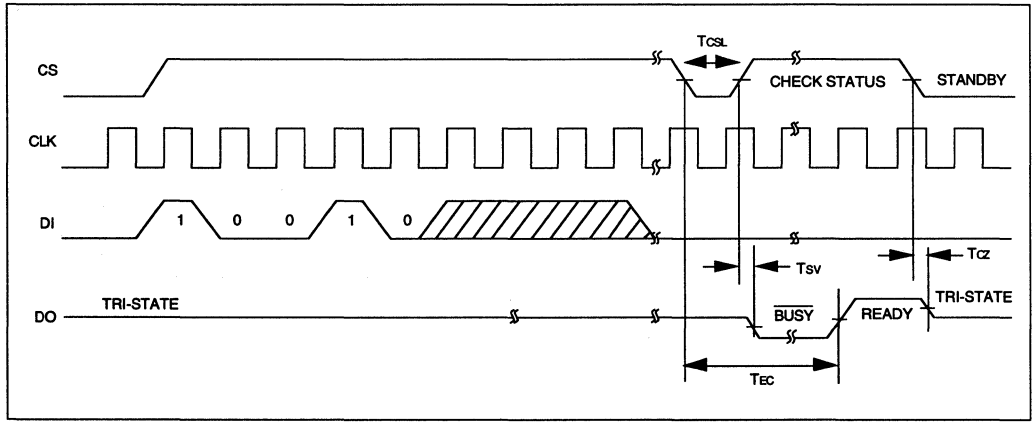


TIMING DIAGRAMS (Cont.)

ERASE



ERAL



NOTES

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

93C56/66 - /P

PACKAGE:	P	PLASTIC DIP
	SN	PLASTIC SOIC (150 mil Body)
	SM	PLASTIC SOIC (207 mil Body)
TEMPERATURE RANGE:	Blank	0°C to +70°C
	I	-40°C to +85°C
	E	-40°C to +125°C
DEVICE TYPE:	93C56	2K CMOS Serial EEPROM
	93C56T	2K CMOS Serial EEPROM (in Tape and Reel Form)
	93C66	4K CMOS Serial EEPROM
	93C66T	4K CMOS Serial EEPROM (in Tape and Reel Form)

93LC46/56/66

1K/2K/4K 2.0V CMOS Serial EEPROM

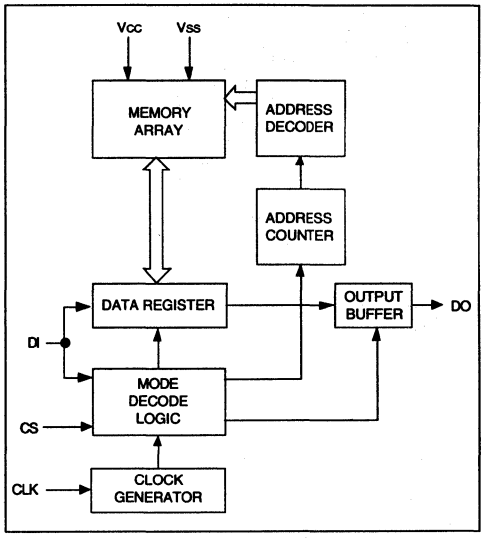
FEATURES

- Single supply with programming operation down to 2.0V (Commercial only)
- Low power CMOS technology
  - 1 mA active current typical
  - 5 µA standby current (typical) at 3.0V
- ORG pin selectable memory configuration
  128 x 8 or 64 x 16 bit organization (93LC46)
  256 x 8 or 128 x 16 bit organization (93LC56)
  512 x 8 or 256 x 16 bit organization (93LC66)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8-pin PDIP/SOIC and 14-pin SOIC package (SOIC in JEDEC and EIAJ standards)
- Available for extended temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

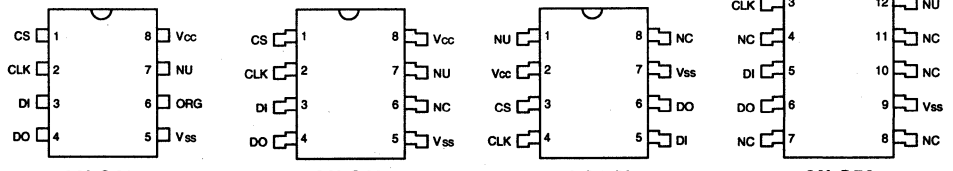
DESCRIPTION

The Microchip Technology Inc. 93LC46/56/66 are 1K, 2K and 4K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. The 93LC Series is available in standard 8-pin DIP and 8/14-pin surface mount SOIC packages. The 93LC46X/56X/66X are offered in "SN" package only.

BLOCK DIAGRAM



PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss .... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
ORG	Memory Configuration
NU	Not Utilized
NC	No Connect
Vcc	Power Supply

DC AND AC ELECTRICAL CHARACTERISTICS

Commercial Vcc = +2.0V to +6.0V (C): Tamb = 0°C to +70°C
Industrial Vcc = +2.5V to +6.0V (I) : Tamb = -40°C to +85°C

Parameter	Symbol	Min	Max	Units	Conditions
High level input voltage	V_{IH1}	2.0	Vcc +1	V	$V_{DD} \geq 2.5V$
	V_{IH2}	0.7 Vcc	Vcc +1	V	$V_{DD} < 2.5V$
Low level input voltage	V_{IL1}	-0.3	0.8	V	$V_{DD} \geq 2.5V$
	V_{IL2}	-0.3	0.2 Vcc	V	$V_{DD} < 2.5V$
Low level output voltage	V_{OL1}	—	0.4	V	I_{OL} = 2.1 mA; Vcc = 4.5V
	V_{OL2}	—	0.2	V	I_{OL} =100 µA; Vcc = Vcc Min.
High level output voltage	V_{OH1}	2.4	—	V	I_{OH} = -400 µA; Vcc = 4.5V
	V_{OH2}	Vcc-0.2	—	V	I_{OH} = -100 µA; Vcc = Vcc Min.
Input leakage current	I_{LI}	-10	10	µA	V_{IN} = 0.1V to Vcc
Output leakage current	I_{LO}	-10	10	µA	V_{OUT} = 0.1V to Vcc
Internal capacitance (all inputs/outputs)	C_{INT}	—	7	pF	V_{IN}/V_{OUT} = 0 V (Note 1 & 3) Tamb = +25°C, F_{CLK} = 1 MHz
Operating current	Icc write	—	3	mA	F_{CLK} = 2 MHz; Vcc = 6.0V (Note 3)
	Icc read	—	1	mA	F_{CLK} = 2 MHz; Vcc = 6.0V
			500	µA	F_{CLK} = 1 MHz; Vcc = 3.0V
Standby current	Iccs	—	100	µA	CLK = CS = 0V; Vcc = 6.0V
			30	µA	CLK = CS = 0V; Vcc = 3.0V
Endurance	—	100,000		E/W Cycles	1,000,000 E/W cycles typical
Clock frequency	F_{CLK}	—	2	MHz	Vcc ≥ 4.5V
			1	MHz	Vcc < 4.5V
Clock high time	T_{CKH}	250	—	ns	
Clock low time	T_{CKL}	250	—	ns	
Chip select setup time	T_{CSS}	50	—	ns	Relative to CLK
Chip select hold time	T_{CSH}	0	—	ns	Relative to CLK
Chip select low time	T_{CSL}	250	—	ns	
Data input setup time	T_{DIS}	100	—	ns	Relative to CLK
Data input hold time	T_{DIH}	100	—	ns	Relative to CLK
Data output delay time	T_{PD}	—	400	ns	C_L = 100 pF
Data output disable time	T_{CZ}	—	100	ns	C_L = 100 pF (Note 3)
Status valid time	T_{SV}	—	500	ns	C_L = 100 pF
Program cycle time	T_{WC}	—	10	ms	ERASE/WRITE mode (Note 2)
	T_{EC}	—	15	ms	ERAL mode
	T_{WL}		30	ms	WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and F_{CLK} = 1 MHz.
Note 2: Typical program cycle time is 4 ms per word.
Note 3: This parameter is periodically sampled and not 100% tested.

INSTRUCTION SET FOR 93LC46: ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
EWEN	1	00	1 1 X X X X	—	High-Z	9
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	9
ERAL	1	00	1 0 X X X X	—	(RDY/$\overline{BSY}$)	9
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	25
WRAL	1	00	0 1 X X X X	D15 - D0	(RDY/$\overline{BSY}$)	25
EWDS	1	00	0 0 X X X X	—	High-Z	9

INSTRUCTION SET FOR 93LC46: ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	18
EWEN	1	00	1 1 X X X X X	—	High-Z	10
ERASE	1	11	A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	10
ERAL	1	00	1 0 X X X X X	—	(RDY/$\overline{BSY}$)	10
WRITE	1	01	A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	18
WRAL	1	00	0 1 X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	18
EWDS	1	00	0 0 X X X X X	—	High-Z	10

INSTRUCTION SET FOR 93LC56: ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

INSTRUCTION SET FOR 93LC56: ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X	—	High-Z	12

INSTRUCTION SET FOR 93LC66: ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

INSTRUCTION SET FOR 93LC66: ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

5

FUNCTIONAL DESCRIPTION

When the ORG pin is connected to Vcc, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the ready/busy status during a programming operation. The READY/$\overline{\text{BUSY}}$ status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V at nominal conditions.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

ERASE/WRITE ENABLE AND DISABLE

The 93LC46/56/66 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 4 ms per word (Typical).

WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.
The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 4 ms per word (Typical).

ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at Vcc = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The ERAL cycle takes 15 ms maximum (8 ms typical).

WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at Vcc = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The WRAL cycle takes 30 ms maximum (16 ms typical).

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93LCXX. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) and an ERASE or WRITE operation has been initiated.

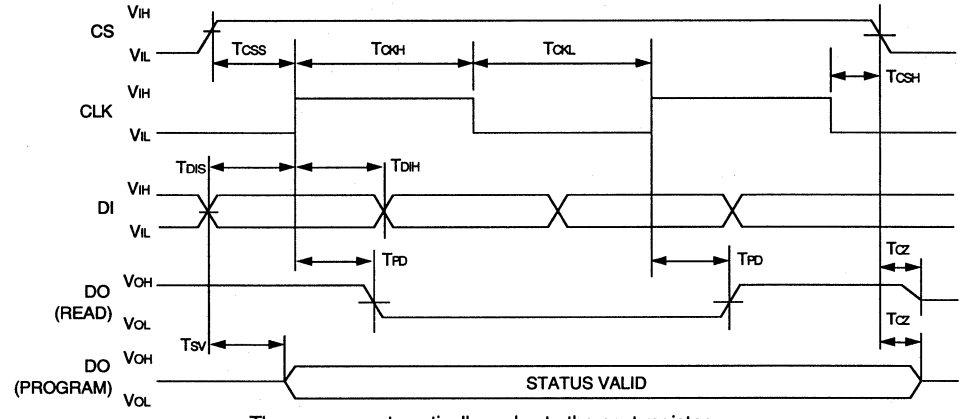
Organization (ORG)

When ORG is connected to Vcc or floated, the (x16) memory organization is selected. When ORG is tied to Vss, the (x8) memory organization is selected. ORG can only be floated for clock speeds of 1 MHz or less for the (X16) memory organization. For clock speeds greater than 1 MHz, ORG must be tied to Vcc or Vss.

5

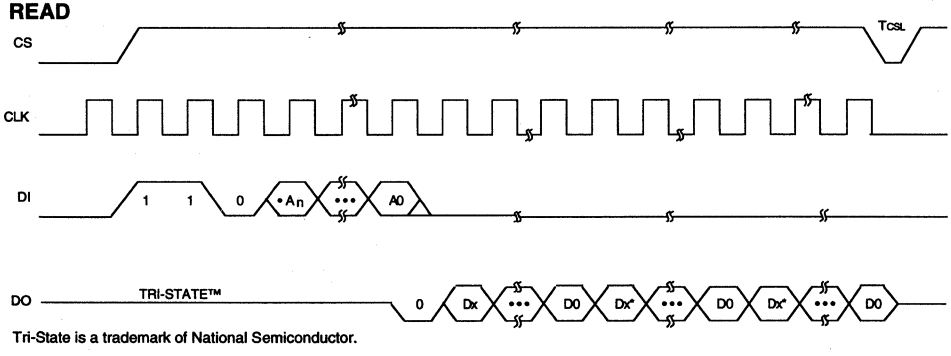
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



- The memory automatically cycles to the next register.

READ



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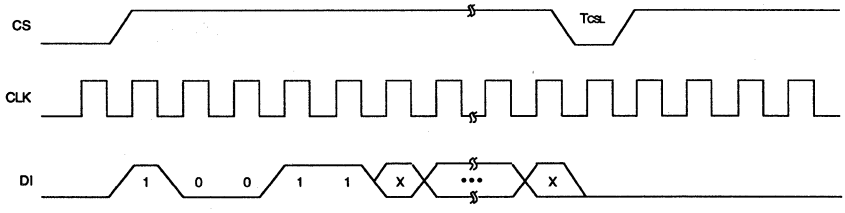
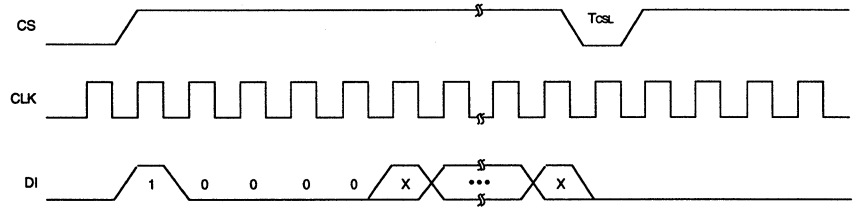
EWEN

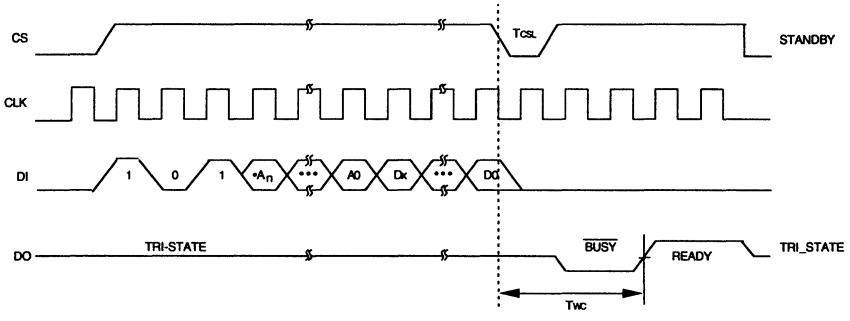


EWDS

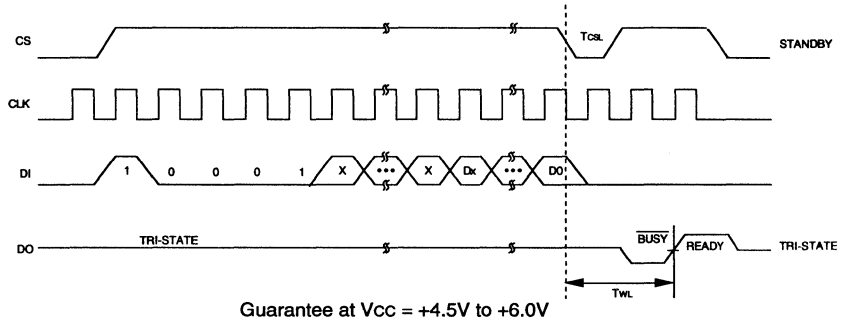


TIMING DIAGRAMS (Cont.)

WRITE

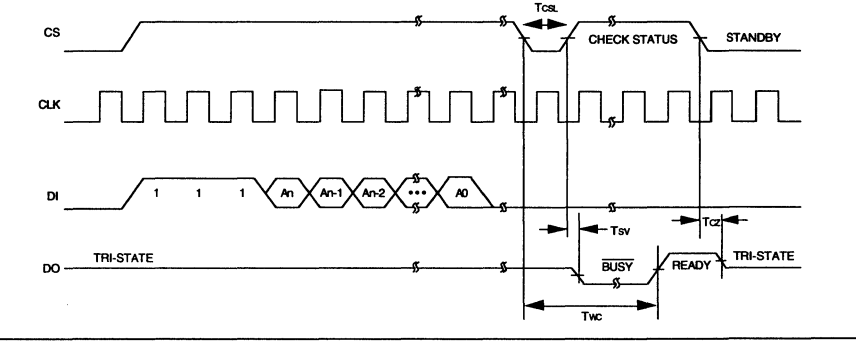


WRAL

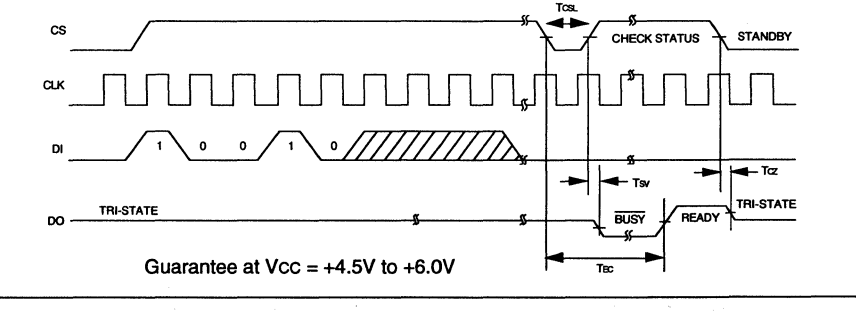


Guarantee at Vcc = +4.5V to +6.0V

ERASE



ERAL



Guarantee at Vcc = +4.5V to +6.0V

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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

93LC46B/56B/66B - /P

PACKAGE:

P	PLASTIC DIP
SN	PLASTIC SOIC (150 mil Body) 8-Lead
SM	PLASTIC SOIC (207 mil Body) 8-Lead
SL	PLASTIC SOIC (150 mil Body) 14-Lead

TEMPERATURE RANGE:

Blank	0°C to +70°C
I	-40°C to +85°C

DEVICE TYPE:

Configuration	
CMOS Serial EEPROM	93LC46B/56B/66B
CMOS Serial EEPROM In Alternate Pinouts (SN pkg. only)	93LC56X/66X
CMOS Serial EEPROM In Tape & Reel	93LC46T/56T/66T
CMOS Serial EEPROM In Tape & Reel	93LC56XT/66XT

93LC46B/56B/66B

1K/2K/4K 2.0V CMOS Serial EEPROM

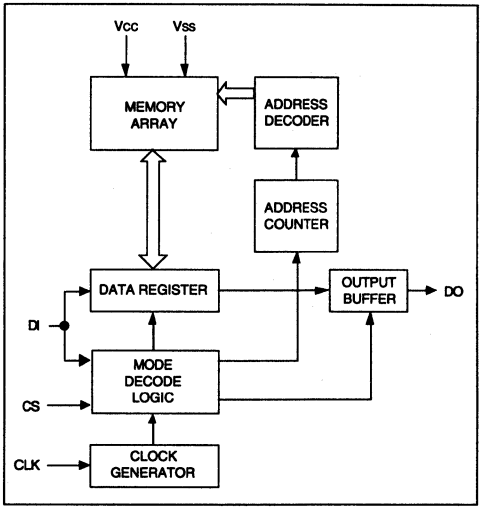
FEATURES

- Single supply with programming operation down to 2.0V (Commercial only)
- Low power CMOS technology
  - 1 mA active current typical
  - 5 μA standby current (typical) at 3.0V
- x16 bit organization
- 64x16 (93LC46B)
- 128x16 (93LC56B)
- 256x16 (93LC66B)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8-pin PDIP/SOIC and 14-pin SOIC package (SOIC in JEDEC and EIAJ standards)
- Available for extended temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

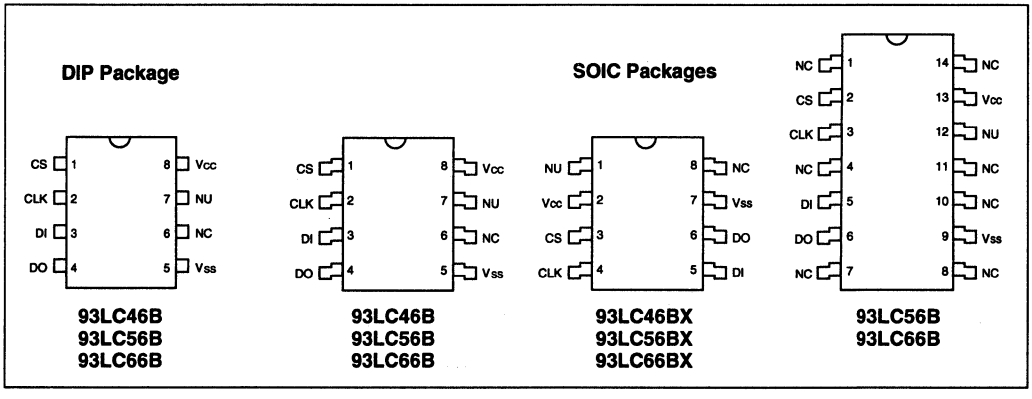
DESCRIPTION

The Microchip Technology Inc. 93LC46B/56B/66B are 1K, 2K and 4K low voltage serial Electrically Erasable PROMs. The device memory is configured as x16. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. The 93LC Series is available in standard 8-pin DIP and 8/14-pin surface mount SOIC packages.

BLOCK DIAGRAM



PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss .... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
NC	No Connect
NU	Not Utilized
Vcc	Power Supply

DC AND AC ELECTRICAL CHARACTERISTICS

Commercial Vcc = +2.0V to +6.0V (C): Tamb = 0°C to +70°C
Industrial Vcc = +2.5V to +6.0V (I) : Tamb = -40°C to +85°C

Parameter	Symbol	Min	Max	Units	Conditions
High level input voltage	VIH1	2.0	Vcc +1	V	VDD ≥ 2.5V
	VIH2	0.7 Vcc	Vcc +1	V	VDD < 2.5V
Low level input voltage	VIL1	-0.3	0.8	V	VDD ≥ 2.5V
	VIL2	-0.3	0.2 Vcc	V	VDD < 2.5V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 mA; Vcc = 4.5V
	VOL2	—	0.2	V	IOL =100 µA; Vcc = Vcc Min.
High level output voltage	VOH1	2.4	—	V	IOH = -400 µA; Vcc = 4.5V
	VOH2	Vcc-0.2	—	V	IOH = -100 µA; Vcc =Vcc Min.
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	7	pF	VIN/VOUT = 0 V (Note 1 & 3) Tamb = +25°C, FCLK = 1 MHz
Operating current	Icc write	—	3	mA	FCLK = 2 MHz; Vcc = 6.0V (Note 3)
	Icc read	—	1	mA	FCLK = 2 MHz; Vcc = 6.0V
			500	µA	FCLK = 1 MHz; Vcc = 3.0V
Standby current	ICCS	—	100	µA	CLK = CS = 0V; Vcc = 6.0V
			30	µA	CLK = CS = 0V; Vcc = 3.0V
Endurance	—	100,000		E/W Cycles	1,000,000 E/W cycles typical
Clock frequency	FCLK	—	2	MHz	Vcc ≥ 4.5V
			1	MHz	Vcc < 4.5V
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	250	—	ns	
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time	TCZ	—	100	ns	CL = 100 pF (Note 3)
Status valid time	TSV	—	500	ns	CL = 100 pF
Program cycle time	TWC	—	10	ms	ERASE/WRITE mode (Note 2)
	TEC	—	15	ms	ERAL mode
	TWL	—	30	ms	WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
Note 2: Typical program cycle time is 4 ms per word.
Note 3: This parameter is periodically sampled and not 100% tested.

INSTRUCTION SET FOR 93LC46B

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
EWEN	1	00	1 1 X X X X	—	High-Z	9
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	9
ERAL	1	00	1 0 X X X X	—	(RDY/$\overline{BSY}$)	9
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	25
WRAL	1	00	0 1 X X X X	D15 - D0	(RDY/$\overline{BSY}$)	25
EWDS	1	00	0 0 X X X X	—	High-Z	9

INSTRUCTION SET FOR 93LC56B

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

INSTRUCTION SET FOR 93LC66B

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

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FUNCTIONAL DESCRIPTION

Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the ready/busy status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V at nominal conditions.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

ERASE/WRITE ENABLE AND DISABLE

The 93LC46B/56B/66B powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 4 ms per word (Typical).

WRITE

The WRITE instruction is followed by 16 bits of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.
The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 4 ms per word (Typical).

ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at Vcc = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The ERAL cycle takes 15 ms maximum (8 ms typical).

WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at Vcc = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The WRAL cycle takes 30 ms maximum (16 ms typical).

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93LCXXB. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) and an ERASE or WRITE operation has been initiated.

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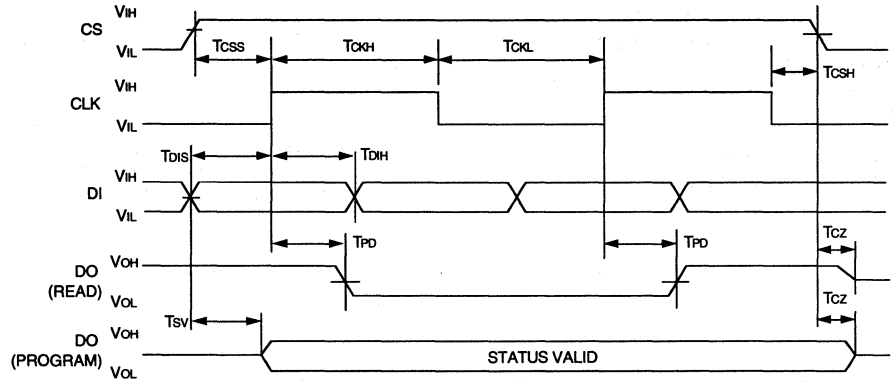
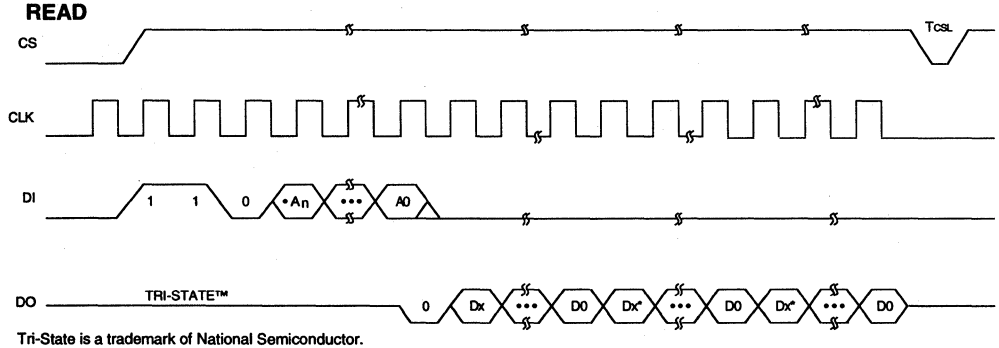
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



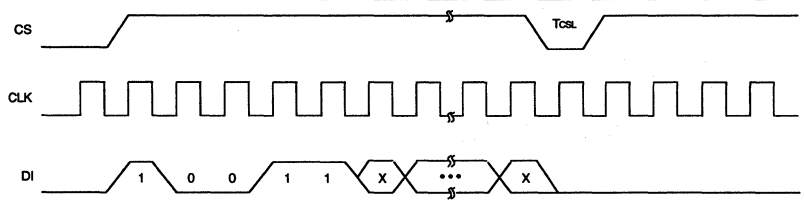
- The memory automatically cycles to the next register.

READ

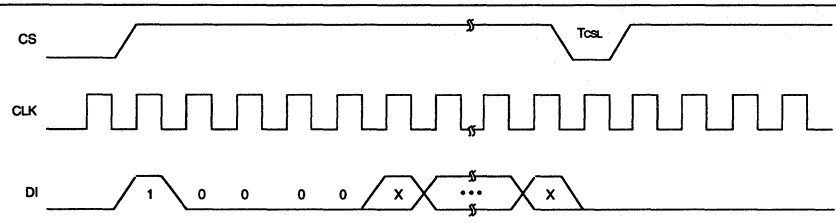


Tri-State is a trademark of National Semiconductor.

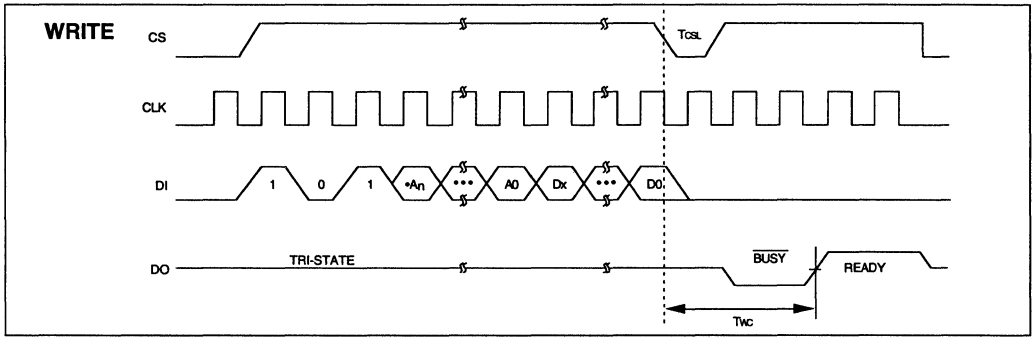
EWEN

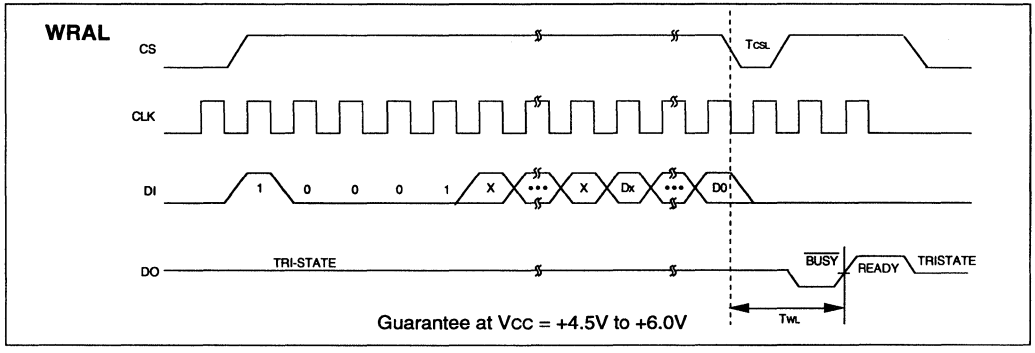


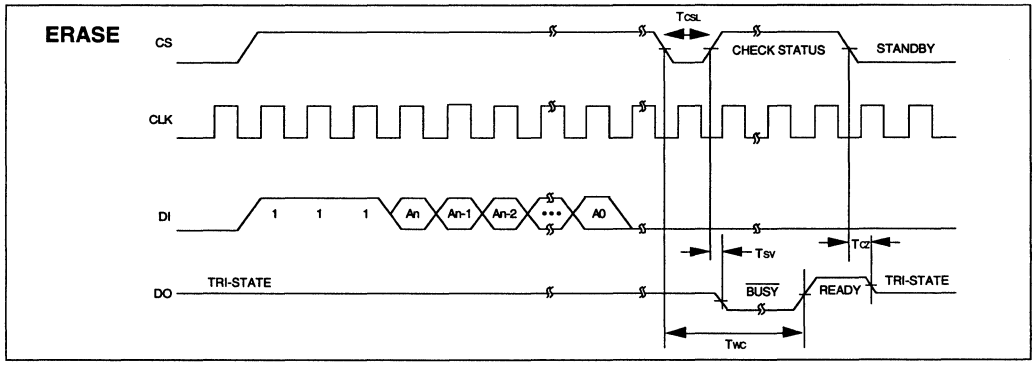
EWDS

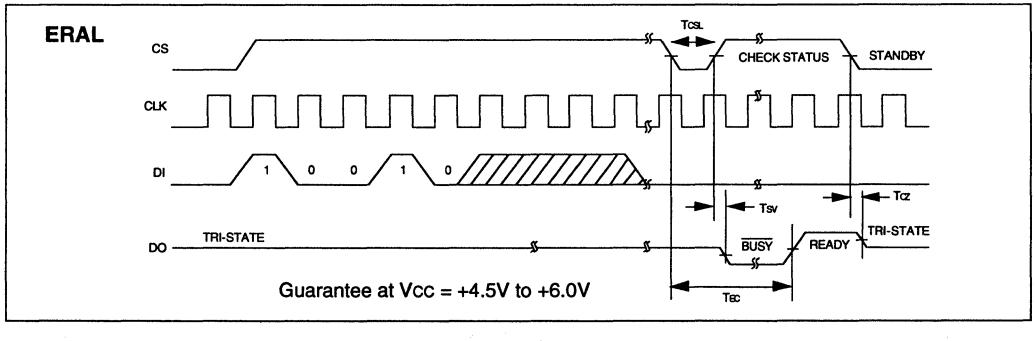


TIMING DIAGRAMS (Cont.)









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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

93LC46B/56B/66B - /P

PACKAGE:

P	PLASTIC DIP
SN	PLASTIC SOIC (150 mil Body) 8-Lead
SM	PLASTIC SOIC (207 mil Body) 8-Lead
SL	PLASTIC SOIC (150 mil Body) 14-Lead (93LC56B/93LC66B)

TEMPERATURE RANGE:

Blank	0°C to +70°C
I	-40°C to +85°C

DEVICE TYPE:

Configuration	
CMOS Serial EEPROM	93LC46B/56B/66B
CMOS Serial EEPROM In Alternate Pinouts (SN pkg. only)	93LC46BX/56BX/66BX
CMOS Serial EEPROM In Tape & Reel	93LC46BT/56BT/66BT
CMOS Serial EEPROM In Tape & Reel	93LC46BXT/56BXT/66BXT

93AA46/56/66

1K/2K/4K 1.8V CMOS Serial EEPROM

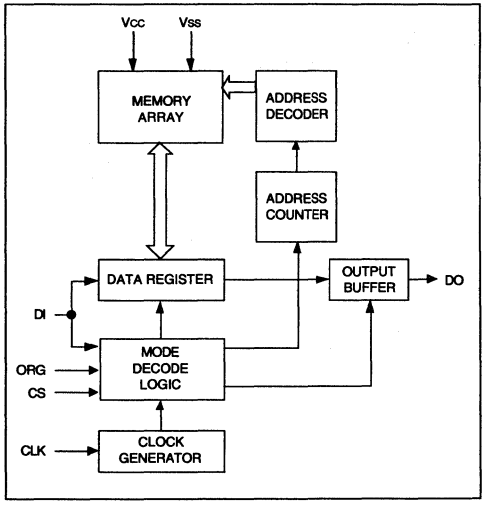
FEATURES

- Single supply with programming operation down to 1.8V
- Low power CMOS technology
  - 70 µA typical active READ current at 1.8V
  - 2 µA typical standby current at 1.8V
- ORG pin selectable memory configuration
  128 x 8 or 64 x 16 bit organization (93AA46)
  256 x 8 or 128 x 16 bit organization (93AA56)
  512 x 8 or 256 x 16 bit organization (93AA66)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8-pin PDIP/SOIC
  (SOIC in JEDEC and EIAJ standards)

DESCRIPTION

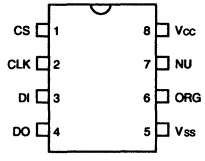
The Microchip Technology Inc. 93AA46/56/66 are 1K, 2K and 4K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. The 93AA Series is available in standard 8-pin DIP and surface mount SOIC packages. The rotated pin-out 93AA46X/56X/66X are offered in the "SN" package only.

BLOCK DIAGRAM



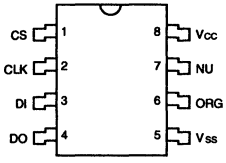
PIN CONFIGURATIONS

DIP Package

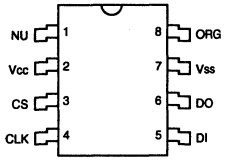


93AA46
93AA56
93AA66

SOIC Packages



93AA46
93AA56
93AA66



93AA46X
93AA56X
93AA66X

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS .... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
ORG	Memory Configuration
NU	Not Utilized
VCC	Power Supply

DC AND AC ELECTRICAL CHARACTERISTICS

VCC = +1.8V to +5.5V
Commercial (C): Tamb = 0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
High level input voltage	VIH1	2.0	—	VCC +1	V	VDD ≥ 2.5V
	VIH2	0.7 VCC	—	VCC +1	V	VDD < 2.5V
Low level input voltage	VIL1	-0.3	—	0.8	V	VDD ≥ 2.5V
	VIL2	-0.3	—	0.2 VCC	V	VDD < 2.5V
Low level output voltage	VOL1	—	—	0.4	V	IOL =2.1 mA; VCC = 4.5V
	VOL2	—	—	0.2	V	IOL =100 µA; VCC = 1.8V
High level output voltage	VOH1	2.4	—	—	V	IOH = -400 µA; VCC = 4.5V
	VOH2	VCC-0.2	—	—	V	IOH = -100 µA; VCC = 1.8V
Input leakage current	ILI	-10	—	10	µA	VIN = 0.1V to VCC
Output leakage current	ILO	-10	—	10	µA	VOUT = 0.1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	—	7	pF	VIN/VOUT = 0V (Note 1 & 2) Tamb = +25°C, FCLK = 1 MHz
Operating current	ICC write	—	—	3	mA	FCLK = 2 MHz; VCC = 5.5V (Note 2)
	ICC read	—	—	1	mA	FCLK = 2 MHz; VCC = 5.5V
				500	µA	FCLK = 1 MHz; VCC = 3.0V
			70		µA	FCLK = 1 MHz; VCC = 1.8V
Standby current	ICCS			100	µA	CLK = CS = 0V; VCC = 5.5V
				30	µA	CLK = CS = 0V; VCC = 3.0V
			2		µA	CLK = CS = 0V; VCC = 1.8V
Endurance	—	100,000	1,000,000		E/W Cycles	
Clock frequency	FCLK				MHz	VCC ≥ 4.5V
				2	MHz	VCC < 4.5V
Clock high time	TCKH	250		1	ns	
Clock low time	TCKL	250			ns	
Chip select setup time	TCSS	50			ns	Relative to CLK
Chip select hold time	TCSH	0			ns	Relative to CLK
Chip select low time	TCSL	250			ns	
Data input setup time	TDIS	100			ns	Relative to CLK
Data input hold time	TDIH	100			ns	Relative to CLK
Data output delay time	TPD			400	ns	CL = 100 pF
Data output disable time	TCZ			100	ns	CL = 100 pF (Note 2)
Status valid time	TSV			500	ns	CL = 100 pF
Program cycle time	TWC		4	10	ms	ERASE/WRITE mode
	TEC		8	15	ms	ERAL mode (VCC = 5V ± 10%)
	TWL		16	30	ms	WRAL mode (VCC = 5V ± 10%)

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
Note 2: This parameter is periodically sampled and not 100% tested.

INSTRUCTION SET FOR 93AA46: ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
EWEN	1	00	1 1 X X X X	—	High-Z	9
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	9
ERAL	1	00	1 0 X X X X	—	(RDY/$\overline{BSY}$)	9
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	25
WRAL	1	00	0 1 X X X X	D15 - D0	(RDY/$\overline{BSY}$)	25
EWDS	1	00	0 0 X X X X	—	High-Z	9

INSTRUCTION SET FOR 93AA46: ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	18
EWEN	1	00	1 1 X X X X X	—	High-Z	10
ERASE	1	11	A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	10
ERAL	1	00	1 0 X X X X X	—	(RDY/$\overline{BSY}$)	10
WRITE	1	01	A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	18
WRAL	1	00	0 1 X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	18
EWDS	1	00	0 0 X X X X X	—	High-Z	10

INSTRUCTION SET FOR 93AA56: ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X	—	High-Z	11

INSTRUCTION SET FOR 93AA56: ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X	—	High-Z	12

INSTRUCTION SET FOR 93AA66: ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

INSTRUCTION SET FOR 93AA66: ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

FUNCTIONAL DESCRIPTION

When the ORG pin is connected to Vcc, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V at nominal conditions.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

ERASE/WRITE ENABLE AND DISABLE

The 93AA46/56/66 power up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 4 ms per word typical.

WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.
The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 4 ms per word typical.

ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at 5V ± 10%.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The ERAL cycle takes 8 ms typical.

WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at 5V ± 10%.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The WRAL cycle takes 16 ms typical.

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93AAXX. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) and an ERASE or WRITE operation has been initiated.

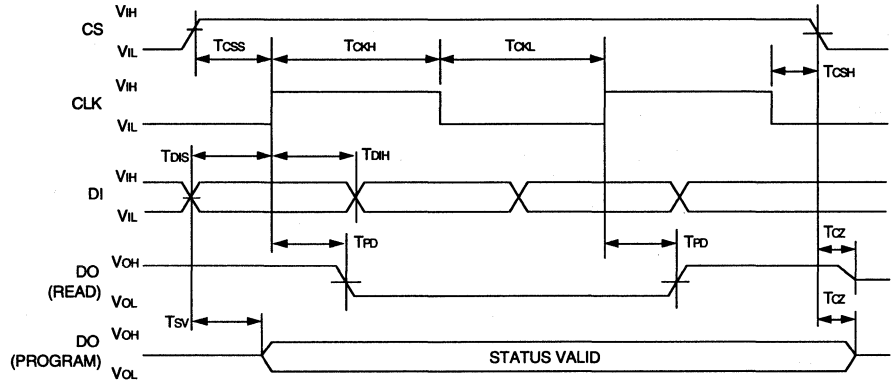
Organization (ORG)

When ORG is connected to VCC, the (x16) memory organization is selected. When ORG is tied to VSS, the (x8) memory organization is selected. ORG can only be floated for clock speeds of 1MHz or less for the (x16) memory organization. For clock speeds greater than 1 MHz, ORG must be tied to VCC or VSS.

5

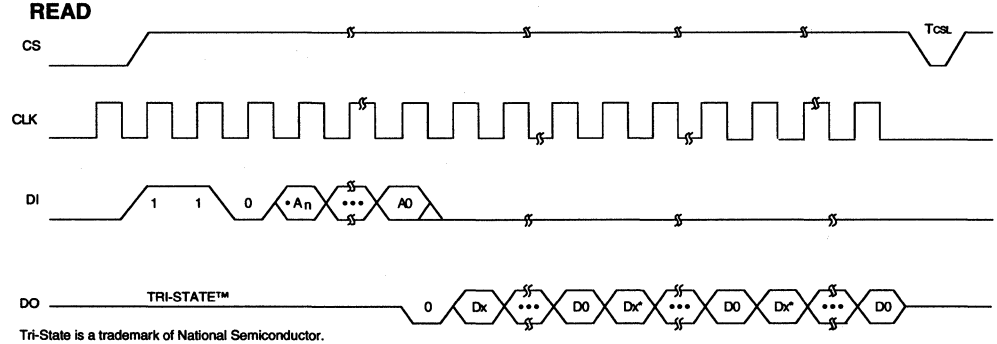
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



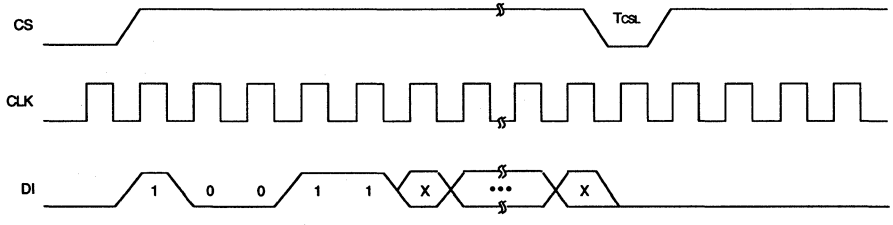
- The memory automatically cycles to the next register.

READ

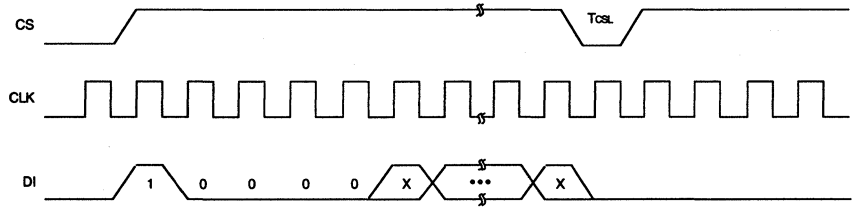


Tri-State is a trademark of National Semiconductor.

EWEN

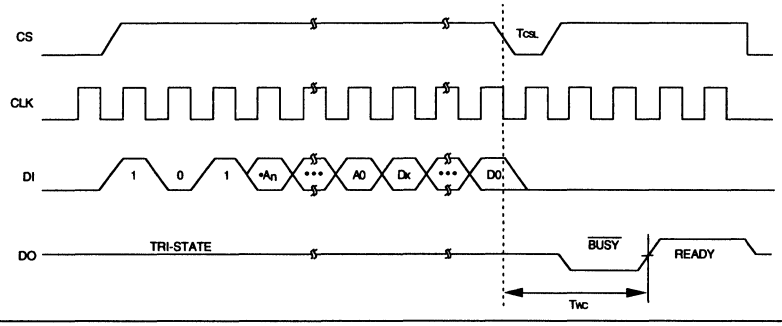


EWDS

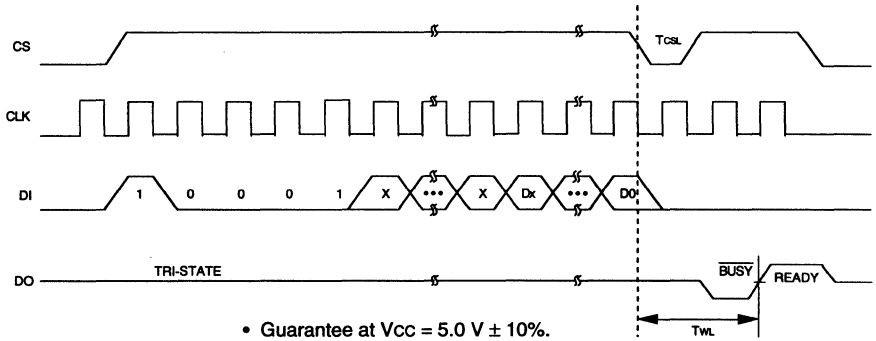


TIMING DIAGRAMS (Cont.)

WRITE

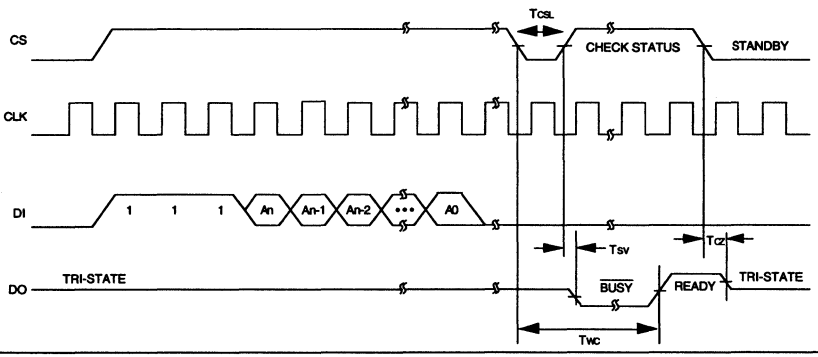


WRAL

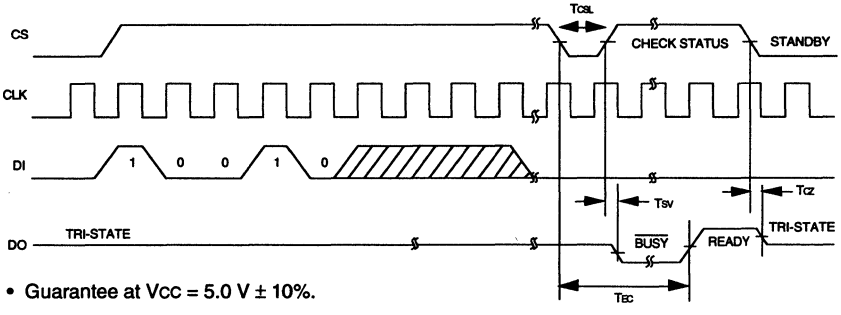


• Guarantee at Vcc = 5.0 V ± 10%.

ERASE



ERAL



• Guarantee at Vcc = 5.0 V ± 10%.

5

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

93AA46/56/66 - /P

PACKAGE:

P	PLASTIC DIP
SN	PLASTIC SOIC (150 mil Body) 8-Lead
SM	PLASTIC SOIC (207 mil Body) 8-Lead (93AA56/93AA66)

TEMPERATURE RANGE: Blank 0°C to +70°C

DEVICE TYPE:

Configuration	(x16) or (x8)
CMOS Serial EEPROM	93AA46/56/66
CMOS Serial EEPROM in alternate pinouts (SN package only)	93AA46X/56X/66X
CMOS Serial EEPROM (in Tape & Reel)	93AA46T/56T/66T
CMOS Serial EEPROM (in Tape & Reel)	93AA46XT/56XT/66XT

93LCS56/66

2K/4K 2.5V CMOS Serial EEPROM with Software Wire Protect

FEATURES

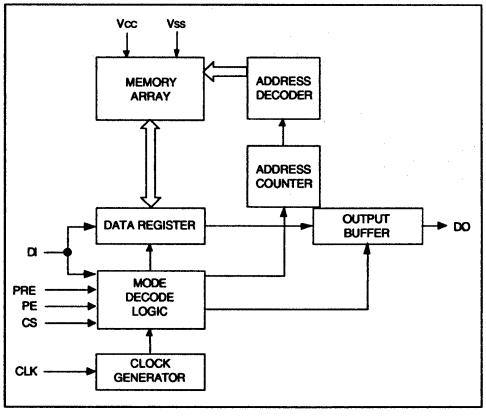
- Single supply with programming operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 5 µA standby current (typical) at 3.0V
- x16 memory organization
  - 128x16 (93LCS56)
  - 256x16 (93LCS66)
- Software write protection of user defined memory space
- Self timed erase and write cycles
- Automatic ERAL before WRAL
- Power on/off data protection
- Industry standard 3-wire serial I/O
- Device status signal during E/W
- Sequential READ function
- 1,000,000 E/W cycles (typical)
- Data retention > 40 years
- 8-pin PDIP/SOIC and 14-pin SOIC packages
- Commercial: 0°C to +70°C
- Industrial: 40°C to +85°C

DESCRIPTION

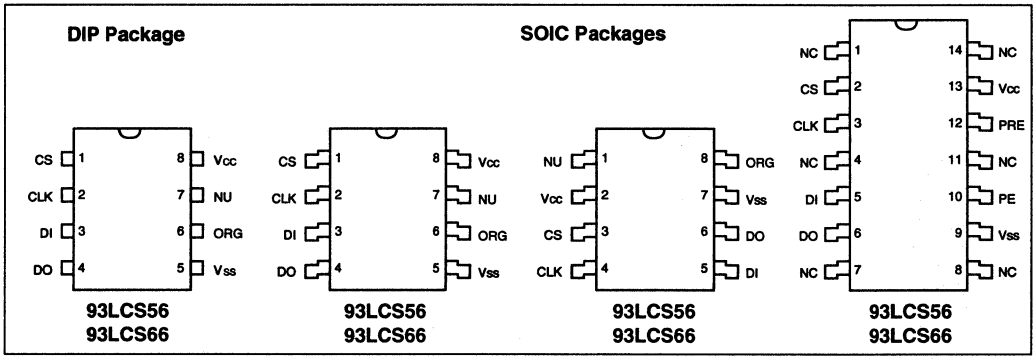
The Microchip Technology Inc. 93LCS56/66 are low voltage Serial Electrically Erasable PROMs with memory capacities of 2K bits/4K bits respectively. A write protect register is included in order to provide a user defined region of write protected memory. All memory locations greater than or equal to the address placed in the write protect register will be protected from any attempted write or erase operation. It is also possible to protect the address in the write protect register permanently by using a one time only instruction (PRDS). Any attempt to alter data in a register whose address is equal to or greater than the address stored in the protect register will be aborted. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications.

5

BLOCK DIAGRAM



PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
PE	Program Enable
PRE	Protect Register Enable
VCC	Power Supply

DC AND AC ELECTRICAL CHARACTERISTICS

VCC = +2.5V to +6.0V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min	Max	Units	Conditions
High level input voltage	VIH1	2.0	VCC +1	V	VDD ≥ 2.5V
	VIH2	0.7 VCC	VCC +1	V	VDD < 2.5V
Low level input voltage	VIL1	-0.3	0.8	V	VDD ≥ 2.5V
	VIL2	-0.3	0.2 VCC	V	VDD < 2.5V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 mA; VCC = 4.5V
	VOL2	—	0.2	V	IOL =100 µA; VCC = 2.5V
High level output voltage	VOH1	2.4	—	V	IOH = -400 µA; VCC = 4.5V
	VOH2	VCC-0.2	—	V	IOH = -100 µA; VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to VCC
Internal capacitance	CINT	—	7	pF	VIN/VOUT = 0V (Note 1 & 3)
(all inputs/outputs)					Tamb = +25°C, FCLK = 1 MHz
Operating current	ICC write	—	3	mA	FCLK = 2 MHz; VCC = 3.0V (Note 3)
	ICC read	—	1	mA	FCLK = 2 MHz; VCC = 6.0V
			500	µA	FCLK = 1 MHz; VCC = 3.0V
Standby current	ICCS	—	100	µA	CLK = CS = 0V; VCC = 6.0V
			30	µA	CLK = CS = 0V; VCC = 3.0V
Endurance	—	100,000	—	E/W Cycles	1,000,000 E/W cycles typical
Clock frequency	FCLK	—	2	MHz	VCC ≥ 4.5V
			1	MHz	VCC < 4.5V
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	250	—	ns	
PRE setup time	TPRES	100	—	ns	Relative to CLK
PE setup time	TPES	100	—	ns	Relative to CLK
PRE hold time	TPREH	0	—	ns	Relative to CLK
PE hold time	TPEH	500	—	ns	Relative to CLK
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time	TCZ	—	100	ns	CL = 100 pF (Note 3)

DC AND AC ELECTRICAL CHARACTERISTICS (CONTINUED)			Vcc = +2.5V to +6.0V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Status valid time	TSV		500	ns	CL = 100 pF
Program cycle time	TWC		10	ms	ERASE/WRITE mode (Note 2)
	TEC		15	ms	ERAL mode
	TWL		30	ms	WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
Note 2: Typical program cycle time is 4 ms per word.
Note 3: This parameter is periodically sampled and not 100% tested.

INSTRUCTION SET FOR 93LCS56*/66

93LCS56/66 (x 16 organization)								
Instruction	**SB**	**Opcode**	**Address**	**Data In**	**Data Out**	**PRE**	**PE**	**Comments**
READ	1	10	A7 - A0*	—	D15 - D0	0	X	Reads data stored in memory, starting at specified address.
EWEN	1	00	11XXXXXX	—	High-Z	0	1	Erase/Write Enable must precede all programming modes.
ERASE	1	11	A7 - A0*	—	(RDY/$\overline{BSY}$)	0	1	Erase data at specified address location if address is unprotected.
ERAL	1	00	10XXXXXX	—	(RDY/$\overline{BSY}$)	0	1	Erase all registers to "FF". Valid only when Protect Register is cleared.
WRITE	1	01	A7 - A0*	D15 - D0	(RDY/$\overline{BSY}$)	0	1	Writes register if address is unprotected.
WRAL	1	00	01XXXXXX	D15 - D0	(RDY/$\overline{BSY}$)	0	1	Writes all registers. Valid only when Protect Register is cleared.
EWDS	1	00	00XXXXXX	—	High-Z	0	X	Erase/Write Disable deactivates all programming instructions.
PRREAD	1	10	XXXXXXXX	—	A7 - A0	1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX	—	High - Z	1	1	Must immediately precede PRCLEAR, PRWRITE and PRDS instructions.
PRCLEAR	1	11	11111111	—	(RDY/$\overline{BSY}$)	1	1	Clears the Protect Register such that all data are NOT write-protected.
PRWRITE	1	01	A7 - A0*	—	(RDY/$\overline{BSY}$)	1	1	Programs address into Protect Register. Thereafter, memory addresses greater than or equal to the address in Protect Register are write-protected.
PRDS	1	00	00000000	—	(RDY/$\overline{BSY}$)	1	1	ONE TIME ONLY instruction after which the address in the Protect Register cannot be altered.

*Address A7 bit is a "don't care" ON 93LCS56.

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FUNCTIONAL DESCRIPTION

The 93LCS56/66 is organized as 128/256 registers by 16 bits. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the ready/busy status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, WRAL, PRREAD, PREN, PRCLEAR, PRWRITE, and PRDS). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

ERASE/WRITE ENABLE AND DISABLE

The 93LCS56/66 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. The PE pin MUST be held "high" while loading the EWEN instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle. The PE pin MUST be latched "high" during loading the ERASE instruction but becomes a "don't care" after loading the instruction.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction. ERASE instruction is valid if specified address is unprotected.

The ERASE cycle takes 4 ms per word typical.

WRITE

The WRITE instruction is followed by 16 bits of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle. The PE pin MUST be latched "high" while loading the WRITE instruction but becomes a "don't care" thereafter.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction. WRITE instruction is valid only if specified address is unprotected.

The WRITE cycle takes 4 ms per word typical.

ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1". The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. PE pin MUST be held "high" while loading the instruction but becomes "don't care" thereafter. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at VCC = 4.5 to 6V and valid only when Protect Register is cleared.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The ERAL cycle takes 15 ms maximum (8 ms typical).

WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. PE pin MUST be held "high" while loading the instruction but becomes "don't care" thereafter. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at VCC = 4.5 to 6V and valid only when Protect Register is cleared.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The WRAL cycle takes 30 ms maximum (16 ms typical).

Note: In order to execute either READ, EWEN, ERAL, WRITE, WRAL, or EWDS instructions, the Protect Register Enable (PRE) pin must be held LOW.

PROTECT REGISTER READ

The Protect Register Read (PRREAD) instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin MUST be held HIGH when loading the instruction and remains HIGH until CS goes LOW. A dummy zero bit precedes the 8-bit output string. The output data bits in the memory Protect Register will toggle on the rising edge of the CLK as in the READ mode.

PROTECT REGISTER ENABLE

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the device must be in the EWEN mode. Both PRE and PE pins MUST be held "high" while loading the instruction. The PREN instruction MUST immediately precede a PRCLEAR, PRWRITE, or PRDS instruction.

PROTECT REGISTER CLEAR

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables all registers for programming instructions such as ERASE, ERAL, WRITE, and WRAL. The PRE and PE pin MUST be held HIGH when loading the instruction. Thereafter, PRE and PE pins become "don't care". A PREN instruction must immediately precede a PRCLEAR instruction.

PROTECT REGISTER WRITE

The Protect Register Write (PRWRITE) instruction writes into the Protect Register the address of the first register to be protected. After this instruction is executed, all registers whose memory addresses are greater than or equal to the address pointer specified in the Protect register are protected from any programming instructions. Note that a PREN instruction must be executed before a PRWRITE instruction and, the Protect Register must be cleared (by a PRCLEAR instruction) before executing the PRWRITE instruction. The PRE and PE pins MUST be held HIGH while loading PRWRITE instruction. After the instruction is loaded, they become "don't care".

PROTECT REGISTER DISABLE

The Protect Register Disable (PRDS) instruction is a ONE TIME ONLY instruction to permanently set the address specified in the Protect Register. Any attempts to change the address pointer will be aborted. The PRE and PE pins MUST be held HIGH while loading PRDS instruction. After the instruction is loaded, they become "don't care". Note that a PREN instruction must be executed before a PRDS instruction.

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PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93LCS56/66. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ and PRREAD mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after held LOW for minimum chip select low time (TCSL) and an ERASE or WRITE operation has been initiated.

Program Enable (PE)

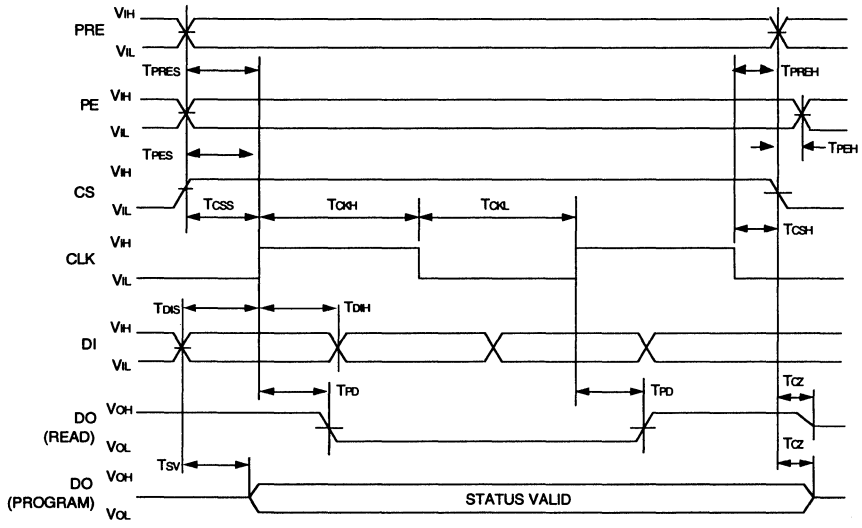
This pin should be held HIGH in the programming mode or when executing the Protect Register programming instructions.

Protect Register Enable (PRE)

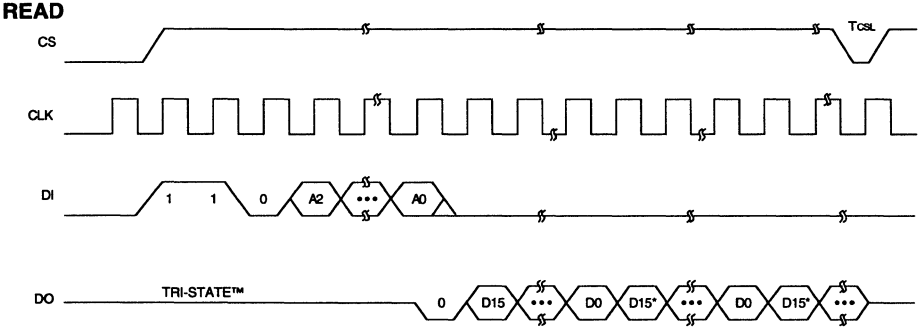
This pin should be held HIGH when executing all Protect Register instructions. Otherwise, it must be held LOW for normal operations.

TIMING DIAGRAMS (Cont.)

SYNCHRONOUS DATA TIMING

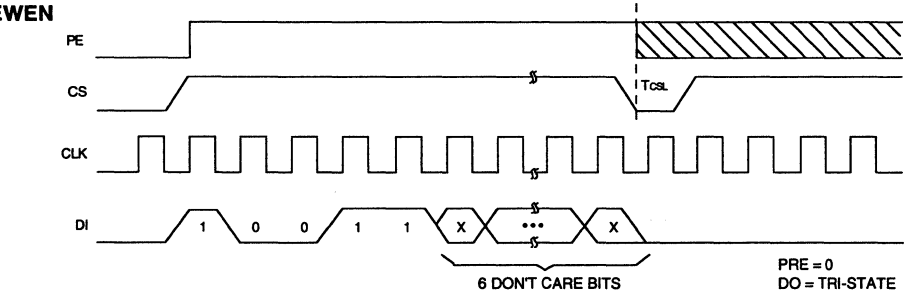


READ



* The memory automatically cycles to the next register. PRE = 0
Tri-State is a trademark of National Semiconductor. PE = X

EWEN



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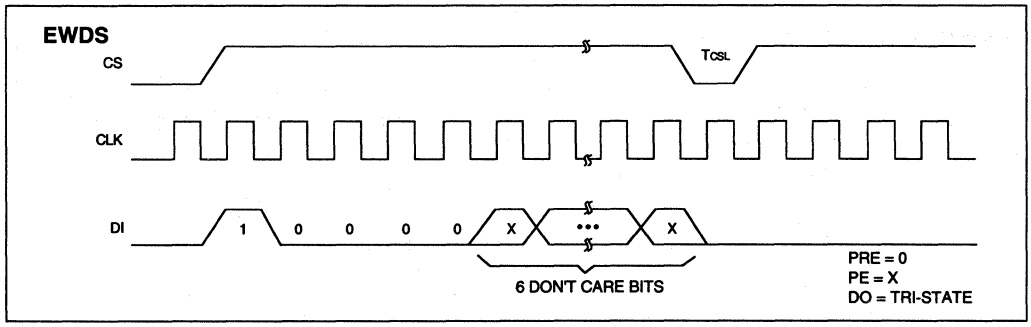
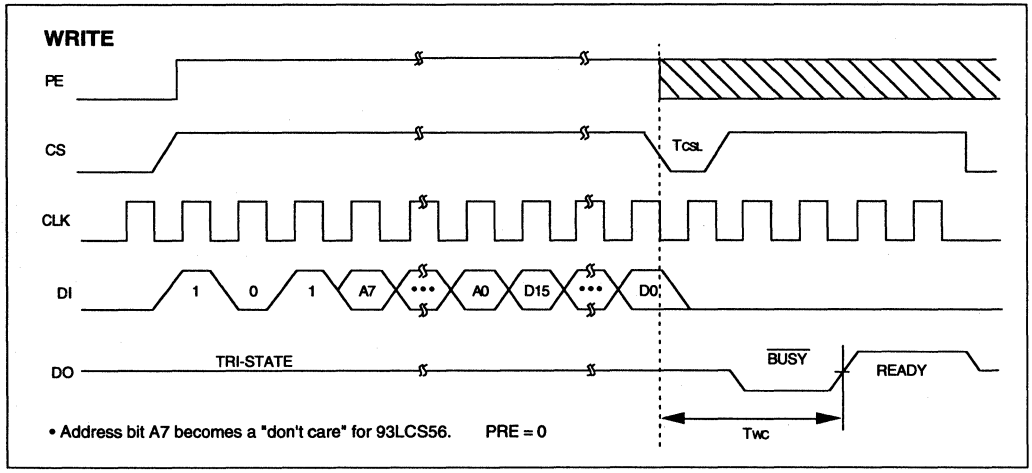
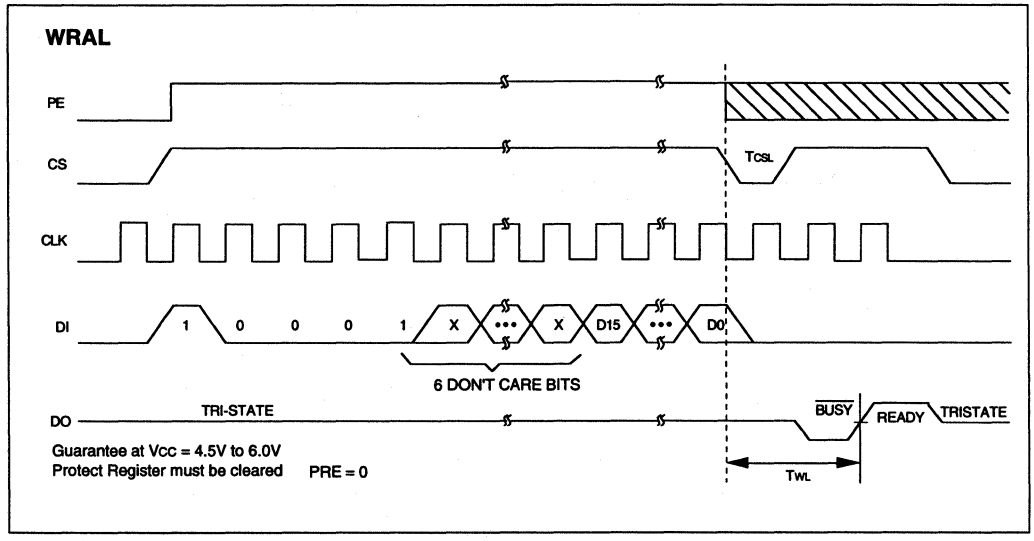
TIMING DIAGRAMS (Cont.)

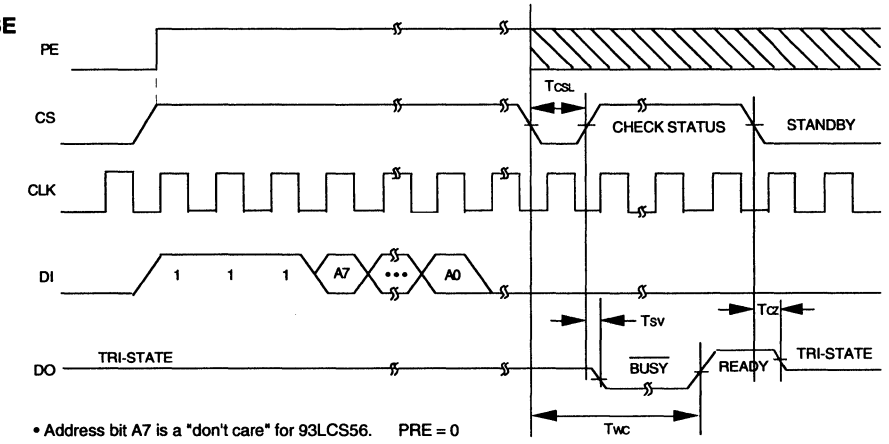






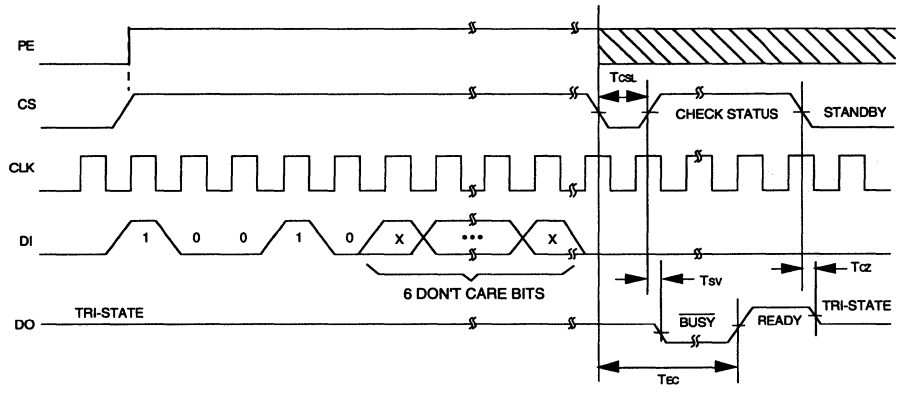
TIMING DIAGRAMS (Cont.)

ERASE



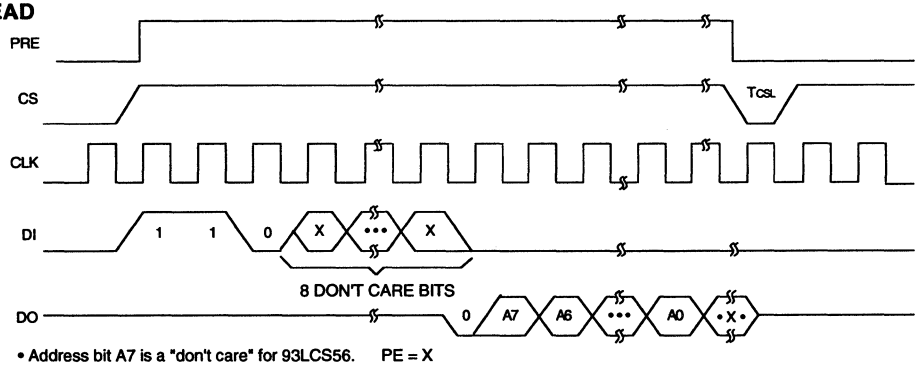
• Address bit A7 is a "don't care" for 93LCS56. PRE = 0

ERAL

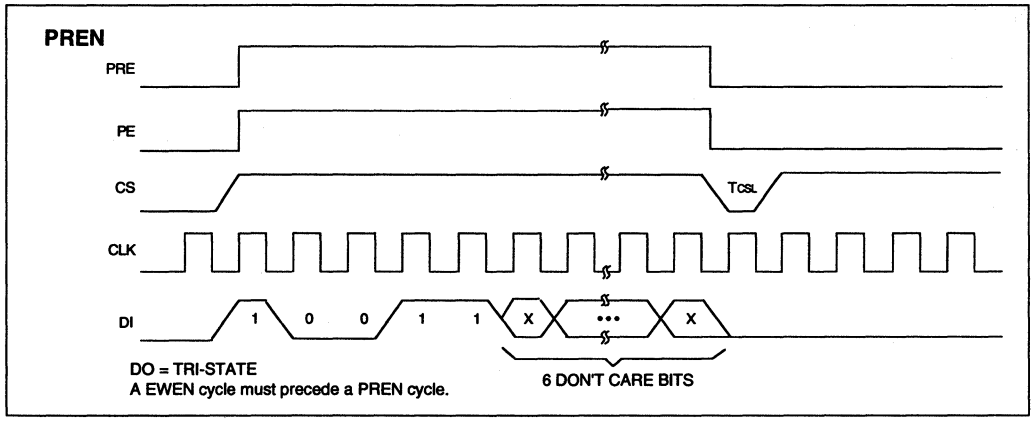


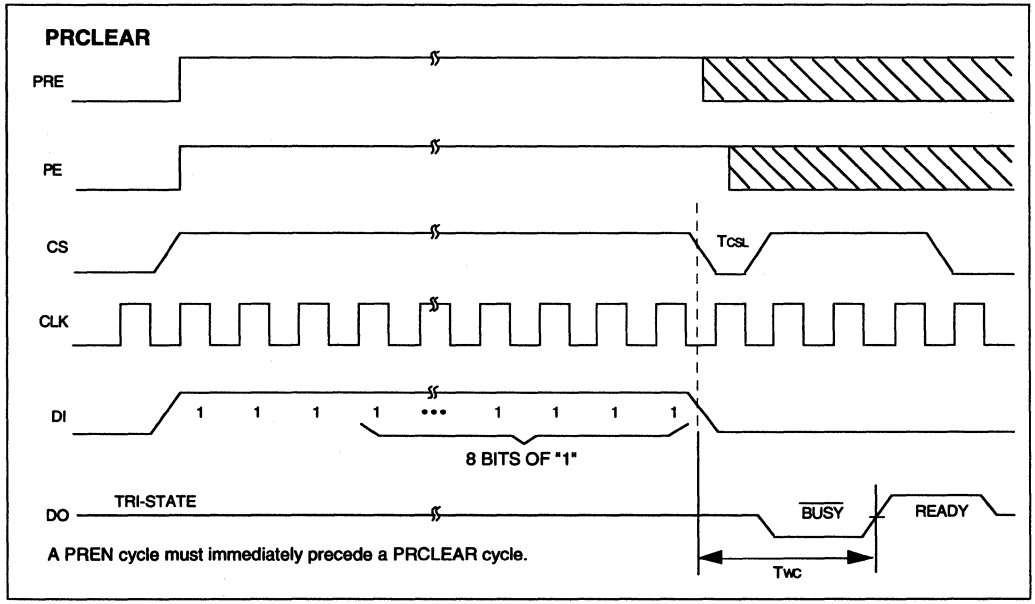
Guarantee at V_{CC} = 4.5V to 6.0V
PRE = 0 Protect Register must be cleared

PRREAD

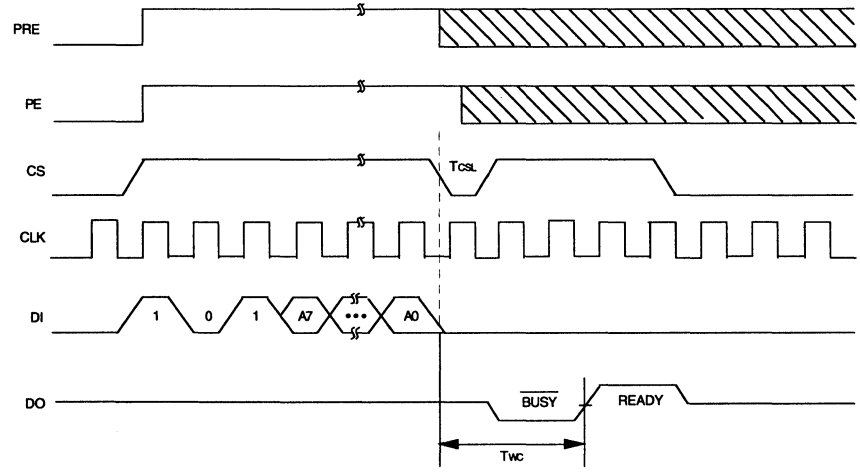


• Address bit A7 is a "don't care" for 93LCS56. PE = X





PRWRITE



Protect Register MUST be cleared before a PRWRITE cycle.
A PREN cycle must immediately precede a PRWRITE cycle.
Address bit A7 is a "don't care" for 93LCS56.

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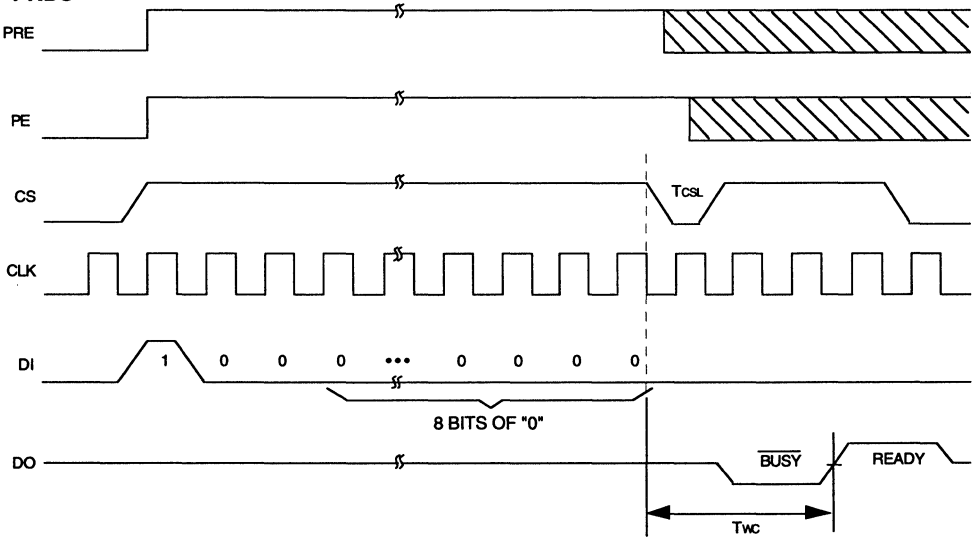
PRDS



ONE TIME ONLY instruction. A PREN cycle must immediately precede a PRDS cycle.

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

93LCS56/66 - /P

PACKAGE:

P	PLASTIC DIP
SN	PLASTIC SOIC (150 mil Body) 8-Lead
SM	PLASTIC SOIC (207 mil Body) 8-Lead
SL	PLASTIC SOIC (150 mil Body) 14-Lead

TEMPERATURE RANGE:

Blank	0°C to +70°C
I	-40°C to +85°C

DEVICE TYPE:

Configuration	(x16)
CMOS Serial EEPROM	93LCS56
CMOS Serial EEPROM in alternate pinouts (SN package only)	93LCS56X
CMOS Serial EEPROM (in Tape & Reel)	93LCS56T
CMOS Serial EEPROM (in Tape & Reel)	93LCS56XT
CMOS Serial EEPROM	93LCS66
CMOS Serial EEPROM	93LCS66X
CMOS Serial EEPROM (in Tape & Reel)	93LCS66T
CMOS Serial EEPROM (in Tape & Reel)	93LCS66XT

Serial EEPROM Cross Reference Guide

The purpose of this document is to provide a quick way to determine which Serial EEPROM parts are basically equivalent to which Microchip devices. The cross reference section is broken down by manufacturer and lists all parts from that manufacturer , and the comparable Microchip part number.

There are subtle differences from manufacturer to manufacturer and device to device, so Microchip recommends consulting the respective manufacturer's databook for specific details.

Microchip provides a wide selection of Serial EEPROM devices, both from a density and a packaging standpoint, as well as several different protocols. If you are interested in a part that is not listed in this book , please refer to the Microchip data book, or contact your local distributor or sales representative for assistance.

The manufacturers included in this document are as follows:

AKM
Atmel
Catalyst
Exel
ISSI
Microchip
Mitsubishi
National
Oki
Philips
Samsung
SGS-Thomson
Siemens
Xicor

Serial EEPROM

Manufacturer	Part Number	Closest Microchip Equivalent	Size
AKM	AK93C45	93C46	1K
AKM	AK93C45L	93C46	1K
AKM	AK93C55	93LC56	2K
AKM	AK93C55L	93AA56	2K
AKM	AK93C57	93LC56	2K
AKM	AK6420	93LC56	2K
AKM	AK93C65	93LC66	4K
AKM	AK93C65L	93AA66	4K
AKM	AK93C67	93LC66	4K
AKM	AK6420	93LC66	4K
ATMEL	AT24C01A	24LC01B/ 24C01A	1K
ATMEL	AT24C01A-2.7	24LC01B	1K
ATMEL	AT24C01A-2.5	24LC01B	1K
ATMEL	AT24C01A-1.8	24AA01	1K
ATMEL	AT59C11	59C11	1K
ATMEL	AT59C11-2.7	59C11	1K
ATMEL	AT59C11-2.5	59C11	1K
ATMEL	AT59C11-1.8	59C11	1K
ATMEL	AT93C46	93C46	1K
ATMEL	AT93C46-2.7	93LC46	1K
ATMEL	AT93C46-2.5	93LC46	1K
ATMEL	AT93C46-1.8	93LC46	1K
ATMEL	AT93C56	93C56	2K
ATMEL	AT93C56-2.7	93LC56	2K
ATMEL	AT93C56-2.5	93LC56	2K
ATMEL	AT93C56-1.8	93AA56	2K
ATMEL	AT93C57	93C56	2K
ATMEL	AT93C57-2.7	93LC56	2K
ATMEL	AT93C57-2.5	93LC56	2K
ATMEL	AT93C57-1.7	93AA56	2K
ATMEL	AT24C02	24C02/ 24LC02B	2K
ATMEL	AT24C02-2.7	24LC02B	2K
ATMEL	AT24C02-2.5	24LC02B	2K
ATMEL	AT24C02-1.8	24AA02	2K
ATMEL	AT93C66	93C66	4K
ATMEL	AT93C66-2.7	93LC66	4K
ATMEL	AT93C66-2.5	93LC66	4K
ATMEL	AT93C66-1.8	93AA66	4K
ATMEL	AT24C04	24C04/ 24LC04B	4K

Manufacturer	Part Number	Closest Microchip Equivalent	Size
ATMEL	AT24C04-2.7	24LC04B	4K
ATMEL	AT24C04-2.5	24LC04B	4K
ATMEL	AT24C04-1.8	24AA04	4K
ATMEL	AT24C08	24LC08B	8K
ATMEL	AT24C08-2.7	24LC08B	8K
ATMEL	AT24C08-2.5	24LC08B	8K
ATMEL	AT24C08-1.8	24AA08	8K
ATMEL	AT24C16	24LC16B	16K
ATMEL	AT24C16-2.7	24LC16B	16K
ATMEL	AT24C16-2.5	24LC16B	16K
ATMEL	AT24C16-1.8	24AA16	16K
ATMEL	AT24C164	24LC164*	16K
ATMEL	AT24C164-2.7	24LC164*	16K
ATMEL	AT24C164-2.5	24LC164*	16K
ATMEL	AT24C164-1.8	24AA164*	16K
Catalyst	CAT59C11/I/A/AI/H	59C11	1K
Catalyst	CAT33C101C/I	93LC46	1K
Catalyst	CAT33C101	93LC46	1K
Catalyst	CAT93C46/I/H	93LC46	1K
Catalyst	CAT93C46AI/H	93LC46	1K
Catalyst	CAT35C102H/I	93C56	2K
Catalyst	CAT93C56/I	93C56	2K
Catalyst	CAT93LC56/I	93LC56	2K
Catalyst	CAT24C02/I	24C02B/ 24LC02B	2K
Catalyst	CAT24LC02/I	24LC02B	2K
Catalyst	CAT24C04.1	24C04A/ 24LC04B	4K
Catalyst	CAT24LC04.1	24LC04B	4K
Catalyst	CAT35C104/H/I	93C66	4K
Catalyst	CAT33C104	93LC66	4K
Catalyst	CAT35C704/I	93C66	4K
Catalyst	CAT33C704/I	93LC66	4K
Catalyst	CAT35C80	93C66	4K
Catalyst	CAT33C80	93LC66	4K
Catalyst	CAT24C08	24LC08B	8K
Catalyst	CAT24LC08	24LC08B	8K
Catalyst	CAT24C16	24LC16B	16K
Catalyst	CAT24LC16	24LC16B	16K
Exel	XL93LC06	93C06	256 bit
Exel	XL24C01A	24C01A/ 24LC01B	1K

* Release mid 1994

Manufacturer	Part Number	Closest Microchip Equivalent	Size
Exel	XL24C01-2.5	24LC01B	1K
Exel	XL93C CS LC 46	93C46	1K
Exel	XL93C CS LC 46-3	93LC46	1K
Exel	XL24C01A-3	24LC01B	1K
Exel	XL24C02	24C02A/ 24LC02B	2K
Exel	XL24C02-3	24LC02B	2K
Exel	XL93C56,LC56	93C56/ LC56	2K
Exel	XL24C01-2.5	24LC02B	2K
Exel	XL93LC56-3	93LC56	2K
Exel	XL93C66,LC66	93C66/ 93LC66	4K
Exel	XL93C66-3,LC66-3	93LC66	4K
Exel	XL24C04	24C04A/ 24LC04B	4K
Exel	XL24C04-3	24LC04B	4K
Exel	XL24C04-2.5	24LC04B	4K
Exel	XL24C16	24LC16B	16K
Exel	XL24C16-3	24LC16B	16K
ISSI	IS93C46	93C46	1K
ISSI	IS93C46-3	93LC46	1K
ISSI	IS93C56	93C56	2K
ISSI	IS93C66	93C66	4K
National	NM93C06	93C06	256 bit
National	NM93C46	93C46	1K
National	NM93C46LZ	93AA46	1K
National	NM93C56	93C56	2K
National	NM93C56LZ	93AA56	2K
National	NM93CS56	93LCS56	2K
National	NM93CS56L	93LCS56	2K
National	NM24C02	24C02A/ 24LC02B	2K
National	NM24C02L	24LC02B	2K
National	NM24C03	24C02A	2K
National	NM24C03L	24LC02B	2K
National	NM93C66	93C66	4K
National	NM93CS66	93LCS66	4K
National	NM93C66L	93LC66	4K
National	NM93CS66L	93LCS66	4K
National	NM93C66LZ	93AA66	4K
National	NM24C04	24C04A/ 24LC04B	4K
National	NM24C04L	24LC04B	4K
National	NM24C05L	24LC04B	4K
National	NM24C08	24LC08B	8K
National	NM24C08L	24LC08B	8K
National	NM24C09	24LC08B	8K
National	NM24C09L	24LC08B	8K
National	NM24C16	24LC16B	16K
National	NM24C16L	24LC16B	16K
National	NM24C17	24LC16B	16K
National	NM24C17L	24LC16B	16K
Oki	MSM16812	93C56	2K
Phillips-Signetics	PCA8581	24C01A	1K
Phillips-Signetics	PCF8582C2	85C82	2K
Phillips-Signetics	PCD8582D2	85C82	2K
Phillips-Signetics	PCF8582F2	85C82	2K
Phillips-Signetics	PCF8594C-2	24AA04	4K
Phillips-Signetics	PCD8594D-2	24LC04B	4K
Phillips-Signetics	PCF8598C-2	24LC08B	8K
Phillips-Signetics	PCD8598D-2	24LC08B	8K
Phillips-Signetics	PCD85898F-2	24LC08B	8K
Samsung	KM93C06	93C06	256 bit
Samsung	KM93C07	93C06	256 bit
Samsung	KM93C46	93C46	1K
Samsung	KM94C46V	93C46	1K
Samsung	KM93C56	93C56	2K
Samsung	KM93CS56	93LCS56	2K
Samsung	KM93C56V	93AA56	2K
Samsung	KM93C57	93C56	2K
Samsung	KM93C57V	93AA56	2K
Samsung	KM93C66	93C66	4K
Samsung	KM93CS66	93LCS66	4K
Samsung	KM93C66V	93AA66	4K
Samsung	KM93C67	93C66	4K
Samsung	KM93C67V	93AA66	4K
SEEQ	2913A	93C46	1K

Manufacturer	Part Number	Closest Microchip Equivalent	Size
SEEQ	2913C	93C46	1K
SEEQ	2914A	93C46	1K
SEEQ	2919G	93C46	1K
SEEQ	2922A	93LC56	2K
SEEQ	2929G	93LC56	2K
SEEQ	2934A	93LC66	4K
SEEQ	2929G	93LC66	4K
SGS-Thomson	ST93C06	93C06	256 bit
SGS-Thomson	ST24C01	24LC01B	1K
SGS-Thomson	ST93C46A	93C46	1K
SGS-Thomson	ST93C46T	93C46	1K
SGS-Thomson	ST93C46	93LC46	1K
SGS-Thomson	ST24W01	24LC01B	1K
SGS-Thomson	ST25W01	24LC01B	1K
SGS-Thomson	ST93C56	93C56	2K
SGS-Thomson	ST93CS56	93LCS56	2K
SGS-Thomson	ST93CS57	93LCS56	2K
SGS-Thomson	ST24C02A	24LC02B	2K
SGS-Thomson	ST24C02C	24LC02B	2K
SGS-Thomson	ST24W02C	24LC02B	2K
SGS-Thomson	ST25C02A	24LC02B	2K
SGS-Thomson	ST25W02C	24LC02B	2K
SGS-Thomson	ST93CS66	93LCS66	4K
SGS-Thomson	ST93CS67	93LCS66	4K
SGS-Thomson	ST24C04	24C04A/ 24LC04B	4K
SGS-Thomson	ST24C04C	24LC04B	4K
SGS-Thomson	ST24W04C	24LC04B	4K
SGS-Thomson	ST25C04	24LC04B	4K
SGS-Thomson	ST25C0RC	24LC04B	4K
SGS-Thomson	ST25W04C	24LC04B	4K
SGS-Thomson	ST24C08	24LC08B	8K
SGS-Thomson	ST24C08C	24LC08B	8K
SGS-Thomson	ST25CO8C	24LC08B	8K
SGS-Thomson	ST24C16C	24LC16B	16K
SGS-Thomson	ST24E16C	24LC16B	16K
SGS-Thomson	ST25C16C	24LC16B	16K
SGS-Thomson	ST25E16C	24LC16B	16K
Siemens	SDA2516-2	24C01A/ 24LC01B	1K
Siemens	SDA2526-2	24C02A/ 24LC02B	2K
Siemens	SDA2546	24C04A/ 24LC04B	4K
Siemens	SDA2586	24LC08B	8K
Xicor	X24C01A	24LC01B	1K
Xicor	X2402	24C02A	2K
Xicor	X24C02	24LC02B	2K
Xicor	X2404	24C04A/ 24LC04B	4K
Xicor	X24C04	24LC04B	4K
Xicor	X24C08	24LC08B	8K
Xicor	X24C16	24LC16B	16K

SECTION 6
PARALLEL EEPROM PRODUCT SPECIFICATIONS

Parallel EEPROMs

Parallel EEPROM Selection Guide

CMOS Parallel EEPROMs

Device	Density/ Organization	Access Time (ns)	Icc (Active/ Standby)	Byte Write Time	Endur-ance (cycles)*	Temp Range	# Pins	Package Types	Operating Voltage
28C04A	4K bits (512 x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C, I	24,32	P,J,L	4.5V - 5.5V
28C16A	16K bits (2K x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C, I	24,28,32	P,J,TS,VS,L	4.5V - 5.5V
28C17A	16K bits (2K x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C, I	28,32	P,J,SO,TS,VS,L	4.5V - 5.5V
28C64A	64K bits (8K x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C, I	28,32	P,J,SO,TS,VS,L	4.5V - 5.5V
28C64AX	64K bits (8K x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C, I	28,32	P,J,SO,TS,VS,L	4.5V - 5.5V
28C04AF	4K bits (512 x 8)	150/200/250	30 mA/100 µA	200 µs	10K	C, I	24,32	P,J,L	4.5V - 5.5V
28C16AF	16K bits (2K x 8)	150/200/250	30 mA/100 µA	200 µs	10K	C, I	24,28,32	P,J,TS,VS,L	4.5V - 5.5V
28C17AF	16K bits (2K x 8)	150/200/250	30 mA/100 µA	200 µs	10K	C, I	28,32	P,J,SO,TS,VS,L	4.5V - 5.5V
28C64AF	64K bits (8K x 8)	150/200/250	30 mA/100 µA	200 µs	10K	C, I	28,32	P,J,SO,TS,VS,L	4.5V - 5.5V

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PACKAGES

P = Plastic DIP
SN = .150" 8ld SOIC
S = Dice in Wafflepack
J = Ceramic DIP
SM = .207" 8ld SOIC
L = PLCC
SL = .150" 14ld SOIC
W = Dice in Wafer Form
VS = 28ld VSOP (8x13.4mm)
K = Ceramic LCC
SO = .300" 28ld SOIC
TS = 28ld TSOP (8x20mm)

* Endurance is guaranteed to 10K cycles at extended (-40°C to +125°C) temperature.

NOTE: NOT ALL COMBINATIONS OF SPEED/TEMPERATURE RANGE/PACKAGE/ETC. ARE AVAILABLE. CONSULT FACTORY FOR SPECIFIC PART INFORMATION.

MICROCHIP

28C04A

4K (512 x 8) CMOS EEPROM

FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - — 30 mA Active
  - — 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >10 years
- Endurance - Minimum 10^4 Erase/Write Cycles
- Automatic Write Operation
  - — Internal Control Timer
  - — Auto-Clear Before Write Operation
  - — On-Chip Address and Data Latches
- $\overline{\text{Data}}$ Polling
- Chip Clear Operation
- Enhanced Data Protection
  - — Vcc Detector
  - — Pulse Filter
  - — Write Inhibit
- 5-Volt-Only Operation
- Organized 512x8 JEDEC standard pinout
  - — 24-pin Dual-In-Line Package
  - — 32-pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  - — Commercial: 0°C to 70°C
  - — Industrial: -40°C to 85°C

DESCRIPTION

The Microchip Technology Inc. 28C04A is a CMOS 4K non-volatile electrically Erasable and Programmable Read Only Memory (EEPROM). The 28C04A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C04A uses $\overline{\text{Data}}$ polling. $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

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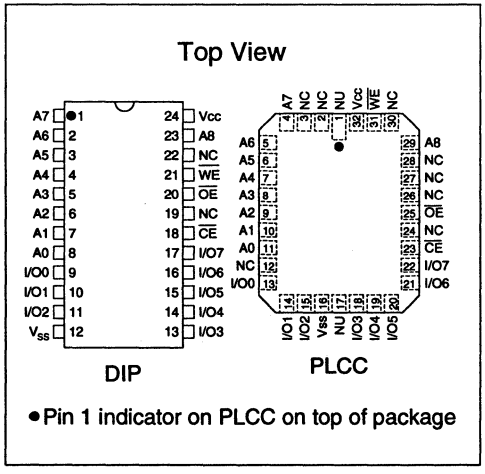
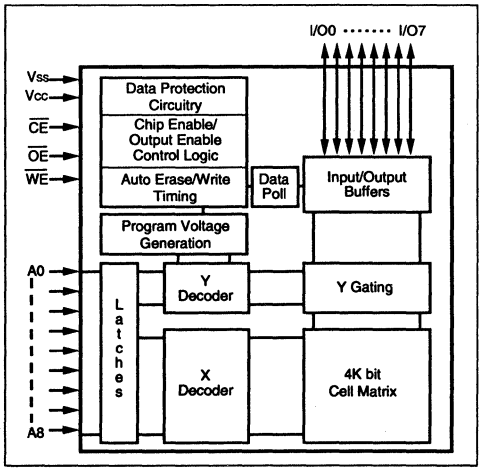
PIN CONFIGURATION



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS
MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss..... -0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. Vss..... -0.6V to +13.5V
Output Voltage w.r.t. Vss..... -0.6V to Vcc+0.6V
Storage temperature ..... -65°C to 125°C
Ambient temp. with power applied ..... -50°C to 95°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0 - A8	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

READ / WRITE OPERATION
DC Characteristics

Vcc = +5V ±10%
Commercial (C): Tamb= 0°C to 70°C
Industrial (I): Tamb= -40°C to 85°C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = -0.1V to Vcc+1
Input Capacitance		CIN		10	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage		ILO	-10	10	µA	VOUT = -0.1V to Vcc+0.1V
Output Capacitance		COUT		12	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	ICC		30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	$\overline{CE}$ = VIH (0°C to 70°C) $\overline{CE}$ = VIH (-40°C to 85°C) CE = Vcc-0.3 to Vcc+1

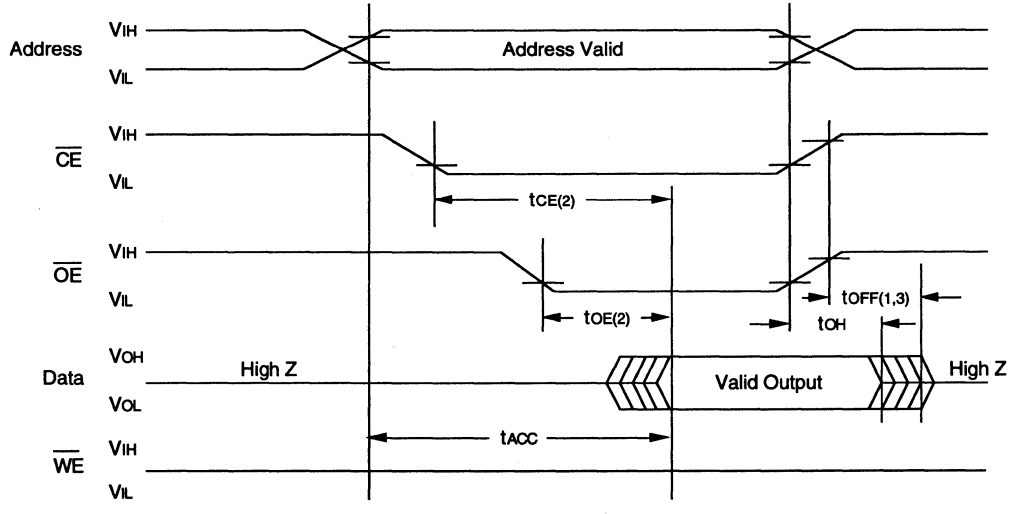
Note: (1) AC power supply current above 5 MHz: 1 mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 ns
Ambient Temperature: Commercial (C): Tamb = 0°C to 70°C
Industrial (I): Tamb = -40°C to 85°C

Parameter	Sym	28C04A-15		28C04A-20		28C04A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first	t_{OH}	0		0		0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

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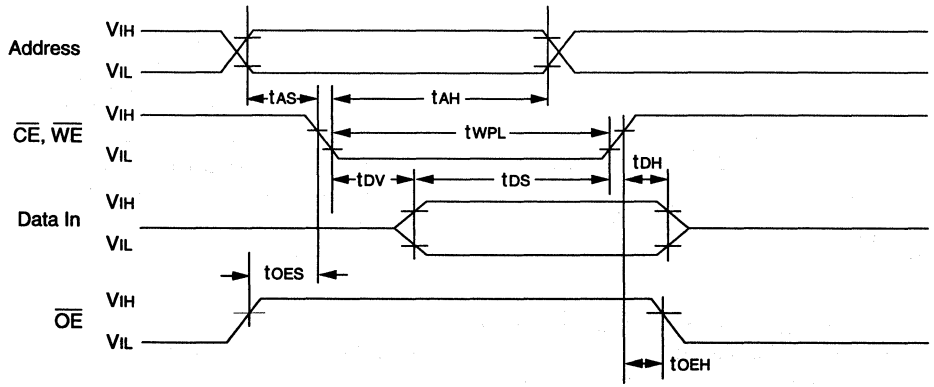
BYTE WRITE
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0°C to 70°C
Industrial (I): Tamb = -40°C to 85°C

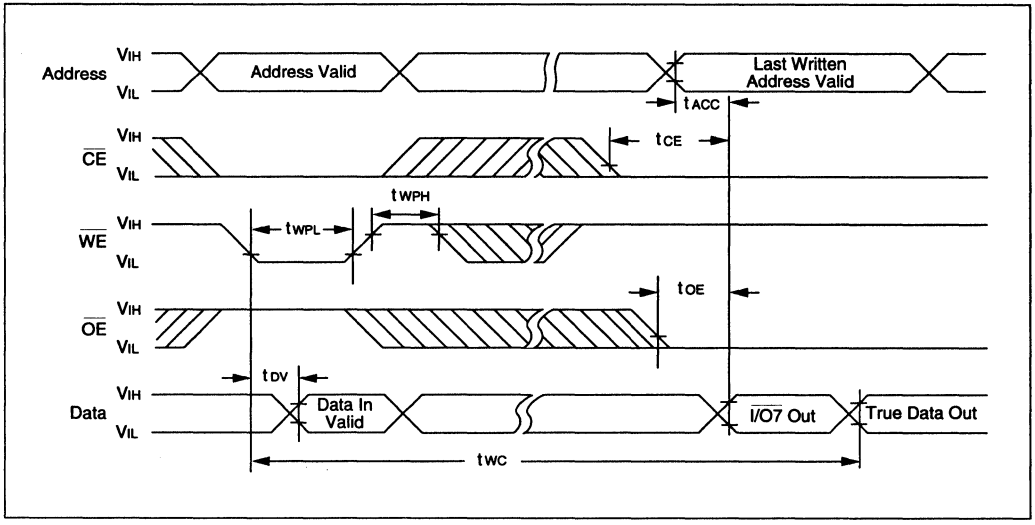
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Write Cycle Time (28C04A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C04AF)	t_{WC}		200	µs	100 µs typical

Note: (1) A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, wichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

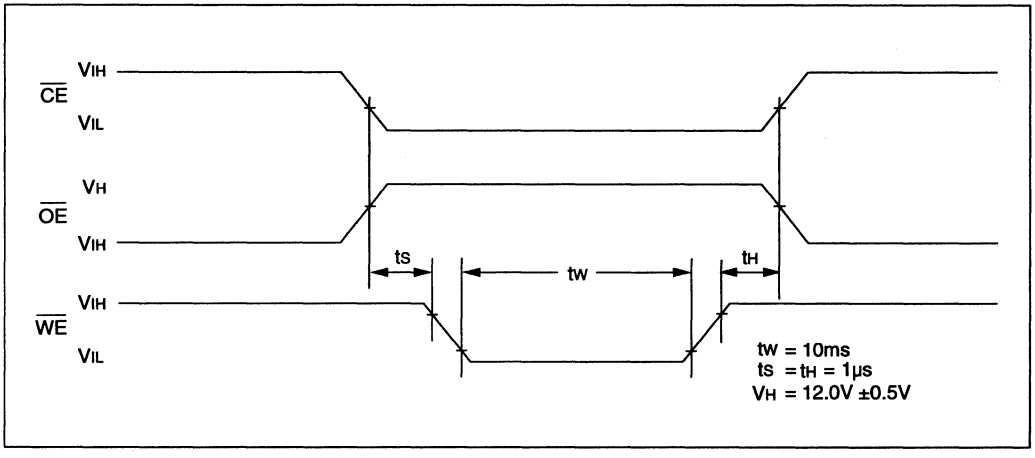
PROGRAMMING WAVEFORMS



$\overline{\text{DATA}}$ POLLING WAVEFORMS



CHIP CLEAR WAVEFORMS



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DEVICE OPERATION

The Microchip Technology Inc. 28C04A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

Read Mode

The 28C04A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The 28C04A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

Write Mode

The 28C04A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the WE pin. On the falling edge of WE, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

Data Polling

The 28C04A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

28C04A F T - 15 I / P

Package:		J	Cerdip
		L	Plastic Leaded Chip Carrier (PLCC)
		P	Plastic DIP
Temperature Range:		Blank	0°C to 70°C
		I	-40°C to 85°C
Access Time:		15	150 ns
		20	200 ns
		25	250 ns
Shipping:		Blank	Tube
		T	Tape and Reel "L" only.
Option:		-	= twc = 1 ms
		F	= twc = 200 µs
Device:	28C04A		512 x 8 CMOS EEPROM

MICROCHIP

28C16A

16K (2K x 8) CMOS EEPROM

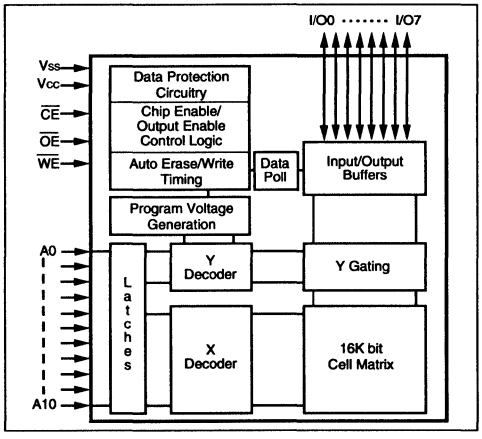
FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - — 30 mA Active
  - — 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >10 years
- High Endurance - Minimum 10^4 Erase/Write Cycles
- Automatic Write Operation
  - — Internal Control Timer
  - — Auto-Clear Before Write Operation
  - — On-Chip Address and Data Latches
- Data polling
- Chip Clear Operation
- Enhanced Data Protection
  - — Vcc Detector
  - — Pulse Filter
  - — Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 2Kx8 JEDEC Standard Pinout
  - — 24-pin Dual-In-Line Package
  - — 32-pin Chip Carrier (Leadless or Plastic)
  - — 28-pin Thin Small Outline Package (TSOP) 8x20mm
  - — 28-pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - — Commercial: 0°C to 70°C
  - — Industrial: -40°C to 85°C

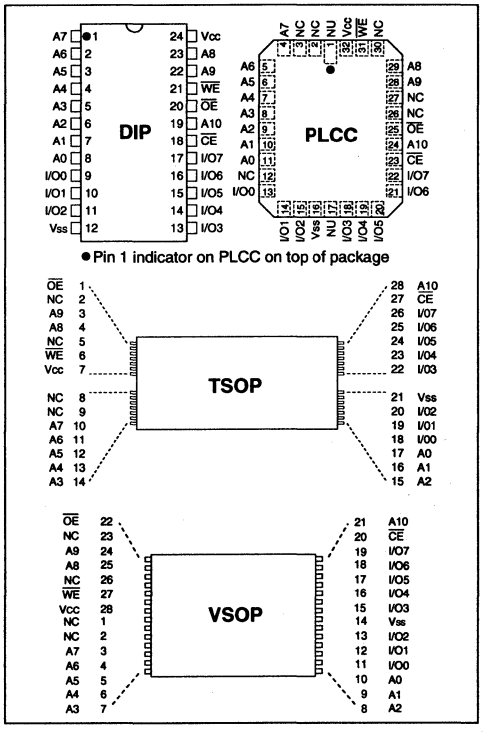
DESCRIPTION

The Microchip Technology Inc. 28C16A is a CMOS 16K non-volatile electrically Erasable PROM. The 28C16A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C16A uses Data polling. Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

BLOCK DIAGRAM



PIN CONFIGURATION



6

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss ..... -0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. Vss ..... -0.6V to +13.5V
Voltage on A9 w.r.t. Vss ..... -0.6V to +13.5V
Output Voltage w.r.t. Vss ..... -0.6V to Vcc+0.6V
Storage temperature ..... -65°C to 125°C
Ambient temp. with power applied ..... -50°C to 95°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0 - A10	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

READ / WRITE OPERATION
DC Characteristics

Vcc = +5V ±10%
Commercial (C): Tamb= 0°C to 70°C
Industrial (I): Tamb= -40°C to 85°C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = -0.1V to Vcc+1
Input Capacitance	—	C_{IN}	—	10	pF	V_{IN} = 0V; Tamb = 25°C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
Output Leakage	—	I_{LO}	-10	10	µA	V_{OUT} = -0.1V to Vcc+0.1V
Output Capacitance	—	C_{OUT}	—	12	pF	V_{IN} = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	I_{CC}	—	30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	$I_{CC(S)TTL}$ $I_{CC(S)TTL}$ $I_{CC(S)CMOS}$	—	2 3 100	mA mA µA	$\overline{CE}$ = V_{IH} (0°C to 70°C) $\overline{CE}$ = V_{IH} (-40°C to 85°C) $\overline{CE}$ = Vcc-0.3 to Vcc+1

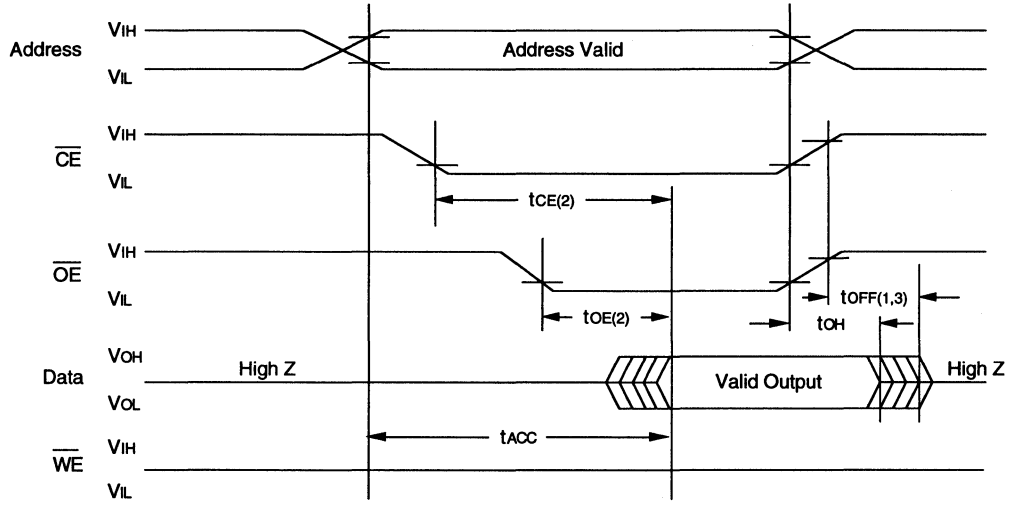
Note: (1) AC power supply current above 5 MHz: 1 mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 ns
Ambient Temperature: Commercial (C): Tamb = 0° C to 70°C
Industrial (I): Tamb = -40° C to 85°C

Parameter	Sym	28C16A-15		28C16A-20		28C16A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	150	—	200	—	250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	150	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	70	—	80	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0	—	0	—	0	—	ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

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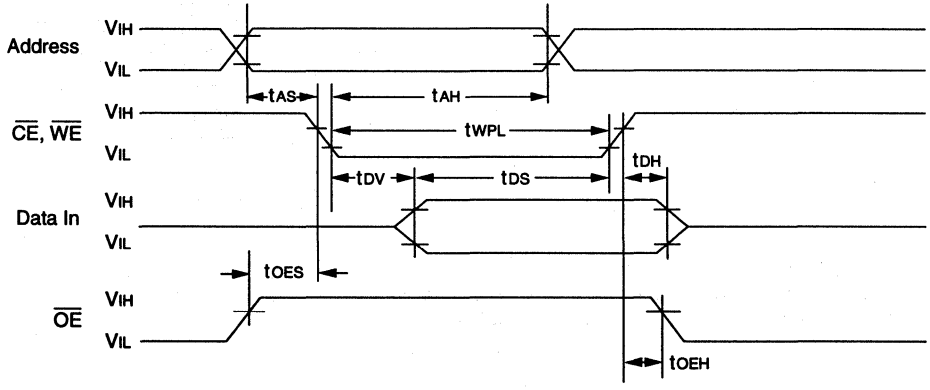
BYTE WRITE
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 ns
Ambient Temperature: Commercial (C): Tamb = 0°C to 70°C
Industrial (I): Tamb = -40°C to 85°C

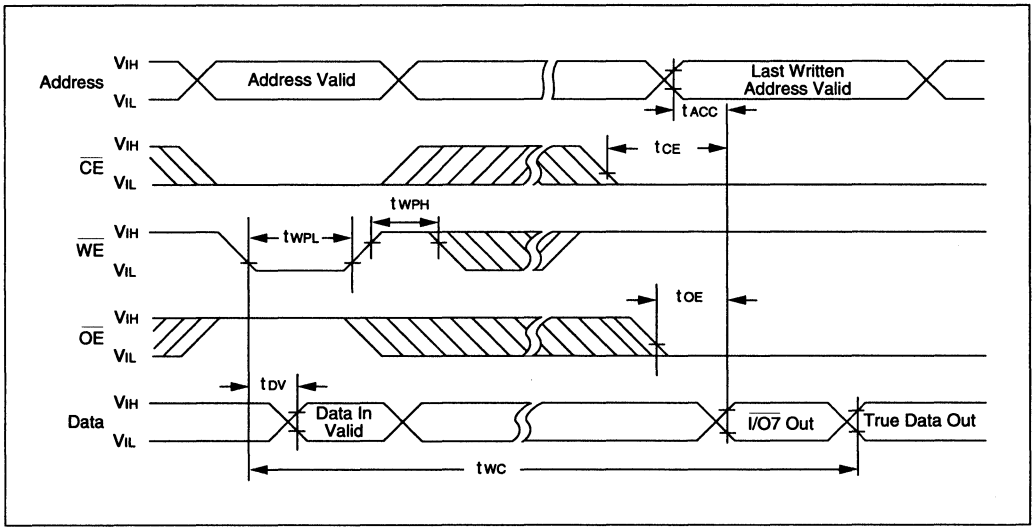
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10	—	ns	
Address Hold Time	t_{AH}	50	—	ns	
Data Set-Up Time	t_{DS}	50	—	ns	
Data Hold Time	t_{DH}	10	—	ns	
Write Pulse Width	t_{WPL}	100	—	ns	Note 1
Write Pulse High Time	t_{WPH}	50	—	ns	
$\overline{OE}$ Hold Time	t_{OEH}	10	—	ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10	—	ns	
Data Valid Time	t_{DV}	—	1000	ns	Note 2
Write Cycle Time (28C16A)	t_{WC}	—	1	ms	0.5 ms typical
Write Cycle Time (28C16AF)	t_{WC}	—	200	µs	100 µs typical

Note: (1) A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, wichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

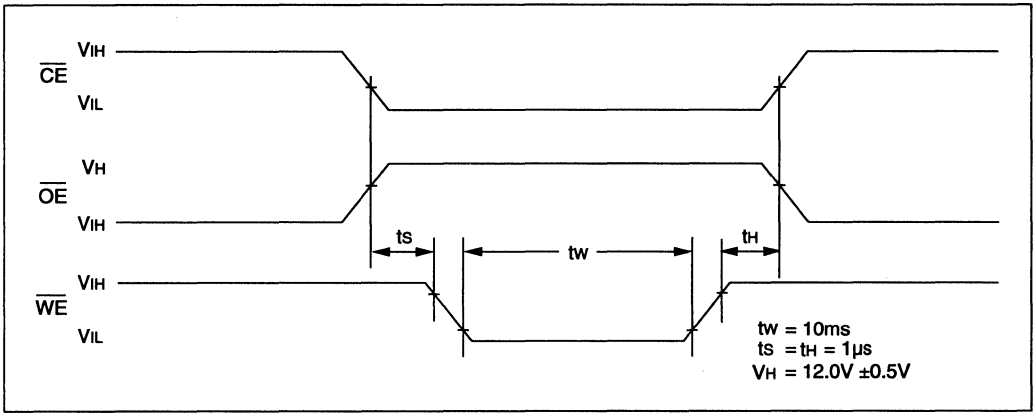
PROGRAMMING WAVEFORMS



DATA POLLING WAVEFORMS



CHIP CLEAR WAVEFORMS



SUPPLEMENTARY CONTROL

Mode	CE	OE	WE	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

Note: VH = 12.0V ±0.5V * Pulsed per programming waveforms.

DEVICE OPERATION

The Microchip Technology Inc. 28C16A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

Read Mode

The 28C16A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

Standby Mode

The 28C16A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal Vcc detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when Vcc is less than the Vcc detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (Vcc).

Write Mode

The 28C16A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

Data Polling

The 28C16A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7EO to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

28C16AF T - 15 I / P

Package:	J	Cerdip
	L	Plastic Leaded Chip Carrier (PLCC)
	P	Plastic DIP
	TS	Thin Small Outline Package (TSOP) 8x20mm
	VS	Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:	Blank	0°C to 70°C
	I	-40°C to 85°C
Access Time:	15	150 ns
	20	200 ns
	25	250 ns
Shipping:	Blank	Tube
	T	Tape and Reel "L" only
Option:	-	= twc = 1 ms
	F	= twc = 200 µs
Device:	28C16A	2K x 8 CMOS EEPROM

MICROCHIP

28C17A

16K (2K x 8) CMOS EEPROM

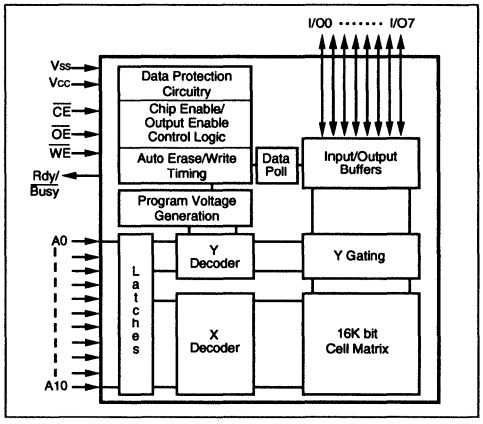
FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - — 30 mA Active
  - — 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >10 years
- High Endurance - Minimum 10^4 Erase/Write Cycles
- Automatic Write Operation
  - — Internal Control Timer
  - — Auto-Clear Before Write Operation
  - — On-Chip Address and Data Latches
- Data Polling
- Ready/Busy
- Chip Clear Operation
- Enhanced Data Protection
  - — Vcc Detector
  - — Pulse Filter
  - — Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 2Kx8 JEDEC Standard Pinout
  - — 28 Pin Dual-In-Line Package
  - — 32-Pin Chip Carrier (Leadless or Plastic)
  - — 28-Pin Thin Small Outline Package (TSOP) 8x20mm
  - — 28-Pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - — Commercial: 0°C to 70°C
  - — Industrial: -40°C to 85°C

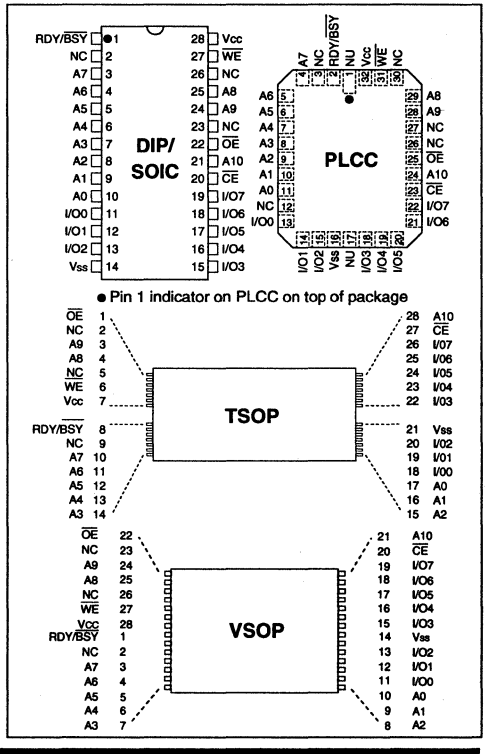
DESCRIPTION

The Microchip Technology Inc. 28C17A is a CMOS 16K non-volatile electrically Erasable PROM. The 28C17A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/Busy output or using Data polling. The Ready/Busy pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

BLOCK DIAGRAM



PIN CONFIGURATION



6

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss..... -0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. Vss..... -0.6V to +13.5V
Voltage on A9 w.r.t. Vss..... -0.6V to +13.5V
Output Voltage w.r.t. Vss..... -0.6V to Vcc+0.6V
Storage temperature ..... -65°C to 125°C
Ambient temp. with power applied ..... -50°C to 95°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0 - A10	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

READ / WRITE OPERATION
DC Characteristics

Vcc = +5V ±10%
Commercial (C): Tamb= 0°C to 70°C
Industrial (I): Tamb= -40°C to 85°C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = -0.1V to Vcc+1
Input Capacitance	—	CIN	—	10	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	—	ILO	-10	10	µA	VOUT = -0.1V to Vcc+0.1V
Output Capacitance	—	COUT	—	12	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	ICC	—	30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	—	2 3 100	mA mA µA	$\overline{CE}$ = VIH (0°C to 70°C) $\overline{CE}$ = VIH (-40°C to 85°C) $\overline{CE}$ = Vcc-0.3 to Vcc+1

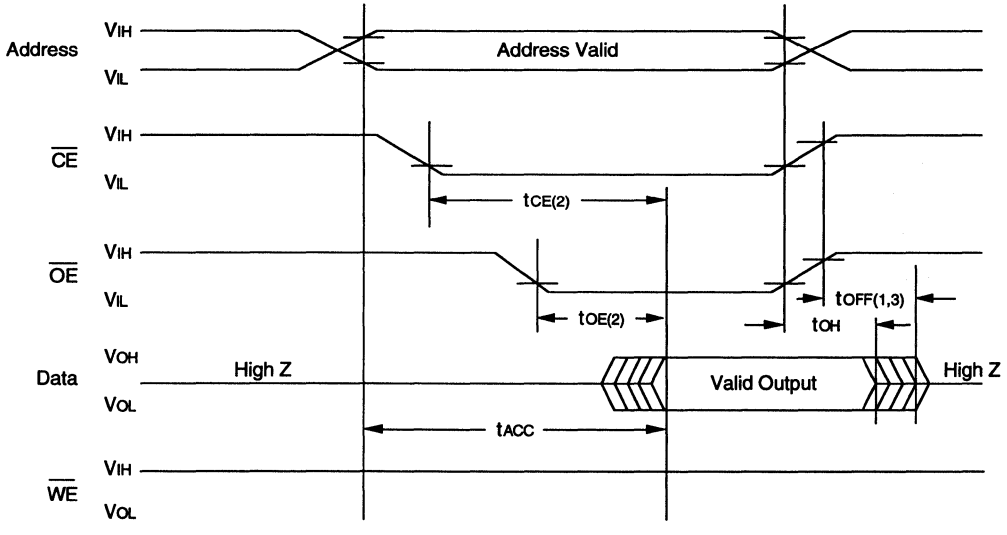
Note: AC power supply current above 5 MHz: 1mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 ns
Ambient Temperature: Commercial (C): Tamb = 0°C to 70°C
Industrial (I): Tamb = -40°C to 85°C

Parameter	Sym	28C17A-15		28C17A-20		28C17A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	150	—	200	—	250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	150	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	70	—	80	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0	—	0	—	0	—	ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

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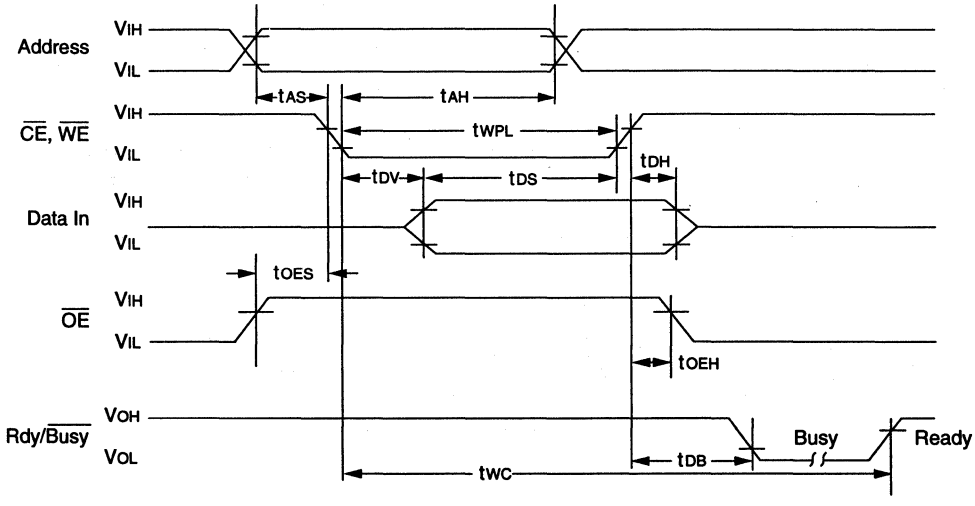
BYTE WRITE
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 ns
Ambient Temperature: Commercial (C): Tamb = 0°C to 70°C
Industrial (I): Tamb = -40°C to 85°C

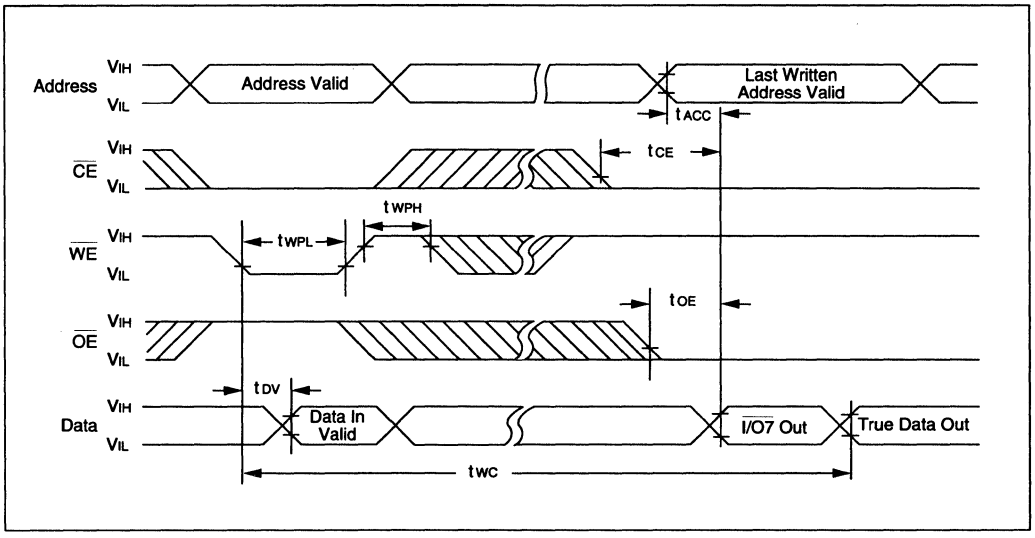
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10	—	ns	
Address Hold Time	t_{AH}	50	—	ns	
Data Set-Up Time	t_{DS}	50	—	ns	
Data Hold Time	t_{DH}	10	—	ns	
Write Pulse Width	t_{WPL}	100	—	ns	Note 1
Write Pulse High Time	t_{WPH}	50	—	ns	
$\overline{OE}$ Hold Time	t_{OEH}	10	—	ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10	—	ns	
Data Valid Time	t_{DV}	—	1000	ns	Note 2
Time to Device Busy	t_{DB}	2	50	ns	
Write Cycle Time (28C17A)	t_{WC}	—	1	ms	0.5 ms typical
Write Cycle Time (28C17AF)	t_{WC}	—	200	µs	100 µs typical

Note: (1) A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, wichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

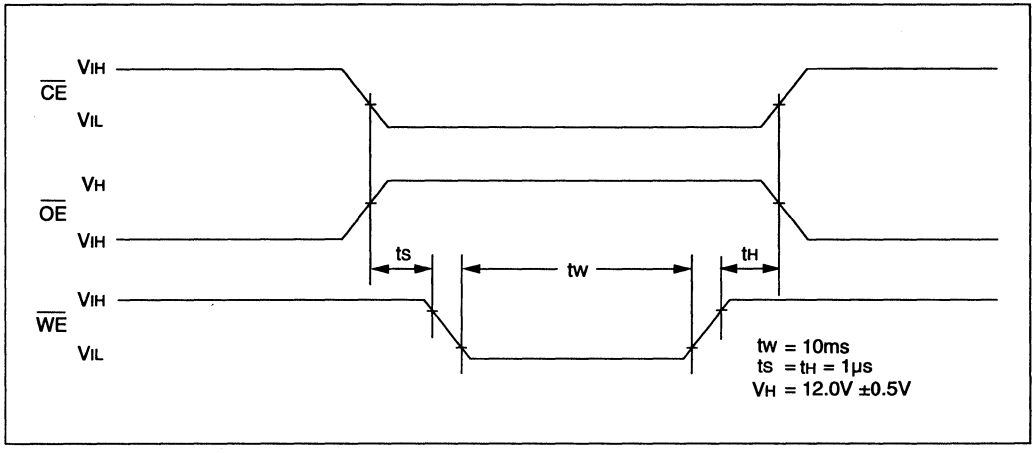
PROGRAMMING WAVEFORMS



DATA POLLING WAVEFORMS



CHIP CLEAR WAVEFORMS



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SUPPLEMENTARY CONTROL						
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{WE}$**	**A9**	**Vcc**	**I/Oi**
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In
Note: VH = 12.0V ±0.5V		* Pulsed per programming waveforms.				

DEVICE OPERATION

The Microchip Technology Inc. 28C17A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$(1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note: (1) Open drain output.
(2) X = Any TTL level.

Read Mode

The 28C17A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

Standby Mode

The 28C17A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal Vcc detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when Vcc is less than the Vcc detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (Vcc).

Write Mode

The 28C17A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C17A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C17A has completed writing and is ready to accept another cycle.

$\overline{Data}$ Polling

The 28C17A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. $\overline{Data}$ polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7EO to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Chip Clear

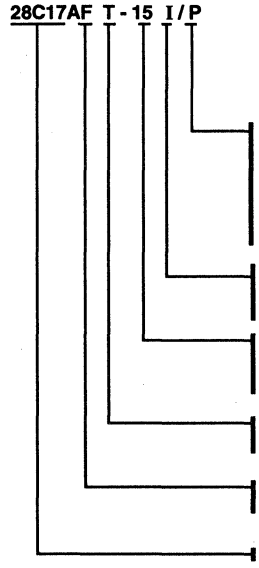
All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Package:	J	Cerdip
	L	Plastic Leaded Chip Carrier (PLCC)
	P	Plastic DIP
	SO	Plastic Small Outline IC
	TS	Thin Small Outline Package (TSOP) 8x20mm
	VS	Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:	Blank	0°C to 70°C
	I	-40°C to 85°C
Access Time:	15	150 ns
	20	200 ns
	25	250 ns
Shipping:	Blank	Tube
	T	Tape and Reel "L" and "SO"
Option:	-	= twc = 1 ms
	F	= twc = 200 µs
Device:	28C17A	2K x 8 CMOS EEPROM

MICROCHIP

28C64A

64K (8K x 8) CMOS EEPROM

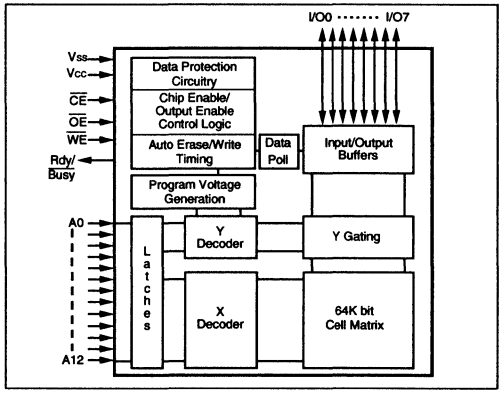
FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - — 30 mA Active
  - — 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >10 years
- High Endurance - Minimum 10^4 Erase/Write Cycles
- Automatic Write Operation
  - — Internal Control Timer
  - — Auto-Clear Before Write Operation
  - — On-Chip Address and Data Latches
- Data Polling
- Ready/Busy
- Chip Clear Operation
- Enhanced Data Protection
  - — Vcc Detector
  - — Pulse Filter
  - — Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 8Kx8 JEDEC Standard Pinout
  - — 28-pin Dual-In-Line Package
  - — 32-pin Chip Carrier (Leadless or Plastic)
  - — 28-pin Thin Small Outline Package (TSOP) 8x20mm
  - — 28-pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - — Commercial: 0°C to 70°C

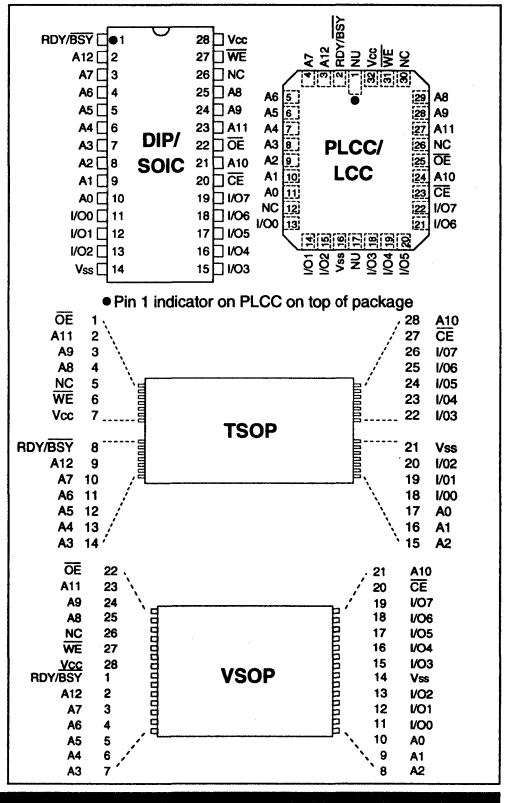
DESCRIPTION

The Microchip Technology Inc. 28C64A is a CMOS 64K non-volatile electrically Erasable PROM. The 28C64A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/Busy output or using Data polling. The Ready/Busy pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

BLOCK DIAGRAM



PIN CONFIGURATION



6

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss ..... -0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. Vss ..... -0.6V to +13.5V
Voltage on A9 w.r.t. Vss ..... -0.6V to +13.5V
Output Voltage w.r.t. Vss ..... -0.6V to Vcc+0.6V
Storage temperature ..... -65°C to 125°C
Ambient temp. with power applied ..... -50°C to 95°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/Busy
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

READ / WRITE OPERATION
DC Characteristics

Vcc = +5V ±10%
Commercial (C): Tamb= 0°C to 70°C
Industrial (I): Tamb= -40°C to 85°C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = -0.1V to Vcc+1
Input Capacitance	—	C_{IN}	—	10	pF	V_{IN} = 0V; Tamb = 25°C; f = 1 MHz (Note 2)
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
Output Leakage	—	I_{LO}	-10	10	µA	V_{OUT} = -0.1V to Vcc+0.1V
Output Capacitance	—	C_{OUT}	—	12	pF	V_{IN} = 0V; Tamb = 25°C; f = 1 MHz (Note 2)
Power Suppy Current, Active	TTL input	I_{CC}	—	30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	$I_{CC(S)TTL}$ $I_{CC(S)TTL}$ $I_{CC(S)CMOS}$	—	2 3 100	mA mA µA	$\overline{CE}$ = V_{IH} (0°C to 70°C) $\overline{CE}$ = V_{IH} (-40°C to 85°C) $\overline{CE}$ = Vcc-0.3 to Vcc+1

Note: (1) AC power supply current above 5 MHz: 2 mA/MHz.
(2) Not 100% tested.

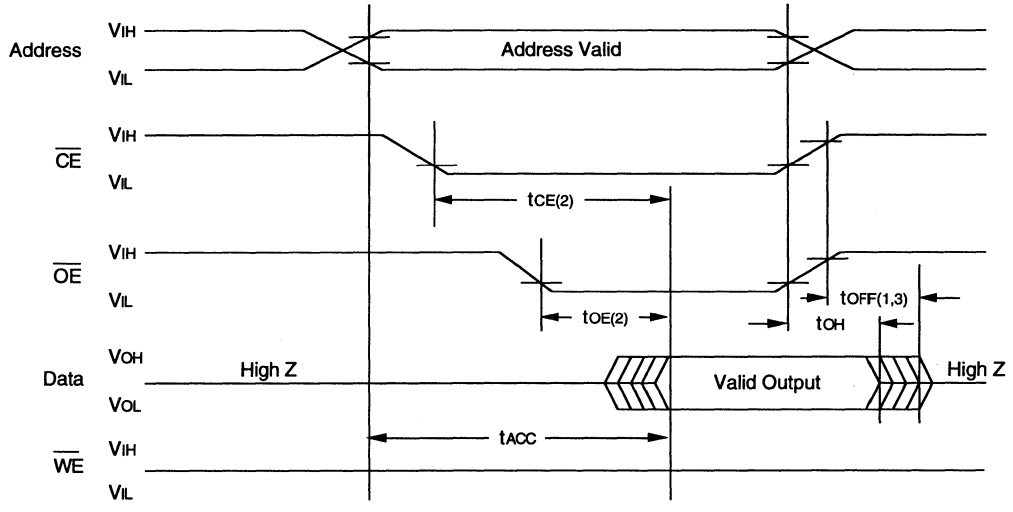
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 ns
Ambient Temperature: Commercial (C): Tamb = 0°C to 70°C
Industrial (I): Tamb = -40°C to 85°C

Parameter	Sym	28C64A-15		28C64A-20		28C64A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	150	—	200	—	250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	150	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	70	—	80	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	Note 1
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0	—	0	—	0	—	ns	Note 1

Note: (1) Not 100% tested.

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

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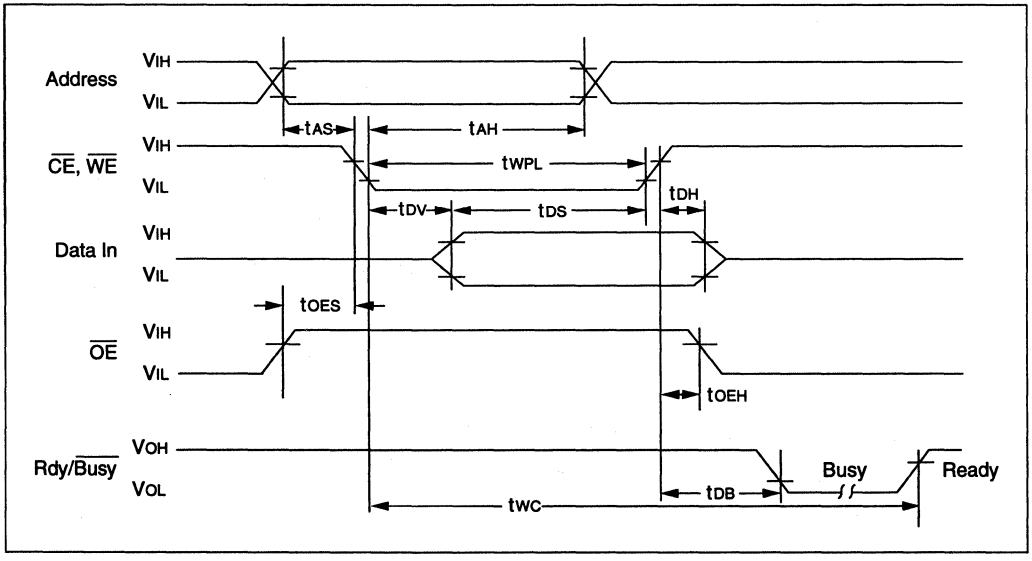
BYTE WRITE
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 ns
Ambient Temperature: Commercial (C): Tamb = 0°C to 70°C
Industrial (I): Tamb = -40°C to 85°C

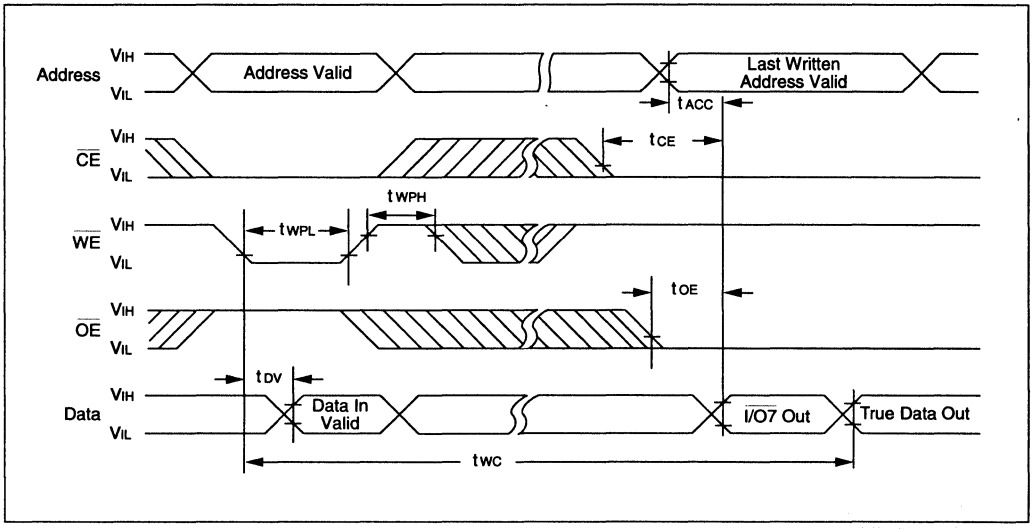
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10	—	ns	
Address Hold Time	t_{AH}	50	—	ns	
Data Set-Up Time	t_{DS}	50	—	ns	
Data Hold Time	t_{DH}	10	—	ns	
Write Pulse Width	t_{WPL}	100	—	ns	Note 1
Write Pulse High Time	t_{WPH}	50	—	ns	
$\overline{OE}$ Hold Time	t_{OEH}	10	—	ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10	—	ns	
Data Valid Time	t_{DV}	—	1000	ns	Note 2
Time to Device Busy	t_{DB}	2	50	ns	
Write Cycle Time (28C64A)	t_{WC}	—	1	ms	0.5 ms typical
Write Cycle Time (28C64AF)	t_{WC}	—	200	µs	100 µs typical

Note: (1) A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, wichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

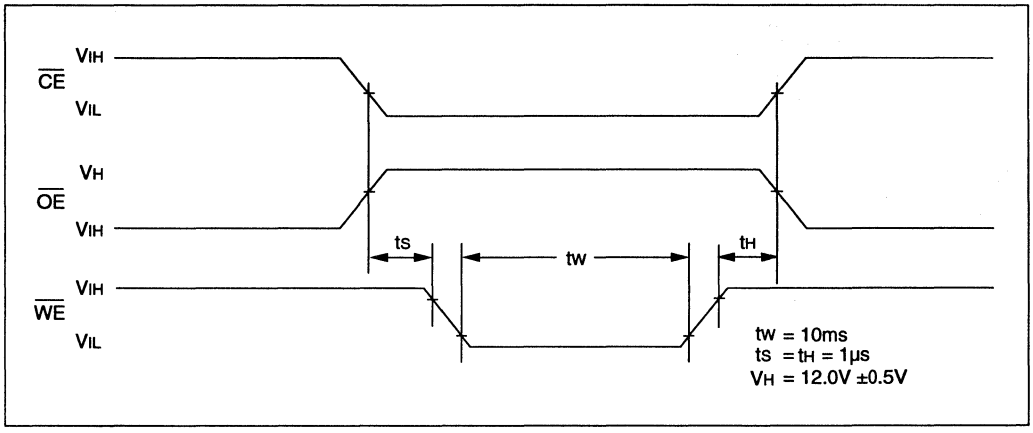
PROGRAMMING WAVEFORMS



DATA POLLING WAVEFORMS



CHIP CLEAR WAVEFORMS



SUPPLEMENTARY CONTROL						
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{WE}$**	**A9**	**Vcc**	**I/OI**
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In
Note: VH = 12.0V ±0.5V		* Pulsed per programming waveforms.				

DEVICE OPERATION

The Microchip Technology Inc. 28C64A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$ (1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note: (1) Open drain output.
(2) X = Any TTL level.

Read Mode

The 28C64A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

Standby Mode

The 28C64A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal Vcc detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when Vcc is less than the Vcc detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (Vcc).

Write Mode

The 28C64A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C64A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C64A has completed writing and is ready to accept another cycle.

$\overline{Data}$ Polling

The 28C64A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. $\overline{Data}$ polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 1FE0 to 1FFF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

28C64AF T - 15 I / P

Package:	J	Cerdip
	L	Plastic Leaded Chip Carrier (PLCC)
	P	Plastic DIP
	SO	Plastic Small Outline IC
	TS	Thin Small Outline Package (TSOP) 8x20mm
	VS	Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:	Blank	0°C to 70°C
	I	-40°C to 85°C
Access Time:	15	150 ns
	20	200 ns
	25	250 ns
Shipping:	Blank	Tube
	T	Tape and Reel "L" and "SO"
Option:	Blank	= twc = 1 ms
	F	= twc = 200 µs
	X	Pin 1 NC (Pin 2 PLCC), twc = 1 ms
Device:	28C64A	8K x 8 CMOS EEPROM

SECTION 7
EPROM PRODUCT SPECIFICATIONS

EPROM Selection Guide

CMOS EPROMs

PART NUMBER	QTP AVAIL.	SIZE	ORG	ACCESS TIME (ns)	SUPPLY VOLTAGE	PACKAGE	TEMP RANGE	STANDBY CURRENT
27C64	YES	64K	8K x 8	120-250	+5V	J,K,L,P,SO,TS	C,I	2mA/100µA
27C128	YES	128K	16K x 8	120-250	+5V	J,K,L,P,SO	C,I	2mA/100µA
27C256	YES	256K	32K x 8	90-200	+5V	J,K,L,P,SO,TS,VS	C,I,E	2mA/100µA
27C512	YES	512K	64K x 8	90-200	+5V	J,K,L,P,SO,TS,VS	C,I,E	2mA/100µA
27C512A	YES	512K	64K x 8	70-150	+5V	J,K,L,P,SO,TS,VS	C,I,E	2mA/30µA
27LV64	YES	64K	8K x 8	200-300	+3V to +5V	J,K,L,P,SO,TS	C,I	1mA/100µA
27LV256	YES	256K	32K x 8	200-300	+3V to +5V	J,K,L,P,SO,TS,VS	C,I	1mA/100µA
27LV512	YES	512K	64K x 8	200-300	+3V to +5V	J,K,L,P,SO,TS,VS	C,I	1mA/100µA
27HC256	NO	256K	32K x 8	55-90	+5V	J,K,L,P,SO,TS,VS	C,I,E	35mA
27HC256L	NO	256K	32K x 8	90	+5V	J,K,L,P,SO,TS,VS	C,I	2mA/100µA
27HC1616	NO	256K	16K x 16	55-70	+5V	40J, 44K	C,I	50mA

PACKAGES

P = Plastic DIP
SN = .150" 8ld SOIC
S = Dice in Wafflepack
J = Ceramic DIP
SM = .207" 8ld SOIC
L = PLCC
SL = .150" 14ld SOIC
W = Dice in Wafer Form
VS = 28ld VSOP (8x13.4mm)
K = Ceramic LCC
SO = .300" 28ld SOIC
TS = 28ld TSOP (8x20mm)

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* Endurance is guaranteed to 10K cycles at extended (-40°C to +125°C) temperature.

NOTE: NOT ALL COMBINATIONS OF SPEED/TEMPERATURE RANGE/PACKAGE/ETC. ARE AVAILABLE. CONSULT FACTORY FOR SPECIFIC PART INFORMATION.

MICROCHIP

27C64

64K (8K x 8) CMOS EPROM

FEATURES

- High speed performance
  - —120 ns access time available
- CMOS Technology for low power consumption
  - —20 mA Active current
  - —100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 8K x 8: JEDEC standard pinouts
  - —28-pin Dual-in-line package
  - —32-pin Chip carrier (leadless or plastic)
  - —28-pin SOIC package
  - —28-pin TSOP package
  - —Tape and reel
- Available for the following temperature ranges:
  - —Commercial: 0°C to 70°C
  - —Industrial: -40°C to 85°C
  - —Automotive: -40°C to 125°C

DESCRIPTION

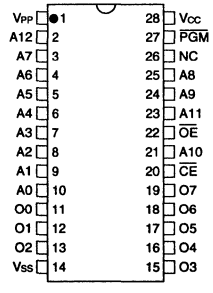
The Microchip Technology Inc. 27C64 is a CMOS 64K bit (electrically) Programmable Read Only Memory. The device is organized as 8K words by 8 bits (8K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120 ns. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

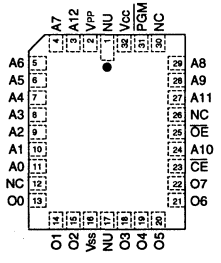
7

PIN CONFIGURATIONS

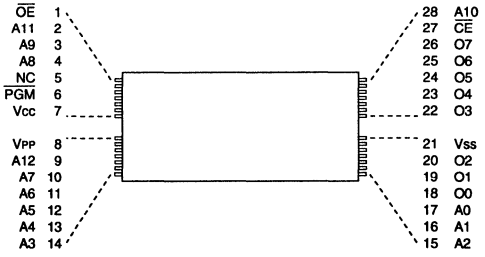
Top View



DIP/SOIC



PLCC/LCC



TSOP

PIN FUNCTION TABLE	
Name	**Function**
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to 150°C
Ambient temp. with power applied ..... -65°C to 125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0°C to 70°C
Industrial: Tamb= -40°C to 85°C
Extended (Automotive): Tamb= -40°C to 125°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb= 25°C; f = 1 MHz
Power Supply Current, Active	C I, E	TTL input TTL input	ICC1 ICC2	— —	20 25	mA mA	VCC = 5.5V; VPP = VCC; f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	ICC(S) — —	— — —	2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current	all	Read Mode	IPP		100	µA	VPP = 5.5V
VPP Read Voltage	all	Read Mode	VPP	VCC-0.7	VCC	V	Note 2

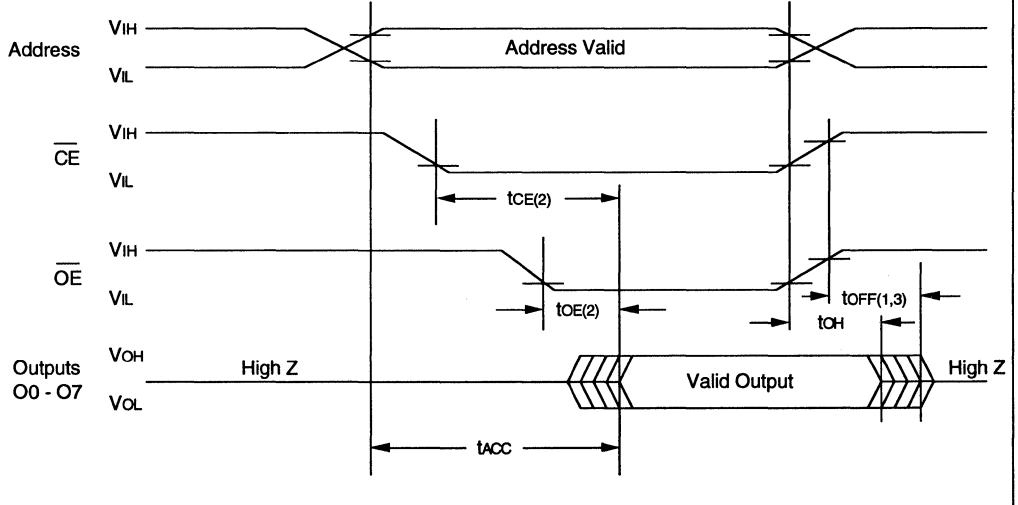
* Parts: C = Commercial Temperature Range; I, E = Industrial and Extended Temperature Ranges
Notes: (1) Active current increases 8 mA per MHz up to operating frequency for all temperature ranges.
(2) VCC must be applied before VPP, and be removed simultaneously or after VPP.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 10 ns
Ambient Temperature: Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C
Extended (Automotive): Tamb = -40°C to 125°C

Parameter	Sym	27C64-12		27C64-15		27C64-17		27C64-20		27C64-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	120	—	150	—	170	—	200	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	120	—	150	—	170	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	65	—	70	—	70	—	75	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	t_{OH}	0	—	0	—	0	—	0	—	0	—	ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

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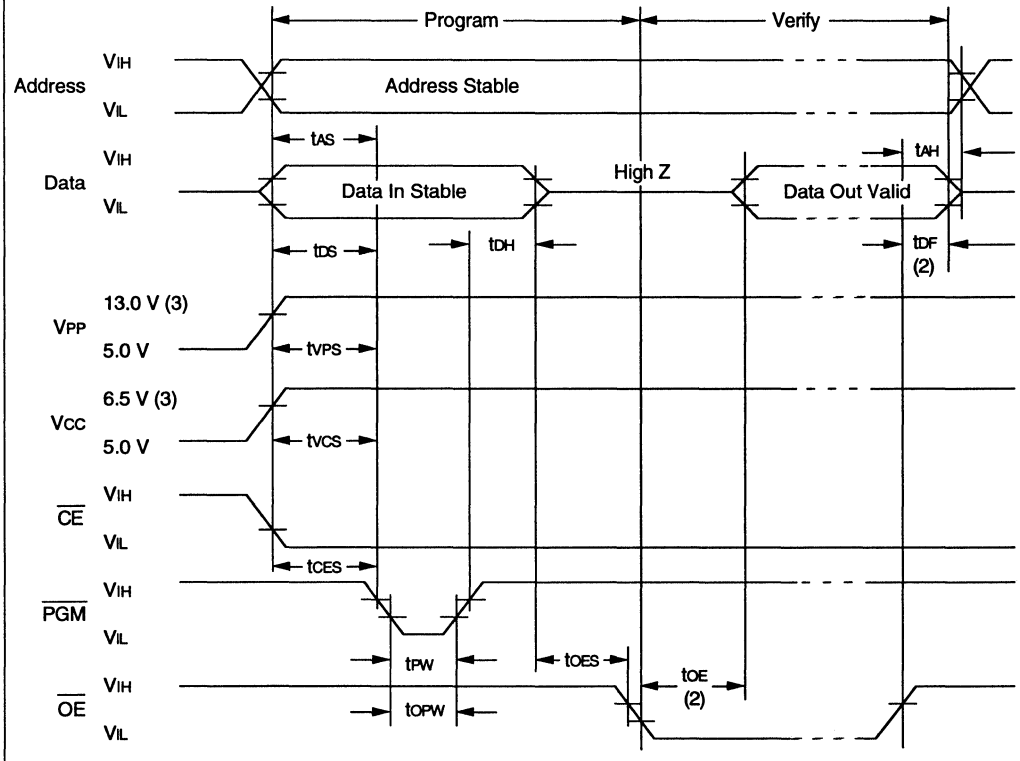
PROGRAMMING **DC Characteristics**		Ambient Temperature: Tamb = 25°C ±5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V				
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4 —	— 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
V_{CC} Current, program & verify	—	I_{CC2}	—	20	mA	Note 1
V_{PP} Current,program	—	I_{PP2}	—	25	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

PROGRAMMING **AC Characteristics** for Program, Program Verify and Program Inhibit Modes		AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V Ambient Temperature: Tamb = 25°C ±5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
V_{PP} Set-Up Time	t_{VPS}	2	—	µs	
Data Valid from $\overline{OE}$	t_{OE}	—	100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µs ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms (1)



Notes: (1) The input timing reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
(2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
(3) V_{CC} = 6.5 V ±0.25 V, V_{PP} = V_H = 13.0 V ±0.25 V for Express algorithm.

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	A9	O0 - O7
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	X	D_{OUT}
Program	V_{IL}	V_{IH}	V_{IL}	V_H	X	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_H	X	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_H	X	High Z
Standby	V_{IH}	X	X	V_{CC}	X	High Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	X	High Z
Identity	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_H	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (t_{OE}).

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm² for approximately 20 minutes.

Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to the proper voltage,
b) V_{PP} is brought to the proper V_H level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A12 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

Identity Mode

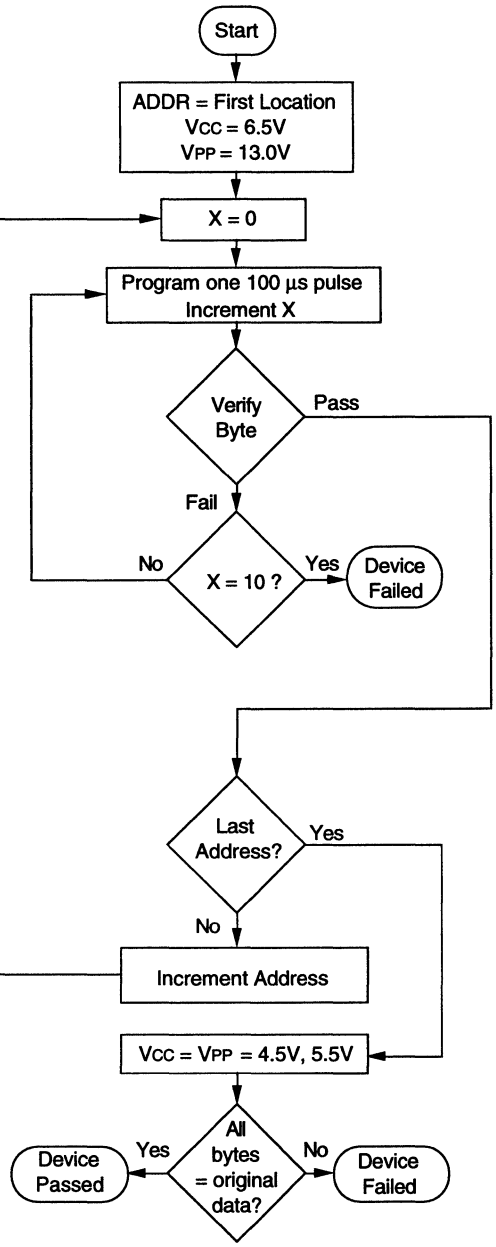
In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	0	0	0	0	0	0	1	0	02

* Code subject to change.

FIGURE 1 - PROGRAMMING EXPRESS ALGORITHM

Conditions:
T_{amb} = 25°C ±5°C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



7

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C64 - 25 I / K

Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	TS	Thin Small Outline Package (TSOP) 8x13.4mm
Temperature Range:	-	0°C to 70°C
	I	-40°C to 85°C
	E	-40°C to 125°C
Access Time:	12	120 ns
	15	150 ns
	17	170 ns
	20	200 ns
	25	250 ns
Device:	27C64	64K (8K x 8) CMOS EPROM

MICROCHIP

27LV64

64K (8K x 8) Low Voltage CMOS EPROM

FEATURES

- Wide voltage range 3.0V to 5.5V
- High speed performance
  —200 ns access time available at 3.0V
- CMOS Technology for low power consumption
  —8 mA active current at 3.0V
  —20 mA active current at 5.5V
  —100 µA standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 8K x 8: JEDEC standard pinouts
  —28-pin Dual-in-line package
  —32-pin Chip carrier (leadless or plastic)
  —28-pin SOIC package
  —28-pin TSOP package
  —Tape and reel
- Available for the following temperature ranges:
  —Commercial: 0°C to 70°C
  —Industrial: -40°C to 85°C

DESCRIPTION

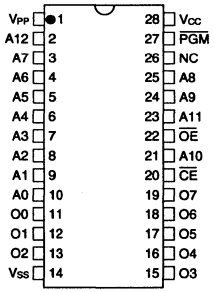
The Microchip Technology Inc. 27LV64 is a low-voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as 8K x 8 (8K-Byte) non-volatile memory product. The 27LV64 consumes only 8mA maximum of active current during a 3.0 volt read operation therefore improving battery performance. This device is designed for very low voltage applications where conventional 5.0 volt only EPROMs can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200 ns at 3.0V. This device allows system designers the ability to use low voltage non-volatile memory with todays low voltage microprocessors and peripherals in battery powered applications.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

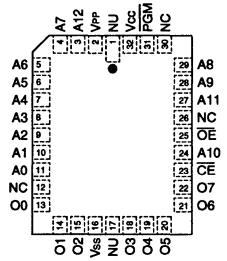
7

PIN CONFIGURATIONS

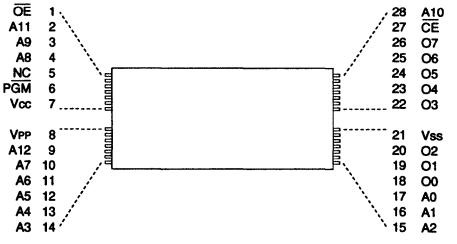
Top View



DIP/SOIC



PLCC/LCC



TSOP

PIN FUNCTION TABLE	
Name	**Function**
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
PGM	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V 0r +3V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to 150°C
Ambient temp. with power applied ..... -65°C to 125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = 3.0V to 5.5V unless otherwise specified
Commercial: Tamb= 0°C to 70°C
Industrial: Tamb= -40°C to 85°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V;Tamb= 25°C; f = 1 MHz
Power Supply Current, Active	C I	TTL input TTL input	ICC1 ICC2	— —	20 @ 5.0V 8 @ 3.0V 25 @ 5.0V 10 @ 3.0V	mA mA mA mA	VCC = 5.5V; VPP = VCC; f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	ICC(S)	—	1 @ 3.0V 2 @ 3.0V 100 @ 3.0V	mA mA µA	 $\overline{CE}$ = VCC ±0.2V

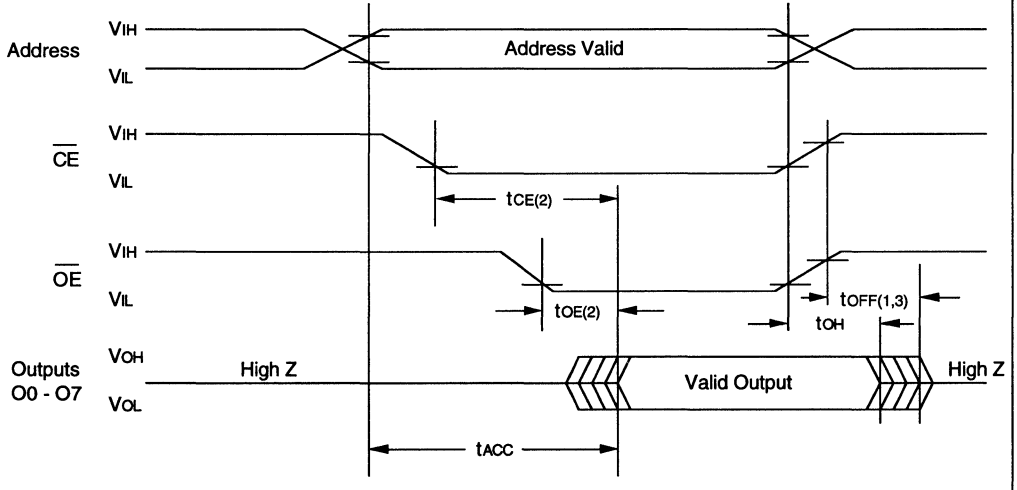
* Parts: C = Commercial Temperature Range; I = Industrial Temperature Range
Notes: (1) Active current increases 8 mA per MHz up to operating frequency for all temperature ranges.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 10 ns
Ambient Temperature: Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C

Parameter	Sym	27LV64-20		27LV64-25		27LV64-30		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	200	—	250	—	300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	200	—	250	—	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	100	—	125	—	125	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	50	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	t_{OH}	0	—	0	—	0	—	ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

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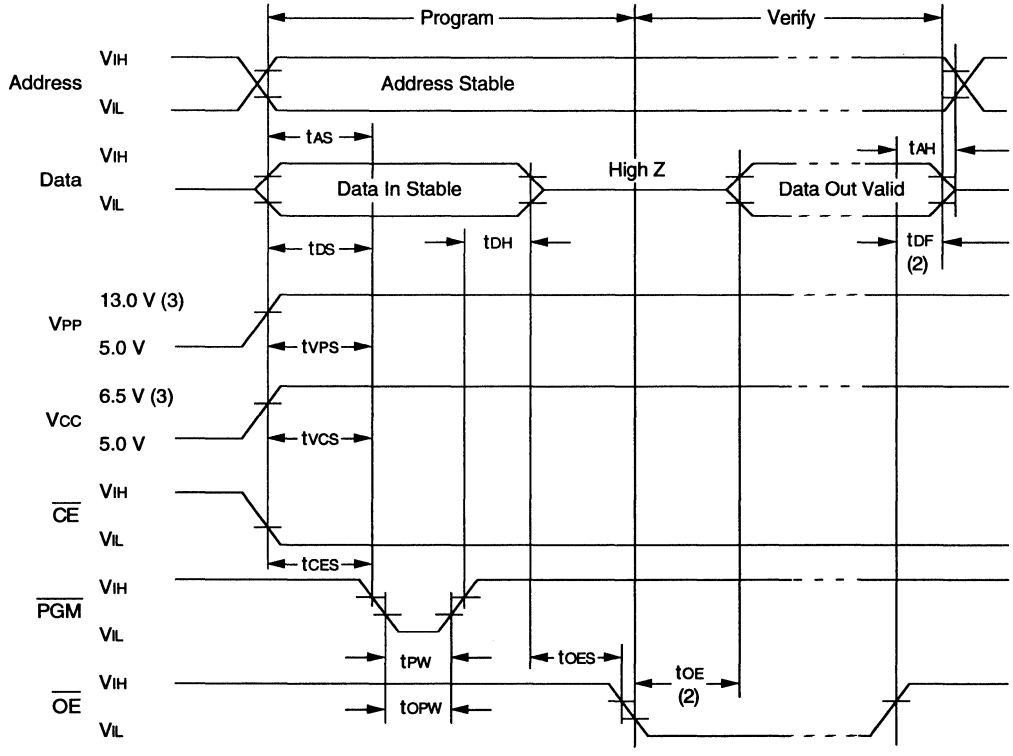
PROGRAMMING **DC Characteristics**		Ambient Temperature: Tamb = 25°C ±5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V				
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
V_{CC} Current, program & verify	—	I_{CC2}	—	20	mA	Note 1
V_{PP} Current,program	—	I_{PP2}	—	25	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

PROGRAMMING **AC Characteristics** for Program, Program Verify and Program Inhibit Modes		AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V Ambient Temperature: Tamb = 25°C ±5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
V_{PP} Set-Up Time	t_{VPS}	2	—	µs	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µs ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms (1)



Notes: (1) The input timing reference is 0.8V for VIL and 2.0V for VIH.
(2) tDF and tOE are characteristics of the device but must be accommodated by the programmer.
(3) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for Express algorithm.

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

7

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

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Erase Mode (U.V. Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

Programming Mode

The express algorithm has been developed to improve on the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to proper voltage,
b) V_{PP} is brought to proper V_H level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A12 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

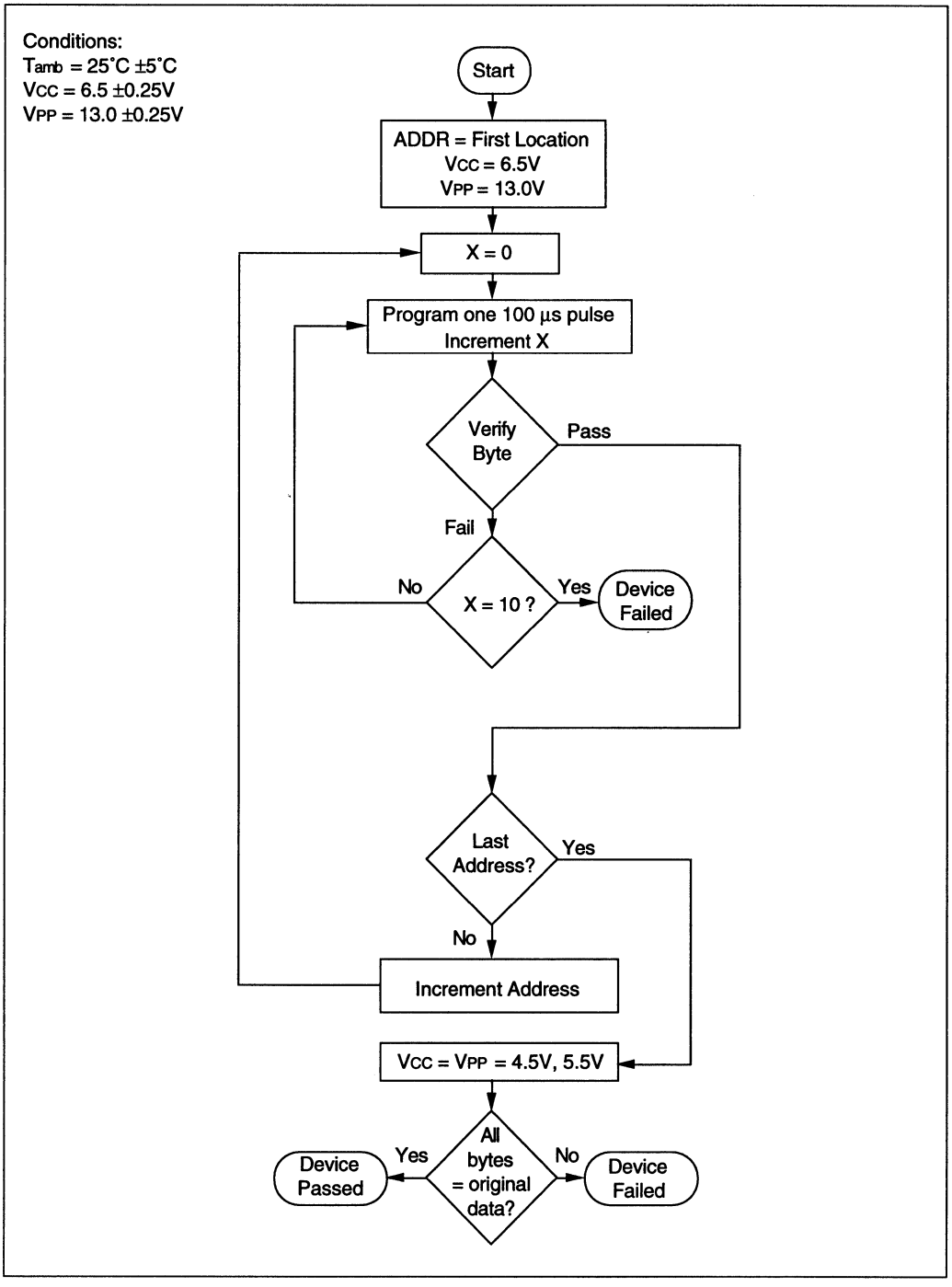
Identity Mode

In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	0	0	0	0	0	0	1	0	02

* Code subject to change.

FIGURE 1 - PROGRAMMING EXPRESS ALGORITHM



7

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27LV64 - 25 I / K

Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	TS	Thin Small Outline Package
Temperature Range:	-	0°C to 70°C
	I	-40°C to 85°C
Access Time:	20	200 ns
	25	250 ns
	30	300 ns
Device:	27LV64	64K (8K x 8) Low voltage CMOS EPROM

MICROCHIP

27C128

128K (16K x 8) CMOS EPROM

FEATURES

- High speed performance
  —120 ns access time available
- CMOS Technology for low power consumption
  —20 mA Active current
  —100 μA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 16K x 8: JEDEC standard pinouts
  —28-pin Dual-in-line package
  —32-pin Chip carrier (leadless or plastic)
  —28-pin SOIC package
  —28-pin TSOP package
  —Tape and reel
- Available for the following temperature ranges:
  —Commercial: 0°C to 70°C
  —Industrial: -40°C to 85°C
  —Automotive: -40°C to 125°C

DESCRIPTION

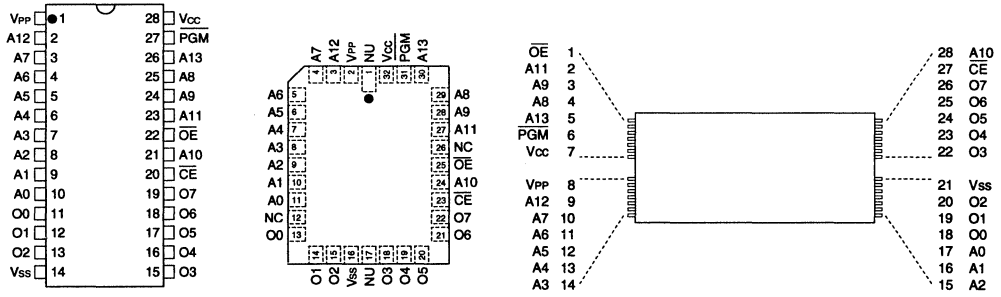
The Microchip Technology Inc 27C128 is a CMOS 128K bit (electrically) Programmable Read Only Memory. The device is organized as 16K words by 8 bits (16K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120 ns. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

7

PIN CONFIGURATIONS

Top View



DIP/SOIC PLCC/LCC TSOP

PIN FUNCTION TABLE	
Name	**Function**
A0 - A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
PGM	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC + 1V
Storage temperature ..... -65°C to 150°C
Ambient temp. with power applied ..... -65°C to 125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C
Extended (Automotive): Tamb = -40°C to 125°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V;Tamb = 25° C; f = 1 MHz
Power Supply Current, Active	C I, E	TTL input TTL input	ICC1 ICC2	— —	20 25	mA mA	VCC = 5.5V; VPP = VCC; f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	ICC(S)	— — —	2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	— VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

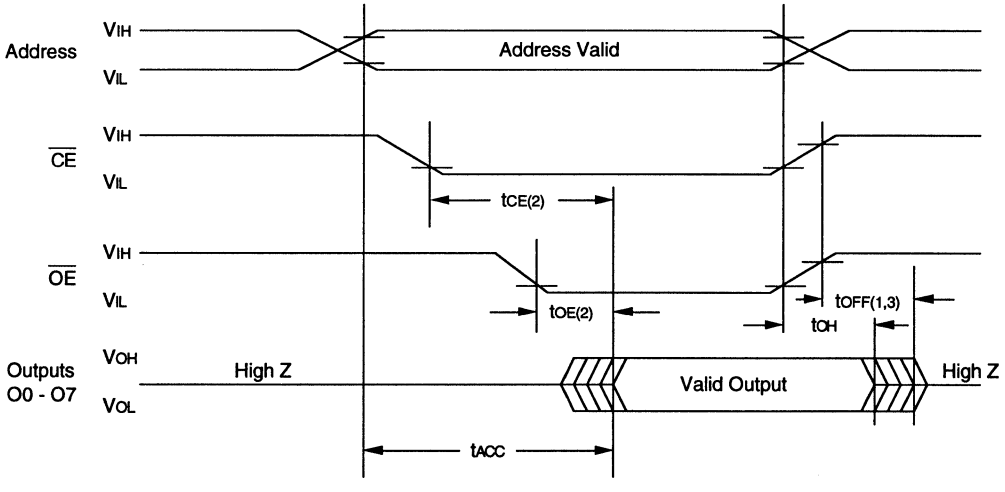
* Parts: C = Commercial Temperature Range; I, E = Industrial and Extended Temperature Ranges
Notes: (1) Active current increases 8 mA per MHz up to operating frequency for all temperature ranges.
(2) VCC must be applied before VPP, and be removed simultaneously or after VPP.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 10 ns
Ambient Temperature: Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C
Extended (Automotive): Tamb = -40°C to 125°C

Parameter	Sym	27C128-12		27C128-15		27C128-17		27C128-20		27C128-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	120	—	150	—	170	—	200	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	120	—	150	—	170	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	65	—	70	—	70	—	75	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	t_{OH}	0	—	0	—	0	—	0	—	0	—	ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

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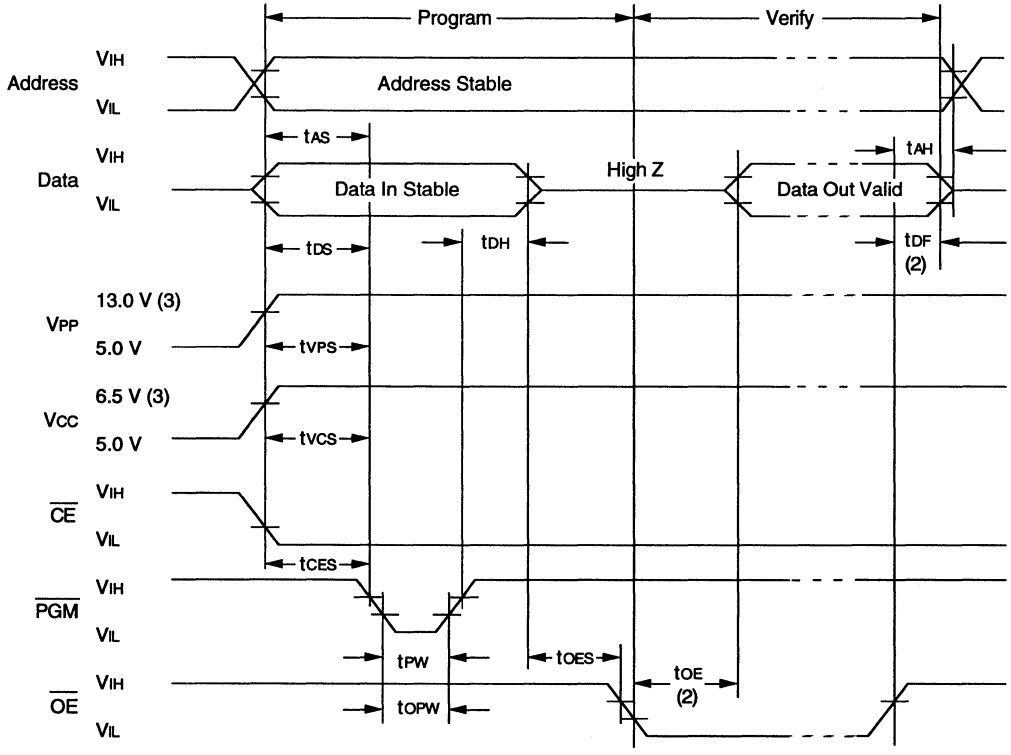
PROGRAMMING **DC Characteristics**		Ambient Temperature: Tamb = 25°C ±5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V				
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
V_{CC} Current, program & verify	—	I_{CC2}	—	20	mA	Note 1
V_{PP} Current, program	—	I_{PP2}	—	25	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

PROGRAMMING **AC Characteristics** for Program, Program Verify and Program Inhibit Modes		AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V Ambient Temperature: Tamb = 25°C ±5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
V_{PP} Set-Up Time	t_{VPS}	2	—	µs	
Data Valid from $\overline{OE}$	t_{OE}	—	100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µs ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms (1)



Notes: (1) The input timing reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
(2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
(3) V_{CC} = 6.5V ±0.25V, V_{PP} = V_H = 13.0V ±0.25V for Express algorithm.

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from CE to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

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Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm² for approximately 20 minutes.

Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to the proper voltage,
b) V_{PP} is brought to the proper V_H level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A13 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure that all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

Identity Mode

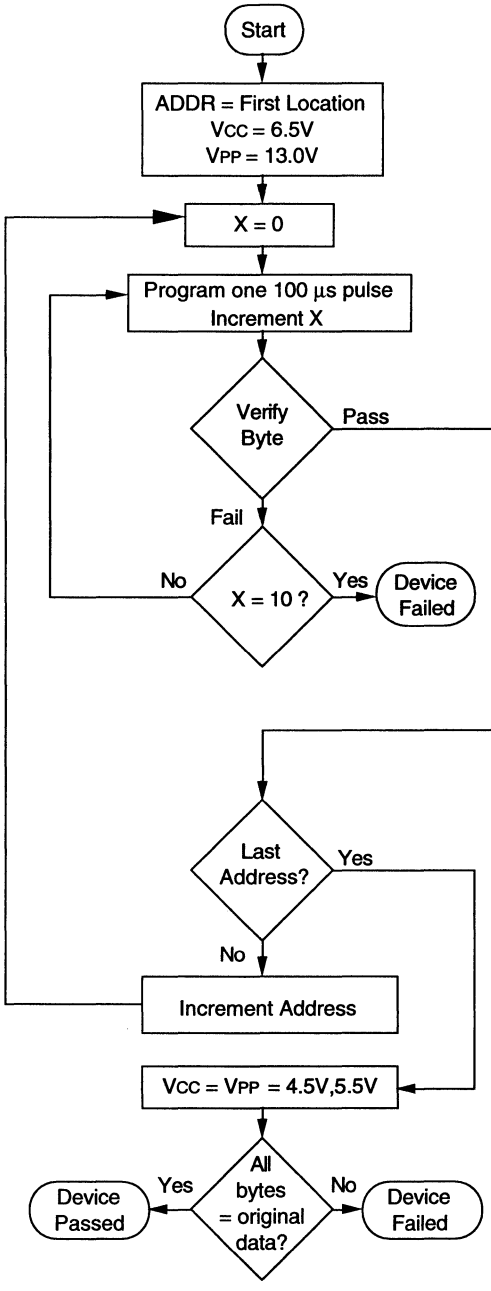
In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc, and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	0	0	1	1	83

* Code subject to change.

FIGURE 1 - PROGRAMMING EXPRESS ALGORITHM

Conditions:
T_{amb} = 25°C ±5°C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C128 - 25 I / P

Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	TS	Thin Small Outline Package (TSOP) 8x13.4mm
Temperature Range:	-	0°C to 70°C
	I	-40°C to 85°C
	E	-40°C to 125°C
Access Time:	12	120 ns
	15	150 ns
	17	170 ns
	20	200 ns
	25	250 ns
Device:	27C128	128K (16K x 8) CMOS EPROM

MICROCHIP

27C256

256K (32K x 8) CMOS EPROM

FEATURES

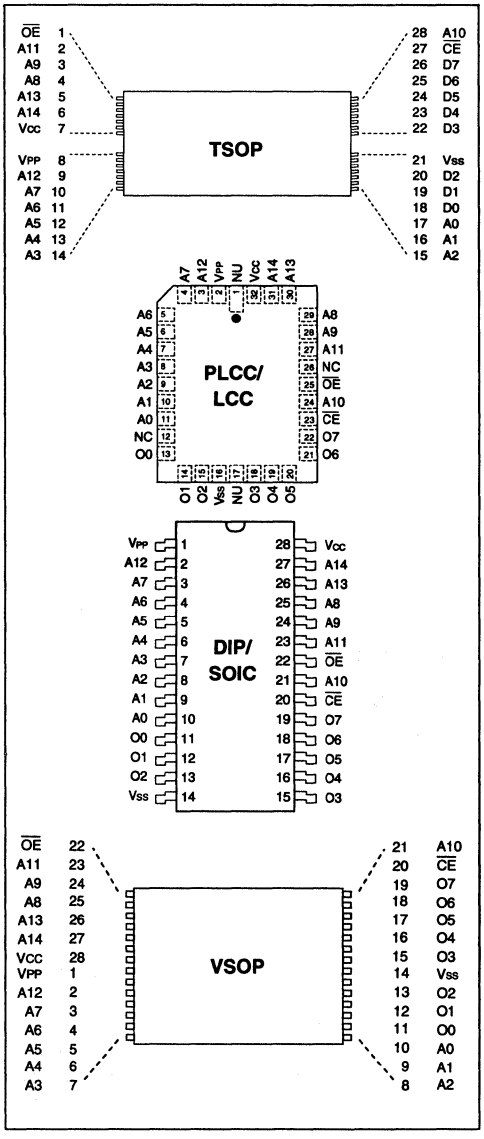
- High speed performance
  - — 90 ns access time available
- CMOS Technology for low power consumption
  - — 20 mA Active current
  - — 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  - — 28-pin Dual-in-line package
  - — 32-pin Chip carrier (leadless or plastic)
  - — 28-pin SOIC package
  - — 28-pin Thin Small Outline Package (TSOP)
  - — 28-pin Very Small Outline Package (VSOP)
  - — Tape and reel
- Available for extended temperature ranges:
  - — Commercial: 0°C to +70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C

DESCRIPTION

The Microchip Technology Inc. 27C256 is a CMOS 256K bit electrically Programmable Read Only Memory (EPROM). The device is organized as 32K words by 8 bits (32K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90 ns This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

PIN CONFIGURATION



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PIN FUNCTION TABLE	
Name	**Function**
A0 - A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14.0V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC + 1.0V
Storage temperature ..... -65°C to 150°C
Ambient temp. with power applied ..... -65°C to 125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C
Extended (Automotive): Tamb = -40°C to 125°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb= 25° C; f = 1 MHz
Power Suppy Current, Active	C I, E	TTL input TTL input	ICC1 ICC2	— —	20 25	mA mA	VCC = 5.5V; VPP = VCC; f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	ICC(S)	—	2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	— VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

* Parts: C = Commercial Temperature Range
I, E = Industrial and Extended Temperature Range

Notes: (1) Active current increases 5 mA per MHz up to operating frequency for all temperature ranges.
(2) VCC must be applied before VPP, and be removed simultaneously or after VPP.

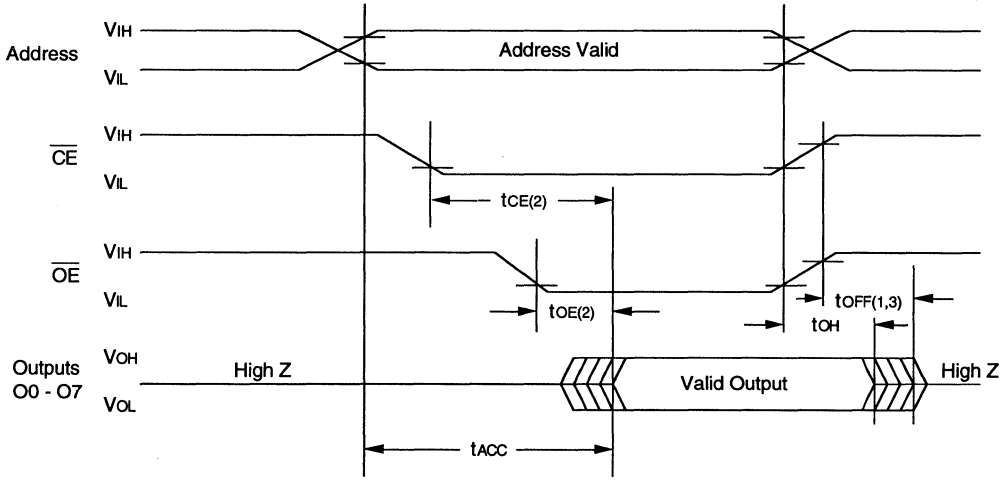
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C
Automotive: Tamb = -40°C to 125°C

Parameter	Sym	27C256-90*		27C256-10*		27C256-12		27C256-15		27C256-20		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC	—	90	—	100	—	120	—	150	—	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	90	—	100	—	120	—	150	—	200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	40	—	45	—	55	—	65	—	75	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	30	0	30	0	35	0	50	0	55	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0	—	0	—	0	—	0	—	0	—	ns	

* -10, -90 AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 1.5V and V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

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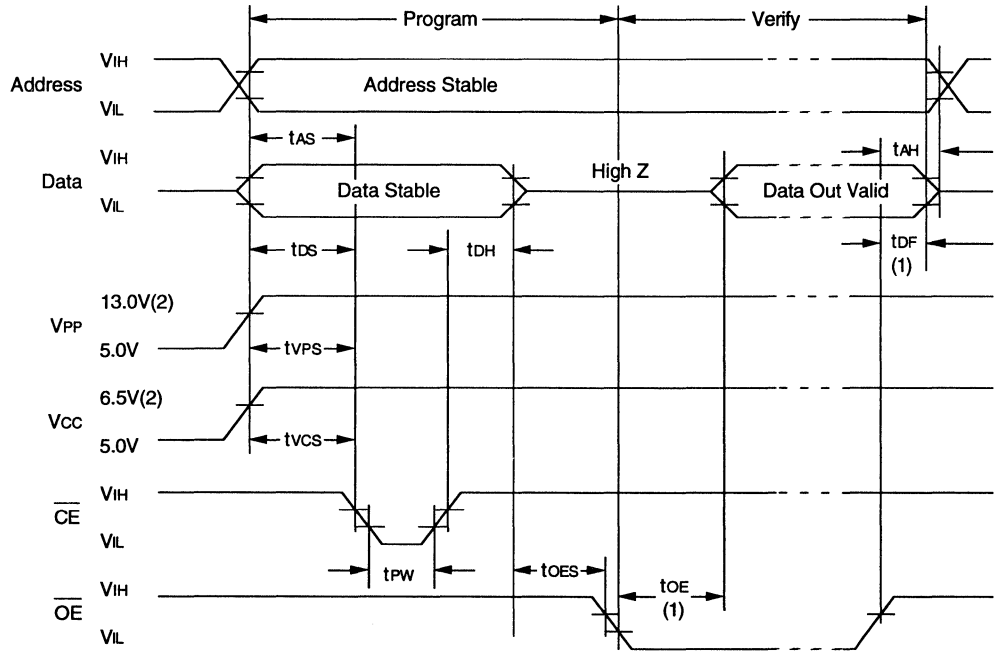
PROGRAMMING DC Characteristics		Ambient Temperature: Tamb = 25°C ±5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V				
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
V_{CC} Current, program & verify	—	I_{CC2}	—	20	mA	Note 1
V_{PP} Current, program	—	I_{PP2}	—	25	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

PROGRAMMING AC Characteristics for Program, Program Verify and Program Inhibit Modes		AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Ambient Temperature: Tamb = 25°C ±5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
V_{PP} Set-Up Time	t_{VPS}	2	—	µs	
Data Valid from $\overline{OE}$	t_{OE}	—	100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µs ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING WAVEFORMS



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5 V ±0.25V, VPP = VH = 13.0V ±0.25V for express algorithm

7

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

When these condition are met, the supply current will drop from 20 mA to 100 µA.

Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and program mode is not defined.

Erase Mode (U.V. Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 µW/cm2 for approximately 20 minutes.

Programming Mode

The express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No over-programming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to proper voltage,
b) V_{PP} is brought to proper V_H level,
c) The $\overline{OE}$ pin is high and
d) the $\overline{CE}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low-going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) The $\overline{CE}$ pin is high and
d) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins.

Identity Mode

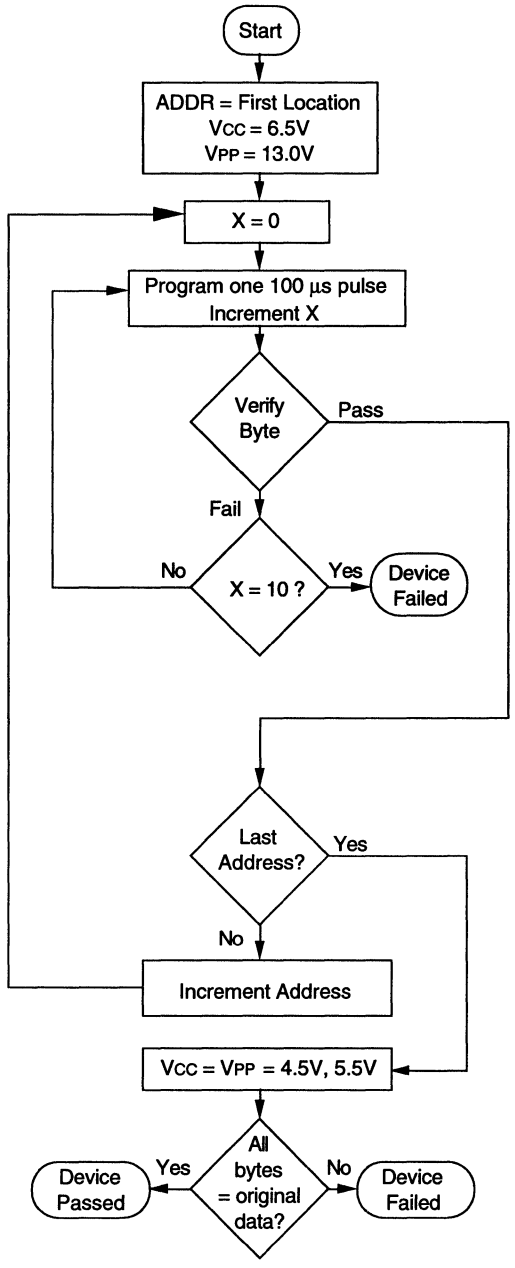
In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	1	1	0	0	8C

* Code subject to change.

FIGURE 1 - PROGRAMMING EXPRESS ALGORITHM

Conditions:
T_{amb} = 25°C ±5°C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C256 - 90 I / TS

Package:	J	CERDIP
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	TS	Thin Small Outline Package (TSOP) 8x20mm
	VS	Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:	-	0°C to 70°C
	I	-40°C to 85°C
	E	-40°C to 125°C
Access Time:	90	90 ns
	10	100 ns
	12	120 ns
	15	150 ns
	20	200 ns
Device:	27C256	256K (32K x 8) CMOS EPROM

MICROCHIP

27HC256

256K (32K x 8) High Speed CMOS EPROM

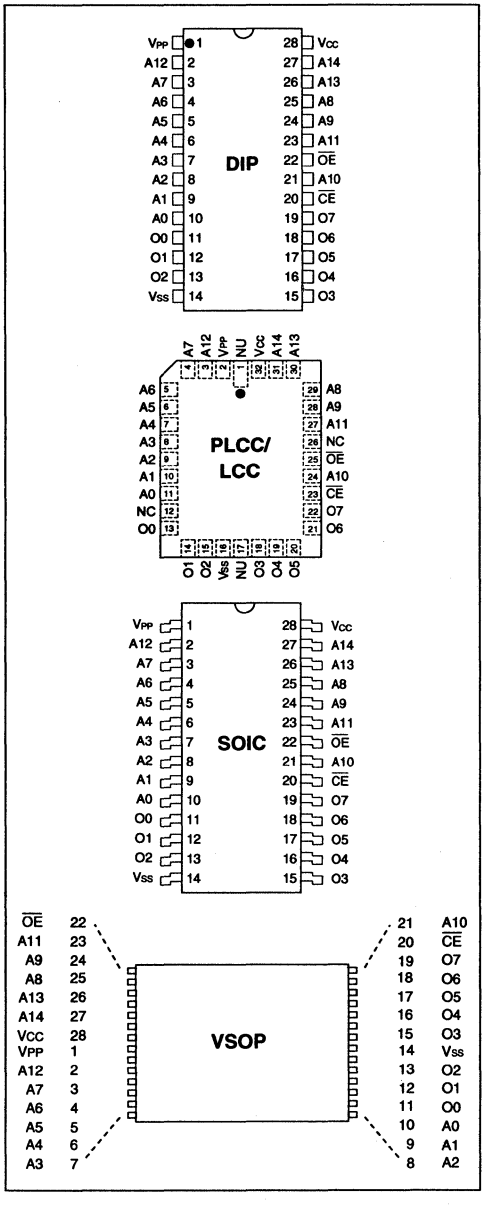
FEATURES

- High speed performance
  - — 55 ns access time available
- CMOS technology for low power consumption
  - — 55 mA active current
  - — 100 µA standby current (low power option)
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Organized in 32K x 8 - JEDEC Standard Pinouts
  - — 28-pin Dual-in-line and SOIC package
  - — 32-pin Chip carrier (leadless or plastic)
  - — 28-pin Very Small Outline package (VSOP)
- Available for the following temperature ranges:
  - —Commercial: 0°C to +70°C
  - —Industrial: -40°C to +85°C
  - —Automotive: -40°C to +125°C

DESCRIPTION

The Microchip Technology Inc. 27HC256 is a CMOS 256K bit electrically Programmable Read Only Memory (EPROM). The device is organized into 32K words of 8 bits each. Advanced CMOS technology allows bipolar speed with a significant reduction in power. A low power option (L) allows further reduction in the standby power requirement to 100 µA The 27HC256 is configured in a standard 256K EPROM pinout which allows an easy upgrade for present 27C256 users. A complete family of packages are offered to provide the utmost flexibility. The 27HC256 allows high performance microprocessors to run at full speed without the need of wait states. CMOS design and processing makes this part suitable for applications where high reliability and reduced power consumption are essential.

PIN CONFIGURATIONS



PIN FUNCTION TABLE	
Name	**Function**
$\overline{A0}$ - A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS
Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V
Temperature under bias ..... -65°C to 125°C
Storage temperature ..... -65°C to 150°C
Maximum exposure to UV 7258Wsec/cm²
ESD protection on all pins ..... 2 KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10% Commercial: Tamb= 0°C to 70°C
Industrial: Tamb= -40°C to 85°C
Extended (Automotive): Tamb= -40°C to 125°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = -0.1V to VCC +1.0V
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -4 mA IOL = 16 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = -0.1V to VCC +0.1V
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I, E	TTL input TTL input	ICC1 ICC2	— —	55 65	mA mA	VCC = 5.5V; VPP = VCC f = 2 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby, Std	C I, E	— —	ICC(S)1	—	35 40	mA mA	
Power Supply Current, Standby, "L" version (low power)	C I, E I, E	TTL input TTL input CMOS input	ICC(S)2	—	2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	VCC -0.7	100 VCC	µA V	VPP = 5.5V Note 2

* Parts: C = Commercial Temperature Range; L = Low Power; I, E = Industrial and Extended Temperature Ranges;

Notes: (1) Active current increases 3 mA per MHz for Commercial part or 5 mA per MHz for Industrial or Extended Temperature parts up to operating frequency.

(2) VCC must be applied simultaneously or before VPP, and removed simultaneously or after VPP.

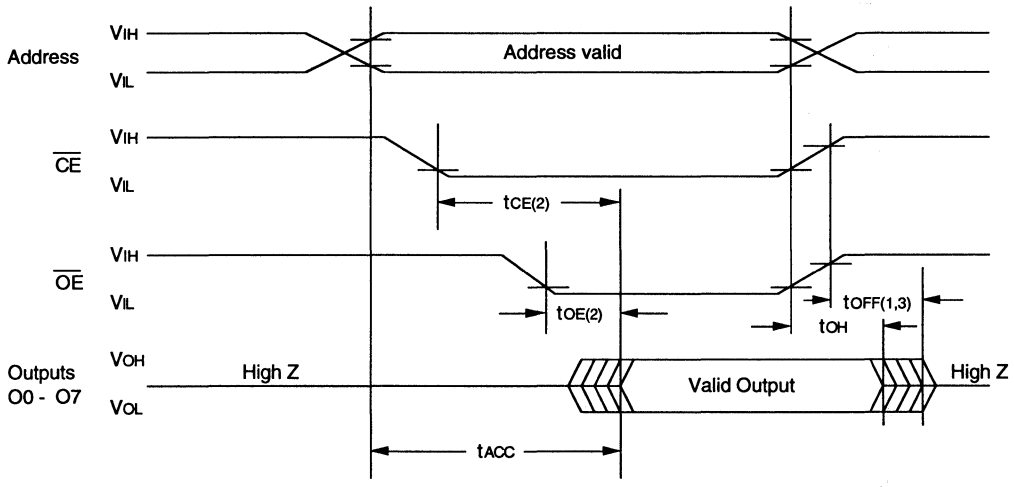
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0.0V; $V_{OH} = V_{OL}$ = 1.5V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 ns
Ambient Temperature: Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C
Extended (Automotive): Tamb = -40°C to 125°C

Parameter	Part*	Sym	27HC256-55		27HC256-70		27HC256-90		Units	Conditions
			Min	Max	Min	Max	Min	Max		
Address to Output Delay	all	tACC	—	55	—	70	—	90	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	L S	tCE1 tCE2	— —	55 45	— —	70 45	— —	90 50	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	all	tOE	—	30	—	35	—	40	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ to O/P High Impedance	all	tOFF	0	25	0	30	0	35	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	all	tOH	0	—	0	—	0	—	ns	

* Parts: S = Standard Power; L = Low Power

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

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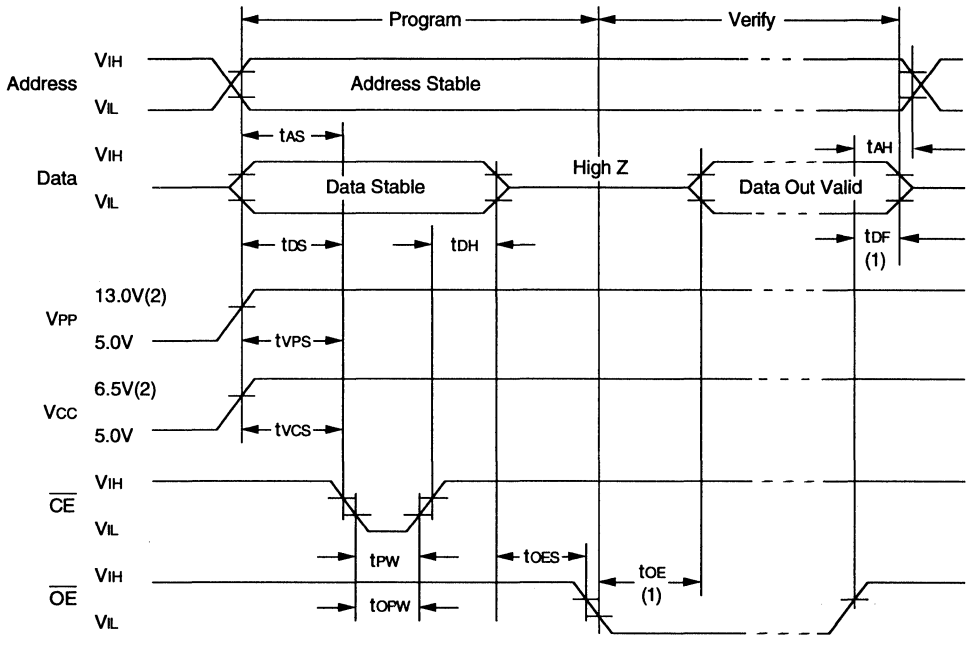
PROGRAMMING **DC Characteristics**		Ambient Temperature: Tamb = 25°C ±5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V				
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = OV to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -4 mA I_{OL} = 16 mA
V_{CC} Current, program & verify	—	I_{CC}	—	55	mA	
V_{PP} Current, program	—	I_{PP}	—	30	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

PROGRAMMING **AC Characteristics** for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V Ambient Temperature: Tamb = 25°C ±5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
V_{PP} Set-Up Time	t_{VPS}	2	—	µs	
Data Valid from $\overline{OE}$	t_{OE}	—	100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µs ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING WAVEFORMS



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for express algorithm

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FUNCTIONAL DESCRIPTION

The 27HC256 has the following functional modes:

—Operation: The 27HC256 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.

—Programming: To receive its permanent data, the 27HC256 must be programmed. Both a program and program/verify procedure are available. It can be programmed with the "Express" algorithm.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

Operation

- Read
- Standby
- Output Disable

For the general characteristics in these operation modes, refer to the table above.

Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC256's memory data is accessed when

— the chip is enabled by setting the $\overline{CE}$ pin low.
— the data is gated to the output pins by setting the $\overline{OE}$ pin low.

For Read operations on the Low Power version, once the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). A faster $\overline{CE}$ access time (t_{CE}) is available on the standard part to provide the additional time for decoding the $\overline{CE}$ signal. Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}$.

Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and a program mode is not defined. When these conditions are met, the supply current will drop from 55 mA to 100 µA on the low power part, and to 35 mA on the standard part.

Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the $\overline{OE}$ pin is high, and the program mode is not defined.

Programming Algorithms

The Express algorithm has been developed to improve programming throughput times in a production environment. Up to 10 pulses of 100 µsec each are applied until the byte is verified. No over-programming is required. A flowchart of this algorithm is shown in Figure 1.

The programming mode is entered when:

a) V_{CC} is brought to the proper level
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low

Since the erased state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A14, and the data is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that memory location.

Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{CE}$ pin is high
d) the $\overline{OE}$ line is low

Inhibit Mode

When Programming multiple devices in parallel with different data only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed, and all other devices with $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

Identity Mode

In this mode specific data is read from the device that identifies the manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ pins must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

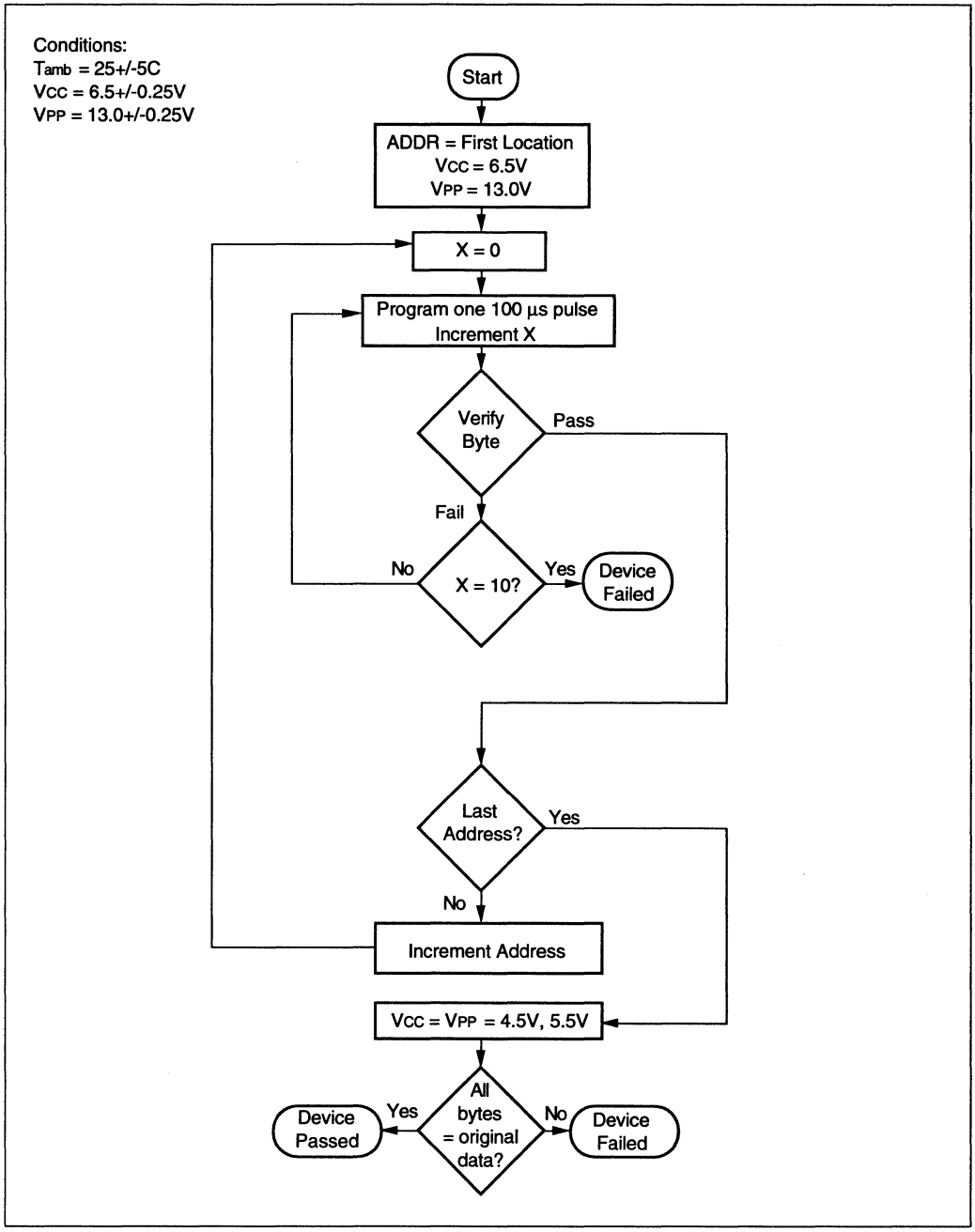
Pin ⟶	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type	V_{IH}	1	0	0	1	0	1	0	0	94

Erasure

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state when exposed to ultraviolet light at wavelengths ≤ 4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537 Å with an intensity of 12,000µW/cm² at 1". The erasure time at that distance is about 15 to 20 min.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

FIGURE 1 - PROGRAMMING EXPRESS ALGORITHM



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing, or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27HC256 L - 55 I / SO

Package:		J	Cerdip DIP
		K	Ceramic Leadless Chip Carrier
		L	PLCC
		P	Plastic DIP
		SO	Plastic SOIC
		VS	Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:		-	0°C to +70°C
		I	-40°C to +85°C
		E	-40°C to + 125°C
Access Time:		55	55 ns
		70	70 ns
		90	90 ns (SOIC only)
Power Type:		-	Standard Power
		L	Low Power
Device:	27HC256		256K (32K x 8) High Speed EPROM

MICROCHIP

27LV256

256K (32K x 8) Low Voltage CMOS EPROM

FEATURES

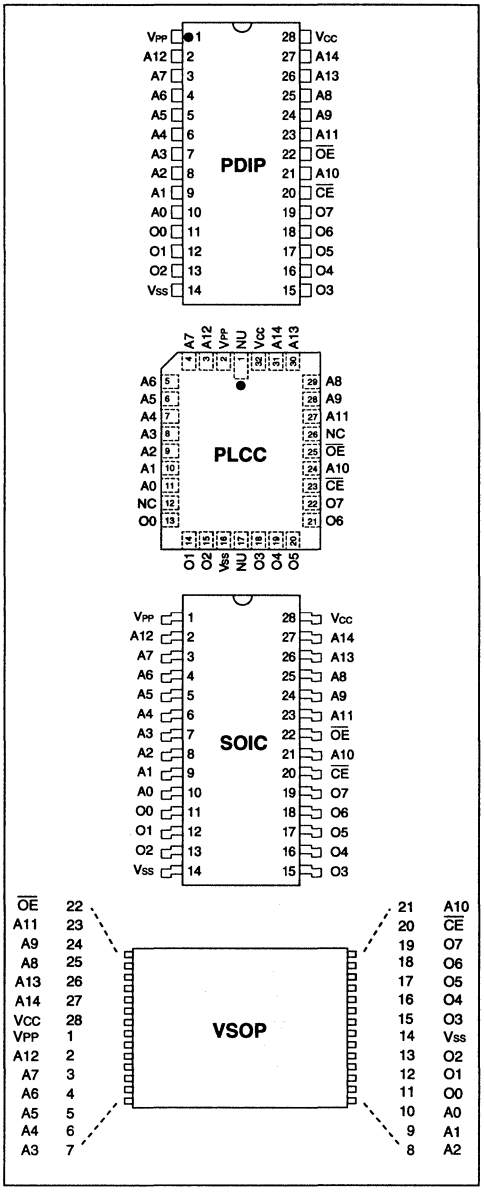
- Wide voltage range 3.0V to 5.5V
- High speed performance
  - — 200 ns access time available at 3.0V
- CMOS Technology for low power consumption
  - — 8 mA Active current at 3.0V
  - — 20 mA Active current at 5.5V
  - — 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "Express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  - — 28-pin Dual-in-line package
  - — 32-pin PLCC package
  - — 28-pin SOIC package
  - — 28-pin VSOP package
  - — Tape and reel
- Available for extended temperature ranges:
  - — Commercial: 0°C to 70°C
  - — Industrial: -40°C to 85°C

DESCRIPTION

The Microchip Technology Inc. 27LV256 is a low voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as a 32K x 8 (32K-Byte) non-volatile memory product. The 27LV256 consumes only 8 mA maximum of active current during a 3.0 volt read operation therefore improving battery performance. This device is designed for very low voltage applications where conventional 5.0 volt only EPROMS can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200 ns at 3.0V. This device allows systems designers the ability to use low voltage non-volatile memory with todays' low voltage microprocessors and peripherals in battery powered applications.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PIN CONFIGURATIONS



PIN FUNCTION TABLE

Name	Function
A0 - A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V or +3V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14.0V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC + 1.0V
Storage temperature ..... -65°C to 150°C
Ambient temp. with power applied ..... -65°C to 125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10% or 3.0V where indicated
Commercial: Tamb= 0°C to 70°C
Industrial: Tamb= -40°C to 85°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V;Tamb= 25°C; f = 1 MHz
Power Suppy Current, Active	C I	TTL input TTL input	ICC1 ICC2	— —	20 @ 5.0V 8 @ 3.0V 25 @ 5.0V 10 @ 3.0V	mA mA mA mA	VCC = 5.5V; VPP = VCC; f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	ICC(S)	—	1 @ 3.0V 2 @ 3.0V 100 @ 3.0V	mA mA µA	 $\overline{CE}$ = VCC ±0.2V

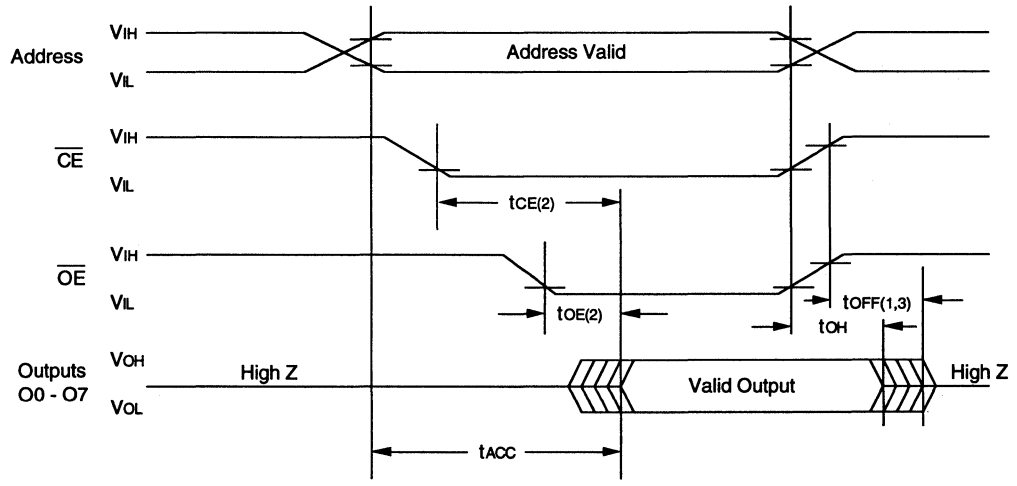
* Parts: C = Commercial Temperature Range
I = Industrial Temperature Range
Notes: (1) Active current increases 5 mA per MHz up to operating frequency for all temperature ranges.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 10 ns
Ambient Temperature: Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C

Parameter	Sym	27LV256-20		27LV256-25		27LV256-30		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	200	—	250	—	300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	200	—	250	—	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	100	—	125	—	125	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	50	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	t_{OH}	0	—	0	—	0	—	ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

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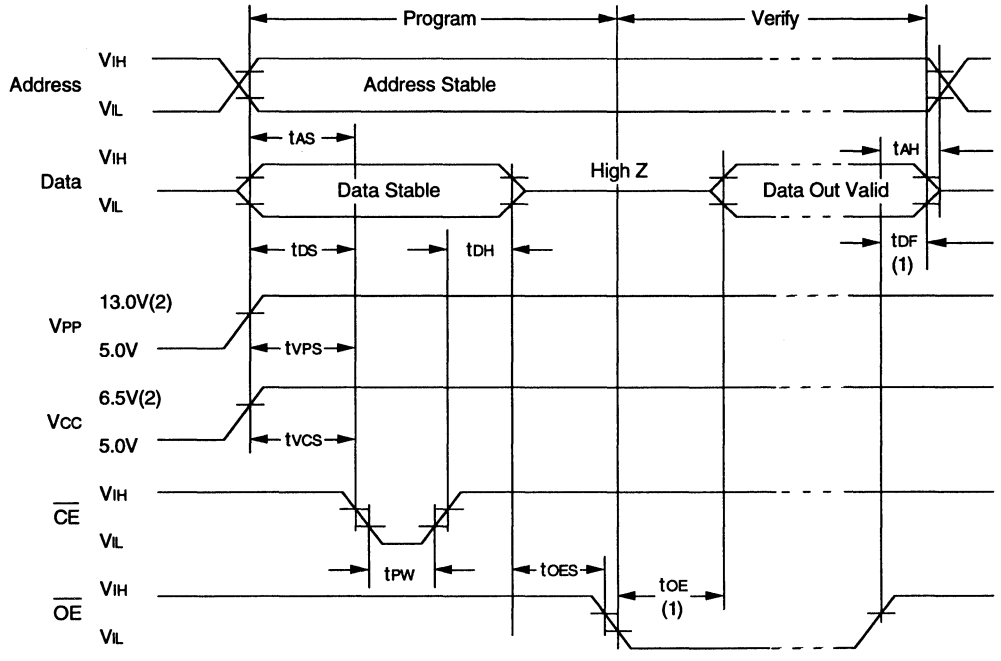
PROGRAMMING **DC Characteristics**		Ambient Temperature: Tamb = 25°C ±5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V				
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
V_{CC} Current, program and verify	—	I_{CC2}	—	20	mA	Note 1
V_{PP} Current, program	—	I_{PP2}	—	25	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

PROGRAMMING **AC Characteristics** for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Ambient Temperature: Tamb = 25°C ±5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
V_{PP} Set-Up Time	t_{VPS}	2	—	µs	
Data Valid from $\overline{OE}$	t_{OE}	—	100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µs ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING WAVEFORMS



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for express algorithm

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MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and program mode is not defined.

Programming Mode

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No over-programming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to proper voltage,
b) V_{PP} is brought to proper V_H level,
c) The $\overline{OE}$ pin is high and
d) the $\overline{CE}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low-going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) The $\overline{CE}$ pin is high and
d) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins.

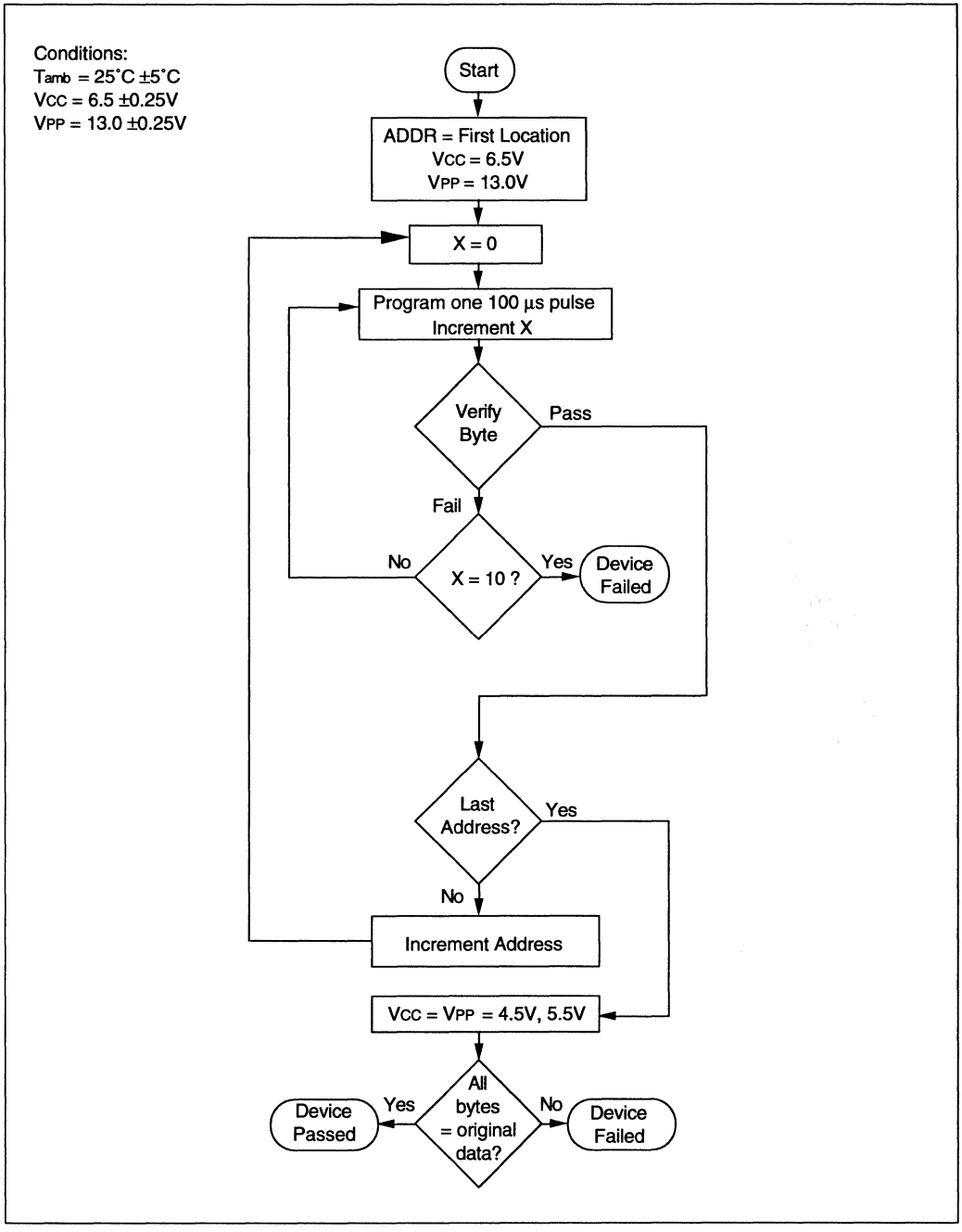
Identity Mode

In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	1	1	0	0	8C

* Code subject to change.

FIGURE 1 - PROGRAMMING EXPRESS ALGORITHM



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27LV256 - 25 I / P

Package:		L	Plastic Leaded Chip Carrier
		P	Plastic DIP
		SO	Plastic SOIC
		VS	Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:		-	0°C to 70°C
		I	-40°C to 85°C
Access Time:		20	200 ns
		25	250 ns
		30	300 ns
Device:	27LV256		256K (32K x 8) Low Voltage CMOS EPROM

MICROCHIP

27HC1616

256K (16K x 16) High Speed CMOS EPROM

FEATURES

- 16 bit configuration
- High speed performance
  —55 ns access time available
- CMOS Technology for low power consumption
  —90 mA Active current
  —50 mA Standby current
- WordWide architecture offers space saving over Bytewide memories
- Organized 16K x 16: JEDEC standard pinouts
  —40-Pin ceramic dual in line package
  —44-Pin ceramic leadless chip carrier
- Temperature range available:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C

DESCRIPTION

The Microchip Technology Inc. 27HC1616 is a CMOS 16K x 16 (256K) Programmable Read Only Memory. The device operates at Bipolar PROM speeds but uses far less current than any Bipolar PROM. The 27HC1616 is an excellent choice for any application requiring blazing speeds and low power consumption. The word wide (16 bit) architecture can replace two 8 bit EPROMS in any 16 bit application saving valuable printed circuit space and components costs. Typical applications for the 27HC1616 include automotive systems control, high speed modems, digital signal processing, or any application that uses the 80386, 68030, 29000, etc. high performance microprocessors.

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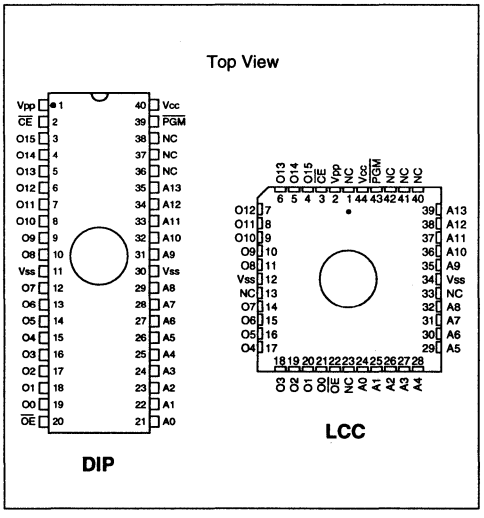
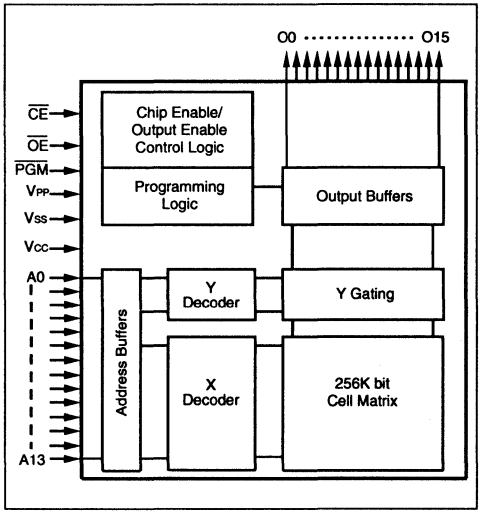
PIN CONFIGURATION



BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0 - A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
PGM	Program Enable
VPP	Programming Voltage
O0 - O15	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14.0V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V
Temperature under bias ..... -65°C to 125°C
Storage temperature ..... -65°C to 150°C
ESD protection on all pins 2KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0°C to 70°C
Industrial: Tamb= -40°C to 85°C

Parameter	Part	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = -0.1 to VCC + 1.0V
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = - 2 mA IOL = 8 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = -0.1 to VCC + 0.1V
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V;Tamb= 25°C; f = 1 MHz
Power Supply Current, Active	all	TTL input	ICC	—	90	mA	VCC = 5.5V; VPP = VCC f = 2 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	all	—	ICC	—	50	mA	
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

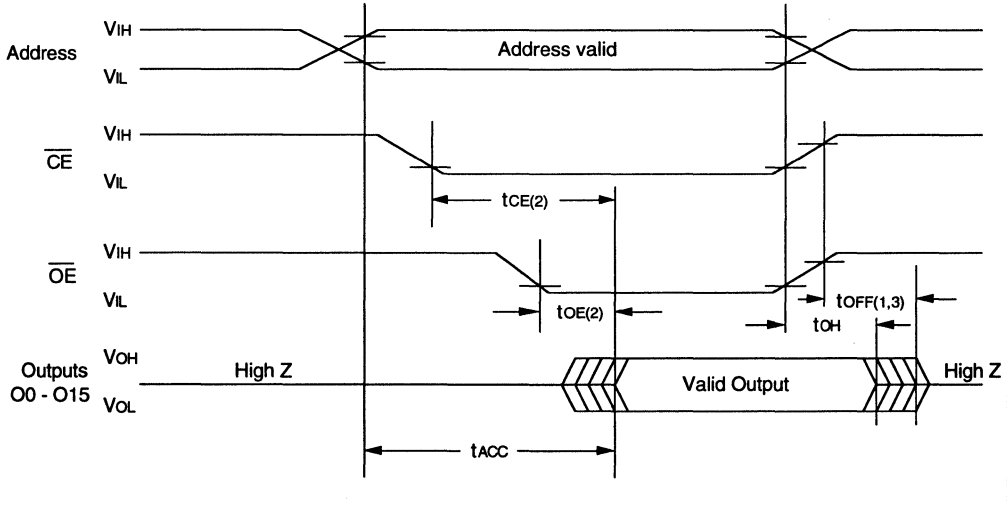
Notes: (1) Active current increases 2 mA per MHz up to operating frequency.
(2) VCC must be applied simultaneously or before VPP and be removed simultaneously or after VPP.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0.0V; $V_{OH} = V_{OL}$ = 1.5V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 ns
Ambient Temperature: Commercial: Tamb= 0°C to 70°C
Industrial: Tamb= -40°C to 85°C

Parameter	Part	Sym	27HC1616-55		27HC1616-70		Units	Conditions
			Min	Max	Min	Max		
Address to Output Delay	all	t_{ACC}	—	55	—	70	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	all	t_{CE2}	—	35	—	45	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	all	t_{OE}	—	30	—	35	ns	$\overline{CE} = V_{IL}$
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	all	t_{OFF}	0	20	0	25	ns	
Output Hold from Address CE or OE, whichever occurs first	all	t_{OH}	0	—	0	—	ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

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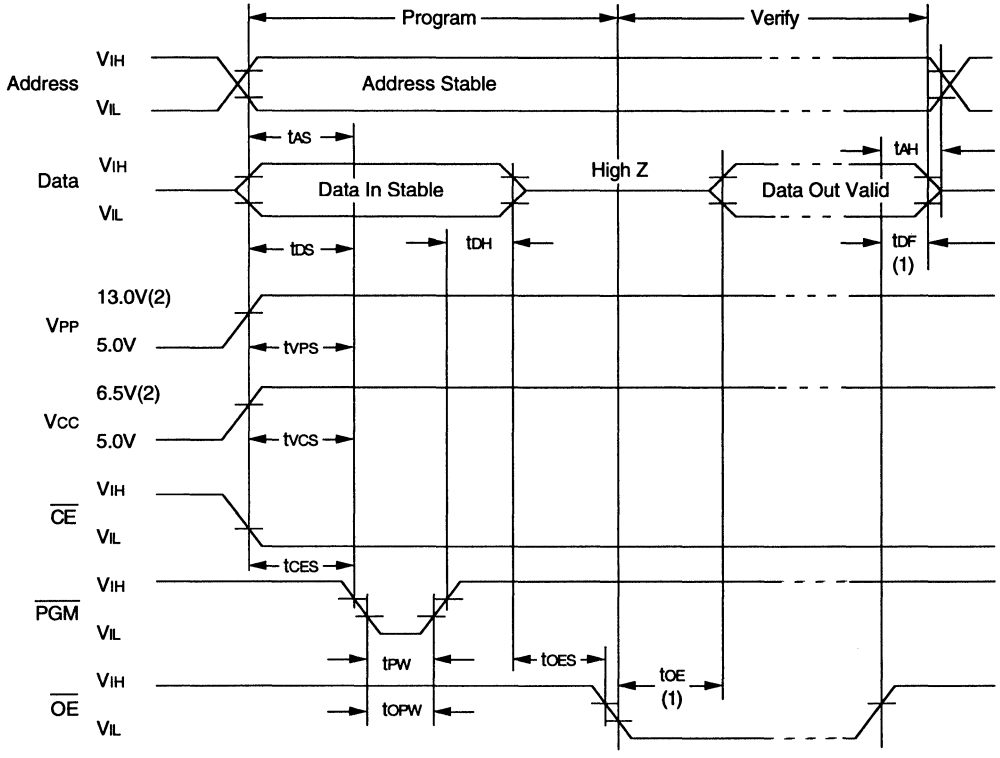
PROGRAMMING DC Characteristics	Ambient Temperature: 25°C ±5°C For V_{PP} and V_{CC} Voltages refer to Programming Algorithm					
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = -.1V to V_{CC} + 1.0V
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4 —	 0.45	V V	I_{OH} = - 2 mA I_{OL} = 8 mA
V_{CC} Current, program & verify	—	I_{CC}	—	90	mA	Note 1
V_{PP} Current,program	—	I_{PP}	—	50	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

PROGRAMMING AC Characteristics for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V and V_{OL} = 0.8V Ambient Temperature: 25°C ±5°C For V_{PP} and V_{CC} Voltages, refer to Programming Algorithm				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
V_{PP} Set-Up Time	t_{VPS}	2	—	µs	
Data Valid from $\overline{OE}$	t_{OE}	—	100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µs ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) tDF and tOE are characteristics of the device but must be accomodated by the programmer
(2) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for express algorithm

FUNCTIONAL DESCRIPTION

The 27HC1616 has the following functional modes:

—Operation: The 27HC1616 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.

—Programming: To receive its permanent data, the 27HC1616 must be programmed. Both a program and program/verify procedure is available. The Express programming algorithm is recommended.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

For the general characteristics in these operation and programming modes, refer to the table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O15
Read	VIL	VIL	VIH	VCC	X	Dout
Program	VIL	VIH	VIL	VH	X	Din
Program Verify	VIH	VIL	VIH	VH	X	Dout
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	X	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care
VH = 12.0 ±0.5V

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OPERATION

Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC1616's memory data is accessed when

—the chip is enabled by setting the $\overline{CE}$ pin low.
—the data is gated to the output pins by setting the $\overline{OE}$ pin low.

Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and the program mode is not defined. When these conditions are met, the supply current will drop from 90 mA to 50 mA.

Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the $\overline{OE}$ pin is high, and the program mode is not defined.

Programming/Verification

The 27HC1616 has to be programmed, and afterward the programmed information verified. Before these operations, the Identity Code can be read to properly set up automated equipment. Multiple devices in parallel can be programmed using the programming and inhibit modes.

Programming Algorithm

The "Express" algorithm has been developed to improve programming through-put times in a production environment. Up to 10 pulses of 100 µs each are applied until the byte is verified. No overprogramming is required. A flowchart of this algorithm is shown in Figure 2.

The programming mode is entered when:

a) V_{CC} is brought to the proper level
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low, and
e) the $\overline{PGM}$ pin is pulsed low.

Since the erased state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A13, and the data is presented to pins O0 - O15. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that memory location.

Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{OE}$ line is low
d) the $\overline{CE}$ pin is low, and
e) the $\overline{PGM}$ line is high.

Inhibit Mode

When Programming multiple devices in parallel with different data only $\overline{PGM}$ needs to be under separate control to each device. By pulsing the $\overline{PGM}$ line low on a particular device, that device will be programmed, and all other devices with corresponding $\overline{PGM}$ or $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

Identity Mode

In this mode specific data is read from the device that identifies the manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ pins must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

Pin ⟶	Input	Output*							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	1	0	1	1	1	97

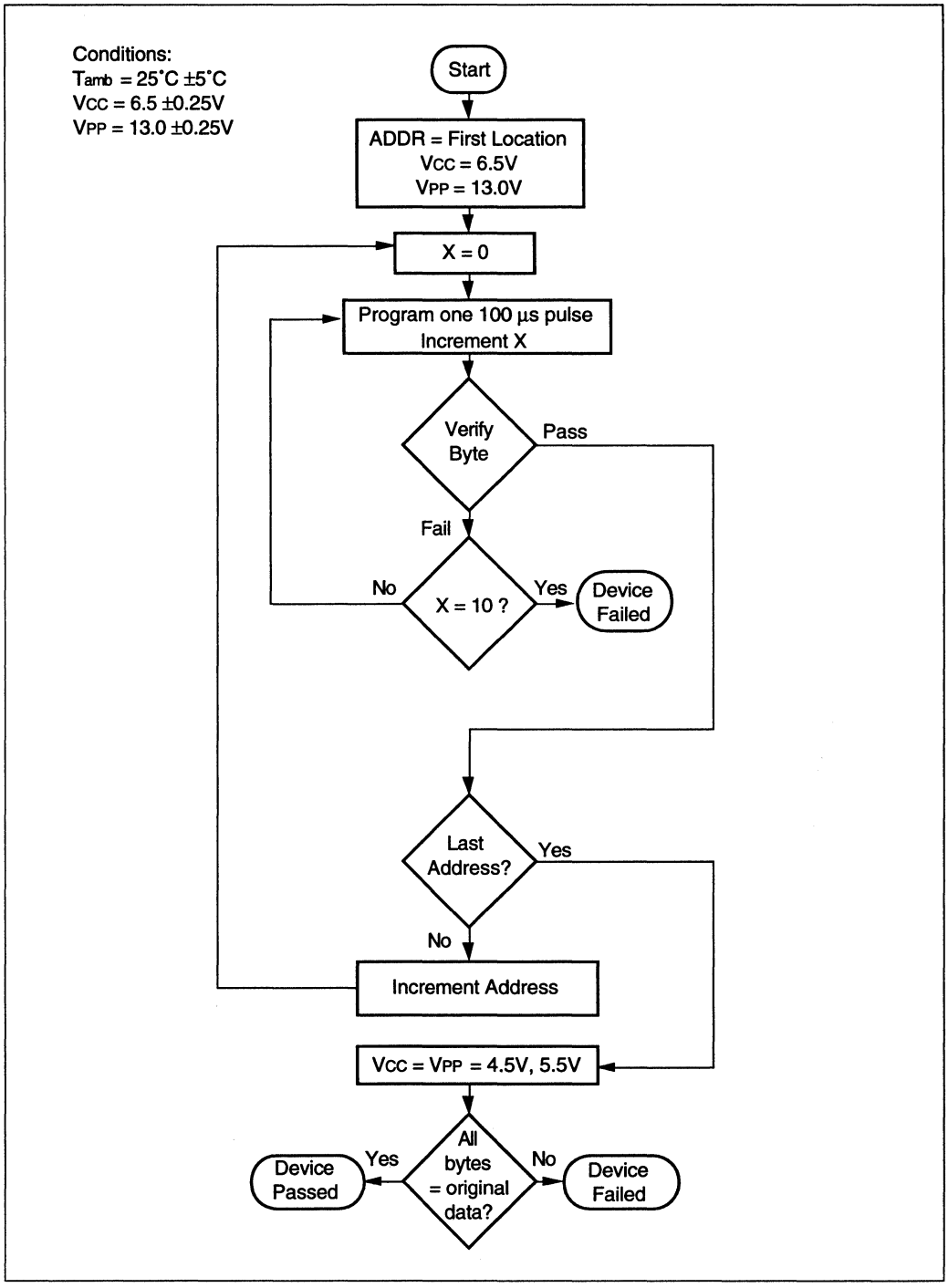
*Code subject to change.
Note: O15 - O8 are 00 for the manufacturer and device type code.

Erasure

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state as a result of being exposed to ultra-violet light at wavelengths ≤ 4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537Å with an intensity of 12,000µW/cm² at 1". The erasure time at that distance is about 15 to 20 minutes.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

FIGURE 1 - PROGRAMMING EXPRESS ALGORITHM



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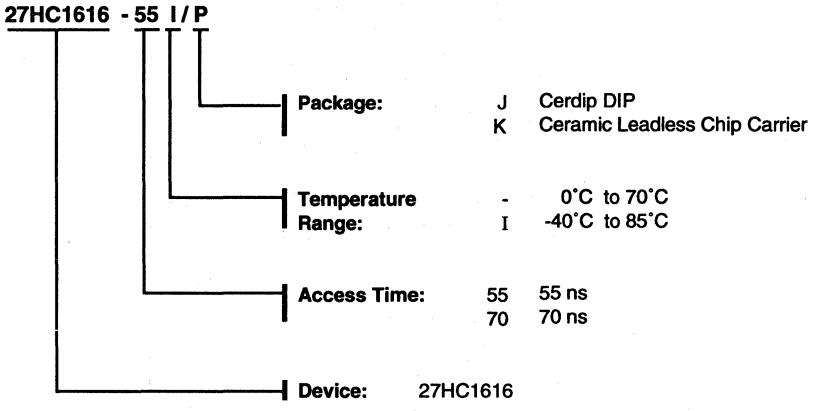
SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



MICROCHIP

27C512

512K (64K x 8) CMOS EPROM

FEATURES

- High speed performance
  - —90 ns access time available
- CMOS Technology for low power consumption
  - —35 mA Active current
  - —100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- High speed express programming algorithm
- Organized 64K x 8: JEDEC standard pinouts
  - —28-pin Dual-in-line package
  - —32-pin Chip carrier (leadless or plastic)
  - —28-pin SOIC package
  - —28-pin TSOP package
  - —Tape and reel
- Available for the following temperature ranges:
  - —Commercial: 0°C to 70°C
  - —Industrial: -40°C to 85°C
  - —Automotive: -40°C to 125°C

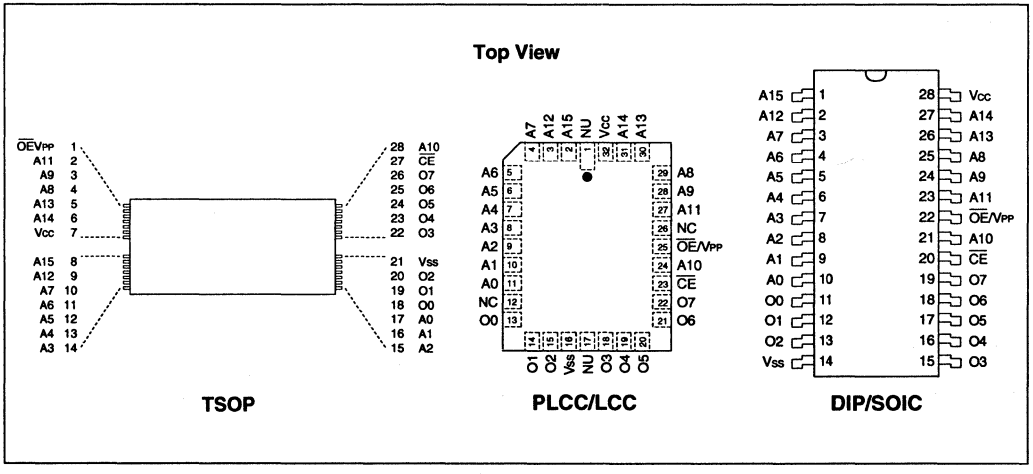
DESCRIPTION

The Microchip Technology Inc. 27C512 is a CMOS 512K bit (electrically) Programmable Read Only Memory. The device is organized into 64K words by 8 bits (64K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90 ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.

A complete family of packages is offered to provide the most flexability in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape or reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

7

PIN CONFIGURATIONS



PIN FUNCTION TABLE	
Name	**Function**
A0 - A15	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/ Programming Voltage
O0 - O7	Data Output
Vcc	+5V Power Supply
Vss	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc and input voltages w.r.t. Vss ..... -0.6V to +7.25V
VPP voltage w.r.t. Vss during programming ..... -0.6V to +14.0V
Voltage on A9 w.r.t. Vss ..... -0.6V to +13.5V
Output voltage w.r.t. Vss ..... -0.6V to Vcc + 1.0V
Storage temperature ..... -65°C to 150°C
Ambient temp. with power applied ..... -65°C to 125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

Vcc = +5V ±10%
Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C
Extended (Automotive): Tamb = -40°C to 125°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	Vcc+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to Vcc
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to Vcc
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V;Tamb= 25°C; f = 1 MHz
Power Supply Current, Active	C I, E	TTL input TTL input	ICC ICC	— —	35 45	mA mA	Vcc = 5.5V f = 1 MHz; $\overline{OE}/V_{PP} = \overline{CE}$ = VIL; Iout = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to Vcc; Note (1)
Power Supply Current, Standby	C I, E C	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	— — —	2 3 100	mA mA µA	 $\overline{CE}$ = Vcc ±0.2V

* Parts: C = Commercial Temperature Range; I, E = Industrial and Extended Temperature Ranges
Notes: (1) Active current increases 2 mA per MHz up to operating frequency for all temperature ranges.

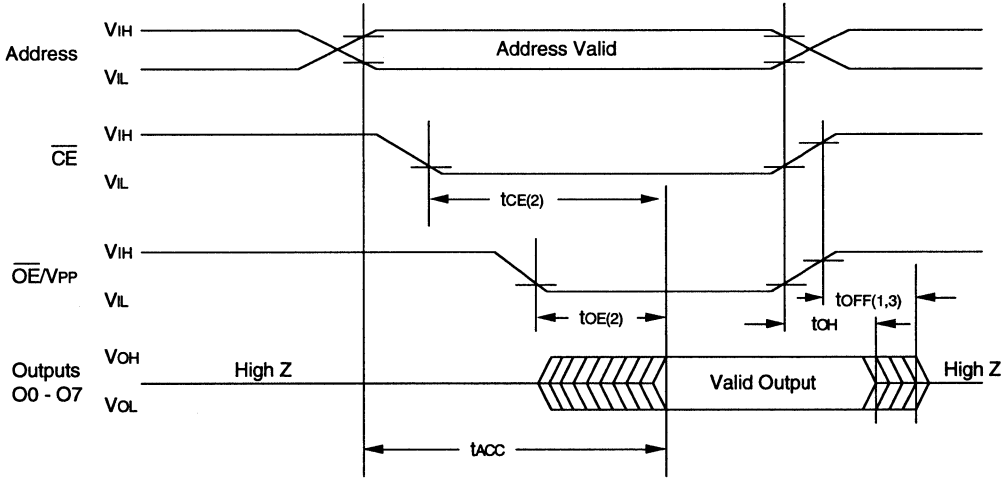
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 2.0V and V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C
Extended (Automotive): Tamb = -40°C to 125°C

Parameter	Sym	27C512-90*		27C512-10		27C512-12		27C512-15		27C512-20		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	90	—	100	—	120	—	150	—	200	ns	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	90	—	100	—	120	—	150	—	200	ns	$\overline{OE}/V_{PP}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	40	—	40	—	50	—	60	—	75	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ to Output High Impedance	t_{OFF}	0	35	0	35	0	40	0	45	0	55	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occured first	t_{OH}	0	—	0	—	0	—	0	—	0	—	ns	

* -90 AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 1.5V and V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

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PROGRAMMING
DC Characteristics

Ambient Temperature: 25°C ±5°C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions (See Note 1)
Input Voltages	Logic "1"	V_{IH}	2.0	V_{CC}+1	V	
	Logic "0"	V_{IL}	-0.1	0.8	V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1"	V_{OH}	2.4		V	I_{OH} = -400 µA
	Logic "0"	V_{OL}	—	0.45	V	I_{OL} = 2.1 mA
V_{CC} Current, program & verify	—	I_{CC2}	—	35	mA	
$\overline{OE}/V_{PP}$ Current, program	—	I_{PP2}	—	25	mA	$\overline{CE}$ = V_{IL}
A9 Product Identification	—	V_{ID}	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before the V_{PP} voltage on $\overline{OE}/V_{PP}$ and removed simultaneously or after the V_{PP} voltage on $\overline{OE}/V_{PP}$.

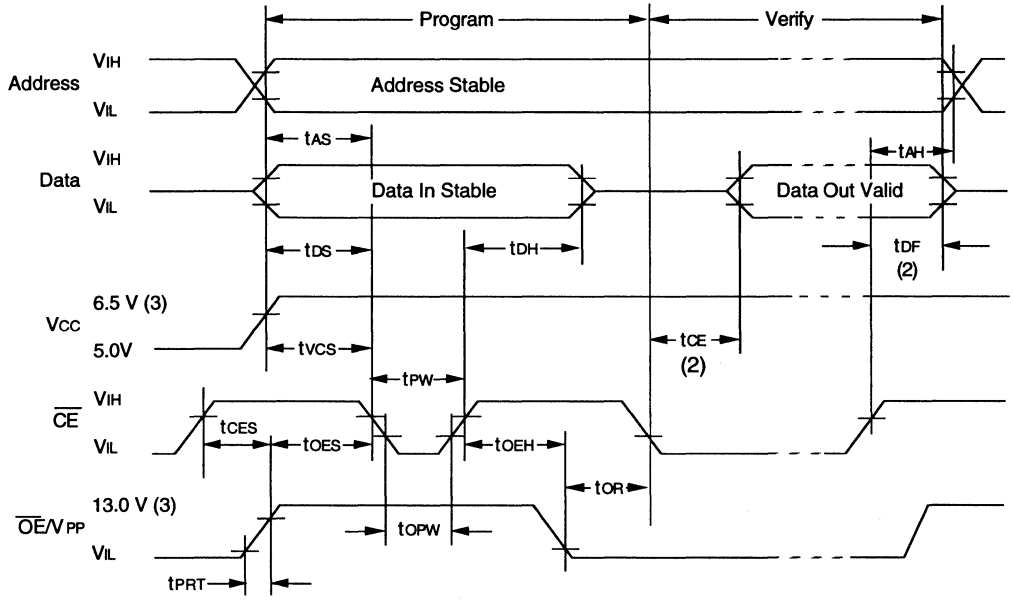
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Ambient Temperature: 25°C ±5°C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
$\overline{OE}$ Hold Time	t_{OEH}	2	—	µs	
$\overline{OE}$ Recovery Time	t_{OR}	2	—	µs	
$\overline{OE}/V_{PP}$ Rise Time During Programming	t_{PRT}	50	—	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µs ± 5%.ɜ is 100 µs ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms (1)



Notes: (1) The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
(2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
(3) V_{CC} = 6.5V ±0.25V, $V_{PP} = V_H$ = 13.0V ±0.5V for express programming algorithm.

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MODES

Operation Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	A9	O0 - O7
Read	V_{IL}	V_{IL}	X	D_{OUT}
Program	V_{IL}	V_H	X	D_{IN}
Program Verify	V_{IL}	V_{IL}	X	D_{OUT}
Program Inhibit	V_{IH}	V_H	X	High Z
Standby	V_{IH}	X	X	High Z
Output Disable	V_{IL}	V_{IH}	X	High Z
Identity	V_{IL}	V_{IL}	V_H	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}/V_{PP}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}/V_{PP}$.

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high and a program mode is not identified.

When this condition is met, the supply current will drop from 35 mA to 100 µA.

Output Enable $\overline{OE}$/VPP

This multifunction pin eliminates bus connection in multiple bus microprcessor systems and the outputs go to high impedance when:

• the $\overline{OE}$/VPP pin is high (VIH).

When a VH input is applied to this pin, it supplies the programming voltage (VPP) to the device.

Erase Mode (UV Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1's" state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

Programming Mode

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. A flowchart of the Express algorithm is shown in Figure 1.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) $\overline{OE}$/VPP is brought to the proper VH level, and
c) $\overline{CE}$ line is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) the $\overline{OE}$/VPP pin is low, and
c) the $\overline{CE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data (although address and data will be available on their input pins).

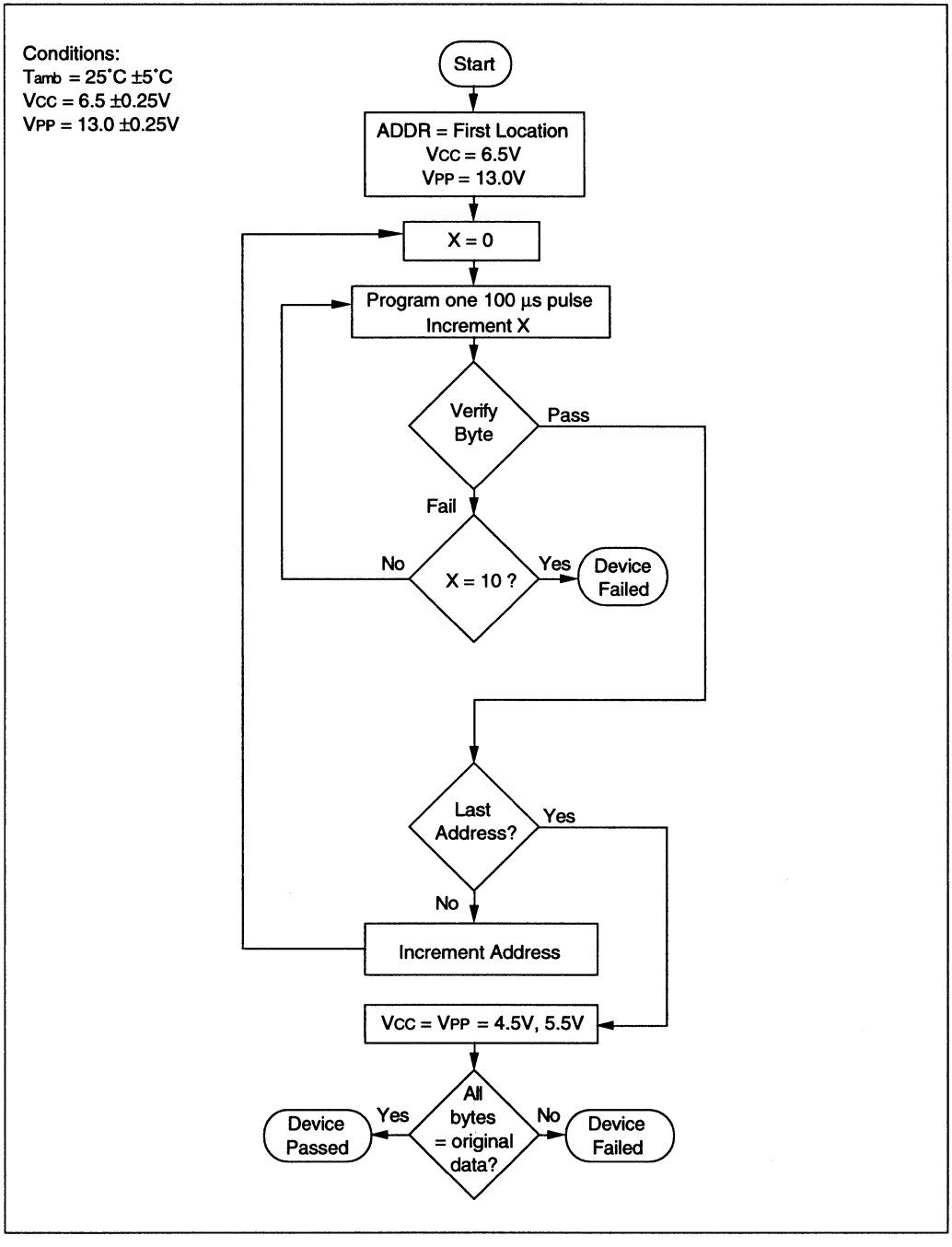
Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc and the device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$/VPP lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	0	0	0	0	1	1	0	1	0D

* Code subject to change.

FIGURE 1 - PROGRAMMING EXPRESS ALGORITHM



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C512 - 90 I / P

Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	TS	Thin Small Outline Package (TSOP) 8x20mm
Temperature Range:	-	0°C to 70°C
	I	-40°C to 85°C
	E	-40°C to 125°C
Access Time:	90	90 ns
	10	100 ns
	12	120 ns
	15	150 ns
	20	200 ns
Device:	27C512	512K (64K x 8) CMOS EPROM

27C512A

512K (64K x 8) CMOS EPROM

FEATURES

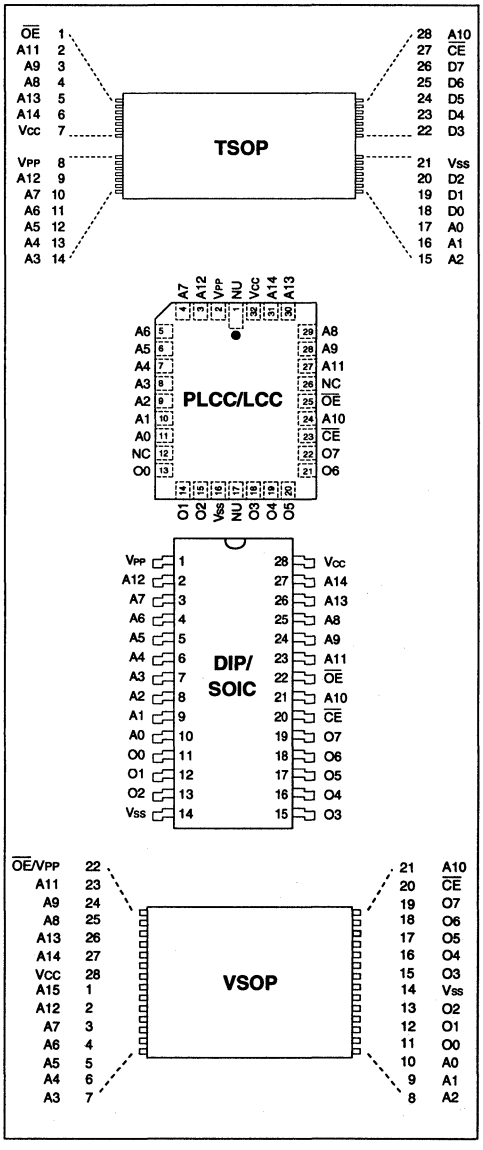
- High speed performance
  - — 70 ns access time available
- CMOS Technology for low power consumption
  - —25 mA Active current
  - —30 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- High speed express programming algorithm
- Organized 64K x 8: JEDEC standard pinouts
  - —28-pin Dual-in-line package
  - —32-pin Chip carrier (leadless or plastic)
  - —28-pin SOIC package
  - —28-pin TSOP package
  - —28-pin VSOP package
  - —Tape and reel
- Available for the following temperature ranges:
  - —Commercial: 0°C to 70°C
  - —Industrial: -40°C to 85°C
  - —Automotive: -40°C to 125°C

DESCRIPTION

The Microchip Technology Inc. 27C512A is a CMOS 512K bit electrically Programmable Read Only Memory (EPROM). The device is organized into 64K words by 8 bits (64K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 70 ns This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape or reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

PIN CONFIGURATIONS



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PIN FUNCTION TABLE	
Name	**Function**
A0 - A15	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/VPP	Output Enable/ Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14.0V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC + 1.0V
Storage temperature ..... -65°C to 150°C
Ambient temp. with power applied ..... -65°C to 125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0°C to 70°C
Industrial: Tamb= -40°C to 85°C
Extended (Automotive): Tamb= -40°C to 125°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I, E	TTL input TTL input	ICC ICC	— —	25 35	mA mA	VCC = 5.5V f = 1 MHz; $\overline{OE}$/VPP = $\overline{CE}$ = VIL; Iout = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note (1)
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	1 2 30	— — —	mA mA µA	 $\overline{CE}$ = VCC ±0.2V

* Parts: C = Commercial Temperature Range; I, E = Industrial and Extended Temperature Ranges
Notes: (1) Active current increases 2 mA per MHz up to operating frequency for all temperature ranges.

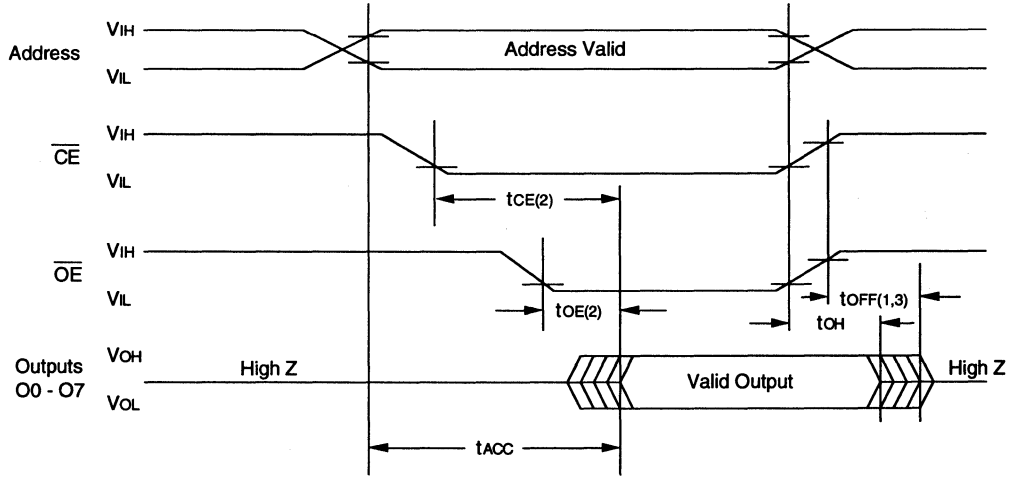
READ OPERATION AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 2.0V and V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 10 ns
Ambient Temperature:
Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C
Extended (Automotive): Tamb = -40°C to 125°C

Parameter	Sym	27C512-70*		27C512-90*		27C512-10*		27C512-12		27C512-15		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC	—	70	—	90	—	100	—	120	—	150	ns	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	70	—	90	—	100	—	120	—	150	ns	$\overline{OE}/V_{PP}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	30	—	40	—	40	—	50	—	60	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ to Output High Impedance	tOFF	0	30	0	35	0	35	0	40	0	45	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occured first	tOH	0	0	0	—	0	—	0	—	0	—	ns	

* -70/90/10 AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0V; V_{OH} = 1.5V and V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

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PROGRAMMING
DC Characteristics

Ambient Temperature: 25°C ±5°C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions (See Note 1)
Input Voltages	Logic "1"	V_{IH}	2.0	V_{CC}+1	V	
	Logic "0"	V_{IL}	-0.1	0.8	V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1"	V_{OH}	2.4		V	I_{OH} = -400 µA
	Logic "0"	V_{OL}	—	0.45	V	I_{OL} = 2.1 mA
V_{CC} Current, program and verify	—	I_{CC2}	—	35	mA	$\overline{CE}$ = V_{IL}
$\overline{OE}/V_{PP}$ Current, program	—	I_{PP2}	—	25	mA	
A9 Product Identification	—	V_{ID}	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before the V_{PP} voltage on $\overline{OE}/V_{PP}$ and removed simultaneously or after the V_{PP} voltage on $\overline{OE}/V_{PP}$.

PROGRAMMING
AC Characteristics

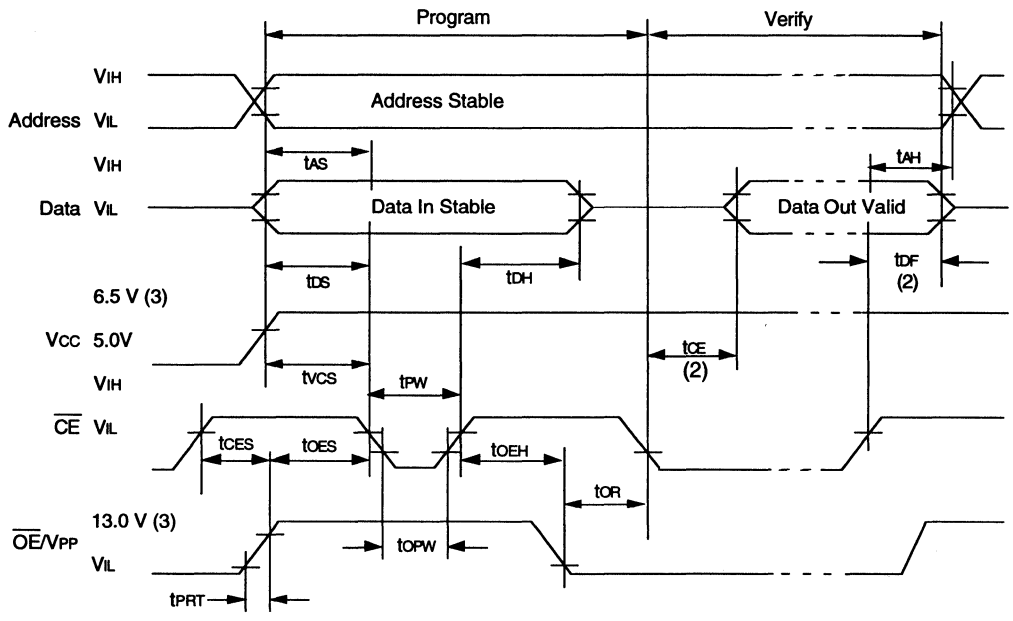
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Ambient Temperature: 25°C ±5°C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
$\overline{OE}$ Hold Time	t_{OEH}	2	—	µs	
$\overline{OE}$ Recovery Time	t_{OR}	2	—	µs	
$\overline{OE}/V_{PP}$ Rise Time During Programming	t_{PRT}	50	—	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µs ± 5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING WAVEFORMS (1)



Notes: (1) The input timing reference level is 0.8V for VIL and 2.0V for VIH.
(2) tDF and tOE are characteristics of the device but must be accommodated by the programmer.
(3) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.5V for express programming algorithm.

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MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$/VPP	A9	O0 - O7
Read	VIL	VIL	X	DOUT
Program	VIL	VH	X	DIN
Program Verify	VIL	VIL	X	DOUT
Program Inhibit	VIH	VH	X	High Z
Standby	VIH	X	X	High Z
Output Disable	VIL	VIH	X	High Z
Identity	VIL	VIL	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$/VPP pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay (tOE) from the falling edge of $\overline{OE}$/VPP.

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high and a program mode is not identified.

When this condition is met, the supply current will drop from 25 mA to 30 μA.

Output Enable $\overline{OE}$/VPP

This multifunction pin eliminates bus connection in multiple bus microprocessor systems and the outputs go to high impedance when:

• the $\overline{OE}$/VPP pin is high (VIH).

When a VH input is applied to this pin, it supplies the programming voltage (VPP) to the device.

Erase Mode (UV Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1's" state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 mW/cm2 for approximately 40 minutes.

Programming Mode

The Express algorithm must be used for best results. It has been developed to improve programming yields and throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. A flowchart of the Express algorithm is shown in Figure 1.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) $\overline{OE}$/VPP is brought to the proper VH level, and
c) $\overline{CE}$ line is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) the $\overline{OE}$/VPP pin is low, and
c) the $\overline{CE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data (although address and data will be available on their input pins).

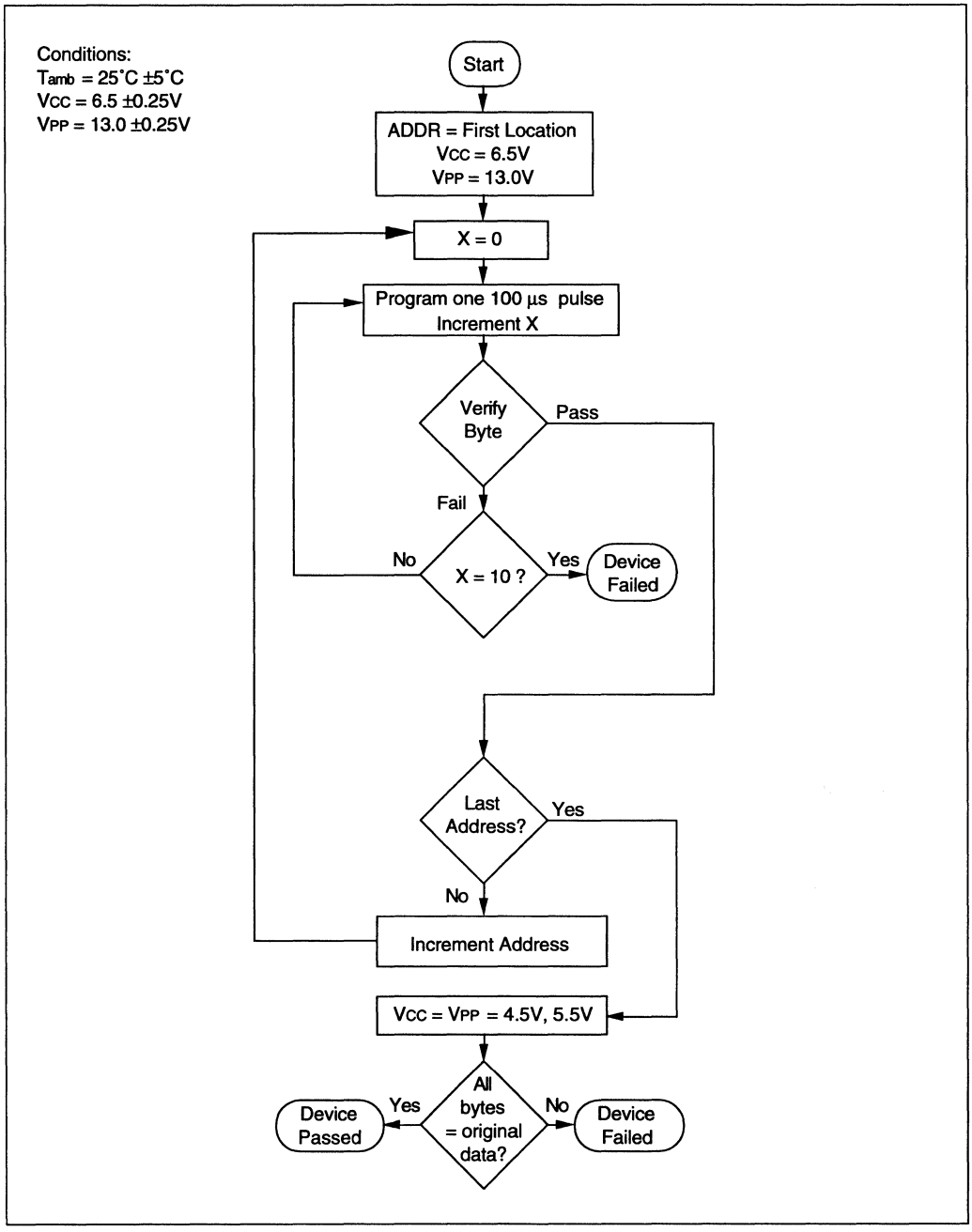
Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and the device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$/VPP lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	1	1	0	0	00

* Code subject to change.

FIGURE 1 - PROGRAMMING EXPRESS ALGORITHM



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C512A - 70 I / P

Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	TS	Thin Small Outline Package (TSOP) 8x20mm
	VS	Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:	-	0°C to 70°C
	I	-40°C to 85°C
	E	-40°C to 125°C
Access Time:	70	70 ns
	90	90 ns
	10	100 ns
	12	120 ns
	15	150 ns
Device:	27C512A	512K (64K x 8) CMOS EPROM

MICROCHIP

27LV512

512K (64K x 8) Low Voltage CMOS EPROM

FEATURES

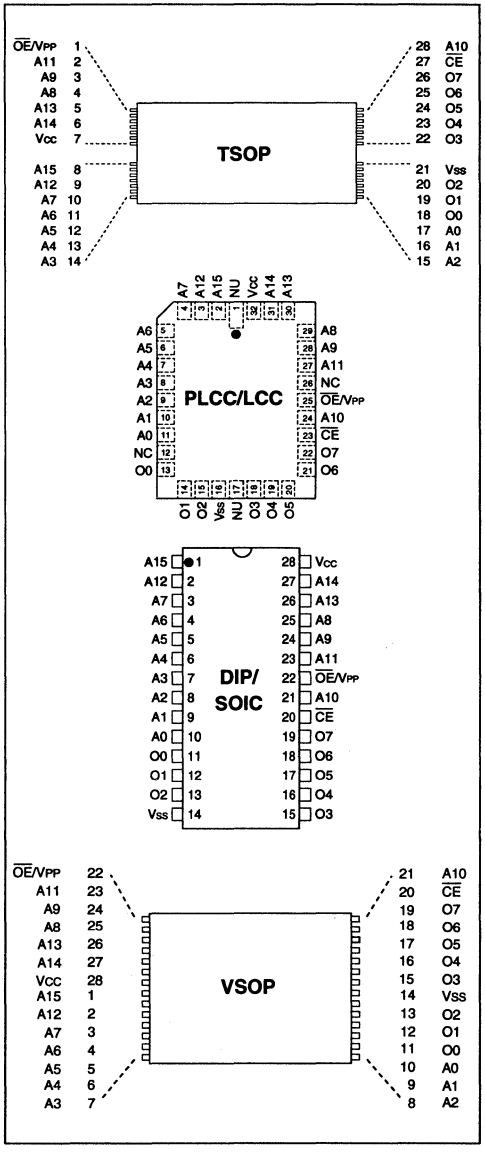
- Wide voltage range 3.0V to 5.5V
- High speed performance
  - — 200 ns access time available at 3.0V
- CMOS Technology for low power consumption
  - — 12 mA Active current at 3.0V
  - — 35 mA Active current at 5.5V
  - — 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- High speed "Express" programming algorithm
- Organized 64K x 8: JEDEC standard pinouts
  - — 28-pin Dual-in-line package
  - — 32-pin PLCC package
  - — 28-pin SOIC package
  - — 28-pin TSOP package
  - — 28-pin VSOP package
  - — Tape and reel
- Available for the following temperature ranges:
  - — Commercial: 0°C to 70°C
  - — Industrial: -40°C to 85°C

DESCRIPTION

The Microchip Technology Inc. 27LV512 is a low-voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as a 64K x 8 (64K-Byte) non-volatile memory product. The 27LV512 consumes only 12 mA maximum of active current during a 3.0 volt read operation therefore improving battery performance. This device is designed for very low-voltage applications where conventional 5.0 volt only EPROMs can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200 ns at 3.0 volts. This device allows systems designers the ability to use low voltage non-volatile memory with today's low-voltage microprocessors and peripherals in battery powered applications.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PIN CONFIGURATIONS



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PIN FUNCTION TABLE	
Name	**Function**
A0 - A15	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/VPP	Output Enable/ Programming Voltage
O0 - O7	Data Output
VCC	+3.0V To +5.5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14.0V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC + 1.0V
Storage temperature ..... -65°C to 150°C
Ambient temp. with power applied ..... -65°C to 125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = 3.0V to 5.5V unless otherwise specified
Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb= 25° C; f = 1 MHz
Power Supply Current, Active	C I	TTL input TTL input	ICC1 ICC2	— —	35 @ 5.0V 12 @ 3.0V 45 @ 5.0V 12 @ 3.0V	mA mA mA mA	VCC = 5.5V f = 1 MHz; $\overline{OE}$/VPP = $\overline{CE}$ = VIL; Iout = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note (1)
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	— — —	1 @ 3.0V 2 @ 3.0V 100 @ 3.0V	mA mA µA	 $\overline{CE}$ = VCC ±0.2V

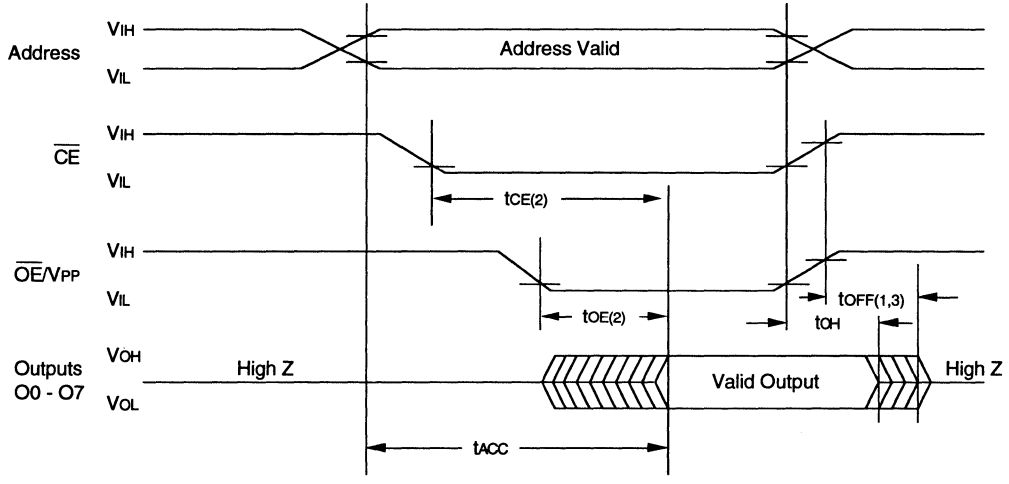
* Parts: C = Commercial Temperature Range; I = Industrial Temperature Range
Note: (1) Active current increases 2 mA per MHz up to operating frequency for all temperature ranges.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 10 ns
Ambient Temperature: Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to 85°C

Parameter	Sym	27LV512-20		27LV512-25		27LV512-30		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	200	—	250	—	300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	200	—	250	—	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	90	—	100	—	125	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	50	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	t_{OH}	0	—	0	—	0	—	ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

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PROGRAMMING
DC Characteristics

Ambient Temperature: 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions (See Note 1)
Input Voltages	Logic "1"	V_{IH}	2.0	V_{CC}+1	V	
	Logic "0"	V_{IL}	-0.1	0.8	V	
Input Current (all inputs)	—	I_L	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1"	V_{OH}	2.4		V	I_{OH} = -400µA
	Logic "0"	V_{OL}	—	0.45	V	I_{OL} = 2.1mA
V_{CC} Current, program & verify	—	I_{CC2}	—	35	mA	
$\overline{OE}/V_{PP}$ Current, program	—	I_{PP2}	—	25	mA	$\overline{CE}$ = V_{IL}
A9 Product Identification	—	V_{ID}	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before the V_{PP} voltage on $\overline{OE}/V_{PP}$ and removed simultaneously or after the V_{PP} voltage on $\overline{OE}/V_{PP}$.

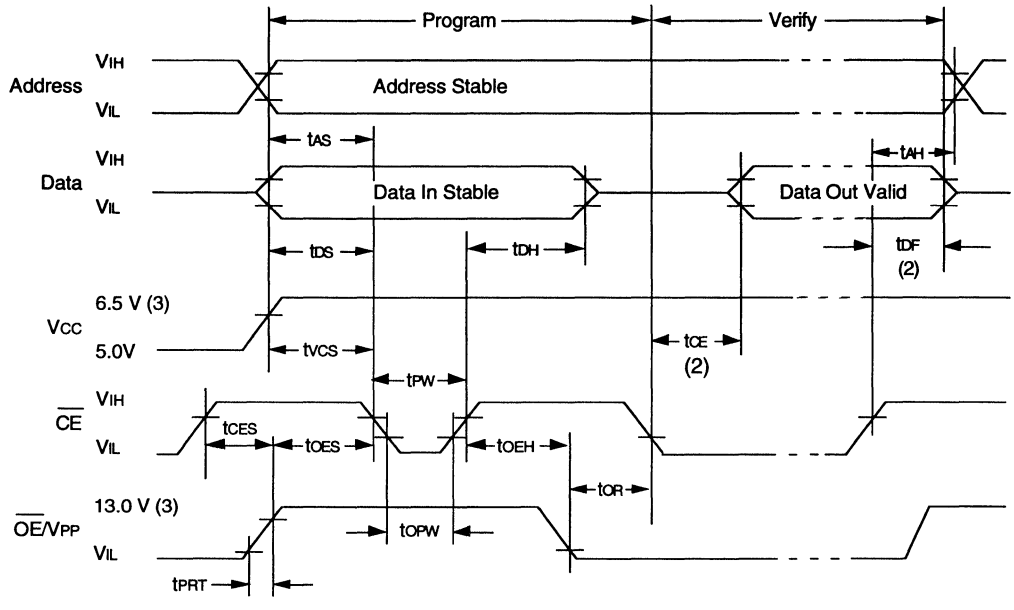
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Ambient Temperature: 25°C ±5°C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
$\overline{OE}$ Hold Time	t_{OEH}	2	—	µs	
$\overline{OE}$ Recovery Time	t_{OR}	2	—	µs	
$\overline{OE}/V_{PP}$ Rise Time During Programming	t_{PRT}	50	—	ns	

Notes: (1) For Express algorithm, initial programming width tolerance is 100 µs ± 5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

READ WAVEFORMS



Notes: (1) The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
(2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
(3) V_{CC} = 6.5V ±0.25V, $V_{PP} = V_H$ = 13.0V ±0.25V for express programming algorithm.

7

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	A9	O0 - O7
Read	V_{IL}	V_{IL}	X	D_{OUT}
Program	V_{IL}	V_H	X	D_{IN}
Program Verify	V_{IL}	V_{IL}	X	D_{OUT}
Program Inhibit	V_{IH}	V_H	X	High Z
Standby	V_{IH}	X	X	High Z
Output Disable	V_{IL}	V_{IH}	X	High Z
Identity	V_{IL}	V_{IL}	V_H	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}/V_{PP}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}/V_{PP}$.

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high and a program mode is not identified.

Output Enable $\overline{OE}$/VPP

This multifunction pin eliminates bus contention in microprocessor based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when:

• the $\overline{OE}$/VPP pin is high (VIH).

When a VH input is applied to this pin, it supplies the programming voltage (VPP) to the device.

Programming Mode

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. A flowchart of the Express algorithm is shown in Figure 1.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) $\overline{OE}$/VPP is brought to the proper VH level, and
c) $\overline{CE}$ line is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) the $\overline{OE}$/VPP pin is low, and
c) the $\overline{CE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data (although address and data will be available on their input pins).

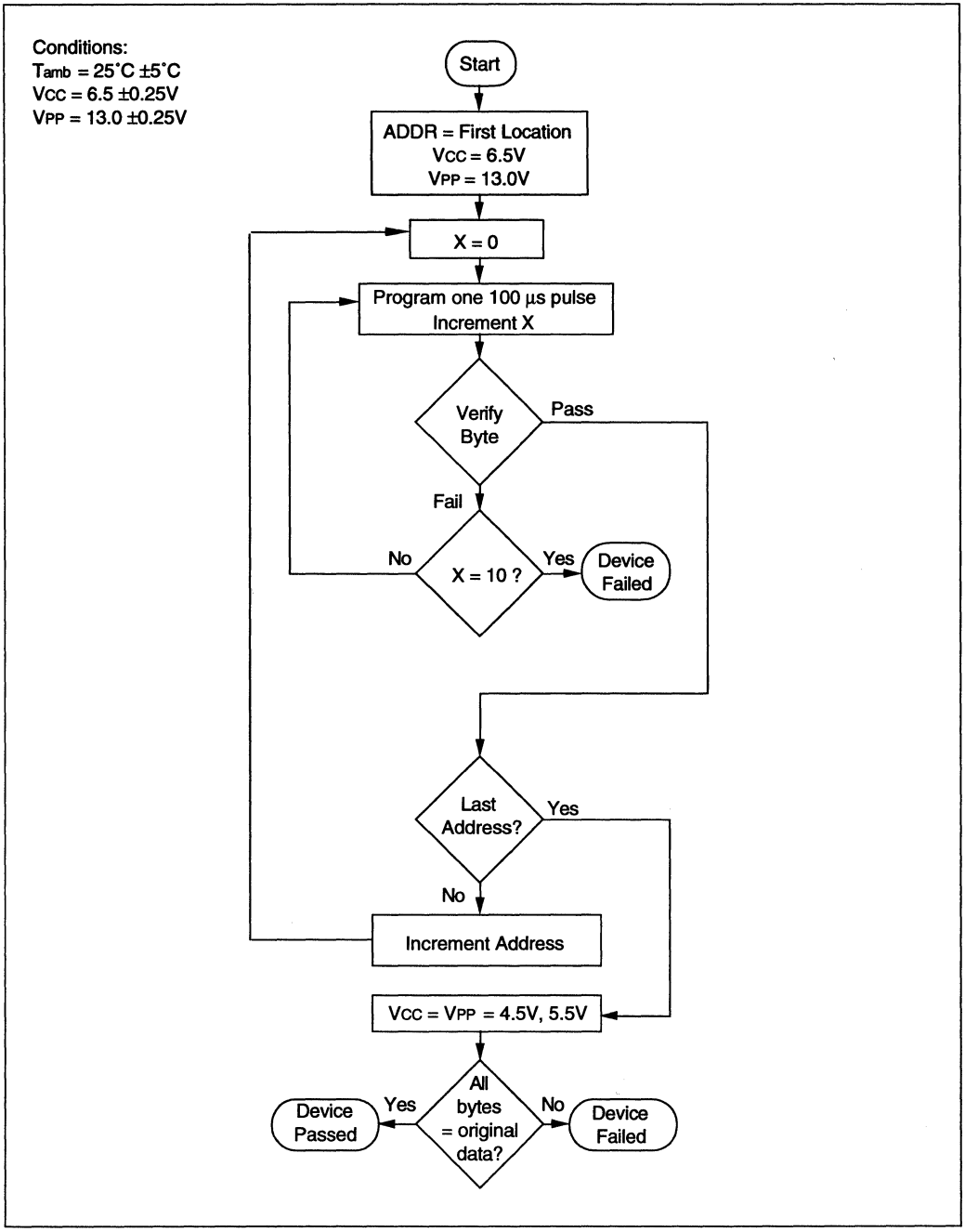
Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc and the device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$/VPP lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	0	0	0	0	1	1	0	1	0D

* Code subject to change.

FIGURE 1 - PROGRAMMING EXPRESS ALGORITHM



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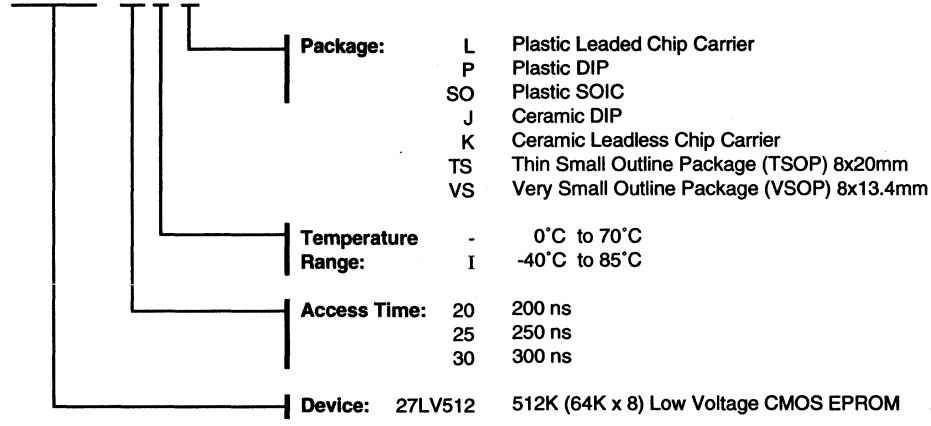
SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



37LV36/65/128

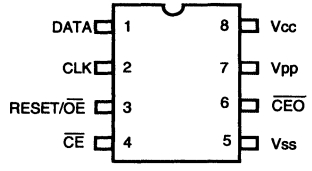
36K/64K/128K Serial EPROM Family

FEATURES

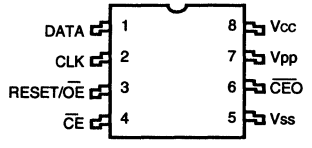
- Operationally equivalent to Xilinx XC1700 family
- Wide voltage range 3.0V to 6.0V
- Maximum read current 10 mA at 5.0 V
- Standby current 100 µA typical
- Industry standard Synchronous Serial Interface / 1 bit per rising edge of clock
- Full Static Operation
- Sequential Read/Program
- Cascadable Output Enable
- 10 MHz Maximum Clock Rate @ 5.0 Vdc
- Programmable Polarity on Hardware Reset
- Programming with industry standard EPROM programmers
- Electrostatic discharge protection > 2000 volts
- 8-pin PDIP/SOIC and 20-pin PLCC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

PIN CONFIGURATIONS

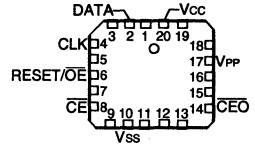
PDIP Package



SOIC Package



PLCC Package

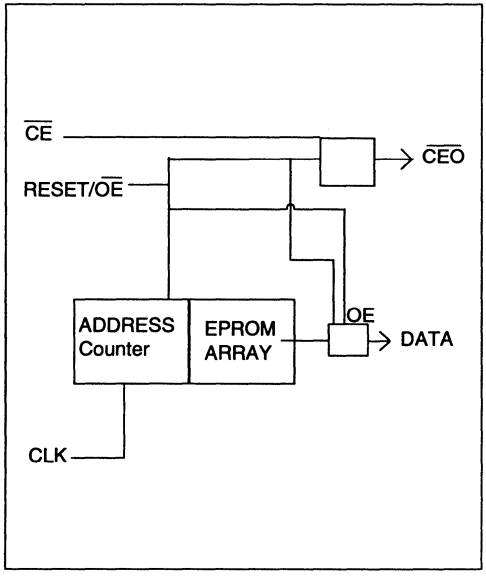


DESCRIPTION

The Microchip Technology Inc. 37LV36/65/128 is a family of Serial OTP EPROM devices organized internally in a x32 configuration. The family also features a cascadable option for increased memory storage where needed. They are suitable for many applications in which look-up table information storage is desirable and provide full static operation in the 3.0V to 6.0V Vcc range. The devices also support the industry standard serial interface to popular RAM-based Field Programmable Gate Arrays (FPGA). Advanced CMOS technology makes this an ideal bootstrap solution for today's high speed RAM based FPGAs. The 37LV36/65/128 family is available in the standard 8-pin plastic DIP, 8-pin SOIC and 20-pin PLCC packages.

DEVICE	BITS	PROGRAMMING WORD
37LV36	36,288	1134 X 32
37LV65	65,536	2048 x 32
37LV128	131,072	4096 x 32

FIGURE 1 - BLOCK DIAGRAM



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

37LVXXX

PACKAGE:	P	Plastic DIP, 8 lead
	SN	Plastic SOIC (150 mil Body), 8 lead
	L	Plastic Leaded Chip Carrier (PLCC), 20 lead
TEMPERATURE RANGE:	Blank	0°C to +70°C
	I	-40°C to +85°C
SHIPPING:	Blank	Tube
	T	Tape and Reel
DEVICE:	37LV128	128K Serial EPROM
	37LV65	64K Serial EPROM
	37LV36	36K Serial EPROM

EPROM Cross Reference Guide

INTRODUCTION

The purpose of this document is to provide a quick way to determine which EPROM parts are mechanical and electrical equivalents to Microchip devices. There is also a listing of manufacturer's part numbering schemes to assist in determining the specifications of a particular part. The cross reference section is broken down by manufacturer and lists all parts from that manufacturer, and the plug compatible Microchip part number.

The one exception to plug compatibility listed in this cross-reference concerns the 28 pin SOIC package. Microchip, along with other manufacturers, make this part in a .300" (JEDEC Standard) width. There are other manufacturers that produce this device in a .330" (EIAJ Standard) wide package. In many cases, the PCB can be laid out to accommodate both versions. The devices that are offered in the .330" package are listed in this reference with an asterisk.

Microchip provides a wide selection of EPROM devices, both from a density and a packaging standpoint. If you are interested in a part that is not listed in this book, please refer to the Microchip data book, or contact your local distributor or sales representative for assistance.

Legend:

AMD®	=	Advanced Micro Devices
T.I.	=	Texas Instruments
SGS	=	ST® SGS-Thomson
Intel®	=	Intel Corporation
Toshiba®	=	Toshiba Corporation
National®	=	National Semiconductor® Corporation
Hitachi®	=	Hitachi Corporation
Atmel®	=	Atmel Corporation

The information contained in this publication regarding competitor devices was obtained from the respective EPROM manufacturer's latest available published technical information and may be subject to updates

AMD is a registered trademark of Advanced Micro Devices.

ST is a registered trademark of SGS-Thomson.

Intel is a registered trademark of Intel Corporation.

Toshiba is a registered trademark of Toshiba Corporation.

National and National Semiconductor are registered trademarks of National Semiconductor Corporation.

Hitachi is a registered trademark of Hitachi Corporation.
Atmel is a registered trademark of Atmel Corporation.
All other trademarks mentioned herein are property of their respective companies.

EPROM CROSS REFERENCE GUIDE

CROSS REFERENCE OF MICROCHIP EPROM PRODUCTS TO THE COMPETITION

HITACHI	DESCRIPTION		MICROCHIP P/N
HN27C256AG-10	UV 256K EPROM,100NS	CERDIP 28	**27C256-10/J**
HN27C256HP-10	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**
HN27C256FP-10T*	OTP 256K EPROM,100NS	SOIC 28	**27C256-10/SO**
HN27C256AG-12	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
HN27C256AG-15	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
HN27C256FP-25T/-30T*	OTP 256K EPROM,200NS	SOIC 28	**27C256-20/SO**
HN27512G-25/-30	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
HN27512P-25/-30	OTP 512K EPROM,200NS	PDIP 28	**27C512-20/P**
HN27C256HG-70/-85	UV 256K HS EPROM,70NS	CERDIP 28	**27HC256-70/J**
HN27C256HP-70/-85	OTP 256K HS EPROM,70NS	PDIP 28	**27HC256-70/P**
HN27C256HFP-85T*	OTP 256K HS EPROM,70NS	SOIC 28	**27HC256-70/SO**

AMD	DESCRIPTION		MICROCHIP P/N
Am27C64-120DC	UV 64K EPROM,120NS	CERDIP 28	**27C64-12/J**
Am27C64-120LC	UV 64K EPROM,120NS	LCC 32	**27C64-12/K**
Am27C64-120JC	OTP 64K EPROM,120NS	PLCC 32	**27C64-12/L**
Am27C64-120PC	OTP 64K EPROM,120NS	PDIP 28	**27C64-12/P**
Am27C64-150DC	UV 64K EPROM,150NS	CERDIP 28	**27C64-15/J**
Am27C64-150LC	UV 64K EPROM,150NS	LCC 32	**27C64-15/K**
Am27C64-150JC	OTP 64K EPROM,150NS	PLCC 32	**27C64-15/L**
Am27C64-150PC	OTP 64K EPROM,150NS	PDIP 28	**27C64-15/P**
Am27C64-200DC	UV 64K EPROM,200NS	CERDIP 28	**27C64-20/J**
Am27C64-200LC	UV 64K EPROM,200NS	LCC 32	**27C64-20/K**
Am27C64-200JC	OTP 64K EPROM,200NS	PLCC 32	**27C64-20/L**
Am27C64-200PC	OTP 64K EPROM,200NS	PDIP 28	**27C64-20/P**
Am27C64-250DC	UV 64K EPROM,250NS	CERDIP 28	**27C64-25/J**
Am27C64-250LC	UV 64K EPROM,250NS	LCC 32	**27C64-25/K**
Am27C64-250JC	OTP 64K EPROM,250NS	PLCC 32	**27C64-25/L**
Am27C64-250PC	OTP 64K EPROM,250NS	PDIP 28	**27C64-25/P**
Am27C64-120DI	UV 64K EPROM,120NS,IND	CERDIP 28	**27C64-12I/J**
Am27C64-150DI	UV 64K EPROM,150NS,IND	CERDIP 28	**27C64-15I/J**
Am27C64-150LI	UV 64K EPROM,150NS,IND	LCC 32	**27C64-15I/K**
Am27C64-150JI	OTP 64K EPROM,150NS,IND	PLCC 32	**27C64-15I/L**
Am27C64-150PI	OTP 64K EPROM,150NS,IND	PDIP 28	**27C64-15I/P**
Am27C64-200DI	UV 64K EPROM,200NS,IND	CERDIP 28	**27C64-20I/J**
Am27C64-200LI	UV 64K EPROM,200NS,IND	LCC 32	**27C64-20I/K**
Am27C64-200JI	OTP 64K EPROM,200NS,IND	PLCC 32	**27C64-20I/L**
Am27C64-200PI	OTP 64K EPROM,200NS,IND	PDIP 28	**27C64-20I/P**
Am27C64-250DI	UV 64K EPROM,250NS,IND	CERDIP 28	**27C64-25I/J**
Am27C64-250LI	UV 64K EPROM,250NS,IND	LCC 32	**27C64-25I/K**
Am27C64-250JI	OTP 64K EPROM,250NS,IND	PLCC 32	**27C64-25I/L**
Am27C64-250PI	OTP 64K EPROM,250NS,IND	PDIP 28	**27C64-25I/P**
Am27C128-120DC	UV 128K EPROM,120NS	CERDIP 28	**27C128-12/J**
Am27C128-120LC	UV 128K EPROM,120NS	LCC 32	**27C128-12/K**
Am27C128-120JC	OTP 128K EPROM,120NS	PLCC 32	**27C128-12/L**
Am27C128-120PC	OTP 128K EPROM,120NS	PDIP 28	**27C128-12/P**
Am27C128-150DC	UV 128K EPROM,150NS	CERDIP 28	**27C128-15/J**
Am27C128-150LC	UV 128K EPROM,150NS	LCC 32	**27C128-15/K**
Am27C128-150JC	OTP 128K EPROM,150NS	PLCC 32	**27C128-15/L**
Am27C128-150PC	OTP 128K EPROM,150NS	PDIP 28	**27C128-15/P**
Am27C128-200DC	UV 128K EPROM,200NS	CERDIP 28	**27C128-20/J**
Am27C128-200LC	UV 128K EPROM,200NS	LCC 32	**27C128-20/K**
Am27C128-200JC	OTP 128K EPROM,200NS	PLCC 32	**27C128-20/L**
Am27C128-200PC	OTP 128K EPROM,200NS	PDIP 28	**27C128-20/P**
Am27C128-250DC	UV 128K EPROM,250NS	CERDIP 28	**27C128-25/J**
Am27C128-250LC	UV 128K EPROM,250NS	LCC 32	**27C128-25/K**
Am27C128-250JC	OTP 128K EPROM,250NS	PLCC 32	**27C128-25/L**
Am27C128-250PC	OTP 128K EPROM,250NS	PDIP 28	**27C128-25/P**
Am27C128-120DI	UV 128K EPROM,120NS,IND	CERDIP 28	**27C128-12I/J**
Am27C128-150DI	UV 128K EPROM,150NS,IND	CERDIP 28	**27C128-15I/J**
Am27C128-150LI	UV 128K EPROM,150NS,IND	LCC 32	**27C128-15I/K**
Am27C128-150JI	OTP 128K EPROM,150NS,IND	PLCC 32	**27C128-15I/L**
Am27C128-150PI	OTP 128K EPROM,150NS,IND	PDIP 28	**27C128-15I/P**
Am27C128-200DI	UV 128K EPROM,200NS,IND	CERDIP 28	**27C128-20I/J**
Am27C128-200LI	UV 128K EPROM,200NS,IND	LCC 32	**27C128-20I/K**

CROSS REFERENCE OF MICROCHIP EPROM PRODUCTS TO THE COMPETITION

AMD (Cont.)	DESCRIPTION	MICROCHIP P/N	
Am27C128-200JI	OTP 128K EPROM,200NS,IND	PLCC 32	**27C128-20I/L**
Am27C128-200PI	OTP 128K EPROM,200NS,IND	PDIP 28	**27C128-20I/P**
Am27C128-250DI	UV 128K EPROM,250NS,IND	CERDIP 28	**27C128-25I/J**
Am27C128-250LI	UV 128K EPROM,250NS,IND	LCC 32	**27C128-25I/K**
Am27C128-250JI	OTP 128K EPROM,250NS,IND	PLCC 32	**27C128-25I/L**
Am27C128-250PI	OTP 128K EPROM,250NS,IND	PDIP 28	**27C128-25I/P**
Am27C256-90DC	UV 256K EPROM,90NS	CERDIP 28	**27C256-90/J**
Am27C256-90LC	OTP 256K EPROM,90NS	PLCC 32	**27C256-90/L**
Am27C256-90JC	OTP 256K EPROM,90NS	PDIP 28	**27C256-90/P**
Am27C256-90PC	OTP 256K EPROM,90NS	SOIC 28	**27C256-90/SO**
Am27C256-100DC	UV 256K EPROM,100NS	CERDIP 28	**27C256-10/J**
Am27C256-100LC	UV 256K EPROM,100NS	LCC 32	**27C256-10/K**
Am27C256-100JC	OTP 256K EPROM,100NS	PLCC 32	**27C256-10/L**
Am27C256-100PC	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**
Am27C256-120DC	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
Am27C256-120LC	UV 256K EPROM,120NS	LCC 32	**27C256-12/K**
Am27C256-120JC	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
Am27C256-120PC	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
Am27C256-150DC	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
Am27C256-150LC	UV 256K EPROM,150NS	LCC 32	**27C256-15/K**
Am27C256-150JC	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
Am27C256-150PC	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
Am27C256-200DC	UV 256K EPROM,200NS	CERDIP 28	**27C256-20/J**
Am27C256-200LC	UV 256K EPROM,200NS	LCC 32	**27C256-20/K**
Am27C256-200JC	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
Am27C256-200PC	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
Am27C256-100DI	UV 256K EPROM,100NS,IND	CERDIP 28	**27C256-10I/J**
Am27C256-100LI	UV 256K EPROM,100NS,IND	LCC 32	**27C256-10I/K**
Am27C256-100JI	OTP 256K EPROM,100NS,IND	PLCC 32	**27C256-10I/L**
Am27C256-100PI	OTP 256K EPROM,100NS,IND	PDIP 28	**27C256-10I/P**
Am27C256-120DI	UV 256K EPROM,120NS,IND	CERDIP 28	**27C256-12I/J**
Am27C256-120LI	UV 256K EPROM,120NS,IND	LCC 32	**27C256-12I/K**
Am27C256-120JI	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
Am27C256-120PI	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
Am27C256-150DI	UV 256K EPROM,150NS,IND	CERDIP 28	**27C256-15I/J**
Am27C256-150LI	UV 256K EPROM,150NS,IND	LCC 32	**27C256-15I/K**
Am27C256-150JI	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
Am27C256-150PI	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
Am27C256-200DI	UV 256K EPROM,200NS,IND	CERDIP 28	**27C256-20I/J**
Am27C256-200LI	UV 256K EPROM,200NS,IND	LCC 32	**27C256-20I/K**
Am27C256-200JI	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**
Am27C256-200PI	OTP 256K EPROM,200NS,IND	PDIP 28	**27C256-20I/P**
Am27C512-90DC	UV 512K EPROM,90NS	CERDIP 28	**27C512-90/J**
Am27C512-90LC	UV 512K EPROM,90NS	LCC 32	**27C512-90/K**
Am27C512-90JC	OTP 512K EPROM,90NS	PLCC 32	**27C512-90/L**
Am27C512-90PC	OTP 512K EPROM,90NS	PDIP 28	**27C512-90/P**
Am27C512-120DC	UV 512K EPROM,120NS	CERDIP 28	**27C512-12/J**
Am27C512-120LC	UV 512K EPROM,120NS	LCC 32	**27C512-12/K**
Am27C512-120JC	OTP 512K EPROM,120NS	PLCC 32	**27C512-12/L**
Am27C512-120PC	OTP 512K EPROM,120NS	PDIP 28	**27C512-12/P**
Am27C512-150DC	UV 512K EPROM,150NS	CERDIP 28	**27C512-15/J**
Am27C512-150LC	UV 512K EPROM,150NS	LCC 32	**27C512-15/K**
Am27C512-150JC	OTP 512K EPROM,150NS	PLCC 32	**27C512-15/L**
Am27C512-150PC	OTP 512K EPROM,150NS	PDIP 28	**27C512-15/P**
Am27C512-200DC	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
Am27C512-200LC	UV 512K EPROM,200NS	LCC 32	**27C512-20/K**
Am27C512-200JC	OTP 512K EPROM,200NS	PLCC 32	**27C512-20/L**
Am27C512-200PC	OTP 512K EPROM,200NS	PDIP 28	**27C512-20/P**
Am27C512-120DI	UV 512K EPROM,120NS,IND	CERDIP 28	**27C512-12I/J**
Am27C512-120LI	UV 512K EPROM,120NS,IND	LCC 32	**27C512-12I/K**
Am27C512-120JI	OTP 512K EPROM,120NS,IND	PLCC 32	**27C512-12I/L**
Am27C512-120PI	OTP 512K EPROM,120NS,IND	PDIP 28	**27C512-12I/P**
Am27C512-150DI	UV 512K EPROM,150NS,IND	CERDIP 28	**27C512-15I/J**
Am27C512-150LI	UV 512K EPROM,150NS,IND	LCC 32	**27C512-15I/K**
Am27C512-150JI	OTP 512K EPROM,150NS,IND	PLCC 32	**27C512-15I/L**

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CROSS REFERENCE OF MICROCHIP EPROM PRODUCTS TO THE COMPETITION

AMD (Cont.)	DESCRIPTION	MICROCHIP P/N	
Am27C512-150PI	OTP 512K EPROM,150NS,IND	PDIP 28	**27C512-15I/P**
Am27C512-200DI	UV 512K EPROM,200NS,IND	CERDIP 28	**27C512-20I/J**
Am27C512-200LI	UV 512K EPROM,200NS,IND	LCC 32	**27C512-20I/K**
Am27C512-200JI	OTP 512K EPROM,200NS,IND	PLCC 32	**27C512-20I/L**
Am27C512-200PI	OTP 512K EPROM,200NS,IND	PDIP 28	**27C512-20I/P**
Am27C512-75DI	UV 512K EPROM,70NS	CERDIP 28	**27C512A-70/J**
Am27C512-75LI	UV 512K EPROM,70NS	LCC 32	**27C512A-70/K**
Am27C512-90DC	UV 512K EPROM,90NS	CERDIP 28	**27C512A-90/J**
Am27C512-90LC	UV 512K EPROM,90NS	LCC 32	**27C512A-90/K**
Am27C512-90JC	OTP 512K EPROM,90NS	PLCC 32	**27C512A-90/L**
Am27C512-90PC	OTP 512K EPROM,90NS	PDIP 28	**27C512A-90/P**
Am27C512-120DC	UV 512K EPROM,120NS	CERDIP 28	**27C512A-12/J**
Am27C512-120LC	UV 512K EPROM,120NS	LCC 32	**27C512A-12/K**
Am27C512-120JC	OTP 512K EPROM,120NS	PLCC 32	**27C512A-12/L**
Am27C512-120PC	OTP 512K EPROM,120NS	PDIP 28	**27C512A-12/P**
Am27C512-150DC	UV 512K EPROM,150NS	CERDIP 28	**27C512A-15/J**
Am27C512-150LC	UV 512K EPROM,150NS	LCC 32	**27C512A-15/K**
Am27C512-150JC	OTP 512K EPROM,150NS	PLCC 32	**27C512A-15/L**
Am27C512-150PC	OTP 512K EPROM,150NS	PDIP 28	**27C512A-15/P**
Am27C512-200DC	UV 512K EPROM,200NS	CERDIP 28	**27C512A-20/J**
Am27C512-200LC	UV 512K EPROM,200NS	LCC 32	**27C512A-20/K**
Am27C512-200JC	OTP 512K EPROM,200NS	PLCC 32	**27C512A-20/L**
Am27C512-200PC	OTP 512K EPROM,200NS	PDIP 28	**27C512A-20/P**
Am27HC256-55DC	UV 256K HS EPROM,55NS	CERDIP 28	**27HC256-55/J**
Am27HC256-55LC	UV 256K HS EPROM,55NS	LCC 32	**27HC256-55/K**
Am27HC256-55JC	OTP 256K HS EPROM,55NS	PLCC 32	**27HC256-55/L**
Am27HC256-55PC	OTP 256K HS EPROM,55NS	PDIP 28	**27HC256-55/P**
Am27HC256-70DC	UV 256K HS EPROM,70NS	CERDIP 28	**27HC256-70/J**
Am27HC256-70LC	UV 256K HS EPROM,70NS	LCC 32	**27HC256-70/K**
Am27HC256-70JC	OTP 256K HS EPROM,70NS	PLCC 32	**27HC256-70/L**
Am27HC256-70PC	OTP 256K HS EPROM,70NS	PDIP 28	**27HC256-70/P**
Am27HC256-55DI	UV 256K HS EPROM,55NS,IND	CERDIP 28	**27HC256-55I/J**
Am27HC256-55JI	OTP 256K HS EPROM,55NS,IND	PLCC 32	**27HC256-55I/L**
Am27HC256-55PI	OTP 256K HS EPROM,55NS,IND	PDIP 28	**27HC256-55I/P**
Am27HC256-70DI	UV 256K HS EPROM,70NS,IND	CERDIP 28	**27HC256-70I/J**
Am27HC256-70LI	UV 256K HS EPROM,70NS,IND	LCC 32	**27HC256-70I/K**
Am27HC256-70JI	OTP 256K HS EPROM,70NS,IND	PLCC 32	**27HC256-70I/L**
Am27HC256-70PI	OTP 256K HS EPROM,70NS,IND	PDIP 28	**27HC256-70I/P**

TI	DESCRIPTION		MICROCHIP P/N
TMS27C128-12JL	UV 128K EPROM,120NS	CERDIP 28	**27C128-12/J**
TMS27PC128-12FML	OTP 128K EPROM,120NS	PLCC 32	**27C128-12/L**
TMS27PC128-12NL	OTP 128K EPROM,120NS	PDIP 28	**27C128-12/P**
TMS27C128-15JL	UV 128K EPROM,150NS	CERDIP 28	**27C128-15/J**
TMS27PC128-15FML	OTP 128K EPROM,150NS	PLCC 32	**27C128-15/L**
TMS27PC128-15NL	OTP 128K EPROM,150NS	PDIP 28	**27C128-15/P**
TMS27C128-20JL	UV 128K EPROM,200NS	CERDIP 28	**27C128-20/J**
TMS27PC128-20FML	OTP 128K EPROM,200NS	PLCC 32	**27C128-20/L**
TMS27PC128-20NL	OTP 128K EPROM,200NS	PDIP 28	**27C128-20/P**
TMS27C128-25JL	UV 128K EPROM,250NS	CERDIP 28	**27C128-25/J**
TMS27PC128-25FML	OTP 128K EPROM,250NS	PLCC 32	**27C128-25/L**
TMS27PC128-25NL	OTP 128K EPROM,250NS	PDIP 28	**27C128-25/P**
TMS27C128-15JE	UV 128K EPROM,150NS,IND	CERDIP 28	**27C128-15I/J**
TMS27PC128-15FME	OTP 128K EPROM,150NS,IND	PLCC 32	**27C128-15I/L**
TMS27PC128-15NE	OTP 128K EPROM,150NS,IND	PDIP 28	**27C128-15I/P**
TMS27C128-20JE	UV 128K EPROM,200NS,IND	CERDIP 28	**27C128-20I/J**
TMS27PC128-20FME	OTP 128K EPROM,200NS,IND	PLCC 32	**27C128-20I/L**
TMS27PC128-20NE	OTP 128K EPROM,200NS,IND	PDIP 28	**27C128-20I/P**
TMS27C128-25JE	UV 128K EPROM,250NS,IND	CERDIP 28	**27C128-25I/J**
TMS27PC128-25FME	OTP 128K EPROM,250NS,IND	PLCC 32	**27C128-25I/L**
TMS27PC128-25NE	OTP 128K EPROM,250NS,IND	PDIP 28	**27C128-25I/P**
TMS27C256-10JL	UV 256K EPROM,100NS	CERDIP 28	**27C256-10/J**
TMS27PC256-10FML	OTP 256K EPROM,100NS	PLCC 32	**27C256-10/L**
TMS27PC256-10NL	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**
TMS27C256-12JL	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**

CROSS REFERENCE OF MICROCHIP EPROM PRODUCTS TO THE COMPETITION

TI (Cont.)	DESCRIPTION	MICROCHIP P/N	
TMS27PC256-12FML	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
TMS27PC256-12NL	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
TMS27C256-15JL	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
TMS27PC256-15FML	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
TMS27PC256-15NL	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
TMS27C256-20JL	UV 256K EPROM,200NS	CERDIP 28	**27C256-20/J**
TMS27PC256-20FML	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
TMS27PC256-20NL	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
TMS27C256-10JE	UV 256K EPROM,100NS,IND	CERDIP 28	**27C256-10I/J**
TMS27PC256-10FME	OTP 256K EPROM,100NS,IND	PLCC 32	**27C256-10I/L**
TMS27PC256-10NE	OTP 256K EPROM,100NS,IND	PDIP 28	**27C256-10I/P**
TMS27C256-12JE	UV 256K EPROM,120NS,IND	CERDIP 28	**27C256-12I/J**
TMS27PC256-12FME	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
TMS27PC256-12NE	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
TMS27C256-15JE	UV 256K EPROM,150NS,IND	CERDIP 28	**27C256-15I/J**
TMS27PC256-15FME	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
TMS27PC256-15NE	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
TMS27C256-20JE	UV 256K EPROM,200NS,IND	CERDIP 28	**27C256-20I/J**
TMS27PC256-20FME	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**
TMS27PC256-20NE	OTP 256K EPROM,200NS,IND	PDIP 28	**27C256-20I/P**
TMS27C512-10JL	UV 512K EPROM,100NS	CERDIP 28	**27C512-10/J**
TMS27PC512-10FML	OTP 512K EPROM,100NS	PLCC 32	**27C512-10/L**
TMS27PC512-10NL	OTP 512K EPROM,100NS	PDIP 28	**27C512-10/P**
TMS27C512-12JL	UV 512K EPROM,120NS	CERDIP 28	**27C512-12/J**
TMS27PC512-12FML	OTP 512K EPROM,120NS	PLCC 32	**27C512-12/L**
TMS27PC512-12NL	OTP 512K EPROM,120NS	PDIP 28	**27C512-12/P**
TMS27C512-15JL	UV 512K EPROM,150NS	CERDIP 28	**27C512-15/J**
TMS27PC512-15FML	OTP 512K EPROM,150NS	PLCC 32	**27C512-15/L**
TMS27PC512-15NL	OTP 512K EPROM,150NS	PDIP 28	**27C512-15/P**
TMS27C512-20JL	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
TMS27PC512-20FML	OTP 512K EPROM,200NS	PLCC 32	**27C512-20/L**
TMS27PC512-20NL	OTP 512K EPROM,200NS	PDIP 28	**27C512-20/P**
TMS27C512-10JE	UV 512K EPROM,100NS,IND	CERDIP 28	**27C512-10I/J**
TMS27PC512-10FME	OTP 512K EPROM,100NS,IND	PLCC 32	**27C512-10I/L**
TMS27PC512-10NE	OTP 512K EPROM,100NS,IND	PDIP 28	**27C512-10I/P**
TMS27C512-12JE	UV 512K EPROM,120NS,IND	CERDIP 28	**27C512-12I/J**
TMS27PC512-12FME	OTP 512K EPROM,120NS,IND	PLCC 32	**27C512-12I/L**
TMS27PC512-12NE	OTP 512K EPROM,120NS,IND	PDIP 28	**27C512-12I/P**
TMS27C512-15JE	UV 512K EPROM,150NS,IND	CERDIP 28	**27C512-15I/J**
TMS27PC512-15FME	OTP 512K EPROM,150NS,IND	PLCC 32	**27C512-15I/L**
TMS27PC512-15NE	OTP 512K EPROM,150NS,IND	PDIP 28	**27C512-15I/P**
TMS27C512-20JE	UV 512K EPROM,200NS,IND	CERDIP 28	**27C512-20I/J**
TMS27PC512-20FME	OTP 512K EPROM,200NS,IND	PLCC 32	**27C512-20I/L**
TMS27PC512-20NE	OTP 512K EPROM,200NS,IND	PDIP 28	**27C512-20I/P**
TMS27C512-80JL	UV 512K EPROM,70NS	CERDIP 28	**27C512A-70/J**
TMS27PC512-80FML	OTP 512K EPROM,70NS	PLCC 32	**27C512A-70/L**
TMS27PC512-80NL	OTP 512K EPROM,70NS	PDIP 28	**27C512A-70/P**
TMS27C512-10JL	UV 512K EPROM,90NS	CERDIP 28	**27C512A-90/J**
TMS27PC512-10FML	OTP 512K EPROM,90NS	PLCC 32	**27C512A-90/L**
TMS27PC512-10NL	OTP 512K EPROM,90NS	PDIP 28	**27C512A-90/P**
TMS27C512-12JL	UV 512K EPROM,120NS	CERDIP 28	**27C512A-12/J**
TMS27PC512-12FML	OTP 512K EPROM,120NS	PLCC 32	**27C512A-12/L**
TMS27PC512-12NL	OTP 512K EPROM,120NS	PDIP 28	**27C512A-12/P**
TMS27C512-15JL	UV 512K EPROM,150NS	CERDIP 28	**27C512A-15/J**
TMS27PC512-15FML	OTP 512K EPROM,150NS	PLCC 32	**27C512A-15/L**
TMS27PC512-15NL	OTP 512K EPROM,150NS	PDIP 28	**27C512A-15/P**
TMS27C512-20JL	UV 512K EPROM,200NS	CERDIP 28	**27C512A-20/J**
TMS27PC512-20FML	OTP 512K EPROM,200NS	PLCC 32	**27C512A-20/L**
TMS27PC512-20NL	OTP 512K EPROM,200NS	PDIP 28	**27C512A-20/P**

SGS	DESCRIPTION		MICROCHIP P/N
M27C64A-15F1	UV 64K EPROM,150NS	CERDIP 28	**27C64-15/J**
M27C64A-15C1	OTP 64K EPROM,150NS	PLCC 32	**27C64-15/L**
M27C64A-15C1TR	OTP 64K EPROM,150NS	PLCC 32	**27C64T-15/L**
M27C64A-20F1	UV 64K EPROM,200NS	CERDIP 28	**27C64-20/J**

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CROSS REFERENCE OF MICROCHIP EPROM PRODUCTS TO THE COMPETITION

SGS (Cont.)	DESCRIPTION	MICROCHIP P/N	
M27C64A-20C1	OTP 64K EPROM,200NS	PLCC 32	**27C64-20/L**
M27C64A-20C1TR	OTP 64K EPROM,200NS	PLCC 32	**27C64T-20/L**
M27C64A-25F1	UV 64K EPROM,250NS	CERDIP 28	**27C64-25/J**
M27C64A-25C1	OTP 64K EPROM,250NS	PLCC 32	**27C64-25/L**
M27C64A-25C1TR	OTP 64K EPROM,250NS	PLCC 32	**27C64T-25/L**
M27C64A-15F6	UV 64K EPROM,150NS,IND	CERDIP 28	**27C64-15I/J**
M27C64A-15C6	OTP 64K EPROM,150NS,IND	PLCC 32	**27C64-15I/L**
M27C64A-15C6TR	OTP 64K EPROM,150NS,IND	PLCC 32	**27C64T-15I/L**
M27C64A-20F6	UV 64K EPROM,200NS,IND	CERDIP 28	**27C64-20I/J**
M27C64A-20C6	OTP 64K EPROM,200NS,IND	PLCC 32	**27C64-20I/L**
M27C64A-20C6TR	OTP 64K EPROM,200NS,IND	PLCC 32	**27C64T-20I/L**
M27C64A-25F6	UV 64K EPROM,250NS,IND	CERDIP 28	**27C64-25I/J**
M27C64A-25C6	OTP 64K EPROM,250NS,IND	PLCC 32	**27C64-25I/L**
M27C64A-25C6TR	OTP 64K EPROM,250NS,IND	PLCC 32	**27C64T-25I/L**
M27C128A-12F1	UV 128K EPROM,120NS	CERDIP 28	**27C128-12/J**
M27C128A-12C1	OTP 128K EPROM,120NS	PLCC 32	**27C128-12/L**
M27C128A-15F1	UV 128K EPROM,150NS	CERDIP 28	**27C128-15/J**
M27C128A-15C1	OTP 128K EPROM,150NS	PLCC 32	**27C128-15/L**
M27C128A-20F1	UV 128K EPROM,200NS	CERDIP 28	**27C128-20/J**
M27C128A-20C1	OTP 128K EPROM,200NS	PLCC 32	**27C128-20/L**
M27C128A-12F6	UV 128K EPROM,120NS,IND	CERDIP 28	**27C128-12I/J**
M27C128A-15F6	UV 128K EPROM,150NS,IND	CERDIP 28	**27C128-15I/J**
M27C128A-15C6	OTP 128K EPROM,150NS,IND	PLCC 32	**27C128-15I/L**
M27C128A-20F6	UV 128K EPROM,200NS,IND	CERDIP 28	**27C128-20I/J**
M27C128A-20C6	OTP 128K EPROM,200NS,IND	PLCC 32	**27C128-20I/L**
M27C256B-90F1	UV 256K EPROM,90NS	CERDIP 28	**27C256-90/J**
M27C256B-90C1	OTP 256K EPROM,90NS	PLCC 32	**27C256-90/L**
M27C256B-90B1	OTP 256K EPROM,90NS	PDIP 28	**27C256-90/P**
M27C256B-90C1	OTP 256K EPROM,90NS	PLCC 32	**27C256T-90/L**
M27C256B-10F1	UV 256K EPROM,100NS	CERDIP 28	**27C256-10/J**
M27C256B-10C1	OTP 256K EPROM,100NS	PLCC 32	**27C256-10/L**
M27C256B-10B1	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**
M27C256B-10N1	OTP 256K EPROM,100NS	VSOP 28	**27C256-10/VS**
M27C256B-10C1	OTP 256K EPROM,100NS	PLCC 32	**27C256T-10/L**
M27C256B-12F1	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
M27C256B-12C1	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
M27C256B-12B1	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
M27C256B-12M1*	OTP 256K EPROM,120NS	SOIC 28	**27C256-12/SO**
M27C256B-12N1	OTP 256K EPROM,120NS	VSOP 28	**27C256-12/VS**
M27C256B-12C1	OTP 256K EPROM,120NS	PLCC 32	**27C256T-12/L**
M27C256B-15F1	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
M27C256B-15C1	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
M27C256B-15B1	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
M27C256B-15M1*	OTP 256K EPROM,150NS	SOIC 28	**27C256-15/SO**
M27C256B-15N1	OTP 256K EPROM,150NS	VSOP 28	**27C256-15/VS**
M27C256B-15C1	OTP 256K EPROM,150NS	PLCC 32	**27C256T-15/L**
M27C256B-20F1	UV 256K EPROM,200NS	CERDIP 28	**27C256-20/J**
M27C256B-20C1	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
M27C256B-20B1	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
M27C256B-20M1*	OTP 256K EPROM,200NS	SOIC 28	**27C256-20/SO**
M27C256B-20C1	OTP 256K EPROM,200NS	PLCC 32	**27C256T-20/L**
M27C256B-10F6	UV 256K EPROM,100NS,IND	CERDIP 28	**27C256-10I/J**
M27C256B-10C6	OTP 256K EPROM,100NS,IND	PLCC 32	**27C256-10I/L**
M27C256B-10B6	OTP 256K EPROM,100NS,IND	PDIP 28	**27C256-10I/P**
M27C256B-10C6	OTP 256K EPROM,100NS,IND	PLCC 32	**27C256T-10I/L**
M27C256B-12F6	UV 256K EPROM,120NS,IND	CERDIP 28	**27C256-12I/J**
M27C256B-12C6	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
M27C256B-12B6	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
M27C256B-12C6	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256T-12I/L**
M27C256B-15F6	UV 256K EPROM,150NS,IND	CERDIP 28	**27C256-15I/J**
M27C256B-15C6	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
M27C256B-15B6	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
M27C256B-15C6	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256T-15I/L**
M27C256B-20F6	UV 256K EPROM,200NS,IND	CERDIP 28	**27C256-20I/J**
M27C256B-20C6	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**

CROSS REFERENCE OF MICROCHIP EPROM PRODUCTS TO THE COMPETITION

SGS (Cont.)	DESCRIPTION	MICROCHIP P/N	
M27C256B-20B6	OTP 256K EPROM,200NS,IND	PDIP 28	27C256-20I/P
M27C256B-20C6	OTP 256K EPROM,200NS,IND	PLCC 32	27C256T-20I/L
M27C512-90F1	UV 512K EPROM,90NS	CERDIP 28	27C512-90/J
M27C512-90C1	OTP 512K EPROM,90NS	PLCC 32	27C512-90/L
M27C512-90B1	OTP 512K EPROM,90NS	PDIP 28	27C512-90/P
M27C512-90C1	OTP 512K EPROM,90NS	PLCC 32	27C512T-90/L
M27C512-10F1	UV 512K EPROM,100NS	CERDIP 28	27C512-10/J
M27C512-10C1	OTP 512K EPROM,100NS	PLCC 32	27C512-10/L
M27C512-10B1	OTP 512K EPROM,100NS	PDIP 28	27C512-10/P
M27C512-10C1	OTP 512K EPROM,100NS	PLCC 32	27C512T-10/L
M27C512-12F1	UV 512K EPROM,120NS	CERDIP 28	27C512-12/J
M27C512-12C1	OTP 512K EPROM,120NS	PLCC 32	27C512-12/L
M27C512-12B1	OTP 512K EPROM,120NS	PDIP 28	27C512-12/P
M27C512-12C1	OTP 512K EPROM,120NS	PLCC 32	27C512T-12/L
M27C512-15F1	UV 512K EPROM,150NS	CERDIP 28	27C512-15/J
M27C512-15C1	OTP 512K EPROM,150NS	PLCC 32	27C512-15/L
M27C512-15B1	OTP 512K EPROM,150NS	PDIP 28	27C512-15/P
M27C512-15C1	OTP 512K EPROM,150NS	PLCC 32	27C512T-15/L
M27C512-20F1	UV 512K EPROM,200NS	CERDIP 28	27C512-20/J
M27C512-20C1	OTP 512K EPROM,200NS	PLCC 32	27C512-20/L
M27C512-20B1	OTP 512K EPROM,200NS	PDIP 28	27C512-20/P
M27C512-20C1	OTP 512K EPROM,200NS	PLCC 32	27C512T-20/L
M27C512-10F6	UV 512K EPROM,100NS,IND	CERDIP 28	27C512-10I/J
M27C512-10C6	OTP 512K EPROM,100NS,IND	PLCC 32	27C512-10I/L
M27C512-10B6	OTP 512K EPROM,100NS,IND	PDIP 28	27C512-10I/P
M27C512-10C6	OTP 512K EPROM,100NS,IND	PLCC 32	27C512T-10I/L
M27C512-12F6	UV 512K EPROM,120NS,IND	CERDIP 28	27C512-12I/J
M27C512-12C6	OTP 512K EPROM,120NS,IND	PLCC 32	27C512-12I/L
M27C512-12B6	OTP 512K EPROM,120NS,IND	PDIP 28	27C512-12I/P
M27C512-12C6	OTP 512K EPROM,120NS,IND	PLCC 32	27C512T-12I/L
M27C512-15F6	UV 512K EPROM,150NS,IND	CERDIP 28	27C512-15I/J
M27C512-15C6	OTP 512K EPROM,150NS,IND	PLCC 32	27C512-15I/L
M27C512-15B6	OTP 512K EPROM,150NS,IND	PDIP 28	27C512-15I/P
M27C512-15C6	OTP 512K EPROM,150NS,IND	PLCC 32	27C512T-15I/L
M27C512-20F6	UV 512K EPROM,200NS,IND	CERDIP 28	27C512-20I/J
M27C512-20C6	OTP 512K EPROM,200NS,IND	PLCC 32	27C512-20I/L
M27C512-20B6	OTP 512K EPROM,200NS,IND	PDIP 28	27C512-20I/P
M27C512-20C6	OTP 512K EPROM,200NS,IND	PLCC 32	27C512T-20I/L
M27C512-80F1	UV 512K EPROM,70NS	CERDIP 28	27C512A-70/J
M27C512-80C1	OTP 512K EPROM,70NS	PLCC 32	27C512A-70/L
M27C512-80B1	OTP 512K EPROM,70NS	PDIP 28	27C512A-70/P
M27C512-80C1	OTP 512K EPROM,70NS	PLCC 32	27C512AT-70/L
M27C512-90F1	UV 512K EPROM,90NS	CERDIP 28	27C512A-90/J
M27C512-90C1	OTP 512K EPROM,90NS	PLCC 32	27C512A-90/L
M27C512-90B1	OTP 512K EPROM,90NS	PDIP 28	27C512A-90/P
M27C512-90C1	OTP 512K EPROM,90NS	PLCC 32	27C512AT-90/L
M27C512-12F1	UV 512K EPROM,120NS	CERDIP 28	27C512A-12/J
M27C512-12C1	OTP 512K EPROM,120NS	PLCC 32	27C512A-12/L
M27C512-12B1	OTP 512K EPROM,120NS	PDIP 28	27C512A-12/P
M27C512-12C1	OTP 512K EPROM,120NS	PLCC 32	27C512AT-12/L
M27C512-15F1	UV 512K EPROM,150NS	CERDIP 28	27C512A-15/J
M27C512-15C1	OTP 512K EPROM,150NS	PLCC 32	27C512A-15/L
M27C512-15B1	OTP 512K EPROM,150NS	PDIP 28	27C512A-15/P
M27C512-15C1	OTP 512K EPROM,150NS	PLCC 32	27C512AT-15/L
M27C512-20F1	UV 512K EPROM,200NS	CERDIP 28	27C512A-20/J
M27C512-20C1	OTP 512K EPROM,200NS	PLCC 32	27C512A-20/L
M27C512-20B1	OTP 512K EPROM,200NS	PDIP 28	27C512A-20/P
M27C512-20C1	OTP 512K EPROM,200NS	PLCC 32	27C512AT-20/L
M27V512-200K1	OTP 512K EPROM,3V,200NS	PLCC 32	27LV512-20/L
M27V512-250K1	OTP 512K EPROM,3V,250NS	PLCC 32	27LV512-25/L
M27V512-300K1	OTP 512K EPROM,3V,300NS	PLCC 32	27LV512-30/L
M27V512-200K6	OTP 512K EPROM,3V,200NS,IND	PLCC 32	27LV512-20I/L
M27V512-250K6	OTP 512K EPROM,3V,250NS,IND	PLCC 32	27LV512-25I/L
M27V512-300K6	OTP 512K EPROM,3V,300NS,IND	PLCC 32	27LV512-30I/L

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CROSS REFERENCE OF MICROCHIP EPROM PRODUCTS TO THE COMPETITION

Intel	DESCRIPTION	MICROCHIP P/N	
27C64A-1Q	UV 64K EPROM,150NS	CERDIP 28	**27C64-15/J**
27C64A-20Q	UV 64K EPROM,200NS	CERDIP 28	**27C64-20/J**
27C64A-25Q	UV 64K EPROM,250NS	CERDIP 28	**27C64-25/J**
27C64A-1T	UV 64K EPROM,150NS,IND	CERDIP 28	**27C64-15I/J**
27C64A-20T	UV 64K EPROM,200NS,IND	CERDIP 28	**27C64-20I/J**
27C64A-25Q	UV 64K EPROM,250NS,IND	CERDIP 28	**27C64-25I/J**
27128A-1Q	UV 128K EPROM,150NS	CERDIP 28	**27C128-15/J**
27128A-20Q	UV 128K EPROM,200NS	CERDIP 28	**27C128-20/J**
27128A-25Q	UV 128K EPROM,250NS	CERDIP 28	**27C128-25/J**
27128A-1T	UV 128K EPROM,150NS,IND	CERDIP 28	27C128-15I/J
27128A-20T	UV 128K EPROM,200NS,IND	CERDIP 28	**27C128-20I/J**
27128A-25T	UV 128K EPROM,250NS,IND	CERDIP 28	**27C128-25I/J**
27C256-120V10Q	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
N27C256-120V10Q	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
P27C256-120V10Q	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
27C256-150V10Q	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
N27C256-150V10Q	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
P27C256-150V10Q	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
27C256-200V10Q	UV 256K EPROM,200NS	CERDIP 28	**27C256-20/J**
N27C256-200V10Q	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
P27C256-200V10Q	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
27C256-120V10T	UV 256K EPROM,120NS,IND	CERDIP 28	**27C256-12I/J**
N27C256-120V10T	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
P27C256-120V10T	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
27C256-150V10T	UV 256K EPROM,150NS,IND	CERDIP 28	**27C256-15I/J**
N27C256-150V10T	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
P27C256-150V10T	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
27C256-200V10T	UV 256K EPROM,200NS,IND	CERDIP 28	**27C256-20I/J**
N27C256-200V10T	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**
P27C256-200V10T	OTP 256K EPROM,200NS,IND	PDIP 28	**27C256-20I/P**
27C512-120V10Q	UV 512K EPROM,120NS	CERDIP 28	**27C512-12/J**
27C512-150V10Q	UV 512K EPROM,150NS	CERDIP 28	**27C512-15/J**
27C512-200V10Q	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
27C512-120V10T	UV 512K EPROM,120NS,IND	CERDIP 28	**27C512-12I/J**
27C512-150V10T	UV 512K EPROM,150NS,IND	CERDIP 28	**27C512-15I/J**
27C512-200V10T	UV 512K EPROM,200NS,IND	CERDIP 28	**27C512-20I/J**
27C512-120V10Q	UV 512K EPROM,120NS	CERDIP 28	**27C512A-12/J**
27C512-150V10Q	UV 512K EPROM,150NS	CERDIP 28	**27C512A-15/J**
27C512-200V10Q	UV 512K EPROM,200NS	CERDIP 28	**27C512A-20/J**

TOSHIBA	DESCRIPTION		MICROCHIP P/N
TC57256AD-12/-120	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
TC57256AD-15/-150	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
TC57256AD-20	UV 256K EPROM,200NS	CERDIP 28	**27C256-20/J**
TC54256AP-15	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
TC54256AF-20*	OTP 256K EPROM,150NS,IND	SOIC 28	**27C256-15I/SO**
TC57512AD-15	UV 512K EPROM,150NS	LCC 32	**27C512-15/K**
TC54512AP-15	OTP 512K EPROM,150NS	PDIP 28	**27C512-15/P**
TC54512AF-15*	OTP 512K EPROM,150NS	SOIC 28	**27C512-15/SO**
TC57512AD-20	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
TC54512AP-20	OTP 512K EPROM,200NS	PDIP 28	**27C512-20/P**
TC54512AF-20*	OTP 512K EPROM,200NS	SOIC 28	**27C512-20/SO**
TC54512AP-17	OTP 512K EPROM,150NS,IND	PDIP 28	**27C512-15I/P**
TC54512AP-20	OTP 512K EPROM,200NS,IND	PDIP 28	**27C512-20I/P**
TC57H256D-70/-85	UV 256K HS EPROM,70NS	CERDIP 28	**27HC256-70/J**

NATIONAL	DESCRIPTION		MICROCHIP P/N
NM27C64Q150	UV 64K EPROM,150NS	CERDIP 28	**27C64-15/J**
NM27C64N150	OTP 64K EPROM,150NS	PDIP 28	**27C64-15/P**
NM27C64Q200	UV 64K EPROM,200NS	CERDIP 28	**27C64-20/J**
NM27C64N200	OTP 64K EPROM,200NS	PDIP 28	**27C64-20/P**
NM27C64QE150	UV 64K EPROM,150NS,IND	CERDIP 28	**27C64-15I/J**
NM27C64NE150	OTP 64K EPROM,150NS,IND	PDIP 28	**27C64-15I/P**
NM27C128Q150	UV 128K EPROM,120NS	CERDIP 28	**27C128-12/J**
NM27C128N150	OTP 128K EPROM,120NS	PDIP 28	**27C128-12/P**

CROSS REFERENCE OF MICROCHIP EPROM PRODUCTS TO THE COMPETITION

National (Cont.)	DESCRIPTION	MICROCHIP P/N	
NM27C128Q200	UV 128K EPROM,200NS	CERDIP 28	27C128-20/J
NM27C128N200	OTP 128K EPROM,200NS	PDIP 28	27C128-20/P
NM27C128QE150	UV 128K EPROM,150NS,IND	CERDIP 28	27C128-15I/J
NM27C128NE150	OTP 128K EPROM,150NS,IND	PDIP 28	27C128-15I/P
NM27C256Q100	UV 256K EPROM,100NS	CERDIP 28	27C256-10/J
NM27C256V100	OTP 256K EPROM,100NS	PLCC 32	27C256-10/L
NM27C256N100	OTP 256K EPROM,100NS	PDIP 28	27C256-10/P
NM27C256Q120	UV 256K EPROM,120NS	CERDIP 28	27C256-12/J
NM27C256V120	OTP 256K EPROM,120NS	PLCC 32	27C256-12/L
NM27C256N120	OTP 256K EPROM,120NS	PDIP 28	27C256-12/P
NM27C256Q150	UV 256K EPROM,150NS	CERDIP 28	27C256-15/J
NM27C256V150	OTP 256K EPROM,150NS	PLCC 32	27C256-15/L
NM27C256N150	OTP 256K EPROM,150NS	PDIP 28	27C256-15/P
NM27C256Q200	UV 256K EPROM,200NS	CERDIP 28	27C256-20/J
NM27C256V200	OTP 256K EPROM,200NS	PLCC 32	27C256-20/L
NM27C256N200	OTP 256K EPROM,200NS	PDIP 28	27C256-20/P
NM27C256QE100	UV 256K EPROM,100NS,IND	CERDIP 28	27C256-10I/J
NM27C256VE100	OTP 256K EPROM,100NS,IND	PLCC 32	27C256-10I/L
NM27C256NE100	OTP 256K EPROM,100NS,IND	PDIP 28	27C256-10I/P
NM27C256QE120	UV 256K EPROM,120NS,IND	CERDIP 28	27C256-12I/J
NM27C256VE120	OTP 256K EPROM,120NS,IND	PLCC 32	27C256-12I/L
NM27C256NE120	OTP 256K EPROM,120NS,IND	PDIP 28	27C256-12I/P
NM27C256QE150	UV 256K EPROM,150NS,IND	CERDIP 28	27C256-15I/J
NM27C256VE150	OTP 256K EPROM,150NS,IND	PLCC 32	27C256-15I/L
NM27C256NE150	OTP 256K EPROM,150NS,IND	PDIP 28	27C256-15I/P
NM27C256QE200	UV 256K EPROM,200NS,IND	CERDIP 28	27C256-20I/J
NM27C256VE200	OTP 256K EPROM,200NS,IND	PLCC 32	27C256-20I/L
NM27C256NE200	OTP 256K EPROM,200NS,IND	PDIP 28	27C256-20I/P
NM27C512Q120	UV 512K EPROM,120NS	CERDIP 28	27C512-12/J
NM27C512V120	OTP 512K EPROM,120NS	PLCC 32	27C512-12/L
NM27C512N120	OTP 512K EPROM,120NS	PDIP 28	27C512-12/P
NM27C512Q150	UV 512K EPROM,150NS	CERDIP 28	27C512-15/J
NM27C512V150	OTP 512K EPROM,150NS	PLCC 32	27C512-15/L
NM27C512N150	OTP 512K EPROM,150NS	PDIP 28	27C512-15/P
NM27C512Q200	UV 512K EPROM,200NS	CERDIP 28	27C512-20/J
NM27C512V200	OTP 512K EPROM,200NS	PLCC 32	27C512-20/L
NM27C512N200	OTP 512K EPROM,200NS	PDIP 28	27C512-20/P
NM27C512QE120	UV 512K EPROM,120NS,IND	CERDIP 28	27C512-12I/J
NM27C512VE120	OTP 512K EPROM,120NS,IND	PLCC 32	27C512-12I/L
NM27C512NE120	OTP 512K EPROM,120NS,IND	PDIP 28	27C512-12I/P
NM27C512QE150	UV 512K EPROM,150NS,IND	CERDIP 28	27C512-15I/J
NM27C512VE150	OTP 512K EPROM,150NS,IND	PLCC 32	27C512-15I/L
NM27C512NE150	OTP 512K EPROM,150NS,IND	PDIP 28	27C512-15I/P
NM27C512QE200	UV 512K EPROM,200NS,IND	CERDIP 28	27C512-20I/J
NM27C512VE200	OTP 512K EPROM,200NS,IND	PLCC 32	27C512-20I/L
NM27C512NE200	OTP 512K EPROM,200NS,IND	PDIP 28	27C512-20I/P
NM27C512Q120	UV 512K EPROM,120NS	CERDIP 28	27C512A-12/J
NM27C512V120	OTP 512K EPROM,120NS	PLCC 32	27C512A-12/L
NM27C512N120	OTP 512K EPROM,120NS	PDIP 28	27C512A-12/P
NM27C512Q150	UV 512K EPROM,150NS	CERDIP 28	27C512A-15/J
NM27C512V150	OTP 512K EPROM,150NS	PLCC 32	27C512A-15/L
NM27C512N150	OTP 512K EPROM,150NS	PDIP 28	27C512A-15/P
NM27C512Q200	UV 512K EPROM,200NS	CERDIP 28	27C512A-20/J
NM27C512V200	OTP 512K EPROM,200NS	PLCC 32	27C512A-20/L
NM27C512N200	OTP 512K EPROM,200NS	PDIP 28	27C512A-20/P

ATMEL	DESCRIPTION		MICROCHIP P/N
AT27C256R-90DC	UV 256K EPROM,90NS	CERDIP 28	27C256-90/J
AT27C256R-90JC	OTP 256K EPROM,90NS	PLCC 32	27C256-90/L
AT27C256R-90PC	OTP 256K EPROM,90NS	PDIP 28	27C256-90/P
AT27C256R-90RC*	OTP 256K EPROM,90NS	SOIC 28	27C256-90/SO
AT27C256R-90TC	OTP 256K EPROM,90NS	VSOP 28	27C256-90/VS
AT27C256R-12DC	UV 256K EPROM,120NS	CERDIP 28	27C256-12/J
AT27C256R-12LC	UV 256K EPROM,120NS	LCC 32	27C256-12/K
AT27C256R-12JC	OTP 256K EPROM,120NS	PLCC 32	27C256-12/L

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CROSS REFERENCE OF MICROCHIP EPROM PRODUCTS TO THE COMPETITION

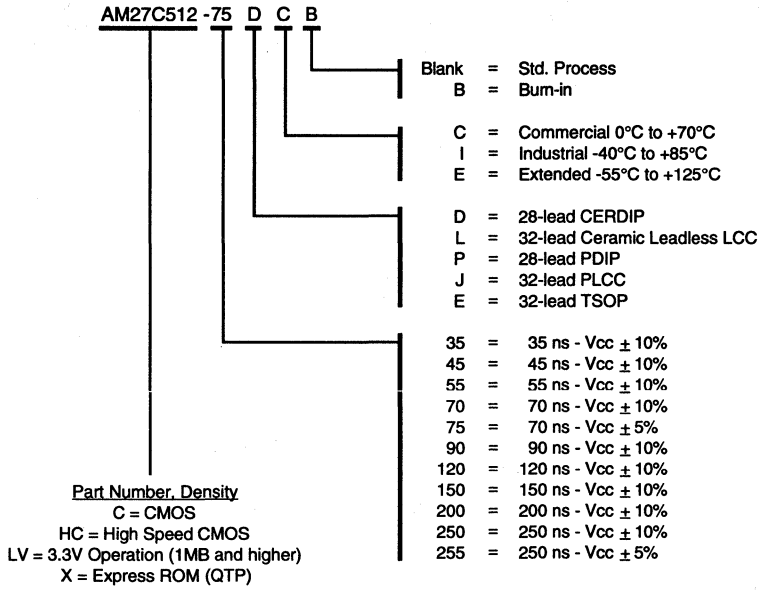
Atmel (Cont.)	DESCRIPTION	MICROCHIP P/N	
AT27C256R-12PC	OTP 256K EPROM,120NS	PDIP 28	27C256-12/P
AT27C256R-12RC*	OTP 256K EPROM,120NS	SOIC 28	27C256-12/SO
AT27C256R-12TC	OTP 256K EPROM,120NS	VSOP 28	27C256-12/VS
AT27C256R-15DC	UV 256K EPROM,150NS	CERDIP 28	27C256-15/J
AT27C256R-15LC	UV 256K EPROM,150NS	LCC 32	27C256-15/K
AT27C256R-15JC	OTP 256K EPROM,150NS	PLCC 32	27C256-15/L
AT27C256R-15PC	OTP 256K EPROM,150NS	PDIP 28	27C256-15/P
AT27C256R-15RC*	OTP 256K EPROM,150NS	SOIC 28	27C256-15/SO
AT27C256R-15TC	OTP 256K EPROM,150NS	VSOP 28	27C256-15/VS
AT27C256R-20DC	UV 256K EPROM,200NS	CERDIP 28	27C256-20/J
AT27C256R-20LC	UV 256K EPROM,200NS	LCC 32	27C256-20/K
AT27C256R-20JC	OTP 256K EPROM,200NS	PLCC 32	27C256-20/L
AT27C256R-20PC	OTP 256K EPROM,200NS	PDIP 28	27C256-20/P
AT27C256R-20RC*	OTP 256K EPROM,200NS	SOIC 28	27C256-20/SO
AT27C256R-20TC	OTP 256K EPROM,200NS	VSOP 28	27C256-20/VS
AT27C256R-12DI	UV 256K EPROM,120NS,IND	CERDIP 28	27C256-12I/J
AT27C256R-12LI	UV 256K EPROM,120NS,IND	LCC 32	27C256-12I/K
AT27C256R-12JI	OTP 256K EPROM,120NS,IND	PLCC 32	27C256-12I/L
AT27C256R-12PI	OTP 256K EPROM,120NS,IND	PDIP 28	27C256-12I/P
AT27C256R-12RI*	OTP 256K EPROM,120NS,IND	SOIC 28	27C256-12I/SO
AT27C256R-15DI	UV 256K EPROM,150NS,IND	CERDIP 28	27C256-15I/J
AT27C256R-15LI	UV 256K EPROM,150NS,IND	LCC 32	27C256-15I/K
AT27C256R-15JI	OTP 256K EPROM,150NS,IND	PLCC 32	27C256-15I/L
AT27C256R-15PI	OTP 256K EPROM,150NS,IND	PDIP 28	27C256-15I/P
AT27C256R-15RI*	OTP 256K EPROM,150NS,IND	SOIC 28	27C256-15I/SO
AT27C256R-20DI	UV 256K EPROM,200NS,IND	CERDIP 28	27C256-20I/J
AT27C256R-20LI	UV 256K EPROM,200NS,IND	LCC 32	27C256-20I/K
AT27C256R-20JI	OTP 256K EPROM,200NS,IND	PLCC 32	27C256-20I/L
AT27C256R-20PI	OTP 256K EPROM,200NS,IND	PDIP 28	27C256-20I/P
AT27C256R-20RI*	OTP 256K EPROM,200NS,IND	SOIC 28	27C256-20I/SO
AT27C512R-90DC	UV 512K EPROM,90NS	CERDIP 28	27C512A-90/J
AT27C512R-90LC	UV 512K EPROM,90NS	LCC 32	27C512A-90/K
AT27C512R-90JC	OTP 512K EPROM,90NS	PLCC 32	27C512A-90/L
AT27C512R-90PC	OTP 512K EPROM,90NS	PDIP 28	27C512A-90/P
AT27C512R-90RC*	OTP 512K EPROM,90NS	SOIC 28	27C512A-90/SO
AT27C512R-90TC	OTP 512K EPROM,90NS	VSOP 28	27C512A-90/VS
AT27C512R-12DC	UV 512K EPROM,120NS	CERDIP 28	27C512A-12/J
AT27C512R-12LC	UV 512K EPROM,120NS	LCC 32	27C512A-12/K
AT27C512R-12JC	OTP 512K EPROM,120NS	PLCC 32	27C512A-12/L
AT27C512R-12PC	OTP 512K EPROM,120NS	PDIP 28	27C512A-12/P
AT27C512R-12RC*	OTP 512K EPROM,120NS	SOIC 28	27C512A-12/SO
AT27C512R-12TC	OTP 512K EPROM,120NS	VSOP 28	27C512A-12/VS
AT27C512R-15DC	UV 512K EPROM,150NS	CERDIP 28	27C512A-15/J
AT27C512R-15LC	UV 512K EPROM,150NS	LCC 32	27C512A-15/K
AT27C512R-15JC	OTP 512K EPROM,150NS	PLCC 32	27C512A-15/L
AT27C512R-15PC	OTP 512K EPROM,150NS	PDIP 28	27C512A-15/P
AT27C512R-15RC*	OTP 512K EPROM,150NS	SOIC 28	27C512A-15/SO
AT27C512R-15TC	OTP 512K EPROM,150NS	VSOP 28	27C512A-15/VS
AT27C512R-20DC	UV 512K EPROM,200NS	CERDIP 28	27C512A-20/J
AT27C512R-20LC	UV 512K EPROM,200NS	LCC 32	27C512A-20/K
AT27C512R-20JC	OTP 512K EPROM,200NS	PLCC 32	27C512A-20/L
AT27C512R-20PC	OTP 512K EPROM,200NS	PDIP 28	27C512A-20/P
AT27C512R-20RC*	OTP 512K EPROM,200NS	SOIC 28	27C512A-20/SO
AT27HC256R-55DC	UV 256K HS EPROM,55NS	CERDIP 28	27HC256-55/J
AT27HC256R-55LC	UV 256K HS EPROM,55NS	LCC 32	27HC256-55/K
AT27HC256R-70DC	UV 256K HS EPROM,70NS	CERDIP 28	27HC256-70/J
AT27HC256R-70LC	UV 256K HS EPROM,70NS	LCC 32	27HC256-70/K
AT27HC256R-70JC	OTP 256K HS EPROM,70NS	PLCC 32	27HC256-70/L
AT27HC256R-70PC	OTP 256K HS EPROM,70NS	PDIP 28	27HC256-70/P
AT27HC256R-90DC	UV 256K HS EPROM,90NS	CERDIP 28	27HC256-90/J
AT27HC256R-90LC	UV 256K HS EPROM,90NS	LCC 32	27HC256-90/K
AT27HC256R-90JC	OTP 256K HS EPROM,90NS	PLCC 32	27HC256-90/L
AT27HC256R-90PC	OTP 256K HS EPROM,90NS	PDIP 28	27HC256-90/P
AT27HC256R-55DI	UV 256K HS EPROM,55NS,IND	CERDIP 28	27HC256-55I/J
AT27HC256R-55LI	OTP 256K HS EPROM,55NS,IND	PLCC 32	27HC256-55I/L

CROSS REFERENCE OF MICROCHIP EPROM PRODUCTS TO THE COMPETITION

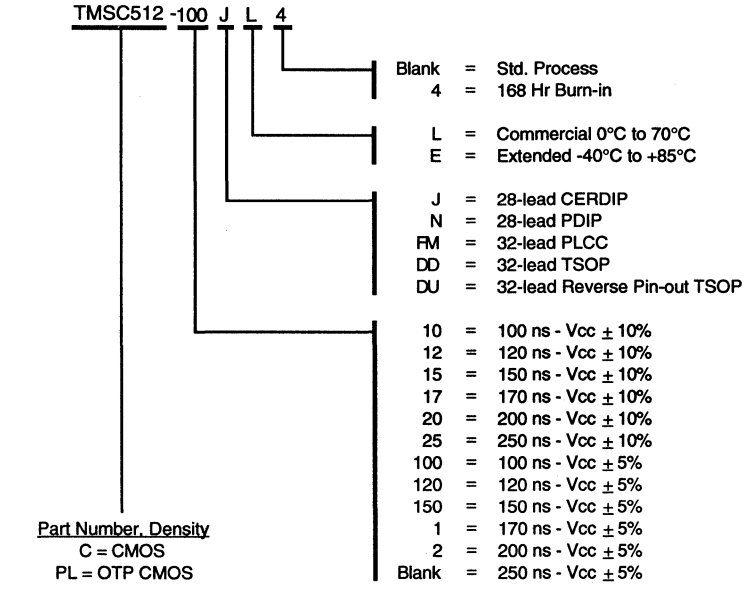
Atmel (Cont.)	DESCRIPTION	MICROCHIP P/N	
AT27HC256R-70DI	UV 256K HS EPROM,70NS,IND	CERDIP 28	**27HC256-70I/J**
AT27HC256R-70LI	UV 256K HS EPROM,70NS,IND	LCC 32	**27HC256-70I/K**
AT27HC256R-70JI	OTP 256K HS EPROM,70NS,IND	PLCC 32	**27HC256-70I/L**
AT27HC256R-70PI	OTP 256K HS EPROM,70NS,IND	PDIP 28	**27HC256-70I/P**
AT27LV256R-20DC	OTP 256K EPROM,3V,200NS	CERDIP 28	**27LV256-20/J**
AT27LV256R-20LC	OTP 256K EPROM,3V,200NS	LCC 32	**27LV256-20/K**
AT27LV256R-20JC	OTP 256K EPROM,3V,200NS	PLCC 32	**27LV256-20/L**
AT27LV256R-20PC	OTP 256K EPROM,3V,200NS	PDIP 28	**27LV256-20/P**
AT27LV256R-20RC*	OTP 256K EPROM,3V,200NS	SOIC 28	**27LV256-20/SO**
AT27LV256R-20TC	OTP 256K EPROM,3V,200NS	VSOP 28	**27LV256-20/VS**
AT27LV256R-25DC	OTP 256K EPROM,3V,250NS	CERDIP 28	**27LV256-25/J**
AT27LV256R-25LC	OTP 256K EPROM,3V,250NS	LCC 32	**27LV256-25/K**
AT27LV256R-25JC	OTP 256K EPROM,3V,250NS	PLCC 32	**27LV256-25/L**
AT27LV256R-25PC	OTP 256K EPROM,3V,250NS	PDIP 28	**27LV256-25/P**
AT27LV256R-25RC*	OTP 256K EPROM,3V,250NS	SOIC 28	**27LV256-25/SO**
AT27LV256R-25TC	OTP 256K EPROM,3V,250NS	VSOP 28	**27LV256-25/VS**
AT27LV256R-20DI	OTP 256K EPROM,3V,200NS,IND	CERDIP 28	**27LV256-20I/J**
AT27LV256R-20LI	OTP 256K EPROM,3V,200NS,IND	LCC 32	**27LV256-20I/K**
AT27LV256R-25DI	OTP 256K EPROM,3V,250NS,IND	CERDIP 28	**27LV256-25I/J**
AT27LV256R-25LI	OTP 256K EPROM,3V,250NS,IND	LCC 32	**27LV256-25I/K**
AT27LV512R-20DC	OTP 512K EPROM,3V,200NS	CERDIP 28	**27LV512-20/J**
AT27LV512R-20LC	OTP 512K EPROM,3V,200NS	LCC 32	**27LV512-20/K**
AT27LV512R-20JC	OTP 512K EPROM,3V,200NS	PLCC 32	**27LV512-20/L**
AT27LV512R-20PC	OTP 512K EPROM,3V,200NS	PDIP 28	**27LV512-20/P**
AT27LV512R-20RC*	OTP 512K EPROM,3V,200NS	SOIC 28	**27LV512-20/SO**
AT27LV512R-20TC	OTP 512K EPROM,3V,200NS	VSOP 28	**27LV512-20/VS**
AT27LV512R-25DC	OTP 512K EPROM,3V,250NS	CERDIP 28	**27LV512-25/J**
AT27LV512R-25LC	OTP 512K EPROM,3V,250NS	LCC 32	**27LV512-25/K**
AT27LV512R-25JC	OTP 512K EPROM,3V,250NS	PLCC 32	**27LV512-25/L**
AT27LV512R-25PC	OTP 512K EPROM,3V,250NS	PDIP 28	**27LV512-25/P**
AT27LV512R-25RC*	OTP 512K EPROM,3V,250NS	SOIC 28	**27LV512-25/SO**
AT27LV512R-25TC	OTP 512K EPROM,3V,250NS	VSOP 28	**27LV512-25/VS**
AT27LV512R-20DI	OTP 512K EPROM,3V,200NS,IND	CERDIP 28	**27LV512-20I/J**
AT27LV512R-20LI	OTP 512K EPROM,3V,200NS,IND	LCC 32	**27LV512-20I/K**
AT27LV512R-25DI	OTP 512K EPROM,3V,250NS,IND	CERDIP 28	**27LV512-25I/J**
AT27LV512R-25LI	OTP 512K EPROM,3V,250NS,IND	LCC 32	**27LV512-25I/K**

COMPETITIVE PART NUMBER BREAKDOWN

ADVANCED MICRO DEVICES

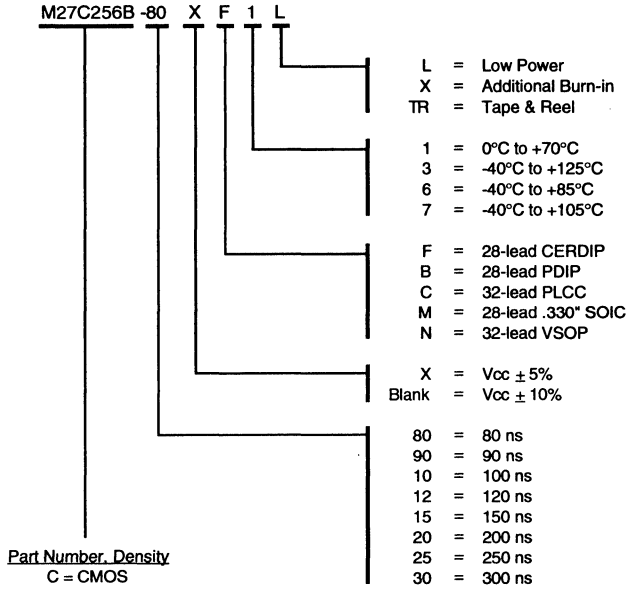


TEXAS INSTRUMENTS

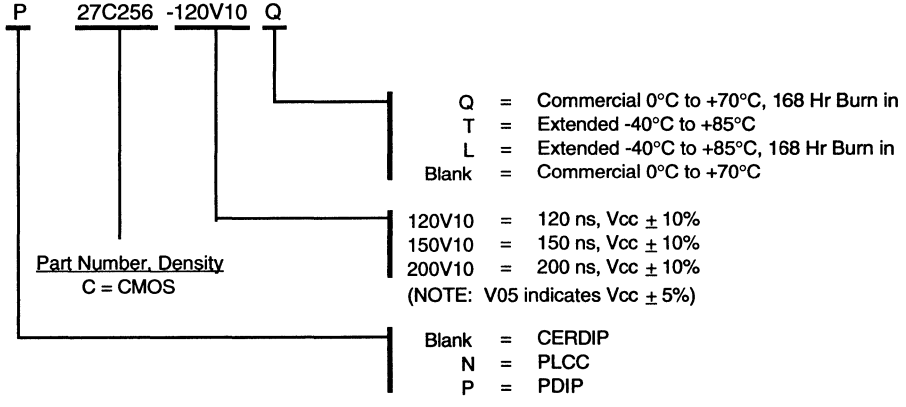


COMPETITIVE PART NUMBER BREAKDOWN (CONT.)

SGS-THOMSON



INTEL CORPORATION



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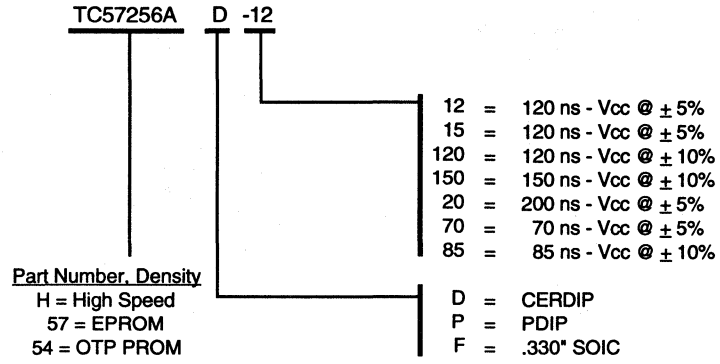
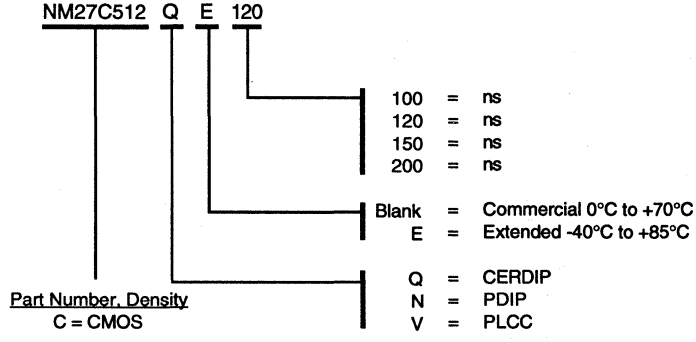
COMPETITIVE PART NUMBER BREAKDOWN (CONT.)

TOSHIBA CORPORATION

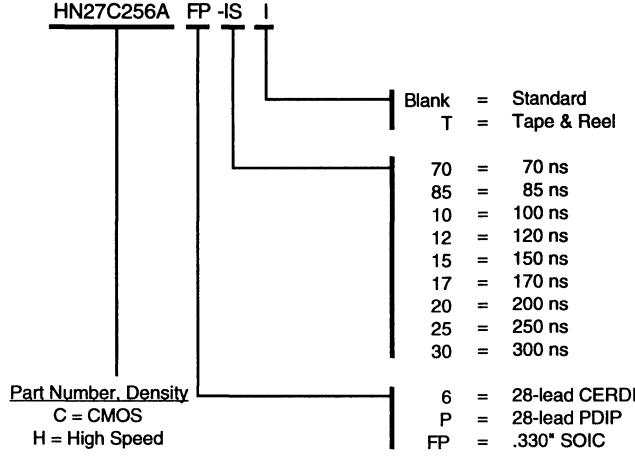


NATIONAL SEMICONDUCTOR CORPORATION

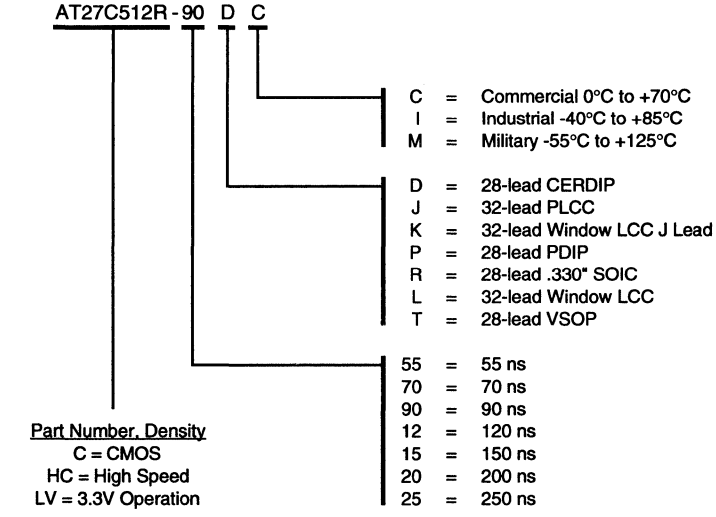


COMPETITIVE PART NUMBER BREAKDOWN (CONT.)

HITACHI CORPORATION



ATMEL CORPORATION



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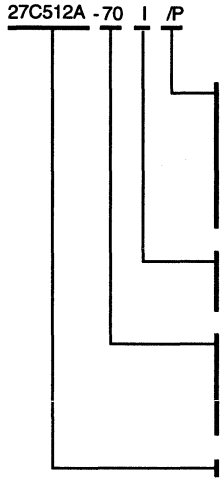
COMPETITIVE PART NUMBER BREAKDOWN (CONT.)

MICROCHIP TECHNOLOGY INCORPORATED



Package:	J	=	CERDIP
	K	=	Ceramic Leadless Chip Carrier
	L	=	Plastic Leaded Chip Carrier
	P	=	PDIP
	SO	=	Plastic SOIC
	TS	=	Thin Small Outline Package (TSOP) 8x20mm
	VS	=	Very Small Outline Package (TSOP) 8x13.4mm
Temperature Range:	-	=	0°C to 70°C
	I	=	-40°C to 85°C
	E	=	-40°C to 125°C
Access Time:	70	=	70 ns
	90	=	90 ns
	10	=	100 ns
	12	=	120 ns
	15	=	150 ns
Device:	27C512A		512K (64K x 8) CMOS EPROM
			T=Tape and Reel

MICROCHIP

Memory Products Division

EPROM Programming Guide

All Microchip EPROMs should be programmed using the Express algorithm (shown on reverse side). Other algorithms can cause high programming fallout and even retention failures due to undue stress on the chips. This list will be updated as information becomes available. Programmer models and revisions shown are subject to change by the manufacturers at any time.

Manufacturer	Model	Software Rev	Status
DATA I/O	S1000	24 or 25	Verified Express
DATA I/O	29B	24	Verified Express
DATA I/O	288	1.0	Vendor specifies Express
DATA I/O	2900	1.1, 1.2, 1.7	Vendor specifies Express
DATA I/O	3900	1.0, 1.4	Vendor specifies Express
DATA I/O	Autosite	1.0, 1.5	Vendor specifies Express
DATA I/O	Unisite	3.0, 3.1, 3.2	Vendor specifies Express
STAG	PP42	8.0	Verified close to Express, but user must manually select double-voltage verify
STAG	PP39		Same
ELAN	5000/932 Turbo	6.02V1	Vendor specifies Express
ELAN	5000/932	5.05V1	Vendor specifies Express
EPRO	Model 124		User-programmable to Express
LOGICAL DEVICES	AllPro 88,40	2.2	Express AND Low Voltage Support No Express support for Windows version (Exar)
LOGICAL DEVICES	GangPro 8+	1.1	Vendor specifies Express on latest releases
LOGICAL DEVICES	GangPro S		Fast, Rapid only
LOGICAL DEVICES	GangPro S,	1.0	Vendor specifies Express on latest releases
LOGICAL DEVICES	Husky		Fast, Rapid only
BYTEK	Multitrk-4000		Vendor specifies Express on latest releases

7

ADAPTERS

PLCC-to-DIP

Emulation Technology 32-28-01-P600

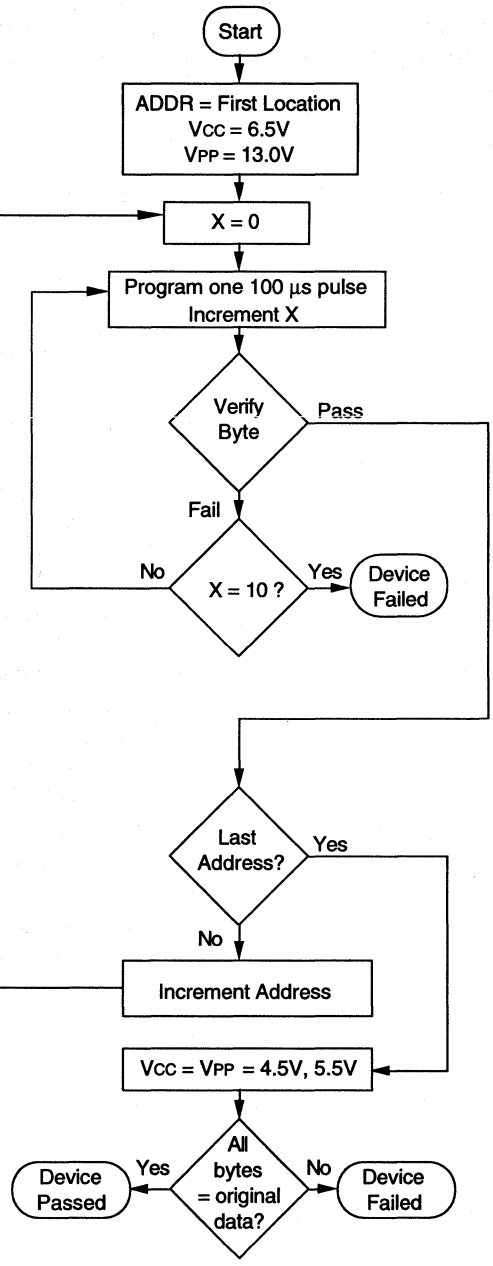
TSOP-to-DIP

Emulation Technology AS-32-28-02TS-6ENP-GANG-S

Emulation Technology Phone 408-982-0660, FAX 408-982-0664

EXPRESS ALGORITHM

Conditions:
T_{amb} = 25°C ±5°C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



SECTION 8
LOGIC PRODUCTS

MICROCHIP

AY0438

32-Segment CMOS LCD Driver

FEATURES

- Drives up to 32 LCD segments of arbitrary configuration
- CMOS process for: wide supply voltage range, low-power operation, high-noise immunity, wide temperature range
- CMOS, NMOS and TTL-compatible inputs
- Electrostatic discharge protection on all pins
- Cascadable
- On-chip oscillator
- Requires only three control lines
- Can be used to drive relays, solenoids, print head drives, etc.

APPLICATIONS

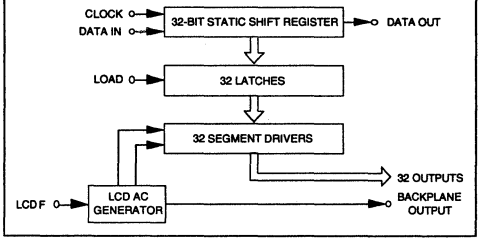
- Industrial displays
- Consumer product displays
- Telecom product displays
- Automotive dashboard displays

DESCRIPTION

The AY0438 is a CMOS LSI circuit that drives a liquid crystal display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.

The AY0438 can drive any standard or custom parallel drive LCD display, whether it be field effect or dynamic scattering; 7-, 9-, 14- or 16-segment characters; decimals; leading + or -; or special symbols. Several AY0438 devices can be cascaded. The AC frequency of the LCD waveforms can either be supplied by the user or generated by attaching a capacitor to the LCD input, which controls the frequency of an internal oscillator.

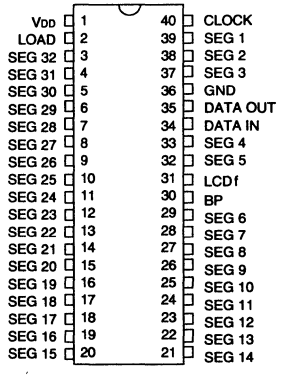
BLOCK DIAGRAM



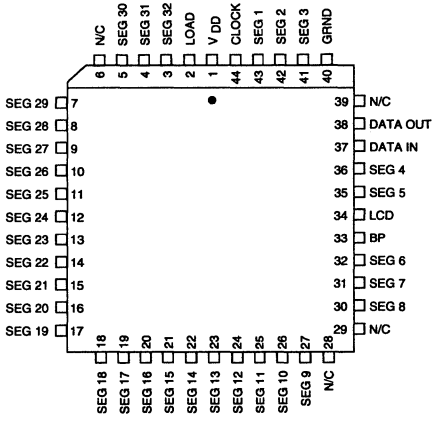
PIN CONFIGURATION

40-LEAD DUAL INLINE

Top View



44 PLCC



The device also acts as a versatile peripheral, able to drive displays, motors, relays and solenoids within its output limitations.

The AY0438 is available in 40-lead dual-in-line ceramic and plastic packages. Unpackaged dice are also available.

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PIN DESCRIPTION

Pin #	Name	Direction	Description
1	V_{DD}	-	Supply voltage
2	Load	Input	Latch data from registers
3-29, 32, 33, 37-39	Seg 1-32	Output	Direct drive outputs
30	BP	Output	Backplane drive output
31	LCDΦ	Input	Backplane drive input
34	Data In	Input	Data input to shift register
35	Data Out	Output	Data output from shift register
36	Vss	Ground	Ground
40	Clock	Input	System clock input

FIGURE 1 TIMING DIAGRAM

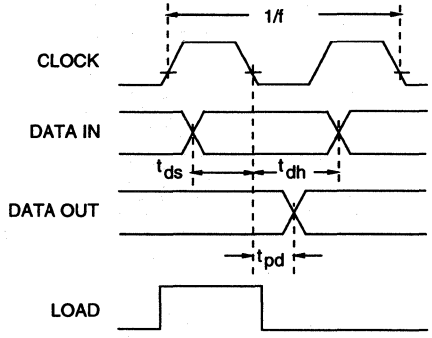
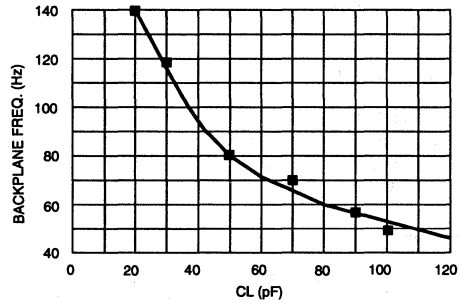


FIGURE 2 OSCILLATOR FREQUENCY GRAPH (TYPICAL @ 25°C)



OPERATING NOTES

1. The shift register loads, shifts, and outputs on the falling edge of the clock.
2. A logic 1 on Data In causes a segment to be visible.
3. A logic 1 on Load causes a parallel load of the data in the shift register into latches that control the segment drivers.
4. If LCDΦ is driven, it is in phase with the backplane output.
5. To cascade units, either connect backplane of one circuit to LCDΦ of all other circuits (thus one capacitor provides frequency control for all circuits) or connect LCDΦ of all circuits to a common driving signal. If the former is chosen, tie just one backplane to the LCD and use a different backplane output to drive the LCDΦ inputs. The data can be loaded to all circuits in parallel or else Data Out can be connected to Data In to form a long serial shift register.

6 The supply voltage of the AY0438 is equal to half the peak driving voltage of the LCD.

7. The LCDΦ pin can be used in two modes, driven or oscillating. If LCDΦ is driven, the circuit will sense this condition and pass the LCDΦ input to the backplane output. If the LCDΦ pin is allowed to oscillate, its frequency is inversely proportional to capacitance and the LCD drivingwaveforms have a frequency 2^8 slower than the oscillator itself. The relationship is shown graphically (see Figure 2). The frequency is nearly independent of supply voltage. If LCDΦ is oscillating, it is important to keep coupling capacitance to backplane and segments as low as possible. Similarly, it is recommended that the load capacitance on LCDΦ be as large as is practical.
8. There are two obvious signal races to be avoided in this circuit, (1) changing Data In when the clock is falling, and (2) changing Load when the clock is falling.
9. The number of a segment corresponds to how many pulses have occurred since its data was present at the input. For example, the data on SEG 17 was input 17 clock pulses earlier.
10. It is acceptable to tie the load line high. In this case the latches are transparent. Also, remote control would only require two signal lines: clock and Data In.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VDD.....-0.3V to +12V
Inputs (CLK, Data In, Load) .....VCC to VDD +0.3V
LCDΦ Input.....-0.3V to VDD +0.3V
Power Dissipation 250mW
Storage Temperature .....-65°C to +125°C
Operating Temperature Industrial .....-40°C to +85°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS — VDD = +5V unless otherwise noted, TA = -40°C to +85°C

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Supply Voltage	VDD	+3.0	-	+8.5	V	
Supply Current	IDD	-	25	60	µA	LCDΦ OSC < 15 kHz
		-	13	30	µA	LCDΦ OSC < 100Hz
Input High Level	VIH	0.5VDD	-	VDD	V	
Input Low Level Clock,	VIL1	0	-	0.1 VDD	V	3.0V ≤ VDD ≤ 8.5V
Data,	VIL2	0	-	0.1 VDD	V	3.0V ≤ VDD ≤ 8.5V
Input Leakage Current Load	IL	-	0.01	±10	µA	VIN = 0V and +5.0V
Input Capacitance	CI	-	-	5.0	pF	VDD = +5.0V
Segment Output Voltage	VOH	0.8VDD	-	VDD	V	IOH = -100µA
	VOL	0	-	0.1VDD	V	IOL = 100µA
LCDΦ Input High Level	VIN	0.9VDD	-	VDD	V	
LCDΦ Input Low Level	VIL	0	-	0.1VDD	V	
LCDΦ Input Leakage Current Level	IL	-	-	10	µA	VIN = 0V and +5.0V VDD = +5.0V

AC CHARACTERISTICS

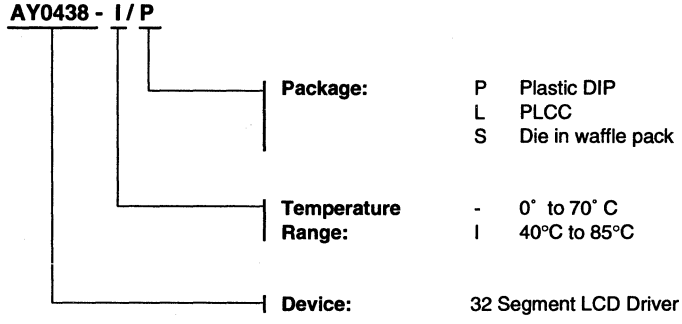
Characteristics	Sym	Min	Typ	Max	Units	Conditions
Clock Rate	f	DC	-	1.5	MHz	50% duty cycle
Data Set-up Time	tds	150	-	-	nsec	Data change to Clk falling edge
Data Hold Time	tdh	50	-	-	nsec	
Load Pulse Width	tpw	175	-	-	nsec	
Data Out Prop. Delay	tpd	-	-	500	nsec	CL = 55pF

8

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



SECTION 9
DEVELOPMENT SYSTEMS AND SOFTWARE TOOLS

MICROCHIP BBS

Microchip Bulletin Board Service

Get current information and help on Microchip's Bulletin Board Service (BBS)! Microchip wants to provide you with the best responsive service possible. To accomplish this, the systems team monitors the BBS, posting the latest component data and software tool updates, providing technical help and embedded systems insights, and discussing how Microchip products provide project solutions. Extend your technical groups staff with microcontroller and memory experts through Microchip's BBS communication channel.

CONNECTING TO MICROCHIP

Connect worldwide to the Microchip BBS using the Compuserve communications network. In most cases, a local call is your only expense. The Microchip BBS connection does not use Compuserve membership services, therefore **you do not need Compuserve membership to join Microchip's BBS.**

The procedure to connect will vary slightly from country to country. Please check with your local Compuserve agent for details if you have a problem. Compuserve services allows multiple users at buad rates up to 9600. To connect:

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal Compuserve setting which is 7E1.
2. Dial your local Compuserve phone number.
3. Type **<RETURN>** and a garbage string will appear because Compuserve is expecting a 7E1 setting.
4. Type **+<RETURN>** and Host Name: will appear.
5. Type **MCHIPBBS<RETURN>** and you will be connect to the Microchip BBS.

To learn Compuserve's phone number closest to you, set your modem to 7E1, and dial (800) 848 8980, and follow Compuserve's directions. If you are dialing from overseas, you may call 614-457-1550 for voice information.

Connect without charge to the bulletin board. However, you are responsible for your phone charges. Access is available to all, but users are required to register the first time they "log in." No registration fees are required at this time.

USING THE BULLETIN BOARD

The Microchip Bulletin Board is a multi-faceted tool. Topic information includes:

- Special Interest Groups
- Files
- Mail
- Bug lists
- Technical assistance
- Consultant Directory

Special Interest Groups

Special Interest Groups, or SIGs, offer you the opportunity to discuss technical issues and topics with other users. Take advantage of the Microchip user community's broad background to glean information not available by any other method.

SIGs exists for most Microchip systems, including:

- PIC16/17-SW
- PICMASTER
- PRO MATE™
- UTILITIES
- ENDURANCE
- MEMORY PRODUCTS
- BUGS
- APP NOTE

These groups are moderated by Microchip staff.

Files

The Microchip Systems BBS is used regularly to distribute bug reports, history files, and interim patches for Microchip software products.

Users can contribute files for distribution on the BBS. These files will be monitored, scanned, and approved or disapproved by the SIG moderator. No executable files are accepted from the user community in general.

Mail

The BBS can be used to distribute mail to other users of the service.

This is an excellent way to get questions answered by the Microchip staff, as well as to keep in touch with fellow Microchip product users worldwide.

The BBS is an evolving product intended to serve your needs. We welcome your ideas and input. Consider mailing a message to your SIG moderator, or to the SYSOP, if you have ideas or questions about particular Microchip products, or BBS operation.

NOTES:

PICSEE™ TOOLS

PICSEE Product Development Tools

INTRODUCTION

The PICSEE Development Systems provide the product development engineer with cost effective and timely design tool solutions for the MTA8XXXX family of 8-bit CMOS microcontrollers with serial EEPROM. They are designed specifically for the MTA8XXXX family. These tools work in conjunction with existing hardware and software design tools for the PIC16CXX microcontroller family. This allows the development engineer to efficiently implement systems utilizing these multichip modules with a minimal learning curve and capital investment.

PICSEEKIT — P/N AC812001

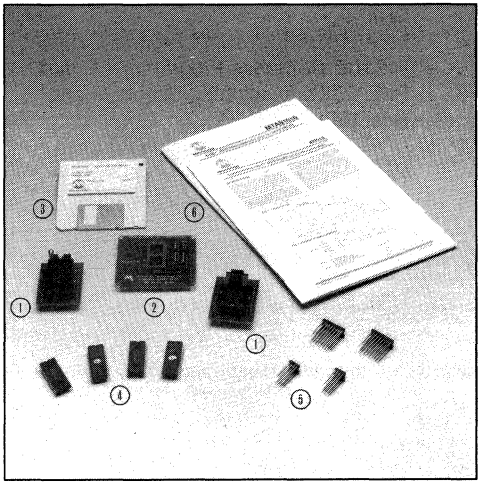
- Supports MTA81010
- Programming Adapters for PDIP and SOIC packages
- Daughter card for PICPROBE-16A
- I²C™ bus Serial Communication Application Software

This kit is supports the MTA81010 multichip module. It contains programming adapters, a PICMASTER™ emulator daughter board and MTA81010 product samples in 28-lead PDIP. Also included is an M-DOS®, PC-compatible 3.5-inch software diskette that contains example source code for implementing the I²C serial bus protocol to communicate with a Serial EEPROM. Documentation is provided for all of the included hardware and software.

Programming Support

Two programming adapters are provided to allow the MTA81010's internal program EPROM as well as it's data EEPROM to be programmed on existing programmers. Any programmer that supports Microchip's PIC16C54 can program the MTA81010's internal EPROM. Also, any programmer that supports Microchip's 24LC01B Serial EEPROM can program the MTA81010's internal Serial EEPROM. There is one adapter for MTA81010's in DIP packages and another for SOIC packages. Both DIP and SOIC programming adapters interface to programmers via a 300 mil DIP header.

FIGURE 1 - PICSEE™ INTRODUCTION DESIGN KIT



Description of Contents

1 • PICSEE PDIP and SOIC to PIC16C54 or 24LC01B Programming Adapter Sockets
2 • Header Interface for PICMASTER-16A and PICPROBE-16A
3 • Serial EEPROM Example Software Disk
4 • MTA81010 Product Samples
5 • 8- and 18-Pin Programming Adapter Plugs
6 • Complete Systems Documentation

I²C is a trademark of Philips.
MS-DOS is a registered trademark of Microsoft Corp.

Emulation Support

The emulator daughter board allows the developer to use Microchip's PICMASTER in-circuit emulator to emulate the MTA81010 Microcontroller with Serial EEPROM. This daughter board replaces Microchip's PIC16C5X Emulator Probe Header (P/N AC162009) emulator probe to support the MTA81010. The daughter board provides the required translation from a PIC16C54 pin out to the MTA81010 pin out. It also contains a discrete 24LC01B Serial EEPROM to provide the same functions as the MTA81010's internal EEPROM. This provides a cost-effective emulation solution to customers who may wish to purchase a PICMASTER in-circuit emulator or those that already have a PICMASTER.

Software Support

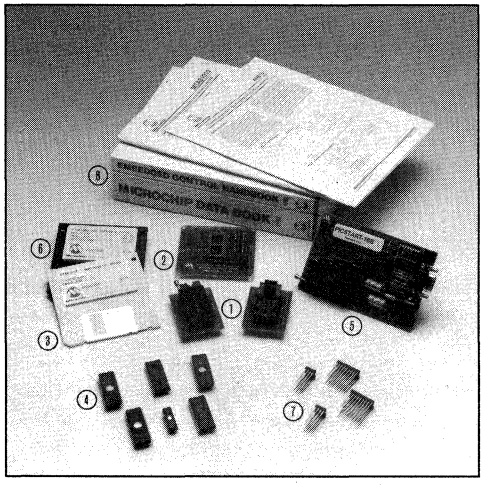
Example source code for I²C Bus communication with a serial EEPROM is included in the PICSEE. This pre-tested code can be used directly or modified by the developer to meet their specific needs. This example code is provided royalty free and license free.

PICSEESTART — P/N DV813001

- Complete Low-Cost Development Solution for MTA81010
- Combines PICSEEKIT AC812001 and PICSTART DV163001
- MPALC Assembler
- MPSIM Simulator
- Low-Cost Programmer
- Programming Adapter Sockets
- I²C Bus Applications Software

This kit combines the PICSEEKIT (P/N AC812001) with a PICSTART™ (P/N DV163001) to form a complete low-cost development system for the MTA81010 multichip module. It is designed to support the MTA81010 during the software development and initial prototype phases of new product development. It contains tools for software development and debugging, as well as programmer for programming the MTA81010's internal EPROM program memory. For a more detailed description, please refer to the PICSEEKIT P/N AC812001 and PICSTART P/N DV163001 product descriptions.

FIGURE 2 - PICSEESTART™ DEVELOPMENT KIT



Description of Contents

1 • PICSEE PDIP and SOIC to PIC16C54 or 24LC01B Programming Adapter Sockets
2 • Header Interface for PICMASTER-16A and PICPROBE-16A
3 • Serial EEPROM Example Software Disk
4 • MTA81010/PIC16CXX Product Samples
5 • PIC16CXX Device Programmer Board
6 • PIC16CXX Assembler, Simulator and Host Software
7 • 8- and 18-Pin Programming Adapter Plugs
8 • Complete Systems Documentation

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

PART NUMBER	DESCRIPTION
AC812001	PICSEEKIT FOR MTA81010
DV813001	PICSEESTART FOR MTA81010

MICROCHIP

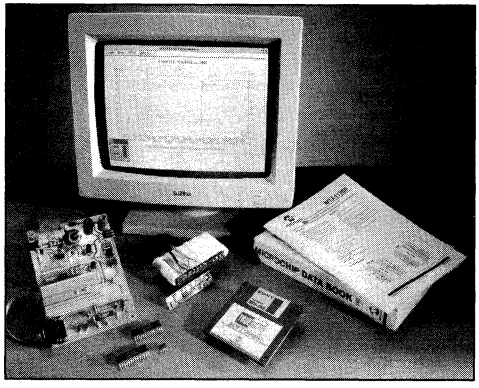
TRUEGAUGE™

TrueGauge™ Intelligent Battery Management Development Tool

INTRODUCTION

The MTA11200 TrueGauge Intelligent Battery Management IC is supported by a user friendly tool for system development. The DV114001 operates under Microsoft Windows®. This development tool enables for management of all phases of product development, including inception, debugging and maintenance. System design verification can be accomplished before a hardware prototype needs to be built, thus reducing time and cost. The user interface provides a graphically-oriented development environment. The data logging feature saves measured data into a file that can be imported to Excel®.

FIGURE 1 - TRUEGAUGE DEVELOPMENT TOOL KIT



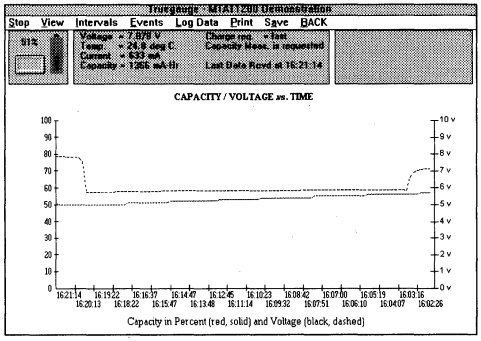
SUMMARY OF FEATURES

The TrueGauge development tool is a tool for system development under Windows. The development tool kit contains the following:

- NiCd battery with TrueGauge module
- NiMH battery with TrueGauge module
- Stand-alone TrueGauge module
- Charger/Discharger Interface Board
- Universal Power Supply with power cord
- PC Interface Cable with DB9-DB25 converter
- Design/Verification software on a 3.5" diskette
- MTA11200 and 24LC01B product samples
- MTA11200 Datasheet
- TrueGauge Development Tool User's Guide

Battery status information is plotted on the computer allowing for the real-time monitor of battery management parameters (see Figure 2).

FIGURE 2 - CAPACITY/VOLTAGE OVER TIME



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TrueGauge is a trademark of Microchip Technology Inc.
Microsoft Windows and Excel are registered trademarks of Microsoft Corporation.

Parameters can be changed easily and downloaded to the TrueGauge module (see Figures 3 and 4).

FIGURE 3 - CONFIGURATION CONTROL PANEL

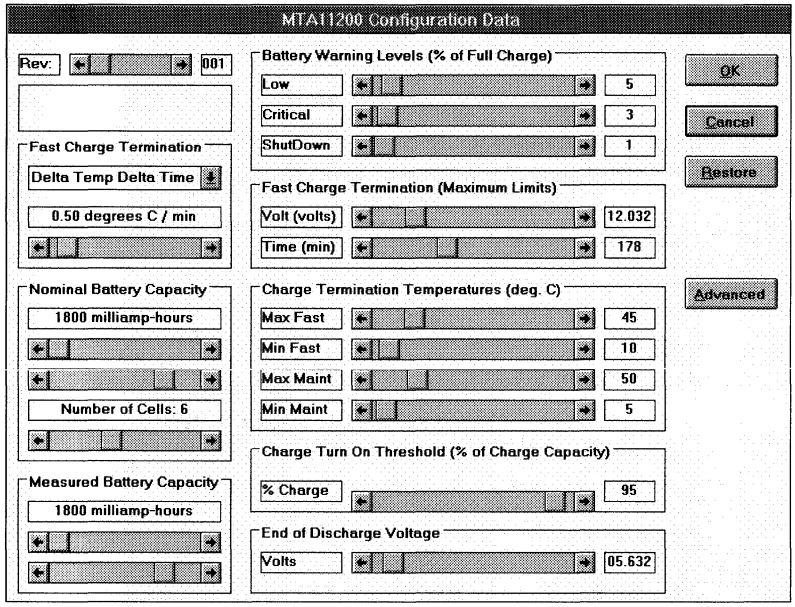
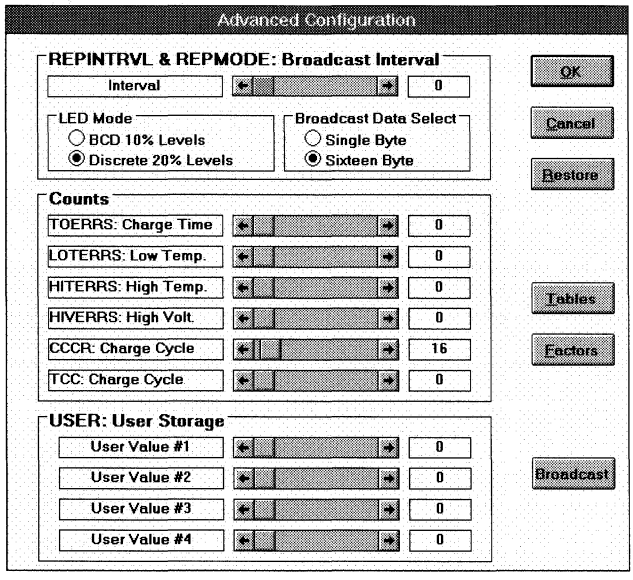


FIGURE 4 - ADVANCED CONFIGURATION DISPLAY



System design verification can be accomplished before hardware implementation (see Figures 6, 7 and 8).

FIGURE 5 - TRUEGAUGE VOLTAGE AND CAPACITY VS. TIME

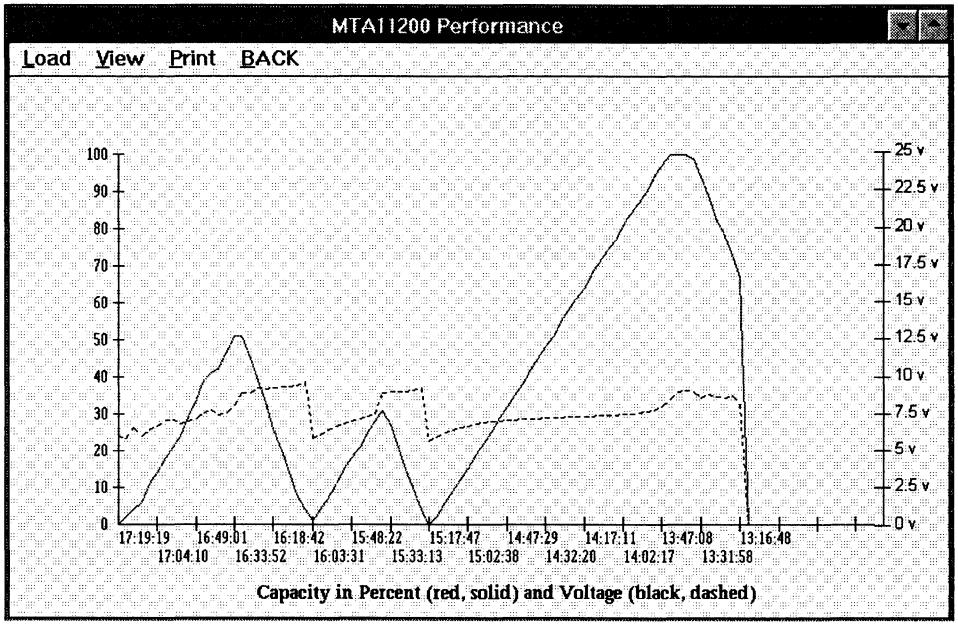


FIGURE 6 - TEMPERATURE VS. TIME

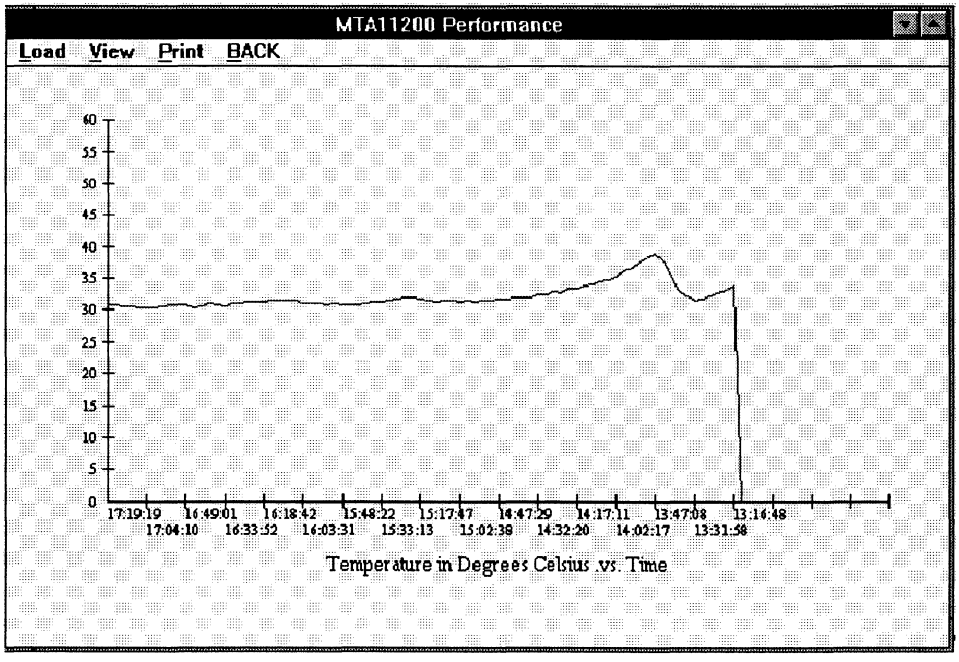


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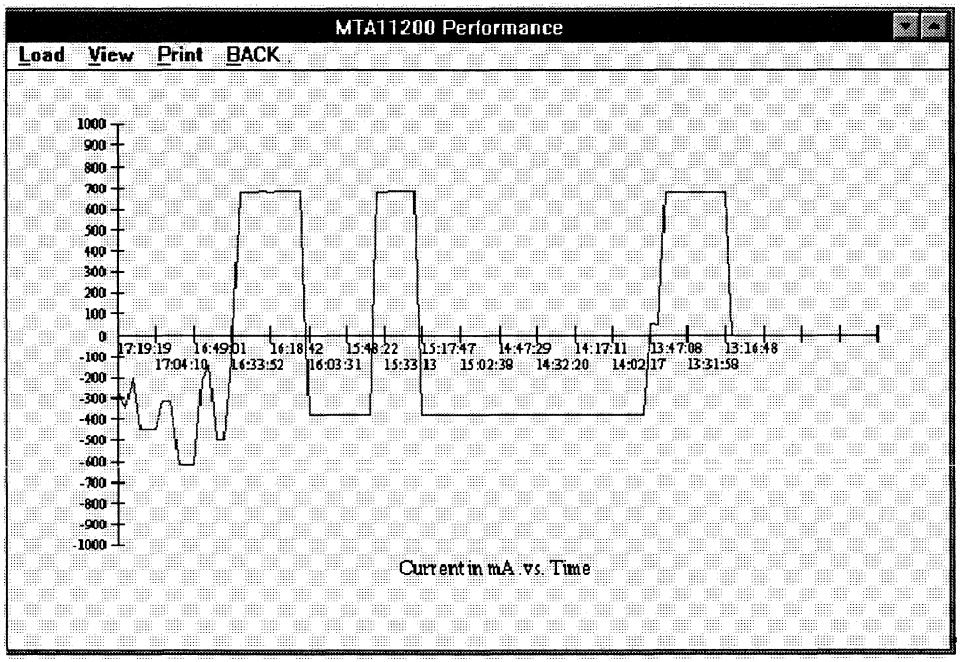
FIGURE 7 - CURRENT VS. TIME



A data logging feature saves measured data into a file that can be imported to Microsoft Excel (see Figure 8).

FIGURE 8 - EXAMPLE OF DATA LOG FILE

Time	Remaining Capacity (%)	Voltage	Temperature (C)	Current (mA)	Total Capacity (mA-Hr)	Flag_byte	Error_byte
22:39:13	9	8.645	23.88281	647	1200	BB	0
22:39:15	9	8.645	23.88672	647	1200	BB	0
22:39:23	9	8.646	23.90234	648	1200	BB	0
22:39:34	9	8.646	23.92188	647	1200	BB	0
22:39:44	9	8.647	23.9375	647	1200	BB	0
22:39:55	9	8.647	23.95313	647	1200	BB	0
22:40:04	10	8.647	23.96484	647	1200	BB	0
22:40:14	10	8.648	23.96875	647	1200	BB	0
22:40:25	10	8.648	23.98047	647	1200	BB	0

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

PART NUMBER	DESCRIPTION
DV114001	TRUEGAUGE DEVELOPMENT TOOL

MICROCHIP

PICMASTER™ System

PICMASTER Universal In-Circuit Emulator System

SYSTEM FEATURES

General:

- Complete Hi-Performance PC-based Microcontroller Development System for the PIC16/17 families.
- For use on PC-compatible 286, 386, and 486 machines under Microsoft Windows® 3.X environment.
- Assembler Software, Emulator System, and EPROM Programmer unit, sample kit, and demonstration hardware and software provide a complete microcontroller product development environment.

Emulator System:

- Hi-Performance In-Circuit Emulation of Microchip Microcontrollers.
- Real-time instruction emulation.
- Single and Multiple instruction step execution.
- Program Memory emulation and memory mapping capability up to 64K words. Instruction execution can be mapped into either emulation memory or user prototype memory.
- Real-time trace memory capture of 40 bits of information for each instruction cycle in an 8Kx40 trace buffer. Trace region can range from 0 to 64K in any address combinations.
- Real-time trace data can be captured and displayed without halting emulation.
- Unlimited number of hardware breakpoints can be set anywhere in the program memory.
- External Break with "AND"/"OR" capability with internal breakpoints.
- Multiprocessor emulation capability. Up to eight PICMASTER emulators can be synchronized on a single PC, for multi-processor development.
- Extended 48-bit cycle counter.
- Trigger Output available on any range of addresses.
- Full Symbolic Debug Capability. Symbolic display and alter of all register files, special purpose registers, stack registers, and bank registers.
- Selectable Internal Emulator Clock or User Target (Prototype) System Clock.
- User selectable internal or external Power Supply (provided).

PICMASTER is a trademark of Microchip Technology Inc.
Windows is a registered trademark of Microsoft Corp.

EPROM Programmer System:

- PRO MATE™ Device Programmer unit for all current PIC16/17 products.
- Operates as a Stand-alone Unit or in Conjunction with a PC-compatible host system.
- Performs READ, PROGRAM, and VERIFY functions in Stand-alone mode.
- PC Host Software provides file display and editing, file transfer to and from programmer unit, device serialization, and program voltage calibration.

Macro Assembler:

- Provides translation of Assembler source code to object code for the PIC16/17 family of microcontrollers.
- Macro-assembly and conditional assembly capability.
- Produces Object files, Listing files, Symbol files, and special files required for symbolic debug with the PICMASTER Emulator System.
- Binary / Hex output formats: INHX8S, INHX8M, INHX16, and PICMASTER.

Demo Board:

The PICDEM-I Demostration Board provides a user with a simple hardware tool through which software can be exercised and debugged. A step-by-step tutorial enables first-time users of PICMASTER to become familiar with all the features of the emulator. A generous prototype area (200 holes) allows the user to build additional hardware for their project.

SYSTEM DESCRIPTION

The PICMASTER Universal In-Circuit Emulator System is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16/17 family. The PICMASTER system currently supports the PIC16C54, PIC16C55, PIC16C56 and PIC16C57 at clock frequencies of 4 MHz; the PIC16C64, PIC16C71, PIC16C74, PIC16C84 to 10 MHz; and the PIC17C42 at 4 MHz.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new microcontroller architectures with data and program memory paths to 16 bits.

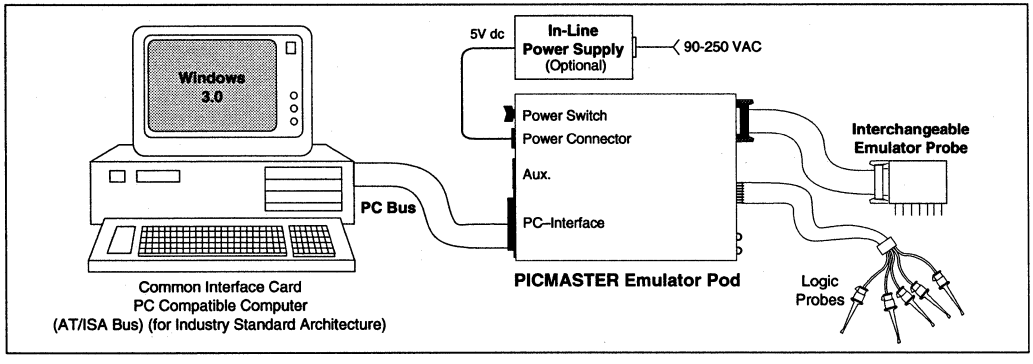
The Emulator System is designed to operate on low-cost PC-compatible machines ranging from 286-AT® class ISA-bus systems through the new 486 EISA-bus machines. The development software runs in the Microsoft Windows 3.X environment, allowing the operator access to a wide range of supporting software and accessories.

Provided with the PICMASTER System is a high performance, real-time In-Circuit Emulator, a microcontroller programmer unit, a macro assembler program, and a simulator program. Sample programs are provided to help quickly familiarize the user with the development system and the PIC16/17 microcontroller families.

Coupled with the user's choice of text editor, the system is ready for development of products containing any of Microchip's microcontroller products.

A "Quick Start" Product Sample Pak containing user programmable parts is included for additional convenience (only devices supported by the probe header).

Microchip provides additional customer support to developers through an electronic Bulletin Board System (BBS). Customers have access to the latest updates in software as well as application source code examples. Consult your local sales representative for information on accessing the BBS system.



PRO MATE is a trademark of Microchip Technology Inc.
AT is a registered trademark of IBM Corp.

Host System Requirements:

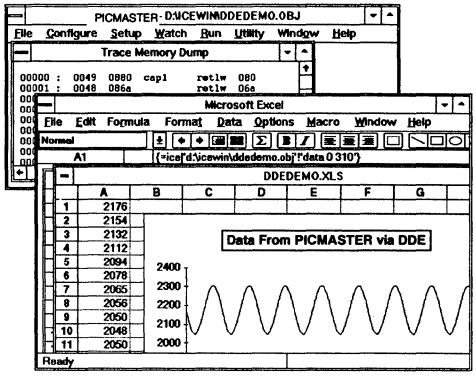
The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.X environment was chosen to best make these features available to you the end user. To properly take advantages of these features, PICMASTER requires installation on a system having the following minimum configuration:

- PC/AT-compatible machine: 286, 386SX, 386DX, or 486 with ISA or EISA Bus.
- EGA, VGA, 8514/A, Hercules graphic card (EGA or higher recommended).
- MS-DOS® / PC-DOS version 3.1 or greater.
- Microsoft® Windows version 3.0 or greater operating in either standard or 386 enhanced mode).
- 1 Mbyte RAM (2 Mbytes recommended).
- One 3.5" floppy disk drive.
- Approximately 10 Mbytes of hard disk (1 Mbyte required for PICMASTER, remainder for Windows 3.X system).
- One 8-bit PC/AT (ISA) I/O expansion slot (half size)
- Microsoft® mouse or compatible (highly recommended).

Emulator System Components:

The PICMASTER Emulator Universal System consists primarily of four major components:

- **Host-Interface Card:** The PC Host Interface Card connects the emulator system to a PC compatible system. This high-speed parallel interface requires a single half-size standard AT / ISA slot in the host system. A 37-conductor cable connects the interface card to the external Emulator Control Pod.
- **Emulator Control Pod:** The Emulator Control Pod contains all emulation and control logic common to all microcontroller devices. Emulation memory, trace memory, event and cycle timers, and trace/breakpoint logic are contained here. The Pod controls and interfaces to an interchangeable target-specific emulator probe via a 14" precision ribbon cable.
- **Target-specific Emulator Probe:** A probe specific to microcontroller family to be emulated is installed on the ribbon cable coming from the control pod. This probe configures the universal system for emulation of a specific microcontroller. Currently, the PIC16C5X family, PIC16CXX family, and the PIC17C42 microcontrollers are supported. Future microcontroller probes will be available as they are released.



- **PC Host Emulation Control Software:** Host software necessary to control and provide a working user interface is the last major component of the system. The emulation software runs in the Windows 3.X environment, and provides the user with full display, alter, and control of the system under emulation. The Control Software is also universal to all microcontroller families.

  The Windows 3.X System is a multitasking operating system which will allows the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

  PICMASTER emulation can operate in one window, while a text editor is running in a second window. Dynamic Data Exchange (DDE), a feature of Windows 3.X, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

  Under Windows 3.X, up to eight PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16CXX processor and a PIC17CXX processor).

PRO MATE Device Programmer:

The PRO MATE Programmer system included in the PICMASTER Development System provides the product developer with the ability to program (transfer) the developer's software into PIC16/17 microcontrollers.

The programmer unit comes complete with accessories for use with a PC host computer. Supplied are interface cables and connectors to a standard PC serial port , a power supply unit, and host operating software.

The PRO MATE Programmer will work in either standalone mode, or in PC host connected mode. Connected to a PC host, many more features are available to the user.

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STAND-ALONE MODE

Stand-alone mode is useful in situations where a PC may not be available or even required, such as in the field or in a lab production environment. In stand-alone mode the following programming functions are available:

VERIFY

VERIFY preforms two functions. For a programmed part, the device in the programming socket will be compared to the program data stored in internal memory. If the data and fuse settings are correct, VERIFIED will be displayed. VERIFY will also confirm that erased parts are blank. A device in the socket will display ERASED if all programmable locations are blank.

PROGRAM

In stand-alone mode, devices inserted into the programmer socket will be programmed with data currently stored in memory. Pressing the PROGRAM key will cause the unit to program and verify both the program memory and the device fuses. If all program successfully, PGM OKAY will be displayed.

READ

A pre-programmed device placed in the programmer socket can be read into the programmer unit by pressing the READ key. Program and fuse data will be read and stored into internal memory. Various options exist with the READ function.

PC HOST CONNECT MODE

When the PRO MATE is connected to a host PC system, many more options and conveniences are available to the user. Host mode allows full interactive control over the PRO MATE unit. A full screen, user-friendly software program is provided to fully assist the user.

As in stand-alone mode, parts may be Read, Programmed, Blank checked, and Verified. Also, all fuses and ID locations may be specified. In addition, other features available in host-mode are:

Editing

A large screen buffer editing facility allows the user to change and program location in hexadecimal. Complete program and fuse data can be loaded and saved to DOS disk files. Files generated by the Assembler program are directly loadable into programmer memory.

VDD and VPP Adjust

The programming environment voltage settings of VDD max, VDD min, and VPP can be set and altered only on PC host mode. The voltage settings allow the user to program the part in the environment that the part will be used. The part will be programmed at VDD max and verified at VDD min. VPP is the programming voltage.

PICMASTER PROBE Specifications

Table 1 shows the current probe specifications for the PICMASTER In-Circuit Emulator. The devices are supported regardless of program memory type (ROM, EPROM or EEPROM), process technology or voltage range. That is, selecting the PROBE that supports the PIC16C54 (-16A) also supports the PIC16CR54, PIC16C54A and the PIC16LC54A devices. The probe would also support other variations as they become available (such as PIC16CR54A).

TABLE 1: PICMASTER PROBE SPECIFICATIONS

PICMASTER PROBE	Devices Supported	PROBE Maximum Frequency	PROBE Operating Voltage
PROBE - 16A	PIC16C54, PIC16C55, PIC16C56, and PIC16C57	4 MHZ	4.5V - 5.5V
PROBE - 16B	PIC16C71	10 MHZ	4.5V - 5.5V
PROBE - 16C	PIC16C84	10 MHZ	4.5V - 5.5V
PROBE - 16D	PIC16C54, PIC16C55, PIC16C56, PIC16C57, and PIC16C58	20 MHz	4.5V - 5.5V
PROBE - 16E	PIC16C64	10 MHZ	4.5V - 5.5V
PROBE - 16F	PIC16C74	10 MHZ	4.5V - 5.5V
PROBE - 17A	PIC17C42	16 MHZ	4.5V - 5.5V

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBER	DESCRIPTION
EM167007	Complete PICMASTER-16A System for PIC16C5X
EM167010	Complete PICMASTER-16A System for PIC16C5X without Programmer
EM167011	Complete PICMASTER-16B System for PIC16C71
EM167012	Complete PICMASTER-16B System for PIC16C71 without Programmer
EM167013	Complete PICMASTER-16C System for PIC16C84
EM167014	Complete PICMASTER-16C System for PIC16C84 without Programmer
EM167017	Complete PICMASTER-16E System for PIC16C64
EM167018	Complete PICMASTER-16E System for PIC16C64 without Programmer
EM167019	Complete PICMASTER-16F System for PIC16C74/C73
EM167020	Complete PICMASTER-16F System for PIC16C74/C73 without Programmer
EM177001	Complete PICMASTER-17 System for PIC17C42
EM177004	Complete PICMASTER-17 System for PIC17C42 without Programmer

MICROCHIP

PRO MATE™

CMOS Microcontroller Programmer Unit

SYSTEM FEATURES

EPROM Programmer System:

- PRO MATE Programmer unit for the PIC16CXX, PIC17CXX Microcontroller family.
- Operates as a Stand-alone Unit or in Conjunction with a PC Compatible host system.
- READS, PROGRAMS, and VERIFIES in Stand-alone mode.
- PC Host Software provides file display and editing, and transfer to and from Programmer unit
- Communication Via RS-232

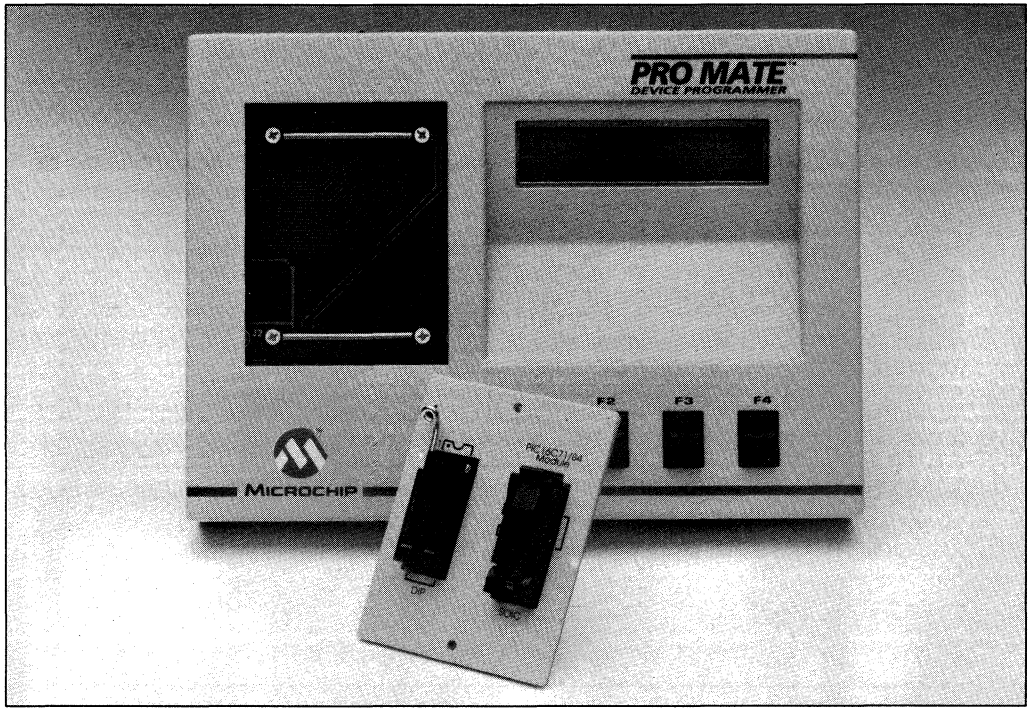
SYSTEM DESCRIPTION

PRO MATE Programmer:

The PRO MATE Programmer system provides the product developer with the ability to program user software into PIC16CXX, PIC17CXX CMOS microcontrollers.

The programmer unit comes complete with accessories to be used with the PC host computer. Supplied are interface cables and connectors to a standard PC serial port, a universal input power supply unit, and host operating software.

The PRO MATE Programmer will work in either stand-alone mode, or in PC host connected mode. Connected to a PC host, many more features are available to the user.



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STAND-ALONE MODE

Stand-alone mode is useful in situations where a PC may not be available or even required, such as in the field or in a lab production environment. In stand-alone mode the following programming functions are available:

VERIFY

VERIFY performs two functions. For a programmed part, the device in the programming socket will be compared to the program data stored in internal memory. If the data and fuse settings are correct, VERIFIED will be displayed. VERIFY will also confirm that erased parts are blank. A device in the socket will display ERASED if all programmable locations are blank.

PROGRAM

In stand-alone mode, devices inserted into the programmer socket will be programmed with data currently stored in memory. Pressing the PROGRAM key will cause the unit to program and verify both the program memory and the device fuses. If all program successfully, PGM OKAY will be displayed.

READ

A pre-programmed device placed in the programmer socket can be read into the programmer unit by pressing the READ key. Program and fuse data will be read and stored into internal memory. Various options exist with the READ function.

PC HOST CONNECT MODE

The PRO MATE provides a very user friendly user interface which allows complete control over the programming session.

The PRO MATE host software is a DOS windowed environment with full mouse support to allow the user to point and click when entering commands.

The Host Software communicates with the PRO MATE via the serial port of the PC. Any of the four (COM 1-4) ports may be used. The communication is done at 19200 baud to insure fast throughput. Communication will be established with the PRO MATE Device Programmer prior to any transfers taking place.

Serialization is done by generating a serialization file, and then using that file to serialize locations in the PIC microcontroller. Once a serialization file is generated, it may be used over different programming sessions. Serial numbers are automatically marked as used when a PIC is programmed successfully with that serial number.

Complete control over the programming environment is also provided. Control over the programming and verify voltage of Vdd insures that the Microcontroller will perform in the desired environment. Programming (Vpp) voltage is also adjustable to insure complete compatibility with future programming algorithms.

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

SOCKET PART NUMBER	DESCRIPTION
AC164001	PIC16C54 thru C57 18 & 28 Lead PDIP Socket Module
AC164002	PIC16C54 thru C57 18 & 28 Lead SOIC Socket Module
AC164003	PIC16C54/56 20 lead SSOP Socket Adapter†
AC164010	PIC16C71/84 18 Lead PDIP/SOIC Socket Module
AC164011	PIC16C55/57 28 Lead SSOP Socket Adapter†
AC164012	PIC16C64/C74 40 Lead PDIP Socket Module
AC164013	PIC16C64/C74 44 Lead PLCC Socket Module
AC164014	PIC16C64/C74 44 Lead PQFP Socket Adapter†
AC174001	PIC17C42 40 Lead PDIP Socket Module
AC174002	PIC17C42 44 Lead PLCC Socket Module
AC174003	PIC17C42 44 Lead QFP Socket Module

PROGRAMMER PART NUMBER	DESCRIPTION
PG007001	Programmer Kit as described above
PG007002	Programmer Kit without power supply

Socket modules are sold separately.

† This item is a socket adapter. When using this adapter, a PDIP socket module is also required.

MICROCHIP

PICSTART™-16B1

PIC16CXX Low-Cost Microcontroller Development System

SYSTEM FEATURES

EPROM Programmer System:

- EPROM Programmer unit for the PIC16C5X and selected PIC16CXX Microcontroller family members. Supports PIC16C54, PIC16C55, PIC16C56, PIC16C57, PIC16C71, PIC16C84.
- Operates with a PC-compatible host system.
- READS, PROGRAMS, and VERIFIES EPROM Memory.
- PC Host Software provides file display and editing, and transfer to and from Programmer unit.
- Universal power supply
- RS232 interface cable
- Universal power plug adapters

Macro Assembler:

- Provides translation of Assembler source code to object code for all PIC16CXX microcontroller product family.
- Macro-Assembly capability.
- Provides Object files, Listing files, Symbol files, and special files required for symbolic debug with the PIC16CXX Emulator System.
- Output formats: INHX8S, INHX8M and INHX16.

Simulator:

- Instruction-level Simulator of the PIC16CXX microcontroller product family.
- For PC-compatible systems running the MS-DOS® operating system.
- Full screen simulation user interface.
- Symbolic debugging capability.
- I/O stimulus input capability.

"Quick Start" Sample Kit:

- Provides the User / Developer with a sample kit of PIC16CXX parts for initial prototype use.

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MS-DOS is a registered trademark of Microsoft Corp.

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SYSTEM DESCRIPTION

The PICSTART-16B1 Development System provides the product development engineer with an alternative low-cost introductory microcontroller design tool set for the PIC16CXX family where full real-time emulation is not required. The equipment in the PICSTART-16B1 system operates on any PC compatible machine running the MS-DOS/PC-DOS operating system.

Provided in the System is an MS-DOS-based Software Simulator program (MPSIM), a microcontroller EPROM programmer, and a macro assembler program (MPALC).

Sample software programs to be run on the simulator are provided to help the user to quickly become familiar with the development system and the PIC16CXX microcontroller line.

The user need only provide his or her own preferred text editor and the system is ready for development of end products using the PIC16C54, PIC16C55, PIC16C56, PIC16C57, PIC16C71 or PIC16C84 microcontrollers.

A "Quick Start" PIC16CXX Product Sample Pak containing user programmable parts is also included.

Microchip provides additional customer support to developers through an electronic Bulletin Board System (BBS). Customers have access to the latest updates in software as well as application source code examples. Consult your local sales representative for information on accessing the BBS.

PICSTART-16B1 Development Programmer:

The Microchip device programmer system included in the PICSTART-16B1 Development System provides the product developer with the ability to program user software into PIC16CXX EPROM microcontrollers. It is designed to be a development programmer and not recommended for use in a production environment.

The programmer unit connects to a standard PC serial port.

A full screen, user-friendly software program is provided for full interactive control over the programmer. Parts may be Read, Programmed, Blank checked and Verified. Also, all fuses and ID locations may be specified.

A large screen buffer editing facility allows the user to change and program location in hexadecimal. Complete program data can be loaded and saved to DOS disk files. Files generated by the MPALC Assembler program are directly loadable into programmer memory.

MPSIM Simulator:

The MPSIM Simulator program provides the developer with an instruction and limited I/O simulator software program for debugging PIC16CXX assembler code.

The simulator is meant for use with smaller projects not requiring precise more extensive development equipment. Since the PIC16CXX architecture is essentially a single tasking microcontroller without interrupts, many applications can be developed by using a simulator program alone.

The MPSIM Simulator has the following features to assist in the debugging of software/firmware for the user.

Program Load/Save

Commands exist to load assembled object file programs into simulation memory. Conversely, programs may be saved from program simulation memory back to the PC disk.

Display & Alter

Provisions are made to display and alter Program Memory, Register Files, and status register bits. Also simulator information such as cycle times, elapsed time, and step count can be displayed.

Utility Functions

Various utility functions exist which assist the user in operating the simulator. Memory and registers can be cleared by command. Memory can be searched to find occurances of instructions, register use, and ASCII data.

Disassembler

Program memory can be disassembled showing both hexadecimal data and instruction mnemonics for specified address ranges.

Symbolic Debugging

The simulator provides for symbolic referencing to aid and simplify debugging. The symbol table may be displayed. New symbols defined and unwanted symbols deleted.

Execution and Trace

During program execution, address ranges, registers, register contents, and others can be traced.

Breakpoints

The user may specify up to 512 breakpoints at any one time.

SALES AND SUPPORT

To order or to obtain information, e.g., on the pricing or delivery, please use the listed part number, and refer to the listed sales offices.

PART NUMBER	DESCRIPTION
DV163003	PICSTART-16B1 DEVELOPMENT SYSTEM

MS-DOS is a registered trademark of Microsoft Corp.

MICROCHIP

PICSTART™-16C

PIC16CXX Low-Cost Microcontroller Development System

SYSTEM FEATURES

EPROM Programmer System:

- EPROM Programmer unit for the PIC16CXX Microcontroller family. Supports the PIC16C64 and the PIC16C74.
- Operates with a PC-compatible host system.
- READS, PROGRAMS, and VERIFIES EPROM Memory.
- PC Host Software provides file display and editing, and transfer to and from Programmer unit.
- Universal power supply
- RS232 interface cable
- Universal power plug adapters

Macro Assembler:

- Provides translation of Assembler source code to object code for all PIC16CXX microcontroller product family.
- Macro-Assembly capability.
- Provides Object files, Listing files, Symbol files, and special files required for symbolic debug with the PIC16CXX Emulator System.
- Output formats: INHX8S, INHX8M and INHX16.

Simulator:

- Instruction-level Simulator of the PIC16CXX microcontroller product family.
- For PC-compatible systems running the MS-DOS® operating system.
- Full screen simulation user interface.
- Symbolic debugging capability.
- I/O stimulus input capability.

"Quick Start" Sample Kit:

- Provides the User / Developer with a sample kit of the supported PIC16CXX parts for initial prototype use.

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MS-DOS is a registered trademark of Microsoft Corp.

SYSTEM DESCRIPTION

The PICSTART-16C Development System provides the product development engineer with an alternative low-cost introductory microcontroller design tool set for the PIC16CXX family where full real-time emulation is not required. The equipment in the PICSTART-16C system operates on any PC compatible machine running the MS-DOS/PC-DOS operating system.

Provided in the System is an MS-DOS-based Software Simulator program (MPSIM), a microcontroller EPROM programmer, and a macro assembler program (MPASM).

Sample software programs to be run on the simulator are provided to help the user to quickly become familiar with the development system and the PIC16CXX microcontroller line.

The user need only provide his or her own preferred text editor and the system is ready for development of end products using the PIC16C64 or the PIC16C74.

A "Quick Start" PIC16CXX Product Sample Pak containing user programmable parts is also included.

Microchip provides additional customer support to developers through an electronic Bulletin Board System (BBS). Customers have access to the latest updates in software as well as application source code examples. Consult your local sales representative for information on accessing the BBS.

PICSTART-16C Development Programmer:

The Microchip device programmer system included in the PICSTART-16C Development System provides the product developer with the ability to program user software into PIC16CXX EPROM microcontrollers. It is designed to be a development programmer and not recommended for use in a production environment.

The programmer unit connects to a standard PC serial port.

A full screen, user-friendly software program is provided for full interactive control over the programmer. Parts may be Read, Programmed, Blank checked, and Verified. Also, all fuses and ID locations may be specified.

A large screen buffer editing facility allows the user to change and program location in hexadecimal. Complete program data can be loaded and saved to DOS disk files. Files generated by the MPASM Assembler program are directly loadable into programmer memory.

MPSIM Simulator:

The MPSIM Simulator program provides the developer with an instruction and limited I/O simulator software program for debugging PIC16CXX assembler code.

The simulator is meant for use with smaller projects not requiring precise more extensive development equipment. Since the PIC16CXX architecture is essentially a single tasking microcontroller without interrupts, many applications can be developed by using a simulator program alone.

The MPSIM Simulator has the following features to assist in the debugging of software/firmware for the user.

Program Load/Save

Commands exist to load assembled object file programs into simulation memory. Conversely, programs may be saved from program simulation memory back to the PC disk.

Display & Alter

Provisions are made to display and alter Program Memory, Register Files, and status register bits. Also simulator information such as cycle times, elapsed time, and step count can be displayed.

Utility Functions

Various utility functions exist which assist the user in operating the simulator. Memory and registers can be cleared by command. Memory can be searched to find occurances of instructions, register use, and ASCII data.

Disassembler

Program memory can be disassembled showing both hexadecimal data and instruction mnemonics for specified address ranges.

Symbolic Debugging

The simulator provides for symbolic referencing to aid and simplify debugging. The symbol table may be displayed. New symbols defined and unwanted symbols deleted.

Execution and Trace

During program execution, address ranges, registers, register contents, and others can be traced.

Breakpoints

The user may specify up to 512 breakpoints at any one time.

SALES AND SUPPORT

To order or to obtain information, e.g., on the pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

PART NUMBER	DESCRIPTION
DV163002	PICSTART-16C DEVELOPMENT SYSTEM

MS-DOS is a registered trademark of Microsoft Corp.

MICROCHIP

PICDEM-I

Low-Cost PIC16/17 Demonstration Board

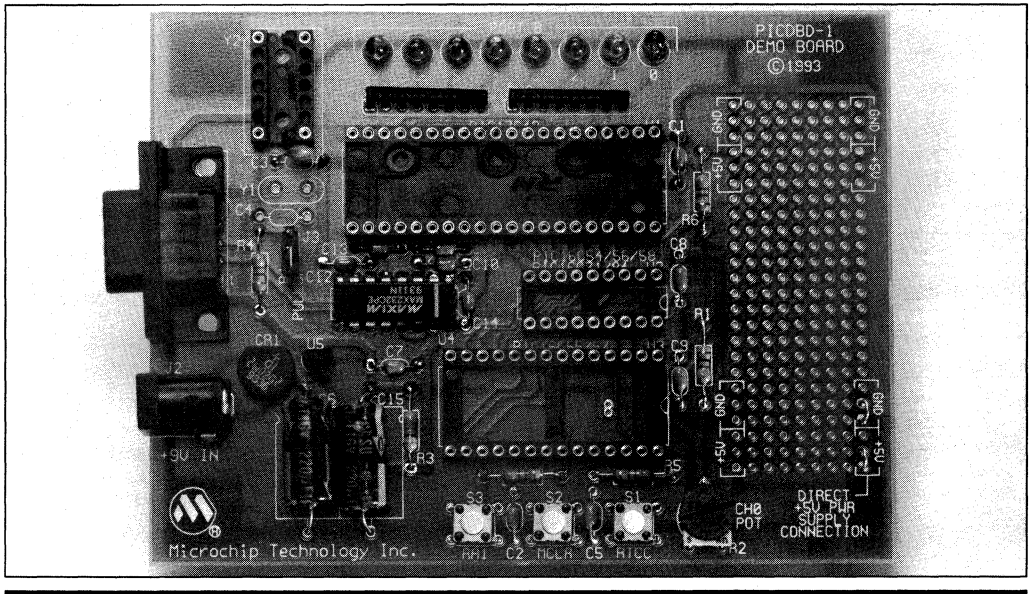
PRODUCT INFORMATION

The PICDEM-I is a simple board which demonstrates the capabilities of several Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58), PIC16C71, PIC16C84 and PIC17C42. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5" disk. The users can program the samples (one each of PIC17C42, PIC16C71 and PIC16C55) provided with the PICDEM-I, on a PRO MATE™ or PICSTART™ programmer and easily debug/test the sample code, or the user can connect the PICDEM-I with the PICMASTER emulator and download the sample code to the emulator and debug/test the code. Additionally, a generous 200-hole prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s).

FEATURES:

Hardware:

- 40-pin, 28-pin and 18-pin Precision sockets for all supported microcontrollers.
- On board +5V regulator and filter rectifier for direct input from 9V AC/DC wall adapter.
- RS232 socket and associated hardware for direct connection to RS232 interface.
- 5K pot to simulate analog input for PIC16C71.
- Three push button Key for external stimulus and RESET.
- Eight bright LEDs connect to PortB, help in displaying 8-bit binary values on PortB.
- Socket for "canned" crystal Oscillator.
- Unpopulated holes provided for Xtal connection
- Jumper to disconnect on board RC Oscillator.
- 200-hole prototype area for user's hardware.



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Software:

- Program for PIC16C71 to demonstrate on-chip A/D features.
- Program for PIC16C84 to demonstrate on-chip EEPROM.
- Program for PIC17C42 to demonstrate on-chip USART.
- Program for PIC16C5X to demonstrate key input capability.
- All demo programs supplied on 3.5" disk,
- Additional programs available on Microchip's BBS.

DOCUMENTATION

- A comprehensive User's Guide with easy to follow step-by-step Getting Started and a Tutorial.
- Schematics for the entire circuit.

SAMPLES

Three UV erasable devices supplied:

- PIC17C42
- PIC16C71
- PIC16C55

SALES AND SUPPORT

To order or to obtain information, e.g., on the pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

PART NUMBER	DESCRIPTION
DM163001	LOW-COST DEMONSTRATION BOARD FOR PIC16C5X, PIC16C71, PIC16C84 AND PIC17C42

MICROCHIP MPASM Universal Assembler

Universal PIC16/17 Microcontroller Assembler Software

This product brief describes the technical aspects of the PIC16/17 Assembler developed by Byte Craft Limited and distributed by Microchip Technology. The MPASM Cross Assembler is a PC hosted symbolic assembler. It supports all microcontroller series, including the PIC16C5X, PIC16CXX and PIC17CXX families.

MPASM offers fully featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from the Microchip Universal Emulator System (PICMASTER).

MPASM REQUIREMENTS

MPASM will run on any IBM PC/XT®, AT® or compatible computer running DOS 4.1 or later. The distribution media is 3 1/2", low density (720K) floppies. It is distributed at the root level, and may be executed directly from the floppy.

No special display or ancillary devices are required.

MPASM ASSEMBLER FEATURES

MPASM supports the 12-bit PIC16C5X, the 14-bit PIC16CXX, and the 16-bit PIC17CXX cores.

All instructions are single-word and single-cycle, except for branches, which execute in two cycles. Most instructions operate on one or more operands.

MPASM have the following features to assist in developing software for specific user applications:

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro Assembly Capability
- Provides Object, Listing, Symbol and special files required for debugging with one of the Microchip Emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.
- Output formats: INHX8S, INHX8M, INHX32 and relocatable objects.

MPASM DIRECTIVE LANGUAGE

MPASM provides a full featured directive language represented by four basic classes of directives:

- **Data Directives** are those that control the allocation of memory and provide a way to refer to data items symbolically, by meaningful names.
- **Listing Directives** control the MPASM listing display. They allow the specification of titles and subtitles, page ejects and other listing control.
- **Control Directives** permit sections of conditionally assembled code.
- **Macro Directives** control the execution and data allocation within macro body definitions.

MPASM INSTRUCTION SET

MPASM supports the entire instruction set of the PIC16C5X, PIC16CXX and PIC17CXX microcontrollers, as represented in the following four classes of instructions:

- Data Move Operations
- Arithmetic and Logical Operations
- Bit Manipulation Operations
- Special Control Operations

The Microchip microcontroller set is used to operate on data located in any of the file registers, including the I/O registers. There are:

- Data Transfer Operations
- Logical Operations
- Rotate Operations

MPASM provides bit level file register operations to manipulate and test individual bits in any addressable register, literal and control operations permitting operations on literals and branches to subroutines in program memory.

The Microchip microcontroller instruction sets allow read and write of special function registers such as the PC and status registers.

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MPLINK

MPLINK supports the linking of multiple relocatable objects created by MPASM into a single absolute hex file, suitable for simulating, emulating, and programming. MPLINK supports the hex outputs supported by MPASM and absolute listing file.

MPLIB

MPLIB provides the ability to group several relocatable objects into a logical collection, in one file. Libraries created by MPLIB can be referenced by MPASM. Only those objects required by the linking phase are included in the resulting hex output.

MICROCHIP MPALC Cross Assembler

PIC16CXX Microcontroller Cross Assembler Software

This product brief describes the technical aspects of the Microchip Assembler (MPALC) developed by Microchip Technology Incorporated.

The MPALC Cross Assembler is a PC hosted symbolic assembler. It supports the PIC16C5X and PIC16CXX microcontroller series.

MPALC offers fully featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPALC REQUIREMENTS

MPALC will run on any IBM PC/XT®, AT® or compatible computer, running DOS 3.31 or later. The distribution media is 3 1/2", low density (720k) floppies. It is distributed at the root level, and may be executed directly from the floppy.

No special display or ancillary devices are required.

MPALC ASSEMBLER FEATURES

MPALC supports the 12-bit PIC16C5X and the 14-bit PIC16CXX cores. The 12-bit core has 33 instructions, the 14-bit core has 35.

All instructions in both instruction sets are single-word and single-cycle, except for branches, which execute in two cycles. Most instructions operate on one or more operands.

MPALC has the following features to assist in developingsoftware for specific user applications:

- Provides translation of Assembler source code to object code for PIC16C5X and PIC16CXX Microchip micro-controllers.
- Macro Assembly capability
- Provides Object, Listing, Symbol and special files required for debugging with one of the Microchip Emulator systems.
- Output formats: INHX8S, INHX8M and INHX16.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPALC DIRECTIVE LANGUAGE

MPALC provides a full-featured directive language represented by the following four classes of directives:

- **Data Directives** are those that control the allocation of memory and provide a way to refer to data items symbolically, by meaningful names.
- **Listing Directives** control the MPALC listing format. They allow the specification of titles, subtitles, page ejects and other listing controls.
- **Control Directives** permit sections of conditionally assembled code.
- **Macro Directives** control the execution and data allocation within macro body definitions.

MPALC INSTRUCTION SET

MPALC supports the entire instruction set of the PIC16C5X and PIC16CXX micro-controllers, as represented in the following four classes of instructions:

- Data Move Operations
- Arithmetic and Logical Operations
- Bit Manipulation Operations
- Control Operations

The Microchip microcontroller instruction set is used to operate on data located in any of the file registers, including the I/O registers. There are:

- Two data transfer operations
- Six arithmetic operations (the PIC16CXX series provides two more).
- Six logical operations
- Three rotate operation

MPALC provides bit level file register operations to manipulate and test individual bits in any addressable register, literal and control operations permitting operations on literals and branches to subroutines in program memory.

The PIC16C5X and PIC16CXX instruction sets allow read and write of special function registers such as the PC and status registers.

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NOTES:

MICROCHIP

MPSIM Simulator

PIC16C5X and PIC16CXX Microcontroller Simulator

MPSIM is a discrete event simulator software application designed to imitate operation of the PIC16C5X and PIC16CXX microcontrollers. It allows the user to debug software that will use any of these microcontrollers.

At any instruction boundary, you may examine and/or modify any data area within the processor, or provide external stimulus to any of the pins. MPSIM gives you a solid, low cost, source-level debug tool to help you through the early design verification stages of you project.

MPSIM REQUIREMENTS

MPSIM requires an IBM PC/XT®, AT® or compatible computer running DOS version 3.31 or later. The PC needs a 3 1/2" floppy disk drive and at least 256K of main memory; MPSIM.EXE occupies roughly 150K. Recommended is a hard disk drive with 5 Mb of available storage.

MPSIM SIMULATOR

The MPSIM Simulator program provides the developer with an instruction and limited I/O simulator software program for debugging Microchip microcontroller assembler code.

The simulator is meant for use with smaller projects not requiring precise, more extensive development equipment. Since the PIC16C5X architecture is essentially a single tasking microcontroller without interrupts, many applications can be developed by using a simulator program alone.

The PIC16CXX family supports various peripherals and interrupt strategies. These interrupts can be simulated but certain peripheral functions (such as A/D conversions) are not.

The MPSIM Simulator has the following features to assist in the debugging of software / firmware for the user:

Program Load / Save

Commands exist to load assembled object file programs into simulation memory. Conversely, programs may be saved from program simulation memory back to the PC disk.

Display and Alter

Provisions are made to display and alter Program Memory, Register Files and status register bits. Also, simulator information such as cycle times, elapsed time, and step count can be displayed.

Disassembler

Program memory can be disassembled showing both hexadecimal data and instruction mnemonics for specified address ranges.

Utility Functions

Various utility functions exist which assist the user in operating the simulator. Memory and registers can be cleared by command. Memory can be searched to find occurrences of instructions, register use and ASCII data.

Symbolic Debugging

The simulator provides for symbolic referencing to aid and simplify debugging. The symbol table may be displayed. New symbols defined and unwanted symbols deleted.

Execution and Trace

During program execution, a number of items can be traced. Address ranges, registers and register contents and others.

Breakpoints

The user may specify up to 512 breakpoints at any one time.

Assembler Support

MPSIM supports both the Microchip MPALC and the MPASM Universal Assembler.

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NOTES:

MP-C Code Development System

MP-C CODE DEVELOPMENT SYSTEM FOR PIC16/17

This product brief describes the technical aspects of the **MP-C** Code Development System for PIC16/17 microcontrollers developed by Byte Craft Limited.

The **MP-C** Code Development System is a complete 'C' compiler and integrated development environment for Microchip's PIC16/17 family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the PICMASTER Universal Emulator memory display (emulator software versions 1.13 and later).

MP-C is fast and efficient. You can quickly produce stand-alone single-chip microcontroller applications. These, taken with its other advantages make the Byte Craft **MP-C** Code Development System the first choice in intelligent compiler technology.

MP-C Requirements

The compiler will run on any IBM PC®, PC/XT®, PC/AT® or compatible computer, running DOS 4.1 or later. The distribution media is $3\frac{1}{2}$", low density (720k) floppies. It may be executed directly from the floppy, or copied to your hard drive to execute more conveniently.

MP-C Code Development System Features

MP-C supports the 12-bit PIC16C5X, the 14-bit PIC16CXX, and 16-bit PIC17CXX cores. It is a rule-based compiler with expert systems tailored for each of these platforms for optimal efficiency.

The compiler generates executable code directly from the compile process. There is no need for an extra step to assemble code generated by the compiler.

MP-C has the following features to assist in developing PIC16/17 software for specific user applications:

- Provides Object, Listing, Symbol and special files required for debugging with other Microchip Development systems.
- Supports interrupt routines
- Checks source against target hardware definitions
- Generates efficient, tight object code
- Includes a linker and built-in macro assembler
- 'C' enhancements specific to the PIC16/17 families' instruction sets
- Output formats: INHX8S, INHX8M, and INHX32.

MP-C Microprocessor Specific Extensions

The **MP-C** Code Development System includes common 'C' enhancements such as ROM arrays, binary constants and case statements together with functions specific to the PIC16/17 architecture.

- **Binary Constants** of the form *0b01011110* which are logical extensions to the conventional *0x1a3b* style of hexadecimal constants. You may also use *0B* as leading characters.
- **Case Statements** are supported well by the PIC16/17 instruction set and the compiler provides a superset of the standard 'C' case statement. For example, *case 4,5:*, *case '0'..'9'*, and complex case statements are allowed.
- **Processor Specific Functions** that are specific to the PIC16/17 family. For example *NOP()* and *SLEEP()* produce the equivalent PIC16/17 instruction.
- **"At" or @ Extension** allows you to fix a variable to a specific address in memory, for example: *int N @ 0x0C.*

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SALES AND SUPPORT

The **MP-C** Code Development System is supplied and supported directly by Byte Craft Limited of Waterloo, Ontario.

If you have any questions please contact their technical support personnel at **(519)888-6911**, or fax your questions to **(519)746-6751**.

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NOTES:

MICROCHIP

*fuzzy*TECH®/MCU-MP

*fuzzy*TECH/MCU-MP for PIC16/17

*fuzzy*TECH/MCU-MP EDITION FOR MICROCHIP PIC16/17

This product brief describes the technical aspects of the *fuzzy*TECH-MP Fuzzy Logic Development System for PIC16/17 microcontrollers developed by INFORM™ Software Corporation specifically for Microchip Technology.

The *fuzzy*TECH-MP Development System comes in two versions. The first, the Explorer edition, contains everything you need for a comprehensive working knowledge about fuzzy-logic system design. It is easy-to-use, all graphic editors and tools guide you step-by-step through the development phases of fuzzy systems. The Explorer edition supports two input variables and one output variable.

The full featured version offers all of the capabilities of the Explorer edition, *plus* it has the additional flexibility of eight input variables and four output variables for designing more complex systems. The full features are enabled with a parallel key lock.

Both systems generate assembly code compatible with the MPASM, Microchip's Universal Assembler, that can be integrated into your application. Examining this code provides you with further insights into the fabrics of fuzzy logic systems.

*fuzzy*TECH-MP System Requirements

*fuzzy*TECH-MP will run on any IBM PC® (386 or higher) or compatible computer, running DOS 4.1 or later, and MS-Windows® 3.0 or later. Because *fuzzy*TECH-MP makes extensive use of graphics, a color graphic monitor (VGA) is required, and higher resolutions of 800 x 600 or 1024 x 768 are recommended.

What is Fuzzy Logic?

Fuzzy logic is a technology that enhances mode-based system designs using both intuition and engineering heuristics. Fuzzy logic uses elements of everyday language to represent desired system behavior, thus circumventing the need for rigorous mathematical modeling.

It is an efficient way of designing, optimizing and maintaining highly complex systems transparently.

Fuzzy Logic Applications

Fuzzy logic finds its home in unique applications:

- When no adequate mathematical model for a given problem is readily apparent.
- When non-linearities, time constraints or multiple parameters exist.
- When engineering know-how about the given problem is available or can be acquired during the design process.

The *fuzzy*TECH-MP Implementation

*fuzzy*TECH-MP provides the following standard features:

- Windows Compatible with full graphical user interface
- 8-Input variables (2 for the Explorer version)
- 4-Output variables (1 for the Explorer version)
- 8-Bit resolution on input and output variables
- 16-Bit computation resolution for the PIC16CXX and PIC17CXX microcontrollers
- No theoretical limit on rules, antecedents and linguistic conjunctions (chip limitations will place a practical limit on these)
- MAX-MIN and MAX-DOT inference methods
- CoM and MoM defuzzification methods
- MPASM Compatible
- PICMASTER Compatible

*fuzzy*TECH-MP

*fuzzy*TECH-MP is available directly from Microchip Technology and its authorized distributors. Contact your local sales office for more information.

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IBM-PC is a registered trademark of IBM Corporation.
Windows is a registered trademark of Microsoft Corporation.

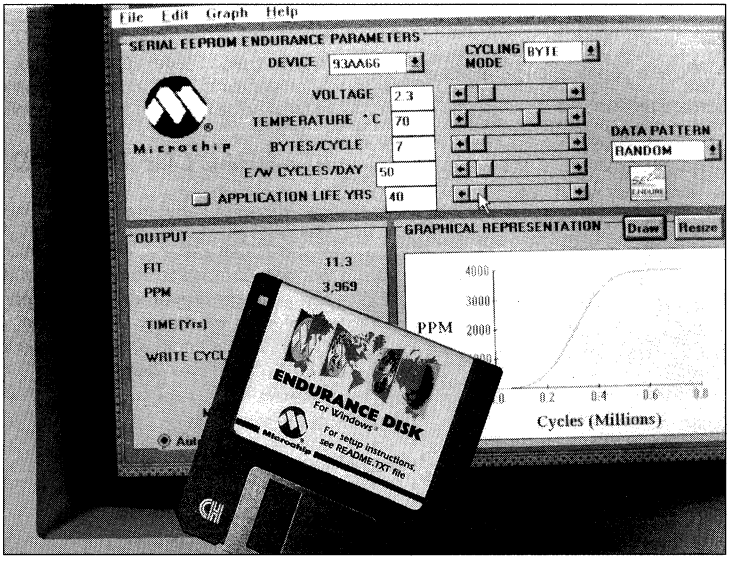
SALES AND SUPPORT

To order or to obtain information, e.g., on the pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

PART NUMBER	DESCRIPTION
SW005003	FUZZY TECH-MP EXPLORER
SW005004	FUZZY TECH-MP FULL FEATURED

MICROCHIP TOTAL ENDURANCE™

Serial EEPROM Endurance Model



FEATURES

- IBM® PC compatibility
- Windows® 3.1 or DOS 3.1 compatibility
- Automatic or manual recalculation
- Real-time update of data
- Full-screen or windowed graphical view
- Hypertext on-screen help
- Key or slide-bar entry of parameters
- On-screen editing of parameters
- Single-click copy of plot to clipboard
- Numeric export to delimited text file
- On-disk Endurance Tutorial

SYSTEM REQUIREMENTS

- DOS 3.1 or higher
- Windows 3.1
- 1MB memory
- '386 or '486 processor recommended
- Math coprocessor recommended

DEVICE SUPPORT

- Microchip 2-wire 24CXX/24LCXXB/85CXX
- Microchip 3-WIRE 93CXX/93LCXX Series
- Microchip 4-wire 59C11

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Total Endurance is a trademark of Microchip Technology Inc.
IBM PC is a registered trademark of IBM Corp.
Windows is a registered trademark of Microsoft Corp.

DESCRIPTION

Microchip's revolutionary Total Endurance disk provides electronic systems designers with unprecedented visibility into Serial EEPROM-based applications. This advanced software model (with a very friendly user interface) eliminates time and guesswork from Serial EEPROM-based designs by accurately predicting the device's performance and reliability within a user-defined application environment. Design trade-off analysis which formerly consumed days or weeks can now be performed in minutes, with a level of accuracy that delivers a truly robust design.

Users may input the following application parameters:

- Serial EEPROM device type
- Bytes to be written per cycle
- Cycling mode - byte or page
- Data pattern type - random or worst-case
- Temperature in °C
- Erase/Write cycles per day
- Application lifetime or target PPM level

The model will respond with FIT rate, PPM level, application life and a plot of the PPM level vs. number of cycles. The model is available in both DOS and Windows versions.

BACKGROUND

Microchip's research into the Erase/Write endurance of Serial EEPROMs has resulted in the conclusion that endurance depends upon three primary effects: the physical properties of the EEPROM cell, the internal error-correction technology employed, and the application environment. EEPROM endurance specified as a "typical" value in device data sheets must therefore be evaluated on a case-by-case basis, taking into account the manner in which the device will be used in the application. The Microchip Total Endurance software applies the user-defined application parameters to a complex mathematical model in order to emulate the EEPROM's performance and reliability in the system.

USING OF THE MODEL

The user has simply to choose a Microchip serial EEPROM device from the device-list menu and begin entering the application parameters. The entire process can take literally seconds to complete, and the model will output the PPM level and FIT rate of the device vs. the number of Erase/Write cycles. If the user has specified an application lifetime, the model will output PPM and FIT rates at that point in time. Alternately, the user may input a desired PPM level and the model will calculate the application lifetime which will result in that survival rate. The user may then trade-off any of the parameters (device type, voltage, application life, temperature, # of bytes per cycle, # of cycles per day etc.) to arrive at an optimal solution for the intended application.

ACCURACY OF THE MODEL

The accuracy of the Microchip Total Endurance model has been verified against test data to within ten percent of the actual values. However, Microchip makes no warranty as to its accuracy or applicability of the information to any given application. It is intended to be used as a guide to aid designers of Serial EEPROM-based systems in performing trade-off analysis and developing robust and reliable designs.

SECTION 10
QUALITY AND RELIABILITY

MICROCHIP

Product Quality

A CORPORATE COMMITMENT

Microchip Technology Inc. has evolved a culture where a commitment to quality is an integral part. By empowering every employee to be responsible for the quality of their work, the entire corporation is involved in the quality process. This interaction creates an environment for continuous improvement throughout the organization. The benefits of the system are then not only enhanced product quality and reliability but also product services.

THE CHALLENGE OF COMPLEXITY

Integrating an Ideal

Microchip's quality programs and business plan are vertically integrated and touch all levels of the company. From the top down, the President and CEO actively leads programs to ensure continuous improvement is a perpetual process. Improvement and cross functional teams work to enhance performance at every department level. Incorporating the improvement objectives into the business plan creates a unity of purpose and mandates that the two merge as one measurement.

Determination to be the Best

A fundamental concept at Microchip is the commitment to continuous improvement. All areas are constantly looking for ways to improve every aspect of the company. This has allowed products and processes to become world class in quality and reliability. These programs are the foundation for success.

PROCESS TECHNOLOGY

All the products manufactured at Microchip make use of a common N-Well CMOS baseline process to which modules are added in order to create the specific functions required by the product (EEPROM, Microcontroller, Logic and EPROM).

The baseline process, which has been in Manufacturing for the last 8 years, uses minimum dimensions of 1.5µm, 360Å gate oxide thickness, N^+ doped polysilicon gates and arsenic implanted source-drain diffusions for the N-channel devices.

A more advanced process uses minimum dimensions of 1µm, 250Å gate oxide thickness, polycide gate and LDD junction for the N-channel devices. A double level metal modules can be added to both processes.

All of these devices utilize a proprietary passivation suitable for a wide variety of package types. Microchip's processes have been developed with reliability and manufacturability as their primary goals.

EEPROM

Microchip's CMOS floating gate EEPROM technology produces a non-volatile memory cell by storing or removing charge from the floating gate. Charge is transferred bidirectionally to the floating gate by Fowler-Nordheim tunneling through a sub-10 nm oxide over the drain of the transistor. This technology produces a memory cell with a typical endurance of > 10^6 cycles and greater than 10 years of data retention. (See EEPROM application note for details).

EPROM

This technology uses a non-volatile memory cell which stores charge on a self aligned floating gate. Electrons are provided to the floating gate via hot electron injection from the drain depletion region. Each byte can typically be programmed in 100 microseconds, and can retain that data for more than 10 years with unlimited reads. Block erasing is accomplished with a high intensity UV source through the package window. Windowed parts can be erased and reprogrammed more than 100 times.

Microcontroller and Logic

Logic products are built on a variety of Microchip's processes and their derivatives. These products have process modules for production of controllers that feature ROM, Analog, EPROM, and EEPROM. By utilizing the standard processing modules, the designs meld these technologies and their flexibility while maintaining the high quality and reliability standards expected.

QUALITY

Design for Quality and Reliability

Product reliability is designed into all Microchip processes and products. Design margins are established to guarantee every product can be produced economically, error-free and within the tolerances of the manufacturing process. Product Introduction Teams representing manufacturing, engineering, quality and product divisions ensure that exacting standards are met for each specific product.

Documentation and Procurement Specifications

Microchip's documentation control program assures the correct and current document always is available at the point of use. Active documents are revision coded and serialized. Procurement specifications bear the same requirements. These document control procedures, which are common in the industry for military and high reliability products, are employed by Microchip, system wide.

In Line Controls and Process Assessment

Product integrity is assured by sampling and inspection plans performed in line. This enables Microchip to control and improve product quality levels as product moves through the manufacturing operation. Microchip's acceptance sampling plans in assembly emphasize the attempt to eliminate defective product as it is discovered. Acceptance and sampling plans are based on proprietary low fraction defective (<1000ppm) quality statistics.

To determine whether a process is within normal manufacturing variation, statistical techniques are put to work at selected process steps. In-process controls are performed by operators in the wafer fabrication and assembly operations. Operators take immediate corrective action if a process step is out of its control limit. Through these in-line controls the true capability of a process is generated. (See Appendix A - Controls)

Control of Customer Quality is attained through a statistical program based on minimum defect capability levels. These levels are defined as the error levels associated with the circuit design and science limitations of the chemistry and physics of processing.

Material controls prevent defective piece parts from getting into the line. Microchip's assembly material control sample plan is typical of the emphasis placed on safeguards. (See Appendix B - Material Controls).

Testing for Margin

Microchip conducts a product's initial test under stringent requirements. All quality assurance tests are run to tighter limits than customer specifications. As part of an outgoing quality assurance program, products are tested at least two machine tolerances tighter than those limits specified by the customer on every parameter. Margin testing accounts for normal tolerances of any particular test system and provides the assurance that Microchip's products meet a customer's specifications.

Variation from Expectation

Microchip works to make variation from target as small as possible. The better process is the one that holds the narrowest dispersion. Processes are targeted to maintain Cpk's of >1.5 and currently have typical values of >2.0. Higher process capability values are continually strived for indicating that better process control is being obtained.

Outgoing Quality

Quality Control samples all outgoing product from final testing. These samples measure in line defect levels after screens have been applied. Root cause analysis follows, initiating technical change to effect continuous improvement.

Programmability Yield

Using programmable devices adds a complexity to the Quality Level interpretation. It is not unlikely that some programmable devices will not program. The programmability yield is dependent on (but not limited to): programmers, technology, array size, and handling.

Any device that does not program properly will not be used in the end system. Therefore, programmability yields should not be used to calculate AQLs.

For convenience, Microchip offers programming services for certain devices. This service is an advantage to the customer since it not only eliminates programmability rejects, but also reduces the handling of the parts. See the individual data sheets for details on our Quick-Turnaround-Production (QTP) service.

RELIABILITY

Process Qualification

No priority is more important than the one where processes under which Microchip products are built operate without fail. All products are stressed beyond normal use limits when undergoing high temperature operating life and retention bake tests. This is done to ensure that the devices meet the strictest reliability guidelines and will maintain industry low failure rates.

Package Qualification

Package qualification measures a component's ability to withstand extreme thermal and mechanical stresses. All products are stressed to high level industrial specifications to ensure reliability.

Ongoing Sampling of Key Reliability Variables

Microchip conducts accelerated mechanical tests, operating life tests and memory retention tests to explore the many ways failures might occur. Data obtained from continuous testing is used to identify potential reliability problems and for defining action courses to improve product. Microchip's reliability knowledge is shared with customers. This data is available for use in customer's own quality and reliability improvement programs and is published in regular quarterly and yearly reports.

RELIABILITY CONCEPTS

Definition

Reliability is the probability of a system or circuit performing its predefined function adequately under specific conditions for a given period of time. Thus, the reliability of a microcircuit is a function of both stress conditions and the time of operation.

The reliability (or probability of survival) range runs from 0 (no chance of survival) to 1 (no chance of failure). Current microelectronic circuits are manufactured and controlled to such tight specifications that reliability figures for the total operation time approaching 1 (i.e., 0.9999) are common. As a result, the complement of reliability, or the failure probability, is more often quoted in current literature.

The failure rate is the rate at which failures occur on units surviving to a specific number of hours of operation. Failure rates per unit circuit-hour would generally be very small. To avoid reporting such small numbers, failure rates have been defined for greater circuit-hours. One thousand circuit-hours is defined as one circuit operating for one thousand hours, or 1,000 circuits operating for 1 hour, etc. The numbers of circuit-hours is the number of circuits multiplied by the number of operation hours for each circuit.

Two methods to define failure rate are commonly used:

- Percent failures per thousand circuit-hours
- Absolute failures per 10^9 circuit-hours, or FITs.

Note that a failure rate of 0.0001%/1000 hours and 1 FIT are equivalent numbers.

Bathtub Curve: Failure Rate Over Time

The generic representational graph of failure rate vs. time takes the shape of a bathtub curve. (Figure 1).

The early failure rate (infant mortality) period starts from initial operation (time T_0) and decreases as time goes on.

Time T_1 signifies the end of the infant mortality period. The next phase of the curve occurs between time T_1 and T_2. This long period of time is distinguished by a nearly constant and very low failure rate. After T_2 is passed, the failure rate starts to increase slowly. This last phase of failure rate vs. time is known as the wear-out period.

Temperature Dependency

In order to establish failure rates in a reasonable time, it is necessary to accelerate the incidence of the failure modes. Higher environmental stress levels than those encountered under normal conditions are needed. The accelerating parameter most employed is junction temperature, although voltage and humidity, for example, are also used. Higher temperatures are capable of accelerating many common failure modes dramatically.

Arrhenius Equation

A number of mathematical models were developed to quantify the relationship between accelerated failure rates and increased junction temperatures. The one model most commonly used employs the Arrhenius Equation. It is as follows:

$$AF = e^x, \text{ where } x = \frac{E_A}{K}\left[\frac{1}{T_N} - \frac{1}{T_A}\right]$$

AF = Acceleration Factor (non-dimensional)

e = 2.718281828 ... (non-dimensional constant)

E_A = Activation energy level (electron volts)

k = Boltzmann's constant = 8.6172×10^{-5} (electron-volts/degree Kelvin)

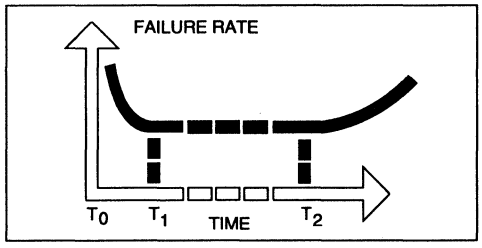
T_N = Normal junction temperature (degrees Kelvin)

T_A = Accelerated junction temperature (degrees Kelvin)

Thus, the time to achieve a certain probability of failure at time T_1 under temperature T_N can be compressed to T_1 divided by AF at the accelerated temperature, T_A. Note that for true acceleration, the acceleration factor AF is independent of the probability of the fail point specified.

AF, the dependent variable of the Arrhenius Equation is a function of several variables. T_N and T_A are specified for the situation under consideration. E_A is a function of the particular mode of failure, and is determined by experimental evaluation.

FIGURE 1: BATHTUB CURVE



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Activation Energy Level

Activation energy levels in semiconductors generally are in the 0.3 - 1.1 electron-volt range. Each failure mode has its own activation energy. Some typical examples are:

FAILURE MECHANISM	E_A (eV)
Oxide/Dielectric Breakdown	0.3
Electromigration	0.5 to 0.7
Surface Related Contamination	1.0
Intermetalics	1.0
Floating Gate Charge Loss	0.6
Hot Electron Trapping	-.1
Charge Trapping	0.12

A compromise value of 0.6 electron-volts is often used when there is no specific information relating to the failure modes being accelerated.

RELIABILITY TESTS

Operating Life Test

The Operating Life Test is run under dynamic bias conditions where inputs are clocked. The test is conducted at high temperature to accelerate the failure mechanisms. The normal temperature for the test is +125°C for 1,000 hours. Readouts occur at 24, 168, 500 and 1,000 hours. Early hour failures are usually associated with manufacturing defects or otherwise marginal material.

Retention Bake

The Retention Bake Test is performed to accelerate data loss on floating gate devices. The test consists of unbiased baking at elevated temperature. Usually the test lasts for 1,000 hours at +150°C. The failure mechanism that is accelerated is charge leakage from a stored element.

Endurance Cycling

Endurance Cycling establishes the number of times a device can be programmed and erased. Normally the test is conducted at rated temperature conditions and is followed by retention bake. The standard cycling at Microchip is done at 85°C using a byte cycle mode and is followed by a bake of both a checkerboard and an inverse checkerboard of 48 hours at 150°C.

Temperature Cycle

The Temperature Cycle test simulates stresses which occur to systems during power up/power down sequences. The test is intended to reveal any deficiencies resulting from thermal expansion mismatch of the die/package structure. Normally the test is conducted by cycling between -65°C and +150°C in an air ambient. Duration for the test is typically 500 cycles for both plastic and ceramic packages. Endpoint criteria are both electrical and visual/mechanical.

Thermal Shock

The Thermal Shock test is similar to the Temperature Cycle test except that the ambient during cycling is liquid-to-liquid. This stimulates rapid thermal environmental changes. The mechanisms accelerated are identical to those in the Temperature Cycle test except that the Thermal Shock test is a more accelerated test with temperatures normally +125°C to -55°C. The number of cycles are 500 for qualification testing.

Autoclave

The autoclave test determines the survivability of devices in molded plastic packages to a hot, humid environment. The test exposes unbiased, plastic packaged devices to saturated steam at 121°C and 15 pounds per square inch (one atmosphere) gauge pressure. The 168 or more hours of testing allows moisture to penetrate into the die. Chemical corrosion of the die metallization may occur if ionic contaminants are present and the die surface protection is deficient or damaged. Charge leaks from floating devices usually happen before a corrosion mechanism develops.

RELIABILITY TESTS (CONT.)

Temperature Humidity Test

The Temperature Humidity test determines the survivability of devices in molded plastic packages functioning in a hot, humid environment. By convention, test conditions are 85°C with 85% relative humidity. The parts are biased to lend themselves to electrochemical corrosion. The duration of the test is usually 1,000 hours or more. The test checks the adequacy of the die surface protection and the plastic's lack of ionic impurities. The applied bias is 5 volts on alternating pins or set up for minimum power to reduce internal heating and consequent moisture evaporation on the device. Similar to the Autoclave test, charge loss on floating gate devices is a principle failure mechanism.

HAST

The Highly Accelerated Stress Test is similar to the Temperature Humidity Test but with more stringent temperature exposure. Devices are subjected to 130°C with 85% relative humidity and an alternating bias of 5 volts and ground on device pins. The duration of the test is 168 hours. This tests for ionic contamination and corrosion, but floating gate devices may also fail for charge loss.

QUALIFICATION CATEGORIES

In general, qualification is required for new design, major changes in old design, process or material when either wafer fabrication or package assembly operations are affected. Cross functional teams which include reliability develop new products for introduction. In other areas, Microchip utilizes the concept of a Change Control Board which meets regularly to establish which criteria is to be used for all specific proposed changes. This board is made up of representative leaders of various groups and departments throughout Microchip to insure all concerns are heard early during the process.

QUALIFICATION PROGRAMS

Qualifications guarantee changes to or new processes and technologies are properly evaluated for reliability performance.

Reliability Monitoring

Microchip's reliability monitoring program is a comprehensive effort to measure the reliability of all process families with strict regularity. The program strives to improve performance through failure analysis and corrective action. Numerous screening procedures are used and estimates of product life and expected failure rates are provided.

Typical tests and frequencies include:

- Die Monitor on selected product for -
  - Dynamic Life
  - Retention Bake
  - Endurance
- Periodic (weekly, monthly and quarterly) package monitors to evaluate:
  - Mechanical stresses
  - Alignment
  - Temperature and moisture stresses
  - Corrosion resistance
  - Marking permanency

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APPENDIX A - IN LINE CONTROLS

CONTROLS - PLASTIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced
			Quality	Prod	MIL-STD
Die Visual	Reject defectives 100% rescreen per LTPD	10% sample LTPD 10	- X	X -	MIL-STD-883C Method 2010
Wafer Saw	Machine Shut Down	One kerf per lot	X	-	MIL-STD-883C Method 2010
Die Attach	Machine Shut Down	4X/Lot/Machine LTPD 15	X	-	N/A
Wire Bond	Machine Shut Down	1% AQL each 1/2 shift	X	-	MIL-STD-883C Method 2010
Post Wire Bond	Reject defectives 100% rescreen per LTPD	LTPD 15	X	-	MIL-STD-883C Method 2010
Mold Press	Machine Shut Down	One sample /4 hrs	X	-	N/A
Die Plating	Reject defectives 100% rescreen per LTPD	Every 4 hrs LTPD 10	X	-	N/A
Trim and Form	Reject defectives 100% rescreen per LTPD	Once/ 2 hrs LTPD 10	X	-	N/A
External Visual and Documentation Verification	Reject defectives 100% rescreen per LTPD	100% LTPD 2	- X	X -	MIL-STD-883C Method 2010, Method 2016

CONTROLS - CERAMIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced
			Quality	Prod	MIL-STD
Die Visual	Reject defectives 100% rescreen per LTPD	10% LTPD 10	- X	X -	MIL-STD-883C Method 2010
Wafer Saw	Machine Shut Down	One kerf per lot	X	-	MIL-STD-883C Method 2010
Die Attach	Machine Shut Down	Non-destruct each 2 hrs destruct each shift	X	-	MIL-STD-883C Method 2010
Wire Bond	Machine Shut Down	4X/shift/machine	X	-	MIL-STD-883C Method 2010
Preseal Visual	Reject defectives 100% rescreen per LTPD	100% LTPD 15	- X	X -	MIL-STD-883C Method 2010
Package Seal	Machine Shut Down	LTPD 15	X	-	N/A
Environmental Stress Centrifuge Temp Cycle	Machine Shut Down	LTPD 5 84(0) 84(0)	X	-	MIL-STD-883C Method 2001 Method 1010
Fine Leak	Reject defectives 100% rescreen per LTPD	LTPD 5	X	-	MIL-STD-883C Method 1014
Gross Leak	Reject defectives 100% rescreen per LTPD	LTPD 5	X	-	MIL-STD-883C Method 1014
Lead Trim	Reject defectives 100% rescreen per LTPD	100% LTPD 2	- X	X -	MIL-STD-883C Method 2009
External Visual and Documentation Verification	Reject defectives 100% rescreen per LTPD	100% LTPD 2	- X	X -	MIL-STD-883C Method 2010, Method 2016

APPENDIX B - MATERIAL CONTROLS PACKAGE

MATERIALS CONTROLS - PLASTIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced
			Quality	Prod	MIL-STD
Lead Frame	Reject defectives 100% rescreen per LTPD	Visual, LTPD 2 Functional, LTPD 10 and material spec	X	-	N/A
Die Attach Epoxy	Reject	Functional, LTPD 15 and material spec	X	-	N/A
Gold Wire	Reject	Per material spec	X	-	N/A
Molding Compound	Reject	Spiral flow, 3X/lot Functional, 1X/lot and material spec	X	-	N/A

MATERIALS CONTROLS - CERAMIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced
			Quality	Prod	MIL-STD
Base/Lead Frame	Reject 100% rescreen per LTPD	Visual, LTPD 10 Functional, LTPD 10 Bake test, LTPD 15 Dimensions, LTPD 50 and material spec	X	-	MIL-M-38510
Package	Reject 100% rescreen per LTPD	Visual, LTPD 10 Functional, LTPD 10 Bake test, LTPD 15 Dimensions, LTPD 50 Plating, LTPD 10 and material spec	X	-	MIL-M-38510
Preform	Reject	Visual, LTPD 10 Functional, LTPD 15	X	-	MIL-M-38510
Bond Wire	Reject	Per material spec 2 spools/lot	X	-	MIL-M-38510
Lid	Reject	Visual, LTPD 7 Functional, LTPD 10 and material spec	X	-	MIL-M-38510

MICROCHIP

Product Reliability

OVERVIEW

Microchip Technology Inc.'s products provide competitive leadership in quality and reliability, with demonstrated performance of less than 100 FITs (Failures in Time) operating life for most products. The designed-in reliability of Microchip's products are supported by ongoing reliability data monitors. This document presents current data for your use - to provide you with results you can count on.

The test descriptions included in this document explain Microchip's quality and reliability system. The product data demonstrates its results.

The customer's quality requirements are Microchip's top priority. Ongoing customer feedback and device performance monitoring drive Microchip, leading to continuing improvements in the long-term quality and reliability.

FAILURE RATE CALCULATION

Extended field life is simulated by using high ambient temperature. In the semiconductor technology, high temperatures dramatically accelerate the mechanisms leading to component failure. Using performance results at different temperatures, an activation energy is determined using the Arrhenius equation. For each type of failure mechanism, the activation energy expresses the degree to which temperature increases the failure rate.

The activation energy values determined by Microchip Technology agree closely with those published in the literature. For complex CMOS devices in production at Microchip Technology, an activation energy of 0.6 eV has been shown to be representative of typical failures on operating life. By definition, failure is reached when a device no longer meets the data sheet specifications as a direct result of the reliability test environment to which it was exposed. Common failure modes for CMOS integrated circuits are identified for each test environment.

To establish a field failure rate, the acceleration factor is applied to the device operating hours observed at high temperature stress and extrapolated to a failure rate at 55°C ambient temperature in still air.

The actual failure rate experienced could be considerably less than that calculated if lower device temperatures occur in the application board, such as would be the case if a fan, a heat sink, or air flow by convection is used.

Environment	Typical Failure Mechanism
Operating Life	Process parameter drift/shift Metal electromigration Internal leakage path Lifted bond/ball bond chip-out
Temperature Cycle	Lifted bond/ball chip-out Cracked die or surface cracks Bond pad corrosion
Biased-Humidity	Internal circuit corrosion
Autoclave	Inter-pin leakage Charge loss
High Temp. Bake	Charge loss
High Temp. Reverse Bias	Charge gain, Parameter drift/shift

DEFINITIONS

FIT (Failure In Time): Expresses the estimated field failure rate in number of failures per billion power-on device-hours. 100 FITS equals 0.01% fail per 1,000 device-hours.

Operating Life Test: The device is dynamically exercised at a high ambient temperature (usually 125°C) to quickly simulate field life. Derating from high temperature, an ambient use condition failure rate can be calculated.

Temperature Cycle: The devices are exposed to severe extremes of temperature in an alternating fashion (-65°C for 15 minutes, 150°C for 15 minutes per cycle). Package strength, bond quality and consistency of assembly process are stressed using this environment.

Biased-Humidity: Moisture and bias are used to accelerate corrosion-type failures in plastic packages. The conditions include 85°C ambient temperature with 85% relative humidity. Typical bias voltage is +5 volts and ground on alternating pins.

Autoclave (pressure cooker): Using a pressure of one atmosphere above atmospheric pressure, plastic packaged devices are exposed to moisture at 121°C. The pressure forces moisture permeation of the package and accelerates related failure mechanisms, if present, on the device.

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Thermal Shock: Exposes devices to extreme temperatures from -55°C to +125°C by alternate immersion in liquid media.

Retention Bake: A 150°C temperature stress is used to accelerate charge loss in the memory cell and measure the data retention on the EPROM and EEPROM portions of the circuitry.

HAST: Moisture, extreme heat and bias are used to accelerate corrosion and contamination in plastic packages. The conditions are 130°C and 85% relative humidity. Typical bias voltage is +5 Volts and ground on alternating pins.

RELIABILITY CONTROL SYSTEM

A comprehensive qualification system ensures that released products are designed, processed, packaged and tested to meet both design functionality and strict reliability objectives. Once qualified, a reliability monitor system ensures that wafer fabrication and assembly process performance is stable over time. A set of baseline specifications is maintained that states which changes require requalification. These process changes can only be made after successful demonstration of reliability performance. This system results in reliable field performance, while enabling the smooth phase-in of improved designs and product capability.

RELIABILITY DATA SUMMARY

Introduction

This section provides a reliability summary of Microchip Technology's product. Included is reliability data and packaging information obtained over the recent past.

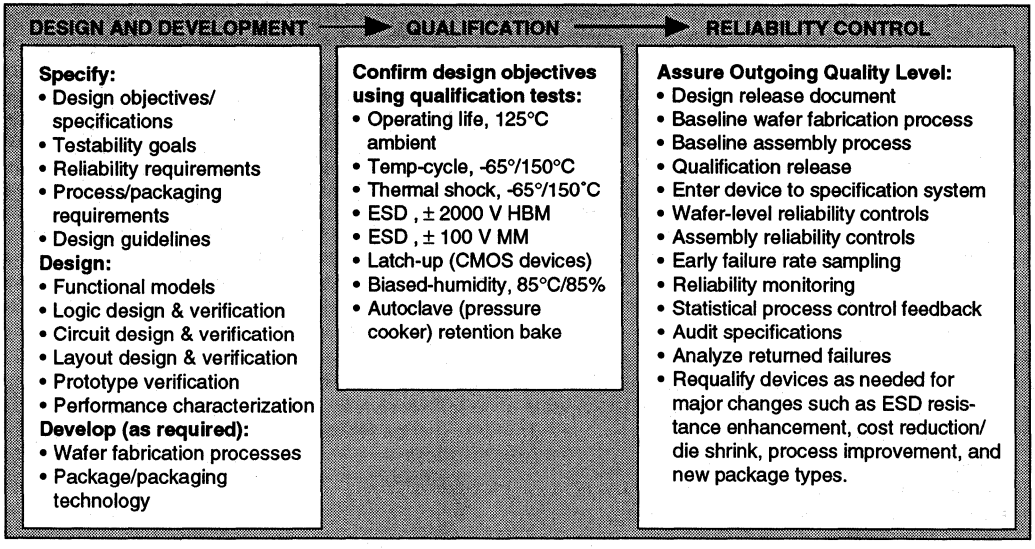
Plastic Package Characteristics and Codes

As part of an on going product program, Microchip Technology will apply its Quality and Reliability process in evaluating the latest developments in plastic packaging technology, and implement the highest reliability materials and assembly techniques. The plastic packages that are currently available from Microchip are listed in the table below.

Package Description Identification Code

Package Description	Identification Code
Plastic Leadless Chip Carrier	L
Plastic Dual In Line (600)	P
Plastic Dual In Line (300)	SP
Plastic SOIC (.150)	SL/SN
Plastic SOIC (.207)	SM
Plastic SOIC (.300)	SO
Plastic TSOP (8 x 20mm)	TS
Plastic SSOP (.207)	SS

RELIABILITY CONTROL SYSTEM DIAGRAM

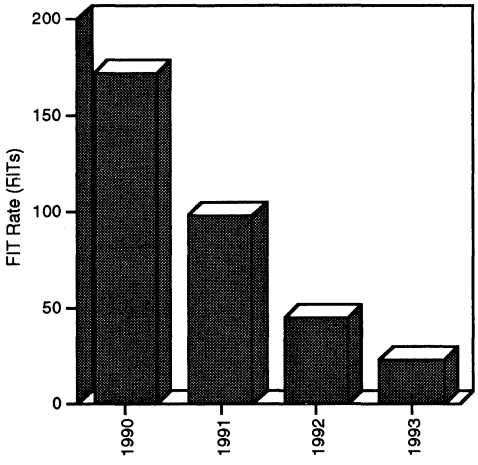


HIGH TEMPERATURE (125°C) DYNAMIC LIFE TEST

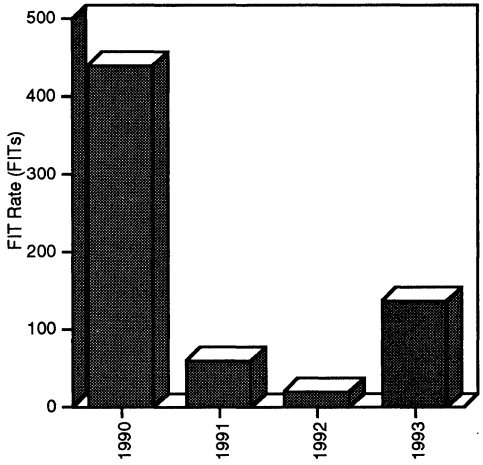
Graph set for EEPROM, PIC16/17 and EPROM for all conditions

High temperature dynamic life testing accelerates random failure modes which would occur in user applications. Voltage bias and address signals are used to exercise the device in a manner similar to user systems.

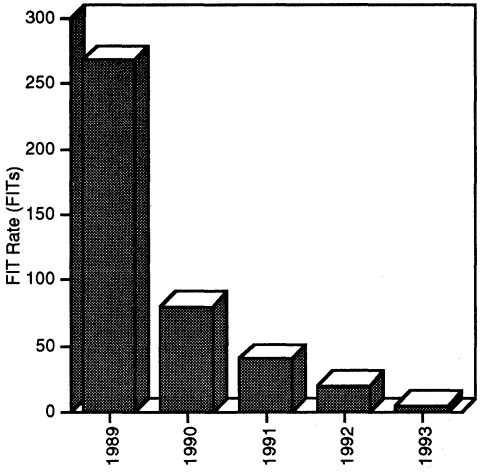
EEPROM DYNAMIC LIFE



EPROM DYNAMIC LIFE



PIC16/17 MICROCONTROLLER DYNAMIC LIFE



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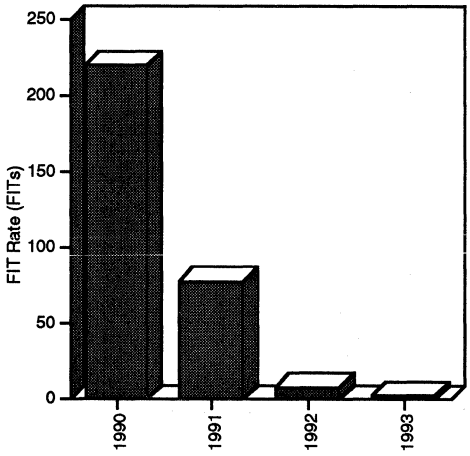
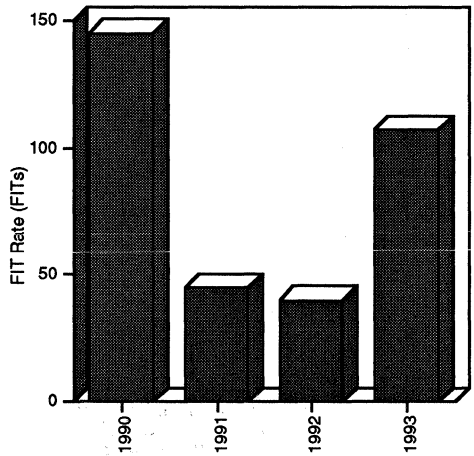
DATA RETENTION BAKE

Data storage in applicable devices is done by developing a charge on the floating gate structure in the memory cell. Charge loss in this cell structure results in a conversion of zeroes to ones. In order to evaluate the level of this type of failure, devices are subjected to a 150°C bake. This bake accelerates charge loss in the memory cell and 1000 hours at 150°C is equivalent to approximately 13.5 years in the field at 55°C.

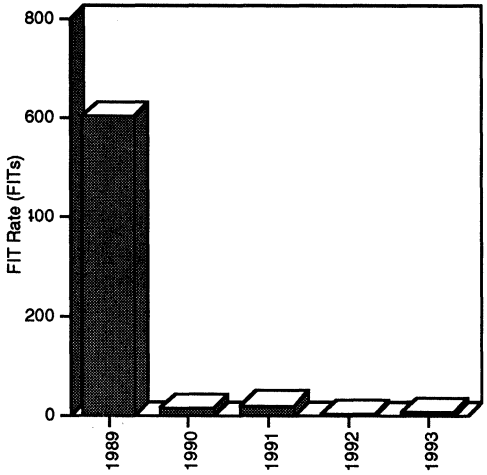
EEPROM RETENTION BAKE



EPROM RETENTION BAKE



PIC16/17 MICROCONTROLLER RETENTION BAKE



NOTE: Representation of reliability data typically shows calendar year grouping along the x-axis, except for 1993 which includes only first, second and third quarters. This provides the equal time interval normally expected for graphical presentation. However, Chi-square statistics demand equivalent device-hours for fair interval comparison. Such data grouping assures that relatively small sample sizes do not indicate unrepresentative FIT rates.

BIASED 85°/85% R.H.

Microchip Technology evaluates plastic encapsulated devices ability to withstand high temperature, high humidity environments while under electrical bias. This is done by utilizing the industry standard test method known as 85/85. This stress is designed to create corrosion of the metal or internal device leakage if ionic contaminants are present but also may cause charge loss in memory cells.

Operating Hours

package	24	168	504	1008
PDIP	0/3566	1/3566	1/3565	2/3564
PLCC	0/2447	3/2447	1/2444	5/2443
SOIC	0/2997	5/2997	0/2865	0/2865
TSOP	0/377	0/377	0/377	0/377

PCT (AUTOCLAVE)

Originally, this test was designed to evaluate corrosion of bond pads due to penetrating moisture combining with contaminant residue on the metal surface. The corrosion failure rate for this test has become nearly zero and a new failure mode has surfaced. This is memory cell charge loss due to moisture penetration along the floating gate allowing a conduction path for removal of stored charge. This moisture path is between the seal of the metal and the passivation which can then be traced to the substrate near the edge of the floating gate. This failure type is the primary mode in the data provided.

Operating Hours

package	24	168
PDIP	0/8147	4/8147
PLCC	0/3322	0/3322
SOIC	0/6464	7/6464
TSOP	0/142	1/142

TEMPERATURE CYCLING

This thermal tests evaluates air to air rapid temperature change evaluating built in material stresses. This is a worst case simulation of system power up/ power down and is based on stringent military packaging requirements.

Operating Results

package	15 cycles	500 cycles
PDIP	0/2054	3/2054
PLCC	0/907	1/907
SOIC	0/837	0/837
TSOP	0/96	0/96
SSOP	0/94	0/94

THERMAL SHOCK

Thermal shock is the most extreme case of temperature cycling by using liquid immersion for the technique to change the device environment. This accelerates any stress related failures with the rapidly changing gradient. After the temperature stressing a constant force centrifuge test is also preformed prior to final electrical testing to further uncover any defects that may have occurred under stress.

Operating Results

package	15 cycles	500 cycles
PDIP	0/2314	0/2314
PLCC	0/878	6/878
SOIC	0/1090	0/1090
TSOP	0/96	0/96
SSOP	0/94	0/94

HAST (130°/85% R.H.)

Highly Accelerated Stress Testing evaluates plastic encapsulated devices' ability to withstand extreme high temperature, high humidity environments while under electrical bias. This is done by a new method known as HAST. This stress is designed to create corrosion of the metal or internal device leakage if ionic contaminants are present but also may cause charge loss in memory cells.

Operating Results

package	24 hours	168 hours
PDIP	1/2192	0/809
PLCC	2/527	0/281
SOIC	0/976	0/488

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PRODUCT RELIABILITY DATA

CMOS PIC16/17								
		Operating Hours						
Device	Operation	24	168	504	1008	Fails	Device Hours	FITs 60% CL @ 55°C
PIC16C57	DLT	0/9350	2/9350	0/4400	0/4400	2	5,266,800	14
PIC16C56	DLT	0/6511	0/6511	0/2601	1/2601	1	3,278,688	15
PIC16C55	DLT	0/8066	1/8066	1/4256	1/4255	3	4,929,624	20
PIC16C54	DLT	1/11509	0/11508	3/6569	1/6566	5	7,449,816	20
PC16C84	DLT	0/607	0/607	0/555	0/555	0	568,176	39
PIC16C71	DLT	0/304	0/304	0/304	0/304	0	306,432	72
PIC16C57	BAKE	0/10308	0/10308	1/2218	0/2217	1	3,594,360	5
PIC16C56	BAKE	0/7888	2/7888	0/1615	0/1615	2	3,187,800	8
PIC16C55	BAKE	0/8959	0/8959	1/2633	1/2632	2	3,716,328	7
PIC16C54	BAKE	0/12690	0/12690	1/4024	0/4023	1	5,511,576	3
PIC16C84	BAKE	0/485	0/485	0/485	0/485	0	488,880	16
EEPROM								
		Operating Hours						
Device	Operation	24	168	504	1008	Fails	Device Hours	FITs 60% CL @ 55°C
24CXX	DLT	0/14842	0/14842	1/4360	3/4359	4	6,155,352	20
93CXX	DLT	2/5308	4/5306	0/1989	0/1989	6	2,562,216	68
24LCXX	DLT	0/9161	3/9161	2/6132	3/6130	8	6,688,920	34
93LCXX	DLT	0/3941	3/3941	3/1811	2/1808	8	2,181,816	103
28C16	DLT	0/1915	0/1915	0/765	0/765	0	964,320	23
28C64	DLT	1/4498	1/4497	0/2127	0/2127	2	2,542,200	29
24CXX	BAKE	2/12649	1/12647	1/2840	2/2839	6	4,510,008	14
93CXX	BAKE	0/5472	0/5472	0/1045	0/1045	0	1,797,096	4
24LCXX	BAKE	0/7778	0/7778	0/3484	1/3484	1	4,233,264	4
93LCXX	BAKE	0/4729	0/4729	0/2527	0/2527	0	2,917,152	3
28C16	BAKE	1/3248	1/3247	2/607	1/605	5	1,054,392	51
28C64	BAKE	0/3222	3/3222	1/859	1/858	5	1,262,352	42
EPROM								
		Operating Hours						
Device	Operation	24	168	504	1008	Fails	Device Hours	FITs 60% CL @ 55°C
27HC256	DLT	0/1933	1/1933	0/1013	0/1013	1	1,175,664	41
27C256	DLT	1/8517	4/8516	0/1569	0/1569	5	2,748,672	55
27C512	DLT	0/2815	4/2815	0/954	0/954	4	1,274,280	98
27HC256	BAKE	0/2192	5/2192	0/532	0/532	5	815,136	66
27C256	BAKE	2/8513	3/8510	0/2193	1/2193	6	3,271,872	19
27C512	BAKE	2/2406	13/2404	1/380	2/379	18	722,616	233

Operation Legend: DLT - Dynamic Life Test (125°C)
Bake - Retention Bake (150°C)

MICROCHIP

EEPROM Endurance

INTRODUCTION

A unique feature of non-volatile memory devices is the dual requirement both to change and to maintain data states. It is this combination of requirements that provides the contrasting nature that defines the complexities involved in change and maintaining such change. Anything that enhances the physics to allow a data state change in contrast degrades the retention of that change. It also holds that any retention enhancements inhibit the data changing capabilities. A balance must be struck between the combinations to achieve the field requirements of customer applications.

Erase/Write cycling has many variables which greatly effect the lifetime of the device. To accurately make comparisons between specifications and the actual requirements, or any other comparisons, these factors must be well understood and taken into account.

TECHNOLOGY OVERVIEW

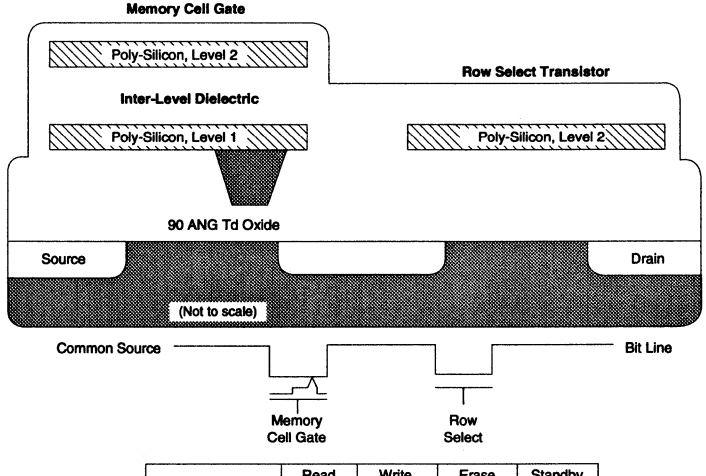
Silicon Technology

The basic technology employed by Microchip Technology for EEPROM's is a FLOTOX structure as drawn below. This is a an industry standard architecture base which has been enhanced by Microchip to provide improvements to the quality and reliability of the devices produced.

Circuit Technology

These cells are then structured in either an 8 or 16 bit word organization for data storage with between 32 words (256 byte device) and 8K words (64K device) using standard binary decoding schemes found industry wide on memory devices. Data can then be transmitted either into the device for storage or read from the device when needed along a single DATA pin. The device has no restriction on the number of read cycles that can be processed per byte without damage but the storage process does have finite limitations.

Currently two different schemes of error correction are being utilized on Microchip EEPROM's. The 24CXX, 93CXX, 85CXX, 59CXX and 28CXX device types utilize a modified Hamming code redundancy scheme with four parity bits per eight bit byte. This has been the industry standard correction scheme for enhancement of cycling lifetimes by eliminating single bit per word errors. An alternative approach has been developed utilizing an AND cell concept of redundant memory cells. This further enhances the write/erase lifetime over the Hamming code and has been implemented on the 24LCXXB and 93LCXX circuits.



	Read	Write	Erase	Standby
Bit Line	1.6 volts	18.0 volts	0.0 volts	0.0 volts
Row Select Gate	5.0 volts	20.0 volts	20.0 volts	0.0 volts
Memory Cell Gate	5.0 volts	0.0 volts	20.0 volts	0.0 volts
Common Source	0.0 volts	Float	0.0 volts	0.0 volts

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Reliability Endurance

The endurance failure rate curve for the Microchip devices is presented in the standard form for this curve from EEPROM FLOTOX manufacturers. Microchip does write/erase cycle all EEPROM devices prior to shipment to remove the infant mortality endurance failures from the population. This characteristic curve, with two failure increase sections, is shown below for reference. Both sections have single bits failing as the dominant mechanism.

The first of the failure increase sections is usually related to breakdown of oxides from latent oxide defects that are inherent to any process. These oxides have reached a time dependent dielectric breakdown condition and permanently rupture. This generally characterizes the first 200K write/erase cycles under any conditions. The second curve is the standard trap up of electrons within the tunnel dielectric which closes the write/erase threshold window until the device no longer adequately programs or erases.

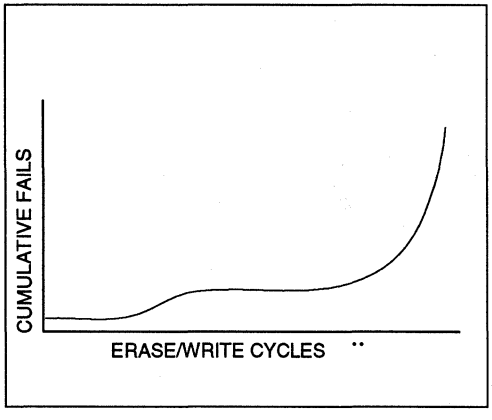
This curve depends on multiple parameters, but the trap up failure increase portion often does not occur until one million write/erase cycles or greater.

The first failures from endurance cycling and the long term end of life failures are due to different mechanisms.

The failures from 200K to 500K cycles have historically been attributed to "fast trap up" around the industry. Analysis at Microchip has shown that these failures are not actually trap up but oxide breakdown in nature. They most often manifest themselves as single bit charge loss or charge pump failure, both due to the formation of a conductive path within the gate oxide layer.

These oxide breakdown failures can be related to defects of three types of categories.

Type 1 is a residual chemical stain left behind on the wafer after processing due to an inadequate rinse. These are very difficult to physically detect and are best inferred from a pattern of bits (a bit cluster) that fail.



Type 2 is a physical defect which can be found upon microscopic or SEM analysis resulting in the failure. This is most often a particle, polysilicon nodule or metal short.

Type 3 is a physical defect with low activation energy that cannot be detected until end of life evaluation because of it's change in state (subsequent consumption) during latter processing steps.

The end of life mechanism is called "oxide trap up". This is where the tunnel dielectric oxide layer loses it's ability to pass charge and begins to retain some portion of the charge that it passes to the floating gate. These excess electrons within the oxide act as a charge shield, resulting in insufficient charge movement while significantly raising the voltage required to continue transmitting a constant charge level. Since the programming voltage is not adjustable this results in less charge movement for either the write or erase state. These states, whether charged negatively or charged positively, approach a central point and become indistinguishable to the detection circuitry of the device. This results in a failure to read the correct pattern, (impossible to distinguish between a programmed one and a programmed zero) beginning with the extreme voltage values of the operating specification.

MEASUREMENT OF CYCLING

Microchip Technology defines a device lifetime in the strictest sense, that is, stated lifetime has to exhibit the truest correlation to customer results. All units shipped from Microchip have Error Correction circuitry engaged for customer use. Error Correction amends any one error per byte for Hamming and one error per bit for AND cell which allows the device to read correct data. An endurance failure is determined when any one bit is not capable of being correctly written and maintained in that state indefinitely.

The device lifetime is defined when a specified percentage of devices, (Microchip currently uses a cumulative 2.5 percent), have a customer detectable error under worst case operating conditions.

Ongoing monitors are acquired from every wafer lot of material manufactured for shipment. Samples are subjected to byte cycling of a checkerboard pattern at 85°C in rapid succession to the specified number of guaranteed cycles. These units then are baked at 150°C for 48 hours in both checkerboard and inverse checkerboard forms and electrically tested to ensure that data sheet requirements are met. This data is accumulated on a monthly basis and reviewed to measure both results of continuous improvement programs and conformance against the device standards.

ENDURANCE VARIABLES

a. Temperature: Within the FLOTOX technology, temperature has an inverse effect on the endurance of a EEPROM device. The activation energy of these cycling failures is approximately 0.15 eV. The long term trap up portion of the curve is worsened by temperature to a greater extent than the early fails due to the difficult failure mechanisms that are activated.

b. Delay between cycles: This has been reported in the industry as having an enhanced effect on the lifetime of EEPROM devices. For some technologies this does have a positive effect, however, this is not strictly the case for FLOTOX manufacturers. While the second failure rate increase period (associated with end of life) may be impacted by this due to a decreased rate of electron trapping, the first failure rate is actually not impacted by this variable.

c. Write timing The decrease in write time to the device correlates directly with write/erase cycling failure rate of the device. This shorter pulse reduces the cell time at voltage which then provides an enhanced life prior to the occurrence of a time dependent oxide breakdown. It also passes fewer electrons through the oxide providing less potential trapping possibilities while maintaining adequate margins for the written state.

Please note that the rise time of the signal, which the customer does not have control over is also a dominant effect.

d. Vcc voltage The higher voltages generate higher fields within the device. This causes more stress which is offset by the operational increase of internal timers and actually shortens the write time of the device.

Lower voltages this has the opposite effects on the individual parameters except in cycles obviously where the write timer is externally controlled. This overall effect is minor compared to the others in magnitude on the failure rate curve and is variable over the customer operating range with a maximum at Vcc=5.5 Volts.

e. **Pattern effect** The pattern that is programmed in the device does play a first order role in the overall lifetime. The act of programming a non-volatile memory inflicts damage on the device that cannot be repaired. This damage is the result of exposure to high electric fields which over a period of time either breakdown or trap up the effected oxide causing failures. The act of writing a cell from a one to a zero provides the maximum amount of stress by exercising the charge pump and passing electrons through the tunnel dielectric. (Please note that to write a zero even from a zero state causes an automatic byte erase prior to the write converting the bit to a one and returning it to it's original state!) Conversely writing a one from a one then passes no charge through the cell and therefore does no damage to the cell but does stress the charge pump.

From an array standpoint, this would allow a checkerboard/ inverse checkerboard patterned device to endure twice the number of write cycles that an all zero patterned device would last. In general this appears to be approximately correct but does neglect the charge pump and other peripheral wearout mechanisms.

f. **Cycling mode** Three modes exist in Microchip devices that are primarily used for endurance evaluations. The byte write mode (one single byte written at a time) is the standard mode used by the customer in the field as well as the method of monitoring that has been chosen internally. This is to best estimate field lifetime expectations and actual failure rates. A second technique exists called block mode which exercises all the cells of the array simultaneously. The lifetime expectations are approximately twice as long for these block cycled devices as equivalently cycled byte cycled circuits based on experimental findings. This effect has been traced back to the rise time of the programming signal at the memory cell. The faster this voltage rise occurs, the more damage occurs and the shorter the lifetime. The block mode has a much slower rise time given the entire array being utilized provides a much larger resistive/capacitive load which slows the signal rise ultimately resulting in the greater lifetime. Please note that the page mode which can be utilized by the customers falls between the block and byte modes with respect to failure rate.

g. Array Size This effect is a direct result of how fast most devices will fail due to a single bit not working simply due to the number of bits involved. This is not exactly double the failure rate with a doubling of the memory size since some circuits fail within the charge pump or decoding circuitry sections and are therefore not directly related to array size.

FIELD RESULTS

Microchip Technology, after significant experimentation, has developed a model of the Endurance failure rates as a function of all the variables listed above. This model is available to the customer in the form of a diskette called *Total Endurance*™. This allows the customer to bypass confusing information and conditions other than their application and directly predict the failures seen in their application conditions within a few percent. This also allows the customer to adjust operating parameters and immediately evaluate the impact on the results of the final system. Results for a typical application (obtained from the *Total Endurance* model are listed at right for reference).

Device	Application Life	Cum Percent
24C02A	10 years	1 PPM
24C04A	10 years	2 PPM
93C46	10 years	1 PPM
93C56	10 years	1 PPM
24LC02B	10 years	1 PPM
24LC04B	10 years	1 PPM
24LC16B	10 years	512 PPM
93LC46B	10 years	1 PPM
93LC56B	10 years	1 PPM

Typical conditions used are 25°C, Byte mode operation with 24 cycles per day, V_{CC}=4.5 Volts with a random pattern writing one quarter of the array at each occasion. The failure rates quoted are the expected failure rate at the end of the application life using an unlimited number of read cycles. For more information on Endurance, it is recommended that the user obtain a copy of *Total Endurance*.

SECTION 11
PACKAGING

PACKAGING

Commercial/Industrial Outlines and Parameters

COMMERCIAL AND INDUSTRIAL PARTS

Part Number Suffix Designations:

XXXXXXXXXX - XX X / XX XXX

Examples:

27C256T-15I/J
PIC16C54-RCI/SO

ROM Code or Special Requirements

Case Outline

D = Ceramic
J = Cerdip (with window if EPROM) - all product except Microcontrollers
K = LCC (Ceramic Leadless Chip Carrier, not thermally enhanced)
L = PLCC (Plastic Leaded Chip Carrier)
P = Plastic
S = Die in Waffle Pack
W = Die in Wafer Form
CB = COB (Chip-On-Board)
JN = Cerdip, no window - for Microcontrollers only
JW = Cerdip, windowed - for Microcontrollers only
PQ = PQFP
SJ = Skinny Cerdip
SL = 14-Lead Small Outline .150 mil
SM = Small Outline .207 mil
SN = Small Outline .150 mil
SO = Small Outline .300 mil
SP = Skinny Plastic Carrier
SS = Shrink Small Outline Package
TS = Thin Small Outline (TSOP) 8mm x 20mm
VS = Very Small Outline (VSOP) 8 x 13mm

Process Temperature

Blank = 0°C to +70°C
I = -40°C to +85°C
E = -40°C to +125°C

Speed (EPROM / High Density EEPROM)	**Frequency**	**Crystal Frequency Designator for PIC16/17 Microcontrollers**
-55 = 55 ns	Blank = 20.5 MHz	LP = 4 µs - Low Power
-70 = 70 ns	-14 = 14.4 MHz	RC = 2 µs - Resistor Capacitor
-90 = 90 ns	-25 = 25.6 MHz	XT = 1 µs - Crystal
-10 = 100 ns	-32 = 32.8 MHz	HS = 20 MHz - High Speed Crystal
-12 = 120 ns		-10 = 10 MHz - High Speed Crystal
-15 = 150 ns		-04 = 4 MHz - Crystal or RC
-17 = 170 ns		-16 = 16 MHz - High Speed Crystal
-20 = 200 ns		-20 = 20 MHz - High Speed Crystal
-25 = 250 ns		-25 = 25 MHz - High Speed Crystal

OPTION

- = twc = 1 ms
F = twc = 200 µs
X = Rotated pinout
T = Tape and Reel

Device Type (Up To 10 Digits)

C = Indicates CMOS
LC = Indicates Low Power CMOS
AA = 1.8V
LV = Low Voltage
HC = High Speed
LCS = Low Power Security

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SECTION 1: HERMETIC

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SECTION 2: PLASTIC

Packaging Diagrams and Parameters

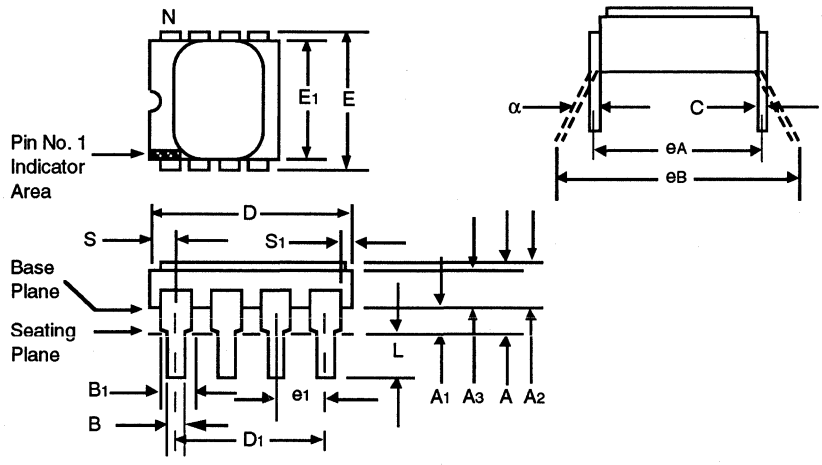
Ceramic Side Brazed Dual In-line Family

Symbol List for Ceramic Side Brazed Dual In-line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body (lid)
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body (lid)
A_3	Base body thickness
B	Width of terminal leads
B_1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D_1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E_1	Body width parameters not including leads
e_A	Linear spacing of true minimum lead position center line to center line
e_B	Linear spacing between true lead position outside of lead to outside of lead
e_1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	Total number of potentially usable lead positions
S	Distance from true position center line of Number 1 lead to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body

Notes:
1. Controlling parameter: inches.
2. Parameter "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B_1" is nominal.

Packaging Diagrams and Parameters

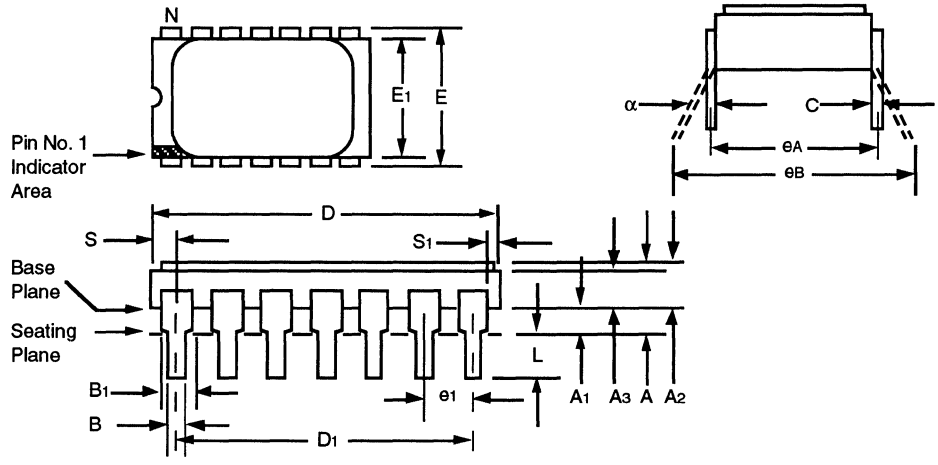
Package Type: 8-Lead Ceramic Side Brazed Dual In-line (300 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	3.937		0.130	0.155	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.4064	0.508		0.016	0.020	
B1	1.3716	1.3716	Typical	0.054	0.054	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	13.0048	13.4112		0.512	0.528	
D1	7.4168	7.8232	Reference	0.292	0.308	Reference
E	7.5692	8.2296		0.298	0.324	
E1	7.112	7.620		0.280	0.300	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.620	9.652		0.300	0.380	
L	3.302	3.810		0.130	.150	
N	8	8		8	8	
S	2.540	3.048		0.100	0.120	
S1	0.127	–		.005	–	

Packaging Diagrams and Parameters

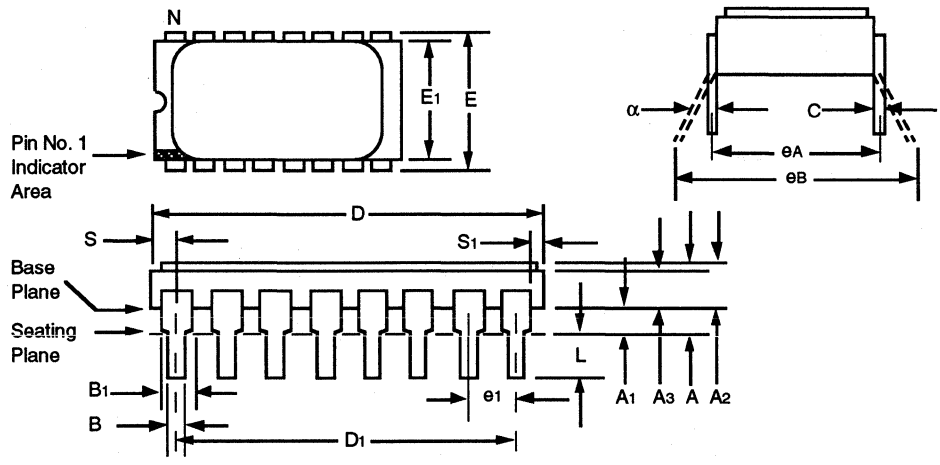
Package Type: 14-Lead Ceramic Side Brazed Dual In-line (300 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	4.064		0.130	0.160	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.2032	0.3048	Typical	0.008	0.012	Typical
D	18.796	19.2278		0.740	0.757	
D1	15.0368	15.4432	Reference	0.592	0.608	Reference
E	7.620	8.382		0.300	0.330	
E1	7.0612	7.5692		0.278	0.298	
e1	2.3622	2.7432	Typical	0.093	0.108	Typical
eA	7.366	7.874	Reference	0.290	0.310	Reference
eB	7.620	9.652		0.300	0.380	
L	3.175	4.191		0.125	0.165	
N	14	14		14	14	
S	–	2.4892		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

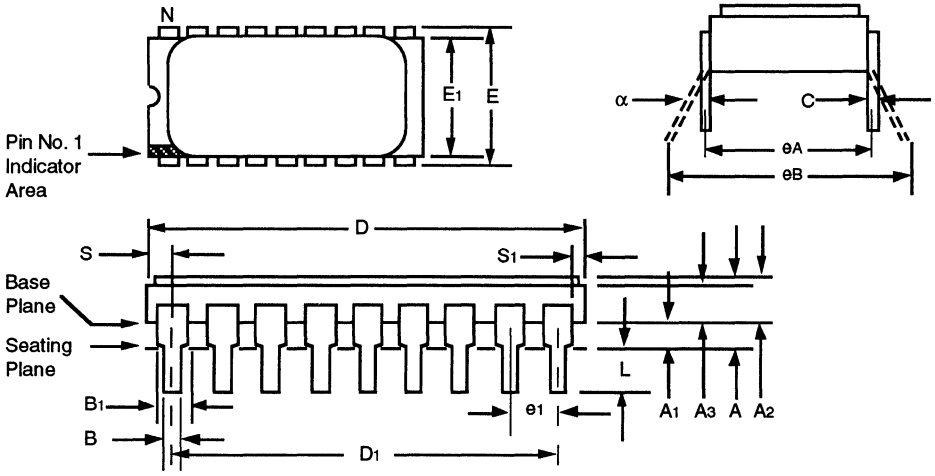
Package Type: 16-Lead Ceramic Side Brazed Dual In-line (300 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	4.064		0.130	0.160	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.4064	0.508		0.016	0.020	
B1	1.3716	1.3716	Typical	0.054	0.054	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	19.812	20.574		0.780	0.810	
D1	17.653	17.907	Reference	0.695	0.705	Reference
E	7.620	8.382		0.300	0.330	
E1	7.1628	7.4676		0.282	0.294	
e1	2.413	2.667	Typical	0.095	0.105	Typical
eA	7.366	7.874	Reference	0.290	0.310	Reference
eB	7.620	9.652		0.300	0.380	
L	3.175	4.191		0.125	0.165	
N	16	16		16	16	
S	–	2.032		–	0.080	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

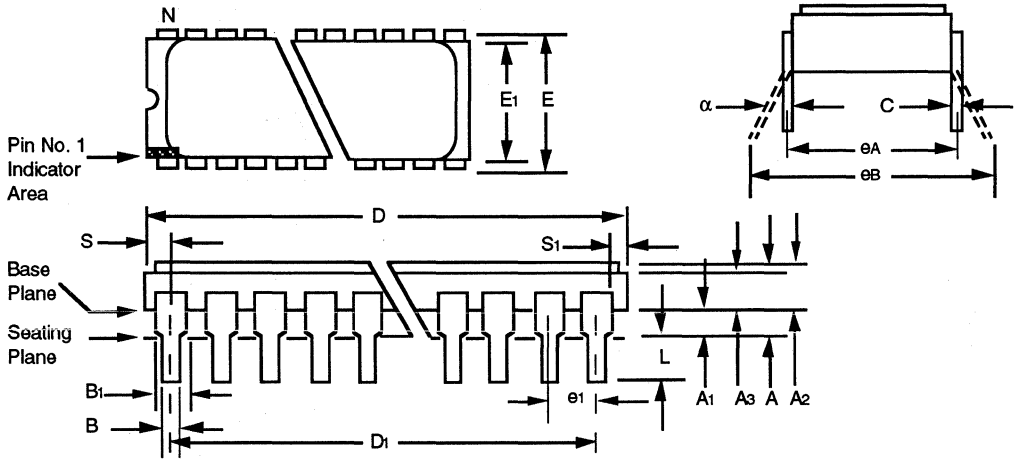
Package Type: 18-Lead Ceramic Side Brazed Dual In-line (300 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	4.064		0.130	0.160	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.4064	0.508		0.016	0.020	
B1	1.3716	1.3716	Typical	0.054	0.054	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	22.352	23.114		0.880	0.910	
D1	20.193	20.447	Reference	0.795	0.805	Reference
E	7.620	8.382		0.300	0.330	
E1	7.0612	7.5692		0.278	0.298	
e1	2.413	2.667	Typical	0.095	0.105	Typical
eA	7.366	7.874	Reference	0.290	0.310	Reference
eB	7.620	9.652		0.300	0.380	
L	3.175	4.191		0.125	0.165	
N	18	18		18	18	
S	–	2.4892		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

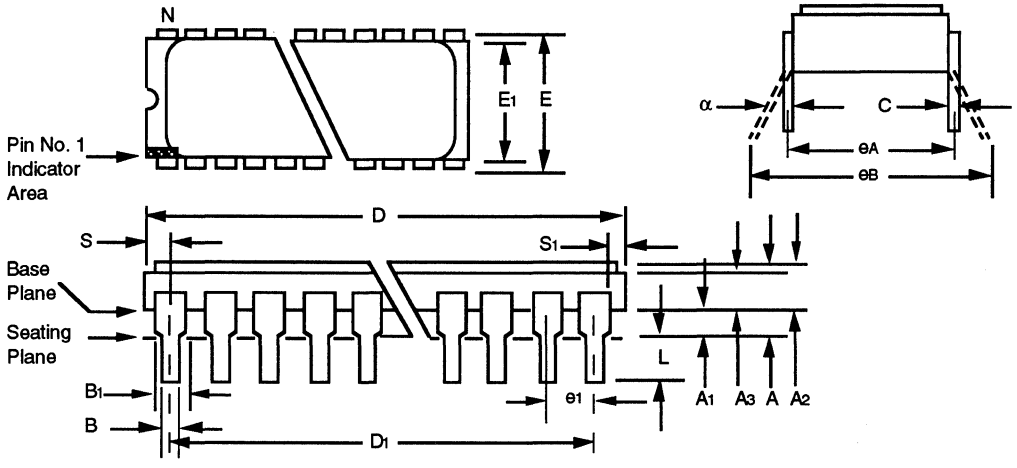
Package Type: 22-Lead Ceramic Side Brazed Dual In-line (400 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	2.667	4.064		0.105	0.160	
A1	0.7112	1.2192		0.028	0.048	
A2	2.032	3.302		0.080	0.130	
A3	1.778	2.921		0.070	0.115	
B	0.4318	0.5842		0.017	0.023	
B1	1.016	1.016	Typical	0.040	0.040	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	27.1526	27.8638		1.069	1.091	
D1	25.2968	25.6032	Reference	0.992	1.008	Reference
E	10.160	10.922		0.400	0.430	
E1	9.7282	9.9822		0.383	0.393	
e1	2.3368	2.7432	Typical	0.092	0.108	Typical
eA	9.906	10.414	Reference	0.390	0.410	Reference
eB	10.160	12.192		0.400	0.480	
L	3.175	4.191		0.125	0.165	
N	22	22		22	22	
S	–	2.032		–	0.080	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

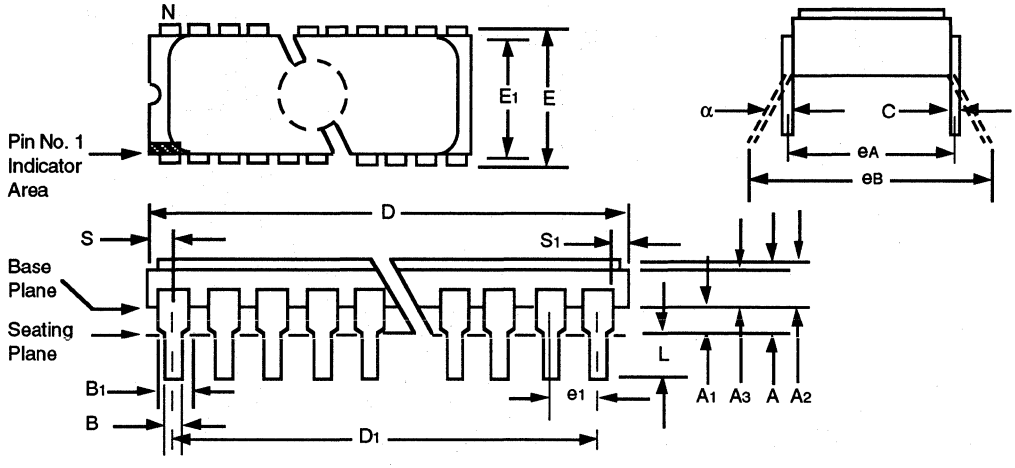
Package Type: 24-Lead Ceramic Side Brazed Dual In-line (600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	30.1752	30.7848		1.188	1.212	
D1	27.7368	28.1432	Reference	1.092	1.108	Reference
E	14.986	16.002		0.590	0.630	
E1	14.7828	14.9352		0.582	0.588	
e1	2.3368	2.7432	Typical	0.092	0.108	Typical
eA	14.986	15.748	Reference	0.590	0.620	Reference
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	24	24		24	24	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

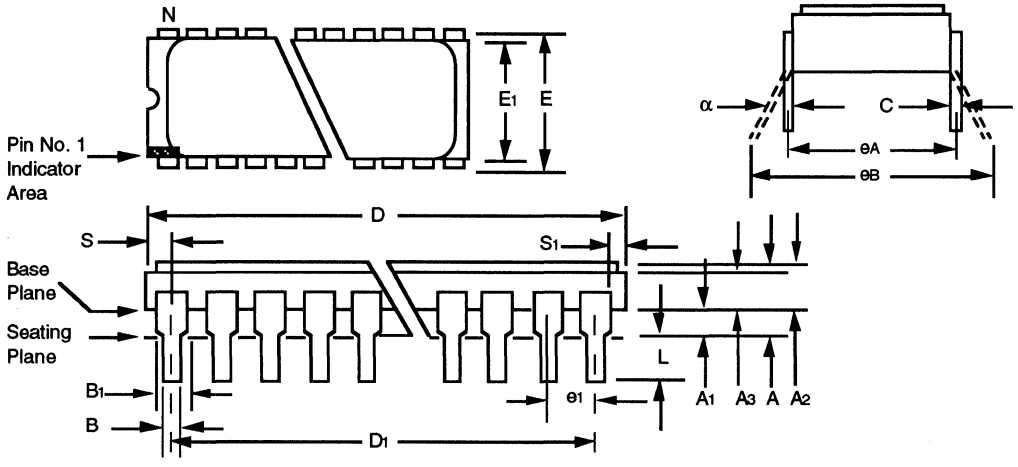
Package Type: 24-Lead Ceramic Side Brazed Dual In-line with Window (600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	30.1752	30.7848		1.188	1.212	
D1	27.7368	28.1432	Reference	1.092	1.108	Reference
E	14.986	16.002		0.590	0.630	
E1	14.7828	14.9352		0.582	0.588	
e1	2.3368	2.7432	Typical	0.092	0.108	Typical
eA	14.986	15.748	Reference	0.590	0.620	Reference
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	24	24		24	24	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

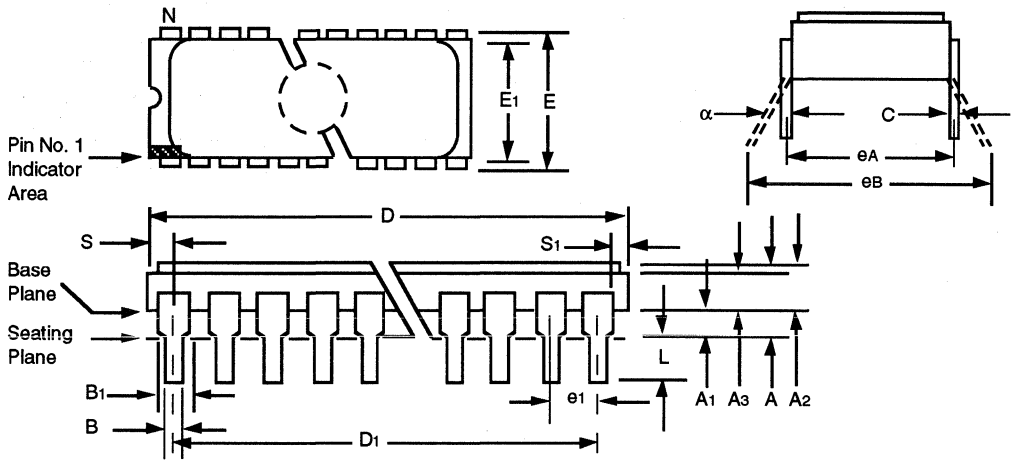
Package Type: 28-Lead Ceramic Side Brazed Dual In-line (600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.064		0.120	0.160	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.4572	0.508		0.018	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	35.2044	35.9156		1.386	1.414	
D1	32.8168	33.2232	Reference	1.292	1.308	Reference
E	14.986	16.002		0.590	0.630	
E1	14.7828	15.1892		0.582	0.598	
e1	2.4892	2.5908	Typical	0.098	0.102	Typical
eA	14.986	15.494	Reference	0.590	0.610	Reference
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	28	28		28	28	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

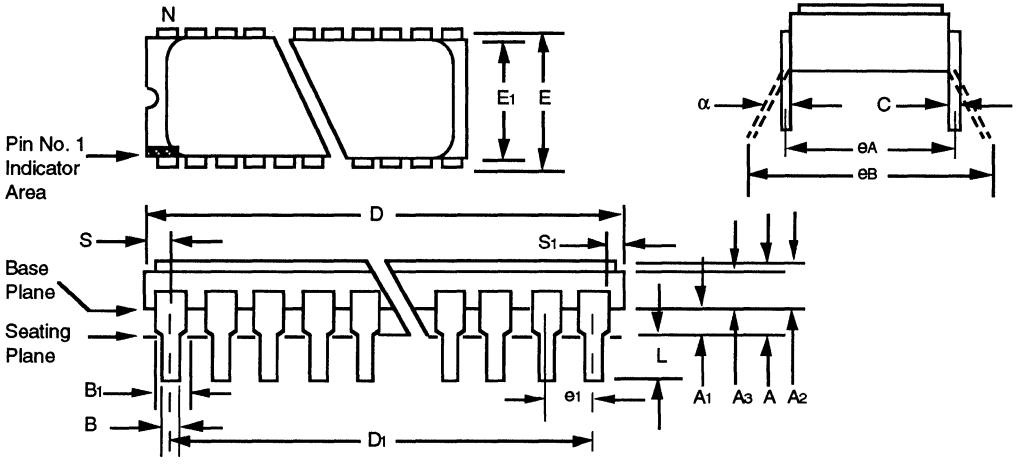
Package Type: 28-Lead Ceramic Side Brazed Dual In-line with Window (600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.064		0.120	0.160	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.4572	0.508		0.018	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	35.2044	35.9156		1.386	1.414	
D1	32.8168	33.2232	Reference	1.292	1.308	Reference
E	14.986	16.002		0.590	0.630	
E1	14.7828	15.1892		0.582	0.598	
e1	2.4892	2.5908	Typical	0.098	0.102	Typical
eA	14.986	15.494	Reference	0.590	0.610	Reference
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	28	28		28	28	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

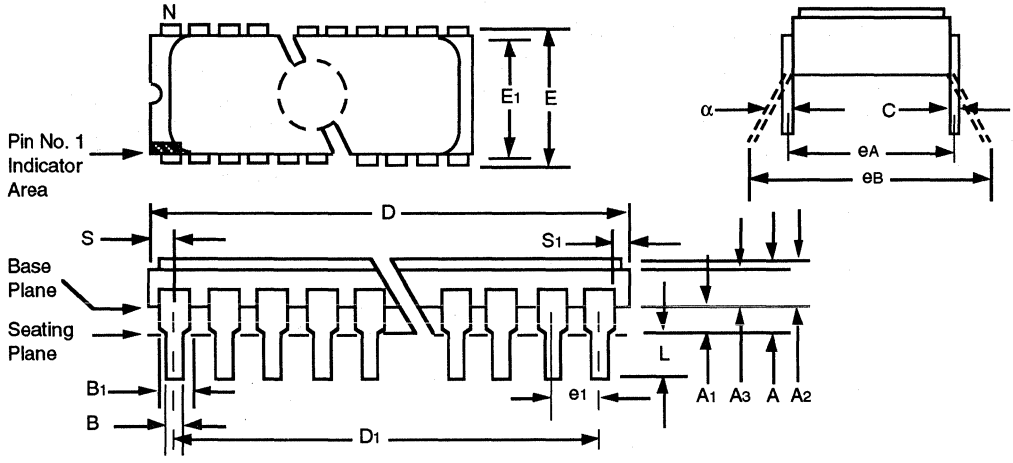
Package Type: 40-Lead Ceramic Side Brazed Dual In-line (600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.829	2.235		.072	.088	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	50.546	51.308		1.990	2.020	
D1	48.056	48.463	Reference	1.892	1.908	Reference
E	15.240	16.256		0.600	0.640	
E1	14.478	15.748		0.570	0.620	
e1	2.3368	2.7432	Typical	0.092	0.108	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	40	40		40	40	
S	–	2.4892		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

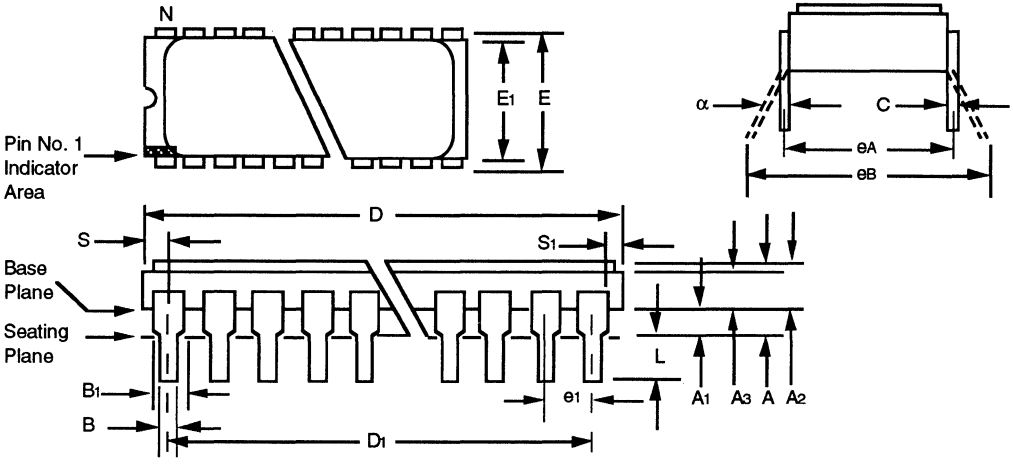
Package Type: 40-Lead Ceramic Side Brazed Dual In-line with Window (600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.829	2.235		.072	.088	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	50.546	51.308		1.990	2.020	
D1	48.056	48.463	Reference	1.892	1.908	Reference
E	15.240	16.256		0.600	0.640	
E1	14.478	15.748		0.570	0.620	
e1	2.3368	2.7432	Typical	0.092	0.108	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	40	40		40	40	
S	–	2.4892		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

Package Type: 48-Lead Ceramic Side Brazed Dual In-line (600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.829	2.235		0.072	0.088	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.2286	0.3048	Typical	0.009	0.012	Typical
D	60.3504	61.5696		2.376	2.424	
D1	58.2168	58.6232	Reference	2.292	2.308	Reference
E	15.240	16.256		0.600	0.640	
E1	14.478	15.748		0.570	0.620	
e1	2.3368	2.7432	Typical	0.092	0.108	Typical
eA	15.240	15.290	Reference	0.600	0.600	Reference
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	48	48		48	48	
S	–	2.4892		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

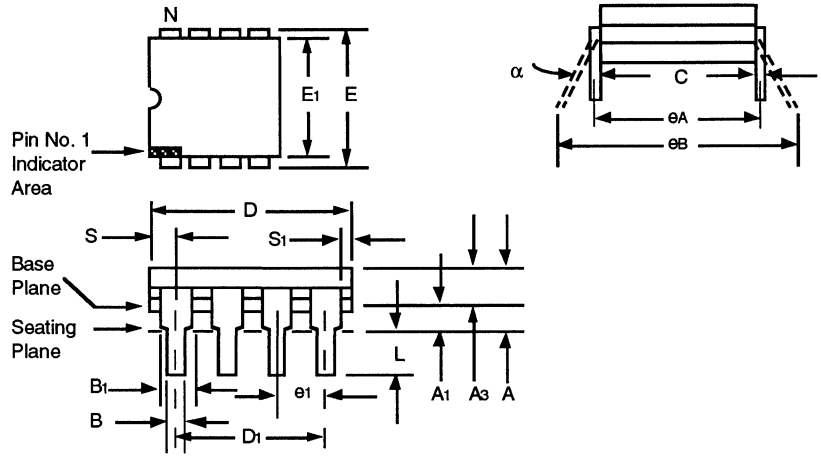
Ceramic Cerdip Dual In-line Family

Symbol List for Ceramic Cerdip Dual In-line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body (lid)
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body (lid)
A_3	Base body thickness
B	Width of terminal leads
B_1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D_1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E_1	Body width parameters not including leads
e_A	Linear spacing of true minimum lead position center line to center line
e_B	Linear spacing between true lead position outside of lead to outside of lead
e_1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	Total number of potentially usable lead positions
S	Distance from true position center line of Number 1 lead to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body

Notes:
1. Controlling parameter: inches.
2. Parameter "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B_1" is nominal.

Packaging Diagrams and Parameters

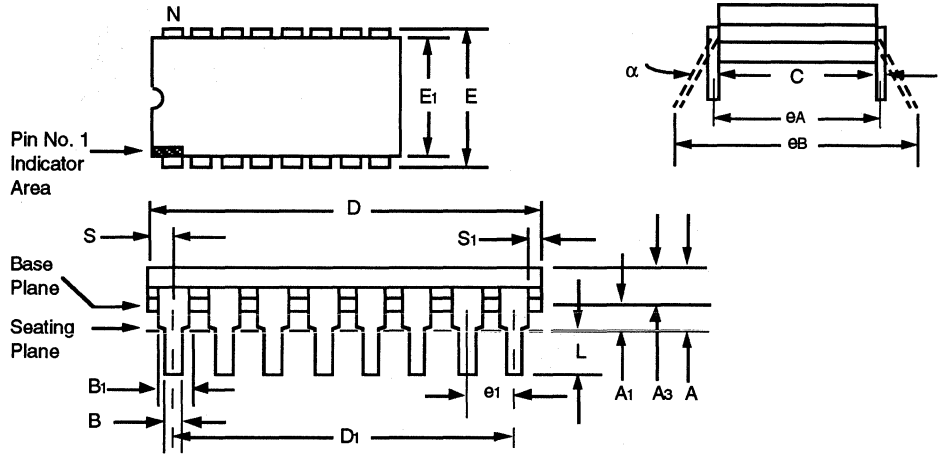
Package Type: 8-Lead Cerdip Dual In-line (300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.524		0.015	0.060	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.3556	0.5843		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	9.398	10.287		0.370	0.405	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	7.620	8.255		0.300	0.325	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.366	8.128	Referemce	0.290	0.320	Reference
eB	7.620	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	8	8		8	8	
S	0.508	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

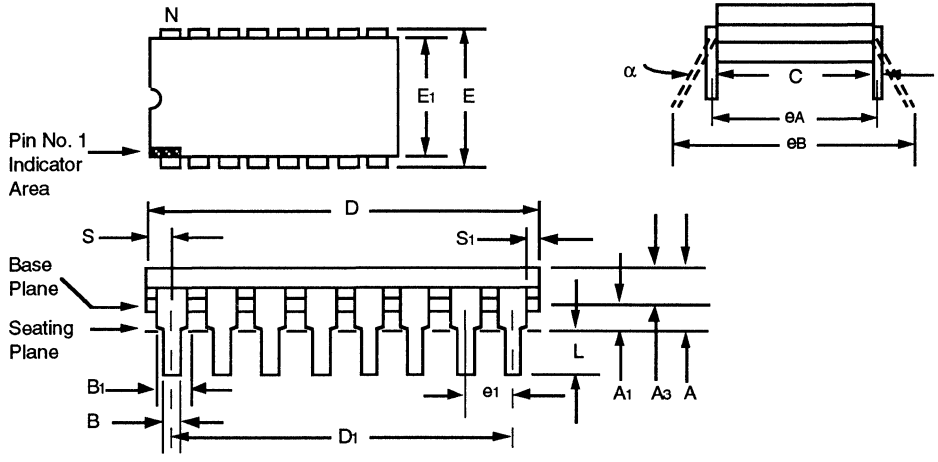
Package Type: 16-Lead Ceramic Cerdip Dual In-line (300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.191	5.080		0.165	0.200	
A1	0.381	1.524		0.015	0.060	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.3556	0.5842		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	19.050	20.320		0.750	0.800	
D1	17.780	17.780	Reference	0.700	0.700	Reference
E	7.493	8.255		0.295	0.325	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.366	8.128	Reference	0.290	0.320	Reference
eB	7.62	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	16	16		16	16	
S	5.08	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

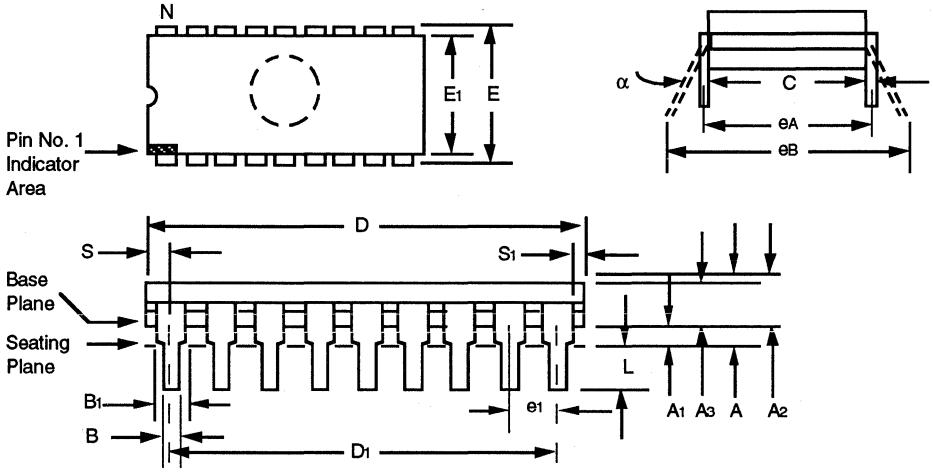
Package Type: 18-Lead Ceramic Cerdip Dual In-line (300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.778		0.015	0.070	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.3556	0.5842		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	22.352	23.622		0.880	0.930	
D1	20.320	20.320	Reference	0.800	0.800	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	7.366	8.128	Typical	0.290	0.320	Typical
eB	7.62	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	18	18		18	18	
S	.508	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

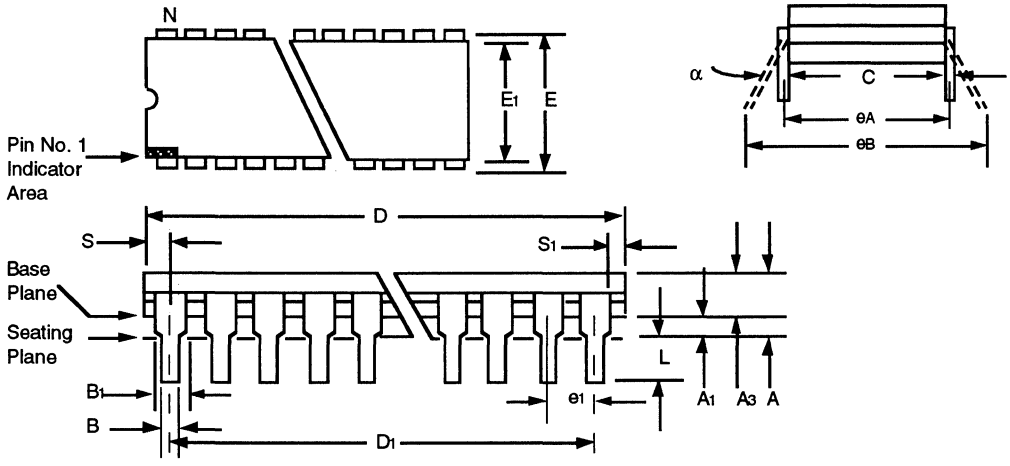
Package Type: 18-Lead Cerdip Dual In-line with Window (300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.7780		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.3556	0.5842		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	22.352	23.622		0.880	0.930	
D1	20.320	20.320	Reference	0.800	0.800	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	7.366	8.128	Typical	0.290	0.320	Typical
eB	7.620	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	18	18		18	18	
S	0.508	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

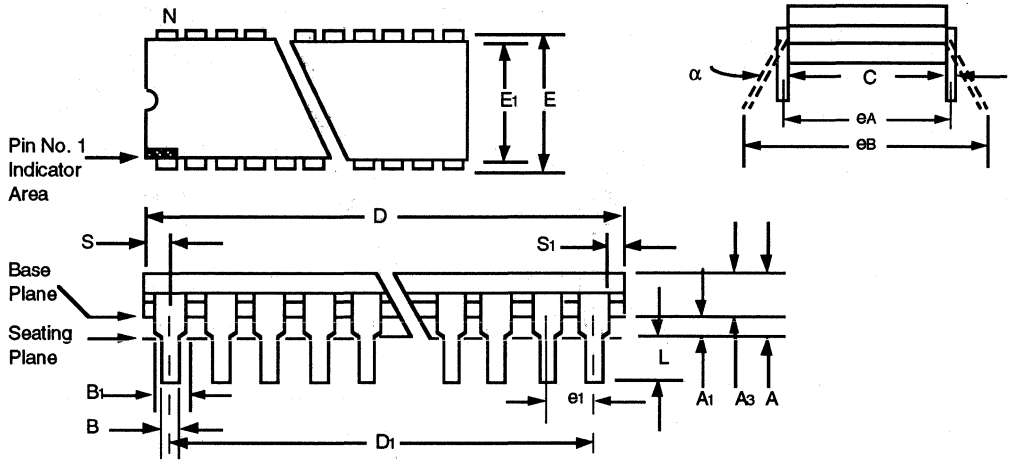
Package Type: 22-Lead Ceramic Cerdip Dual In-line (400 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A_1	0.381	1.778		0.015	0.070	
A_2	—	—	Ref. A_3	—	—	Ref. A_3
A_3	3.810	4.445		0.150	0.175	
B	0.3556	0.5842		0.014	0.023	
B_1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	26.670	27.940		1.050	1.100	
D_1	25.400	25.400	Reference	1.000	1.000	Reference
E	10.160	10.922		0.400	0.430	
E_1	8.890	10.414		0.350	0.410	
e_1	2.540	2.540	Reference	0.100	0.100	Reference
e_A	9.906	10.668	Typical	0.390	0.420	Typical
e_B	10.160	12.700		0.400	0.500	
L	3.175	3.810		0.125	0.150	
N	18	18		22	22	
S	—	1.270		—	0.050	
S_1	0.127	1.270		0.005	0.050	

Packaging Diagrams and Parameters

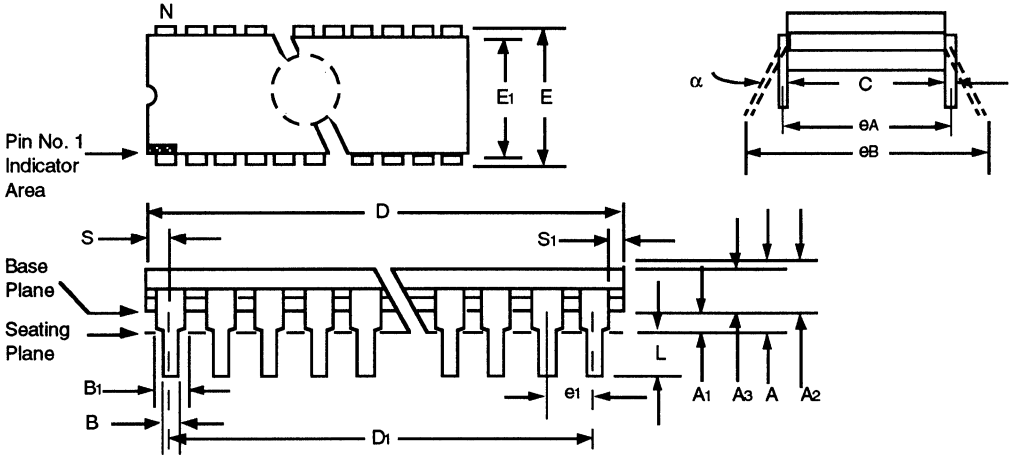
Package Type: 24-Lead Ceramic Cerdip Dual In-line (300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.905		0.015	0.075	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.3556	0.5842		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	7.366	8.128	Typical	0.290	0.320	Typical
eB	7.62	11.43		0.300	0.450	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

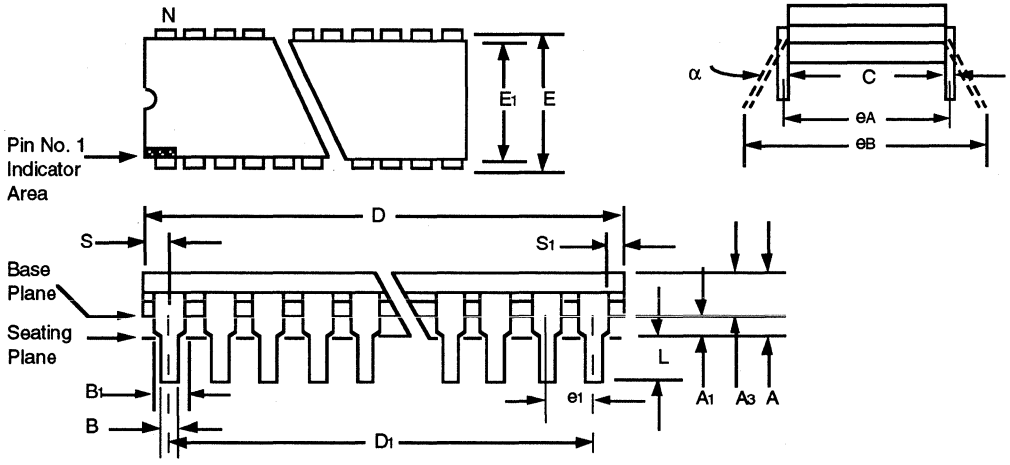
Package Type: 24-Lead Ceramic Cerdip Dual In-line with Window (300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.905		0.015	0.075	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.3556	0.5842		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	7.366	8.128	Typical	0.290	0.320	Typical
eB	7.620	11.43		0.300	0.450	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

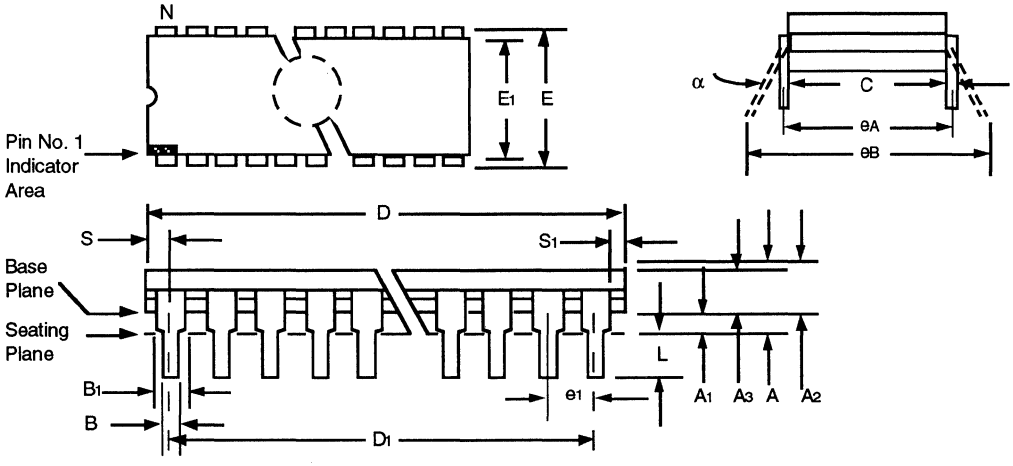
Package Type: 24-Lead Ceramic Cerdip Dual In-line (600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.905		0.015	0.075	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.3556	0.5842		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	14.986	15.748	Typical	0.590	0.620	Typical
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

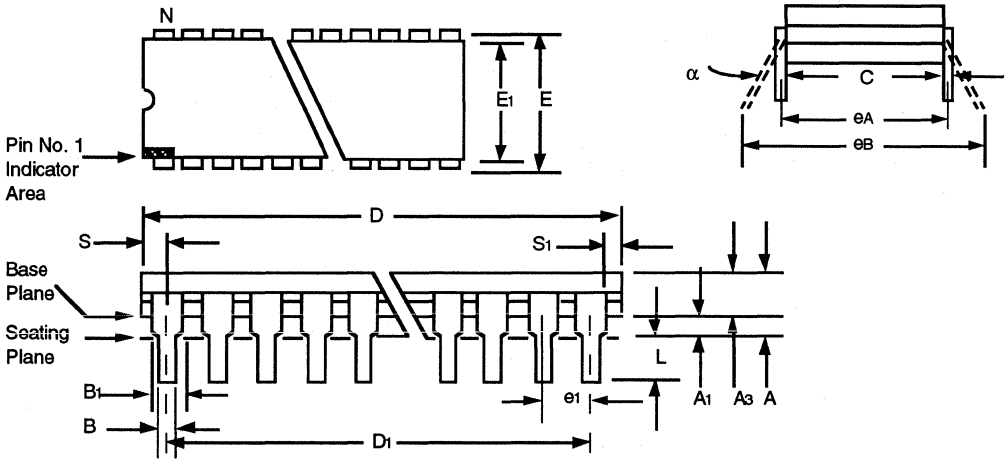
Package Type: 24-Lead Ceramic Cerdip Dual In-line with Window (600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.905		0.015	0.075	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.3556	0.5842		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	14.986	15.748	Typical	0.590	0.620	Typical
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

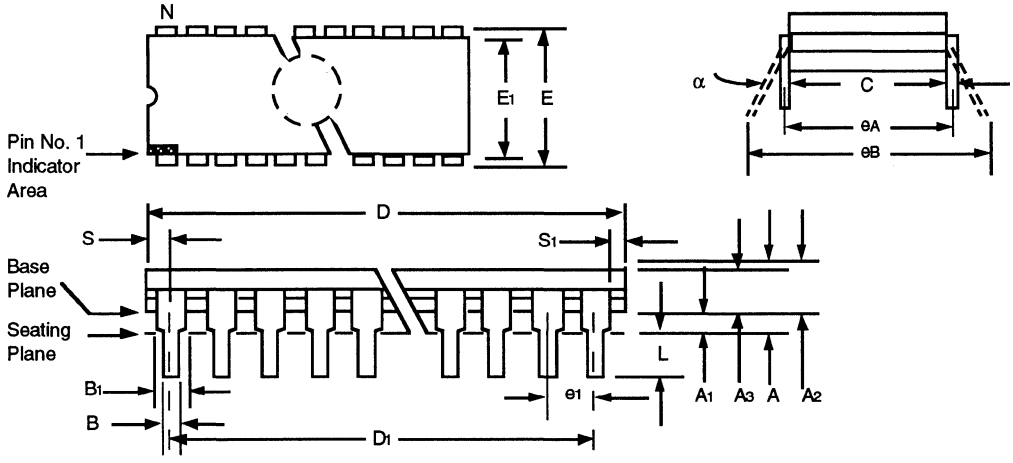
Package Type: 28-Lead Ceramic Cerdip Dual In-line (600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.461		—	0.215	
A1	0.381	1.524		0.015	0.060	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.3556	0.5842		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	36.195	37.465		1.425	1.475	
D1	33.020	33.020	Reference	1.300	1.300	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	14.986	15.748	Typical	0.590	0.620	Typical
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	28	28		28	28	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

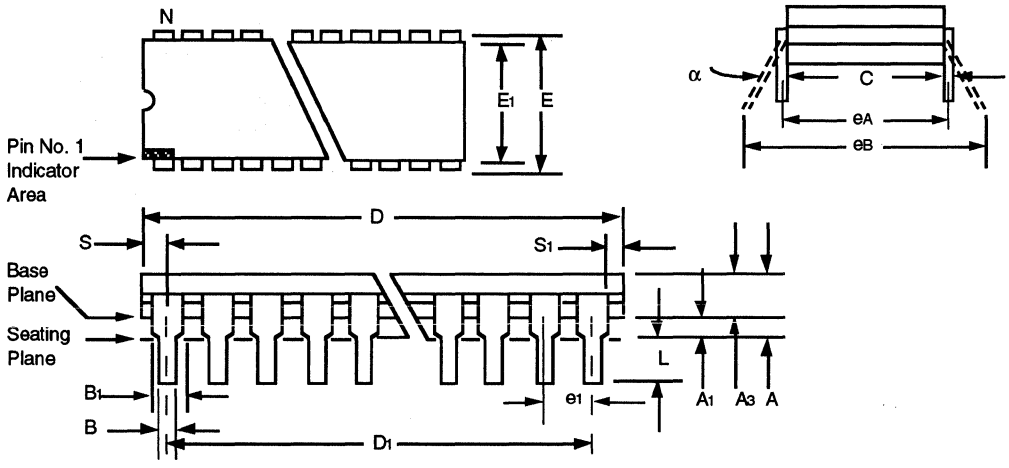
Package Type: 28-Lead Ceramic Cerdip Dual In-line with Window (600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.461		—	0.215	
A1	0.381	1.524		0.015	0.060	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.3556	0.5842		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	36.195	37.465		1.425	1.475	
D1	33.020	33.020	Reference	1.300	1.300	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	14.986	15.748	Reference	0.590	0.620	Reference
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	28	28		28	28	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

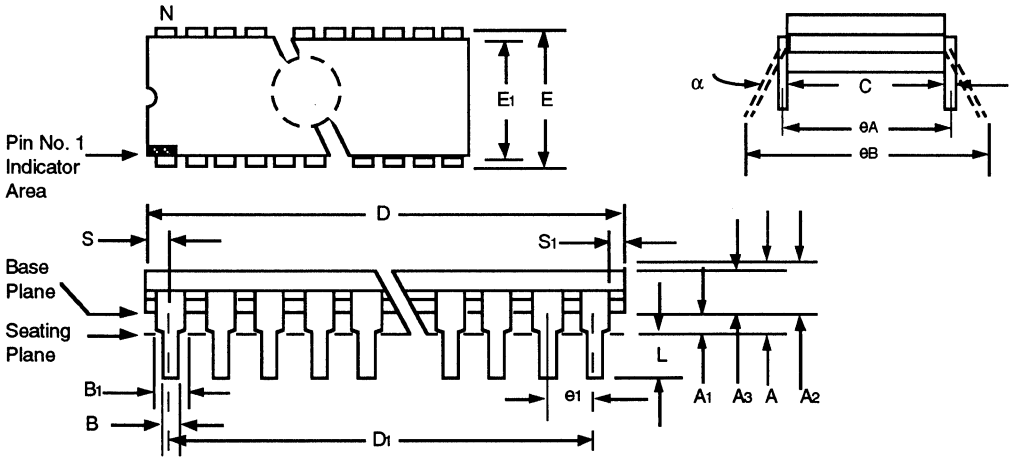
Package Type: 40-Lead Ceramic Cerdip Dual In-line (600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	–	–	Ref. A3	–	–	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.3556	0.5842		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	14.986	16.002	Reference	0.590	0.630	Reference
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	40	40		40	40	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

Package Type: 40-Lead Ceramic Cerdip Dual In-line with Window (600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	3.810	4.699	Ref. A3	0.150	0.185	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.3556	0.5842		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Reference	0.100	0.100	Reference
θA	14.986	16.002	Typical	0.590	0.630	Typical
θB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	40	40		40	40	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

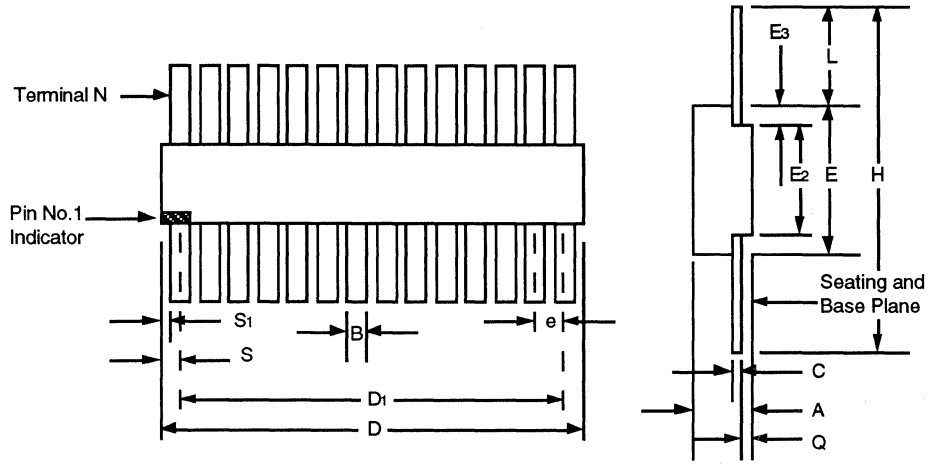
Ceramic Flatpack Family

Symbol List for Ceramic Flatpack Package Parameters	
Symbol	**Description of Parameters**
A	Distance between seating plane to highest point of body (lid)
B	Width of terminal leads
C	Thickness of terminal leads
D	Largest overall package parameter of length
D_1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E_2, E_3	Body width parameters not including leads
e	Linear spacing between center lines of body standoffs (terminal leads)
H	Other package width parameter
L	Distance from package body to end of lead
N	Total number of potentially usable lead positions
Q	Distance between seating plane and lead
S	Distance from true position center line of Number 1 lead to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body

Notes:
1. Controlling parameter: inches.
2. Parameter "e1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameters "B" and "C" are nominal.

Packaging Diagrams and Parameters

Package Type: 28-Lead Ceramic Flatpack



Package Group: Ceramic Flatpack (CFPK)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	2.286	3.302		0.090	0.130	
B	0.381	0.4826		0.015	0.019	Typical
C	0.0762	0.1524		0.003	0.006	Typical
D	17.780	18.796		0.700	0.740	
D_1	16.3068	16.7132		0.642	0.658	Reference
E	9.652	10.668		0.380	0.420	
E_2	4.572	–		0.180	–	
E_3	0.762	–		0.030	–	
e	1.270	1.270	BSC	0.050	0.050	Typical
H	22.352	29.464		0.880	1.160	
L	6.350	9.398		0.250	0.370	
N	28	28		28	28	
Q	0.6604	1.143		0.026	0.045	
S	0.889	1.016		0.035	0.040	
S_1	0.254	0.381		0.010	0.015	

Packaging Diagrams and Parameters

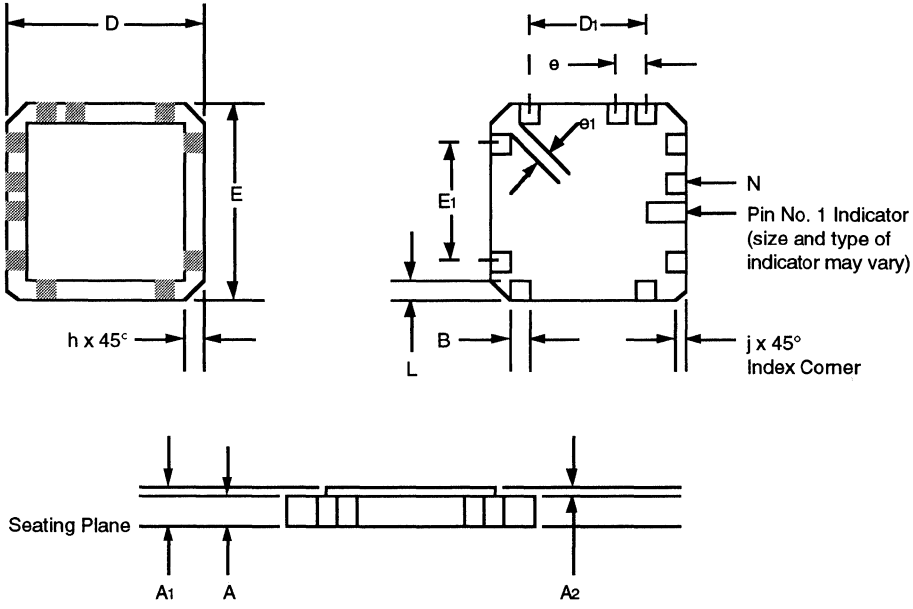
Ceramic Leadless Chip Carrier Family

Symbol List for Ceramic Leadless Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Thickness of base body
A_1	Total package height
A_2	Distance from base body to highest point of body (lid)
B	Width of terminal lead pin
D	Largest overall package dimension of length
D_1, E_1	Body length dimension - end lead center to end lead center
E	Largest overall package dimension of width
e	Linear spacing
e_1	Linear spacing between edges of true lead positions (of corner terminal lead pads) lead corner to lead corner
h	Depth of major index feature
j	Width of minor index feature
L	Distance from package edge to end of effective pad
N	Total number of potentially usable lead positions

Notes:
1. Controlling dimension: inches.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by PC board hole size.
4. Dimension "B" is nominal.
5. Corner configuration optional.

Packaging Diagrams and Parameters

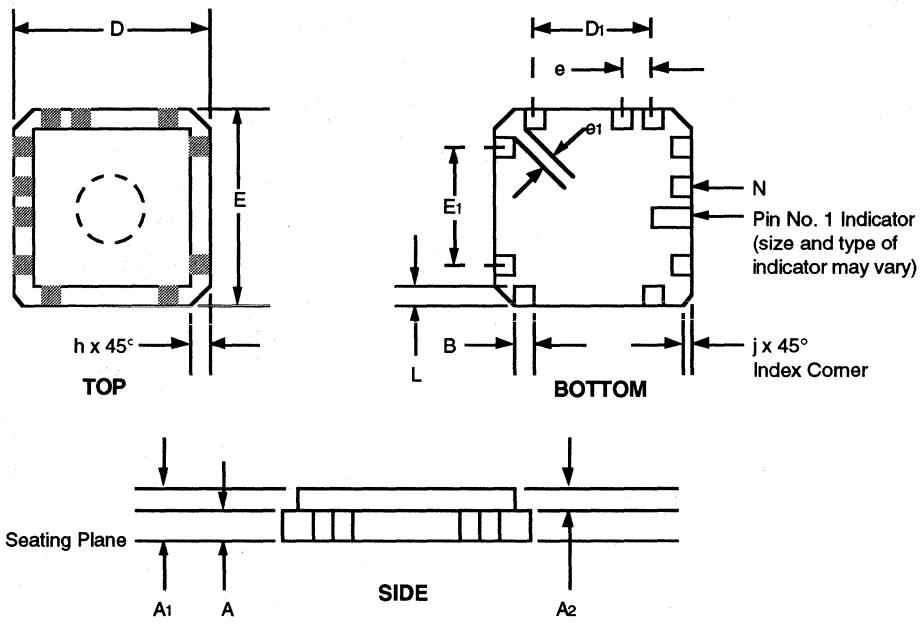
Package Type: 28-Lead Ceramic Leadless Chip Carrier



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	1.651	2.540		0.065	0.100	
A2	0.254	0.381		0.010	0.015	
B	0.5588	0.7112	Typical	0.022	0.028	Typical
D	11.2268	11.684		0.442	0.460	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.2268	11.684		0.442	0.460	
E1	7.620	7.620	Typical	0.300	0.300	Typical
e	1.270	1.270	Reference	0.050	0.050	Reference
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	28	28		28	28	

Packaging Diagrams and Parameters

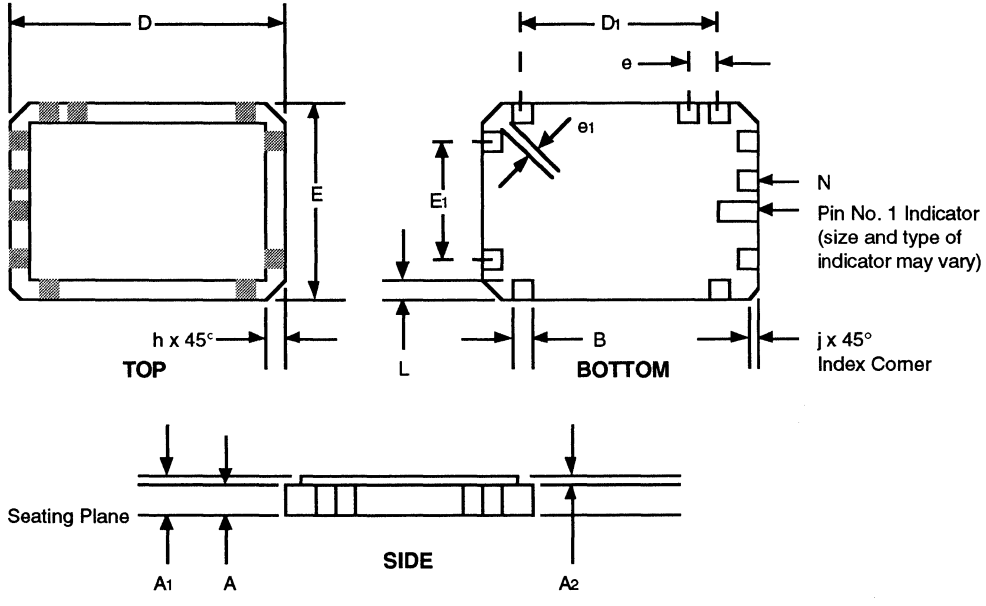
Package Type: 28-Lead Ceramic Leadless Chip Carrier with Window



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	2.540		0.090	0.100	
A2	0.889	1.143		0.035	0.045	
B	0.5588	0.7112	Typical	0.022	0.028	Typical
D	11.2268	11.684		0.442	0.460	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.2268	11.684		0.442	0.460	
E1	7.620	7.620	Reference	0.300	0.300	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	28	28		28	28	

Packaging Diagrams and Parameters

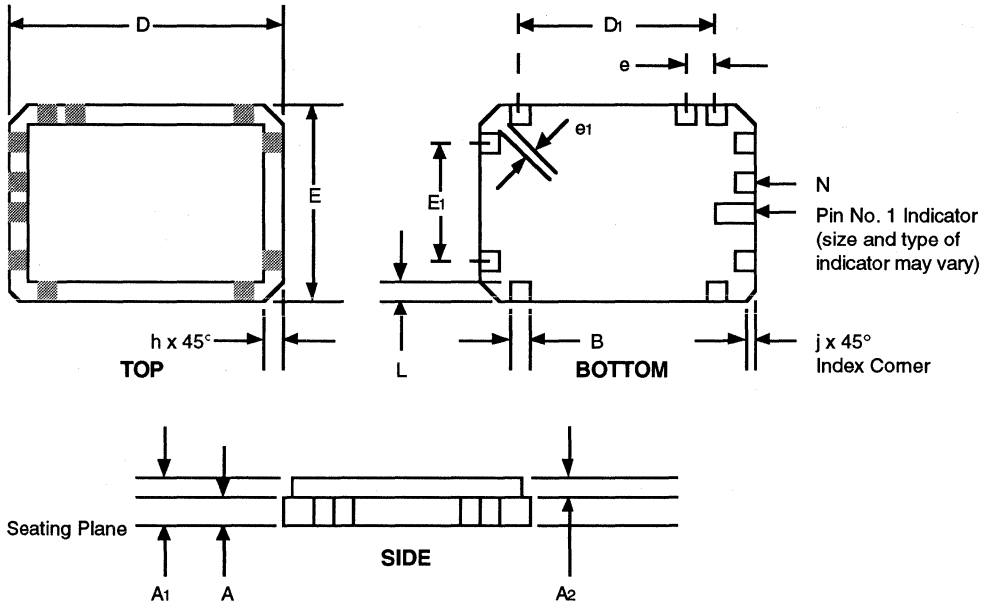
Package Type: 32-Lead Ceramic Leadless Chip Carrier



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.54	3.048		0.100	0.120	
A2	0.254	0.381		0.010	0.015	
B	0.635	0.6604	Typical	0.025	0.026	Typical
D	13.716	14.224		0.540	0.560	
D1	9.9822	10.3378	Reference	0.393	0.407	Reference
E	11.2268	11.6332		0.442	0.458	
E1	7.4422	7.7978	Reference	0.293	0.307	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

Packaging Diagrams and Parameters

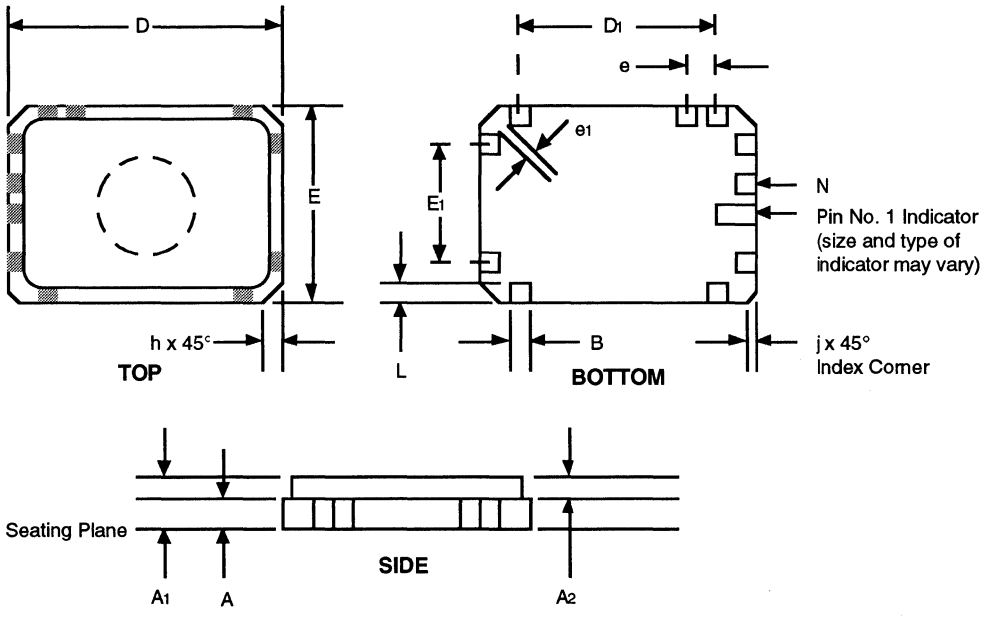
Package Type: 32-Lead Ceramic Leadless Chip Carrier - FRIT



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	3.302		0.090	0.130	
A2	0.635	1.143		0.025	0.045	
B	0.5588	0.7112	Typical	0.022	0.028	Typical
D	13.716	14.224		0.540	0.560	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.2268	11.6332		0.442	0.458	
E1	10.160	10.160	Reference	0.400	0.400	Reference
e	1.270	1.270	Reference	0.050	0.050	Reference
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

Packaging Diagrams and Parameters

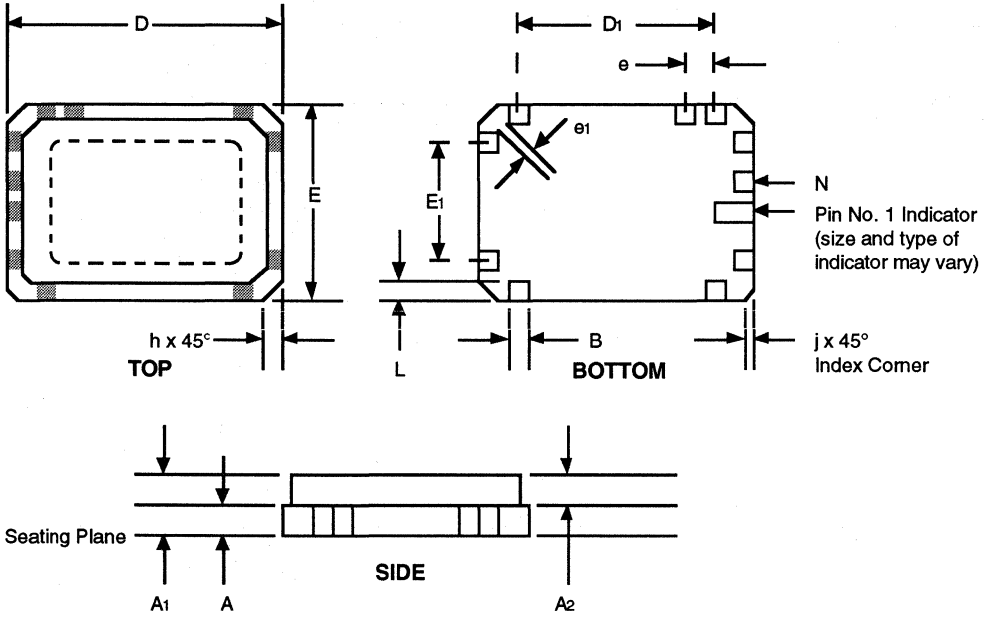
Package Type: 32-Lead Ceramic Leadless Chip Carrier with Window



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	3.302		0.090	0.130	
A2	0.889	1.143		0.035	0.045	
B	0.5588	0.7112	Typical	0.022	0.028	Typical
D	13.716	14.224		0.540	0.560	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.2268	11.6332		0.442	0.458	
E1	10.160	10.160	Reference	0.400	0.400	Reference
e	1.270	1.270	Reference	0.050	0.050	Reference
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

Packaging Diagrams and Parameters

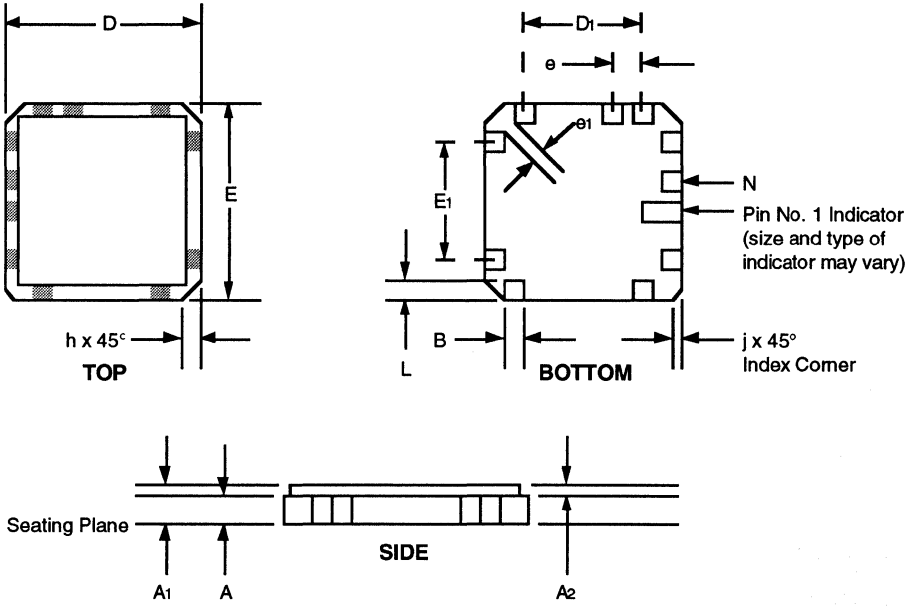
Package Type: 32-Lead Ceramic Leadless FRIT-Seal Chip Carrier with Window



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	3.302		0.090	0.130	
A2	0.889	1.143		0.035	0.045	
B	0.5588	0.7112	Typical	0.022	0.028	Typical
D	13.716	14.224		0.540	0.560	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.2268	11.6332		0.442	0.458	
E1	10.160	10.160	Reference	0.400	0.400	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

Packaging Diagrams and Parameters

Package Type: 44-Lead Ceramic Leadless Chip Carrier



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.3716	2.0828		0.054	0.082	
A1	1.778	3.048		0.070	0.120	
A2	0.254	1.143		0.010	0.045	
B	0.5842	0.7112	Typical	0.023	0.028	Typical
D	16.256	16.8148		0.640	0.662	
D1	12.700	12.700	Reference	0.500	0.500	Reference
E	16.256	16.8148		0.640	0.662	
E1	12.700	12.700	Reference	0.500	0.500	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	44	44		44	44	

Packaging Diagrams and Parameters

Ceramic Leaded Chip Carrier Family

Symbol List for Ceramic Leaded Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Distance from seating plane to highest point of body
A_1	Distance from lead shoulder to seating plane
CP	Seating plane coplanarity
D/E	Outside dimension
D_1/E_1	Body dimension
D_2/E_2	Footprint
D_3/E_3	Footprint
LT	Lead thickness
N	Total number of potentially usable lead positions
N_d	Total number of leads on short side (rectangular)
N_e	Total number of leads on long side (rectangular)

Notes:

1 All dimensions and tolerances conform to ANSI Y14.5M-1982.

2 Datum plane -H- located at top of parting line and coincident with top of lead. Where lead exits body.

3 Datums D–E and F–G to be determined where center leads exit body at datum plane -H-.

4 To be determined at seating plane -C-.

5 Transition is optional.

6 Square: Details of pin 1 identifier are optional but must be located within one of the two zones indicated.
Rectangle: Details of pin 1 identifier are optional but must be located within zone indicated. If the number of terminals on a side is odd, terminal 1 is the center terminal.

7 Location to datums -A- and -B- to be determined at plane -H-.

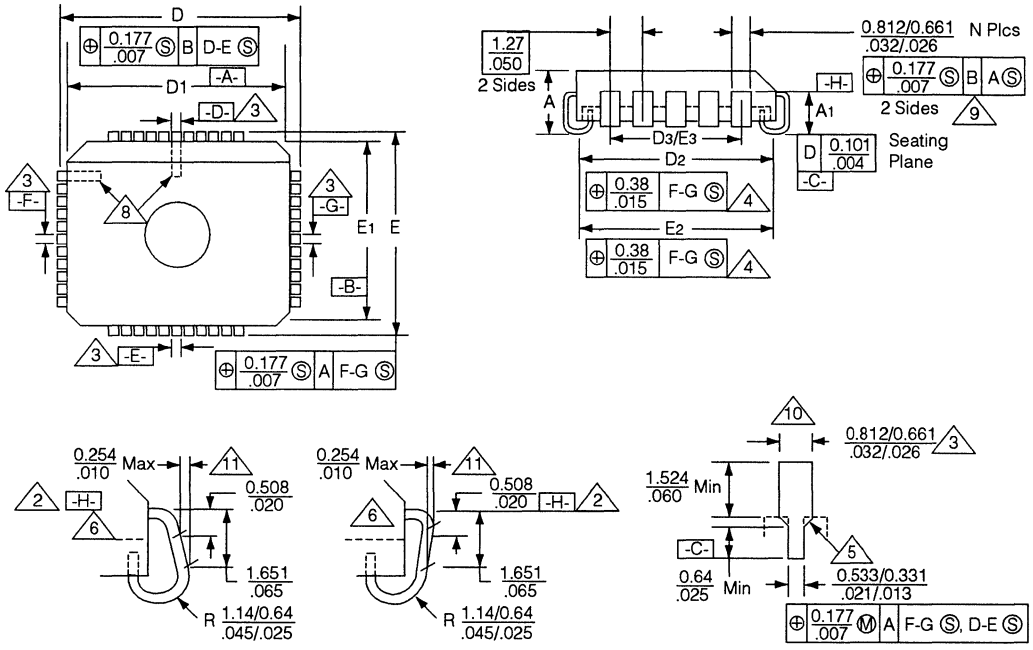
8 All dimensions and tolerances include lead trim offset and lead finish.

9 These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.

10 Controlling dimension: inches.

Packaging Diagrams and Parameters

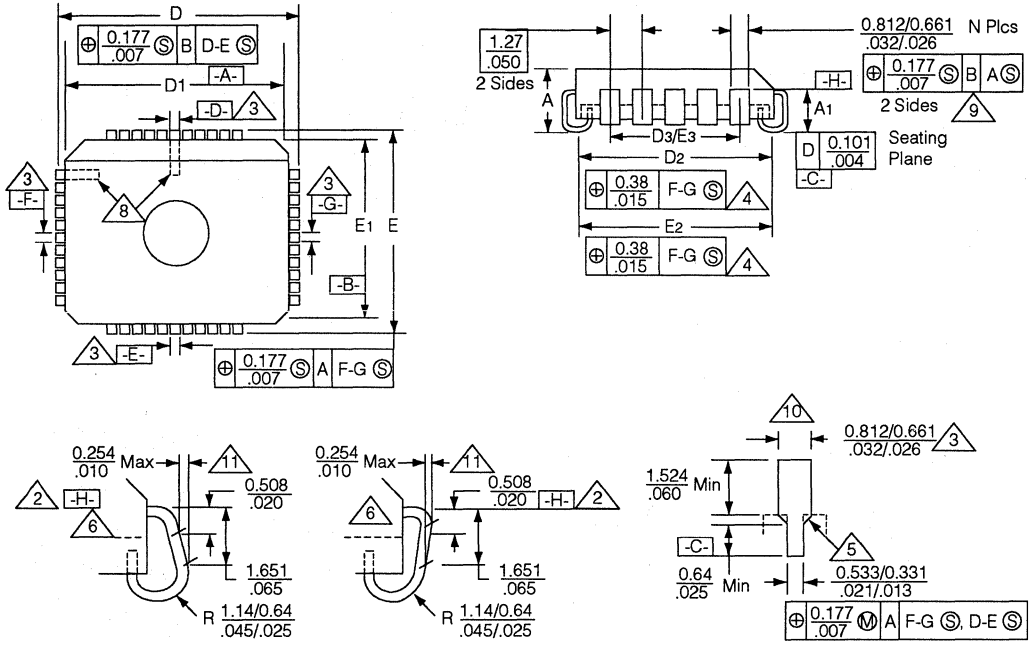
Package Type: 68-Lead Ceramic Leaded Chip Carrier (Window)



Package Group: Ceramic Leaded Chip Carrier (CLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		.165	.185	
A1	2.286	3.048		.090	.120	
D	24.968	25.222		.983	.993	
D1	23.977	24.333		.944	.958	
D2	22.860	23.876		.900	.940	
D3	20.320	-	Reference	.800	-	Reference
E	24.968	25.222		.983	.993	
E1	23.977	24.333		.944	.958	
E2	22.860	23.876		.900	.940	
E3	20.320	-	Reference	.800	-	Reference
N	68	-		68	-	
CP	-	.1016		-	.004	
LT	.1524	.2032		.006	.008	

Packaging Diagrams and Parameters

Package Type: 84-Lead Ceramic Leaded Chip Carrier (Window)



Package Group: Ceramic Leaded Chip Carrier (CLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		.165	.185	
A1	2.286	3.048		.090	.120	
D	30.048	30.353		1.183	1.195	
D1	28.829	29.591		1.135	1.165	
D2	27.940	28.956		1.100	1.140	
D3	25.400	-	Reference	1.000	-	Reference
E	30.048	30.353		1.183	1.195	
E1	28.829	29.591		1.135	1.165	
E2	27.940	28.956		1.100	1.140	
E3	25.400	-	Reference	1.000	-	Reference
N	84	-		84	-	
CP	-	.1016		-	.004	
LT	.1524	.2032		.006	.008	

Packaging Diagrams and Parameters

Plastic Dual In-line Family

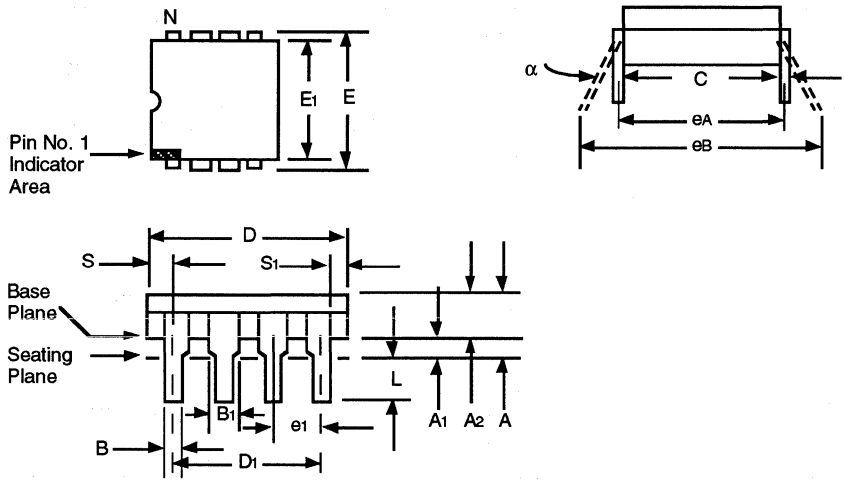
Symbol List for Plastic Dual In-line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
A2	Base body thickness
B	Width of terminal leads
B1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E1	Body width parameters not including leads
eA	Linear spacing of true minimum lead position center line to center line
eB	Linear spacing between true lead position outside of lead to outside of lead
e1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	Total number of potentially usable lead positions
S	Distance from true position center line of No. 1 lead to the extremity of the body
S1	Distance from other end lead edge positions to the extremity of the body

Notes:

1. Controlling parameter: inches.
2. Parameter "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B_1" is nominal.
5. Details of pin Number 1 identifier are optional.
6. Parameters "$D + E_1$" do not include mold flash/protrusions. Mold flash or protrusions shall not exceed .010 inches.

Packaging Diagrams and Parameters

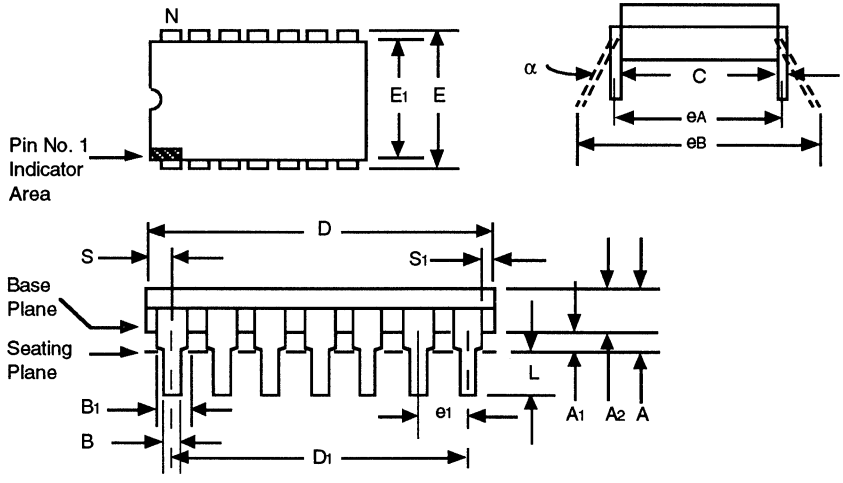
Package Type: 8-Lead Plastic Dual In-line (300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.3556	0.5588		0.014	0.022	
B1	1.397	1.651		0.055	0.065	
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	9.017	10.922		0.355	0.430	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.4892	2.5908	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	8	8		8	8	
S	0.889	–		0.035	–	
S1	0.254	–		0.010	–	

Packaging Diagrams and Parameters

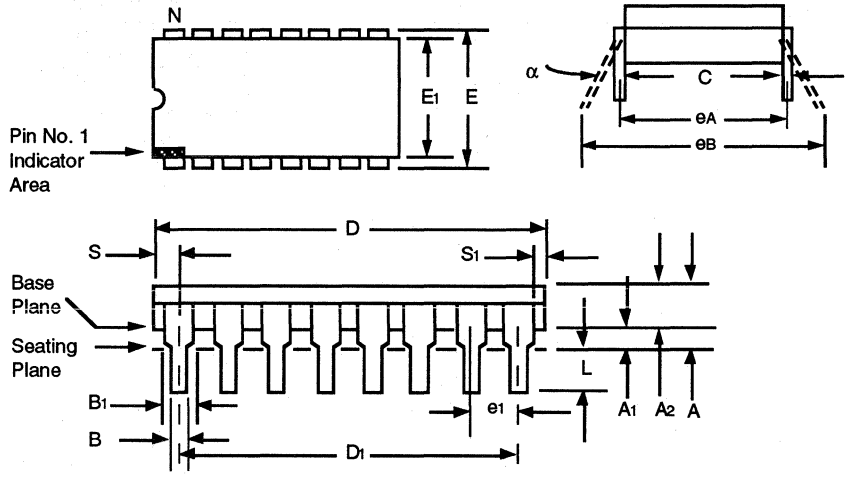
Package Type: 14-Lead Plastic Dual In-line (300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.3556	0.5588		0.014	0.022	
B1	1.524	1.524	Reference	0.060	0.060	Reference
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	18.415	19.431		0.725	0.765	
D1	15.240	15.240	Reference	0.600	0.600	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.4892	2.5908	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	14	14		14	14	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

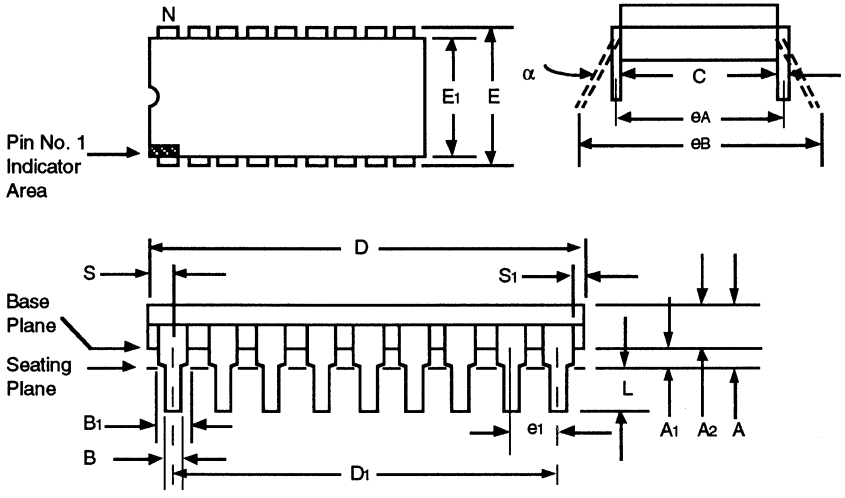
Package Type: 16-Lead Plastic Dual In-line (300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.3556	0.5588		0.014	0.022	
B1	1.524	1.524	Reference	0.060	0.060	Reference
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	18.923	19.939		0.745	0.785	
D1	17.780	17.780	Reference	0.700	0.700	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.4892	2.5908	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.0480	3.556		0.120	0.140	
N	16	16		16	16	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

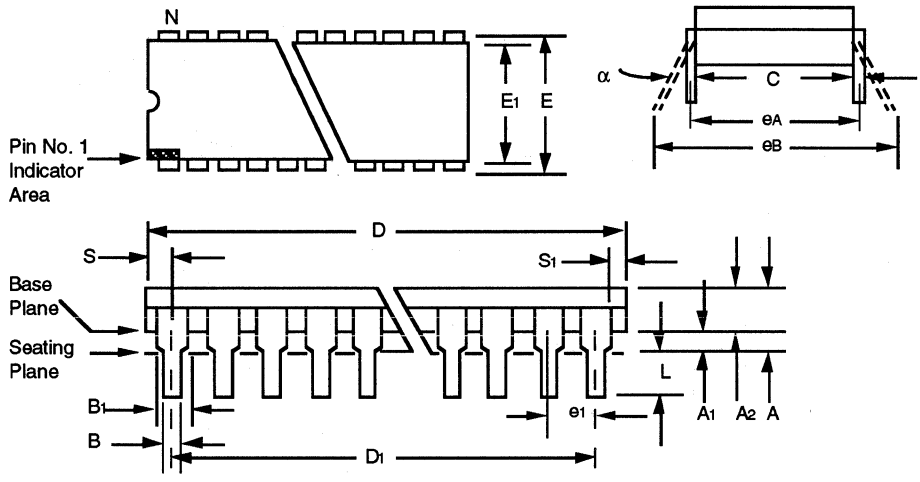
Package Type: 18-Lead Plastic Dual In-line (300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.3556	0.5588		0.014	0.022	
B1	1.524	1.524	Reference	0.060	0.060	Reference
C	0.203	0.381	Typical	0.008	0.015	Typical
D	22.479	23.495		0.885	0.925	
D1	20.320	20.320	Reference	0.800	0.800	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.4892	2.5908	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	18	18		18	18	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

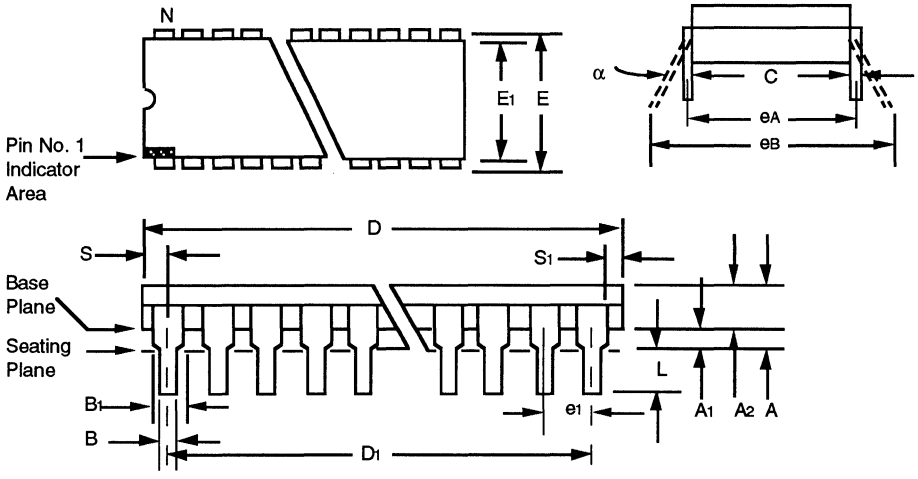
Package Type: 22-Lead Plastic Dual In-line (400 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.572		–	.180	
A1	0.381	–		0.015	–	
A2	3.175	3.810		0.125	0.150	
B	0.3556	0.5588		0.014	0.022	
B1	1.524	1.524	Reference	0.060	0.060	Reference
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	26.670	28.448		1.050	1.120	
D1	25.400	25.400	Reference	1.000	1.000	Reference
E	9.906	10.795		0.390	0.425	
E1	8.382	9.398		0.330	0.370	
e1	2.4892	2.5908	Typical	0.098	0.102	Typical
eA	10.160	10.160	Reference	0.400	0.400	Reference
eB	10.160	12.192		0.400	0.480	
L	3.048	3.556		0.120	0.140	
N	22	22		22	22	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

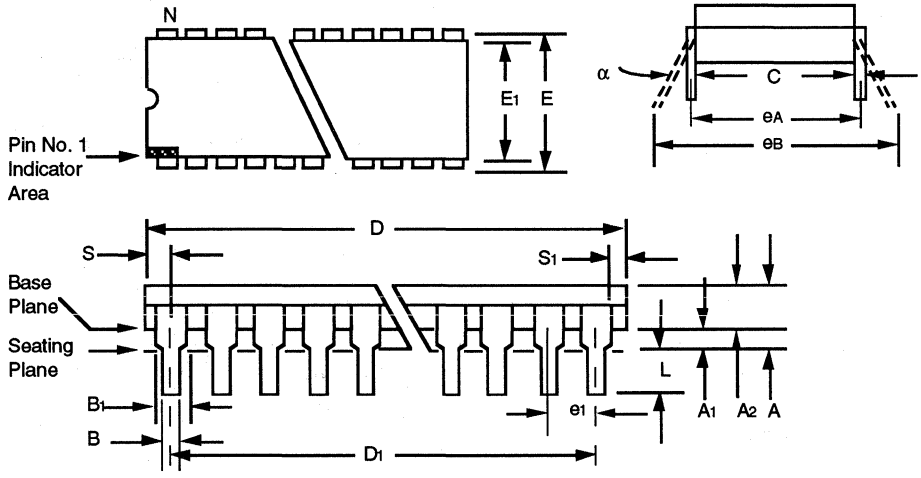
Package Type: 24-Lead Plastic Dual In-line (600 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.508	–		0.020	–	
A2	3.175	4.064		0.125	0.160	
B	0.3556	0.5588		0.014	0.022	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	30.353	32.385		1.195	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	15.240	15.875		0.600	0.625	
E1	12.827	14.224		0.505	0.560	
e1	2.4892	2.5908	Typical	0.098	0.102	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eB	15.494	17.272		0.610	0.680	
L	3.048	3.556		0.120	0.140	
N	24	24		24	24	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

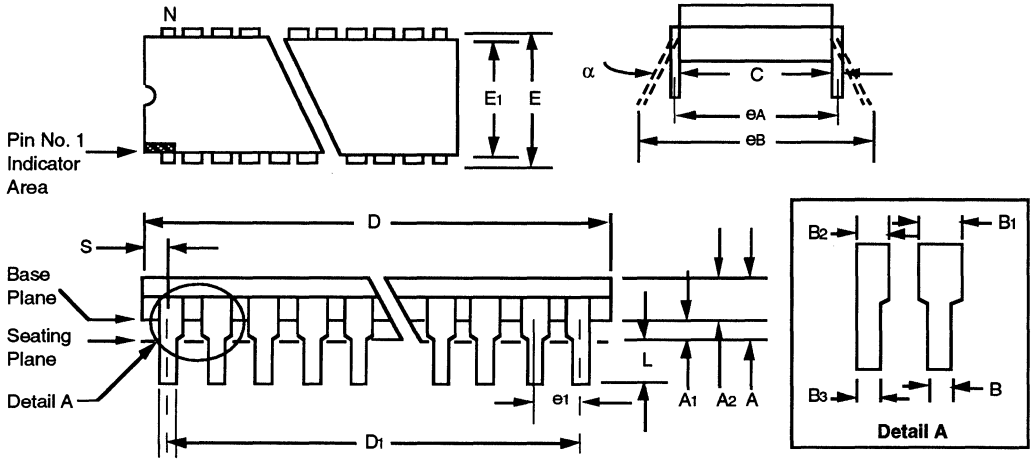
Package Type: 24-Lead Plastic Dual In-line (300 mil)



Package Group: Plastic Dual In-line Package (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.3556	0.5588		0.014	0.022	
B1	1.524	1.524	Typical	0.060	0.060	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	31.242	32.258		1.230	1.270	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.4892	2.5908	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	24	24		24	24	
S	0.889	–		0.035	–	
S1	0.381	–		0.015	–	

Packaging Diagrams and Parameters

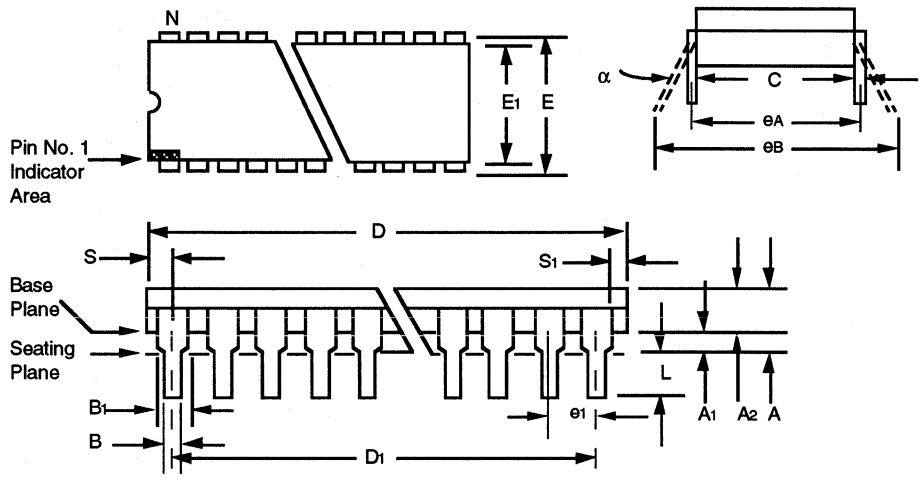
Package Type: 28-Lead Dual In-line Plastic (300 mil)



Package Group: Plastic Dual-In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.6322	4.572		.143	.180	
A1	.381	–		.015	–	
A2	3.175	3.556		.125	.140	
B	.4064	0.5588		.016	.022	Typical
B1	1.016	1.651	Typical	.040	.065	
B2	.762	1.016	4 places	.030	.040	4 places
B3	.2032	.508	4 places	.008	.020	4 places
C	.2032	.3302	Typical	.008	.013	Typical
D	34.163	35.179		1.385	1.395	
D1	33.02	33.02	Reference	1.300	1.300	Reference
E	7.874	8.382		.310	.330	
E1	7.112	7.493		.280	.295	
e1	2.54	2.54	Typical	.100	.100	Typical
eA	7.874	7.874	Reference	.310	.310	Reference
eB	8.128	9.652		.320	.380	
L	3.175	3.683		.125	.145	
N	28	-		28	-	
S	.5842	1.2192		.023	.048	

Packaging Diagrams and Parameters

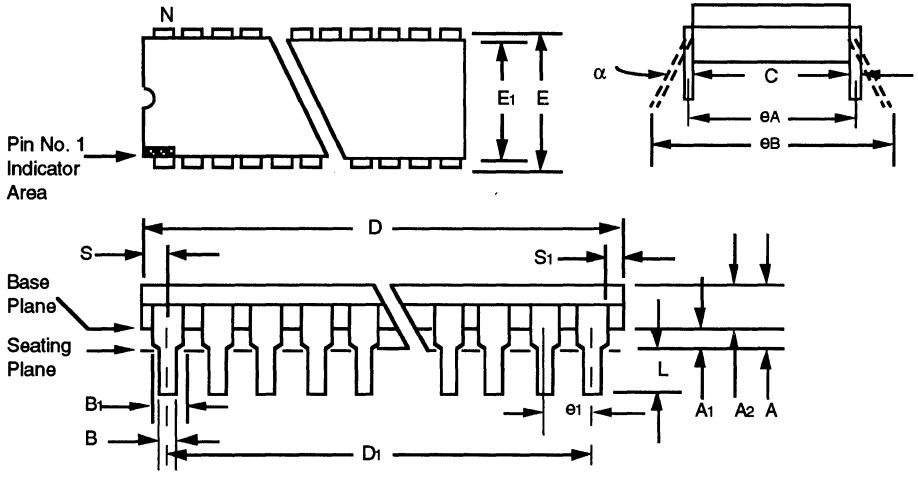
Package Type: 28-Lead Dual In-line Plastic (600 mil)



Package Group: Plastic Dual-In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.508	–		0.020	–	
A2	3.175	4.064		0.125	0.160	
B	0.3556	0.5588		0.014	0.022	
B1	1.270	1.778	Typical	0.050	0.070	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	35.052	37.084		1.380	1.460	
D1	33.020	33.020	Reference	1.300	1.300	Reference
E	15.240	15.875		0.600	0.625	
E1	12.827	13.970		0.505	0.550	
e1	2.4892	2.5908	Typical	0.098	0.102	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	28	28		28	28	
S	0.889	–		0.035	–	
S1	0.508	–		0.020	–	

Packaging Diagrams and Parameters

Package Type: 40-Lead Plastic Dual In-line (600 mil)

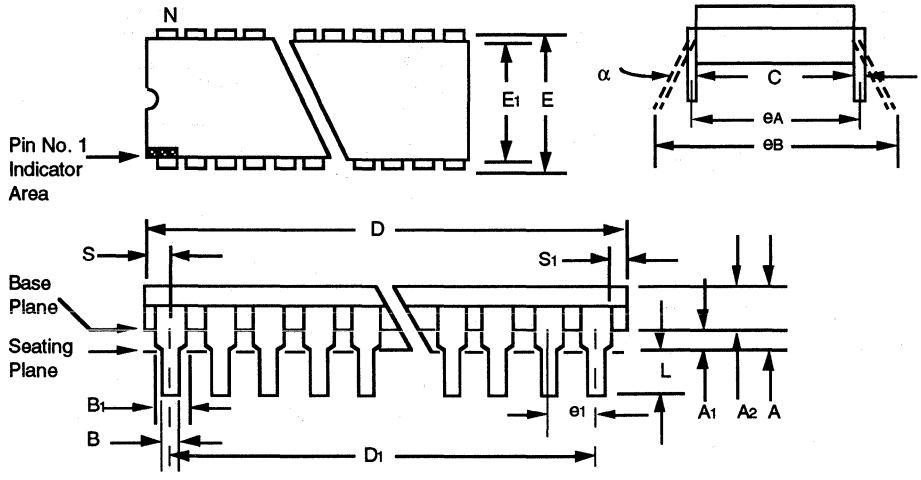


Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.381	–		0.015	–	
A2	3.175	4.064		0.125	0.160	
B	0.3556	0.5588		0.014	0.022	
B1	1.270	1.778	Typical	0.050	0.070	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	51.181	52.197		2.015	2.055	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15.875		0.600	0.625	
E1	13.462	13.970		0.530	0.550	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	40	40		40	40	
S	1.270	–		0.050	–	
S1	0.508	–		0.020	–	

11

Packaging Diagrams and Parameters

Package Type: 48-Lead Plastic Dual In-line (600 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.381	–		0.015	–	
A2	3.175	4.064		0.125	0.160	
B	0.3556	0.5588		0.014	0.022	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	61.468	62.230		2.420	2.450	
D1	58.420	58.420	**Reference**	2.300	2.300	**Reference**
E	15.240	15.875		0.600	0.625	
E1	13.716	14.224		0.540	0.560	
e1	2.4892	2.5908	**Typical**	0.098	0.102	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	48	48		48	48	
S	1.270	–		0.050	–	
S1	0.508	–		0.020	–	

Packaging Diagrams and Parameters

Plastic Leaded Chip Carrier Family

Symbol List for Plastic Leaded Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Distance from seating plane to highest point of body
A1	Distance from lead shoulder to seating plane
CP	Seating plane coplanarity
D/E	Outside dimension
D1/E1	Plastic body dimension
D2/E2	Footprint
D3/E3	Footprint
LT	Lead thickness
N	Total number of potentially usable lead positions
Nd	Total number of leads on short side (rectangular)
Ne	Total number of leads on long side (rectangular)

Notes:

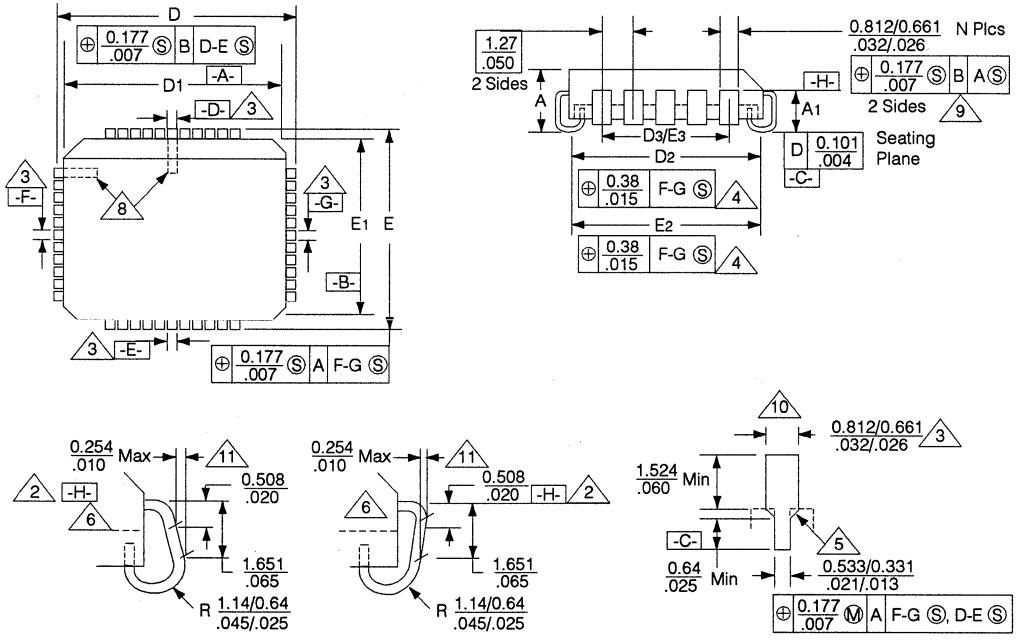
1 All dimensions and tolerances conform to ANSI Y14.5M-1982.
2 Datum plane -H- located at top of mold parting line and coincident with top of lead. Where lead exits plastic body.
3 Datums D–E and F–G to be determined where center leads exit plastic body at datum plane -H-.
4 To be determined at seating plane -C-.
5 Transition is optional.
6 Plastic body details between leads are optional.
7 Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is .254 mm/.010 in. per side. Dimensions D and E include mold mismatch and are determined at parting line.
8 Square: Details of pin 1 identifier are optional but must be located within one of the two zones indicated.
Rectangle: Details of pin 1 identifier are optional but must be located within zone indicated. If the number of terminals on a side is odd, terminal 1 is the center terminal.
9 Location to datums -A- and -B- to be determined at plane -H-.
10 All dimensions and tolerances include lead trim offset and lead finish.
11 These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
12 Controlling dimension: inches.

X Sum of dam bar protrusions to be 0.17 (.007) max per lead.

Y Feature is not required, but is optional at manufacturer's discretion.

Packaging Diagrams and Parameters

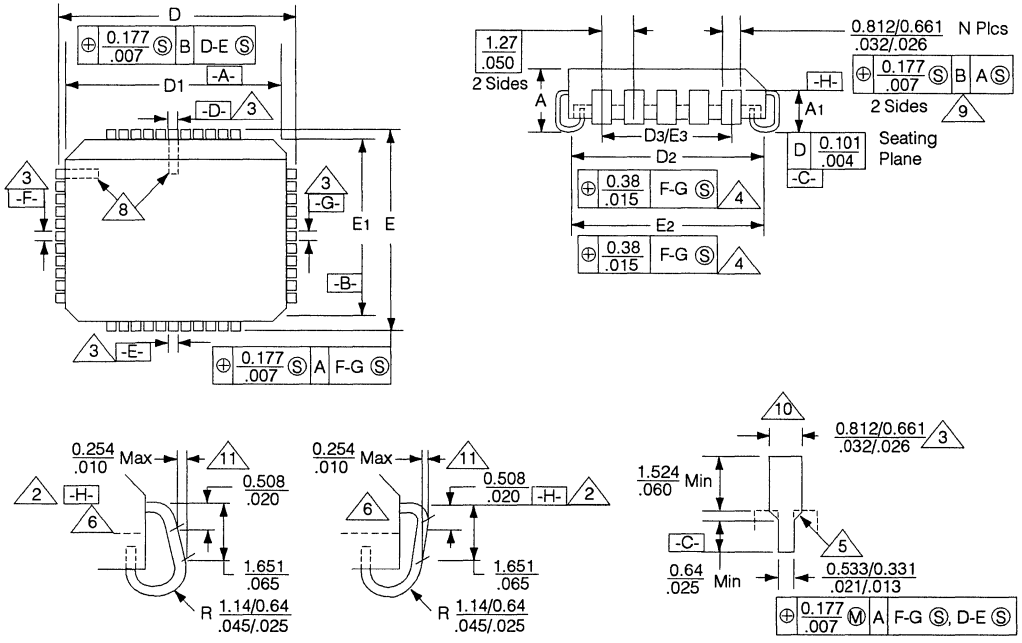
Package Type: 28-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A1	2.413	2.921		0.095	0.115	
D	12.319	12.573		0.485	0.495	
D1	11.430	11.5824		0.450	0.456	
D2	10.414	10.922		0.410	0.430	
D3	7.620	7.620	Reference	0.300	0.300	Reference
E	12.319	12.573		0.485	0.495	
E1	11.430	11.5824		0.450	0.456	
E2	10.414	10.922		0.410	0.430	
E3	7.620	7.620	Reference	0.300	0.300	Reference
N	28	28		28	28	
CP	–	0.1016		–	0.004	
LT	0.2032	0.381		0.008	0.015	

Packaging Diagrams and Parameters

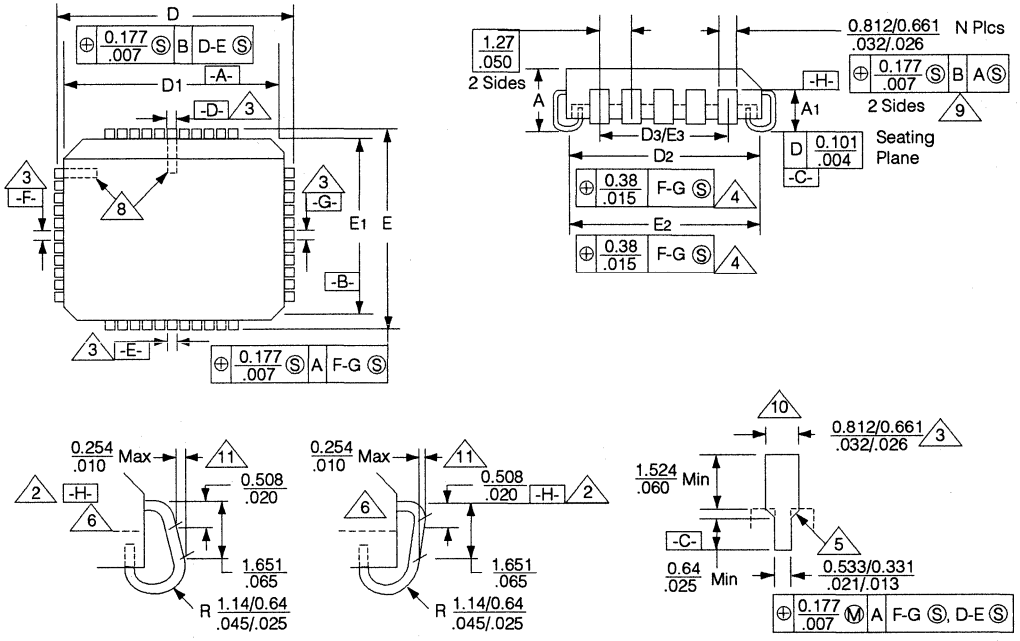
Package Type: 32-Lead Plastic Leaded Chip Carrier (Rectangle)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.048	3.556		0.120	0.140	
A1	1.905	2.413		0.075	0.095	
D	12.319	12.573		0.485	0.495	
D1	11.3538	11.5062		0.447	0.453	
D2	4.826	5.334		0.190	0.210	
D3	7.620	7.620	Reference	0.300	0.300	Reference
E	14.859	15.113		0.585	0.595	
E1	13.8938	14.0462		0.547	0.553	
E2	6.096	6.858		0.240	0.270	
E3	10.160	10.160	Reference	0.400	0.400	Reference
N	32	32		32	32	
Nd	7	7		7	7	
Ne	9	9		9	9	
CP	–	0.1016		–	0.004	
LT	0.2032	0.381		0.008	0.015	

Packaging Diagrams and Parameters

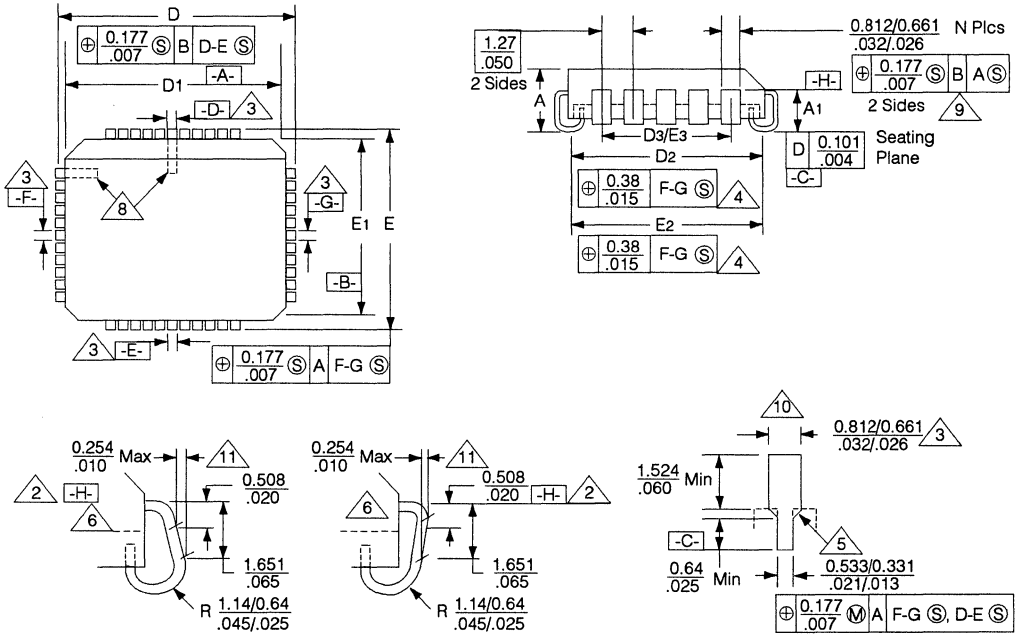
Package Type: 44-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A_1	2.413	2.921		0.095	0.115	
D	17.399	17.653		0.685	0.695	
D_1	16.510	16.6624		0.650	0.656	
D_2	15.494	16.002		0.610	0.630	
D_3	12.700	12.700	Reference	0.500	0.500	Reference
E	17.399	17.653		0.685	0.695	
E_1	16.510	16.6624		0.650	0.656	
E_2	15.494	16.002		0.610	0.630	
E_3	12.700	12.700	Reference	0.500	0.500	Reference
N	44	44		44	44	
CP	–	0.1016		–	0.004	
LT	0.203	0.381		0.008	0.015	

Packaging Diagrams and Parameters

Package Type: 68-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		.165	.185	
A1	2.286	2.794		.090	.110	
D	25.019	25.273		.985	.995	
D1	24.130	24.3332		.950	.958	
D2	22.860	23.622		.900	.930	
D3	20.320	-	Reference	.800	-	Reference
E	25.019	25.273		.985	.995	
E1	24.130	24.3332		.950	.958	
E2	22.860	23.622		.900	.930	
E3	20.320	-	Reference	.800	-	Reference
N	68	-		68	-	
CP	-	.1016		-	.004	
LT	.2032	.254		0.008	0.010	

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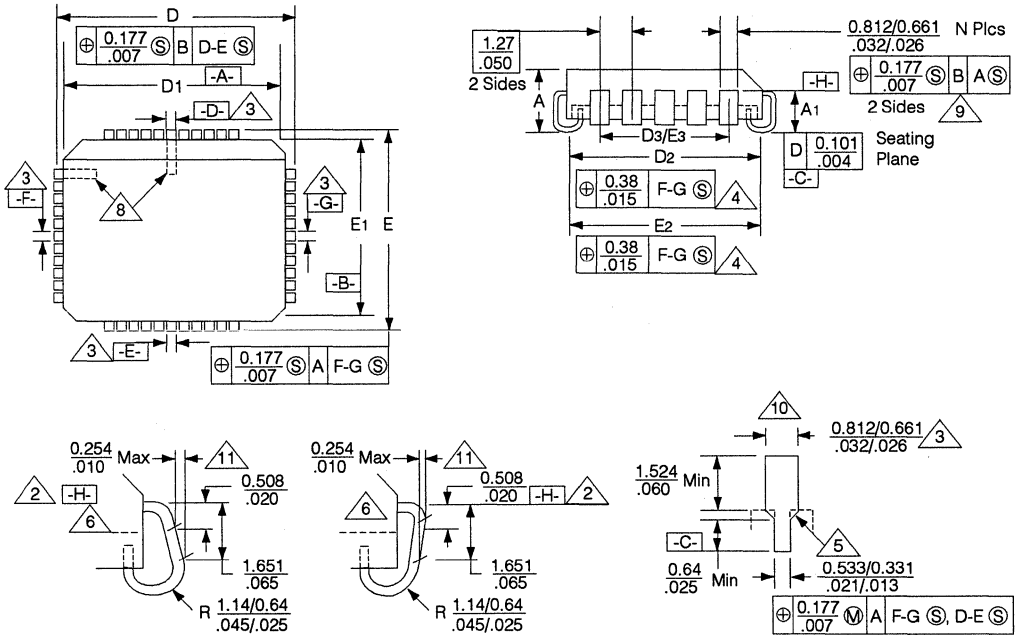
Packaging Diagrams and Parameters

Package Type: 84-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		.165	.185	
A1	2.286	2.794		.090	.110	
D	30.099	30.353		1.185	1.195	
D1	29.210	29.4132		1.150	1.158	
D2	27.940	28.702		1.100	1.130	
D3	25.400	-	Reference	1.000	-	Reference
E	30.099	30.353		1.185	1.195	
E1	29.210	29.4132		1.150	1.158	
E2	27.940	28.702		1.100	1.130	
E3	25.400	-	Reference	1.000	-	Reference
N	84	-		84	-	
CP	-	.1016		-	.004	
LT	.2032	.254		.008	.010	

Packaging Diagrams and Parameters

Plastic Small Outline Family

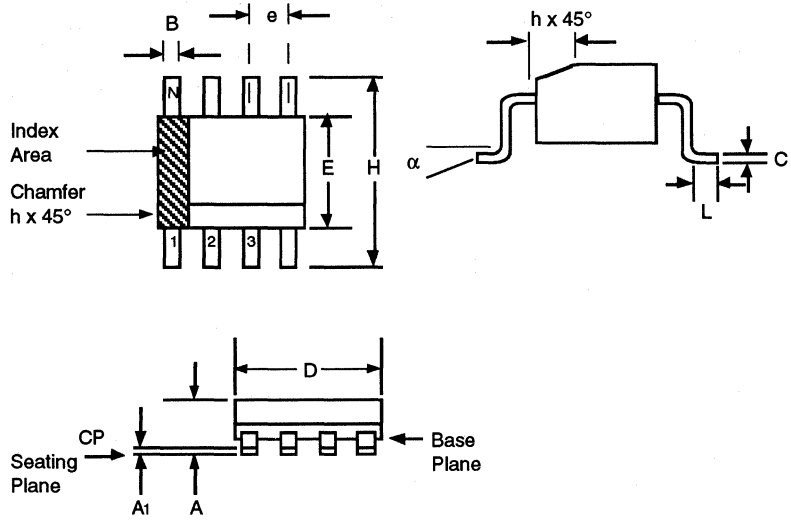
Symbol List for Small Outline Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
N	Total number of potentially usable lead positions
CP	Seating plane coplanarity

Notes:

1. Controlling parameter: inches.
2. All packages are gull wing lead form.
3. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .006 package ends and .010 on sides.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area to indicate pin 1 position.
5. Terminal numbers are shown for reference.

Packaging Diagrams and Parameters

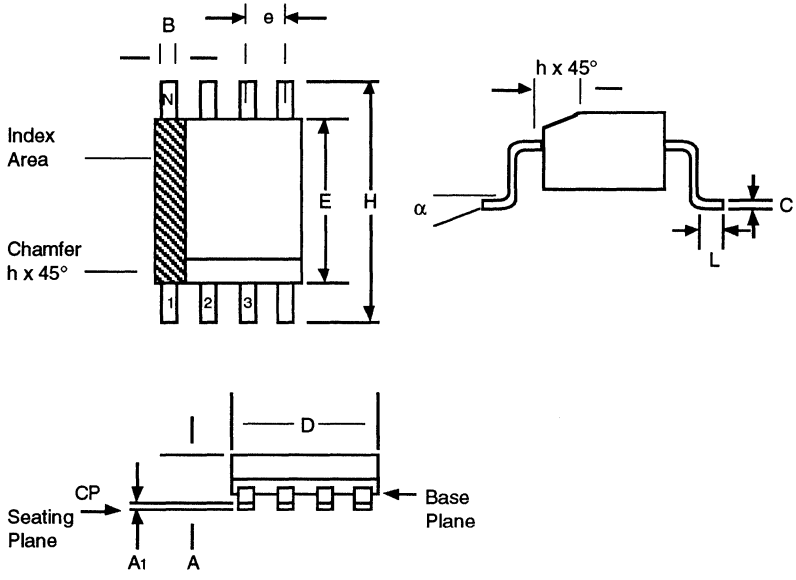
Package Type: 8-Lead Plastic Surface Mount (SOIC - Narrow, 150 mil Body)



Package Group: Plastic SOIC (SN)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.3716	1.7272		0.054	0.068	
A1	0.1016	0.24892		0.004	0.0098	
B	0.3556	0.4826		0.014	0.019	
C	0.1905	0.24892		0.0075	0.0098	
D	4.8006	4.9784		0.189	0.196	
E	3.810	3.9878		0.150	0.157	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	5.8166	6.1976		0.229	0.244	
h	0.381	0.762		0.015	0.030	
L	0.508	1.016		0.020	0.040	
N	8	8		8	8	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

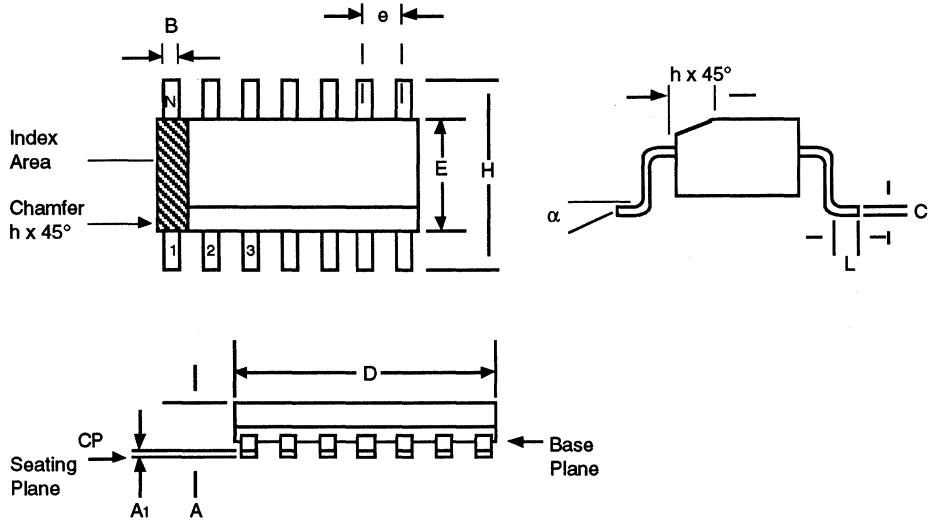
Package Type: 8-Lead Plastic Surface Mount (SOIC - Medium, 200 mil Body)



Package Group: Plastic SOIC (SM)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.778	2.032		0.070	0.080	
A1	0.1016	0.24892		0.004	0.0098	
B	0.3556	0.4826		0.014	0.019	
C	0.1905	0.24892		0.0075	0.0098	
D	5.08	5.334		0.200	0.210	
E	5.1562	5.4102		0.203	0.213	
e	1.270	1.270	Reference	0.050	0.050	Reference
H	7.62	8.382		0.300	0.330	
h	0.381	0.762		0.015	0.030	
L	0.508	1.016		0.020	0.040	
N	14	14		14	14	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

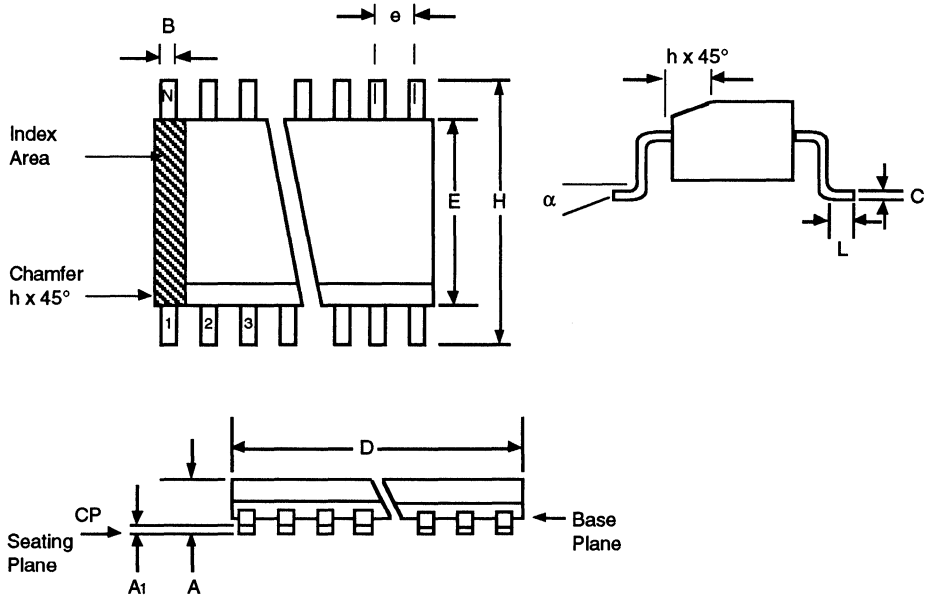
Package Type: 14-Lead Plastic Surface Mount (SOIC - Narrow, 150 mil Body)



Package Group: Plastic SOIC (SL)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.3716	1.7272		0.054	0.068	
A1	0.1016	0.24892		0.004	0.0098	
B	0.3556	0.4826		0.014	0.019	
C	0.1905	0.24892		0.0075	0.0098	
D	8.5598	9.9822		0.337	0.393	
E	3.810	3.9878		0.150	0.157	
e	1.270	1.270	Reference	0.050	0.050	Reference
H	5.8166	6.1976		0.229	0.244	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	14	14		16	16	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

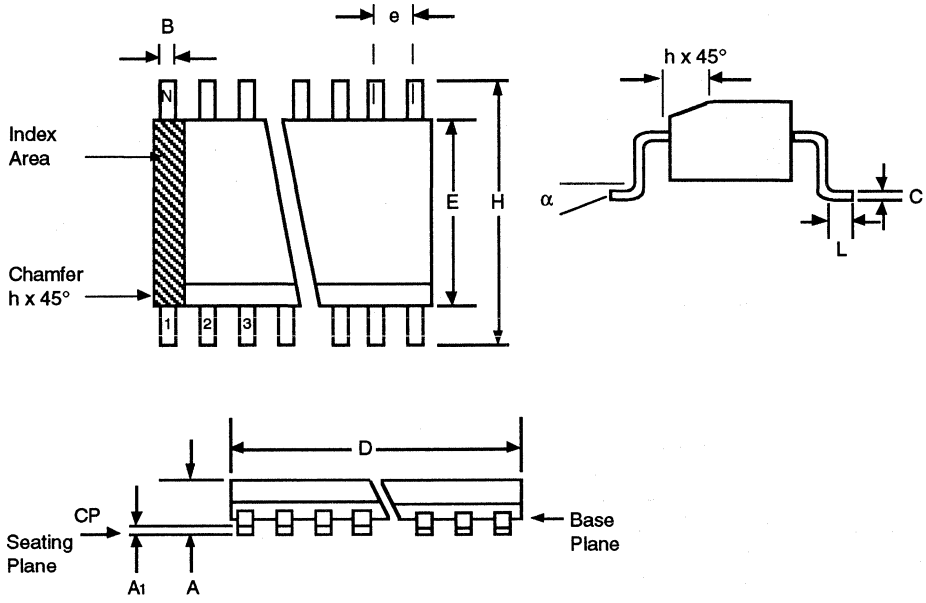
Package Type: 18-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A_1	0.1016	0.29972		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	11.3538	11.7348		0.447	0.462	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Reference	0.050	0.050	Reference
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	18	18		18	18	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

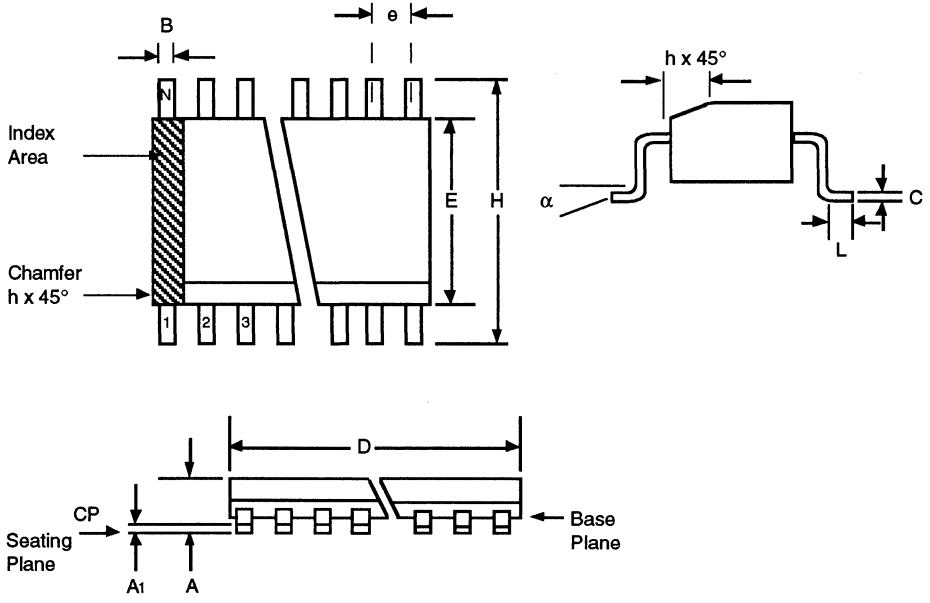
Package Type: 24-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A1	0.1016	0.29972		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	15.2146	15.5956		0.599	0.614	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Reference	0.050	0.050	Reference
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	24	24		24	24	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

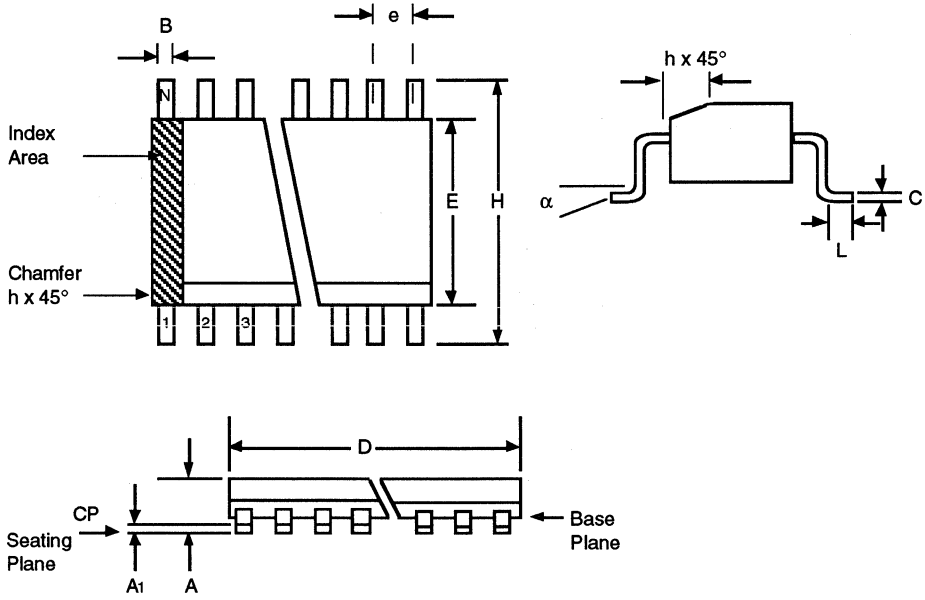
Package Type: 28-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	17.7038	18.0848		0.697	0.712	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	28	28		28	28	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Surface Mount (SOIC - Wide, 330 mil Body)



Package Group: Plastic SOIC (SW)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0	8°		0	8°	
A	2.286	2.6416		.090	.104	
A1	0.1016	0.2794		.004	.011	
B	0.3556	0.508		.014	.020	
C	0.2286	0.3048		.009	.012	
D	17.780	18.0848		.700	.712	
E	8.636	8.890		.340	.350	
e	1.27	1.27	Reference	.050	.050	Reference
H	11.7602	12.1158		.463	.477	
h	0.254	0.7366		.010	.029	
L	0.508	1.0668		.020	.042	
N	28	28		28	28	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

Plastic Shrink Small Outline Family

Symbol List for Shrink Small Outline Package Parameter	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
N	Total number of potentially usable lead positions
CP	Seating plane coplanarity

Notes: 1. Controlling parameter: mm.

2. All packages are gull wing lead form.

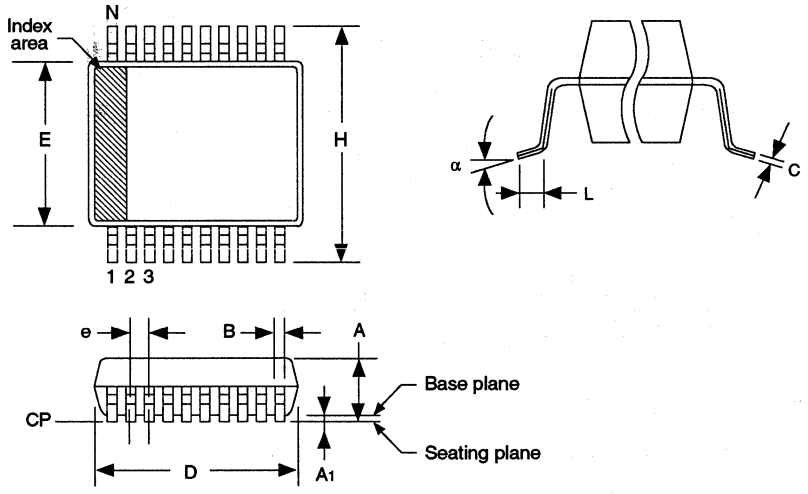
3. "D" and "E" are reference datums and do not include mold flash or protrusions.
Mold flash or protrusions shall not exceed 0.15mm .006 package ends and .010" on sides.

4. A .25mm visual index feature must be located within the crosshatched area to indicate pin 1 position.

5. Terminal numbers are shown for reference.

Packaging Diagrams and Parameters

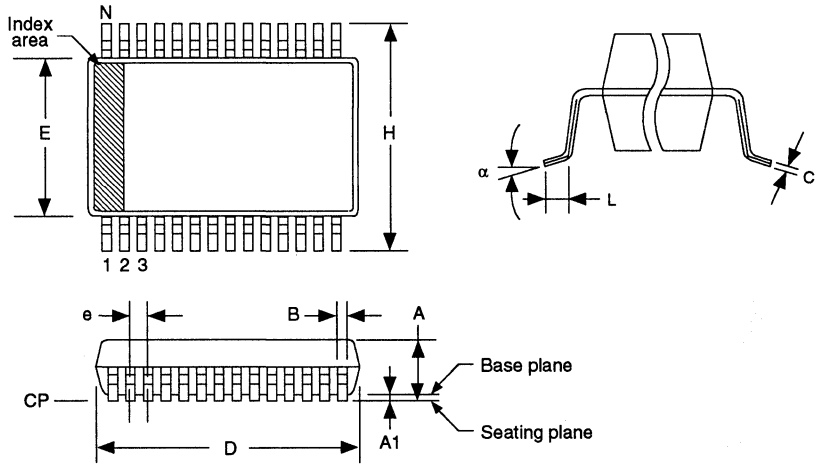
Package Type: 20-Lead Plastic Surface Mount (SSOP - 209 mil Body 5.30mm)



Package Group: Plastic SSOP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.73	1.99		0.068	0.078	
A_1	0.05	0.21		0.002	0.008	
B	0.25	0.38		0.010	0.015	
C	0.13	0.22		0.005	0.009	
D	7.07	7.33		0.278	0.289	
E	5.20	5.38		0.205	0.212	
e	0.65	0.65	Reference	0.0256	0.0256	Reference
H	7.65	7.90		0.301	0.311	
L	0.55	0.95		0.022	0.037	
N	20	20		20	20	
CP	-	0.1016		-	0.004	

Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Surface Mount (SSOP - 209 mil Body 5.30mm)



Package Group: Plastic SSOP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.73	1.99		0.068	0.078	
A_1	0.05	0.21		0.002	0.008	
B	0.25	0.38		0.010	0.015	
C	0.13	0.22		0.005	0.009	
D	10.07	10.33		0.396	0.407	
E	5.20	5.38		0.205	0.212	
e	0.65	0.65	Reference	0.0256	0.0256	Reference
H	7.65	7.90		0.301	0.311	
L	0.55	0.95		0.022	0.037	
N	28	28		28	28	
CP	-	0.1016		-	0.004	

Packaging Diagrams and Parameters

Plastic Thin Small Outline and Very Small Outline Families (TSOP, VSOP)

Symbol List for Thin Small Outline Package Parameter	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the guage plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
N	Total number of potentially useable lead positions
CP	Seating plane coplanarity

Notes: 1. Controlling parameter: inches.

2. All packages are gull wing lead form.

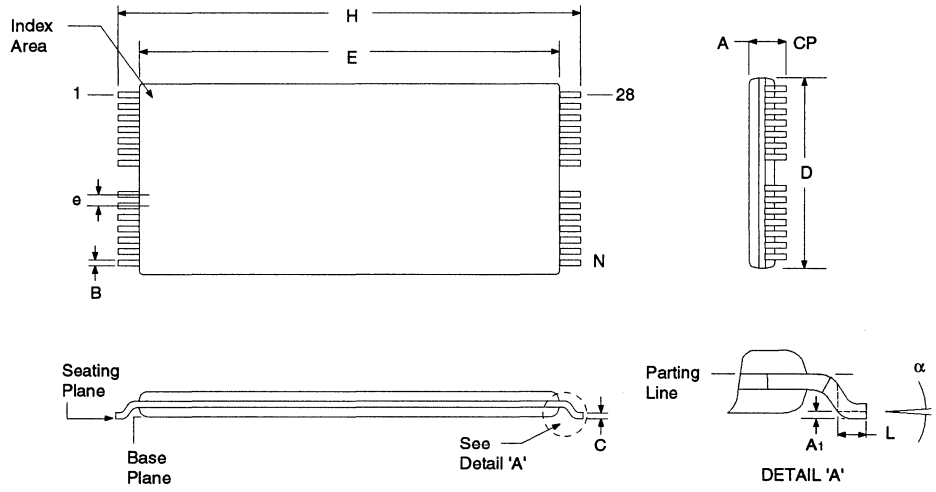
3. "D" and "E" are reference datums and do not include mold flash or protrusions.
Mold flash or protrusions shall not exceed .005 per side.

4. A visual index feature must be located within the crosshatched area to indicate pin 1 position.

5. Terminal numbers are shown for reference.

Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Surface Mount (TSOP 8 x 20mm)

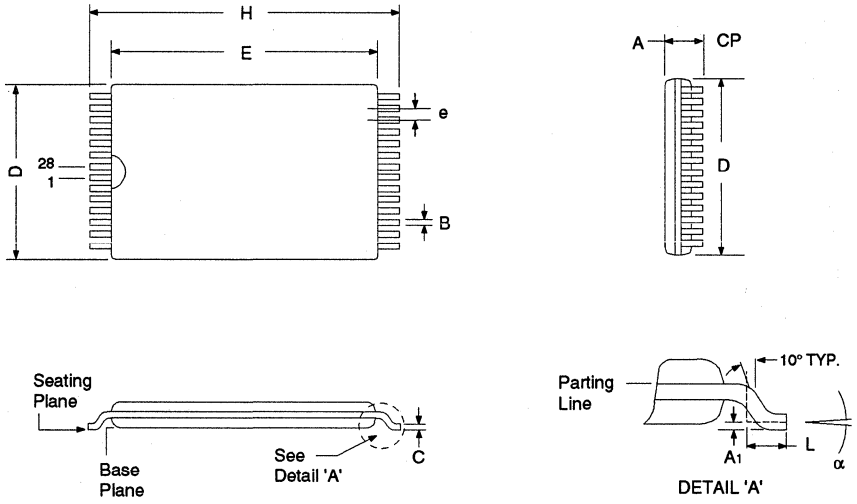


Package Group: Plastic TSOP (TS)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0	8°		0	8°	
A	-	1.19		-	.047	
A_1	0.00	0.15		.000	.006	
B	0.15	0.25		.006	.010	
C	0.10	0.20		.004	.008	
D	7.80	8.20		.307	.323	
E	18.29	18.49		.720	.728	
e	.51	-	Reference	.020	-	Reference
H	19.81	20.19		.780	.795	
	-	-		-	-	
L	0.41	0.61		.016	.024	
N	28	28		28	28	
CP	-	0.1016		-	.004	

11

Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Surface Mount (VSOP 8 x 13mm)



Package Group: Plastic VSOP (VS)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0	8°		0	8°	
A	-	1.25		-	.049	
A_1	0.00	0.15		.000	.006	
B	0.15	0.30		.006	.012	
C	0.13	0.22		.005	.0086	
D	7.90	8.10		.311	.319	
E	11.70	11.90		.461	.469	
e	.55	-	Reference	.022	-	Reference
H	13.10	13.70		.516	.539	
	-	-		-	-	
L	0.30	0.70		.012	.027	
CP	-	0.1016		-	.004	

Packaging Diagrams and Parameters

Plastic Metric Quad Flatpack Family (MQFP)

Symbol List for Metric Plastic Quad Flat Pack Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min and max lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body
b	Width of terminals
C	Thickness of terminals
D_1/E_1	Largest overall package parameter including leads
D/E	Largest overall package parameter including leads
D_3/E_3	Center of end lead to center of end lead
e	Linear spacing of true minimum lead position center line to center line
L	Length of terminal for soldering to a substrate
N	Total number of potentially usable lead positions
CP	Seating plane coplanarity

Notes

1. All dimensioning and tolerancing conform to ANSI Y14, BM-1582.
2. Datum Plane -H- is located at bottom of hold parting line and coincident with bottom of lead, where lead exits body.
3. Datums A-B and -D- to be determined at Datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include hold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 do not include hold mismatch and are determined at Datum Plane -H-.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. These dimensions to be determined at Datum plane -H-.
8. All dimensions in millimeters.
9. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot.
10. Exact shape of this feature is optional.
11. N is the number of leads.
12. Controlling parameters: millimeters
13. All packages are gull wing lead form.

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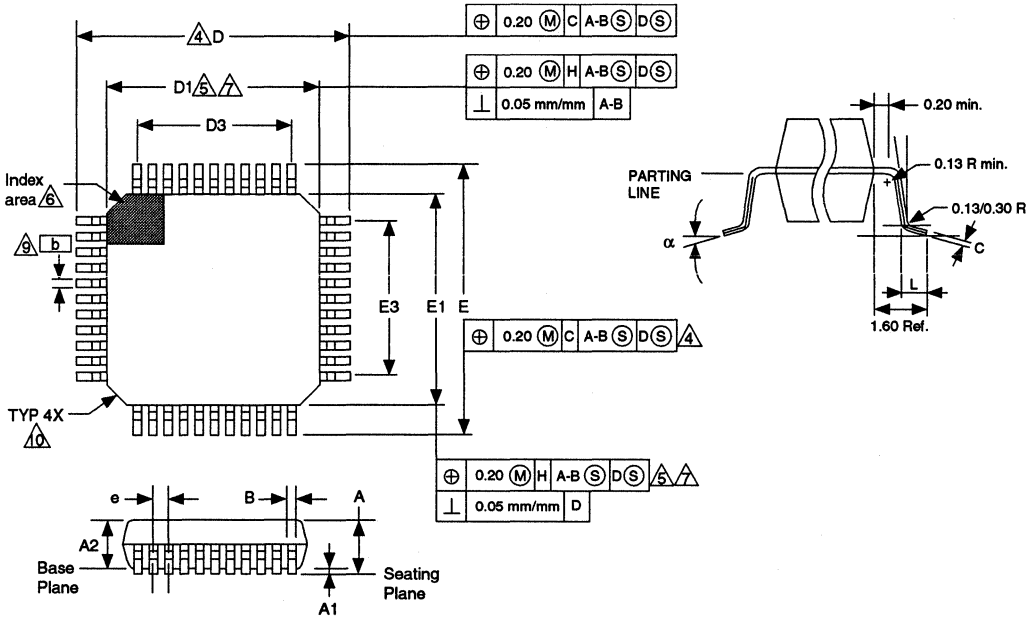
Packaging Diagrams and Parameters

Package Type: 44-Lead Plastic Surface Mount (MQFP 10x10mm Body 1.6/0.15mm Lead Form)



Package Group: Plastic MQFP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	7°		0°	7°	
A	2.00	2.35		0.0787	0.0925	
A_1	0.05	0.25		0.0020	0.0098	
A_2	1.95	2.10		0.768	0.0827	
b	0.30	0.45	Typical	0.0118	0.0177	Typical
C	0.15	0.18		.006	.007	
D	12.95	13.45		0.510	0.530	
D_1	9.90	10.10		0.390	0.398	
D_3	8.00	8.00	Reference	0.315	0.315	Reference
E	12.95	13.45		0.510	0.530	
E_1	9.90	10.10		0.390	0.398	
E_3	8.00	8.00	Reference	.315	.315	Reference
e	0.80	0.80		.0315	.0315	
L	0.73	1.03		.0287	.0406	
N	44	44		44	44	
CP	0.102			.004		

MICROCHIP

Devices in Die/Wafer Form - Non-Volatile Memory

INTRODUCTION

Microchip Technology Inc.'s non-volatile memory devices are available in wafer form and in die form. All products sold as die or wafers have been characterized and qualified according to the requirements of Microchip Technology Inc. Specifications SPI-41014, "Characterization and Qualification of Integrated Circuits", and QCI-39000, "Worldwide Quality Conformance Requirements".

PRODUCT INTEGRITY

Product supplied in die or wafer form will be 100 percent visually inspected to the criteria defined in Microchip Technology Inc. Specification, QCI-30014, "Standard Visual Inspection Procedure of Dice Prior to Assembly for Commercial Products"

Die/Wafer thickness is 18 mils or 21 mils depending on product.

Wafers at reduced thicknesses are also available.

CAUTION

Some EEPROM products use EEPROM cells for device configuration. Exposure to ultra-violet light or x-rays must be avoided. Exposure to ultra-violet light or x-rays may cause the device to operate improperly.

These products are susceptible to damage from electrostatic discharge. Extreme care is urged in the handling and assembly of these products.

BONDABILITY OF DIE TO SUBSTRATE

Dice are capable of bonding either by using a gold eutectic bond to a gold plated pedestal containing 60 micro-inches of gold, or by using an electrically conductive adhesive (e.g. epoxy) to any substrate.

BONDABILITY OF WIRES TO DIE

Dice shall be capable of thermosonic gold or ultrasonic wire bonding such that the minimum conditions of MIL-STD 883, Method 2011 on "Bond Strength (Destructive Bond pull Test)" are met.

PAD METALLIZATION

Pad metallization is silicon doped aluminum.

BACK SIDE PREPARATION

Die and wafer back sides are backlapped and are without any gold coating.

ELECTRICAL

Dice are guaranteed to fully meet data sheet specifications at the commercial temperature range of 0°C to 70°C.

The die back side is grounded through contacts internal to the part. Thus, it is permitted to float the die mounting surface. It is recommended that the die mounting surface be grounded in multi-chip assemblies.

PACKAGING

Die shipped by Microchip Technology Inc. are placed in a "waffle pack" with sufficient cavity area to restrain the die while maintaining their orientation. Lint free paper inserts are placed over the waffle packs and each pack is secured with a plastic locking clip. Groups of waffle packs are assembled into sets for shipment. A label with lot number, quantity, part number and packing date is placed on each waffle pack.

Wafers shipped by Microchip Technology Inc. are separated by lint free paper and dry packed in a shipping container of appropriate size which is labeled with lot number, quantity, part number and packing date.

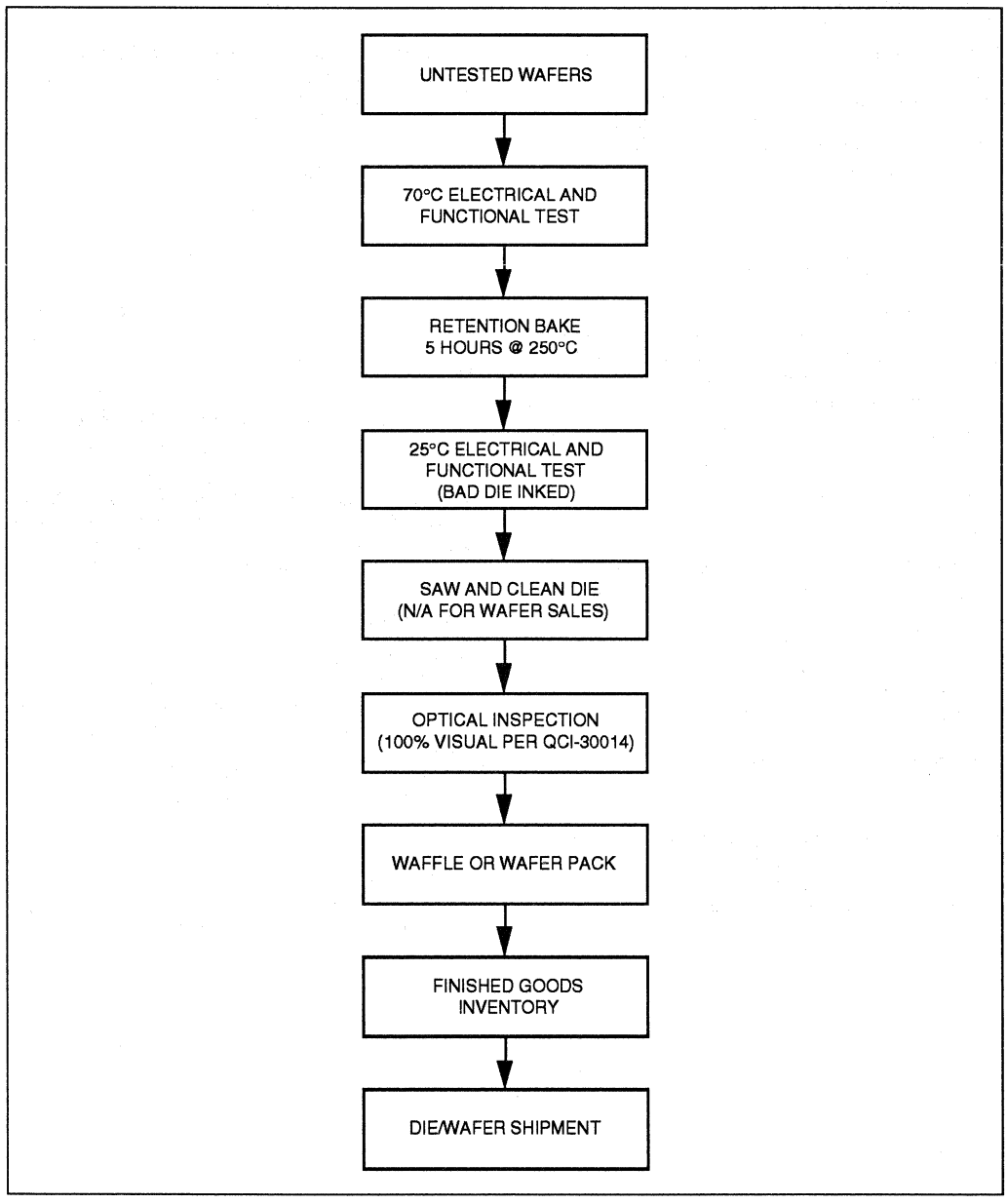
DIE/WAFER PRODUCT OFFERING

All Microchip Technology Inc.'s serial EEPROMs, parallel EEPROMs and EPROMS are available in die or wafer form in the commercial temperature range of 0°C to 70°C. Part number suffixes of /s and /w are used to designate devices in die and wafer form, respectively.

TEST FLOW

All Microchip Technology Inc.'s die products are subjected to functional and parametric testing at the wafer level. The typical EEPROM test flow is shown in Figure 1.

FIGURE 1 - EEPROM TEST FLOW



SECTION 12
OFFICE LOCATIONS

Factory Representatives

12

ASIA

Hong Kong

Memec (Asia Pacific) Ltd.
Unit No. 2520-2525
Tower 1, Metroplaza
Hing Fong Road, Kwai Fong
N.T., Hong Kong
Tel: 852 410 2760
Fax: 852 418 1600

Korea

Memec (Asia Pacific) Ltd.
JE Woong Bldg. Third Floor
176-11 Nonhyum-Dong
Kangnam-ku
Seoul, Korea
Tel: 82 2 518 8181
Fax: 82 2 518 9419

Singapore

Memec (Asia Pacific) Ltd.
Singapore Representative Office
10 Anson Road #14-02
International Plaza
Singapore 0207
Tel: 65 222 4962
Fax: 65 222 4939

Taiwan

Memec (Asia Pacific) Ltd.
14F-1, No. 171, Sec. 5,
Min Sheng East Road
Hai Hwa Bldg.
Taipei, Taiwan
Tel: 886 2 7602028
Fax: 886 2 7651488

CANADA

Alberta

Enerlec Sales, Ltd.
37 Evergreen Terrace
Calgary, Alb. T2Y 2V9
Tel: 403 256 3627
Fax: 403 254 9121

British Columbia

Enerlec Sales, Ltd.
3671 Viking Way #7
Richmond, B.C. V6V 1W1
Tel: 604 273 0882
Fax: 604 273 0884

Ontario

Dynasty Components, Inc.
1140 Morrison Drive - Unit 110
Ottawa, Ontario K2H 859
Tel: 613 596 9800
Fax: 613 596 9886

Dynasty Components, Inc.
357 Hillsdale Avenue, E.
Toronto, Ontario M4S 1T9
Tel: 416 587 2278
Fax: 416 489 3527

Quebec

Dynasty Components, Inc.
1870 Blvd. des Sources, # 304
Pointe Claire, P.Q. H9R 5N4
Tel: 514 984 5342
Fax: 514 694 6826

EUROPE

Ireland

Eltech Agencies Ltd.
27 Maccurtain Street
Cork
Tel: 353 21 509366
Fax: 353 21 509344

MEXICO

CompTech de Mexico
An Morelos Sur 882
Col Centro
Cuernavaca, Morelos
CP62000 Mexico
Tel: 52 73 122733, 52 73 142864
52 73 183572
Fax: 52 73 126368

Electronica Seta, S.A. de C.V.
Galeana No. 114-20 Piso
La Loma, Tlalnepantla
54060 Edo. de Mexico
Tel: 390 77 13, 390 82 87,
390 44 91, 390 85 26,
390 58 95
Fax: 390 94 68

Semiconductores Profesionales
Madrid No. 55
Col. Del Carmen Coyoacan
04100 Mexico, D.F.
Tel: 658 60 11, 658 67 80,
658 36 61, 659 47 56
Fax: 658 60 44

SOUTH AMERICA

Argentina

Ibars Electronic Corporation
7760 W. 20th Avenue
Suite 2
Hialeah, FL 33016 U.S.A.
Tel: 305 557 6305/06
Fax: 305 557 7429

Brazil

Aplicacoes Eletronicas Artimar Ltda.
Rua Marques De Itu, 70-10 And.
Caixa Postal 5881 e 9498
CEP 01223 - Sao Paulo, Brazil
Tel: 231 0277
Fax: 255 0511

Columbia

Ibars Electronic Corporation
7760 W. 20th Avenue
Suite 2
Hialeah, FL 33016 U.S.A.
Tel: 305 557 6305/06
Fax: 305 557 7429

Venezula

Ibars Electronic Corporation
7760 W. 20th Avenue
Suite 2
Hialeah, FL 33016 U.S.A.
Tel: 305 557 6305/06
Fax: 305 557 7429

USA

Alabama

Electramark, Inc.
500 Wynn Drive, Suite 521
Huntsville, AL 35816
Tel: 205 830 4400
Fax: 205 830 4406

Arizona

Western High Tech Marketing, Inc.
9414 E. San Salvador, Suite 206
Scottsdale, AZ 85258
Tel: 602 860 2702
Fax: 602 860 2712

Arkansas

CompTech Sales, Inc.
18700 Woodbriar Lane
Catoosa, OK 74015
Tel: 918 266 1966
Fax: 918 266 1808

12

Factory Representatives

California

Trinity Technologies
1261 Oakmead Parkway
Sunnyvale, CA 94086
Tel: 408 733 9000
Fax: 408 733 9970

Competitive Technology, Inc.
200 Baha Street, Suite 101
Costa Mesa, CA 92626
Tel: 714 540 5501
Fax: 714 540 5171

Eagle Technical Sales
1900 Sunset Drive, Suite A
Escondido, CA 92025
Tel: 619 743 6550
Fax: 619 743 6585

Colorado

Western Region Marketing, Inc.
9176 Marshall Place
Westminster, CO 80030
Tel: 303 428 8088
Fax: 303 426 8585

Connecticut

S-J Associates Inc.
10 Copper Ridge Circle
Guilford, CT 06437
Tel: 203 458 7558
Fax: 203 458 1181

S-J Associates Inc.
15 Coventry Lane
Naugatuck, CT 06770
Tel: 203 723 4707
Fax: 203 723 1629

Delaware

S-J Mid-Atlantic, Inc.
131-D Gaither Drive
Mt. Laurel, NJ 08054
Tel: 609 866 1234
Fax: 609 866 8627

Florida

Electramark Florida, Inc.
14021-B North Dale Mabry
Tampa, FL 33618
Tel: 813 962 1882
Fax: 813 961 0664

Electramark Florida, Inc.
401 Whooping Loop, Suite 1565
Altamonte Springs, FL 32701
Tel: 407 830 0844
Fax: 407 830 0847

Florida (cont.)

Electramark Florida, Inc.
10360 NW 18 Manor
Plantation, FL 33322
Tel: 305 424 2872
Fax: 305 452 1974

Georgia

Electramark, Inc.
6030H Unity Drive
Norcross, GA 30071
Tel: 404 446 7915
Fax: 404 263 6389

Illinois

Spectrum Sales
100 St. Francois Street
Suite 114
Florissant, MO 63031
Tel: 314 921 1313
Fax: 314 921 0701

Janus Incorporated
650 E. Devon Ave.
Itasca, IL 60143
Tel: 708 250 9650
Fax: 708 250 8761

Indiana

Electro Reps, Inc.
125 Airport North Office Park
Fort Wayne, IN 46825
Tel: 219 489 8205
Fax: 219 489 8408

Electro Reps, Inc.
7240 Shadeland Station #275
Indianapolis, IN 46256
Tel: 317 842 7202
Fax: 317 841 0230

Iowa

Spectrum Sales
1364 Elmhurst Dr. NE
Cedar Rapids, IA 52402
Tel: 319 366 0576
Fax: 319 366 0635

Kansas

Spectrum Sales
5382 W. 95th Street
Prairie Village, KS 66207
Tel: 913 648 6811
Fax: 913 648 6823

Kentucky

Electro Reps, Inc.
7240 Shadeland Station #275
Indianapolis, IN 46256
Tel: 317 842 7202
Fax: 317 841 0230

TMC Electronics
7838 Laurel Avenue
Cincinnati, OH 45243
Tel: 513 271 3860
Fax: 513 271 6321

Louisiana

CompTech Sales, Inc.
15415 Katy Fwy., Suite 209
Houston, TX 77094
Tel: 713 492 0005
Fax: 713 492 6116

CompTech Sales, Inc.
2401 Gateway Dr., Suite 114
Irving, TX 75063
Tel: 214 751 1181
Fax: 214 550 8113

Maryland

S-J New York
265 Sunrise Highway
Rockville Centre, NY 11570
Tel: 516 536 4242
Fax: 516 536 9638

Massachusetts

S-J Associates Inc.
44 Mall Road
Burlington, MA 01803
Tel: 617 272 5552
Fax: 617 272 5515

Michigan

J.L. Montgomery Associates, Inc.
2215 Oak Industrial Drive N.E.
Grand Rapids, MI 49505
Tel: 616 458 5490
Fax: 616 458 5709

Minnesota

Com-Tek Sales, Inc.
6525 City West Parkway
Eden Prairie, MN 55344
Tel: 612 941 7181
Fax: 612 941 4322

Mississippi

Electramark, Inc.
4910 Corporate Dr., Suite J
Huntsville, AL 35805
Tel: 205 830 4400
Fax: 205 830 4406

Missouri

Spectrum Sales
100 St. Francois Street, Suite 114
Florissant, MO 63031
Tel: 314 921 1313
Fax: 314 921 0701

Spectrum Sales
5382 W. 95th Street
Prairie Village, KS 66207
Tel: 913 648 6811
Fax: 913 648 6823

Nebraska

Spectrum Sales
5382 W. 95th Street
Prairie Village, KS 66207
Tel: 913 648 6811
Fax: 913 648 6823

Nevada

Western High Tech Marketing, Inc.
(Clark County Only)
9414 E San Salvador, Suite 206
Scottsdale, AZ 85258
Tel: 602 860 2702
Fax: 602 860 2712

New Jersey

Parallax
734 Walt Whitman Rd.
Melville, NY 11747
Tel: 516 351 1000
Fax: 516 351 1606

S-J Mid-Atlantic, Inc.
131-D Gaither Drive
Mt. Laurel, NJ 08054
Tel: 609 866 1234
Fax: 609 866 8627

New Mexico

Western High Tech Marketing, Inc.
9414 E San Salvador, Suite 206
Scottsdale, AZ 85258
Tel: 505 884 2256
Fax: 505 884 2258

New York

Apex Associates, Inc.
1210 Jefferson Rd.
Rochester, NY 14623
Tel: 716 272 7040
Fax: 716 272 7756

S-J New York
265 Sunrise Highway
Rockville Centre, NY 11570
Tel: 516 536 4242
Fax: 516 536 9638

Parallax
734 Walt Whitman Road
Melville, NY 11747
Tel: 516 351 1000
Fax: 516 351 1606

North Carolina

Zucker Associates
4070 Barrett Drive
Raleigh, NC 27609
Tel: 919 782 8433
Fax: 919 782 8476

North Dakota

Comp-Tech Sales, Inc.
6525 City West Parkway
Eden Prairie, MN 55344
Tel: 612 941 7181
Fax: 612 941 4322

Ohio

TMC Electronics
9200 Montgomery Road
Suite 11A
Cincinnati, OH 45242
Tel: 513 984 6720
Fax: 513 984 6874

TMC Electronics
7017 Pearl Rd.
Middleburg Heights, OH 44130
Tel: 216 885 5544
Fax: 216 885 5011

Oklahoma

CompTech Sales, Inc.
18700 Woodbriar Lane
Catoosa, OK 74015
Tel: 918 266 1966
Fax: 918 266 1808

Oregon

Micro Sales
1865 NW 169th Place, Suite 210
Beaverton, OR 97006
Tel: 503 645 2841
Fax: 503 645 3754

Pennsylvania

S-J Mid-Atlantic, Inc.
131-D Gaither Drive
Mt. Laurel, NJ 08054
Tel: 609 866 1234
Fax: 609 866 8627

TMC Electronics
(Western Pennsylvania)
7838 Laurel Avenue
Cincinnati, OH 45243
Tel: 513 271 3860
Fax: 513 271 6321

Rhode Island

S-J New England
44 Mall Road
Burlington, MA 01803
Tel: 617 272 5552
Fax: 617 272 5515

South Carolina

Zucker Associates
4070 Barrett Drive
Raleigh, NC 27609
Tel: 919 782 8433
Fax: 919 782 8476

South Dakota

CompTech Sales, Inc.
6525 City West Parkway
Eden Prairie, MN 55344
Tel: 612 941 7181
Fax: 612 941 4322

Tennessee

Electramark, Inc.
(Western Tennessee)
4910 Corporate Dr., Suite J
Huntsville, AL 35805
Tel: 205 830 4400
Fax: 205 830 4406

Zucker Associates
(Eastern Tennessee)
4070 Barrett Drive
Raleigh, NC 27609
Tel: 919 782 8433
Fax: 919 782 8476

Factory Representatives

Texas

CompTech Sales, Inc.
11130 Jollyville Rd., Suite 200
Austin, TX 78759
Tel: 512 343 0300
Fax: 512 345 2530

CompTech Sales, Inc.
3120 Wheeling Road
El Paso, TX 79930
Tel: 915 566 1022
Fax: 915 566 1030

CompTech Sales, Inc.
15415 Katy Fwy., Suite 209
Houston, TX 77094
Tel: 713 492 0005
Fax: 713 492 6116

CompTech Sales, Inc.
2401 Gateway Dr., Suite 114
Irving, TX 75063
Tel: 214 751 1181
Fax: 214 550 8113

CompTech Sales, Inc.
85 NE Loop 410, Suite 202
San Antonio, TX 78216
Tel: 210 525 9913
Fax: 210 979 0311

CompTech Sales, Inc.
505 E. Jackson, Suite 300
Harlingen, TX 78550
Tel: 512 421 4501
Fax: 512 421 3265

Utah

Western Region Marketing, Inc.
3539 S Main - Suite 210
Salt Lake City, UT 84115
Tel: 801 268 9768
Fax: 801 268 9796

Virginia

S-J Chesapeake
900 S. Washington Street
Suite B2
Falls Church, VA 20046
Tel: 703 533 2233
Fax: 703 533 2236

Washington

Micro Sales
2122-112th Avenue, NE
Bellevue, WA 98004-1493
Tel: 206 451 0568
Fax: 206 453 0092

West Virginia

TMC Electronics
7838 Laurel Avenue
Cincinnati, OH 45243
Tel: 513 271 3860
Fax: 513 271 6321

Wisconsin

Janus, Inc.
375 Williamstowne
Delafield, WI 53018
Tel: 414 646 5420
Fax: 414 646 5421

Wyoming

Western Region Marketing, Inc.
9176 Marshall Place
Westminster, CO 80030
Tel: 303 428 8088
Fax: 303 426 8585

Distributors

12

AFRICA

South Africa

Pace Electronic Components Pty
Cnr. Van Acht & Gewel Streets
P.O. Box 701
Isando 1600, Transvaal
Tel: 11 974 1211
Fax: 11 974 1271

ASIA

Hong Kong

Maxisum Limited
Unit 2520-2525 Tower 1
Metroplaza, Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852 4180909
Fax: 852 4181600

Japan

Dainichi Contronics Inc.
Dainichi Bldg. 1-7 Karaku
1-Chome, Bunkyo-Ku
Tokyo 112, Japan
Tel: 3 3818 8081
Fax: 3 3818 8088

Marubeni Hytech Co., Ltd.
Marubeni Hytech Building
4-20-22, Koishikawa
Bunkyo-Ku
Tokyo 112, Japan
Tel: 3 817 4921
Fax: 3 817 4880

Nippon Precision Device Corp.
Nichibei Time 24 Bldg.
35 Tansu-Cho, Shinjuku-Ku
Tokyo 162, Japan
Tel: 3 3260 1411
Fax: 3 3260 7100

Korea

ProChips Inc.
779-12, Daelim 3-Dong
Youngdeungpo-Ku
Seoul, Korea
Tel: 02 849 8567
Fax: 02 849 8659

Taiwan, R.O.C.

Pinnacle Technologies Co. Ltd.
3F, 5 Lane 768, Sec. 4
Pa-Teh Road
Taipei, Taiwan
Tel: 02 788 4800
Fax: 02 788 5969

Solomon Technology Corp.
5th Floor, No. 293, Sec. 5
Chung Hsiao E. Rd.
Taipei, Taiwan
Tel: 886 2 760 5858
Fax: 886 2 756 9959

AUSTRALIA

NSD Australia
205 Middleborough Road
Box Hill, Victoria 3128
Tel: 61 03 890 0970
Fax: 61 03 899 5191

CANADA

Alberta

Future Electronics
3833 - 29th Street N.E.
Calgary, Alberta, TIY 6B5
Tel: 403 250 5550
Fax: 403 291 7054

Farnell Electronic Services
3015 - 5th Ave.
Suite 210
Calgary, Alberta, T2A 6T8
Tel: 403 273 2780
Fax: 403 273 7458

Future Electronics
4606 - 97th Street
Edmonton, Alberta, T6E 5N9
Tel: 403 438 2858
Fax: 403 434 0812

Semad Electronics
6815 8th St. N.E., Ste. 175
Calgary, Alberta, T2E 7H7
Tel: 403 252 5664
Fax: 1 800 565 9779

British Columbia

Future Electronics
1695 Boundary Road
Vancouver, B.C., V5K 4X7
Tel: 604 294 1166
Fax: 604 294 1206

Farnell Electronic Services
8525 Baxter Place, Unit 101
Production Court
Burnaby, B.C., V5A 4V7
Tel: 604 421 6222
Fax: 604 421 0582

Semad Electronics
3700 Gilmore Way
Burnaby, B.C., V5G 4M1
Tel: 604 451 3444
Fax: 604 451 3445

Manitoba

Future Electronics
106 King Edward
Winnipeg, Manitoba, R3H ON8
Tel: 204 786 7711
Fax: 204 783 8133

Farnell Electronic Services
1313 Border Street, Unit 35
Winnipeg, Manitoba, R3H OX4
Tel: 204 697 2300
Fax: 204 697 2293

Ontario

Future Electronics
1050 Baxter Road
Ottawa, Ontario, K2C 3P2
Tel: 613 820 8313
Fax: 613 820 3271

Farnell Electronic Services
39 Robertson Road
Suite 506, Bell Mews
Nepean, Ontario, K2H 8R2
Tel: 613 596 6980
Fax: 613 596 6987

Semad Electronics
2781 Lancaster Road, Suite 302
Ottawa, Ontario, K1B 1A7
Tel: 613 526 4866
Fax: 613 523 4372

Future Electronics
5935 Airport Road, Suite 200
Mississauga, Ontario, L4V IW5
Tel: 416 612 9200
Fax: 416 612 9185

Farnell Electronic Services
300 N. Rivermede Road
Concord, Ontario, L4K 2Z4
Tel: 416 798 4884
Fax: 416 798 4889

Semad Electronics
85 Spy Court
Markham, Ontario, L3R 4Z4
Tel: 416 475 3922
Fax: 416 475 4158

Distributors

Quebec

Farnell Electronic Services
6600 Trans Canada Highway
Pointe-Claire, Quebec H9R 4S2
Tel: 514 694 7710
Fax: 514 694 9989

Semad Electronics
243 Place Frontenac
Pointe Clare, Quebec, H9R 4Z7
Tel: 514 694 0860
Fax: 514 694 0965

Future Electronics
1000 Ave. St. Jean Baptiste
Suite 100
Quebec City, Quebec, G2E 5G5
Tel: 418 877 6666
Fax: 418 877 6671

Future Electronics
237 Hymas Blvd.
Point Claire P.Q. H9R 5C7
Tel: 514 694 7710
Fax: 514 695 3707

EUROPE

Austria

Elbatex Electronics GmbH
Rotermuehlgasse 26
A-1120 Wien
Tel: 43 222 8135646
Fax: 43 222 834276

Elbatex Gruppe
Eitnergasse 6
A1233 Wien
Tel: 43 1 81602 0
Fax: 43 1 863211 201

Belgium

Sonetech N.V.
De Limburg Stirumlaan 243
Bus 3
B-1780 Wemmel
Tel: 32 2 460 0707
Fax: 32 2 460 1200

Portugal

Digicontrole
Dpt Comercial
Ave. Eng Arantes E Oliveira 52d
1900 Lisboa

Denmark

Exatec A/S
Mileparken 20E
2740 Skovlund
Tel: 45 44 92 7000
Fax: 45 44 92 6020

England

Eiger Technology Ltd.
14 Howard Court
Manor Park Avenue
Manor Park Runcorn
Cheshire, England WA7 1SJ
Tel: 44 928 579009
Fax: 44 928 579123

Farnell Electronics
Canal Road
Leeds, LS12 2TU
Tel: 44 532 636311
Fax: 44 532 633411

Future Electronics Ltd.
Future House Poyle Road
Colnbrook, Berks, SL3 0EZ
Tel: 44 753 687000
Fax: 44 753 689100

H.B. Electronics Ltd.
Lever Street
Bolton, Lancashire, BL3 6BJ
Tel: 44 204 2 5544
Fax: 44 204 384911

Hawke Components Ltd.
26 Campbell Court
Bramley
NR Basingstoke, Hants, RG26 5EG
Tel: 44 256 880800
Fax: 44 256 880325

Farnell Electronic Services
346 Edinburgh Ave.
Slough, Berks, SL1 4TU
Tel: 44 753 824131
Fax: 44 753 824160

Polar Electronics PLC
Cherrycourt Way
Leighton Buzzard
Bedfordshire LU7 8YY
Tel: 44 525 377093
Fax: 44 525 378367

France

Farnell Electronic Services
16 Avenue des Andes
ZA de Courtaboeuf - BP 16
91941 LES ULIS Cedex A
Tel: 33 1 64 460200
Fax: 33 1 64 463898

Mecodis
Parc d'Activites
3 Allee des Erables
94042 CRETEIL Cedex
Tel: 33 1 43 994400
Fax: 33 1 43 999828

Germany

Avnet E2000 GmbH
Stahlgruberring 12
D-81801 Muenchen 82
Tel: 089 45110 01
Fax: 089 45110 210

Future Electronics Deutschland
Munchner Strasse 18
85774 Unterfohing
Munich, Germany
Tel: 49 89 957 1950
Fax: 49 89 957 1940

Metronik GmbH
Leonhardsweg 2
D82003 Unterhaching
Tel: 89 611080
Fax: 89 6112246

Rutronik RSC-Halbleiter GmbH
Industriestr 2
75228 Ispringen/Pforzheim
Germany
Tel: 49 07231 8010
Fax: 49 07231 82282

Semitron W. Roeck & Co.
Im Gut 1
D79790 Kuessaberg
Tel: 49 7742 80010
Fax: 49 7742 6901

Greece

P. Caritato & Associates S.A.
Ilia Iliou 31
Athens 11743
Tel: 30 1 9020115
Fax: 30 1 9017024

Israel

Elina Electronics Ltd.
14 Raoul Wallenberg St.
P.O. Box 13190
Tel Aviv 61131
Tel: 972 3 498543
Fax: 972 3 498745

Italy

Eurelettronica Srl
Viale E. Fermi 8
20090 Assago Milano
Tel: 39 2 457 841
Fax: 39 2 488 0275

Farnell Spa
Viale Milanofiori E/5
20090 Assago Milano,
Tel: 39 2 8247 0215
Fax: 39 2 8247 0278

Kevin
Via del Gradenigo, 3
20148 Milano
Tel: 39 2 4870 6300
Fax: 39 2 4870 6500

Netherlands

Semicon B.V.
Gulberg 33
P.O. Box 258
NL-5670 AG Nuenen
Tel: 31 40 837075
Fax: 31 40 832300

Norway

Odin Elektronik AB
P.O. Box 9376 Gronlund
N0135 Oslo
Tel: 47 22 677 290
Fax: 47 677 380

Spain

Sagitron
Corazon de Maria 80/82
28002 Madrid
Tel: 34 1416 9261
Fax: 34 1415 8652

Sweden

MEMEC Scandinavia AB
Kvarnholmsvagen 52
131 31 Nacka
Tel: 46 8 6434190
Fax: 46 8 6431195

Switzerland

Elbatex Gruppe AG
Hardstr. 72
CH-5430 Wettingen
Tel: 41 1 56 275111
Fax: 41 1 56 275454

Ellyptic AG
Fellenbergsuresse 281
CH 8047 Zurich

Semitron W. Roeck & Co.
Promenadenstrasse 6
CH 8437 Zurich

Turkey

Inter Muehendislik Danismanlik
Ve Ticaret A.S.1
Hasircibasi Caddesi No. 55
81310 Kadikoy
Istanbul
Tel: 90 1 349 94 00
Fax: 90 1 349 94 30

SOUTH AFRICA

Isando

Pace Electronic Components Ltd.
Cnr. Vanacht & Gewel Streets
P.O. Box 701
Isando 1600, Transvaal
Tel: 27 11 974 1211/6
Fax: 27 11 974 1271

SOUTH AMERICA

Brazil

Aplicacoes Electronicas Artimar
Rue Marques de Itu,70-1- AND.
Caixa Postal 5881*9498
Cep 01223
Sao Paulo, Brazil
Tel: 55112310277
Fax: 55112550511

USA

Alabama

Future Electronics
4835 University Square, Suite 12
Huntsville, AL 35816
Tel: 205 830 2322
Fax: 205 830 6664

Pioneer Technologies
4835 University Square #5
Huntsville, AL 35816
Tel: 205 837 9300
Fax: 205 837 9358

Arizona

Bell Industries
140 S. Linden Lane #102
Tempe, AZ 85281
Tel: 602 966 3600
Fax: 602 967 6584

Future Electronics
4636 E. University Dr.
Suite 245
Phoenix, AZ 85034
Tel: 602 968 7140
Fax: 602 968 0334

California

Bell Industries
1161 N. Fairoaks Ave.
Sunnyvale, CA 94089
Tel: 408 734 8570
Fax: 408 734 8875

Future Electronics
2220 O'Toole Avenue
San Jose, CA 95131
Tel: 408 434 1122
Fax: 408 433 0822

Pioneer Technical Products
134 Rio Robles
San Jose, CA 95134
Tel: 408 954 9100
Fax: 408 954 9113

Bell Industries
4311 Anthony Court, Suite 100
Rocklin, CA 95677
Tel: 916 652 0414
Fax: 916 652 0403

Bell Industries
220 Technology Drive, Suite 100
Irvine, CA 92718
Tel: 714 727 4500
Fax: 714 453 4610

Bell Industries
30101 Agoura Court, Suite 118
Agoura Hills, CA 91301
Tel: 818 865 7900, 1 800 256 6666
Fax: 818 991 7695

Future Electronics
27489 W. Agoura Road, Suite 300
Agoura Hills, CA 91301
Tel: 818 865 0040, 1 800 876 6008
Fax: 818 865 1340

Distributors

California (cont.)

Pioneer Standard
5126 Clareton Drive #160
Agoura Hills, CA 91301
Tel: 818 865 5800
Fax: 818 865 5814

Future Electronics
1692 Browning Ave.
Irvine, CA 92714
Tel: 714 250 4141
Fax: 714 250 4185

Pioneer Standard
217 Technology Drive #110
Irvine, CA 92718
Tel: 714 573 5090, 1 800 535 1430
Fax: 714 753 5074

Aegis Electronic Group, Inc.
1015 Chestnut Ave.
Suite G2
Carlsbad, CA 92008
Tel: 619 729 2026
Fax: 619 729 9295

Bell Industries
5520 Ruffin Road, Suite 209
San Diego, CA 92123
Tel: 619 576 3294
Fax: 714 453 4610

Future Electronics
5151 Shoreham Place
Suite 220
San Diego, CA 92122
Tel: 619 625 2800
Fax: 619 625 2810

Pioneer Standard
4370 La Jolla Village Dr., 4th Floor
San Diego, CA 92122
Tel: 619 546 4906
Fax: 619 535 8154

Colorado

Bell Industries
1873 S. Bellaire St.
Denver, CO 80222
Tel: 303 691 9010
Fax: 303 691 9036

Future Electronics
12600 W. Colfax Avenue
Suite B110
Lakewood, CO 80215
Tel: 303 232 2008
Fax: 303 232 2009

Connecticut

Future Electronics
700 West Johnson Ave.
Cheshire, CT 06410
Tel: 203 250 0083
Fax: 203 250 0081

Phase 1 Technology Corporation
36A Padanarm Road
Danbury, CT 06811
Tel: 203 791 9042
Fax: 201 790 6128

Pioneer Standard
Two Trap Falls #101
Shelton, CT 06484
Tel: 203 929 5600
Fax: 203 929 9791

Florida

Bell Industries
650 S. Northlake Blvd, Suite 400
Altamonte Springs, FL 32701
Tel: 407 339 0078
Fax: 407 339 0139

Future Electronics
650 S. Northlake Blvd.
Suite 520
Altamonte Springs, FL 32701
Tel: 407 767 8414
Fax: 407 834 9318

Pioneer Technologies
337 South-North Lake #1000
Altamonte Springs, FL 32701
Tel: 407 834 9090
Fax: 407 834 0865

Future Electronics
2200 Tall Pines Drive
Suite 108
Largo, FL 34641
Tel: 813 530 1222
Fax: 813 538 9598

Pioneer Technologies
674 S. Military Trail
Deerfield Beach, FL 33442
Tel: 305 428 8877
Fax: 305 481 2950

Georgia

Pioneer Technologies
4250 C Rivergreen Parkway
Duluth, GA 30136
Tel: 404 623 1003
Fax: 404 623 0665

Georgia

Bell Industries
3020 Business Park Drive
Suite A
Norcross, GA 30071
Tel: 404 446 7167
Fax: 404 446 7264

Future Electronics
3150 Holcomb Bridge Road
Suite 130
Norcross, GA 30071
Tel: 404 441 7676
Fax: 404 441 7580

Illinois

Bell Industries
870 Cambridge Drive
Elk Grove Village, IL 60007
Tel: 708 640 1910
Fax: 708 640 1942

Future Electronics
3150 W. Higgins Rd., Suite 160
Hoffman Estates, IL 60195
Tel: 708 882 1255
Fax: 708 490 9290

Pioneer Standard
2171 Executive Drive #200
Addison, IL 60101
Tel: 708 495 9680
Fax: 708 495 9831

Indiana

Bell Industries
3433 E. Washington Blvd.
Fort Wayne, IN 46803
Tel: 219 422 4300
Fax: 219 423 3420

Bell Industries
5230 W. 79th St.
Indianapolis, IN 46268
Tel: 317 875 8200
Fax: 317 875 8219

Future Electronics
8425 Woodfield Crossing
Suite 175
Indianapolis, IN 46240
Tel: 317 469 0477
Fax: 317 469 0448

Pioneer Standard
9350 N. Priority Way W. Dr.
Indianapolis, IN 46240
Tel: 317 573 0880
Fax: 317 573 0979

Kansas

Future Electronics
8826 Santa Fe Drive, Suite 150
Overland Park, KS 66212
Tel: 913 649 1531
Fax: 913 649 1786

Maryland

Bell Industries
8945 Guilford Rd., Suite 130
Columbia, MD 21046
Tel: 410 290 5100
Fax: 410 290 8006

Future Electronics
6716 Alexander Bell Drive #101
Columbia, MD 21046
Tel: 410 290-0600
Fax: 410 290 0328

Pioneer Technologies
9100 Gaither Road
Gaithersburg, MD 20877
Tel: 301 921 0660
Fax: 301 921 4255

Vantage Components, Inc.
6925 R. Oakland Mills Road
Columbia, MD 21045
Tel: 401 720 5100
Fax: 401 381 2172

Massachusetts

Bell Industries
100 Burtt Road, Suite 106
Andover, MA 01810
Tel: 508 474 8880
Fax: 508 474 8902

Future Electronics
41 Main Street
Bolton, MA 01740
Tel: 508 779 3000
Fax: 508 779 5143

Pioneer Standard
44 Hartwell Ave.
Lexington, MA 02173
Tel: 617 861 9200
Fax: 617 863 1547

Michigan

Future Electronics
35200 Schoolcraft Road, Suite 106
Livonia, MI 48150
Tel: 313 261 5270
Fax: 313 261 8125

Future Electronics
4505 Broadmoor SE
Grand Rapids, MI 49512
Tel: 616 698 6800
Fax: 616 698 6821

Pioneer Standard
4595 Broadmoor, Suite 235
Grand Rapids, MI 49512
Tel: 616 698 1800
Fax: 616 698 1831

Pioneer Standard
44190 Plymouth Oaks Drive
Plymouth, MI 48170
Tel: 313 416 2157
Fax: 313 416 2415

Minnesota

Digi-Key Corporation
701 Brooks Ave. So.
P.O. Box 677
Thief River Falls, MN 55344
Tel: 218 681 6674
Fax: 218 681 3380

Future Electronics
10025 Valley View Road, Suite 196
Eden Prairie, MN 55344
Tel: 612 994 2200
Fax: 612 994 2520

Pioneer Standard
7625 Golden Triangle
Eden Prairie, MN 55344
Tel: 612 944 3355
Fax: 612 944 3794

Missouri

Future Electronics
12125 Woodcrest Executive Dr.
Suite 220
St. Louis, MO 63141
Tel: 314 469 6805, 1 800 727 6805
Fax: 314 469 7226

New Jersey

Bell Industries
271 Route 46 West
Suites F202-203
Fairfield, NJ 07004
Tel: 201 227 6060
Fax: 201 227 2626

Future Electronics
12 East Stow Road, Suite 200
Marlton, NJ 08053
Tel: 609 596 4080
Fax: 609 596 4266

Future Electronics
1259 Route 46 East
Parsippany, NJ 07054
Tel: 201 299 0400
Fax: 201 299 1377

Phase 1 Technology Corporation
295 Molnar Drive
Elmwood Park, NJ 07407
Tel: 201 791 2990
Fax: 201 791 2552

Pioneer Standard
14A Madison Road
Fairfield, NJ 07006
Tel: 201 575 3510
Fax: 201 575 3454

Vantage Components, Inc.
23 Sebago Street
Clifton, NJ 07013
Tel: 201 777 4100
Fax: 201 777 6194

New Mexico

Bell Industries
11728 Linn N.E.
Albuquerque, NM 87123
Tel: 505 292 2700
Fax: 505 275 2819

New York

Future Electronics
200 Salina Meadows, Suite 130
Syracuse, NY 13212
Tel: 315 451 2371
Fax: 315 451 7258

Future Electronics
300 Linden Oaks
Rochester, NY 14625
Tel: 716 272 1120
Fax: 716 272 7182

Distributors

New York (cont.)

Pioneer Standard
840 Fairport Park
Fairport, NY 14450
Tel: 716 381 7070
Fax: 716 381 5955

Pioneer Standard
1249 Front Street, Suite 201
Binghampton, NY 13904
Tel: 607 722 9300
Fax: 607 722 9562

Phase 1 Technology Corporation
46 Jefryne Blvd.
Deer Park, NY 11729
Tel: 516 254 2600
Fax: 516 254 2693

Future Electronics
801 Motor Parkway
Hauppauge, NY 11788
Tel: 516 234 4000
Fax: 516 234 6183

Pioneer Standard
60 Crossways Park West
Woodbury, NY 11797
Tel: 516 677 1726
Fax: 516 921 2143

Vantage Components, Inc.
1056 West Jericho Turnpike
Smithtown, NY 11787
Tel: 516 543 2000
Fax: 516 543 2030

North Carolina

Future Electronics
5225 Capital Blvd.
1 North Commerce Center
Raleigh, NC 27604
Tel: 919 790 7111
Fax: 919 790 9022

Pioneer Technologies
2200 Gateway Centre Blvd.
Suite 215
Morrisville, NC 27560
Tel: 919 460 1530
Fax: 919 460 1540

Ohio

Future Electronics
6009-E Landerhaven Dr.
Mayfield Heights, OH 44124
Tel: 216 449 6996
Fax: 216 449 8987

Future Electronics
1430 Oak Court, Suite 203
Beavercreek, OH 45430
Tel: 513 426 0090
Fax: 513 426 8490

Pioneer Standard
4800 East 131st St.
Cleveland, OH 44105
Tel: 216 587 3600
Fax: 216 587 3906

Bell Industries
444 Windsor Park Drive
Dayton, OH 45459
Tel: 513 435 8660
Fax: 513 435 6765

Pioneer Standard
4433 Interpoint Blvd.
Dayton, OH 45424
Tel: 513 236 9900
Fax: 513 236 8133

Pioneer Standard
6421 East Main #201
Reynoldsburg, OH 43068
Tel: 614 221 0043
Fax: 614 759 1955

Bell Industries
31200 Solon Road
Solon, OH 44139
Tel: 216 498 2002
Fax: 216 498 2006

Oklahoma

Pioneer Standard
9717 E. 42nd St.
Tulsa, OK 74146
Tel: 918 664 7840
Fax: 918 665 1891

Oregon

Bell Industries
9275 S.W. Nimbus
Beaverton, OR 97005
Tel: 503 644 1500
Fax: 503 520 1948

Future Electronics
15236 N.W. Greenbrier Pkwy.
Beaverton, OR 97006
Tel: 503 645 9454
Fax: 503 645 1559

Pennsylvania

Future Electronics
12 E. Store Road, Suite 200
Marlton, NJ 08053
Tel: 609 596 4080
Fax: 609 596 4266

Bell Industries
2550 Metropolitan Drive
Trevose, PA 19053
Tel: 215 953 2800
Fax: 215 364 4928

Pioneer Technologies
500 Enterprise Road
Keith Valley Business Center
Horsham, PA 21567
Tel: 215 674 4000
Fax: 215 674 3107

Pioneer Standard
259 Kappa Drive
Pittsburgh, PA 15238
Tel: 412 782 2300
Fax: 412 963 8255

Texas

Bell Industries
1701 Greenville Ave., Suite 306
Richardson, TX 75081
Tel: 214 690 9096, 1 800 525 6666
Fax: 214 690 0467, 1 800 444 0139

Future Electronics
800 E. Campbell, Suite 130
Richardson, TX 75081
Tel: 214 437 2437
Fax: 214 669 2347

Pioneer Standard
13765 Beta Road
Dallas, TX 75244
Tel: 214 386 7300
Fax: 214 490 6419

Future Electronics
9020 II Capital of Texas Highway N.
Suite 610
Austin, TX 78759
Tel: 512 502 0991
Fax: 512 502 0740

Pioneer Standard
1826-D Kramer Lane
Austin, TX 78758
Tel: 512 835 4000, 1 800 252 5004
Fax: 512 835 9829

Pioneer Standard
8200 Interstate 10 W. #705
San Antonio, TX 78230
Tel: 210 377 3440
Fax: 210 377 3626

Future Electronics
10333 Richmond Ave., Suite 970
Houston, TX 77042
Tel: 713 556 8696
Fax: 713 589 7069

Pioneer Standard
10530 Rockley Road, Suite 100
Houston, TX 77099
Tel: 713 785 1155
Fax: 713 785 4558

Utah

Bell Industries
6912 S. 185 West, Suite B
Midvale, UT 84047
Tel: 801 561 9691
Fax: 801 255 2477

Future Electronics
3450 S. Highland Drive, Suite 301
Salt Lake City, UT 84106
Tel: 801 467 4448
Fax: 801 467 3604

Washington

Bell Industries
8553,- 154th Ave. N.E.
Redmond, WA 98052
Tel: 206 867 5410
Fax: 206 867 5159

Future Electronics
19102 N. Creek Parkway South
Suite 118
Bothell, WA 98011
Tel: 206 489 3400
Fax: 206 489 3411

Wisconsin

Bell Industries
W. 226 N. 900 Eastmound Dr.
Waukesha, WI 53186
Tel: 414 547 8879
Fax: 414 547 6547

Future Electronics
250 N. Patrick Blvd.
Suite 170
Brookfield, WI 53045
Tel: 800 999 8079
Fax: 414 879 0250

Pioneer Standard
120 Bishops Way #163
Brookfield, WI 53005
Tel: 414 784 3480
Fax: 414 784 8207

Authorized Distributor for Obsolete Products

Rochester Electronics, Inc.
10 Malcolm Hoyt Drive
Newburyport, MA 01950
Tel: 508 462 9332
Fax: 508 462 9512

NOTES

Factory Sales

AMERICAS

Corporate Office
Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602 786-7200 Fax: 602 899-9210

Atlanta
Microchip Technology Inc.
1521 Johnson Ferry Road NE, Suite 170
Marietta, GA 30062
Tel: 404 509-8800 Fax: 404 509-8600

Boston
Microchip Technology Inc.
Five The Mountain Road, Suite 120
Framingham, MA 01701
Tel: 508 820-3334 Fax: 508 820-4326

Chicago
Microchip Technology Inc.
665 Tollgate Road, Unit C
Elgin, IL 60123-9312
Tel: 708 741-0171 Fax: 708 741-0638

Dallas
Microchip Technology Inc.
17480 N Dallas Parkway, Suite 114
Dallas, TX 75287
Tel: 214 733-0391 Fax: 214 250-4631

AMERICAS (continued)

Los Angeles
Microchip Technology Inc.
18201 Von Karman, Suite 455
Irvine, CA 92715
Tel: 714 263-1888 Fax: 714 263-1338

New York
Microchip Technology Inc.
150 Motor Parkway, Suite 416
Hauppauge, NY 11788
Tel: 516 273-5305 Fax: 516 273-5335

San Jose
Microchip Technology Inc.
2107 N First Street, Suite 590
San Jose, CA 95131
Tel: 408 436-7950 Fax: 408 436-7955

ASIA/PACIFIC
Microchip Technology Inc.
Unit No. 2520-2525
Tower 1, Metroplaza
Hing Fong Road, Kwai Fong
N.T., Hong Kong
Tel: 852 410 2715 Fax: 852 401 3431

EUROPE

United Kingdom
Arizona Microchip Technology Ltd.
Unit 6, The Courtyard
Meadow Bank, Furlong Road
Bourne End, Buckinghamshire SL8 5AJ
Tel: 44 0628 851 077 Fax: 44 0628 850 259

Germany
Arizona Microchip Technology GmbH
Alte Landstrasse 12-14
85521 Ottobrunn, Germany
Tel: 49 089 609 6072 Fax: 49 089 609 1997

France
Arizona Microchip Technology SARL
2, Rue Du Buisson aux Fraises
F-91300 Massy, France
Tel: 33 01 6930 9090 Fax: 33 01 6930 9079

Italy
Arizona Microchip Technology SARL
Centro Direzionale Colleoni
Palazzo Pegaso Ingresso No. 2
Via Paracelso 23
Brianza (M1), Italy
Tel: 39 039 689 9933 Fax: 39 039 602 1585

JAPAN
Microchip Technology International Inc.
Shinyokohama Gotoh Bldg. 8F, 3-22-4
Shinyokohama, Kohoku-Ku, Yokohama-Shi
Kanagawa 222 Japan
Tel: 81 45 471-6166 Fax: 81 45 471-6122

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Microchip Technology Inc. • 2355 W. Chandler Blvd. • Chandler, AZ 85224-6199 • (602) 786-7200 • Printed in the USA 4/94

Microchip Worldwide Sales and Distribution

MICROCHIP
Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602.786.7200 Fax: 602.899.9210