LOGIC
DEVICES INCORPORATED

1994 Static Random Access Memory

Data Book

JULY 1994

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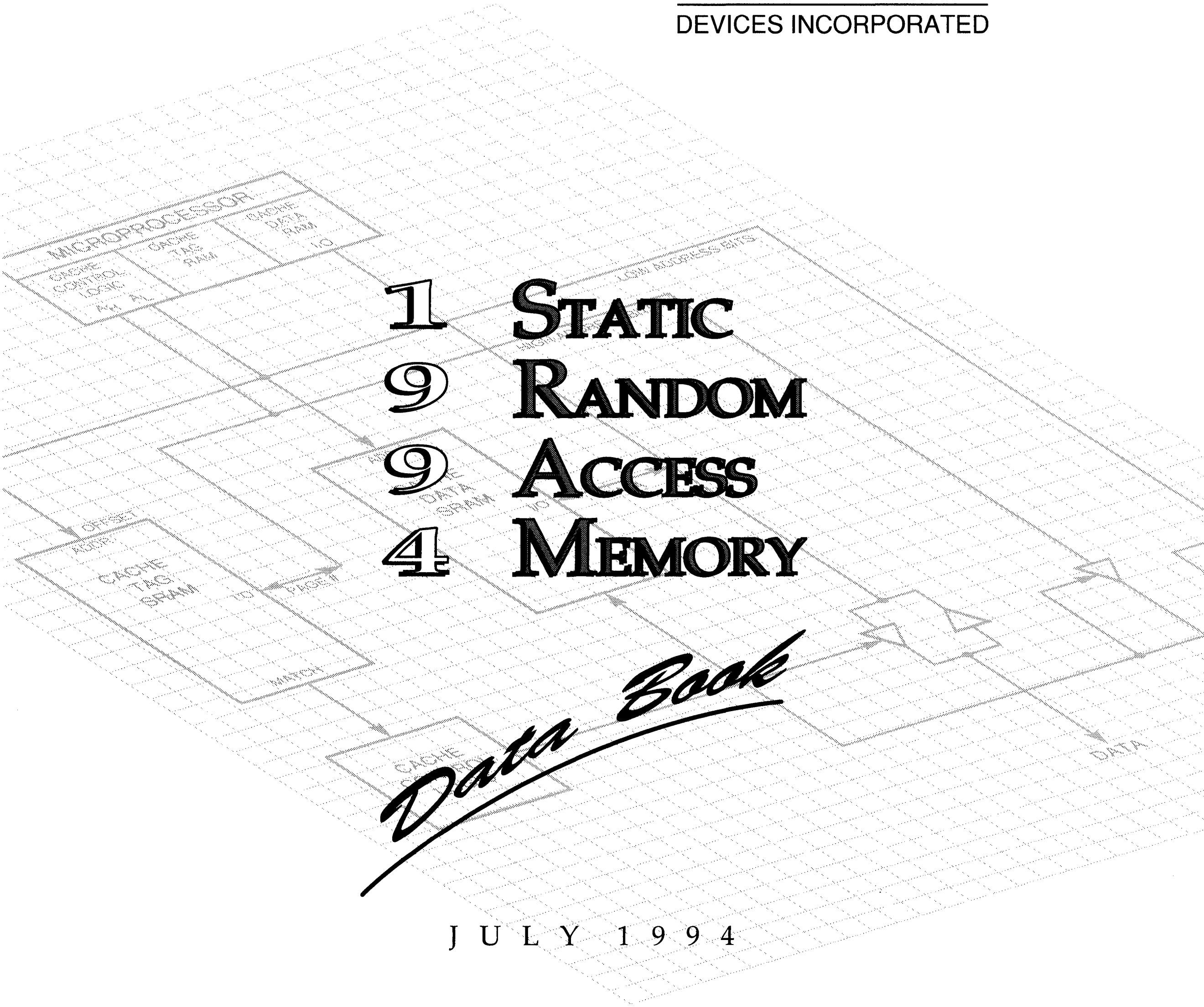

1994 Static Random Access Memory

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Ordering Information

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TO CONSTRUCT A VALID PART NUMBER:

In order to construct a valid LOGIC Devices part number, begin with the generic number obtained from the data sheet header. To this number, append two or three characters from the tables below indicating the desired package code, temperature range, and screening. Finally, append one or two digits indicating the performance grade desired. Most devices are offered in several speed grades with the part number suffix indicating a critical path delay in nanoseconds.

FOR MORE INFORMATION ON AVAILABLE PART NUMBERS:

All products are not offered with all combinations of package styles, temperature ranges, and screening. The Ordering Information table on the last page of each data sheet indicates explicitly all valid combinations of package, temperature, screening, and performance codes for a given product.

L	7C108	C	M	B	20	L
(1)	(2)	(3)	(4)	(5)	(6)	(7)

Key:
(1) Prefix, LOGIC Devices Inc.
(2) Device number
(3) Package code
(4) Temperature range
(5) Screening
(6) Performance/speed grade
(7) Low power designation

Package Codes

Suffix	Description
C, I*	CerDIP
D, H*	Sidebraze, Hermetic DIP
E	Commercial Pin Grid Array
G	Ceramic Pin Grid Array
J	Plastic J-Lead Chip Carrier
K, T*	Ceramic Leadless Chip Carrier
M	CerFlat
P, N*	Plastic DIP
Q	Plastic Quad Flatpack
W	Plastic SOJ (J-Lead)
Y	Ceramic SOJ (J-Lead)

*Some devices are available in packages of two widths. For devices available in a single width, C, D, K, and P are used.

Temperature Range

Suffix	Description
C	Commercial 0°C to +70°C
M	Military –55°C to +125°C

Screening

Suffix	Description
No Designator	Commercial Flow
B	MIL-STD-883 Class B Compliant

16K Static RAMs

L6116

2K x 8 Static RAM (Low Power)

FEATURES

- 2K x 8 Static RAM with Chip Select Powerdown, Output Enable
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 10 ns maximum
- Low Power Operation
  Active:
  425 mW typical at 25 ns
  Standby (typical):
  400 µW (L6116)
  200 µW (L6116-L)
- Data Retention at 2 V for Battery Backup Operation
- DESC SMD No.
  5962-84036 — L6116
  5962-89690 — L6116
  5962-88740 — L6116-L
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with IDT6116, Cypress CY7C128/CY6116
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin CerDIP
  - 24-pin Plastic SOJ
  - 24-pin Ceramic Flatpack
  - 28-pin Ceramic LCC
  - 32-pin Ceramic LCC

DESCRIPTION

The **L6116** is a high-performance, low-power CMOS Static RAM. The storage circuitry is organized as 2048 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. These devices are available in five speeds with maximum access times from 10 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption for the L6116 is 425 mW (typical) at 25 ns. Dissipation drops to 60 mW (typical) for the L6116 and 50 mW (typical) for the L6116-L when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L6116 and L6116-L consume only 30 µW and 15 µW (typical) respectively, at 3 V, allowing effective battery backup operation.

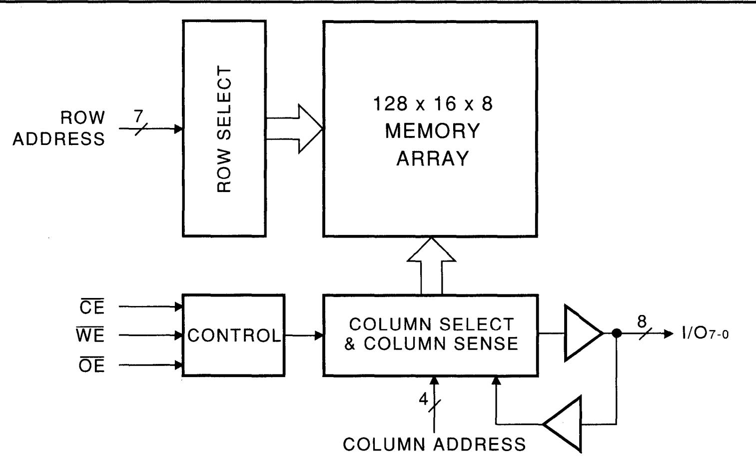
The L6116 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{10}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ and $\overline{OE}$ LOW, while $\overline{WE}$ remains HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is HIGH, or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both LOW. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L6116 can withstand an injection current of up to 200 mA on any pin without damage.

L6116 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature .... –65°C to +150°C
Operating ambient temperature .... –55°C to +125°C
VCC supply voltage with respect to ground .... –0.5 V to +7.0 V
Input signal with respect to ground .... –3.0 V to +7.0 V
Signal applied to high impedance output .... –3.0 V to +7.0 V
Output current into low outputs .... 25 mA
Latchup current .... > 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ VCC ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ VCC ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ VCC ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ VCC ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

			L6116			L6116-L			
Symbol	Parameter	Test Condition	Min	Typ	Max	Min	Typ	Max	Unit
VOH	Output High Voltage	VCC = 4.5 V, IOH = –4.0 mA	2.4			2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA			0.4			0.4	V
VIH	Input High Voltage		2.2		VCC +0.3	2.2		VCC +0.3	V
VIL	Input Low Voltage	(Note 3)	–3.0		0.8	–3.0		0.8	V
IIX	Input Leakage Current	Ground ≤ VIN ≤ VCC	–10		+10	–10		+10	μA
IOZ	Output Leakage Current	(Note 4)	–10		+10	–10		+10	μA
ICC2	VCC Current, TTL Inactive	(Note 7)		12	25		10	15	mA
ICC3	VCC Current, CMOS Standby	(Note 8)		80	300		40	150	μA
ICC4	VCC Current, Data Retention	VCC = 3.0 V (Note 9)		10	150		5	50	μA
CIN	Input Capacitance	Ambient Temp = 25°C, VCC = 5.0 V			5			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

			L6116-					
Symbol	Parameter	Test Condition	25	20	15	12	10	Unit
ICC1	VCC Current, Active	(Note 6)	115	135	160	195	220	mA

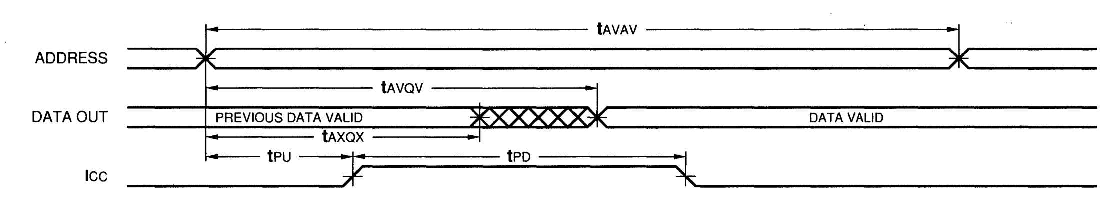
2

SWITCHING CHARACTERISTICS *Over Operating Range*

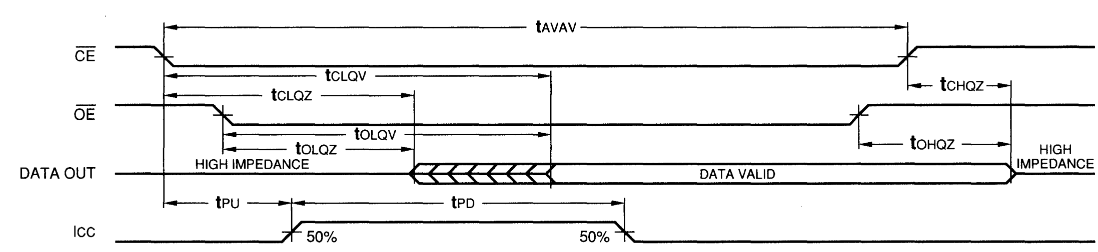
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L6116–									
		25		20		15		12		10	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Read Cycle Time	25		20		15		12		10	
tAVQV	Address Valid to Output Valid (Notes 13, 14)		25		20		15		12		10
tAXQX	Address Change to Output Change	3		3		3		3		3	
tCLQV	Chip Enable Low to Output Valid (Notes 13, 15)		25		20		15		12		10
tCLQZ	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3		3	
tCHQZ	Chip Enable High to Output High Z (Notes 20, 21)		10		8		8		5		4
tOLQV	Output Enable Low to Output Valid		12		10		8		6		5
tOLQZ	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0		0	
tOHQZ	Output Enable High to Output High Z (Notes 20, 21)		10		8		5		5		4
tPU	Input Transition to Power Up (Notes 10, 19)	0		0		0		0		0	
tPD	Power Up to Power Down (Notes 10, 19)		25		20		20		20		18
tCHVL	Chip Enable High to Data Retention (Note 10)	0		0		0		0		0	

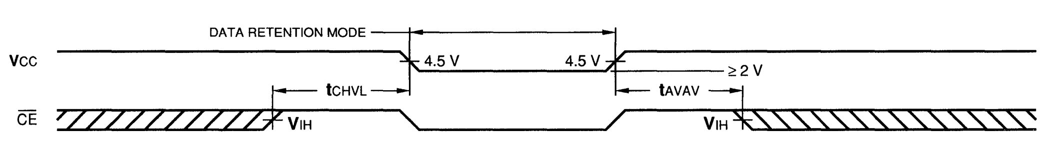
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}$/$\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

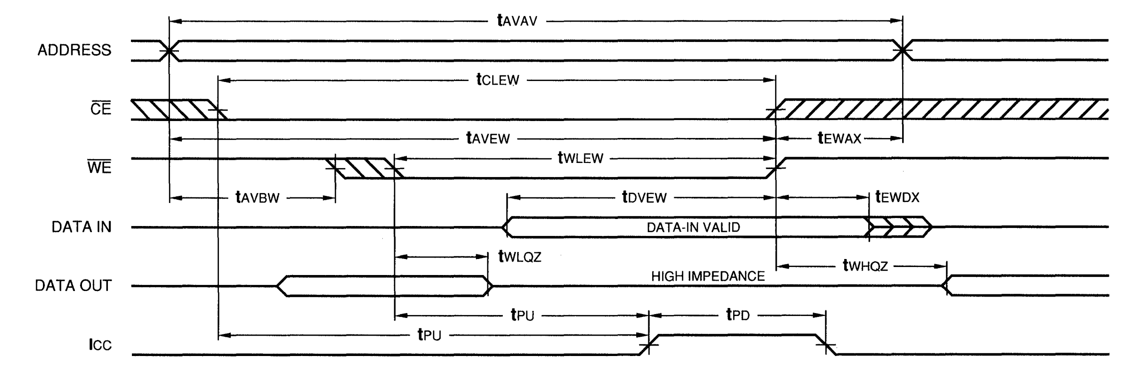


SWITCHING CHARACTERISTICS *Over Operating Range*

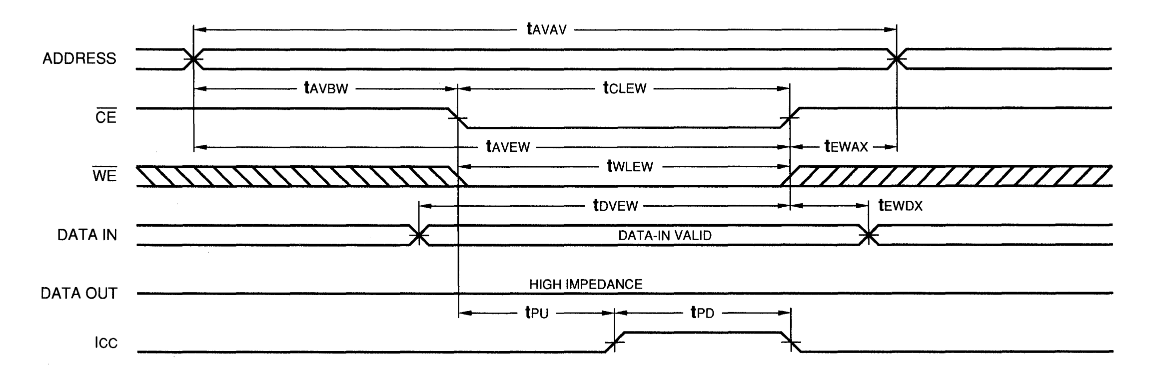
Write Cycle *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L6116–									
		25		20		15		12		10	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	20		20		15		12		10	
t_{CLEW}	Chip Enable Low to End of Write Cycle	15		15		12		10		8	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	15		15		12		10		8	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	15		15		12		10		8	
t_{DVEW}	Data Valid to End of Write Cycle	10		10		7		6		5	
t_{EWDX}	End of Write Cycle to Data Change	1		1		1		1		1	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		7		5		4		4

Write Cycle — $\overline{WE}$ Controlled *Notes 16, 17, 18, 19*



Write Cycle — $\overline{CE}$ Controlled *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE}$ = V_{CC}.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ ≤ V_{IL}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ V_{IH}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

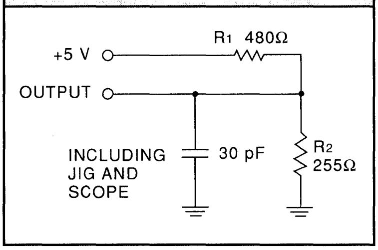


FIGURE 1b.

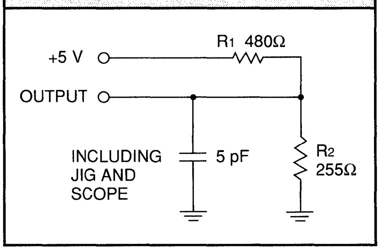
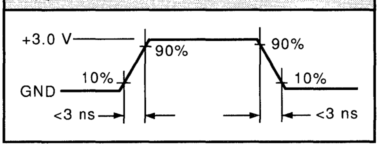
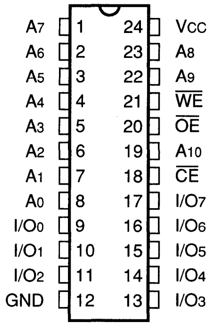


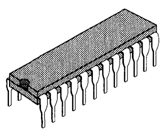
FIGURE 2.

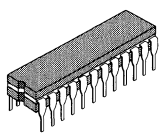


ORDERING INFORMATION

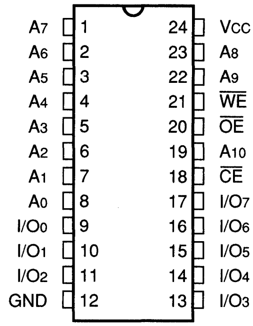
24-pin — 0.3" wide

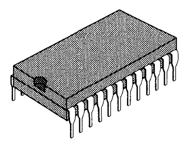


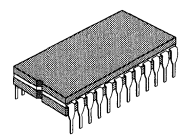




24-pin — 0.6" wide





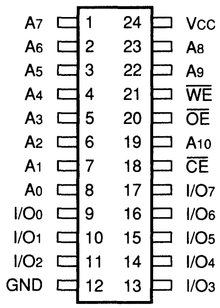


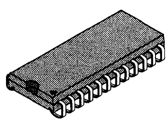
Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic DIP (P1)	Ceramic DIP (C4)
0°C to +70°C — Commercial Screening				
20 ns	L6116PC20*	L6116CC20*	L6116NC20*	L6116IC20*
15 ns	L6116PC15*	L6116CC15*	L6116NC15*	L6116IC15*
12 ns	L6116PC12*	L6116CC12*	L6116NC12*	L6116IC12*
10 ns	L6116PC10*	L6116CC10*	L6116NC10*	L6116IC10*
–55°C to +125°C — Commercial Screening				
25 ns		L6116CM25*		L6116IM25*
20 ns		L6116CM20*		L6116IM20*
15 ns		L6116CM15*		L6116IM15*
12 ns		L6116CM12*		L6116IM12*
–55°C to +125°C — MIL-STD-883 Compliant				
25 ns		L6116CMB25*		L6116IMB25*
20 ns		L6116CMB20*		L6116IMB20*
15 ns		L6116CMB15*		L6116IMB15*
12 ns		L6116CMB12*		L6116IMB12*

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L6116CMB12L)**

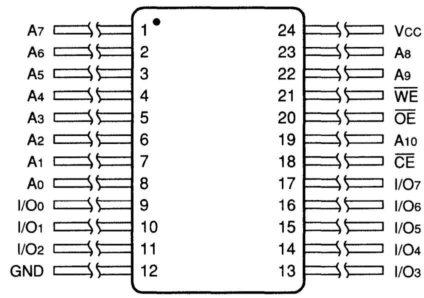
ORDERING INFORMATION

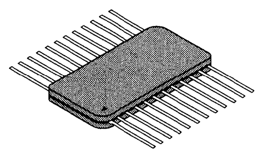
24-pin — 0.3" wide





24-pin



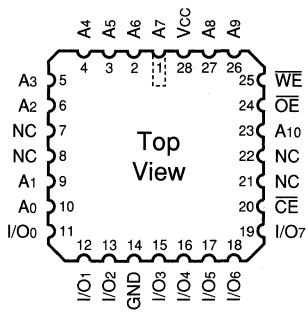


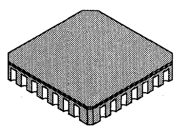
Speed	Plastic SOJ (W1)	Ceramic Flatpack (M1)
	0°C to +70°C — Commercial Screening	
20 ns	L6116WC20*	L6116MC20*
15 ns	L6116WC15*	L6116MC15*
12 ns	L6116WC12*	L6116MC12*
10 ns	L6116WC10*	L6116MC10*
	–55°C to +125°C — Commercial Screening	
25 ns		L6116MM25*
20 ns		L6116MM20*
15 ns		L6116MM15*
12 ns		L6116MM12*
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns		L6116MMB25*
20 ns		L6116MMB20*
15 ns		L6116MMB15*
12 ns		L6116MMB12*

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L6116MMB15L)**

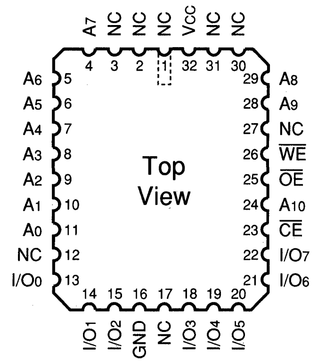
ORDERING INFORMATION

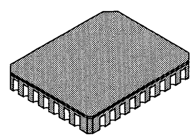
28-pin





32-pin





Speed	Ceramic Leadless Chip Carrier (K1)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening	
20 ns	L6116KC20*	L6116TC20*
15 ns	L6116KC15*	L6116TC15*
12 ns	L6116KC12*	L6116TC12*
10 ns	L6116KC10*	L6116TC10*
	–55°C to +125°C — Commercial Screening	
25 ns	L6116KM25*	L6116TM25*
20 ns	L6116KM20*	L6116TM20*
15 ns	L6116KM15*	L6116TM15*
12 ns	L6116KM12*	L6116TM12*
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns	L6116KMB25*	L6116TMB25*
20 ns	L6116KMB20*	L6116TMB20*
15 ns	L6116KMB15*	L6116TMB15*
12 ns	L6116KMB12*	L6116TMB12*

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L6116KMB12L)**

64K Static RAMs

3

DEVICES INCORPORATED

L7C187
64K x 1 Static RAM

FEATURES

- ❑ 64K x 1 Static RAM with Separate I/O, Chip Select Powerdown
- ❑ Auto-Powerdown™ Design
- ❑ Advanced CMOS Technology
- ❑ High Speed — to 12 ns maximum
- ❑ Low Power Operation
  Active: 225 mW typical at 25 ns
  Standby: 400 µW typical
- ❑ Data Retention at 2 V for Battery Backup Operation
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Plug Compatible with IDT7187, Cypress CY7C187
- ❑ Package Styles Available:
  - 22-pin Plastic DIP
  - 22-pin Ceramic DIP
  - 24-pin Plastic SOJ
  - 22-pin Ceramic LCC

DESCRIPTION

The **L7C187** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 65,536 words by 1 bit per word. This device is available in four speeds with maximum access times from 12 ns to 25 ns.

Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 225 mW (typical) at 25 ns. Dissipation drops to 60 mW (typical) when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C187 consumes only 30 µW (typical) at 3 V, allowing effective battery backup operation.

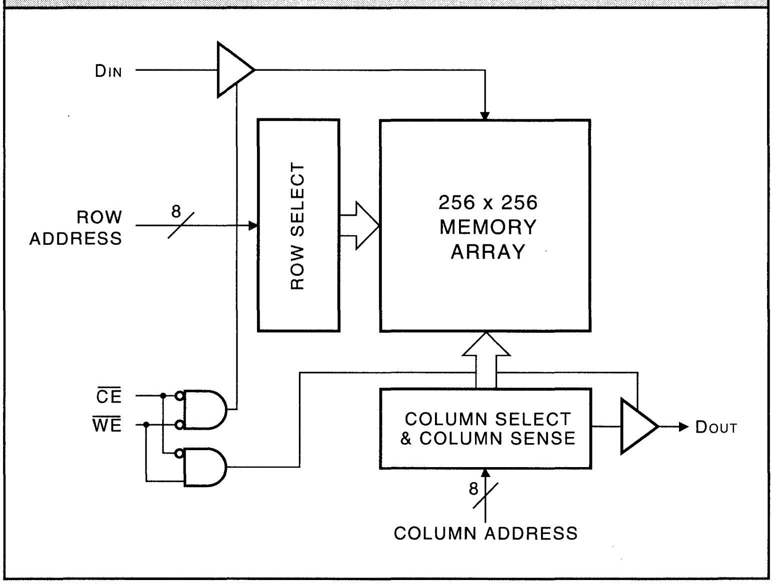
The L7C187 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state output simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{15}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ LOW while $\overline{WE}$ remains HIGH. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ is HIGH or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both LOW. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C187 can withstand an injection current of up to 200 mA on any pin without damage.

L7C187 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
VCC supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ VCC ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ VCC ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ VCC ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ VCC ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C187			
Symbol	**Parameter**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	–10		+10	μA
I_{OZ}	Output Leakage Current	(Note 4)	–10		+10	μA
I_{CC2}	VCC Current, TTL Inactive	(Note 7)		12	25	mA
I_{CC3}	VCC Current, CMOS Standby	(Note 8)		80	300	μA
I_{CC4}	VCC Current, Data Retention	V_{CC} = 3.0 V (Note 9)		10	150	μA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

			L7C187-				
Symbol	**Parameter**	**Test Condition**	**25**	**20**	**15**	**12**	**Unit**
I_{CC1}	VCC Current, Active	(Note 6)	60	75	90	110	mA

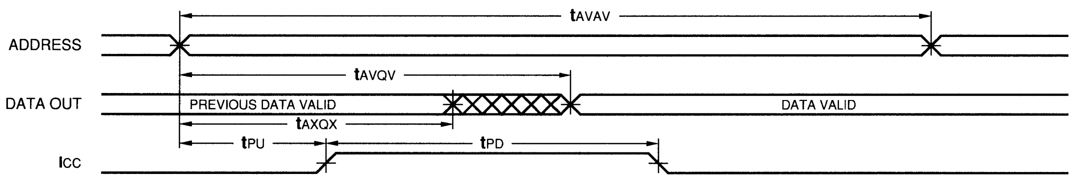
SWITCHING CHARACTERISTICS *Over Operating Range*

READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

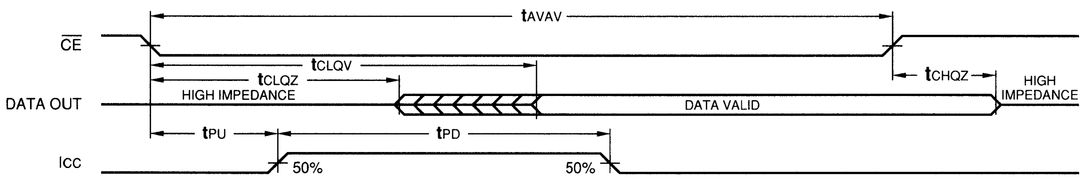
		L7C187–							
		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	25		20		15		12	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		25		20		15		12
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		25		20		15		12
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		10		8		8		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		25		20		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

3

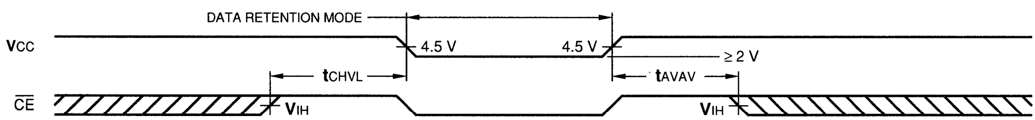
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

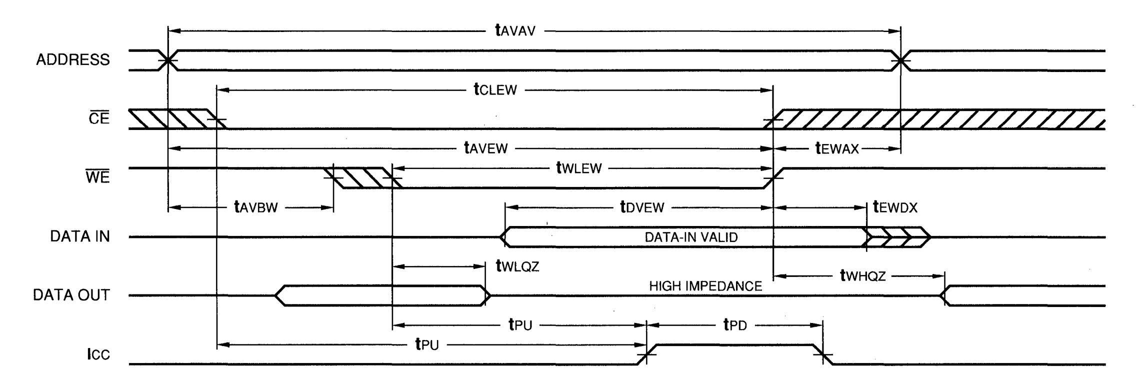


SWITCHING CHARACTERISTICS *Over Operating Range*

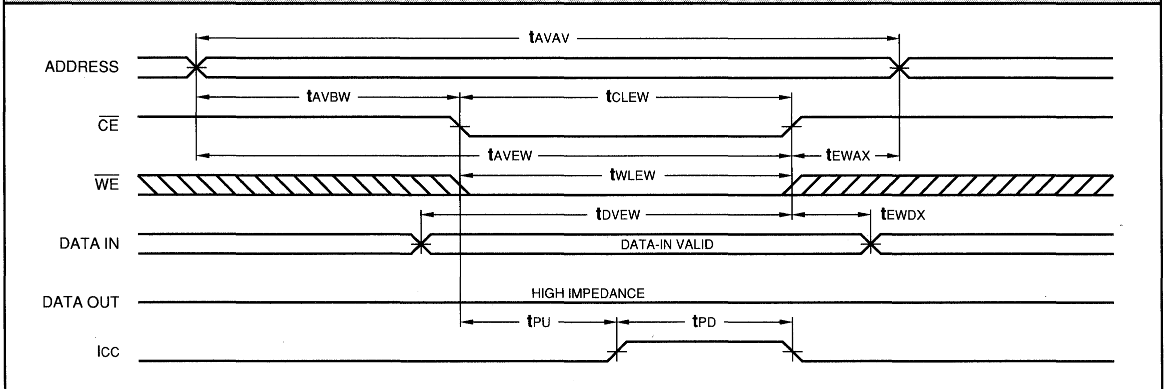
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C187–							
		25		20		15		12	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{AVAV}	Write Cycle Time	20		20		15		12	
t_{CLEW}	Chip Enable Low to End of Write Cycle	15		15		12		10	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	15		15		12		10	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	15		15		12		10	
t_{DVEW}	Data Valid to End of Write Cycle	10		10		7		6	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		7		5		4

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE}$ = V_{CC}.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ ≤ V_{IL}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ V_{IH}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

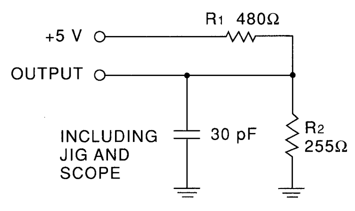


FIGURE 1b.

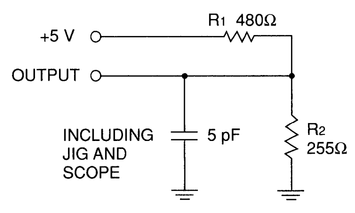
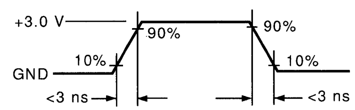
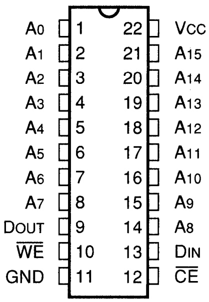


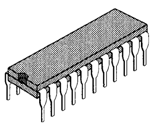
FIGURE 2.

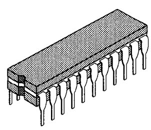


ORDERING INFORMATION

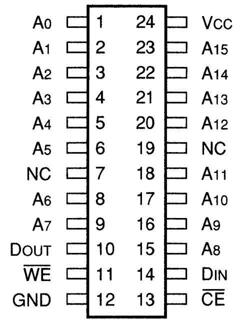
22-pin — 0.3" wide

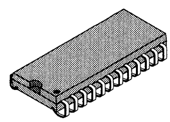






24-pin — 0.3" wide

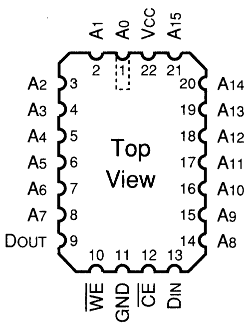


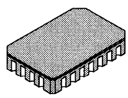


Speed	Plastic DIP (P8)	Ceramic DIP (C3)	Plastic SOJ (W1)
	0°C to +70°C — Commercial Screening		
20 ns	L7C187PC20	L7C187CC20	L7C187WC20
15 ns	L7C187PC15	L7C187CC15	L7C187WC15
12 ns	L7C187PC12	L7C187CC12	L7C187WC12
	–55°C to +125°C — Commercial Screening		
25 ns		L7C187CM25	
20 ns		L7C187CM20	
15 ns		L7C187CM15	
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns		L7C187CMB25	
20 ns		L7C187CMB20	
15 ns		L7C187CMB15	

ORDERING INFORMATION

22-pin





Speed	Ceramic Leadless Chip Carrier (K4)		
	0°C to +70°C — Commercial Screening		
20 ns	L7C187KC20		
15 ns	L7C187KC15		
12 ns	L7C187KC12		
	–55°C to +125°C — Commercial Screening		
25 ns	L7C187KM25		
20 ns	L7C187KM20		
15 ns	L7C187KM15		
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns	L7C187KMB25		
20 ns	L7C187KMB20		
15 ns	L7C187KMB15		

L7C162
16K x 4 Static RAM

FEATURES

- ❑ 16K x 4 Static RAM with Separate I/O and High Impedance Write
- ❑ Auto-Powerdown™ Design
- ❑ Advanced CMOS Technology
- ❑ High Speed — to 12 ns maximum
- ❑ Low Power Operation
  Active: 325 mW typical at 25 ns
  Standby: 400 µW typical
- ❑ Data Retention at 2 V for Battery Backup Operation
- ❑ DESC SMD No. 5962-89712
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Plug Compatible with IDT 71982 and Cypress CY7C162
- ❑ Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Plastic SOJ
  - 28-pin Ceramic LCC

DESCRIPTION

The **L7C162** is a high-performance, low-power CMOS static RAM. The storage cells are organized as 16,384 words by 4 bits per word. Data In and Data Out are separate. This device is available in four speeds with maximum access times from 12 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 325 mW (typical) at 25 ns. Dissipation drops to 60 mW (typical) when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C162 consumes only 30 µW (typical) at 3 V, allowing effective battery backup operation.

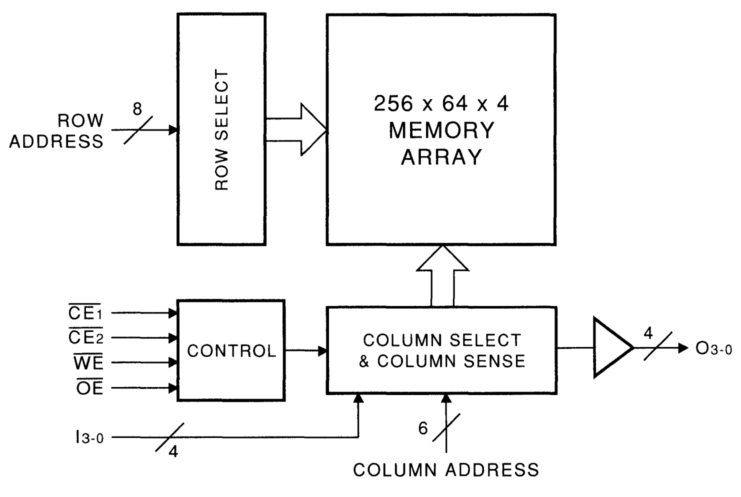
The L7C162 provides asynchronous (unclocked) operation with matching access and cycle times. Two active-low Chip Enables and a three-state output with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A13. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE1}$, $\overline{CE2}$, and $\overline{OE}$ LOW while $\overline{WE}$ remains HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{WE}$ is LOW or $\overline{CE1}$, $\overline{CE2}$, or $\overline{OE}$ is HIGH.

Writing to an addressed location is accomplished when the active-low $\overline{CE1}$, $\overline{CE2}$, and $\overline{WE}$ inputs are all LOW. Any of these signals may be used to terminate the write operation. The Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C162 can withstand an injection current of up to 200 mA on any pin without damage.

L7C162 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
VCC supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ VCC ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ VCC ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ VCC ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ VCC ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C162			
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	VCC = 4.5 V, IOH = –4.0 mA	2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA			0.4	V
VIH	Input High Voltage		2.2		VCC +0.3	V
VIL	Input Low Voltage	(Note 3)	–3.0		0.8	V
IIX	Input Leakage Current	Ground ≤ VIN ≤ VCC	–10		+10	μA
IOZ	Output Leakage Current	(Note 4)	–10		+10	μA
ICC2	VCC Current, TTL Inactive	(Note 7)		12	25	mA
ICC3	VCC Current, CMOS Standby	(Note 8)		80	300	μA
ICC4	VCC Current, Data Retention	VCC = 3.0 V (Note 9)		10	150	μA
CIN	Input Capacitance	Ambient Temp = 25°C, VCC = 5.0 V			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

			L7C162-				
Symbol	Parameter	Test Condition	25	20	15	12	Unit
ICC1	VCC Current, Active	(Note 6)	100	120	140	165	mA

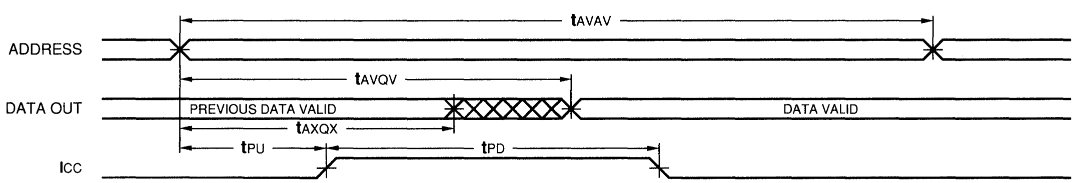
SWITCHING CHARACTERISTICS *Over Operating Range*

READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

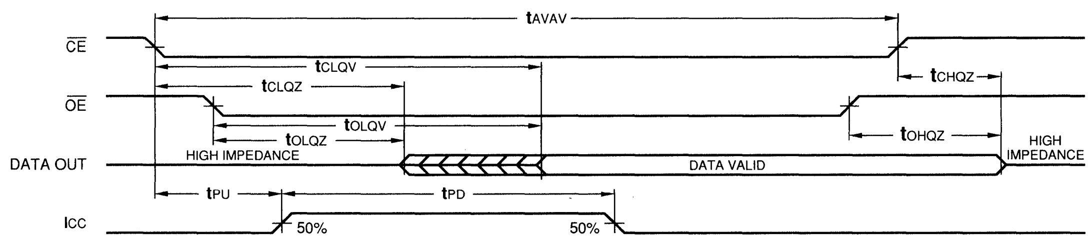
		L7C162–							
		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	25		20		15		12	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		25		20		15		12
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		25		20		15		12
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		10		8		8		5
t_{OLQV}	Output Enable Low to Output Valid		12		10		8		6
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		8		5		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		25		20		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

3

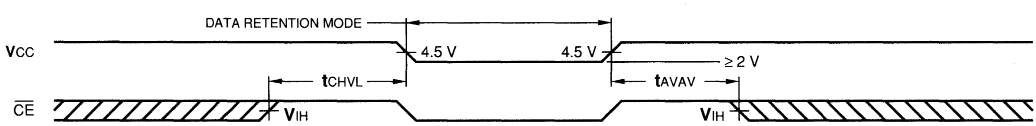
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}$/$\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

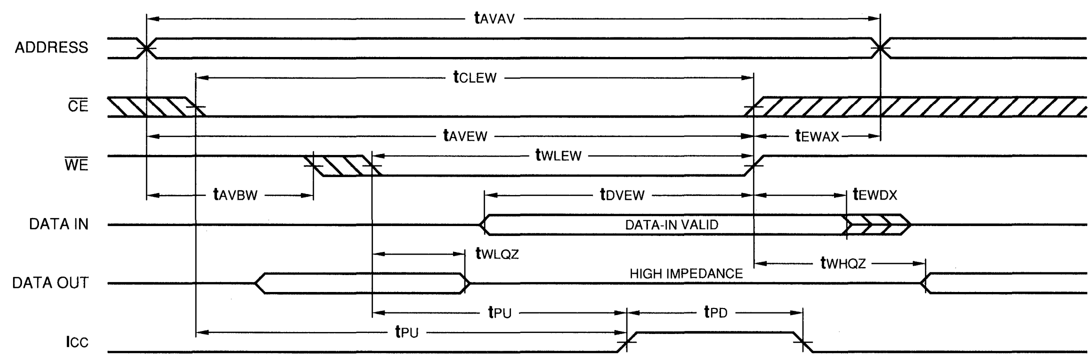


SWITCHING CHARACTERISTICS *Over Operating Range*

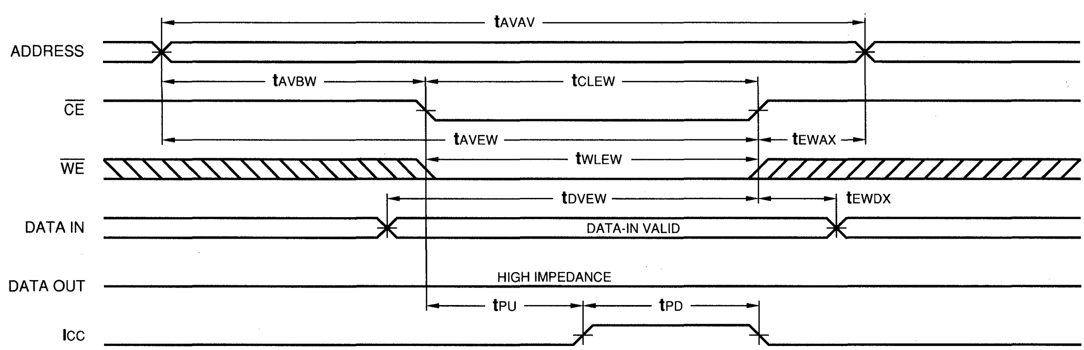
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C162–							
		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	20		20		15		12	
t_{CLEW}	Chip Enable Low to End of Write Cycle	15		15		12		10	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	15		15		12		10	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	15		15		12		10	
t_{DVEW}	Data Valid to End of Write Cycle	10		10		7		6	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		7		5		4

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND $\leq V_{OUT} \leq V_{CC}$. The device is disabled, i.e., $\overline{CE}_1 = V_{CC}$, $\overline{CE}_2 = V_{CC}$.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}_1 \leq V_{IL}$, $\overline{CE}_2 \leq V_{IL}$, $\overline{WE} \leq V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}_1 \geq V_{IH}$, $\overline{CE}_2 \geq V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}_1 = V_{CC}$, $\overline{CE}_2 = V_{CC}$. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}_1$ must be $\geq V_{CC} - 0.2$ V or $\overline{CE}_2$ must be $\geq V_{CC} - 0.2$ V. All other inputs must meet $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}_1$ low, $\overline{CE}_2$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}_1$ and $\overline{CE}_2$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}_1$ and $\overline{CE}_2$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}_1$ and $\overline{CE}_2$ going active, the output remains in a high impedance state.

18. If $\overline{CE}_1$ and $\overline{CE}_2$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}_2$ ($\overline{CE}_1$ active) or the falling edge of $\overline{CE}_1$ ($\overline{CE}_2$ active).

b. Falling edge of $\overline{WE}$ ($\overline{CE}_1$, $\overline{CE}_2$ active).

c. Transition on any address line ($\overline{CE}_1$, $\overline{CE}_2$ active).

d. Transition on any data line ($\overline{CE}_1$, $\overline{CE}_2$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

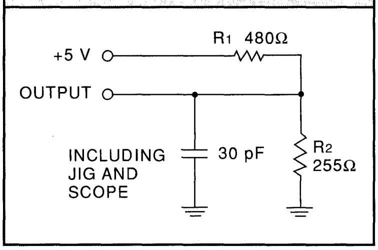


FIGURE 1b.

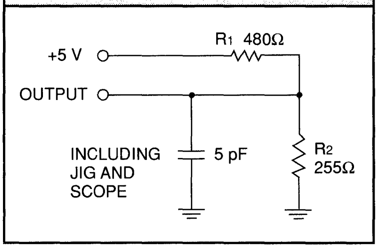
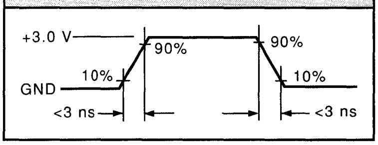
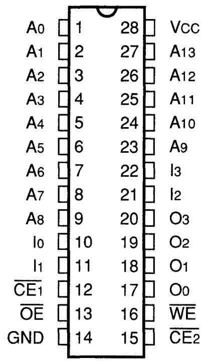


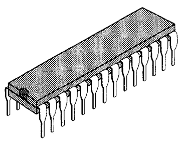
FIGURE 2.

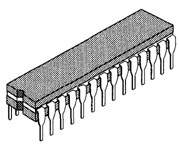


ORDERING INFORMATION

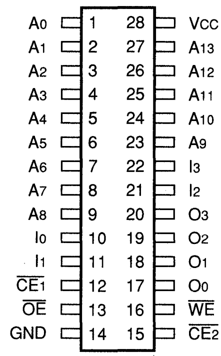
28-pin — 0.3" wide

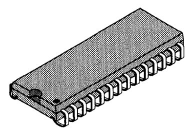






28-pin — 0.3" wide

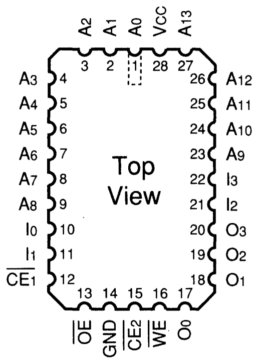


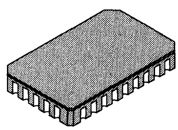


Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic SOJ (W2)
	0°C to +70°C — Commercial Screening		
20 ns	L7C162PC20	L7C162CC20	L7C162WC20
15 ns	L7C162PC15	L7C162CC15	L7C162WC15
12 ns	L7C162PC12	L7C162CC12	L7C162WC12
	–55°C to +125°C — Commercial Screening		
25 ns		L7C162CM25	
20 ns		L7C162CM20	
15 ns		L7C162CM15	
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns		L7C162CMB25	
20 ns		L7C162CMB20	
15 ns		L7C162CMB15	

ORDERING INFORMATION

28-pin





Speed	Ceramic Leadless Chip Carrier (K5)
	0°C to +70°C — Commercial Screening
20 ns	L7C162KC20
15 ns	L7C162KC15
12 ns	L7C162KC12
	–55°C to +125°C — Commercial Screening
25 ns	L7C162KM25
20 ns	L7C162KM20
15 ns	L7C162KM15
	–55°C to +125°C — MIL-STD-883 Compliant
25 ns	L7C162KMB25
20 ns	L7C162KMB20
15 ns	L7C162KMB15

LOGIC
DEVICES INCORPORATED

L7C164/166
16K x 4 Static RAM

FEATURES

- ❑ 16K x 4 Static RAM with Common I/O
- ❑ Auto-Powerdown™ Design
- ❑ Advanced CMOS Technology
- ❑ High Speed — to 12 ns maximum
- ❑ Low Power Operation
  Active: 325 mW typical at 25 ns
  Standby: 400 µW typical
- ❑ Data Retention at 2 V for Battery Backup Operation
- ❑ DESC SMD No.
  5962-89692 — L7C164
  5962-89892 — L7C166
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Plug Compatible with IDT 7188 and Cypress CY7C164/166
- ❑ Package Styles Available:
  - 22/24-pin Plastic DIP
  - 22/24-pin Ceramic DIP
  - 24-pin Plastic SOJ
  - 22/28-pin Ceramic LCC

DESCRIPTION

The **L7C164** and **L7C166** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 16,384 words by 4 bits per word. Data In and Data Out signals share I/O pins. The L7C164 has a single active-low Chip Enable. The L7C166 has a single Chip Enable and an Output Enable. These devices are available in four speeds with maximum access times from 12 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 325 mW (typical) at 25 ns. Dissipation drops to 60 mW (typical) when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C164 and L7C166 consume only 30 µW (typical) at 3 V, allowing effective battery backup operation.

The L7C164 and L7C166 provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased capacity.

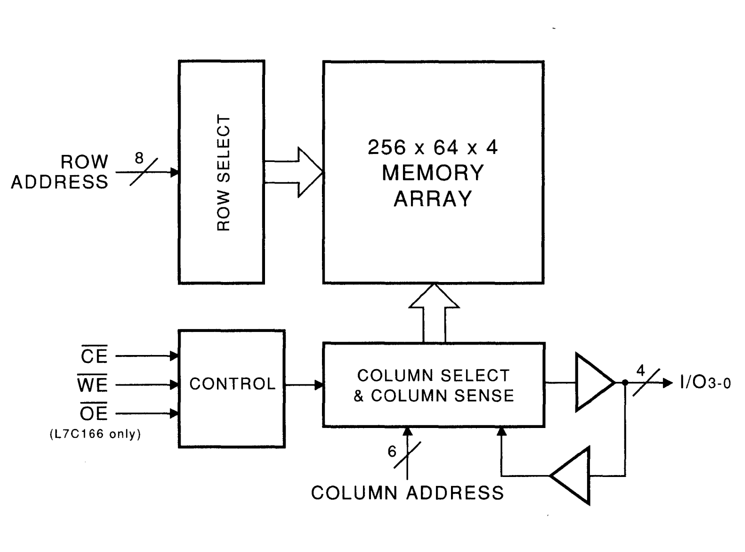
Memory locations are specified on address pins A_0 through A_{13}. For the L7C164, reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ LOW while $\overline{WE}$ remains HIGH. For the L7C166, $\overline{CE}$ and $\overline{OE}$ must be LOW while $\overline{WE}$ remains HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is HIGH, or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are LOW. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C164 and L7C166 can withstand an injection current of up to 200 mA on any pin without damage.

3

L7C164/166 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Military	–55°C to +125°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Data Retention, Commercial	0°C to +70°C	$2.0\ V \le V_{CC} \le 5.5\ V$
Data Retention, Military	–55°C to +125°C	$2.0\ V \le V_{CC} \le 5.5\ V$

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C164/166			
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	–10		+10	μA
I_{OZ}	Output Leakage Current	(Note 4)	–10		+10	μA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		12	25	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		80	300	μA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		10	150	μA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

			L7C164/166-				
Symbol	Parameter	Test Condition	25	20	15	12	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	100	120	140	165	mA

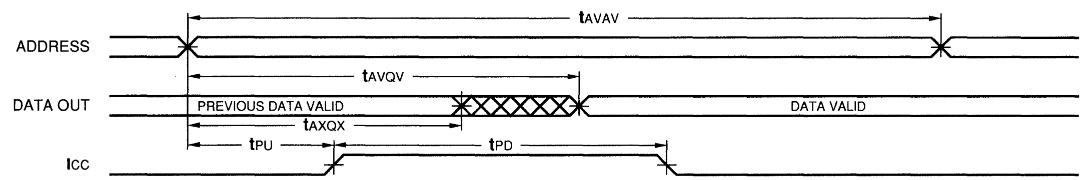
SWITCHING CHARACTERISTICS *Over Operating Range*

READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

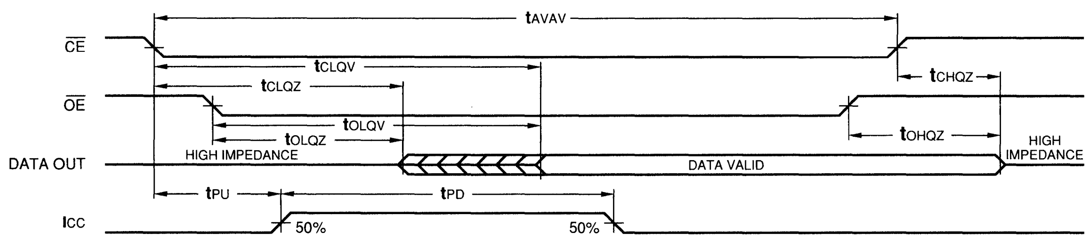
		L7C164/166–							
		25		20		15		12	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{AVAV}	Read Cycle Time	25		20		15		12	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		25		20		15		12
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		25		20		15		12
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		10		8		8		5
t_{OLQV}	Output Enable Low to Output Valid		12		10		8		6
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		8		5		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		25		20		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

3

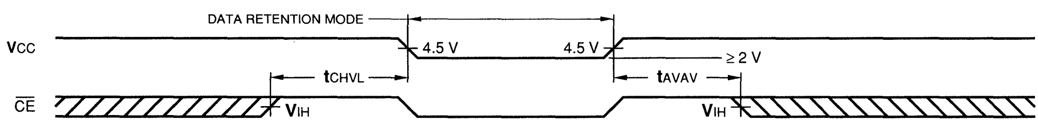
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}$/$\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

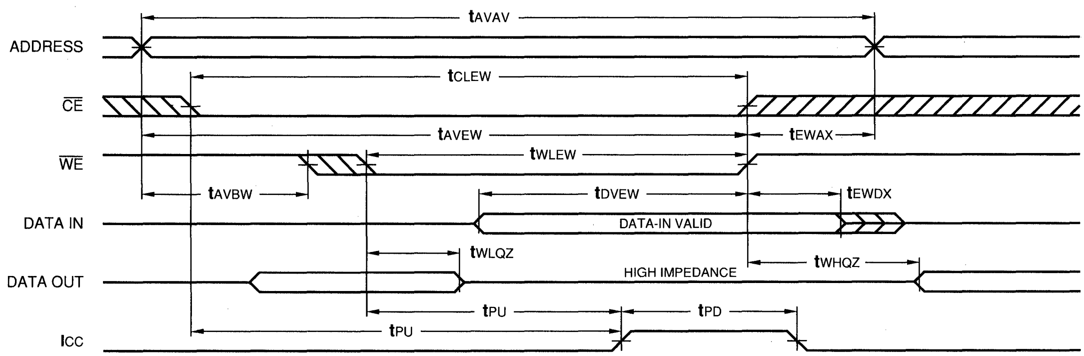


SWITCHING CHARACTERISTICS *Over Operating Range*

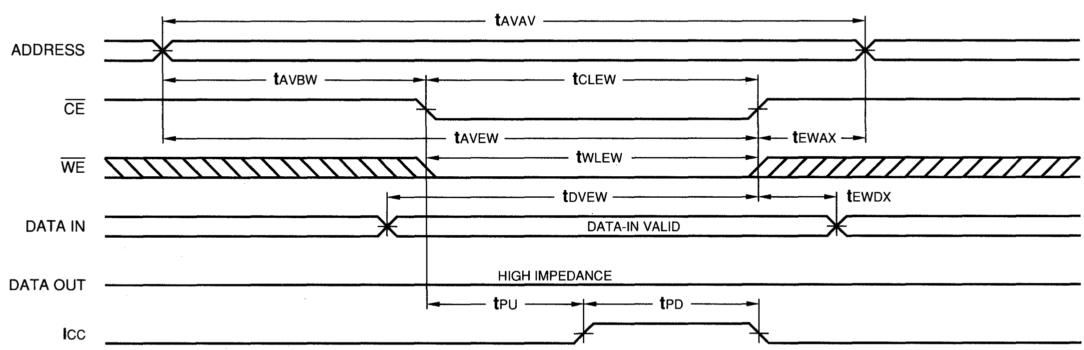
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

Symbol	Parameter	L7C164/166– 25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max
t_{AVAV}	Write Cycle Time	20		20		15		12	
t_{CLEW}	Chip Enable Low to End of Write Cycle	15		15		12		10	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	15		15		12		10	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	15		15		12		10	
t_{DVEW}	Data Valid to End of Write Cycle	10		10		7		6	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		7		5		4

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



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4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE}$ = V_{CC}.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ ≤ V_{IL}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ V_{IH}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

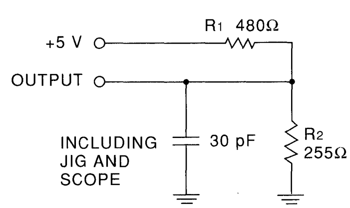


FIGURE 1b.

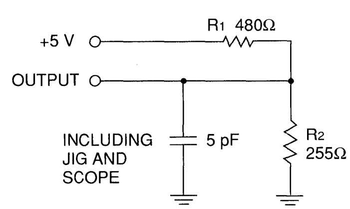
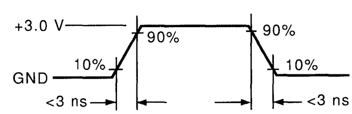


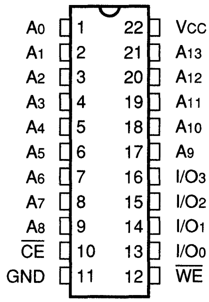
FIGURE 2.



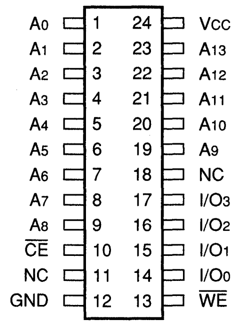
3

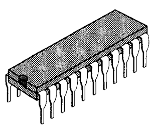
L7C164 — ORDERING INFORMATION

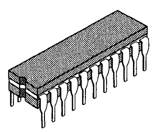
22-pin — 0.3" wide

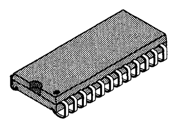


24-pin — 0.3" wide





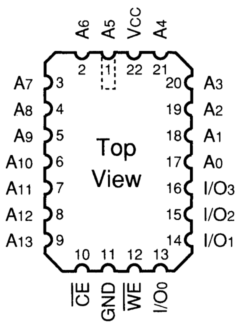


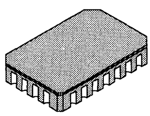


Speed	Plastic DIP (P8)	Ceramic DIP (C3)	Plastic SOJ (W1)
	0°C to +70°C — Commercial Screening		
20 ns	L7C164PC20	L7C164CC20	L7C164WC20
15 ns	L7C164PC15	L7C164CC15	L7C164WC15
12 ns	L7C164PC12	L7C164CC12	L7C164WC12
	–55°C to +125°C — Commercial Screening		
25 ns		L7C164CM25	
20 ns		L7C164CM20	
15 ns		L7C164CM15	
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns		L7C164CMB25	
20 ns		L7C164CMB20	
15 ns		L7C164CMB15	

L7C164 — ORDERING INFORMATION

22-pin

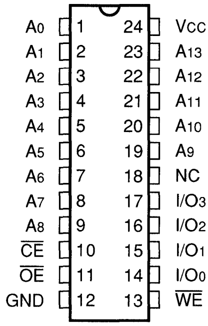


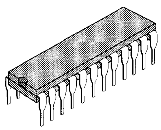


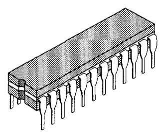
Speed	Ceramic Leadless Chip Carrier (K4)	
	0°C to +70°C — Commercial Screening	
20 ns	L7C164KC20	
15 ns	L7C164KC15	
12 ns	L7C164KC12	
	–55°C to +125°C — Commercial Screening	
25 ns	L7C164KM25	
20 ns	L7C164KM20	
15 ns	L7C164KM15	
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns	L7C164KMB25	
20 ns	L7C164KMB20	
15 ns	L7C164KMB15	

L7C166 — ORDERING INFORMATION

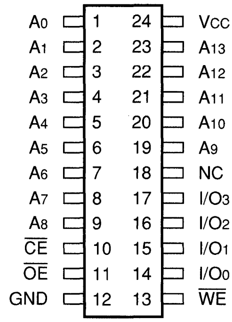
24-pin — 0.3" wide

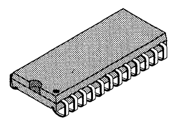






24-pin — 0.3" wide

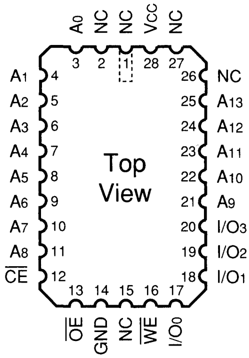


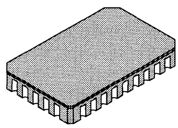


Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic SOJ (W1)
	0°C to +70°C — Commercial Screening		
20 ns	L7C166PC20	L7C166CC20	L7C166WC20
15 ns	L7C166PC15	L7C166CC15	L7C166WC15
12 ns	L7C166PC12	L7C166CC12	L7C166WC12
	–55°C to +125°C — Commercial Screening		
25 ns		L7C166CM25	
20 ns		L7C166CM20	
15 ns		L7C166CM15	
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns		L7C166CMB25	
20 ns		L7C166CMB20	
15 ns		L7C166CMB15	

L7C166 — ORDERING INFORMATION

28-pin





Speed	Ceramic Leadless Chip Carrier (K5)	
	0°C to +70°C — Commercial Screening	
20 ns	L7C166KC20	
15 ns	L7C166KC15	
12 ns	L7C166KC12	
	–55°C to +125°C — Commercial Screening	
25 ns	L7C166KM25	
20 ns	L7C166KM20	
15 ns	L7C166KM15	
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns	L7C166KMB25	
20 ns	L7C166KMB20	
15 ns	L7C166KMB15	

L7C185
8K x 8 Static RAM (Low Power)

FEATURES

- 8K x 8 Static RAM with Chip Select Powerdown, Output Enable
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 12 ns maximum
- Low Power Operation
  Active:
  425 mW typical at 25 ns
  Standby (typical):
  400µW (L7C185)
  200 µW (L7C185-L)
- Data Retention at 2 V for Battery Backup Operation
- DESC SMD No. 5962-38294
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with IDT7164, Cypress CY7C185/186
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Plastic SOJ
  - 28-pin Ceramic Flatpack
  - 28-pin Ceramic LCC
  - 32-pin Ceramic LCC

DESCRIPTION

The **L7C185** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 8,192 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. These devices are available in four speeds with maximum access times from 12 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption for the L7C185 is 425 mW (typical) at 25 ns. Dissipation drops to 60 mW (typical) for the L7C185 and 50 mW (typical) for the L7C185-L when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C185 and L7CL185-L consume only 30 µW and 15 µW (typical) respectively at 3 V, allowing effective battery backup operation.

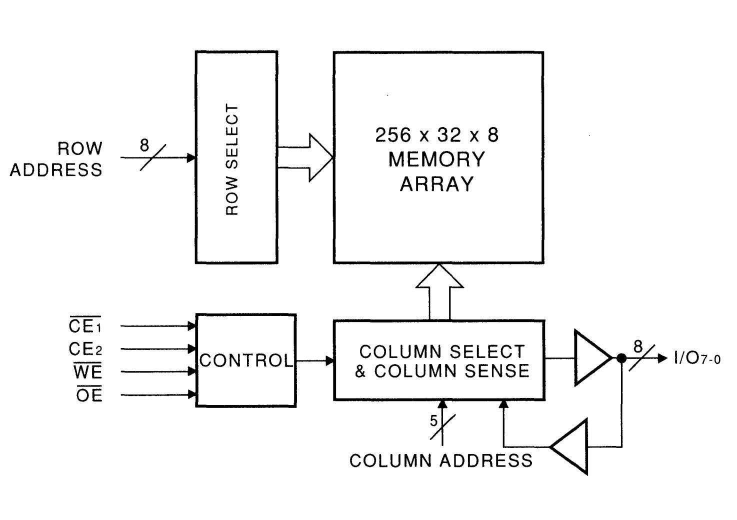
The L7C185 provides asynchronous (unclocked) operation with matching access and cycle times. Two Chip Enables (one active-low) and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{12}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE_1}$ and $\overline{OE}$ LOW, and CE_2 and $\overline{WE}$ HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE_1}$ or $\overline{OE}$ is HIGH, or CE_2 or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE_1}$ and $\overline{WE}$ inputs are both LOW, and CE_2 is HIGH. Any of these signals may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C185 can withstand an injection current of up to 200 mA on any pin without damage.

L7C185 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
VCC supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ VCC ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ VCC ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ VCC ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ VCC ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

			L7C185			L7C185-L			
Symbol	Parameter	Test Condition	Min	Typ	Max	Min	Typ	Max	Unit
VOH	Output High Voltage	VCC = 4.5 V, IOH = –4.0 mA	2.4			2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA			0.4			0.4	V
VIH	Input High Voltage		2.2		VCC +0.3	2.2		VCC +0.3	V
VIL	Input Low Voltage	(Note 3)	–3.0		0.8	–3.0		0.8	V
IIX	Input Leakage Current	Ground ≤ VIN ≤ VCC	–10		+10	–10		+10	μA
IOZ	Output Leakage Current	(Note 4)	–10		+10	–10		+10	μA
ICC2	VCC Current, TTL Inactive	(Note 7)		12	25		10	15	mA
ICC3	VCC Current, CMOS Standby	(Note 8)		80	300		40	150	μA
ICC4	VCC Current, Data Retention	VCC = 3.0 V (Note 9)		10	150		5	50	μA
CIN	Input Capacitance	Ambient Temp = 25°C, VCC = 5.0 V			5			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

			L7C185-				
Symbol	Parameter	Test Condition	25	20	15	12	Unit
ICC1	VCC Current, Active	(Note 6)	115	135	160	195	mA

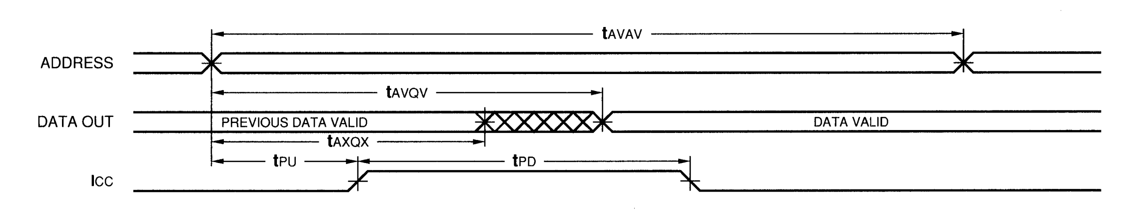
SWITCHING CHARACTERISTICS *Over Operating Range*

READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

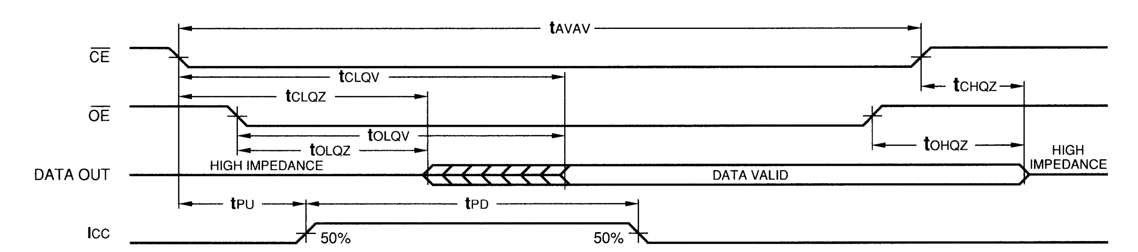
		L7C185–							
		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	25		20		15		12	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		25		20		15		12
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		25		20		15		12
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		10		8		8		5
t_{OLQV}	Output Enable Low to Output Valid		12		10		8		6
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		8		5		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		25		20		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

3

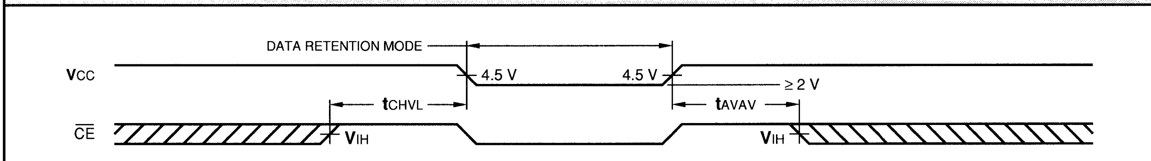
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}$/$\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

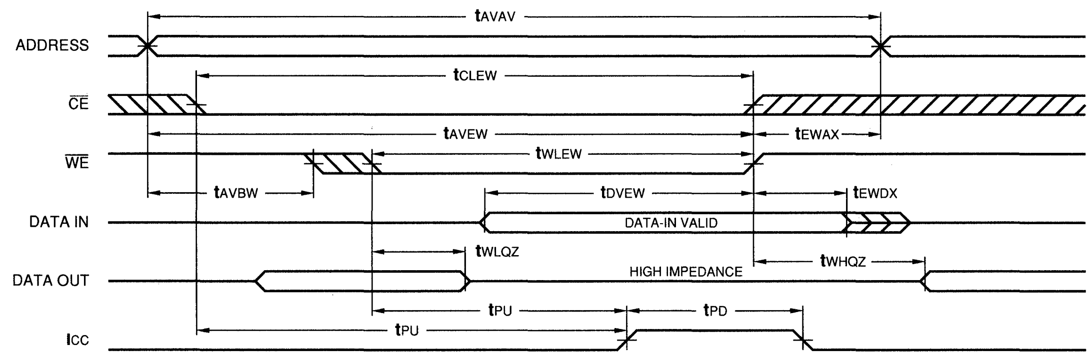


SWITCHING CHARACTERISTICS *Over Operating Range*

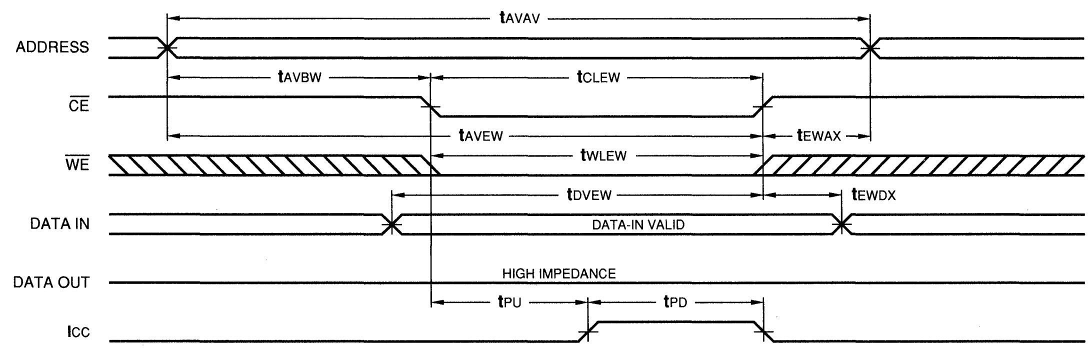
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C185–							
		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	20		20		15		12	
t_{CLEW}	Chip Enable Low to End of Write Cycle	15		15		12		10	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	15		15		12		10	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	15		15		12		10	
t_{DVEW}	Data Valid to End of Write Cycle	10		10		7		6	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		7		5		4

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE}_1$ = V_{CC}, CE_2 = GND.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}_1$ ≤ V_{IL}, CE_2 ≥ V_{IH}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}_1$ ≥ V_{IH}, CE_2 ≤ V_{IL}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}_1$ = V_{CC}, CE_2 = GND. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}_1$ must be ≥ V_{CC} – 0.2 V or CE_2 must be ≤ 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}_1$, CE_2, and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}_1$ low, CE_2 high).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}_1$ and CE_2 transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}_1$ and CE_2 active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}_1$ and CE_2 going active, the output remains in a high impedance state.

18. If $\overline{CE}_1$ and CE_2 goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Rising edge of CE_2 ($\overline{CE}_1$ active) or the falling edge of $\overline{CE}_1$ (CE_2 active).

b. Falling edge of $\overline{WE}$ ($\overline{CE}_1$, CE_2 active).

c. Transition on any address line ($\overline{CE}_1$, CE_2 active).

d. Transition on any data line ($\overline{CE}_1$, CE_2, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}_1$, CE_2, or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

3

FIGURE 1a.

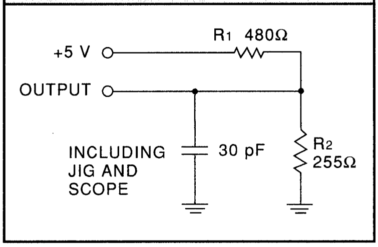


FIGURE 1b.

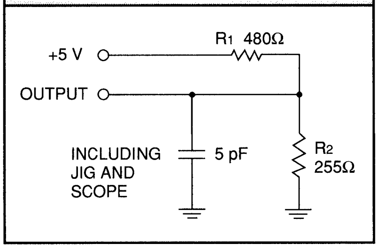
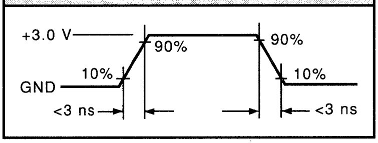
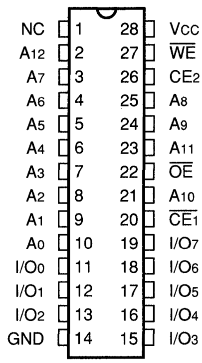


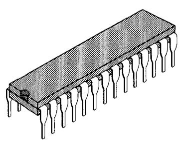
FIGURE 2.

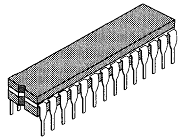


ORDERING INFORMATION

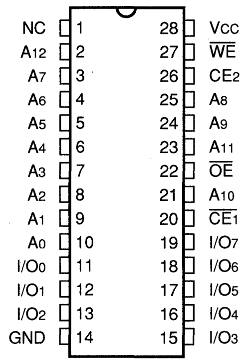
28-pin — 0.3" wide

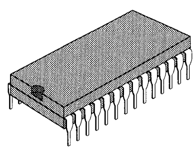


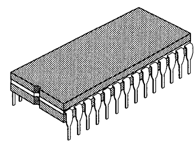




28-pin — 0.6" wide





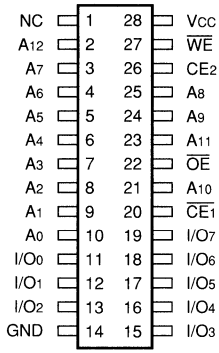


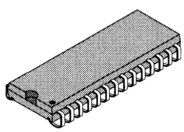
Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic DIP (P9)	Ceramic DIP (C6)
	0°C to +70°C — Commercial Screening			
20 ns	L7C185PC20*	L7C185CC20*	L7C185NC20*	L7C185IC20*
15 ns	L7C185PC15*	L7C185CC15*	L7C185NC15*	L7C185IC15*
12 ns	L7C185PC12*	L7C185CC12*	L7C185NC12*	L7C185IC12*
	–55°C to +125°C — Commercial Screening			
25 ns		L7C185CM25*		L7C185IM25*
20 ns		L7C185CM20*		L7C185IM20*
15 ns		L7C185CM15*		L7C185IM15*
	–55°C to +125°C — MIL-STD-883 Compliant			
25 ns		L7C185CMB25*		L7C185IMB25*
20 ns		L7C185CMB20*		L7C185IMB20*
15 ns		L7C185CMB15*		L7C185IMB15*

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C185CMB15L)**

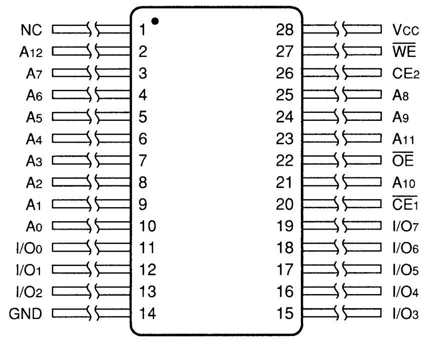
ORDERING INFORMATION

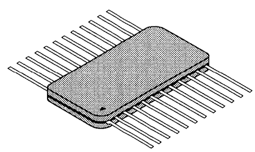
28-pin — 0.3" wide





28-pin



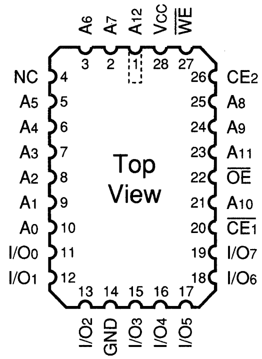


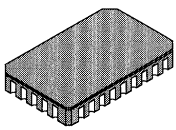
Speed	Plastic SOJ (W2)	Ceramic Flatpack (M2)
	0°C to +70°C — Commercial Screening	
20 ns	L7C185WC20*	L7C185MC20*
15 ns	L7C185WC15*	L7C185MC15*
12 ns	L7C185WC12*	L7C185MC12*
	–55°C to +125°C — Commercial Screening	
25 ns		L7C185MM25*
20 ns		L7C185MM20*
15 ns		L7C185MM15*
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns		L7C185MMB25*
20 ns		L7C185MMB20*
15 ns		L7C185MMB15*

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C185MMB15L)**

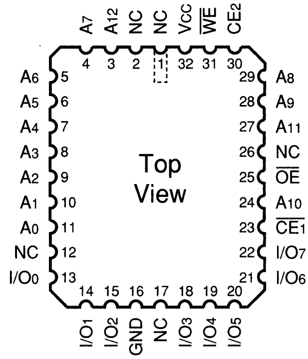
ORDERING INFORMATION

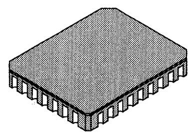
28-pin





32-pin





Speed	Ceramic Leadless Chip Carrier (K5)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — COMMERCIAL SCREENING	
20 ns	L7C185KC20*	L7C185TC20*
15 ns	L7C185KC15*	L7C185TC15*
12 ns	L7C185KC12*	L7C185TC12*
	–55°C to +125°C — COMMERCIAL SCREENING	
25 ns	L7C185KM25*	L7C185TM25*
20 ns	L7C185KM20*	L7C185TM20*
15 ns	L7C185KM15*	L7C185TM15*
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
25 ns	L7C185KMB25*	L7C185TMB25*
20 ns	L7C185KMB20*	L7C185TMB20*
15 ns	L7C185KMB15*	L7C185TMB15*

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C185KMB15L)**

256K Static RAMs

4

L7C197
256K x 1 Static RAM

FEATURES

- ❑ 256K x 1 Static RAM with Separate I/O, Chip Select Powerdown
- ❑ Auto-Powerdown™ Design
- ❑ Advanced CMOS Technology
- ❑ High Speed — to 15 ns maximum
- ❑ Low Power Operation
  Active: 165 mW typical at 35 ns
  Standby: 5 mW typical
- ❑ Data Retention at 2 V for Battery Backup Operation
- ❑ DESC SMD No. 5962-88544
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Plug Compatible with IDT71257, Cypress CY7C197
- ❑ Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Ceramic DIP
  - 24-pin Plastic SOJ
  - 28-pin Ceramic LCC

DESCRIPTION

The **L7C197** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 262,144 words by 1 bit per word. This device is available in four speeds with maximum access times from 15 ns to 35 ns.

Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 165 mW (typical) at 35 ns. Dissipation drops to 50 mW (typical) when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C197 consumes only 150 µW (typical) at 3 V, allowing effective battery backup operation.

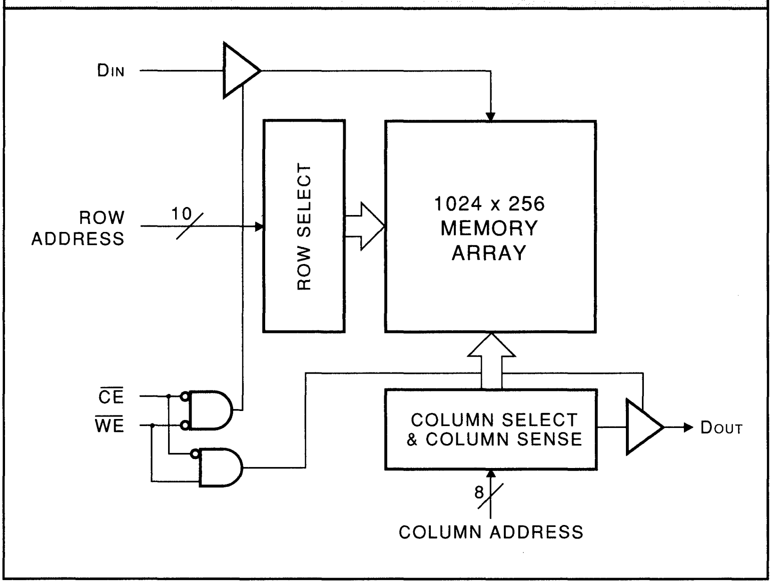
The L7C197 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state output simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A0 through A17. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ LOW while $\overline{WE}$ remains HIGH. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ is HIGH or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both LOW. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C197 can withstand an injection current of up to 200 mA on any pin without damage.

L7C197 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature .... –65°C to +150°C
Operating ambient temperature .... –55°C to +125°C
VCC supply voltage with respect to ground .... –0.5 V to +7.0 V
Input signal with respect to ground .... –3.0 V to +7.0 V
Signal applied to high impedance output .... –3.0 V to +7.0 V
Output current into low outputs .... 25 mA
Latchup current .... > 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ VCC ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ VCC ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ VCC ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ VCC ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

			L7C197			
Symbol	**Parameter**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
VOH	Output High Voltage	VCC = 4.5 V, IOH = –4.0 mA	2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA			0.4	V
VIH	Input High Voltage		2.2		VCC +0.3	V
VIL	Input Low Voltage	(Note 3)	–3.0		0.8	V
IIX	Input Leakage Current	Ground ≤ VIN ≤ VCC	–10		+10	μA
IOZ	Output Leakage Current	(Note 4)	–10		+10	μA
ICC2	VCC Current, TTL Inactive	(Note 7)		10	20	mA
ICC3	VCC Current, CMOS Standby	(Note 8)		1	3	mA
ICC4	VCC Current, Data Retention	VCC = 3.0 V (Note 9)		50	200	μA
CIN	Input Capacitance	Ambient Temp = 25°C, VCC = 5.0 V			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

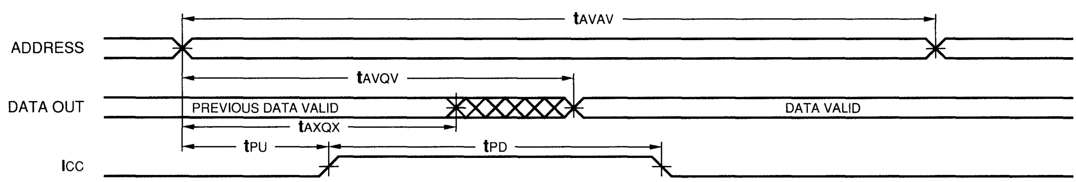
			L7C197-				
Symbol	**Parameter**	**Test Condition**	**35**	**25**	**20**	**15**	**Unit**
ICC1	VCC Current, Active	(Note 6)	75	100	125	160	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

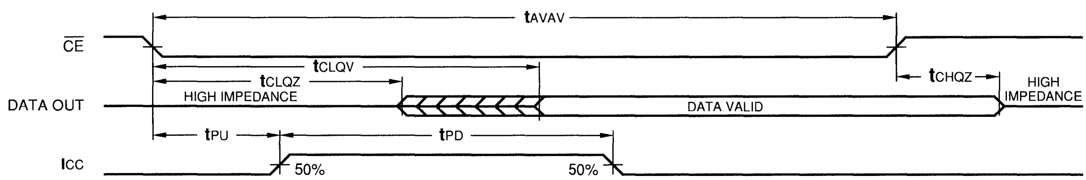
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C197–							
		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	35		25		20		15	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		35		25		20		15
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		35		25		20		15
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		15		10		8		8
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		35		25		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

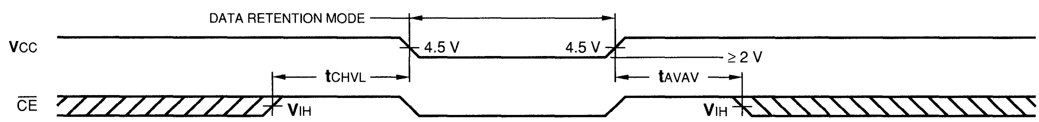
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

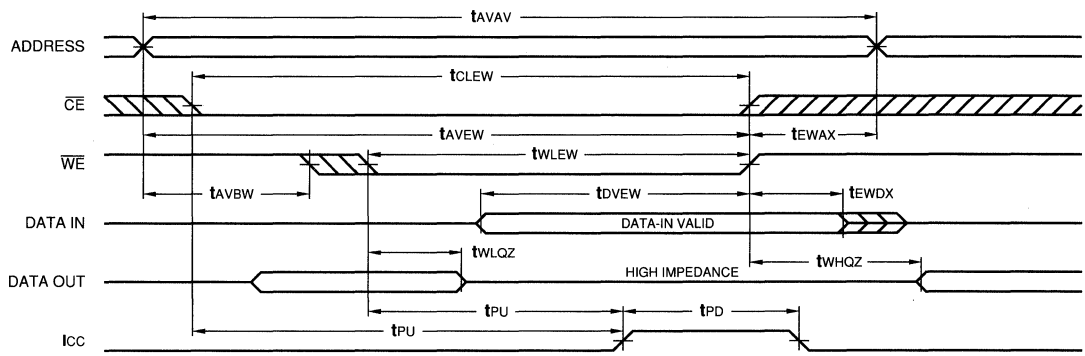


SWITCHING CHARACTERISTICS *Over Operating Range*

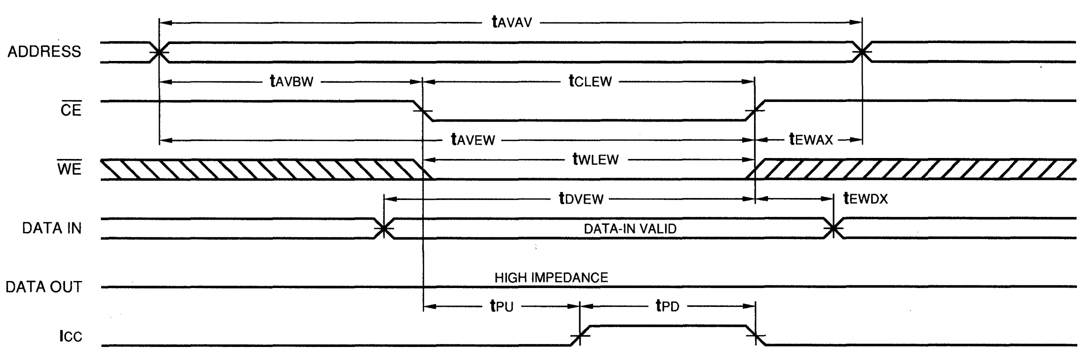
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C197–							
		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	25		20		20		15	
t_{CLEW}	Chip Enable Low to End of Write Cycle	25		15		15		12	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	25		15		15		12	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	20		15		15		12	
t_{DVEW}	Data Valid to End of Write Cycle	15		10		10		7	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		10		7		7		5

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE}$ = V_{CC}.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ ≤ V_{IL}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ V_{IH}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

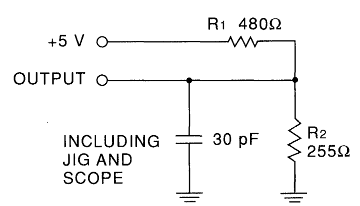


FIGURE 1b.

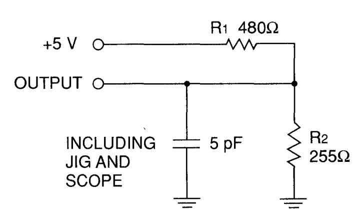
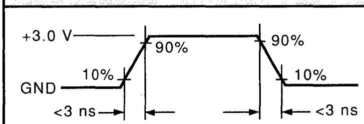


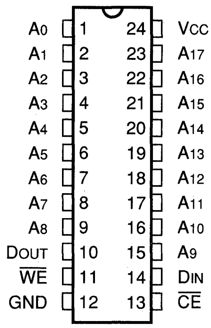
FIGURE 2.

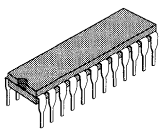


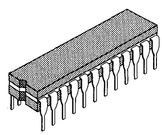
4

ORDERING INFORMATION

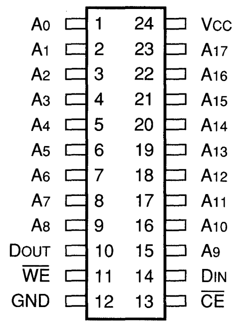
24-pin — 0.3" wide

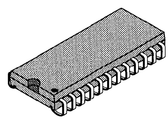






24-pin — 0.3" wide

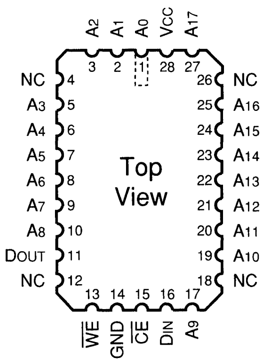


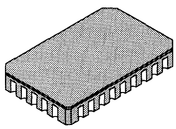


Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic SOJ (W1)
	0°C to +70°C — Commercial Screening		
25 ns	L7C197PC25	L7C197CC25	L7C197WC25
20 ns	L7C197PC20	L7C197CC20	L7C197WC20
15 ns	L7C197PC15	L7C197CC15	L7C197WC15
	–55°C to +125°C — Commercial Screening		
35 ns		L7C197CM35	
25 ns		L7C197CM25	
20 ns		L7C197CM20	
	–55°C to +125°C — MIL-STD-883 Compliant		
35 ns		L7C197CMB35	
25 ns		L7C197CMB25	
20 ns		L7C197CMB20	

ORDERING INFORMATION

28-pin





Speed	Ceramic Leadless Chip Carrier (K5)	
	0°C to +70°C — Commercial Screening	
25 ns	L7C197KC25	
20 ns	L7C197KC20	
15 ns	L7C197KC15	
	–55°C to +125°C — Commercial Screening	
35 ns	L7C197KM35	
25 ns	L7C197KM25	
20 ns	L7C197KM20	
	–55°C to +125°C — MIL-STD-883 Compliant	
35 ns	L7C197KMB35	
25 ns	L7C197KMB25	
20 ns	L7C197KMB20	

LOGIC DEVICES INCORPORATED

L7C194/195
64K x 4 Static RAM

FEATURES

- ❑ 64K x 4 Static RAM with Common I/O
- ❑ Auto-Powerdown™ Design
- ❑ Advanced CMOS Technology
- ❑ High Speed — to 15 ns maximum
- ❑ Low Power Operation
  Active: 210 mW typical at 35 ns
  Standby: 5 mW typical
- ❑ Data retention at 2 V for Battery Backup Operation
- ❑ DESC SMD No.
  5962-88681 — L7C194
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Plug Compatible with IDT 71258/61298 and Cypress CY7C194/195
- ❑ Package Styles Available:
  - 24/28-pin Plastic DIP
  - 24/28-pin Ceramic DIP
  - 24/28-pin Plastic SOJ
  - 28-pin Ceramic LCC

DESCRIPTION

The **L7C194** and **L7C195** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 65,536 words by 4 bits per word. Data In and Data Out signals share I/O pins. The L7C194 has a single active-low Chip Enable. The L7C195 has a single Chip Enable and an Output Enable. These devices are available in four speeds with maximum access times from 15 ns to 35 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 210 mW (typical) at 35 ns. Dissipation drops to 50 mW (typical) when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C194 and L7C195 consume only 150 µW (typical) at 3 V, allowing effective battery backup operation.

The L7C194 and L7C195 provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{15}. For the L7C194, reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ LOW while $\overline{WE}$ remains HIGH. For the L7C195, $\overline{CE}$ and $\overline{OE}$ must be LOW. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is HIGH, or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are LOW. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C194 and L7C195 can withstand an injection current of up to 200 mA on any pin without damage.

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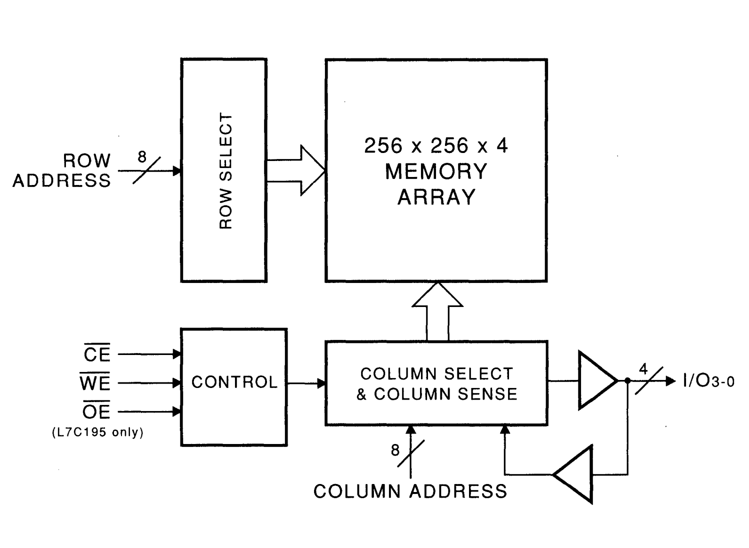
L7C194/195 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
VCC supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ VCC ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ VCC ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ VCC ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ VCC ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

			L7C194/195			
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	VCC = 4.5 V, IOH = –4.0 mA	2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA			0.4	V
VIH	Input High Voltage		2.2		VCC +0.3	V
VIL	Input Low Voltage	(Note 3)	–3.0		0.8	V
IIX	Input Leakage Current	Ground ≤ VIN ≤ VCC	–10		+10	μA
IOZ	Output Leakage Current	(Note 4)	–10		+10	μA
ICC2	VCC Current, TTL Inactive	(Note 7)		10	20	mA
ICC3	VCC Current, CMOS Standby	(Note 8)		1	3	mA
ICC4	VCC Current, Data Retention	VCC = 3.0 V (Note 9)		50	200	μA
CIN	Input Capacitance	Ambient Temp = 25°C, VCC = 5.0 V			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

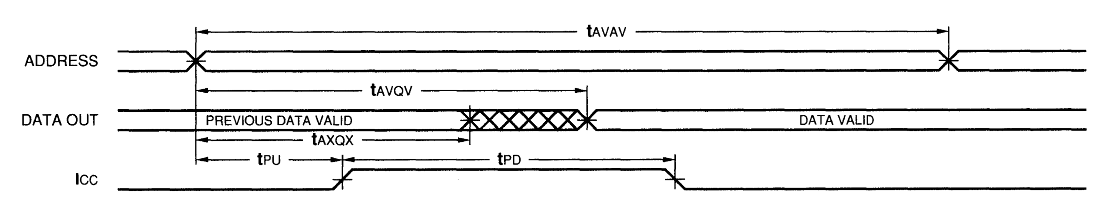
			L7C194/195-				
Symbol	Parameter	Test Condition	35	25	20	15	Unit
ICC1	VCC Current, Active	(Note 6)	75	100	125	160	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

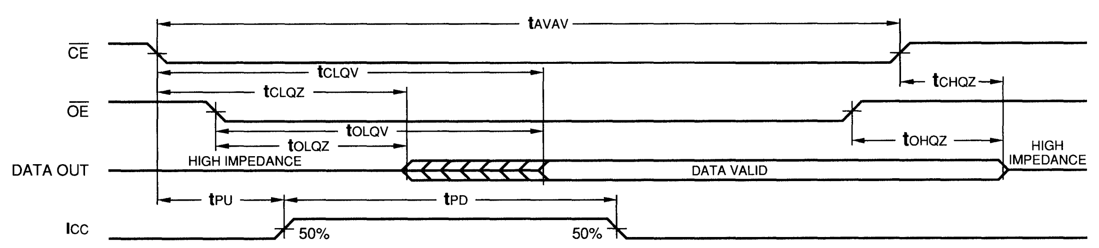
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C194/195–							
		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	35		25		20		15	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		35		25		20		15
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		35		25		20		15
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		15		10		8		8
t_{OLQV}	Output Enable Low to Output Valid		15		12		10		8
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		10		8		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		35		25		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

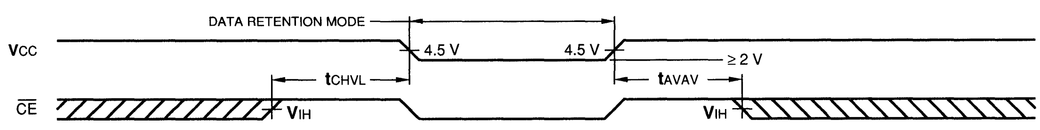
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}/\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

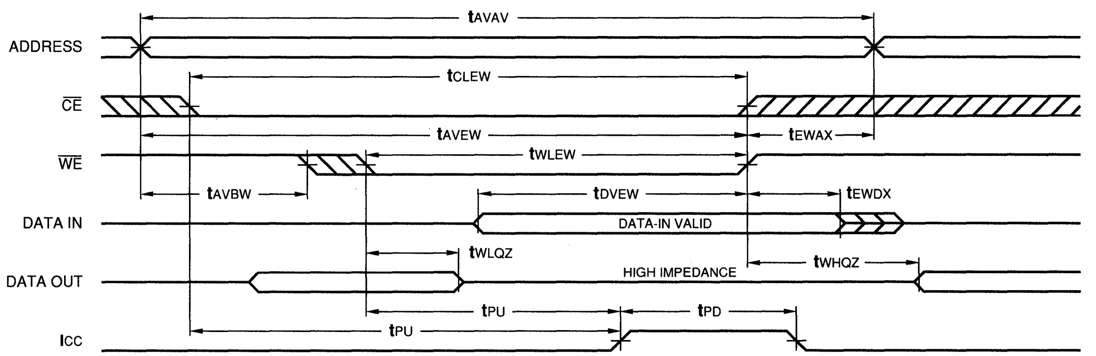


SWITCHING CHARACTERISTICS *Over Operating Range*

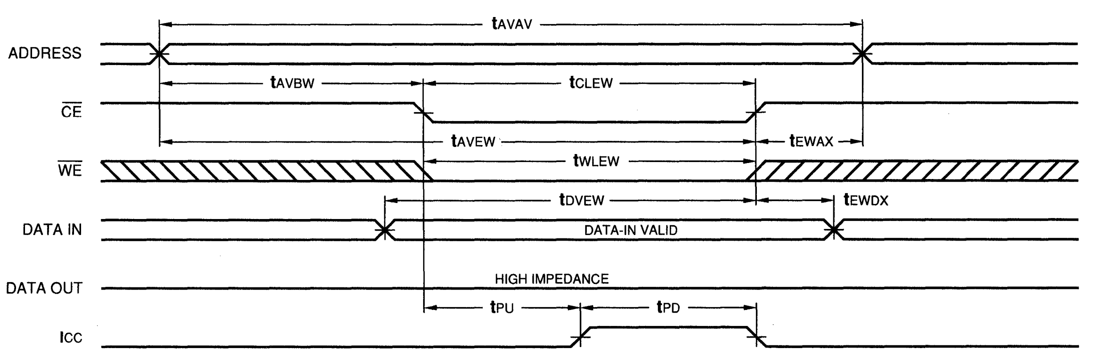
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C194/195–							
		35		25		20		15	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{AVAV}	Write Cycle Time	25		20		20		15	
t_{CLEW}	Chip Enable Low to End of Write Cycle	25		15		15		12	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	25		15		15		12	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	20		15		15		12	
t_{DVEW}	Data Valid to End of Write Cycle	15		10		10		7	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		10		7		7		5

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND $\leq V_{OUT} \leq V_{CC}$. The device is disabled, i.e., $\overline{CE} = V_{CC}$.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \leq V_{IL}$, $\overline{WE} \leq V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \geq V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\geq V_{CC} - 0.2$ V. All other inputs must meet $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

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FIGURE 1a.

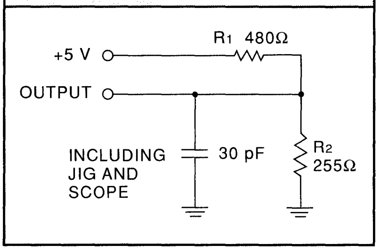


FIGURE 1b.

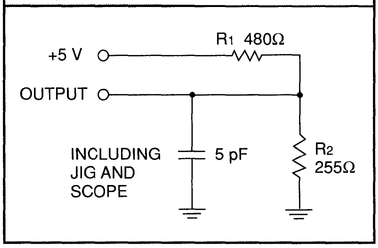
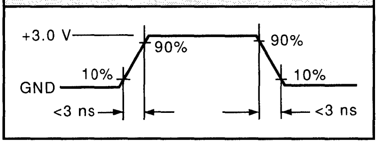
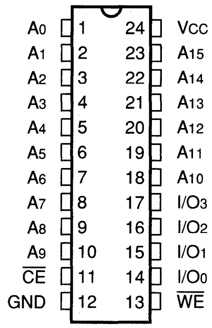


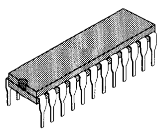
FIGURE 2.

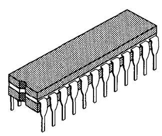


L7C194 — ORDERING INFORMATION

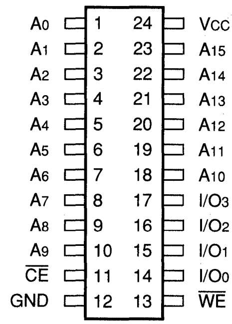
24-pin — 0.3" wide

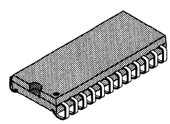






24-pin — 0.3" wide

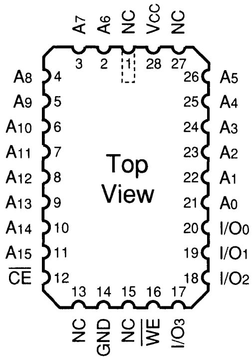


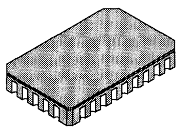


Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic SOJ (W1)
	0°C to +70°C — Commercial Screening		
25 ns	L7C194PC25	L7C194CC25	L7C194WC25
20 ns	L7C194PC20	L7C194CC20	L7C194WC20
15 ns	L7C194PC15	L7C194CC15	L7C194WC15
	–55°C to +125°C — Commercial Screening		
35 ns		L7C194CM35	
25 ns		L7C194CM25	
20 ns		L7C194CM20	
	–55°C to +125°C — MIL-STD-883 Compliant		
35 ns		L7C194CMB35	
25 ns		L7C194CMB25	
20 ns		L7C194CMB20	

L7C194 — ORDERING INFORMATION

28-pin





Speed	Ceramic Leadless Chip Carrier (K5)	
	0°C to +70°C — Commercial Screening	
25 ns	L7C194KC25	
20 ns	L7C194KC20	
15 ns	L7C194KC15	
	–55°C to +125°C — Commercial Screening	
35 ns	L7C194KM35	
25 ns	L7C194KM25	
20 ns	L7C194KM20	
	–55°C to +125°C — MIL-STD-883 Compliant	
35 ns	L7C194KMB35	
25 ns	L7C194KMB25	
20 ns	L7C194KMB20	

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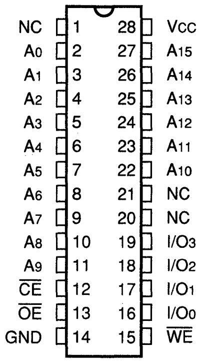
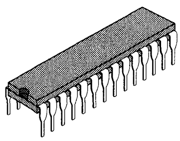
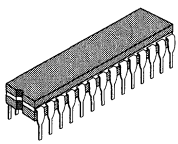
L7C195 — ORDERING INFORMATION

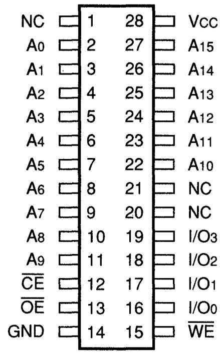
28-pin — 0.3" wide

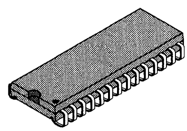






28-pin — 0.3" wide





Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic SOJ (W2)
0°C to +70°C — Commercial Screening			
25 ns	L7C195PC25	L7C195CC25	L7C195WC25
20 ns	L7C195PC20	L7C195CC20	L7C195WC20
15 ns	L7C195PC15	L7C195CC15	L7C195WC15
–55°C to +125°C — Commercial Screening			
35 ns		L7C195CM35	
25 ns		L7C195CM25	
20 ns		L7C195CM20	
–55°C to +125°C — MIL-STD-883 Compliant			
35 ns		L7C195CMB35	
25 ns		L7C195CMB25	
20 ns		L7C195CMB20	

L7C199
32K x 8 Static RAM (Low Power)

FEATURES

- 32K x 8 Static RAM with Chip Select Powerdown, Output Enable
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 15 ns maximum
- Low Power Operation
  Active:
  350 mW typical at 35 ns
  Standby (typical):
  5 mW (L7C199)
  0.5 mW (L7C199-L)
- Data Retention at 2 V for Battery Backup Operation
- DESC SMD No.
  5962-88662 — L7C199
  5962-88552 — L7C199-L
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with IDT71256, Cypress CY7C198/199
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Plastic SOJ
  - 28-pin Ceramic Flatpack
  - 28-pin Ceramic LCC
  - 32-pin Ceramic LCC

DESCRIPTION

The **L7C199** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 32,768 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. These devices are available in four speeds with maximum access times from 15 ns to 35 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption for the L7C199 is 350 mW (typical) at 35 ns. Dissipation drops to 50 mW (typical) for the L7C199 and 25 mW (typical) for the L7C199-L when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C199 and L7C199-L consume only 150 µW and 30µW (typical) respectively, at 3 V, allowing effective battery backup operation.

The L7C199 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

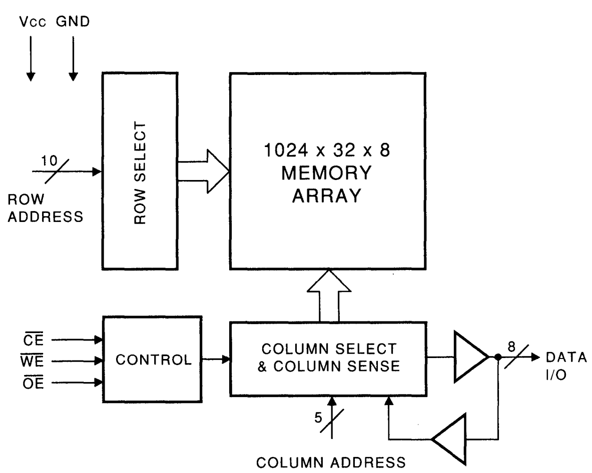
Memory locations are specified on address pins A_0 through A_{14}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ and $\overline{OE}$ LOW while $\overline{WE}$ remains HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is HIGH, or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both LOW. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C199 can withstand an injection current of up to 200 mA on any pin without damage.

4

L7C199 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
VCC supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ VCC ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ VCC ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ VCC ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ VCC ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

			L7C199			L7C199-L			
Symbol	**Parameter**	**Test Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
VOH	Output High Voltage	VCC = 4.5 V, IOH = –4.0 mA	2.4			2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA			0.4			0.4	V
VIH	Input High Voltage		2.2		VCC +0.3	2.2		VCC +0.3	V
VIL	Input Low Voltage	(Note 3)	–3.0		0.8	–3.0		0.8	V
IIX	Input Leakage Current	Ground ≤ VIN ≤ VCC	–10		+10	–10		+10	μA
IOZ	Output Leakage Current	(Note 4)	–10		+10	–10		+10	μA
ICC2	VCC Current, TTL Inactive	(Note 7)		10	20		5	10	mA
ICC3	VCC Current, CMOS Standby	(Note 8)		1	3		0.1	0.5	mA
ICC4	VCC Current, Data Retention	VCC = 3.0 V (Note 9)		50	200		10	75	μA
CIN	Input Capacitance	Ambient Temp = 25°C, VCC = 5.0 V			5			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

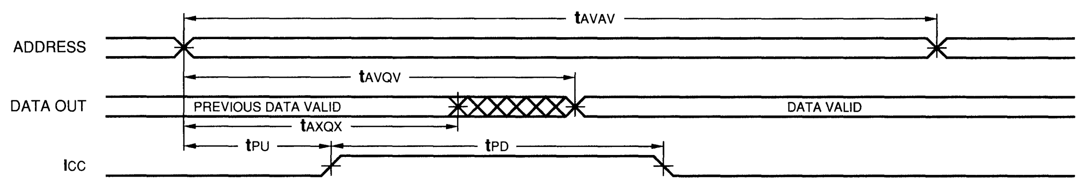
			L7C199-				
Symbol	**Parameter**	**Test Condition**	**35**	**25**	**20**	**15**	**Unit**
ICC1	VCC Current, Active	(Note 6)	95	120	145	180	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

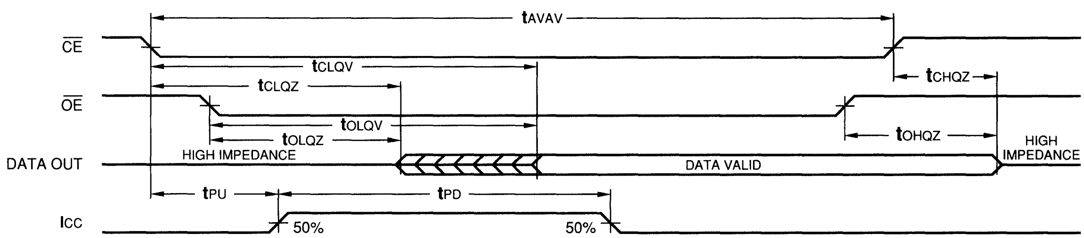
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C199–							
		35		25		20		15	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{AVAV}	Read Cycle Time	35		25		20		15	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		35		25		20		15
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		35		25		20		15
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		15		10		8		8
t_{OLQV}	Output Enable Low to Output Valid		15		12		10		8
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		10		8		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		35		25		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

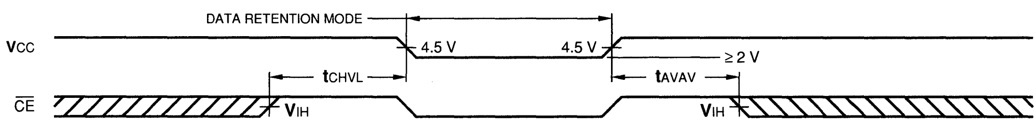
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}/\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

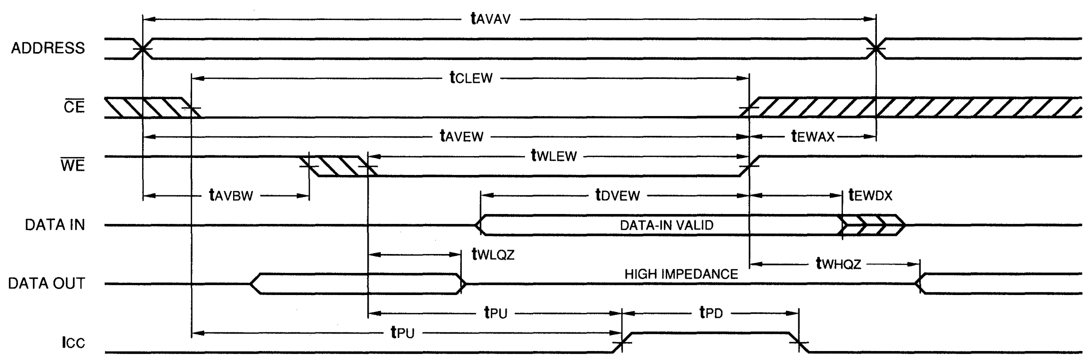


SWITCHING CHARACTERISTICS *Over Operating Range*

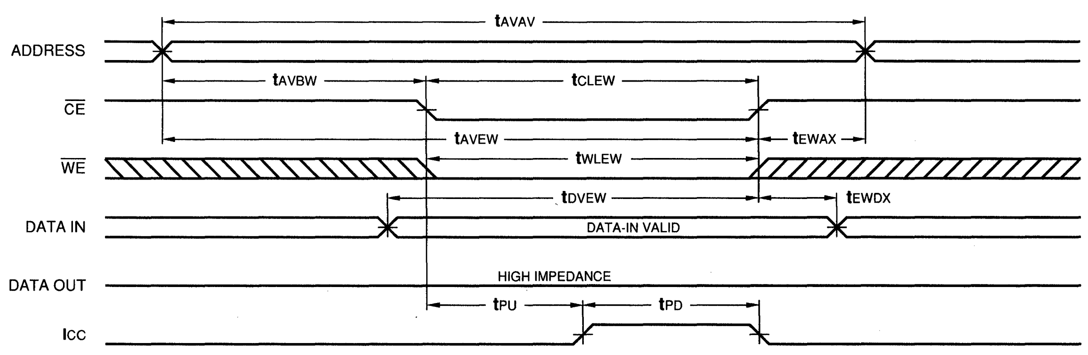
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C199–							
		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	25		20		20		15	
t_{CLEW}	Chip Enable Low to End of Write Cycle	25		15		15		12	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	25		15		15		12	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	20		15		15		12	
t_{DVEW}	Data Valid to End of Write Cycle	15		10		10		7	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		10		7		7		5

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE}$ = V_{CC}.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ ≤ V_{IL}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ V_{IH}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

4

FIGURE 1a.

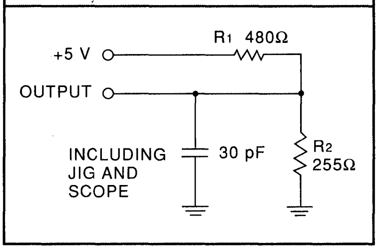


FIGURE 1b.

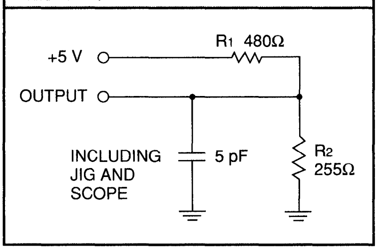
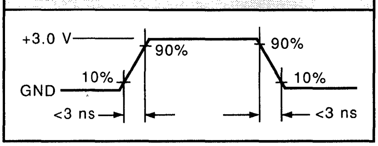
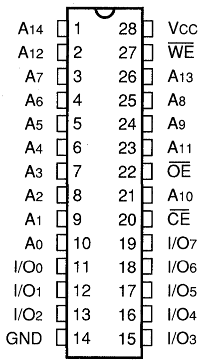


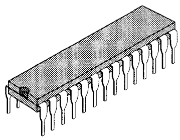
FIGURE 2.

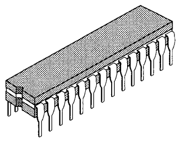


ORDERING INFORMATION

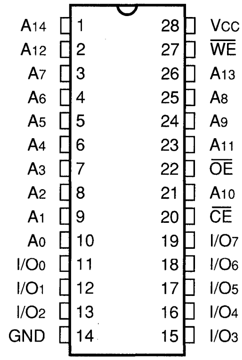
28-pin — 0.3" wide

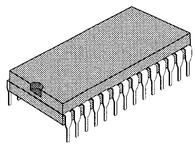


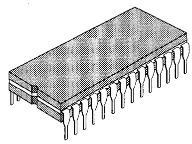




28-pin — 0.6" wide







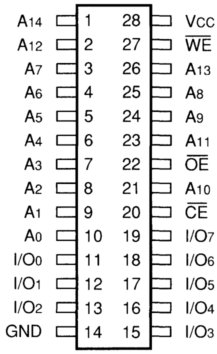
Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic DIP (P9)	Ceramic DIP (C6)
	0°C to +70°C — Commercial Screening			
25 ns	L7C199PC25*	L7C199CC25*	L7C199NC25*	L7C199IC25*
20 ns	L7C199PC20*	L7C199CC20*	L7C199NC20*	L7C199IC20*
15 ns	L7C199PC15*	L7C199CC15*	L7C199NC15*	L7C199IC15*
	–55°C to +125°C — Commercial Screening			
35 ns		L7C199CM35*		L7C199IM35*
25 ns		L7C199CM25*		L7C199IM25*
20 ns		L7C199CM20*		L7C199IM20*
	–55°C to +125°C — MIL-STD-883 Compliant			
35 ns		L7C199CMB35*		L7C199IMB35*
25 ns		L7C199CMB25*		L7C199IMB25*
20 ns		L7C199CMB20*		L7C199IMB20*

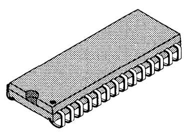
***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C199CMB20L)**

4

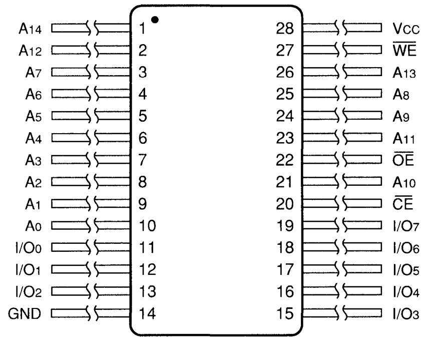
ORDERING INFORMATION

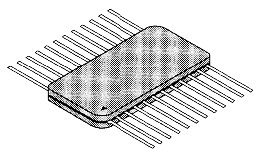
28-pin — 0.3" wide





28-pin



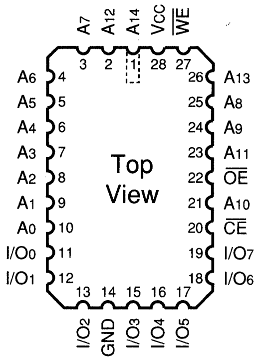


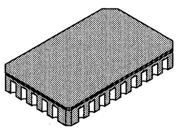
Speed	Plastic SOJ (W2)	Ceramic Flatpack (M2)
	0°C to +70°C — Commercial Screening	
25 ns	L7C199WC25*	L7C199MC25*
20 ns	L7C199WC20*	L7C199MC20*
15 ns	L7C199WC15*	L7C199MC15*
	–55°C to +125°C — Commercial Screening	
35 ns		L7C199MM35*
25 ns		L7C199MM25*
20 ns		L7C199MM20*
	–55°C to +125°C — MIL-STD-883 Compliant	
35 ns		L7C199MMB35*
25 ns		L7C199MMB25*
20 ns		L7C199MMB20*

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C199MMB20L)**

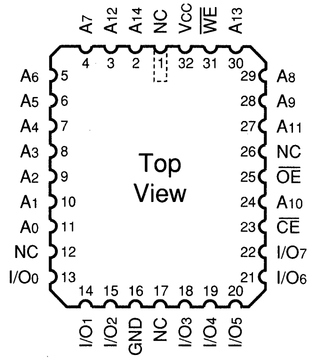
ORDERING INFORMATION

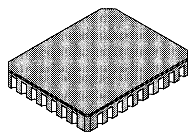
28-pin





32-pin





Speed	Ceramic Leadless Chip Carrier (K5)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening	
25 ns	L7C199KC25*	L7C199TC25*
20 ns	L7C199KC20*	L7C199TC20*
15 ns	L7C199KC15*	L7C199TC15*
	–55°C to +125°C — Commercial Screening	
35 ns	L7C199KM35*	L7C199TM35*
25 ns	L7C199KM25*	L7C199TM25*
20 ns	L7C199KM20*	L7C199TM20*
	–55°C to +125°C — MIL-STD-883 Compliant	
35 ns	L7C199KMB35*	L7C199TMB35*
25 ns	L7C199KMB25*	L7C199TMB25*
20 ns	L7C199KMB20*	L7C199TMB20*

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C199KMB20L)**

1M Static RAMs

5

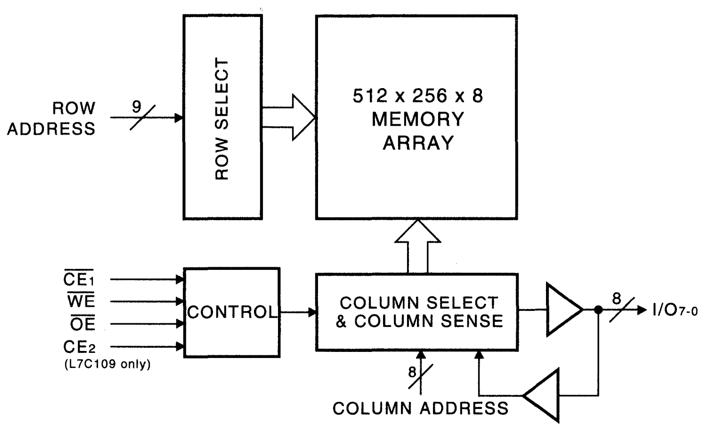
L7C108/109

128K x 8 Static RAM (Low Power)

FEATURES

- ❑ 128K x 8 Static RAM with Chip Select Powerdown, Output Enable
- ❑ Auto-Powerdown™ Design
- ❑ Advanced CMOS Technology
- ❑ High Speed — to 15 ns maximum
- ❑ Low Power Operation
  Active:
  550 mW typical at 25 ns
  Standby (typical):
  5 mW (L7C108/109)
  0.5 mW (L7C108-L/109-L)
- ❑ Data Retention at 2 V for Battery Backup Operation
- ❑ DESC SMD No. 5962-89598
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Plug Compatible with Cypress CY7C108/109, IDT71024/71B024, Micron MT5C1008, Motorola MCM6226A/62L26A, Sony CXK581020
- ❑ Package Styles Available:
  - 32-pin Plastic DIP
  - 32-pin Sidebraze, Hermetic DIP
  - 32-pin Plastic SOJ
  - 32-pin Ceramic SOJ
  - 32-pin Ceramic LCC

L7C108/109 Block Diagram



DESCRIPTION

The **L7C108** and **L7C109** are high-performance, low-power CMOS static RAMs. The storage circuitry is organized as 131,072 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. The L7C108 has a single active-low Chip Enable. The L7C109 has two Chip Enables (one active-low). These devices are available in four speeds with maximum access times from 15 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 550 mW (typical) at 25 ns. Dissipation drops to 50 mW (typical) and 25 mW (typical) for the low-powered versions when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C108/L7C109 and L7CL108-L/L7C109-L consume only 1.5 mW and 60 µW (typical) respectively, at 3 V, allowing effective battery backup operation.

The L7C108 and L7C109 provide asynchronous (unclocked) operation with matching access and cycle times. The Chip Enables and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{16}. For the L7C108, reading from a designated location is accomplished by presenting an address and driving $\overline{CE}_1$ and $\overline{OE}$ LOW while $\overline{WE}$ remains HIGH. For the L7C109, $\overline{CE}_1$ and $\overline{OE}$ must be LOW while CE_2 and $\overline{WE}$ are HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE}_1$ or $\overline{OE}$ is HIGH, or CE_2 (L7C109) or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE}_1$ and $\overline{WE}$ inputs are both LOW, and CE_2 (L7C109) is HIGH. Any of these signals may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C108 and L7C109 can withstand an injection current of up to 200 mA on any pin without damage.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature .... –65°C to +150°C
Operating ambient temperature .... –55°C to +125°C
VCC supply voltage with respect to ground .... –0.5 V to +7.0 V
Input signal with respect to ground .... –3.0 V to +7.0 V
Signal applied to high impedance output .... –3.0 V to +7.0 V
Output current into low outputs .... 25 mA
Latchup current .... > 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ VCC ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ VCC ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ VCC ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ VCC ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C108/109			L7C108-L/109-L			
Symbol	Parameter	Test Condition	Min	Typ	Max	Min	Typ	Max	Unit
VOH	Output High Voltage	VCC = 4.5 V, IOH = –4.0 mA	2.4			2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA			0.4			0.4	V
VIH	Input High Voltage		2.2		VCC +0.3	2.2		VCC +0.3	V
VIL	Input Low Voltage	(Note 3)	–3.0		0.8	–3.0		0.8	V
IIX	Input Leakage Current	GND ≤ VIN ≤ VCC	–10		+10	–10		+10	μA
IOZ	Output Leakage Current	(Note 4)	–10		+10	–10		+10	μA
ICC2	VCC Current, TTL Inactive	(Note 7)		10	20		5	10	mA
ICC3	VCC Current, CMOS Standby	(Note 8)		1	3.0		0.1	0.5	mA
ICC4	VCC Current, Data Retention	VCC = 3.0 V (Note 9)		500	1000		20	100	μA
CIN	Input Capacitance	Ambient Temp = 25°C, VCC = 5.0 V			5			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

			L7C108/109-				
Symbol	Parameter	Test Condition	25	20	17	15	Unit
ICC1	VCC Current, Active	(Note 6)	145	180	210	215	mA

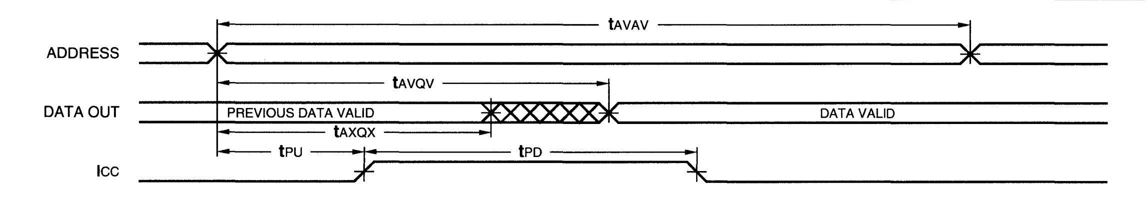
SWITCHING CHARACTERISTICS *Over Operating Range*

READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

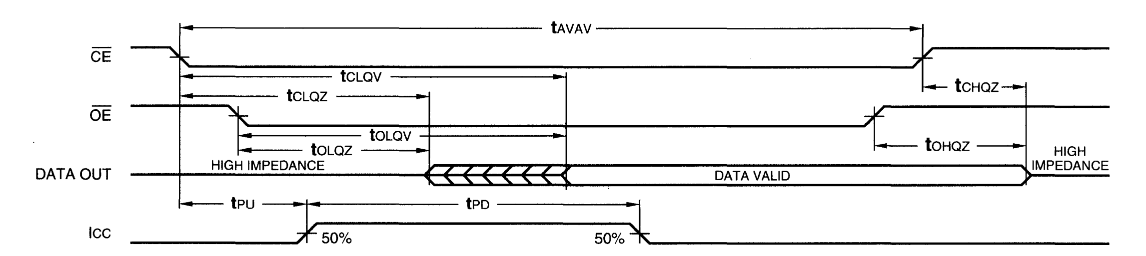
		L7C108/109–							
		25		20		17		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	25		20		17		15	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		25		20		17		15
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		25		20		17		15
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		10		8		8		7
t_{OLQV}	Output Enable Low to Output Valid		10		10		9		7
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		7		6		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		25		20		17		15
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

5

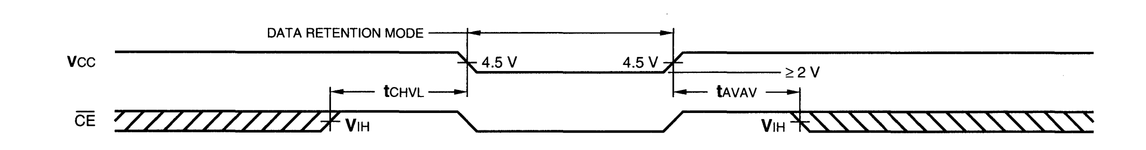
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}/\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

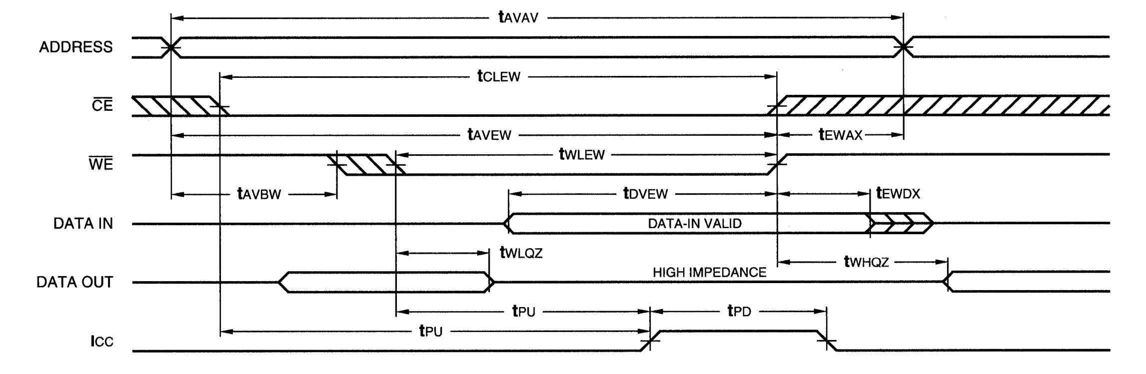


SWITCHING CHARACTERISTICS *Over Operating Range*

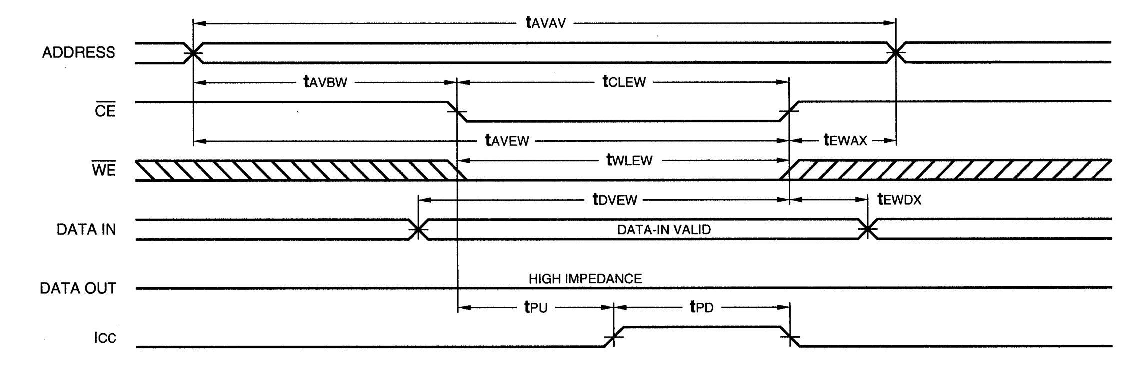
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C108/109–							
		25		20		17		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	20		20		17		15	
t_{CLEW}	Chip Enable Low to End of Write Cycle	15		15		13		12	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	15		15		13		12	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	15		15		13		12	
t_{DVEW}	Data Valid to End of Write Cycle	10		9		8		7	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		7		6		5

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND $\leq V_{OUT} \leq V_{CC}$. The device is disabled, i.e., $\overline{CE}_1 = V_{CC}$, CE_2 = GND.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}_1 \leq V_{IL}$, $CE_2 \geq V_{IH}$, $\overline{WE} \leq V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}_1 \geq V_{IH}$, $CE_2 \leq V_{IL}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}_1 = V_{CC}$, CE_2 = GND. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}_1$ must be $\geq V_{CC} - 0.2$ V or CE_2 must be ≤ 0.2 V. All other inputs must meet $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}_1$, CE_2, and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}_1$ low, CE_2 high).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}_1$ and CE_2 transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}_1$ and CE_2 active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}_1$ and CE_2 going active, the output remains in a high impedance state.

18. If $\overline{CE}_1$ and CE_2 goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Rising edge of CE_2 ($\overline{CE}_1$ active) or the falling edge of $\overline{CE}_1$ (CE_2 active).

b. Falling edge of $\overline{WE}$ ($\overline{CE}_1$, CE_2 active).

c. Transition on any address line ($\overline{CE}_1$, CE_2 active).

d. Transition on any data line ($\overline{CE}_1$, CE_2, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}_1$, CE_2, or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

5

FIGURE 1a.

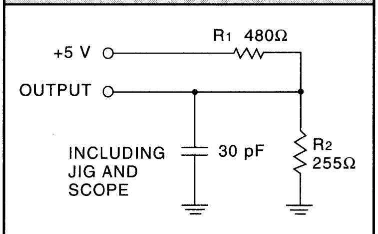


FIGURE 1b.

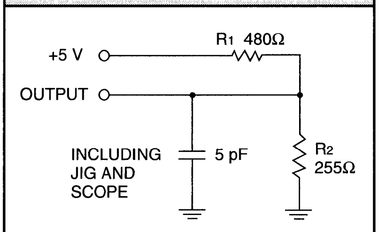
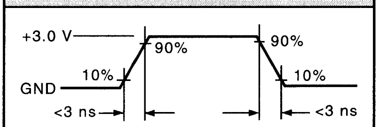
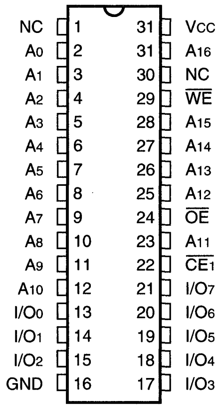


FIGURE 2.

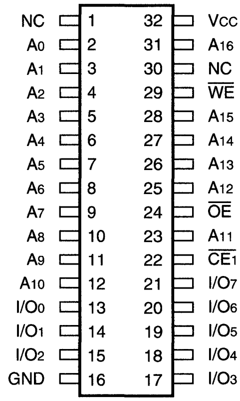


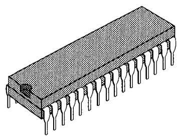
L7C108 ORDERING INFORMATION

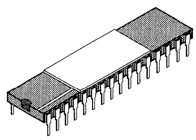
32-pin — 0.4" wide

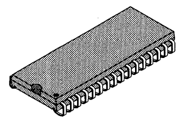


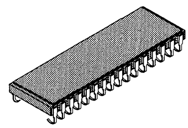
32-pin









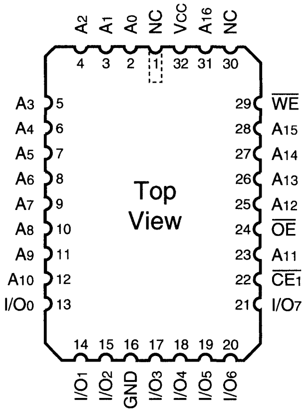


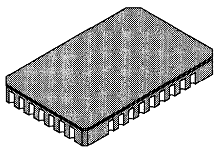
Speed	Plastic DIP (P13)	Sidebraze Hermetic DIP (D12)	Plastic SOJ (0.4" wide) (W6)	Ceramic SOJ (0.440" wide) (Y1)
	0°C to +70°C — Commercial Screening			
25 ns	L7C108PC25*	L7C108DC25*	L7C108WC25*	L7C108YC25*
20 ns	L7C108PC20*	L7C108DC20*	L7C108WC20*	L7C108YC20*
17 ns	L7C108PC17*	L7C108DC17*	L7C108WC17*	L7C108YC17*
15 ns	L7C108PC15*	L7C108DC15*	L7C108WC15*	L7C108YC15*
	–55°C to +125°C — Commercial Screening			
25 ns		L7C108DM25*		L7C108YM25*
20 ns		L7C108DM20*		L7C108YM20*
17 ns		L7C108DM17*		L7C108YM17*
	–55°C to +125°C — MIL-STD-883 Compliant			
25 ns		L7C108DMB25*		L7C108YMB25*
20 ns		L7C108DMB20*		L7C108YMB20*
17 ns		L7C108DMB17*		L7C108YMB17*

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C108DMB17L)**

L7C108 ORDERING INFORMATION

32-pin



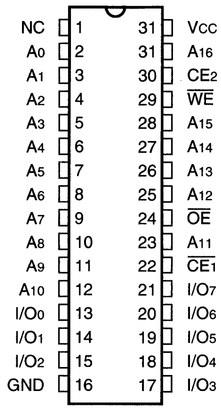


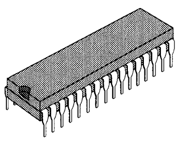
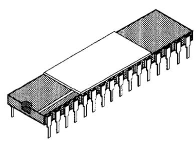
Speed	Ceramic Leadless Chip Carrier (K10)		
	0°C to +70°C — Commercial Screening		
25 ns	L7C108KC25*		
20 ns	L7C108KC20*		
17 ns	L7C108KC17*		
15 ns	L7C108KC15*		
	–55°C to +125°C — Commercial Screening		
25 ns	L7C108KM25*		
20 ns	L7C108KM20*		
17 ns	L7C108KM17*		
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns	L7C108KMB25*		
20 ns	L7C108KMB20*		
17 ns	L7C108KMB17*		

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C108KMB17L)**

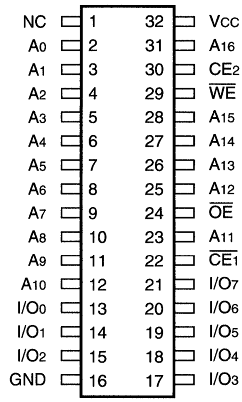
L7C109 ORDERING INFORMATION

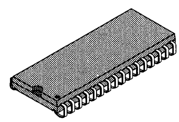
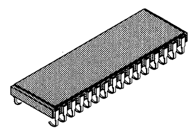
32-pin — 0.4" wide



32-pin



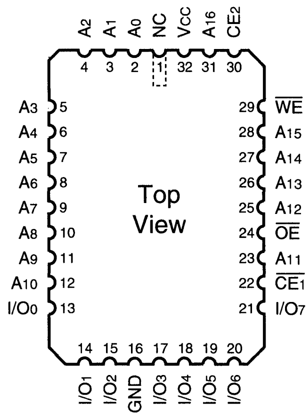



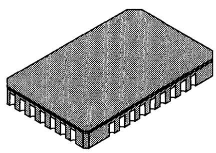
Speed	Plastic DIP (P13)	Sidebraze Hermetic DIP (D12)	Plastic SOJ (0.4" wide) (W6)	Ceramic SOJ (0.440" wide) (Y1)
	0°C to +70°C — Commercial Screening			
25 ns	L7C109PC25*	L7C109DC25*	L7C109WC25*	L7C109YC25*
20 ns	L7C109PC20*	L7C109DC20*	L7C109WC20*	L7C109YC20*
17 ns	L7C109PC17*	L7C109DC17*	L7C109WC17*	L7C109YC17*
15 ns	L7C109PC15*	L7C109DC15*	L7C109WC15*	L7C109YC15*
	–55°C to +125°C — Commercial Screening			
25 ns		L7C109DM25*		L7C109YM25*
20 ns		L7C109DM20*		L7C109YM20*
17 ns		L7C109DM17*		L7C109YM17*
	–55°C to +125°C — MIL-STD-883 Compliant			
25 ns		L7C109DMB25*		L7C109YMB25*
20 ns		L7C109DMB20*		L7C109YMB20*
17 ns		L7C109DMB17*		L7C109YMB17*

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C109DMB17L)**

L7C109 ORDERING INFORMATION

32-pin





Speed	Ceramic Leadless Chip Carrier (K10)		
	0°C to +70°C — Commercial Screening		
25 ns	L7C109KC25*		
20 ns	L7C109KC20*		
17 ns	L7C109KC17*		
15 ns	L7C109KC15*		
	–55°C to +125°C — Commercial Screening		
25 ns	L7C109KM25*		
20 ns	L7C109KM20*		
17 ns	L7C109KM17*		
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns	L7C109KMB25*		
20 ns	L7C109KMB20*		
17 ns	L7C109KMB17*		

*The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C109KMB17L)

5

Special Architecture Static RAMs

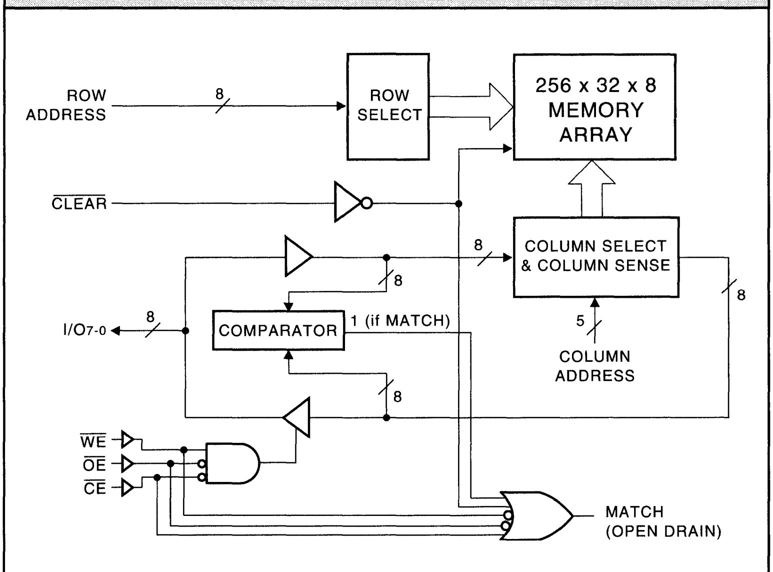
6

L7C174
8K x 8 Cache-Tag Static RAM

FEATURES

- ❑ 8K x 8 CMOS Static RAM with 8-bit Tag Comparison Logic
- ❑ High Speed Address-to-MATCH — 12 ns maximum
- ❑ High Speed Flash Clear
- ❑ High Speed Read Access Time — 12 ns maximum
- ❑ Low Power Operation
  Active: 300 mW typical at 35 ns
  Standby: 500 µW typical
- ❑ Data Retention at 2 V for Battery Backup Operation
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Plug Compatible with IDT7174, IDT71B74, MK48H74
- ❑ Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Plastic SOJ
  - 32-pin Ceramic LCC

L7C174 Block Diagram



DESCRIPTION

The **L7C174** is a high-performance, low power CMOS static RAM optimized for use as the address tag comparator in high speed cache memory systems. One L7C174 can be used to map 8K cache lines into a 1 megabyte address space by comparing 20 address bits organized as 13-line address bits and 7-page address bits.

The storage circuitry is organized as 8192 words by 8 bits per word and includes an 8-bit data comparator with MATCH output. The 8-bit data is input/output on shared I/O pins and comparison is performed between 8-bit incoming data and accessed memory locations. Also provided is a high speed CLEAR control which clears all memory locations to zero when activated. This allows all address tag bits to be cleared when powering on or when flushing the cache.

This device is available in five speed grades with maximum address-to-MATCH times of 12 ns to 35 ns. Operation is from a single +5 V power supply with power consumption only being 300 mW (typical) at 35 ns. Dissipation drops to 500 µW (typical) when the memory is deselected (Enable is high).

The L7C174 consumes only 30 µW (typical) at 3 V allowing effective battery backup operation. For minimal power consumption, data may be retained in inactive storage with a supply voltage as low as 2 V.

The L7C174 provides fully asynchronous (unclocked) operation with matching access and cycle times. An active low Chip Enable and Output Enable along with a three state I/O bus simplify the connection of several chips for increased storage capacity. Wide tag addresses are easily accommodated by paralleling devices and Wire-ORing the MATCH outputs. A low on the MATCH output indicates a data mismatch.

Memory locations are specified on address pins A0 through A12 with functions defined in the Truth Table.

During CLEAR, the state of the I/O pins remain completely defined by the WE, CE, and OE control inputs. Data In has the same polarity as Data Out.

Latchup and static discharge protection are provided on-chip. The L7C174 can withstand an injection current of up to 200 mA on any pin without damage.

Truth Table

$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{CLEAR}$	MATCH	I/O	FUNCTION
X	X	X	L	H	—	Reset all bits to low
X	H	X	H	H	High-Z	Deselect chip
H	L	H	H	L	D_{IN}	No MATCH
H	L	H	H	H	D_{IN}	MATCH
H	L	L	H	H	D_{OUT}	Read
L	L	X	H	H	D_{IN}	Write

X = Don't Care; L = V_{IL}; H = V_{IH}

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
Active Operation, Military	–55°C to +125°C	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
Data Retention, Commercial	0°C to +70°C	$2.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
Data Retention, Military	–55°C to +125°C	$2.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C174			
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage (Note 11)	V_{CC} = 4.5 V, I_{OH} = –4.0 mA (all except MATCH pin)	2.4			V
V_{OL}	Output Low Voltage (Note 11)	I_{OL} = 8.0 mA (all except MATCH pin)			0.4	V
		I_{OL} = 18.0 mA (MATCH pin)			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	–10		+10	μA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}, $\overline{OE}$ = V_{CC} (except MATCH pin)	–10		+10	μA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		100	500	μA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		10	200	μA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

			L7C174-					
Symbol	Parameter	Test Condition	35	25	20	15	12	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	90	115	140	165	195	mA

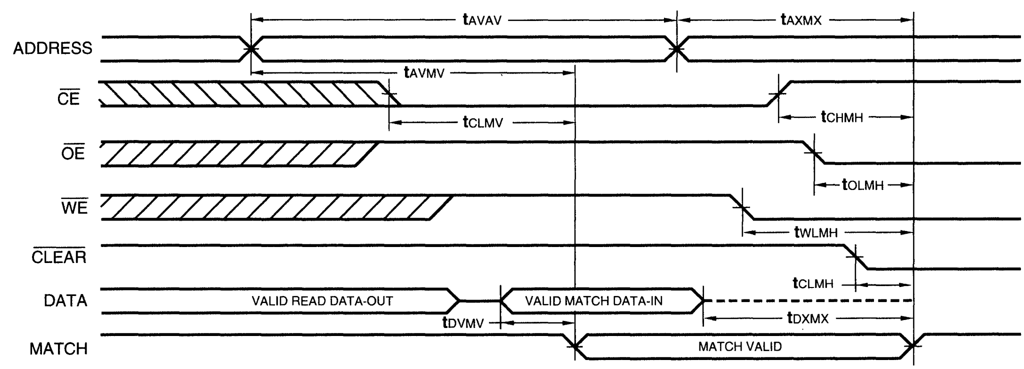
SWITCHING CHARACTERISTICS *Over Operating Range*

MATCH AND $\overline{\text{CLEAR}}$ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

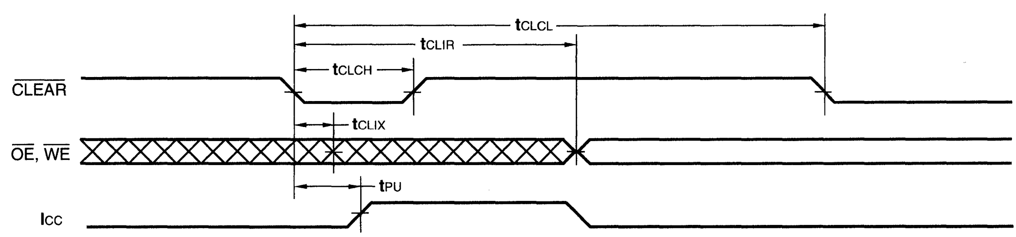
		L7C174–									
		35		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	MATCH Cycle Time	35		25		20		15		12	
t_{AVMV}	Address Valid to MATCH Valid		30		22		20		15		12
t_{AXMX}	Address Change to MATCH Change	3		3		3		3		3	
t_{CLMV}	Chip Enable Low to MATCH Valid		20		15		10		10		8
t_{CHMH}	Chip Enable High to MATCH High	3		3		3		3		3	
t_{OLMH}	Output Enable Low to MATCH High	3		3		3		3		3	
t_{WLMH}	Write Enable Low to MATCH High	3		3		3		3		3	
t_{CLMH}	$\overline{\text{CLEAR}}$ Low to MATCH High	0	25	0	20	0	15	0	12	0	10
t_{DVMV}	Data Valid to MATCH Valid		20		15		15		13		10
t_{DXMX}	Data Change to MATCH Change	0		0		0		0		0	
t_{CLCL}	$\overline{\text{CLEAR}}$ Cycle Time	65		55		45		35		30	
t_{CLCH}	$\overline{\text{CLEAR}}$ Pulse Width	20		15		15		12		12	
t_{CLIX}	$\overline{\text{CLEAR}}$ Low to Inputs Don't Care	0		0		0		0		0	
t_{CLIR}	$\overline{\text{CLEAR}}$ Low to Inputs Recognized		70		60		50		50		45

6

MATCH CYCLE *Note 19*



$\overline{\text{CLEAR}}$ CYCLE *Note 25*

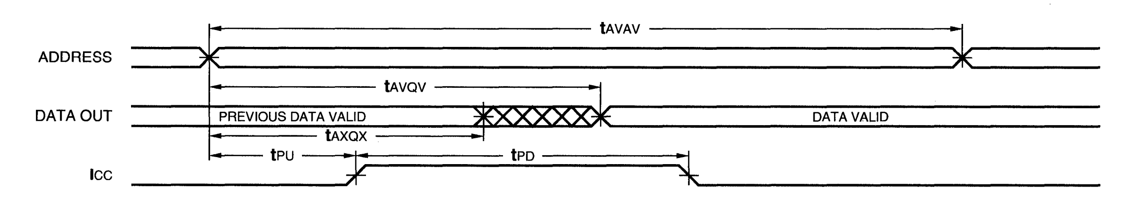


SWITCHING CHARACTERISTICS *Over Operating Range*

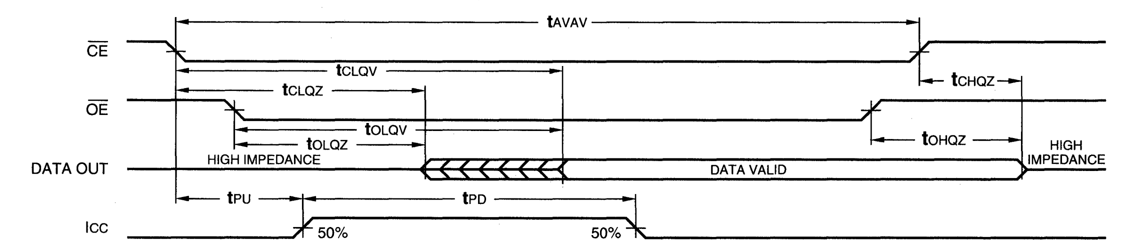
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C174–									
		35		25		20		15		12	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{AVAV}	Read Cycle Time	35		25		20		15		12	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		35		25		20		15		12
t_{AXQX}	Address Change to Output Change	3		3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		15		12		10		8		8
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		15		10		8		8		5
t_{OLQV}	Output Enable Low to Output Valid		15		12		10		8		6
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		12		10		8		5		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		35		25		20		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0		0	

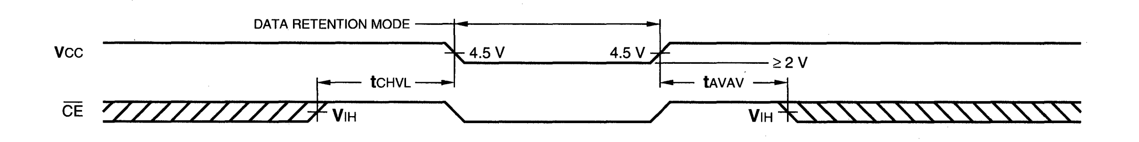
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}$/$\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

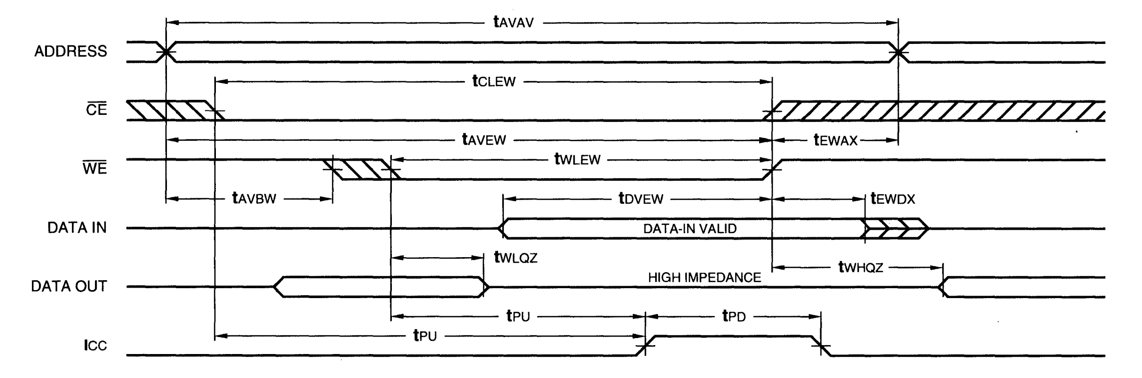


SWITCHING CHARACTERISTICS *Over Operating Range*

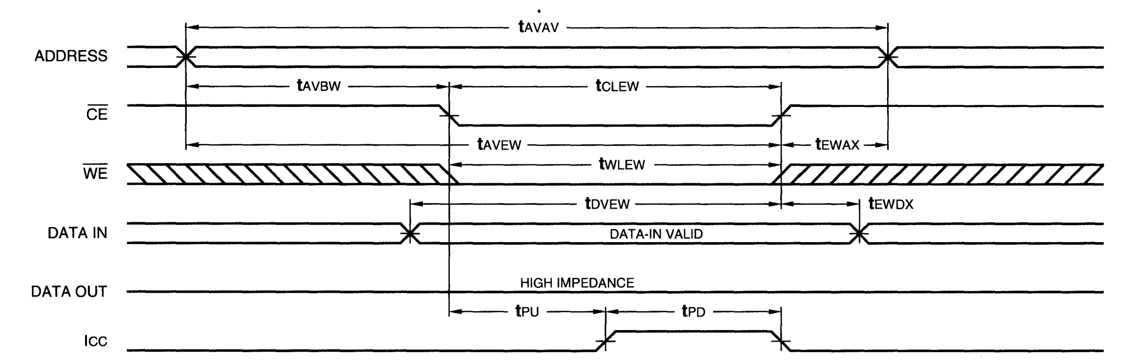
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C174–									
		35		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	25		20		20		15		12	
t_{CLEW}	Chip Enable Low to End of Write Cycle	25		15		15		12		10	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	25		15		15		12		10	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	20		15		15		12		10	
t_{DVEW}	Data Valid to End of Write Cycle	15		10		10		7		6	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		10		7		7		5		4

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.2$ V. All other inputs must meet $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

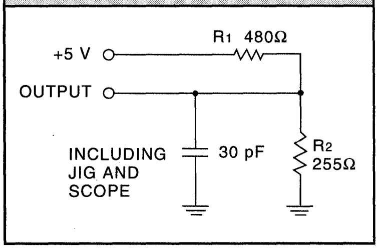


FIGURE 1b.

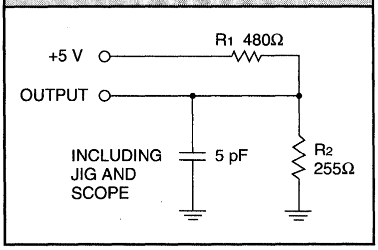
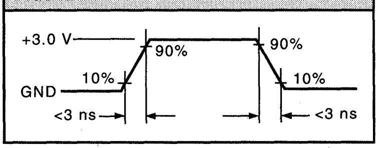
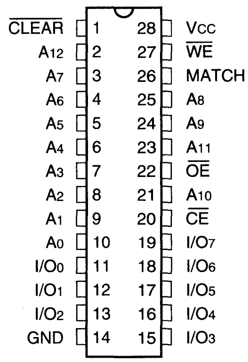


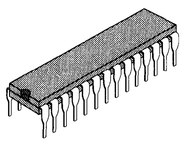
FIGURE 2.

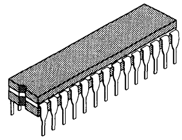


ORDERING INFORMATION

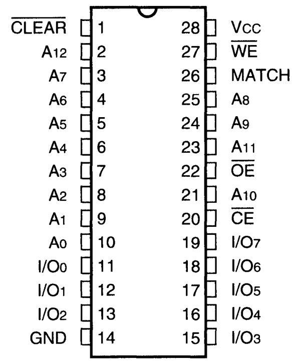
28-pin — 0.3" wide

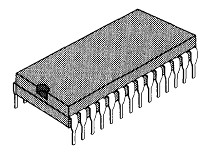


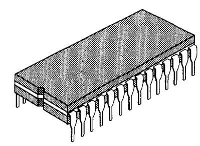




28-pin — 0.6" wide



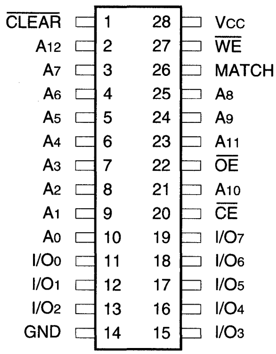


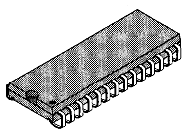


Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic DIP (P9)	Ceramic DIP (C6)
	0°C to +70°C — Commercial Screening			
25 ns	L7C174PC25	—	L7C174NC25	—
20 ns	L7C174PC20	L7C174CC20	L7C174NC20	L7C174IC20
15 ns	L7C174PC15	L7C174CC15	L7C174NC15	L7C174IC15
12 ns	L7C174PC12	L7C174CC12	L7C174NC12	L7C174IC12
	–55°C to +125°C — Commercial Screening			
25 ns		L7C174CM25		L7C174IM25
20 ns		L7C174CM20		L7C174IM20
15 ns		L7C174CM15		L7C174IM15
	–55°C to +125°C — MIL-STD-883 Compliant			
25 ns		L7C174CMB25		L7C174IMB25
20 ns		L7C174CMB20		L7C174IMB20
15 ns		L7C174CMB15		L7C174IMB15

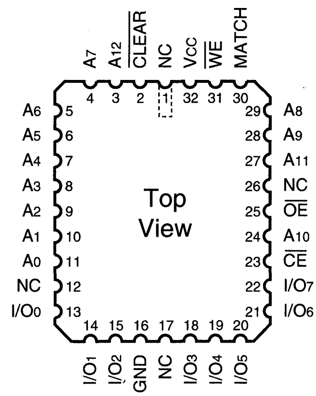
ORDERING INFORMATION

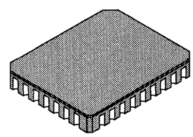
28-pin — 0.3" wide





32-pin





Speed	Plastic SOJ (W2)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening	
35 ns	L7C174WC35	—
25 ns	L7C174WC25	—
20 ns	L7C174WC20	L7C174KC20
15 ns	L7C174WC15	L7C174KC15
12 ns	L7C174WC12	L7C174KC12
	–55°C to +125°C — Commercial Screening	
25 ns		L7C174KM25
20 ns		L7C174KM20
15 ns		L7C174KM15
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns		L7C174KMB25
20 ns		L7C174KMB20
15 ns		L7C174KMB15

Quality and Reliability

7

Copies of the LOGIC Devices **"Quality Assurance Program Manual"** and **"Reliability Manual"** may be obtained from LOGIC Devices by contacting our applications group at (408) 737-3346 between 8:00 AM and 6:00 PM Pacific time, Monday through Friday.

Technology and Design Features

8

Latchup and ESD Protection

Latchup is a destructive phenomenon which was once common in CMOS circuits but has now been largely eliminated by improved circuit design techniques. Latchup takes place because of the existence in CMOS of an inherent PNPN or NPNP structure between VCC and ground. Either of these two can form a pair of transistors connected so as to form a positive feedback loop, with the collector of one transistor driving the base of the other. The result is a low-impedance path from VCC to ground, which cannot be interrupted except by the removal of power. This condition can be destructive if the area involved is sufficiently large to dissipate excessive power. One example of the formation of such a structure is shown in Figure 1. The equivalent circuit is shown in Figure 2.

As shown in Figure 1, the N+ regions which form the source and drain of an N-channel MOS transistor also act as the emitters of a parasitic NPN transistor. The P-well forms the base region and the N-substrate is the collector. The current gain of this transistor is relatively high because it is formed vertically and therefore the base width is quite small. This is especially true of fine-geometry CMOS processes which tend to have very shallow wells to reduce sidewall capacitance. The P+ region in the well is called a "well tap" and is present to form a low-resistance connection between the well and ground. The source region cannot serve this function because it forms a diode between the N+ source and the P-well.

Also shown in Figure 1 is an additional parasitic PNP transistor. The source and drain regions of the P-channel MOS device form the emitters, the N-substrate is the base, and the P-well is the collector. This transistor is a PNP, and generally has a beta (β) much less than 1 since it is formed laterally and the gate region is relatively large. Like the vertical NPN, it can have multiple emitters. The N+ region tied to VCC in the substrate functions similarly to the well tap discussed above.

Note that the base of the NPN and the collector of the PNP are a common region (the P-well), and similarly the base of the PNP and the collector of the NPN are common (the N-substrate). Thus, the PNPN structure necessary for latchup is formed. Also, due to the the physical distance between the well and substrate taps and the base regions which they attempt to contact, a small resistance exists between the base regions and their respective well taps, denoted RS (substrate) and RW (well).

Latchup begins when a perturbation causes one of the bipolar transistors to turn on. An example would be excursion of the output pad below ground or above VCC due to transmission-line ringing. If the pad goes more than 0.7 V below ground, the NPN will turn on since its base is at approximately ground potential. The NPN's collector current will cause a voltage drop across RS, the bulk substrate resistance. This voltage drop turns on the PNP.

The PNP transistor's collector current forces a similar voltage drop across RW, the well resistance. This raises the base voltage of the NPN above ground and can cause the NPN to continue to conduct even after the output pad returns to a normal voltage range. In this case, the current path shifts to the grounded emitter.

Note that any effect which can cause a transient turn-on of either transistor can cause the latchup process. Common causes include:

1. Ringing of unprotected I/O pins outside the ground to VCC region.
2. Radiation-induced carriers generated in the base of the bipolar transistors.
3. Hot-powerup of the device, with inputs driven HIGH before VCC is applied.
4. Electrostatic discharge.

PROTECTING AGAINST LATCHUP

Latchup, while once a severe problem for CMOS, is now a relatively well-understood phenomenon. In order for latchup to occur, the product of the current gains of the two parasitic transistors must exceed 1. Thus, the primary means for avoiding latchup is the insertion of structures known as "guard rings" around all MOS transistors (and other structures) likely to be subjected to latchup-causing transients. This includes output buffer transistors and any devices which form a part of the ESD protection network. These guard rings absorb current which would otherwise drive the base of the lateral device, and thus dramatically reduce its gain.

Since external electrical perturbations are the dominant cause of latchup in non-radiation environments, protecting the "periphery" of the chip is most important. Therefore, since guard rings require a lot of area, they are generally used only in critical areas such as those mentioned above.

As an additional protective measure, strict rules are enforced in the layout regarding the positioning of the substrate and well taps. They are spaced closely together throughout

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FIGURE 1. PARASITIC TRANSISTOR STRUCTURES IN PARALLEL CMOS

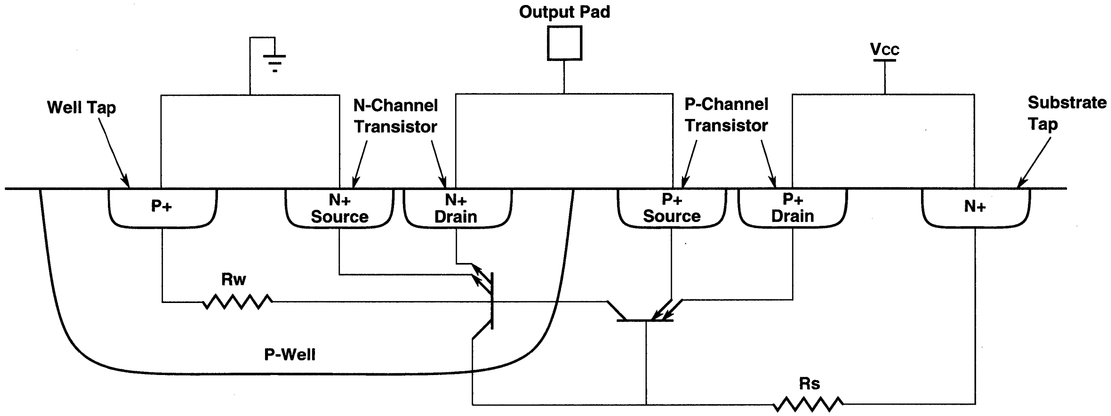
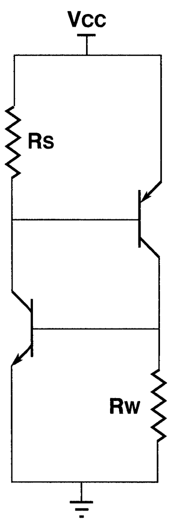


FIGURE 2. EQUIVALENT CIRCUIT FOR LATCHUP PATH



the die, reducing the values of RS and RW. This makes it more difficult to develop the base drive necessary to regenerate the latchup condition.

Measurement of susceptibility to latchup is done by connecting a current source to an input or output of the device under test. By increasing the current forced to flow into the pin and noting the point at which latchup occurs, a measure of the device's ability to resist latchup-inducing carrier injection is obtained. Note that depending on the device, the current source may require a rather large voltage compliance in order to provide an adequate test.

While early CMOS devices had a latchup trigger current of a few tens of milliamps, most current LOGIC Devices products typically can withstand more than 1 amp without latching. As a result, latchup is no longer a practical concern, except for extreme conditions such as driving multiple inputs HIGH with a low-impedance source during powerup of the device.

ELECTROSTATIC DISCHARGE

Input protection structures on CMOS devices are used to protect against damage to the gate oxides of input transistors when accumulated static charge is discharged through a device. This charge can often reach potentials of several thousand volts. The input protection network is designed to shunt this charge safely to ground or VCC, bypassing the delicate MOS transistors.

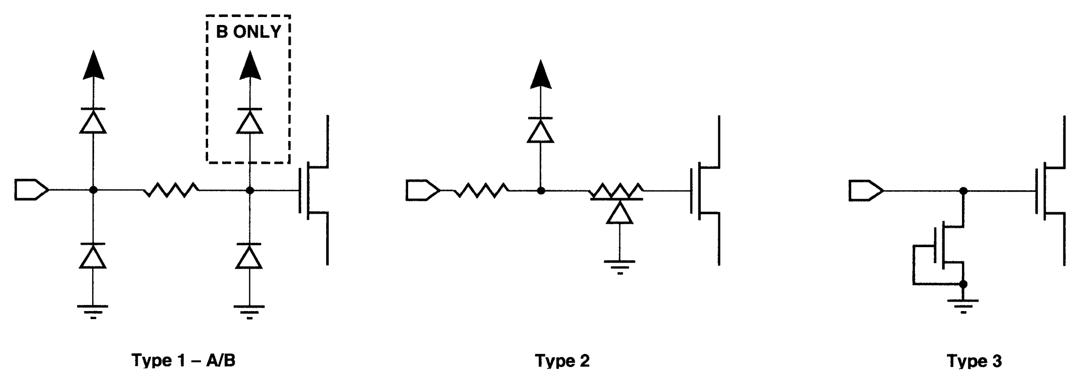
Several features are required of a good input protection network. Since static discharge pulses exhibit very fast rise-times, it must have a very fast turn-on time. It must be capable of carrying large instantaneous currents without damage. It must prevent the voltage at the circuit input from rising above approximately 10 V during the time when the several-thousand-volt discharge is shunted to ground. It must not create appreciable delay for fast edges which are within the 0–5 V input range. And finally, it must be well protected against latchup caused by inputs which are driven beyond the supply rails, injecting current into the substrate. Much research and experimentation has been devoted to optimizing the tradeoffs between these conflicting goals.

All LOGIC Devices products employ one of the three input protection structures shown in Figure 3. Most devices currently use the Type 1 input protection. This structure is designed to absorb very high static discharge energies and will draw substantial current from the input pin if driven beyond either supply rail. Hence, it provides a "hard" clamp. Besides its advantages for static protection, this clamp can effectively reduce undershoot energy, preventing oscillation of an unterminated input back above the 0.8 V V_{IL} MAX level. This makes the circuit ideal for noisy environments and ill-behaved signals. This input structure may not be driven to a high level without power applied to the device, however. To do so would result in current flowing through the diode connected to the device's V_{CC} rail, and supplying power to the entire board or system backward through the device V_{CC} pin. This may overstress the bond wire or device metallization, resulting in failure.

The Type 2 structure employs a series resistor prior to the two clamp diodes. This results in a "soft" clamping effect. This structure will withstand the transient application of voltages outside the supply rails for brief periods without drawing excessive current. In contrast to the Type 1 structure, this circuit will provide only a modest reduction of the energy in an undershoot pulse. However, it is somewhat more tolerant of power-up sequences which cause the inputs to be driven before V_{CC} is applied. In the course of routine product upgrades, devices employing this structure are being redesigned to use a Type 1 input protection.

The Type 3 structure uses a large area N-channel transistor (part of an open-drain output buffer) to protect the input. The drain-well junction of this device serves the function of a diode connected between the input and ground, protecting against negative excursions of the input. The avalanche breakdown of the output device serves to protect against positive pulses, giving the effect of a zener diode between the input and ground. This circuit is used only for inputs which are designed to have their inputs driven without power applied. The lack of a diode to V_{CC} prevents sourcing of power from the inputs to the V_{CC} supply.

Figure 3. Input Protection Devices



Power Dissipation in LOGIC Devices Products

In calculating the power dissipation of LOGIC Devices products, attention must be given to a number of formerly second-order effects which were generally ignored when dealing with bipolar and NMOS technologies. By far the dominant contributor to power dissipation in most CMOS devices is the effective current path from the supply to ground, created by the repetitive charging and discharging of the load capacitance. This is distinct from DC loading effects, which may also consume power. The power dissipated in the load capacitance is proportional to CV^2F, where C is the load capacitance, V is the voltage swing, and F is the switching frequency. This mechanism can frequently contribute 80% or more of the total device dissipation of a truly complementary device operating at a high clock rate.

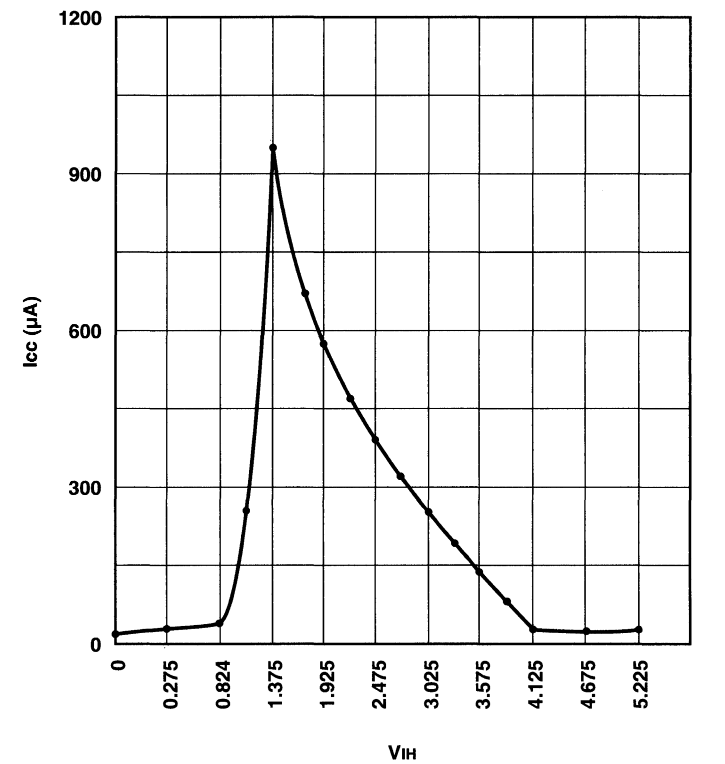
The second contributor to the power dissipation of a CMOS device is the DC current path between V_{CC} and ground present in the input level translators. These circuits are voltage amplifiers which are designed to convert worst case 0.8–2.0 V TTL-compatible input levels to 0 and 5 V internal levels. With 2.0 V applied to the input of most level translator circuits, about 1 mA will flow from the power supply to ground. A floating input will at best have similar results, and may result in oscillations which can dissipate orders of magnitude more power and cause malfunctioning of the device.

The power dissipation of input level translators exhibits a strong peak at about 1.4 V but is reduced substantially when the input voltage exceeds 3.0 V (see Figure 1). Fortunately, this voltage is easy to achieve in practice, even for bipolar devices with TTL I/O structures. These generally will produce a V_{OH} of at least 3.5 V if not fully loaded. As a result, dissipation in the input structures is usually negligible compared to other sources.

Two further sources of power dissipation in CMOS come from the core logic. The sources of internal power dissipation are the same as those discussed for external nodes, namely repetitive charging of the parasitic load capacitances on each gate output, and the power drawn due to a direct current path to ground when gate input voltage levels transition through the linear region. In practice, the internal voltage waveforms are characterized by high edge rates and rail-to-rail swings. For this reason, the latter source of dissipation is usually negligible, unless NMOS or other non-complementary logic design techniques have been used.

The capacitance of typical internal nodes in CMOS logic circuits are a few femtofarads. However, there can be thousands, or tens of thousands of such nodes. As a result, the core

FIGURE 1.



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power dissipation is strongly dependent on the average rate at which these nodes switch (the "F" in CV^2F). Fortunately, for most complex logic circuits, with non-pathological external stimulus only a small fraction of the logic nodes switch on any given cycle. For this reason, internal power is generally quite small for these device types. Exceptions include devices containing long shift registers or other structures which can exhibit high duty cycles on most internal nodes. These devices can dissipate significant power in the core logic if stimulated with alternating data patterns and clocked at a high rate.

To summarize, of the several contributors to power dissipation, the CV^2F power of the outputs is usually dominant. Because output loading is system-dependent, it is not possible for the manufacturer to accurately predict total power dissipation in actual use. As a result, LOGIC Devices extrapolates measured power dissipation values to a zero-load environment and publishes the resulting value. This value includes the effects of worst-case input and power-supply voltages, temperature, and stimulus pattern, but not CV^2F. This value is weakly frequency dependent, and the frequency at which it is measured is published in the device data sheet. The maximum value is for worst-case pattern, and the typical is for a more random pattern and is therefore more representative of what would be experienced in actual practice.

A good estimate of total power dissipation in a particular system under worst-case conditions can be obtained by adding the calculated output power to the *typical* published figure. The output power is given by:

$$\frac{NCV^2F}{4}$$

where:

N = the number of device outputs (divided by 2 to account for the assumption that on average, half of the outputs switch on any given cycle)

C = the output load capacitance, per pin, given in Farads

V = the power supply voltage

F = the clock frequency (divided by 2 to account for the fact that a registered output can at most switch at only half the clock rate).

A less pessimistic estimate, appropriate for complex devices when reasonable input voltage levels and non-pathological patterns can be expected, would neglect the published value and use only the calculated value as given above.

Package Information

LOGIC Devices/MIL-STD-1835 Package Code Cross-Reference

LOGIC DEVICES PACKAGE CODE	DESCRIPTION	MIL-STD-1835 PACKAGE DESIGNATOR	MIL-STD-1835 DIMENSION REFERENCE
CERAMIC DIP			
C1	24-pin, 0.3" wide	GDIP3-T24	D-9
C2	20-pin, 0.3" wide	GDIP1-T20	D-8
C3	22-pin, 0.3" wide	N/A	N/A
C4	24-pin, 0.6" wide	GDIP1-T24	D-3
C5	28-pin, 0.3" wide	GDIP4-T28	D-15
C6	28-pin, 0.6" wide	GDIP1-T28	D-10
C7	16-pin, 0.3" wide	GDIP1-T16	D-2
C8	18-pin, 0.3" wide	GDIP1-T18	D-6
C9	32-pin, 0.6" wide	GDIP1-T32	D-16
C10	28-pin, 0.4" wide	N/A	N/A
C11	40-pin, 0.6" wide	GDIP1-T40	D-5
SIDEBRAZE, HERMETIC DIP			
D1	24-pin, 0.6" wide	CDIP2-T24	D-3
D2	24-pin, 0.3" wide	CDIP4-T24	D-9
D3	40-pin, 0.6" wide	CDIP2-T40	D-5
D4	64-pin, 0.9" wide, cavity up	CDIP1-T64	D-13
D5	48-pin, 0.6" wide	CDIP2-T48	D-14
D6	64-pin, 0.9" wide, cavity down	CDIP1-T64	D-13
D7	20-pin, 0.3" wide	CDIP2-T20	D-8
D8	22-pin, 0.3" wide	N/A	N/A
D9	28-pin, 0.6" wide	CDIP2-T28	D-10
D10	28-pin, 0.3" wide	CDIP3-T28	D-15
D11	28-pin, 0.4" wide	N/A	N/A
D12	32-pin, 0.4" wide	N/A	N/A
CERAMIC PGA			
G1	68-pin, cavity up	CMGA3-P68	P-AC
G2	68-pin, cavity down	CMGA3-P68	P-AC
G3	84-pin	CMGA15-P84	P-BC
G4	120-pin	CMGA3-P121	P-AC
CERAMIC LEADLESS CHIP CARRIER			
K1	28-pin, 0.450" x 0.450"	CQCC1-N28	C-4
K2	44-pin, 0.650" x 0.650"	CQCC1-N44	C-5
K3	68-pin, 0.950" x 0.950"	CQCC1-N68	C-7
K4	22-pin, 0.290" x 0.490"	N/A	N/A
K5	28-pin, 0.350" x 0.550"	CQCC4-N28	C-11A
K6	20-pin, 0.290" x 0.425"	CQCC3-N20	C-13
K7	32-pin, 0.450" x 0.550"	CQCC1-N32	C-12
K8	20-pin, 0.350" x 0.350"	CQCC1-N20	C-2
K9	48-pin, 0.550" x 0.550"	N/A	N/A
K10	32-pin, 0.450" x 0.700"	N/A	N/A
CERAMIC FLATPACK			
M1	24-pin	GDFP2-F24	F-6
M2	28-pin	GDFP2-F28	F-11
CERAMIC SOJ			
Y1	32-pin, 0.440" wide	N/A	N/A

Thermal Considerations

The temperature at which a semiconductor device operates is one of the primary determinants of its reliability. This temperature is often referred to as the "junction temperature", although this term is more appropriate for bipolar than MOS technologies. Heat dissipated in the device during operation escapes through a path consisting of one or more series thermal impedances terminating in the surrounding air (see Figure. 1).

The presence of this nonzero thermal impedance causes the temperature of the device to rise above that of the air. Each of the components of the overall thermal impedance causes a rise in temperature which is linearly dependent on the power dissipated in the device. The coefficient is called θ, and has the units °C/W. The θ value for each thermal impedance represents the amount of temperature rise across the impedance as a function of the power dissipation. Usually, θ is given a subscript indicating the two points between which the impedance is measured. Thus the junction temperature of an operating device is given by:

$$T_j = T_{AMB} + (Pd \bullet \theta_{JA})$$

where:

T_j = junction temperature of the device, °C,

T_{AMB} = ambient air temperature, in°C

Pd = power dissipation of the device, in W,

θ_{JA} = sum of all thermal impedances between the die and the ambient air, in °C/W.

The thermal impedance of a given device is dependent on several factors. The package type is the predominant effect; ceramic packages have much lower thermal impedances than plastic, and packages with large surface areas tend to dissipate heat faster. Another factor which is beyond the control of the device manufacturer but which is nonetheless important is the temperature and flow rate of the cooling air. Secondary effects include the size of the die, the method of attaching the die to the package, and the organization of high power dissipation elements on the die.

Because all LOGIC Devices products are built with low-power CMOS technology, thermal impedance is less of a concern than it would be for higher power technologies. As an example, consider a typical NMOS multiplier similar to the LMU16, packaged in a 64-pin plastic DIP. Assuming 1 W power dissipation and θ_{JA} of 50°C/W, the actual die temperature would be 50°C above the surrounding air. By contrast, the LOGIC Devices LMU16 has a typical power dissipation of only 60 mW. This device in the same package would operate at only 3° above the ambient air temperature. Since operating temperature has an exponential relationship to device failure rate (see Quality and Reliability Manuals), the reduction of die temperature available with LOGIC Devices low-power CMOS translates to a marked increase in expected reliability.

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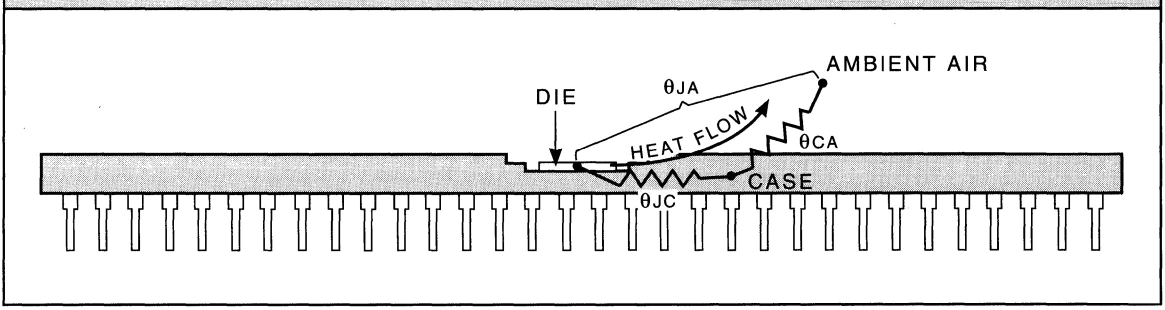
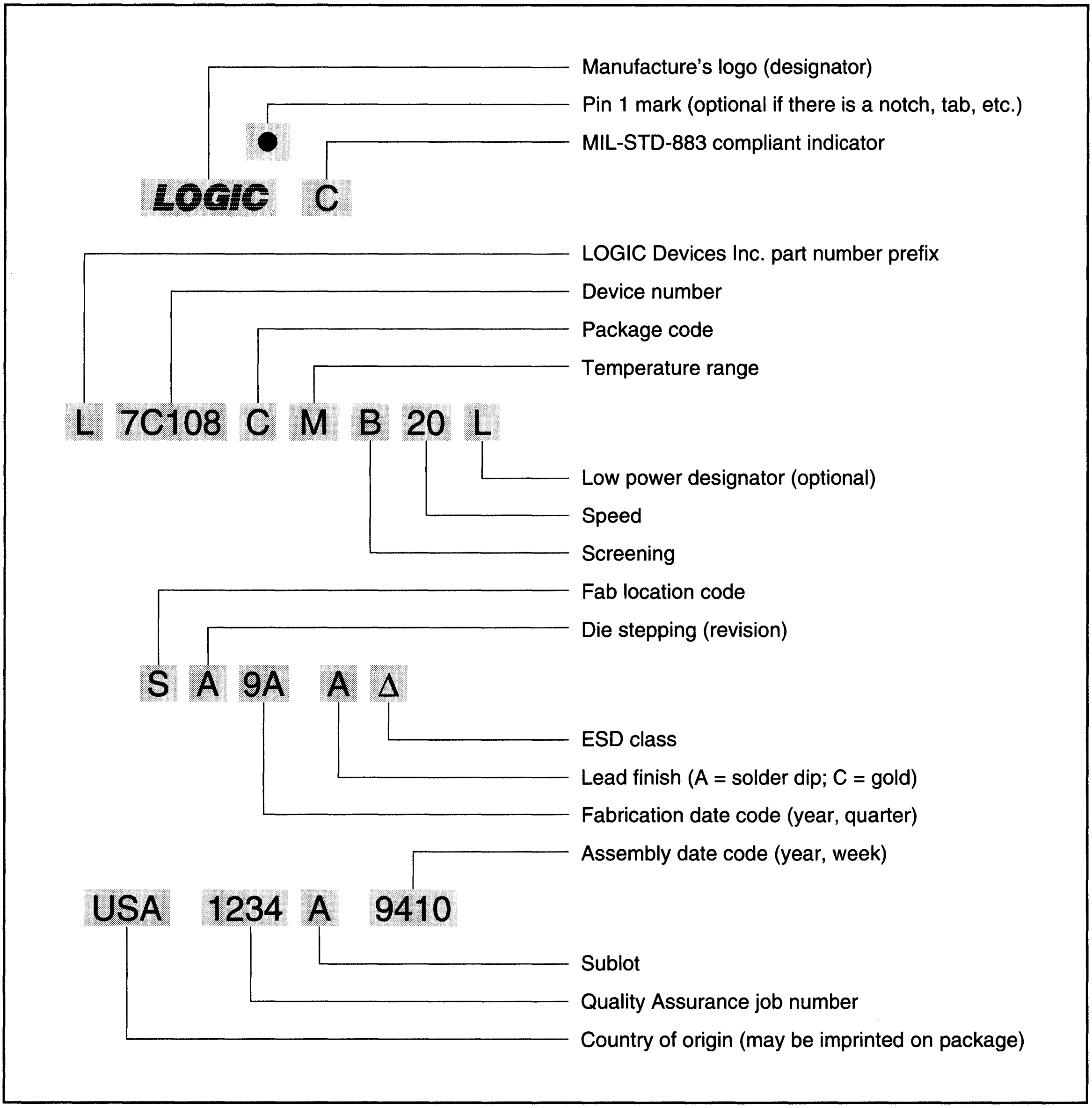
FIGURE 1.



Package Marking Guide



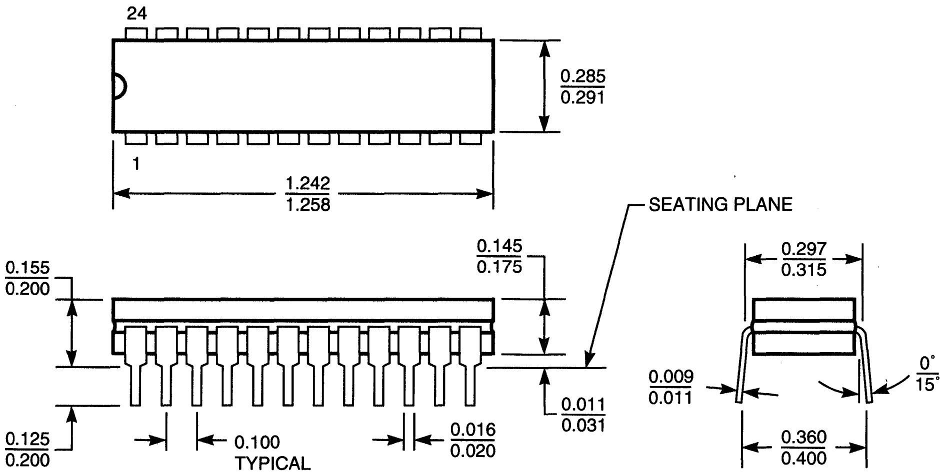
NOTE: Package marking may occur on top and bottom of package due to space limitations

Mechanical Drawings

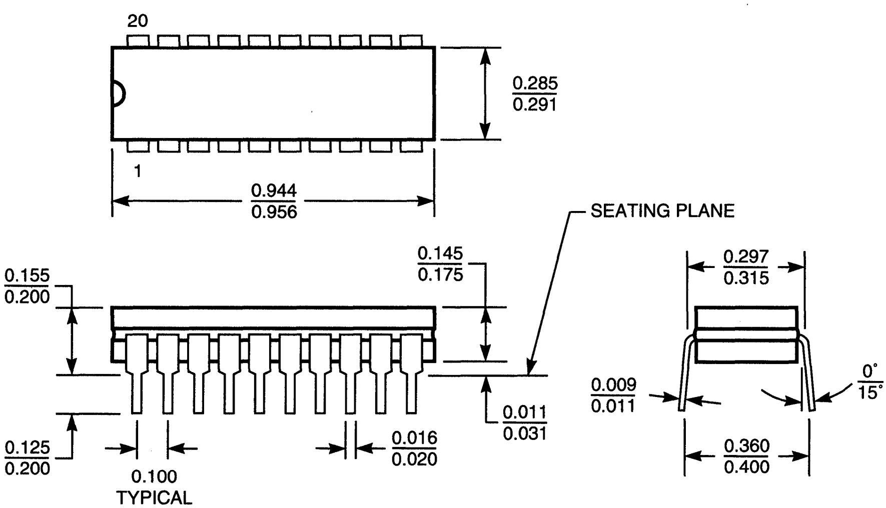
- ❑ Ceramic Dual In-line Package
- ❑ Sidebraze, Hermetic Dual In-line Package
- ❑ Commercial Pin Grid Array
- ❑ Ceramic Pin Grid Array
- ❑ Plastic J-Lead Chip Carrier
- ❑ Ceramic Leadless Chip Carrier
- ❑ Ceramic Flatpack
- ❑ Plastic Dual In-line Package
- ❑ Plastic Quad Flatpack
- ❑ Plastic Small Outline J-Lead
- ❑ Ceramic Small Outline J-Lead

Ceramic DIP (Ordering Code: C, I)

C1 — 24-pin, 0.3" wide

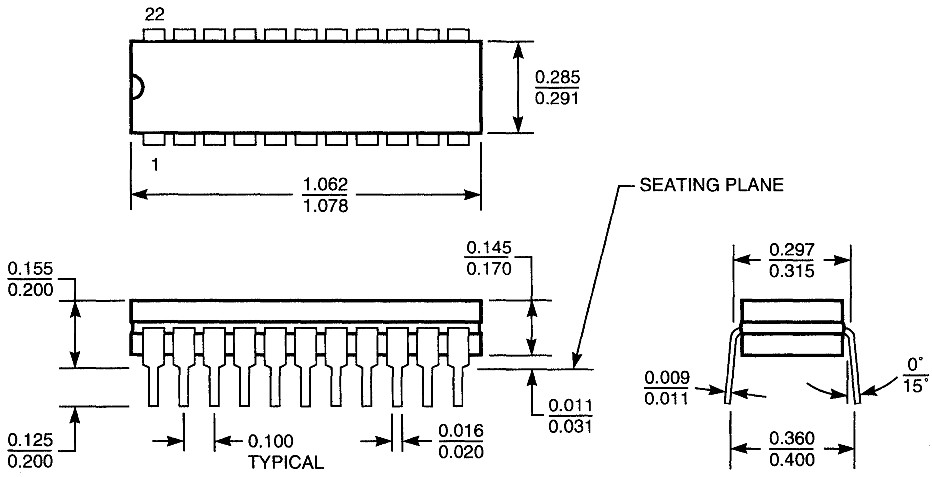


C2 — 20-pin, 0.3" wide

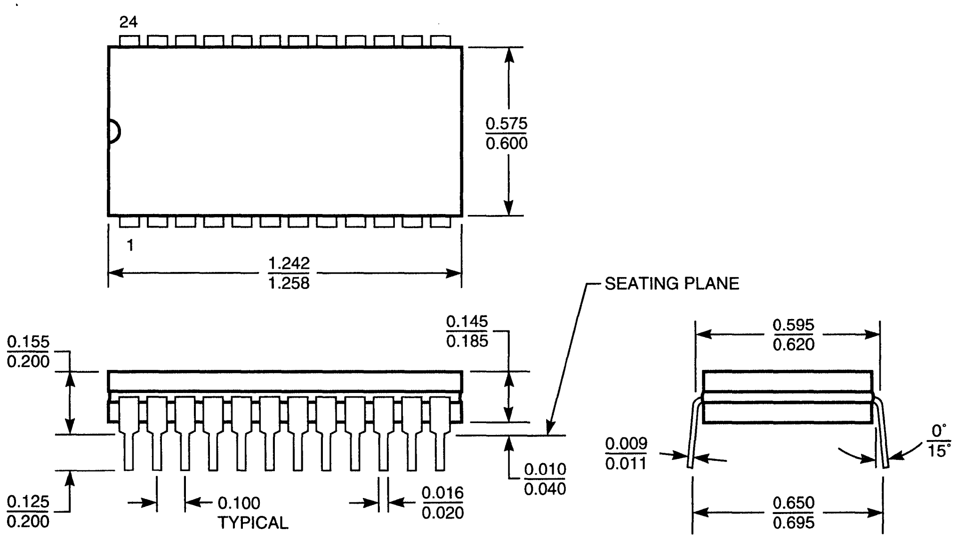


CERAMIC DIP (ORDERING CODE: C, I)

C3 — 22-pin, 0.3" wide

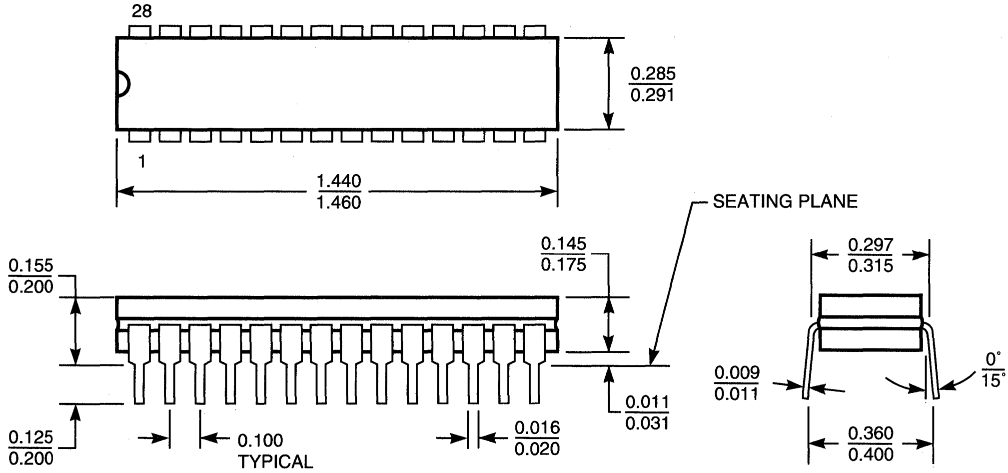


C4 — 24-pin, 0.6" wide

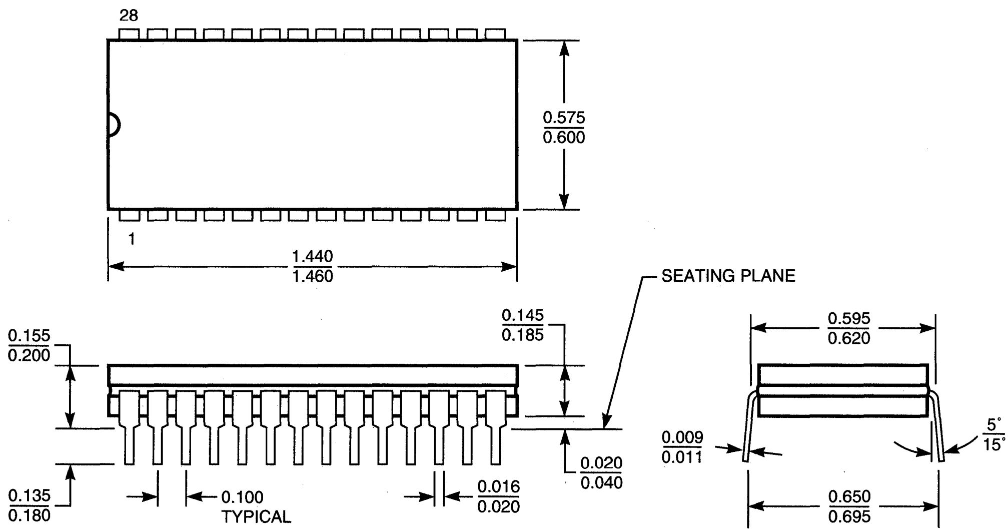


Ceramic DIP (Ordering Code: C, I)

C5 — 28-pin, 0.3" wide

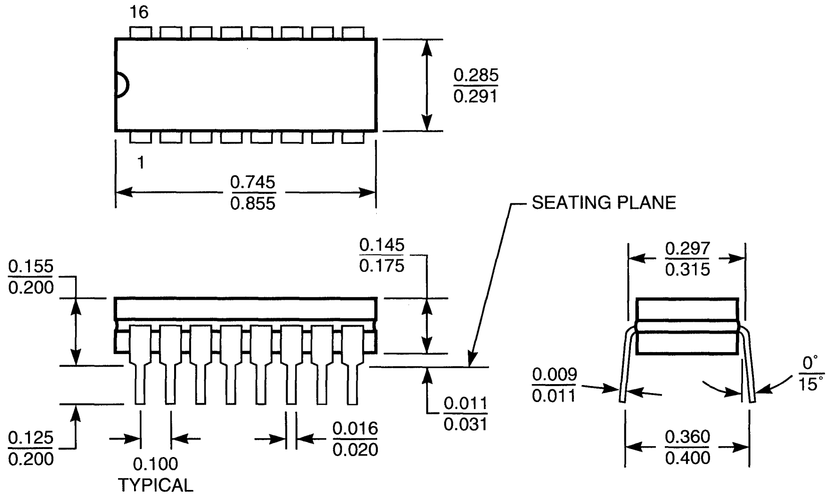


C6 — 28-pin, 0.6" wide

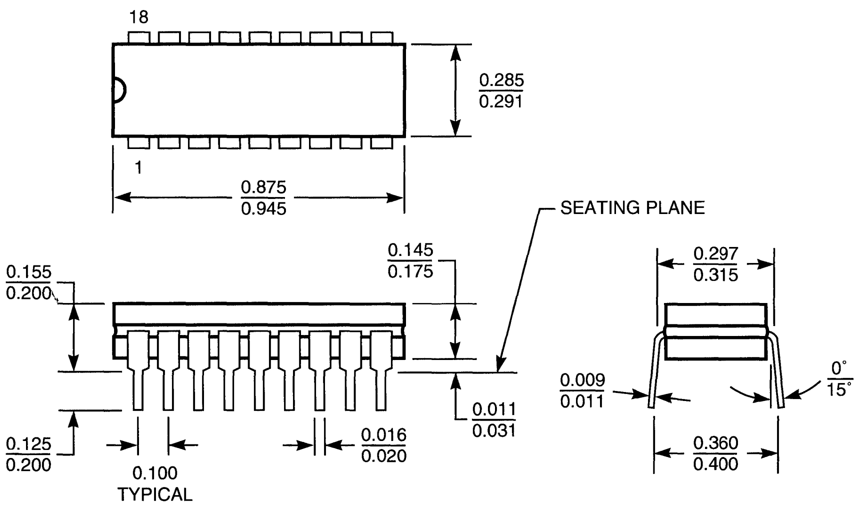


Ceramic DIP (Ordering Code: C, I)

C7 — 16-pin, 0.3" wide

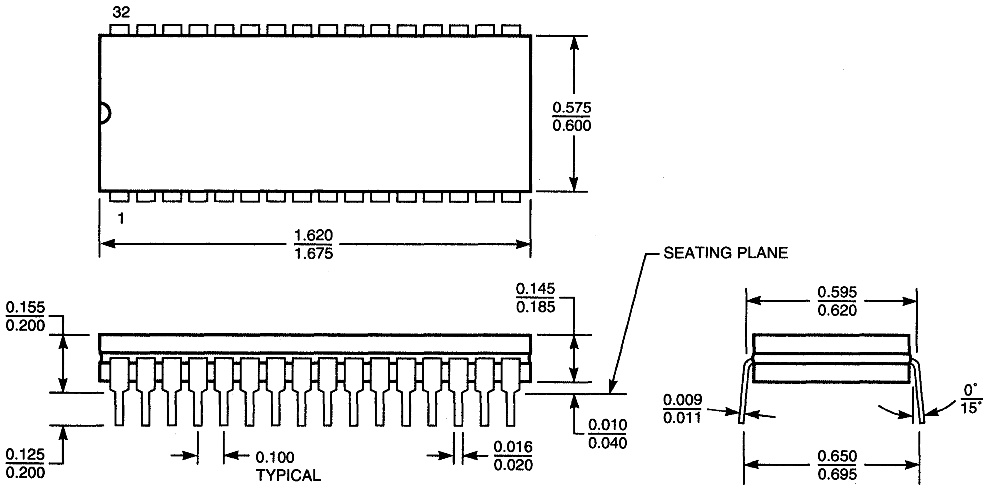


C8 — 18-pin, 0.3" wide

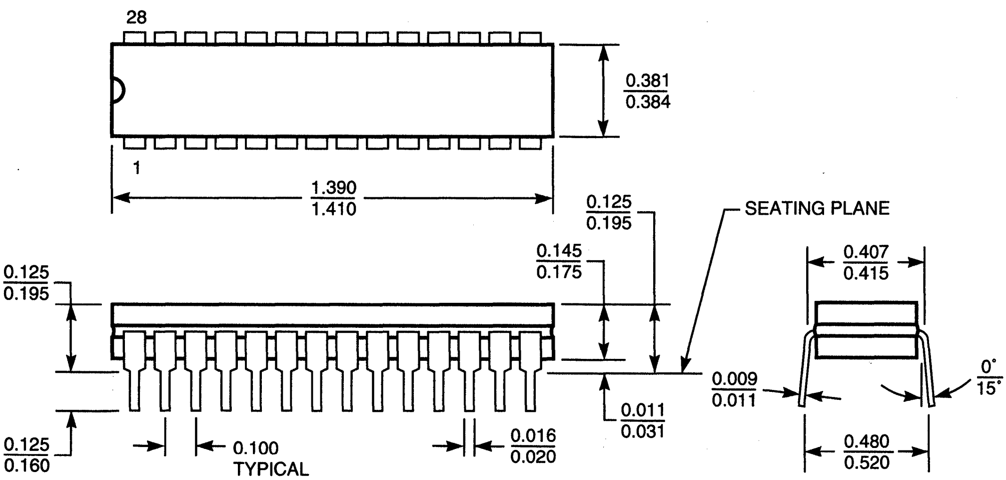


Ceramic DIP (Ordering Code: C, I)

C9 — 32-pin, 0.6" wide

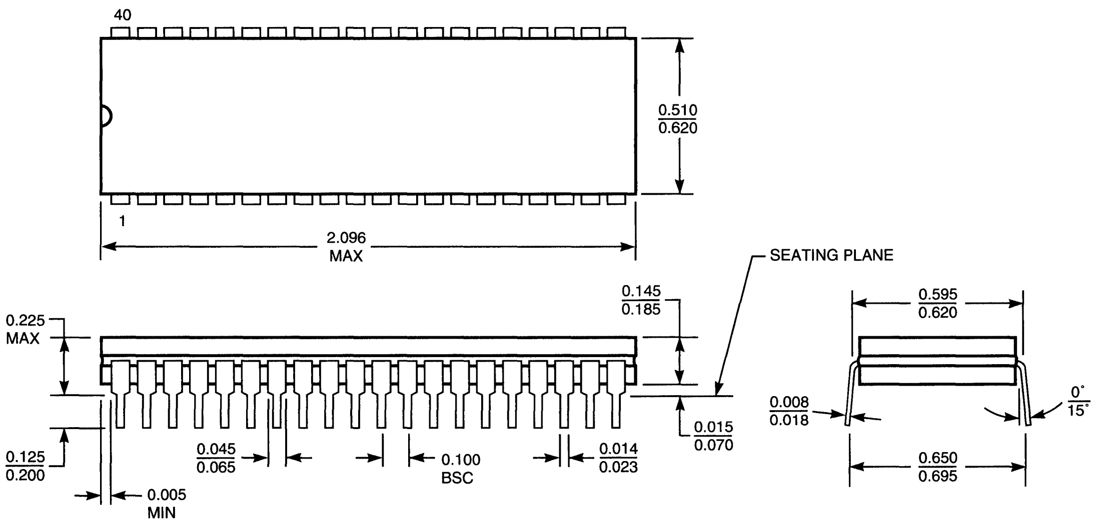


C10 — 28-pin, 0.4" wide



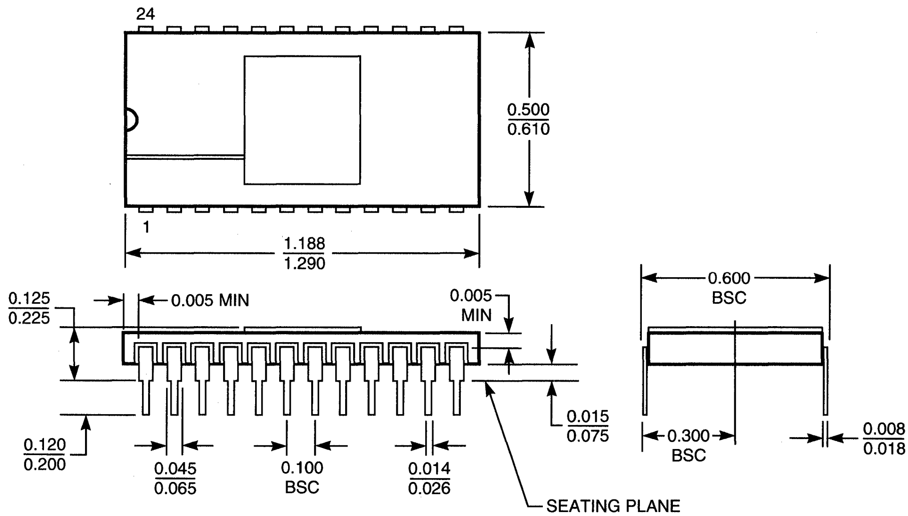
Ceramic DIP (Ordering Code: C, I)

C11 — 40-pin, 0.6" wide

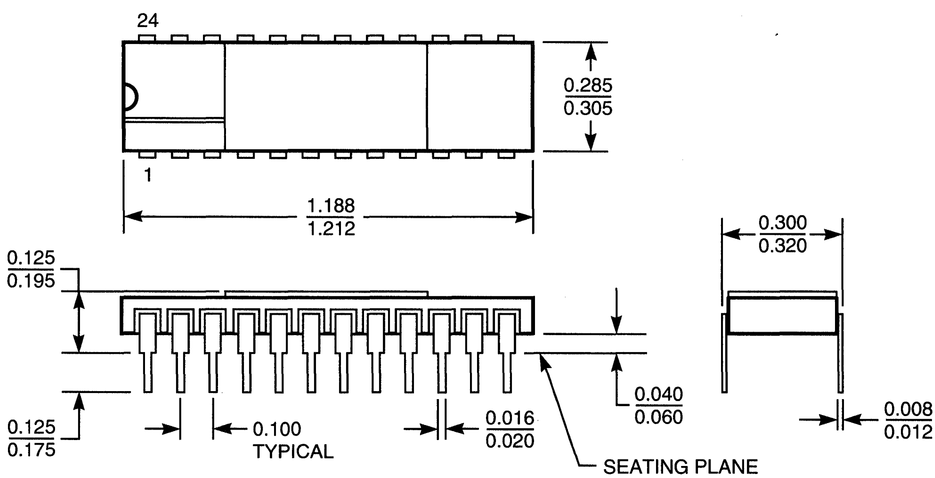


Sidebraze, Hermetic DIP (Ordering Code: D, H)

D1 — 24-pin, 0.6" wide

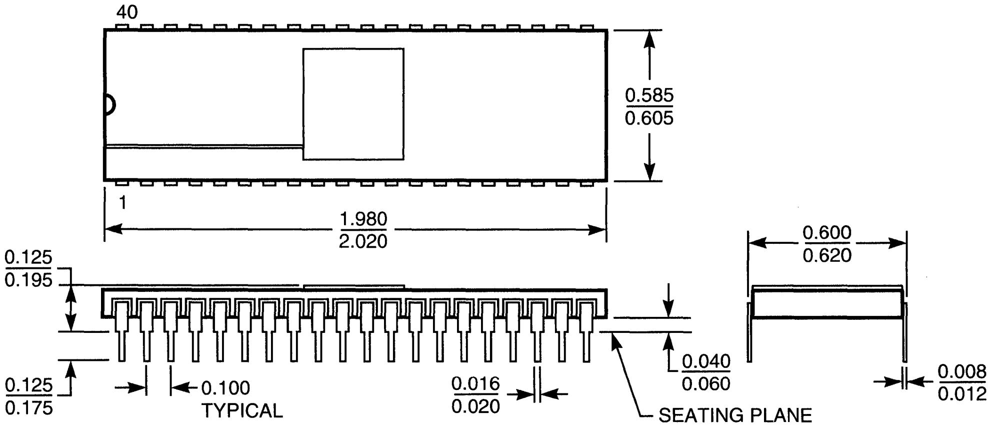


D2 — 24-pin, 0.3" wide

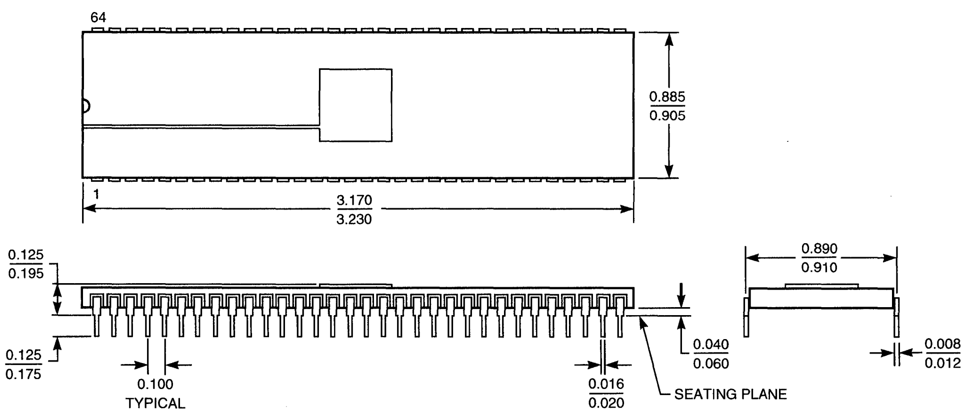


Sidebraze, Hermetic DIP (Ordering Code: D, H)

D3 — 40-pin, 0.6" wide

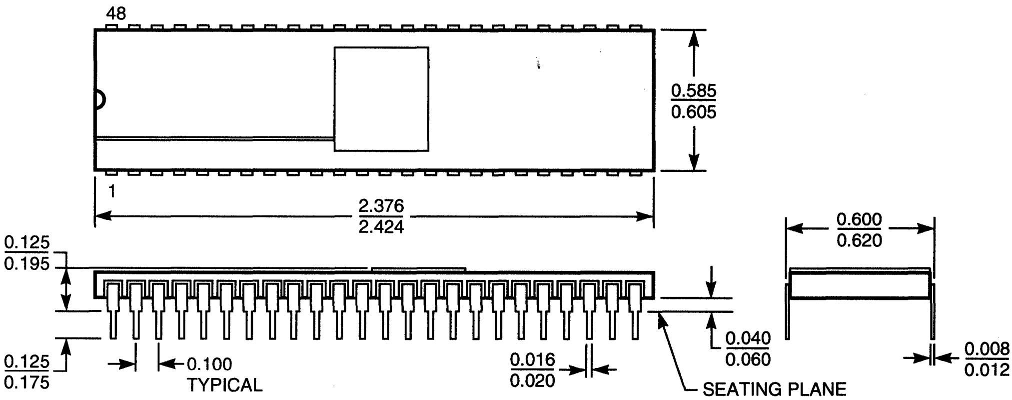


D4 — 64-pin, 0.9" wide, cavity up

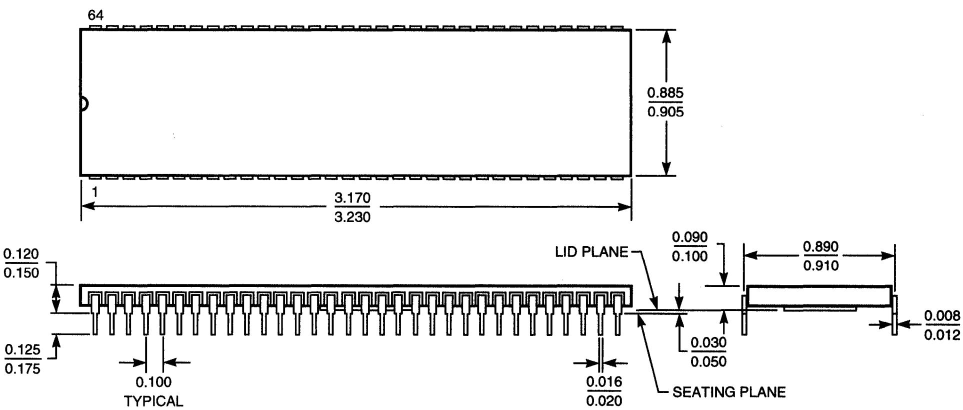


Sidebraze, Hermetic DIP (Ordering Code: D, H)

D5 — 48-pin, 0.6" wide

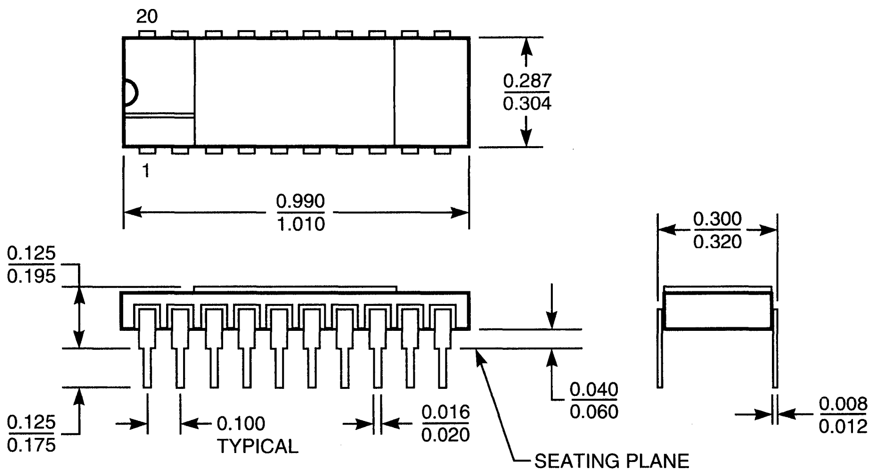


D6 — 64-pin, 0.9" wide, cavity down

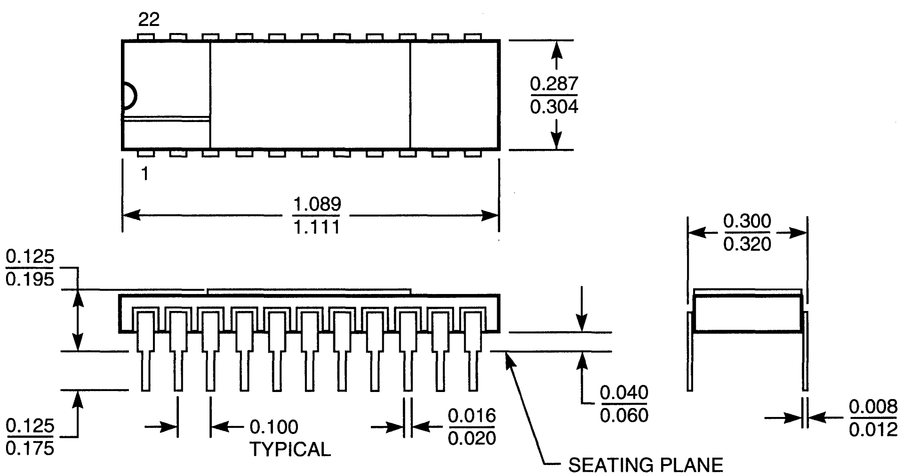


Sidebraze, Hermetic DIP (Ordering Code: D, H)

D7 — 20-pin, 0.3" wide

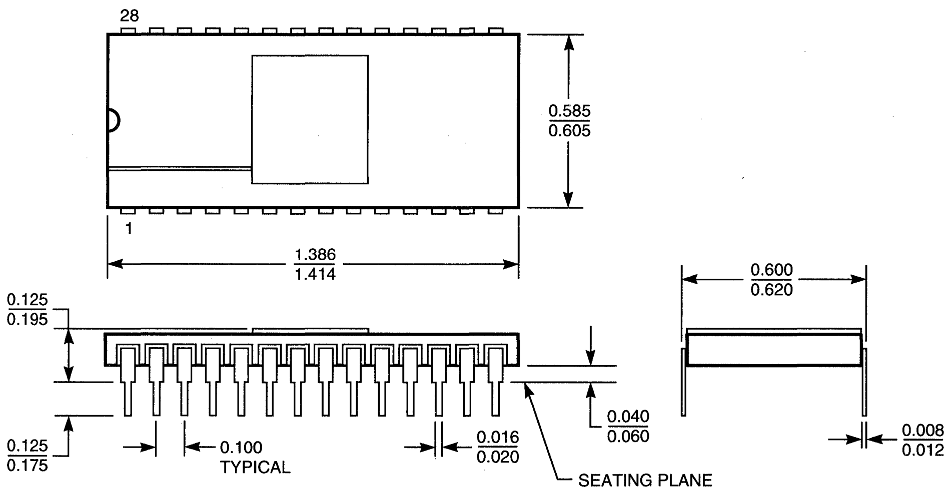


D8 — 22-pin, 0.3" wide

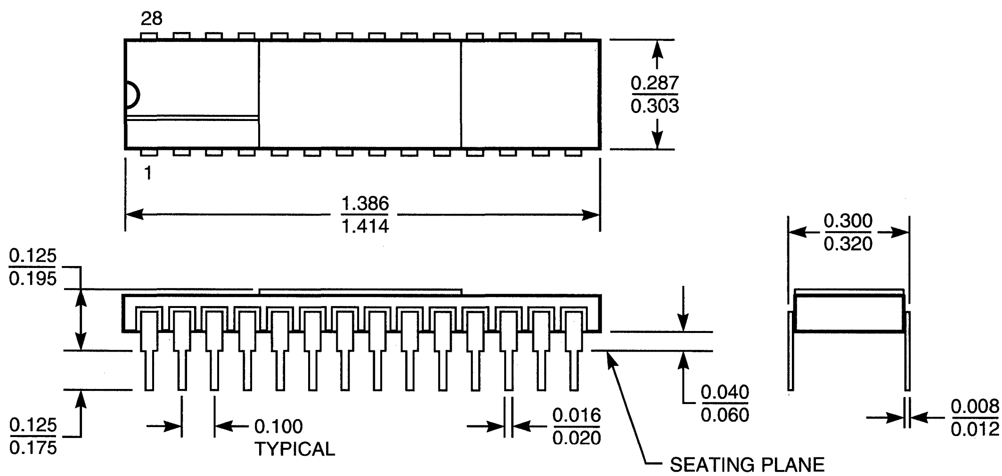


Sidebraze, Hermetic DIP (Ordering Code: D, H)

D9 — 28-pin, 0.6" wide

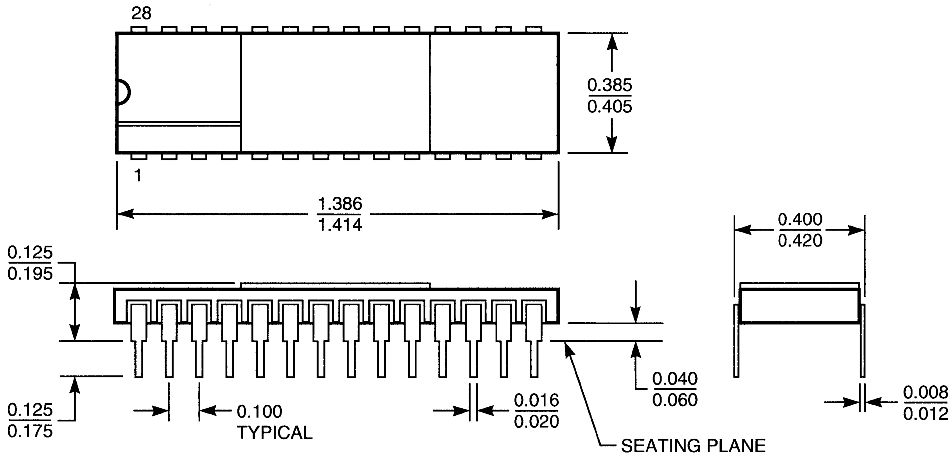


D10 — 28-pin, 0.3" wide

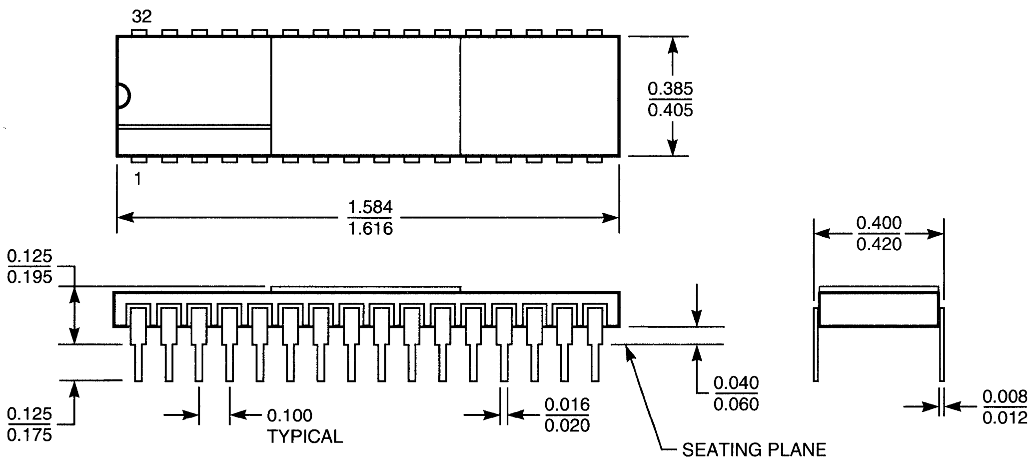


Sidebraze, Hermetic DIP (Ordering Code: D, H)

D11 — 28-pin, 0.4" wide

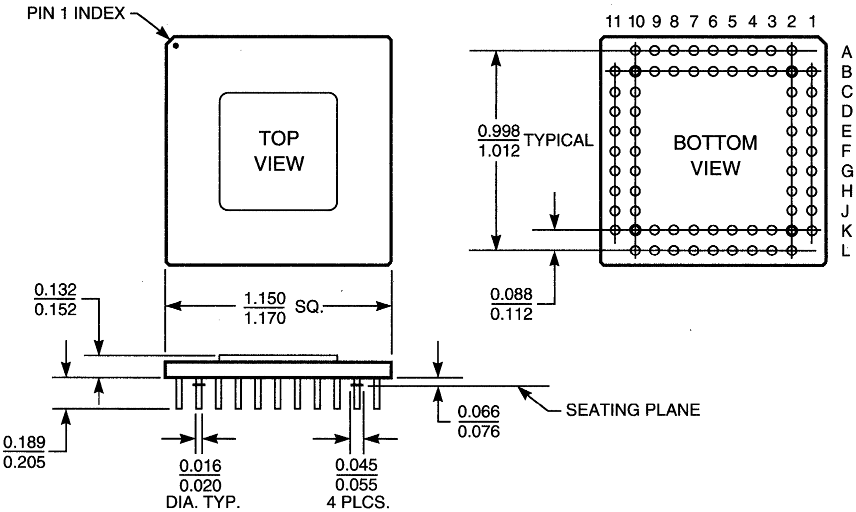


D12 — 32-pin, 0.4" wide

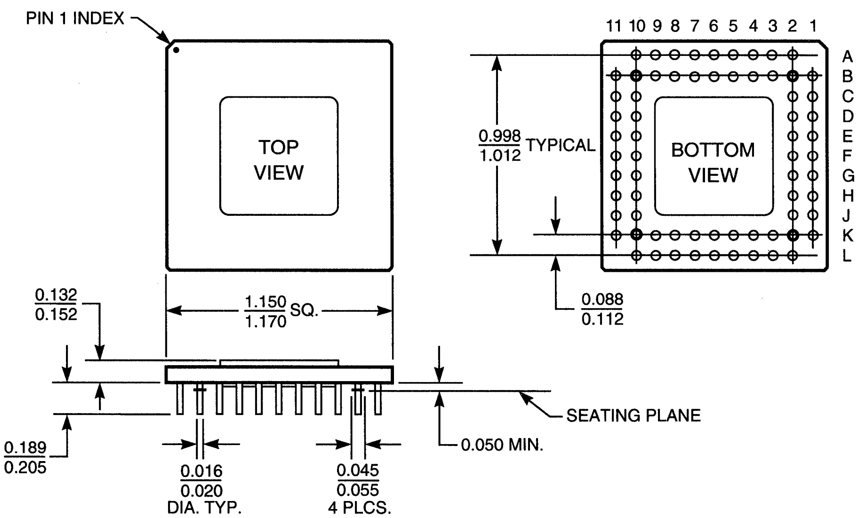


COMMERCIAL PGA (ORDERING CODE: E)

E1 — 68-pin, cavity up

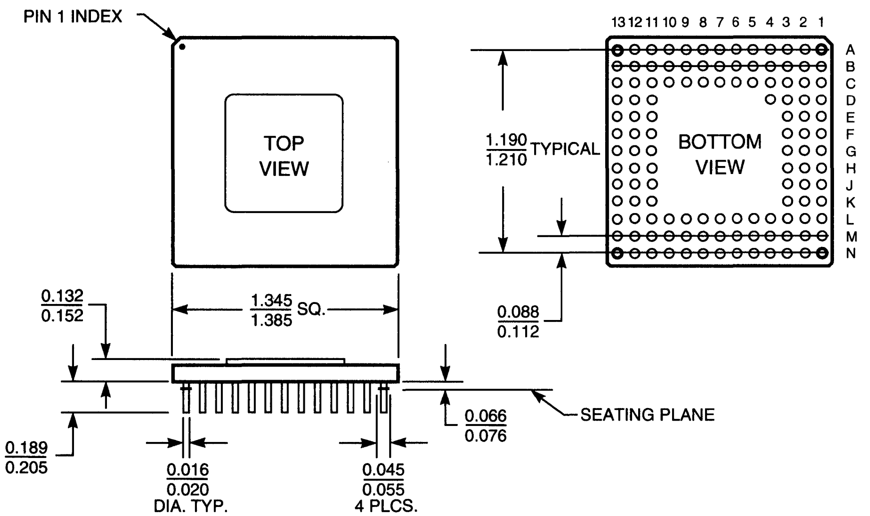


E2 — 68-pin, cavity down



Commercial PGA (Ordering Code: E)

E3 — 120-pin



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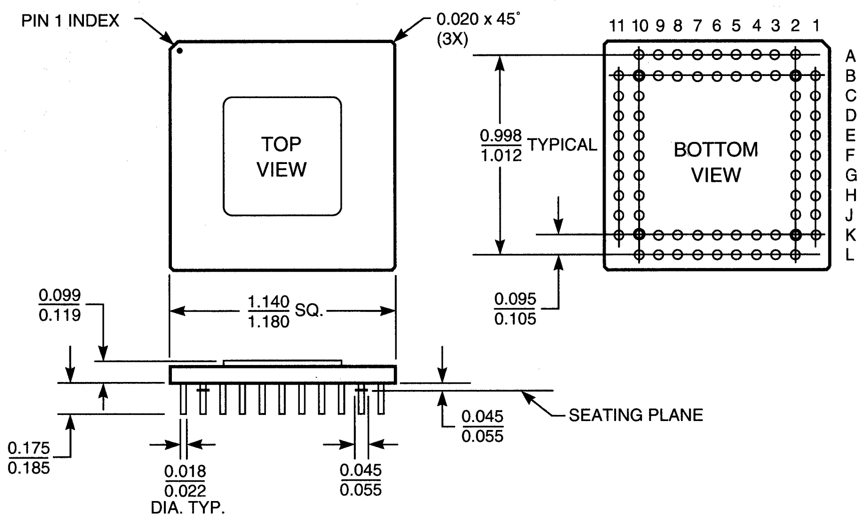
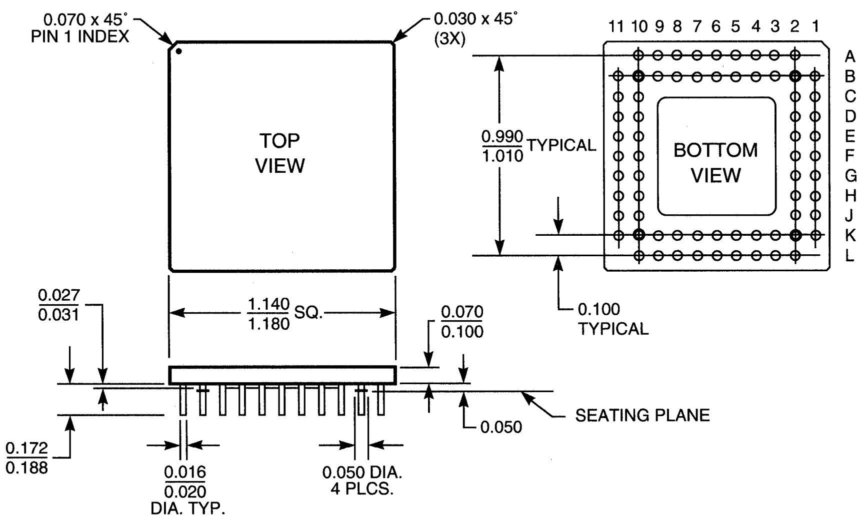
Ceramic PGA (Ordering Code: G)

G1 — 68-pin, cavity up

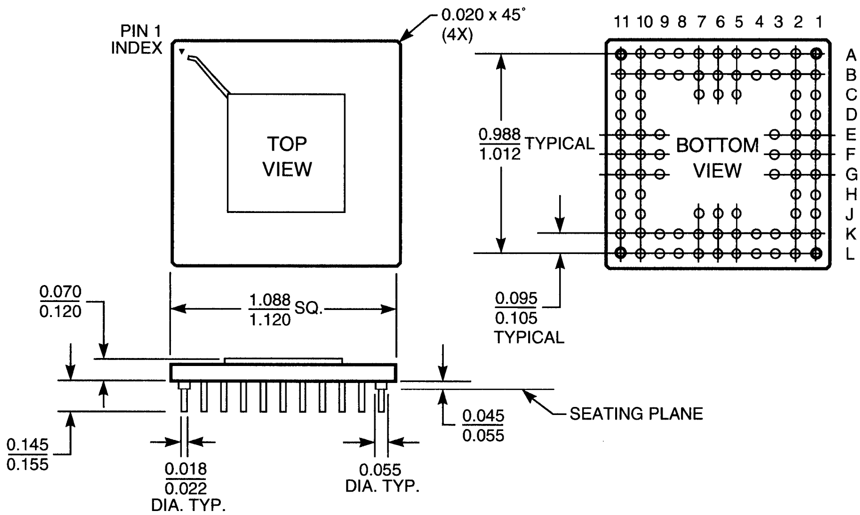


G2 — 68-pin, cavity down

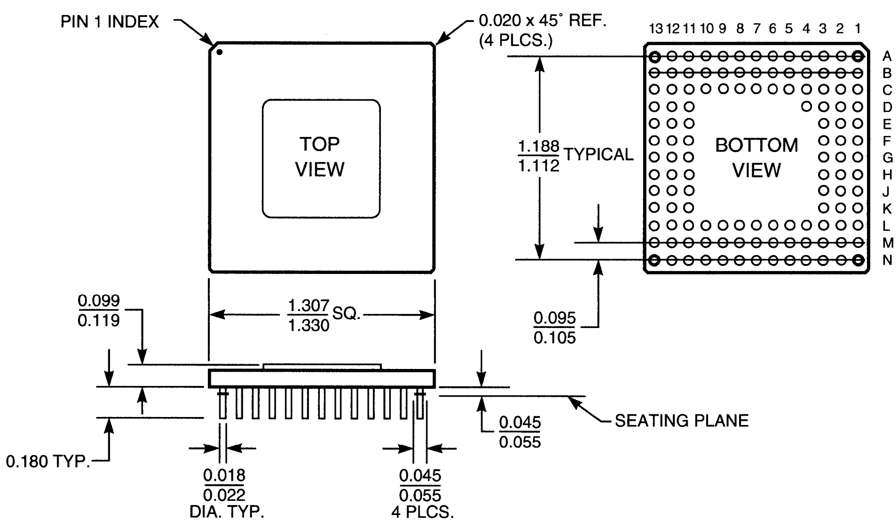


Ceramic PGA (Ordering Code: G)

G3 — 84-pin



G4 — 120-pin



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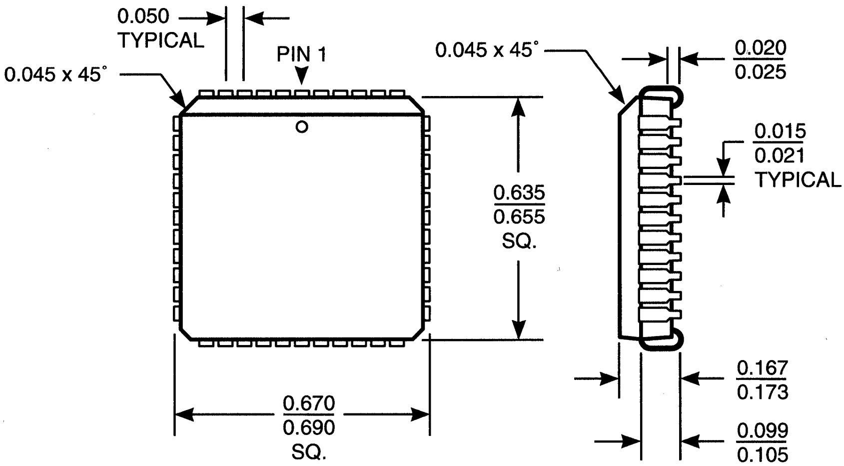
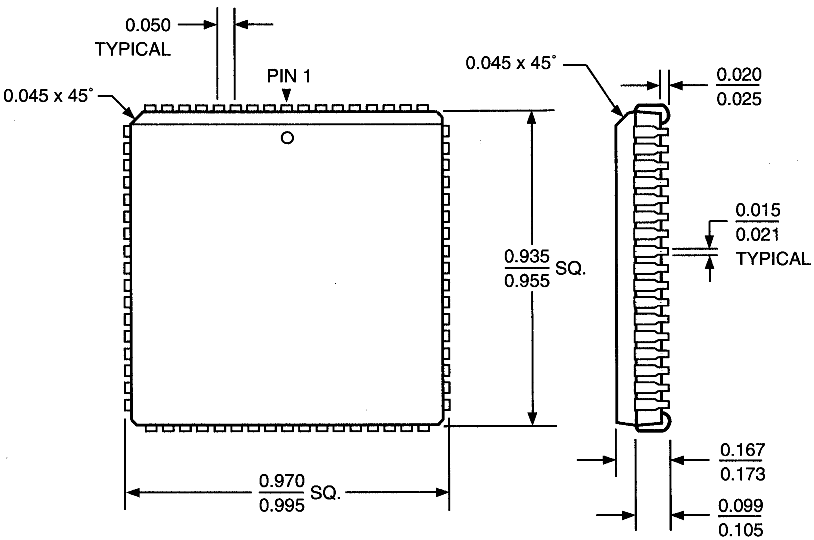
Plastic J-Lead Chip Carrier (Ordering Code: J)

J1 — 44-pin, 0.690" x 0.690"

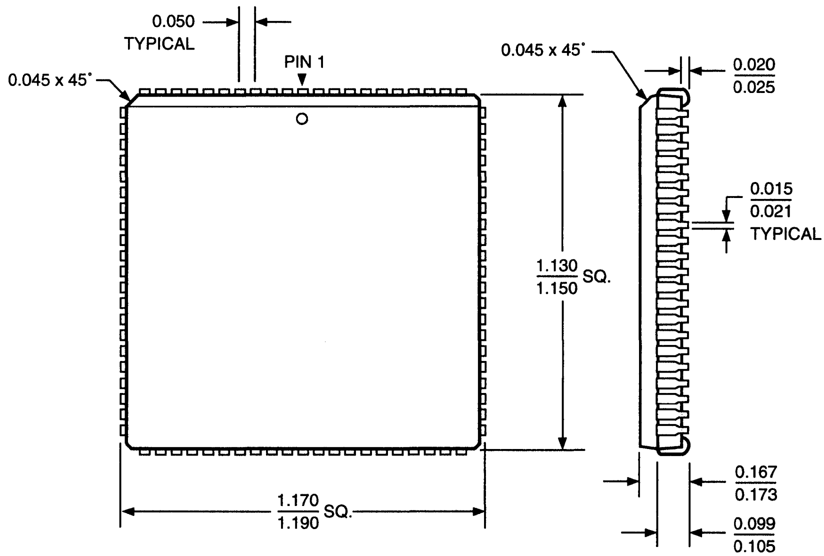


J2 — 68-pin, 0.990" x 0.990"

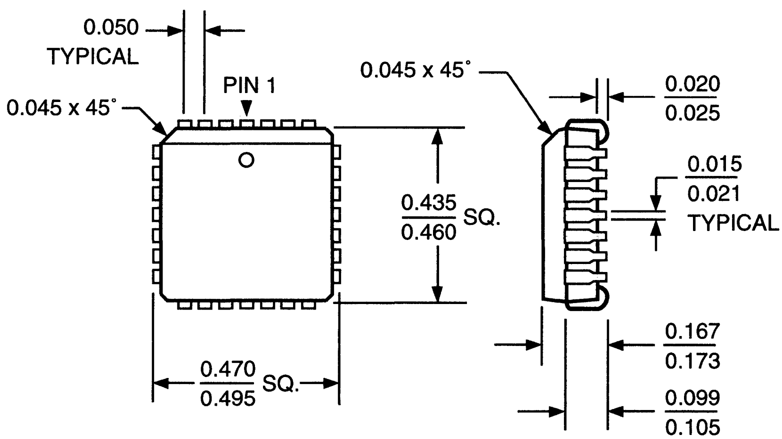


Plastic J-Lead Chip Carrier (Ordering Code: J)

J3 — 84-pin, 1.190" x 1.190"

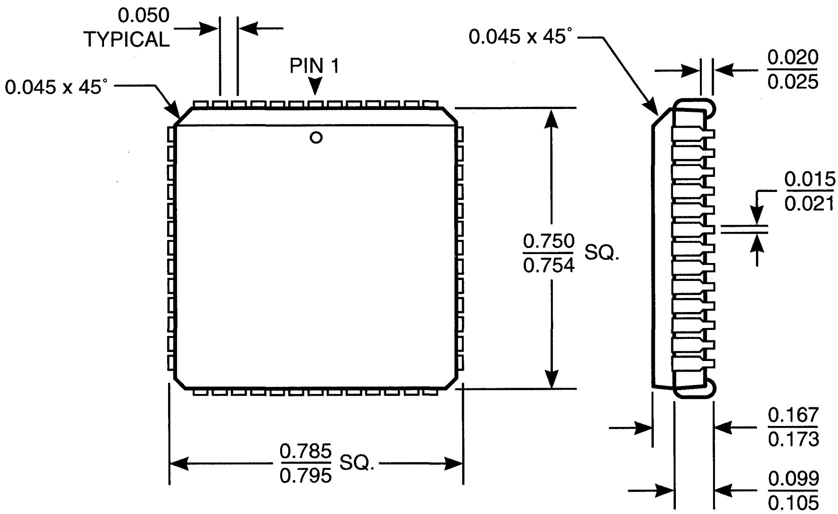


J4 — 28-pin, 0.490" x 0.490"

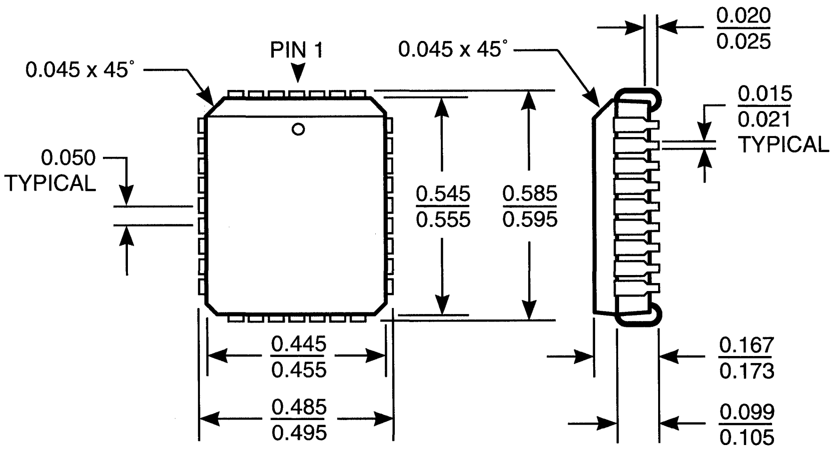


Plastic J-Lead Chip Carrier (Ordering Code: J)

J5 — 52-pin, 0.790" x 0.790"

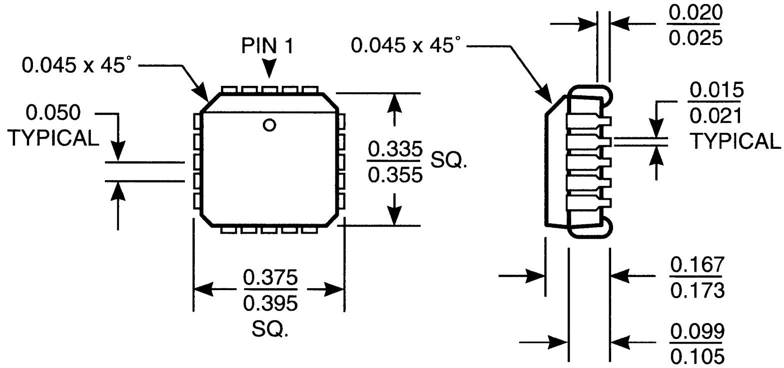


J6 — 32-pin, 0.490" x 0.590"



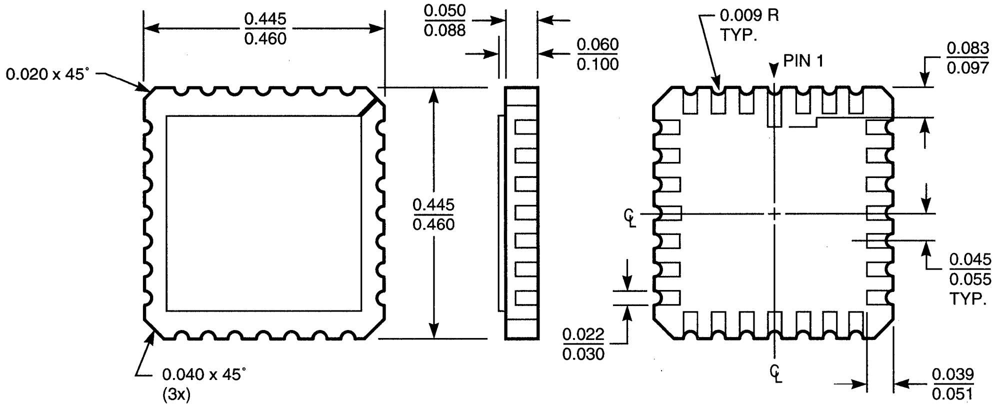
Plastic J-Lead Chip Carrier (Ordering Code: J)

J7 — 20-pin, 0.390" x 0.390"



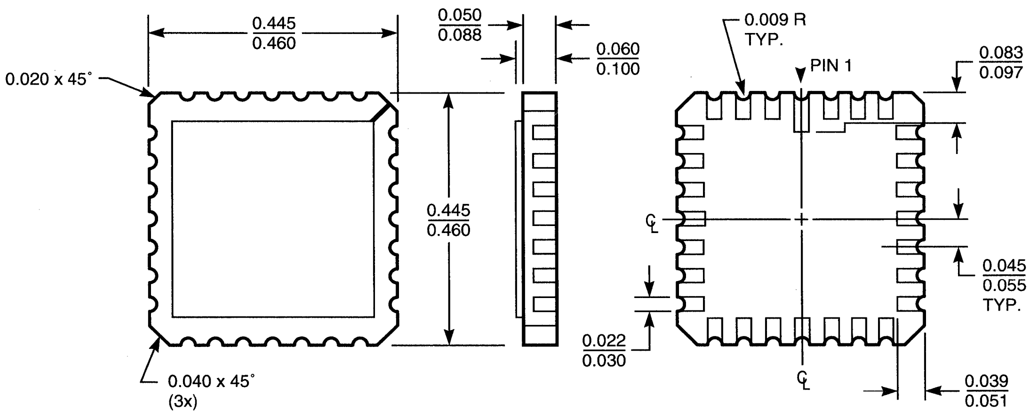
Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K1 — 28-pin, 0.450" x 0.450"



Top View   Side View   Bottom View

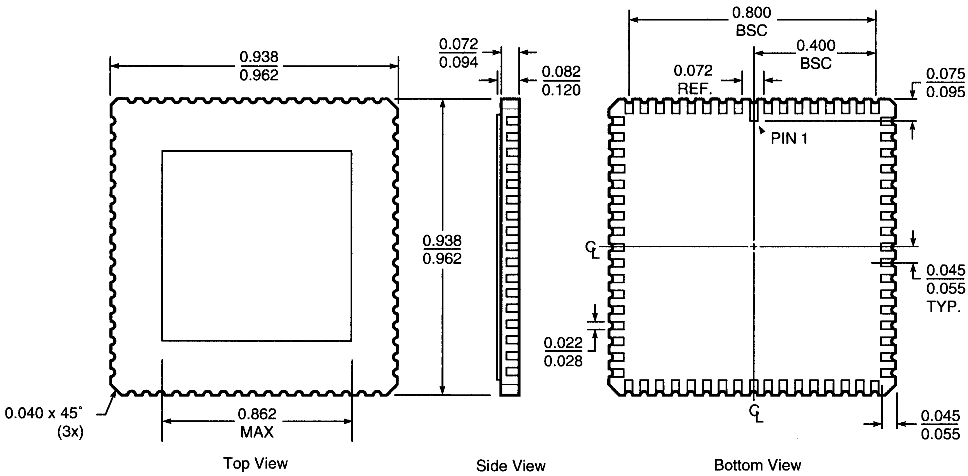
K2 — 44-pin, 0.650" x 0.650"



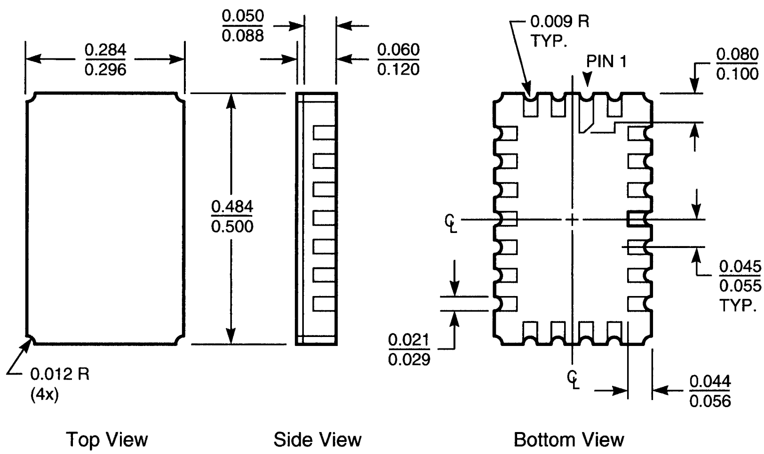
Top View   Side View   Bottom View

Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K3 — 68-pin, 0.950" x 0.950"

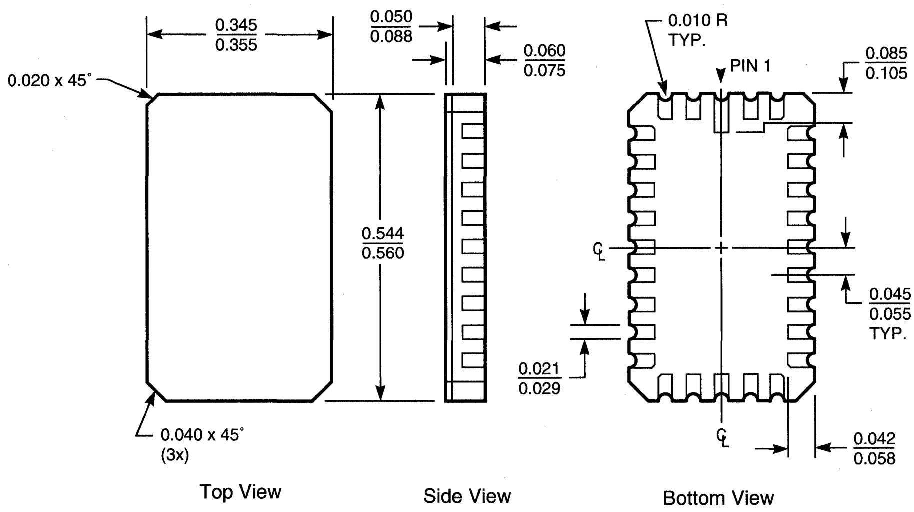


K4 — 22-pin, 0.290" x 0.490"

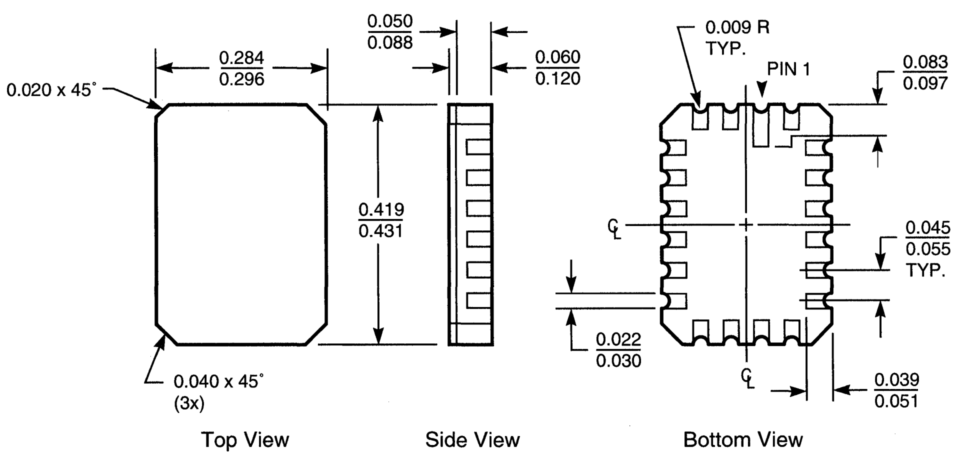


Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K5 — 28-pin, 0.350" x 0.550"

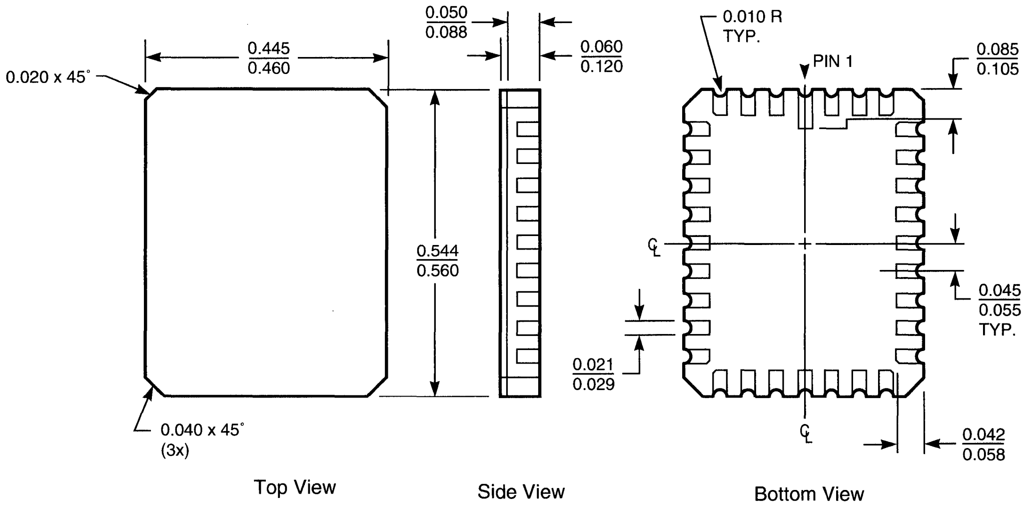


K6 — 20-pin, 0.290" x 0.425"

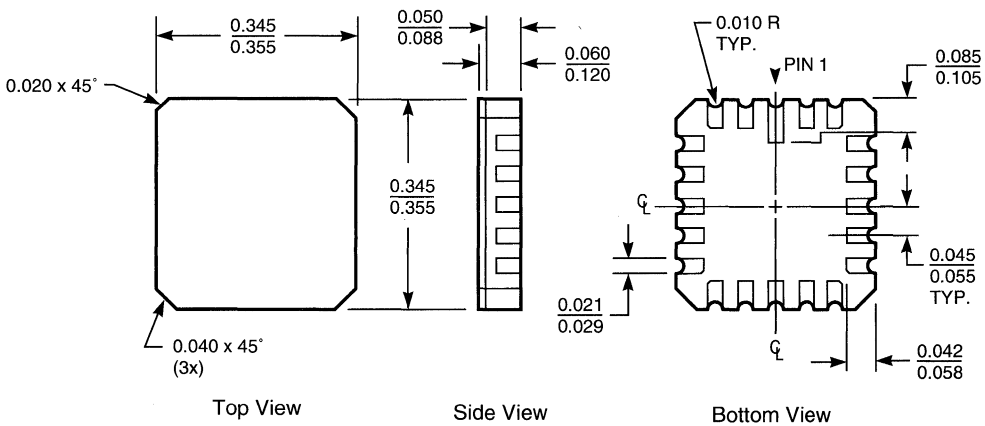


Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K7 — 32-pin, 0.450" x 0.550"

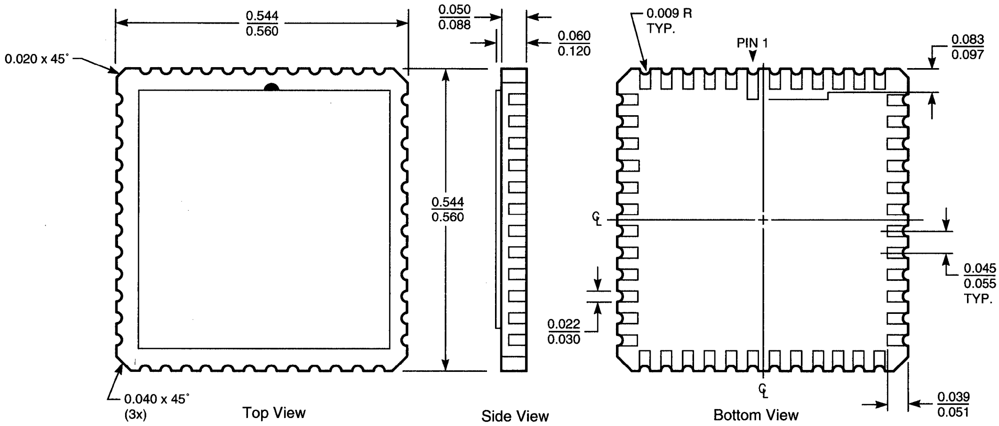


K8 — 20-pin, 0.350" x 0.350"

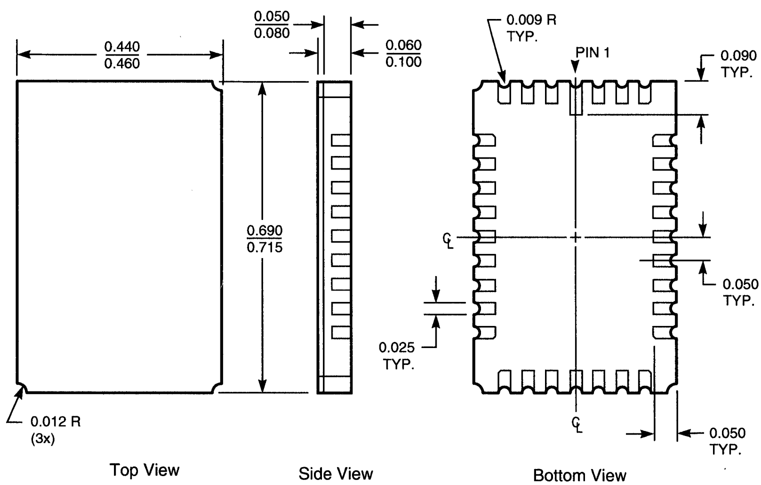


Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K9 — 48-pin, 0.550" x 0.550"

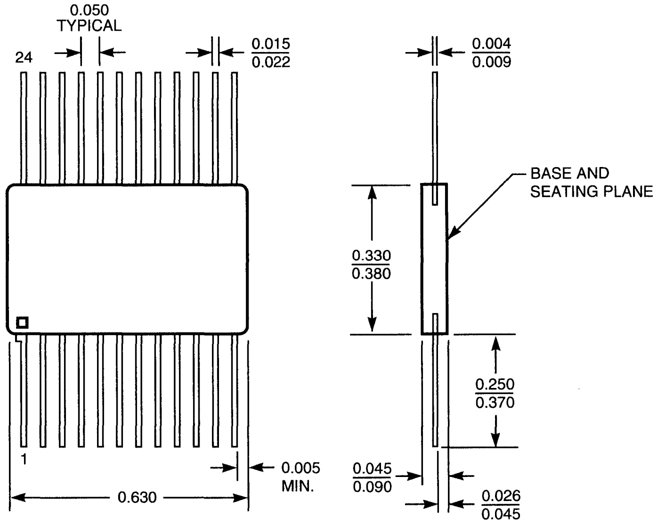


K10 — 32-pin, 0.450" x 0.700"

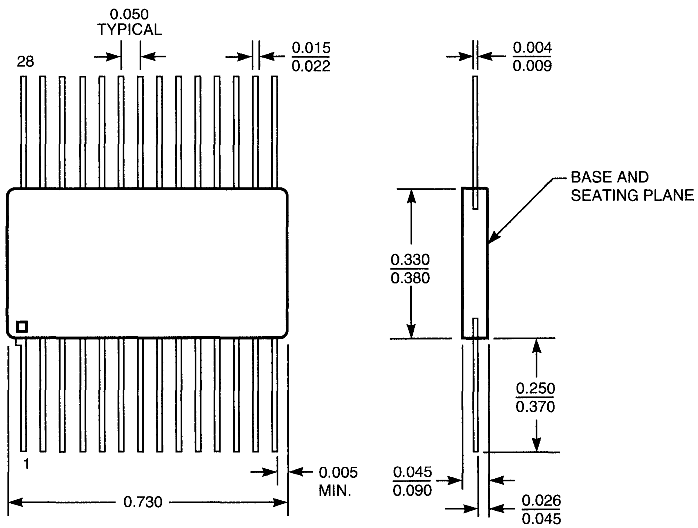


Ceramic Flatpack (Ordering Code: M)

M1 — 24-pin

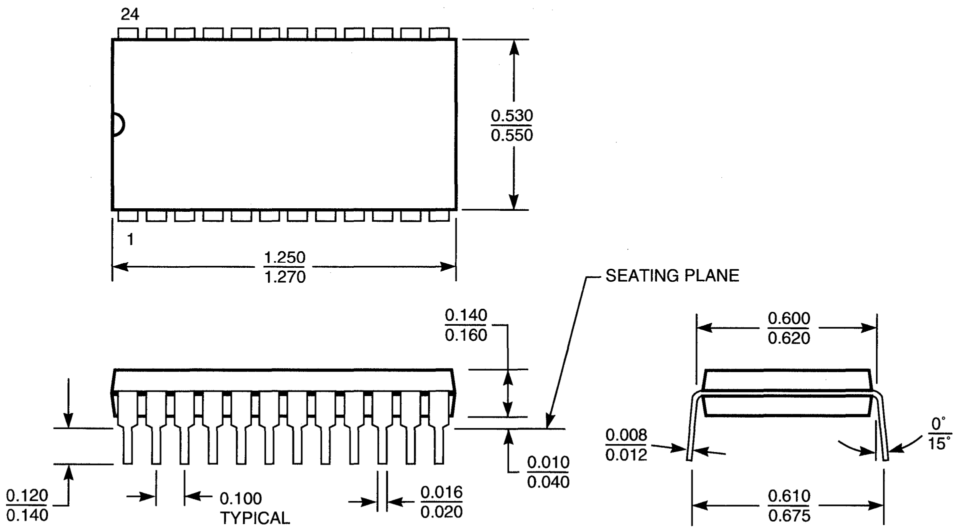


M2 — 28-pin

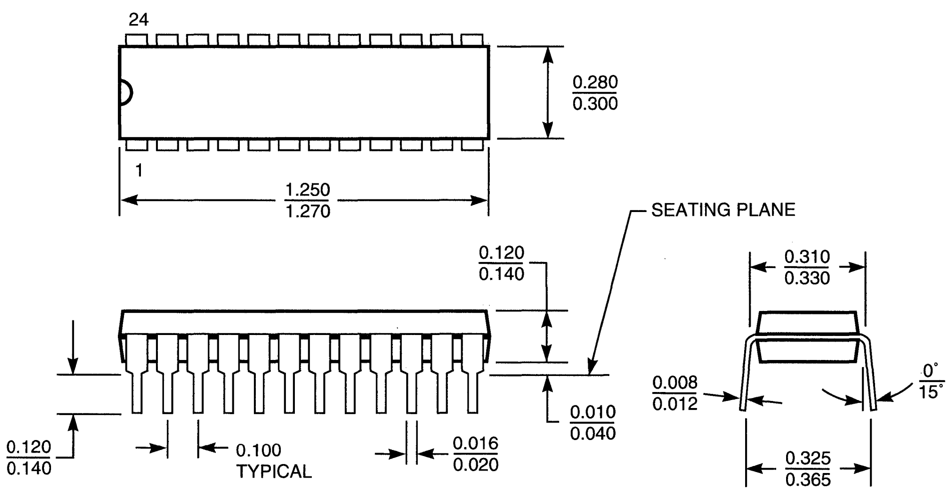


Plastic DIP (Ordering Code: P, N)

P1 — 24-pin, 0.6" wide

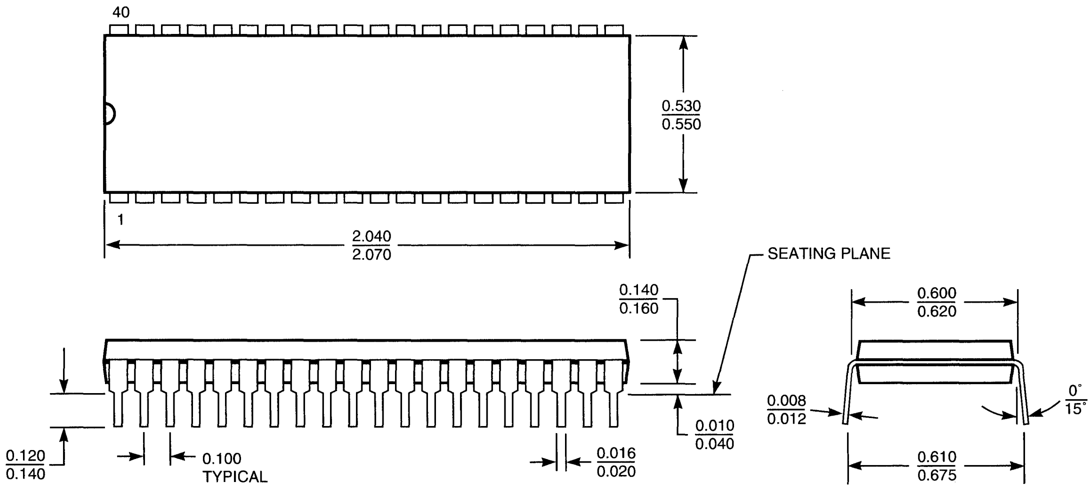


P2 — 24-pin, 0.3" wide

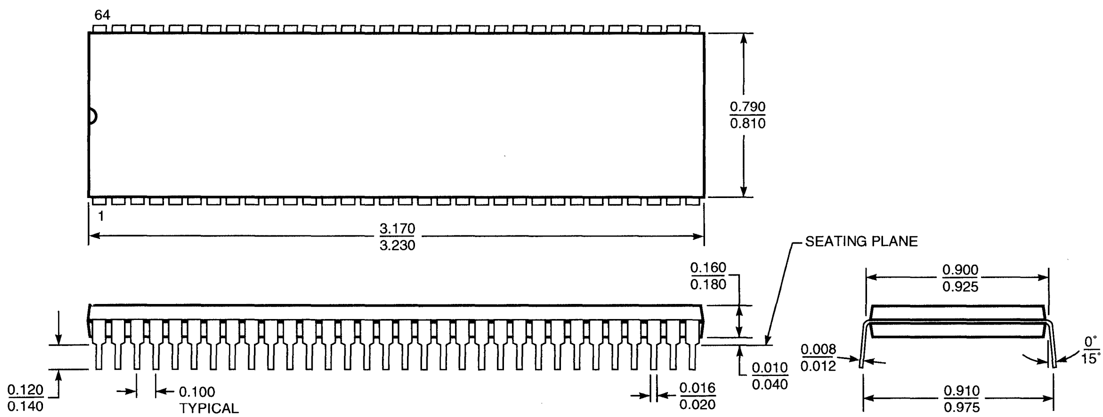


Plastic DIP (Ordering Code: P, N)

P3 — 40-pin, 0.6" wide

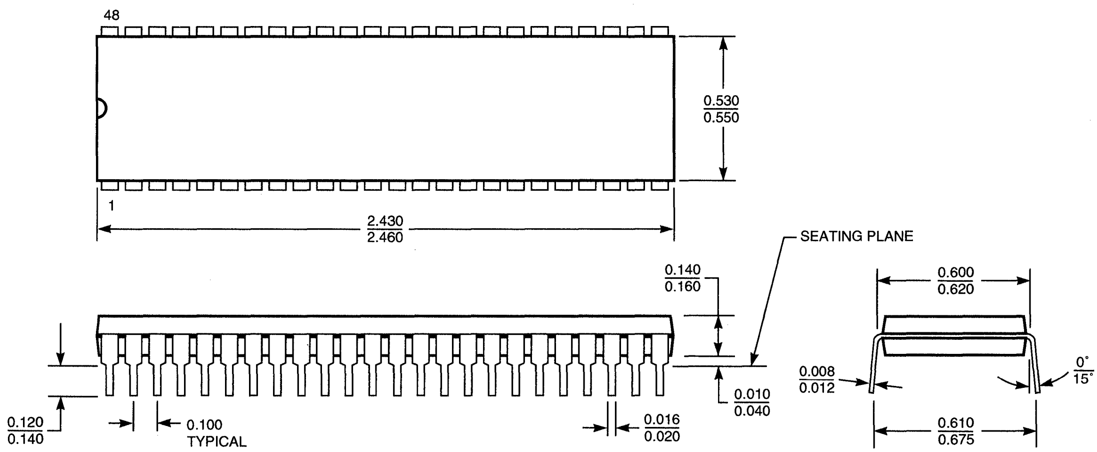


P4 — 64-pin, 0.9" wide

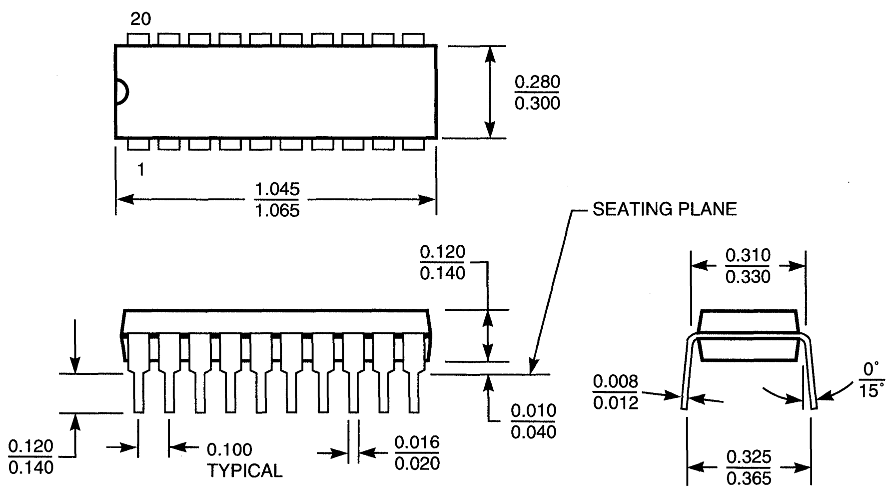


Plastic DIP (Ordering Code: P, N)

P5 — 48-pin, 0.6" wide

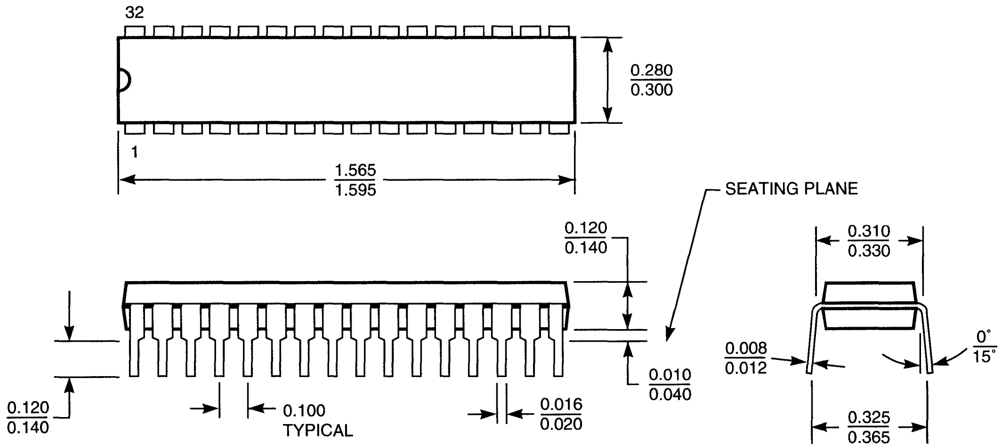


P6 — 20-pin, 0.3" wide

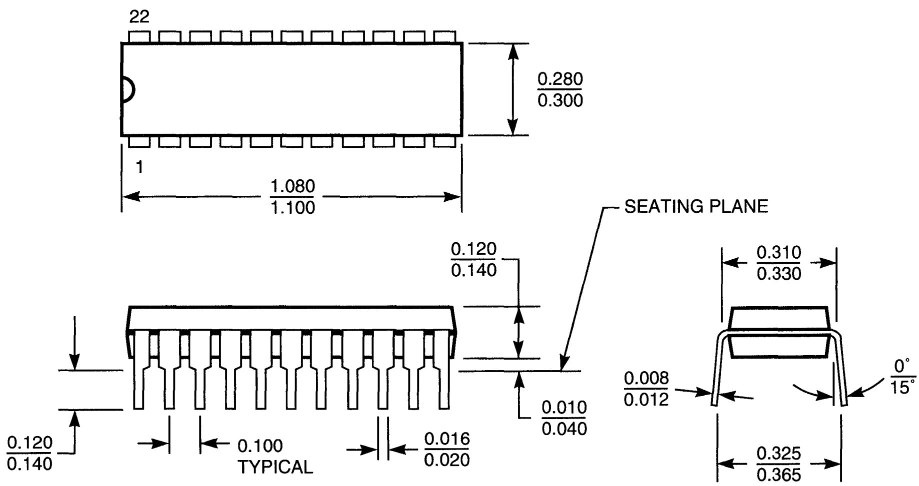


Plastic DIP (Ordering Code: P, N)

P7 — 32-pin, 0.3" wide

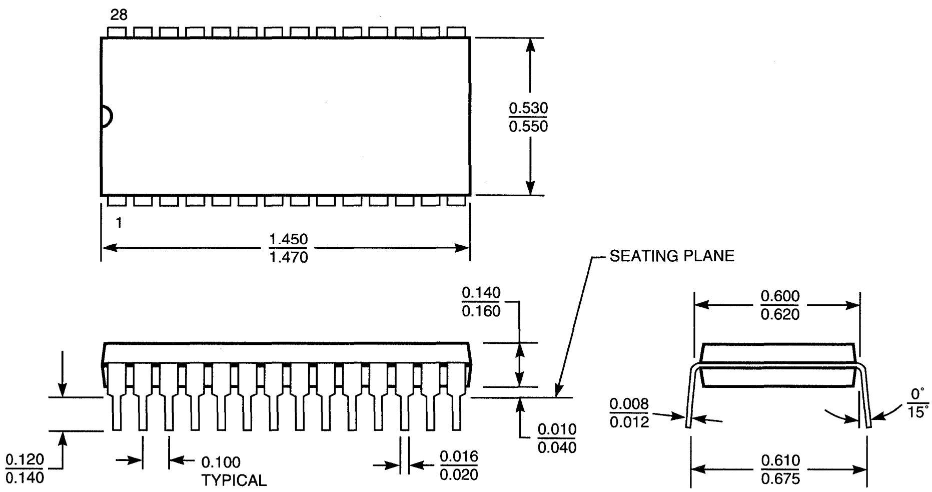


P8 — 22-pin, 0.3" wide

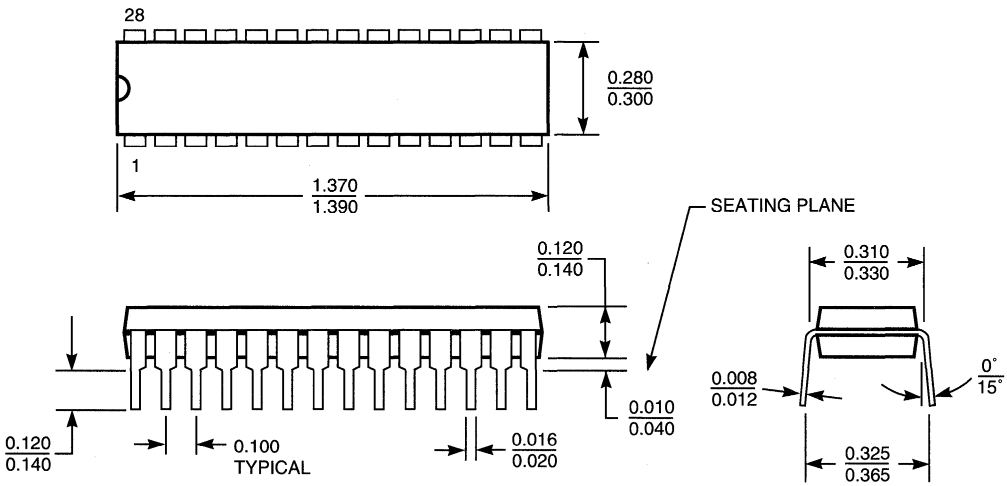


PLASTIC DIP (ORDERING CODE: P, N)

P9 — 28-pin, 0.6" wide

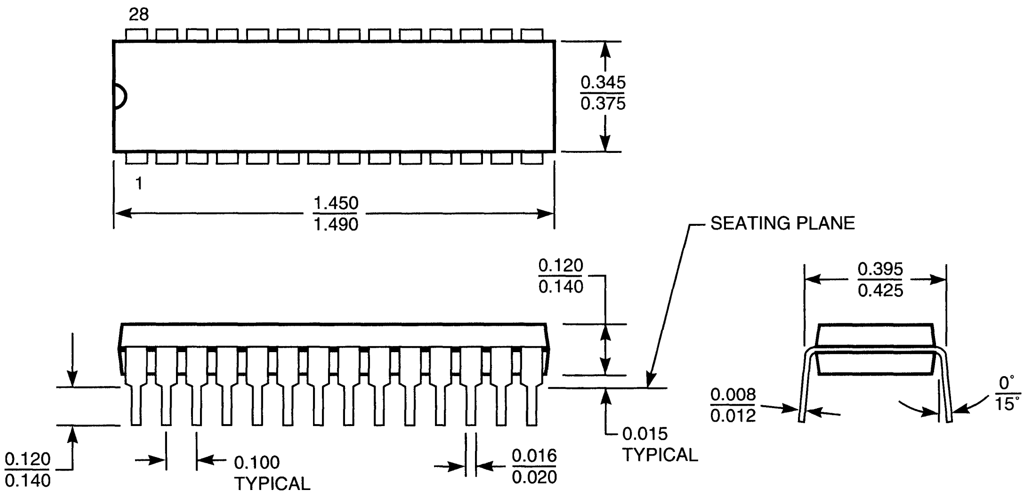


P10 — 28-pin, 0.3" wide

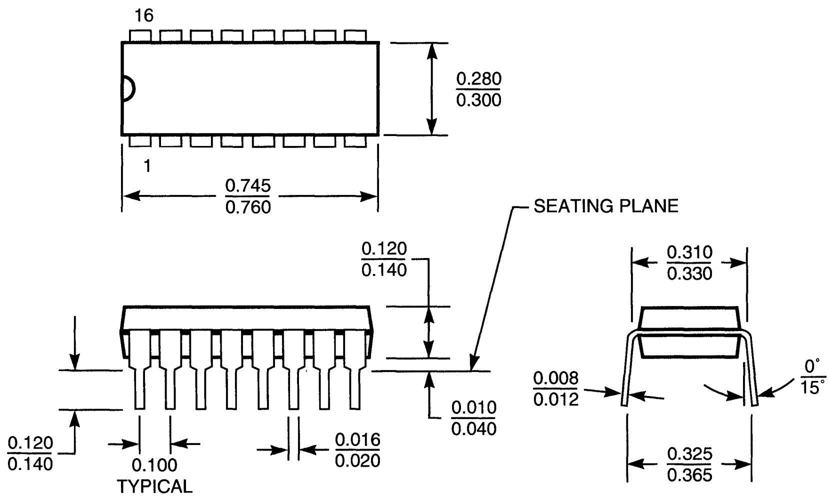


Plastic DIP (Ordering Code: P, N)

P11 — 28-pin, 0.4" wide

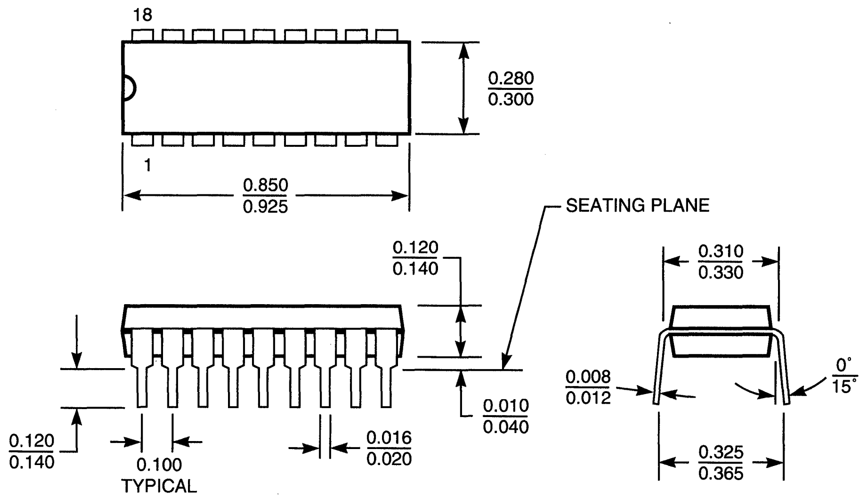


P12 — 16-pin, 0.3" wide

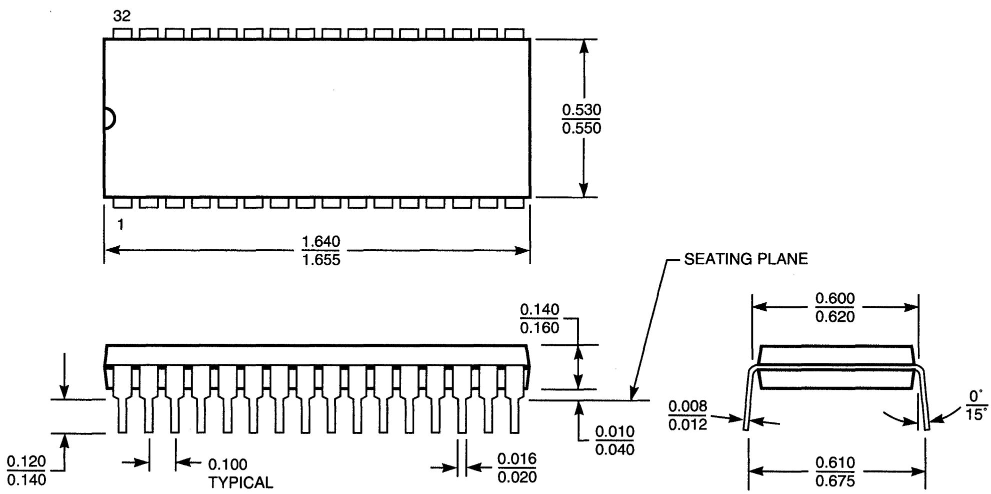


Plastic DIP (Ordering Code: P, N)

P13 — 18-pin, 0.3" wide

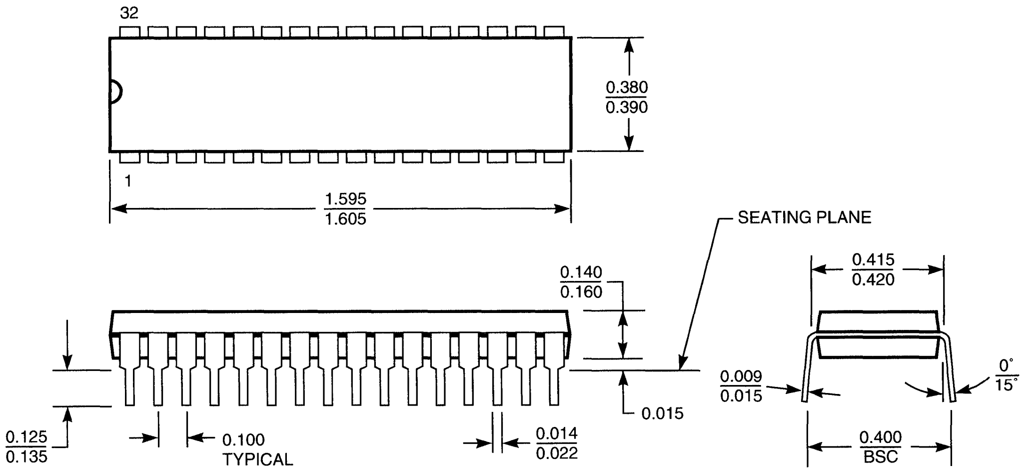


P14 — 32-pin, 0.6" wide



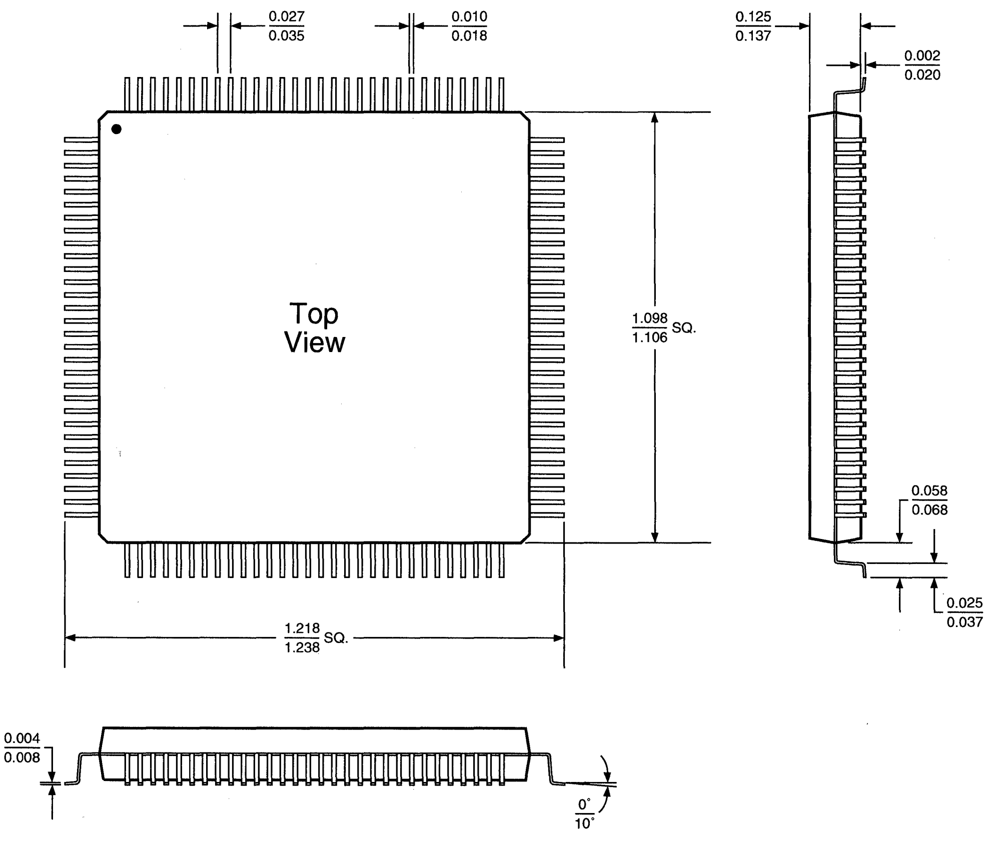
Plastic DIP (Ordering Code: P, N)

P15 — 32-pin, 0.4" wide



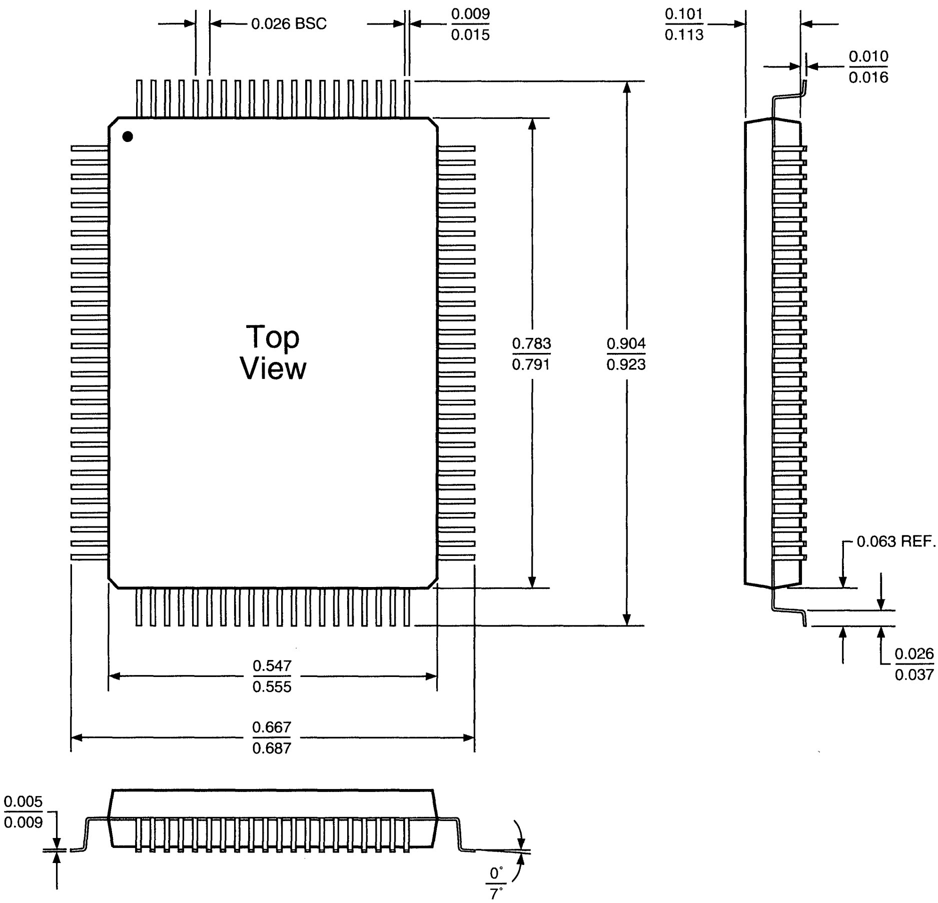
Plastic Quad Flatpack (Ordering Code: Q)

Q1 — 120-pin



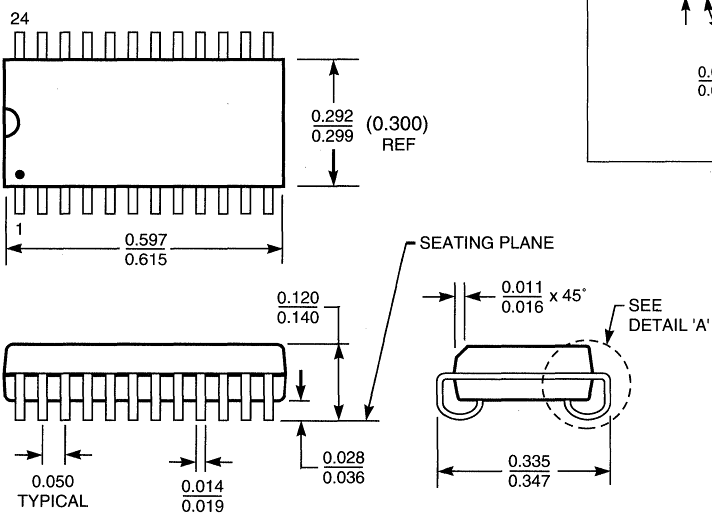
Plastic Quad Flatpack (Ordering Code: Q)

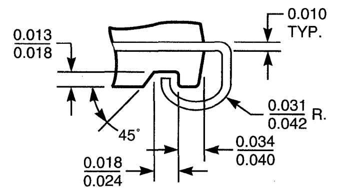
Q2 — 100-pin



Plastic SOJ (Ordering Code: W)

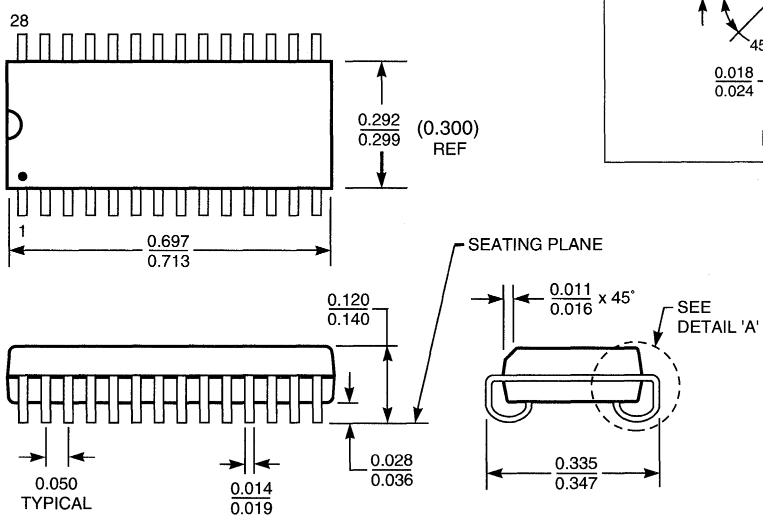
W1 — 24-pin, 0.3" wide

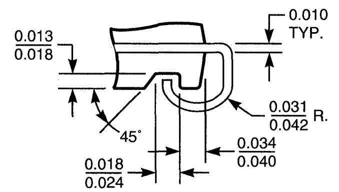




Detail A

W2 — 28-pin, 0.3" wide

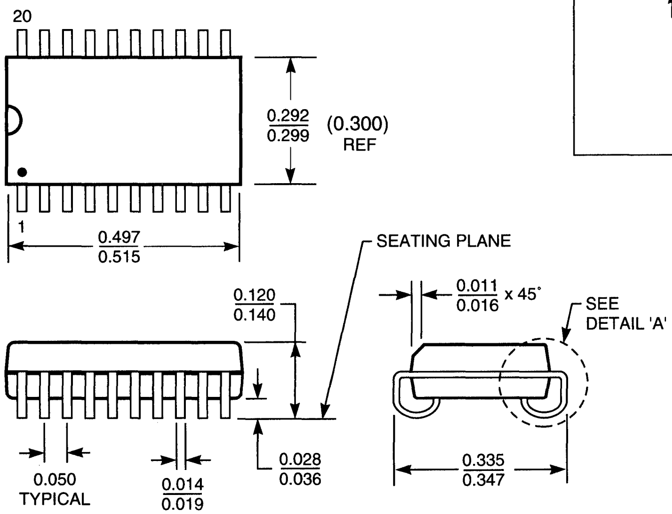


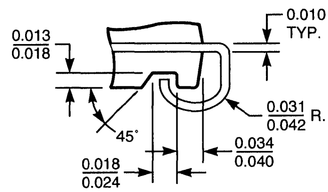


Detail A

Plastic SOJ (Ordering Code: W)

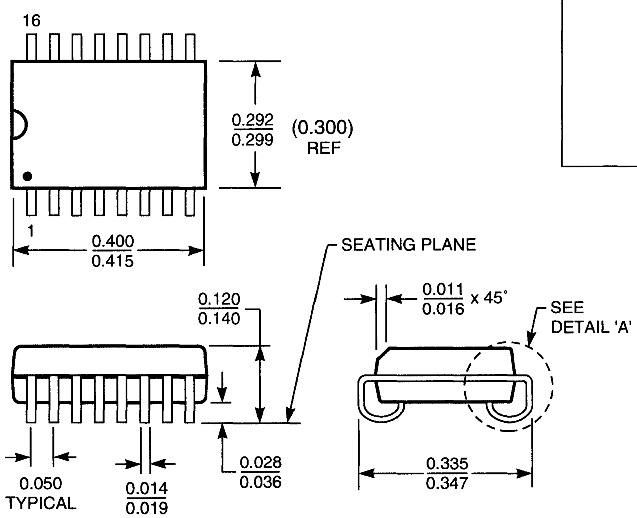
W3 — 20-pin, 0.3" wide

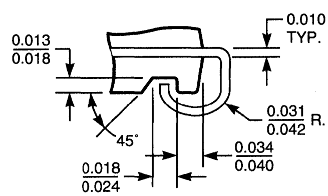




Detail A

W4 — 16-pin, 0.3" wide

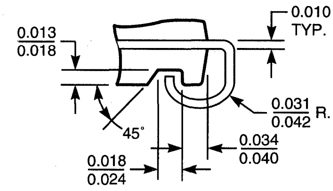




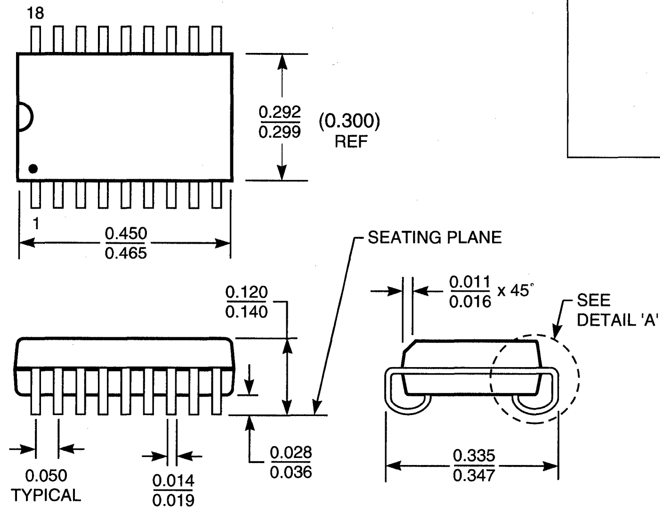
Detail A

Plastic SOJ (Ordering Code: W)

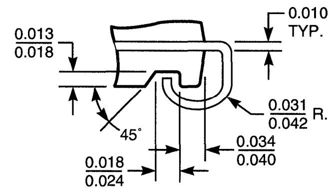
W5 — 18-pin, 0.3" wide



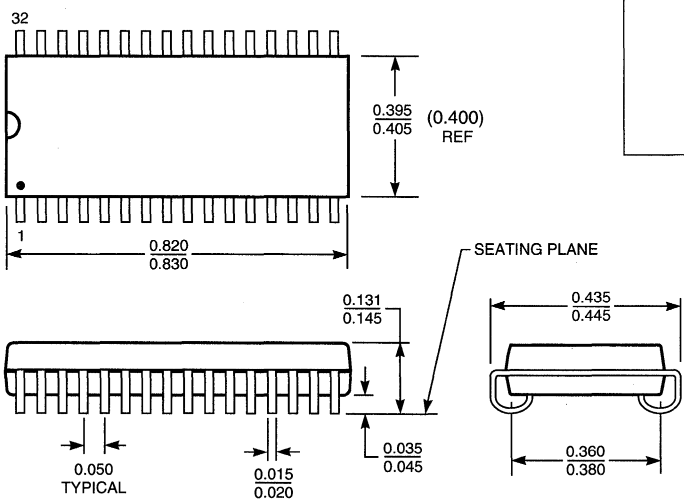
Detail A



W6 — 32-pin, 0.4" wide

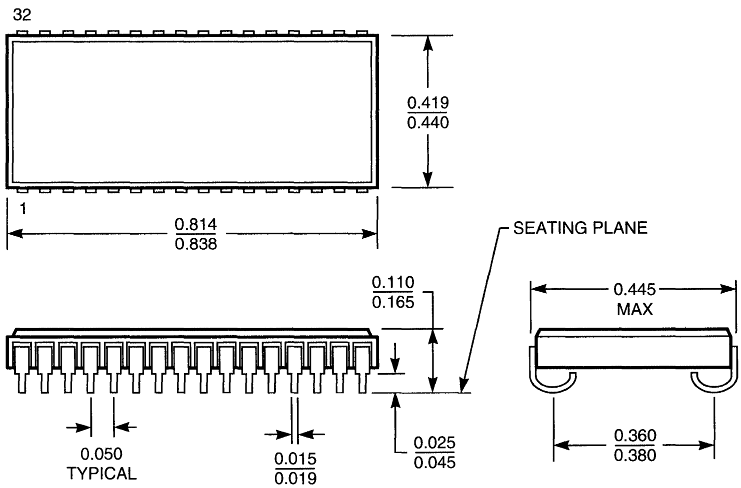


Detail A



Ceramic SOJ (Ordering Code: Y)

Y1 — 32-pin, 0.440" wide



Product Listing

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DSP PRODUCTS

PART NO.	PRODUCT DESCRIPTION	SPEED (ns) COM.	SPEED (ns) MIL.	POWER (mW)	PACKAGE AVAILABILITY
VIDEO IMAGING PRODUCTS					
LF2242	12/16-bit Half-Band Digital Filter	15	TBA	—	44-lead PLCC
LF2246	11 x 10-bit Image Filter	25	TBA	—	120-pin PGA, 120-pin PQFP
LF2249	12 x 12-bit Digital Mixer	25	TBA	—	120-pin PGA, 120-pin PQFP
LF2250	12 x 10-bit Matrix Multiplier	25	TBA	—	120-pin PGA, 120-pin PQFP
LF2272	Colorspace Converter (3 x 12-bits)	25	TBA	—	120-pin PGA
LF43881	8 x 8-bit Digital Filter	33	40	—	84-pin PGA/PLCC, 100-pin PQFP
LF43891	9 x 9-bit Digtial Filter	33	40	—	84-pin PGA/PLCC, 100-pin PQFP
ARITHMETIC LOGIC UNITS					
L4C381	16-bit Cascadable ALU	15	20	75	68-lead LCC/PLCC, 68-pin PGA
L29C101	16-bit ALU Slice (Quad 2901)	35	45	75	64-pin DIP, 68-pin PGA
BARREL SHIFTERS					
LSH32	32-bit Barrel Shifter	20	30	50	68-lead LCC/PLCC, 68-pin PGA
LSH33	32-bit Barrel Shifter w/Registers	20	30	50	68-lead LCC/PLCC, 68-pin PGA
CORRELATORS					
L10C23	64 x 1 Digital Correlator	20	20	125	24-pin DIP, 28-lead LCC
MULTIPLIERS					
LMU08	8 x 8-bit, Signed	35	45	40	40-pin DIP, 44-lead LCC/PLCC
LMU8U	8 x 8-bit, Unsigned	35	45	40	40-pin DIP, 44-lead LCC/PLCC
LMU557	8 x 8-bit, Latched Output	60	70	85	40-pin DIP
LMU558	8 x 8-bit, Unregistered	60	70	85	40-pin DIP
LMU12	12 x 12-bit	35	45	60	64-pin DIP. 68-pin PGA
LMU112	12 x 12-bit, Reduced Pinout	50	55	50	48-pin DIP, 52-lead PLCC
LMU16	16 x 16-bit	45	55	60	64-pin DIP, 68-pin PGA
LMU216	16 x 16-bit, Surface Mount	45	55	60	68-lead LCC/PLCC
LMU17	16 x 16-bit, Microprogrammable	45	55	60	64-pin DIP, 68-pin PGA
LMU217	16 x 16-bit, Microprog., Surf. Mount	45	55	60	68-lead LCC/PLCC
LMU18	16 x 16-bit, 32 Outputs	35	45	125	84-pin PGA, 84-lead PLCC
MULTIPLIER-ACCUMULATORS					
LMA1009	12 x 12-bit	45	55	60	64-pin DIP, 68-pin PGA
LMA2009	12 x 12-bit, Surface Mount	45	55	60	68-lead LCC/PLCC
LMA1010	16 x 16-bit	45	55	60	64-pin DIP, 68-pin PGA
LMA2010	16 x 16-bit, Surface Mount	45	55	60	68-lead LCC/PLCC
MULTIPLIER-SUMMERS					
LMS12	12 x 12 + 26-bit, FIR	40	50	75	84-pin PGA, 84-lead PLCC

DSP PRODUCTS (CONTINUED)

PART NO.	PRODUCT DESCRIPTION	SPEED (ns) COM.	MIL.	POWER (mW)	PACKAGE AVAILABILITY
PIPELINE REGISTERS					
L29C520	4 x 8-bit Multilevel (1-4 Stages)	14	16	50	24-pin DIP/FP, 28-lead LCC/PLCC
L29C521	4 x 8-bit Multilevel (1-4 Stages)	14	16	50	24-pin DIP/FP, 28-lead LCC/PLCC
LPR520	4 x 16-bit Multilevel (1-4 Stages)	15	18	50	40-pin DIP, 44-lead LCC/PLCC
LPR521	4 x 16-bit Multilevel (1-4 Stages)	15	18	50	40-pin DIP, 44-lead LCC/PLCC
LPR200	8 x 16-bit Multilevel (1-8 Stages)	10	12	50	48-pin DIP, 52-lead LCC/PLCC
LPR201	7 x 16-bit Multilevel (1-7 Stages)	10	12	50	48-pin DIP, 52-lead LCC/PLCC
L29C524	14 x 8-bit Dual 7-Deep (1-14 Stages)	15	20	50	28-pin DIP/FP, 28-lead PLCC
L29C525	16 x 8-bit Dual 8-Deep (1-16 Stages)	15	20	50	28-pin DIP/FP, 28-lead PLCC
L10C11	4/8-bit Var. Length (3-18 Stages)	15	20	50	24-pin DIP, 28-lead PLCC
REGISTER FILES					
LRF07	8 x 8-bit Register File (3-Port)	20	25	50	40-pin DIP, 44-lead LCC
SHADOW REGISTERS					
L29C818	8-bit Serial Scan Shadow Register	15	24	50	24-pin DIP, 28-lead LCC

PERIPHERAL PRODUCTS

PART NO.	PRODUCT DESCRIPTION	SPEED (ns) COM.	MIL.	POWER (mW)	PACKAGE AVAILABILITY
L5380	SCSI Bus Controller	4 Mb/s	2 Mb/s	50	40-pin DIP, 44-lead LCC/PLCC
L53C80	SCSI Bus Controller	4 Mb/s	2 Mb/s	50	48-pin DIP, 44-lead LCC/PLCC

MEMORY PRODUCTS

PART NO.	PRODUCT DESCRIPTION	SPEED (ns) COM.	SPEED (ns) MIL.	POWER (mW) OPER.	POWER (mW) INACTIVE	PACKAGE AVAILABILITY
16K STATIC RAMS						
L6116	2K x 8, Common I/O + OE	12	15	250	75	24-pin DIP/SOJ, 28/32-lead LCC
64K STATIC RAMS						
L7C187	64K x 1, Separate I/O	12	15	135	75	22-pin DIP, 24-pin SOJ
L7C162	16K x 4, Separate I/O	12	15	210	75	28-pin DIP/SOJ/LCC
L7C164	16K x 4, Common I/O	12	15	210	75	22-pin DIP, 24-pin SOJ
L7C166	16K x 4, Common I/O + OE	12	15	210	75	24-pin DIP/SOJ, 28-lead LCC
L7C185	8K x 8, Common I/O	12	15	320	75	28-pin DIP/FP/SOJ, 28/32-lead LCC
256K STATIC RAMS						
L7C197	256K x 1, Separate I/O	15	20	165	100	24-pin DIP/SOJ, 28-lead LCC
L7C194	64K x 4, Common I/O	15	20	210	100	24-pin DIP/SOJ, 28-lead LCC
L7C195	64K x 4, Common I/O + OE	15	20	210	100	28-pin DIP/SOJ
L7C199	32K x 8, Common I/O + OE	15	20	490	100	28-pin DIP/FP/SOJ, 28/32-lead LCC
1M STATIC RAMS						
L7C108	128K x 8, Common I/O, 1 CE + OE	15	20	550	50	32-pin DIP/SOJ, 32-lead LCC
L7C109	128K x 8, Common I/O, 2 CE + OE	15	20	550	50	32-pin DIP/SOJ, 32-lead LCC
SPECIAL ARCHITECTURE STATIC RAMS						
L7C174	8K x 8, Cache-Tag	12	15	320	0.5	28-pin DIP/SOJ, 32-lead LCC

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DESC SMD PRODUCTS (LISTED BY LOGIC DEVICES PART NUMBER)

PART NO.	DESC SMD NUMBER	AVAILABILITY	PRODUCT DESCRIPTION
DSP PRODUCTS			
L10C23	5962-89711	Released	64 x 1 Digital Correlator
L29C101	5962-89517	Released	16-bit ALU Slice (Quad 2901)
L29C520	5962-91762	Released	4 x 8-bit Multilevel Pipeline Register
L29C521	5962-91762	Released	4 x 8-bit Multilevel Pipeline Register
L29C525	5962-91696	Released	16 x 8-bit Dual 8-Deep Pipeline Register
L29C818	5962-90515	Released	8-bit Serial Scan Shadow Register
L4C381	5962-89959	Released	16-bit Cascadable ALU
LF2250	5962-93260	Released	12 x 10-bit Matrix Multiplier
LMA1009	5962-90996	Released	12 x 12-bit Multiplier-Accumlator
LMA2009	5962-90996	Released	12 x 12-bit Multiplier-Accumlator
LMA1010	5962-88733	Released	16 x 16-bit Multiplier-Accumlator
LMA2010	5962-88733	Released	16 x 16-bit Multiplier-Accumlator
LMS12	TBA	Future	12 x 12 + 26-bit Multiplier-Summer, FIR
LMU08	5962-88739	Released	8 x 8-bit Parallel Multiplier
LMU8U	5962-88739	Released	8 x 8-bit Parallel Multiplier
LMU16	5962-86873	Released	16 x 16-bit Parallel Multiplier
LMU216	5962-86873	Released	16 x 16-bit Parallel Multiplier
LMU17	5962-87686	Released	16 x 16-bit Parallel Multiplier
LMU217	5962-87686	Released	16 x 16-bit Parallel Multiplier
LMU18	5962-94523	Released	16 x 16-bit Parallel Multiplier w/32 outputs
LPR520	5962-89716	Released	4 x 16-bit Multilevel Pipeline Register
LPR521	5962-89716	Released	4 x 16-bit Multilevel Pipeline Register
LSH32	5962-89717	Released	32-bit Barrel Shifter
PERIPHERAL PRODUCTS			
L5380	5962-90548	Released	SCSI Bus Controller
L53C80	5962-90548	Released	SCSI Bus Controller
MEMORY PRODUCTS			
L6116	5962-84036	Released	2K x 8 Static RAM
L6116	5962-89690	Released	2K x 8 Static RAM
L6116	5962-88740	Released	2K x 8 Static RAM, Low Power
L7C108	5962-89598	Released	128K x 8 Static RAM
L7C109	5962-89598	Released	128K x 8 Static RAM
L7C162	5962-89712	Released	16K x 4 Static RAM
L7C164	5962-89692	Future	16K x 4 Static RAM
L7C166	5962-89892	Future	16K x 4 Static RAM
L7C168	5962-86705	Released	4K x 4 Static RAM
L7C174	TBA	Pending	8K x 8 Static RAM, Cache-Tag
L7C185	5962-38294	Released	8K x 8 Static RAM
L7C191	5962-90664	Consult Factory	64K x 4 Static RAM
L7C192	5962-89935	Consult Factory	64K x 4 Static RAM
L7C194	5962-88681	Consult Factory	64K x 4 Static RAM
L7C197	5962-88544	Consult Factory	256K x 1 Static RAM
L7C199	5962-88552	Released	32K x 8 Static RAM, Low Power
L7C199	5962-88662	Released	32K x 8 Static RAM

DESC SMD PRODUCTS (LISTED BY SMD NUMBER)

DESC SMD NO.	LOGIC PART NO.	AVAILABILITY	PRODUCT DESCRIPTION
DSP PRODUCTS			
5962-86873	LMU16/LMU216	Released	16 x 16-bit Parallel Multiplier
5962-87686	LMU17/LMU217	Released	16 x 16-bit Parallel Multiplier
5962-88733	LMA1010/LMA2010	Released	16 x 16-bit Multiplier-Accumlator
5962-88739	LMU08/8U	Released	8 x 8-bit Parallel Multiplier
5962-89517	L29C101	Released	16-bit ALU Slice (Quad 2901)
5962-89711	L10C23	Released	64 x 1 Digital Correlator
5962-89716	LPR520/LPR521	Released	4 x 16-bit Multilevel Pipeline Register
5962-89717	LSH32	Released	32-bit Barrel Shifter
5962-89959	L4C381	Released	16-bit Cascadable ALU
5962-90515	L29C818	Released	8-bit Serial Scan Shadow Register
5962-90996	LMA1009/LMA2009	Released	12 x 12-bit Multiplier-Accumlator
5962-91696	L29C525	Released	16 x 8-bit Dual 8-Deep Pipeline Register
5962-91762	L29C520/L29C521	Released	4 x 8-bit Multilevel Pipeline Register
5962-93260	LF2250	Released	12 x 10-bit Matrix Multiplier
5962-94523	LMU18	Released	16 x 16-bit Parallel Multiplier w/32 outputs
PERIPHERAL PRODUCTS			
5962-90548	L5380/L53C80	Released	SCSI Bus Controller
MEMORY PRODUCTS			
5962-38294	L7C185	Released	8K x 8 Static RAM
5962-84036	L6116	Released	2K x 8 Static RAM
5962-86705	L7C168	Released	4K x 4 Static RAM
5962-88544	L7C197	Consult Factory	256K x 1 Static RAM
5962-88552	L7C199	Released	32K x 8 Static RAM, Low Power
5962-88662	L7C199	Released	32K x 8 Static RAM
5962-88681	L7C194	Consult Factory	64K x 4 Static RAM
5962-88740	L6116	Released	2K x 8 Static RAM, Low Power
5962-89598	L7C108/L7C109	Released	128K x 8 Static RAM
5962-89690	L6116	Released	2K x 8 Static RAM
5962-89692	L7C164	Future	16K x 4 Static RAM
5962-89712	L7C162	Released	16K x 4 Static RAM
5962-89892	L7C166	Future	16K x 4 Static RAM
5962-89935	L7C192	Consult Factory	64K x 4 Static RAM
5962-90664	L7C191	Consult Factory	64K x 4 Static RAM

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