82544GC Gigabit Ethernet Controller Datasheet and Hardware Design Guide

Application Note (AP-427)

Networking Silicon

Notice: This document contains information on products in the design phase of development. Product features and specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

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Revision History

Revision	Revision Date	Description
0.75	July 2001	**Initial publication of preliminary design guide information based upon OR-2754 (A44740-0020) and OR-2740 (A61057-001).** 1. Additions to the document include the block diagram, signal descriptions, targeted electrical and timing specifications, package and pinout information, thermal specifications and ballout information. 2. Upgraded text on the serial EEPROM. 3. Added text about integrated magnetics modules/RJ-45 connectors. 4. Added information on the IEEE Unfiltered Jitter Test, 5. Clarified Cell Type columns in ballout table to differentiate PCI cell type and I/O cell types. Changed RX_DATA [9:0], TEST, and RBC [1:0] to BI-DIR. Changed JTAG_TDO to OUT. 6. The schematic diagram changed to a dual port design, with many specific differences over the previous single port design based on the 82544EI device. 7. REF resistor changed back to 2.49K. 8. LED circuit changed to eliminate combined LINK/ACTIVITY LED. 9. New values shown for ZN_COMP, ZP_COMP, and LAN_POWER_GOOD resistors. 10. Adjustments were made to the schematic to support the IEEE Unfiltered Jitter Test. 11. Revised the JTAG circuitry to accommodate both 82544GC devices, removing the pullup resistor on JTAG_TMS. 12. New schematic uses an integrated magnetic module/RJ-45 connector with integrated LEDs.
0.76	July 2001	**Minor Changes, as follows:** 1. SWDPIO default value changed from 0DFh to DFh 2. SWDPINS default value changed from 0DEh to FFh 3. Changed document title to “Datasheet and Hardware Design Guide.”
0.77	Sept. 2001	**Change to address errata: Add TEST1 pin, pull up or tie to VCC. Change TEST to TEST0 for consistency.**
0.80	Dec 2003	Removed confidential status.

Figures

Tables

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1.0 Introduction

The 82544GC Gigabit Ethernet Controller is an integrated third-generation Ethernet LAN component capable of providing 1000, 100, and 10 Mbps data rates. It is a single-chip device, containing both the MAC and PHY layer functions, and optimized for LAN on Motherboard (LOM) designs, enterprise networking, and Internet appliances that use the Peripheral Component Interconnect (PCI) and PCI-X bus backplanes.

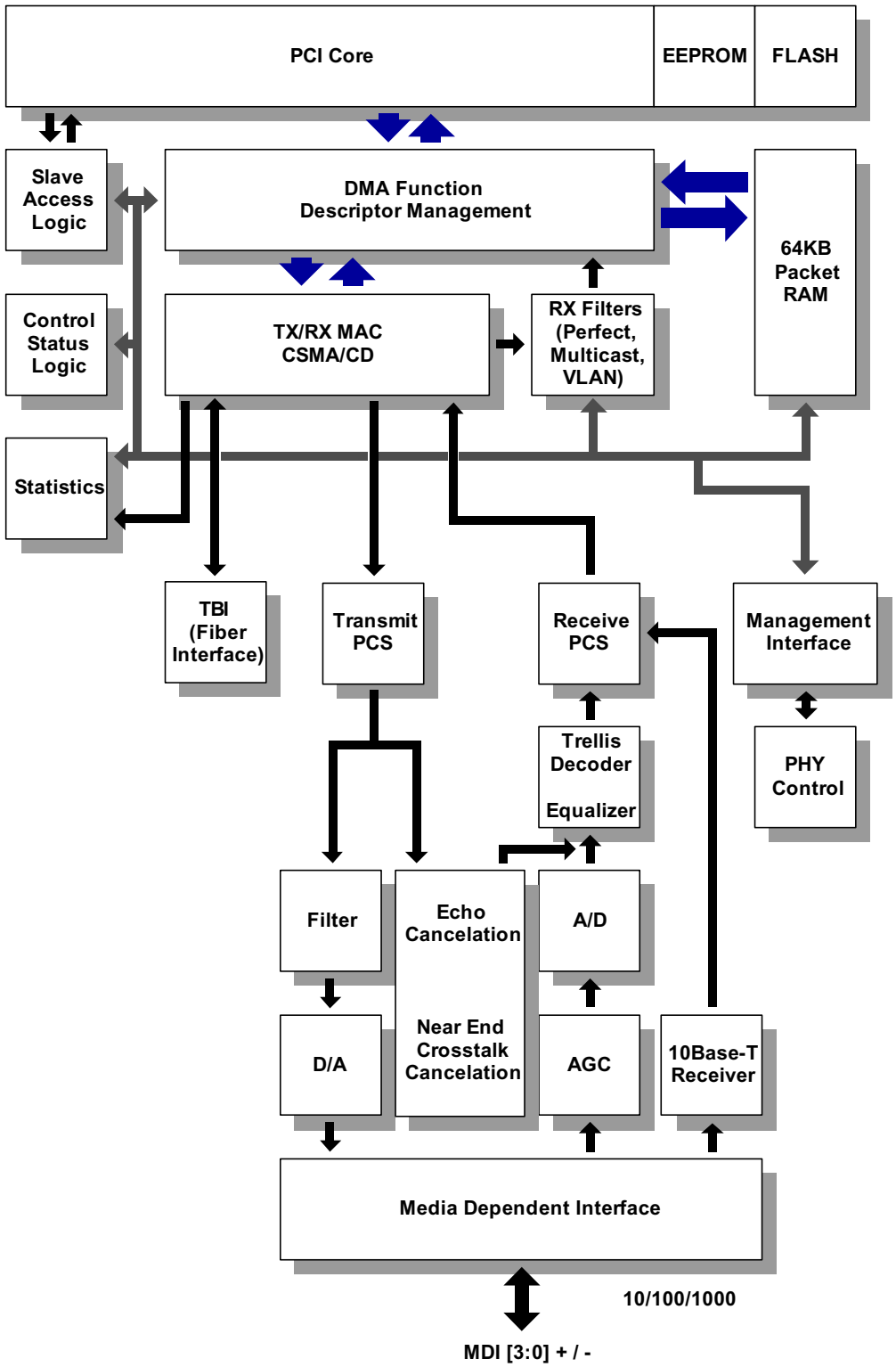
The 82544GC utilizes a 32/64 bit, 33/66 MHz direct interface to the PCI bus, compliant with the PCI Local Bus Specification, Revision 2.2. It also supports the emerging PCI-X extension to the PCI Local Bus, Revision 1.0a. The controller interfaces with the host processor through on-chip command and status registers and a shared host memory area, which is set up during initialization.

The 82544GC Gigabit Ethernet Controller provides a highly optimized architecture to deliver high performance and PCI/PCI-X bus efficiency. Its hardware, acceleration features enable offloading of various tasks, such as TCP/UDP/ IP checksum calculations and TCP segmentation, from the host processor. The 82544GC device accommodates highly-configurable Ethernet designs, which require minimal CPU overhead from interrupts and register accesses.

The physical layer circuitry provides an IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX and 10BASE-T applications. With the addition of an appropriate serializer/ deserializer (SERDES), the 82544GC controller also provides an Ethernet interface for 1000BASE-SX or 1000BASE-LX applications.

The 82544GC Gigabit Ethernet Controller is packaged in a 21mm x 21mm, 364-ball grid array.

Figure 1. Gigabit Ethernet Controller Block Diagram



1.1 Scope of this Design Guide

This application note contains Ethernet design guidelines applicable to LAN on Motherboard (LOM) designs, enterprise networking, and Internet appliances that use the PCI and PCI-X bus backplanes. These designs may use either a twisted pair copper medium or a fiber optic medium.

Section 7.0 contains a schematic showing the 82544GC device utilized in a dual 10/100/1000 Mb/s implementation.

This document also contains datasheet specifications for the 82544GC Gigabit Ethernet Controller, including signal descriptions, DC and AC parameters, packaging data, and pinout information.

1.2 Reference Documents

This application note assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- 82544EI/82544GC Gigabit Ethernet Controller Software Developer•s Manual, Revision 0.25 (reference number: OR-3000), Intel Corporation.
- PCI Local Bus Specification, Revision 2.2, PCI Special Interest Group.
- PCI-X Specification, Revision 1.0a, PCI Special Interest Group.
- PCI Bus Power Management Interface Specification, Rev. 1.1, PCI Special Interest Group.
- IEEE Standard 802.3, 1996 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3u, 1995 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3x, 1997 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3z, 1998 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3ab, 1999 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- 82559 Fast Ethernet Controllers Timing Device Selection Guide, AP-419, Intel Corporation.

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2.0 Features of the 82544GC Gigabit Ethernet Controller

2.1 PCI/PCI-X Features

32/64 bit 33/66MHz, PCI Rev 2.2 compliant host interface

Operates in either 5 V or 3.3 V PCI signaling environments

Host interface also compliant to the PCI-X addendum, revision 1.0a, from 50 to 133 MHz

64-bit addressing for systems with more than 4 GBytes of physical memory

Efficient PCI bus master operation, supported by optimized internal DMA controller

Incorporates PCI-X protocol enhancements to the PCI local bus.

Command usage optimization for advanced PCI commands such as MWI, MRM and MRL, and PCI-X commands such as MRD, MRB and MWB

2.2 MAC Specific Features

Offers both hardware and software based IEEE 802.3z Auto-Negotiation and Link Setup for Ten Bit Interface (TBI) mode

IEEE 802.3x compliant flow control support

- „ Enables control of the transmission of Pause packets through software or hardware triggering
- „ Provides indications of receive FIFO status through programming interface

Internally implements the IEEE 802.3 MII management interface for monitoring and control of the internal PHY

Offers an external link interface: Ten-Bit Interface (TBI) as specified in IEEE 802.3z standard for 1000Mbps full duplex operation with 1.25 Gbps Gigabit Ethernet Transceivers (SERDES)

2.3 PHY Specific Features

Full IEEE 802.3ab Auto-Negotiation of speed, duplex and flow control configuration

Complete full duplex and half duplex support

Next page support

Automatic MDI crossover operation for 100BASE-TX and 10BASE-T modes

Automatic polarity correction

Digital implementation of adaptive equalizer and cancellers for echo and crosstalk

2.4 Host Offloading Features

Receive and transmit IP and TCP/UDP checksum offloading capabilities

TCP segmentation (Large send)

Packet filtering based on checksum errors

Supports various address filtering modes:

- 16 exact matches (unicast or multicast)
- 4096-bit hash filter for multicast frames
- Promiscuous unicast and promiscuous multicast transfer modes

IEEE 802.1q VLAN support

- Ability to add and strip IEEE 802.1q VLAN tags
- Packet filtering based on VLAN tagging, supporting 4096 tags

SNMP and RMON statistic counters

2.5 Additional Performance Features

Provides adaptive Inter Frame Spacing (IFS) capability, enabling collision reduction in half duplex networks

Programmable host memory receive buffers (256 bytes to 16 Kbytes)

Programmable cache line size from 16 bytes to 128 bytes for efficient usage of PCI bandwidth

Implements a total of 64 Kbytes of configurable receive and transmit data FIFOs

- The default allocation is 48 Kbytes for Receive data FIFO and 16 Kbytes for transmit data FIFO.

Descriptor ring management hardware for transmit and receive

- Optimized descriptor fetching and write-back mechanisms for efficient system memory and PCI bandwidth usage

Provides a mechanism for reducing the number of interrupts generated by receive and transmit operations

Supports reception and transmission of packets with length up to 16 Kbytes

2.6 Additional Device Features

Implements enhanced ACPI register set and power-down functionality supporting D0 & D3 states and Wake on LAN capability with Power Management Event support

Provides a four-wire 64 x 16 serial EEPROM interface for loading product configuration information

Provides external parallel interface for up to 4 Mbits of Flash or Boot EPROM for boot agent capability

Provides seven general purpose user mode pins

Provides six activity and link indication outputs to directly drive LEDs

Supports little endian byte ordering for both 32 and 64 bit systems

Supports big endian byte ordering for 64 bit systems

Provides loopback capabilities

Provides boundary scan through IEEE 1149.1 (JTAG) Test Access Port

2.7 Technology Features

Implemented in 0.18∝process

Packaged in 364 TFBGA package (21mm x 21mm)

Implemented as low power CMOS device

Targeted power dissipation is 2.5 Watts maximum

Targeted operating temperature range is 0 ..55 C ambient.

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3.0 Signal Descriptions

Special Note: The targeted signal names are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

3.1 Signal Type Definitions

The signals of the 82544GC controller are electrically defined in the following fashion:

Name	Definition
I	A standard input-only digital signal.
O	A standard output-only digital signal.
TS	A bi-directional, three-state digital input/output signal.
STS	A sustained, digital, three-state signal that is driven by one owner at a time. An agent that drives an STS pin low must actively drive it high for at least one clock before letting it float. The next owner of the signal cannot start driving it any sooner than one clock after it is released by the previous owner.
OD	An open-drain digital signal. It is wired-ORed with other agents. The signaling agent asserts the signal, but the signal is returned to the inactive state by a weak pull-up resistor. The pull-up resistor may take two or three clock periods to fully restore the signal to the de-asserted state.
A	PHY analog data signal.
P	A power connection, voltage reference, or other reference connection.

3.2 PCI/PCI-X Bus Interface

When RST# is asserted, the 82544GC Gigabit Ethernet Controller will not drive any PCI output or bi-directional pins except PME#.

3.2.1 PCI Address, Data and Control Signals

Signal Name	Type	Name and Function
AD[63:0]	TS	**Address and Data.** Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[63:0] contain a physical address (64 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. The 82544GC device uses little endian byte ordering. During data phases AD[7:0] contain the least significant byte (LSB) and AD[63:56] contain the most significant byte (MSB). The 82544GC controller may be optionally connected to a 32-bit PCI Local Bus. On a 32-bit bus, AD[63:32] and other signals corresponding to the high order byte lanes do not participate in the bus cycle.
CBE[7:0]#	TS	**Bus Command and Byte Enables.** Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, CBE#[7:0] define the bus command. During the data phase CBE#[7:0] are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. CBE#[0] applies to byte 0 (LSB) and CBE#[7] applies to byte 7 (MSB).
PAR	TS	**Parity.** Parity issued to implement Even Parity across AD[31:0] and CBE#[3:0]. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted after a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. When the 82544GC controller is a bus master, it drives PAR for address and write data phases. As a slave, it drives PAR for read data phases.
PAR64	TS	**Parity 64.** Parity issued to implement Even Parity across AD[63:32] and CBE#[7:4]. PAR64 is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted after a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. When the 82544GC controller is a bus master, it drives PAR64 for address and write data phases. As a slave, it drives PAR64 for read data phases.
FRAME#	STS	**FRAME.** FRAME# is driven by the 82544GC device to indicate the beginning and duration of an access. FRAME# is asserted to indicate the beginning of a bus transaction. While FRAME# is asserted, data transfers continue. When FRAME# is asserted, the transaction is in the final data phase.
IRDY#	STS	**Initiator Ready.** IRDY# indicates the ability of the 82544GC controller (as a bus master device) to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock in which both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[63:0]. During a read, it indicates the master is ready to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82544GC controller drives IRDY# when acting as a master and samples it when acting as a slave.

Signal Name	Type	Name and Function
TRDY# S	TS	**Target Ready.** TRDY# indicates the ability of the 82544GC controller (as a selected device) to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock in which both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[63:0]. During a write, it indicates the target is ready to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82544GC device drives IRDY# when acting as a slave and samples it when acting as a master.
STOP# S	TS	**Stop.** STOP# indicates the current target is requesting the master to stop the current transaction. As a slave, the 82544GC controller drives STOP# to request the bus master to stop the transaction. As a master, the 82544GC controller receives STOP# from the slave and stops the current transaction.
IDSEL	I	**Initialization Device Select.** IDSEL is used by the 82544GC device as a chip select during configuration read and write transactions.
DEVSEL# ST	S	**Device Select.** When being actively driven by the 82544GC controller, DEVSEL# indicates to the bus master that it has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
VIO	P	**VIO.** VIO is a voltage reference for PCI interface (3.3 V or 5 V). It is used as the clamping voltage. **NOTE:** An external resistor is required between the voltage reference and the VIO balls.The targeted resistor value is 100 K .

3.2.2 Arbitration Signals

Signal Name	Type	Name and Function
REQ64# T	S	**Request Transfer.** REQ64# is generated by the current initiator to indicate its desire to perform a 64-bit transfer. REQ64# has the same timing as the FRAME# signal.
ACK64#	TS	**Acknowledge Transfer.** ACK64# is generated by the currently-addressed target in response to a REQ64# assertion by the initiator. ACK64# has the same timing as the DEVSEL# signal.
REQ#	TS	**Request Bus.** REQ# indicates to the arbiter that the 82544GC controller desires use of the bus. This is a point to point signal.
GNT#	I	**Grant Bus.** GNT# indicates to the 82544GC device that access to the bus has been granted. This is a point to point signal
LOCK#	I	**Lock Bus.** LOCK# is asserted by an initiator to require sole access to a target memory device during two or more separate transfers. The 82544GC device does not implement bus locking.

3.2.3 Interrupt Signal

Signal Name	Type	Name and Function
INTA#	TS	**Interrupt A.** The signal is used to request an interrupt by the 82544GC controller. This is an active low, level-triggered interrupt signal.

3.2.4 System Signals

Signal Name	Type	Name and Function
CLK	I	**PCI_Clock.** CLK provides timing for all transactions on the PCI bus and is an input to the 82544GC device. All other PCI signals, except RST# and INTA# lines are sampled on the rising edge of CLK. All other timing parameters are defined with respect to this edge.
M66EN	I	**66 MHz Enable.** M66EN indicates whether the system bus is enabled for 66MHz if the slot is capable of that operating frequency. This signal is ignored by the 82544GC controller, but should be connected properly for future compatibility.
RST#	I	**PCI Reset.** Most of the internal state of the 82544GC controller is reset on the de-assertion (rising edge) of RST#. Whenever RST# is asserted, all PCI output signals except PME# are floated and inputs are ignored. The PME# context is preserved, depending on power management settings.

3.2.5 Error Reporting Signals

Signal Name	Type	Name and Function
SERR#	OD	**System Error.** SERR# is used by the 82544GC controller to report address parity errors. SERR# is open drain and is actively driven for a single PCI clock when reporting the error.
PERR#	STS	**Parity Error.** PERR# is used by the 82544GC controller to report data parity errors during all PCI transactions except by a Special Cycle. PERR# is sustained tri-state and must be driven active by the 82544GC controller receive data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected.

3.2.6 Power Management Signals

Signal Name	Type	Name and Function
LAN_PWR_GOOD	I	**Power Good (Power-On Reset).** The LAN_PWR_GOOD signal indicates that good power is available for 82544GC device. When the signal is zero, the 82544GC controller will hold the entire chip in reset state and float all PCI signals.
PME#	OD	**Power Management Event.** The 82544GC device will drive this signal to zero when it receives a wakeup event and either the PME_En bit in the Power Management Control / Status Register is 1 or the Advanced Power Management Enable (APME) bit of the Wake Up Control Register (WUC) is 1.
APM_WAKEUP	O	**Advance Power Management Wakeup.** When APM Wakeup is enabled in the 82544GC controller and the 82544GC controller receives a Magic Packet* it will set this signal to a logic 1 for 50 ms.
AUX_PWR	I	**Auxiliary Power Available.** If AUX_PWR equals 1, it indicates that Auxiliary Power is available and the 82544GC device should support $D3_{cold}$ power state.
PWR_STATE[1:0]	O	**Power State.** The bits are set in the following power states: 00b = D0u, D1, or D3 state with wakeup disabled • No PHY operation is required 01b = D0u, D1, or D3 state with wakeup enabled • PHY operation is required in this state, although it may be at low speed. 11b = D0 active state • Full speed PHY operation is required. The resulting meaning of the bits is as follows: • Bit 1: asserted when normal (full power/speed) operation is required. • Bit 0: asserted when link is required. The polarity of bit 0 and 1 may be individually inverted by setting the IPS0 and IPS1 bits in the Extended Device Control Register (CTRL_EXT), respectively.

3.2.7 Impedance Compensation Signals

Signal Name	Type	Name and Function
ZN_COMP	I/O	**N Device Impedance Compensation.** Connect to an external precision resistor (to VDD) that is indicative of the PCI/PCI-X trace load. This cell is used to dynamically determine the drive strength required on the N-channel transistors in the PCI/PCI-X IO cells.
ZP_COMP	I/O	**P Device Impedance Compensation.** Connect to an external precision resistor (to VSS) that is indicative of the PCI/PCI-X trace load. This cell is used to dynamically determine the drive strength required on the P-channel transistors in the PCI/PCI-X IO cells.

3.3 Ten-Bit Interface (TBI) Signals

The TBI is a MAC interface that can connect to an external Serializer/Deserializer (SERDES) device for fiber-based designs. When the 82544GC controller is not in TBI mode, the TBI signals are in a high-impedance state.

The 82544GC device has a special GMII test mode for the IEEE Unfiltered Jitter Test. This test mode reuses the TBI signals as GMII outputs. After PHY conformance testing is completed, it is permissible to gang the TBI interface pins together to reduce the number of pulldown resistors needed.

Signal Name	Type	Name and Function
TBI_MODE	I	**TBI Mode Enable.** This signal forces the device into TBI mode when TBI_MODE is asserted (high).
TX_DATA[9:0]	O	**Transmit Data.** Parallel TBI data bus to be transmitted through a serializer/deserializer (SERDES). If TBI mode is not used, connect these pins to ground through pulldown resistors. During GMII test mode these pins become GMII outputs.
GTX_CLK	O	**Transmit Clock.** Operates at 125 MHz. If TBI mode is not used, connect this ball to ground through a pulldown resistor. During GMII test mode this pin becomes the transmit clock test output.
EWRAP O		**Enable Wrap.** EWRAP is low in normal operation. When it is high, the SERDES device is forced to transceiver loopback the serialized transmit data to the receiver. If TBI mode is not used, connect this ball to ground through a pulldown resistor.
RX_DATA[9:0]	I	**Receive Data.** Parallel TBI data bus received from a serializer/ deserializer (SERDES). If TBI mode is not used, connect these balls to ground through a pulldown resistor. During GMII test mode these pins become GMII outputs.
RBC0	I	**Receive Clock.** RBC0 is the 62.5 MHz receive clock. If TBI mode is not used, connect this ball to ground through a pulldown resistor. During GMII test mode this pin becomes an output.
RBC1	I	**Receive Clock:** RBC1 is the 62.5 MHz receive clock shifted 180 degrees from RBC0. If TBI mode is not used, connect this ball to ground through a pulldown resistor. During GMII test mode this pin becomes the receive clock test output.

3.4 EEPROM/FLASH Interface Signals

Signal Name	Type	Name and Function
EE_DI	O	**EEPROM DI.** This pin is an output to the memory device.
EE_DO	I	**EEPROM DO.** This pin is an input from the memory device. Internal pullup resistor provided.
EE_CS	O	**EEPROM CSO.** Used to enable the device.
EE_SK	O	**EEPROM Serial Clock.** The clock rate of the EEPROM interface is approximately 1 MHz.
FL_ADDR[18:0]	O	**FLASH Address Outputs.** Used to address FLASH or Boot ROM
FL_CS#	O	**FLASH Chip Select.** Used to enable FLASH or Boot ROM
FL_OE#	O	**FLASH Output Enable.** Used to enable buffers in FLASH.
FL_WE#	O	**FLASH Write Enable Output.** Used for write cycles.
FL_DATA[7:0]	TS	**FLASH Data I/O.** Bi-directional data bus for FLASH data. These signals have internal pullup devices.

3.5 Miscellaneous Signals

3.5.1 LED Signals

Signal Name	Type	Name and Function
LINK_UP#	O	**Link Up.** LINK_UP# indicates link connectivity
RX_ACTIVITY#	OD	**Receive Activity.** Flashes an LED to indicate link receive activity. This output uses an open drain cell to allow a wired-OR of activity signals.
TX_ACTIVITY#	OD	**Transmit Activity.** Flashes an LED to indicate link transmit activity. This output uses an open drain cell to allow a wired-OR of activity signals.
LINK10#	OD	**Link 10.** Drives an LED to indicate link at 10 Mbps. This output uses an open drain cell.
LINK100#	OD	**Link 100.** Drives an LED to indicate link at 100 Mbps. This output uses an open drain cell.
LINK1000#	OD	**Link 1000.** Drives an LED to indicate link at 1000 Mbps. This output uses an open drain cell.

3.5.2 Other Signals

Signal Name	Type	Name and Function
LOS	I	**Loss of Signal.** Loss of signal from the optical transceiver when TBI_MODE=1
XOFF	I	**External XOFF.** This is an external indication of the Above High Threshold for flow control.
XON	I	**External XON.** This provides an external indication of Below Low Threshold for flow control.

Signal Name	Type	Name and Function
ABV_HI	O	**Above High Threshold.** Output indicating the RX FIFO fullness is above the programmed high threshold.
BLW_LO	O	**Below Low Threshold.** Output indicating the RX FIFO fullness is below the programmed low threshold.
SDP[7:6] SDP[4:0]	TS	**S/W Defined Pins.** These pins are reserved pins which are software programmable with respect to input/output capability. These default to inputs upon power up but may have their direction and output values defined in the EEPROM. The upper four bits may be mapped to the General Purpose Interrupt bits when configured as inputs. **SPECIAL NOTE:** SDP5 is intentionally missing from the group of software-defined pins.
TEST0	I	**Factory Test Pin.** Connect this ball to ground through a pulldown resistor.
TEST1	I	Factory Test Pin. Attach an external pullup resistor to the test pin to ensure the test mode is disabled. Use a common value resistor such as 1K ohms (the value is not critical). Alternatively, the pin may be connected directly to the 3.3V supply.
GMII_TEST[1:0]	I	**GMII Test Mode Pins.** For normal operation, the test pins are connected to ground through a common pulldown resistor. For PHY Unfiltered Jitter Test, drive both pins high.
COL_TEST	O	**Collision Test Pin.** For normal operation, these pins are connected to ground through a pulldown resistor. During GMII test mode it is driving as an output.
CRS_TEST	O	**Carrier Sense Test Pin.** For normal operation, this pin is connected to ground through a pulldown resistor. It is driven as an output during GMII test mode.

3.6 PHY Signals

3.6.1 Crystal Signals

Signal Name	Type	Name and Function
XTAL1	I	**XTAL1.** 25MHz +/- 50ppm input; can be connected to an oscillator or a crystal. If a crystal is used, XTAL2 must be connected as well.
XTAL2	O	**XTAL2.** Output of internal oscillator circuit used to drive crystal into oscillation. If an external oscillator is used, XTAL2 must be disconnected.

3.6.2 Analog Signals

Signal Name	Type	Name and Function
REF	P	**Reference.** External 2.49K resistor connection to VSS.
MDI[0]+/-	A	**Media Dependent Interface[0].** 1000BASE-T: In MDI configuration, MDI[0]+/- corresponds to BI_DA+/- and in MDIX configuration MDI[0]+/- corresponds to BI_DB+/-. 100BASE-TX: In MDI configuration, MDI[0]+/- is used for the transmit pair and in MDIX configuration MDI[0]+/- is used for the receive pair. 10BASE-T: In MDI configuration, MDI[0]+/- is used for the transmit pair and in MDIX configuration MDI[0]+/- is used for the receive pair.
MDI[1]+/-	A	**Media Dependent Interface[1].** 1000BASE-T: In MDI configuration, MDI[1]+/- corresponds to BI_DB+/-, and in MDIX configuration, to the BI_DA+/-. 100BASE-TX: In MDI configuration, MDI[1]+/- is used for the receive pair, and in MDIX configuration, the transmit pair. 10BASE-T: In MDI configuration, MDI[1]+/- is used for the receive pair, and in MDIX configuration, the transmit pair.
MDI[2]+/-	A	**Media Dependent Interface[2].** 1000BASE-T: In MDI configuration, MDI[2]+/- corresponds to BI_DC+/-, and in MDIX configuration, to the BI_DD+/-. 100BASE-TX: Unused. 10BASE-T: Unused.
MDI[3]+/-	A	**Media Dependent Interface[3].** 1000BASE-T: In MDI configuration, MDI[3]+/- corresponds to BI_DD+/-, and in MDIX configuration, to the BI_DC+/-. 100BASE-TX: Unused. 10BASE-T: Unused.

3.7 Test Interface Signals

Signal Name	Type	Name and Function
JTAG_TCK	I	**JTAG Clock.** Input
JTAG_TDI	I	**JTAG TDI.** Input
JTAG_TDO	O	**JTAG TDO.** Output
JTAG_TMS	I	**JTAG TMS.** Input
JTAG_TRST#	I	**JTAG Reset.** Active low reset for JTAG. Terminate this signal through a resistor to ground. Do not leave unconnected.

3.8 Power Supply Connections

3.8.1 Digital Supplies

Signal Name	Type	Name and Function
VDDO	P	**VDDO.** 3.3 V I/O power supply.
DVDDH	P	**DVDDH.** 1.8 V Digital core power supply.
DVDDL	P	**DVDDL.** 1.5 V Digital core power supply.

3.8.2 Analog Supplies

Signal Name	Type	Name and Function
AVDDH	P	**AVDDH.** 3.3 V Analog power supply.
AVDDL	P	**AVDDL.** 2.5 V Analog power supply.

3.8.3 Ground and No Connects

Signal Name	Type	Name and Function
GND	P	**Grounds.**
NO_CONNECT	P	**No Connects.** Do not connect to these pins to any circuit. Do not use pullup or pulldown resistors.

4.0 Targeted Electrical and Timing Specifications

4.1 Targeted Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings (Referenced to VSS [Ground])[a]

Symbol	Parameter	Min	Max	Units
$V_{DD(3.3)}$	DC supply voltage on VDDD or AVDDH with respect to VSS	VSS - 0.5	4.6	V
$V_{DD(2.5)}$	DC supply voltage on AVDDL with respect to VSS	VSS - 0.5	4.6 or $V_{DD(2.5)}$ + 0.5 (whichever is less)[b]	V
$V_{DD(1.8)}$	DC supply voltage on DVDDH with respect to VSS	VSS - 0.5	4.6 or $V_{DD(2.5)}$ + 0.5 (whichever is less)[b]	V
$V_{DD(1.5)}$	DC supply voltage on DVDDL with respect to VSS	VSS - 0.5	4.6 or $V_{DD(2.5)}$ + 0.5 (whichever is less)[b]	V
V_{DD}	DC supply voltage	VSS - 0.5	4.6	V
VI / VO	LVTTL input voltage	VSS - 0.5	4.6	V
VI / VO	5 V compatible input voltage	VSS - 0.5	6.6	V
I_O	DC output current (by cell type): I_{OL} = 3 mA I_{OL} = 6 mA I_{OL} = 12 mA		 10 20 40	mA
T_{STG}	Storage temperature range	-40	125	°C
	ESD per MIL_STD-883 Test Method 3015, Specification 2001V Latchup Over/Undershoot: ±150 mA, 125 C		V_{DD} overstress: $V_{DD(3.3)}$(7.2 V)	V

a. Permanent device damage is likely to occur if the ratings in this table are exceeded. These values should not be used as the limits for normal device operations.
b. This specification applies to biasing the device to a steady state for an indefinite duration. During normal device powerup, explicit power sequencing is not required.

4.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions[a]

Symbol	Parameter	Min	Max	Units
$V_{DD(3.3)}$	DC supply voltage on VDDD or AVDDH[b]	3.0	3.6	V
$V_{DD(2.5)}$	DC supply voltage on AVDDL[c]	2.38	2.62	V
$V_{DD(1.8)}$	DC supply voltage on DVDDH[c]	1.71	1.89	V
$V_{DD(1.5)}$	DC supply voltage on DVDDL[c]	1.43	1.57	V
VIO	PCI bus voltage reference	3.0	5.25	V
t_R/t_F	Input rise/fall time (normal input)	0	200	ns

Table 2. Recommended Operating Conditions[a]

Symbol	Parameter	Min	Max	Units
t_r/t_f	Input rise/fall time (Schmitt input)	0	10	ms
T_A	Operating temperature range (ambient)	0	55	C
T_J	Junction temperature		125	C

a. For normal device operations, adhere to the limits in this table. Sustained operation of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, might result in permanent guaranteed if conditions exceed recommended operating conditions.
b. It is recommended that VDD0 = AVDDH during powerup and normal operation.
c. It is recommended that both VDDO and AVVDH are greater than AVDDL > DVDDH > DVDDL during powerup. However, voltage sequencing is not a strict requirement as long as the power supply ramp is faster than approximately 200 ms.

4.3 Targeted DC Specifications

Table 3. DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD(3.3)}$	DC supply voltage on VDDO or AVDDH		3.00	3.3	3.60	V
$V_{DD(2.5)}$	DC supply voltage on AVDDL		2.38	2.5	2.62	V
$V_{DD(1.8)}$	DC supply voltage on DVDDH		1.71	1.8	1.89	V
$V_{DD(1.5)}$	DC supply voltage on DVDDL		1.43	1.5	1.57	V

Table 4. Power Supply Characteristics … 1 (Sheet 1 of 2)

Symbol	Parameter	Condition	Min	Typ[a]	Max[b]	Units
$I_{CC(3.3)}$	3.3 V supply current	TBI mode		200	230	mA
		1000BASE-T		130	160	
		100BASE-T		90	110	
		10BASE-T		85	105	
		Powerdown[c]		85	105	
		Quiescent[d]		50	60	
$I_{CC(2.5)}$	2.5 V supply current	TBI mode		2.2	2.6	mA
		1000BASE-T		340	410	
		100BASE-T		85	105	
		10BASE-T		125	150	
		Powerdown[c]		85	105	
		Quiescent[d]		2.0	2.5	

Table 4. Power Supply Characteristics …1 (Sheet 2 of 2) (Continued)

Symbol	Parameter	Condition	Min	Typ[a]	Max[b]	Units
$I_{CC(1.8)}$	1.8 V supply current	TBI mode		170	200	mA
		1000BASE-T		300	360	
		100BASE-T		160	200	
		10BASE-T		110	135	
		Powerdown[c]		90	110	
		Quiescent[d]		15	20	
$I_{CC(1.5)}$	1.5 V supply current	TBI mode		0.4	0.5	mA
		1000BASE-T		200	240	
		100BASE-T		0.3	0.4	
		10BASE-T		0.2	0.3	
		Powerdown[c]		0.1	0.15	
		Quiescent[d]		0.1	0.15	

a. Typical conditions are T_A = 25 C, voltages are nominal. Where applicable, network traffic is moderate at full duplex and the system interface is PCI 66 MHz.
b. Maximum conditions are T_A = minimum, voltages are maximum. Where applicable, network traffic is continuous at full duplex and the system interface is PCI-X 100 to 133 MHz.
c. In the powerdown mode, the controller is in the $D3_{hot}$ state, with PME# wake-up enabled. Link is present at 100 Mbps.
d. In the quiescent mode, the controller is in the $D3_{cold}$ state, with wake-up disabled. Link is not present.

Table 5. Power Supply Characteristics …2 (Sheet 1 of 2)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	LVTTL	2.0		$V_{DD(3.3)}$	V
		5 V tolerant	2.0		5.5	
		3.3 V PCI	$0.5_{VDD(3.3)}$		$V_{DD(3.3)}$	
V_{IL}	Input low voltage	LVTTL	VSS		0.8	V
		5 V tolerant	VSS		0.8	
		3.3 V PCI	VSS		$0.3V_{DD(3.3)}$	
V_{T+}	Switching threshold: Positive edge	LVTTL & 5 V tolerant	1.2		2.4	V
V_{T+}	Switching threshold: Negative edge	LVTTL & 5 V tolerant	0.6		1.8	V
V_H	Schmitt trigger-hysteresis		0.3		1.5	V
I_{IN}	Input current	$V_{IN} = V_{DD(3.3)}$ or VSS	-10		10	µA
	Inputs with pull-down resistor (50 K)	$V_{IN} = V_{DD(3.3)}$	28		191	
	Inputs with pull-up resistor (50 K)	V_{IN} = VSS	-28		-191	

Table 5. Power Supply Characteristics … 2 (Sheet 2of 2) (Continued)

Symbol	Parameter		Condition	Min	Typ	Max	Units
I_{OL}	Output low current:						mA
	Type LVTTL	3 mA	V_{OL} = 0.4 V	3			
		6 mA		6			
		12 mA		12			
	Type: 5 V tol	3 mA		3			
		6 mA		6			
I_{OH}	Output high current						mA
	Type: LVTTL	3 mA	V_{OL} = 0.4 V	-3			
		6 mA		-6			
	Type: 5 V tol	3 mA		-2			
		6 mA		-2			
V_{OH}	Output high voltage						V
	LVTTL		I_{OH} = 0 mA	$V_{DD(3.3)}$ -0.1			
	5 V tolerant		I_{OH} = 0 mA	$V_{DD(3.3)}$ -0.2			
	3.3 V PCI		I_{OH} = -500 µA	$0.9V_{DD(3.3)}$			
V_{OL}	Output low voltage						V
	LVTTL		I_{OL} = 0 mA	0.1			
	5 V tolerant		I_{OL} = 0 mA	0.1			
	3.3 V PCI		I_{OL} = 1500 µA	$0.1V_{DD(3.3)}$			
I_{OZ}	Off-state output leakage current		V_O = V_{DD} or VSS	-10		10	µA
I_{OS}	Output short circuit current					-250	µA
C_{IN}	Input capacitance[a]		Input and bi-directional buffers		4		pF
			5 V tolerant		8		
C_{OUT}	Output capacitance[a]		Output buffers		6		pF
			5 V tolerant		10		

a. $V_{DD(3.3)}$ = 0 V; T_A = 25 C; f = 1 MHz

4.4 Targeted AC Characteristics

Table 6. AC Characteristics: 3.3 V Interfacing

Symbol	Parameter	Min	Typ	Max	Units
f_{PCICLK}	CLK frequency in PCI mode			66	MHz
	CLK frequency in PCI-X mode	66		133	

Table 7. Switching Current

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{OH(min)}$	Switching current high	$V_{OUT} = 0.3V_{CC(3.3)}$	TBD			mA
$I_{OH(max)}$	Switching current high	$V_{OUT} = 0.7V_{CC(3.3)}$			TBD	mA
$I_{OL(min)}$	Switching current low	$V_{OUT} = 0.6V_{CC(3.3)}$	TBD			mA
$I_{OL(max)}$	Switching current low	$V_{OUT} = 0.18V_{CC(3.3)}$			TBD	mA

Table 8. 25Mhz Clock Input Requirements

Symbol	Parameter[a]	Min	Typ	Max	Units
$f_{i\_TX\_CLK}$	TX_CLK_IN Frequency	25 – 50ppm	25	25 + 50ppm	MHz

a. This parameter applies to an oscillator connected to the XTAL1 input. Alternatively, a crystal may be connected to XTAL1 and XTAL 2 as the frequency source for the internal oscillator.

Table 9. Link Interface Clock Requirements

Symbol	Parameter	Min	Typ	Max	Units
f_{GTX}[a]	GTX_CLK Frequency		125		MHz

a. GTX_CLK is used externally only for test purposes.

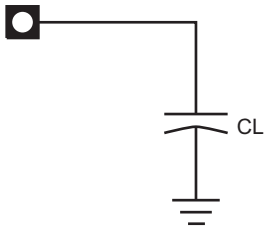
Table 10. EEPROM Interface Clock Requirements

Symbol	Parameter	Min	Typ	Max	Units
f_{SK}				1	MHz

Table 11. AC Test Loads for General Output Pins

Symbol	Signal Name	Value	Units
C_L	TDO	10	pF
C_L	EWRAP, GTX_CLK, ABV_HI, BLW_LO, PWR_STATE[1:0], APM_WAKEUP, PME#, TX_DATA,[9:0], SDP[7:0]	16	pF
C_L	FL_ADDR[18:0], FL_OE#, FL_CS#, FL_WE#, FL_DATA[7:0], EE_SK, EE_DI	18	pF
C_L	RX_ACTIVITY, TX_ACTIVITY, LINK_UP	20	pF

Figure 2. AC Test Loads for General Output Pins



4.5 Targeted Timing Specifications

Timing specifications are **preliminary** and subject to change.

4.5.1 PCI/PCI-X Bus Interface

4.5.1.1 PCI/PCI-X Bus Interface Clock

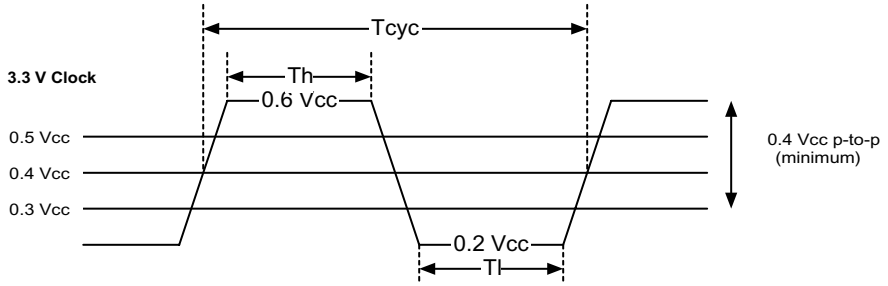
Table 12. PCI/PCI-X Bus Interface Clock Parameters

Symbol	Parameter[a]	PCI-X 133 MHz		PCI-X 66 MHz		PCI 66 MHz		PCI 33 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
T_{CYC}	CLK Cycle Time	7.5	20	15	20	15	30	30		ns	
T_H	CLK High Time	3		6		6		11		ns	
T_L	CLK Low Time	3		6		6		11		ns	
	CLK Slew Rate	1.5	4	1.5	4	1.5	4	1	4	V/ns	a
	RST# Slew Rate[b]	50		50		50		50		mV/ns	b

a. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown.

b. The minimum RST# slew rate applies only to the rising (de-assertion) edge of the reset signal, and ensures that system noise cannot render an otherwise monotonic signal to appear to bounce in the switching range.

Figure 3. PCI/PCI-X Clock Timing



4.5.1.2 PCI/PCI-X BUS Interface Timing

Table 13. PCI/PCI-X BUS Interface Timing Parameters[a, b, c]

Symbol	Parameter	PCI-X 133 MHz		PCI-X 66 MHz		PCI 66 MHz		PCI 33 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
T_{VAL}	CLK to Signal Valid Delay - bused signals	0.7	3.8	0.7	3.8	2	6	2	11	ns	a,b,c
$T_{VAL}(ptp)$	CLK to Signal Valid Delay - point-to-point signals	0.7	3.8	0.7	3.8	2	6	2	12	ns	a,b,c
T_{ON}	Float to Active Delay	0		0		2		2		ns	a
T_{OFF}	Active to Float Delay		7		7		14		28	ns	a
T_{SU}	Input Setup Time to - bused signals	1.2		1.7		3		7		ns	c
$T_{SU}(ptp)$	Input Setup Time to CLK - point-to-point signals	1.2		1.7		5		10,12		ns	c
T_{H}	Input Hold Time from CLK	0.5		0.5		0		0		ns	
T_{RRSU}	REQ64# to RST# setup time	10* T_{CYC}		10* T_{CYC}		10* T_{CYC}		10* T_{CYC}		ns	
T_{RRH}	RST# to REQ64# hold time	0		0		0		0		ns	

a. Output timing measurement as shown.
b. REQ# and GNT# are point-to-point signals, and have different output valid delay and input set up times than do bused signals. GNT# has a set up of 10; REQ# has a set up of 12. All other signals are bused
c. Input timing measurement as shown.

Figure 4. PCI Bus Interface Output Timing Measurement Conditions

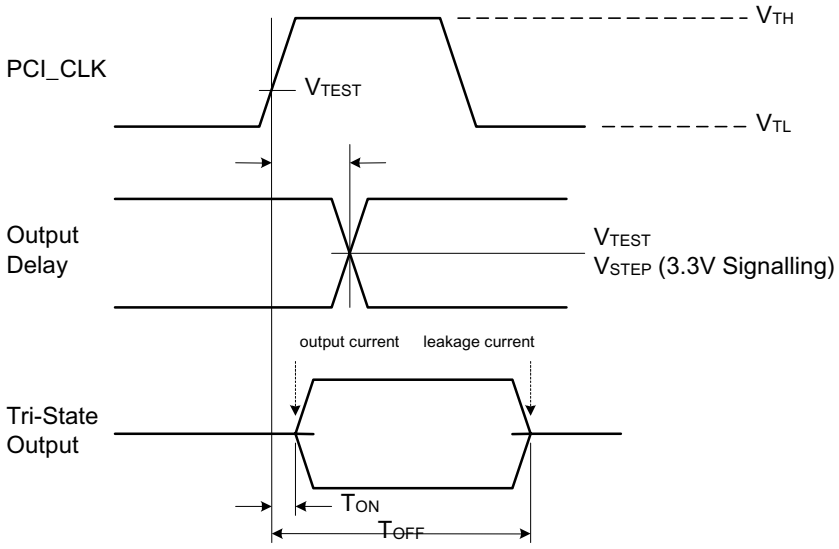


Figure 5. PCI Bus Interface Input Timing Measurement Conditions

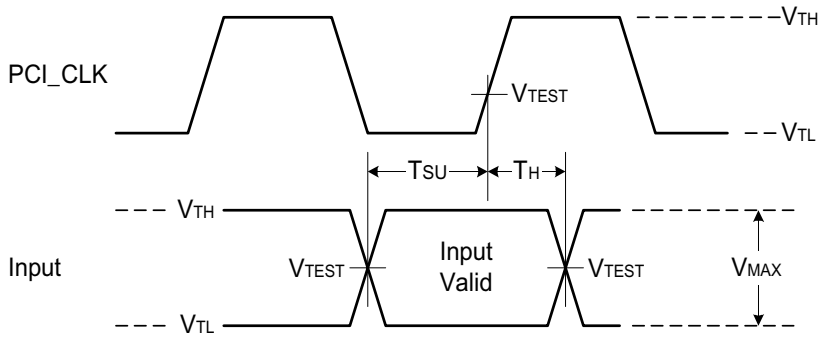


Table 14. PCI/PCI-X Bus Interface Timing Measurement Conditions

Symbol	Parameter	PCI-X	PCI 66 MHZ 3.3V	Units	Notes
V_{TH}	Input Measurement Test Voltage (high)	$0.6*V_{CC}$	$0.6*V_{CC}$	V	
V_{TL}	Input Measurement Test Voltage (low)	$0.25*V_{CC}$	$0.2*V_{CC}$	V	
V_{TEST}	Output Measurement Test Voltage	$0.4*V_{CC}$	$0.4*V_{CC}$	V	
	Input Signal Slew Rate	1.5	1.5	V / ns	

Figure 6. T_{VAL} (max) Rising Edge Test Load

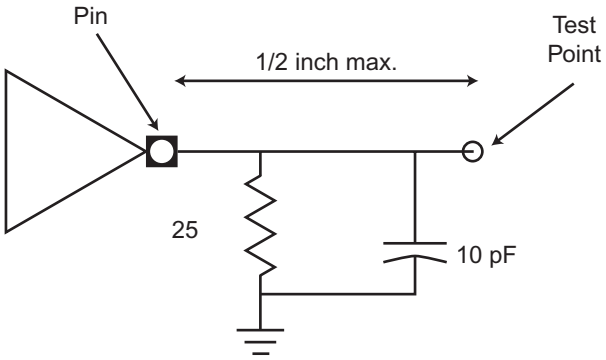


Figure 7. T_{VAL} (max) Falling Edge Test Load

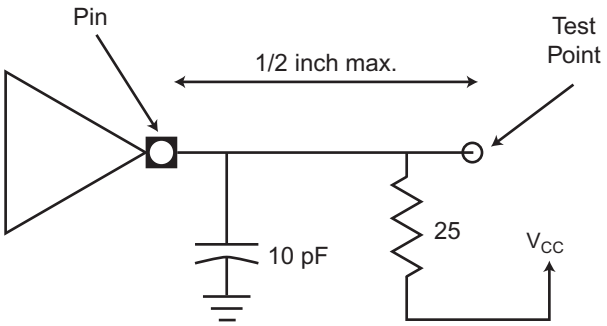


Figure 8. T_{VAL} (min) Test Load

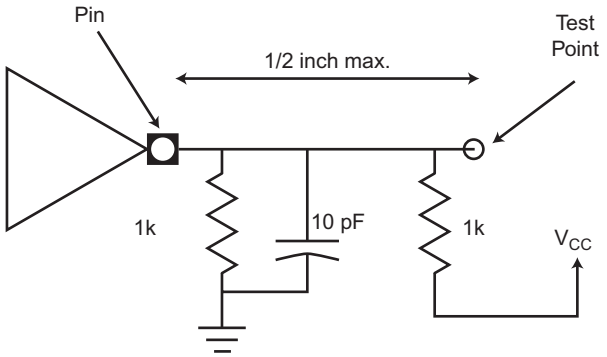
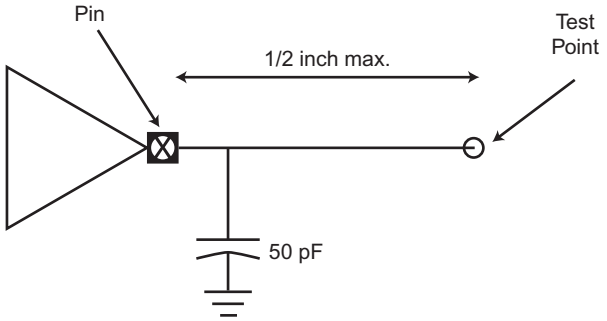
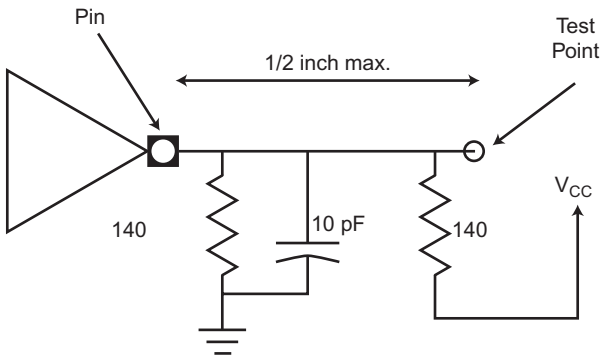


Figure 9. T_{VAL} Test Load (PCI 5V Signalling Environment)



Note: 50 pF load used for maximum times. Minimum times are specified with 0 pF load.

Figure 10. Output Slew Rate Test Load (PCI-X only)



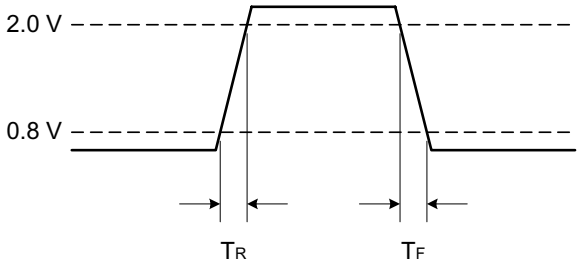
4.5.2 Targeted Link Interface Timing

4.5.2.1 Link Interface Rise and Fall Time

Table 15. Rise and Fall Time Definition

Symbol	Parameter	Condition	Min	Max	Units
T_R	Clock Rise Time	0.8V to 2.0V	0.7		ns
T_F	Clock Fall Time	2.0V to 0.8V	0.7		ns
T_R	Data Rise Time	0.8V to 2.0V	0.7		ns
T_F	Data Fall Time	2.0V to 0.8V	0.7		ns

Figure 11. Link Interface Rise/Fall Timing



4.5.2.2 Link Interface Transmit Timing

Figure 12. Transmit Interface Timing

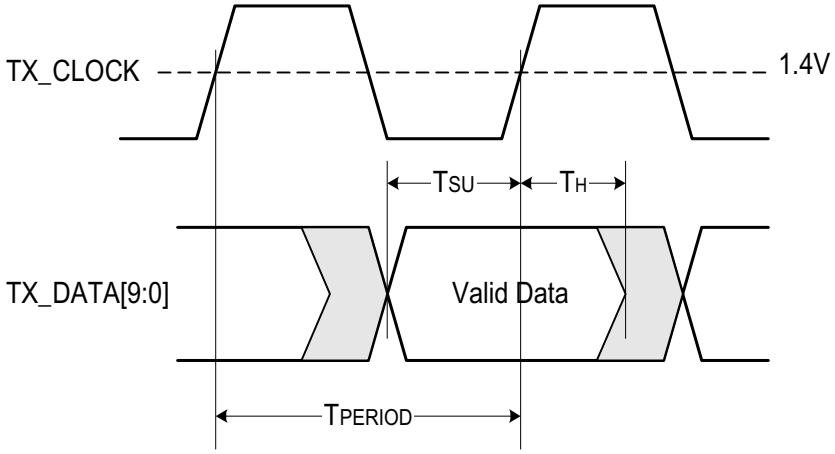


Table 16. Transmit Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{PERIOD}	GTX_CLK Period[a] TBI Mode (1000Mb/s)		8		ns
T_{SETUP}	Data Setup to Rising GTX_CLK		2.5		ns
T_{HOLD}	Data Hold from Rising GTX_CLK		1.0		ns
T_{DUTY}	GTX_CLK Duty Cycle	40		60	%

a. *±100ppm tolerance on GTX_CLK*

4.5.2.3 Link Interface Receive Interface Timing

Figure 13. Receive Interface Timing

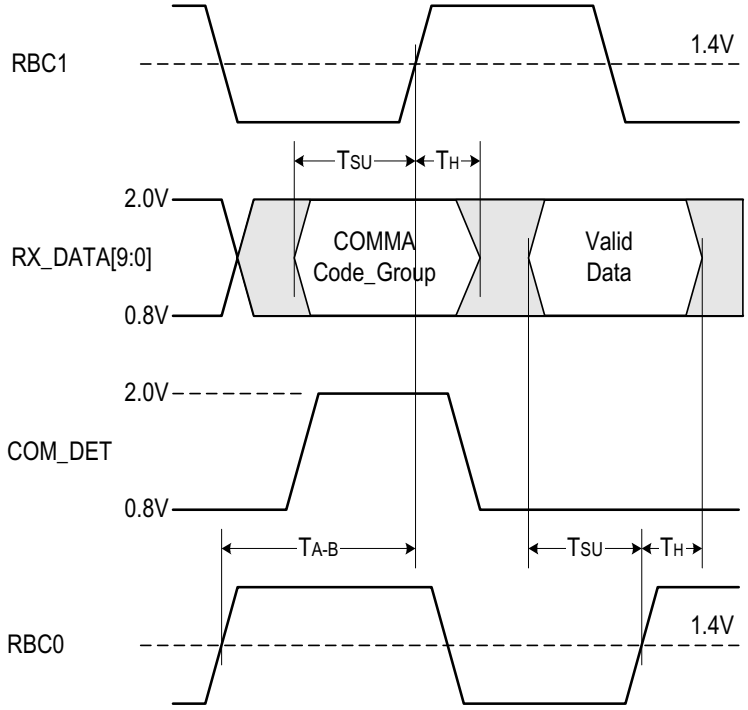


Table 17. Receive Interface Receive Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{FREQ}	RBC0/RBC1 Frequency TBI Mode (1000Mb/s)		62.5		MHz
T_{SETUP}	Data Setup before Rising RBC0 / RBC1		2.5		ns
T_{HOLD}	Data Hold after Rising RBC0 / RBC1		1		ns
T_{DUTY}	RBC0 / RBC1 Duty Cycle	40		60	%
T_{A-B}	RBC0 / RBC1 Skew	7.5		8.5	ns

4.5.3 FLASH Interface

Figure 14. Flash Read Timing

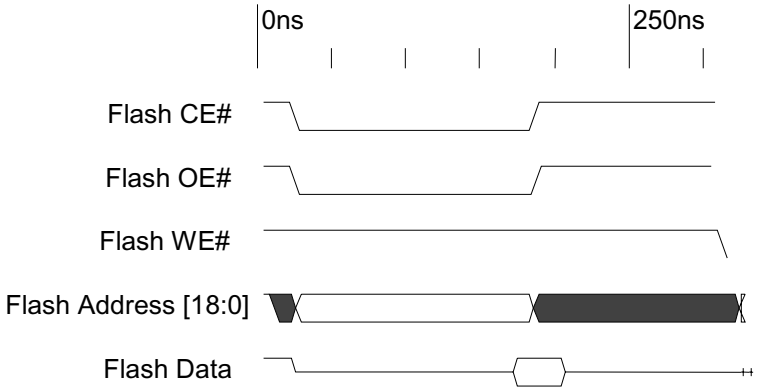


Table 18. Targeted Flash Read Operation Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{CE}	Flash CE# or OE# to Read Data Delay			160	ns
T_{ACC}	Flash Address Setup time			160	ns
T_{HOLD}	Data hold time	0			ns

Figure 15. Flash Write Timing

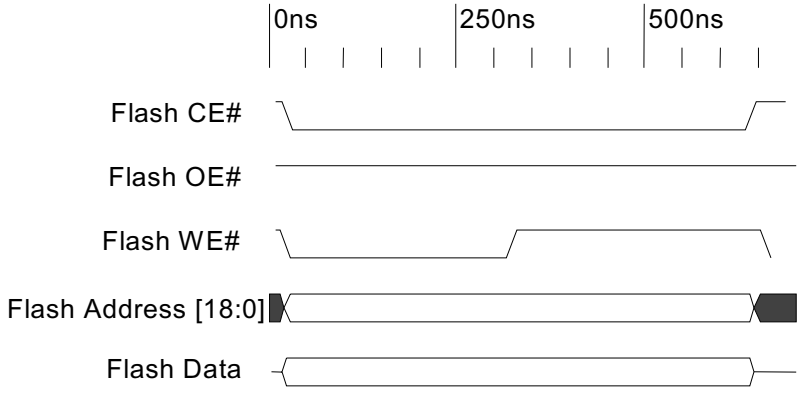


Table 19. Targeted Flash Write Operation Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{WE}	Flash Write Pulse Width (WE#)		160		ns
T_{AH}	Flash Address Hold Time	0			ns
T_{DS}	Flash Data Setup Time	160			ns

4.5.4 EEPROM Interface

Table 20. EEPROM Interface Clock Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{PW}	EE_SK Pulse width[a]		T_{PERIOD}*128		ns

a. The EE_SK EEPROM clock output is derived from GTX_CLK.

Table 21. EEPROM Interface Clock Data Timing

Symbol	Parameter[a]	Min	Typ	Max	Units
T_{DOS}	EE_DO Setup Time	T_{CYC}*2			ns
T_{DOH}	EE_DO Hold Time	0			ns

a. The EE_DO setup and hold time is a function of the CLK cycle time as indicated, but is referenced to O_EE_SK.

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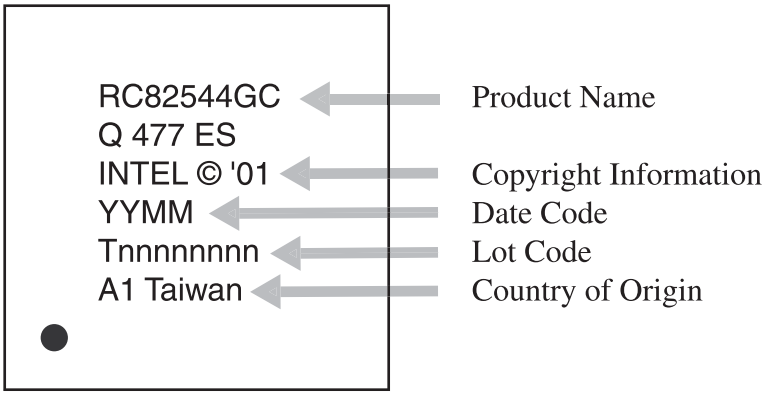
5.0 Package and Pinout Information

This section describes the 82544GC device, manufactured in a 364-lead ball grid array measuring 21x21mm. External product identification is shown in Figure 16. The nominal ball pitch is 1mm. The pin number-to-signal mapping is indicated in Table 23.

5.1 Device Identification

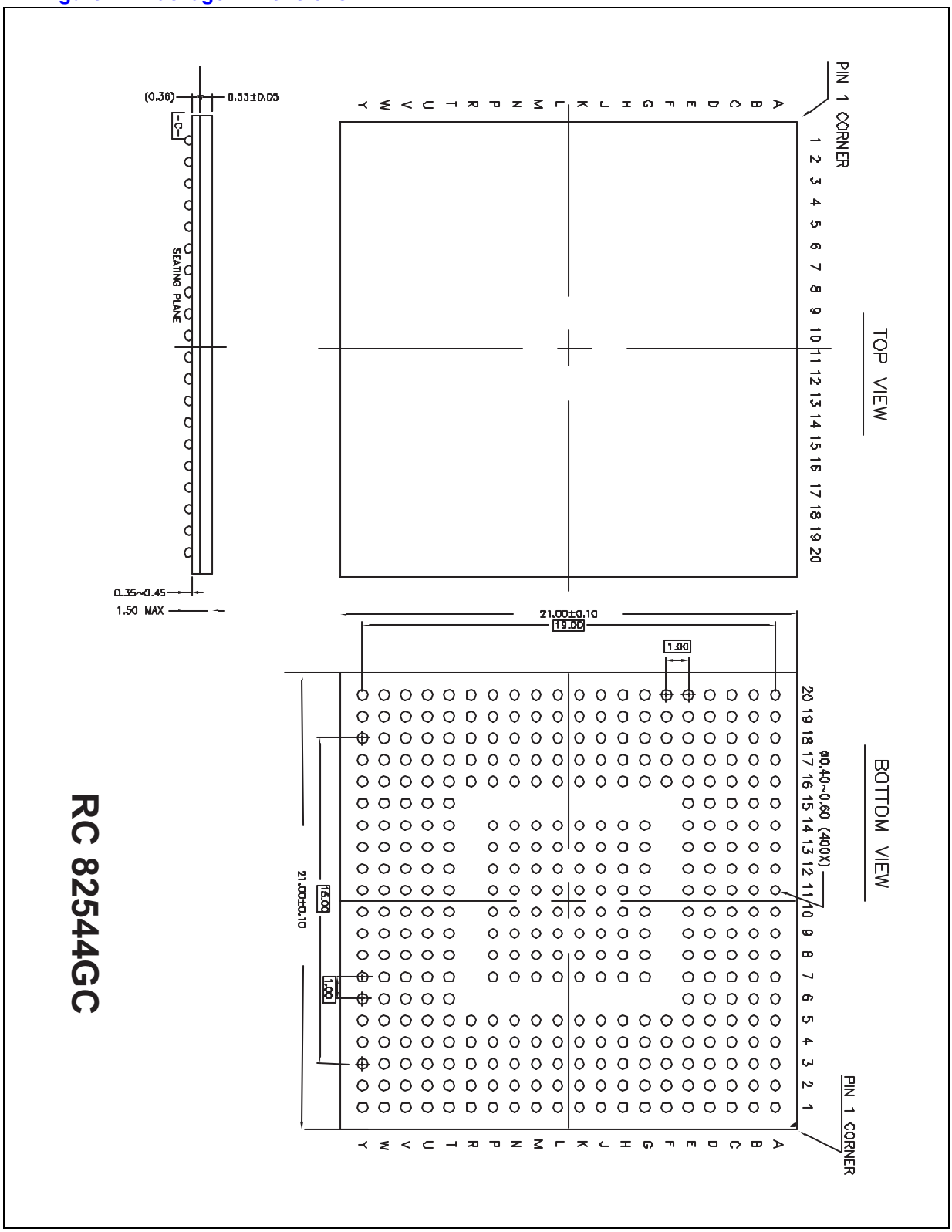
Figure 16. Device Identification:



5.2 Mechanical Specifications

The drawing on the following page indicates the complete package dimensions. The ball grid to bond-pad number mapping is shown in Figure 17.

Figure 17. Package Dimensions



5.3 Targeted Thermal Specifications

The 82544GC device is specified for operation when T_A (ambient temperature) is within the range of 0° −55° C.

T_C (case temperature) is calculated using the equation:

$T_C = T_A + P (\theta_{JA} - \theta_{JC})$

T_J (junction temperature) is calculated using the equation:

$T_J = T_A + P\ \theta_{JA}$

P (power consumption) is calculated by using the typical Icc as indicated in Table 4 and nominal Vcc. The thermal resistances are shown in Table 22.

Table 22. 82543GC Gigabit Ethernet Controller Thermal Characteristics

Symbol	Parameter	Value @ Given Airflow (m/s)			Units
		0	1	2	
θ_{JA}	Thermal Resistance, Junction-to-Ambient	19.2	17	15	° C/Watt
θ_{JC}	Thermal Resistance, Junction-to-Case	0.1	0.1	0.1	° C/Watt

Thermal resistances are determined empirically with test devices mounted on standard thermal test boards. Real system designs may have somewhat different characteristics due to board thickness, arrangement of ground planes, and proximity of other components. Use case temperature measurements to assure that the 82544GC device is operating under recommended conditions.

5.4 RC82544EI and FW82544GC Thermal Characteristics

The 82544 Gigabit Ethernet Controller with integrated PHY is available in two different packages, a PBGA 27x27mm version and a TFBGA 21x21mm version.

Product Name	Size	Package	θ_{JC}	θ_{JA} (0 m/s air flow)	Operating Temp.
RC82544EI	27x27mm	416 PBGA	0.1 °C/W	15.0 °C/W	0 – 70° C
FW82544GC	21x21mm	364 TFBGA	0.1 °C/W	19.2 °C/W	0 – 55° C

Both parts are using the same die and are spec-ed for a maximum junction temperature T_J of 120°C, where

$T_j = T_{ambient} + \theta_{JA} * P$, and $\theta_{JA} = \theta_{JC} + \theta_{CA}$

Due to its different package, the overall thermal resistance of the 82544GC is higher than the overall thermal resistance of the 82544EI. As a result, the maximum operating temp (ambient temperature T_A) for the 82544GC is lower than for the 82544EI.

5.4.1 How to Reduce the Case to Ambient Thermal Resistance, $\theta_{CA,}$ on an 82544 LOM

One element that OEMs can influence in their designs is the thermal resistance θ_{CA}. If increased airflow is not an option, the thermal resistance can be reduced by adding a heat sink to your on 82544 PCB design. The manufacturers of add-on heat sinks should provide detailed literature and technical reports on improvements in θ_{CA} with their products.

The alternative to help reduce θ_{CA} on a 82544 LOM design is build a heat sink into the printed circuit board. This is can be accomplished by adding copper to the board and drilling numerous thermal vias for heat dissipation under the BGA package.

Since all the GND balls on 82544EI/GC are clustered together and adjacent to one another, it is fairly easy for OEMs to use the following layout technique to dissipate heat using the PCB:

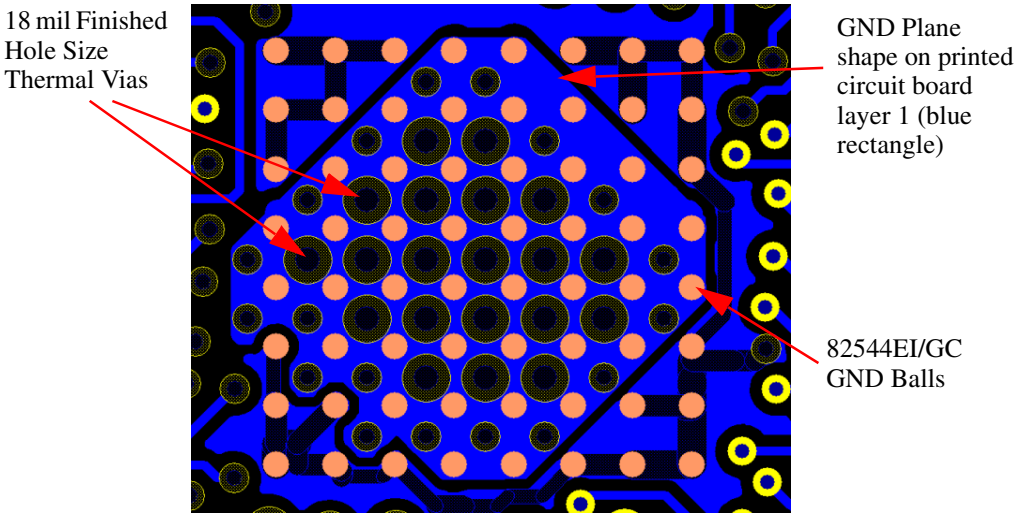


Figure 18. : The GND balls on 82544

1. On the first layer of the board, create a copper plane shape under the GND balls of the 82544GC. This will create a strong GND connection between balls and provide a large target for the thermal vias.
2. Drilling at least 4 thermal vias, which are about 14-18 mils in finished hole size, connect them to the plane shape on the first board layer and tie them to the internal ground plane. The vias should go through all board layers. The vias will act as a conduit for heat dissipation. Bury the thermal via tie legs on all plane layers to maximize heat transfer
3. Minimize any interrupted ground plane under the 82544GC BGA and within 0.5 inch of the edge of the 82544 package. Solid ground planes help to transfer the heat easily to other regions

of the PCB. Large cuts in the plane inhibit the transfer of heat which increases the case temperature of the silicon.

Figure 19. Good Ground Plane Design will Help Remove Heat from the 82544 Controller

4. On the bottom layer, add another copper plane for heat dissipation and good grounding.

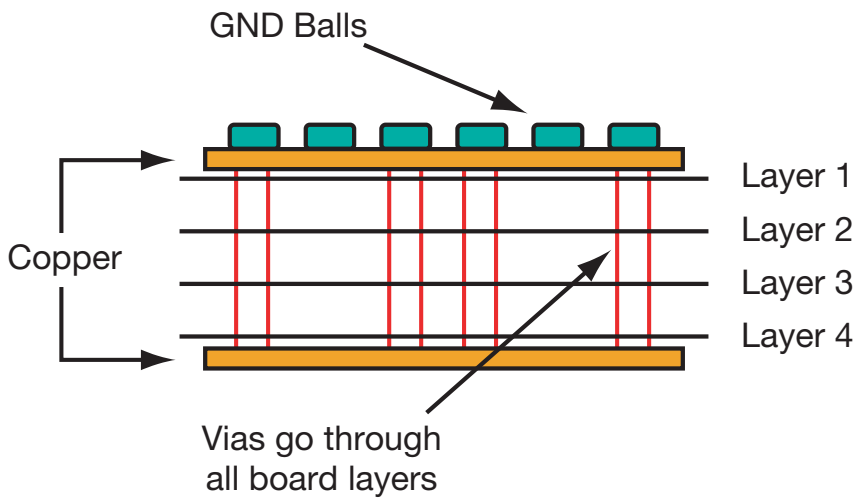


Figure 20. Recommended Layout Diagram

5.4.2 Typical Results

Following the above recommendations can dramatically reduce the case temperature of the 82544 Gigabit Ethernet Controller:

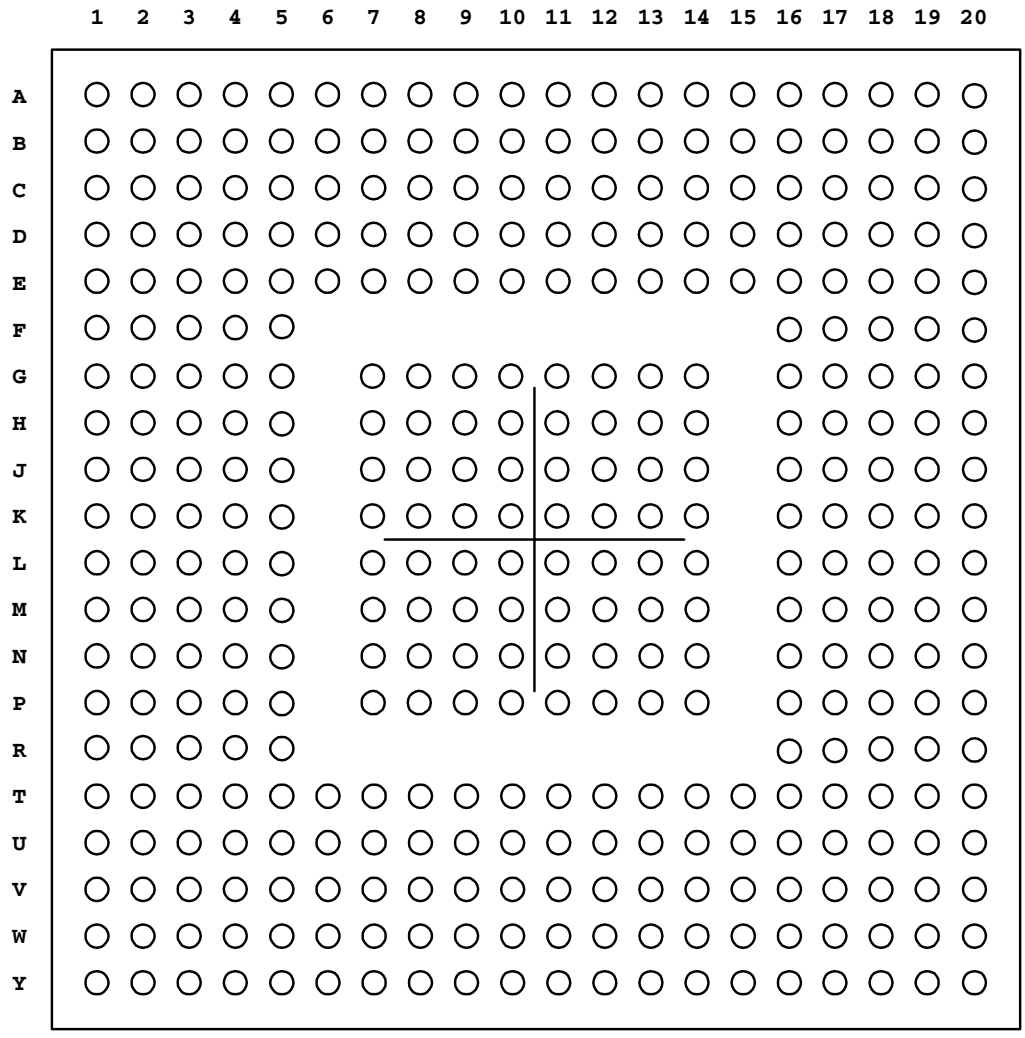
PCB Design	Effective Ground Plane Area	Case Temperature	Notes
Before Thermal Modification	5.25 Squre inch	98.9 ^{o} C	Gigabit Transmit and Receive at wire speed, ambient air temperature is 22 ^{o} C
After Thermal Modifications	15.75 Squre Inch	60.9 ^{o} C	Gigabit Transmit and Receive at wire speed, ambient air temperature is 25 ^{o} C

5.5 Targeted Ball Mapping Diagram

The figure below represents the overall targeted signal ballout map from a top view. Following the figure is a table (in two-column format) mapping the signal names to targeted ball numbers and pad cell types:

Note: The 82544GC device employs five categories of VDD connections:

- VDDO (3.3V)
- DVDDH (1.8V)
- AVDDH (Analog 3.3V)
- AVDDL (Analog 2.5V)
- DVDDL (1.5V)



5.6 Pin Number to Signal Mapping

Table 23. Pin Number to Signal Mapping

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
PCI Address, Data and Control Signals		
AD0	PCI BI-DIR	T14
AD1	PCI BI-DIR	V14
AD2	PCI BI-DIR	Y15
AD3	PCI BI-DIR	W14
AD4	PCI BI-DIR	T13
AD5	PCI BI-DIR	V13
AD6	PCI BI-DIR	Y14
AD7	PCI BI-DIR	U12
AD8	PCI BI-DIR	V12
AD9	PCI BI-DIR	T12
AD10	PCI BI-DIR	W12
AD11	PCI BI-DIR	Y12
AD12	PCI BI-DIR	V11
AD13	PCI BI-DIR	T11
AD14	PCI BI-DIR	Y11
AD15	PCI BI-DIR	W10
AD16	PCI BI-DIR	U8
AD17	PCI BI-DIR	Y7
AD18	PCI BI-DIR	Y6
AD19	PCI BI-DIR	V7
AD20	PCI BI-DIR	T7
AD21	PCI BI-DIR	W6
AD22	PCI BI-DIR	Y5
AD23	PCI BI-DIR	V6
AD24	PCI BI-DIR	U6
AD25	PCI BI-DIR	V5
AD26	PCI BI-DIR	W4
AD27	PCI BI-DIR	V4
AD28	PCI BI-DIR	Y3
AD29	PCI BI-DIR	U4
AD30	PCI BI-DIR	V3
AD31	PCI BI-DIR	V1
AD32	PCI BI-DIR	L16
AD33	PCI BI-DIR	M20
AD34	PCI BI-DIR	M19
AD35	PCI BI-DIR	M16
AD36	PCI BI-DIR	M18
AD37	PCI BI-DIR	M17
AD38	PCI BI-DIR	N20
AD39	PCI BI-DIR	N16
AD40	PCI BI-DIR	P20
AD41	PCI BI-DIR	N18
AD42	PCI BI-DIR	P19
AD43	PCI BI-DIR	P16
AD44	PCI BI-DIR	R20
AD45	PCI BI-DIR	P18
AD46	PCI BI-DIR	P17
AD47	PCI BI-DIR	T20
AD48	PCI BI-DIR	R16
AD49	PCI BI-DIR	U20
AD50	PCI BI-DIR	R18
AD51	PCI BI-DIR	T19
AD52	PCI BI-DIR	V20
AD53	PCI BI-DIR	T18
AD54	PCI BI-DIR	W20
AD55	PCI BI-DIR	V19
AD56	PCI BI-DIR	T17
AD57	PCI BI-DIR	U18
AD58	PCI BI-DIR	V18
AD59	PCI BI-DIR	U16
AD60	PCI BI-DIR	V17
AD61	PCI BI-DIR	W18
AD62	PCI BI-DIR	Y19
AD63	PCI BI-DIR	T16
CBE0#	PCI BI-DIR	Y13
CBE1#	PCI BI-DIR	V10
CBE2#	PCI BI-DIR	T8
CBE3#	PCI BI-DIR	Y4
CBE4#	PCI BI-DIR	V16

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
CBE5#	PCI BI-DIR	Y18
CBE6#	PCI BI-DIR	Y17
CBE7#	PCI BI-DIR	T15
PAR	PCI BI-DIR	U10
PAR64	PCI BI-DIR	V15
FRAME#	PCI BI-DIR	V8
IRDY#	PCI BI-DIR	W8
TRDY#	PCI BI-DIR	Y8
STOP#	PCI BI-DIR	V9
IDSEL	PCI BI-DIR	T6
DEVSEL#	PCI BI-DIR	T9
VIO	POWER	Y1
VIO	POWER	Y20
Arbitration Signals		
REQ64#	PCI BI-DIR	U14
ACK64#	PCI BI-DIR	W16
REQ#	PCI BI-DIR	W2
GNT#	PCI BI-DIR	T3
LOCK#	PCI BI-DIR	Y9
Interrupt Signal		
INTA#	BI-DIR	Y2
System Signals		
CLK	PCI IN	U2
M66EN	PCI IN	Y16
RST#	PCI IN	T5
Error Reporting Signals		
SERR#	PCI BI-DIR	T10
PERR#	PCI BI-DIR	Y10
Power Management Signals		
LAN_PWR_GOOD	IN	A17
PME#	OPEN DRAIN	T4
APM_WAKEUP	BI-DIR	L20
AUX_PWR	PCI IN	R3
PWR_STATE1	BI-DIR	R1
PWR_STATE0	BI-DIR	T1
Impedance Compensation Signals		
ZN_COMP	IN	T2
ZP_COMP	IN	R5

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
TBI Interface Signals		
TBI_MODE	IN	A16
TX_DATA0	BI-DIR	D4
TX_DATA1	BI-DIR	D5
TX_DATA2	BI-DIR	C4
TX_DATA3	BI-DIR	E4
TX_DATA4	BI-DIR	C5
TX_DATA5	BI-DIR	E5
TX_DATA6	BI-DIR	B5
TX_DATA7	BI-DIR	E6
TX_DATA8	BI-DIR	D7
TX_DATA9	BI-DIR	C7
GTX_CLK	BI-DIR	C6
EWRAP	BI-DIR	E10
RX_DATA0	BI-DIR	B7
RX_DATA1	BI-DIR	A7
RX_DATA2	BI-DIR	C8
RX_DATA3	BI-DIR	E8
RX_DATA4	BI-DIR	E9
RX_DATA5	BI-DIR	D9
RX_DATA6	BI-DIR	C9
RX_DATA7	BI-DIR	B9
RX_DATA8	BI-DIR	D10
RX_DATA9	BI-DIR	A9
RBC0	BI-DIR	C11
RBC1	BI-DIR	B10
EEPROM/FLASH Interface Signals		
EE_DI	BI-DIR	C19
EE_DO	IN	B20
EE_CS	BI-DIR	C20
EE_SK	BI-DIR	D20
FL_ADDR0	BI-DIR	J20
FL_ADDR1	BI-DIR	G20
FL_ADDR2	BI-DIR	H20
FL_ADDR3	BI-DIR	H16
FL_ADDR4	BI-DIR	G19
FL_ADDR5	BI-DIR	G18
FL_ADDR6	BI-DIR	H18

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
FL_ADDR7	BI-DIR	E20
FL_ADDR8	BI-DIR	F20
FL_ADDR9	BI-DIR	F18
FL_ADDR10	BI-DIR	J18
FL_ADDR11	BI-DIR	F19
FL_ADDR12	BI-DIR	F17
FL_ADDR13	BI-DIR	F16
FL_ADDR14	BI-DIR	D19
FL_ADDR15	BI-DIR	E16
FL_ADDR16	BI-DIR	G17
FL_ADDR17	BI-DIR	D17
FL_ADDR18	BI-DIR	D18
FL_CS#	BI-DIR	J19
FL_OE#	BI-DIR	G16
FL_WE#	BI-DIR	E18
FL_DATA0	BI-DIR	K17
FL_DATA1	BI-DIR	K19
FL_DATA2	BI-DIR	K20
FL_DATA3	BI-DIR	L18
FL_DATA4	BI-DIR	K18
FL_DATA5	BI-DIR	K16
FL_DATA6	BI-DIR	J16
FL_DATA7	BI-DIR	J17
LED Signals		
LINK_UP#	BI-DIR	M1
RX_ACTIVITY#	BI-DIR	N1
TX_ACTIVITY#	BI-DIR	N2
LINK10#	BI-DIR	M3
LINK100#	BI-DIR	N4
LINK1000#	BI-DIR	N3
Other Signals		
LOS	IN	A10
XOFF	IN	A20
XON	IN	B18
ABV_HI	BI-DIR	C17
BLW_LO	BI-DIR	A18
SDP0	BI-DIR	G4
SDP1	BI-DIR	G5

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
SDP2	BI-DIR	H5
SDP3	BI-DIR	J1
SDP4	BI-DIR	J4
SDP6	BI-DIR	J3
SDP7	BI-DIR	J2
TEST0	IN	E11
TEST1	IN	L3
GMII_TEST0	IN	K4
GMII_TEST1	IN	K5
COL_TEST	OUT	E7
CRS_TEST	OUT	A6
PHY Signals		
XTAL1	IN	A3
XTAL2	OUT	A4
REF	IN	E3
MDI[0]-	BI-DIR	B1
MDI[0]+	BI-DIR	B2
MDI[1]-	BI-DIR	C1
MDI[1]+	BI-DIR	C2
MDI[2]-	BI-DIR	D1
MDI[2]+	BI-DIR	D2
MDI[3]-	BI-DIR	E1
MDI[3]+	BI-DIR	E2
Test Interface Signals		
JTAG_TCK	IN	P1
JTAG_TDI	IN	P4
JTAG_TDO	OUT	P2
JTAG_TMS	IN	P5
JTAG_TRST#	IN	N5
Digital Power Supplies		
VDDO	3.3V POWER	B8
VDDO	3.3V POWER	B14
VDDO	3.3V POWER	B19
VDDO	3.3V POWER	C10
VDDO	3.3V POWER	D6
VDDO	3.3V POWER	D11
VDDO	3.3V POWER	E17
VDDO	3.3V POWER	H4

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
VDDO	3.3V POWER	H19
VDDO	3.3V POWER	L17
VDDO	3.3V POWER	M2
VDDO	3.3V POWER	N19
VDDO	3.3V POWER	R4
VDDO	3.3V POWER	R17
VDDO	3.3V POWER	U1
VDDO	3.3V POWER	U3
VDDO	3.3V POWER	U7
VDDO	3.3V POWER	U11
VDDO	3.3V POWER	U15
VDDO	3.3V POWER	U19
VDDO	3.3V POWER	W5
VDDO	3.3V POWER	W9
VDDO	3.3V POWER	W13
VDDO	3.3V POWER	W17
DVDDH	1.8V POWER	G7
DVDDH	1.8V POWER	G8
DVDDH	1.8V POWER	G9
DVDDH	1.8V POWER	G12
DVDDH	1.8V POWER	G13
DVDDH	1.8V POWER	G14
DVDDH	1.8V POWER	H7
DVDDH	1.8V POWER	H8
DVDDH	1.8V POWER	H13
DVDDH	1.8V POWER	H14
DVDDH	1.8V POWER	J7
DVDDH	1.8V POWER	J14
DVDDH	1.8V POWER	M7
DVDDH	1.8V POWER	M14
DVDDH	1.8V POWER	N7
DVDDH	1.8V POWER	N8
DVDDH	1.8V POWER	N13
DVDDH	1.8V POWER	N14
DVDDH	1.8V POWER	P7
DVDDH	1.8V POWER	P8
DVDDH	1.8V POWER	P9
DVDDH	1.8V POWER	P12

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
DVDDH	1.8V POWER	P13
DVDDH	1.8V POWER	P14
DVDDL	1.5V POWER	A8
DVDDL	1.5V POWER	A11
DVDDL	1.5V POWER	A12
DVDDL	1.5V POWER	H1
Analog Power Supplies		
AVDDH	3.3V POWER	B4
AVDDH	3.3V POWER	C16
AVDDH	3.3V POWER	F1
AVDDH	3.3V POWER	W1
AVDDL	2.5V POWER	A19
AVDDL	2.5V POWER	G1
AVDDL	2.5V POWER	G2
AVDDL	2.5V POWER	G3
Grounds and No Connects		
GND	POWER	A1
GND	POWER	A2
GND	POWER	A5
GND	POWER	B3
GND	POWER	B6
GND	POWER	B11
GND	POWER	B17
GND	POWER	C3
GND	POWER	D3
GND	POWER	D8
GND	POWER	D14
GND	POWER	E19
GND	POWER	F3
GND	POWER	G10
GND	POWER	G11
GND	POWER	H2
GND	POWER	H9
GND	POWER	H10
GND	POWER	H11
GND	POWER	H12
GND	POWER	H17
GND	POWER	J8

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
GND	POWER	J9
GND	POWER	J10
GND	POWER	J11
GND	POWER	J12
GND	POWER	J13
GND	POWER	K1
GND	POWER	K2
GND	POWER	K7
GND	POWER	K8
GND	POWER	K9
GND	POWER	K10
GND	POWER	K11
GND	POWER	K12
GND	POWER	K13
GND	POWER	K14
GND	POWER	L2
GND	POWER	L7
GND	POWER	L8
GND	POWER	L9
GND	POWER	L10
GND	POWER	L11
GND	POWER	L12
GND	POWER	L13
GND	POWER	L14
GND	POWER	L19
GND	POWER	M4
GND	POWER	M5
GND	POWER	M8
GND	POWER	M9
GND	POWER	M10
GND	POWER	M11
GND	POWER	M12
GND	POWER	M13
GND	POWER	N9
GND	POWER	N10
GND	POWER	N11
GND	POWER	N12
GND	POWER	N17

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
GND	POWER	P10
GND	POWER	P11
GND	POWER	R2
GND	POWER	R19
GND	POWER	U5
GND	POWER	U9
GND	POWER	U13
GND	POWER	U17
GND	POWER	V2
GND	POWER	W3
GND	POWER	W7
GND	POWER	W11
GND	POWER	W15
GND	POWER	W19
NO_CONNECT		A13
NO_CONNECT		A14
NO_CONNECT		A15
NO_CONNECT		B12
NO_CONNECT		B13
NO_CONNECT		B15
NO_CONNECT		B16
NO_CONNECT		C12
NO_CONNECT		C13
NO_CONNECT		C14
NO_CONNECT		C15
NO_CONNECT		C18
NO_CONNECT		D12
NO_CONNECT		D13
NO_CONNECT		D15
NO_CONNECT		D16
NO_CONNECT		E12
NO_CONNECT		E13
NO_CONNECT		E14
NO_CONNECT		E15
NO_CONNECT		F2
NO_CONNECT		F4
NO_CONNECT		F5
NO_CONNECT		H3

Signal Name	Cell Type (IN/OUT/BI-DIR)	Ball #
NO_CONNECT		J5
NO_CONNECT		K3
NO-CONNECT		L1
NO_CONNECT		L4
NO_CONNECT		L5
NO_CONNECT		P3

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6.0 Designing with the 82544GC Gigabit Ethernet Controller

Note: Product features, signal names and targeted specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

6.1 PCI/PCI-X Interface

The 82544GC controller provides an interface to the 32/64 bit, 33/66 MHz PCI bus. In addition, the device supports the new PCI-X extension. PCI-X specifies an enhanced protocol and data transfers over the 32/64 bit bus at speeds up to 133 MHz.

6.1.1 Operation as PCI Master and Slave

The 82544GC controller operates as a PCI slave device for configuration and register programming. Once the device has been properly initialized, it will also operate as a PCI master. The 82544GC controller accesses memory directly to fetch memory descriptors, to read transmit data and to write receive data.

6.1.2 PCI Signaling Environment

The 82544GC Gigabit Ethernet Controller operates in either a 5V or 3.3V PCI signaling environment. Connect the device's VIO terminals to either 5V or 3.3V to choose the appropriate level for the PCI/PCI-X bus. These connections will bias the 82544GC PCI I/O buffers for the correct switching strength. However, all other digital inputs and outputs use 3.3V signaling unless specified separately.

6.2 Design and Layout Considerations for All 82544GC Controller Circuits

This section describes circuits and connections that are common to all 82544GC-based designs, regardless of whether they employ an optical fiber or twisted-pair transmission medium.

Critical signal traces should be kept as short as possible to decrease the likelihood of being affected by high frequency noise from other signals, including noise carried on power and ground planes. Keeping the traces as short as possible can also reduce capacitive loading.

6.2.1 Routing the 82544GC Gigabit Ethernet Controller PCI/PCI-X Local Bus

For guidelines on connecting the PCI/PCI-X bus on the 82544GC controller, consult the PCI Local Bus Specification and the PCI-X Specification. Due to the higher bus speed, the PCI-X specification has more stringent requirements on the number of devices that can be placed on the bus. In addition, PCI-X specification calls for more tightly controlled board impedance for add-on cards.

6.2.2 Serial EEPROM

The 82544GC controller uses a 64 register by 16-bit serial EEPROM device for storing product configuration information. Several words of the EEPROM are accessed automatically by the device after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the stored information is available to software for storing the MAC address, serial numbers, and additional configuration information.[1]

Intel has an MS-DOS* software utility called EEUPDATE, which can be used to program EEPROM images in development or production line environments. To obtain a copy of this program, contact your Intel representative.

The EEPROM access algorithm programmed into the 82544GC controller is compatible with most, but not all, commercially available 3.3V Microwire* interface, serial EEPROM devices, with a 64 x 16 organization and a 1 MHz speed rating. The 82544GC's EEPROM access algorithm drives extra pulses on the shift clock at the beginnings and ends of read and write cycles. The extra pulses may violate the timing specifications of some EEPROM devices. In selecting a serial EEPROM, choose a device that specifies "don't care" shift clock states between accesses.

EEPROMs that have been found to work satisfactorily with the 82544GC controller are listed in the following table:

Table 24. EEPROM Manufacturers

Manufacturer	Manufacturer's Part Number
Atmel	AT93C46
Catalyst	CAT93C46
ST Microelectronics	M93C46

The EEPROM interface trace routing is not critical because the interface runs at a very slow speed.

6.2.3 EEPROM Address Map

The following table is the EEPROM address map for the 82544GC Gigabit Ethernet Controller. Each of the data words will be described in subsequent sections.

Table 25. EEPROM Address Map

Word Address	HW Access	Description (Hi Byte)	Description (Low Byte)	Default Image Value (hex)
0	Yes	IA Byte 2	IA Byte 1	IA(2,1)
1	Yes	IA Byte 4	IA Byte 3	IA(4,3)
2	Yes	IA Byte 6	IA Byte 5	IA(6,5)
3	No	Compatibility high	Compatibility low	0000
4-7	No	Reserved	Reserved	0000
8	No	PBA, byte 1	PBA, byte 2	TBD
9	No	PBA, byte 3	PBA, byte 4	TBD

1. An EEPROM may not be required in all applications.

Table 25. EEPROM Address Map (Continued)

Word Address	HW Access	Description (Hi Byte)	Description (Low Byte)	Default Image Value (hex)
A	Yes	Init Control 1, high byte	Init Control 1, low byte	See Text
B	Yes	Subsystem_ID, high byte	Subsystem_ID, low byte	1008
C	Yes	Subsystem_Vendor, high byte	Subsystem_Vendor, low byte	8086
D	Yes	Device ID, high	Device ID, low	1008
E	Yes	Vendor ID, high	Vendor ID, low	8086
F	Yes	Init Control 2, high byte	Init Control 2, low byte	See Text
10-1F	No	OEM Rsvd	OEM Rsvd	0000
20	Yes	Software Defined Pins Control, high byte	Software Defined Pins Control, low byte	See Text
21	Yes	Circuit Control, high	Circuit Control, low	0011
22	Yes	D0 Power	D3 Power	See Text
23-3E	No	RESERVED	RESERVED	0000
30-32	No	PXE Configuration	PXE Configuration	0000
33-3E	Fixed	Reserved	Reserved	0000
3F	No	Checksum, high byte	Checksum, low byte	Checksum of words 0-3E

6.2.3.1 Example EEPROM Image Files

Figure 21 is a typical EEPROM file for an Intel® PRO/1000 XT Gigabit Ethernet Adapter (Copper).

Figure 21. Typical Intel® PRO/1000 XT Gigabit Ethernet Adapter (Copper) EEPROM File

0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0200	00B3	0040	0000	0000	0000	0000	0000
A515	8007	660A	1107	8086	1008	8086	F26C
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	0011	3711	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	XXXX

Figure 22 is a typical EEPROM file for an Intel® PRO/1000 XF Gigabit Ethernet Adapter (Fiber).

Figure 22. Typical Intel® PRO/1000 XF Gigabit Ethernet Adapter (Fiber) EEPROM File

0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0200	00B3	0040	0000	0000	0000	0000	0000
A504	8402	6C0B	1109	8086	1009	8086	B86C
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	0011	2414	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	XXXX

6.2.3.2 Ethernet Address (Words 0x00-0x02)

The Ethernet Individual Address (IA) is a 6 byte field that must be unique for each Ethernet port (and unique for each copy of the EEPROM image). The first three bytes are vendor specific. The value from this field is loaded into the *Receive Address Register 0* (RAL0/RAH0).

6.2.3.3 Compatibility Fields (Word 0x03)

Two words in the EEPROM image are reserved for compatibility information to be used by software drivers. Typical values are 0000H for a fiber-based design and 0400H for a copper-based design.

6.2.3.4 PBA Number (Word 0x08h, 0x09)

A nine-digit PBA (printed board assembly) number used for Intel manufactured adapter cards will be stored in a four byte field. Other hardware manufacturers may use these fields as they wish. Network driver software should not rely on this field to identify the product or its capabilities.

6.2.3.5 Initialization Control Word 1 (Word 0x0A)

The first word read by the 82544GC controller contains initialization values which:

- Sets defaults for some internal registers
- Enable/disable specific features

- Determine which PCI configuration space values will be loaded from the EEPROM

Table 26. Initialization Control Word 1 (Word 0x0A)

Bit	Name	Description
15:14	Signature	The Signature field is a signature of 01b, indicating to the device that there is a valid EEPROM present. If the Signature field is not 01b, the other bits in this word are ignored, no further EEPROM read is performed, and default values are used for the configuration space IDs.
13	64/32 BAR	When asserted, the base address register is configured to indicate the device is mapable in the 32-bit space. Default is 64-bit memory mapping.
12	IPS0	Default setting for the Power State output invert bit 0 (CTRL_EXT[14]). The hardware default value is 0.
11	FRCSPD	Default setting for the Force Speed bit in the Device Control register (CTRL[11]). Hardware default value is 1. 10/100/1000 Mb/s systems will typically use a setting of 0.
10	FD	Default setting for duplex setting. Mapped to CTRL[0] & TXCW[5]. The hardware default value is 1.
9	LRST	Default setting for link reset. Mapped to CTRL[3]. When 0 hardware will initiate Auto-Negotiation upon power up or assertion of RST# without driver intervention. The hardware default is value 1.
8	IPS1	Default setting for the Power State Output invert bit 1 (CTRL_EXT[16]). The hardware default value is 0.
7:5	Reserved	Reserved for future use.
4	ILOS	Default setting for the Loss-of-signal polarity setting for CTRL[7]. The hardware default value is 0.
3	Power Management	0 = The Power Management Registers set is read only, and the 82544GC controller will not execute a hardware transition to D3. 1 = Full support for power management
2	PME Clock	Loaded into the PME_Clock bit of the Power Managment Capabilities Register (PMC).
1	Load Subsystem Ids	This bit, when equal to 1, indicates that the device is to load its PCI Subsystem ID and Subsystem Vendor ID from the EEPROM (words 0x0B, 0x0C).
0	Load Vendor/Device Ids	This bit, when equal to 1, indicates that the device is to load its PCI Vendor and Device IDs from the EEPROM (words 0x0D, 0x0E).

6.2.3.6 Subsystem ID (Word 0x0B)

If the signature bits (15:14) and bit 1 (Load Subsystem IDs) of word 0x0A are valid, this word will be read in to initialize the Subsystem ID.

6.2.3.7 Subsystem Vendor ID (Word 0x0C)

If the signature bits (15:14) and bit 1 (Load Subsystem IDs) of word 0x0A are valid, this word will be read in to initialize the Subsystem Vendor ID.

6.2.3.8 Device ID (Word 0x0D)

If the signature bits (15:14) and bit 0 (Load Vendor/Device IDs) of word 0x0A are valid, this word will be read in to initialize the Device ID.

6.2.3.9 Vendor ID (Word 0x0E)

If the signature bits (15:14) and bit 0 (Load Vendor/Device IDs) of word 0x0A are valid, this word will be read in to initialize the Vendor ID.

6.2.3.10 Initialization Control Word 2 (Word 0x0F)

This is the second word read by the 82544GC controller and contains additional initialization values which:

- Set defaults for some internal registers
- Enable/disable specific features

Table 27. Initialization Control Word 2 (Word 0x0F)

Bit	Name	Description
15	APM PME# Enable	Initial value of the Assert PME On APM Wakeup bit in the Wake Up Control Register (WUC.APMPME). Typically set to 1 for Intel LAN controller cards.
14	ASDE	Initial value of the Auto-Speed Detection Enable (ASDE) bit of the Device Control Register (CTRL). The Hardware default is 0. Typically set to 1 for 10/100/1000 M/bps implementation.
13:12	Pause Capability	Desired PAUSE capability for advertised configuration base page. Mapped to TXCW[8:7].
11	ANE	Auto-Negotiation Enable. Mapped to TXCW[31]. Fiber implementations typically set this to 1 to automatically enable auto-negotiation.
10:9	FLASH Size Indication	Indicates FLASH size. 00b=64KB;(01b=128KB; 10b=256KB; 11b=512KB. 00b is default in hardware. These bits impact the requested memory space for the FLASH and Expansion ROM BARs in PCI config space.
8	FLASH Disable	A value of 1 disables the FLASH logic. The Expansion ROM and secondary FLASH access BARs in PCI config space are disabled.
7	MSI Disable	If 1, this bit disables Message Signalled Interrupts in standard PCI mode.
6	133 MHz Capable	Mapped to 133 MHz Capable bit of the PCI-X Status Register (PCIXS). If 1, then the system is 133 MHz capable.
5	DMCR_Map	Indicates how the Designed Maximum Cumulative Read size bits in the PCI-X Status register is mapped. When set to 1 the DMCR value reflects the hard-coded design capability as indicated by the Max_Read bit below. When set to 0 the DMCR is mapped directly to the Maximum Memory Read Byte Count indicated in the PCI-X Command register. Default is 0 (reflects DMMRBC).
4	Max_Read	Indicates the maximum read value as advertised in the Designed Maximum Memory Read Byte Count field in the PCI-X Status Register.) If Max_Read is set to 0, or if there is no EEPROM, the advertised maximum read is 2KB. If it is set to 1 the advertised maximum read is 4KB. It is not recommended to set Max_Read=1 (thus advertising 4KB) as transmit FIFO overruns become possible under specific operating conditions.
3	64-bit	Loaded to the 64-bit Device field of the PCI-X Status Register.

Table 27. Initialization Control Word 2 (Word 0x0F)

Bit	Name	Description
2	APM Enable	Initial value of Advanced Power Management Wake Up Enable in the Wake Up Control Register (WUC.APME). Typically set to 1 to enable APM for Intel LAN controller cards.
1	Force CSR Read Split	Used to force all device control/status register-reads to be split when operating in a PCI-X environment. When cleared to 0 (default), certain critical registers will be decoded for non-split access.
0	Reserved	Reserved for future use.

6.2.3.11 OEM Reserved Words (Words 0x10-1F)

Words 0x10-0x1F have been reserved for general OEM use on the 82544GC controller. Future Intel products may use this space differently.

6.2.3.12 Software Defined Pins Control (Word 0x20)

This field contains initial settings for the Software Defined Pins.

Table 28. Software Defined Pins Control (Word 0x20)

Bit	Name	Description
15:14 12:8	SWDPIO	Software Defined Pins – direction. These seven bits override the hardware default for the directionality of the Software defined Pins. 0 = inputs; 1 = outputs. Bits 11:8 control the lower four pins and set the initial value of CTRL.SWDPIOLO. Bits 15:14 and bit 12 control the upper three pins and set the initial value of CTRL_EXT.SWDPIOHI. The default value for this byte is DFh.
7:6 4:0	SWDPINS	Software Defined Pins – value. These seven bits override the hardware default value output on the Software Defined pins if their direction is set to output. Bits 3:0 control the lower four pins and set the initial value of CTRL.SWDPINSLO. Bits 7:6 and bit 4 control the upper three pins and set the initial value of CTRL_EXT.SWDPINSHI. The default value for this byte is FFh.

Special Note: SDP5 is intentionally missing from the group of software-defined pins.

6.2.3.13 Circuit Control (Word 0x21)

This word is loaded into the Circuit Control Register for setting PCI-X driver strength. It should have a value of 0x0021.

6.2.3.14 D0 Power (Word 0x22 high byte)

If the signature bits are valid and Power Management is not disabled, the value in this field is used in the PCI Power Management Data Register when the Data_Select field of the Power Management Control/Status Register (PMCSR) is set to 0 or 4. It indicates the power usage and heat dissipation of the entire Ethernet port circuit in tenths of a watt in D0 mode. For example, a power estimate of 3.6 W yields 20d or 14h. 14h would be the programmed value.

6.2.3.15 D3 Power (Word 0x22 low byte)

If the signature bits are valid and Power Management is not disabled, the value in this field is used in the PCI Power Management Data Register when the *Data_Select* field of the *Power Management Control/Status Register* (PMCSR) is set to 3 or 7. It indicates the power usage and heat dissipation of the entire Ethernet port circuit in tenths of a watt in D3 mode.

6.2.3.16 PXE Configuration (Words 0x30-0x32)

Several words have been reserved for use by the Intel Boot Agent software, which includes PXE. If employed in the application, the Intel Boot Agent code resides in FLASH.

6.2.3.17 Checksum Word Calculation (Word 0x3Fh)

The Checksum word (0x3Fh) should be calculated such that after adding all the words (0x00h-0x3Fh), including the Checksum word itself, the sum should be 0xBABA. The initial value in the 16 bit summing register should be 0x0000 and the carry bit should be ignored after each addition. This checksum is not accessed by the 82544GC device. If CRC checking is required, it must be performed by software.

6.2.4 FLASH Memory

The 82544GC controller provides an external parallel interface to an optional FLASH or boot EPROM device. Accesses to the FLASH memory are controlled by the Ethernet device, but are accessible to host software as normal PCI reads or writes to the FLASH memory mapping range. The user can also map FLASH memory to I/O space. The 82544GC device supports 8-bit wide parallel FLASH memory up to 4Mb (512KB); an appropriate size for typical applications would be 1 Mb (128KB). The size of the FLASH implemented in the design may be encoded into bits in the EEPROM. FLASH and expansion ROM base address registers are reconfigured based on these EEPROM settings.

Representative flash memory devices that have been found to work satisfactorily with the 82544GC controller are listed in the following table (two different sizes):

Table 29. FLASH Memory Manufacturers

Manufacturer	Manufacturer's Part Number
Atmel	AT49LV010
Silicon Storage Technology	SST39V512

The FLASH memory interface trace routing is not critical because the interface runs at a very slow speed. In a tightly space-constrained design, the FLASH memory device is a good choice for placement in relative isolation from the 82544GC controller.

6.2.5 25 MHz Crystal

All designs require a 25 MHz clock source. The 82544GC Gigabit Ethernet Controller uses the 25 MHz source to generate clocks up to 125 MHz for the MAC and PHY circuits. For optimum results with lowest cost, connect a 25 MHz parallel resonant crystal and appropriate load capacitors to the XTAL1 and XTAL2 leads. Alternatively, a 25 MHz oscillator may be connected to XTAL1 with

XTAL2 left unconnected. In either case, the frequency tolerance of the timing device should be 50ppm or better. Refer to the application note, *82559 Fast Ethernet Controllers Timing Device Selection Guide, AP-419*, for more information on choosing crystals.

The 82544GC component uses the 25 MHz clock input to generate Ethernet data clocks as high as 125 MHz. Thus, the crystal is important to physical layer specification (IEEE) conformance as well as to EMI characteristics.

There are three steps to crystal qualification:

1. Verify that the vendor's published specifications in the component data sheet meet the required conditions for frequency, frequency tolerance, temperature, oscillation mode and load capacitance.
2. Independently measure the component's electrical parameters in real systems. Measure frequency at GTX_CLK to avoid test probe loading effects at XTAL2. Check that the measured behavior is consistent from sample to sample and that it meets the published specifications. For crystals, it is also important to examine startup behavior while varying system voltage and temperature.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems. When changing crystals, new EMI scans are not required if the existing design has sufficient margin and no other changes are made.

Place the crystal and load capacitors on the printed circuit boards as close to the 82544GC component as possible. If an oscillator is used instead, connect the clock signal with the shortest, most direct trace possible. Keep other traces away from the clock trace.

6.2.6 Power Supplies

The 82544GC controller requires four power supplies. The designer can typically tie the VDDO (3.3V I/O) and AVDDH (3.3V Analog) leads to a single 3.3V source. The other power supplies are DVDDH (1.3 V digital), DVDDL (1.5 V digital) and AVDDL (2.5 V analog).

A central power supply can provide all the required voltage sources, or the power can be derived and regulated locally near the Ethernet control circuitry. Keep in mind that all five sources must remain present during powerdown in order to use the 82544GC Ethernet controller's LAN wake up capability. This consideration makes it likely that at least some of the voltage sources will be local.

The 82544GC controller has a LAN_PWR_GOOD input to hold the device in reset during the power ramp and until all the voltage sources are stable. LAN_PWR_GOOD should also hold the device in reset a few extra milliseconds while the 82544GC controller's frequency reference (crystal or oscillator) stabilizes. In the situation where a central power supply furnishes all the voltage sources, LAN_PWR_GOOD can usually be tied directly to the POWER_GOOD output on the power supply. Designs that generate some of the voltages locally for the Ethernet controller may require delaying LAN_PWR_GOOD assertion with additional circuitry to assure that all the sources have time to reach stable operating voltages.

The power sources are all expected to ramp up during a brief power-up interval with LAN_PWR_GOOD deasserted. Do not leave the 82544GC controller in a prolonged state where some, but not all, voltages are applied. The only exception to this rule is in powerdown mode, where the device can continue to be powered up without VIO reference (either 5V or 3.3V) being present.

6.2.7 Power Supply Filtering

The 82544GC controller switches relatively high currents at high frequencies, requiring generous use of both bulk capacitance and high speed decoupling capacitance adjacent to the device. In the case of a double-sided printed circuit board design, some of the capacitors can be placed directly under the controller.

Provide approximately six to eight bypass capacitors along each side of the controller, selecting values in the range of 0.001µF to 0.01µF. If possible, orient the capacitors close to the device and adjacent to power pads. Decoupling capacitors should connect to the power planes with short, thick (15 mils – 0.4mm or more) traces and 14 mil (0.35mm) vias. Capacitor arrays may be used to reduce the overall package count.

Furnish approximately 30µF of bulk capacitance for each of the four voltage levels. A convenient way to do this is to use about a dozen 10µF capacitors, placing them as close to the device power connections as possible.

Use decoupling and bulk capacitors generously. If the design turns out to be “quieter” than expected, it is easy to delete capacitors during manufacturing.

6.2.8 Power Management and Wake Up

The 82544GC Gigabit Ethernet Controller supports low power operation as defined in the PCI Bus Power Management Specification. There are two defined power states, D0 and D3. The D0 state provides full power operation and is divided into two sub-states: $D0_u$ (uninitialized) and $D0_a$ (active). The D3 state provides low power operation and is also divided into two sub-states: $D3_{hot}$ and $D3_{cold}$.

To enter the low power state, the software driver must stop data transmission and reception. Either the operating system or the driver must program the Power Management Control/Status Register (PMCSR) and the Wakeup Control Register (WUC). If wakeup is desired, the appropriate wakeup LAN address filters must also be set. Then the system can optionally assert PCI_RESET_N. The initial power management settings are specified by EEPROM bits.

When the 82544GC controller transitions to either of the D3 low power states, VDDO and AVDDH (3.3V), AVDDL (2.5V), DVDDH (1.8V), and DVDDL (1.5V) must continue to be supplied to the device. Otherwise, it will not be possible to use a wakeup mechanism. This is an important consideration in deciding whether to provide the power sources locally or from a central power supply. Commercial power supplies commonly provide 3.3V_AUX, but not the full range of voltages required by the 82544GC device.

The AUX_POWER signal is a logic input to the 82544GC controller that denotes auxiliary power is available. If AUX_POWER is asserted, the 82544GC device will advertise that it supports wake up from a $D3_{cold}$ state. The controller will also adjust the effect of reset upon the Power Management Enable (PME_N) pin so that PCI_RESET_N deassertion cannot disable certain powerdown and wakeup settings.

The 82544GC supports both Advanced Power Management (APM) wakeup and Advanced Configuration and Power Interface (ACPI) wakeup. APM wakeup has also been known in the past as “Wake on LAN”.

APM wakeup uses the APM_WAKEUP signal to wake the system up and can optionally use the PME# signal. APM_WAKEUP is an active high output that pulses for approximately 50ms. when the controller receives a special “Magic Packet”.

ACPI wakeup uses the PME_N signal to wake the system up. PME_N is an active low signal that goes active in response to receiving a “Magic Packet”, a network wakeup packet, or link status change indication. PME_N remains asserted until it is disabled through the Power Management Control/Status Register.

6.2.9 Light Emitting Diodes

The 82544GC controller provides several high-current, open-drain outputs to directly drive LEDs for link status, speed and duplex mode. Trace routing to the LEDs should have a low priority, as these are low frequency signals.

6.2.10 Test Access Port

The test access port conforms to the IEEE 1149.1a-1994 (JTAG) Boundary Scan specification. To use the test access port, connect these balls to pads accessible by your test equipment. Be sure to connect the TRST# input to ground through a pulldown resistor (approximately 1k value) so that the test capability cannot be invoked by mistake.

A BSDL (Boundary Scan Definition Language) file describing the 82544GC device is available for use in your test environment.

6.3 Design and Layout Considerations for 1000BASE-T Circuits

In 1000BASE-T systems, the main design elements are the 82544GC Gigabit Ethernet Controller, the magnetics module, and the RJ-45 connector. Since the transmission line medium extends onto the printed circuit board, special attention must be paid to layout and routing of the differential signal pairs.

Designing for gigabit operation will be the primary concern, but 82544GC controller Ethernet designs for twisted pair copper wiring will also operate at 10 and 100 Mbps. System level tests should be performed at all three speeds.

6.3.1 Magnetics Module

Magnetics modules for 1000BASE-T Ethernet are very similar to those designed solely for 10/100Mbps, except that there are four differential signal pairs instead of two.

The magnetics module has a critical effect on overall IEEE and emissions conformance. The device should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Occasionally, components that meet basic specifications may cause the system to fail IEEE testing because of interactions with other components or the printed circuit board itself. Carefully qualifying new magnetics modules can go a long way toward preventing this type of problem.

The steps involved in magnetics module qualification are similar to those for oscillator qualification:

1. Verify that the vendor’s published specifications in the component data sheet meet the required IEEE specifications.
2. Independently measure the component’s electrical parameters on the test bench, checking samples from multiple lots. Check that the measured behavior is consistent from sample to sample as well as meeting the published specifications.

3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems. Vary temperature and voltage while performing system level tests.

Magnetics modules that have been found to work satisfactorily with the 82544GC controller are listed in the following table:

Table 30. Magnetics Module Manufacturers

Manufacturer	Manufacturer's Part Number
Pulse Engineering	5007
Bel Fuse	S558-5999-P3

6.3.2 Combination Magnetics/RJ-45 Connectors

Recently, manufacturers have designed combination magnetics module/RJ-45 connectors. These integrated components offer significant space savings for LAN on motherboard designs. Multiport integrated modules are available as well as single-port designs.

Follow the same steps (listed above) for discrete components to qualify integrated magnetics module/RJ-45 connectors.

Table 31. Combination Magnetics/RJ-45 Connector Manufacturers

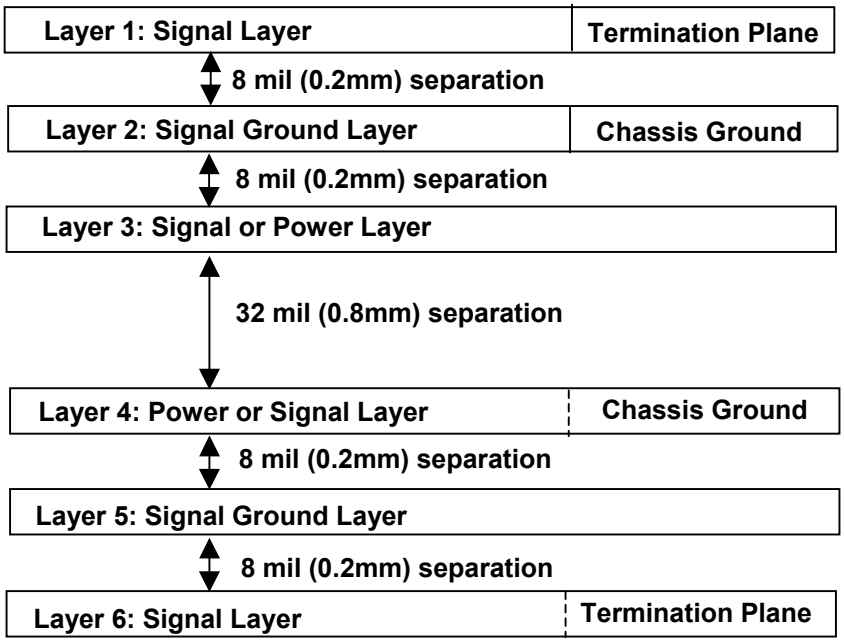
Manufacturer	Manufacturer's Part Number
TBD	TBD

6.3.3 Unused Connections

Follow good engineering practices with respect to unused inputs by terminating them with pullup or pulldown resistors, unless the data sheet, developer's manual or reference design indicates otherwise. Do not attach pullup or pulldown resistors to any balls identified as No Connect. The 82544GC Gigabit Ethernet Controller may have special test modes that could be entered inadvertently.

6.3.4 Board Stack Up Recommendations for 1000BASE-T Designs

Printed circuit boards for 1000BASE-T designs using the 82544GC Gigabit Ethernet Controller will typically have six, eight or more layers. The following diagram illustrates a possible board stack up for a six-layer, 62 mil (1.6mm) printed circuit board.



Descriptions of the board layers are as follows:

- Layer 1 is a signal layer. It typically contains the differential analog pairs from the 82544GC device to the magnetics module and from the magnetics module to the RJ-45 connector. The termination plane described in Section 6.3.6 is also fabricated in Layer 1.
- Layer 2 is a signal ground layer. The chassis ground is also fabricated in Layer 2.
- Layer 3 and 4 are used for power and/or signal layers. In the vicinity of the 82544GC device, one or both layers may be broken up into power planes for the four voltage levels required for the device. The remaining area in these layers may be used for signal routing. In the vicinity of the RJ-45 connector, additional chassis ground metal can be fabricated in Layer 4.
- Layer 5 can be used as an additional ground layer.
- Layer 6 is a signal layer. Additional termination plane area can also be fabricated in Layer 6.

This board stack up configuration can be adjusted to conform to your company's design rules. For instance, some companies disallow asymmetrical power planes due to increased risk of board warpage. In some cases, this concern can be overcome by adding extra metal fill in an offsetting board layer.

6.3.5 Transmission Line Layout for 1000BASE-T Designs

The following sections detail the key interfaces in the gigabit Ethernet LAN circuit that need special placement and routing attention. The important signals are the differential signal pairs running from the 82544GC Ethernet controller to the magnetics module and then to the RJ-45 connector.

The interface from the 82544GC device to the magnetics module operates with analog signaling at a clock rate of 125 MHz. The four pairs of signals should be treated as high-speed transmission lines, with careful attention to layout guidelines. Each pair of signal should have a target differential impedance of 100 Ω If a particular tool or layout vendor cannot design differential traces, it is permissible to specify 55-65 Ω single-ended traces as long as the spacing between the two traces is minimized. As an example, consider a differential trace pair on Layer 1 that is 8 mils (0.2mm) wide and 2 mils (0.05mm) thick, with a spacing of 8 mils (0.2mm). If the fiberglass layer is 8 mils (0.2mm) thick with a dielectric constant, E_R, of 4.7, the calculated single-ended impedance would be approximately 61 Ω and the calculated differential impedance would be approximately 100 Ω

When performing a board layout, do not allow the CAD tool auto-router to route the differential pairs without intervention. In most cases, the differential pairs will have to be routed manually.

6.3.5.1 Trace Length and Symmetry in 1000BASE-T Designs

The differential pairs should be routed to be as short and symmetrical as possible. The overall length of differential pairs should be less than four inches measured from the 82544GC controller across the magnetics module to the RJ-45 connector. The distance between the magnetics module and the RJ-45 connector is somewhat more important than the distance between the 82544GC device and the magnetics module.

The lengths of the differential traces (within each pair) should be equal within 50 mils (1.25mm) and as symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. Minimize the distance from trace to trace within each pair to be no more than 30 mils (0.75mm).

To reduce crosstalk interference on signals between pairs, the minimum distance between unlike differential pairs must be 50 mils (1.25mm). This rule also applies to differential pairs from other Ethernet controller circuits on the same board.

6.3.5.2 Impedance Discontinuities in 1000BASE-T Designs

Impedance discontinuities cause unwanted signal reflections. To minimize impedance discontinuity, traces within differential pairs must not have bends over 45 degrees. If possible, the corners of all bends should be rounded to enhance performance.

Avoid vias and other transmission line irregularities. If vias must be used, a reasonable via budget is two per differential trace. Unused pads and stub traces should also be avoided.

6.3.5.3 Signal Clutter in 1000BASE-T Designs

To maintain best signal integrity, keep digital signals far away from the analog traces. A good rule of thumb is no digital signal should be within 300 mils (7.5mm) of the differential pairs. If digital signals on other board layers cannot be separated by a ground plane, they should be routed at right

angles with respect to the differential pairs. If there is another LAN controller on the board, take care to keep the differential pairs from that circuit away. Ganged RJ-45 connectors are allowed, but the signals for each circuit must also be carefully separated.

Integrated magnetics modules with RJ-45 jacks may be utilized as indicated in Section 6.3.2. When using integrated components, be careful that the 82544GC Ethernet controller is not placed too close to the back edge of the board as this may lead to increased EMI.

6.3.5.4 Signal Terminations for 1000BASE-T Designs

The four differential pairs are terminated with 49.9 Ω (1% tolerance) resistors, placed near the 82544GC controller. One resistor connects to the MDI+ signal trace and another resistor connects to the MDI- signal trace. The opposite ends of the resistors connect together and to ground through a single 0.01µF capacitor. Do not vary the suggested component values. Be sure to lay out symmetrical pads and traces for these components such that the length and symmetry of the differential pairs are not disturbed.

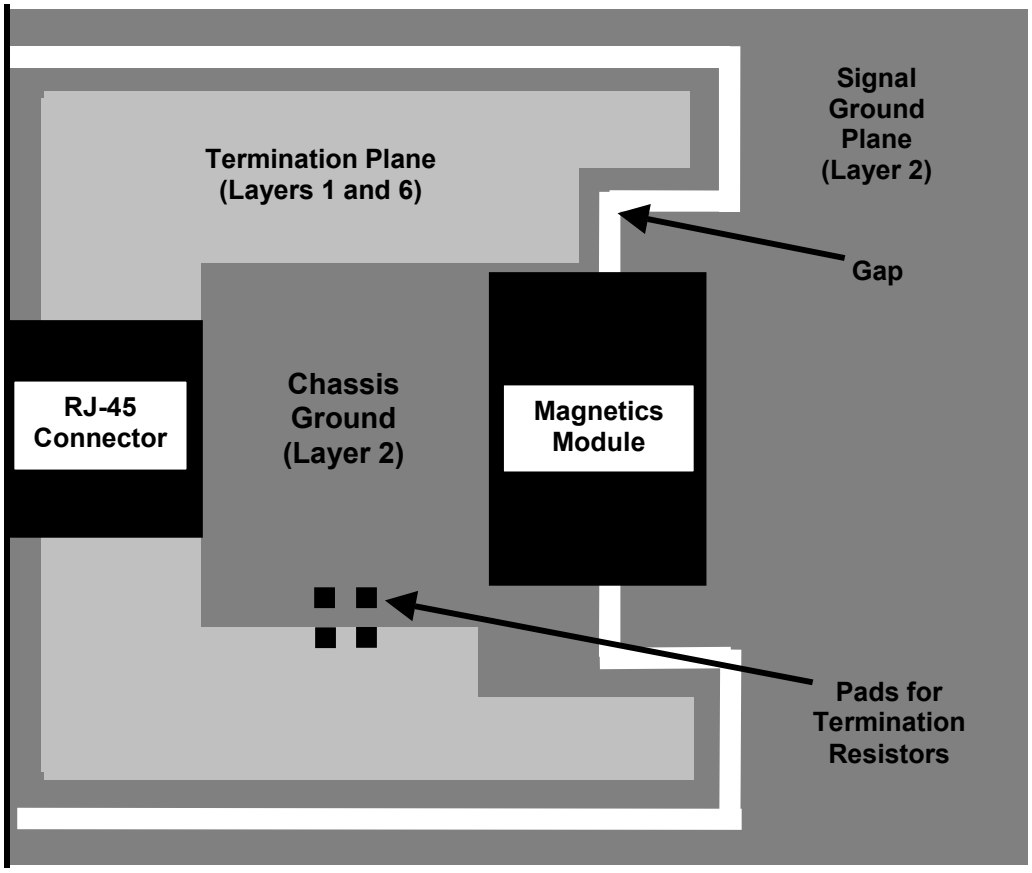
6.3.6 Termination Plane and Chassis Ground in 1000BASE-T Designs

For gigabit Ethernet designs, it is common practice to terminate center tap magnetics module connections (RJ-45 side) to ground as a path for low frequency noise. Depending on the overall shielding and grounding design, the specific ground used for this purpose may vary. Intel recommends the use of a dedicated termination plane, with the center tap leads connected to the termination plane through 75 Ω resistors.

The termination plane is typically fabricated in Layer 1, with a matching chassis ground plane underneath as illustrated in the following figure. The clearance between the termination plane and any traces should be at least 50 mils (1.25mm) to prevent arcing during high voltage tests. The termination plane/chassis ground layer combination has some capacitance, which can be augmented by adding a discrete 1500pF capacitor.

Integrated magnetics model/RJ-45 connectors also contain the termination plane, 75 Ω termination resistors, and, in some cases, a 1000 – 1500 pF capacitor. If you are considering the use of integrated components, evaluate their internal design carefully. Make certain that the electrical parameters, EMI, and high voltage test results are equivalent to, or better than, the characteristics of a discrete design.

Additional capacitors are required to interconnect chassis ground and signal ground. The suggested technique is to use several different capacitor values, for example, two 1000pF, one 4.7µF, and one 10uF. Depending on the available board space, place one set of capacitors on each side of the magnetics module. Modifications to this interconnection scheme are possible. See the diagram below:



6.3.7 1000BASE-T Physical Layer Conformance Testing

Physical layer conformance testing (also known as IEEE testing) is a fundamental capability for all companies with Ethernet LAN products. If your company does not have the resources and equipment to perform these tests, consider contracting the tests to an outside facility.

Crucial tests for 1000BASE-T designs are as follows, listed in priority order:

- Bit Error Rate. Good indicator of real world network performance. Perform bit error rate testing with long and short cables and many link partners. The test limit is 10^{-11} errors.
- Output Amplitude, Symmetry and Droop. Use the appropriate 82544GC controller PHY test waveform.
- Return Loss. Indicator of proper impedance matching, measured through the RJ-45 connector back toward the magnetics module.
- Unfiltered Jitter Test. Indicator of clock recovery ability as master and slave.

The Unfiltered Jitter Test requires activation of a special test mode on the MAC as well as selecting test waveforms in the PHY. This test mode will expose the transmit clock (on GTX_CLK) and the internal receive clock (on RBC1) from the internal GMII interface for use as scope triggers. Since the 82544GC device is an integrated MAC/PHY controller, these signals are not brought out during normal operation.

Using the MAC test mode requires some special connections and layout changes. Connect GMII_TEST0 and GMII_TEST1 inputs to a common 1K pulldown resistor and to a common test point. Use "cuttable" traces to connect TX_DATA[9:0] and RX_DATA[9:0] balls to their pulldown resistors. A cuttable trace is defined as a copper circuit strip placed conspicuously on an outside board layer so that it can be easily cut with a tool such as a utility knife. It is permissible to gang the signals together to minimize the number of resistors, as shown in the reference schematic in this manual., as long as the traces are individually accessible. Connect the GTX_CLK signal to its own 1K pulldown resistor with a test point. Connect RBC1 to its own 1K pulldown resistor with a test point. Finally, connect RBC0 to its own 1K pulldown resistor without a test point. Do not gang any of these three test clock outputs with any other signals. COL_TEST and CRS_TEST require individual 1K pulldown resistors on each signal.

To perform the IEEE Unfiltered Jitter Test on your prototype boards, first cut all the traces on the TX_DATA and RX_DATA signals. They will become outputs during the test. Drive the test point connected to GMII_TEST[1:0] to a logic high value. Now the GTX_CLK is available at its test point and the receive clock is available at the test point labeled RBC1. Follow the IEEE specifications for details on how to perform the test. The remaining signals of the GMII interface (RBC0, COL_TEST, CRS_TEST, TX_DATA[9:0] and RX_DATA[9:0]) are now active outputs, but are not needed for IEEE testing.

After your prototypes meet the Unfiltered Jitter Test, you can change the board layout to replace the cuttable traces with more direct traces, if desired. In normal operation (with GMII_TEST[1:0] = 00), the controller floats RBC[1:0], COL_TEST, CRS_TEST, TX_DATA[9:0], RX_DATA[9:0], and GTX_CLK. You can now gang all of these signals to minimize the number of pulldown resistors to approximately four.

There are several other PHY conformance tests to consider before committing your design to volume production. Consult IEEE specification 802.3ab for details.

6.4 Design and Layout Considerations for 1000BASE-SX Circuits

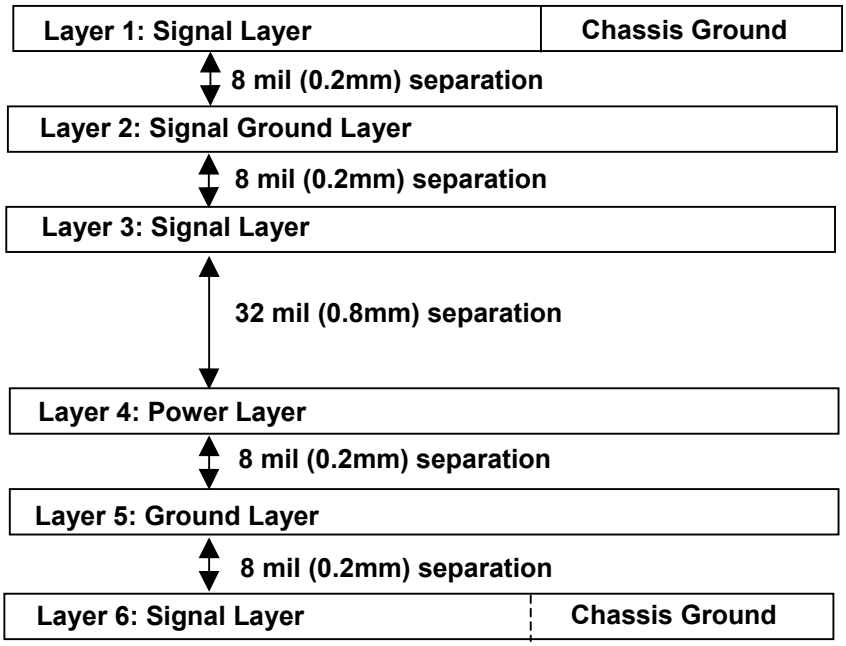
In 1000BASE-SX systems, the main design elements are the 82544GC Gigabit Ethernet Controller, a serializer/deserializer (SERDES) device, and an optical transceiver. A Signal Detect (SD) output from the optical transceiver connects to the 82544GC controller LOS input, indicating the presence of the optical carrier. Depending on the model of optical transceiver used, the SD signal may need conditioning.

1000BASE-SX systems operate only at gigabit data speeds.

1000BASE-SX designs require less attention to the physical transmission medium because the optical transceivers are manufactured as closed, tested units. However, the analog signals between the SERDES and the optical transceiver run at gigahertz speeds, requiring careful attention to layout and routing.

6.4.1 Board Stack Up Recommendations for 1000BASE-SX Designs

Printed circuit boards for 82544GC controller based 1000BASE-SX designs will be similar to those used for 1000BASE-T designs. The following diagram illustrates a possible board stack up for a six-layer, 62 mil (1.6mm) printed circuit board.



Descriptions of the board layers are as follows:

- Layer 1 is a signal layer. It typically contains the high-speed differential analog pairs from the SERDES device to the optical transceiver. The chassis ground is also fabricated in Layer 1.
- Layer 2 is a signal ground layer.
- Layer 3 is a signal layer. The data and clock signals between the 82544GC controller and the SERDES device are routed in Layer 3.
- Layer 4 is used as the power layer.
- Layer 5 is an additional ground layer.
- Layer 6 is a signal layer. In the vicinity of the optical transceiver, additional chassis ground metal can be fabricated in Layer 6.

As suggested earlier, you should adapt this stack up configuration to the design rules in force at your company, particularly those rules aimed at preventing board warpage.

6.4.2 High Speed Signal Layout for 1000BASE-SX Designs

The following sections detail the key interfaces in the gigabit Ethernet LAN circuit that need special placement and routing attention. The important signals are the data and clock lines between the 82544GC Ethernet controller and the SERDES device and between the SERDES device and the optical transceiver.

The 10-bit interface (TBI) from the 82544GC device to the SERDES operates at a clock rate of 125 MHz for transmit and 62.5 MHz for receive. (There are two 62.5 MHz receive clocks 180° out of phase.) The 20 data lines, TX_CLK, RBC0 and RBC1 should be treated as high-speed transmission lines, with careful attention to routing.

The data lines between the SERDES and the optical transceiver use pseudo-ECL switching and are clocked at a 1.25GHz rate. The two pairs of signals should have target differential impedance of 100 Ω If a particular tool or layout vendor cannot design differential traces, it is permissible to use 55 Ω single-ended traces.

As with 1000BASE-T designs, 1000BASE-SX designs are likely to require manual routing on the high-speed traces.

6.4.2.1 Trace Length and Symmetry in 1000BASE-SX Designs

The high-speed traces between the 82544GC controller and the SERDES should be routed to be less than 1.5 inches in length. The lengths of the RX_DATA traces, RBC0 trace and RBC1 trace should be equal within 50 mils (1.25mm). Similarly, the TX_DATA and TX_CLK traces should be equal in length. To reduce crosstalk interference, RX_DATA and TX_DATA lines should be separated by at least 50 mils (1.25mm) if they are on the same plane.

The differential pairs between the SERDES and optical transceiver should be routed to be as short and as symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. The overall length of these differential pairs should be no more than two inches.

The lengths of the differential traces (within each pair) should be equal within 10 mils (0.25mm). The distance from trace to trace within each pair should be minimized – 6 mil (0.15mm) spacing is good. To reduce crosstalk interference on signals between pairs, the minimum distance between unlike differential pairs must be 50 mils (1.25mm).

6.4.2.2 Impedance Discontinuities in 1000BASE-SX Designs

Differential pairs must not have bends over 45 degrees. Round the corners of all bends if possible and avoid other transmission line irregularities.

Due to the pinout of the typical SERDES device used in 1000BASE-SX applications, vias will be required to make the receive and transmit differential signals cross on the way to the optical transceiver. Avoid using more than two vias in each of the traces that cross over. As with 1000BASE-T designs, unused pads and stubs should also be avoided.

6.4.2.3 Signal Terminations for 1000BASE-SX Designs

The PECL signals have AC terminations on each line. Obtain Intel's 1000BASE-SX reference schematic and copy the resistors and capacitors exactly. Make the pads and traces for these components as short and symmetrical as possible. These terminations should be placed as close as possible to the driven ends of the differential traces.

6.4.3 Chassis Ground in 1000BASE-SX Designs

Chassis ground layers isolate analog ground noise from digital ground noise. The separation between the chassis ground and the signal ground should be at least 50 mils (1.25mm). High-speed data lines should not cross any plane splits.

6.4.4 1000BASE-SX Physical Layer Conformance Testing

Physical layer conformance tests for optical fiber designs are more specialized than tests for copper gigabit designs. If your company does not have an optical adapter for the network analyzer, consider contracting the tests to an outside facility.

Important tests for 1000BASE-SX designs are as follows, listed in priority order:

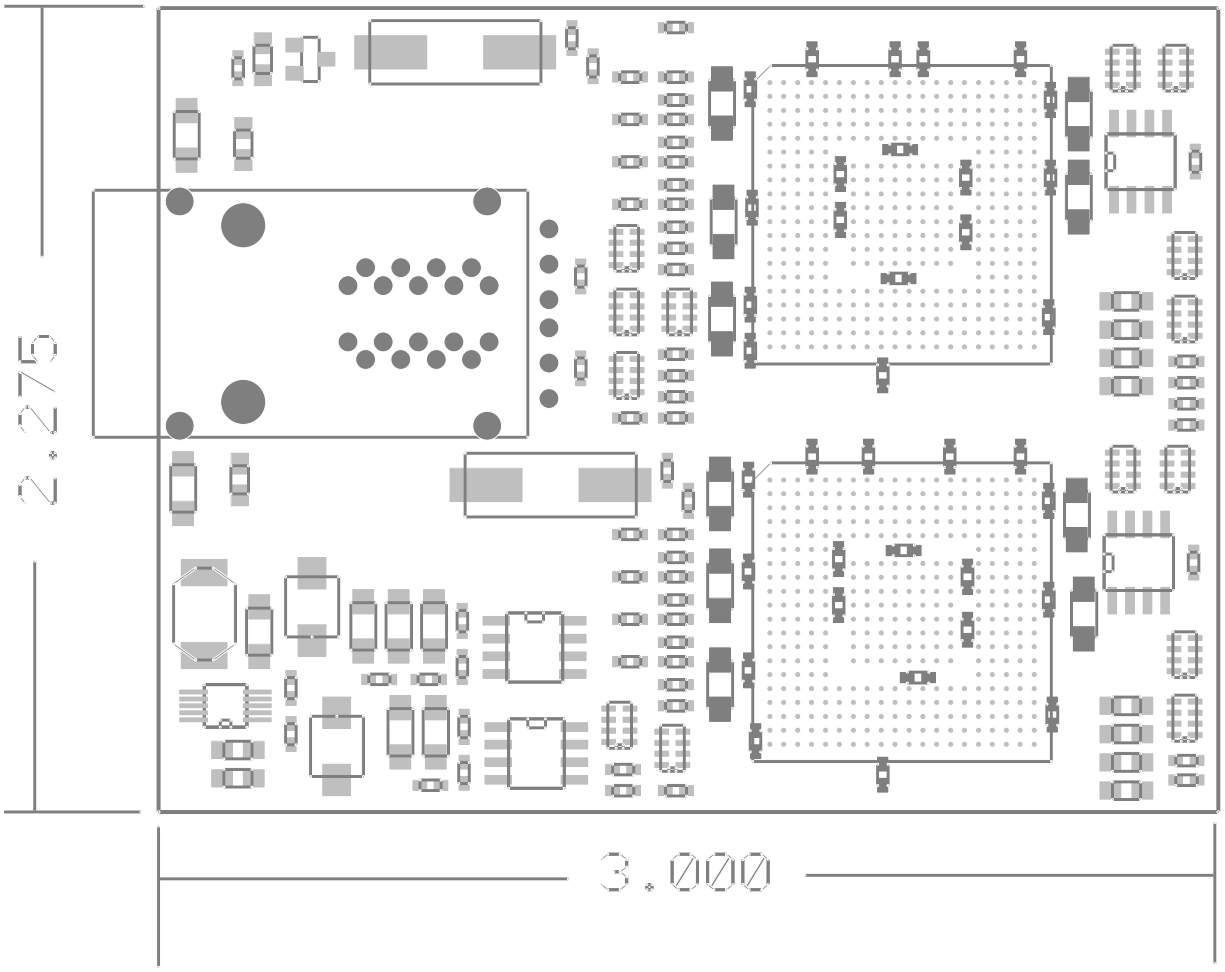
- Bit Error Rate. The test limit for the fiber implementation is 10^{-12} errors.
- Jitter. Indication of clock integrity.
- Extinction Ratio and Launch Power. Tests specific to fiber Ethernet implementations.

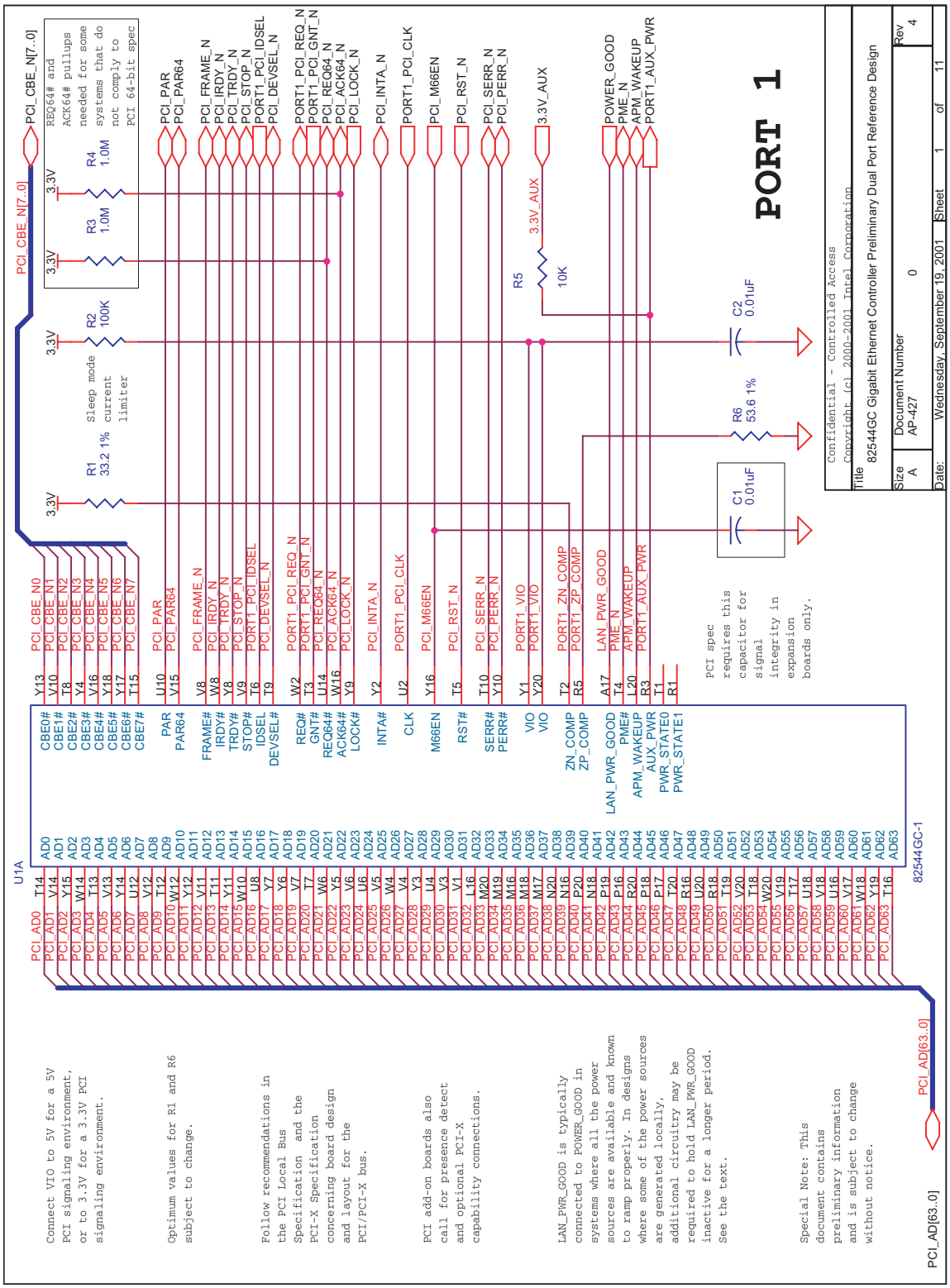
7.0 Reference Design Schematic

The following pages contain a reference schematic for a dual part gigabit design based on the 82544GC controller.

Figure 23 is a representation of how such a design could fit into a board space of less than seven square inches (including voltage regulators and a dual combination magnetics module/RJ-45 connector). This figure is for illustration purposes only; some of the components in the reference schematic may vary slightly (e.g., the reference schematic does not contain voltage regulators).

Figure 23. Proposed Layout for Dual Port Gigabit Design based on 82544GC Gigabit Ethernet Controller




PORT 1
82544GC-1
U1A
PCI_CBE_N[7..0]
PCI_AD[63..0]
R1 33.2 1%
R2 100K
R3 1.0M
R4 1.0M
R5 10K
R6 53.6 1%
C1 0.01uF
C2 0.01uF
3.3V
3.3V_AUX
Sleep mode current limiter
REQ64# and ACK64# pullups needed for some systems that do not comply to PCI 64-bit spec
PCI spec requires this capacitor for signal integrity in expansion boards only.
Connect VIO to 5V for a 5V PCI signaling environment, or to 3.3V for a 3.3V PCI signaling environment.
Optimum values for R1 and R6 subject to change.
Follow recommendations in the PCI local Bus Specification and the PCI-X Specification concerning board design and layout for the PCI/PCI-X bus.
PCI add-on boards also call for presence detect and optional PCI-X capability connections.
LAN_PWR_GOOD is typically connected to POWER_GOOD in systems where all the power sources are available and known to ramp properly. In designs where some of the power sources are generated locally, additional circuitry may be required to hold LAN_PWR_GOOD inactive for a longer period. See the text.
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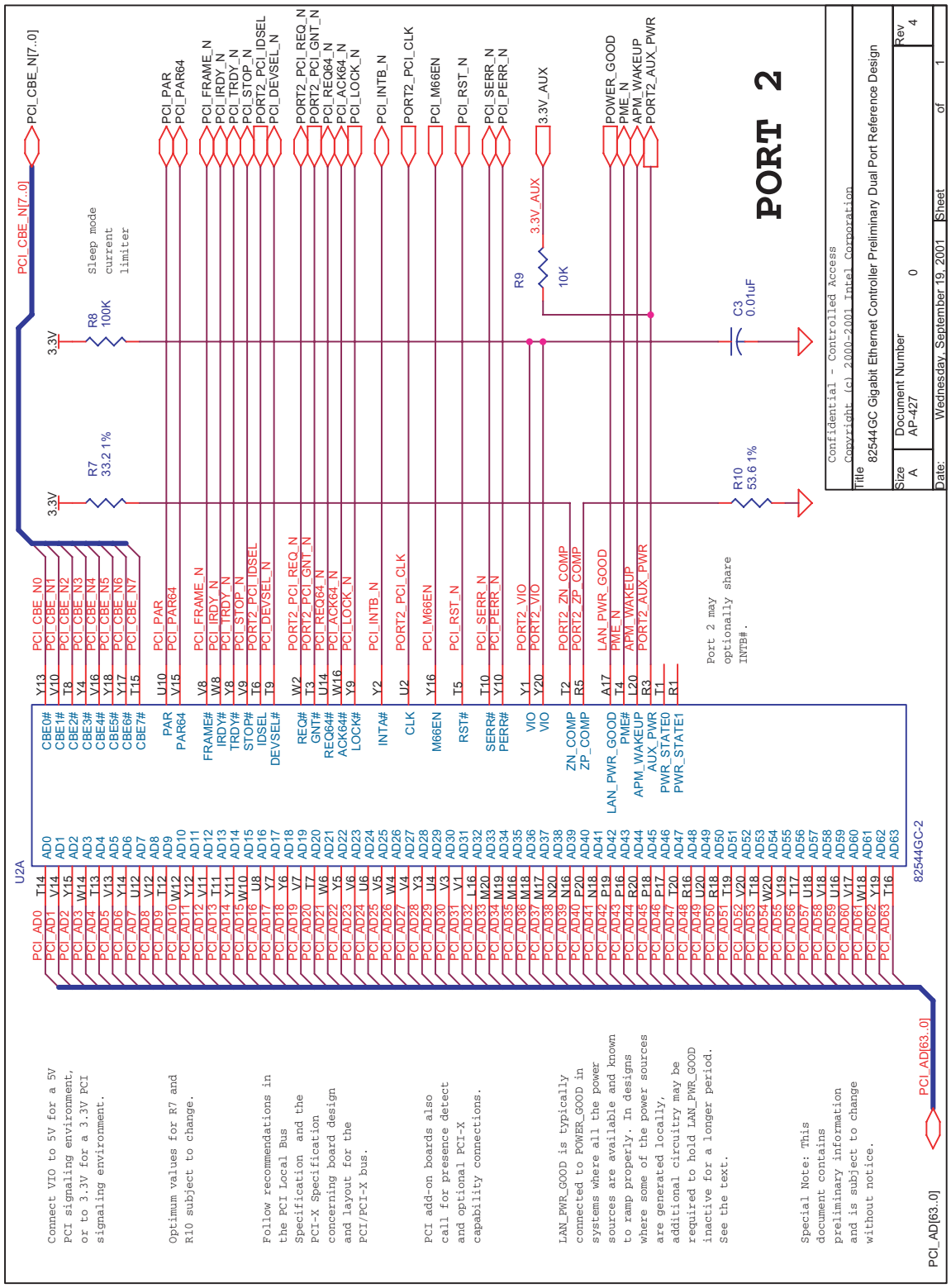
PORT 2
U2A
82544GC-2
PCI_CBE_N[7..0]
PCI_AD[63..0]
3.3V
3.3V_AUX
R7 33.2 1%
R8 100K
R9 10K
R10 53.6 1%
C3 0.01uF
Sleep mode current limiter
Port 2 may optionally share INTB#.
Connect VIO to 5V for a 5V PCI signaling environment, or to 3.3V for a 3.3V PCI signaling environment.
Optimum values for R7 and R10 subject to change.
Follow recommendations in the PCI Local Bus Specification and the PCI-X Specification concerning board design and layout for the PCI/PCI-X bus.
PCI add-on boards also call for presence detect and optional PCI-X capability connections.
LAN_PWR_GOOD is typically connected to POWER_GOOD in systems where all the power sources are available and known to ramp properly. In designs where some of the power sources are generated locally, additional circuitry may be required to hold LAN_PWR_GOOD inactive for a longer period. See the text.
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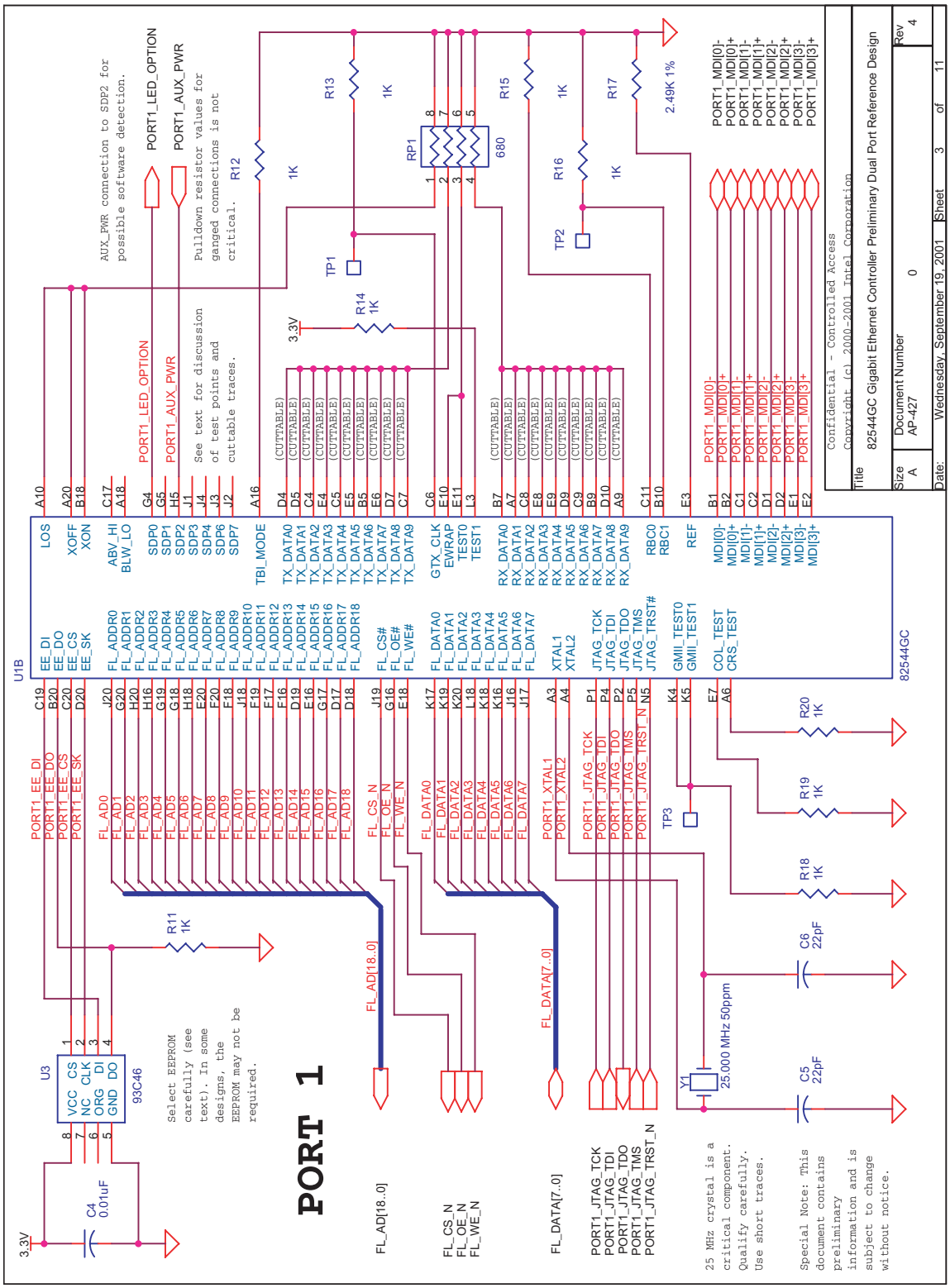
PORT 1
U1B
82544GC
U3
93C46
Select EEPROM carefully (see text). In some designs, the EEPROM may not be required.
AUX_PWR connection to SDP2 for possible software detection.
Pulldown resistor values for ganged connections is not critical.
See text for discussion of test points and cuttable traces.
25 MHz crystal is a critical component. Qualify carefully. Use short traces.
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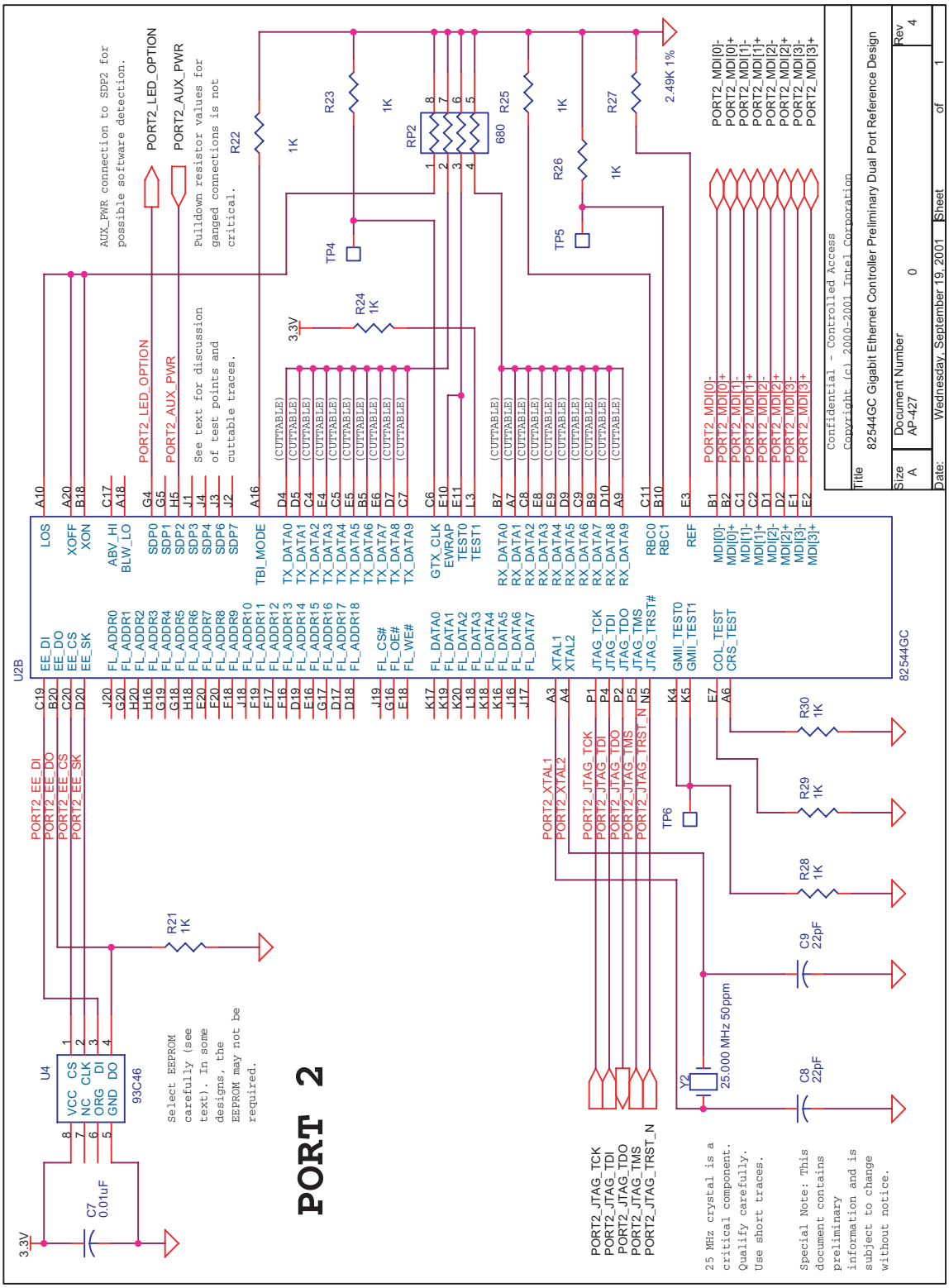
PORT 2
U2B
82544GC
U4
93C46
Y2
25.000 MHz 50ppm
R21 1K
R22
R23
R24 1K
R25 680
R26 1K
R27 1K
R28 1K
R29 1K
R30 1K
RP2
TP4
TP5
TP6
C7 0.01uF
C8 22pF
C9 22pF
2.49K 1%
3.3V
PORT2_LED_OPTION
PORT2_AUX_PWR
AUX_PWR connection to SDP2 for possible software detection.
Pulldown resistor values for ganged connections is not critical.
See text for discussion of test points and cuttable traces.
Select EEPROM carefully (see text). In some designs, the EEPROM may not be required.
25 MHz crystal is a critical component. Qualify carefully. Use short traces.
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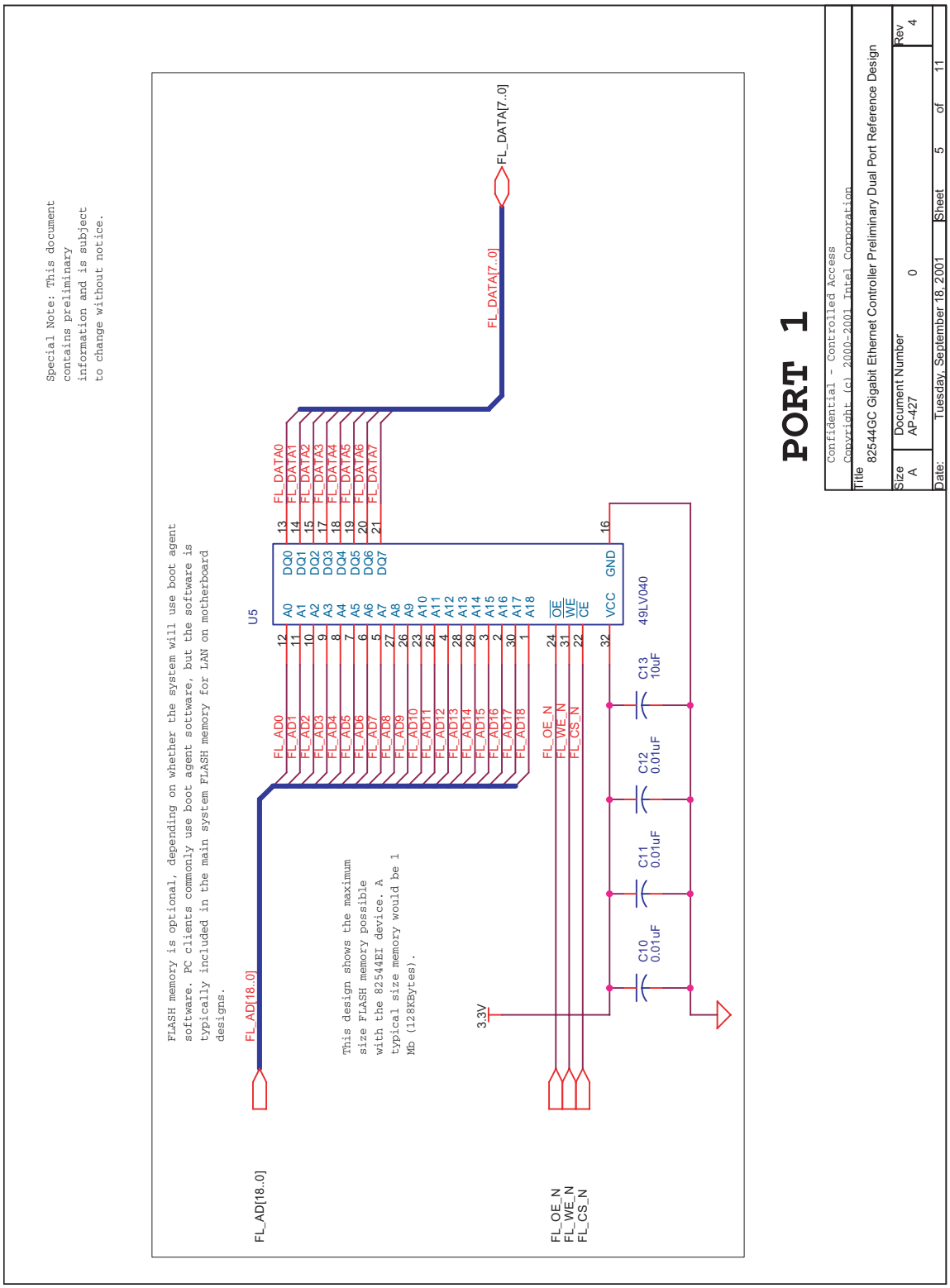
Special Note: This document
contains preliminary
information and is subject
to change without notice.
FLASH memory is optional, depending on whether the system will use boot agent
software. PC clients commonly use boot agent software, but the software is
typically included in the main system FLASH memory for LAN on motherboard
designs.
This design shows the maximum
size FLASH memory possible
with the 82544EI device. A
typical size memory would be 1
Mb (128KBytes).
U5
49LV040
FL_AD[18..0]
FL_DATA[7..0]
FL_OE_N
FL_WE_N
FL_CS_N
3.3V
C10 0.01uF
C11 0.01uF
C12 0.01uF
C13 10uF
PORT 1
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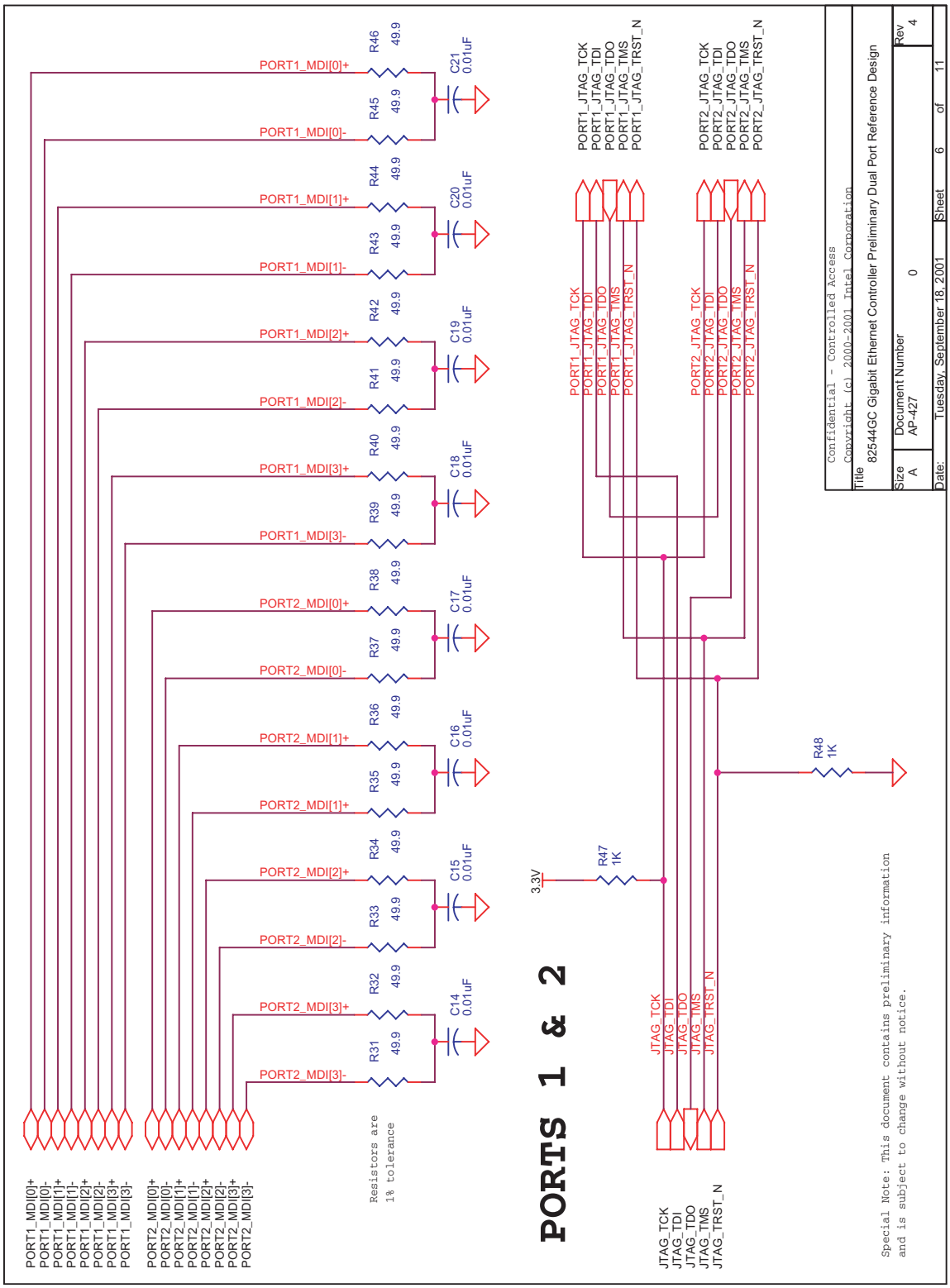
PORTS 1 & 2
PORT1_MDI[0]+
PORT1_MDI[0]-
PORT1_MDI[1]+
PORT1_MDI[1]-
PORT1_MDI[2]+
PORT1_MDI[2]-
PORT1_MDI[3]+
PORT1_MDI[3]-
PORT2_MDI[0]+
PORT2_MDI[0]-
PORT2_MDI[1]+
PORT2_MDI[1]-
PORT2_MDI[2]+
PORT2_MDI[2]-
PORT2_MDI[3]+
PORT2_MDI[3]-
R46 49.9
R45 49.9
R44 49.9
R43 49.9
R42 49.9
R41 49.9
R40 49.9
R39 49.9
R38 49.9
R37 49.9
R36 49.9
R35 49.9
R34 49.9
R33 49.9
R32 49.9
R31 49.9
C21 0.01uF
C20 0.01uF
C19 0.01uF
C18 0.01uF
C17 0.01uF
C16 0.01uF
C15 0.01uF
C14 0.01uF
Resistors are 1% tolerance
3.3V
R47 1K
R48 1K
PORT1_JTAG_TCK
PORT1_JTAG_TDI
PORT1_JTAG_TDO
PORT1_JTAG_TMS
PORT1_JTAG_TRST_N
PORT2_JTAG_TCK
PORT2_JTAG_TDI
PORT2_JTAG_TDO
PORT2_JTAG_TMS
PORT2_JTAG_TRST_N
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST_N
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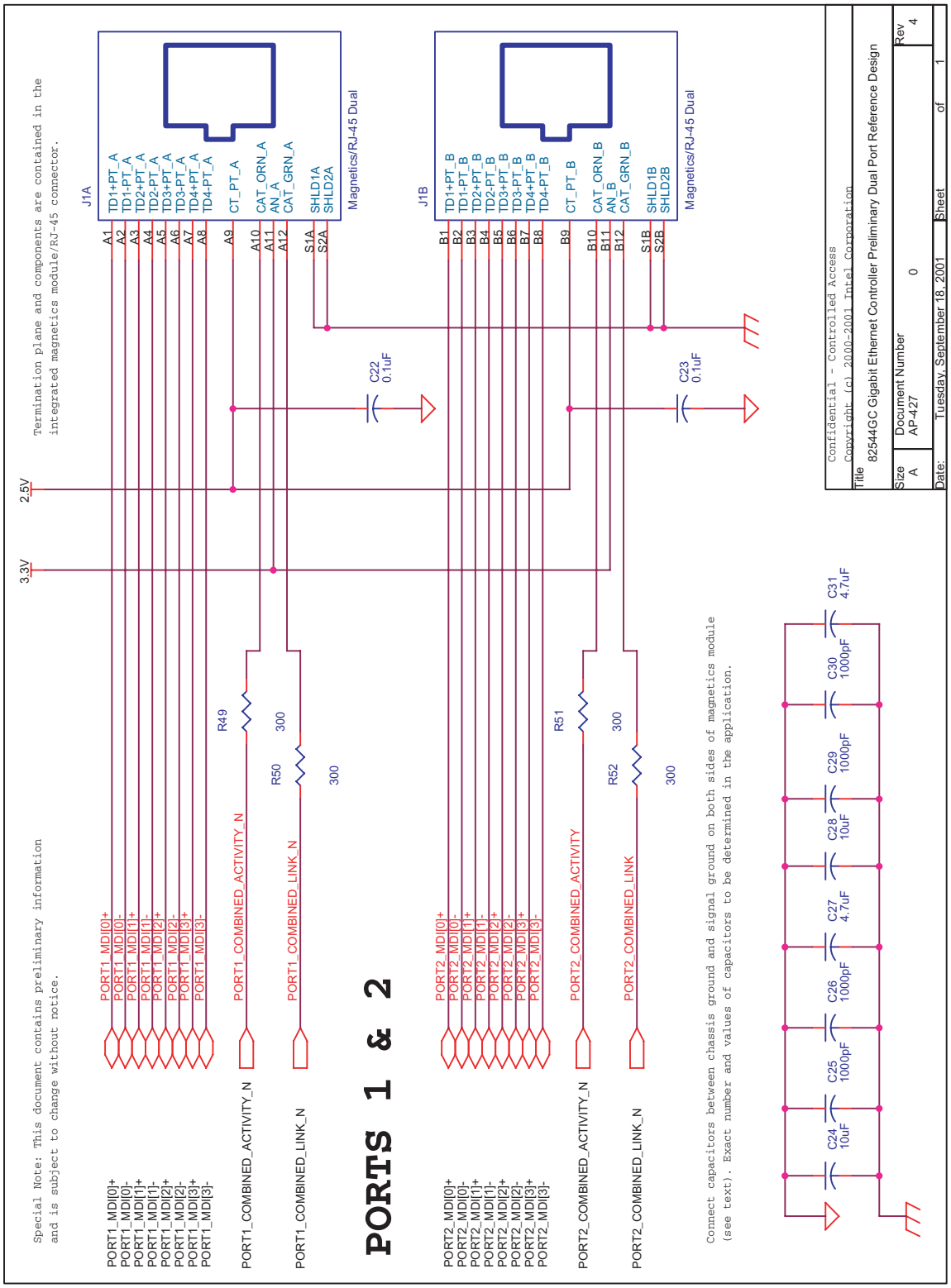
Special Note: This document contains preliminary information and is subject to change without notice.
Termination plane and components are contained in the integrated magnetics module/RJ-45 connector.
PORTS 1 & 2
J1A
J1B
Magnetics/RJ-45 Dual
3.3V
2.5V
R49
R50
R51
R52
300
C22 0.1uF
C23 0.1uF
C24 10uF
C25 1000pF
C26 1000pF
C27 4.7uF
C28 10uF
C29 1000pF
C30 1000pF
C31 4.7uF
Connect capacitors between chassis ground and signal ground on both sides of magnetics module (see text). Exact number and values of capacitors to be determined in the application.
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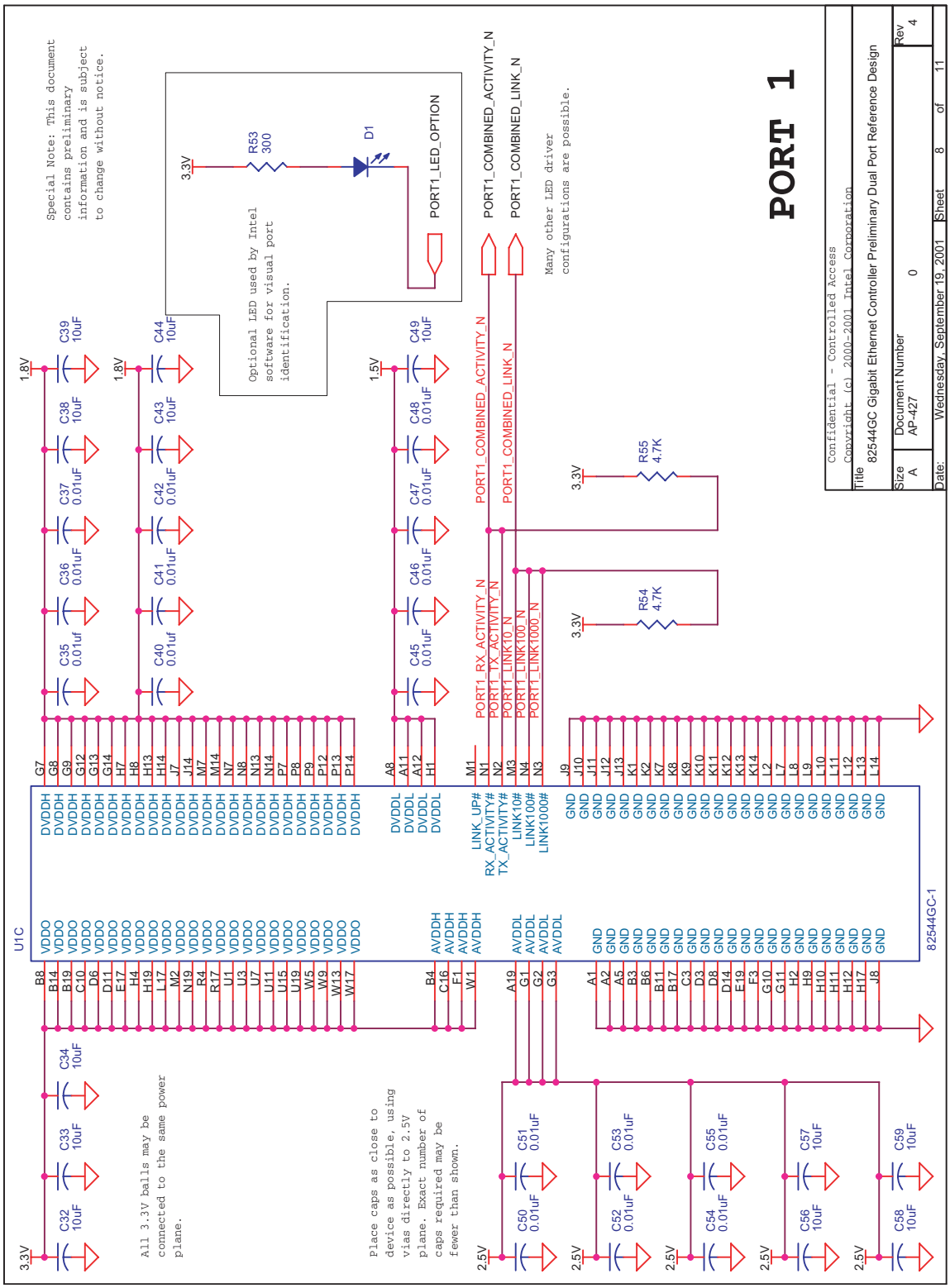
PORT 1
Special Note: This document contains preliminary information and is subject to change without notice.
Optional LED used by Intel software for visual port identification.
3.3V
R53 300
D1
PORT1_LED_OPTION
PORT1_COMBINED_ACTIVITY_N
PORT1_COMBINED_LINK_N
Many other LED driver configurations are possible.
U1C
82544GC-1
All 3.3V balls may be connected to the same power plane.
Place caps as close to device as possible, using vias directly to 2.5V plane. Exact number of caps required may be fewer than shown.
R55 4.7K
R54 4.7K
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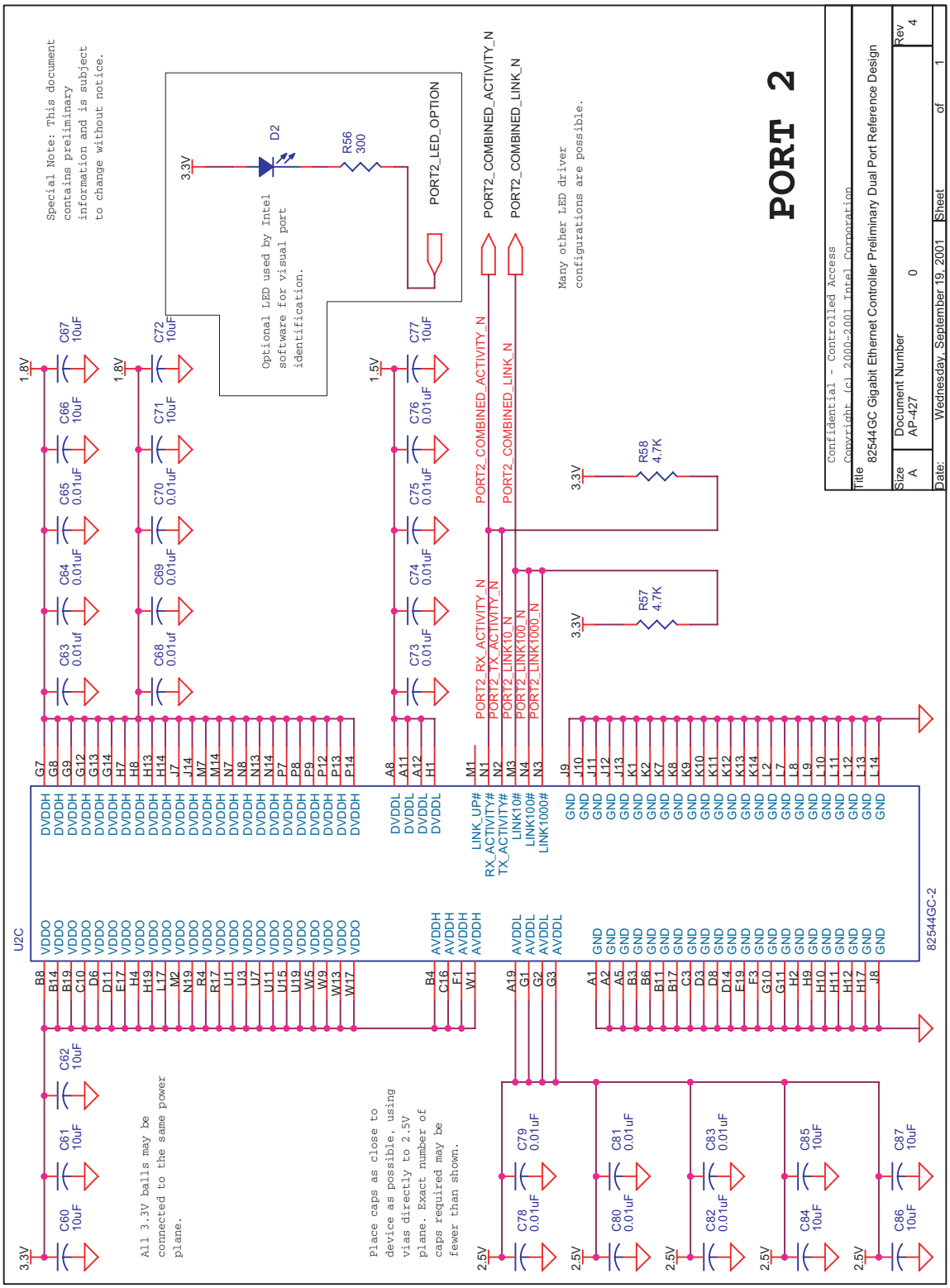
PORT 2
Special Note: This document contains preliminary information and is subject to change without notice.
Optional LED used by Intel software for visual port identification.
Many other LED driver configurations are possible.
All 3.3V balls may be connected to the same power plane.
Place caps as close to device as possible, using vias directly to 2.5V plane. Exact number of caps required may be fewer than shown.
PORT2_LED_OPTION
PORT2_COMBINED_ACTIVITY_N
PORT2_COMBINED_LINK_N
PORT2_COMBINED_ACTIVITY_N
PORT2_RX_ACTIVITY_N
PORT2_TX_ACTIVITY_N
PORT2_LINK10_N
PORT2_LINK100_N
PORT2_LINK1000_N
LINK_UP#
RX_ACTIVITY#
TX_ACTIVITY#
LINK10#
LINK100#
LINK1000#
U2C
82544GC-2
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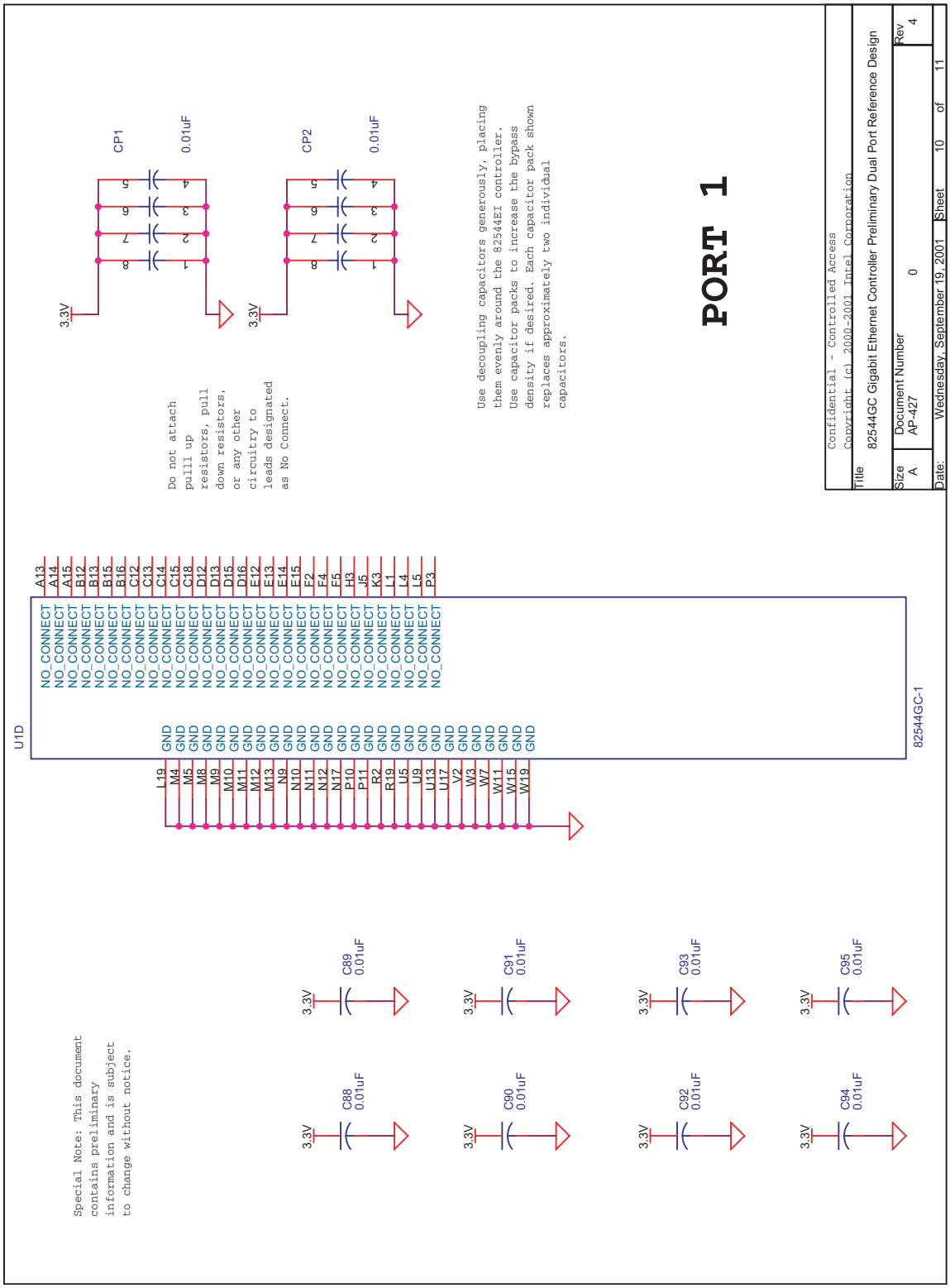
PORT 1
CP1
0.01uF
CP2
0.01uF
3.3V
Do not attach pull up resistors, pull down resistors, or any other circuitry to leads designated as No Connect.
Use decoupling capacitors generously, placing them evenly around the 82544EI controller. Use capacitor packs to increase the bypass density if desired. Each capacitor pack shown replaces approximately two individual capacitors.
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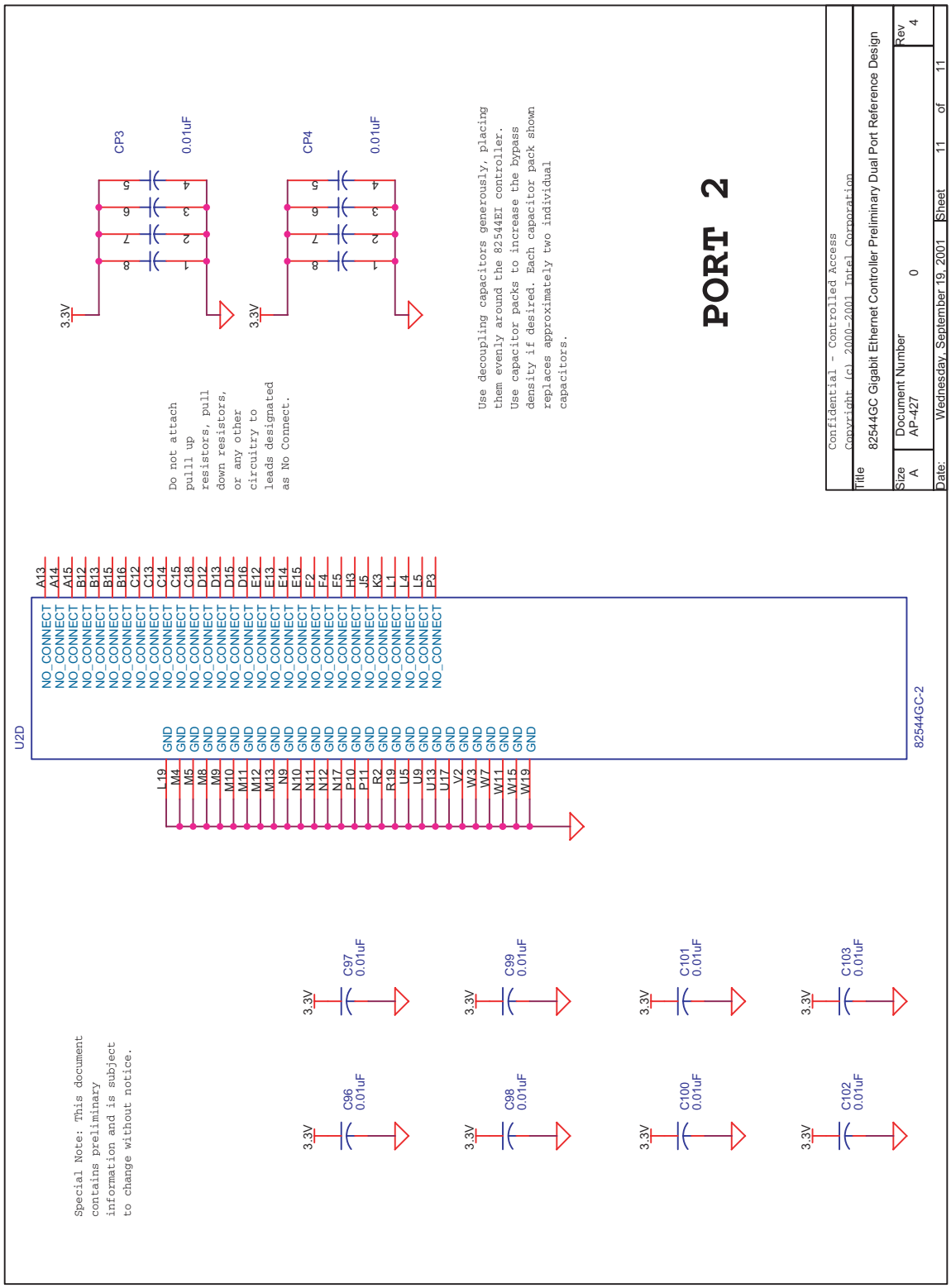
U1D
82544GC-1
NO_CONNECT
GND
C88 0.01uF
C89 0.01uF
C90 0.01uF
C91 0.01uF
C92 0.01uF
C93 0.01uF
C94 0.01uF
C95 0.01uF
Special Note: This document contains preliminary information and is subject to change without notice.


PORT 2
CP3
0.01uF
CP4
0.01uF
3.3V
Do not attach pull up resistors, pull down resistors, or any other circuitry to leads designated as No Connect.
Use decoupling capacitors generously, placing them evenly around the 82544EI controller. Use capacitor packs to increase the bypass density if desired. Each capacitor pack shown replaces approximately two individual capacitors.
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U2D
82544GC-2
NO_CONNECT
GND
C96 0.01uF
C97 0.01uF
C98 0.01uF
C99 0.01uF
C100 0.01uF
C101 0.01uF
C102 0.01uF
C103 0.01uF
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