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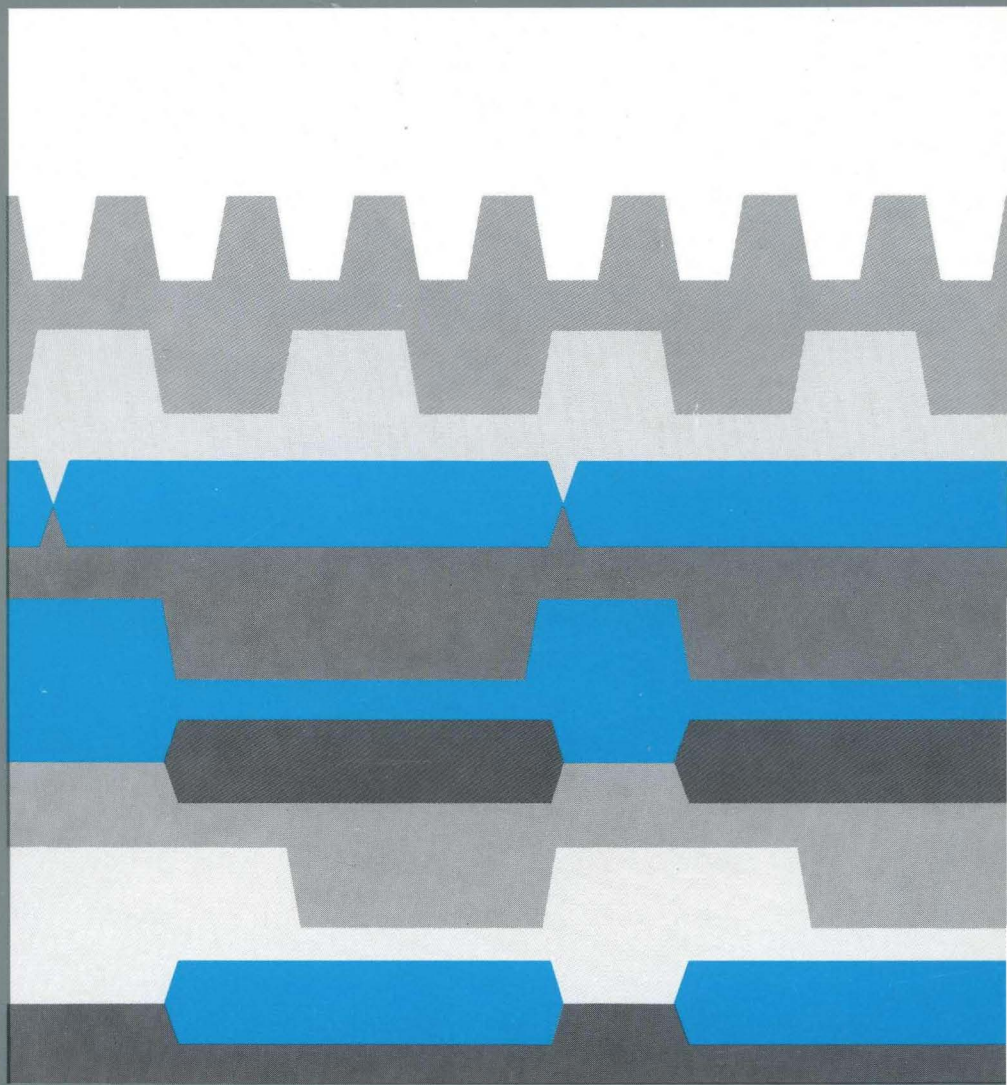
NONVOLATILE MEMORY DATA BOOK ADDENDUM



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Nonvolatile Memory Data Book Addendum

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Nonvolatile Memory Data Book Addendum
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Flash Memory

SECTION 2

2

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HN28F101 Series

1M (128K x 8-bit) Flash Memory

■ DESCRIPTION

The Hitachi HN28F101 is a 1-Megabit CMOS Flash Memory organized as 131,072 x 8-bit. The HN28F101 is capable of in-system electrical chip erasure and reprogramming.

The HN28F101 programs and erases data with a 12 V V_{PP} supply and a 5 V V_{CC} supply. The HN28F101 conforms to the JEDEC Standard Dual-Supply EEPROM Command Set. Its fast, high-reliability programming algorithm is initiated with Command Inputs. There are two methods of erasing the HN28F101: Manual and Automatic, both are initiated with Command Inputs.

The Manual Chip Erase method follows a fast, high-reliability erase algorithm. The Automatic Chip Erase function erases all data automatically without external control; Status Polling is used to inform the CPU of erase completion. Both erase methods provide a fast erase time without voltage stress to the device or deterioration in data reliability.

Hitachi's HN28F101 is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Plastic DIP and 32-lead PLCC, TSOP, and SOP packages. This allows an easy upgrade to the HN28F4001, 4 Megabit Flash Memory, as well as socket replacement with EPROMs and Mask ROMs. The HN28F101 TSOP package is offered in both standard and reverse bend pinouts.

■ FEATURES

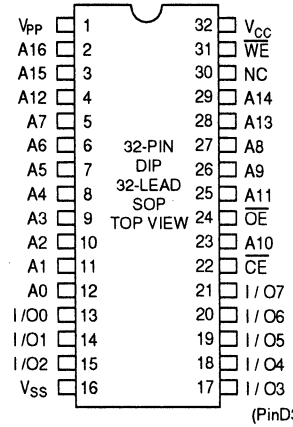
- Dual Power Supply:
  V_{CC} = 5 V ± 10%
  V_{PP} = 12.0 V ± 0.6 V (Erase/Program)
- Fast Access Times:
  120 ns/150 ns/200 ns (max)
- Low Power Dissipation:
  Read Current: 10 mA (typ)
  Standby Current: 20 µA (max)
- Byte Programming:
  Programming Time: 25 µs/Byte (typ)
  Address, Data, Control Latch Function
- Automatic Chip Erase Function:
  Erase Time: 1 sec (typ)
  Internal Pre-Write and Erase Verify
  Status Polling Function
- Erase Endurance:
  10,000 times (min)
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
  EPROM and Mask ROM Compatible
- Packages:
  32-pin Plastic DIP
  32-lead PLCC
  32-lead Plastic TSOP (Type I)
  32-lead Plastic SOP

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN28F101P-12	120 ns	32-pin Plastic DIP
HN28F101P-15	150 ns	(DP-32)
HN28F101P-20	200 ns	
HN28F101CP-12	120 ns	32-lead PLCC
HN28F101CP-15	150 ns	(CP-32)
HN28F101CP-20	200 ns	
HN28F101TD-12	120 ns	32-lead Plastic TSOP
HN28F101TD-15	150 ns	(TFP-32D)
HN28F101TD-20	200 ns	8 x 20 mm
HN28F101RD-12	120 ns	32-lead Plastic TSOP
HN28F101RD-15	150 ns	(TFP-32DR)
HN28F101RD-20	200 ns	8 x 20 mm
		Reverse bend
HN28F101T-12	120 ns	32-lead Plastic TSOP
HN28F101T-15	150 ns	(TFP-32DA)
HN28F101T-20	200 ns	8 x 14 mm
HN28F101R-12	120 ns	32-lead Plastic TSOP
HN28F101R-15	150 ns	(TFP-32DAR)
HN28F101R-20	200 ns	8 x 14 mm
		Reverse bend
HN28F101FP-12	120 ns	32-lead Plastic SOP
HN28F101FP-15	150 ns	(FP-32D)
HN28F101FP-20	200 ns	

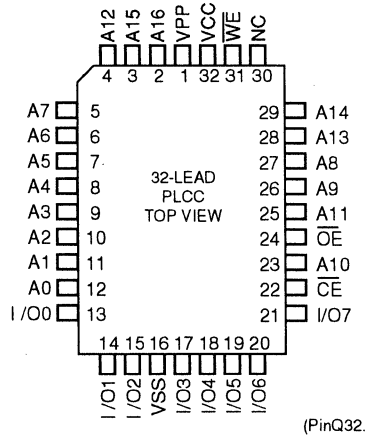
■ PIN ARRANGEMENT

HN28F101P Series
HN28F101FP Series



(PinD32.HN28F101)

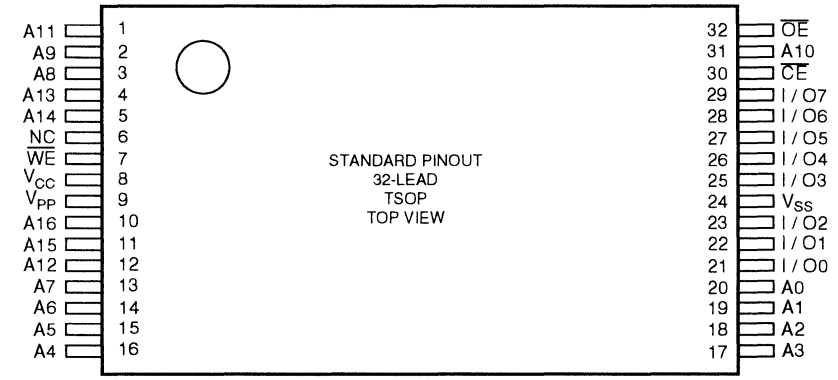
HN28F101CP Series



(PinQ32.HN28F101)

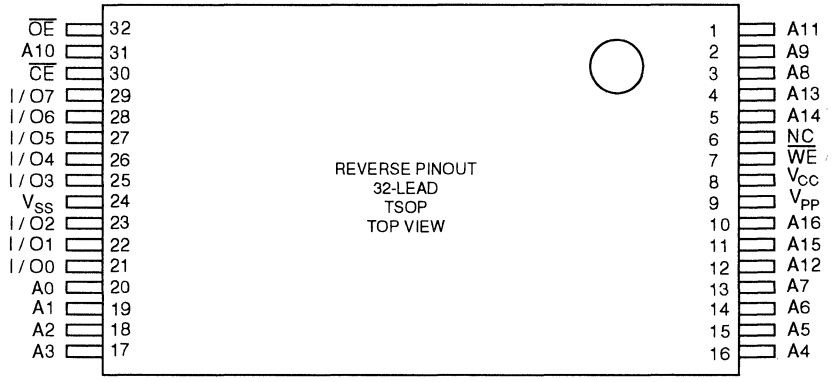
■ PIN ARRANGEMENT (continued)

HN28F101TD Series
HN28F101T Series



(PinT132.HN28F101T)

HN28F101RD Series
HN28F101R Series

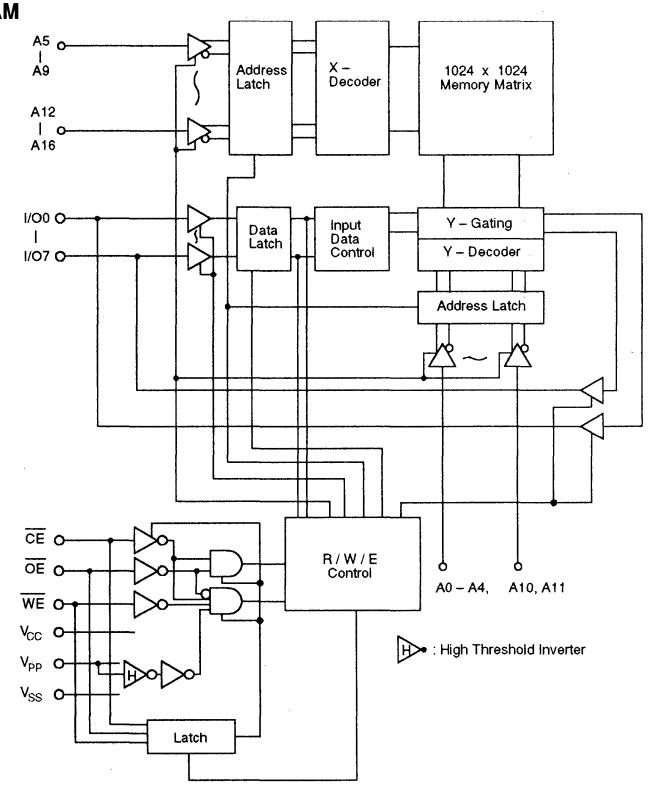


(PinT132.HN28F101R)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN28F101)

■ MODE SELECTION

Mode		V_{PP}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_9	I/O_0 to I/O_7
Read	Read	V_{CC} [6]	V_{IL}	V_{IL}	V_{IH}	A_9	D_{OUT}
	Output Disable	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X [6]	High-Z
	Standby	V_{CC}	V_{IH}	X	X	X	High-Z
	Identifier [1]	V_{CC}	V_{IL}	V_{IL}	V_{IH}	V_H [2]	ID
Command	Read [3,5]	V_{PP}	V_{IL}	V_{IL}	V_{IH}	A_9	D_{OUT}
	Output Disable	V_{PP}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
	Standby	V_{PP}	V_{IH}	X	X	X	High-Z
	Write[4]	V_{PP}	V_{IL}	V_{IH}	V_{IL}	A_9	D_{IN}

Notes:
1. Device Identifier Code can be output in Command Program Mode. Refer to Command Address and Data Input Table.
2. $11.4\ V \leq V_H \leq 12.6\ V$
3. Data can also be read when 12 V is applied to V_{PP}. Device Identifier Code can be output by Command Inputs. See Device Identifier Mode Description Table for more details.
4. Refer to Command Address and Data Input Table. Data is programmed, erased, or verified after inputting Commands.
5. Status of Automatic Erase can be verified in this mode by Status Polling on I/O_7. I/O_6 to I/O_6 are in high impedance states.
6. X = Don't Care. $V_{PP} = 0\ V$ to V_{CC}.

■ COMMAND ADDRESS AND DATA INPUT

Command	Bus Cycles Required	First Cycle			Second Cycle		
		Operation Mode [1]	Address [2]	Data [3]	Operation Mode [1]	Address [2]	Data [3]
Read [4]	1	Write	X	00H	Read	RA	D_{OUT}
Read Identifier Codes	2	Write	X	90H	Read	IA	ID
Set-up Erase/Erase [5]	2	Write	X	20H	Write	X	20H
Erase Verify	2	Write	EVA	A0H	Read	X	EVD
Setup Auto Erase/Auto Erase [6]	2	Write	X	30H	Write	X	30H
Setup Program/Program [7]	2	Write	X	40H	Write	PA	PD
Program Verify [7]	2	Write	X	C0H	Read	X	PVD
Reset	2	Write	X	FFH	Write	X	FFH

Notes:
1. Refer to Command Program Mode in Mode Selection about operation mode.
2. Refer to Device Identifier Mode. IA = Identifier Address, PA = Programming Address, EVA = Erase Verify Address, RA = Read Address.
3. Refer to Device Identifier Mode. PA are latched by Programming Command. ID = Identifier Output Code, PD = Programming Data, PVD = Programming Verify Output Data, EVD = Erase Verify Output Data.
4. Command latch default value when applying 12 V to V_{PP} is "00H". Device is in Read Mode after V_{PP} is set to 12 V (before other Command is input).
5. All data in the chip is erased. Erase data according to the Manual Chip Erase Flowchart.
6. All data in the chip is erased. Data is automatically programmed to 00H and erased automatically by internal logic circuitry. External Manual Erase Verify is not necessary. Erasure completion is verified by Status Polling on I/O_7.
7. Program data according to the Programming Flowchart.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +14	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-10 to +80	°C

Notes:
1. Relative to V_{SS}.
2. V_{IN} and V_{OUT} = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.

■ CAPACITANCE (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to 70°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{CC} - 1 to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC1}	-	6	15	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	10	30	mA	I_{OUT} = 0 mA, f = 8 MHz
Standby V_{CC} Current	I_{SB1}	-	-	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	-	-	20	µA	$\overline{CE}$ = V_{CC}
V_{PP} Current	I_{PP1}	-	-	20	µA	V_{PP} = 5.5 V
Input Voltage [3]	V_{IL}	-0.3[1]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 0.3[2]	V	
Output Voltage	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes:
1. V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns. If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.
3. Only defined for DC and long cycle function test. V_{IL} max = 0.45 V, V_{IH} min = 2.4 V for AC function test.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

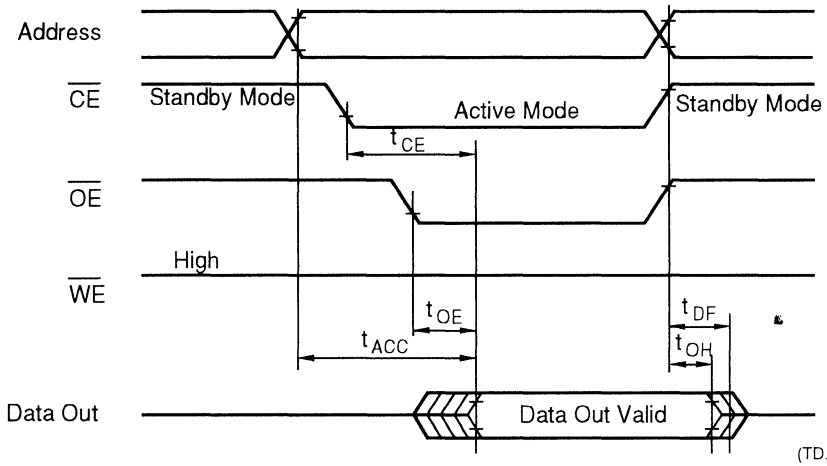
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	HN28F101-12		HN28F101-15		HN28F101-20		Test Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	120	-	150	-	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	120	-	150	-	200	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	60	-	70	-	80	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	40	0	50	0	60	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN28F101)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 V ± 0.6 V, T_a = 0 to 70°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current		I_{LI}	-	-	2	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current		I_{LO}	-	-	2	µA	V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	Read	I_{CC1}	-	6	15	mA	I_{OUT} = 0 mA, f = 1 MHz
		I_{CC2}	-	10	30	mA	I_{OUT} = 0 mA, f = 8 MHz
	Program	I_{CC3}	-	2	10	mA	
	Erase	I_{CC4}	-	10	40	mA	Automatic Erase
		I_{CC5}	-	5	15	mA	Manual Erase
Standby V_{CC} Current		I_{SB1}	-	-	1	mA	$\overline{CE}$ = V_{IH}
		I_{SB2}	-	-	200	µA	$\overline{CE}$ = V_{CC}
V_{PP} Current	Read	I_{PP1}	-	-	1	mA	V_{PP} = 12.6 V
	Program	I_{PP2}	-	5	30	mA	Programming
	Erase	I_{PP3}	-	35	80	mA	Automatic Erase
		I_{PP4}	-	10	30	mA	Manual Erase
Input Voltage [3]		V_{IL}	-0.3[4]	-	0.8	V	
		V_{IH}	2.2	-	V_{CC} + 0.3[5]	V	
Output Voltage		V_{OL}	-	-	0.45	V	I_{OH} = 2.1A
		V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}, or V_{CC} and V_{PP} must be applied simultaneously.
2. V_{PP} must not exceed 14 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12 V.
4. V_{IL} min = -1.0 V for pulse width ≤ 20 ns.
5. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 v ± 0.6 V, T_a = 0 to 70°C)

Test Conditions

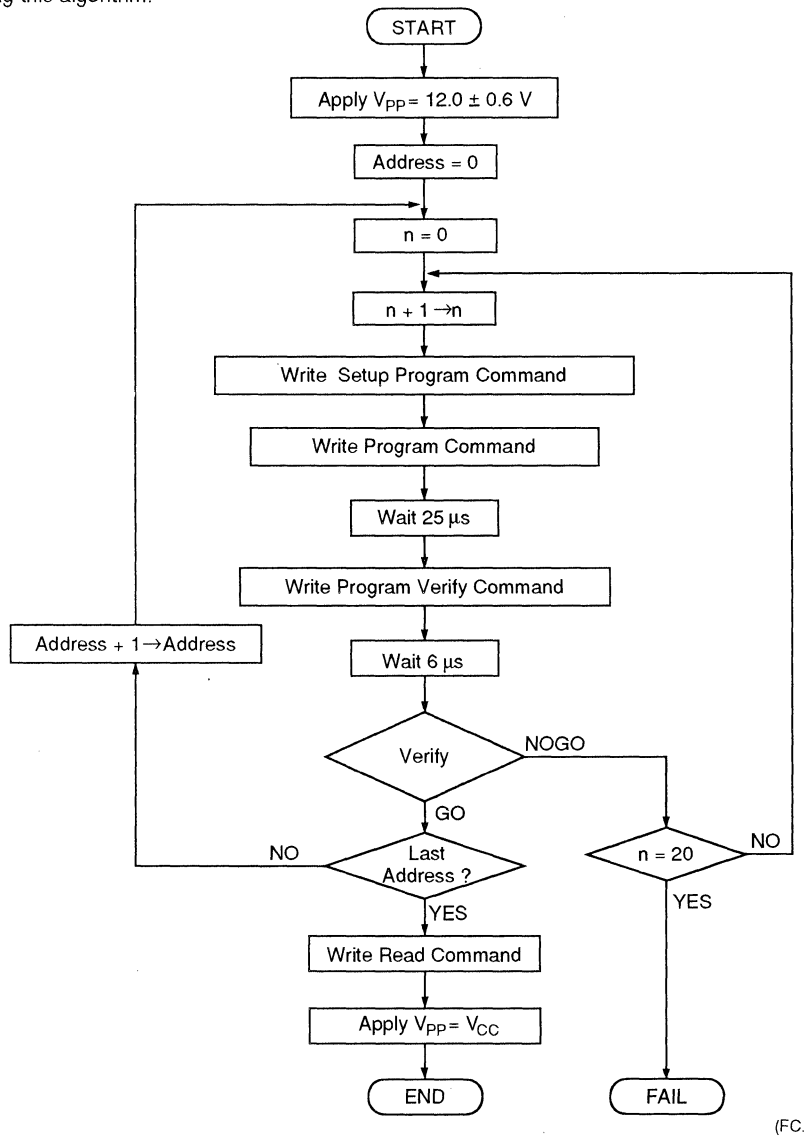
- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	HN28F101-12		HN28F101-15		HN28F101-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Programming Cycle Time	t_{CWC}	120	-	150	-	200	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Address Hold Time	t_{AH}	60	-	60	-	60	-	ns
Data Setup Time	t_{DS}	50	-	50	-	50	-	ns
Data Hold Time	t_{DH}	10	-	10	-	10	-	ns
Chip Enable Setup Time	t_{CES}	0	-	0	-	0	-	ns
Chip Enable Hold Time	t_{CEH}	50	-	50	-	50	-	ns
V_{PP} Setup Time	t_{VPS}	100	-	100	-	100	-	ns
V_{PP} Hold Time	t_{VPH}	100	-	100	-	100	-	ns
Write Enable Pulse Width	t_{WEP}	70	-	70	-	80	-	ns
Write Enable High Time	t_{WEH}	40	-	40	-	40	-	ns
Output Enable Setup Time Before Command Prog.	t_{OEWS}	0	-	0	-	0	-	ns
Output Enable Setup Time Before Verify	t_{OERS}	6	-	6	-	6	-	µs
Verify Access Time	t_{VA}	-	120	-	150	-	150	ns
Output Enable Setup Time Before Status Polling	t_{OEPS}	120	-	120	-	120	-	ns
Status Polling Access Time	t_{SPA}	-	120	-	150	-	200	ns
Standby Time Before Prog.	t_{PPW}	25	-	25	-	25	-	µs
Erase Standby Time	t_{ET}	9	11	9	11	9	11	ms
Output Disable Time	t_{DF}	0	40	0	50	0	60	ns
Automatic Erase Time	t_{AET}	-	30	-	30	-	30	s

Notes:
1. $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ must be fixed high during V_{PP} transition from 5 V to 12 V or from 12 V to 5 V.
2. Except for sending a Command Program, a Read operation at V_{PP} = 12 V is similar to a Read operation at V_{PP} = V_{CC}.
3. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.
4. Addresses are taken in on the falling edge of the Write Enable pulse and latched on the rising edge of the Write Enable pulse during Chip Enable low. Data is latched on the rising edge of the Write Enable pulse during Chip Enable low.

■ PROGRAMMING FLOWCHART

The HN28F101 can be programmed with the fast, high-reliability programming algorithm shown in the following flowchart. This algorithm provides faster programming time without voltage stress to the device or deterioration in reliability of programmed data. Random transition of $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ are not permitted when executing this algorithm.



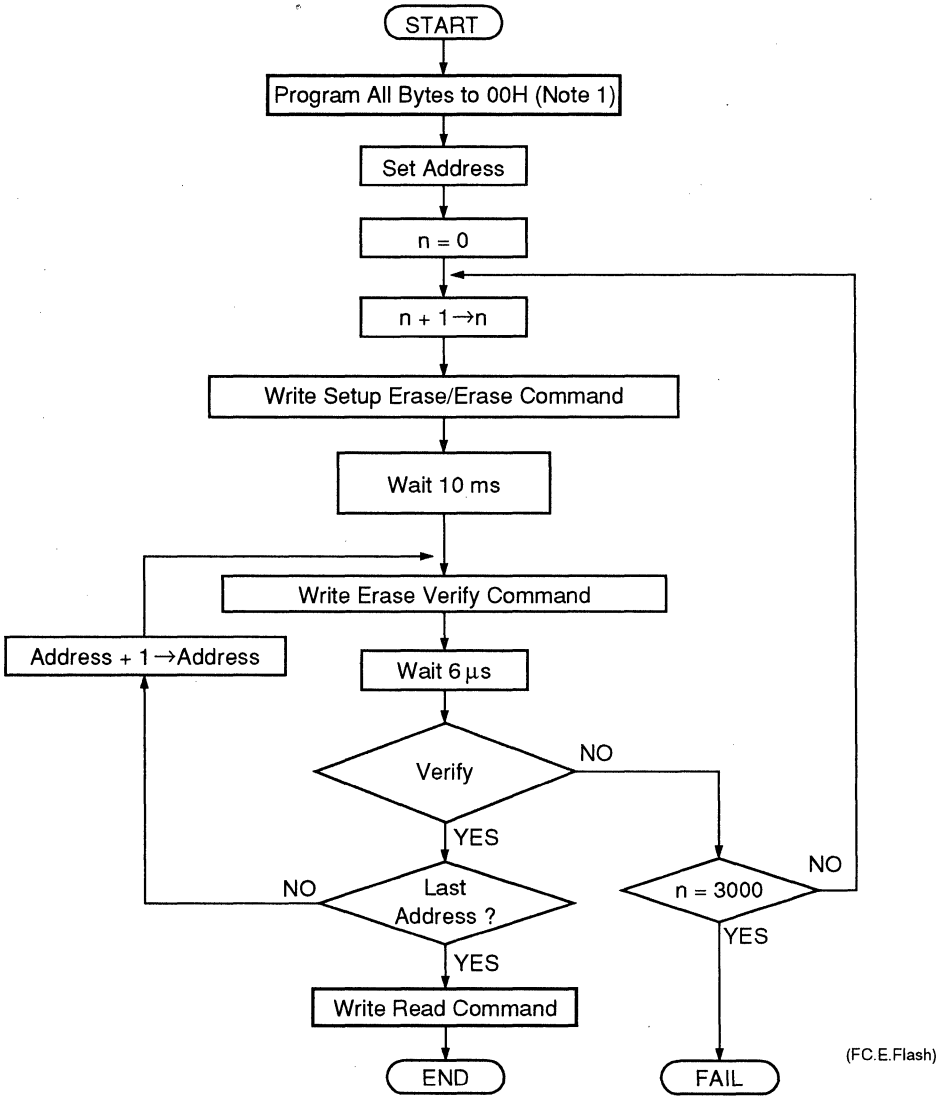
(FC.P.Flash)

Note: In the case of programming two or more HN28F101 devices simultaneously, the following steps should be applied to the verified devices to avoid over programming:

1. Set-up Program Command: Write FFH
2. Program Command: Write FFH
3. Program Verify Command: Write 00H
4. Program Verify Address: Read Address

■ MANUAL CHIP ERASE FLOWCHART

The HN28F101 can be erased with the fast, high-reliability erase algorithm shown in the following flowchart. This algorithm provides a fast erase time without voltage stress to the device or deterioration in reliability of programmed data. Random transition of $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ are not permitted when executing this algorithm.

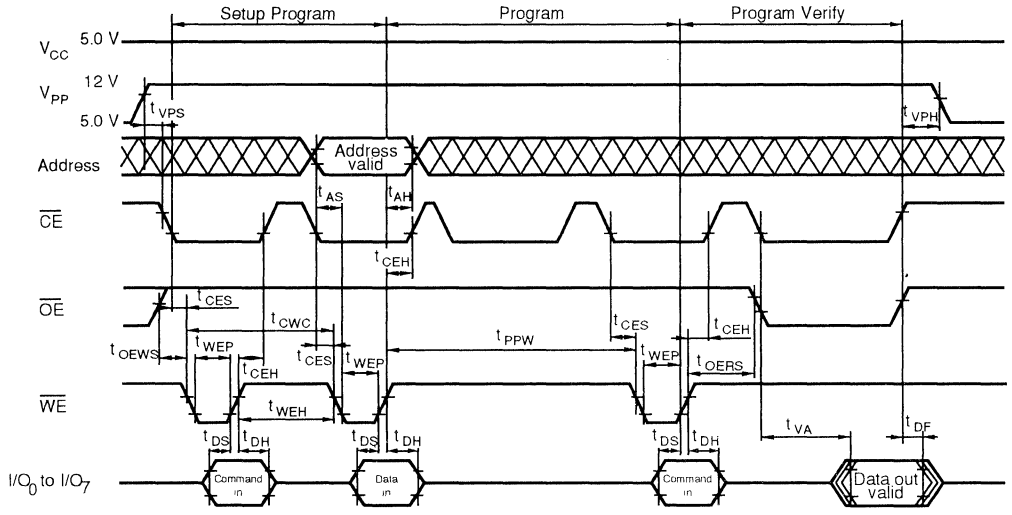


Note 1: Refer to Fast High-Reliability Programming Flowchart.

Note: In the case of erasing two or more HN28F101 devices simultaneously, the following steps should be applied to the verified devices to avoid over erasing:

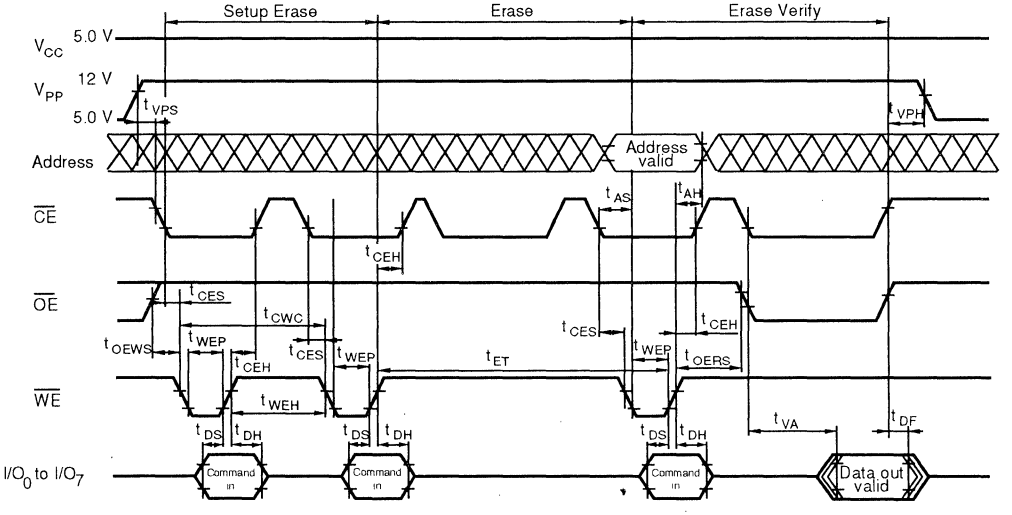
1. Set-up Erase Command: Write A0H
2. Erase Verify Address: Verify Address
3. Erase Command: Write A0H
4. EraseVerify Command: Write A0H

■ PROGRAMMING TIMING WAVEFORM



(TD.P.HN28F101)

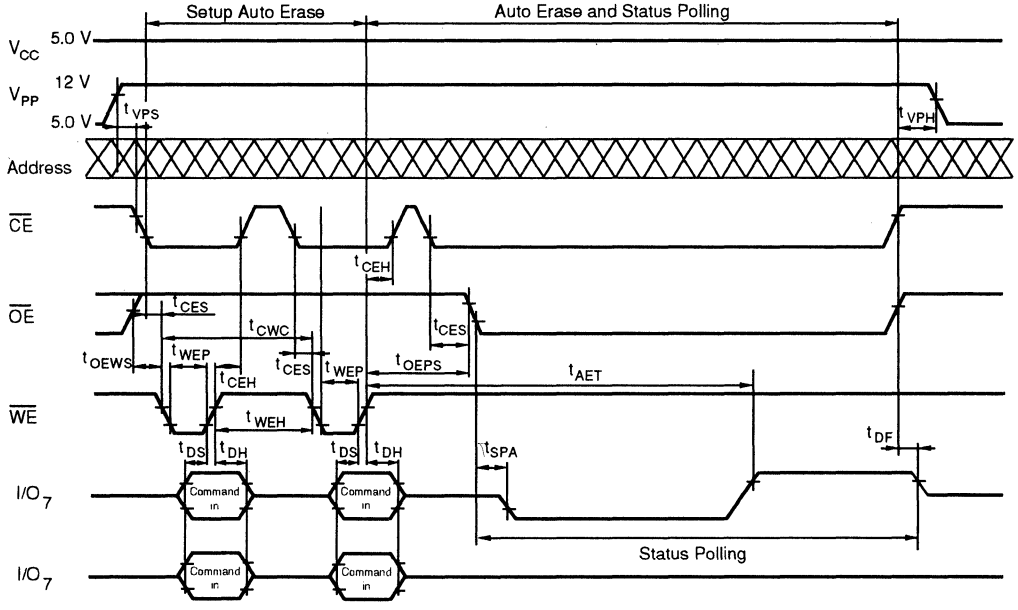
■ MANUAL CHIP ERASE TIMING WAVEFORM



(TD.E.HN28F101)

■ AUTOMATIC CHIP ERASE TIMING WAVEFORM

The fast Automatic Erase algorithm shown in the following timing waveform can be applied. All of the data in the chip is erased. External pre-write and erae verify are not required because the cells are pre-written, erased and verified automatically by internal control circuitry. Erasure completion can be verified by Status Polling after the Automatic Erase starts. Erasure completion can be verified by Status Polling. This algorithm provides a fast erase time without any voltage stress to the device or deterioration in data reliability.



(TD.AE.HN28F101)

■ STATUS POLLING

The HN28F101 features Status Polling as a method to indicate that the embedded algorithms are either in progress or completed. While the Automatic Chip Erase algorithm is in operation, the I/O_7 pin is lowered to V_{OL} until the erase operation is completed. Upon completion of the erase operation, the I/O_7 pin is set to V_{OH}. The Status Polling feature is only active during the Automatic Chip Erase algorithm.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

■ HN28F101 SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	0	1	1	0	0	1	19

Notes: The HN28F101 Series Identifier Codes can be read by two methods:

1. Write 90H to the device with $\overline{CE} = V_{IL}$ and $A_0 = \overline{OE} = V_{IH}$ (all other addresses are Don't Care). The Device Code of 19H will appear after the fall of OE. The Manufacturer Code of 07H will appear after A_0 transitions to V_{IL}.
2. Apply 12.0 V ± 0.6 V to A_0. With $A_0 = V_{IH}$ (all other addresses are LOW), $V_{PP} = V_{CC}$, $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{WE} = V_{IH}$. The Device Code of 19H will appear. After A_0 transitions to V_{IL} the Manufacturer Code of 07H will appear on the I/O lines.

4M (512K x 8-bit) Flash Memory

■ DESCRIPTION

The Hitachi HN28F4001 is a 4-Megabit CMOS Flash Memory organized as 524,288 x 8-bit. The HN28F4001 is capable of in-system electrical chip and block erasure and reprogramming.

The HN28F4001 programs and erases data with a 12 V V_{PP} supply and a 5 V V_{CC} supply. The HN28F4001 conforms to the JEDEC Standard Dual-Supply EEPROM Command Set. Its Automatic Commands do not require complicated external control to program or erase data because of its automatic verify programming, chip erase and block erase functions.

The block architecture of the HN28F4001 segments the device into 32 blocks of 16KBytes each. This feature allows the user to erase and reprogram one random block of data and more than one block of data simultaneously.

Hitachi's HN28F4001 is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-lead SOP and TSOP packages. This allows an easy upgrade from the HN28F101, 1 Megabit Flash Memory, as well as socket replacement with Mask ROMs. The HN28F4001 TSOP is offered in both standard and reverse bend pinouts.

■ FEATURES

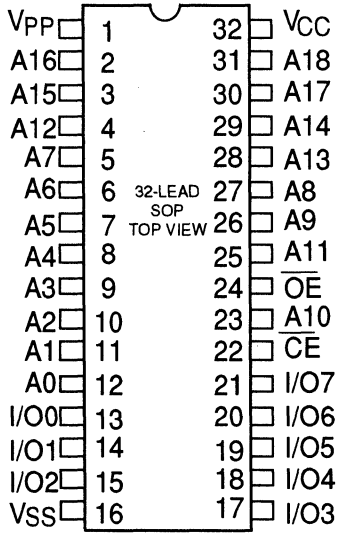
- Dual Power Supply:
  V_{CC} = 5 V ± 10%
  V_{PP} = 12.0 V ± 0.6 V (Erase/Program)
- Fast Access Times:
  150 ns/170 ns (max)
- Low Power Dissipation:
  Read Current: 15 mA (typ)
  Standby Current: 1 µA (typ)
- Automatic Byte Programming:
  Programming Time: 40 µs/Byte (typ)
  Address, Data, Control Latch Function
  Internal Automatic Program Verify
  Data Polling Function
- Automatic Chip and Block Erase:
  Erase Time: 4 sec (typ)
  Internal Pre-Write and Erase Verify
  Status Polling Function
- Block Architecture:
  Block Size: 16KBytes x 32 Blocks
  Simultaneous Erase of Multiple Blocks
- Erase Endurance:
  10,000 times (min)
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
  Mask ROM Compatible
- Packages:
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type I)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN28F4001FP-15	150 ns	32-lead Plastic SOP
HN28F4001FP-17	170 ns	(FP-32D)
HN28F4001T-15	150 ns	32-lead Plastic TSOP
HN28F4001T-17	170 ns	(TFP-32D)
HN28F4001R-15	150 ns	32-lead Plastic TSOP
HN28F4001R-17	150 ns	(TFP-32DR)
		Reverse bend

■ PIN ARRANGEMENT

HN28F4001FP Series



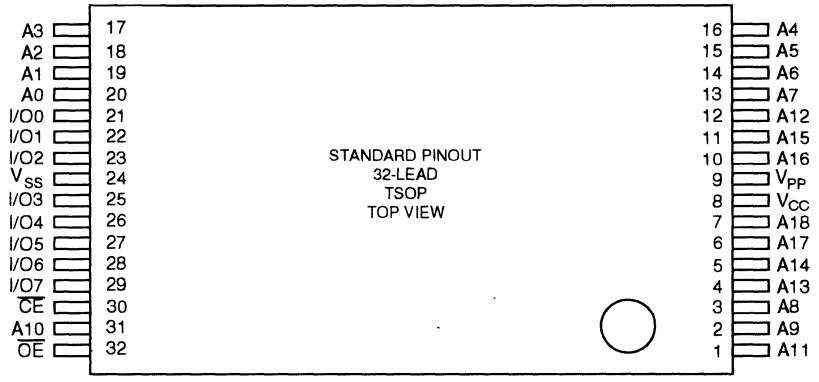
(PinD32.HN28F4001)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground

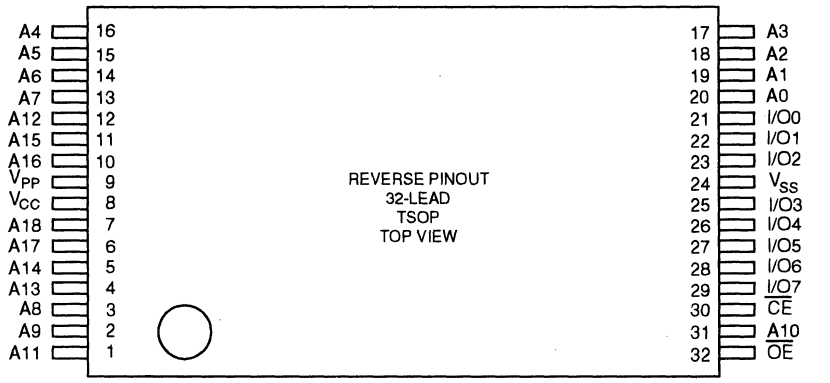
■ PIN ARRANGEMENT (continued)

HN28F4001T Series



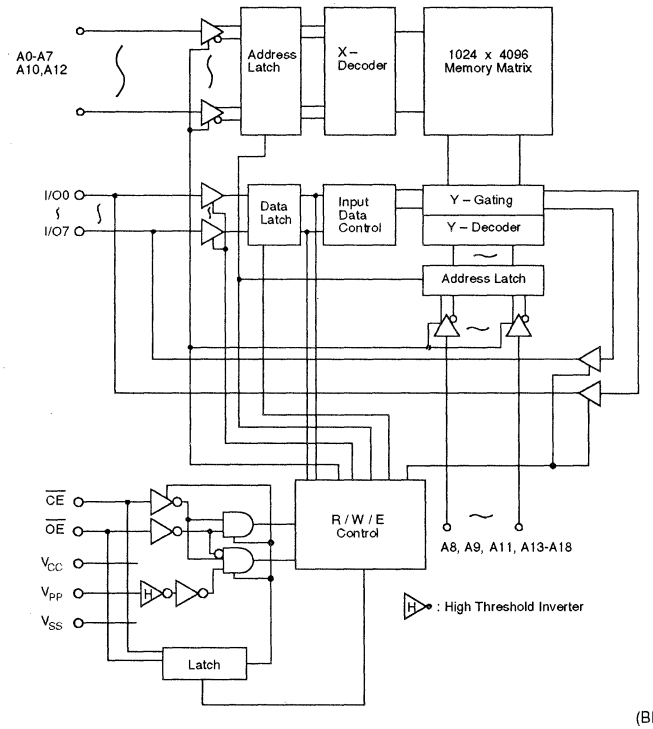
(PinT132.HN28F4001T)

HN28F4001R Series



(PinT132.HN28F4001R)

■ BLOCK DIAGRAM



(BD.HN28F4001)

■ MODE SELECTION

Mode		$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	I/O_0 to I/O_7
Read	Read	V_{IL}	V_{IL}	A_9	A_0	V_{SS} to V_{cc} [6]	D_{OUT}
	Output Disable	V_{IL}	V_{IH}	X	X	V_{SS} to V_{cc}	High-Z
	Standby	V_{IH}	X	X	X	V_{SS} to V_{cc}	High-Z
	Identifier [1]	V_{IL}	V_{IL}	V_H [2]	V_{IL}	V_{SS} to V_{cc}	Code"07"
		V_{IL}	V_{IL}	V_H [2]	V_{IH}	V_{SS} to V_{cc}	Code"80"
Command	Read [3,5]	V_{IL}	V_{IL}	A_9	A_0	V_{PP}	D_{OUT}
Program	Standby	V_{IH}	X	X	X	V_{PP}	High-Z
	Write [4]	V_{IL}	V_{IH}	A_9	A_0	V_{PP}	D_{IN}

Notes:
1. Device Identifier Code can be output in Command Program Mode. Refer to Command Address and Data Input Table.
2. $11.4\ V \leq V_H \leq 12.6\ V$
3. Data can also be read when 12 V is applied to V_{PP}. Device Identifier Code can be output by Command Inputs. See Device Identifier Mode Description Table for more details.
4. Refer to Command Address and Data Input Table. Data is programmed, erased, or verified after inputting Commands.
5. Status of Programming and Erase can be verified in this mode. Status Outputs on I/O_7. I/O_0 to I/O_6 are in high impedance states.
6. X = Don't Care. $V_{PP} = 0V$ to V_{CC}.

■ COMMAND ADDRESS AND DATA INPUT

Command	Bus Cycles Required	First Cycle			Second Cycle		
		Operation Mode [1]	Address [2]	Data [3]	Operation Mode [1]	Address [2]	Data [3]
Read (Memory) [4]	1	Write	X	00H	Read	RA	D_{OUT}
Read Identifier Codes	2	Write	X	90H	Read	IA	ID
Set-up Chip Erase/ Chip Erase [5]	2	Write	X	20H	Write	X	20H
Set-up Block Erase/ Block Erase [8]	2	Write	X	60H	Write	BA	60H
Erase Verify [5]	2	Write	EVA	A0H	Read	X	EVD
Setup Auto Chip Erase/ Auto Chip Erase [6]	2	Write	X	30H	Write	X	30H
Setup Auto Block Erase/ Auto Block Erase [9]	2	Write	X	20H	Write	BA	D0H
Setup Program/Program [7]	2	Write	X	40H	Write	PA	PD
Program Verify [7]	2	Write	PA	C0H	Read	X	PVD
Setup Auto Program/ Auto Program [10]	2	Write	X	10H	Write	PA	PD
Reset	1 or 2	Write	X	FFH	Write[11]	X	FFH[11]

Notes:
1. Refer to Command Program Mode in Mode Selection about operation mode.
2. Refer to Device Identifier Mode. IA = Identifier Address, PA = Programming Address, EVA = Erase Verify Address, RA = Read Address, BA = Block Address. Addresses are latched on the rising edge of chip-enable pulse.
3. Refer to Device Identifier Mode. PA are latched by Programming Command. ID = Identifier Output Code, PD = Programming Data, PVD = Programming Verify Output Data, EVD = Erase Verify Output Data.
4. Command latch default value when applying 12 V to V_{PP} is "00H". Device is in Read Mode after V_{PP} is set to 12 V (before other Command is input).
5. All data in the chip is erased. Erase data according to the Manual Chip Erase Flowchart.
6. All data in the chip is erased. Data is automatically programmed to 00H and erased by internal logic circuitry. External Manual Erase Verify is not required. Erasure completion must be verified by Status Polling on I/O_7.
7. Program data according to the Manual Programming Flowchart.
8. Block data indicated by BA is erased. Erase data according to the Manual Block Erase Flowchart.
9. Block data indicated by BA is erased. Data is automatically programmed to 00H and erased by internal logic circuitry. External Manual Erase Verify is not required. Erasure completion must be verified by Status Polling on I/O_7.
10. One Byte of data is programmed. Data is programmed automatically by internal logic circuit. External program verify is not required. Program completion must be verified by Data Polling on I/O_7.
11. Write Reset Command twice to exit from program setup state or auto verify program setup state. Write it once to exit from others. The Reset Command is not valid during the following:
    (1) Standby time (t_{ET}) during Manual Erase.
    (2) Erase time (t_{AETC}, t_{AETB}) during Automatic Erase.
    (3) Programming time (t_{AVT}) after inputting setup command (10H) in Auto Verify Programming.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +14.0	V
A_9 Voltage [1,2]	V_{ID}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-65 to +125	°C
Storage Temperature Under Bias	T_{BIAS}	-10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT} and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{IN}	-	4	6	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}	-	10	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = V_{SS} to V_{CC}
Operating V_{CC} Current	I_{CC1}	-	3	30	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	15	50	mA	I_{OUT} = 0 mA, f = 6.7 MHz
Standby V_{CC} Current	I_{SB1}	-	0.2	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	-	1	20	µA	$\overline{CE}$ = V_{CC} ± 0.3V
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage [3]	V_{IL}	-0.5 [1]	-	0.8 [3]	V	
	V_{IH}	2.2 [3]	-	V_{CC} + 0.5 [2]	V	
Output Voltage	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns. V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns. If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.
3. Only defined for DC and long cycle function test. V_{IL} max = 0.4 and V_{IH} min = 3.0 V for AC function test.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

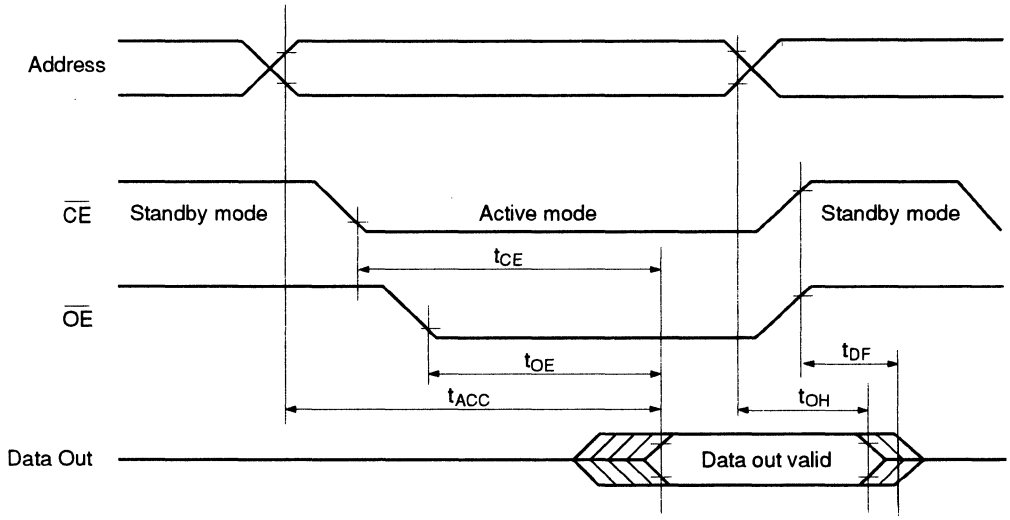
Test Conditions

- Input pulse levels: 0.4 V / 3.0 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN28F4001-15		HN28F4001-17		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	150	-	170	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	150	-	170	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	70	-	70	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z[1]	t_{DF}	0	50	0	60	ns	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



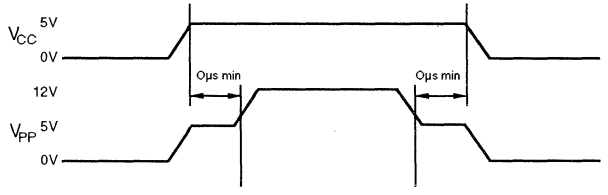
(TD.R.HN28F4001)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 V ± 0.6 V, T_a = 0 to +70°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current		I_{LI}	-	-	2	µA	$V_{IN} = V_{SS}$ to V_{CC}
Output Leakage Current		I_{LO}	-	-	2	µA	$V_{OUT} = V_{SS}$ to V_{CC}
Operating V_{CC} Current	Read	I_{CC1}	-	3	30	mA	I_{OUT} = 0 mA, f = 1 MHz
		I_{CC2}	-	15	50	mA	I_{OUT} = 0 mA, f = 6.7 MHz
	Program	I_{CC3}	-	7	30	mA	Programming
	Erase	I_{CC4}	-	15	30	mA	Erasing
	Program Verify	I_{CC5}	-	3	15	mA	Programming Verify
	Erase Verify	I_{CC6}	-	3	15	mA	Erase Verify
Standby V_{CC} Current		I_{SB1}	-	0.3	1	mA	$\overline{CE} = V_{IH}$
		I_{SB2}	-	40	200	µA	$\overline{CE} = V_{CC} \pm 0.3$ V
V_{PP} Current	Read	I_{PP1}	-	80	200	µA	V_{PP} = 12.6 V
	Program	I_{PP2}	-	13	50	mA	Programming
	Erase	I_{PP3}	-	40	80	mA	Automatic Erase
	Program Verify	I_{PP4}	-	1	10	mA	Programming Verify
	Erase Verify	I_{CC5}	-	0.5	10	mA	Erase Verify
Input Voltage		V_{IL}	-0.5 [5]	-	0.8 [7]	V	
		V_{IH}	2.2 [7]	-	V_{CC} + 0.5 [6]	V	
Output Voltage		V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA
		V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{CC}/V_{PP} power on/off timing: V_{CC} must be applied before or simultaneously with V_{PP}, and removed after or simultaneously with V_{PP}. These conditions must be satisfied at power on and off caused by power failure to the device.



2. V_{PP} must not exceed 14 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12 V.
4. When $\overline{CE} = V_{IL}$, do not change V_{PP} from V_{IL} to 12 V or 12 V to V_{IL}.
5. V_{IL} min = -1.0 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed. Read operation can not be guaranteed.
7. Only defined for DC and long cycle function test. V_{IL} max = 0.4 and V_{IH} min = 3.0 V for AC function test.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 V ± 0.6 V, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0V

Item	Symbol	HN28F4001-15		HN28F4001-17		Unit	Test Condition
		Min.	Max.	Min.	Max.		
V_{PP} Setup Time	t_{VPS}	100	-	100	-	ns	
Output Enable Setup Time	t_{OES}	100	-	100	-	ns	
$\overline{OE}$ / $\overline{CE}$ Setup Time after Command Write	t_{OESA} t_{CESA}	6 6	- -	6 6	- -	µs µs	
Chip Enable Hold Time	t_{CEH}	60	-	60	-	ns	
Chip Enable Pulse Width	t_{CEP}	60	-	60	-	ns	
Address Setup Time	t_{AS}	50	-	50	-	ns	
Address Hold Time	t_{AH}	20	-	20	-	ns	
Data Setup Time	t_{DS}	50	-	50	-	ns	
Data Hold Time	t_{DH}	20	-	20	-	ns	
$\overline{CE}$ / $\overline{OE}$ Setup Time before Status Polling	t_{CESP} t_{OESP}	120 120	- -	120 120	- -	ns ns	
$\overline{CE}$ / $\overline{OE}$ Setup Time before Command Write	t_{CESC} t_{OESC}	100 100	- -	100 100	- -	ns ns	
$\overline{CE}$ / $\overline{OE}$ Setup Time before Verify	t_{CESV} t_{OESV}	6 6	- -	6 6	- -	µs µs	
$\overline{CE}$ to Output Delay in Verify	t_{CEV}	-	300	-	300	ns	$\overline{OE}$ = V_{IL}
V_{PP} Hold Time	t_{VPH}	100	-	100	-	ns	
Total Auto Chip Erase Time	t_{AETC}	-	30	-	30	s	
Total Auto Block Erase Time	t_{AETB}	-	30	-	30	s	
Total Auto Verify Programming Time	t_{AVT}	10	2000	10	2000	µs	
Standby Time Before Programming	t_{PPW}	25	-	25	-	µs	
Erase Standby Time	t_{ET}	0.95	-	0.95	-	ms	
Block Address Load Cycle	t_{BALC}	0.12	3	0.12	3	µs	
Block Address Load Time	t_{BAL}	10	-	10	-	µs	

Notes:
1. $\overline{CE}$ and $\overline{OE}$ must be fixed high during V_{PP} transition from 5 V to 12 V or from 12 V to 5 V.
2. Except for sending a Command Program, a Read operation at V_{PP} = 12 V is similar to a Read operation at V_{PP} = V_{CC}.
3. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

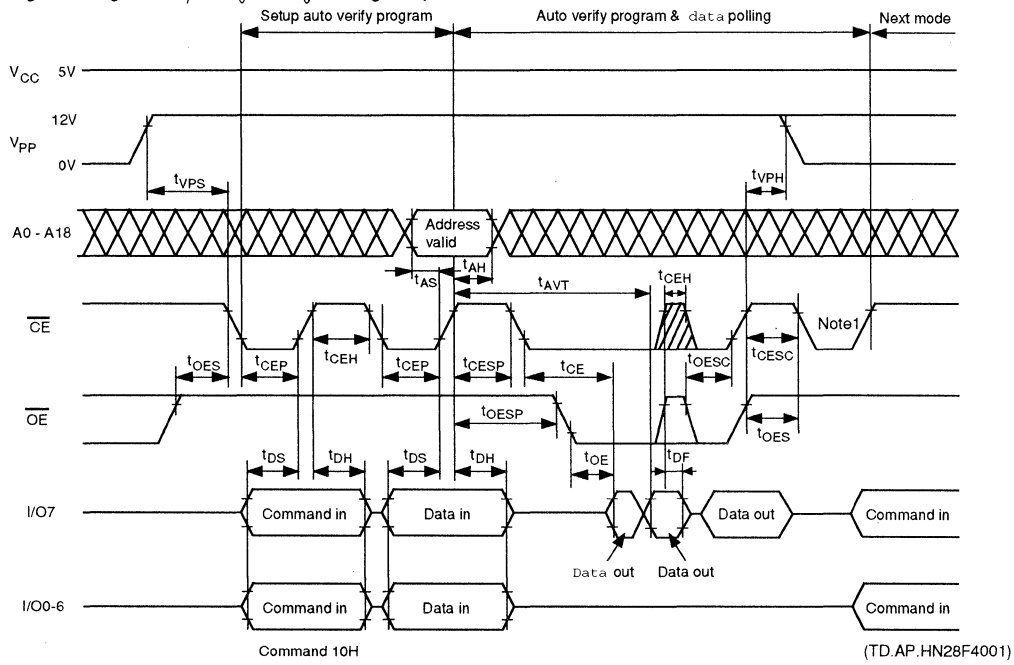
■ PROGRAMMING AND ERASE TIME [1]

	Mode	Min.	Typ.	Min.	Unit
Block (16KB) Erase Time	Automatic [2]	-	4	30	s
	Manual [3,4]	-	1	30	s
Chip (512KB) Erase Time	Automatic	-	4	30	s
	Manual [3,4]	-	1	30	s
Block (16KB) Erase Time	Automatic	-	0.7	33 [7]	s
	Manual [4,5]	-	1	30	s

Notes:
1. These values are the same for all read access versions.
2. Automatic Block Erase does not depend on the number of blocks erased simultaneously.
3. Excludes pre-write process before Erasure and Verify process (6 µs x 16KB or 512KB).
4. Excludes system overhead.
5. Minimum Byte Program time = 31 µs (25 µs Program + 6 µs Verify).
6. T_a = 25°C, V_{PP} = 12V, V_{CC} = 5V.
7. Theoretical value calculated from t_{AVT} max. 2 ms x 16KB = 33 seconds.
8. Theoretical value calculated from Manual Programming Flowchart. (25 µs + 6 µs) x 100 times x 16KB = 51 seconds.

■ AUTOMATIC PROGRAMMING TIMING WAVEFORM

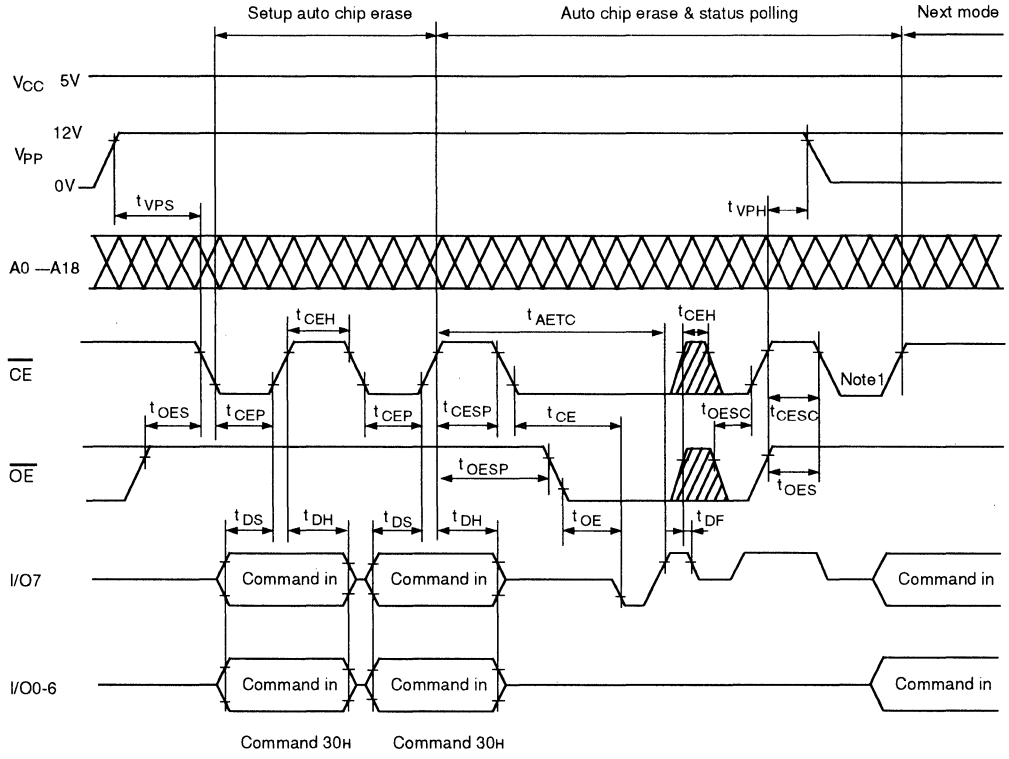
One Byte of data is programmed. External programming verification is not required because these operations are executed automatically by internal control circuitry. Programming completion can be verified by Data Polling after the Automatic Programming starts. Device outputs reverse input data during auto programming on I/O_7. I/O_0 to I/O_6 are high impedance.



Notes:
1. To exit from Data Polling in the Automatic Programming Mode, write the next Command. Example: Write Reset Command or Read Command to read data after programming.
2. During Program Time (t_{AVT}) after writing Setup Auto Verify Programming Command (10H), the device does not accept any Commands, including Reset.

■ AUTOMATIC CHIP ERASE TIMING WAVEFORM

The fast Automatic Chip Erase algorithm shown in the following timing waveform can be applied. All of the data in the chip is erased. External pre-write and erase verify are not required because the cells are pre-written and data is erased automatically by internal control circuitry. Erasure completion can be verified by Status Polling after the Automatic Erase starts. The device outputs V_{OL} level during erasure and V_{OH} level after erasure on I/O_7. I/O_0 to I/O_6 are high impedence.



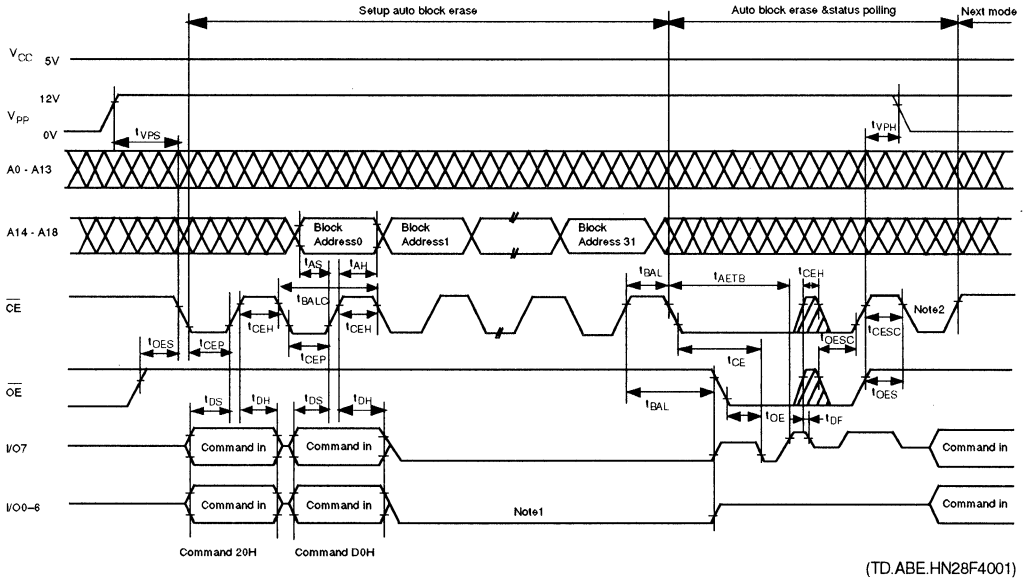
(TD.ACE.HN28F4001)

Notes: 1. To exit from Status Polling in the Automatic Chip Erase Mode, write the next Command. Example: Write Reset Command or Read Command to read data after it has been erased.
2. During Erase Time (t_{AETC}), the device does not accept any Commands, including Reset.

■ AUTOMATIC BLOCK ERASE TIMING WAVEFORM

All of the data in the block (16KBytes) indicated by A_{14} to A_{18} is erased. External pre-write and erase verify is not required because the cells are pre-written and data in the block is erased automatically by internal control circuitry. Erasure completion can be verified by Status Polling after the automatic erase starts. The device outputs V_{OL} level during erasure and V_{OH} level after erasure on I/O_7. I/O_0 to I/O_6 are high impedence.

As indicated below, a single random block or any combination of multiple blocks can be erased simultaneously.

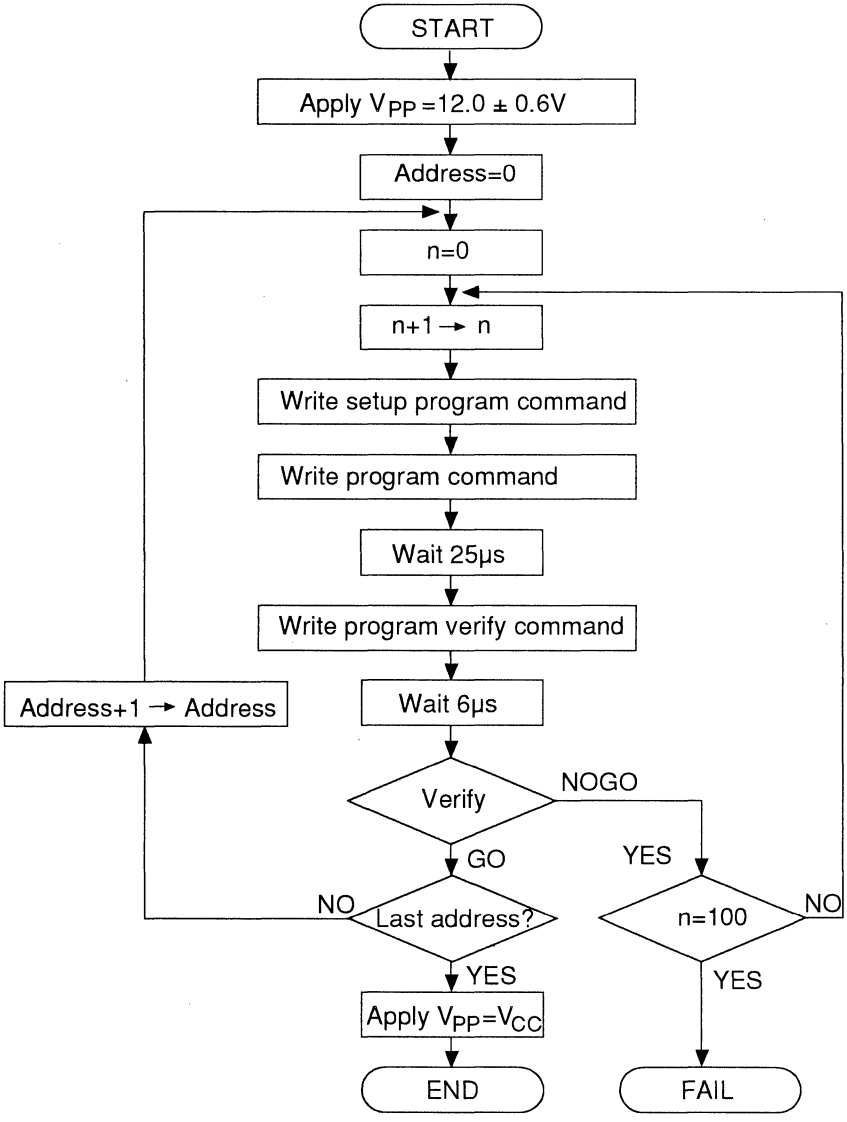


(TD.ABE.HN28F4001)

Notes:
1. I/O_0 to I/O_7 must not be held at FFH (V_{IH} level) when inputting Block addess from A_{14} to A_{18} after writing Command D0H. (Set V_{IL} is shown in the above figure). If FFH is held, the device will Reset and change to the Read Mode.
2. To exit from Status Polling mode, write the next Command.
3. During Block Erase Time (t_{AETB}), the device does not accept any Commands, including Reset.

■ MANUAL PROGRAMMING FLOWCHART

The HN28F4001 can be programmed with the fast, high-reliability programming algorithm shown in the following flowchart. This algorithm provides fast programming time without any voltage stress to the device or deterioration in reliability of programmed data.

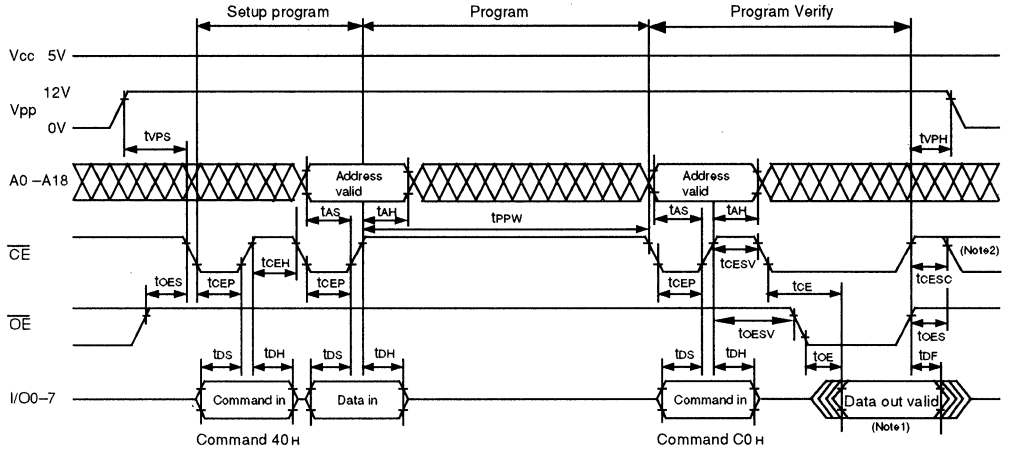


(FC.P.HN28F4001)

Note: In case two or more devices are programmed simultaneously, the following steps should be applied to avoid over-programming the verified device:

1. Setup Program Command: Write FFH
2. Program Command: Write FFH
3. Program Verify Command: Write 00H
4. Program Verify Address: Read Address

■ MANUAL PROGRAMMING TIMING WAVEFORM



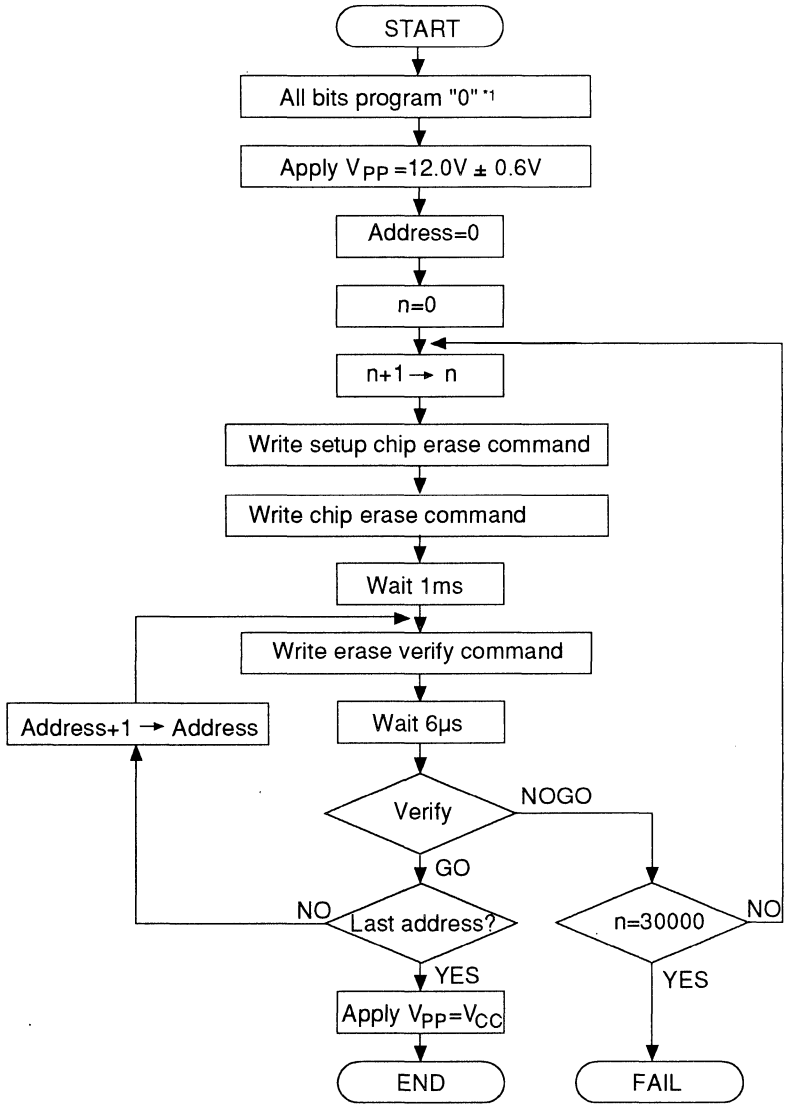
(TD.MP.HN28F4001)

Notes: 1. The data output level during program verification may result in an intermediate level between V_{OH} and V_{OL} due to insufficient programming.

2. After reading Program Verify data ($\overline{CE}$ and $\overline{OE}$ turn from V_{IL} level to V_{IH} level), write the next Command to read, program, erase and program verify.
Example: Write Program Verify Command or set Program Verify address to verify next address continuously.

■ MANUAL CHIP ERASE FLOWCHART

The HN28F4001 can be erased with the fast, high-reliability chip erase algorithm shown in the following flowchart. This algorithm provides a fast erase time without any voltage stress to the device or deterioration in data reliability.

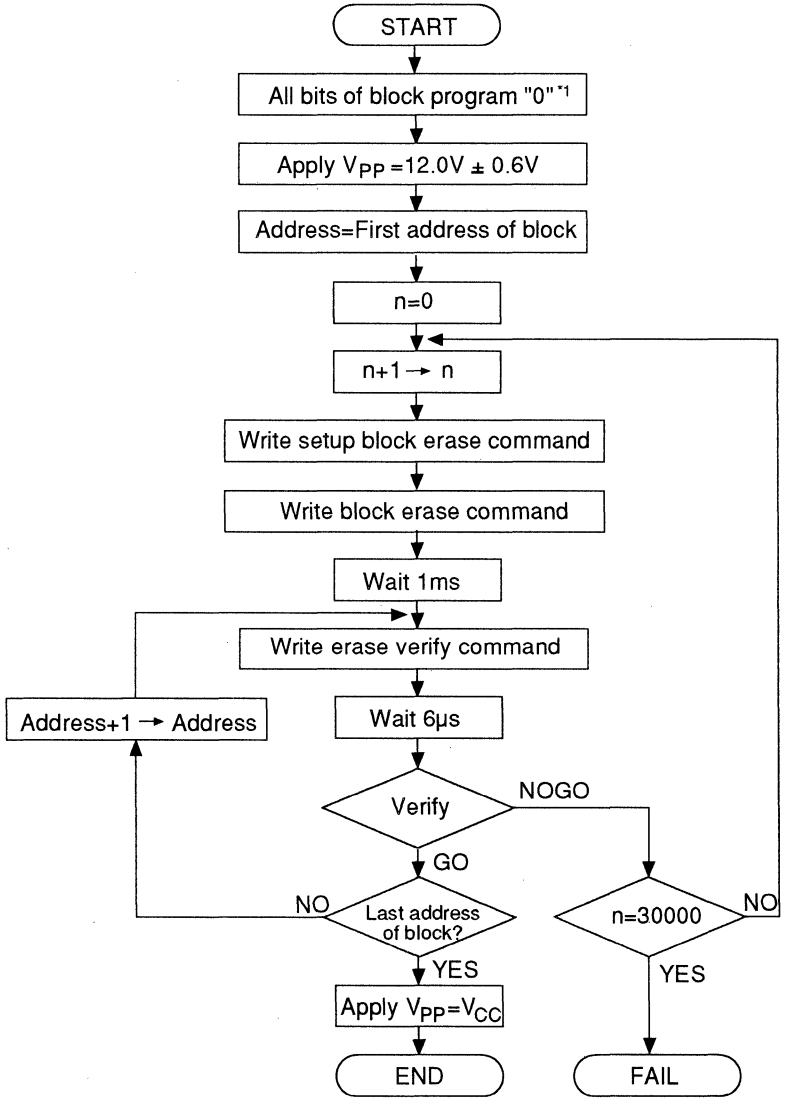


(FC.CE.HN28F4001)

Note: 1. Program data according to Manual Programming Flowchart.
2. In case two or more devices are erased simultaneously, the following steps should be applied to avoid over-erasing the verified device:
   1. Setup Erase Command: Write FFH
   2. Erase Command: Write FFH
   3. Erase Verify Command: Write 00H
   4. Erase Verify Address: Read Address

■ MANUAL BLOCK ERASE FLOWCHART

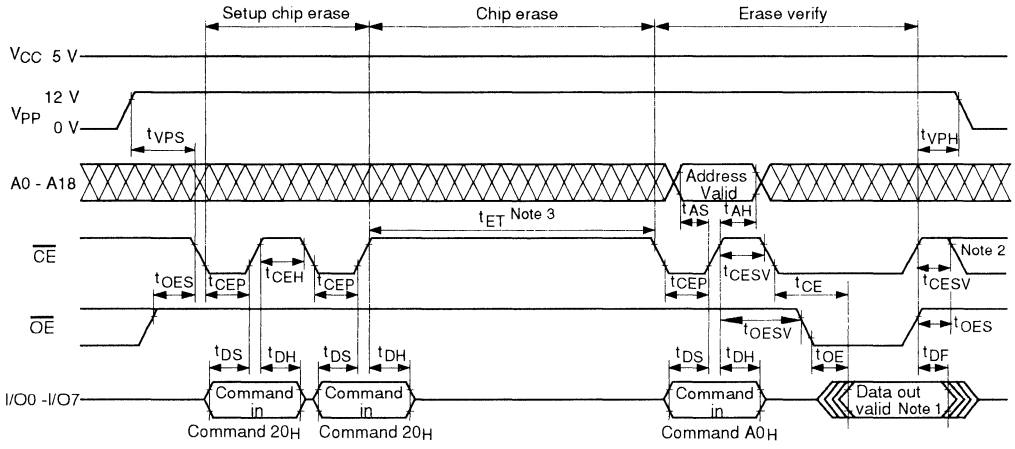
The HN28F4001 can be erased with the fast, high-reliability block erase algorithm shown in the following flowchart. This algorithm provides a fast block (16KBytes) erase time without any voltage stress to the device or deterioration in data reliability.



(FC.BE.HN28F4001)

Note: 1. Program data according to Manual Programming Flowchart.
2. In case two or more devices are erased simultaneously, the following steps should be applied to avoid over-erasing the verified device:
   1. Setup Erase Command: Write FFH
   2. Erase Command: Write FFH
   3. Erase Verify Command: Write 00H
   4. Erase Verify Address: Read Address

■ MANUAL CHIP ERASE TIMING WAVEFORM

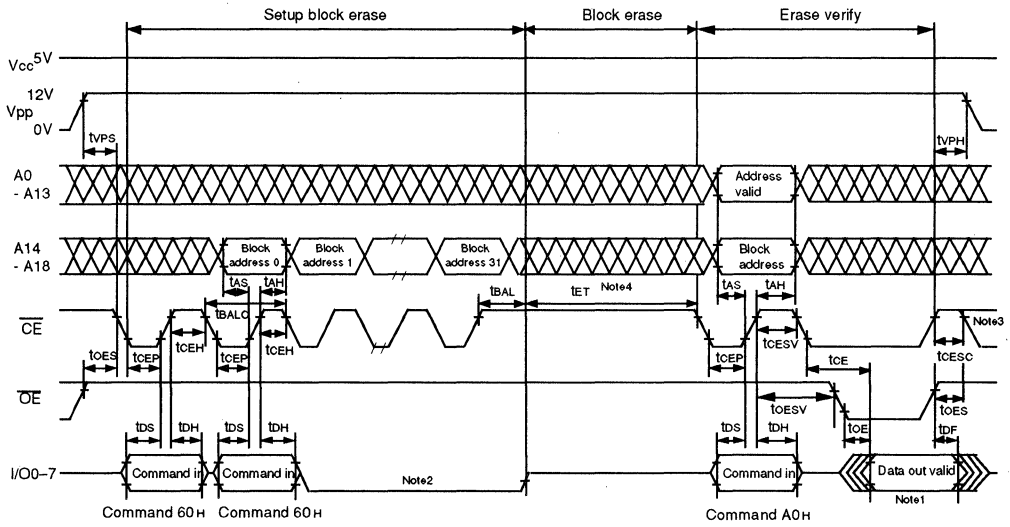


(TD.CE.HN28F4001)

Notes:
1. The data output level during erase verification may result in an intermediate level between V_{OH} and V_{OL} due to insufficient erasing.
2. After reading Erase Verify data ($\overline{CE}$ and $\overline{OE}$ turn from V_{IL} level to V_{IH} level), write the next Command to read, program, erase and program verify.
   Example: Write Erase Verify Command or set Erase Verify address to verify next address continuously.
3. During Standby Erase Time (t_{ET}), the device does not accept any Commands, including Reset.

■ MANUAL BLOCK ERASE TIMING WAVEFORM

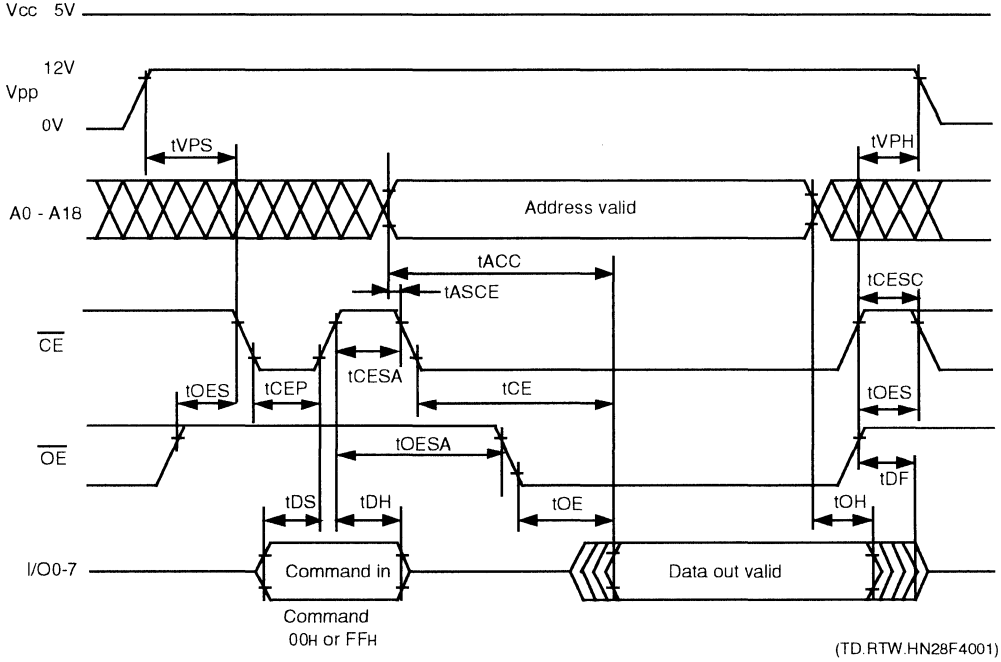
As indicated below, a single random block or any combination of multiple blocks can be erased simultaneously.



(TD.BE.HN28F4001)

Notes:
1. The data output level during erase verification may result in an intermediate level between V_{OH} and V_{OL} due to insufficient erasing.
2. I/O_0 to I/O_7 must not be held at FFH (V_{IH} level) when inputting Block addess from A_{14} to A_{18} after writing Command 60H twice. (Set V_{IL} is shown in the above figure). If FFH is held, the device will Reset and change to the Read Mode.
3. After reading Erase Verify data ($\overline{CE}$ and $\overline{OE}$ turn from V_{IL} level to V_{IH} level), write the next Command to read, program, erase and program verify.
   Example: Write Erase Verify Command or set Erase Verify address to verify next address continuously.
4. During Standby Erase Time (t_{ET}), the device does not accept any Commands, including Reset.

■ READ TIMING WAVEFORM (V_{PP} APPLIED)



Notes: 1. When 12V is applied to V_{PP}, programmed data might be destroyed by the voltage fluctuation of the supplu voltage, such as a large V_{CC} ramp. To suppress voltage fluctuation of V_{CC}, insertion of a bypass capacitor is recommended.

■ DEVICE IDENTIFIER MODE DESCRIPTION

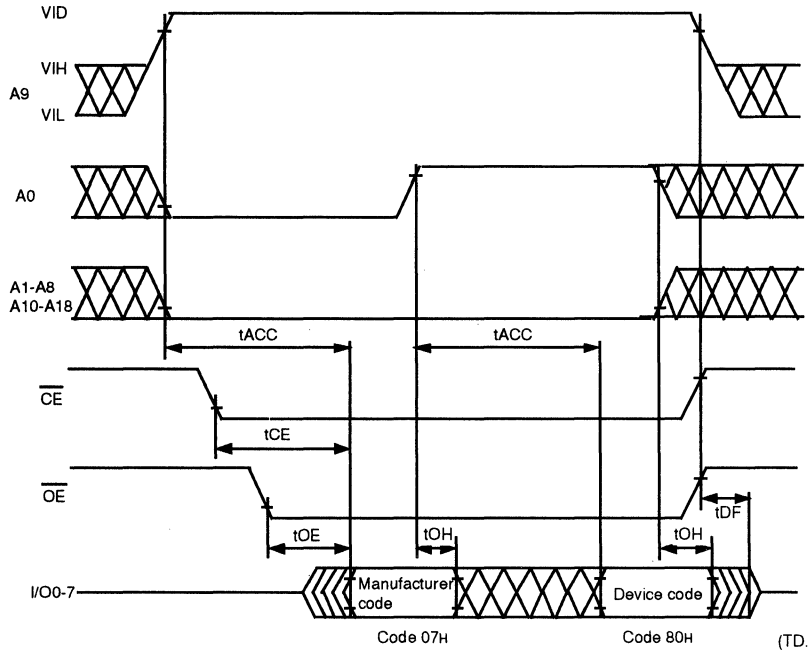
The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

■ HN28F4001 SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	0	0	0	0	0	0	80

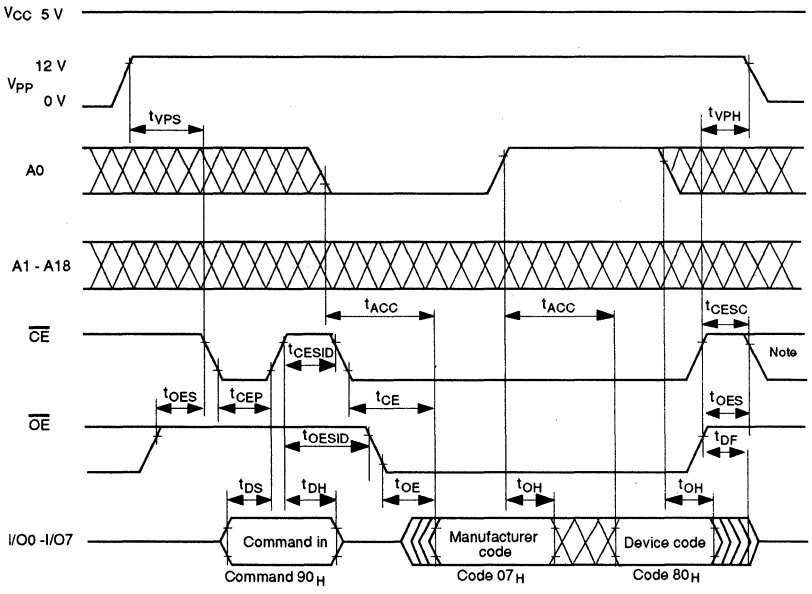
Notes: 1. Device identifier code can be read out by applying 12.0 V ± 0.5 V to A9 when $V_{PP} = V_{CC}$, or inputting Command while V_{PP}=12 V.
2. $V_{CC} = V_{PP}$=5.0 V ± 10% when applying 12 V to A9.
V_{CC} =5.0 V ± 10% and V_{PP}=12.0 V ± 0.6 V in command inputs.
3. A1 to A8, A10 to A18, $\overline{CE}$, and $\overline{OE} = V_{IL}$.

■ IDENTIFIER CODE READ TIMING WAVEFORM (V_{PP} = V_{SS} to V_{CC})



(TD.ID1.HN28F4001)

■ IDENTIFIER CODE READ TIMING WAVEFORM (V_{PP} = 12V)



(TD.ID2.HN28F4001)

Note: 1. To exit from the Identifier Code Read mode, write the next Command.

Mask ROM

SECTION 3
Mask ROM

HITACHI
Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

4M (256K x 16-bit) and (512K x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62415 Series is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 262,144 x 16-bit and 524,288 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62415 Series is offered in 40-pin Plastic DIP, 40-lead Plastic SOP, 44-lead Plastic QFP and TQFP, 48-lead Plastic SOP and 44-lead Plastic TSOP packages.

■ FEATURES

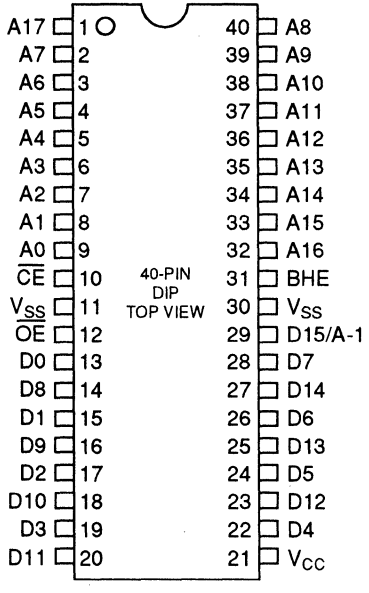
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  120 ns/150 ns (max)
- Low Power Consumption:
  Active Current: 150 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  256K x 16-bit (Word-Wide)
  512K x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  40-pin Plastic DIP
  40-lead Plastic SOP
  44-lead Plastic QFP
  44-lead Plastic TQFP
  48-lead Plastic SOP
  44-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62415P	120 ns	40-pin Plastic
	150 ns	DIP (DP-40)
HN62415FA	120 ns	40-lead Plastic
	150 ns	SOP (FP-40D)
HN62415FP	120 ns	44-lead Plastic
	150 ns	QFP (FP-44A)
HN62415TFP	120 ns	44-lead Plastic
	150 ns	TQFP (TFP-44)
HN62415F	120 ns	48-lead Plastic
	150 ns	SOP (FP-48DA)
HN62415TT	120 ns	44-lead Plastic
	150 ns	TSOP (TTP-44D)

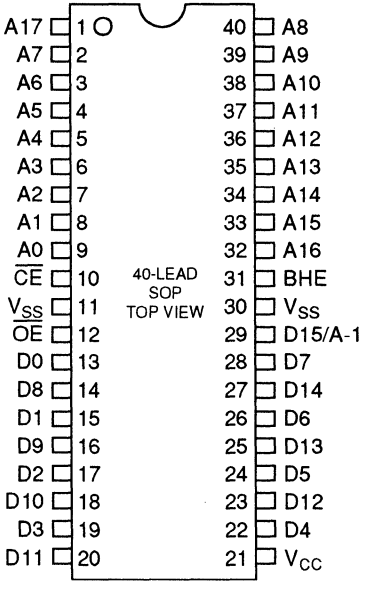
■ PIN ARRANGEMENT

HN62415P Series



(PinD40.HN62415)

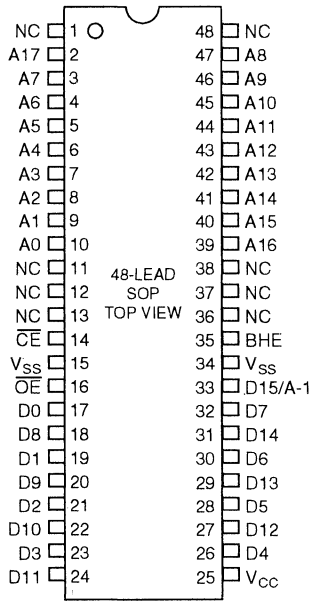
HN62415FA Series



(PinT240.HN62415)

■ PIN ARRANGEMENT (cont.)

HN62415F Series



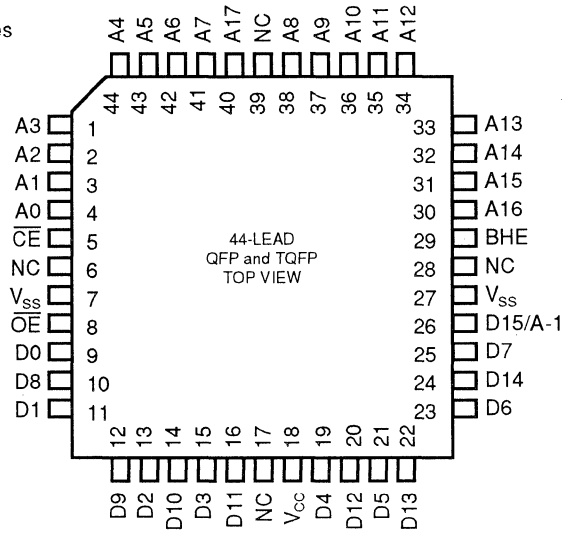
Note:
Pins 11, 12, 13, 36, 37, and 38 are connected to the inner lead frame.

(PinT248.HN62415)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

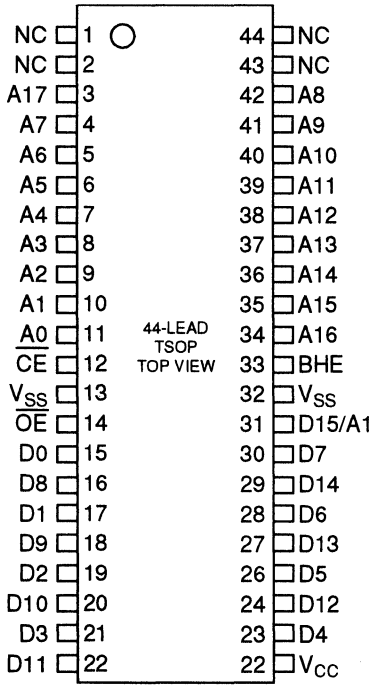
HN62415FP Series
HN62415TFP Series



(PinQ44.HN62415)

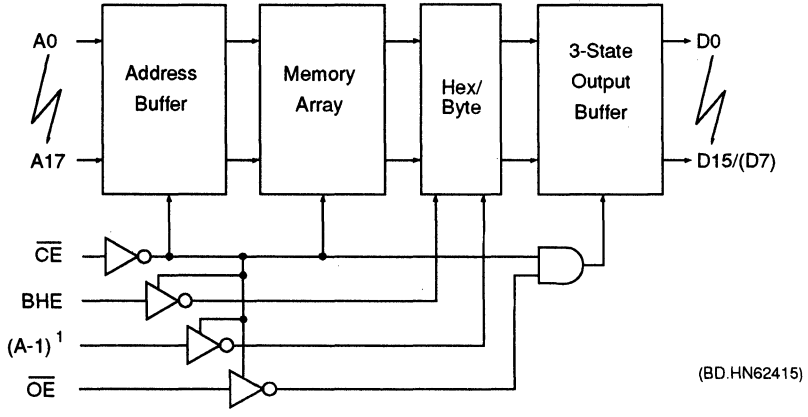
■ PIN ARRANGEMENT (cont.)

HN62415TT Series



(PinT244.HN62415)

■ BLOCK DIAGRAM



(BD.HN62415)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.4 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	60	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}= Min.
Standby V_{CC} Current	I_{SB1}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
	I_{SB2}	-	3	mA	V_{CC} = 5.5 V, CE ≥ 2.4V
Input Voltage	V_{IH}	2.4	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.6	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

3

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

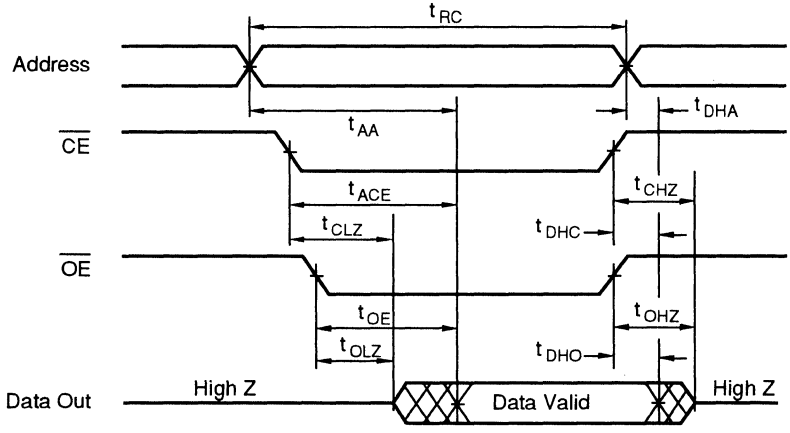
- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62415-12		HN62415-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120	-	150	-	ns
Address Access Time	t_{AA}	-	120	-	150	ns
$\overline{CE}$ Access Time	t_{ACE}	-	120	-	150	ns
$\overline{OE}$ Access Time	t_{OE}	-	60	-	70	ns
BHE Access Time	t_{BHE}	-	120	-	150	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
$\overline{CE}$ to Output in High Z[1]	t_{CHZ}	-	60	-	70	ns
$\overline{OE}$ to Output in High Z[1]	t_{OHZ}	-	60	-	70	ns
BHE to Output in High Z[1]	t_{BHZ}	-	60	-	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	-	10	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	-	10	-	ns
BHE to Output in Low Z	t_{BLZ}	5	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM

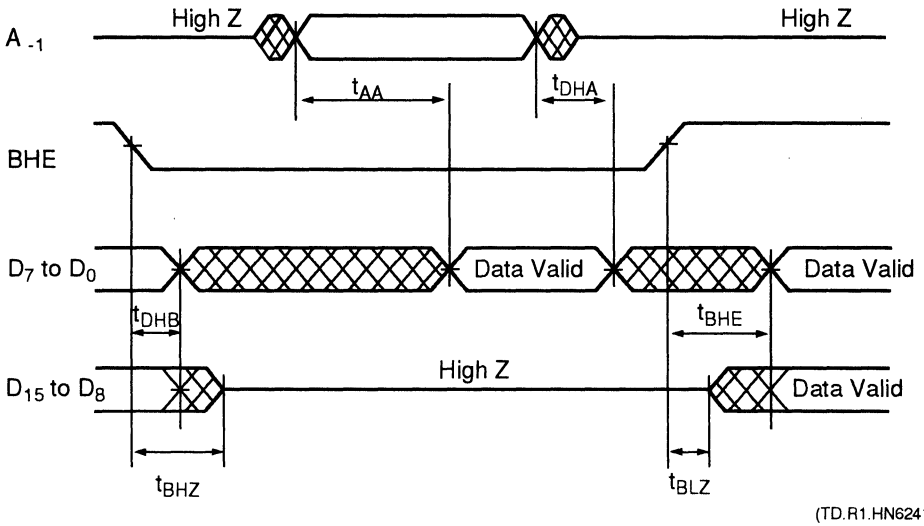
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



(TD.R.HN62415)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

Word Mode/Byte Mode Switch



(TD.R1.HN62415)

Note: 1. $\overline{CE}$ and $\overline{OE}$ are enabled, A_{17} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

4M (256K x 16-bit) and (512K x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62W415 Series is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 262,144 x 16-bit and 524,288 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density provideS enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62W415 Series is offered in 40-pin Plastic DIP, 40-lead Plastic SOP, 44-lead Plastic QFP and TQFP, 48-lead Plastic SOP and 44-lead Plastic TSOP packages.

■ FEATURES

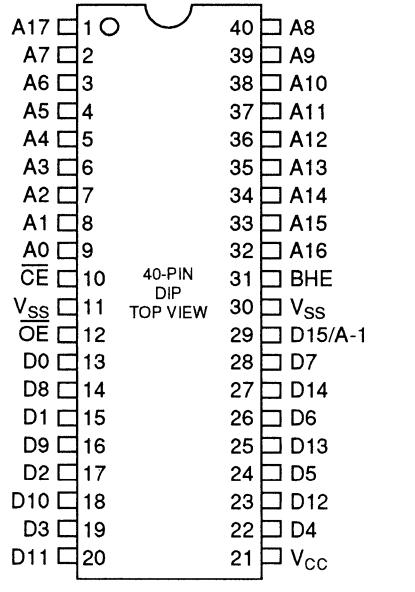
- Single Power Supply:
  V_{CC} = 3.0 to 5.5V
- Fast Access Times:
  250 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  256K x 16-bit (Word-Wide)
  512K x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  40-pin Plastic DIP
  40-lead Plastic SOP
  44-lead Plastic QFP
  44-lead Plastic TQFP
  48-lead Plastic SOP
  44-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62W415P	250 ns	40-pin Plastic DIP (DP-40)
HN62W415FA	250ns	40-lead Plastic SOP (FP-40D)
HN62W415FP	250ns	44-lead Plastic QFP (FP-44A)
HN62W415TFP	250ns	44-lead Plastic TQFP (TFP-44)
HN62W415F	250ns	48-lead Plastic SOP (FP-48DA)
HN62W415TT	250ns	44-lead Plastic TSOP (TTP-44D)

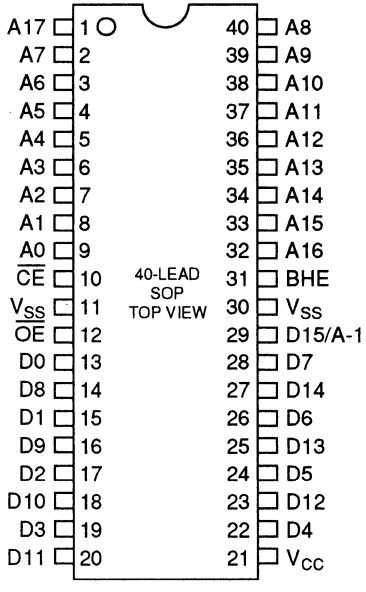
■ PIN ARRANGEMENT

HN62W415P Series



(PinD40.HN62415)

HN62W415FA Series

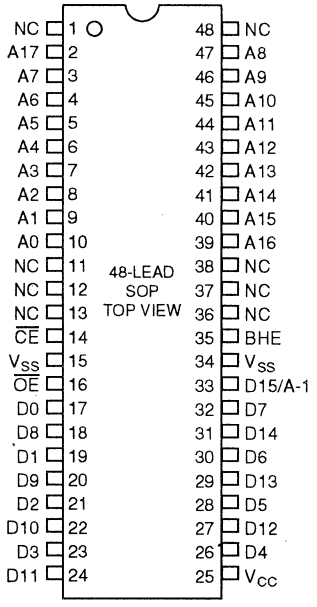


(PinT240.HN62415)

3

■ PIN ARRANGEMENT (cont.)

HN62W415F Series



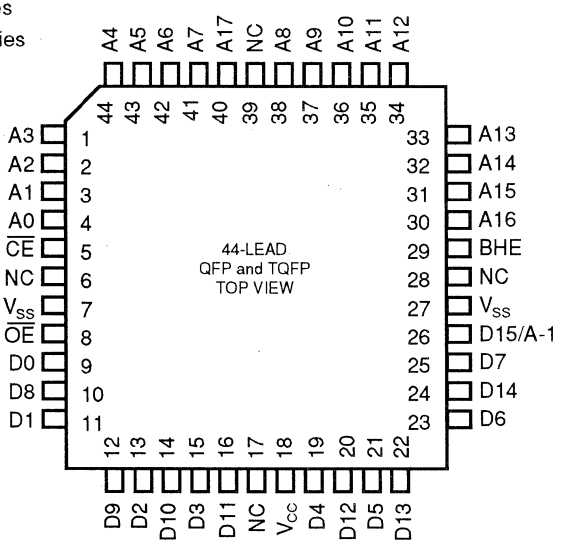
Note:
Pins 11, 12, 13, 36, 37, and 38 are connected to the inner lead frame.

(PinT248.HN62415)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

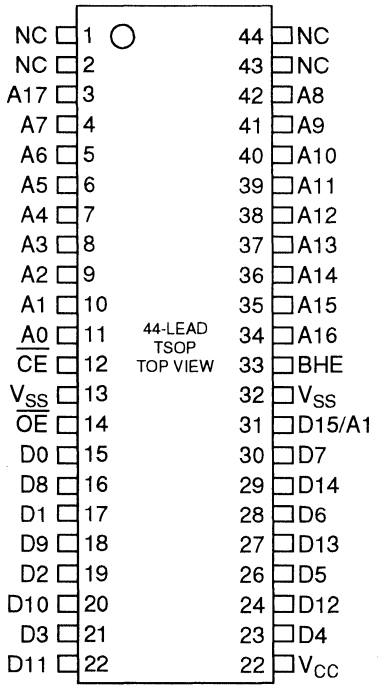
HN62W415FP Series
HN62W415TFP Series



(PinQ44.HN62415)

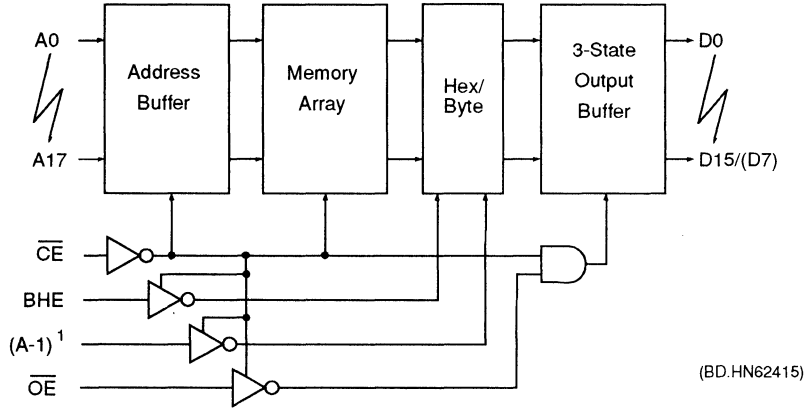
■ PIN ARRANGEMENT (cont.)

HN62W415TT Series



(PinT244.HN62415)

■ BLOCK DIAGRAM



(BD.HN62415)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.4 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	30	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}= Min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.4	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.6	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

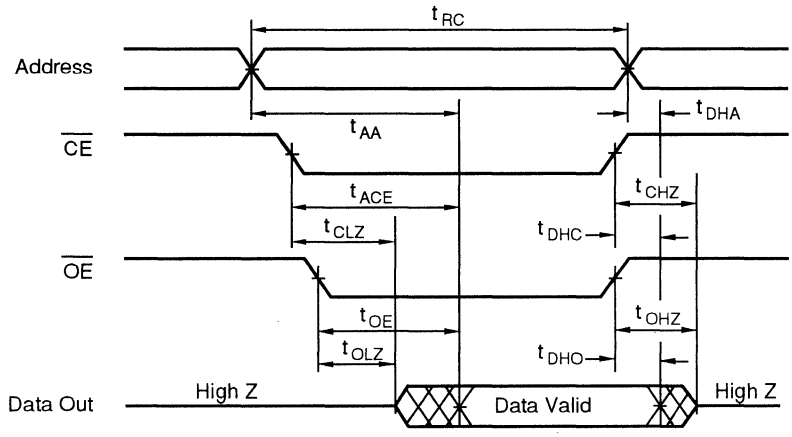
Item	Symbol	HN6W2415-12 Min.	HN6W2415-12 Max.	Unit
Read Cycle Time	t_{RC}	250	-	ns
Address Access Time	t_{AA}	-	250	ns
$\overline{CE}$ Access Time	t_{ACE}	-	250	ns
$\overline{OE}$ Access Time	t_{OE}	-	100	ns
BHE Access Time	t_{BHE}	-	250	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	ns
$\overline{CE}$ to Output in High Z[1]	t_{CHZ}	-	100	ns
$\overline{OE}$ to Output in High Z[1]	t_{OHZ}	-	100	ns
BHE to Output in High Z[1]	t_{BHZ}	-	100	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	-	ns
BHE to Output in Low Z	t_{BLZ}	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

3

■ READ TIMING WAVEFORM

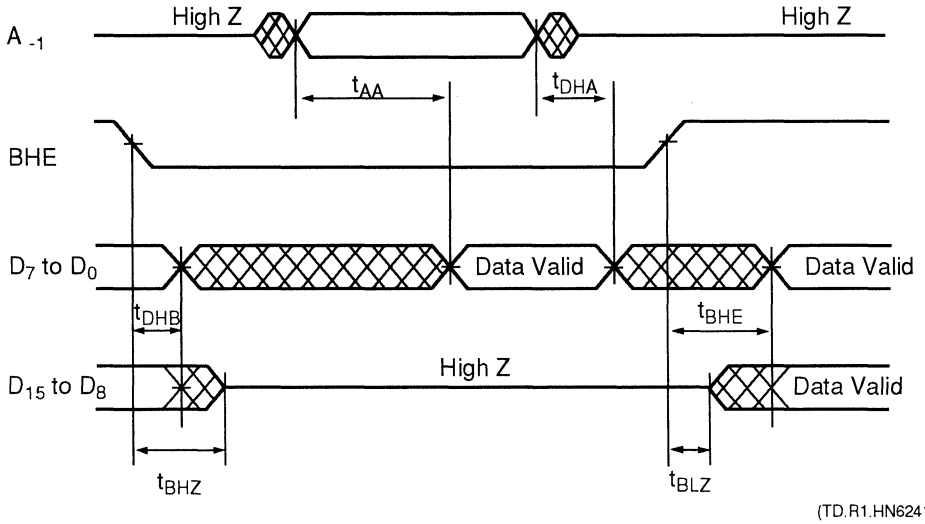
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



(TD.R.HN62415)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

Word Mode/Byte Mode Switch



(TD.R1.HN62415)

Note: 1. $\overline{CE}$ and $\overline{OE}$ are enabled, A_{17} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

4M (512K x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62335B Series is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 524,288 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62335B Series is offered with JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages. This allows socket replacement with EPROMs and Flash Memory.

■ FEATURES

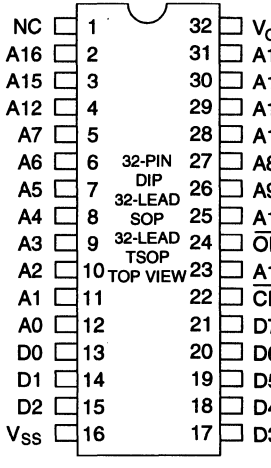
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  120 ns/150 ns (max)
- Low Power Consumption:
  Active Current: 150 mW (typ)
  Standby Current: 5 µW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
  EPROM and Flash Memory Compatible
- Packages:
  32-pin Plastic DIP
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62335BP	120 ns	32-pin Plastic DIP
	150 ns	(DP-32)
HN62335BF	120 ns	32-lead Plastic SOP
	150 ns	(FP-32D)
HN62335BTT	120 ns	32-lead Plastic TSOP
	150 ns	(TTP-32D)

■ PIN ARRANGEMENT

HN62335BP/F/TT Series

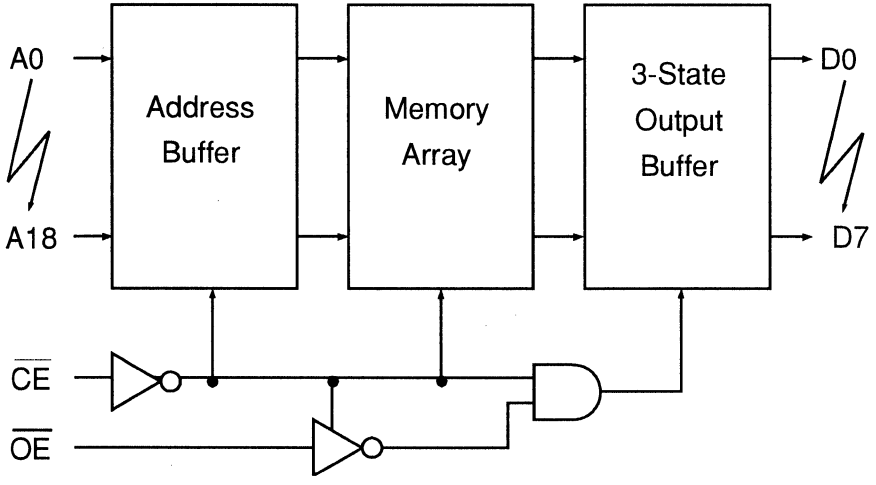


(PinD32.HN62314B,334B)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
D_0 - D_7	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN62314B,334B)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	60	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}= min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.4	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.6	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

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■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

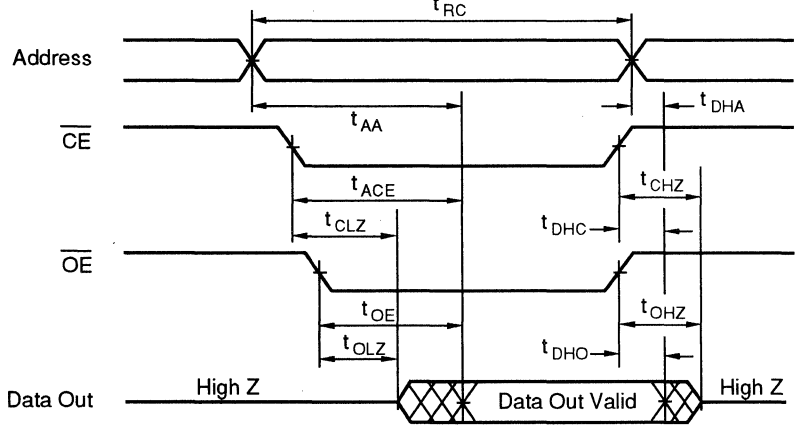
Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62335B-12		HN62335B-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120	-	150	-	ns
Address Access Time	t_{AA}	-	120	-	150	ns
$\overline{CE}$ Access Time	t_{ACE}	-	120	-	150	ns
$\overline{OE}$ Access Time	t_{OE}	-	60	-	70	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	ns
$\overline{CE}$ to Output in High Z	t_{CHZ} [1]	-	60	-	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ} [1]	-	60	-	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	-	5	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	-	5	-	ns

Note: 1. t_{CHZ} and t_{OHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM



(TD.R.HN62314B,334B)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

4M (512K x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62W335B Series is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 524,288 x 8-bit.

The low supply voltage and power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density provides enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62W335B Series is offered with JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages. This allows socket replacement with EPROMs and Flash Memory.

■ FEATURES

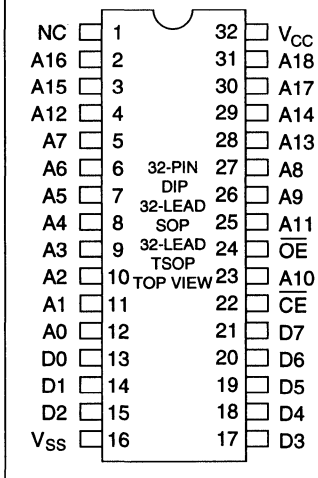
- Single Power Supply:
  V_{CC} = 3.0 to 5.5V
- Fast Access Times:
  250 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
  EPROM and Flash Memory Compatible
- Packages:
  32-pin Plastic DIP
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62W335BP	250 ns	32-pin Plastic DIP (DP-32)
HN62W335BF	250 ns	32-lead Plastic SOP (FP-32D)
HN62W335BTT	250 ns	32-lead Plastic TSOP (TTP-32D)

■ PIN ARRANGEMENT

HN62W335BP/F/TT Series

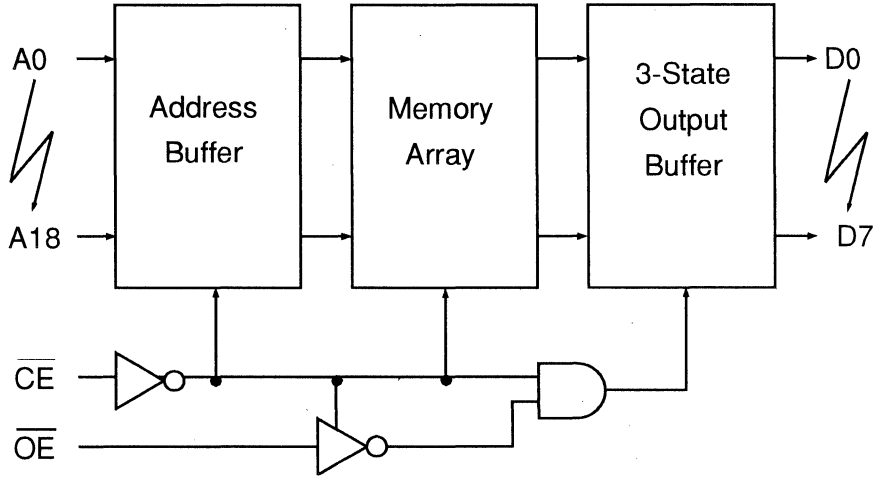


(PinD32.HN62314B,334B)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
D_0 - D_7	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN62314B,334B)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	30	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}= min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.4	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.6	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

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■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0 V, T_a = 0 to 70°C)

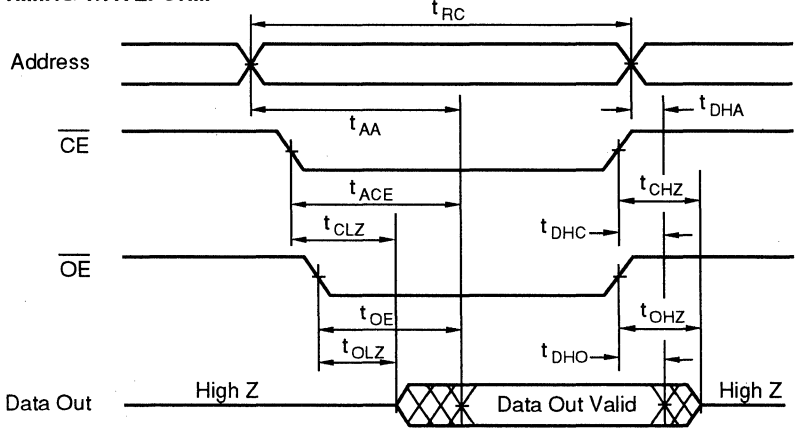
Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62W335B-25 Min.	HN62W335B-25 Max.	Unit
Read Cycle Time	t_{RC}	250	-	ns
Address Access Time	t_{AA}	-	250	ns
$\overline{CE}$ Access Time	t_{ACE}	-	250	ns
$\overline{OE}$ Access Time	t_{OE}	-	100	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	ns	
Output Hold Time from $\overline{OE}$	t_{DHO}	0	ns	
$\overline{CE}$ to Output in High Z	t_{CHZ} [1]	-	100	ns
$\overline{OE}$ to Output in High Z	t_{OHZ} [1]	-	100	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	-	ns

Note: 1. t_{CHZ} and t_{OHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM



(TD.R.HN62314B,334B)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

8M (512K x 16-bit) and (1M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62448 Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized either as 524,288 x 16-bit or as 1,048,576 x 8-bit.

The high density and high speed access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

Hitachi's HN62448 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP, 44-lead Plastic TSOP and 44-lead Plastic QFP packages. The HN62448 is also packaged in a 48-lead Plastic SOP.

■ FEATURES

- Single Power Supply
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  100 ns/120 ns (max)
- Low Power Consumption:
  Active Current: 250 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  512K x 16-bit (Word-Wide)
  1M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  44-lead Plastic TSOP (Type II)
  48-lead Plastic SOP
  44-pin Plastic QFP

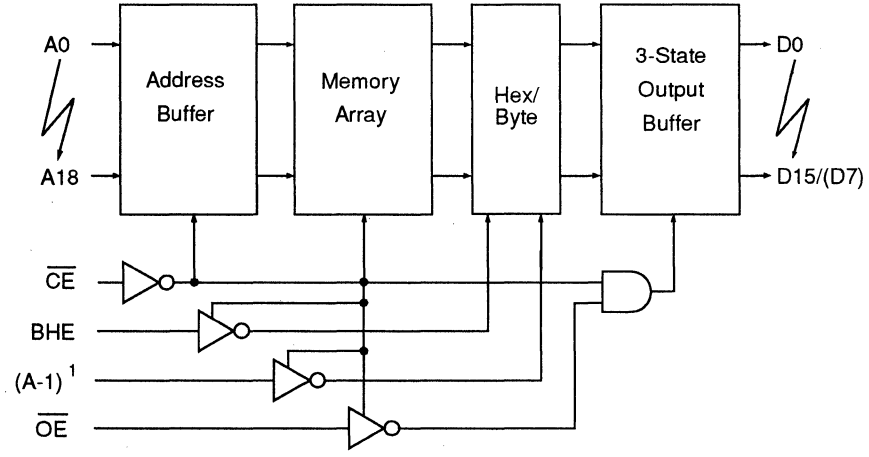
■ ORDERING INFORMATION

Type No	Access Time	Package
HN62448P	100 ns 120 ns	42-pin Plastic DIP (DP-42)
HN62448FB	100 ns 120 ns	44-lead Plastic SOP (FP-44D)
HN62448TT	100 ns 120 ns	44-lead Plastic TSOP (TTP-44D)
HN62448F	100 ns 120 ns	48-lead Plastic SOP (FP-48DA)
HN62448FP	100 ns 120 ns	44-pin Plastic QFP (FP-44A)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM

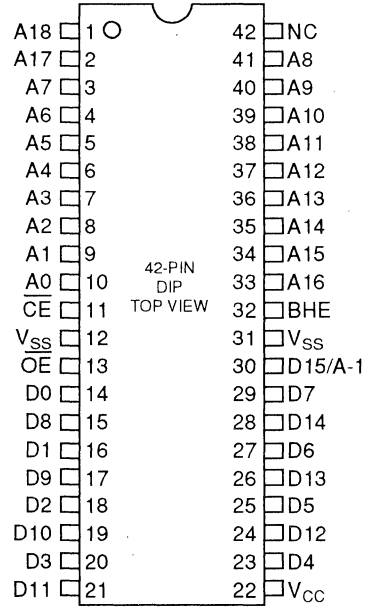


(BD.HN62418)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

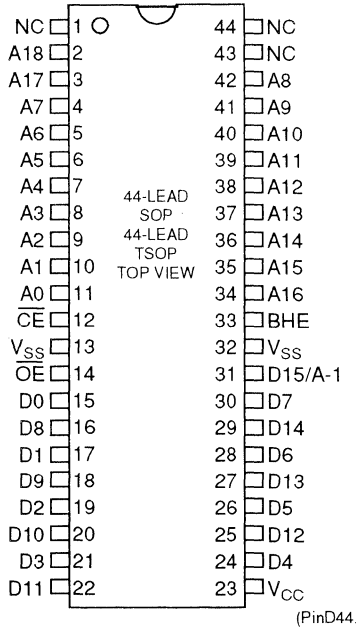
■ PIN ARRANGEMENT

HN62448P Series



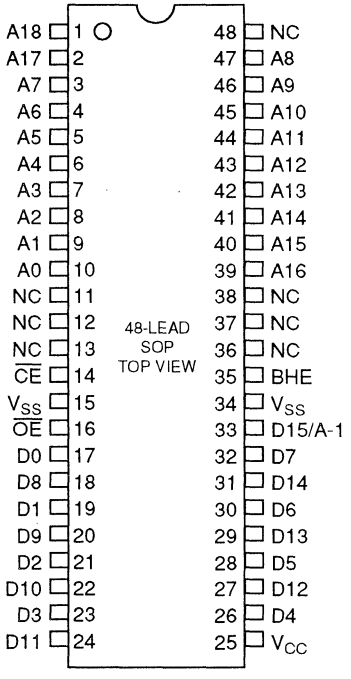
(PinD42.HN62438N)

HN62448FB Series
HN62448TT Series



(PinD44.HN62438N)

HN62448F Series



Note:
Pins 11, 12, 13, 36, 37 and 38 are connected to the inner lead frame.

(PinT248.HN62438N)

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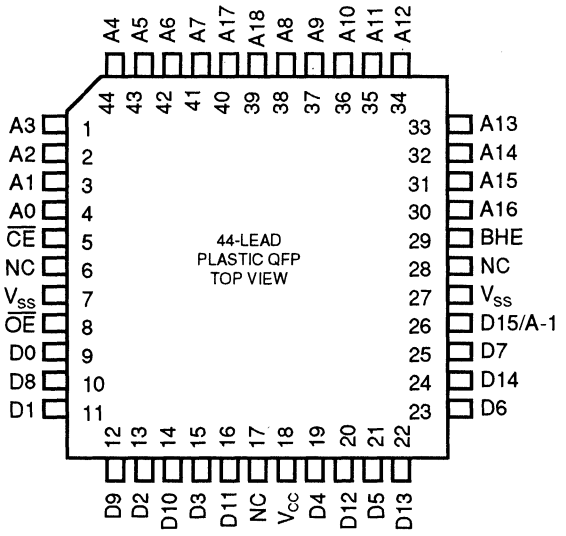
■ PIN ARRANGEMENT, contd.

HN62448FP Series



(PinQ44.HN62418)

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.4 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	80	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}= Min.
Standby V_{CC} Current	I_{SB1}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.4	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.45	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62448-10		HN62448-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100	-	120	-	ns
Address Access Time	t_{AA}	-	100	-	120	ns
$\overline{CE}$ Access Time	t_{ACE}	-	100	-	120	ns
$\overline{OE}$ Access Time	t_{OE}	-	50	-	60	ns
BHE Access Time	t_{BHE}	-	100	-	120	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}[1]	-	40	-	40	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}[1]	-	40	-	40	ns
BHE to Output in High Z	t_{BHZ}[1]	-	40	-	40	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	-	5	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	-	5	-	ns
BHE to Output in Low Z	t_{BLZ}	5	-	5	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

3

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

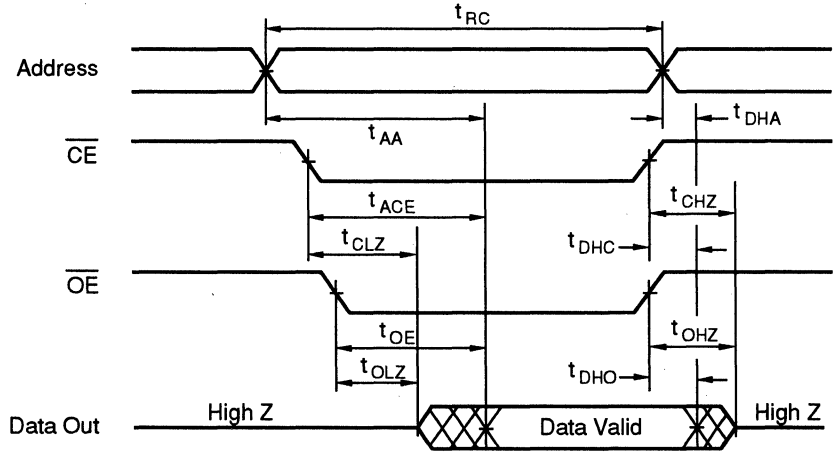
(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ READ TIMING WAVEFORM

Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})

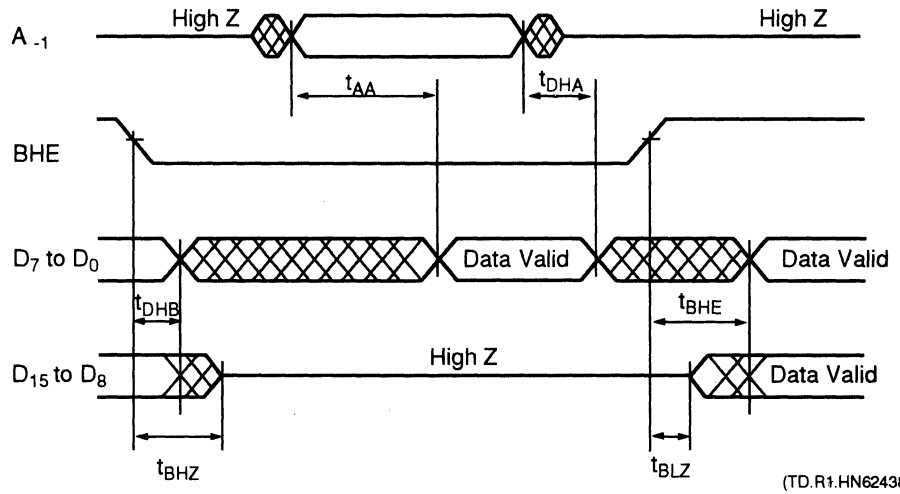


(TD.R.HN62438N)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

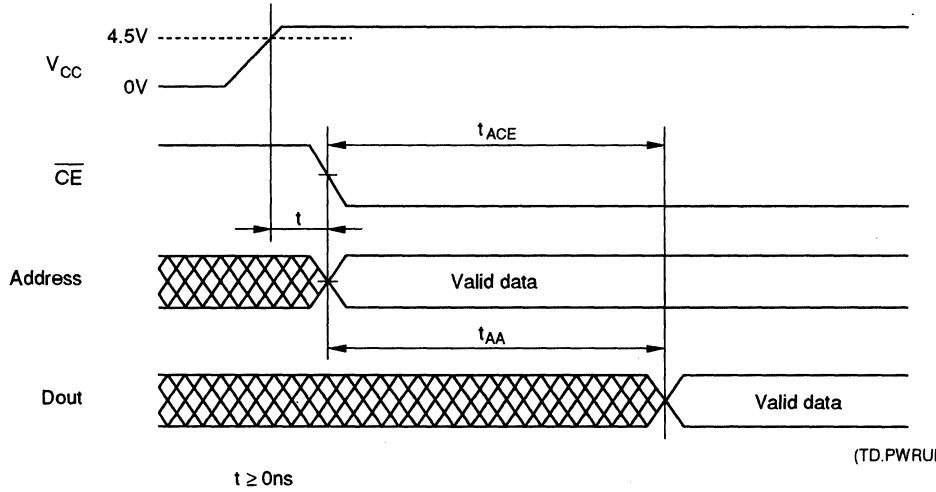
■ READ TIMING WAVEFORM

Word Mode/Byte Mode Switch



Note: 1. $\overline{CE}$ and $\overline{OE}$ are of select status. A_{18} to A_0 are fixed.
2. D_{15}/A_{-1} terminal is of output state when $\overline{BHE} = V_{IH}$, $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

■ POWER-UP SEQUENCE



Note: This device uses an Address Transient Detector (ATD). After power-up to 4.5V, transfer either $\overline{CE}$ or Address.

8M (512K x 16-bit) and (1M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62448N Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized either as 524,288 x 16-bit or as 1,048,576 x 8-bit.

The high density and high speed Fast Address Access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

Hitachi's HN62448N is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP, 44-lead Plastic TSOP and 44-lead Plastic QFP packages. The HN62448N is also packaged in a 48-lead Plastic SOP.

■ FEATURES

- Single Power Supply
  $V_{CC} = 5\ V \pm 10\%$
- Fast Access Times:
  100 ns/120 ns (max)
- Fast Address Access Times (A_0, A_1):
  50 ns/60 ns (max)
- Low Power Consumption:
  Active Current: 250 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  512K x 16-bit (Word-Wide)
  1M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  44-lead Plastic TSOP (Type II)
  48-lead Plastic SOP
  44-pin Plastic QFP

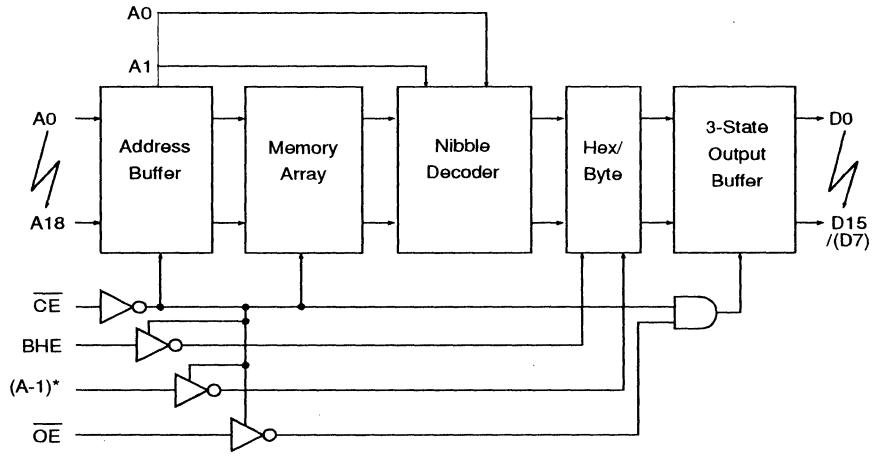
■ ORDERING INFORMATION

Type No	Access Time	Package
HN62448NP	100 ns 120 ns	42-pin Plastic DIP (DP-42)
HN62448NFB	100 ns 120 ns	44-lead Plastic SOP (FP-44D)
HN62448NTT	100 ns 120 ns	44-lead Plastic TSOP (TTP-44D)
HN62448NF	100 ns 120 ns	48-lead Plastic SOP (FP-48DA)
HN62448NFP	100 ns 120 ns	44-pin Plastic QFP (FP-44A)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM

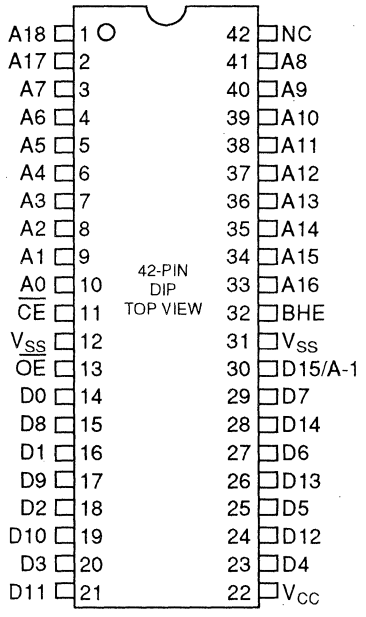


(BD.HN62438N)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

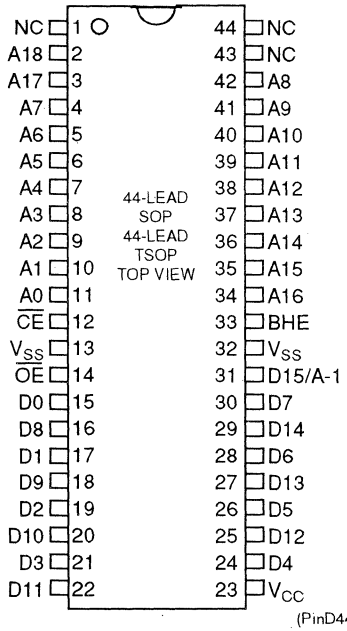
■ PIN ARRANGEMENT

HN62448NP Series



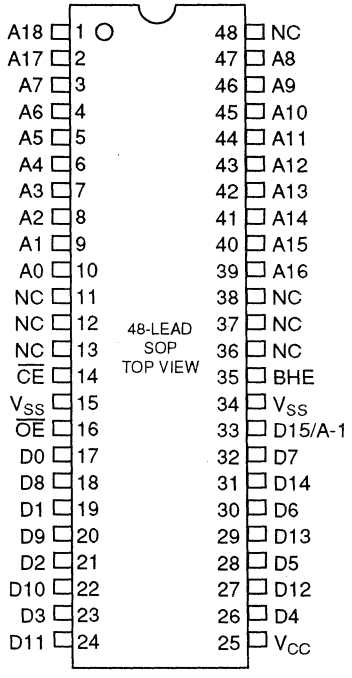
(PinD42.HN62438N)

HN62448NFB Series
HN62448NTT Series



(PinD44.HN62438N)

HN62448NF Series

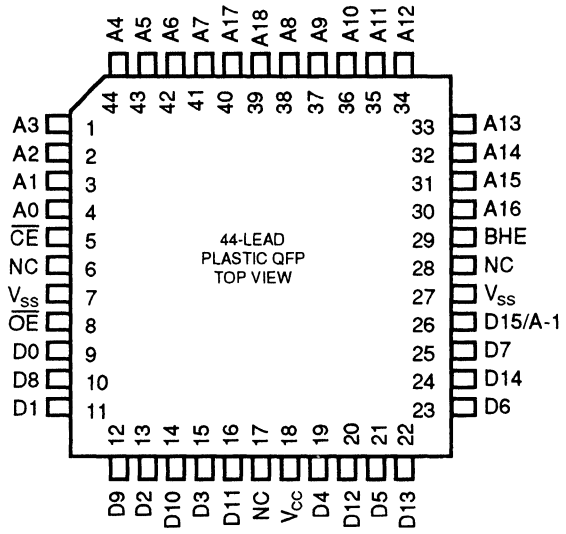


Note:
Pins 11, 12, 13, 36, 37 and 38 are connected to the inner lead frame.

(PinT248.HN62438N)

■ PIN ARRANGEMENT, contd.

HN62448NFP Series



(PinQ44.HN62418)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62448N-10		HN62448N-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100	-	120	-	ns
Fast Address Read Cycle Time	t_{BC}	50	-	60	-	ns
Address Access Time	t_{AA}	-	100	-	120	ns
Fast (Address Access) Time	t_{BA}	-	50	-	60	ns
$\overline{CE}$ Access Time	t_{ACE}	-	100	-	120	ns
$\overline{OE}$ Access Time	t_{OE}	-	50	-	60	ns
BHE Access Time	t_{BHE}	-	100	-	120	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
$\overline{CE}$ to Output in High Z	t_{CHZ} [1]	-	50	-	60	ns
$\overline{OE}$ to Output in High Z	t_{OHZ} [1]	-	50	-	60	ns
BHE to Output in High Z	t_{BHZ} [1]	-	50	-	60	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	-	5	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	-	5	-	ns
BHE to Output in Low Z	t_{BLZ}	5	-	5	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

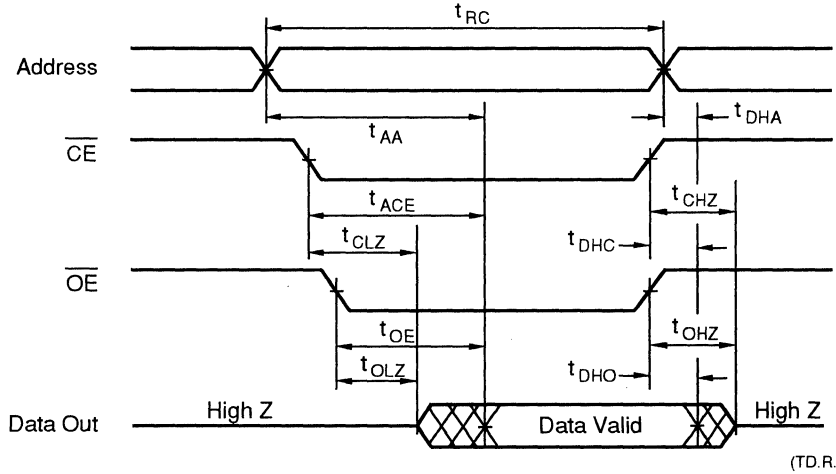
■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.4 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	120	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min.
Standby V_{CC} Current	I_{SB1}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
	I_{SB2}	-	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.4V
Input Voltage	V_{IH}	2.4	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.45	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ READ TIMING WAVEFORM

Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



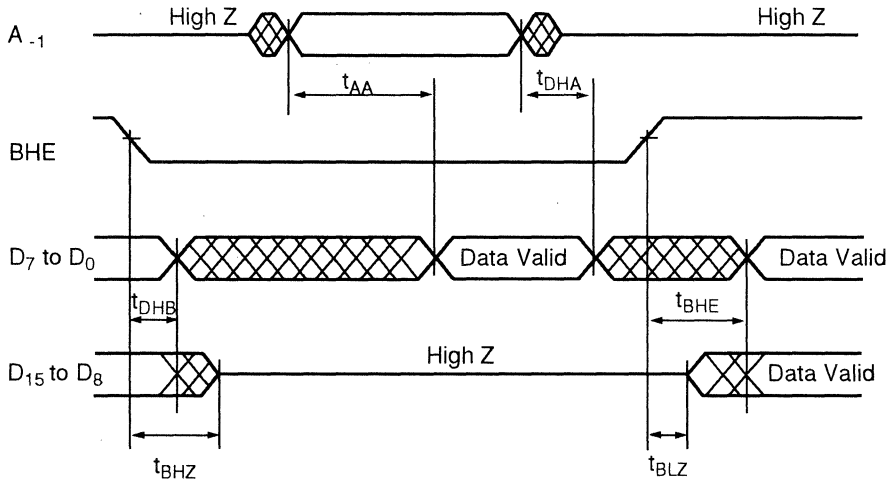
(TD.R.HN62438N)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

3

■ READ TIMING WAVEFORM

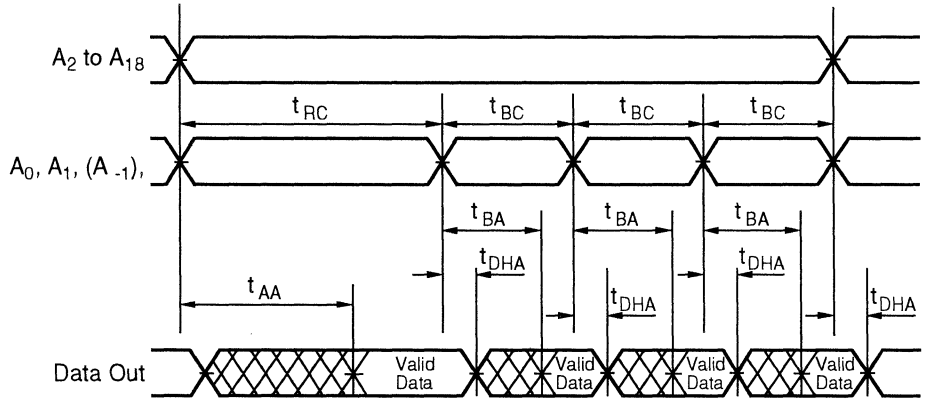
Word Mode/Byte Mode Switch



(TD.R1.HN62438N)

Note: 1. $\overline{CE}$ and $\overline{OE}$ are of select status. A_{18} to A_0 are fixed.
2. D_{15}/A_{-1} terminal is of output state when $\overline{BHE} = V_{IH}$, $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

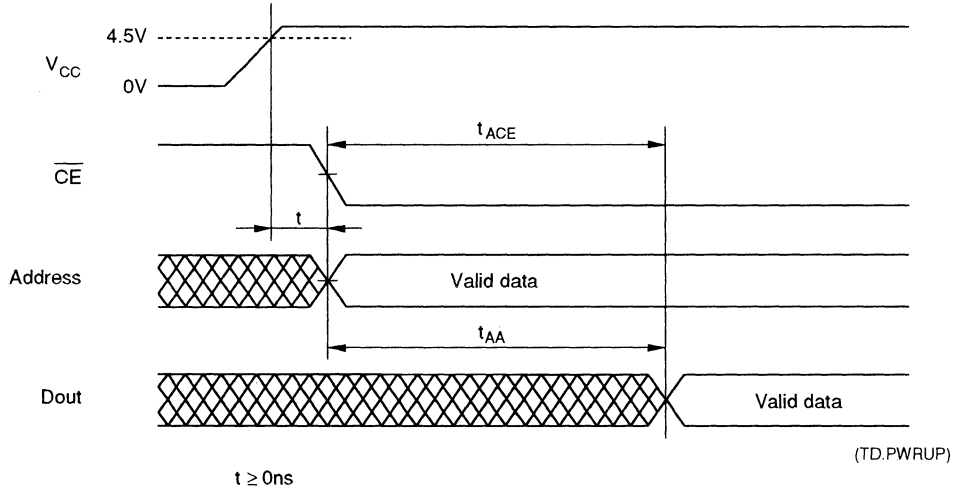
Fast Address Access



(TD.RN.HN62438N)

Note: $\overline{CE}$ and $\overline{OE}$ are enabled.

■ POWER-UP SEQUENCE



Note: This device uses an Address Transient Detector (ATD). After power-up to 4.5V, transfer either $\overline{CE}$ or Address.

3

16M (1M x 16-bit) and (2M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN624316 is a 16-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 16-bit and 2,097,152 x 8-bit.

The high density and high speed provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

Hitachi's HN624316 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP and 48-lead Plastic TOP packages. The HN624316 is also packaged in a 48-lead Plastic SOP.

■ FEATURES

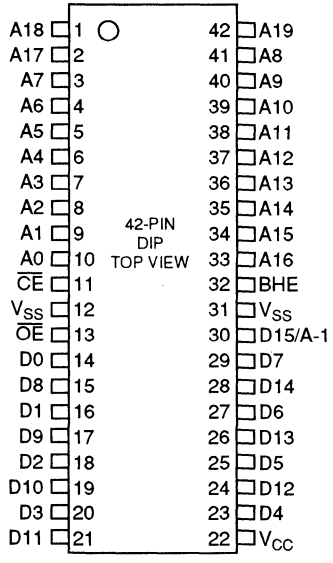
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Random Access Times:
  120 ns/150 ns (max)
- Low Power Consumption:
  Active Current: 300 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  1M x 16-bit (Word-Wide)
  2M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  48-lead Plastic SOP
  48-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN624316P	120 ns 150 ns	42-pin Plastic DIP (DP-42)
HN624316FB	120 ns 150 ns	44-lead Plastic SOP (FP-44D)
HN624316F	120 ns 150 ns	48-lead Plastic SOP (FP-48DA)
HN624316TT	120 ns 150 ns	48-lead Plastic TSOP (TTP-48D)

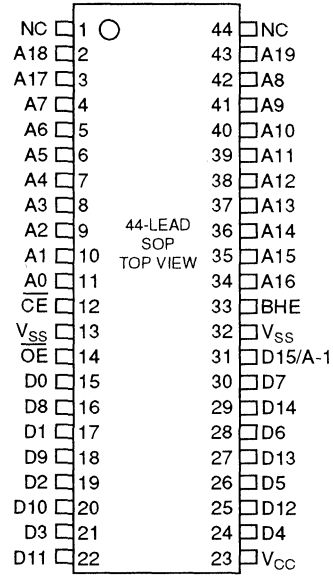
■ PIN ARRANGEMENT

HN624316P Series



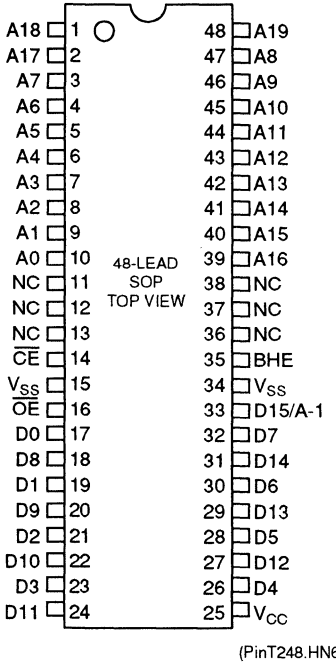
(PinD42.HN624316N)

HN624316FB Series



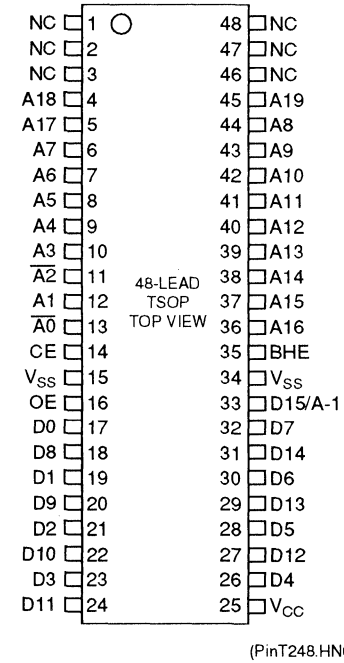
(PinT244.HN624316N)

HN624316F Series



(PinT248.HN624316N)

HN624316TT Series



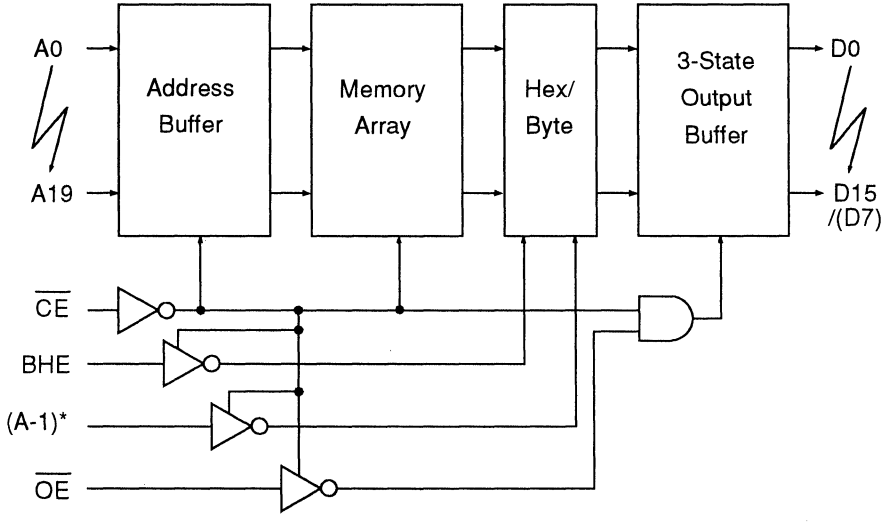
(PinT248.HN624116)

3

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{19}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN624116)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_{IN}, V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance [1]	C_{IN}	-	-	15	pF	V_{IN} = 0V
Output Capacitance [1]	C_{OUT}	-	-	15	pF	V_{OUT} = 0V

Notes: 1. This parameter is sampledand not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	100	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}=min
Standby V_{CC} Current	I_{SB1}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
	I_{SB2}	-	-	3	mA	V_{CC} = 5.5 V, CE ≥ 2.2V
Input Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -205 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 1.6 mA

3

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

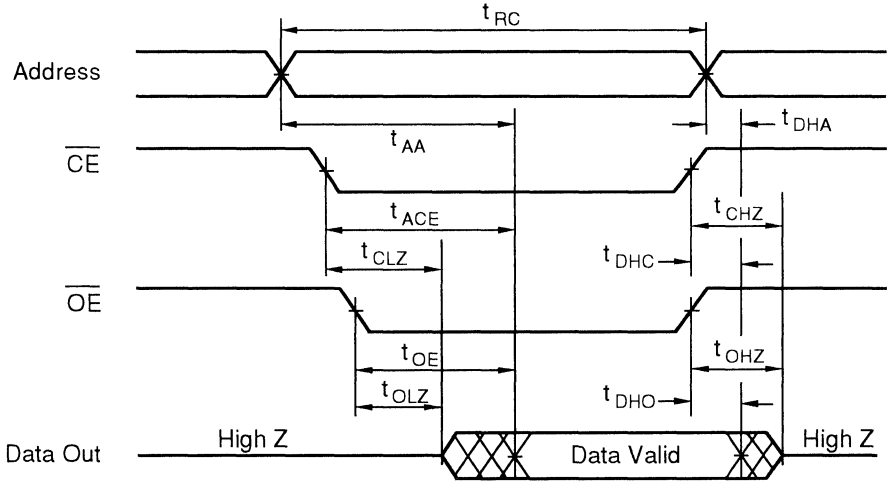
- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Reference level for measuring timing: 1.5 V

Item	Symbol	HN624316-12		HN624316-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120	-	150	-	ns
Address Access Time	t_{AA}	-	120	-	150	ns
Chip Enable Access Time	t_{ACE}	-	120	-	150	ns
Output Enable Access Time	t_{OE}	-	60	-	70	ns
BHE Access Time	t_{BHE}	-	120	-	150	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	60	-	70	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	60	-	70	ns
BHE to Output in High-Z [1]	t_{BHZ}	-	60	-	70	ns
Chip Enable to Output in Low-Z	t_{CLZ}	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	10	-	10	-	ns
BHE to Output in Low-Z	t_{BLZ}	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM

Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})

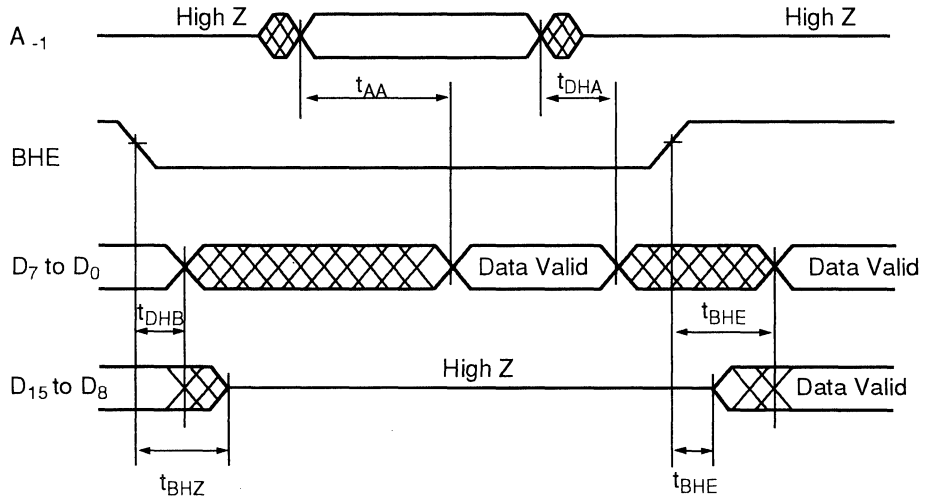


Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

(TD.R.HN624316N)

3

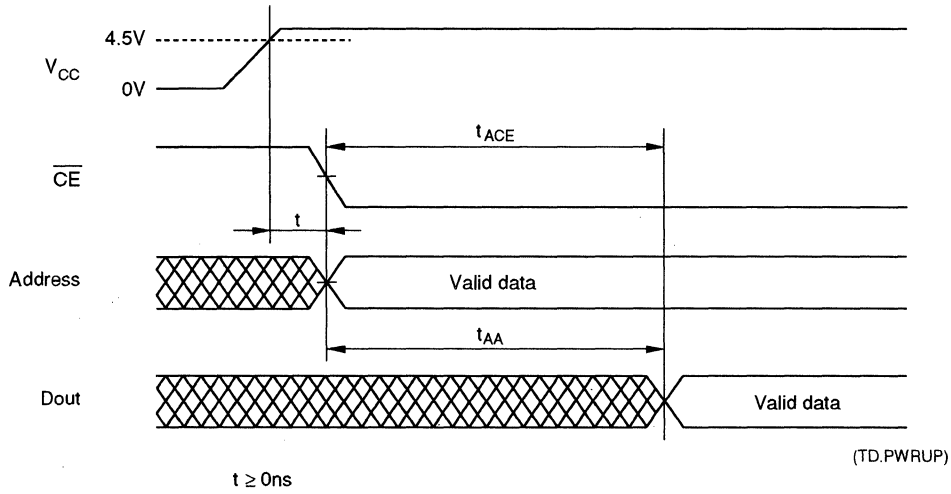
Word Mode/Byte Mode Switch



(TD.R1.HN624316N)

Note: 1. If $\overline{CE}$ and $\overline{OE}$ are enabled, A_{19} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

■ POWER-UP SEQUENCE



Note: This device uses an Address Transient Detector (ATD). After power-up to 4.5V, transfer either $\overline{CE}$ or Address.

16M (1M x 16-bit) and (2M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN624316N is a 16-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 16-bit and 2,097,152 x 8-bit.

The high density and high speed Fast Address Access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

Hitachi's HN624316N is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP and 48-lead Plastic TOP packages. The HN624316N is also packaged in a 48-lead Plastic SOP.

■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Random Access Times:
  120 ns/150 ns (max)
- Fast Address Access Times (A_0, A_1):
  60 ns/70 ns (max)
- Low Power Consumption:
  Active Current: 300 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  1M x 16-bit (Word-Wide)
  2M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  48-lead Plastic SOP
  48-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN624316NP	120 ns 150 ns	42-pin Plastic DIP (DP-42)
HN624316NFB	120 ns 150 ns	44-lead Plastic SOP (FP-44D)
HN624316NF	120 ns 150 ns	48-lead Plastic SOP (FP-48DA)
HN624316NTT	120 ns 150 ns	48-lead Plastic TSOP (TTP-48D)

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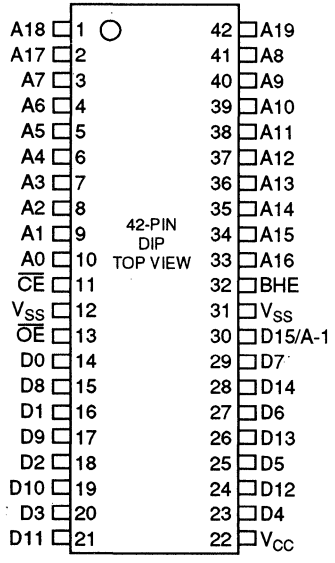
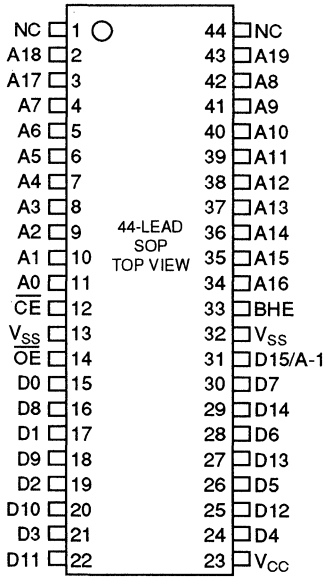
■ PIN ARRANGEMENT

HN624316NP Series



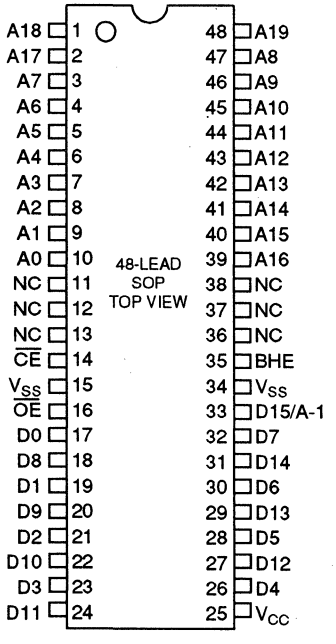
(PinD42.HN624316N)

HN624316NFB Series



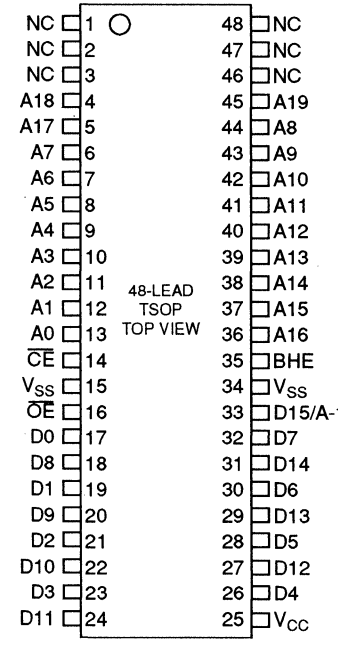
(PinT244.HN624316N)

HN624316NF Series



(PinT248.HN624316N)

HN624316NTT Series

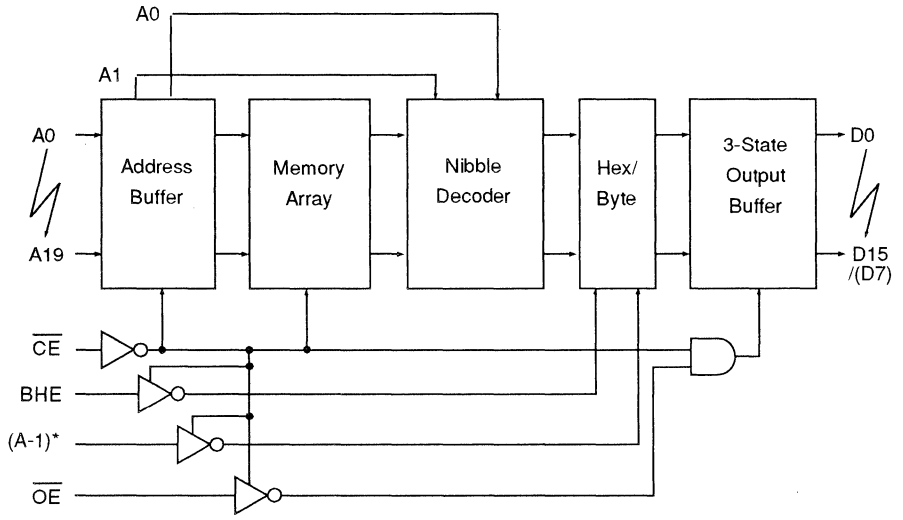


(PinT248.HN624116)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{19}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN624316N)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_{IN}, V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance [1]	C_{IN}	-	-	15	pF	V_{IN} = 0V
Output Capacitance [1]	C_{OUT}	-	-	15	pF	V_{OUT} = 0V

Notes: 1. This parameter is sampledand not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	120	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}=min
Standby V_{CC} Current	I_{SB}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -205 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Reference level for measuring timing: 1.5 V

Item	Symbol	HN624316N-12		HN624316N-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120	-	150	-	ns
Fast Address Read Cycle Time	t_{BC}	60	-	70	-	ns
Address Access Time	t_{AA}	-	120	-	150	ns
Fast Address Access Time	t_{BA}	-	60	-	70	ns
Chip Enable Access Time	t_{ACE}	-	120	-	150	ns
Output Enable Access Time	t_{OE}	-	60	-	70	ns
BHE Access Time	t_{BHE}	-	120	-	150	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	60	-	70	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	60	-	70	ns
BHE to Output in High-Z [1]	t_{BHZ}	-	60	-	70	ns
Chip Enable to Output in Low-Z	t_{CLZ}	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	10	-	10	-	ns
BHE to Output in Low-Z	t_{BLZ}	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, t_{BHZ} are defined as the time at which the output becomes an open circuit and are

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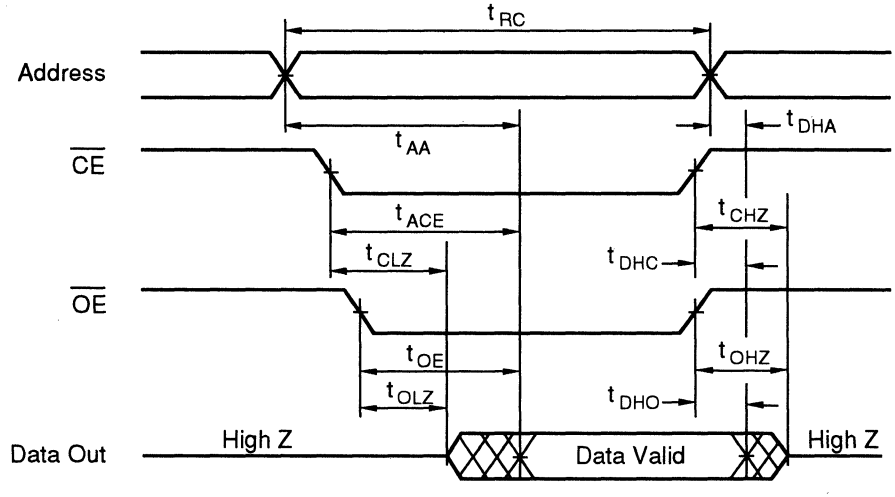
■ READ TIMING WAVEFORM

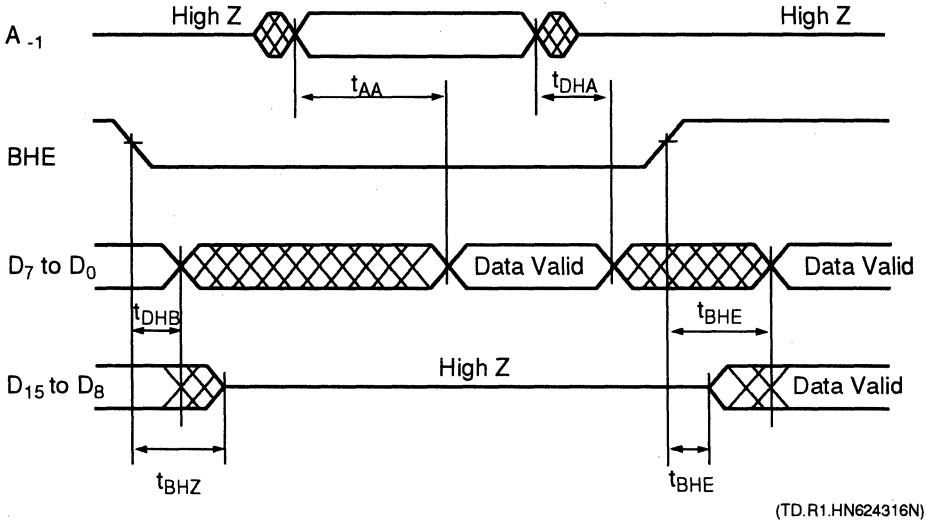
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

(TD.R.HN624316N)

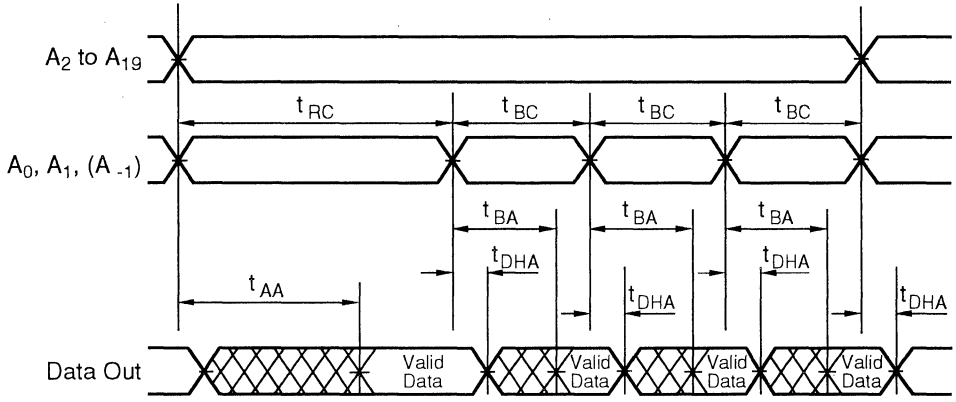
Word Mode/Byte Mode Switch



(TD.R1.HN624316N)

Note: 1. If $\overline{CE}$ and $\overline{OE}$ are enabled, A_{19} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

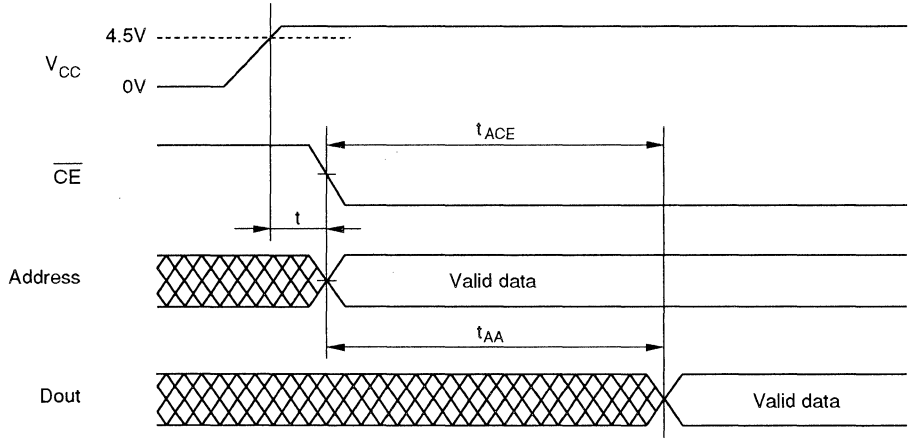
Fast Address Access



Note: $\overline{CE}$ and $\overline{OE}$ are enabled.

(TD.RN.HN624316N)

■ POWER-UP SEQUENCE



(TD.PWRUP)

t ≥ 0ns

Note: This device uses an Address Transient Detector (ATD). After power-up to 4.5V, transfer either $\overline{CE}$ or Address.

EPROM (UV Erasable and OTP)

SECTION 4

4

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

HN27C4096A Series

4M (256K x 16-bit) UV and OTP EPROM

■ DESCRIPTION

The Hitachi HN27C4096A is a 4-Megabit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 262,144 x 16-bits.

The HN27C4096A features fast address access times of 100, 120 and 150 ns and low power dissipation. This combination makes the HN27C4096A suitable for high speed 16 and 32-bit microcomputer systems. The HN27C4096A offers high speed programming using page programming mode.

Hitachi's HN27C4096A is offered in JEDEC-Standard Word-Wide EPROM pinouts in 40-pin Ceramic DIP and 44-lead Ceramic and Plastic LCC packages. This allows socket replacement with Mask ROMs.

The Ceramic DIP and Ceramic LCC packages are erasable by exposure to Ultraviolet light. The PLCC packaged device is One-Time Programmable and once programmed, can not be rewritten.

■ FEATURES

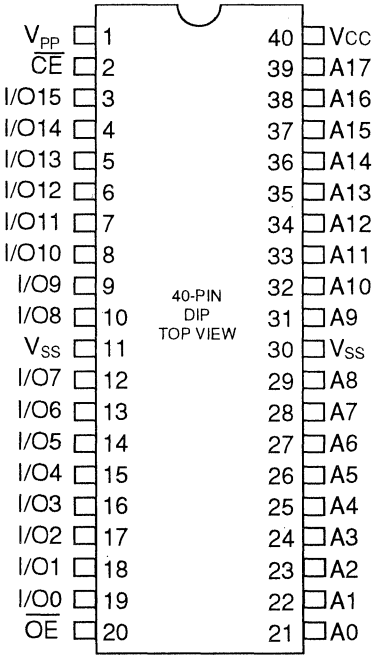
- Fast Access Times:
  100 ns/120 ns/150 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 35 mW/MHz (typ)
  Standby Mode: 5 µW (max)
- High Speed Page and Word Programming:
  Page Programming Time: 3.5 sec (min)
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Pin Arrangement:
  JEDEC Standard Word-Wide EPROM
  Mask ROM Compatible
- Packages:
  40-pin Ceramic DIP
  44-lead Ceramic LCC
  44-lead PLCC

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C4096AG-10	100 ns	40-pin Ceramic DIP
HN27C4096AG-12	120 ns	(DG-40A)
HN27C4096AG-15	150 ns	
HN27C4096ACC-10	100 ns	44-lead Ceramic LCC
HN27C4096ACC-12	120 ns	(CC-44)
HN27C4096ACC-15	150 ns	
HN27C4096ACP-12	120 ns	44-lead PLCC
HN27C4096ACP-15	150 ns	(CP-44)

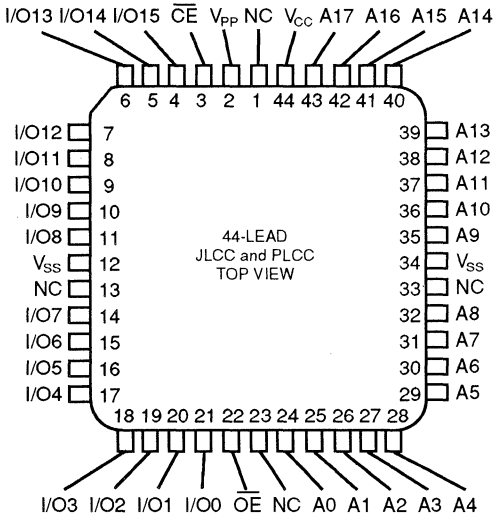
■ PIN ARRANGEMENT

HN27C4096AG Series



(PinD40.HN27C4096)

HN27C4096ACC Series
HN27C4096ACP Series

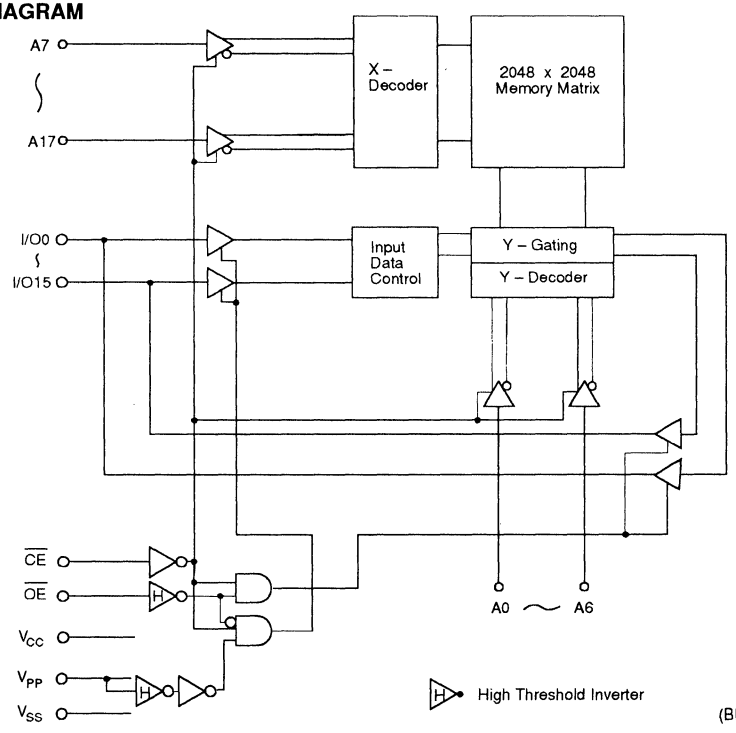


(PinQ44.HN27C4096)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
I/O_0 - I/O_{15}	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN27C4096)

■ MODE SELECTION

Mode		V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	A_9	I/O
Read		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IL}	X[1]	D_{OUT}
Output Disable		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
Standby		V_{SS}-V_{CC}	V_{CC}	V_{IH}	X	X	High-Z
Page Prog.	Page Prog. Set	V_{PP}	V_{CC}	V_{IH}	V_H[2]	X	High-Z
	Page Data Latch	V_{PP}	V_{CC}	V_{IL}	V_H	X	D_{IN}
	Page Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
	Page Prog. Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
	Page Prog. Reset	V_{CC}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Word Prog.	Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	D_{IN}
	Program Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
	Optional Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	X	D_{OUT}
	Program Inhibit	V_{PP}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Identifier		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_H	ID

Notes: 1. X = Don't Care. V_{PP} = 0 V to V_{CC}.
2. 11.5 V ≤ V_H ≤ 12.5 V

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 and $\overline{OE}$ Voltage [2]	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-65 to +125 [4] -55 to +125 [5]	°C
Storage Temperature Under Bias	T_{BIAS}	0 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT}, and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.
4. HN27C4096AG and HN27C4096ACC.
5. HN27C4096ACP.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	12	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	20	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 5.5 V/0.45 V
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	-	100	mA	I_{OUT} = 0 mA, f = 10 MHz
Standby V_{CC} Current	I_{SB1}	-	-	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	-	1	20	µA	$\overline{CE}$ = V_{CC} ± 0.3 V
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.3 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

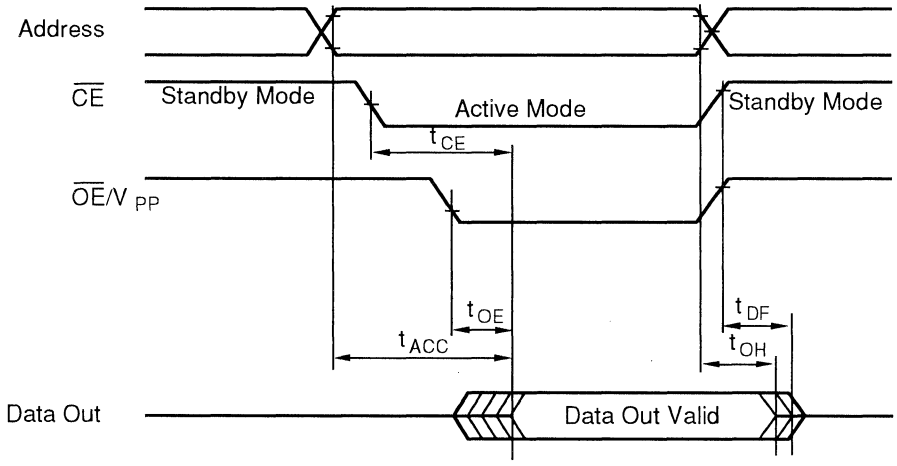
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V/2.0 V

Item	Symbol	HN27C4096A-10		HN27C4096A-12		HN27C4096A-15		Unit	Test Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	100	-	120	-	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	100	-	120	-	150	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	60	-	60	-	70	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	35	0	40	0	50	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C4096)

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■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 6.5 V/ 0.45 V
Operating V_{CC} Current	I_{CC}	-	-	50	mA	
Operating V_{PP} Current	I_{PP}	-	-	70 [7]	mA	$\overline{CE}$ = V_{IL}
Input Voltage [3]	V_{IH}	2.2	-	V_{CC} +.5 [6]	V	
	V_{IL}	- 0.1 [5]	-	0.8	V	
	V_H	11.5	12.0	12.5	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.
7. I_{PP} = 40 mA in Word Programming Mode.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 v ± 0.3 V, T_a = 25°C ± 5°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
Data Hold Time	t_{DH}	2	-	-	µs	
Chip Enable Setup Time	t_{CES}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Setup Time	t_{OES}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
Programming Pulse Width	t_{PW}	47.5	50.0	52.5	µs	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Chip Enable Pulse Width During Data Latch	t_{LW}	1	-	-	µs	
Output Enable = V_H Setup Time	t_{OHS}	2	-	-	µs	
Output Enable = V_H Hold Time	t_{OHH}	2	-	-	µs	
Output Enable Hold Time	t_{OEH}	2	-	-	µs	
V_{PP} Hold Time	t_{VRS}	1	-	-	µs	
Page Programming Reset Time	t_{VLW}	1	-	-	µs	

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

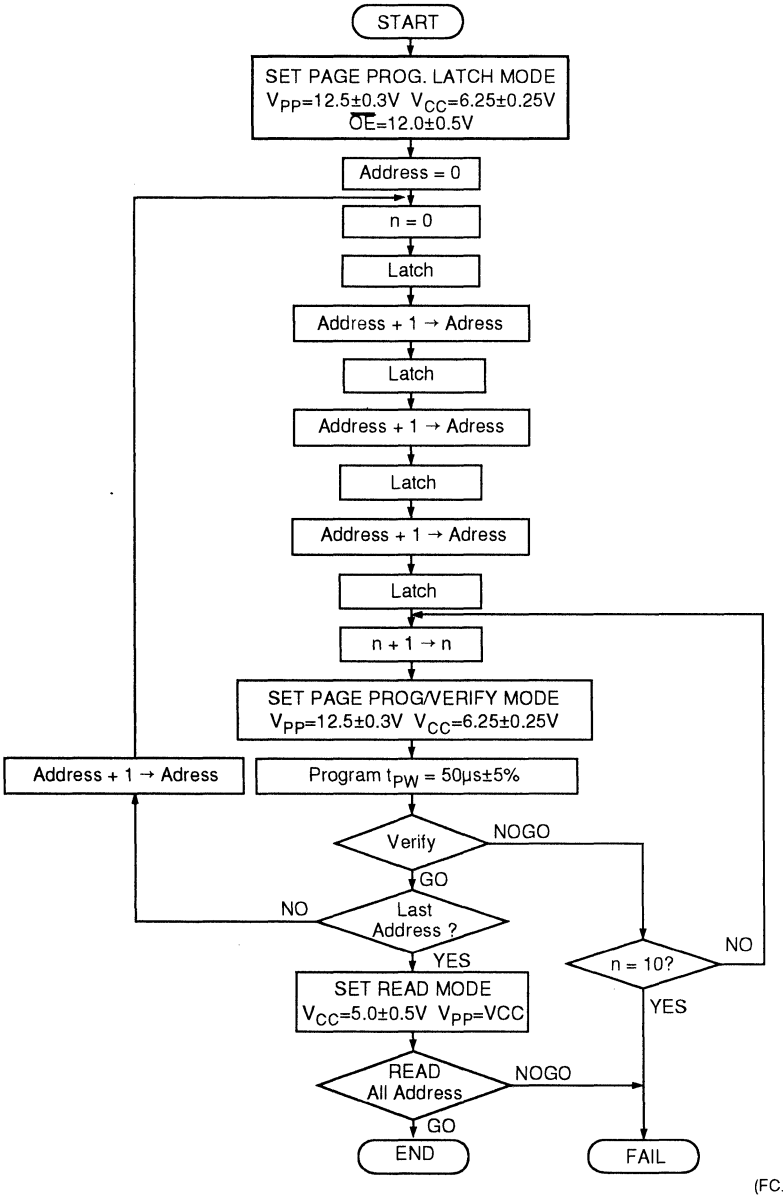
2. Page Program Mode will be reset when V_{PP} is set to V_{CC} or less.

4

■ PAGE PROGRAMMING FLOWCHART

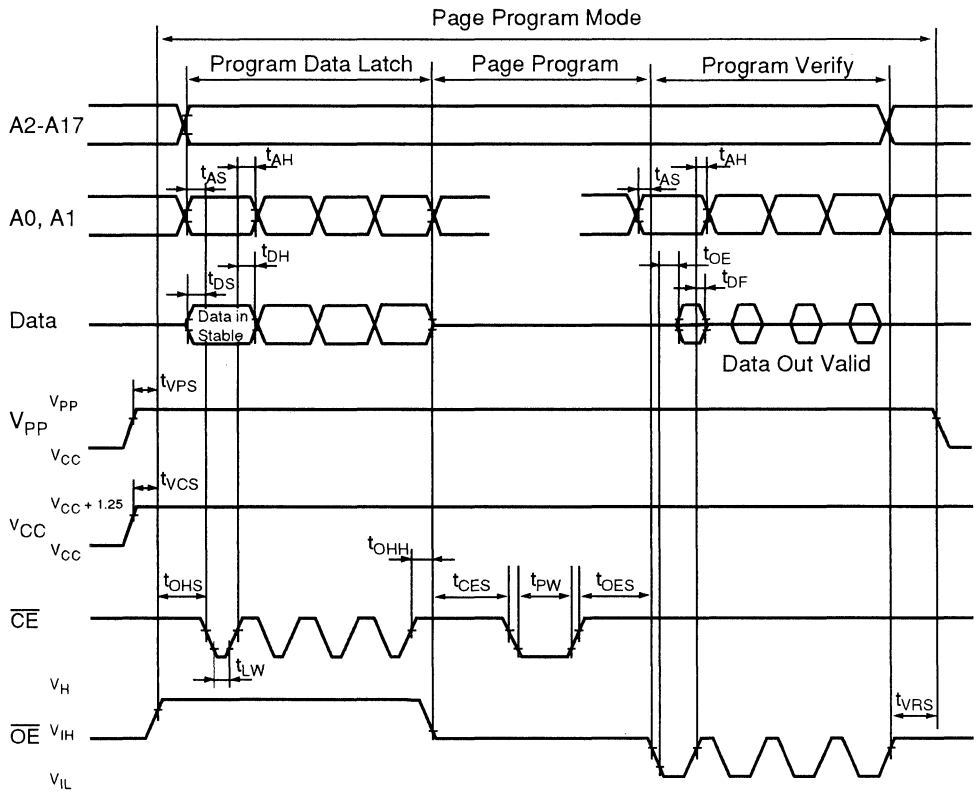
The Hitachi HN27C4096A can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

Note: 1. To set the device into Page Programming, apply 12.5 V to V_{PP} then followed by applying 12 V to $\overline{OE}$. The device operates in Page Program Mode until reset.
2. To reset the Page Program Mode, set $V_{PP} = V_{CC}$ or less.



(FC.PP.HN27C4096)

■ PAGE PROGRAMMING TIMING WAVEFORM

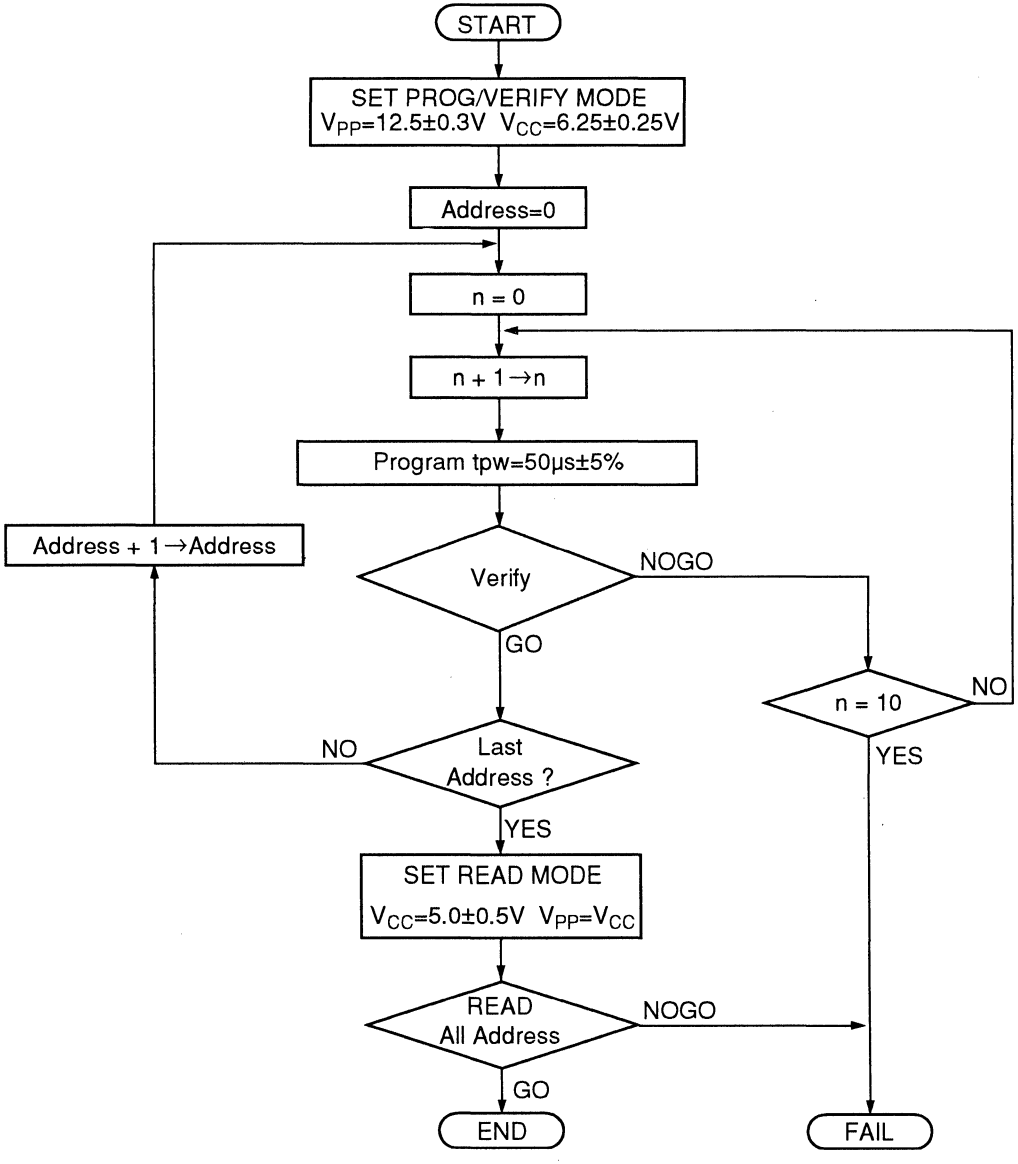


(TD.PP.HN27C4096)

4

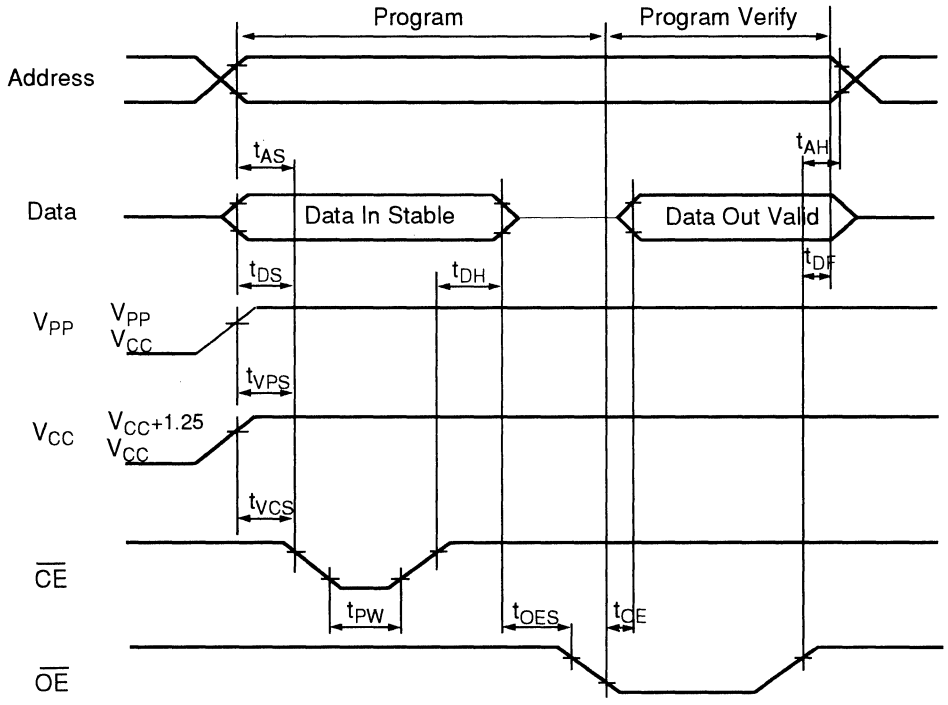
■ WORD PROGRAMMING FLOWCHART

The Hitachi HN27C4096A can be programmed with the high performance Word Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27C4096)

■ WORD PROGRAMMING TIMING WAVEFORM



(TD.P.HN27C4096)

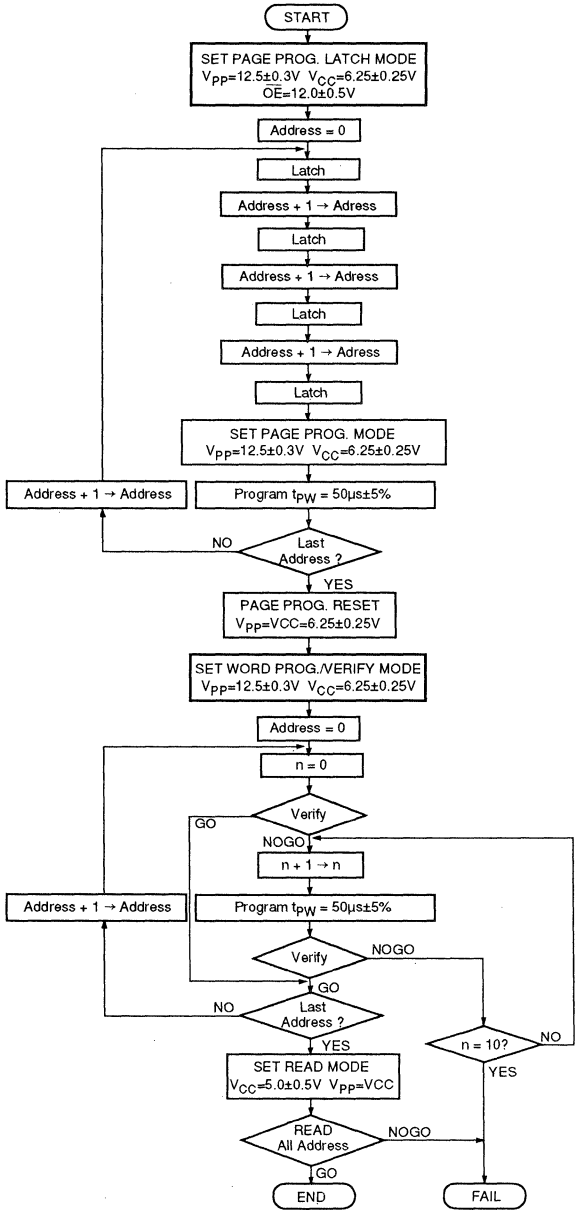
4

■ OPTIONAL PAGE PROGRAMMING FLOWCHART

The Hitachi HN27C4096A can be programmed with the high performance Optional Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

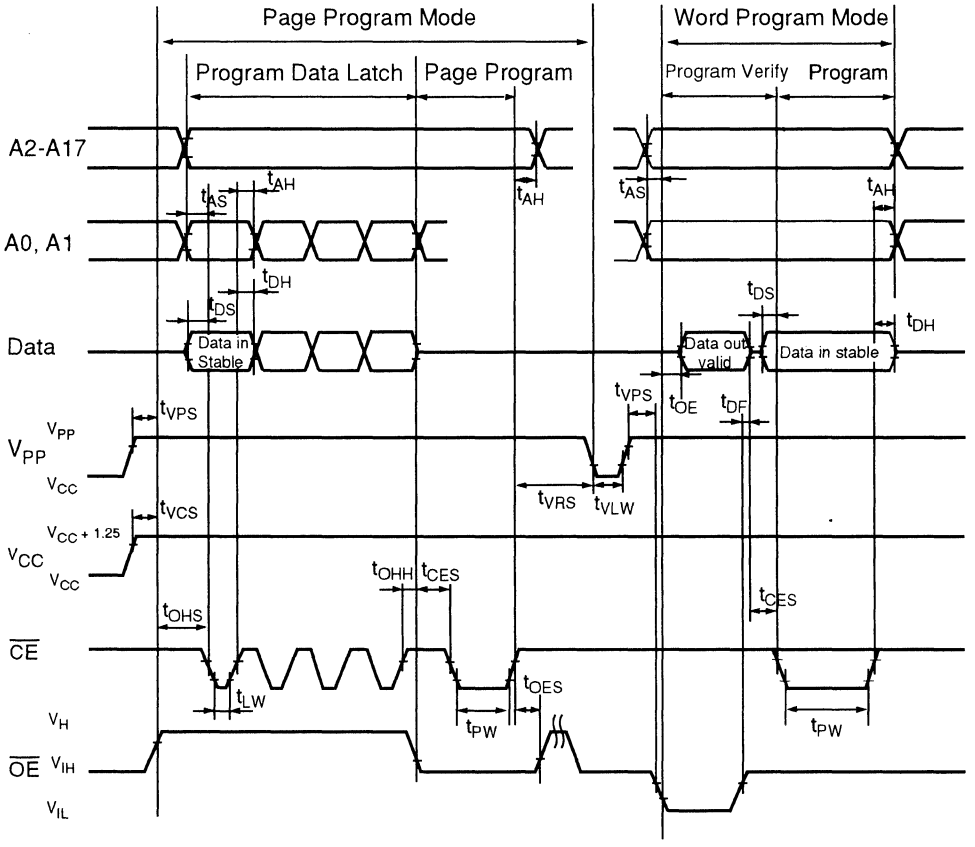
This programming algorithm is a combination of Page Programming and Word Verify. It can be used to avoid the increased programming verify time when a programmer with a slower machine cycle is used and shorten the total programming time.

Please refer to the timing specifications for page programming and word programming.



(FC.OPP.HN27C4096)

■ OPTIONAL PAGE PROGRAMMING TIMING WAVEFORM



(TD.OPP.HN27C4096)

4

■ ERASING THE HN27C4096A

The Hitachi HN27C4096A Ceramic DIP and Ceramic LCC packages allow these devices to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

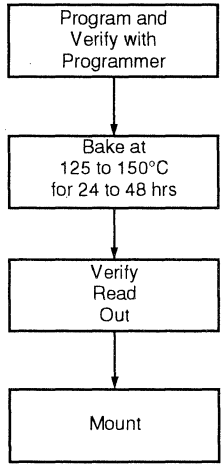
■ HN27C4096A SERIES IDENTIFIER CODE

Identifier	A_0	I/O_8-I/O_{15}	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	X	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	X	1	0	1	0	0	0	1	0	A2

Notes:
1. V_{CC} = 5.0 V ± 10%
2. A_9 = 12.0 V ± 0.5V
3. A_1-A_8, A_{10}-A_{17}, $\overline{CE}$, $\overline{OE}$ = V_{IL}
4. X = Don't Care

■ HN27C4096ACP RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C4096ACP package, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

4M (256K x 16-bit) UV and OTP EPROM

■ DESCRIPTION

The Hitachi HN27C4096AH is a 4-Megabit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 262,144 x 16-bits.

The HN27C4096AH features fast address access times of 85 and 100 ns with 45 ns 4-Word Burst Mode. This combination makes the HN27C4096AH suitable for high speed 16 and 32-bit microcomputer systems. The HN27C4096AH offers high speed programming using page programming mode.

Hitachi's HN27C4096AH is offered in JEDEC-Standard Word-Wide EPROM pinouts in 40-pin Ceramic DIP and 44-lead Ceramic and Plastic LCC packages. This allows socket replacement with Mask ROMs.

The Ceramic DIP and Ceramic LCC packages are erasable by exposure to Ultraviolet light. The PLCC packaged device is One-Time Programmable and once programmed, can not be rewritten.

■ FEATURES

- Fast Access Times:
  85 ns / 100 ns (max)
- Burst Access Times:
  45 ns / 45 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 35 mW/MHz (typ)
  Standby Mode: 30 mA (max)
- High Speed Page and Word Programming:
  Page Programming Time: 3.5 sec (min)
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Pin Arrangement:
  JEDEC Standard Word-Wide EPROM
  Mask ROM Compatible
- Packages:
  40-pin Ceramic DIP
  44-lead Ceramic LCC
  44-lead PLCC

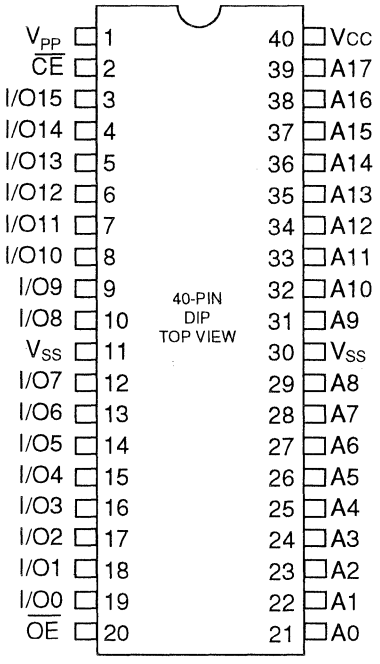
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C4096AHG-85	85 ns	40-pin Ceramic DIP (DG-40A)
HN27C4096AHCC-85	85 ns	44-lead Ceramic LCC (CC-44)
HN27C4096AHCP-10	100 ns	44-lead PLCC (CP-44)

4

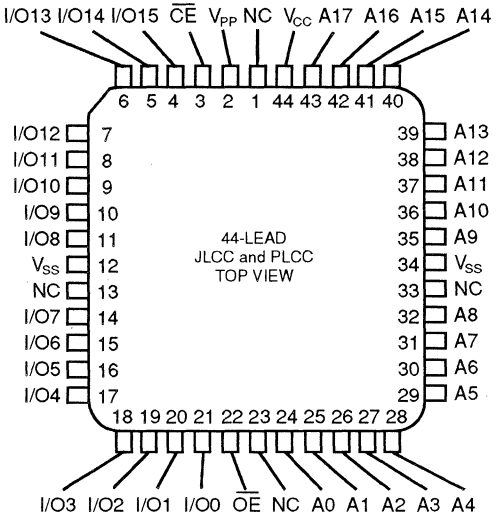
■ PIN ARRANGEMENT

HN27C4096AHG Series



(PinD40.HN27C4096)

HN27C4096AHCC Series
HN27C4096AHCP Series

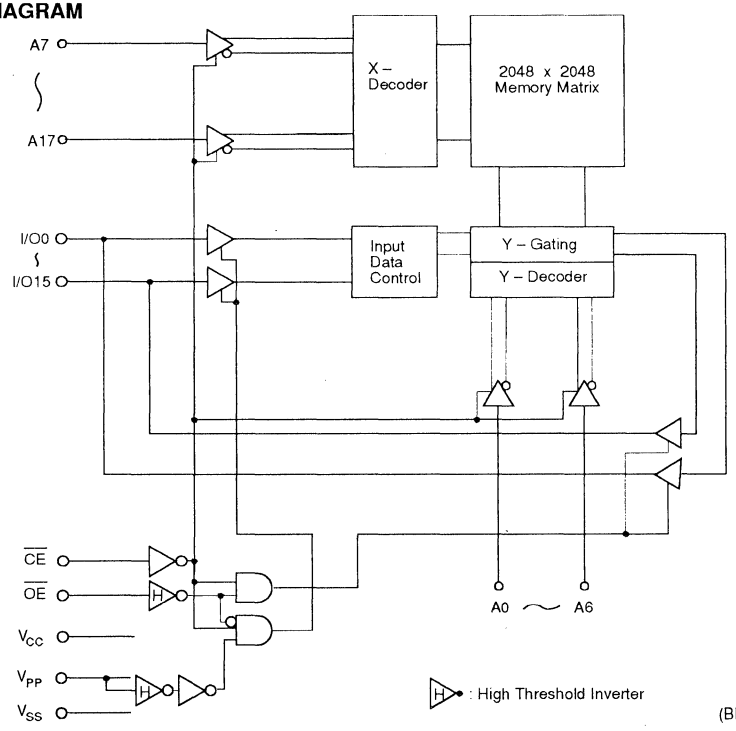


(PinQ44.HN27C4096)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
I/O_0 - I/O_{15}	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode		V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	A_9	I/O
Read		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IL}	X[1]	D_{OUT}
Output Disable		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
Standby		V_{SS}-V_{CC}	V_{CC}	V_{IH}	X	X	High-Z
Page Prog.	Page Prog. Set	V_{PP}	V_{CC}	V_{IH}	V_H[2]	X	High-Z
	Page Data Latch	V_{PP}	V_{CC}	V_{IL}	V_H	X	D_{IN}
	Page Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
	Page Prog. Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
	Page Prog. Reset	V_{CC}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Word Prog.	Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	D_{IN}
	Program Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
	Optional Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	X	D_{OUT}
	Program Inhibit	V_{PP}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Identifier		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_H	ID

Notes: 1. X = Don't Care. V_{PP} = 0 V to V_{CC}.
2. 11.5 V ≤ V_H ≤ 12.5 V

4

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 and $\overline{OE}$ Voltage [2]	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-65 to +125 [4] -55 to +125 [5]	°C
Storage Temperature Under Bias	T_{BIAS}	0 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT}, and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.
4. HN27C4096AHG and HN27C4096AHCC.
5. HN27C4096AHCP.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	12	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	20	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 5.5 V/0.45 V
Operating V_{CC} Current	I_{CC1}	-	-	35	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	-	140	mA	I_{OUT} = 0 mA, f = 11.7 MHz
Standby V_{CC} Current	I_{SB1}	-	-	30	mA	$\overline{CE}$ = V_{IH}
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.3 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

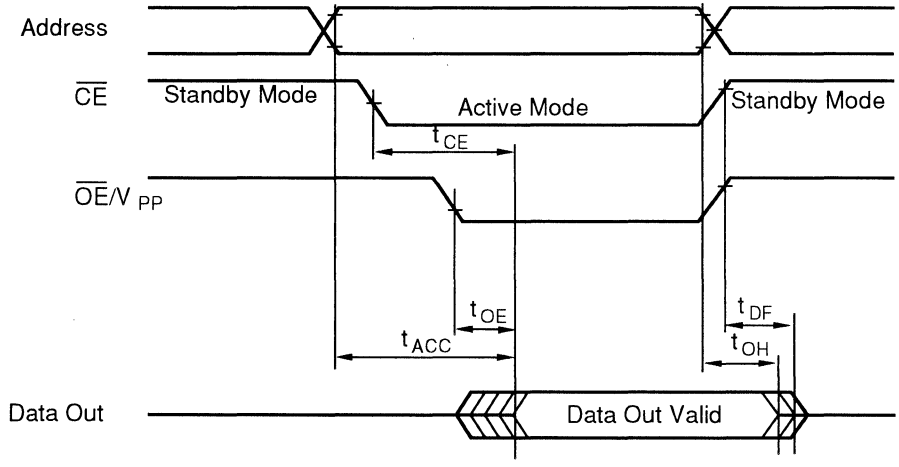
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V/2.0 V

Item	Symbol	HN27C4096AH-85		HN27C4096AH-10		Unit	Test Condition
		Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	85	-	100	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	85	-	100	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	45	-	60	ns	$\overline{CE}$ = V_{IL}
Burst Address Access	t_{BAC}	-	45	-	45	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	30	0	35	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

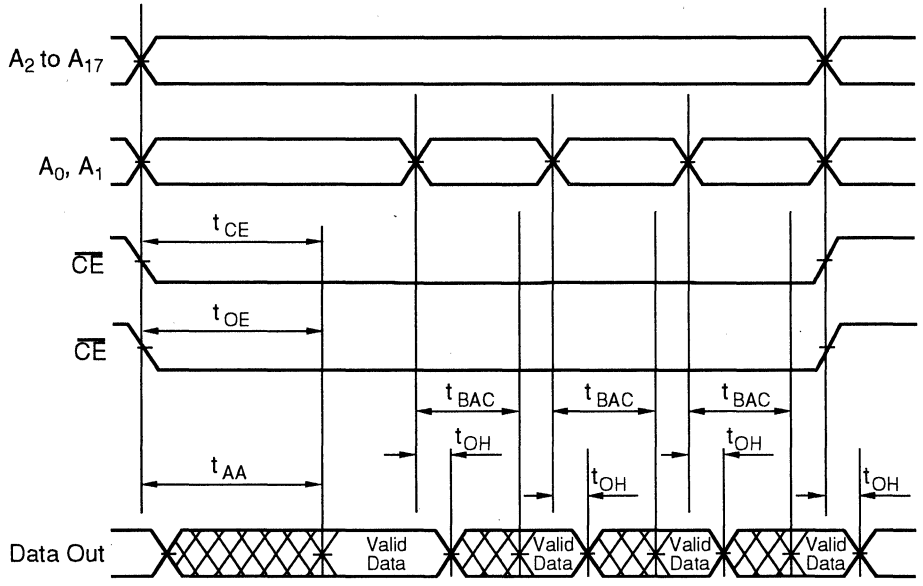
Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C4096)

■ READ TIMING WAVEFORM (BURST ACCESS MODE)



(TD.RNW.HN27C4000)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 6.5 V/ 0.45 V
Operating V_{CC} Current	I_{CC}	-	-	50	mA	
Operating V_{PP} Current	I_{PP}	-	-	70 [7]	mA	$\overline{CE}$ = V_{IL}
Input Voltage [3]	V_{IH}	2.2	-	V_{CC} +.5 [6]	V	
	V_{IL}	- 0.1 [5]	-	0.8	V	
	V_H	11.5	12.0	12.5	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.
7. I_{PP} = 40 mA in Word Programming Mode.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 v ± 0.3 V, T_a = 25°C ± 5°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
Data Hold Time	t_{DH}	2	-	-	µs	
Chip Enable Setup Time	t_{CES}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Setup Time	t_{OES}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
Programming Pulse Width	t_{PW}	47.5	50.0	52.5	µs	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Chip Enable Pulse Width During Data Latch	t_{LW}	1	-	-	µs	
Output Enable = V_H Setup Time	t_{OHS}	2	-	-	µs	
Output Enable = V_H Hold Time	t_{OHH}	2	-	-	µs	
Output Enable Hold Time	t_{OEH}	2	-	-	µs	
V_{PP} Hold Time	t_{VRS}	1	-	-	µs	
Page Programming Reset Time	t_{VLW}	1	-	-	µs	

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

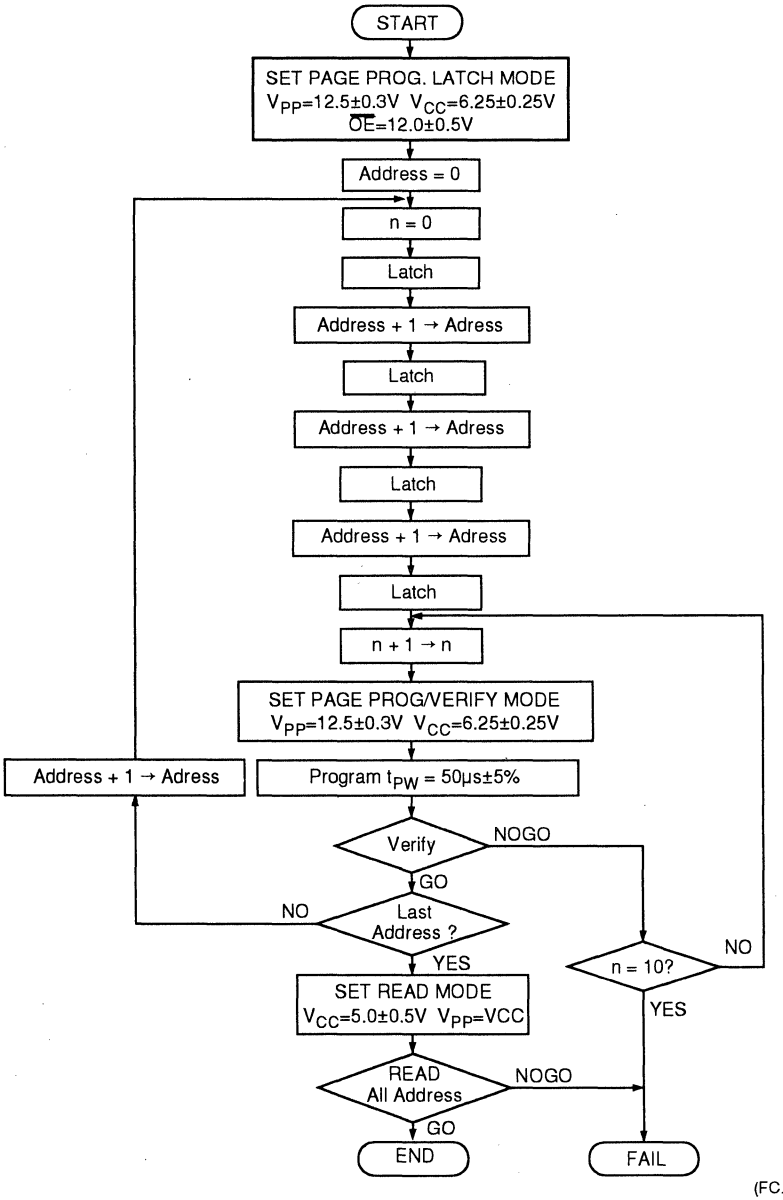
2. Page Program Mode will be reset when V_{PP} is set to V_{CC} or less.

4

■ PAGE PROGRAMMING FLOWCHART

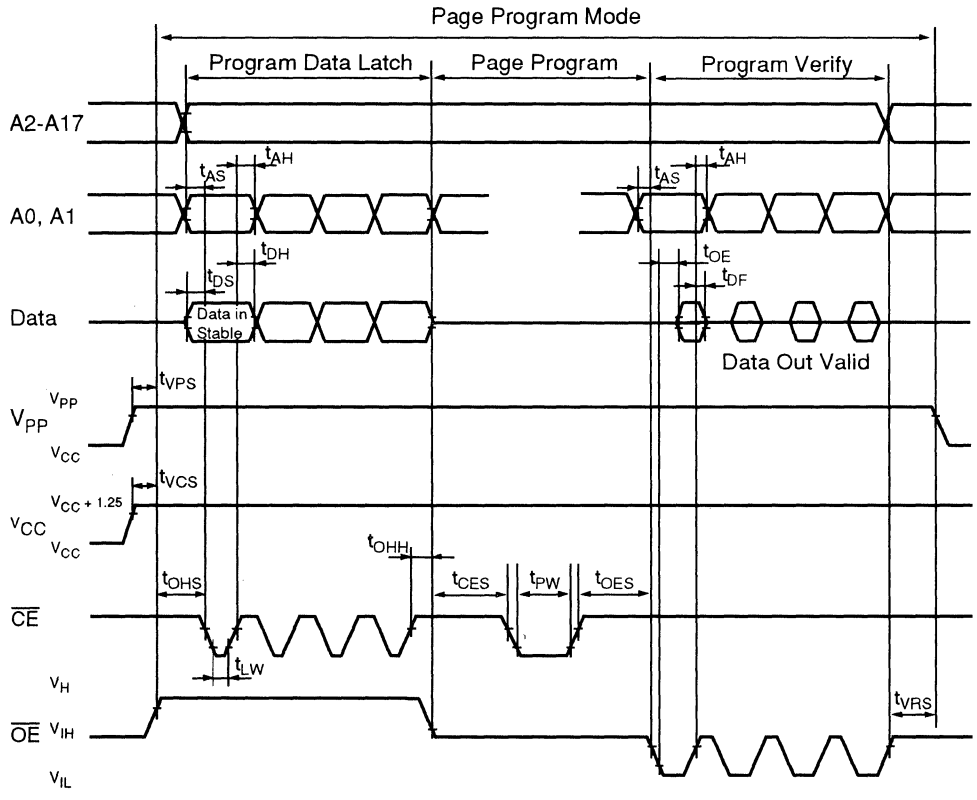
The Hitachi HN27C4096AH can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

Note: 1. To set the device into Page Programming, apply 12.5 V to V_{PP} then followed by applying 12 V to $\overline{OE}$. The device operates in Page Program Mode until reset.
2. To reset the Page Program Mode, set $V_{PP} = V_{CC}$ or less.



(FC.PP.HN27C4096)

■ PAGE PROGRAMMING TIMING WAVEFORM

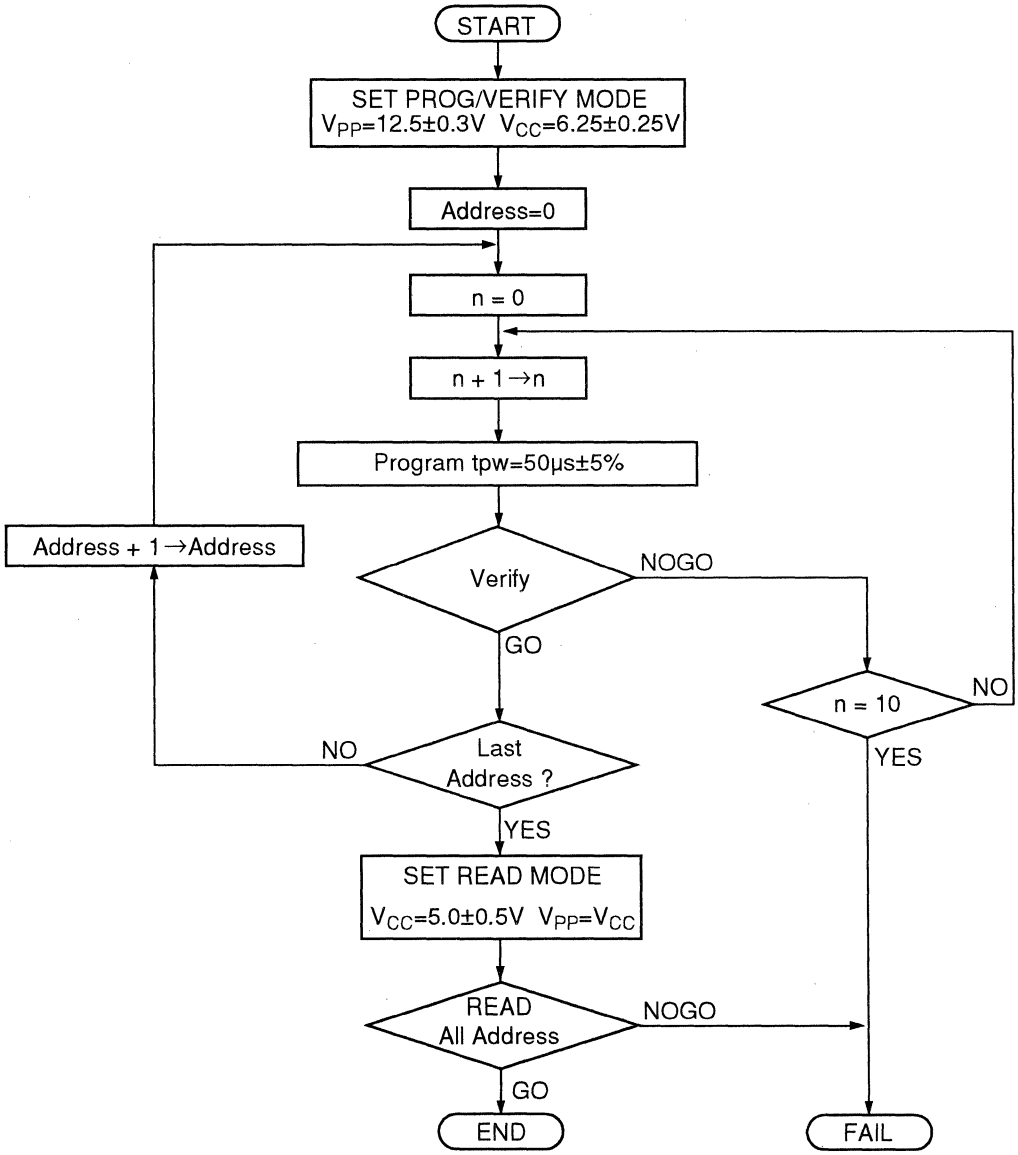


(TD.PP.HN27C4096)

4

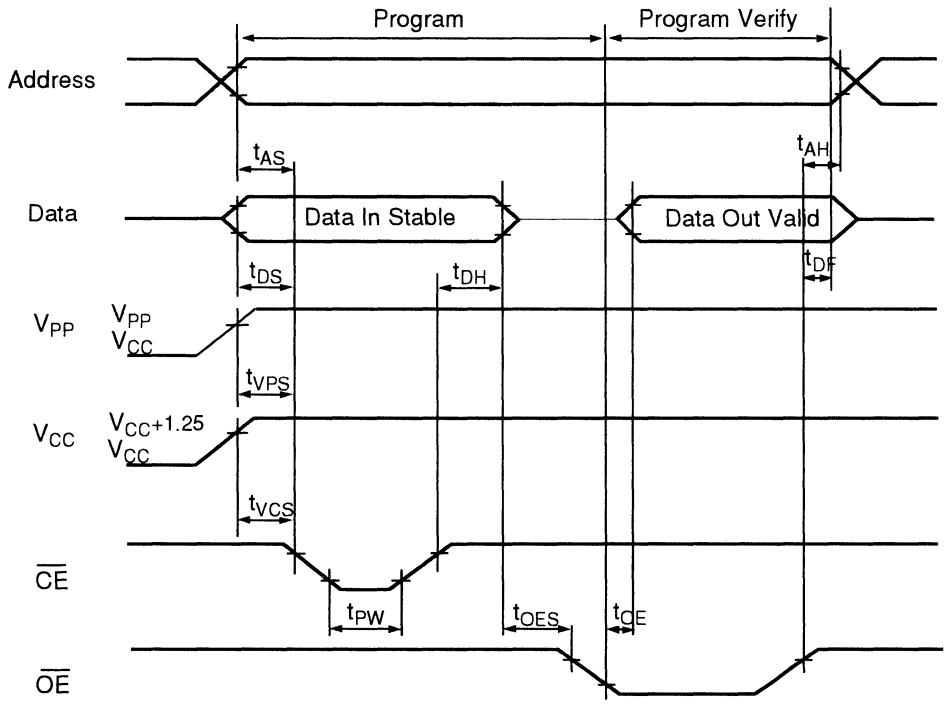
■ WORD PROGRAMMING FLOWCHART

The Hitachi HN27C4096AH can be programmed with the high performance Word Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27C4096)

■ WORD PROGRAMMING TIMING WAVEFORM



(TD.P.HN27C4096)

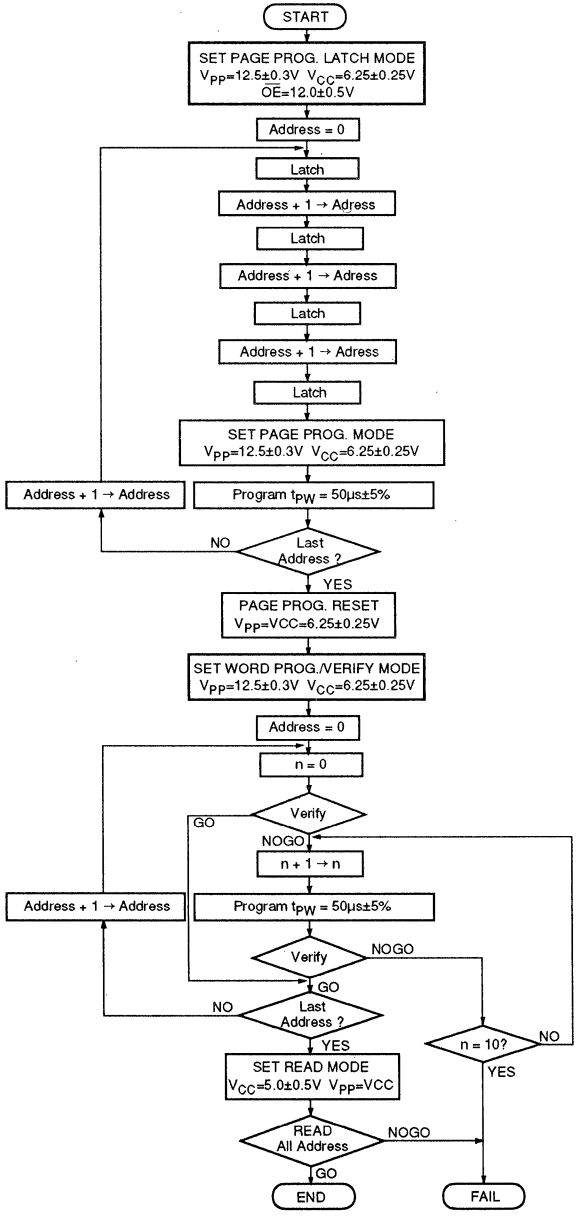
4

■ OPTIONAL PAGE PROGRAMMING FLOWCHART

The Hitachi HN27C4096AH can be programmed with the high performance Optional Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

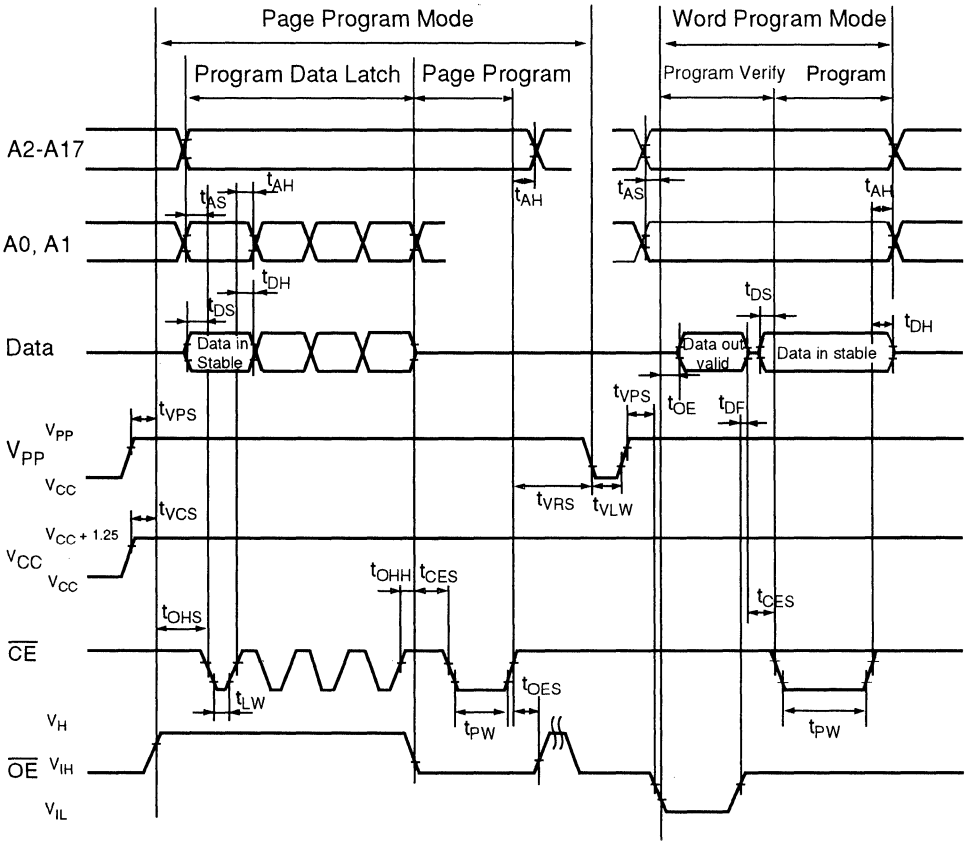
This programming algorithm is a combination of Page Programming and Word Verify. It can be used to avoid the increased programming verify time when a programmer with a slower machine cycle is used and shorten the total programming time.

Please refer to the timing specifications for page programming and word programming.



(FC.OPP.HN27C4096)

■ OPTIONAL PAGE PROGRAMMING TIMING WAVEFORM



(TD.OPP.HN27C4096)

4

■ ERASING THE HN27C4096AH

The Hitachi HN27C4096AH Ceramic DIP and Ceramic LCC packages allow these devices to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

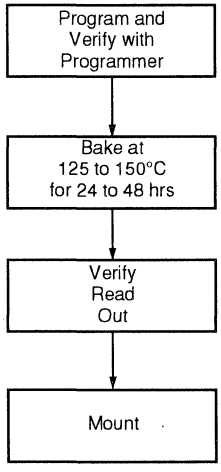
■ HN27C4096AH SERIES IDENTIFIER CODE

Identifier	A_0	I/O_8-I/O_{15}	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	X	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	X	1	0	1	0	0	0	1	0	A2

Notes:
1. V_{CC} = 5.0 V ± 10%
2. A_9 = 12.0 V ± 0.5V
3. A_1-A_8, A_{10}-A_{17}, $\overline{CE}$, $\overline{OE}$ = V_{IL}
4. X = Don't Care

■ HN27C4096AHCP RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C4096AHCP package, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

EEPROM

SECTION 5
EEPROM

5

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

256K (32K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58C256 is a 256-Kilobit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 32,768 x 8-bits. The HN58C256 is capable of in-system electrical Byte and Page reprogrammability.

The HN58C256 achieves fast address access, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58C256 has a 64-Byte Page Programming function to make its erase and write operations faster. The HN58C256 features Data Polling to indicate completion of erase and programming operations.

The HN58C256 provides several levels of data protection. Hardware data protection is provided with noise protection on the $\overline{WE}$ signal and write inhibit on power on and off.

The HN58C256 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

The Hitachi HN58C256 is offered in JEDEC-Standard Byte-Wide EEPROM pinouts in 28-pin Plastic DIP and 28-lead SOP packages.

■ FEATURES

- Single Power Supply:
  V_{cc} = 5V ± 10%
- Fast Access Time:
  200 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 200 µW (typ)
- Automatic Programming:
  Automatic Page Write: 10 ms (max)
  64 Byte Page Size
  Automatic Byte Write: 10 ms (max)
- Data Polling
- Data Protection Circuitry on Power On/Off
- Data Retention: 10 years
- Erase/Write Endurance:
  100,000 cycles in Page Mode
- Pin Arrangement:
  JEDEC Standard Byte-Wide EEPROM
- Packages:
  28-pin Plastic DIP
  28-lead Plastic SOP

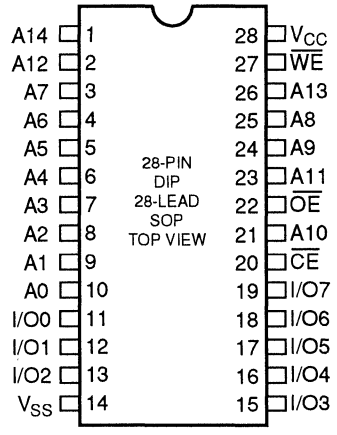
5

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58C256P-20	200 ns	28-pin Plastic DIP (DP-28)
HN58C256FP-20	200 ns	28-lead Plastic SOP (FP-28D)

■ PIN ARRANGEMENT

HN58C256P Series
HN58C256FP Series

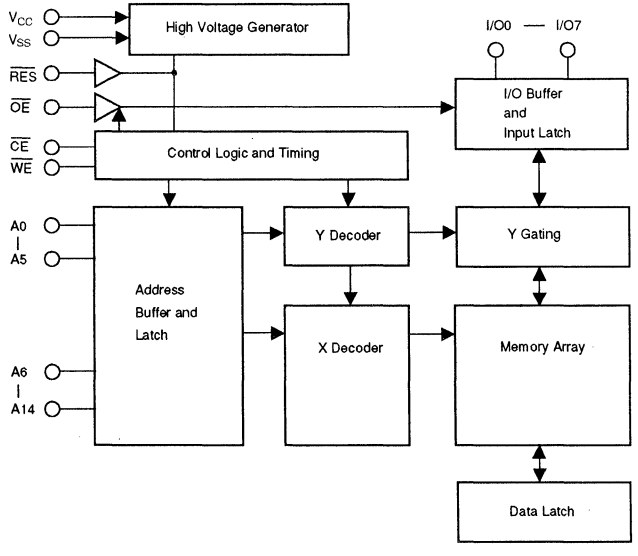


(PinD32.HN58C256)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{14}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



(BD.HN58C256)

■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z
Write Inhibit	X	X	V_{IH}	-
	X	V_{IL}	X	
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	Data Out (I/O_7)

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.
3. Including electrical characterisitics and data retention.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

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■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	200	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	12	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 1 µs
		-	-	30	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 200 ns
Input Voltage	V_{IL}	-0.3 [1]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 1	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{IL} min = -3.0 V for pulse width ≤ 50 ns.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

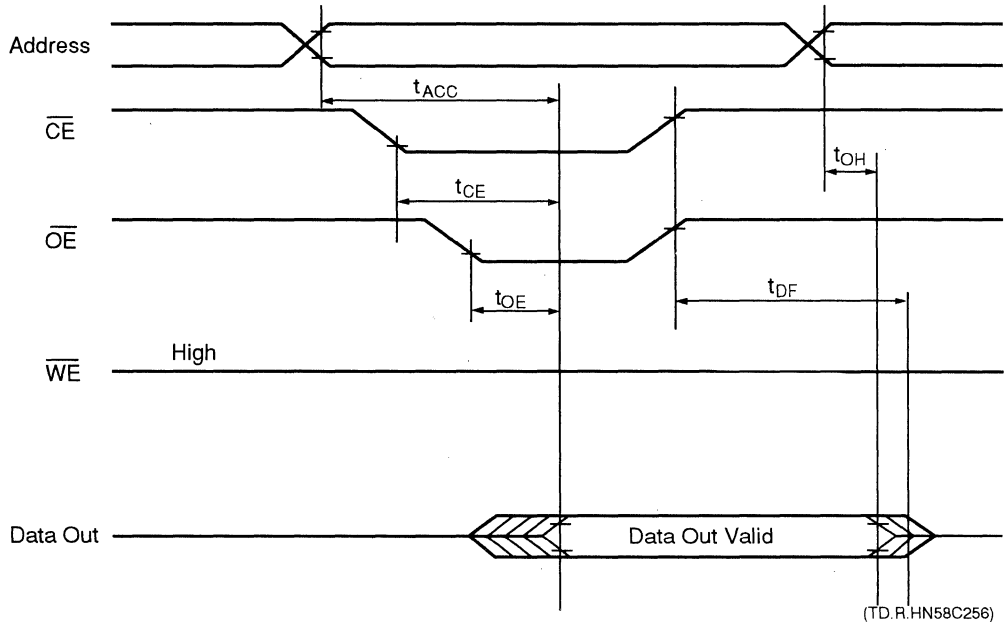
Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN58C256-20 Min.	HN58C256-20 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	200	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z[1]	t_{DF}	0	70	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{CW}[3]	150	-	-	ns	
	t_{WP}[2]	150	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	

Note: 1. Use this device in a longer cycle than this value.
2. Write Enable controlled operation.
3. Chip Enable controlled operation.

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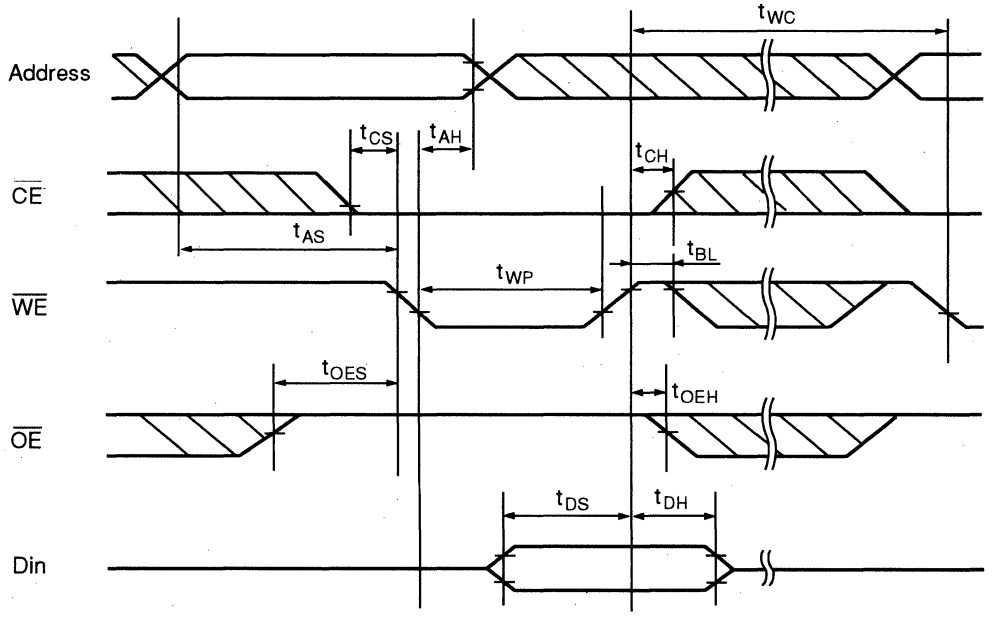
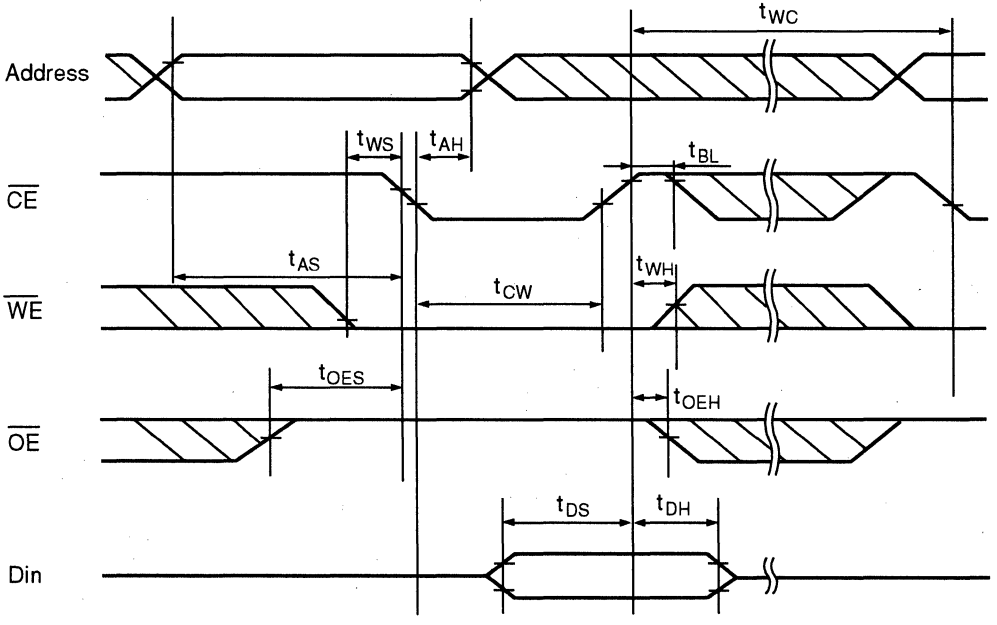
■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.BE1.HN58C256)

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



(TD.BE2.HN58C256)

■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	150	-	-	ns	
	t_{CW}[3]	150	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	200	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	0.35	-	30	µs	

Notes: 1. Use this device in longer cycle than this value.
2. Write Enable controlled operation.
3. Chip Enable controlled operation.

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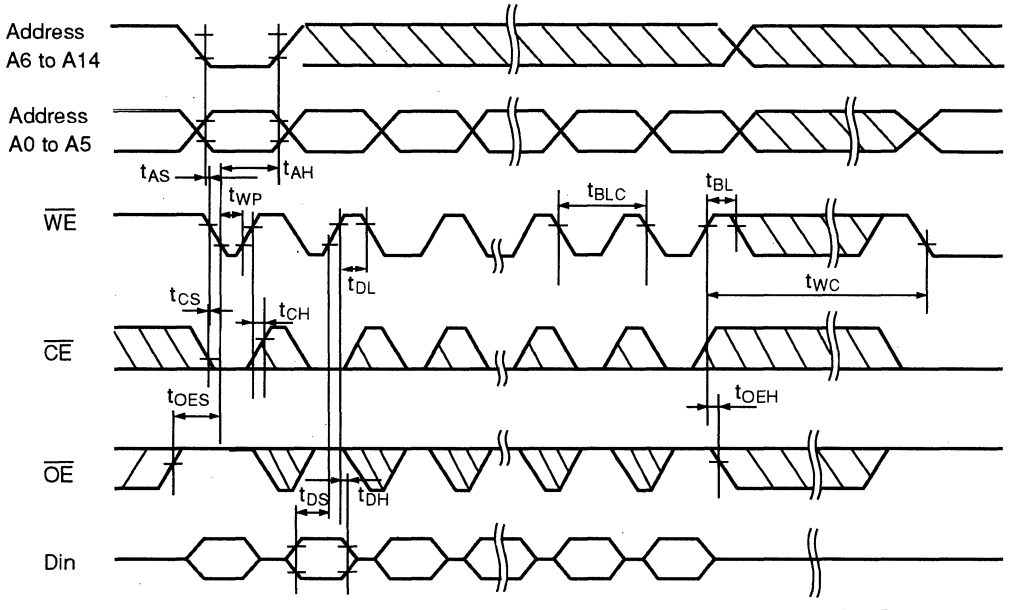
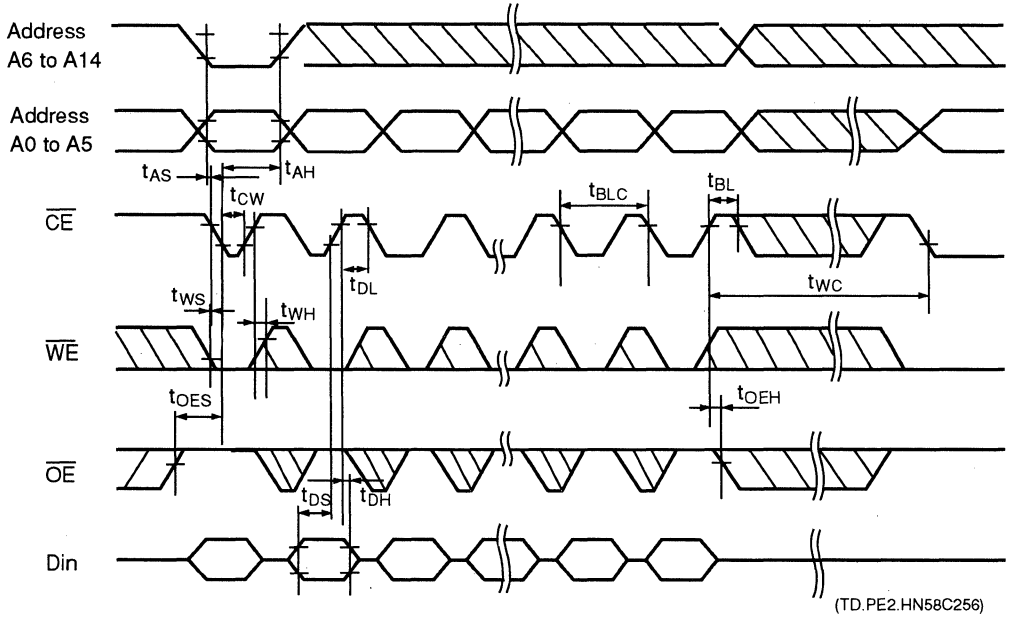
■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.PE1.HN58C256)

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)

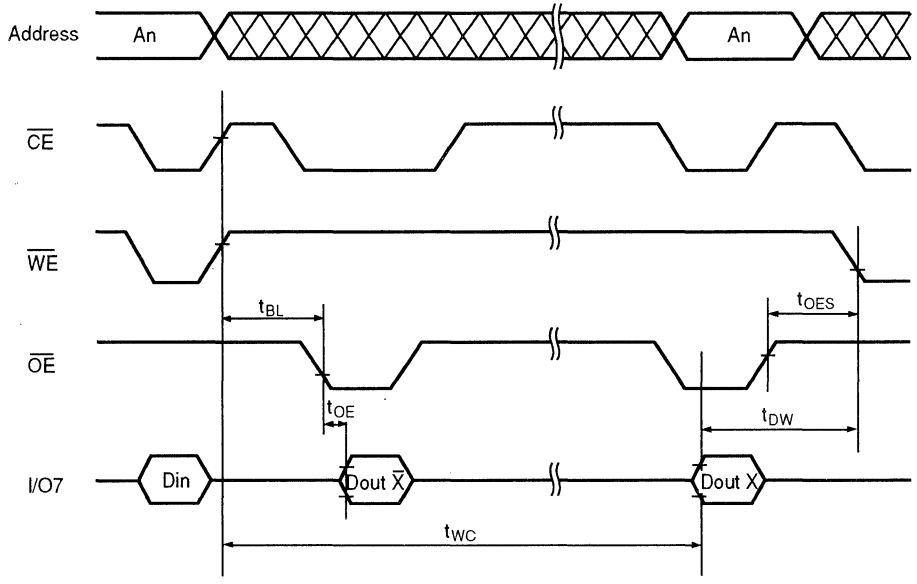


(TD.PE2.HN58C256)

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{DATA}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Byte Load Window	t_{BL}	100	-	-	µs	
Output Enable to Output Delay	t_{OE}	10	-	90	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	10	ms	

■ $\overline{DATA}$ POLLING TIMING WAVEFORM



(TD.DP.EE)

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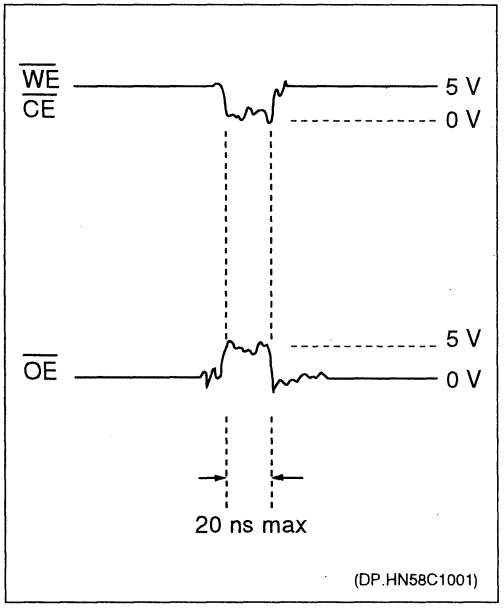
■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 64 Bytes of data to be written into the EEPROM in a single write cycle. Following the initial Byte cycle, an additional 1 to 63 Bytes can be written in the same manner. Each additional Byte load cycle must be started within 30 μs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{WE}$ or $\overline{CE}$ is high for 100 μs after data input, the EEPROM enters erase and write mode automatically and only the input data is written into the EEPROM. Data can be written and accessed 10^5 times in 64 Byte units.



$\overline{Data}$ Polling

$\overline{Data}$ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

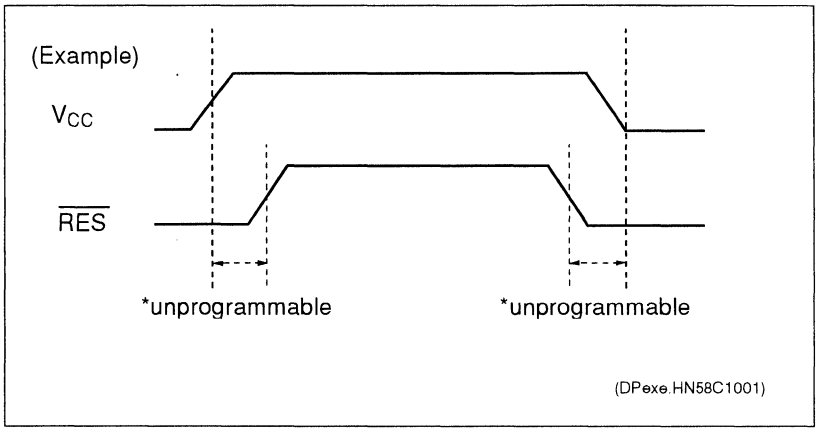
Write/Erase Endurance and Data Retention

The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58C256 has:

1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58C256 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.



■ **FUNCTIONAL DESCRIPTION (continued)**

Data Protection (continued)

2. Data protection at V_{CC} on/off
   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.
   In addition, when V_{CC} is turned on or off, the input level of the control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) must be held as $\overline{CE}=V_{CC}$ or $\overline{OE}=V_{SS}$ or $\overline{WE}=V_{CC}$ level.

5

256K (32K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58C257 is a 256-Kilobit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 32,768 x 8-bits. The HN58C257 is capable of in-system electrical Byte and Page reprogrammability.

The HN58C257 achieves high speed access, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58C257 has a 64-Byte Page Programming function to make its erase and write operations faster. The HN58C257 features $\overline{\text{Data}}$ Polling and a Ready/$\overline{\text{Busy}}$ signal to indicate completion of erase and programming operations.

The HN58C257 provides several levels of data protection. Hardware data protection is provided with the $\overline{\text{RES}}$ pin, in addition to noise protection on the $\overline{\text{WE}}$ signal and write inhibit on power on and off.

The HN58C257 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

The HN58C257 is offered in a 32-lead Plastic TSOP package in both standard and reverse bend pinouts.

■ FEATURES

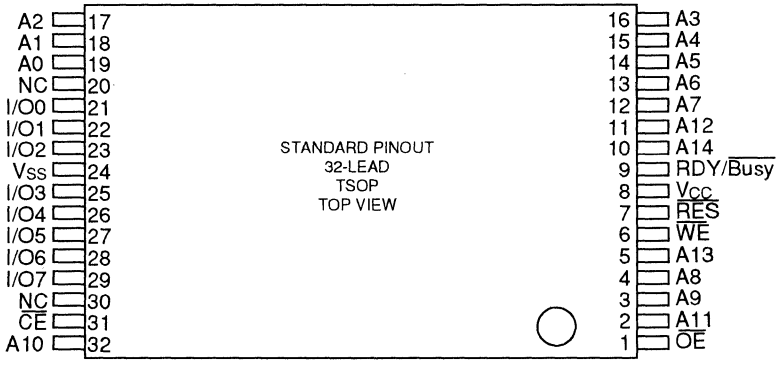
- Single Power Supply:
  V_{cc} = 5V ± 10%
- Fast Access Time:
  200 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 200 µW (typ)
- Automatic Programming:
  Automatic Page Write: 10 ms (max)
  64 Byte Page Size
  Automatic Byte Write: 10 ms (max)
- $\overline{\text{Data}}$ Polling and Ready/$\overline{\text{Busy}}$ Signals
- Hardware Data Protection with $\overline{\text{RES}}$ pin
- Data Protection Circuitry on Power On/Off
- Data Retention: 10 years
- Erase/Write Endurance:
  100,000 cycles in Page Mode
- Packages:
  32-lead Plastic TSOP (Type I)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58C257T-20	200 ns	32-lead Plastic TSOP (TFP-32DA)
HN58C257R-20	200 ns	32-lead Plastic TSOP (TFP-32DAR) Reverse bend

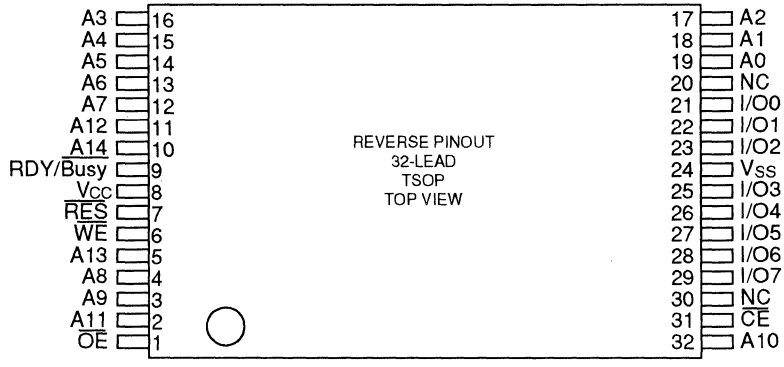
■ PIN ARRANGEMENT

HN58C257T Series



(PinT132.HN58C257T)

HN58C257R Series



(PinT132.HN58C257R)

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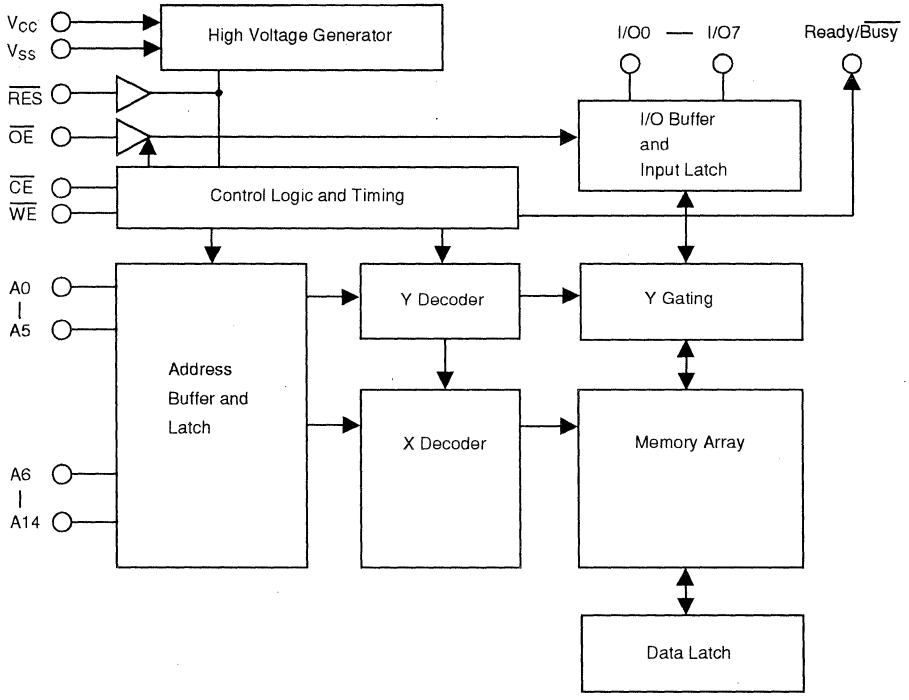
■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{14}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
Rdy/$\overline{Busy}$	Ready/Busy
$\overline{RES}$	Reset

■ BLOCK DIAGRAM



(BD.HN58C257)

■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	D_{OUT}
Standby	V_{IH}	X	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z→V_{OL}	D_{IN}
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	High-Z	-
	X	V_{IL}	X	X	High-Z	-
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O_7)
Program	X	X	X	V_{IL}	High-Z	High-Z

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.
3. Including electrical characterisitics and data retention.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

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■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI} [1]	-	-	2	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	200	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	12	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 1 µs, V_{CC} = 5.5 V
		-	-	30	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 200 ns, V_{CC} = 5.5 V
Input Voltage	V_{IL}	-0.3 [2]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 1	V	
	V_H	V_{CC} - 0.5	-	V_{CC} + 1	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. I_{LI} on $\overline{RES}$ = 100 mA max.
2. V_{IL} min = -3.0 V for pulse width ≤ 50 ns.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

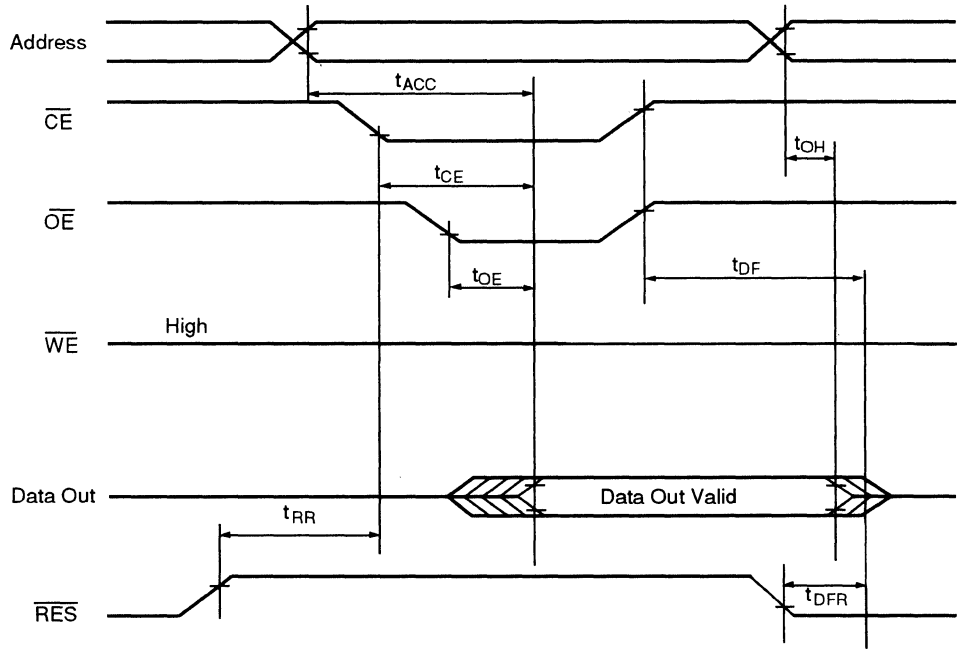
Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN58C257-20 Min.	HN58C257-20 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	200	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z [1]	t_{DF}	0	70	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to Output Delay	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN58C1001)

■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}	0	-	-	ns	
Write Pulse Width	t_{CW}	150	-	-	ns	
	t_{WP}	150	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Write Enable Hold Time	t_{WH}	0	-	-	ns	
Chip Enable Hold Time	t_{CH}	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Note: 1. Use this device in a longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

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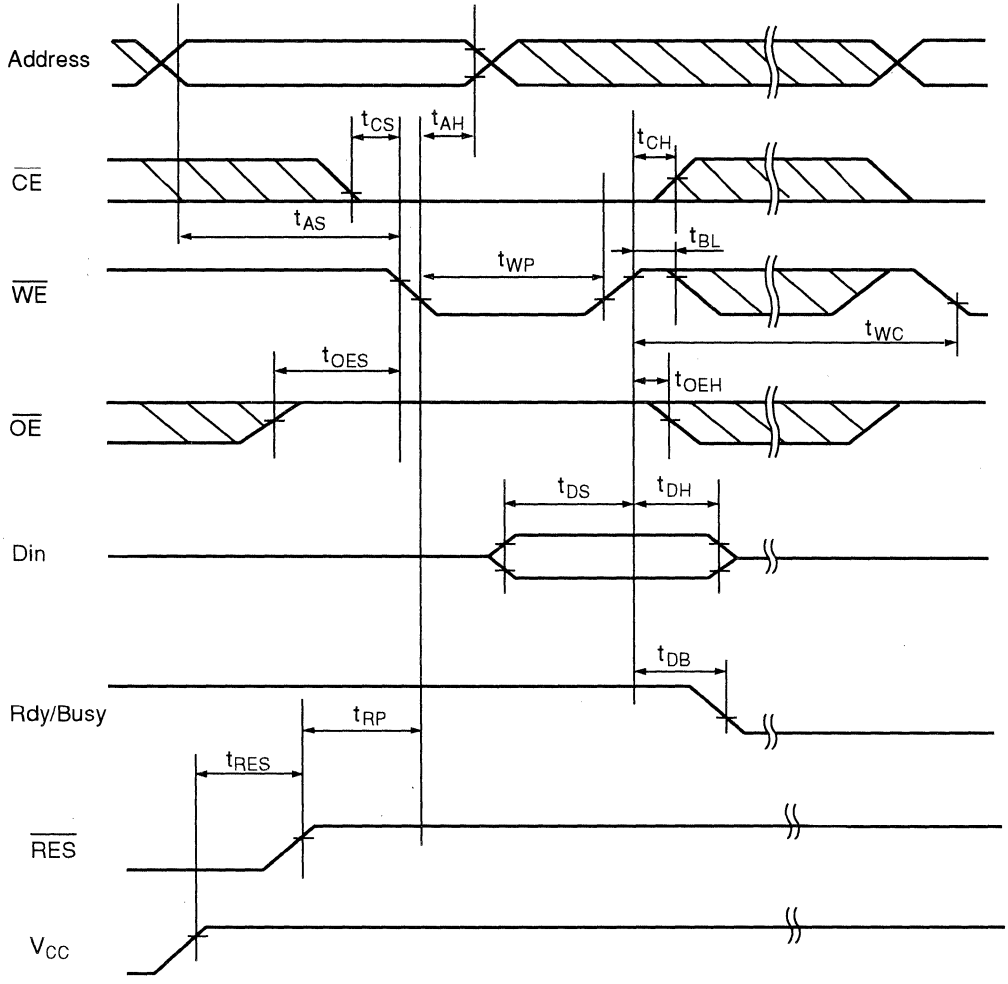
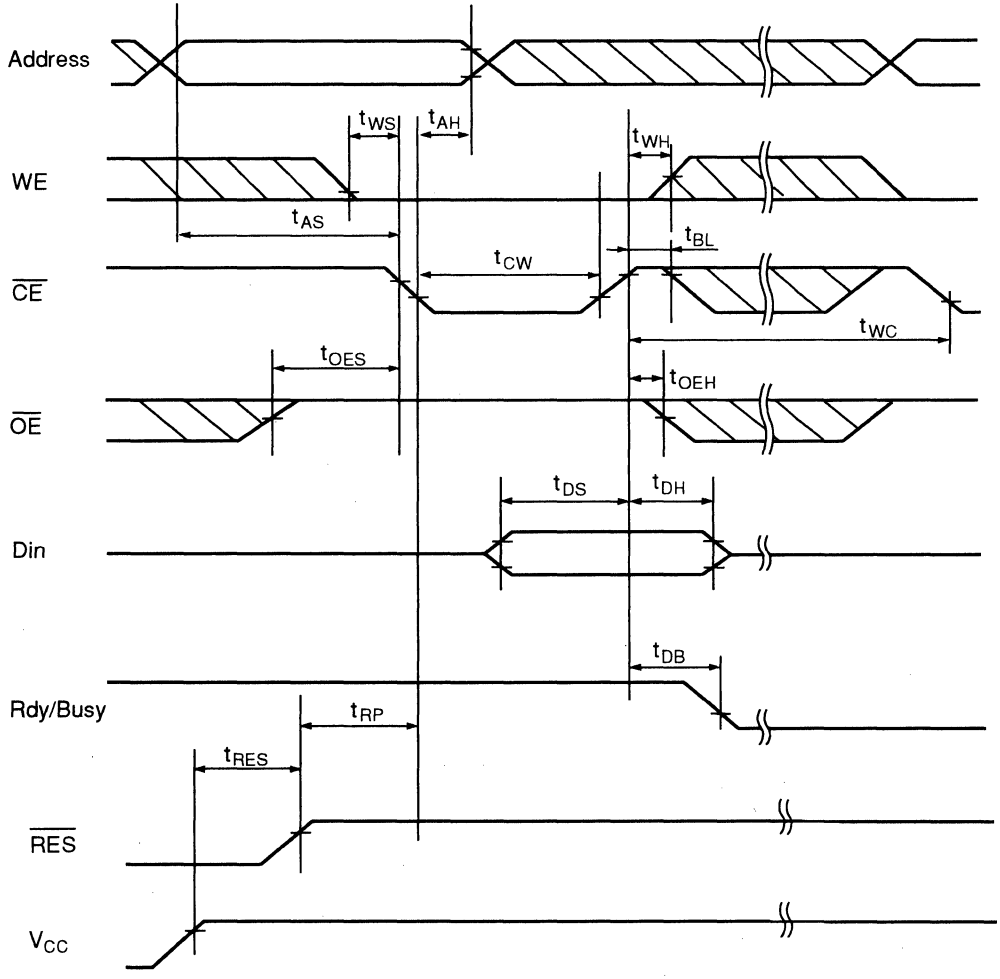
■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.BE1.HN58C257)

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



(TD.BE2.HN58C257)

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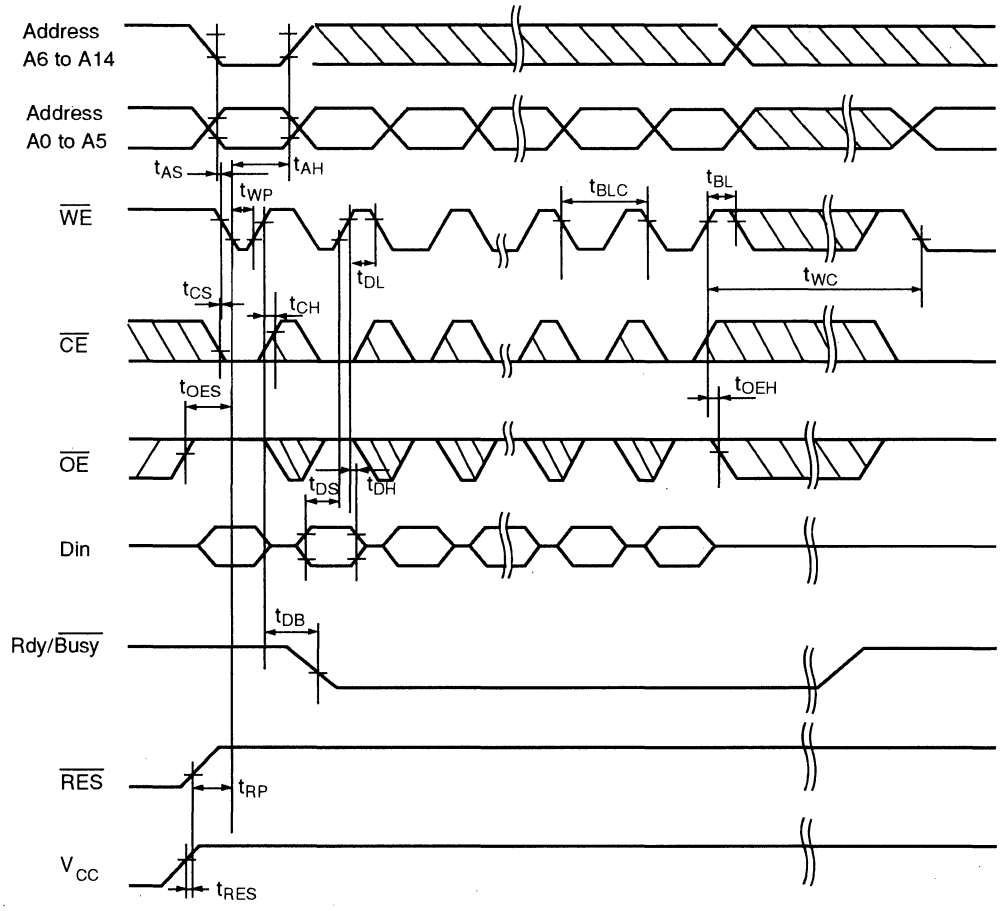
■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	150	-	-	ns	
	t_{CW}[3]	150	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	200	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	0.35	-	30	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Notes: 1. Use this device in longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.PE1.HN58C257)

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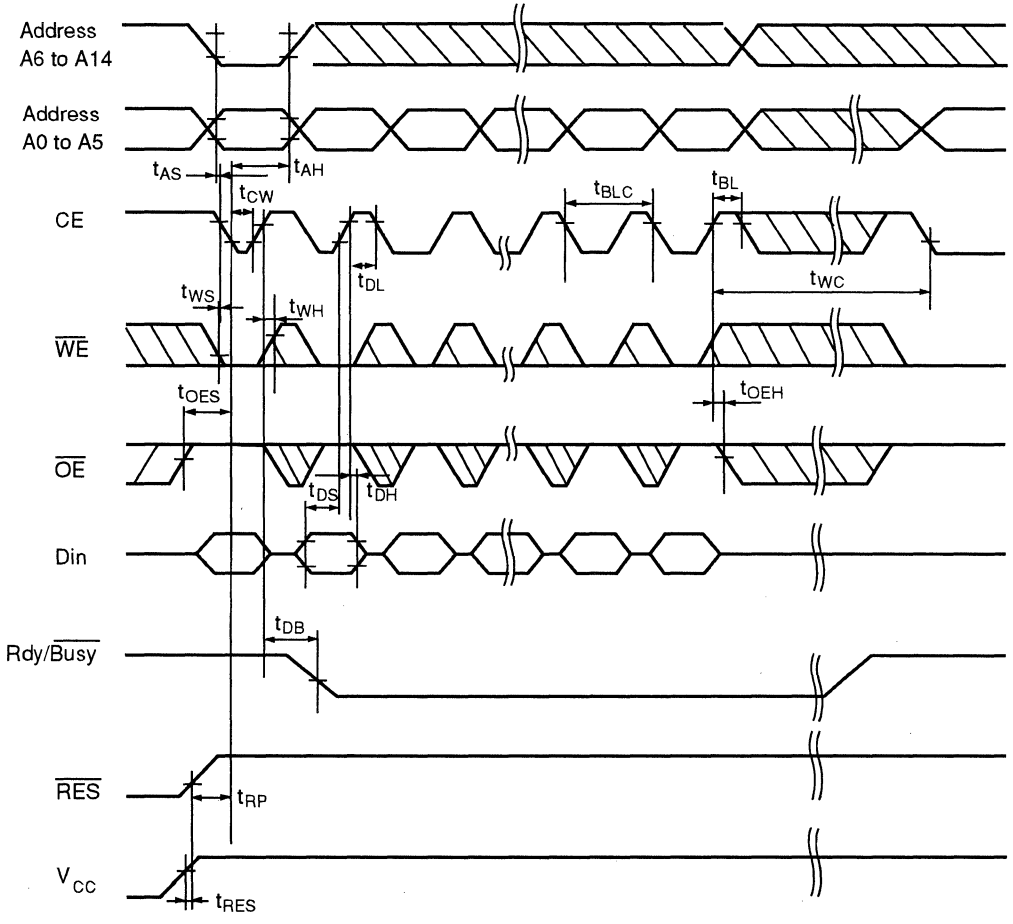
■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)

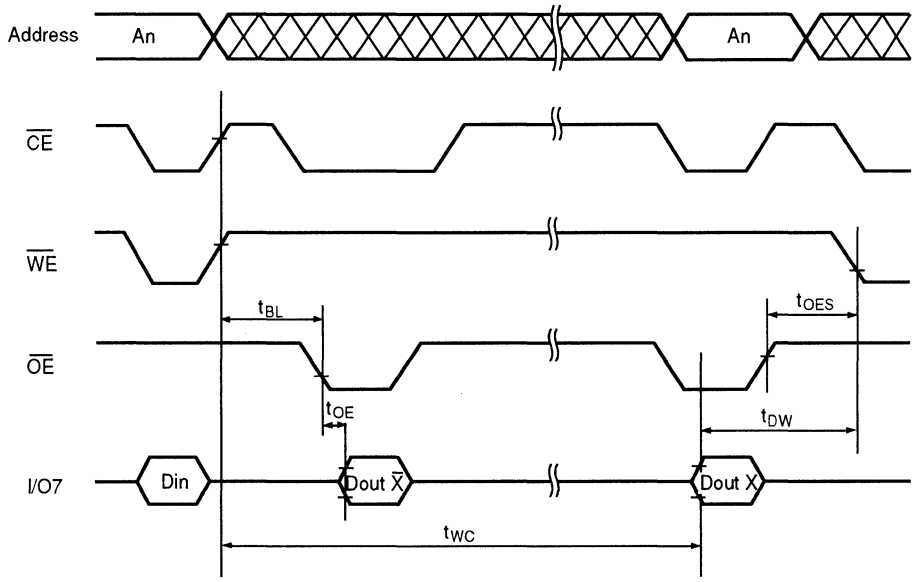


(TD.PE2.HN58C257)

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{DATA}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Byte Load Window	t_{BL}	100	-	-	µs	
Output Enable to Output Delay	t_{OE}	10	-	90	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	10	ms	

■ $\overline{DATA}$ POLLING TIMING WAVEFORM



(TD.DP.EE)

5

■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 64 Bytes of data to be written into the EEPROM in a single write cycle. Following the initial Byte cycle, an additional 1 to 63 Bytes can be written in the same manner. Each additional Byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. Data can be written and accessed 10^5 times in 64 Byte units.

$\overline{Data}$ Polling

$\overline{Data}$ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

Ready/$\overline{Busy}$ Signal

The Ready/$\overline{Busy}$ signal also allows the status of the EEPROM to be determined. The Ready/$\overline{Busy}$ signal is high impedence except in the write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the Ready/$\overline{Busy}$ signal changes to high impedence.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

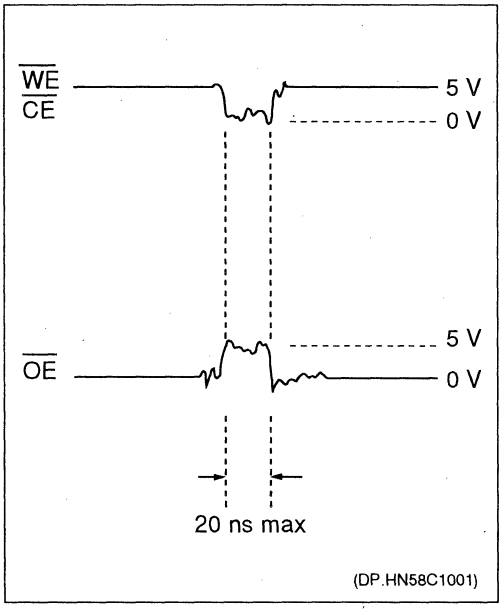
Write/Erase Endurance and Data Retention

The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58C257 has:

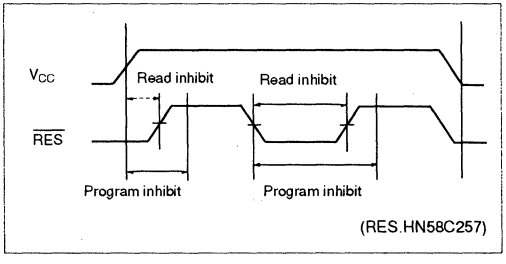
1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58C257 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.



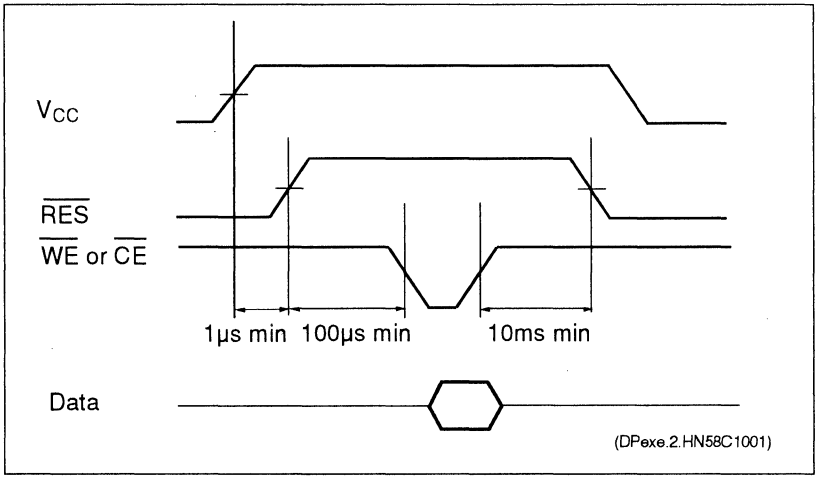
(DP.HN58C1001)

$\overline{RES}$ Signal

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it doesn't provide a latch function.



(RES.HN58C257)



■ FUNCTIONAL DESCRIPTION (continued)

Data Protection (continued)

2. Data protection at V_{cc} on/off

   When V_{cc} is turned on or off, noise on the control pins generated by external circuits (CPU, etc.) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state by using a CPU reset signal to $\overline{RES}$ pin. $\overline{RES}$ pin should be kept at V_{ss} level when V_{cc} is turned on or off.

   The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.

5

256K (32K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58V257 is a 256-Kilobit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 32,768 x 8-bits. The HN58V257 is capable of in-system electrical Byte and Page reprogrammability.

The HN58V257 achieves low supply voltage, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58V257 has a 64-Byte Page Programming function to make its erase and write operations faster. The HN58V257 features $\overline{\text{Data}}$ Polling and a Ready/$\overline{\text{Busy}}$ signal to indicate completion of erase and programming operations.

The HN58V257 provides several levels of data protection. Hardware data protection is provided with the $\overline{\text{RES}}$ pin, in addition to noise protection on the $\overline{\text{WE}}$ signal and write inhibit on power on and off.

The HN58V257 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

The HN58V257 is offered in a 32-lead Plastic TSOP package in both standard and reverse bend pinouts.

■ FEATURES

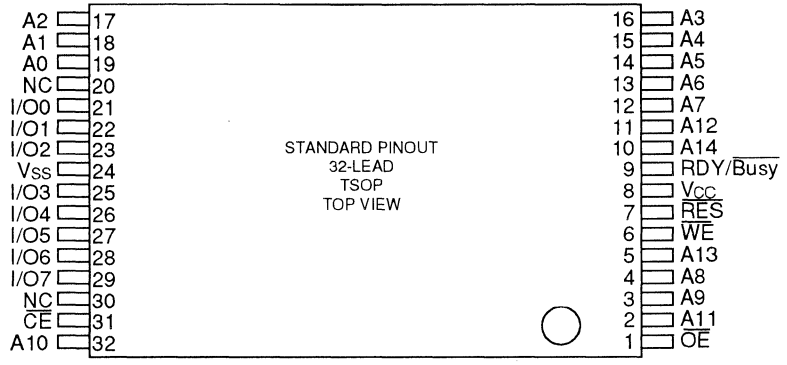
- Single Power Supply:
  V_{cc} = 3V ± 10%
- Access Time:
  350 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 100 µW (typ)
- Automatic Programming:
  Automatic Page Write: 15 ms (max)
  64 Byte Page Size
  Automatic Byte Write: 15 ms (max)
- $\overline{\text{Data}}$ Polling and Ready/$\overline{\text{Busy}}$ Signals
- Hardware Data Protection with $\overline{\text{RES}}$ pin
- Data Protection Circuitry on Power On/Off
- Data Retention: 10 years
- Erase/Write Endurance:
  100,000 cycles in Page Mode
- Packages:
  32-lead Plastic TSOP (Type I)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58V257T-30	300 ns	32-lead Plastic TSOP
HN58V257T-35	350 ns	(TFP-32DA)
HN58V257R-30	300 ns	32-lead Plastic TSOP
HN58V257R-35	350 ns	(TFP-32DAR)
		Reverse bend

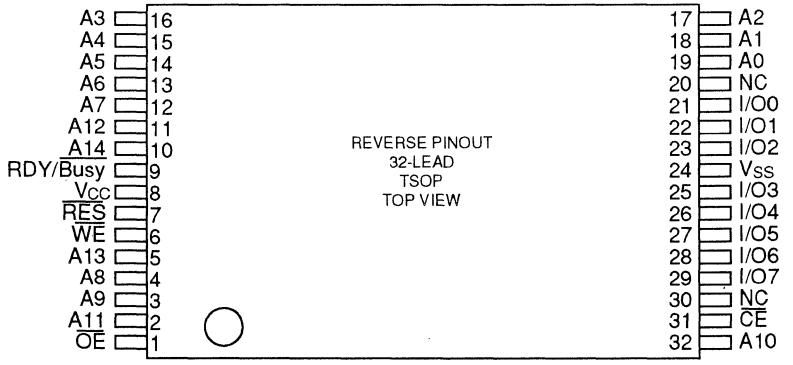
■ PIN ARRANGEMENT

HN58V257T Series



(PinT132.HN58C257T)

HN58V257R Series



(PinT132.HN58C257R)

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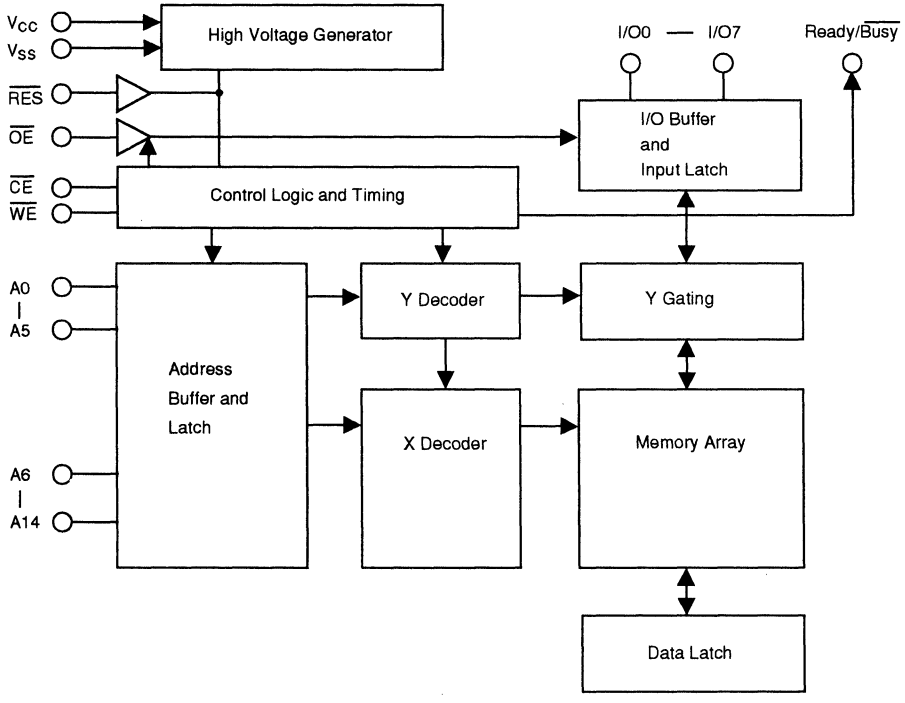
■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{14}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
Rdy/$\overline{Busy}$	Ready/Busy
$\overline{RES}$	Reset

■ BLOCK DIAGRAM



(BD.HN58C257)

■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	D_{OUT}
Standby	V_{IH}	X	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z→V_{OL}	D_{IN}
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	High-Z	-
	X	V_{IL}	X	X	High-Z	-
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O_7)
Program	X	X	X	V_{IL}	High-Z	High-Z

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.
3. Including electrical characterisitics and data retention.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

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■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 to 5.5V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI} [1]	-	-	2	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	6	mA	I_{OUT} = 0 mA, V_{CC} = 3.3 V,Duty = 100%, Cycle = 1 µs
		-	-	15	mA	I_{OUT} = 0 mA, V_{CC} = 3.3 V,Duty = 100%, Cycle = 350 ns
Input Voltage	V_{IL}	-0.3 [2]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} +0.3	V	
	V_H	V_{CC} - 0.5	-	V_{CC} +0.3	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	V_{CC} x 0.8	-	-	V	I_{OH} = -400 µA

Notes: 1. I_{LI} on $\overline{RES}$ = 100 mA max.
2. V_{IL} min = -3.0 V for pulse width ≤ 50 ns.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 2.7 to 5.5V)

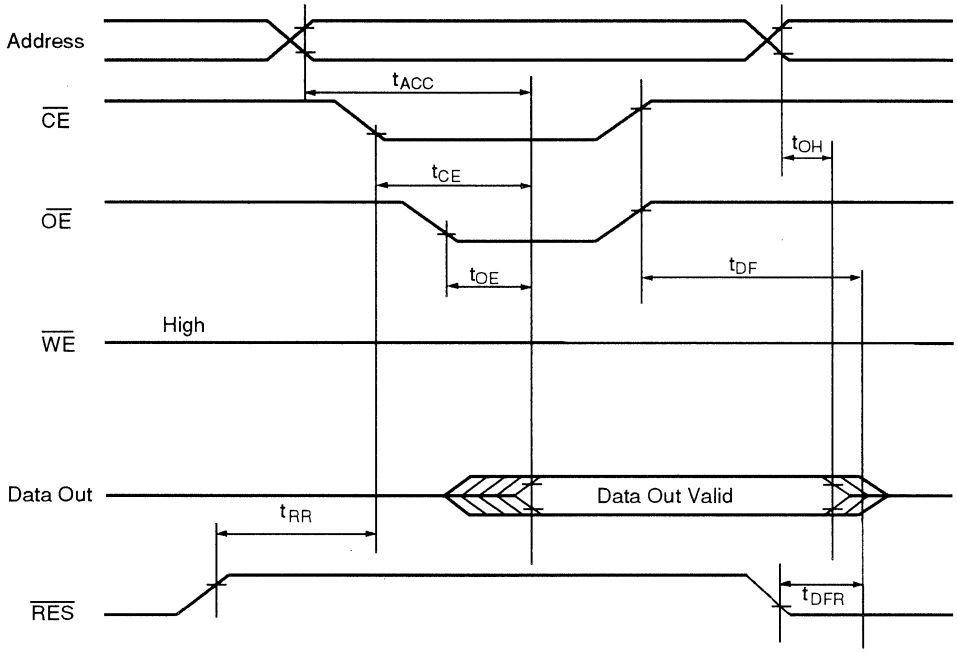
Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN58V257-35 Min.	HN58V257-35 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	350	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	150	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z[1]	t_{DF}	0	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to Output Delay	t_{RR}	0	600	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



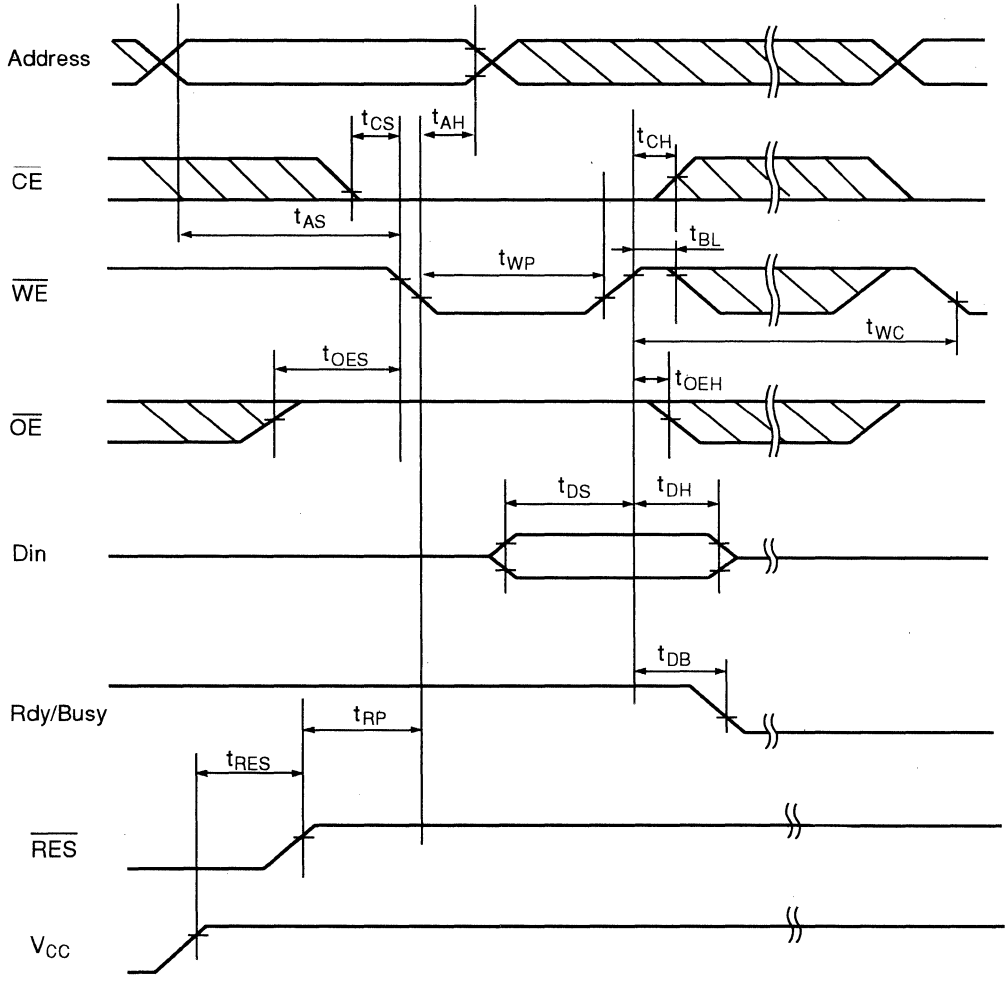
(TD.R.HN58C1001)

■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}	0	-	-	ns	
Write Pulse Width	t_{CW}	250	-	-	ns	
	t_{WP}	250	-	-	ns	
Address Hold Time	t_{AH}	200	-	-	ns	
Data Setup Time	t_{DS}	150	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Write Enable Hold Time	t_{WH}	0	-	-	ns	
Chip Enable Hold Time	t_{CH}	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	15	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

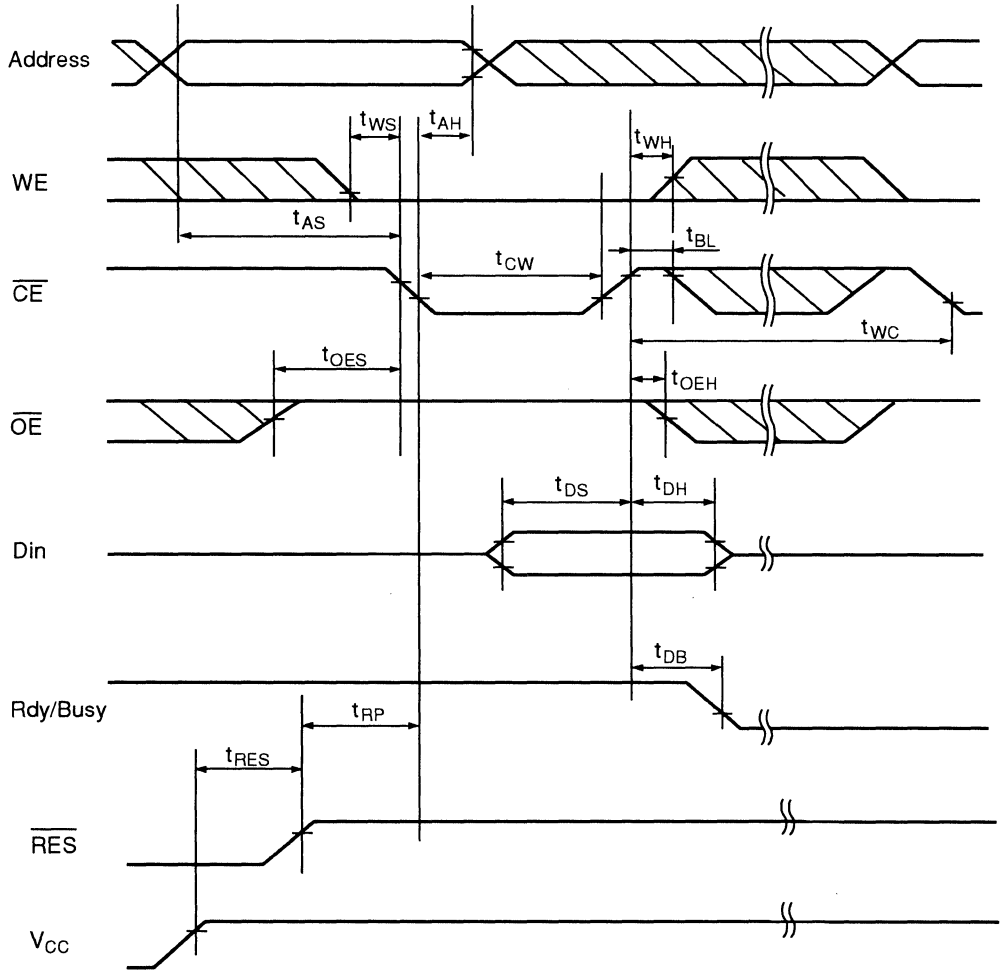
Note: 1. Use this device in a longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.BE1.HN58C257)

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



(TD.BE2.HN58C257)

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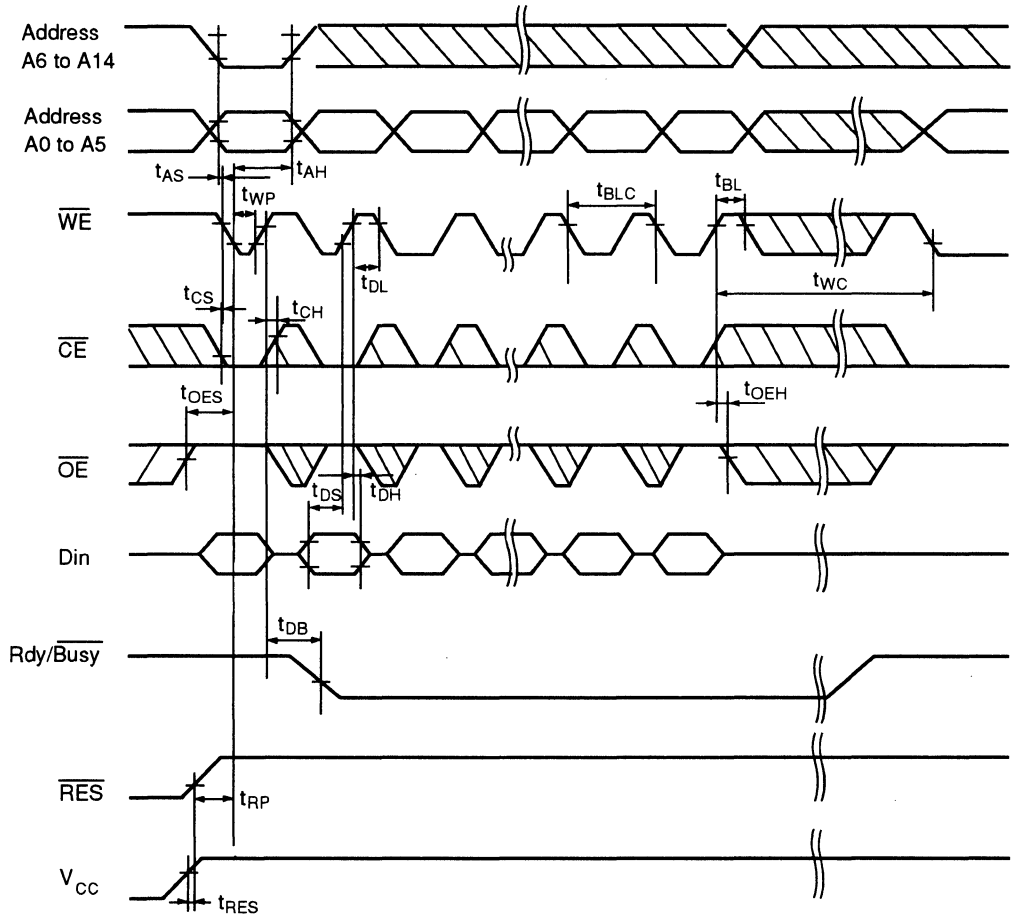
■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	250	-	-	ns	
	t_{CW}[3]	250	-	-	ns	
Address Hold Time	t_{AH}	200	-	-	ns	
Data Setup Time	t_{DS}	150	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	300	-	-	ns	
Write Cycle Time	t_{WC}	15	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	0.55	-	30	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Notes: 1. Use this device in longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.PE1.HN58C257)

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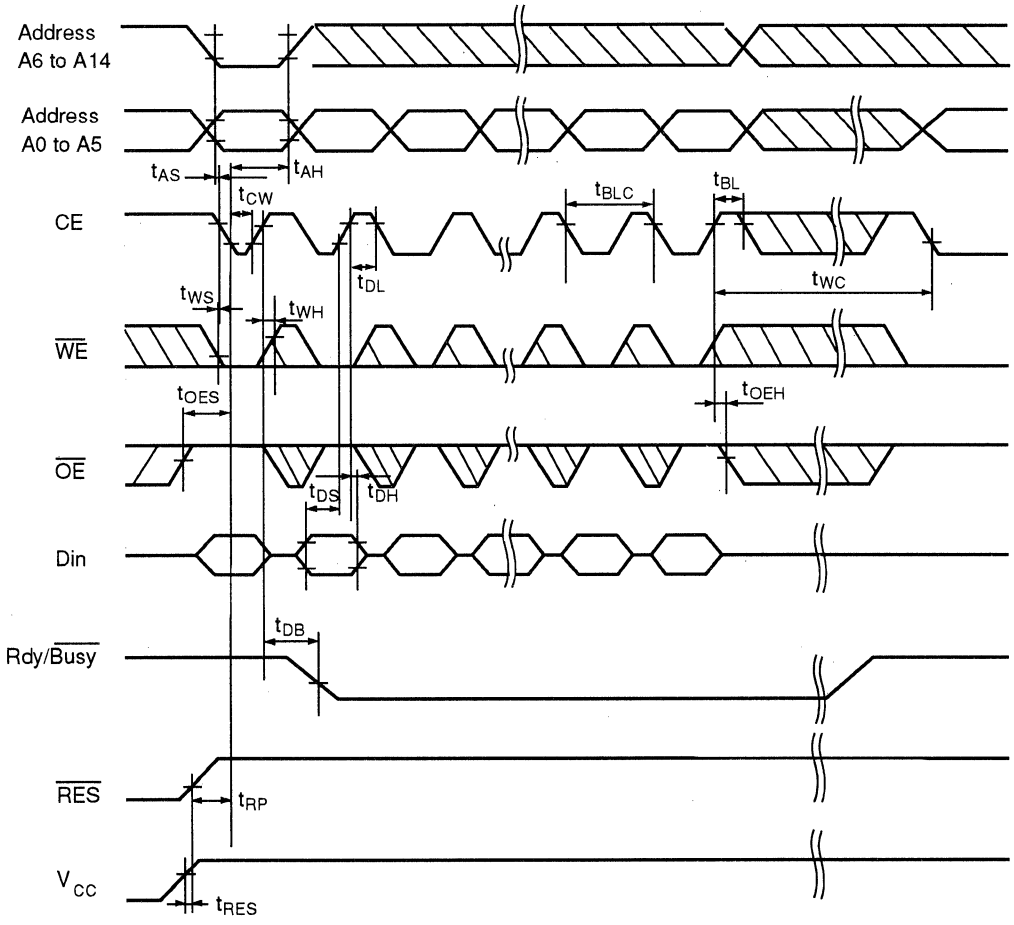
■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)

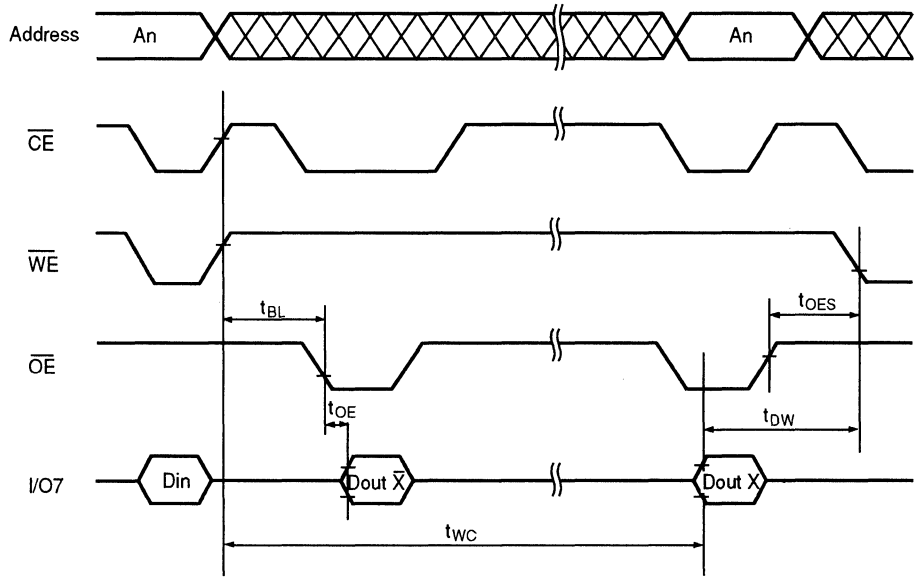


(TD.PE2.HN58C257)

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{DATA}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Byte Load Window	t_{BL}	100	-	-	µs	
Output Enable to Output Delay	t_{OE}	10	-	150	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	15	ms	

■ $\overline{DATA}$ POLLING TIMING WAVEFORM



(TD.DP.EE)

5

■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 64 Bytes of data to be written into the EEPROM in a single write cycle. Following the initial Byte cycle, an additional 1 to 63 Bytes can be written in the same manner. Each additional Byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. Data can be written and accessed 10^5 times in 64 Byte units.

$\overline{Data}$ Polling

$\overline{Data}$ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

Ready/$\overline{Busy}$ Signal

The Ready/$\overline{Busy}$ signal also allows the status of the EEPROM to be determined. The Ready/$\overline{Busy}$ signal is high impedence except in the write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the Ready/$\overline{Busy}$ signal changes to high impedence.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

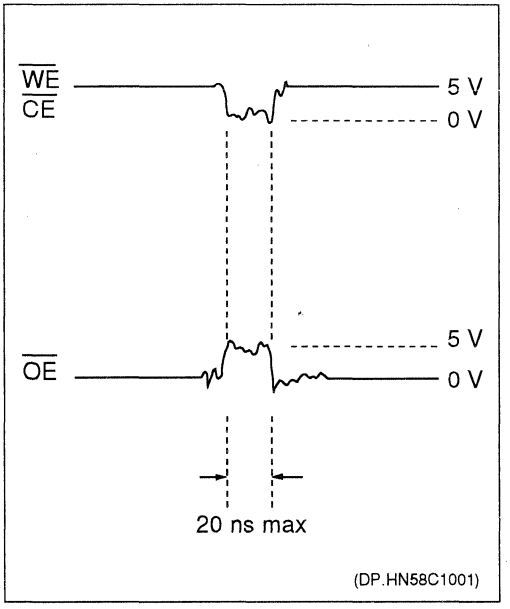
Write/Erase Endurance and Data Retention

The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58V257 has:

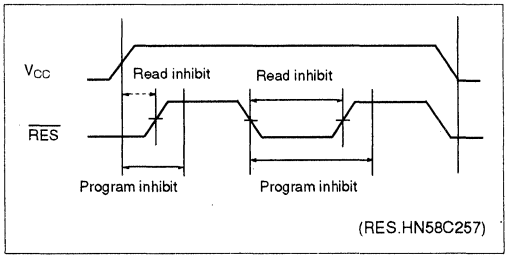
1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58V257 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.



(DP.HN58C1001)

$\overline{RES}$ Signal

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it doesn't provide a latch function.



(RES.HN58C257)

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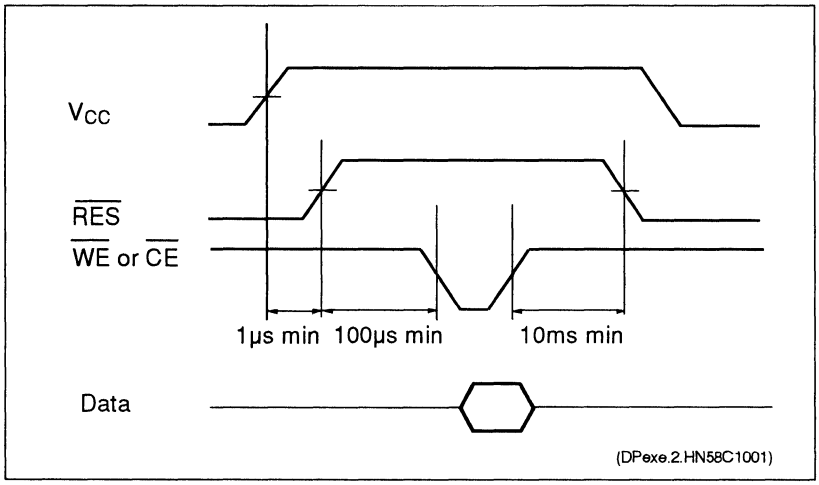


■ **FUNCTIONAL DESCRIPTION (continued)**

Data Protection (continued)

2. Data protection at V_{CC} on/off
   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc.) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state by using a CPU reset signal to $\overline{RES}$ pin. $\overline{RES}$ pin should be kept at V_{SS} level when V_{CC} is turned on or off.
   The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.

5

1M (128K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58C1001 is a 1-Megabit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 131,072 x 8-bits. The HN58C1001 is capable of in-system electrical Byte and Page reprogrammability.

The HN58C1001 achieves high speed access, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58C1001 has a 128-Byte Page Programming function to make its erase and write operations faster. The HN58C1001 features $\overline{\text{Data}}$ Polling and a Ready/$\overline{\text{Busy}}$ signal to indicate completion of erase and programming operations.

The HN58C1001 provides several levels of data protection. Hardware data protection is provided with the $\overline{\text{RES}}$ pin, in addition to noise protection on the $\overline{\text{WE}}$ signal and write inhibit on power on and off. Software data protection is implemented using the JEDEC Optional Standard algorithm.

The HN58C1001 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 10,000 cycles in the Page Mode.

The HN58C1001 is offered in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages. The HN58C1001 TSOP is offered in both standard and reverse bend pinouts.

■ FEATURES

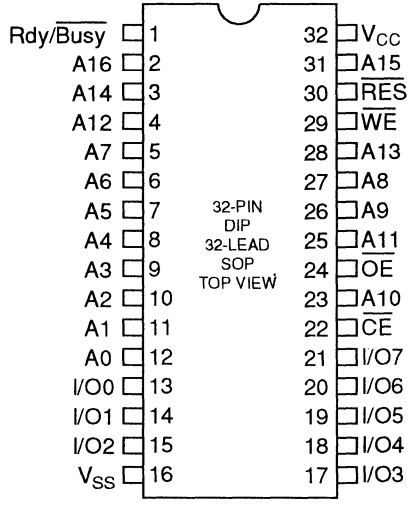
- Single Power Supply:
  V_{cc} = 5V ± 10%
- High Speed Access Times:
  150 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 110 µW (max)
- Automatic Programming:
  Automatic Page Write: 10 ms (max)
  128 Byte Page Size
  Automatic Byte Write: 10 ms (max)
- $\overline{\text{Data}}$ Polling and Ready/$\overline{\text{Busy}}$ Signals
- Hardware Data Protection with $\overline{\text{RES}}$ pin
- Data Protection Circuitry on Power On/Off
- Software Data Protection Algorithm
- Data Retention: 10 years
- Erase/Write Endurance:
  10,000 cycles in Page Mode
- Packages:
  32-pin Plastic DIP
  32-pin Plastic SOP
  32-lead Plastic TSOP (Type I)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58C1001P-15	150 ns	32-pin Plastic DIP (DP-32)
HN58C1001FP-15	150 ns	32-lead Plastic SOP (FP-32D)
HN58C1001T-15	150 ns	32-lead Plastic TSOP (TFP-32DA)
HN58C1001R-15	150 ns	32-lead Plastic TSOP (TFP-32DAR) Reverse bend

■ PIN ARRANGEMENT

HN58C1001P Series
HN58C1001FP Series



(PinD32.HN58C1001)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
Rdy/$\overline{Busy}$	Ready/Busy
$\overline{RES}$	Reset

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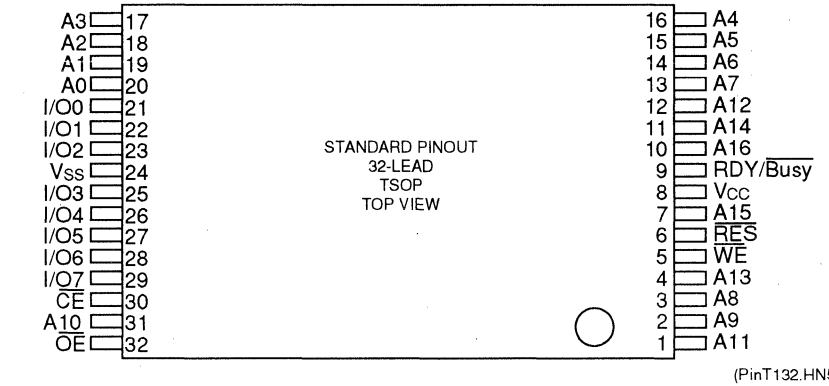
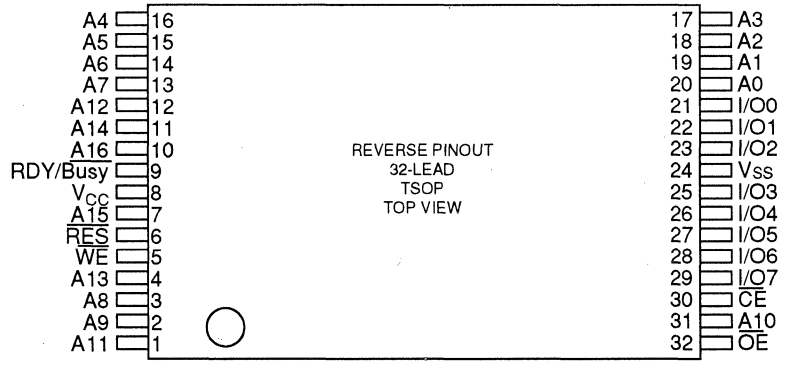
■ PIN ARRANGEMENT (cont.)

HN58C1001T Series



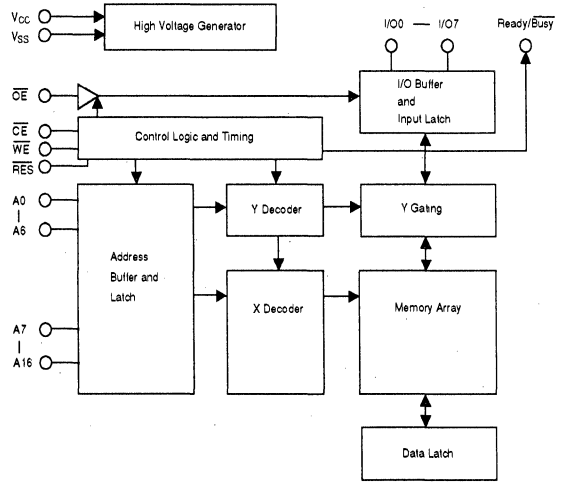
(PinT132.HN58C1001T)

HN58C1001R Series



(PinT132.HN58C1001R)

■ BLOCK DIAGRAM



(BD.HN58C1001)

■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	D_{OUT}
Standby	V_{IH}	X	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z→V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	-	-
	X	V_{IL}	X	X	-	
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O_7)
Program	X	X	X	V_{IL}	High-Z	High-Z

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

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■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	15	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 1 µs
		-	-	50	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 150 ns
Input Voltage	V_{IL}	-0.3 [1]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 0.3	V	
	V_H	V_{CC}-0.5	-	V_{CC} + 1	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
2. I_{LI} on $\overline{RES}$ = 100 µA Max.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

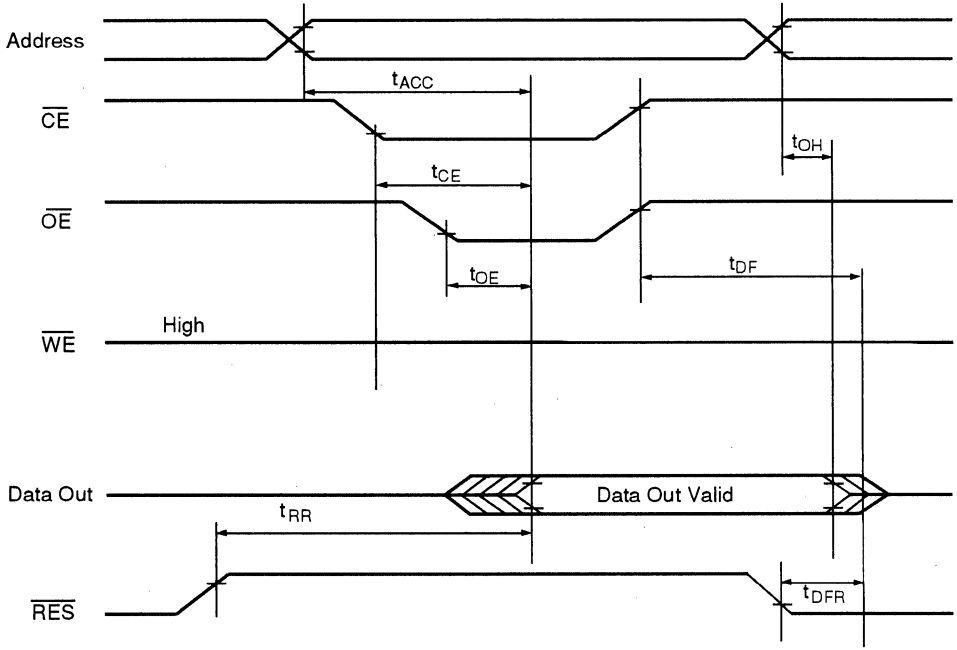
Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 1.8 V

Item	Symbol	HN58C1001-15 Min.	HN58C1001-15 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	150	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	75	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z[1]	t_{DF}	0	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to Output Delay	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN58C1001)

■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{CW}[3]	250	-	-	ns	
	t_{WP}[2]	250	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Note: 1. Use this device in a longer cycle than this value.
2. WE controlled operation.
3. CE controlled operation.

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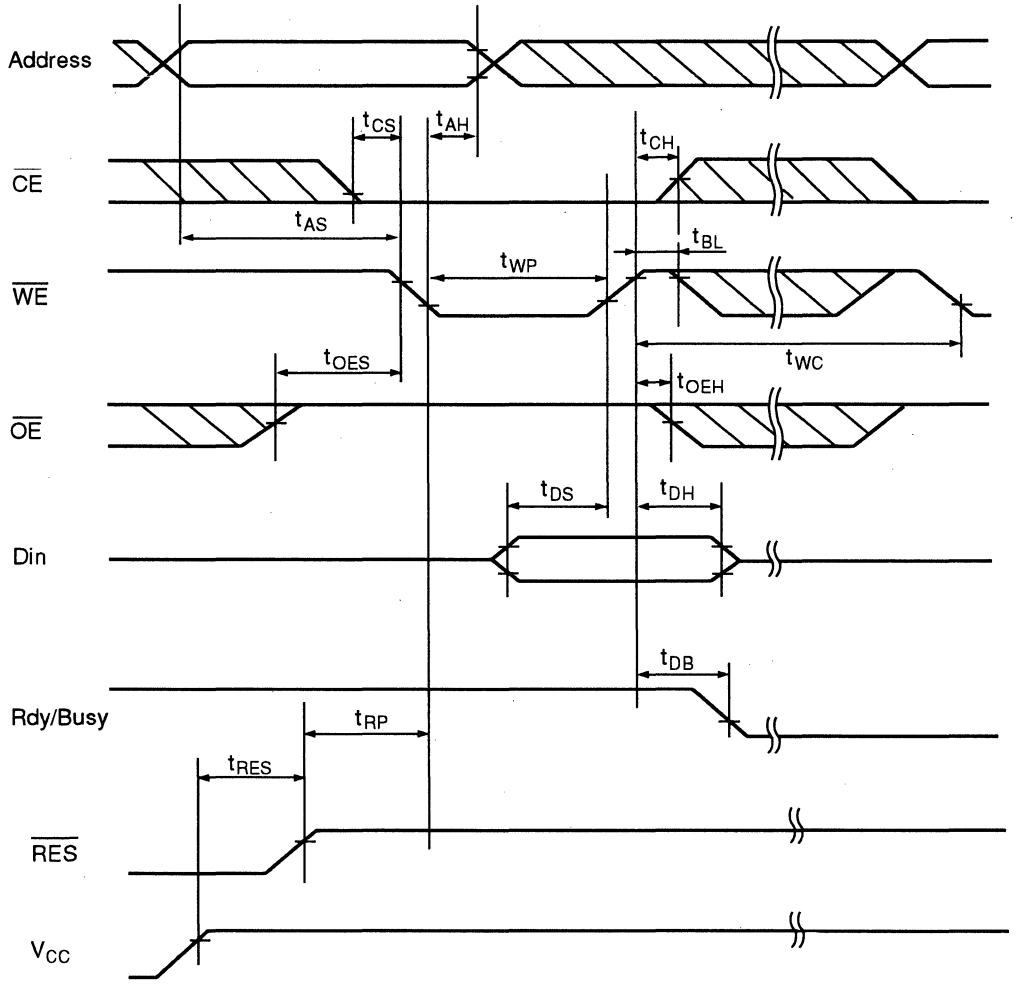
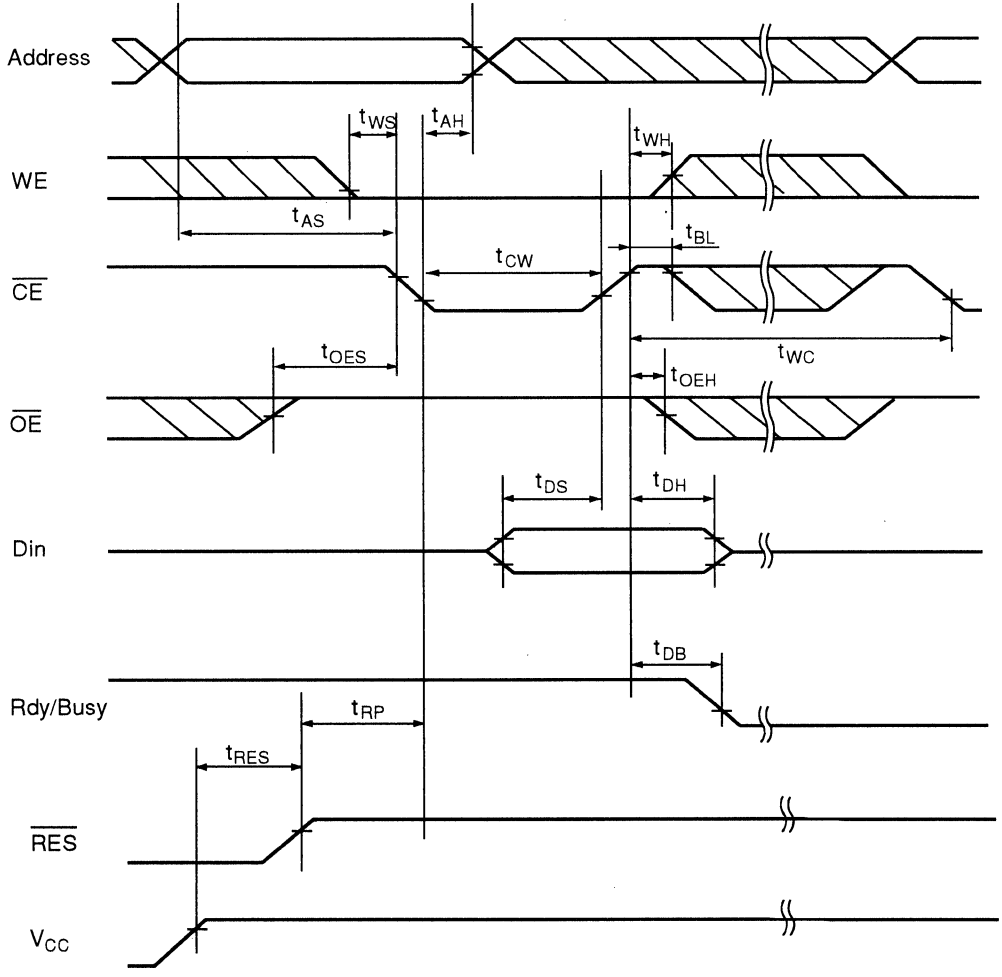
■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.BE1.HN58C1001)

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



(TD.BE2.HN58C1001)

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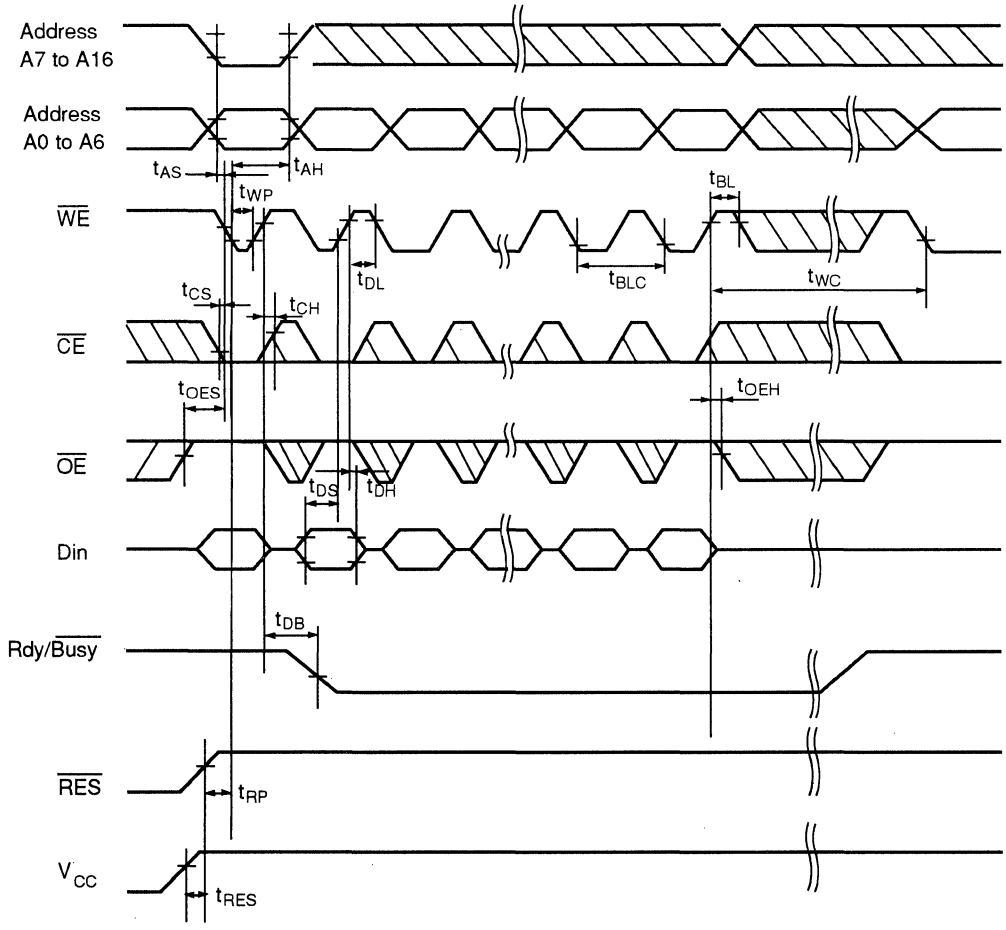
■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	250	-	-	ns	
	t_{CW}[3]	250	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	300	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	0.55	-	30	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Notes: 1. Use this device in longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.PE1.HN58C1001)

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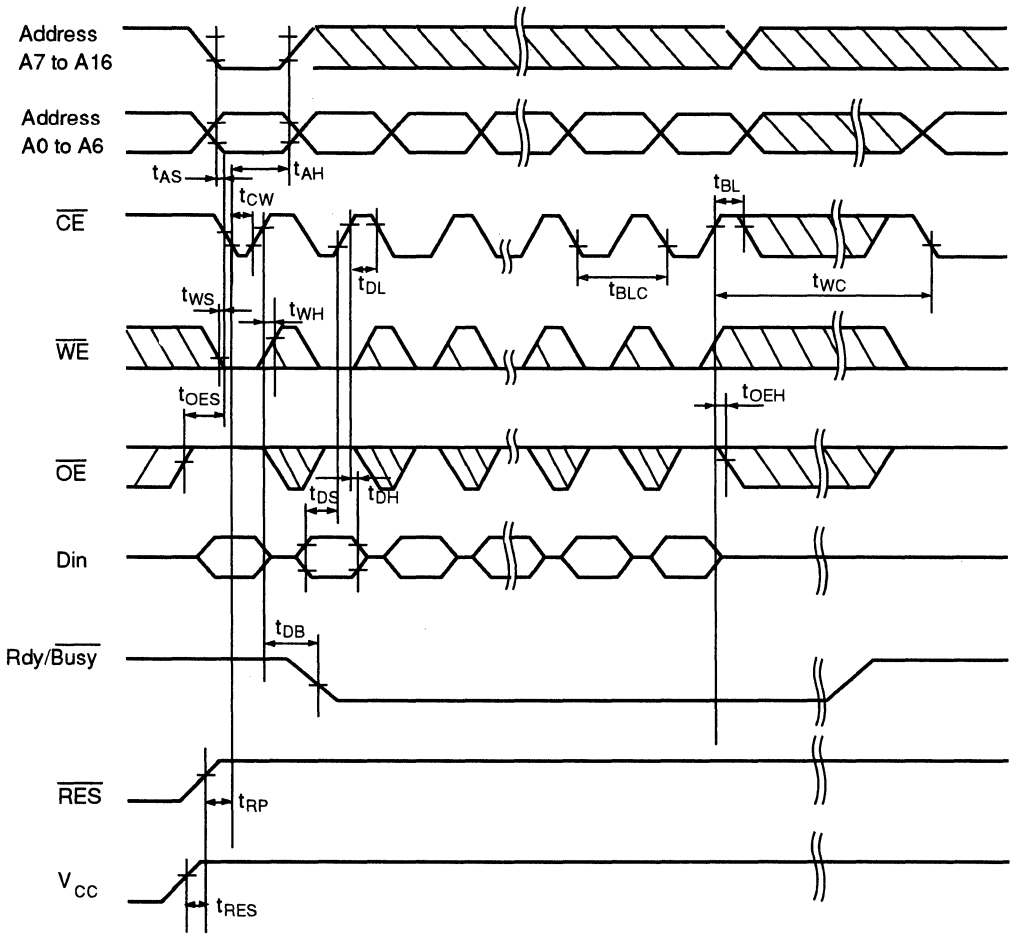
■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)

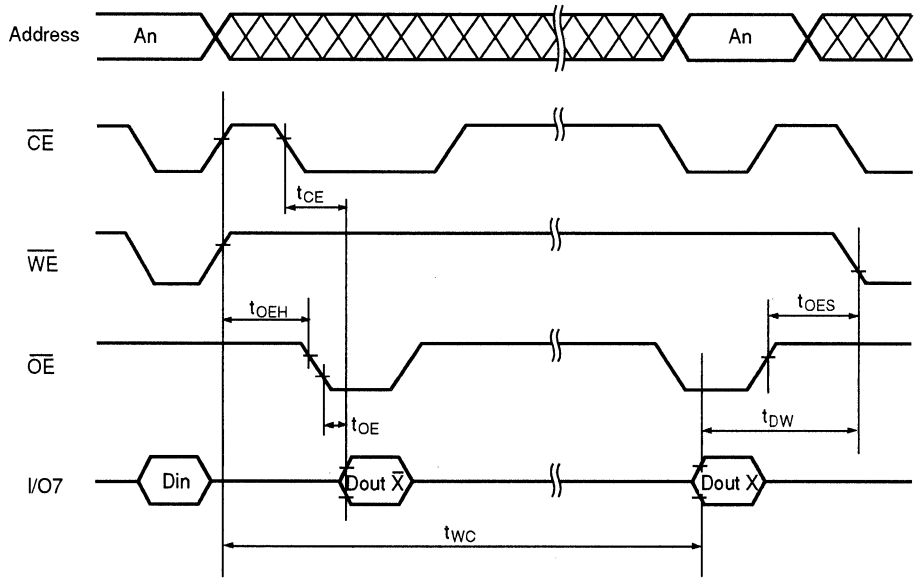


(TD.PE2.HN58C1001)

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{DATA}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	10	ms	

■ $\overline{DATA}$ POLLING TIMING WAVEFORM



(TD.DP.HN58C1001)

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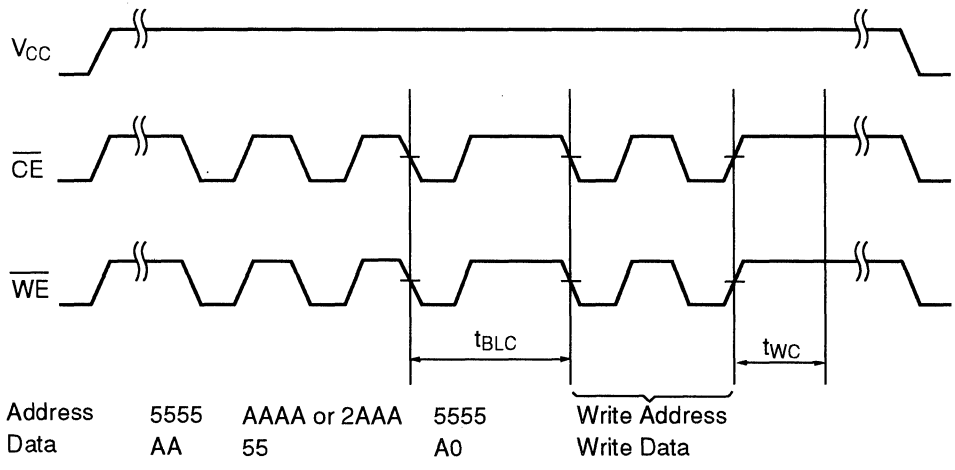
■ AC ELECTRICAL CHARACTERISTICS FOR SOFTWARE DATA PROTECTION CYCLE OPERATION

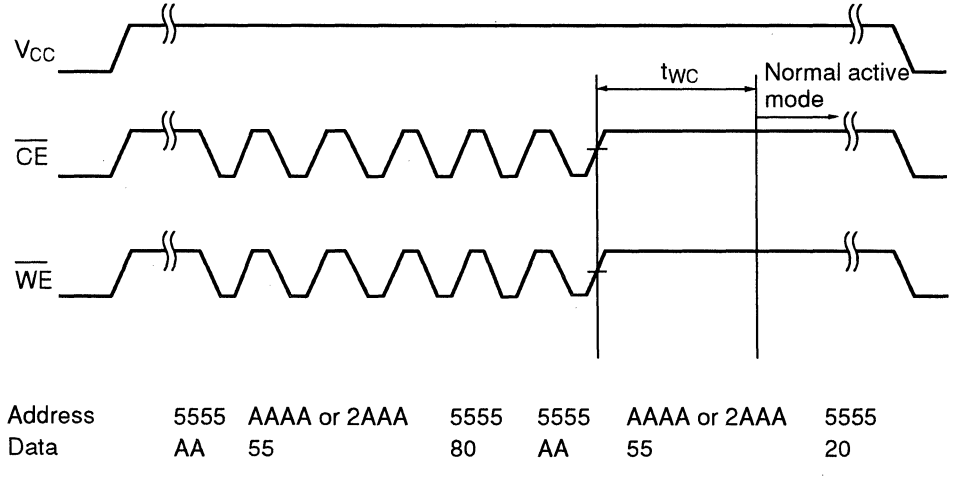
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Byte Load Cycle Time	t_{BLC}	0.55	-	30	µs	
Write Cycle Time	t_{WC}	10	-	-	ms	

■ SOFTWARE DATA PROTECTION TIMING WAVEFORM (Protection Mode)



(TD.SD1.HN58C1001)

■ SOFTWARE DATA PROTECTION TIMING WAVEFORM (Non-Protection Mode)



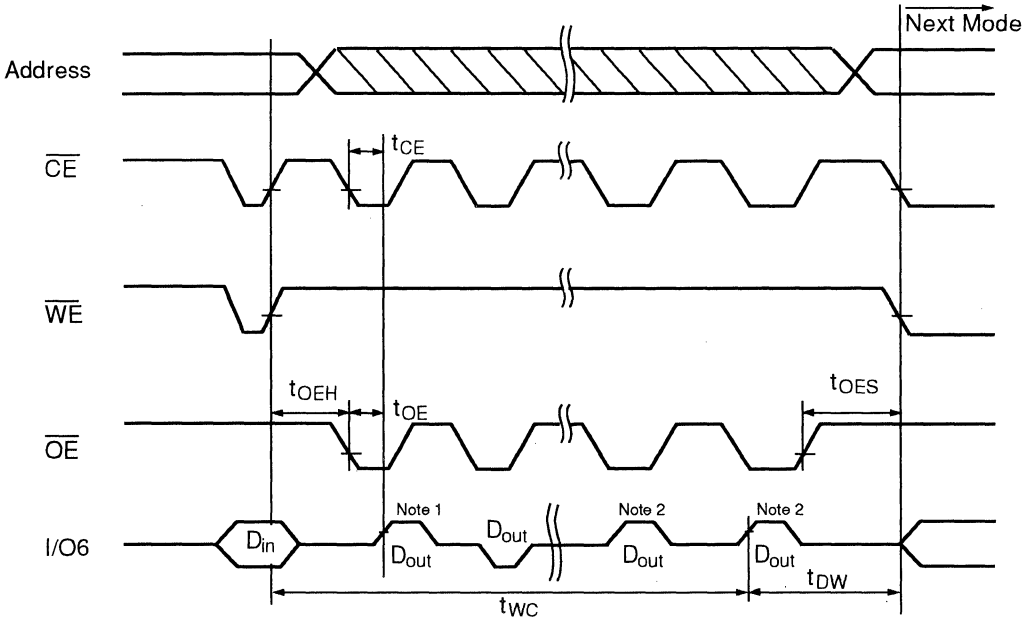
(TD.SD2.HN58C1001)

■ TOGGLE BIT

The HN58C1001 provides another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O_6 will change from "1" to "0" (toggle) for each read. When the internal programming cycle is over, toggling of I/O_6 will stop and the device can be accessible for the next read or program.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
$\overline{OE}$ to Write Setup Time	t_{OES}	0	-	-	ns	
$\overline{OE}$ Hold Time	t_{OEH}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	10	ms	

■ TOGGLE BIT TIMING WAVEFORM



(TD.TB.HN58C1001)

Notes: 1. I/O beginning state is "1".
2. I/O ending state will vary.

5

■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 128 Bytes of data to be written into the EEPROM in a single cycle and allows the undefined data within 128 Bytes to be written corresponding to the undefined address (A_0 to A_6). Loading the first Byte of data, the data load window of 30 μs opens for the second. In the same manner each additional Byte of data can be loaded within 30 μs. In case $\overline{CE}$ and $\overline{WE}$ are kept high for 100 μs after data input, the EEPROM enters erase and write automatically and only the input data are written into the EEPROM. In Page mode the data can be written and accessed 10^5 times per page, and in Byte mode 10^4 times per Byte.

$\overline{\text{Data}}$ Polling

$\overline{\text{Data}}$ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

Write Protection

(1) Noise protection: Noise on a write cycle will not act as a trigger with a $\overline{WE}$ pulse of less than 20 ns.

(2) Write inhibit: Holding $\overline{OE}$ low, $\overline{WE}$ high, or $\overline{CE}$ high, inhibits a write cycle during power on/off.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

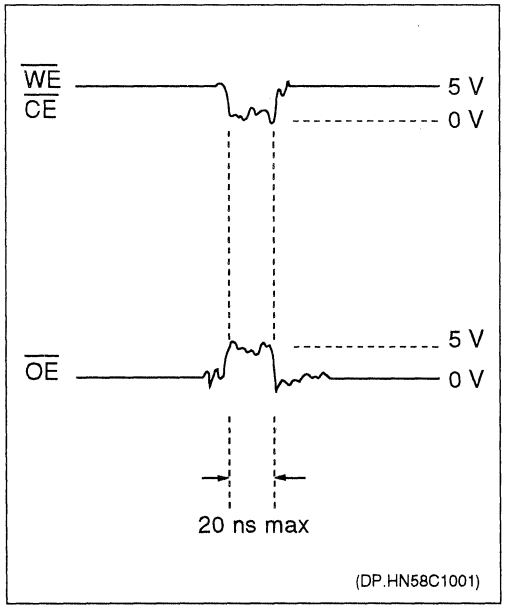
Write/Erase Endurance and Data Retention

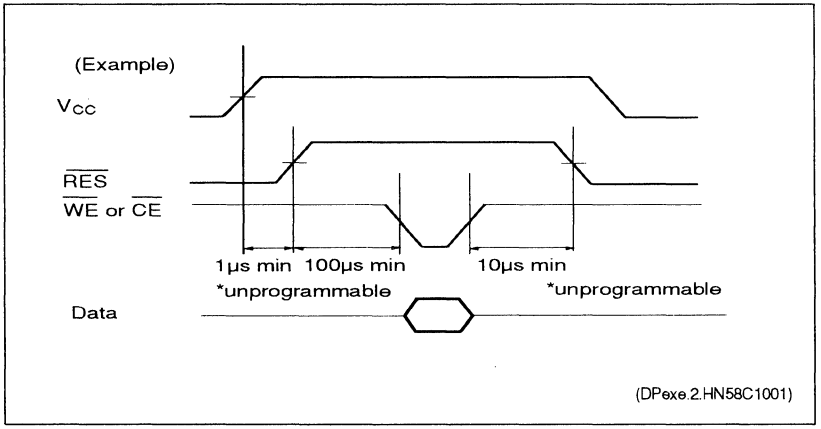
The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58C1001 has:

1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58C1001 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.





■ FUNCTIONAL DESCRIPTION (continued)

Data Protection (continued)

2. Data protection at V_{CC} on/off
   When $\overline{RES}$ is low, the EEPROM cannot be erased and programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during programming because it does not provide a latch function.
   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state by using a CPU reset signal to $\overline{RES}$ pin.
   The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the lost data input.

3. Software data protection
   To prevent unintentional programming caused by noise generated by external circuits, HN58C1001 has a Software data protection function. In Software data protection mode, 3 Bytes of data must be input before the Write data. These Bytes can switch the Non-Protection mode to the Protection mode.

Address	Data
5555	AA
⇓	⇓
AAAA or 2AAA	55
⇓	⇓
5555	A0
⇓	⇓
Write Address	**Write Data** (Normal Data Input)

   The Software data protection mode can be cancelled by inputting the following 6 Bytes. This changes the HN58C1001 turns to the Non-Protection mode and it can write data normally. When the data is input during the cancelling cycle, the data cannot be written.

Address	Data
5555	AA
⇓	⇓
AAAA or 2AAA	55
⇓	⇓
5555	80
⇓	⇓
5555	AA
⇓	⇓
AAAA or 2AAA	55
⇓	⇓
5555	20

5

1M (128K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58V1001 is a 1-Megabit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 131,072 x 8-bits. The HN58V1001 is capable of in-system electrical Byte and Page reprogrammability.

The HN58V1001 achieves low voltage, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58V1001 has a 128-Byte Page Programming function to make its erase and write operations faster. The HN58V1001 features Data Polling and a Ready/Busy signal to indicate completion of erase and programming operations.

The HN58V1001 provides several levels of data protection. Hardware data protection is provided with the $\overline{RES}$ pin, in addition to noise protection on the $\overline{WE}$ signal and write inhibit on power on and off. Software data protection is implemented using the JEDEC Optional Standard algorithm.

The HN58V1001 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

The HN58V1001 is offered in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages. The HN58V1001 TSOP is offered in both standard and reverse bend pinouts.

■ FEATURES

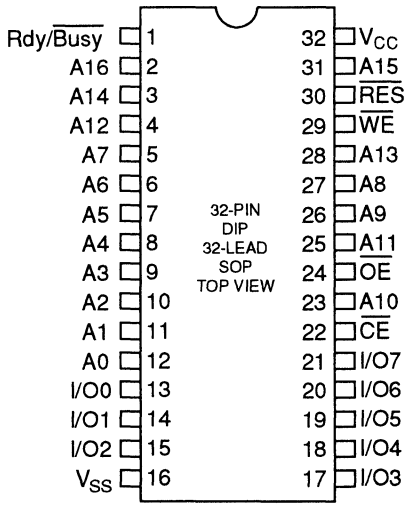
- Single Power Supply:
  V_{CC} = 2.7 to 5.5V
- Address Access Time:
  250 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 110 µW (max)
- Automatic Programming:
  Automatic Page Write: 15 ms (max)
  128 Byte Page Size
  Automatic Byte Write: 15 ms (max)
- Data Polling and Ready/Busy Signals
- Hardware Data Protection with $\overline{RES}$ pin
- Data Protection Circuitry on Power On/Off
- Software Data Protection Algorithm
- Data Retention: 10 years
- Erase/Write Endurance:
  10,000 cycles in Page Mode
- Packages:
  32-pin Plastic DIP
  32-pin Plastic SOP
  32-lead Plastic TSOP (Type I)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58V1001P-25	250 ns	32-pin Plastic DIP (DP-32)
HN58V1001FP-25	250 ns	32-lead Plastic SOP (FP-32D)
HN58V1001T-25	250 ns	32-lead Plastic TSOP (TFP-32DA)
HN58V1001R-25	250 ns	32-lead Plastic TSOP (TFP-32DAR) Reverse bend

■ PIN ARRANGEMENT

HN58V1001P Series
HN58V1001FP Series



(PinD32.HN58C1001)

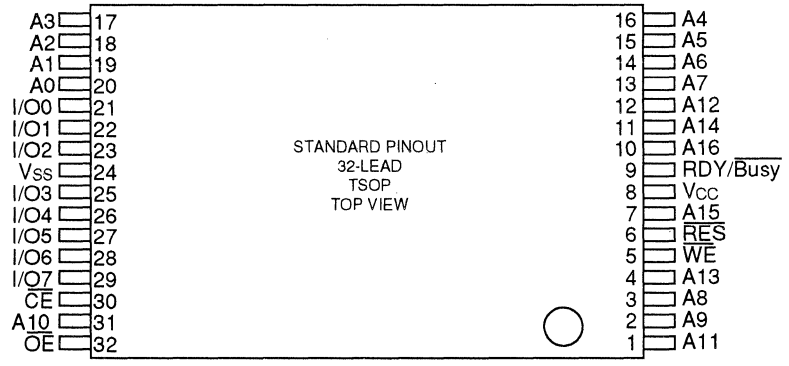
■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
Rdy/$\overline{Busy}$	Ready/Busy
$\overline{RES}$	Reset

5

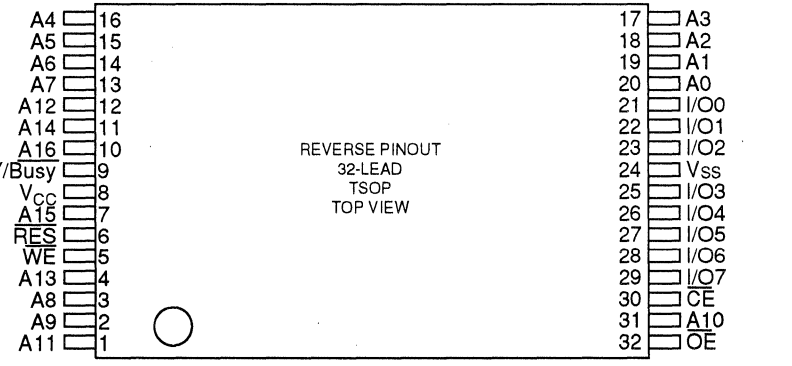
■ PIN ARRANGEMENT (cont.)

HN58V1001T Series



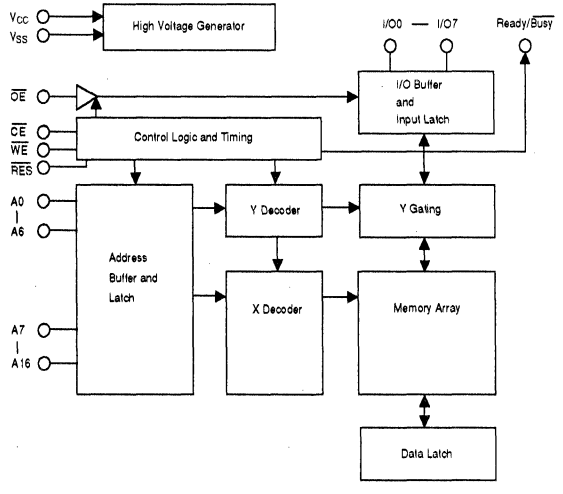
(PinT132.HN58C1001T)

HN58V1001R Series



(PinT132.HN58C1001R)

■ BLOCK DIAGRAM



(BD.HN58C1001)

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■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	D_{OUT}
Standby	V_{IH}	X	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z→V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	-	-
	X	V_{IL}	X	X	-	-
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O_7)
Program	X	X	X	V_{IL}	High-Z	High-Z

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

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■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 to 5.5V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{CC} = 3.6 V, V_{IN} = 3.6 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 3.6 V, V_{OUT} = 3.6 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	6	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 3.3 V
		-	-	15	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 250 ns at V_{CC} = 3.3 V
Input Voltage	V_{IL}	-0.3 [1]	-	0.8	V	
	V_{IH}	2.0 [2]	-	V_{CC} +0.3	V	
	V_H	V_{CC}-0.5	-	V_{CC} + 1	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	V_{CC}x0.8	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
2. V_{IH} min = 2.2 V for V_{CC} = 3.6 to 5.5V.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 2.7 to 5.5V)

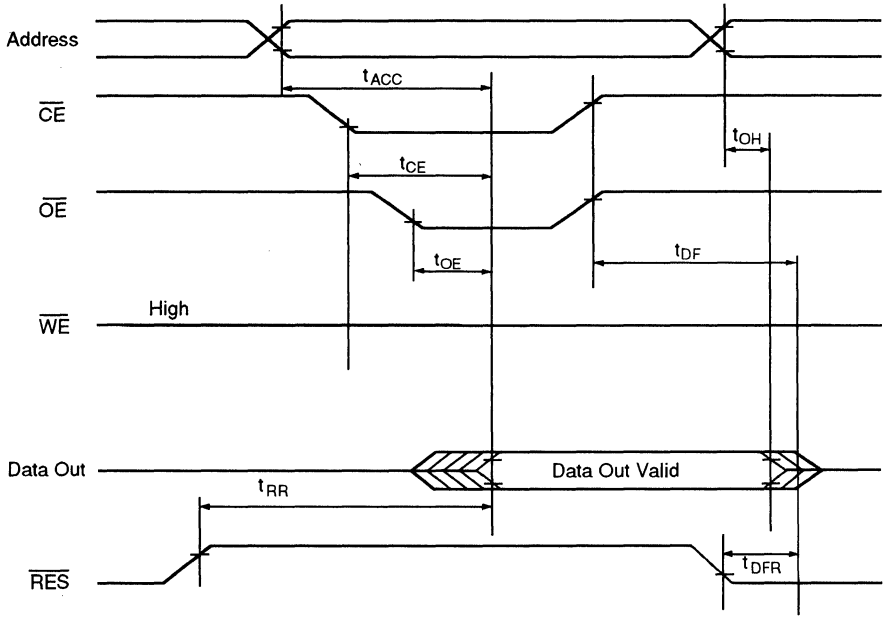
Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 1.8 V

Item	Symbol	HN58V1001-25 Min.	HN58V1001-25 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	250	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	120	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z[1]	t_{DF}	0	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to Output Delay	t_{RR}	0	600	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN58C1001)

■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{CW}[3]	250	-	-	ns	
	t_{WP}[2]	250	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Note: 1. Use this device in a longer cycle than this value.
2. WE controlled operation.
3. CE controlled operation.

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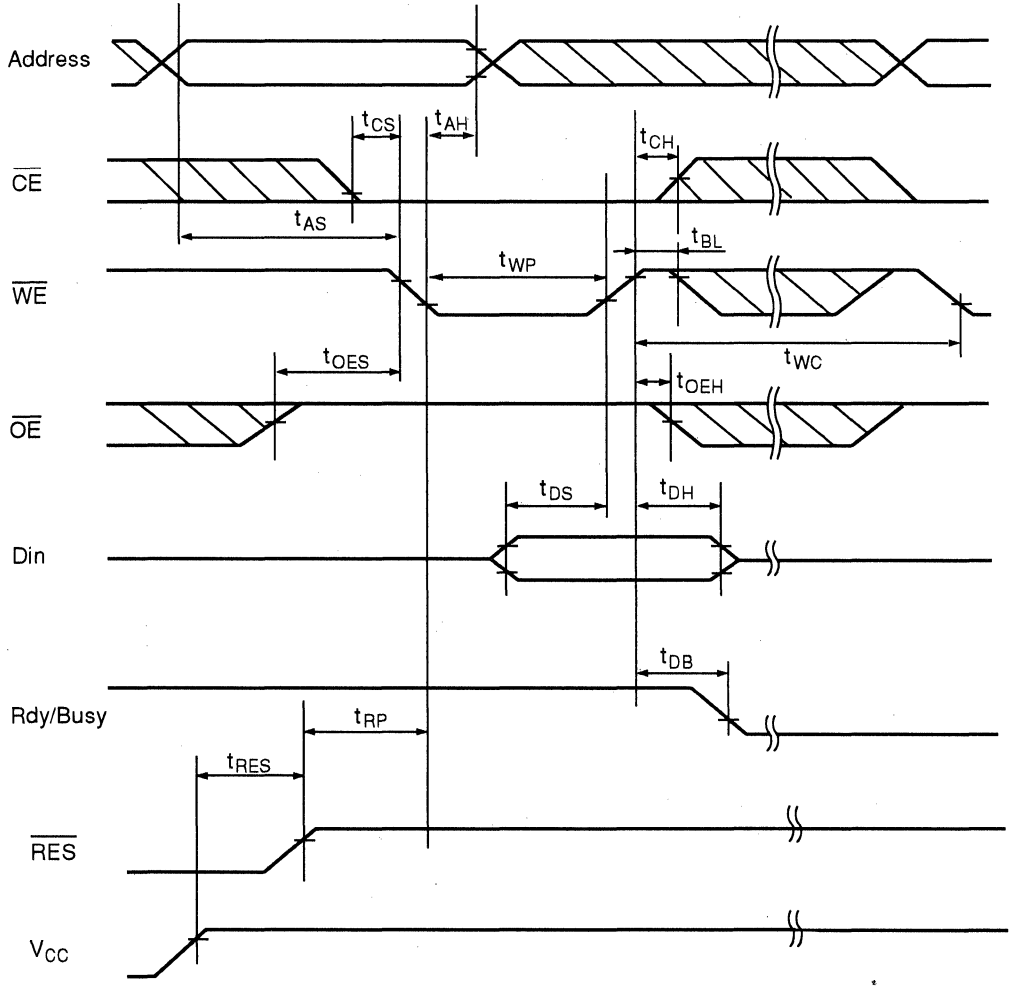
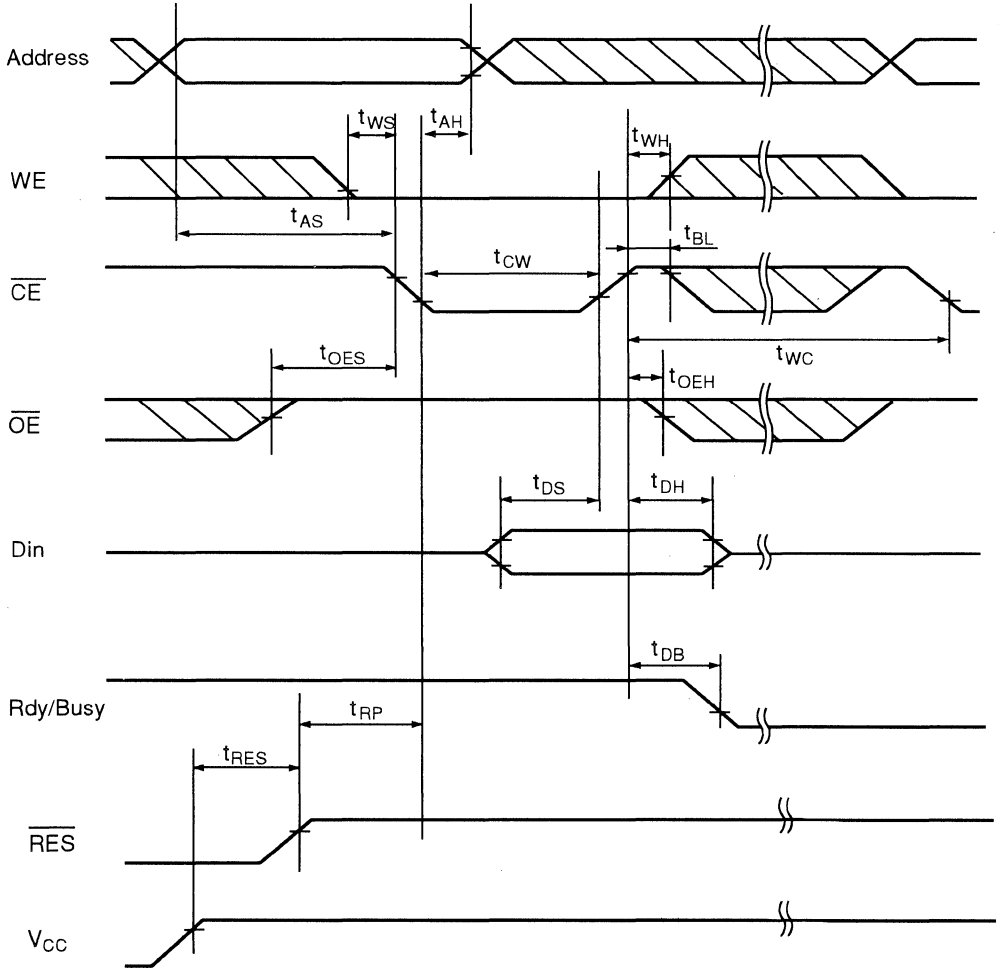
■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.BE1.HN58C1001)

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



(TD.BE2.HN58C1001)

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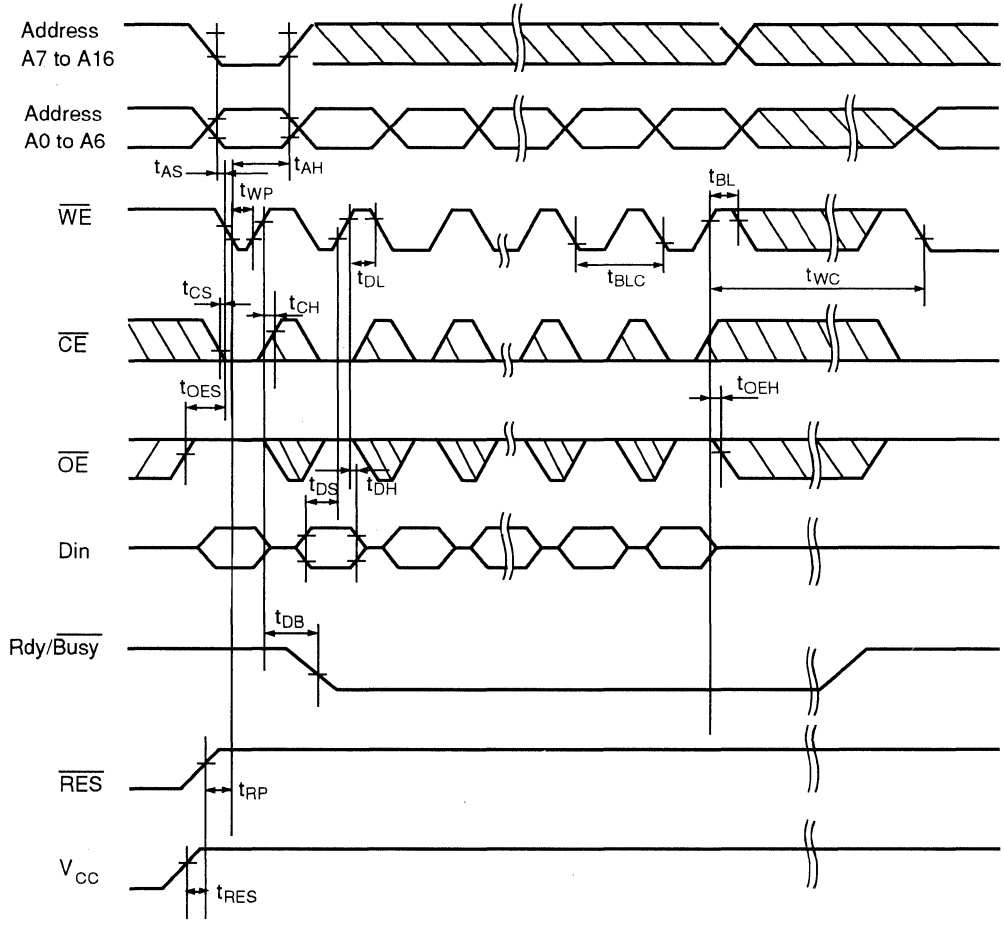
■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	250	-	-	ns	
	t_{CW}[3]	250	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	750	-	-	ns	
Write Cycle Time	t_{WC}	15	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	1	-	30	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Notes: 1. Use this device in longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.PE1.HN58C1001)

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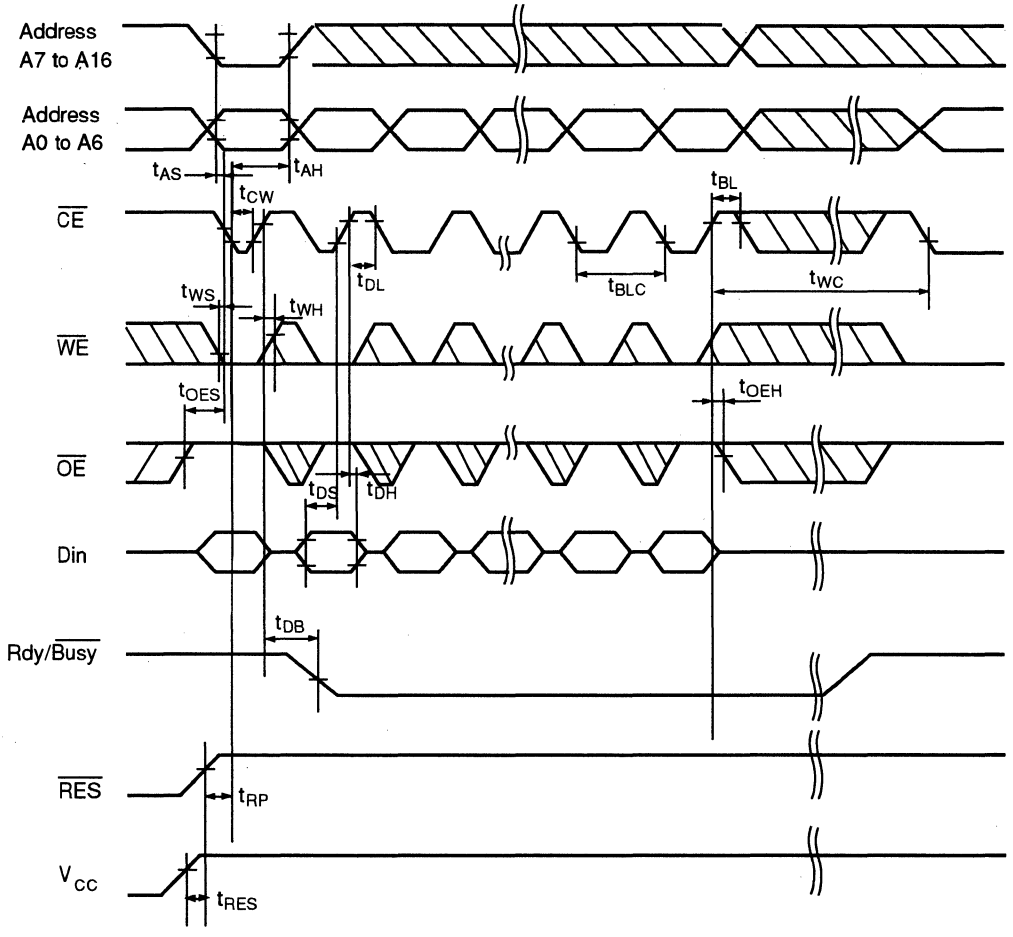
■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)

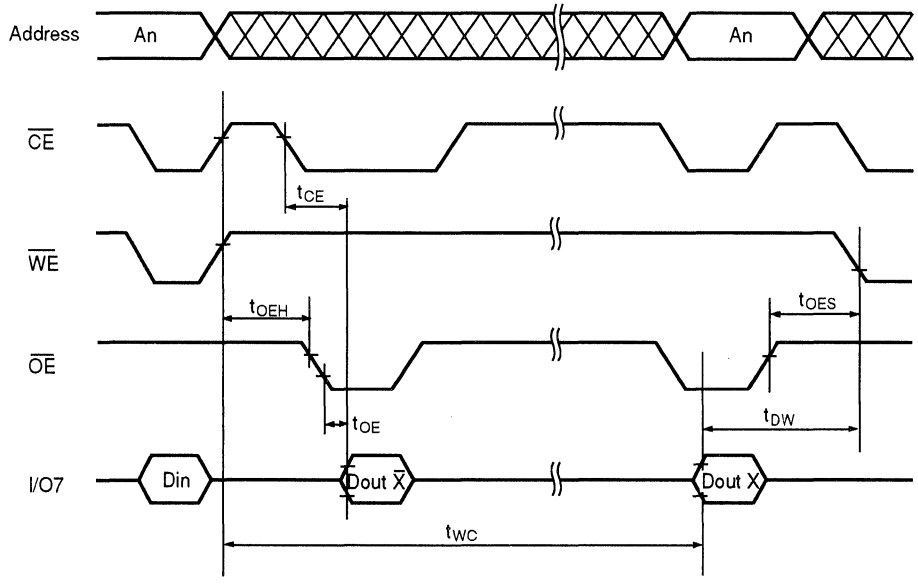


(TD.PE2.HN58C1001)

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{DATA}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	15	ms	

■ $\overline{DATA}$ POLLING TIMING WAVEFORM



(TD.DP.HN58C1001)

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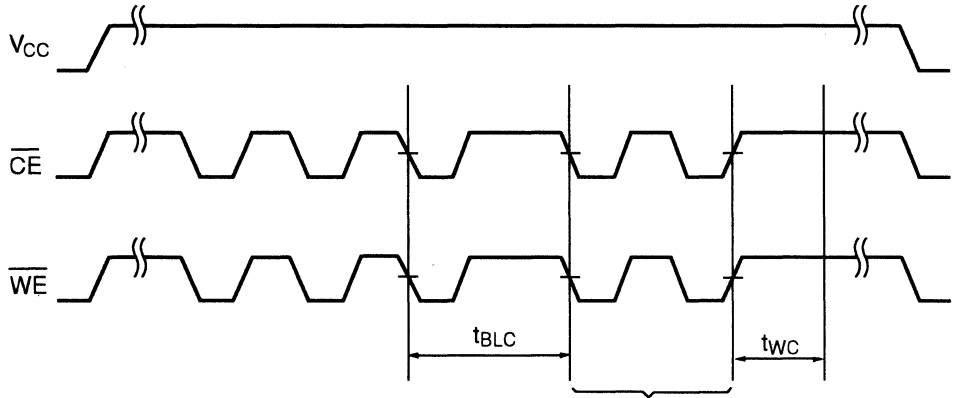
■ AC ELECTRICAL CHARACTERISTICS FOR SOFTWARE DATA PROTECTION CYCLE OPERATION

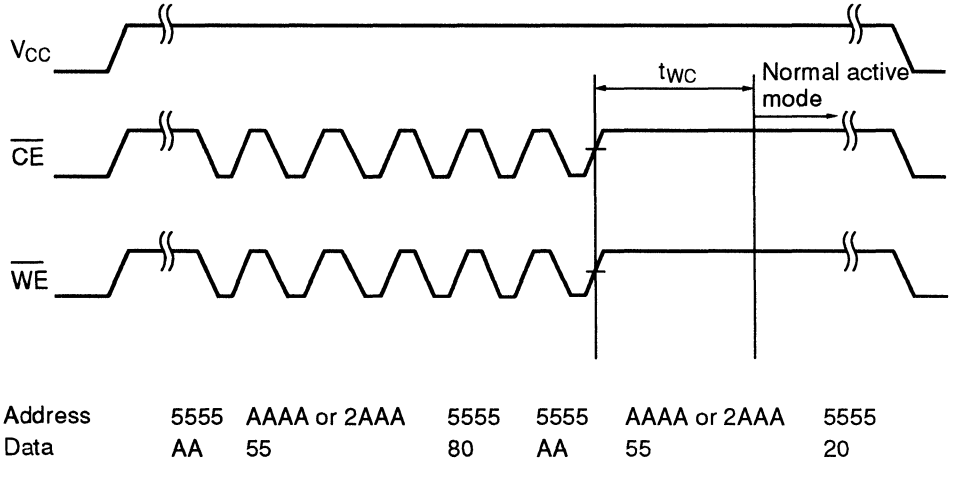
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Byte Load Cycle Time	t_{BLC}	1	-	30	µs	
Write Cycle Time	t_{WC}	15	-	-	ms	

■ SOFTWARE DATA PROTECTION TIMING WAVEFORM (Protection Mode)



(TD.SD1.HN58C1001)

■ SOFTWARE DATA PROTECTION TIMING WAVEFORM (Non-Protection Mode)



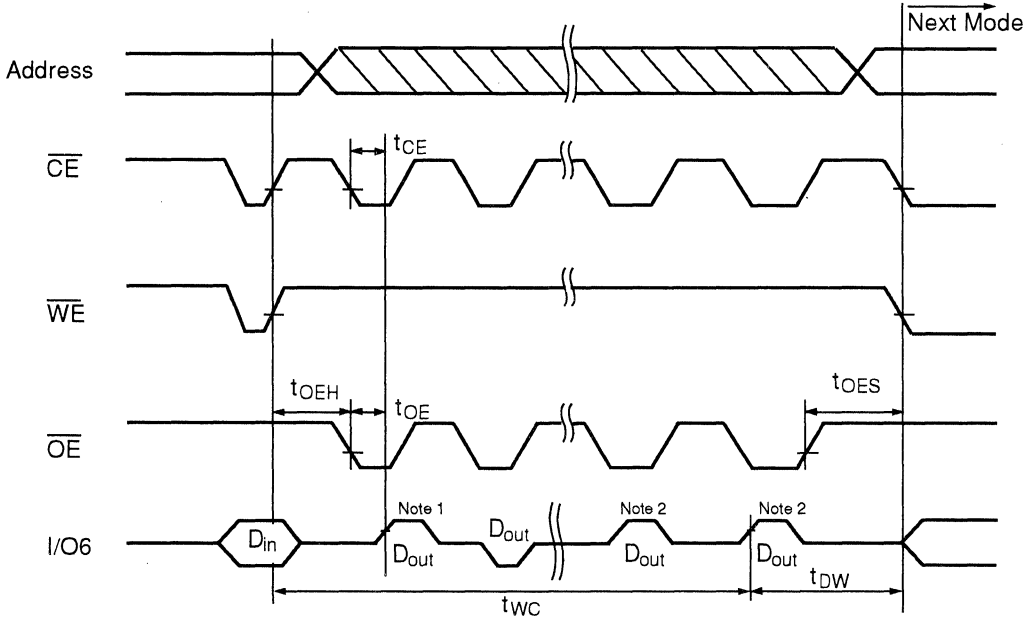
(TD.SD2.HN58C1001)

■ TOGGLE BIT

The HN58V1001 provides another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O_6 will change from "1" to "0" (toggle) for each read. When the internal programming cycle is over, toggling of I/O_6 will stop and the device can be accessible for the next read or program.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
$\overline{OE}$ to Write Setup Time	t_{OES}	0	-	-	ns	
$\overline{OE}$ Hold Time	t_{OEH}	0	-	-	ns	
Write Start Time	t_{DW}	250	-	-	ns	
Write Cycle Time	t_{WC}	-	-	15	ms	

■ TOGGLE BIT TIMING WAVEFORM



(TD.TB.HN58C1001)

Notes: 1. I/O beginning state is "1".
2. I/O ending state will vary.

5

■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 128 Bytes of data to be written into the EEPROM in a single cycle and allows the undefined data within 128 Bytes to be written corresponding to the undefined address (A_0 to A_6). Loading the first Byte of data, the data load window of 30 µs opens for the second. In the same manner each additional Byte of data can be loaded within 30 µs. In case $\overline{CE}$ and $\overline{WE}$ are kept high for 100 µs after data input, the EEPROM enters erase and write automatically and only the input data are written into the EEPROM. In Page mode the data can be written and accessed 10^5 times per page, and in Byte mode 10^4 times per Byte.

$\overline{\text{Data}}$ Polling

$\overline{\text{Data}}$ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

Write Protection

(1) Noise protection: Noise on a write cycle will not act as a trigger with a $\overline{WE}$ pulse of less than 20 ns.

(2) Write inhibit: Holding $\overline{OE}$ low, $\overline{WE}$ high, or $\overline{CE}$ high, inhibits a write cycle during power on/off.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

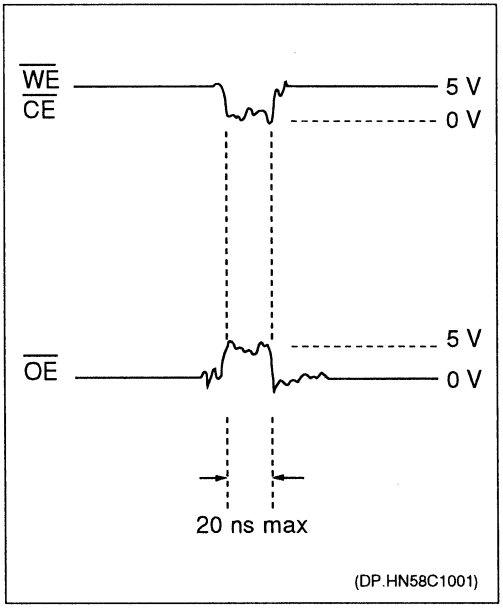
Write/Erase Endurance and Data Retention

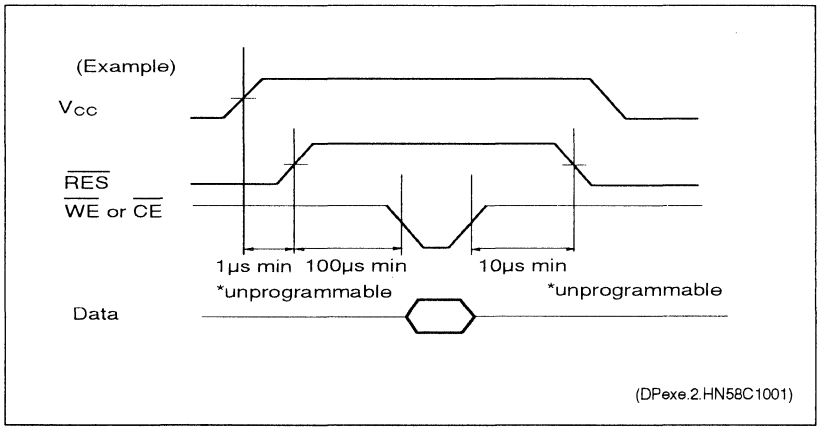
The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58V1001 has:

1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58V1001 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.





■ FUNCTIONAL DESCRIPTION (continued)

Data Protection (continued)

2. Data protection at V_{CC} on/off
   When $\overline{RES}$ is low, the EEPROM cannot be erased and programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during programming because it does not provide a latch function.
   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state by using a CPU reset signal to $\overline{RES}$ pin.
   The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the lost data input.

3. Software data protection
   To prevent unintentional programming caused by noise generated by external circuits, HN58V1001 has a Software data protection function. In Software data protection mode, 3 Bytes of data must be input before the Write data. These Bytes can switch the Non-Protection mode to the Protection mode.

Address	Data
5555	AA
⇓	⇓
AAAA or 2AAA	55
⇓	⇓
5555	A0
⇓	⇓
Write Address	**Write Data** (Normal Data Input)

   The Software data protection mode can be cancelled by inputting the following 6 Bytes. This changes the HN58V1001 turns to the Non-Protection mode and it can write data normally. When the data is input during the cancelling cycle, the data cannot be written.

Address	Data
5555	AA
⇓	⇓
AAAA or 2AAA	55
⇓	⇓
5555	80
⇓	⇓
5555	AA
⇓	⇓
AAAA or 2AAA	55
⇓	⇓
5555	20

5

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